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SEMICONDUCTOR WAFER BONDING

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ABSTRACT

When mirror-polished, flat, and clean wafers of almost any material are brought into contact at room temperature, they are locally attracted to each other by van der Waals forces and adhere or bond. This phenomenon is referred to as wafer bonding. The most prominent applications of wafer bonding are silicon-on-insulator (SOI) devices, silicon-based sensors and actuators, as well as optical devices. The basics of wafer-bonding technology are described, including microclean-room approaches, prevention of interface bubbles, bonding of III-V compounds, low-temperature bonding, ultra-high vacuum bonding, thinning methods such as smart-cut procedures, and twist wafer bonding for compliant substrates. Wafer bonding allows a new degree of freedom in design and fabrication of material combinations that previously would have been excluded because these material combinations cannot be realized by the conventional approach of epitaxial growth.

INTRODUCTION

Wafer bonding refers to the phenomenon wherein mirror-polished, flat, and clean wafers of almost any material, when brought into contact at room temperature, are locally attracted to each other by van der Waals forces and adhere or bond. Wafer bonding is alternatively also known as direct bonding, fusion bonding, or more colloquially as gluing without glue. In most cases, the wafers

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involved in actual applications are semiconductor wafers consisting of single-crystal materials such as silicon or gallium arsenide used in microelectronics or optoelectronics. The bonding at room temperature is usually relatively weak compared with that of covalently or ionically bonded solids. Therefore, for many applications, the room-temperature-bonded wafers have to undergo a heat treatment to strengthen the bonds across the interface. Frequently, one of the two wafers is then thinned down to a thickness that, depending on the specific application, may be in the range of many microns down to a couple of nanometers. Modifications of this generic process flow are quite common for specific applications; e.g. no heating step or no thinning step may be involved, or the heating and bonding steps may be combined.

At present, the most prominent applications of wafer bonding are in the areas of silicon-on-insulator (SOI) devices and silicon-based sensors and actuators. SOI structures consist of a thin, top layer of single-crystal silicon, a layer of silicon dioxide (SiO_2), and a silicon handle substrate that acts as mechanical support. In the fabrication of SOI substrates by wafer bonding, the silicon wafer forming the top layer has to be oxidized before bonding and thinned down to between 0.1 and 10 μm after bonding. SOI devices that are radiation hard are able to operate at high temperatures and have potentially higher packing density and a lower power consumption than devices on conventional silicon substrates. These features make such devices especially attractive for handheld and battery-operated electronic equipment.

In spite of the dominance of silicon-related applications, wafer-bonding technology is by no means restricted to silicon wafers. Proper polishing and control of the chemistry of the surfaces make it possible to bond a variety of solids independently of their structure (amorphous, polycrystalline, single-crystal), their crystallographic orientation and lattice parameter, or the thickness of the wafers. Wafer bonding, therefore, allows the fabrication of material combinations that previously were ruled out by most materials scientists, solid state physicists, and electrical engineers, because these material combinations were not possible by the conventional approach of epitaxial growth. Wafer bonding can also be used as a specific joining technique for many applications, especially in the area of microsystems technologies, but also in the areas of nonlinear optics and light-emitting diodes.

We begin with a short history of wafer bonding and then discuss silicon/silicon wafer bonding in some detail because it is the best-investigated and economically most important example of such bonding. We discuss bonding of dissimilar materials and nonsilicon materials, a promising thinning approach involving hydrogen implantation, and various methods used to perform wafer bonding with high bonding strength at temperatures as low as room temperature. Finally, we discuss the use of wafer bonding to fabricate compliant substrates.

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Because of the large number of papers published on wafer bonding over the last decade, we do not give an exhaustive list of references. We rather refer to the proceedings of a series of symposia devoted to wafer bonding (1–4), recent review articles (5–14), and a special 1995 issue of the *Philips Journal of Research* (15). The subject of SOI devices has been treated extensively elsewhere (16, 17) and is not specifically discussed in this review.

HISTORY OF WAFER BONDING

In 1734, Desaguliers reported that the friction of surfaces decreased with decreasing surface roughness up to the point where the surfaces were so well polished that they stuck together (for a reference, see 18). Desaguliers attributed this phenomenon to the adhesion of two solids in close contact. He had already demonstrated that two pieces of lead when pressed together remained stuck together. It took about the same force per area to separate the two spheres as if they had been a single body. This was probably the first reported case of "cold welding" in which at least one of the two partners had been sufficiently plastically deformed that the close contact of atoms of the two bodies resulted in strong (in this case metallic) bonding. Generally, this can be done only with plastically deformable materials. For brittle materials such as glass, it was observed around 1900 in the newly developing optical industry that glass pieces polished to optical quality tended to stick to each other. The same observation was also made for optically polished so-called end pieces of metal used as reference length scales for precision measurements. The adherence of optically flat pieces of glass and fused quartz was considered mostly a nuisance rather than an advantage. In these cases, the pieces adhering to each other were usually bulk pieces (like prisms) and nowhere as thin as typical wafers now used for wafer bonding. Optical quality does not mean only shiny, mirror-polished surfaces but also deviations from a defined plane of less than a quarter of an optical wavelength, or less than about 100 nm, over the whole piece. This is different from the case of typical wafers in which a bow of many micrometers can be encountered that does not prevent bonding because this bow can be accommodated elastically.

The first systematic investigation of room-temperature adherence of silica (fused quartz) was reported by Lord Rayleigh in 1936 (19); however, his pioneering paper did not induce any further technological developments. The interaction of surfaces was later investigated in detail by Tabor and co-workers with the so-called surface force apparatus, as discussed in detail in a book by Israelachvili (20). The interaction energies of two curved surfaces were measured and attributed to van der Waals forces either between the contacting solids themselves or between monolayers of molecules with high dipole

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moments such as water layers (20). However, this knowledge was not applied to room-temperature wafer bonding for many years.

Anodic bonding of silicon to appropriate sodium-containing glasses of a similar thermal expansion coefficient, which requires the application of high voltages at temperatures around 500°C, was introduced by Wallis & Pommerantz in 1969 (21). Because of space restrictions, we direct the reader to Reference 22 and do not discuss it further. High-temperature bonding of GaAs to an appropriate glass was first reported by Antypas & Edgecumb in 1975 (23) and, although not described in detail here, appears to be similar to present-day III-V compound bonding (see below). III-V compound bonding has enabled the fabrication of a variety of optoelectronic devices and the production of highly efficient light-emitting diodes (LEDs).

Room-temperature bonding of silicon wafers, followed by a high-temperature treatment, was suggested in 1985 by Lasky et al (24, 25) from IBM and by Shimbo et al (26, 27) from Toshiba. The present-day wafer-bonding technology was triggered by these reports. In terms of applications to silicon sensors, in 1985 Petersen and co-workers (28) were the first to suggest the use of wafer bonding as an extension of the well-established anodic bonding (22). From then on, silicon wafer bonding and the associated thinning techniques were further investigated and improved for the fabrication of SOI wafers, as a supposedly less expensive and better quality alternative to the SIMOX (Separation by IMplantation of OXygen) approach, which involves high-dose and high-energy oxygen implantation (16, 17). Simultaneously, the use of wafer bonding for the fabrication of silicon-based sensors and actuators became more widespread. Because wafer bonding of III-V compounds requires a different bonding approach (high-temperature bonding and a hydrogen-containing atmosphere), it developed almost independently of silicon-based wafer bonding.

SILICON WAFER BONDING

Overview

Silicon wafer bonding typically involves the following steps, which are discussed in more detail below.

1. The surfaces of two mirror-polished silicon wafers, which may contain structures such as cavities, are conditioned and prepared for the bonding process. The wafers may be thermally oxidized or just contain a native oxide that is made hydrophilic by proper surface treatment. The wafer surfaces are then typically covered by one or two monolayers of water. The surface oxide may also be removed by a dip in hydrofluoric acid, which leads to a hydrophobic hydrogen coverage of the silicon surfaces.

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2. The two mirror-polished wafer surfaces are brought into contact for bonding at room temperature in air in a sufficiently clean environment in order to avoid particles between the wafers.

3. Directly after room-temperature bonding, the adhesion between the two wafers is determined by van der Waals interactions or hydrogen bridge bonds, which are one or two orders of magnitude weaker than typical covalent bonds. A higher bond energy, required for most practical applications, may be obtained by an appropriate heating step, which for commercial SOI production is frequently performed at temperatures as high as 1100°C. Treatments at intermediate temperatures are also possible.

4. For many (but not all) applications, one of the bonded silicon wafers has to be thinned down to a thickness between about 100 nm to some micrometers, depending on the specific application.

Surface Requirements

Whether two wafers bond depends on the bonding energy at room temperature and the roughness and waviness of the two wafers. The bonding energy is characterized by the energy associated with opening the surface by the so-called crack-opening method, first described by Maszara et al (29) and based on earlier work by Metsik (30). The surface energy per area γ may be determined from the relation

$$\gamma = (3\,\mathrm{E}\,d^3 y^2)/(32\,L^4), \qquad 1.$$

where E is Young's modulus, L the crack length, y the thickness of the blade used to open the crack, and d the thickness of each of the two wafers, as shown in Figure 1. For the case of wafers of different thickness and/or elastic

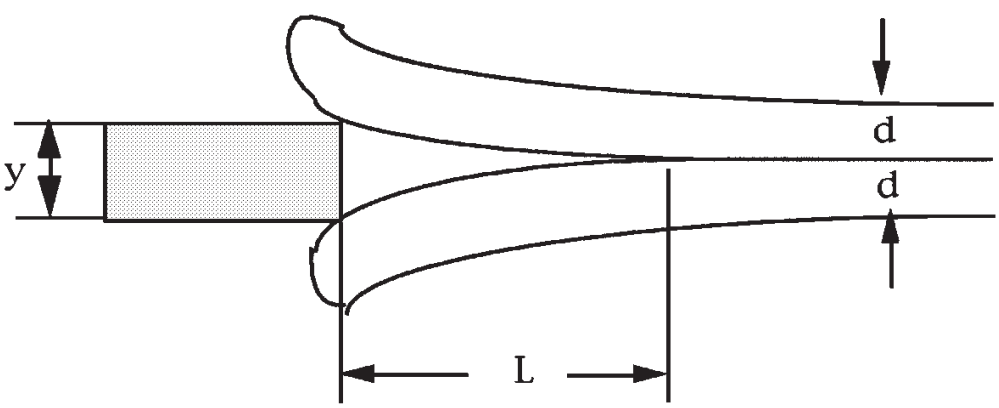

Figure 1 Schematic of crack-opening method that determines the surface energy.

properties, a formula for an averaged γ of the two surface energies is also available (31).

The surface energy depends on the chemical state of the surfaces and is typically around 0.1 J/m^2 for hydrogen bridge–bonded hydrophilic silicon surfaces (which are covered by a thin oxide and one or two monolayers of water) and around 0.02 J/m^2 for (hydrogen covered) hydrophobic silicon surfaces, generated by a hydrofluoric acid wash that removes the thermal oxide (32, 33). The apparent surface energy measured depends on the humidity of the ambient in which the measurement is performed and also on the time elapsed after insertion of the blade (34). Therefore, the use of published values of γ, for which the exact measurement conditions are not given, may lead to erroneous conclusions.

The bondability of wafers depends on the waviness of the surface. Let R characterize half of the wavelength and h half of the gap height. The gap can be closed if the bonding energy gained by closing the interface gap is larger than the elastic energy required to deform the two wafers. There are two regimes of interest (11). If the relation between the thickness d of the wafers and the radius is given by $R > 2d$ (thin wafer), the relevant criterion for gap closing is

$$h^{1/2}/R < [\gamma/(1.2\,\mathrm{E}\,d^3)]^{1/4}, \qquad 2.$$

whereas for $R < 2d$ (thick wafer), the criterion is

$$h^2/R < 6.7\gamma/\mathrm{E}. \qquad 3.$$

Based on these criteria, it is now possible to predict approximately what kind of roughness, surface flatness, and bow can be tolerated for wafer bonding. Generally, prime grade commercial silicon wafers can be bonded easily, even in the more critical case of hydrophobic surfaces (32, 33). The developed theoretical expressions show that even infinitely thick pieces can be bonded, provided the surface flatness is sufficiently good (35), as has long been known to occur for optically polished bulk pieces of glasses or metals. In reality, the roughness and the bow of wafer surfaces cannot be described by just one wavelength and an associated amplitude; rather the whole Fourier spectrum of surface variations must be considered. Some attempts have been made to include information on this spectrum in criteria on the bondability of wafers (36, 37).

Often in micromechanics, structured wafers, e.g. containing cavities, have to be bonded. In this case, the bondable area may be only a small fraction of the total wafer area. In a first approximation, Equation 1 then has to be scaled linearly with the actual area available for bonding, provided the crack length L is much larger than the feature size of the unbondable area (S Mack, unpublished observations).

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Room-Temperature Bonding Step

Inclusion of particles or obstacles on the wafers themselves, the result of insufficient polishing, leads to unbonded areas between the wafers that are generally referred to as interface bubbles or simply bubbles or voids. Even a particle with a diameter of about 1 μm causes a bubble with a lateral diameter of several mm. The existence of such bubbles can be shown by standard non-destructive detection methods such as infrared transmission, ultrasonic microscopy, X-ray topography, or the so-called magic mirror method, which optically detects small surface deflections of the bonded wafers caused by interface bubbles. Destructive methods of analysis such as interface etching and transmission electron microscopy (TEM) may also be applied for smaller feature sizes. Interface bubbles caused by particles can be avoided by proper cleaning and the use of a sufficiently high-quality cleanroom (class 10 or better) or by other specifically designed equipment for wafer bonding. An example is the simple microcleanroom developed at Duke University (38). A microcleanroom allows for fabrication of particle-free wafer bonding, as schematically shown in Figure 2. The microcleanroom is basically a spinner in which the two wafers are placed with the mirror-polished surfaces facing each other, separated by removable spacers. First the space between the wafers is thoroughly flushed with filtered deionized water. Then, after a transparent lid is put over the wafers, they are spin dried at about 3000 rpm under the influence of an infrared lamp. The spacers between the wafers are then removed without opening the lid. The upper wafer then falls on the lower wafer, but is still separated by an air cushion of a couple of micrometers. After opening the lid, the bonding process can be initiated by slightly pressing the wafers together locally with a special tong, which avoids large-scale elastic deformation of the wafer pair. The bonded area then spreads over the whole wafer in a couple of seconds. An example of this bonding process for two hydrophilic 4-inch silicon wafers, as observed by an infrared camera, is shown in Figure 3. The lateral bonding speed of a couple of cm/s (39, 40) is determined by the process of pressing the air out between the two wafers and, consequently, an increase of the lateral bonding speed is observed with decreasing pressure of the ambient in which the bonding is performed.

The room-temperature bonding step may be performed either in air under normal pressure or under vacuum, as dictated by the requirement of evacuated cavities for various micromechanical sensors. Bonding even under reduced pressure (low vacuum) is helpful in bonding wafers with higher surface roughness (HT Lee, unpublished results). Bonding in different atmospheres, such as oxygen or nitrogen, is also possible.

In micromechanics, bonding of not only structured wafers but also of whole stacks of differently structured wafers for complex structures is required. In this

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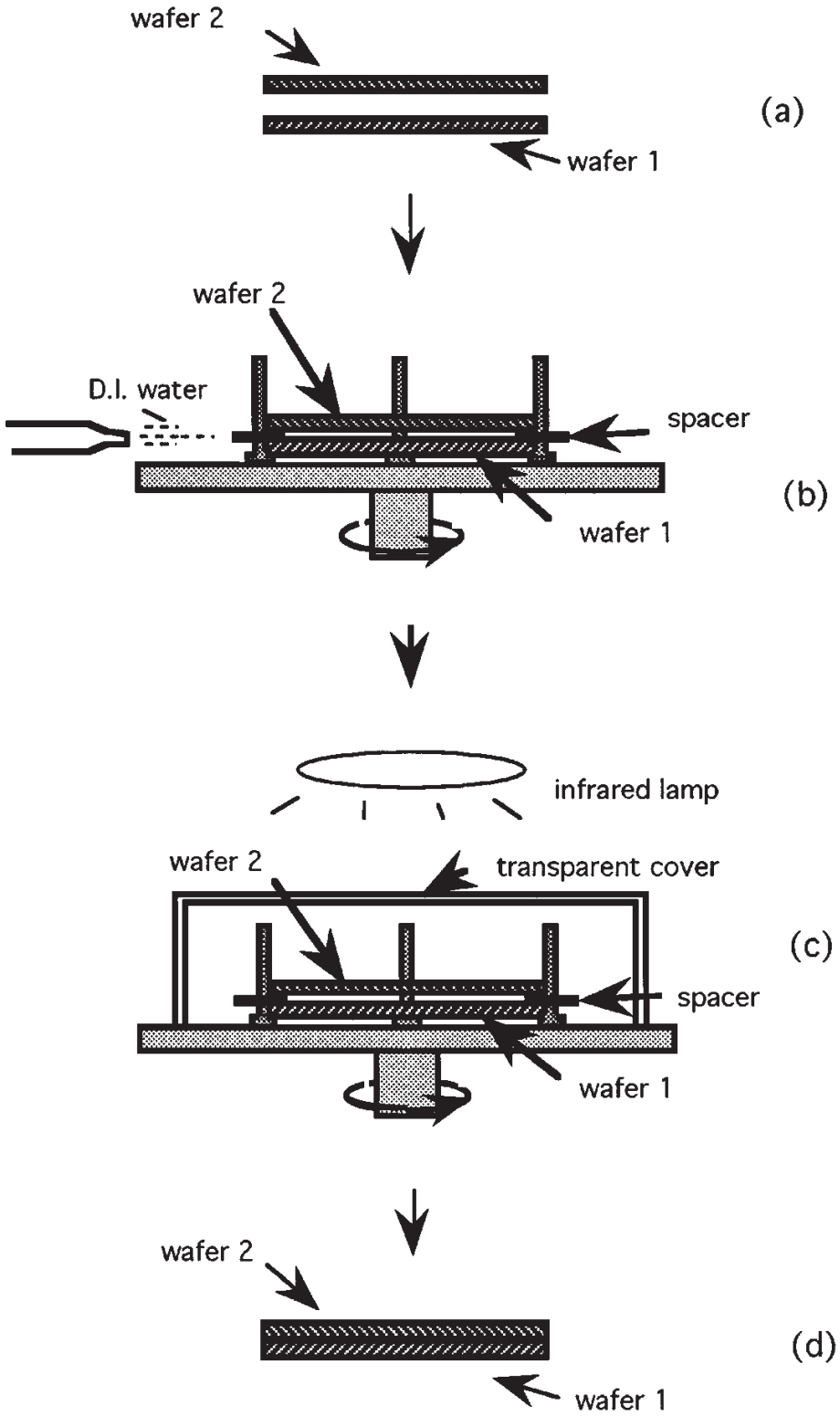

Figure 2 Schematic illustration of a wafer-bonding process using a microcleanroom setup.

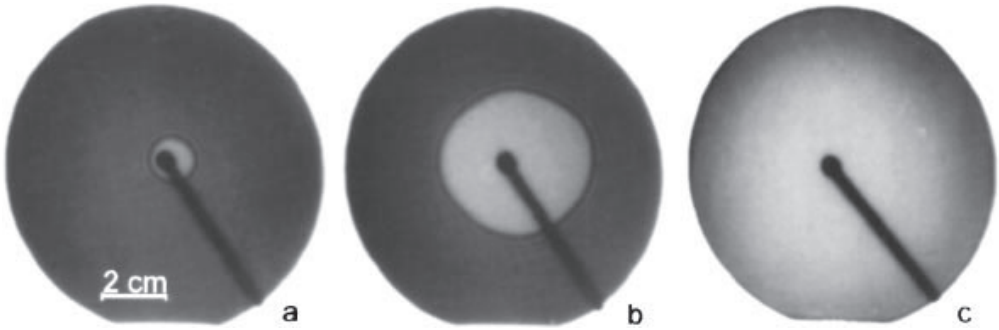

Figure 3 Infrared photograph of initiation and propagation of a bonding wave in wafer bonding of 4-inch silicon wafers. (*a*) Local starting of the contact wave, (*b*) extension after about 2 s, and (*c*) complete bonding after about 5 s. The radial dark line comes from the tong used to intiate the bonding (14).

area, aligned bonding becomes increasingly important. Commercial equipment is now available for aligned wafer bonding.

Heating Step and Reaction Mechanisms

Bonding after exposure to room temperature only is reversible. The two wafers can be easily separated by inserting a wedge at the rim of the wafers. Reversible wafer bonding has been suggested for the protection of semiconductor surfaces from particles or organic contamination (41), but for almost all other applications, a higher bonding or surface energy is required. This is usually accomplished by heating the bonded wafers at elevated temperatures. Typical curves of the surface energy as a function of temperature are shown in Figure 4 for bonded silicon wafers with hydrophilic or hydrophobic surfaces, as measured by the crack-opening method discussed above (33). In the case of hydrophilic surfaces, both silicon wafers were covered with an $\approx$1–2 nm thick layer of native oxide. High-resolution cross-sectional transmission electron micrographs of hydrophilic and hydrophobic silicon wafers after heating to 1100°C demonstrated the presence of a thin oxide layer in the case of hydrophilic bonding and of no interfacial layer in the case of hydrophobic bonding (14).

Several models have been suggested to describe the reactions occurring at the interface during the heating step in silicon wafer bonding (6, 42, 43). The reactions at the bonding interface involving water, OH, and SiH groups can be seen by multiple internal reflection spectroscopy, as clearly demonstrated by Chabal's group at Bell Laboratories (44). The picture that emerges can be described in a simplified form as follows.

For hydrophilic wafers, the initial bonding is via hydrogen-bridge bonds between water molecules. During heating, water molecules have to be removed.

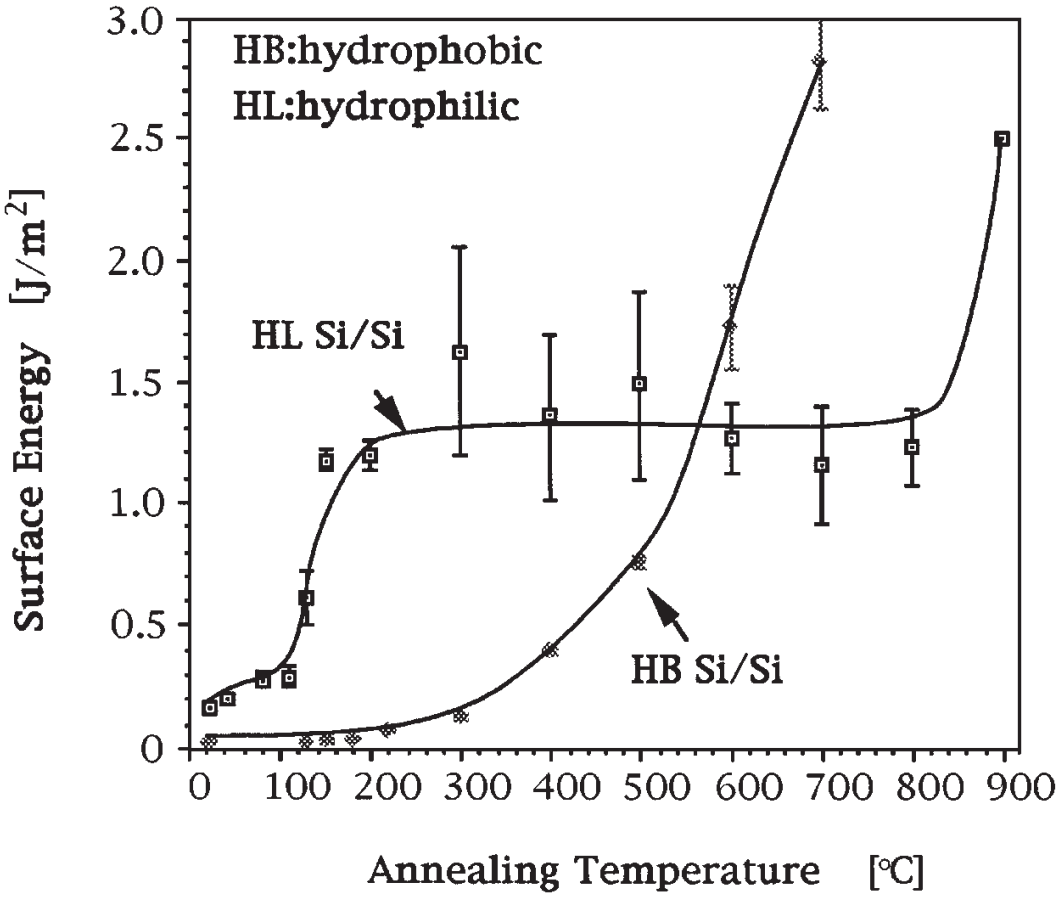

Figure 4 Surface energy of bonded hydrophilic or hydrophobic silicon wafers as a function of annealing temperature (33).

Some of these water molecules are present at the start of the process and some are generated by reaction of silanol bonds across the interface according to

$$\text{Si-OH} + \text{HO-Si} \rightarrow \text{Si-O-Si} + H_2O. \qquad 4.$$

This reaction may occur at temperatures as low as about 100°C. A small part of the removal of water molecules may occur by lateral diffusion along the bonding interface to the rim of the wafers, but most water molecules diffuse through the oxide and oxidize the silicon according to

$$2H_2O + \text{Si} \rightarrow SiO_2 + 2H_2. \qquad 5.$$

This reaction ends at a few hundred degrees, which leads to the plateau shown in Figure 4. The remaining increase of the surface energy is associated with micro-gaps at the interface in which nitrogen may possibly remain trapped and may be eliminated by viscous flow of the oxide at high temperatures. Alternatively, bonding in vacuum, which prevents the trapping of inert gas, and long annealing (e.g. 100 h) at temperatures as low as 150°C may also lead to

the full surface energy (Q-Y Tong & HT Lee, unpublished observations) and a bonding equivalent to that achieved after conventional annealing at 1100°C.

In the case of bonding of hydrophobic surfaces covered by hydrogen, the reaction at the interface is simply the release of the hydrogen and bonding of the silicon across the interface according to

$$\text{Si-H} + \text{H-Si} \rightarrow \text{Si-Si} + H_2. \qquad 6.$$

In both cases, the hydrogen that is generated does not easily diffuse into the silicon at temperatures below about 800°C. Whether hydrogen is actually generated and what happens to it were investigated by Mack et al (45, 46) by bonding hydrophilic or hydrophobic silicon wafers containing cavities of the same size, but different areal densities, to unstructured silicon wafers, as indicated in Figure 5. The membrane of the cavities allowed the measurement of the pressure increase in the cavities with time. As expected for gas generated at the interface and diffusing along it, the pressure increases with decreasing area density of cavities, corresponding to a larger available interface area per cavity, as shown in Figure 6. By mass spectrometry, the main constituent in the cavities was shown to be molecular hydrogen for both hydrophilic and hydrophobic wafers.

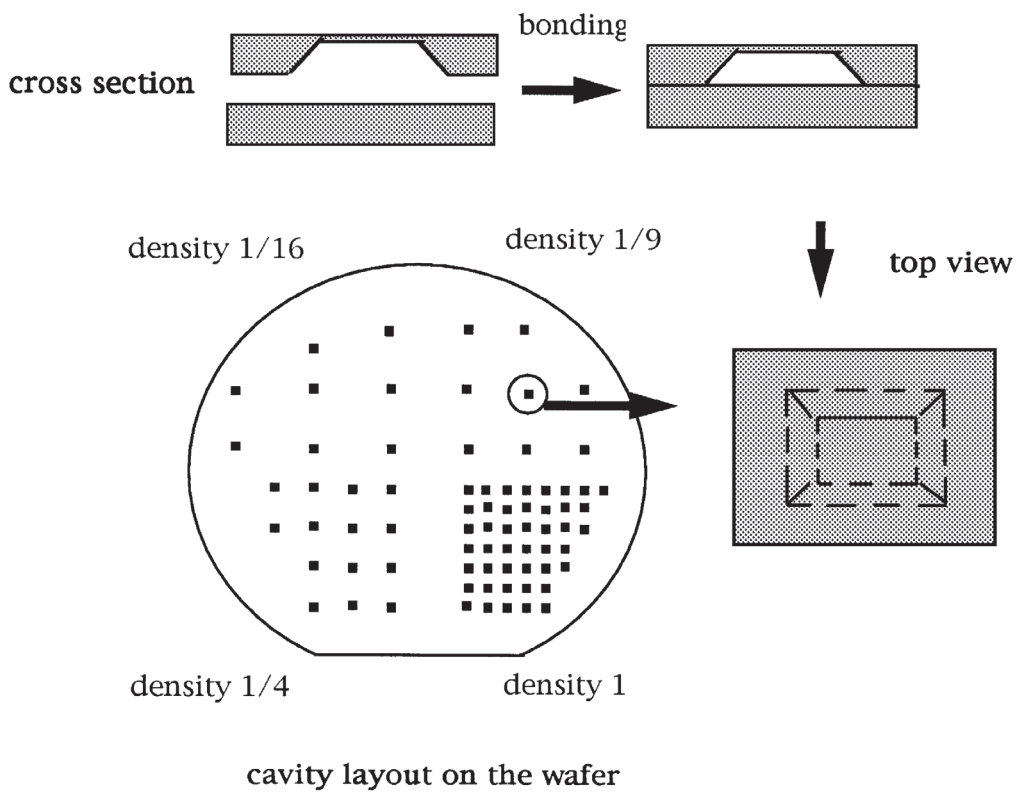

Figure 5 Schematic top view and cross section of test structure cavity (*top*) and cavity layout on the wafer (*bottom*) (45).

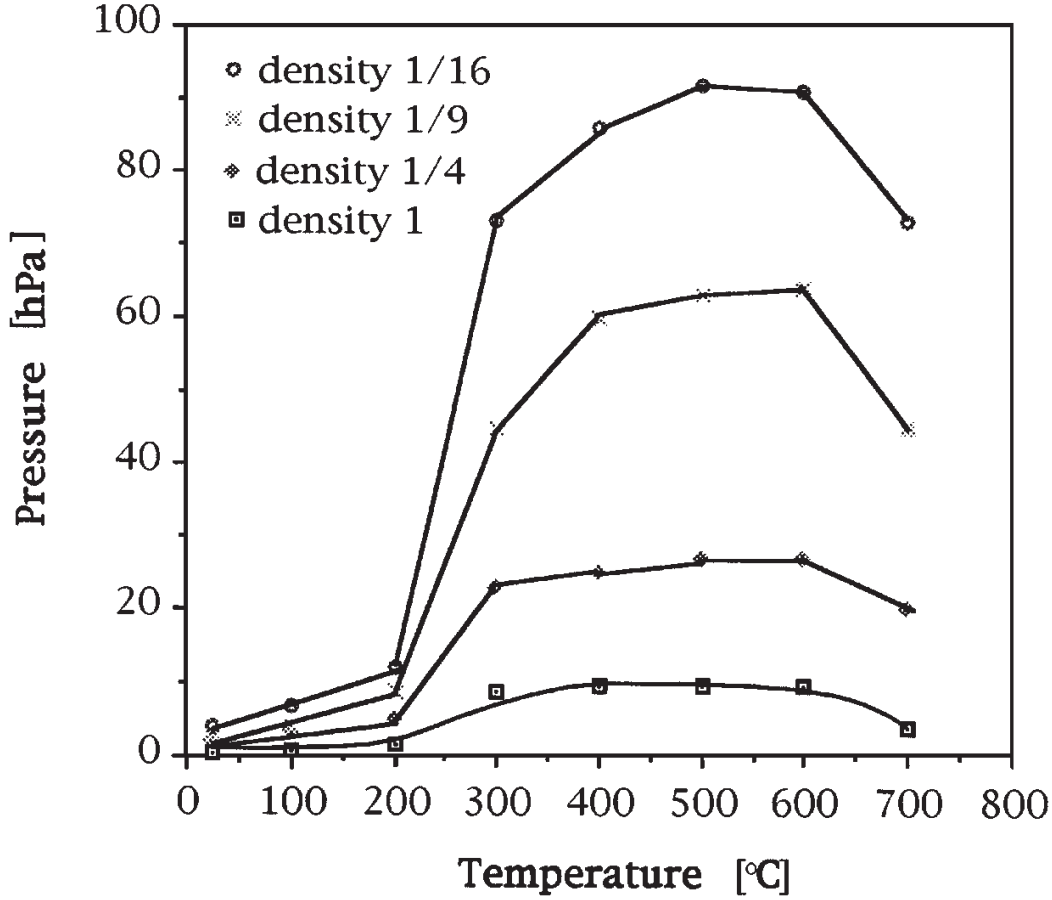

Figure 6 Gas pressure inside cavities after 70 h annealing at specified temperatures for hydrophobic bonding conditions (45).

The generated hydrogen gas can diffuse along the interface even at room temperature. A typical diffusion coefficient is in the order of 10^{-6} cm^2/s.

The presence of hydrogen at the bonding interface is not only undesirable for certain applications such as absolute-pressure sensors in which the sensor cavities should contain a high vacuum, but also for the bonding of unstructured wafers. The associated gas pressure may lead to the generation of gas bubbles at the interface, even for wafers that do not show particle-related bubbles after room-temperature bonding (47, 48). These interface bubbles, with typical lateral extensions of hundreds of micrometers up to centimeters, disappear during high-temperature treatment above 800°C due to the diffusion of hydrogen into the surrounding silicon. Because hydrogen easily dissolves in thermal oxide layers or fused quartz, the hydrogen pressure decreases with increasing thickness of a thermal oxide layer between the two silicon wafers. Therefore, the tendency to form interface bubbles is lower for SOI wafers (with an oxide layer thickness of typically around 0.5–1 μm) as compared with bonding of silicon wafers covered only with native oxide (48).

Hydrophilic bonding of one silicon wafer covered with a native oxide to another wafer covered with a much thicker thermal oxide leads to the best mechanical properties, as compared with other possible bonding combinations (native oxide/native oxide or thermal oxide/thermal oxide), especially after intermediate temperature steps (49). The reason for this is simply that the thin oxide allows the reaction (Equation 5) to occur most easily, which gets rid of the interfacial water. The thicker thermal oxide prevents the formation of microbubbles at the interface (by accommodating the resulting hydrogen gas), which later might act as starting points of mechanical failure in tensile tests of the bonded samples.

A detailed investigation of bubble formation during heating steps (48) showed that the presence of hydrogen gas at the interface is not sufficient to form interface bubbles, even in the unfavorable case of bonding via two thin native oxides, which is especially susceptible to the formation of interface bubbles. It appears that bubble nucleation requires either fairly rough surfaces or, in the case of standard silicon wafers, the presence of thermally unstable hydrocarbon contaminants on the surfaces coming from plastic containers or simply from the ambient in a cleanroom. Therefore, hydrogen-related interface bubbles may be prevented from nucleating if these hydrocarbons have been desorbed before bonding by an annealing step at 600°C in oxygen or at 800°C in argon (48). Alternatively, and much more conveniently, interface bubbles may be avoided by conventional chemical cleaning followed by a treatment in diluted periodic acid (50). As mentioned above, bubble nucleation may also be prevented if the hydrogen and/or hydrocarbon molecules diffuse along the interface to cavities or other pressure-release structures. Procedures that allow attainment of a high-surface energy at relatively modest elevated temperatures or even at room temperature are discussed below.

Thinning Procedures

In many cases, and especially for SOI materials, one of the wafers has to be thinned to create a thin single-crystal silicon layer on top of a thermal oxide layer. Various thinning approaches have been developed and are in use in commercial SOI production.

1. Precision polishing allows the fabrication of layers down to about 1 μm, with a thickness uniformity of about 0.3 μm over the whole wafer, which is sufficient for most bipolar applications (51).

2. These SOI layers may be used as the starting material for a local plasma thinning procedure, which allows wafers to reach a thickness uniformity of about 10 nm (52).

3. The use of p^{++}-boron-doped silicon epi-layers, with stress compensated by the incorporation of germanium as an etch-stop layer, leads to good thickness uniformity in the 10 nm range (53).

4. An etch-stop based on a porous silicon sacrificial layer with similarly good thickness uniformity has been developed (54).

5. An elegant procedure is the so-called smart-cut method (55, 56). It is based on hydrogen implantation before bonding. Heating after wafer bonding leads to splitting of the hydrogen-implanted silicon wafer along hydrogen-filled microcracks induced by the precipitation of the implanted hydrogen (55–58). The great advantage of this procedure, which also allows a thickness uniformity in the 10 nm range, is that the split wafer may be reused after some soft polishing (which is also required for the transferred layer) because its thickness has changed by only about a micrometer or less. This approach, which is actually not a thinning of the wafer, but rather a layer transfer method from one wafer to another, is especially interesting for the layer transfer of expensive materials and is described in more detail in a section devoted to this method.

BEYOND SILICON/SILICON WAFER BONDING

General Remarks

Most materials, if properly polished and their surfaces properly chemically conditioned, do adhere to each other at room temperature and can thus be used for wafer-bonding matter, as has been shown by Haisma et al (5, 12, 15). The materials are not limited to semiconductors and can be present in single-crystal, polycrystalline, or amorphous form. Materials that are too rough or difficult to polish may be covered by process-compatible intermediate layers such as spun-on or chemical vapor-deposited silicon dioxide or silicon nitride, which may be easily polished and bonded. Wafer bonding may be performed via various intermediate layers such as oxides, nitrides, metals, and silicides. Especially important is bonding via polished polysilicon layers, not only for advanced dielectrically isolated (DI) wafers (59), but also for the fabrication of complex three-dimensionally integrated devices. In this context we stress the importance of chemo-mechanical polishing (CMP), which at present is widely available in microelectronics facilities and, therefore, facilitates the inclusion of wafer-bonding processes in device manufacturing.

Whereas a variety of materials have been shown to bond at room temperature (5, 12, 15), not much information is available on the behavior of the

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corresponding bonding interfaces following heating to strengthen the relatively weak van der Waals adhesion. The heating step causes chemical reactions that depend on the surface coverage and the specific materials bonded. No general rule can be given about which reaction will actually occur. In addition, if dissimilar materials such as silicon and fused quartz are bonded to each other, the bonding will depend on the difference in their thermal expansion coefficients and whether thermally induced mechanical stresses will allow heating to a sufficiently high temperature for bond strengthening without debonding, wafer sliding, or even fracture. Fortunately, some materials have thermal expansion coefficients sufficiently close to avoid this problem; for example, silicon and specifically developed glasses with similar expansion coefficients, silicon and silicon carbide, as well as gallium arsenide and sapphire. GaAs bonded on sapphire (60) may become important for combining GaAs-based electronics with superconducting microwave devices based on thin films of high-temperature superconductors epitaxially grown on sapphire. Even if there exists a large difference in the thermal expansion coefficients, heating will not cause much of a problem after one of the wafers has been thinned down to a thin layer, provided the thickness of the layer is below its critical thickness for the formation of thermally induced misfit dislocations (31). Therefore, the problem may be reduced to developing procedures that prevent large temperature differences before the thinning has been performed. One possibility consists of a series of consecutive heating and thinning steps that allow treatment at increasingly higher temperature with decreasing wafer thickness. Examples of successful room-temperature wafer bonding of dissimilar materials and subsequent heating and thinning include silicon on sapphire (SOS) for improved quality of the single-crystal silicon layer, as compared with epitaxially grown silicon (61); crystalline quartz on silicon for high-frequency applications (62); silicon on fused quartz or glass for HDTV projection masks (63, 64); and SiC on silicon or on a high-temperature glass (65, 66). Low-temperature bonding approaches as discussed below are especially important for bonding of dissimilar materials.

Recently, bonding of thin films of polycrystalline ferroelectrics on silicon fabricated by a sol-gel process to another silicon wafer has been accomplished, similar to that already done for bulk crystals (67, 68). Through the bonding process, the usual development of a reaction zone at the interface of ferroelectrics and silicon was avoided. In principle, this approach should allow reconsideration of the fabrication of silicon/ferroelectric FET-type devices. Bonding of wafers of the same material has also been realized for the following technological and widely varying oxides: lithium niobate (69), sapphire (70), lanthanum aluminate (71), and single-crystal quartz (72).

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III-V Compounds

In the specific case of wafer bonding involving III-V compounds, bonding of hydrophilic wafers is possible at room temperature, as has been shown for GaAs/Si and InP/Si (73) or GaAs/GaAs wafer bonding (K Gutjahr, unpublished results). However, heating to higher temperatures generally causes reaction of the water with the III-V compounds. This reaction leads to gaseous reaction products, potentially resulting in large interface bubbles. For this reason, III-V compound bonding has been performed mostly at higher temperatures (500–700°C) in a reducing atmosphere containing hydrogen and by the application of a mechanical compressive force, as described by Liau & Mull (74) and in modification by others (75–91). In most cases, the bonded area is relatively small (on the order of 1 cm^2). For combined opto- and microelectronics (74, 76, 89, 90), GaAs and InP on silicon have been bonded in such procedures. A stack of GaAs wafers with differing crystallographic orientations has been combined by this type of bonding to fabricate devices for optical second harmonic generation (78). GaN has been bonded to InP for better cleavage (88). Bonding of combinations of different III-V compounds (75, 81, 84, 86, 91) has also been reported, which is of particular interest for the fabrication of vertical cavity surface emitting lasers (VCSELs) (77, 86, 90) and light-emitting diodes (LEDs) (80, 85) (pioneered by Hewlett-Packard). In these LEDs, a GaAs substrate, which absorbs part of the emitted light but is required for epitaxial layer growth, is later replaced via a wafer-bonding approach by a III-V compound substrate (GaP) that has a different lattice constant but a higher bandgap and thus does not absorb emitted light. These LEDs, with highly improved efficiency, are now available commercially (85). Very recently, the size of the III-V compound substrates has been extended to a full 2 inches (83) and the process can be considered as wafer bonding. First experiments at MPI Halle indicate that full 4-inch GaAs wafers may be successfully bonded at elevated temperatures in a reducing atmosphere, even without the application of an outside mechanical force (P Kopperschmidt, unpublished results).

An alternative method, pioneered by Yablonovitch et al (92), of transferring thin layers of GaAs-based materials to a substrate such as silicon is epitaxial lift-off. In this technique, the GaAs-based layer to be transferred, which may contain processed devices, is epitaxially grown on a thin AlAs etch-stop layer, which in turn has been epitaxially grown on a GaAs substrate. The whole structure is attached to a wax-type transfer substrate and then the AlAs layer is etched away laterally with hydrofluoric acid. Afterwards, the GaAs layer to be transferred is attached to the new substrate by hydrophilic bonding at room temperature, and the transfer substrate is removed by an appropriate solvent. Due to the relatively slow lateral etch rate of about 100 μm/h, epitaxial lift-off

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is limited to the transfer of layers with lateral dimensions of less than several centimeters.

HYDROGEN IMPLANTATION–INDUCED LAYER TRANSFER

Hydrogen implantation into silicon wafers, with a typical dose of $3–10 \times 10^{16}\,cm^{-2}$ and typical implantation energies in the range of 60 to 180 keV, may be used to transfer silicon layers after wafer bonding and heating via microcrack formation and layer splitting along those microcracks. This smart-cut process developed by Bruel (55, 56) is schematically shown in Figure 7. Heating of a single unbonded wafer leads to the development of surface blistering, which allows convenient surface inspection of the microcrack phenomena by optical microscopy. It appears that the time to generate optically detectable surface blisters strongly depends on temperature, as can be seen in Figure 8 (57). The time to develop sufficiently large cracks for whole-layer splitting is about ten times longer in this example. The time to form surface blisters is longer for highly *n*-doped silicon and shorter for highly *p*-doped layers (64). Below a certain threshold dose, which depends on doping and implantation energy, no splitting is possible (93). A detailed understanding of the atomic mechanisms may be obtained by appropriate infrared spectroscopy (94).

Layer splitting by hydrogen implantation and wafer bonding is of interest for use in expensive materials such as single-crystal SiC or diamond. Transfer of many thin layers onto appropriate inexpensive substrates could substantially decrease the price of these materials. Figure 8 indicates the time required to develop optically detectable surface blisters for Ge, SiC, and diamond (57). Transfer of SiC layers onto silicon (65) or onto a glass with a matching thermal expansion coefficient (66) has been reported. Also, it has been shown that coimplantation of boron at relatively low doses (around $10^{14}\,cm^{-2}$) before hydrogen implantation reduces the silicon layer transfer temperature to $\approx 200°C$. Thus silicon layer transfer to fused quartz becomes possible even though silicon and quartz have vastly different thermal expansion coefficients (64). A promising approach to reduce the cost of the layer transfer process even further is the use of plasma immersion implantation (95), which could achieve implantation faster and possibly at higher temperatures, thereby reducing implantation damage.

Attempts to perform hydrogen-induced layer splitting of other materials such as III-V compounds, sapphire compounds, sapphire, or lanthanum aluminate have thus far been successful only for gallium arsenide (M Bruel, unpublished results). Helium rather than hydrogen implantation into silicon is much less efficient because helium tends to form bubbles instead of microcracks.

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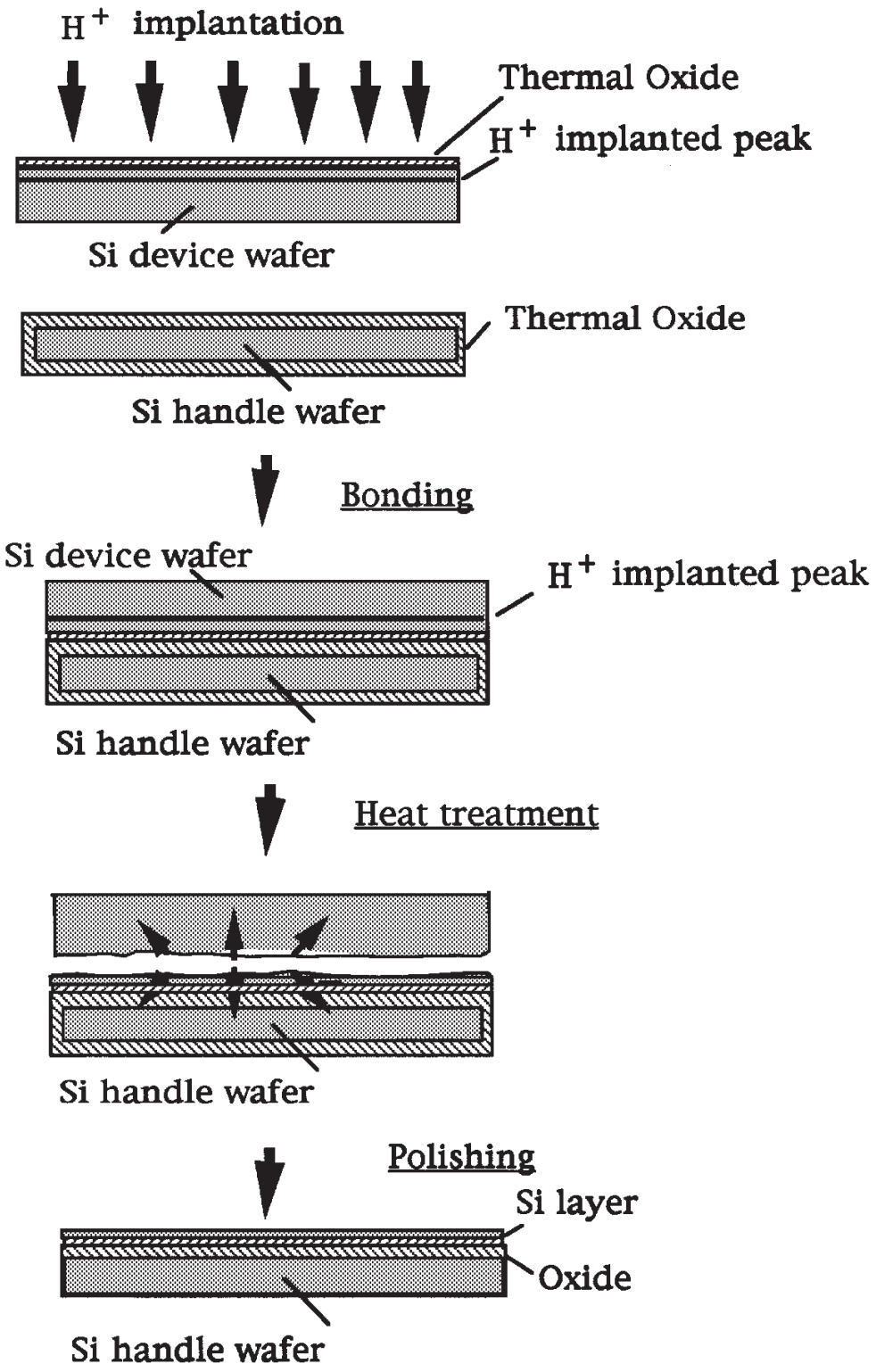

Figure 7 Schematic of different steps in the smart-cut process.

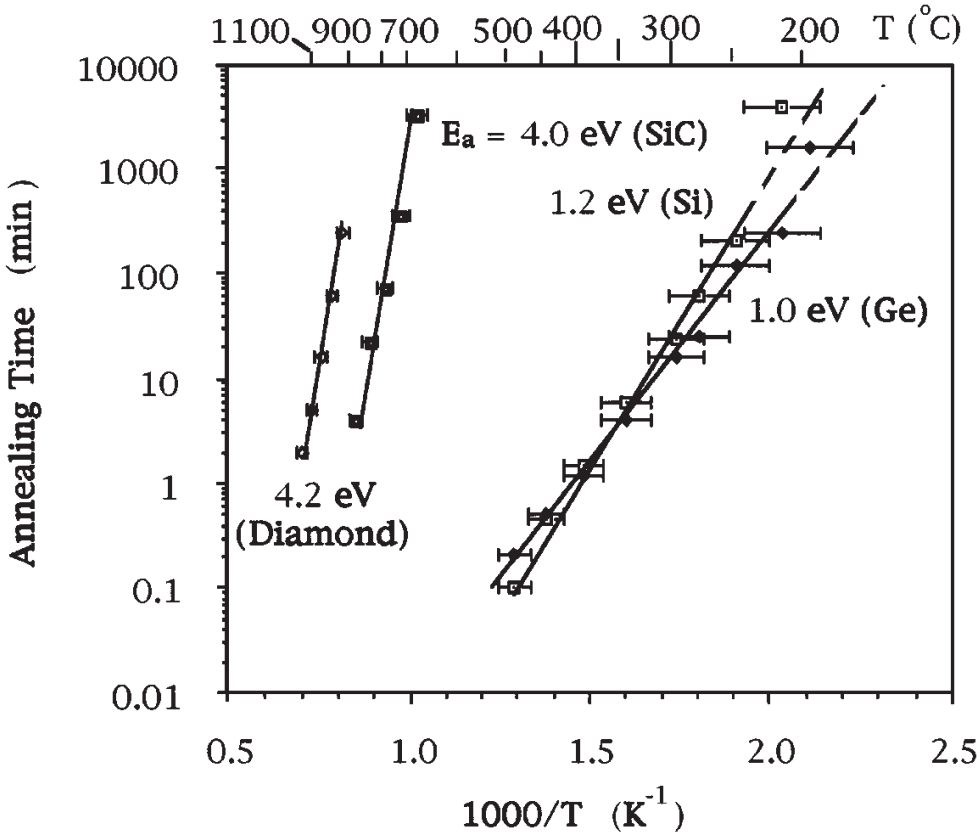

Figure 8 Time required to form optically detectable surface blisters in hydrogen-implanted Si, Ge, SiC, and diamond as a function of annealing temperature (57).

LOW-TEMPERATURE BONDING APPROACHES

Low-temperature bonding methods are desirable not only for bonded dissimilar wafers with different thermal expansion coefficients, but also for normal silicon wafer bonding, where the silicon wafers contain etch-stop or metallization layers that are sensitive to high temperatures. In the case of three-dimensional integration, the wafers may already contain microelectronic devices that would be destroyed by a high-temperature step. Relatively high bonding energies of hydrophilically bonded silicon wafers may be accomplished by long time treatments (up to many days) at temperatures around 200°C (43). An increase of the OH concentration available at the surface by treatment in appropriate chemicals (96) or by an appropriate plasma treatment (97–99) may lead to additional increases in the bonding energy. Plasma treatments need to be handled carefully in order to avoid increased formation of interface bubbles.

It has been the dream of researchers in this area to accomplish wafer bonding at room temperature with the bonded interface showing, immediately after bonding, a bonding strength close to that of the solid material. Presently, a

number of groups are attempting to accomplish this by performing the bonding under ultra-high vacuum (UHV) conditions. Previous attempts to bond fused quartz in UHV at room temperature had resulted only in van der Waals bonding and no covalent bonding (100). The possiblity of room-temperature covalent bonding of clean, adsorbate-free, reconstructed (100) silicon surfaces under UHV conditions has been predicted by molecular dynamics simulation (101). Experimentally, the required surface cleaning can be accomplished either by a heating step before room-temperature bonding (101–104) or by a plasma or ion beam cleaning (105, 106). Successful room-temperature wafer bonding with full bonding energy for 4-inch silicon wafers has been reported (101, 103), as well as bonding of smaller ($\approx$1 cm $\times$ 1 cm) pieces of Si/Si (105), GaAs/Si, and InP/Si (106). An example of a TEM cross section of UHV room-temperature-bonded silicon wafers is shown in Figure 9. Figure 10 shows a plan view of the grid of screw dislocations that are formed by the small rotational misorientation during room-temperature bonding and indicate the presence of covalent bonding. Similar dislocation networks also form after hydrophobic bonding and heating to high temperatures (107–110). Because these dislocations are associated with recombination centers for electrons and holes, a bonding interface should not be located directly in the depletion region of a device. For UHV-bonded as well as hydrophobically bonded silicon, a local rearrangement of bonds often occurs at the interface rather than a dislocation network. It is not yet understood which conditions lead to these differences. Extension of UHV wafer bonding should allow fabrication of cavities with negligible pressure in

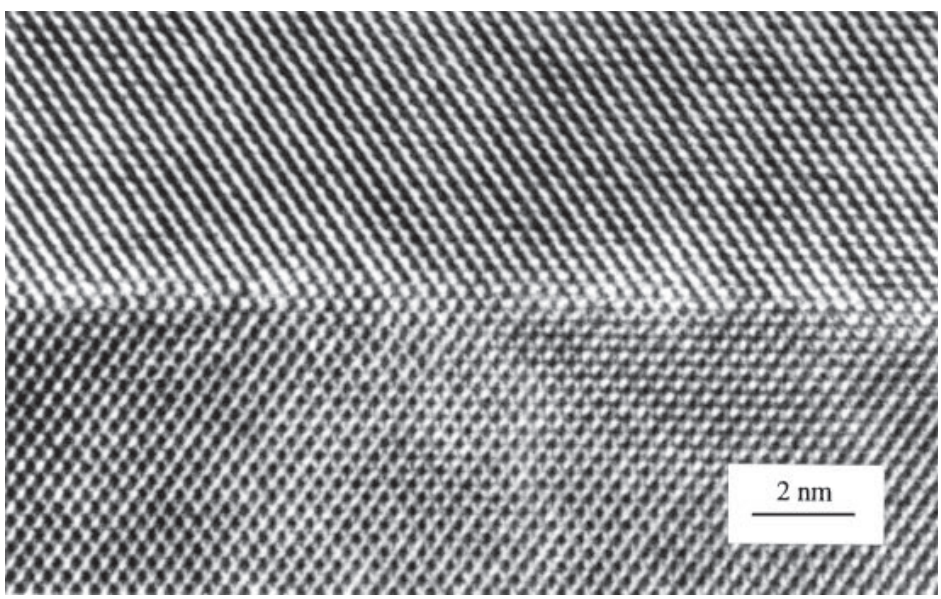

Figure 9 Cross-sectional transmission electron micrographs of the interface of silicon wafers bonded at room temperature in UHV without any further heat treatment (101).

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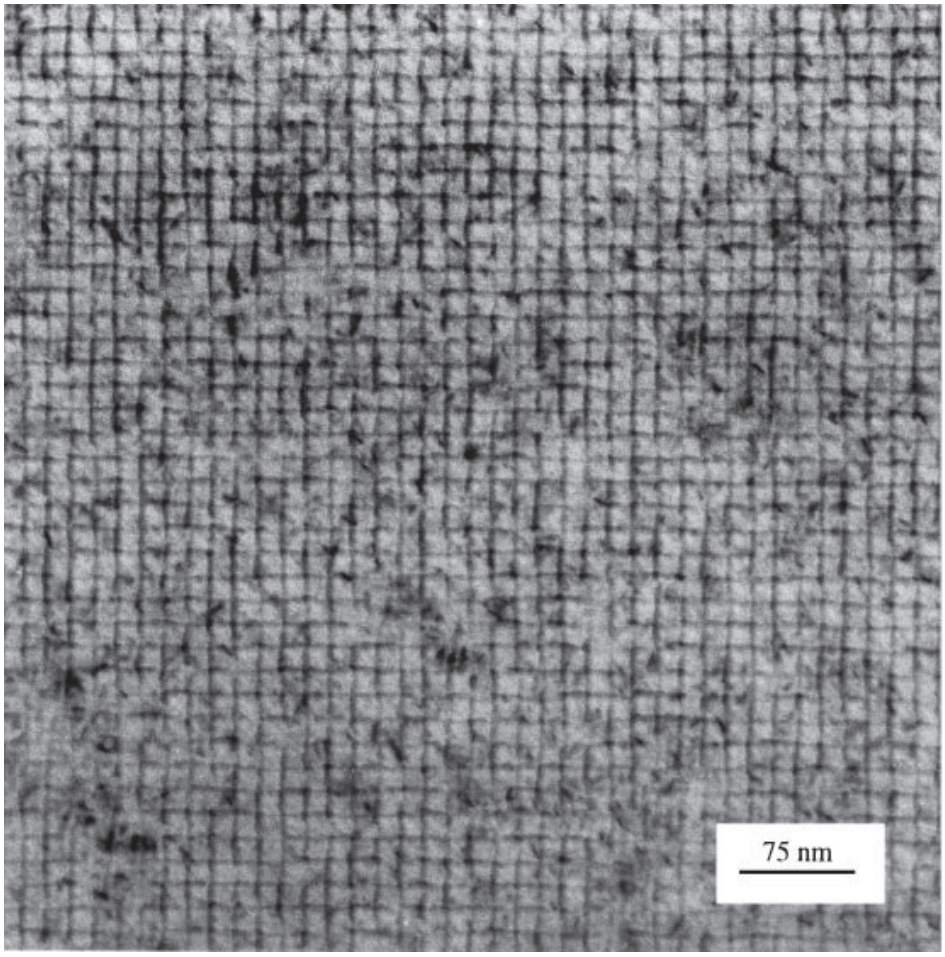

Figure 10 Plan view transmission electron micrograph of the interface of silicon wafers bonded at room temperature in UHV without any further heat treatment (103). The twist angle is around 1°.

the cavities, which is presently not possible for conventional wafer bonding because of the development of hydrogen at the bonding interface.

Recently, vacuum bonding of sputtered metal layers on single-crystal silicon or germanium has been used to fabricate so-called spin-valve transistors in which two semiconductors are separated by a thin metal layer in the 10 nm range (111, 112).

A conceptually different approach to wafer bonding is one in which the surfaces of the wafers have been made reactive by the introduction of monolayers that form covalent bonds at room temperature without creating gaseous reaction products that might lead to interface bubbles. In simplified terms, this approach makes use of a "monolayer superglue" and chemically prepared "designer surfaces." The present attempts to use this approach (113) are hampered by the fact either that (*a*) the surfaces are so reactive that they react immediately with

water vapor from the environment and, therefore, need an intermediate temperature treatment after bonding to drive off the water, or that (*b*) the reactive groups react within the monolayers on one surface instead of across the interface with reactive groups on the opposing surface. A new class of molecules is presently being tested that needs only a small thermal activation for the reaction of their endgroups and is designed to lead to covalent bonds across the interface without the generation of gaseous by-products (G Kräuter, personal communication). Further work is clearly needed to realize the potential of a monolayer superglue.

COMPLIANT SUBSTRATE

In all the applications discussed above, wafer bonding is used either as a convenient joining method or for layer transfer of material A onto a substrate of material B, where epitaxy would not work (e.g. single-crystal silicon on fused quartz) or would lead to a high density of threading dislocations due to the formation of misfit dislocations (e.g. GaAs on Si). Recently, wafer bonding has also been used to create substrates for heteroepitaxial growth, in which the formation of threading dislocations is drastically reduced or prevented, even if the heteroepitaxial layer exceeds many times its critical thickness (114) for the generation of misfit dislocations. The basic idea is that misfit dislocation formation can be prevented if the heteroepitaxial growth occurs on a basically free-standing thin film that is below its critical thickness (115, 116). Although the validity of this concept has been shown experimentally (117), it is not practical to work with free-standing films of a thickness on the order of a couple of nanometers. Rather it would be desirable to connect this film to a substrate such that it could easily shift laterally with respect to the substrate.

The first realization of such a compliant substrate is a conventional SOI wafer in which the silicon layer on the oxide has been thinned down to $\approx$10 nm. The weakly bonded zone in this case is the interface between the silicon layer and the buried oxide. Heteroepitaxial growth of a SiGe layer with a large misfit (i.e. mismatch of the lattice constants) shows a promising reduction of the number of threading dislocations compared with the case of growth of the same SiGe alloy directly on a silicon substrate (118).

The second approach to fabricating a compliant substrate also involves wafer bonding. The idea here is to generate a weakly bonded zone at the interface between two wafers bonded under a large twist angle $\approx$10–30° (119–121). The basic idea is schematically shown in Figure 11. The system investigated first was that of a (100) GaAs layer twist-bonded onto a (100) GaAs substrate. The etch-stop method, first suggested by Antypas & Edgecumbe in 1975 (23),

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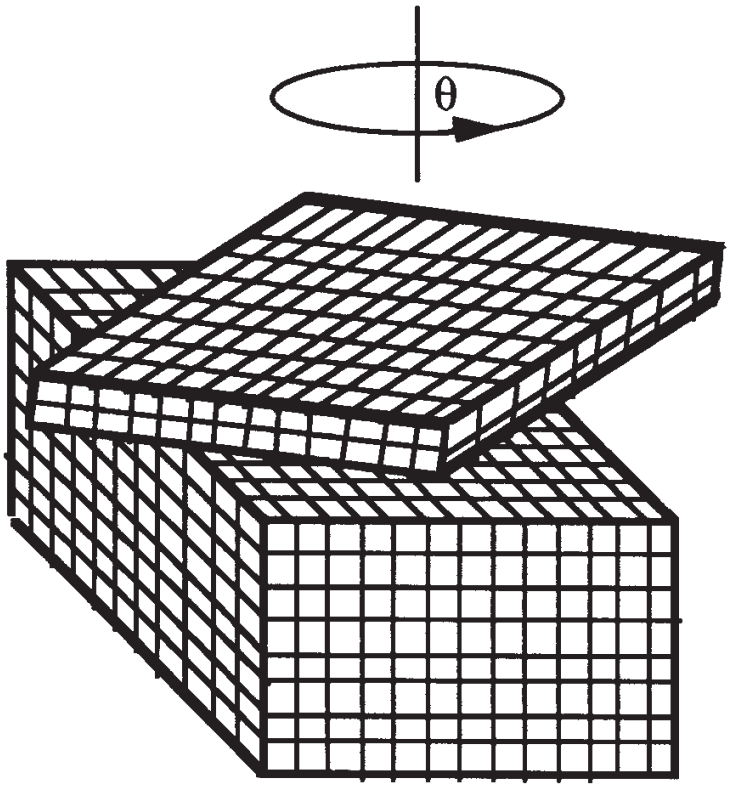

Figure 11 Schematic of fabrication of compliant substrate by twist wafer bonding.

involved epitaxial growth of a thin etch-stop layer of GaAlAs with sufficiently high Al concentration on a GaAs substrate, followed by growth of a second 3–10 nm thick layer of GaAs to be transferred. The bonding was performed under high mechanical compression under hydrogen flow at temperatures over 500°C. The typical sample sizes are about 1 cm^2. Heteroepitaxial growth of different materials ranging from $In_{0.35}Ga_{0.65}P$ (119) to InSb (121) (with misfits ranging from about 1 to 15%, respectively), with a layer thickness well above their respective critical thickness, did not show any threading dislocations in cross-section electron micrographs. Presently, it is not understood how compliant substrates work and various mechanisms have been suggested (122). Clearly, more experiments are needed, and the results have to be verified independently. In addition, it has to be shown that the method can be extended to wafer size. Nevertheless, if actually reproducible, this approach of twist wafer bonding or bonding of other combinations of crystallographically misoriented surfaces could be extended to Si/Si bonding or any combination of appropriate materials and allow heteroepitaxial growth of misfitting material without the usual drawback of threading dislocations, which are detrimental in many electronic or optoelectronic applications.

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OUTLOOK

SOI wafers with diameters up to 8 inches, fabricated by wafer bonding and various thinning techniques, are now commercially available in Japan, in the United States, and in Europe. Fast and astonishing progress has been made in the area of thinning techniques. Only a few years ago, the area of ultra-thin SOI layers ($\ll 1\ \mu$m) was considered to be the domain of SIMOX technology (19), but this is certainly not the case at present. Wafer bonding is now fully competitive with other SOI fabrication techniques in facing the difficult challenge of incorporation into mainstream DRAM and microprocessor technology.

Wafer bonding is already established for industrial fabrication of some sensors, but it still not as common as anodic bonding. Wafer bonding and fusion applications are in use for production of LEDs. In many other areas, wafer bonding applications are still in a research or development stage. The development of new techniques such as hydrogen-implantation-induced layer splitting appears promising not only for SOI silicon wafer production but also for materials other than silicon.

Wafer bonding offers a new degree of freedom in the design of material combinations without the usual restrictions imposed by the structure (amorphous, polycrystalline, orientation, lattice constant) of the materials to be bonded. Since we were educated to take these restrictions seriously, we now must think differently to take advantage of wafer bonding in heretofore unexplored areas. Wafer bonding opens up new design possibilities that presently appear to be more limited by our lack of imagination than by practical constraints.

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