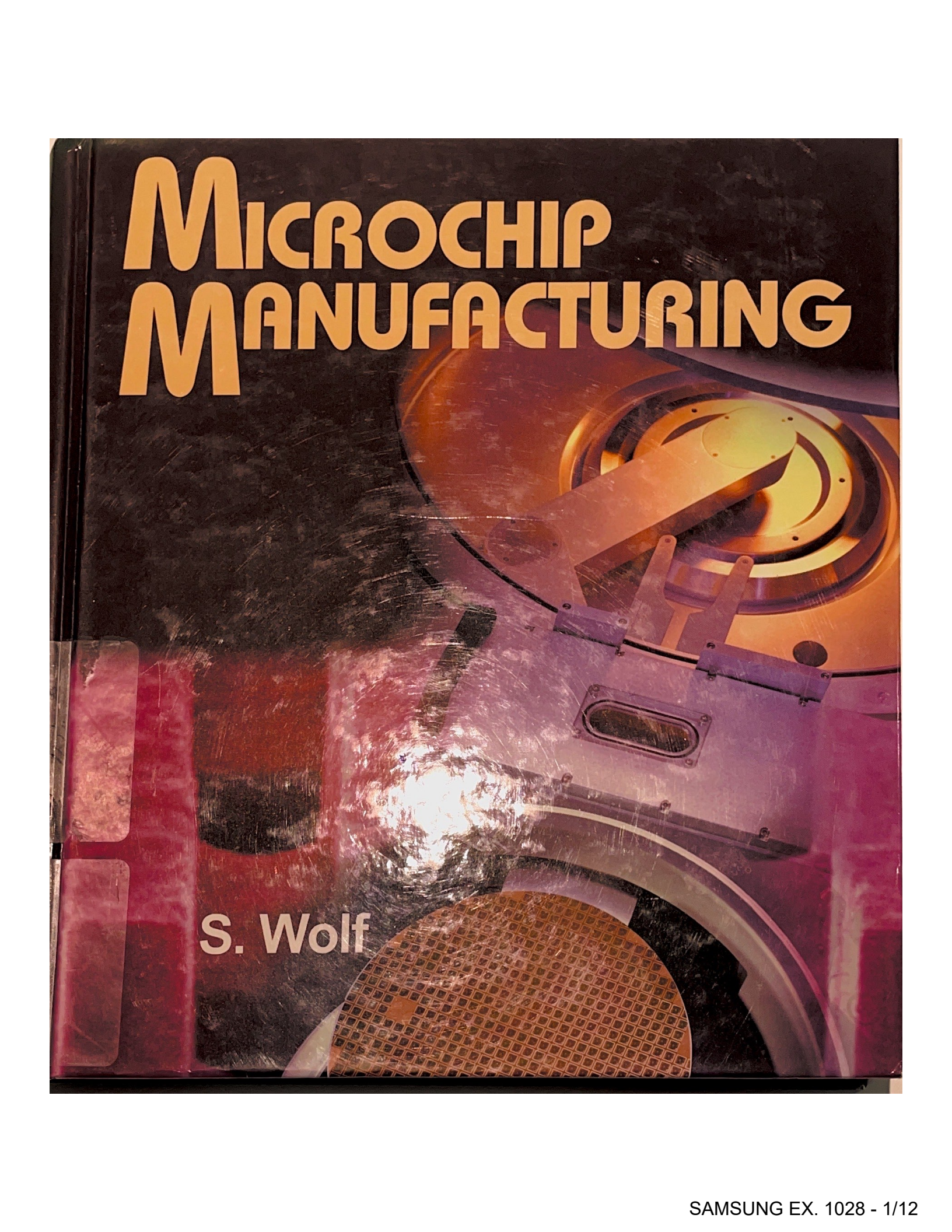


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CHAPTER 17

SILICON EPITAXY AND SILICON-ON-INSULATOR TECHNOLOGY

CHAPTER CONTENTS

- 17.1 EPITAXY DEVICE APPLICATIONS
- 17.2 GROWTH OF EPITAXIAL LAYERS
- 17.3 CHEMICAL-REACTIONS OF SILICON
- 17.4 PROCESS CONSIDERATIONS FOR EPITAXIAL DEPOSITION
- 17.5 EPITAXIAL PROCESS-EQUIPMENT
- 17.6 CHARACTERIZING EPI-LAYERS
- 17.7 SILICON-ON-INSULATOR (SOI)

"I didn't fail 1000 times. The lightbulb was an invention with 1001 steps."

Thomas Edison

The Molecular Dance Floor.

Thanks to the graphic artists, Jerry Healey and Alan Gasperini.

Epitaxy is a process in which a single-crystal film is deposited upon the surface of another crystalline-substrate. The term *epitaxy* comes from two Greek words, *epi* ("upon") and *taxis* ("arranged," or "ordered"). Together they mean *arranged-upon*, and such films are also referred to as *epi-layers* (Fig. 17-1). If the grown-film consists of the same material as the substrate, the process is referred to as *homoepitaxy*. This is the most important use of epitaxy in silicon-technology. On the other hand, if the epitaxial-film is grown on a substrate of different material, the technique is called *heteroepitaxy*. An example of heteroepitaxy is the deposition of silicon on aluminum-oxide (*sapphire*), a method by which *silicon-on-sapphire* (SOS) wafers are fabricated. More details on Si epitaxial-growth can be found in Refs. 1 (and 3 to 6), listed at the end of the chapter.

Epitaxial-growth can be achieved by forming the film from: 1) a vapor-phase (*vapor-phase epitaxy* [VPE]); 2) a liquid-phase (*liquid-phase epi-*

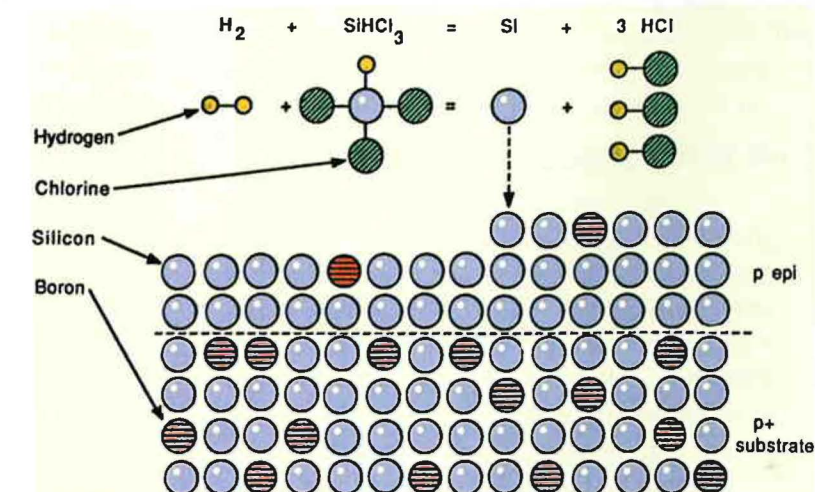


Fig. 17-1 Schematic drawing of a lightly-*p*-doped silicon-epitaxial-film on a heavily-*p*-doped silicon-substrate.

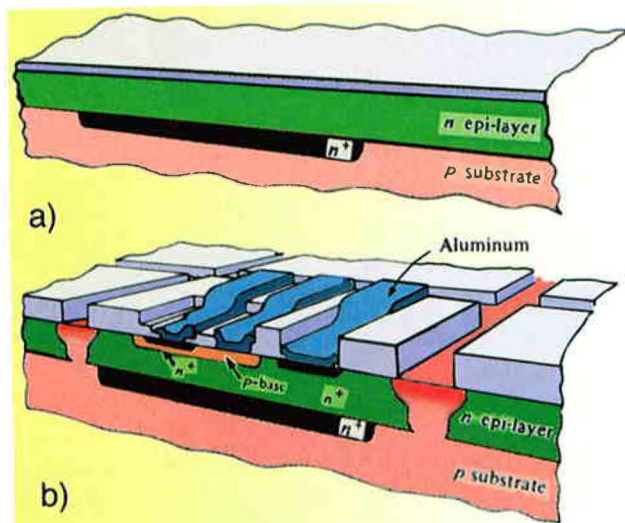


Fig. 17-2 (a) Lightly n -doped epitaxial-layer deposited over heavily n -doped buried-layers in a p -type Si-substrate. (b) Completed SBC-bipolar-transistor-structure built using an epitaxial-layer.

taxy [LPE]); or 3) a solid-phase (*solid-phase epitaxy* [SPE]). High-temperature VPE ($\sim 1000^\circ\text{C}$) is used exclusively to produce epi-layers on silicon wafers because this technique offers tight-control of epi film-thickness and impurity-concentration, together with a high-degree of crystalline perfection.

This chapter describes: 1) the uses of epitaxy in silicon-technology; 2) the basics of epitaxial film-formation; 3) epitaxial process-technology; and 4) epitaxial film-characterization. It also briefly introduces silicon-on-insulator technology (SOI).

17.1 THE DEVICE APPLICATIONS OF EPITAXY

Epi-layers in silicon-technology are mostly used to form lightly-doped layers on heavily-doped substrates for device structures that require such doping-profiles at the wafer surface (see Fig. 17-1). Epitaxial-deposition is chosen because there is no other method in planar-processing for obtaining such lightly-doped layers on more heavily-doped sublayers. Two device structures need this kind of doping-profile: 1) *standard-buried-collector* (SBC) bipolar-transistor structures; and 2) certain types of CMOS ICs.

The BJT-SBC-structure increases the breakdown-

voltage of the collector-base junction of bipolar-transistors. By growing a lightly-doped n -type epi-layer over a heavily-doped n^+ -substrate, the bipolar-device is optimized for high breakdown-voltage of the collector-base junction, while preserving a low-value of collector-resistance. Low collector-resistance is needed to improve device operating-speeds at moderate-currents. Figure 17-2 depicts a cross-section of a bipolar-transistor showing the formation and role of the epi-layer. A key feature of bipolar-epitaxy is that the film is deposited over patterned, n^+ -doped diffused-layers called *buried-layers* or *sub-collectors*. BiCMOS-devices are also fabricated in epitaxial-films deposited over such patterned buried-layers.

Epi-layers are also widely-used in building CMOS integrated-circuits. In these CMOS-circuits the MOSFET-devices are fabricated in a thin ($2\text{--}4\text{-}\mu\text{m}$ -thick), lightly-doped p -type epitaxial-layer deposited over a uniformly heavily- p^+ -doped substrate. The role of such lightly-doped epi-layers on a heavily-doped substrate is to suppress the tendency of CMOS to undergo the failure-mode called *latchup*. Figure 17-3 shows a cross-section of a twin-well CMOS device depicting this type of epi-layer.

Epitaxial-layers also offer the important advantage of improving the reliability of thin gate-oxide films grown on a silicon-surface. This occurs because the epi-layer is free from oxygen, an impurity that exists in CZ-silicon as a result of the CZ crystal-growth process (see Chap. 9). With no oxygen in the epi-layer, oxygen precipitates cannot form (whereas they can occur near the surface of so-called *bulk-CZ-Si*

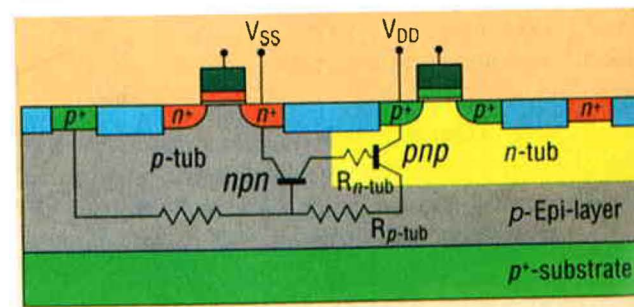


Fig. 17-3 Cross-section of a twin-well CMOS structure built in a p -epitaxial layer and a p^+ substrate.

wafers). The presence of such oxygen-precipitates degrades the electrical integrity of gate-oxides.

17.2 GROWTH OF EPITAXIAL-LAYERS

Epitaxial film-growth follows many of the same steps as the basic thin-film growth-sequence presented in Chap. 7. But other factors also play a role in the successful deposition of an epitaxial-film. These are described with the aid of Figs. 17-4 and 17-5.

Atoms from the vapor-phase are adsorbed on the crystalline silicon-surface and thus become *adatoms*. Such adatoms may migrate along the surface (Fig. 17-4). If this migration is rapid enough, the adatoms can orient themselves to the crystal-structure of the substrate surface. For example, if a migrating adatom encounters a growing *terrace* (such as position B in Fig. 17-5), or a *kink* (such as position C in Fig. 17-5), these are locations where the adatom will bond. In this way, they become an extension of the single-crystal lattice. Epi-growth continues, atom-by-atom, layer-by-layer, as additional adatoms migrate to terrace or kink positions and get incorporated in the crystalline-film that grows on the surface.

However, if adatom migration is constrained during growth, a polycrystalline-film is more likely to be deposited than an epitaxial-layer. This happens if the deposition-rate is too-high or the deposition-temperature is too-low. At any particular deposition-temperature there exists a maximum deposition-rate, above-

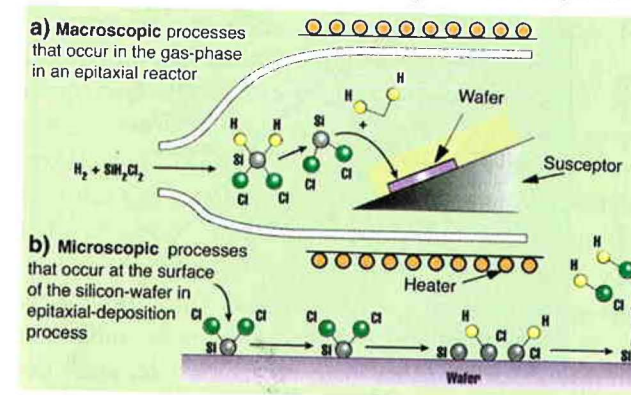


Fig. 17-4 Phenomena that occur during an epitaxial-deposition process at: (a) the *macroscopic* level; and (b) the *microscopic* level.

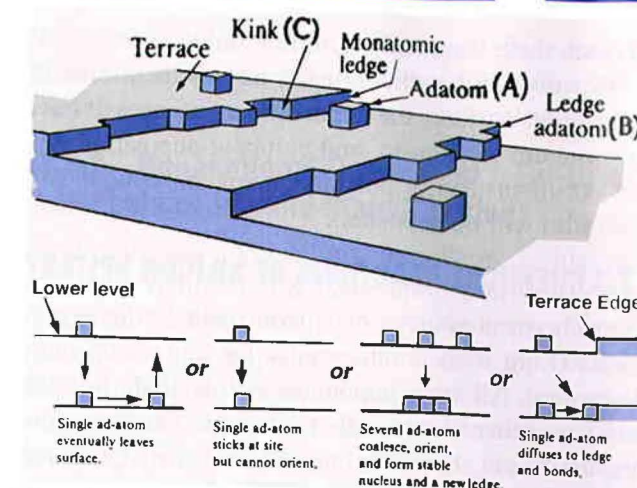


Fig. 17-5 Epitaxial growth-model showing step-wise growth with adatoms in terrace-positions A, adatoms at steps (or terrace-edges) B, and adatoms at stable kink-positions C.

which polycrystalline-films are formed, but below which single-crystal epitaxial-films are deposited. Figure 17-6 shows a plot of the effect of growth-rate and temperature on the formation of single-crystal or polycrystalline-films. At high growth-rates there is not sufficient time for adatoms to migrate to the terrace (or kink) sites. Thus, only polycrystalline-growth can occur. But, as temperature is increased, the surface-migration-rate also rises, allowing time for adatoms

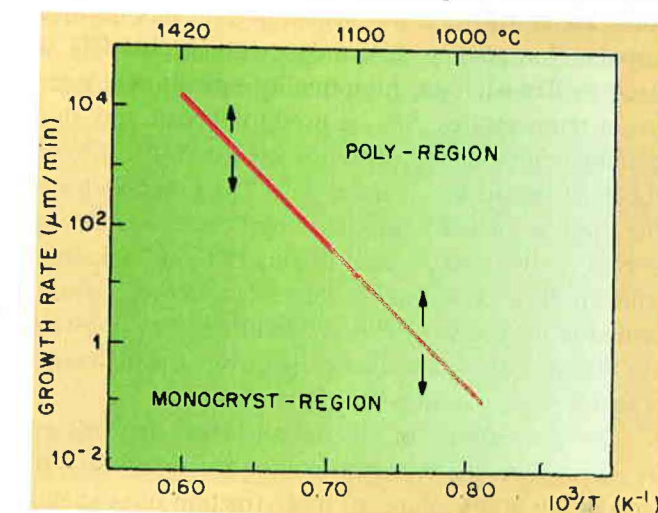


Fig. 17-6 Maximum growth-rate for the formation of single-crystal silicon as a function of temperature.⁷

to reach these sites and orient themselves.

However, if the silicon-wafer has a silicon-dioxide layer on its surface, the depositing adatoms will have no structure to align-to, and epitaxial-deposition will not occur. Instead, a polysilicon (or amorphous-silicon) film will be deposited.

17.3 CHEMICAL REACTIONS OF SILICON EPITAXY

Four chemical-sources of silicon (called *silicon-precursors*) are used commercially for epitaxial silicon deposition. All are compounds with a single Si-atom and four other atoms, either Cl or H. These silicon-precursors are: **1)** *silicon-tetrachloride* (SiCl_4); **2)** *trichlorosilane* (SiHCl_3 - called *TCS*); **3)** *dichlorosilane* (SiH_2Cl_2 - called *DCS*); and **4)** *silane* (SiH_4). Each silicon-precursor has advantages for specific deposition-conditions and epi-film applications.

SiCl_4 was the most widely-used precursor in the early days of IC-fabrication. But, because it needs the highest deposition-temperatures for practical epi-processes, SiCl_4 is not used much any more. Requirements for thinner epi-layers and lower deposition-temperatures have caused it to be largely replaced by SiH_2Cl_2 , SiHCl_3 , and SiH_4 . For example, SiHCl_3 produces epi-films that are very similar in quality to those deposited by SiCl_4 , but they are produced at temperatures about 100°C lower. Thus, SiHCl_3 has become popular for routine Si-epi-depositions. SiH_2Cl_2 is used to deposit thin, high-quality epi-films at even lower temperatures. SiH_4 is used to deposit very-thin epitaxial-films at temperatures below 900°C . When these Si-precursors are fed into the process-chamber, they are heavily-diluted in hydrogen, which also serves as the *carrier-gas*. The carrier-gas maintains uniform flow-conditions in the reactor before, during, and after the growth-cycle. As other gases responsible for the epi-growth are added, the carrier-gas maintains a steady-state gas-flow-condition.

The growth-rate of silicon epi-layers depends on several factors including: **a)** type of precursor used; **b)** deposition-temperature; **c)** mole-fraction of reactants present in the vapor-phase; and **d)** reactor-pressure.

Figure 17-7 illustrates the silicon growth-rate as a

function of temperature for the four precursors listed above. Several key ideas can be learned from this figure. First, one of the factors that controls the deposition-rate is the type of silicon-precursor used. For example, use of SiH_4 provides the highest growth-rate at any temperature, followed by SiH_2Cl_2 , and SiHCl_3 (with SiCl_4 the slowest). Second, two growth-regimes are evident. At temperatures where the deposition-rate increases relatively-slowly with temperature (Regime-B of Fig. 17-7) the mechanism that controls the growth-rate is *gas-phase mass-transport*. Such growth is said to be *mass-transport-limited* (see Ch. 16). At lower-temperatures, the growth-rate strongly depends on temperature, implying that it is controlled by a *thermally-activated process* (i.e., it is *surface-reaction-rate-limited* (Regime-A of Fig. 17-7)).

17.4 PROCESS CONSIDERATIONS FOR EPITAXIAL-DEPOSITION

A variety of important process-considerations must be taken into account when depositing epi-layers for IC-device applications. They are covered in this section.

To begin, the epi-growth-rate is set by choosing the appropriate deposition-temperature and gas-flow conditions for the silicon-precursor being used. As shown in Fig. 17-8, the precursor-gas is diluted in a hydrogen carrier-gas, and its mole-fraction is selected to provide the desired epi-growth-rate.

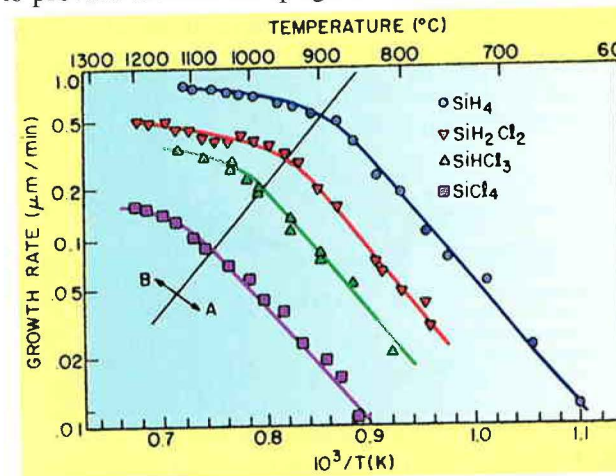


Fig. 17-7 Growth-rates of silicon films as a function of temperature for various silicon-sources.⁸

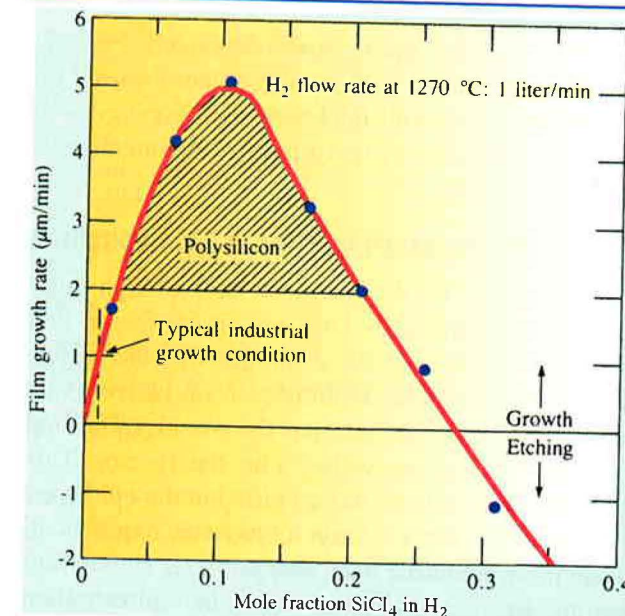


Fig. 17-8 Silicon growth-rate as a function of SiCl_4 -concentration (mole-fraction, Y , of SiCl_4 in H_2).⁹

17.4.1 Intentional Doping of Epitaxial-Films

The doping-level in epitaxial-films is one of their most-important characteristics, and it must be tightly controlled. The correct doping-concentrations for a particular application are produced in epi-layers by adding gases containing the appropriate dopants to the reaction-gases during the epitaxial growth-process. For *p*-type-layers (boron-doping), diborane [B_2H_6] is added to the reactant-gas. For *n*-type-layers either phosphine [PH_3], or arsine [AsH_3], is added for phosphorus or arsenic doping, respectively. At high-temperatures, these dopant-hydrides decompose and release boron, phosphorus, or arsenic into the growing epitaxial-film (Fig. 17-9). These gases are introduced into the reaction-chamber from gas-cylinders, where they are already diluted in hydrogen to concentrations of 20–100 parts-per-million (ppm). Such diluted-concentrations allow better control of the amount of dopant in the gas-stream (because smaller flow-variations are required). When dopant-gases are mixed with the main hydrogen-flow in the epi-reactor, their concentration is further diluted to the ppb-range necessary to produce the desired doping-levels in the epi-films.

Note that extraordinary caution must be exercised when handling the gas-cylinders containing these dopant-gases, since the gases are extremely-toxic.

17.4.2 Unintentional-Doping of Epi-Layers (Autodoping and Solid-State Diffusion)

Most epitaxial-applications in silicon technology call for a *lightly-doped* layer upon a *heavily-doped* substrate. Section 17.4.1 describes how the desired-concentration of dopants in the lightly-doped layers is controlled. However, during epitaxial-deposition, *unintentional-dopants* can also enter the growing-film in two other ways: **1)** dopants from the heavily-doped substrate can diffuse into the growing-film (an effect called *outdiffusion*); and **2)** dopants from the back of the heavily-doped substrate can diffuse out from the wafer, mix in the gas-stream, and become incorporated in the growing-film. This is called *vapor-phase-autodoping*. Outdiffusion and autodoping produce a *transition-layer* in the epi-layer in which the doping-concentration value lies between the substrate and desired epi-layer values. Without these effects, the carrier-concentration values would abruptly-change from those in the highly-doped substrate to those specified in the lightly-doped epi-layer (Fig. 17-10a).

The *transition-layer* between the heavily-doped substrate and the lightly-doped epi-regions is shown in Fig. 17-10b. The region of the epi-film close to the substrate shows higher doping-levels than intended,

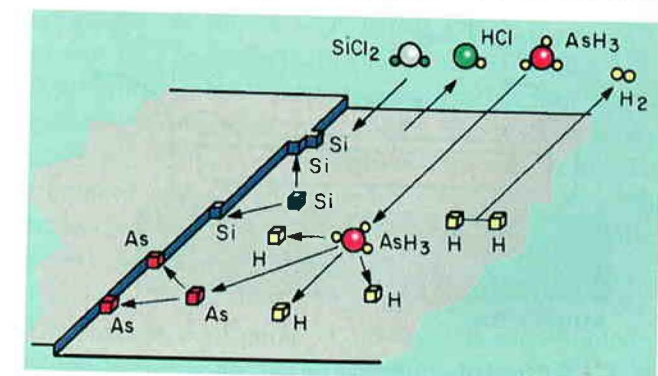


Fig. 17-9 Schematic of the epitaxial growth-process at the microscopic level showing the incorporation of Si and a dopant (in this case, arsenic) into the epi-film.

since dopant has diffused out of the substrate into the growing film during deposition (Region-A in Fig. 17-8b). However, the rapid growth of the film relative to the outdiffusion-front quickly limits this effect.

Thereafter, doping in the transition-layer is controlled by the incorporation of dopants from the vapor-phase. When dopant-atoms in the vapor-phase (evaporated from the substrate) exceed those intentionally-introduced, an *autodoping-tail* develops (Region-B in Fig. 17-10b). Since the high-concentration substrates quickly become covered with more lightly-doped material, the autodoping effect eventually ceases, and the desired concentration is reached. However, if the entire-substrate is heavily-doped, evaporation from the wafer-edges and backside can

continue, even after the front-side is sealed (Fig. 17-10c). Outdiffusion and autodoping impose a limit on the minimum epitaxial-thickness and doping-level, and therefore processes that minimize unintentional-doping are preferred.

17.4.3 Wafer-Preparation Prior to Epi Deposition

To be effective, epi-layers must have a high-quality crystalline-structure. One important factor that impacts this quality is the cleanliness of the wafer-surface. For example, a thin-layer of native-oxide may remain on the surface after the wet-cleaning step done prior to loading wafers into the reactor. This oxide must be removed before growing the epi-layer.

The most common way to remove oxide is to expose the wafers to a *hydrogen pre-bake step* before injecting the reaction-gases into the epi-chamber. That is, wafers are baked in an ultrapure H_2 -gas at a moderate-temperature (850–900°C) for a short period of time (2–3-min). In some cases, this step is performed at the same temperature as the epi deposition-step (e.g., to improve the throughput of single-wafer reactors). For this pre-bake step to be effective, the partial-pressure of oxygen within the reactor (from O_2 or H_2O) must be low enough so that SiO_2 is no longer thermodynamically-stable at the process-temperature. The pre-bake step works by converting SiO_2 to volatile sub-oxides (e.g., SiO) which sublime from the wafer-surface.

17.4.4 Batch Epitaxy Process-Sequence

The sequence of steps for depositing epi-layers in a batch-mode (Fig. 17-11), is identical for all types of batch-reactors. The wafers are carefully cleaned with a chemical pre-cleaning process just before loading them into the system. After the wafers are loaded into the reactor, it is closed and hydrogen is flowed in, to purge the air within. Next, the temperature is raised to 850–900°C. This pre-bake step in H_2 (for about 3-minutes) removes any native-oxide layer still present. Then the temperature is raised to 1150–1200°C, and HCl is flowed into the chamber for another 3-minutes. This slightly-etches the Si-surface to remove

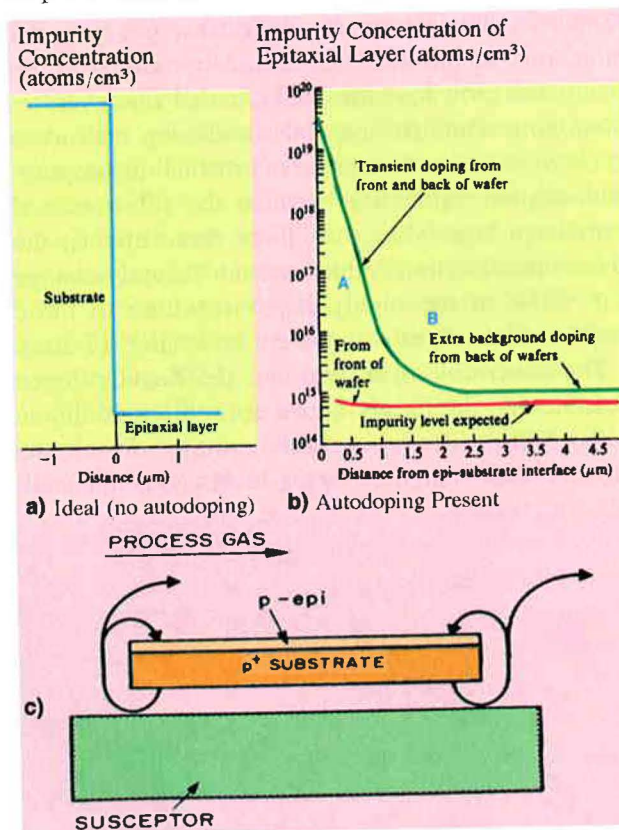


Fig. 17-10 Effect of autodoping on the concentration-profile near the interface between an epitaxial-layer and a heavily-doped-substrate: (a) Ideal-case (no autodoping); (b) Case when autodoping occurs; (c) Back-surface autodoping.

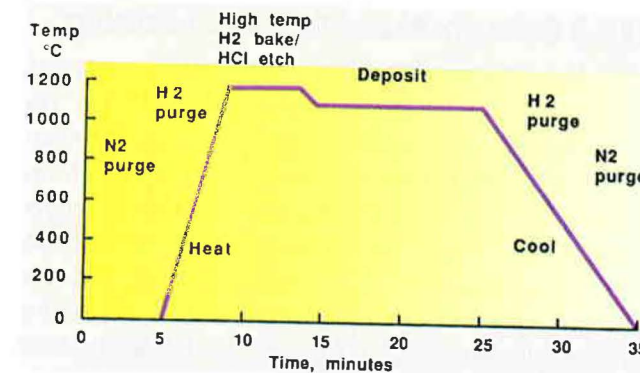


Fig. 17-11 Typical batch epitaxial-deposition cycle.

any other contamination (or lattice damage). Now the Si-surface is clean and ready for epitaxial-deposition. The chamber-temperature is adjusted to the deposition-temperature, and after stabilizing, the silicon-precursor, dopant, and carrier-gases are flowed into the chamber to grow the silicon epi-layer. After the film has been grown, the process-gases and heater-power are turned-off. H_2 -gas is flowed to purge the chamber of the process-gases. When cooled sufficiently, N_2 purges the chamber to ambient-temperature. It can then be opened, unloaded, and reloaded. The whole sequence takes under an hour, and 10–28 wafers are processed at a time.

17.5 EPITAXIAL DEPOSITION EQUIPMENT

Silicon epitaxial-films are deposited in CVD-systems especially designed for epi-layer formation. A number of different reactor-designs have been developed. The two types in widest commercial-use today are: 1) the multi-wafer IR-radiantly-heated barrel-reactors; and 2) the single-wafer IR-lamp-heated reactors. Single-wafer reactors are most popular for large wafer-sizes (≥ 200 -mm).

Generally speaking, epitaxial deposition-systems all have the following subsystems: a) a reaction-chamber (which may be a quartz bell-jar or reactor-tube); b) a gas-distribution subsystem; c) a subsystem for heating the wafers; d) a susceptor that holds the wafers; e) an exhaust-system which removes the gases from the process-chamber; and f) a temperature-monitoring and control subsystem.

17.5.1 Batch Horizontal-Tube Epi-Reactors

The first epitaxial-reactors used for VPE in silicon technology were the batch, horizontal, fused-silica-tube reactors (Fig. 17-12a). In them, a number of wafers are placed on their backs on a flat susceptor (usually made of graphite, coated with silicon-carbide). The susceptor is heated by an rf-induced current. That is, rf-coils surround the tube, and rf-energy is passed through the walls of the fused-silica-tube without heating them. Instead, it is “coupled” to the molecules of the graphite, causing the susceptor to heat-up by rf-induction. The susceptor, in turn, heats the wafers by radiation and convection. The tube walls remain cool, making this a *cold-wall reactor*.

The process gases (at atmospheric-pressure) enter the inlet at the front of the tube. They flow over the wafers, and are exhausted from the outlet at the back. The reactor design is simple and less expensive than that of other epi-reactors. However, it is hard to maintain wafer-to-wafer uniformity. (Note that as shown in the figure, the susceptor is tilted a few degrees in an attempt to improve thickness-uniformity from wafer-to-wafer.) The throughput is also small, because the susceptor cannot hold many large-diameter wafers. For these reasons, batch, horizontal-tube epi-reactors no longer find much use.

17.5.2 Vertical Pancake Epi-Reactors

The so-called *induction-heated, vertical, pancake epi-reactor* is shown schematically in Figs. 17-12b, c, and d. The wafers are placed on a rotating silicon-carbide-coated graphite-susceptor, again heated inductively by underlying rf-coils. The reactant-gases enter the reaction-chamber from the center of the susceptor and are subsequently exhausted from the periphery. The gases are distributed symmetrically across the wafers, resulting in a constant growth-rate. The vertical gas-flow minimizes autodoping-effects. The pancake configuration, however, is susceptible to particulates falling on the wafer (and then becoming embedded in the growing film). The system is capable of processing wafers up to 200-mm in diameter, but the load-size decreases as the wafer-size is increased.

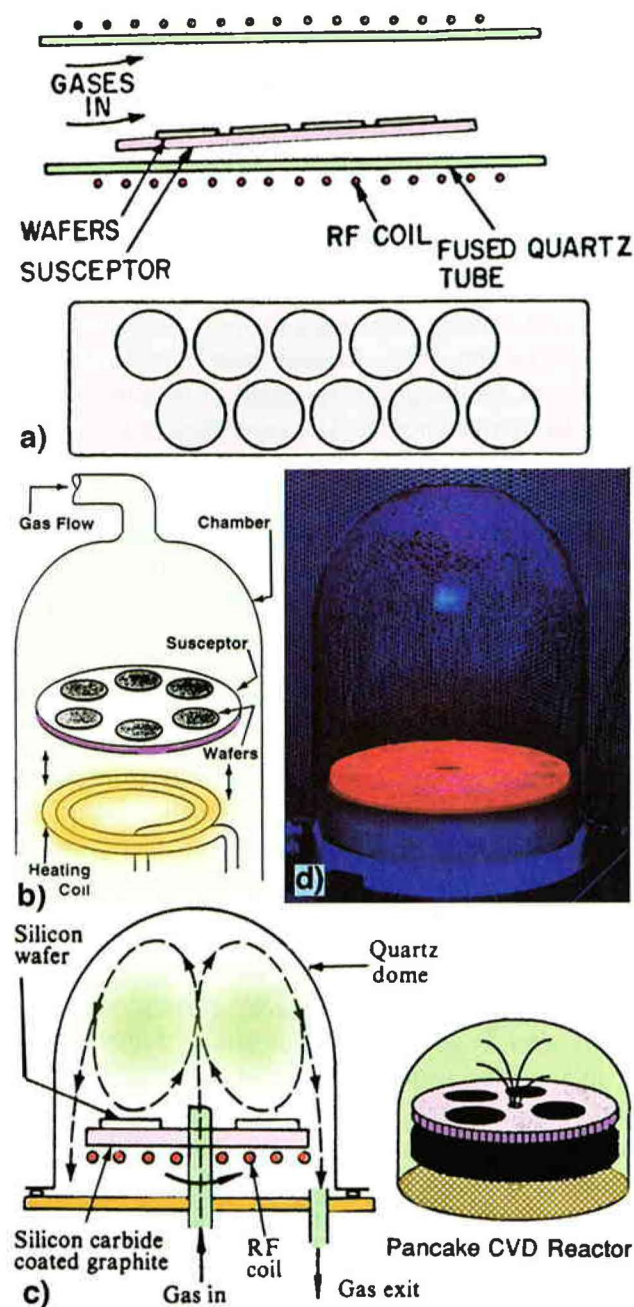


Fig. 17-12 (a) Horizontal-type epitaxial-reactor. (b) Pancake-type epitaxial-reactor. (c) Another schematic drawing of a pancake silicon-epitaxial-reactor. (d) Photograph of a pancake-type silicon-epitaxial-reactor.

17.5.3 Radiantly-Heated Cylindrical Reactors

A *radiantly-heated, barrel (or cylindrical), epitaxial-reactor* is shown schematically in Fig. 17-13. The susceptor has a hexagonal cross-section and is again fabricated from silicon-carbide-coated graphite. More wafers can be loaded onto the hexagonal-shaped susceptor than onto the flat-susceptor of the horizontal-tube epi-reactor because each face of the hexagon can accommodate one (or several) wafers, depending on their diameter. The wafers are held at an angle of 2.5° to the vertical, and the gases flow parallel to the wafer-surfaces. The reaction-chamber is a stainless-steel barrel, with high-intensity quartz-heaters placed about its inside surface. The susceptor rotates in the center of the barrel.

Reactant-gases are injected at the top of the chamber and exhausted from the bottom. Wafers are heated directly by water-cooled quartz-lamps lining the inside of the reactor. Heating the wafer from the front-side decreases the occurrence of thermally-induced slip. Rotation of the wafers in the reaction-gases produces a more uniform film-thickness, compared to batch horizontal-tube systems.

Cylindrical epi-reactors are capable of operating at atmospheric or reduced pressure (80–100-torr). Another advantage they have is that the wafers are held in near-vertical positions, so particles are less likely to land on them. Barrel-reactors are capable of resistivity- and thickness-uniformity better than $\pm 5\%$ across the wafer, wafer-to-wafer, and run-to-run. However, their throughput is low when processing large-diameter wafers (≥ 200 -mm in diameter).

17.5.4 Single-Wafer Epitaxial Systems

Single-wafer epitaxial-reactors were introduced in the 1990's when 150- and 200-mm wafers first came into use. The single-wafer system becomes more economical than a batch-system for large wafers, and is now the most widely used type of epi-tool. Figures 17-14a & b show a cross-section of a single-wafer epi-reactor. The chamber is constructed from fused-silica. Because the process requires extremely-high temperatures (1050–1150°C) the chamber-walls could

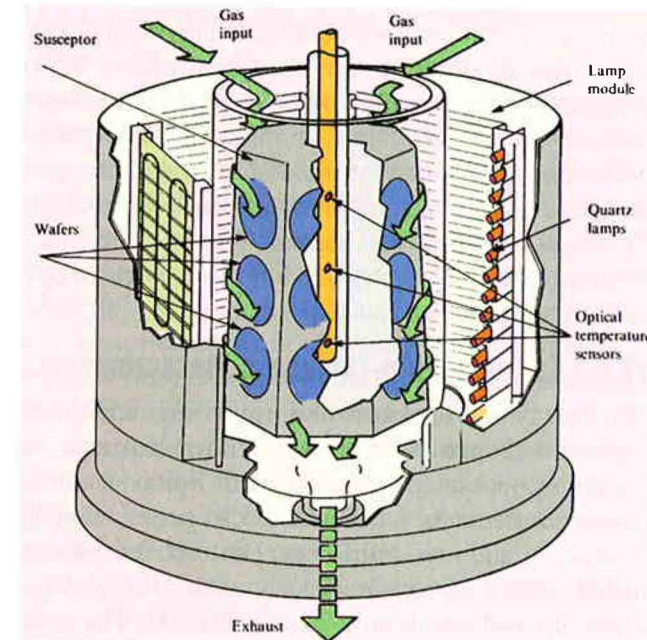


Fig. 17-13 Schematic of a radiantly-heated, cylindrical-type epitaxial reactor. Courtesy of Applied Materials, Inc.

become quite hot. To prevent them from becoming excessively-heated, water and air-cooling must be used. Wall-temperature is kept between 400–600°C.

Such systems have a high epi-layer growth-rates and better reliability and repeatability than batch epi-reactors. They can deposit high-quality films at atmospheric or reduced pressures. The susceptor (and wafer) is rotated to even-out temperature and gas-flow fluctuations. Wafer-rotation has been found to substantially improve process-uniformity.

The system rapidly heats the wafer ($18^\circ\text{C}/\text{sec}$) to the process-temperature using quartz IR-lamps. The top-surface of the wafer is heated by the upper lamp-assembly and the bottom-surface through the susceptor (which is heated by a lower lamp-assembly). Thus, a uniform-temperature is maintained throughout the wafer, preventing slip-defects that could occur during such rapid-temperature ramp-rates. Once the wafer reaches temperature, it is stabilized and “pre-baked” in H_2 (for about 1-minute) to remove any native-oxide on the wafer-surface.

The process-gases (precursors and dopant) are

then fed into the reactor from a side-port. (These gases are pre-mixed before they enter the chamber, along with the H_2 carrier-gas.) They flow over the wafer in a laminar manner and then exit the system from another side-port. By attaching a vacuum pump to the outlet of the reactor, it can also be operated at reduced-pressure.

When the deposition-process is complete, the flow of reactant and dopant gases is halted (but the H_2 flow continues). When the wafer has cooled to about 750°C it is taken from the reactor and moved into a cool-down chamber. This chamber rapidly cools the

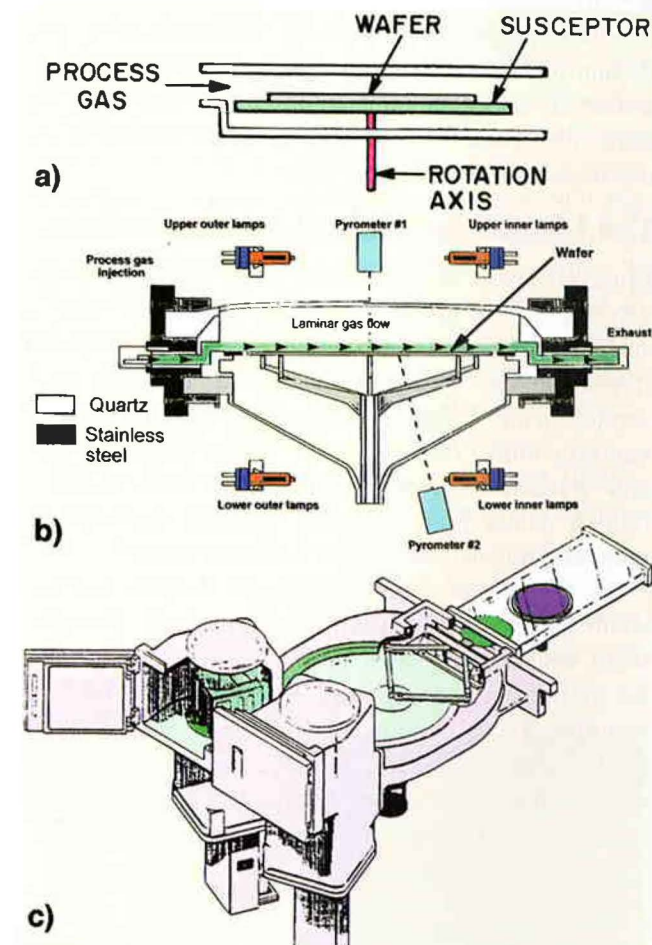


Fig. 17-14 (a) and (b) Cross-section of a single-wafer epitaxial reactor. Courtesy of Applied Materials, Inc. (c) Perspective drawing of a commercial single-wafer epitaxial reactor. Courtesy of ASM International.

wafer to $<200^{\circ}\text{C}$, after which it is put back into the wafer cassette. Single-wafer epitaxial-reactors are manufactured by Applied Materials Inc. (Fig. 17-14b) and by ASM International (Fig. 17-14c).

17.6 CHARACTERIZATION OF EPITAXIAL-FILMS

Characterization of epitaxial-films is performed to monitor the epi-dependent properties of product-devices early in the fabrication sequence. If the epi-quality is poor, it is unlikely that high-quality devices can be made in the film. Epi-layers are inspected for: **a)** surface-quality; **b)** crystallographic-defects; **c)** electrical-properties (resistivity, carrier-lifetime, and dopant-profile); and **d)** film-thickness. Many characterization techniques are common to those used for bulk-silicon and diffused-silicon-layers, and these are discussed elsewhere in the book.

17.6.1 Optical Inspection of Epi-Film Surfaces

Epitaxial-layers are inspected under UV-light either visually (with an optical-microscope), or with a surface-scanning, laser-based, defect-counter. Visual inspection can spot slip-lines, haze, pits, particles, scratches, and spikes. Microscopic evaluation at low-magnification (75–200X) can reveal stacking-faults and pyramidal-defects. Automated laser-scanners (which detect light-scattering centers) can identify, map, and quantify defects in epitaxial-layers.

In some cases crystallographic-defects are too small to be seen even with a microscope. To make them visible, they must be *decorated*. This is done by immersing the epi-surface in a selective-etching solution. These contain HF, an oxidizing-acid (e.g., HNO_3), and acetic-acid. By preferentially-etching the silicon around the defect, it becomes enlarged, making it easier to observe by optical-microscopy.

17.6.2 Electrical Characterization

The two most important electrical-characteristics of epi-layers are their *film-resistivity* and *doping-concentration-profile*. Producing films with the specified resistivity is done by controlling dopant-gas concentrations during deposition. However, varia-

tions in dopant-incorporation and autodoping may cause deviations from the specified-values. Thus, deposited epi-layers must be monitored on a routine basis. *Film-resistivity* is determined from 4-point-probe measurements that yield sheet-resistivity, and these are performed on monitor-wafers (see Chap. 7). *Doping-profiles* are measured using spreading-resistance (SR), or secondary-ion mass-spectroscopy (SIMS), as described in Chaps. 11 and 24.

17.6.3 Epitaxial Film-Thickness Measurements

Thickness and thickness-uniformity are additional important properties of epitaxial-films that must be accurately measured and controlled. Epitaxial thickness-measurements fall into two categories, namely *destructive* and *non-destructive*. Destructive-methods include such junction-depth techniques as *angle-lap-and-stain*, and details are given in Chap. 11. The most common non-destructive method is *infrared reflectance*, as discussed in the next section.

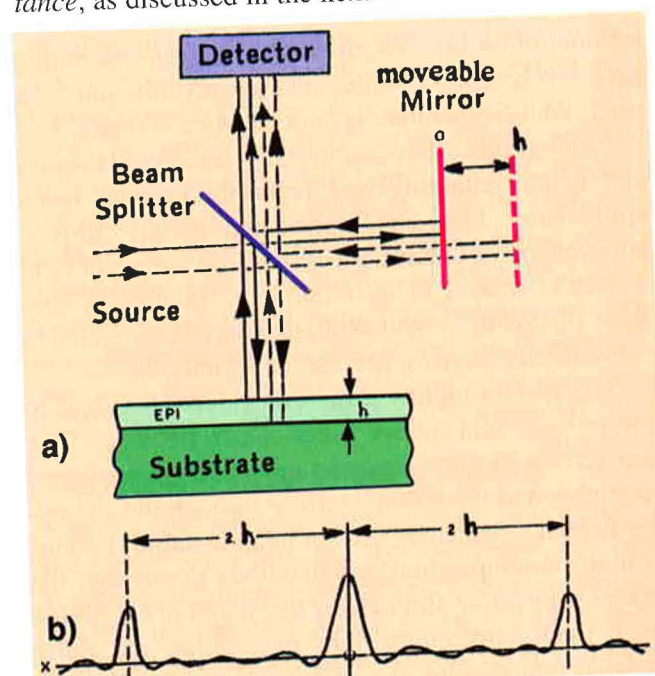


Fig. 17-15 Schematic representation of interferometric measurement of epitaxial-layer-thickness. (a) Interferometer showing path-lengths. (b) Interferogram showing a coherence peak and side-bursts.

17.6.4 Infrared-Reflectance Techniques

When electromagnetic-radiation (particularly in the infrared [IR] range) is incident upon a lightly-doped epitaxial-film on a heavily-doped Si-substrate, the following phenomenon takes place (Fig. 17-15). The incoming IR-light is partially-reflected from the air/film surface and the rest is transmitted through the film (where it strikes the surface of the heavily-doped substrate). The buried-surface reflects this light, and the reflected-beam combines with the radiation reflected from the exposed air/film-surface. The combined beams produce an interference-condition. As the wavelength of the IR-beam is varied, intensity-variations occur in the reflected-signal (depending on the wavelength of incident radiation). These can be correlated to the thickness of the film.

The IR-reflectance-technique is especially effective for lightly-doped epi-layers on heavily-doped substrates - which is exactly the film-structure encountered in silicon ICs. Lightly-doped epi-layers are relatively transparent to infrared-light having wavelengths from 2.5 to $50\text{-}\mu\text{m}$. Accordingly, this is the range of the spectrum typically used in the IR-reflectance-measurement-technique. The heavily-doped substrate behaves as a reflective-surface for radiation in this wavelength-range.

Fourier-transform infrared-spectroscopy (FTIR), is another more sophisticated (and more accurate) non-destructive technique for measuring the thickness of epitaxial-films. More information about it can be found in Ref. 1.

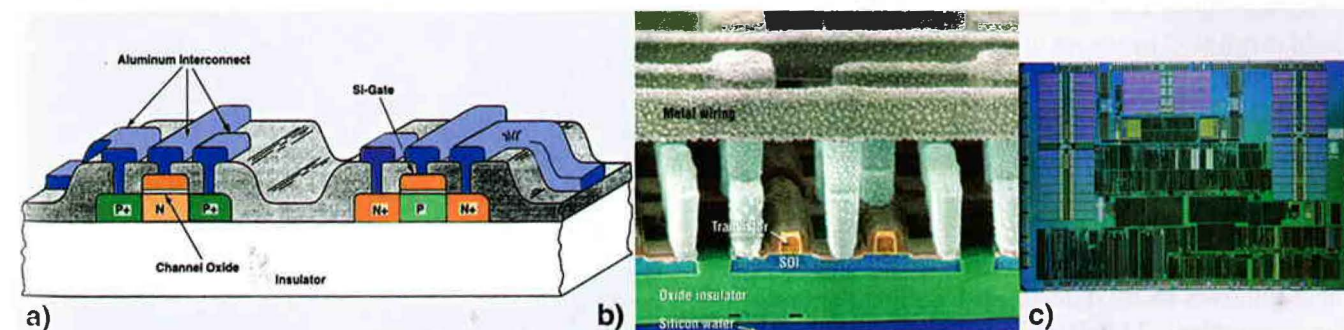


Fig. 17-16 (a) Schematic drawing of a CMOS structure built on an SOI-wafer. (b) SEM photograph of an SOI-IC. (c) Photograph of an SOI-IC. Courtesy of IBM.

17.7 SILICON-ON-INSULATOR TECHNOLOGY (SOI)

Silicon-on-insulator (SOI) circuits consist of ICs made from single-device islands, isolated from the substrate (and each other) by a dielectric region. Each island contains a single transistor. Figure 17-16a is a schematic depiction of MOSFETs fabricated on an SOI wafer. Note that a *buried-oxide (BOX)* beneath the device provides *vertical-isolation*, and the trench-oxide provides *lateral-isolation*. Since the trench-oxide extends all the way through the silicon device layer atop the BOX (and a thermal-oxide exists on the wafer top-surface), dielectric-material continuously surrounds each MOSFET on all its sides.

SOI-technology offers a number of significant advantages over bulk-CMOS technology, including: **1)** SOI-devices exhibit less parasitic-capacitance compared to bulk-Si devices. This reduces power-consumption or gives faster-performance; **2)** SOI-ICs have better immunity against radiation-induced failures, making them useful for space-applications; **3)** CMOS-SOI circuits do not undergo latchup; and **4)** SOI circuits can be manufactured with a fewer number of steps (up to 30% less). On the other hand, SOI-wafers are more costly and may have more defects than either bulk-silicon, or epi-silicon wafers.

SOI technology was first developed in the 1960's, but its early use was restricted to military-applications. However, as the need for higher-speed, lower-power-consumption, and cheaper fabrication-costs continued to drive the industry, chip manufacturers have recently pursued SOI as a technology that may

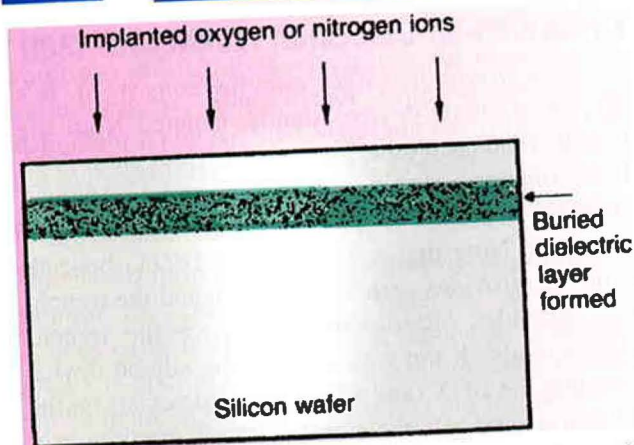


Fig. 17-17 Implanted oxygen-ion process for the formation of a SIMOX wafer.

help meet these goals (Figs. 17-16b & c).

Currently there are two main techniques for fabricating SOI-wafers: 1) *Separation by IMplanting OXYgen (SIMOX)*; and 2) *wafer-bonding (WB)*.^{2,10}

17.7.1 Separation by IMplanting OXYgen (SIMOX)

Separation by IMplanting OXYgen (SIMOX) is the name of a technique that produces SOI-wafers by implanting a very-high dose of oxygen atoms into silicon to produce subsurface-layers of silicon-dioxide. Figure 17-17 shows a schematic of how such SIMOX buried-oxide-layers are fabricated:

1. A bare silicon-wafer is subjected to a high dose ($\sim 2 \times 10^{18}/\text{cm}^2$) oxygen (O^+) implant-step. The implant-energy (150–300-keV) locates the peak of the implant 0.3–0.5-microns beneath the silicon-surface. During the implant the wafers are held at $>600^\circ\text{C}$ to ensure that the silicon maintains its crystallinity.

2. The wafers are then given a post-implant anneal in N_2 for 3–5-hours at a very-high temperature ($1300\text{--}1350^\circ\text{C}$). This causes a continuous *buried-oxide* (BOX) layer of silicon-dioxide to be formed near the peak of the implantation. It also removes many defects (dislocations) created by the implant. This BOX-layer is about $0.5\text{-}\mu\text{m}$ thick, and its depth is set by the location of the

3. If devices in the IC require a thicker Si-surface-layer than can be achieved with the depth of the ion-implanted oxygen, an epitaxial-Si layer can be deposited to provide this additional thickness.

SIMOX technology also has several shortcomings. First, fabricating SIMOX-wafers requires very-high doses of oxygen. Thus, long implantation-times are needed. Second, the implant-step may contaminate the wafer with transition metals. Such metals reduce the minority-carrier-lifetime of the devices. Third, despite the high-temperature anneal, the surface-silicon may still have a high-density of dislocation defects. Their presence can degrade gate-oxide integrity and increase junction-leakage. Finally, SIMOX-wafers are more expensive than bulk-wafers, although the difference in cost is expected to decrease with the growth in popularity of SIMOX.

The recent-introduction of SIMOX-dedicated oxygen-ion-implanters from IBIS Technology and

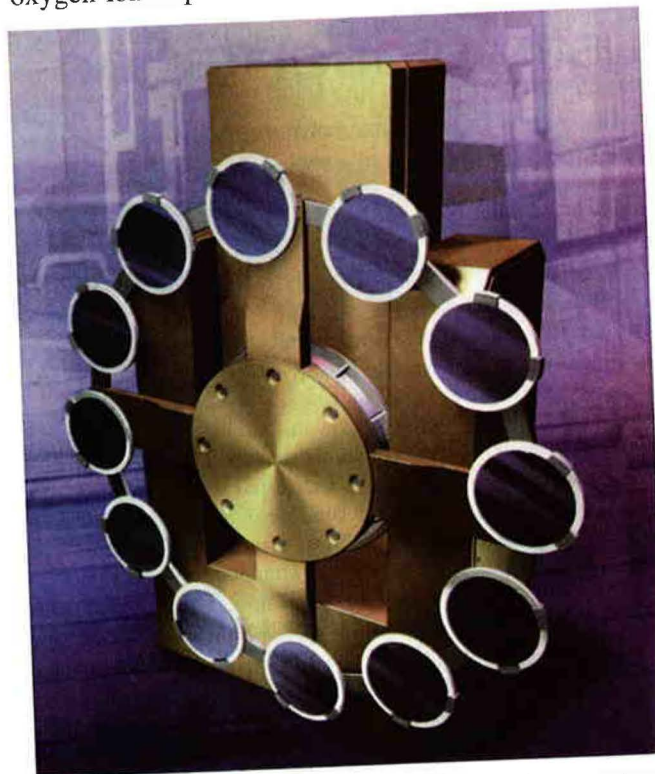


Fig. 17-18 Photograph of a SIMOX implanter wheel. Courtesy of Hitachi.

Hitachi have reduced the severity of these problems (Fig. 17-18). Such machines offer adequate throughput and acceptably low-levels of metallic-contamination. SIMOX materials have been used to build excellent-quality CMOS and bipolar ULSI-circuits.

17.7.2 Wafer-Bonding (Smart Cut)

Another popular technology for producing SOI wafers is *wafer-bonding*, in which two oxidized Si-wafers (or one-oxidized and one-bare wafer) are fused together, face-to-face, through a furnace process (Fig. 17-19). Wafer bonding forms BOX-layers much thicker than are possible with SIMOX (up to $50\text{-}\mu\text{m}$ thick).

A method of wafer-bonding that has been commercialized by SOITEC is called Smart Cut.[®] It allows the sacrificial wafer to be reused and only one wafer is required to make a bonded SOI-substrate. This one-wafer technology is termed Unibond.[®] Figure 17-20 shows how the process works. Two device-quality wafers (labeled A and B) start the process. Wafer-A is oxidized (to about $0.5\text{-}\mu\text{m}$) to form what will become the buried-oxide. Then wafer-A is ion-implanted with H^+ to about $0.2\text{-}\mu\text{m}$ below the oxide-surface. The depth of the H ion-implantation determines the thickness of silicon above the BOX. Wafers-A and B are now cleaned and low-temperature bonded face-to-face. The bonded-wafers are next annealed (at $\leq 600^\circ\text{C}$). During this anneal the implanted-hydrogen forms a gas, and wafer-A delaminates at the peak of the implanted-hydrogen. Wafer-B, which now has a BOX-layer, becomes the SOI-wafer, while

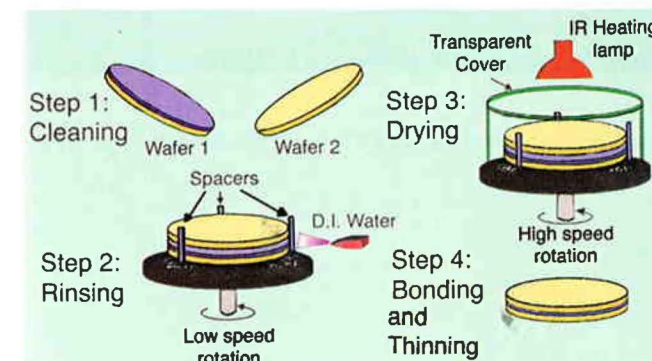


Fig. 17-19 Schematic of the wafer-bonding process.

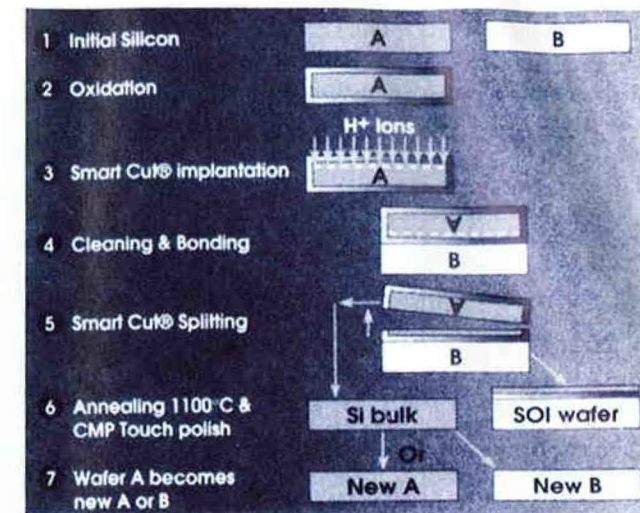


Fig. 17-20 Process flow for fabricating Smart Cut[®] wafers. Courtesy of SOITEC SA.

wafer-A becomes the sacrificial-wafer. Both wafers are annealed at 1100°C to remove defects. Wafer-A, which is now a fraction of a micron thinner than it was before the start of the process, is used as wafer-B when the process starts over. The method has been used to prepare commercially-available 200-mm, SOI-wafers with a silicon-thickness above the BOX of $0.2\text{-}\mu\text{m}$, and a uniformity of better than 5%.

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PROBLEMS

1. Describe what *epitaxy* is. What is the main advantage of epitaxy over other processes that makes it a process useful for some IC applications?
2. What is the role of epitaxy in: (a) bipolar transistor IC technology; and (b) CMOS IC technology? What is main benefit obtained by using a lightly-doped epi-layer on a heavily-doped substrate for a CMOS circuit?
3. List three silicon precursors used for depositing VPE Si-epitaxy layers.
4. List three dopant-gases used for intentionally adding dopants to an epitaxial layer. What are the safety-hazards associated with the use of these gases?
5. Why is epitaxy done in cold-wall reactors? (See p. 275 for a definition of this term.)
6. What are the advantages of *single-wafer* epitaxy reactors over *batch* epitaxy reactors?
7. Define the terms *outdiffusion* and *autodoping*. What measures are taken to suppress autodoping? Why is a highly-abrupt substrate/epitaxy interface difficult to obtain.
8. Referring to Fig. 17-8, determine the mole-fraction of SiCl_4 that will result in the maximum film growth-rate of a silicon-film. Why is epitaxial deposition not carried out under this condition?
9. Explain why the growth-curve shown in Fig. 17-8 becomes negative.
10. The intrinsic-diffusivity of boron in Si (see Appendix B) can be expressed as $D = 0.76 \exp(-3.46-$

$\text{eV/kT})$. Using this expression, calculate the minimum growth-rate that is required when a Si-epi film is grown on a heavily B-doped Si substrate for 20-min at 1200°C . Discuss why lower growth-temperatures must be used in order to obtain Si epi-layers that are less than $1\text{-}\mu\text{m}$ thick.

11. List some circuit applications that would benefit from using an SOI technology to fabricate them.

12. A high-energy (1-MeV) implanter is used to implant oxygen below the silicon-surface to form a buried-oxide layer (SIMOX process). Assume the desired buried-oxide layer is to be $0.2\text{-}\mu\text{m}$ thick: (a) What is the oxygen-dose that must be implanted into the silicon to form this layer? List the assumptions you made in determining this value. (b) What beam-current is required if a 200-mm wafer is to be implanted with this dose in 15-min? (c) How much power is being supplied to the ion beam? Discuss what effects this implantation may have on the wafer.



Servicing a 300-mm etch tool. Photograph courtesy of Applied Materials, Inc.

LITHOGRAPHY I: PHOTORESIST MATERIALS AND PROCESS TECHNOLOGY

CHAPTER CONTENTS

- 18.1 PHOTORESISTS
- 18.2 RESIST MATERIAL PARAMETERS
- 18.3 OPTICAL RESIST TYPES
- 18.4 PHOTORESIST PROCESSING
 - Dehydration Baking and Priming
 - Resist Processing: Spin Coating
 - Soft-Bake
 - Exposure
 - Development
 - After-Develop Inspection
 - Post-Development-Bake
- 18.5 RESIST PROCESSING SYSTEMS

In the Beginning, God said,

$$\begin{aligned} \nabla \cdot E &= \frac{\rho}{\epsilon_0} & \nabla \times E &= -\frac{\partial B}{\partial t} \\ \nabla \cdot B &= 0 & c^2 \nabla \times B &= \frac{j}{\epsilon_0} + \frac{\partial E}{\partial t} \end{aligned}$$

Exposing a photoresist film on a wafer.
Courtesy of ASML.

The patterns that define structures in ICs are created by *lithographic-processes*. A layer of photoresist-material is first spin-coated onto the wafer-substrate. Next, the resist is selectively-exposed to some form of radiation, such as ultraviolet-light or electrons. An *exposure-tool* and *mask* are used to produce the desired selective-exposure. The patterns in the resist are created when the wafer undergoes a subsequent “development” step. The areas of resist that remain after development serve to protect the substrate-regions which they cover. Locations from which resist has been removed can be subjected to a variety subtractive or additive processes that transfer the pattern onto the substrate-surface. (The most common of these are *etching* and *ion-implantation*.) An advanced-IC can have 25 or more of such masking-layers. Approximately one-third of the total cost of semiconductor-manufacturing involves lithographic-processing.

Three chapters of this text are devoted to the details of this critical technology. The first concerns the properties of *photoresist-materials* and the *resist-processing-technology* utilized in ULSI-fabrication. The discussion is restricted to resists exposed by optical (e.g., UV and DUV) radiation. The second deals with the *tools used to expose the resist* (*optical-aligning-equipment*). In the third, *photomasks* as well as alternatives to optical-lithography (including *EUV* and *e-beam patterning-technology*) are described. Note that more details about resist-processing can be found in Refs. 1 - 4, listed at the end of the chapter.

18.1 PHOTORESISTS

Photoresists have been used in the printing-industry to make pre-coated lithographic printing-plates for more than a century. In the 1920s, photoresists were introduced to the printed-circuit-board industry. The semiconductor-industry adopted this technique for wafer-fabrication in the 1950s. By 1991 the semiconductor-industry was consuming about 2500- tons of photoresist per year, which represented sales of around \$220 million. The selling price of photoresist in the late 1990’s was about \$900/gallon.