

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Samsung Electronics Co., Ltd.,
Petitioner,

v.

SiOnyx, LLC,
Patent Owner.

Case No. IPR2024-01430
Patent No. 11,069,737

**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO.
11,069,737 UNDER 35 U.S.C. §§ 311–319 AND 37 C.F.R. § 42.100 *et seq.***

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List of Exhibits

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1001	U.S. Patent No. 11,069,737 (the “’737 patent”)
1002	File History for U.S. Patent No. 11,069,737
1003	Provisional Application No. 61/841,326
1004	Declaration of Dr. Michael Lebby
1005	Curriculum Vitae of Dr. Michael Lebby
1006	U.S. Patent Application Publication No. 2012/0068289 (Alie)
1007	U.S. Patent Application Publication No. 2006/0081900 (Baggenstoss)
1008	International Publication No. WO 2012/122572 (Jiang)
1009	U.S. Patent Application Publication No. 2012/0313204 (Haddad204)
1010	U.S. Patent Application Publication No. 2010/0006969 (Park)
1011	U.S. Patent No. 7,928,389 (Yap)
1012	U.S. Patent Application Publication No. 2011/0227138 (Haddad138)
1013	Samsung’s Proposed Constructions, Inv. No. 337-TA-1403 (Aug. 27, 2024)
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1015	Email from N. Subhedar re: Claim Construction M&C Follow-Up (Sept. 8, 2024)
1016	U.S. Patent No. 8,680,591 (Haddad138 Issued Patent)
1017	U.S. Patent No. 9,496,308 (Haddad204 Issued Patent)
1018	The Authoritative Dictionary of IEEE Standard Terms (7th ed. 2000)
1019	Stephen Y. Chou et al., <i>Nanoimprint Lithography</i> , J. Vac. Sci. Technol. B 14(6), 4129-33 (1996)
1020	Gary S. May & Simon M. Sze, <i>Fundamentals of Semiconductor Fabrication</i> (2003)
1021	Provisional Application No. 61/311,004 (Haddad138-Provisional004)
1022	Provisional Application No. 61/243,434 (Haddad138-Provisional434)
1023	Provisional Application No. 61/311,107 (Haddad138-Provisional107)
1024	U.S. Patent Application Publication No. 2012/0146172 (Carey)
1025	U.S. Patent No. 7,442,629 (Mazur)
1026	U. Gösele & Q.-Y. Tong, <i>Semiconductor Wafer Bonding</i> (1998)
1027	U.S. Patent Application Publication No. 2011/0304003 (Tanida)
1028	S. Wolf, <i>Microchip Manufacturing</i> (2004)
1029	<i>Encyclopedia of Physical Science and Technology</i> (3rd ed. 2002)

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Exhibit	Description
1030	Christoph Posch, <i>Detectors, Pixels, and Signal Processing, in SMART CAMERAS</i> (Ahmed Nabil Belbachir ed., 2010)

I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner”) petitions for *inter partes* review seeking cancellation of claims 1-55 (the “Challenged Claims”) of U.S. Patent No. 11,069,737 (Ex. 1001, the “’737 patent”).

The ’737 patent purports to improve upon traditional photosensitive imager devices by adding a textured layer. Figure 2 depicts an embodiment:

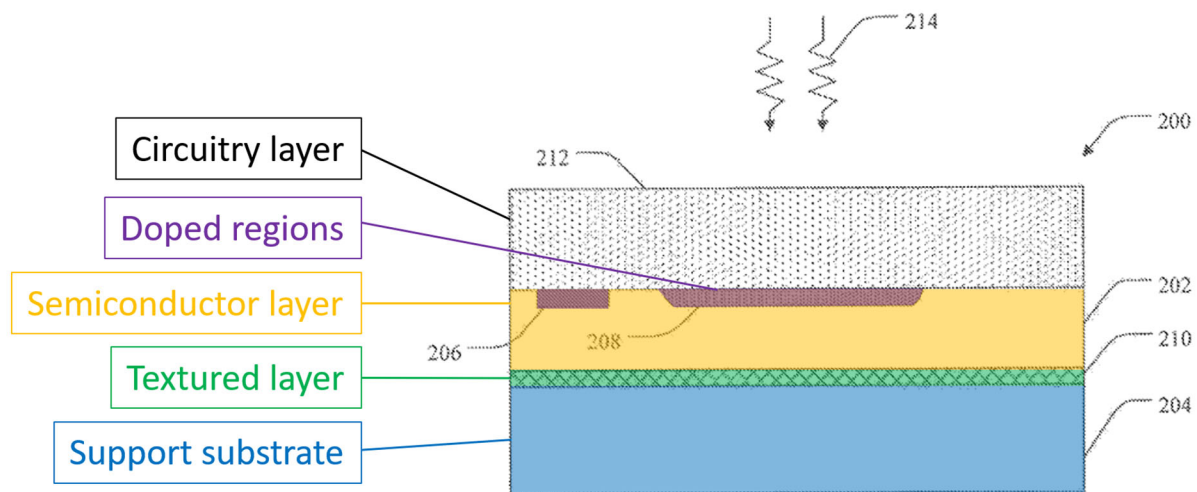


FIG. 2

’737 patent, Fig. 2 (annotated).

Light 214 is incident on a circuitry layer 212 and travels to a semiconductor layer 202. ’737 patent, 6:41-44. The semiconductor layer 202 has doped regions 206 and 208 that form a junction for sensing light. ’737 patent, 6:33-37. On the bottom side of the semiconductor layer is a textured layer containing surface features. ’737 patent, 6:37-39. The textured layer allegedly functions to “diffuse light, to redirect light, and to thus increase the quantum efficiency.” ’737 patent, 9:21-23. The

independent claims of the '737 patent require a photosensitive imager device with a textured region or a method of making one.

A photosensitive imager device with a textured region and a method of making one were not novel. Indeed, SiOnyx, LLC (“SiOnyx” or “Patent Owner”) itself, among others, published patent applications showing the same before the priority date. For example, Figure 5 of Alie depicts a photodetector with a textured region. Alie, [0096]; *see also* Alie, [0006].

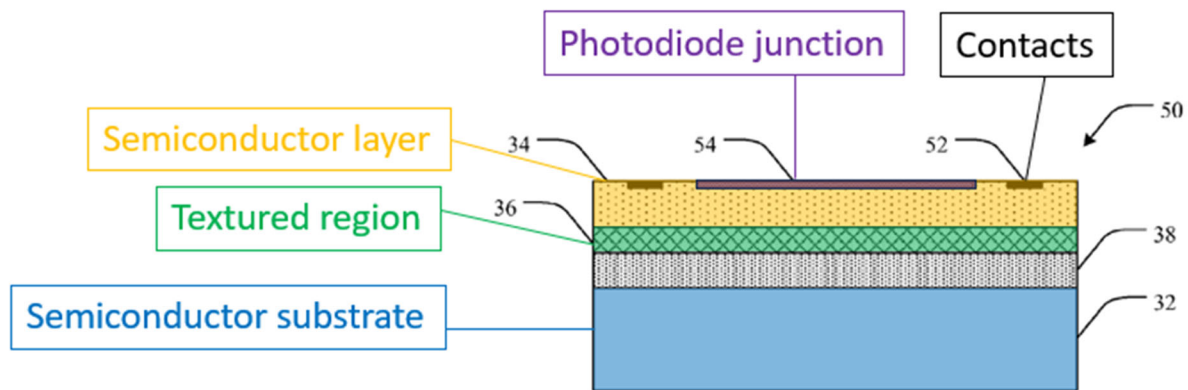


FIG. 5

Alie, Fig. 5 (annotated).

Like the textured region of the '737 patent, Alie’s “textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and/or to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Alie, [0068]. Grounds 1 to 5 show how Alie alone or in combination with other references anticipates or renders obvious claims 1-55.

II. STANDING, MANDATORY NOTICES, AND FEE AUTHORIZATION

A. Grounds for Standing

Pursuant to 37 C.F.R. § 42.104(a), Petitioner certifies that the '737 patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the '737 patent on the grounds identified in this petition.

B. Real Parties-in-Interest

The real parties-in-interest are Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.

C. Related Matters

Petitioner identifies the following related matters.

- *Sensors with Pixels and Products Containing the Same*, Inv. No. 337-TA-1403 (ITC) (the "Related Case")
- *SiOnyx, LLC v. Samsung Electronics, Co., Ltd.*, 2:24-cv-00291 (E.D. Tex.)

D. Counsel Information

Petitioner designates the following counsel:

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Pursuant to 37 C.F.R. § 42.10 (b), Petitioner has filed a power of attorney with the above designation of counsel.

E. Service Information

Service information is provided in the designation of counsel above. Petitioner consents to service of all documents via electronic mail at the email addresses above and at Samsung-SiOnyx-IPR-Cov@cov.com.

F. Payment of Fees Under 37 C.F.R. §42.103

This petition is accompanied by the fees set forth in 37 C.F.R. § 42.15(a). Please charge or credit Deposit Account No. 60-3160 with any shortage or overpayment of fees associated with this petition and any other fees incurred by Petitioner.

III. SUMMARY OF CHALLENGE

- **Ground 1:** Claims 1-11, 13-42, and 44-55 are anticipated, or at a minimum obvious, based on Alie.

- **Ground 2:** Claims 1, 12-13, 21, 24, 30, 43-44, 51, and 54 are obvious based on Alie and Baggenstoss.
- **Ground 3:** Claims 16, 32-42, and 44-55 are obvious based on Alie and Jiang.
- **Ground 4:** Claims 25 and 55 are obvious based on Alie and Haddad204.
- **Ground 5:** Claims 25 and 55 are obvious based on Alie and Park.

The application for the '737 patent was filed on July 8, 2019 and claims priority to a provisional application filed on June 29, 2013. Each of the asserted references is available as prior art under 35 U.S.C. § 102 (AIA),¹ as shown in the following table.

Exhibit	Reference	Date(s)	Availability as Prior Art
1006	U.S. Patent Application Publication No. 2012/0068289 (Alie)	March 22, 2012 (published)	§ 102(a)(1) & (2)
1007	U.S. Patent Application Publication No. 2006/0081900 (Baggenstoss)	April 20, 2006 (published)	§ 102(a)(1) & (2)
1008	International Publication No. WO 2012/122572 (Jiang)	September 13, 2012 (published)	§ 102(a)(1)

¹ Because both the application and the provisional application for the '737 patent were filed after March 16, 2013, the AIA conditions for patentability apply.

Exhibit	Reference	Date(s)	Availability as Prior Art
1009	U.S. Patent Application Publication No. 2012/0313204 (Haddad204)	December 13, 2012 (published)	§ 102(a)(1) & (2)
1010	U.S. Patent Application Publication No. 2010/0006969 (Park)	January 14, 2010 (published)	§ 102(a)(1) & (2)

IV. THE '737 PATENT

A. Overview of the '737 Patent

The '737 patent admits that silicon imaging devices were widely used in both front side illumination (FSI) and backside illumination (BSI) configurations. '737 patent, 1:18-30; *see also* Ex-1004 ¶¶41-43.

The '737 patent purports to improve upon traditional photosensitive imager devices by adding a textured layer. Figure 2 depicts an embodiment:

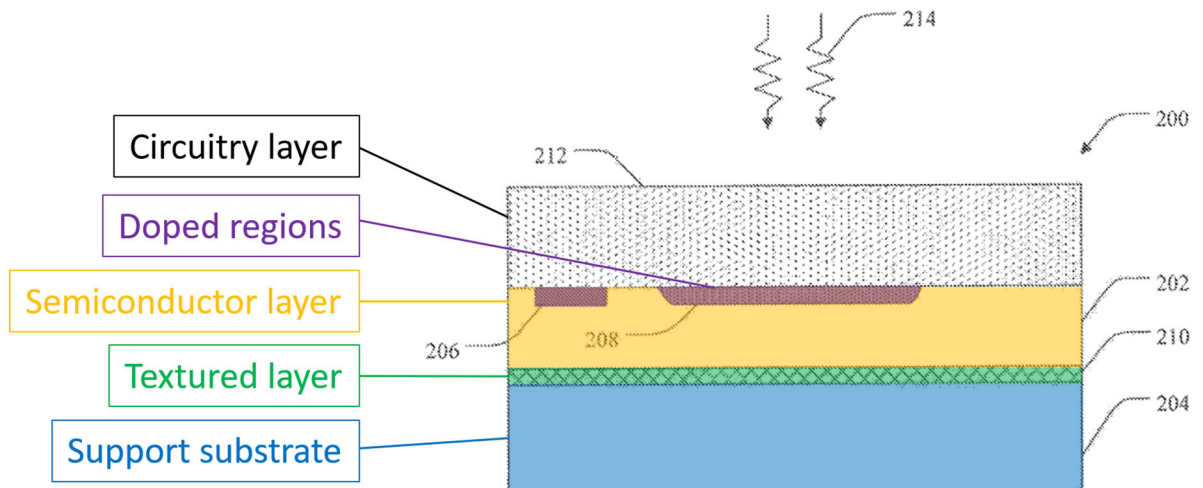


FIG. 2

'737 patent, Fig. 2 (annotated).

B. Prosecution History

The '737 patent was filed on July 8, 2019, claiming priority to Provisional Application No. 61/841,326, filed on June 29, 2013.

Following an office rejection, the applicant added the following limitation to claim 21 (issued claim 1): “wherein the surface features are arranged according to a pattern.” Ex-1002 at 86.

The applicant also added to claim 47 (issued claim 26) limitations regarding CMP processing. Ex-1002 at 88.

The applicant also added a new claim 56 (issued as claim 32). Ex-1002 at 89.

Following the applicant’s amendments, the examiner only rejected claims 80-83. Ex-1002 at 108. After the applicant cancelled those claims, Ex-1002 at 171, the examiner issued a notice of allowance, Ex-1002 at 173; *see also* Ex-1004 ¶¶44-48.

V. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art (“POSITA”) as of June 2013 would have had a Bachelor’s degree in engineering, physics, or a related or equivalent field, and two or more years of experience researching, developing, designing, and/or evaluating image sensors using photonics. Ex-1004 ¶50. A person with less or different education but more relevant practical experience, or vice versa, may also meet this standard. Ex-1004 ¶50.

VI. CLAIM CONSTRUCTION

In IPR proceedings, claims are construed in accordance with their “ordinary and customary meaning” in light of the specification. 37 C.F.R. § 42.100(b); *see Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005). In the Related Case, Petitioner and Patent Owner have proposed competing constructions for certain terms of the ’737 patent. *See* Ex-1013; Ex-1014; Ex-1015. For purposes of this petition, however, Petitioner does not believe that any specialized constructions are necessary.

VII. OVERVIEW OF THE PRIOR ART

A. Alie (Ex-1006)

Alie is prior art because it was published on March 22, 2012, which is more than one year before the ’737 patent’s provisional application filing date of June 29, 2013.

Alie was not listed in an information disclosure statement (IDS) and it was not discussed during prosecution.

Like the ’737 patent, Alie was assigned to SiOnyx. The ’737 patent refers to Alie for “[f]urther details regarding substrates, bonding, and various imager details,” incorporating Alie’s patent application by reference. ’737 patent, 7:18-21. Like the ’737 patent, Alie discloses a photodetector with a textured region. Alie, [0096], [0006].

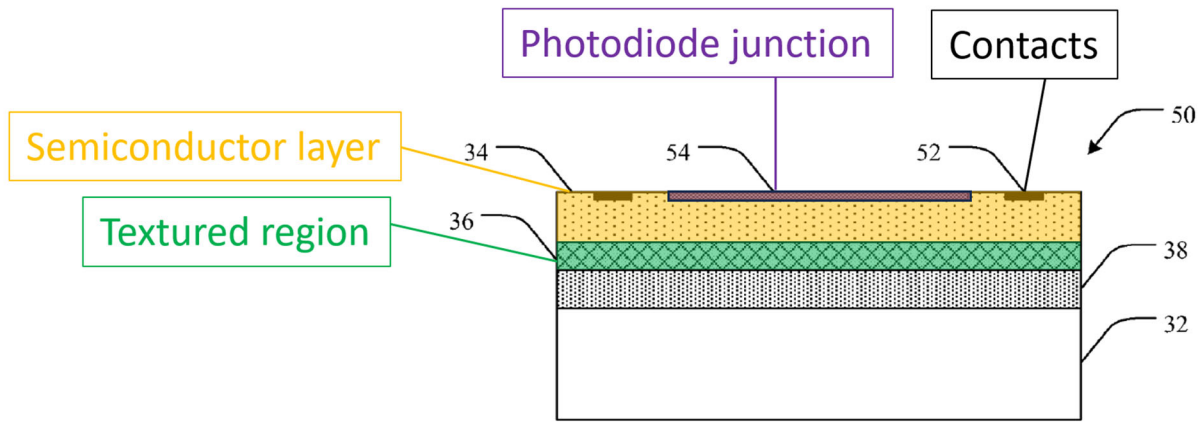


FIG. 5

Alie, Fig. 5 (annotated).

Alie discloses that “[t]he textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and/or to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.”

Alie, [0068]; *see also* Ex-1004 ¶¶55-59.

Like the '737 patent, Alie discloses that its devices can be front side illumination (FSI) or backside illumination (BSI) devices. Alie, [0053].

B. Baggenstoss (Ex-1007)

Baggenstoss is prior art because it was published on April 20, 2006, which is more than one year before the '737 patent's provisional application filing date of June 29, 2013.

Baggenstoss was not listed in an IDS and it was not discussed during prosecution. A parent application (of which Baggenstoss is a divisional) was listed

in an IDS along with over 1,000 other documents, but it was not discussed during prosecution.

Baggenstoss discloses a photodetector with a grated interface formed by trenches 144. Baggenstoss, [0031]-[0032], [0009].

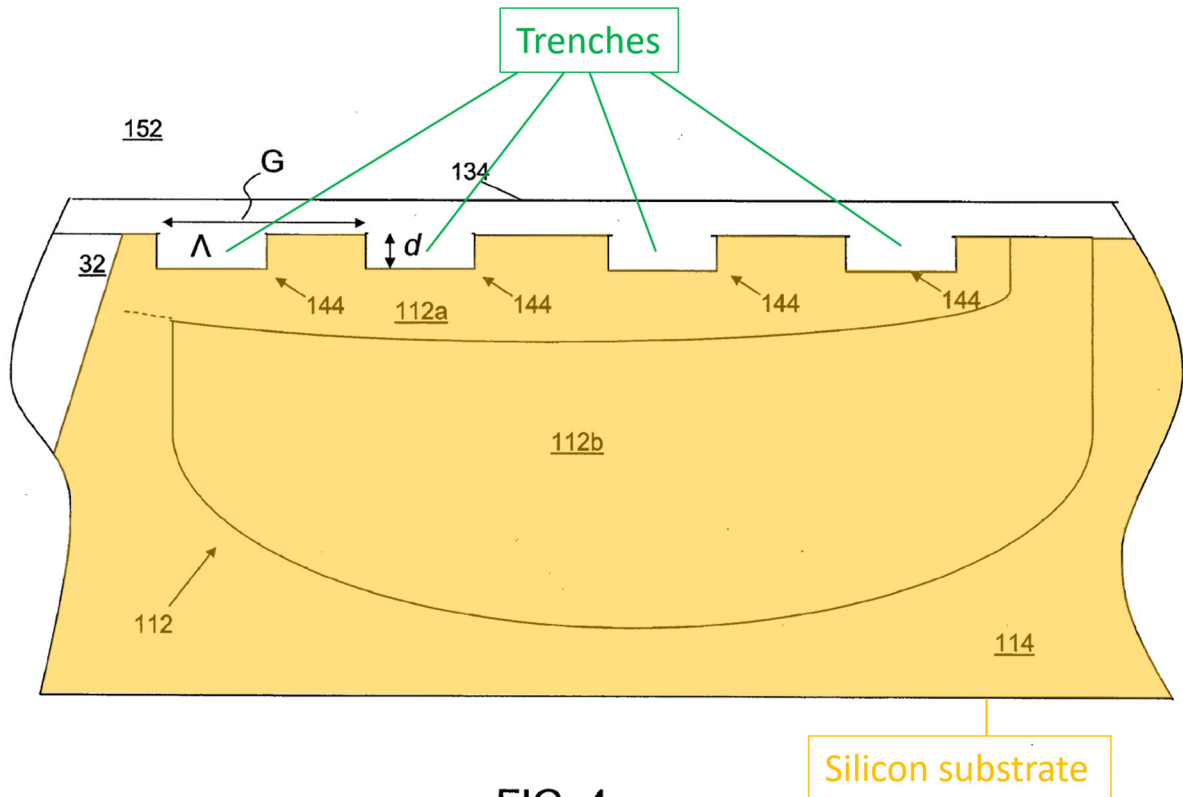


FIG. 4

Baggenstoss, Fig. 4 (annotated).

In another embodiment, Baggenstoss discloses a pixel cell with a “blazed (or step-wise)” gratings formed of trenches 244. Baggenstoss, [0042].

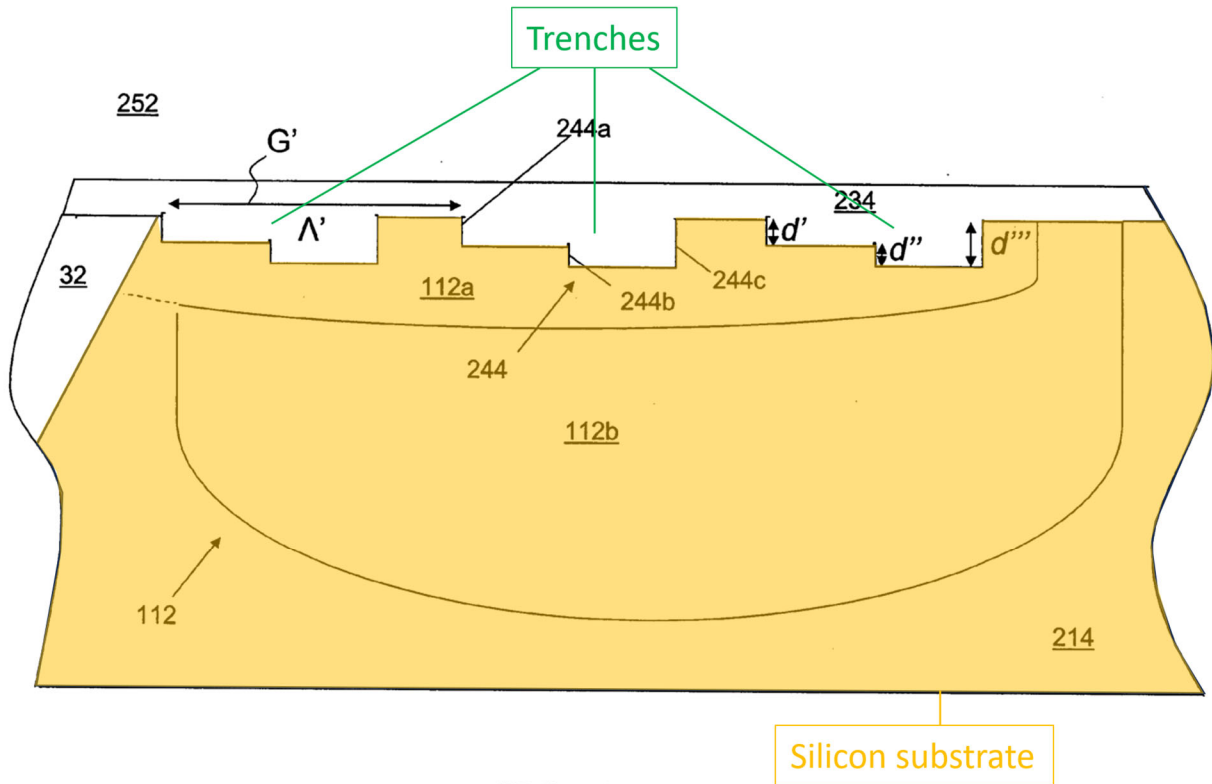


FIG. 11

Baggenstoss, Fig. 11 (annotated).

Baggenstoss teaches that its “grated interface [formed by trenches] allows a greater percentage of incident light to be captured, which is a vast improvement over the art.” Baggenstoss, [0014]; *see also* Ex-1004 ¶¶60-64.

C. Jiang (Ex-1008)

Jiang is prior art to all claims of the '737 patent because it was published on September 13, 2012, which is before the '737 patent's provisional application filing date of June 29, 2013.

Jiang is prior art to claims 16 and 32-55 of the '737 patent also because it was published on September 13, 2012, which is more than one year before the earliest

non-provisional application filing date of November 19, 2013 for the '737 patent family. Although the '737 patent's provisional application was filed on June 29, 2013, it did not support claims 16 and 32-55 because it lacked any disclosure of the device exhibiting a quantum efficiency of at least about 35% for electromagnetic radiation at a wavelength of about 940 nm, as required by these claimSs. Ex-1003.

Jiang was not listed in an IDS and it was not discussed during prosecution.

Like the '737 patent, Jiang was assigned to SiOnyx. The named inventors of the '737 patent, Homayoon Haddad and Jutao Jiang, are also joint inventors of Jiang. Like the '737 patent, Jiang discloses a photodetector with a textured region. Jiang, Abstract, 11:1-4.

Figure 15 of Jiang discloses that the quantum efficiency of an example device with a textured region is well over the claimed 35%, at around 70% for electromagnetic radiation at a wavelength of about 940 nm. Jiang, 1:32-35, 16:19-23; *see also* Ex-1004 ¶¶65-69.

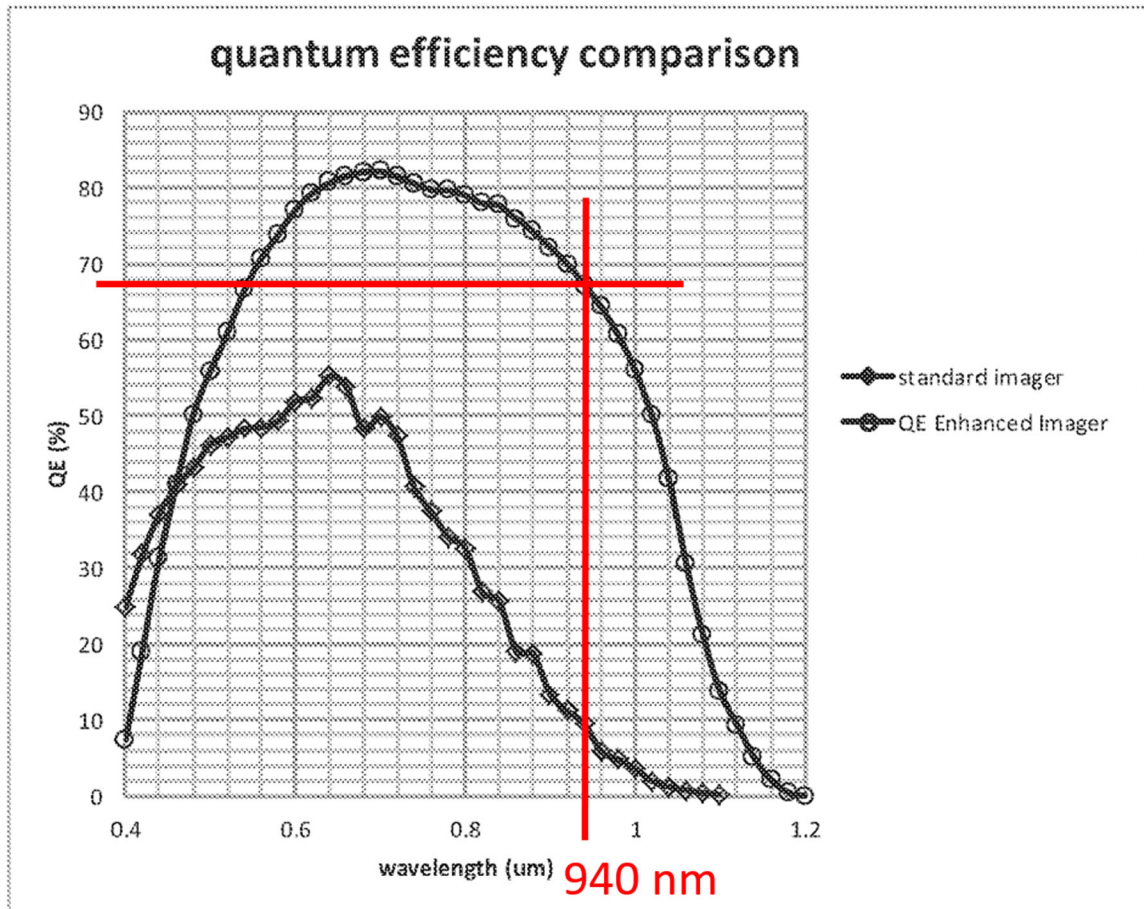


FIG. 15

Jiang, Fig. 15 (annotated).

D. Haddad204 (Ex-1009)

Haddad204 is prior art because it was published on December 13, 2012, which is before the '737 patent's provisional application filing date of June 29, 2013.

Although Haddad204 was listed in an IDS along with over 1,000 other documents, it was not discussed during prosecution.

Like the '737 patent, Haddad204 was assigned to SiOnyx. *See* Ex-1017. The named inventors of the '737 patent, Homayoon Haddad and Jutao Jiang, are also

joint inventors of Haddad204. Like the '737 patent, Haddad204 discloses a photodetector with a textured region including surface features. Haddad204, [0073], [0053]. In particular, Haddad204 discloses “a plurality of pillars of variable sizes ... arranged in a non-uniform array.” Haddad204, [0112]; *see also* Ex-1004 ¶¶70-72. Figure 9a shows a top view and Figure 9b shows a cross-sectional view of such “pillars etched into a semiconductor material.” Haddad204, [0112].

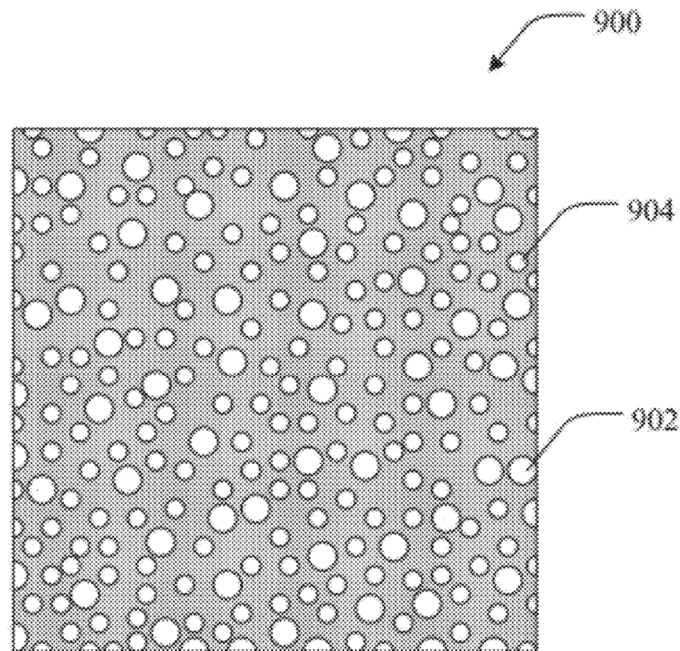


FIG. 9a

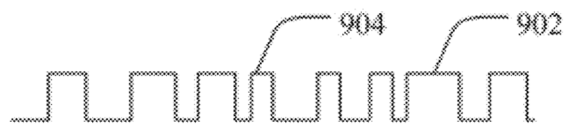


FIG. 9b

Haddad204, Figs. 9a-b.

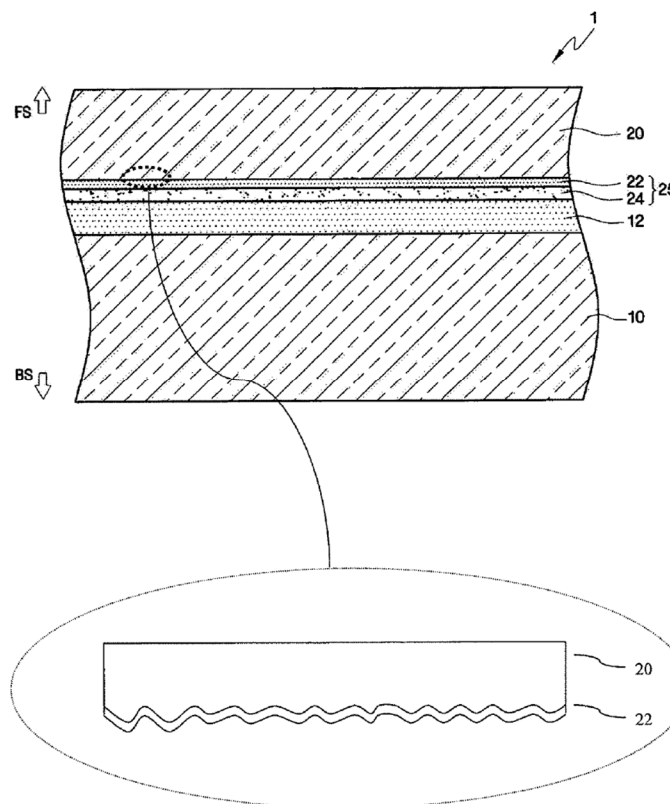
E. Park (Ex-1010)

Park is prior art because it was published on January 14, 2010, which is more than one year before the '737 patent's provisional application filing date of June 29, 2013.

Park was not listed in an IDS and it was not discussed during prosecution.

Like the '737 patent, Park discloses a photodetector with a textured region including surface features. Park, [0072] ("Referring to the inset in FIG. 1 ... reflections may also be reduced by processing the second substrate 20 to have an uneven surface facing the oxide layer 22."), Fig. 8D-2(f).

FIG. 1



Park, Fig. 1.

Park teaches that the uneven surface helps with absorbing incident light by reducing reflection. Park, [0072]; *see also* Ex-1004 ¶¶73-76.

VIII. APPLICATION OF PRIOR ART TO THE CHALLENGED CLAIMS

A. Ground 1: Claims 1-11, 13-42, and 44-55 Are Anticipated, or at a Minimum Obvious, Based on Alie

1. Claim 1

- a) **1[pre]: “A photosensitive imager device capable of detecting visible and infrared electromagnetic radiation, comprising:”**

Alie discloses this preamble under both Petitioner’s and Patent Owner’s proposed constructions in the Related Case. Ex-1004 ¶¶77-80.

In the Related Case, Petitioner proposed that the preamble is limiting and means, “An image sensor pixel capable of detecting visible and infrared electromagnetic radiation.” Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning, and that to the extent a construction is required, it means, “A device with multiple pixels arranged to capture an image from visible and/or infrared light.” Ex-1014, 3-4.

Alie discloses an image sensor pixel. Alie, [0096], Fig. 5; *see also* Ex-1004 ¶79. Alie also discloses a device with multiple pixels. Alie, [0006]; *see also* Ex-1004 ¶79. Alie’s device is capable of detecting visible and infrared electromagnetic radiation and are arranged to capture an image from visible and/or infrared light. Alie, [0006], [0052]-[0053], [0070]; *see also* Ex-1004 ¶79. Specifically, Alie

discloses that using a textured region in its device enhances detection of “the blue green part of the spectrum,” which corresponds to the claimed detection of visible electromagnetic radiation. Alie, [0053]; *see also* Ex-1004 ¶79. Alie also discloses that using a textured region enhances detection of “infrared,” which corresponds to the claimed detection of infrared electromagnetic radiation. Alie, [0070]; *see also* Ex-1004 ¶79.

- b) 1[a]: “a semiconductor layer having a light incident side and an opposed side, said semiconductor layer having multiple doped regions forming at least one junction,”

Alie discloses this limitation. Ex-1004 ¶¶81-85.

Figure 5 depicts a semiconductor photodiode with a semiconductor layer 34 having a top side and a bottom side. Alie, [0096]; *see also* Ex-1004 ¶82.

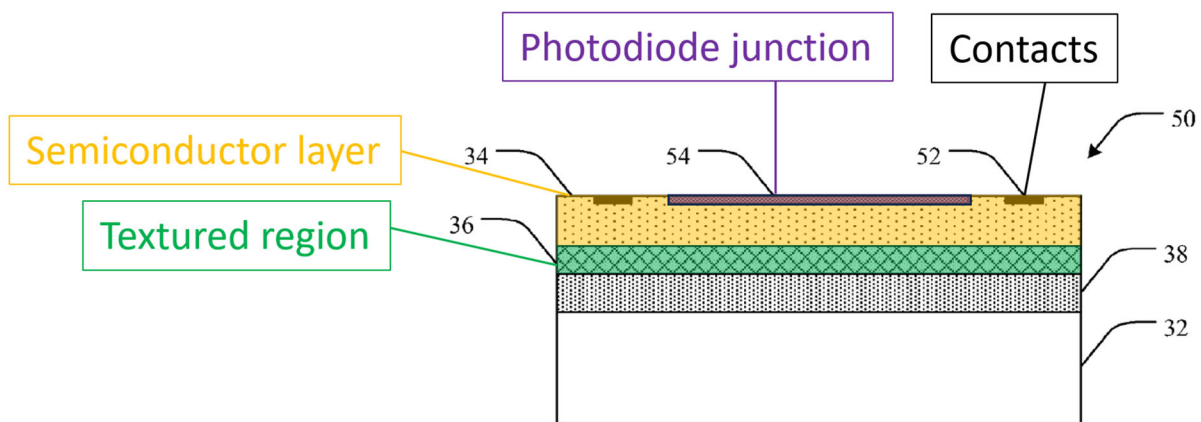


FIG. 5

Alie, Fig. 5 (annotated). On the top side of the semiconductor layer 34 are a photodiode junction 54 and contacts 52. Alie, [0096]. On the bottom side of the

semiconductor layer 34 is a textured region 36. Alie, [0096].

The top side and the bottom side correspond to the claimed light incident side and the opposed side. Ex-1004 ¶83. Which side corresponds to the claimed light incident side depends on whether the Figure 5 device is adapted for a front side illumination architecture or for a backside illumination architecture, as discussed below regarding claim 2. Ex-1004 ¶83.

Alie discloses “forming a p-i-n semiconductor material stack that creates a junction” (i.e., the claimed multiple doped regions forming at least one junction). Alie, [0066]; *see also* Alie, [0066]; Ex-1004 ¶84. Figure 5 depicts the photodiode junction 54 on the top side of the semiconductor layer 34.

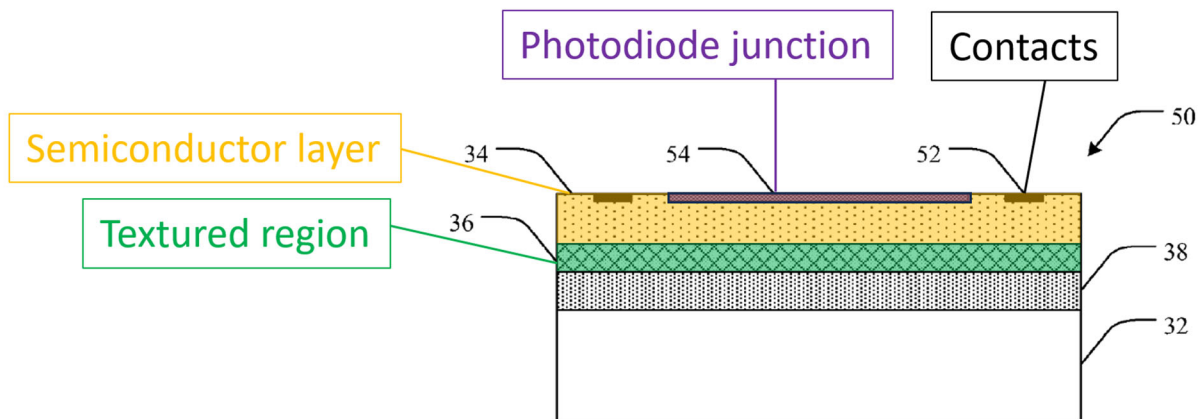


FIG. 5

Alie, Fig. 5 (annotated).

- c) **1[b]: “a textured region comprising a plurality of surface features configured to interact with incident electromagnetic radiation so as to increase the quantum efficiency of the device, wherein the surface features are arranged according to a pattern,”**

Alie discloses this limitation under Patent Owner’s proposed construction in the Related Case. Ex-1004 ¶¶86-90.

In the Related Case, Petitioner proposed that the term “a textured region comprising a plurality of surface features configured to interact with incident electromagnetic radiation so as to increase the quantum efficiency of the device” means “a region that includes features that diffuse electromagnetic radiation, redirect electromagnetic radiation, and/or absorb electromagnetic radiation, thus increasing the quantum efficiency of the device” and is indefinite. Ex-1015, 1. Patent Owner proposed that the term means “a region that includes features that diffuse, redirect, absorb, and/or increase the effective absorption length of the device.” Ex-1015, 2.

Figure 5 depicts a textured region 36. Alie, [0096]; *see also* Alie, [0070] (disclosing a textured region causing “multiple passes of incident electromagnetic radiation,” which “increases the effective absorption length,” which in turn, “increases the quantum efficiency”); Ex-1004 ¶88.

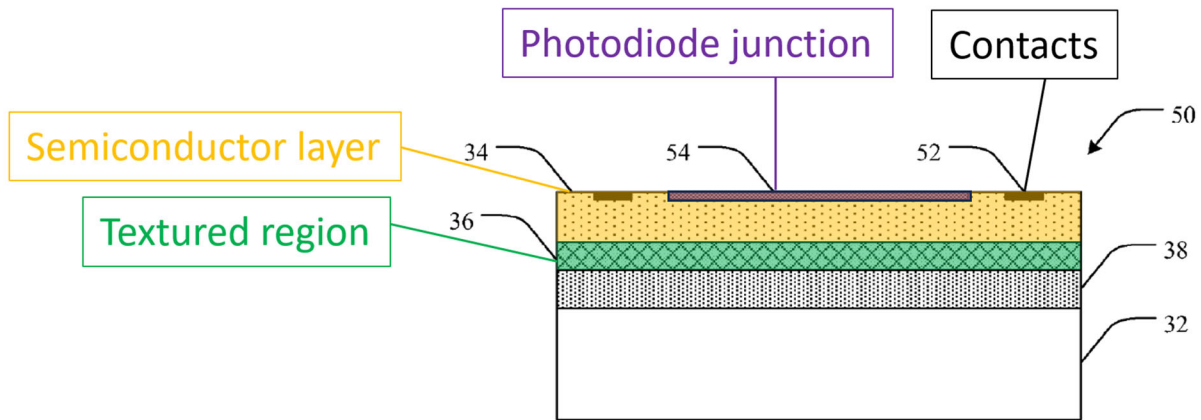


FIG. 5

Alie, Fig. 5 (annotated). Alie discloses that “[t]he textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and/or to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device.” Alie, [0068]. To that end, Alie discloses that its textured region can include “surface features” that “increase the effective absorption length of the device.” Alie, [0068].

In the Related Case, Petitioner proposed that the term “the surface features are arranged according to a pattern” is indefinite. Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning and that, to the extent a construction is required, it means “features coincident with at least one surface that are arranged in a repeating manner.” Ex-1014, 4. Alie discloses that the surface features of its textured region can be arranged according to a pattern under Patent Owner’s proposed construction in the Related Case. Alie, [0072]; *see also* Ex-1004 ¶89. Specifically, Alie discloses that “a substrate such as the semiconductor layer can be

textured and ***patterned*** across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch or a laser process to define a specific structure or ***pattern***.” Alie, [0072].² Alie also discloses that “[n]on-limiting examples of shapes and configurations of surface features include ... gratings,” Alie, [0068], which are features coincident with at least one surface that are arranged in a repeating manner, and are an example of a pattern provided by the provisional application for the ’737 patent. Ex-1003, 13:3-4 (“[A]s is shown in FIG. 5 for example, the shallow trench isolation can be a uniform ***grid pattern*** comprised of [trenches] that form ***a series of spaces and lines*** or pillars.”); *see also* Ex-1004 ¶89.

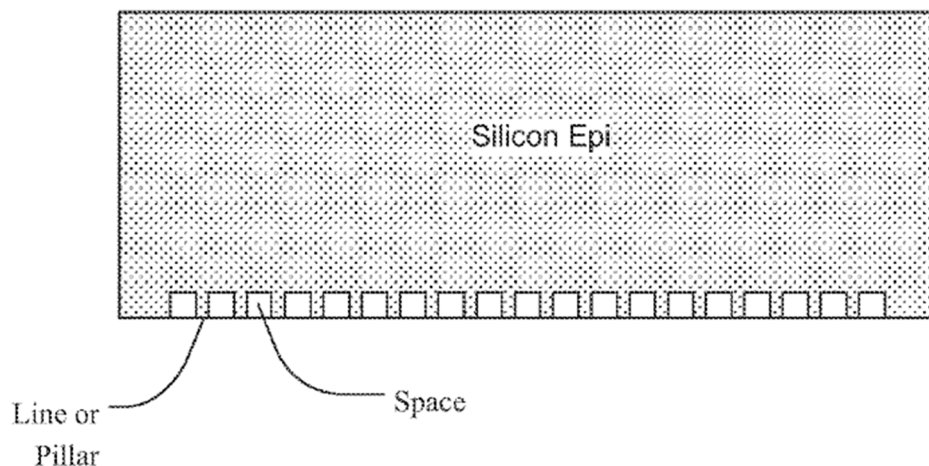


FIG. 5

Ex-1003, Fig. 5; *see also* ’737 patent, 9:14-20 (providing as examples of a pattern “a uniform or substantially uniform grid,” as well as “a non-uniform or a

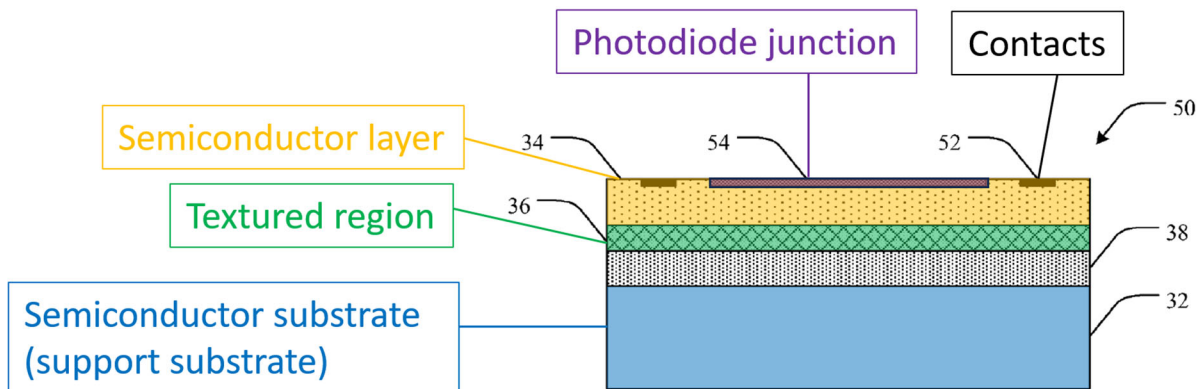
² All emphases in quotes have been added, unless otherwise stated.

substantially non-uniform pattern”).

d) 1[c]: “a support substrate coupled to said semiconductor layer, and”

Alie discloses this limitation. Ex-1004 ¶¶91-92.

Figure 5 depicts a semiconductor substrate 32 (i.e., the claimed support substrate) that is coupled to the semiconductor layer 34. Alie, [0089] (describing the same layers depicted in Figure 3 as “a semiconductor substrate 32 and a semiconductor layer 34 coupled to the semiconductor substrate”), [0096] (“It should be noted that all reference numbers in FIGS. 5 and 6 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided.”); *see also* Ex-1004 ¶92.

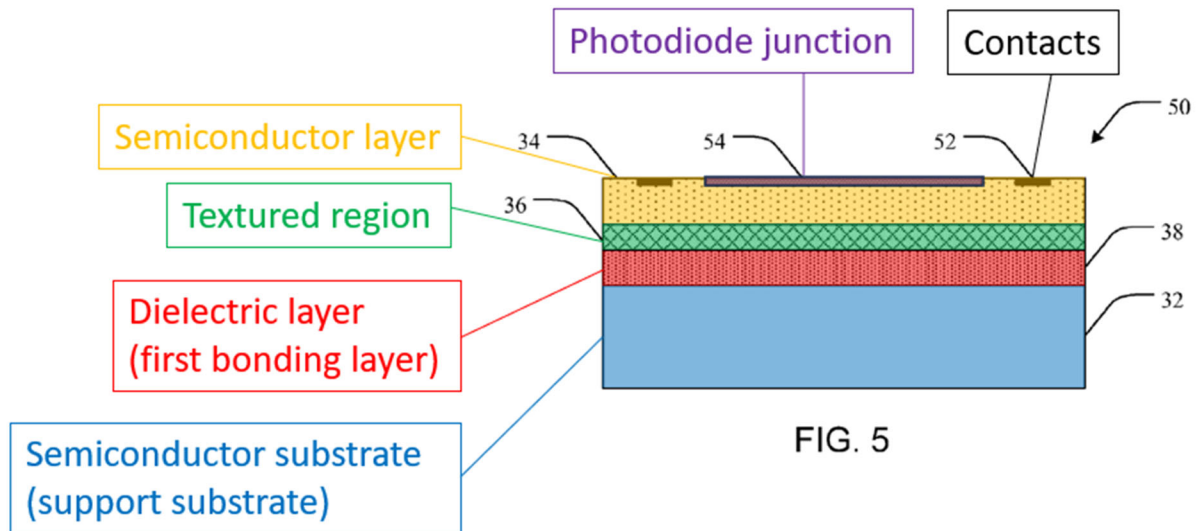


Alie, Fig. 5 (annotated).

e) 1[d]: “a first bonding layer disposed between the semiconductor layer and the support substrate.”

Alie discloses this limitation. Ex-1004 ¶¶93-94.

Figure 5 depicts a dielectric layer 38 (i.e., the claimed first bonding layer) disposed between the semiconductor layer 34 and the semiconductor substrate 32 (i.e., the claimed support substrate). Alie, [0089] (describing the same layers depicted in Figure 3 as “a semiconductor substrate 32 and a semiconductor layer 34 coupled to the semiconductor substrate” and a “dielectric layer 38 coupled between the semiconductor substrate and the semiconductor layer”); *see also* Ex-1004 ¶94.



Alie, Fig. 5 (annotated). The dielectric layer 38 corresponds to the claimed first bonding layer because it is used to “*wafer bond* the semiconductor layer to the semiconductor substrate.” Alie, [0055]; *see also* Alie, [0087]; Ex-1004 ¶94.

2. Claim 2

- a) **“The device of claim 1, wherein the textured region is located on the light incident side of the semiconductor layer.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶95-101.

As depicted in Figure 5, the textured region 36 is located on the bottom side of the semiconductor layer 34, i.e., the claimed light incident side of the semiconductor layer in a backside illuminated architecture. Alie, [0089], [0096]; *see also* Ex-1004 ¶96.

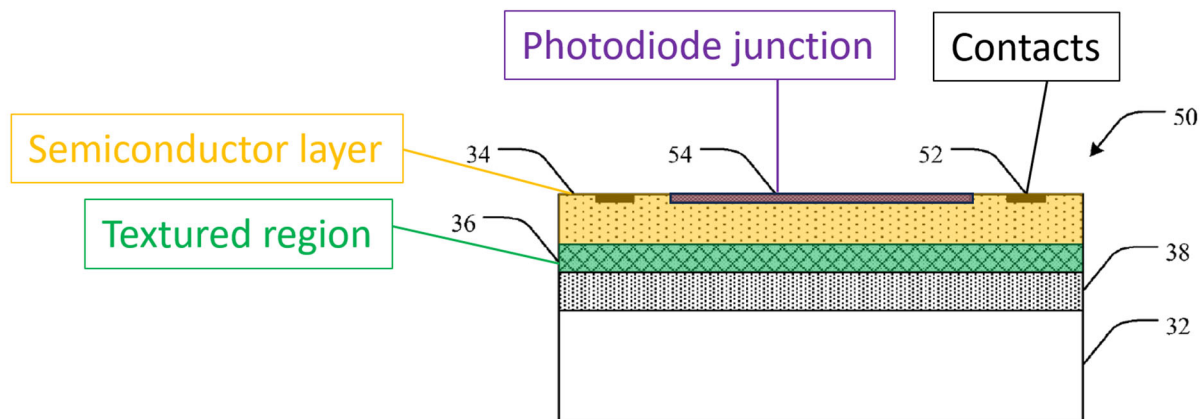


FIG. 5

Alie, Fig. 5 (annotated).

Alie discloses that its device can be used either in a “backside illuminated” architecture or in a “front side illuminated” architecture. Alie, [0053] (“in addition to backside illuminated, front side illuminated architectures are also contemplated to be within the present scope”). In a front side illuminated (FSI) device, incident light

enters the device from the “front side,” i.e., the side of the device containing a photodiode junction and a metallization layer connected to the photodiode junction. Ex-1012, [0048] (“In a typical FSI imager, incident light enters the semiconductor device by first passing by transistors and metal circuitry.”); *see* Ex-1004 ¶97. In a front side illuminated architecture, therefore, the top side of the semiconductor layer 34 with the photodiode junction 54 corresponds to the claimed light incident side. Ex-1004 ¶97.

In a backside illuminated (BSI) device, on the other hand, incident light enters the device from the “backside,” which is the side opposite the front side. *See* Ex-1012, [0048] (disclosing that in BSI imagers “incident light enters the device via the light sensing portion and is mostly absorbed prior to reaching the circuitry”); *see also* Ex-1021, 4 (“BSI imagers are configured to have the light sensing portion opposite the transistor and circuitry”); Ex-1012, [0049] (“the photosensitive diode can be configured with a BSI architecture, and thus electromagnetic radiation would enter the semiconductor substrate from the direction of the textured region [that is located on the opposite side of the multiple doped regions]”); Ex-1024, Fig. 6 (depicting an example BSI device where light is incident on the textured region located on the backside of a silicon material 62 opposite the doped regions 64 and 66); Ex-1004 ¶98. In a backside illuminated architecture, therefore, the bottom side of the semiconductor layer 34 (where the textured region 36 is located) corresponds

to the claimed light incident side. *See* Alie, [0094] (“Additional scattering can be provided by positioning a textured forward scattering layer on the side of the device that receives incident electromagnetic radiation.”); *see also* Ex-1004 ¶98.

For a backside illuminated architecture, it would have been obvious to modify the device of Figure 5 by placing the semiconductor substrate 32 and dielectric layer 38 on the top side of the semiconductor layer 34 opposite the light incident side. Ex-1004 ¶99. The semiconductor substrate 32 would be on top, with the dielectric layer 38 below it for bonding. *See* Alie, [0055] (disclosing that dielectric layers can be used for wafer bonding a semiconductor layer to a semiconductor substrate), [0087] (same); *see also* Ex-1004 ¶99. A provisional application for another reference Haddad¹³⁸ illustrates such an example device with a carrier substrate on top, with a bonding layer below it. Ex-1021, 4-5.

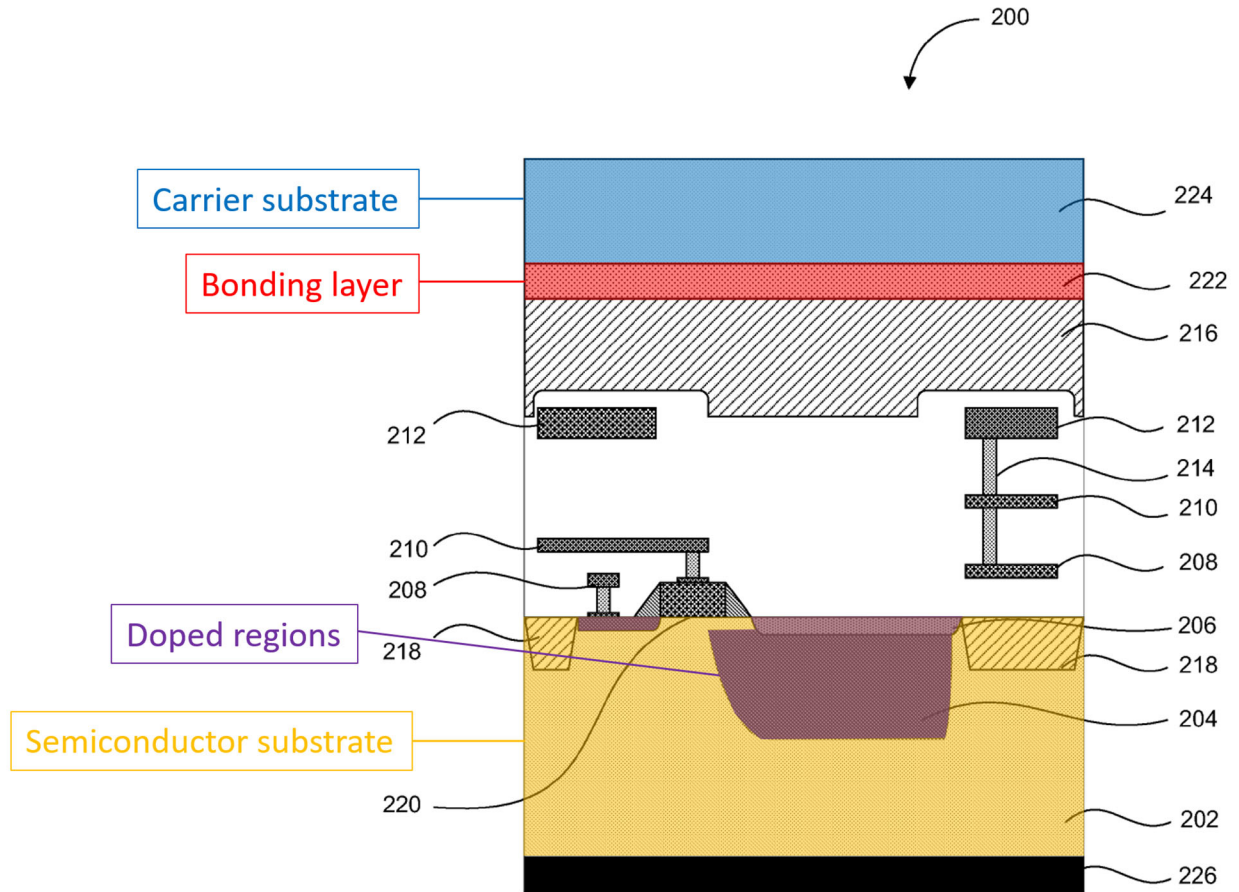


FIG. 4

Ex. 1021, Fig. 4 (annotated).

This modification allows (1) more incident light to enter via the bottom side of the device, and (2) the semiconductor substrate 32 to provide structural support. Ex-1004 ¶100. Alie teaches that absorbing more light leads to an increase in the quantum efficiency, which in turn, leads to an improvement in the signal to noise ratio. Alie, [0068], [0070]; *see also KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007); Ex-1004 ¶100. Haddad138 teaches that the semiconductor substrate can be disposed on either side of the device and can provide support if it is not removed

after manufacture. Ex-1012, [0086]. A POSITA would have had a reasonable expectation of success because a support substrate was routinely placed on either side of a device. Ex-1012, [0086] (“the carrier substrate can be disposed on any surface of the device”); *see also* Ex-1004 ¶100.

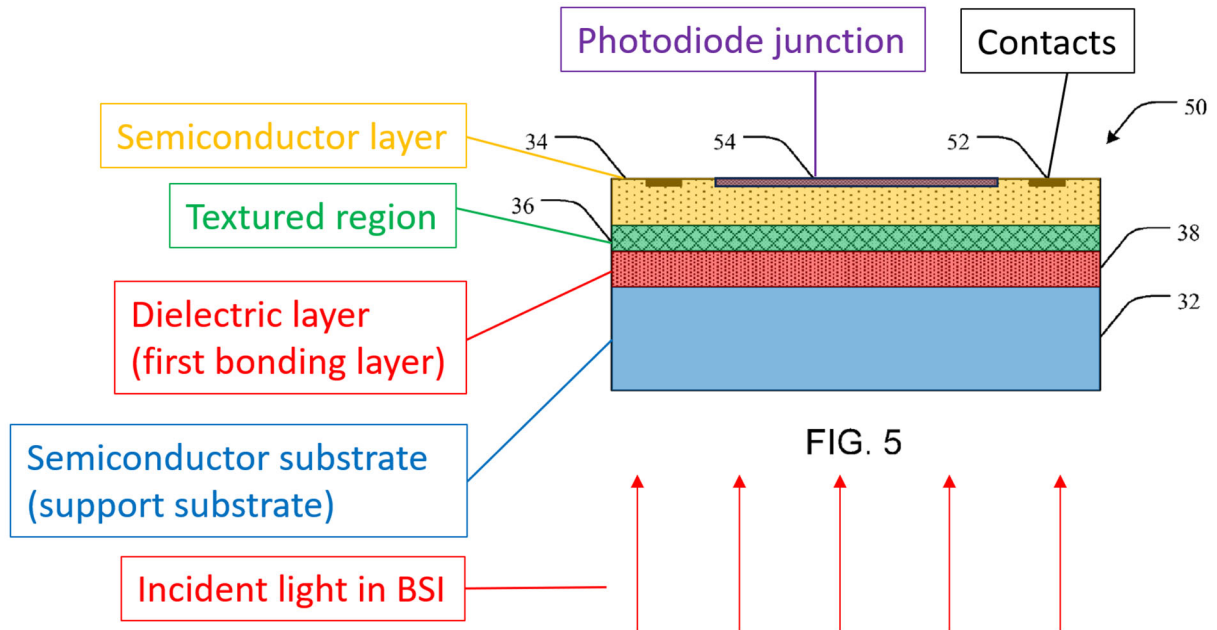
3. Claim 3

- a) **“The device of claim 2, further comprising a device layer coupled to the semiconductor layer on said side opposed to the light incident side.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶102-07.

In a backside illuminated (BSI) architecture such as the one discussed above regarding claim 2, a circuitry or a metallization layer (i.e., the claimed device layer) coupled to a photodiode junction in a semiconductor layer is on the side opposed to the light incident side. *See* Ex-1012, [0048] (disclosing that in BSI imagers “incident light enters the device via the light sensing portion and is mostly absorbed ***prior to reaching the circuitry***”); Ex-1004 ¶103. The provisional application to the ’737 patent refers to such a metallization layer as a device layer. Ex-1003, Fig. 3.

Figure 5 depicts a photodiode junction 54 and contacts 52 on the top side of the semiconductor layer 34, i.e., the claimed side opposed to the light incident side in a backside illuminated architecture. Ex-1004 ¶104.



Alie, Fig. 5 (annotated).

As discussed above regarding claim 2, it would have been obvious to modify the device of Figure 5 by placing the semiconductor substrate 32 and dielectric layer 38 on the top side of the semiconductor layer 34 opposite the light incident side. Ex-1004 ¶105.

A POSITA would have known that contacts 52 connect the photodiode junction 54 to a metallization layer above it (i.e., the claimed device layer). Ex-1004 ¶106. The photodiode junction 54 needs to be connected to a metallization layer above it to send out electrical signals representing the detected light. Ex-1004 ¶106. Otherwise, it would not be possible to make use of the information regarding the detected light. Ex-1004 ¶106. Indeed, a provisional application for another reference Haddad¹³⁸ illustrates an example device with a junction formed by doped regions

that is connected to a metallization layer above it via a transfer gate (with a carrier substrate and a bonding layer on top). Ex-1021, 4-5.

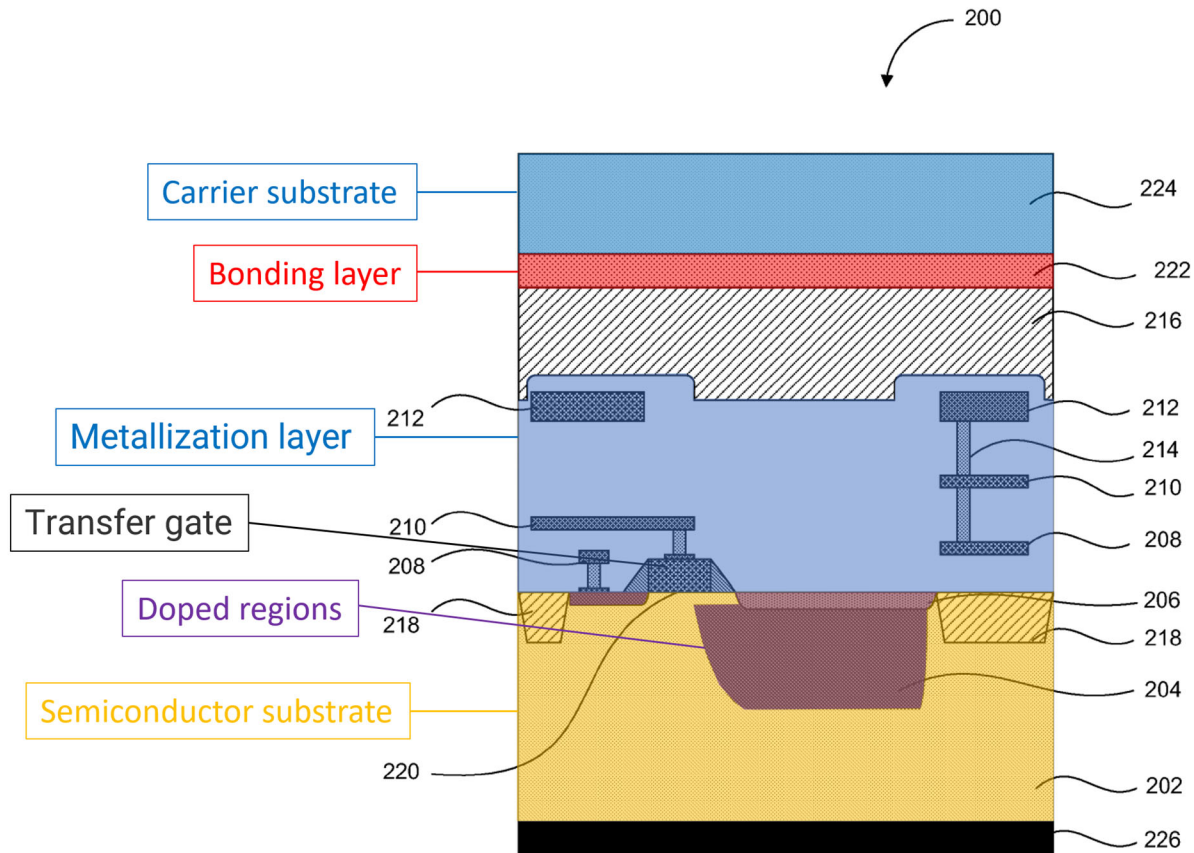


FIG. 4

Ex-1021, Fig. 4 (annotated).

4. Claim 4

- a) **“The device of claim 2, wherein the textured region is formed by etching.”**

Alie discloses this limitation. Ex-1004 ¶¶108-09.

Alie discloses that its textured region “can be formed by various techniques, including plasma etching, reactive ion etching, porous silicon etching ... [and]

chemical etching (e.g. anisotropic etching, isotropic etching).” Alie, [0074]; *see also* Alie, [0072] (“a substrate such as the semiconductor layer can be textured and patterned across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch”).

5. Claim 5

- a) “The device of claim 4, wherein said surface features comprise pyramids.”**

Alie discloses this limitation. Ex-1004 ¶¶110-11.

Alie discloses that “[n]on-limiting examples of shapes and configurations of surface features include ... pyramids.” Alie, [0068].

6. Claim 6

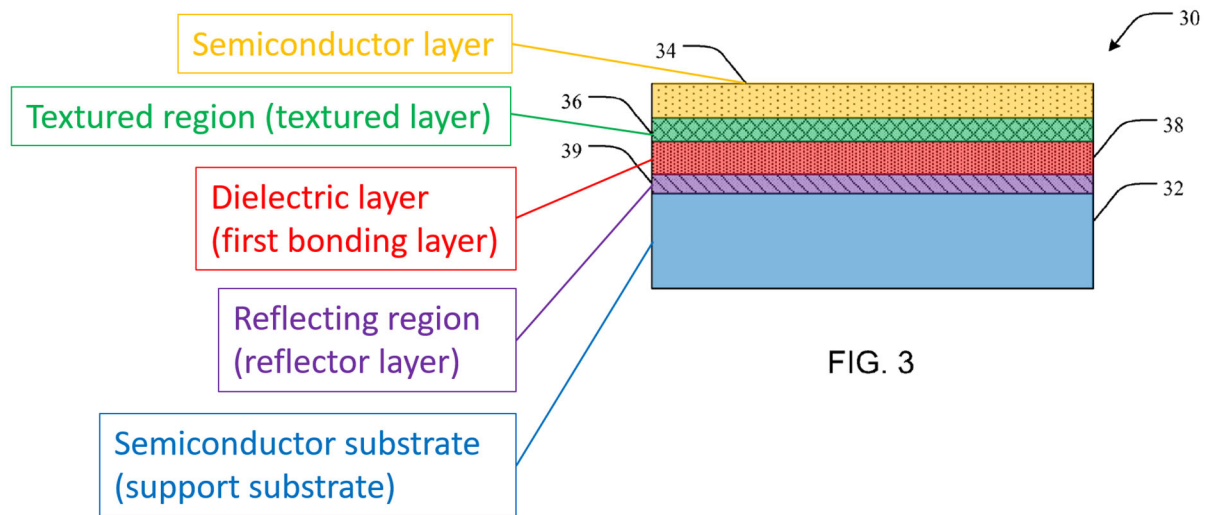
- a) “The device of claim 2, further comprising a reflector layer disposed between the textured layer and the support substrate.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious under Patent Owner’s proposed construction in the Related Case. Ex-1004 ¶¶112-18.

In the Related Case, Petitioner proposed that the term “the textured layer” is indefinite because it lacks antecedent basis. Ex-1013, 5. Patent Owner proposed that the term means the “textured region.” Ex-1014, 3.

Figure 3 discloses a reflecting region 39 (i.e., the claimed reflector layer) disposed between a textured region 36 (i.e., the claimed textured layer) and a

semiconductor substrate 32 (i.e., the claimed support substrate). Alie, [0089]; *see also* Ex-1004 ¶114.



Alie, Fig. 3 (annotated).

For a backside illuminated architecture, it would have been obvious to modify the device of Figure 3 by placing the semiconductor substrate 32, reflecting region 39, and dielectric layer 38 on the side of the semiconductor layer 34 opposite the light incident side. Ex-1004 ¶115. The semiconductor substrate 32 would be on top, with the reflecting region 39 below it, and the dielectric layer 38 below it for bonding. *See* Alie, [0055] (disclosing that dielectric layers can be used for wafer bonding a semiconductor layer to a semiconductor substrate), [0087] (same); *see also* Ex-1004 ¶115. This modification allows (1) more incident light to enter via the bottom side of the device, (2) the reflecting region 39 to reflect incident light into the semiconductor layer 34, and (3) the semiconductor substrate 32 to provide structural

support. Ex-1004 ¶115. Alie teaches that absorbing more light leads to an increase in the quantum efficiency, which in turn, leads to an improvement in the signal to noise ratio. Alie, [0068], [0070]; *see also* KSR, 550 U.S. at 418. Another reference Haddad138 teaches that the semiconductor substrate can be disposed on either side of the device. Ex-1012, [0086]. Haddad138 also teaches that a reflecting layer is advantageously placed on the opposite side of the light incident side. Ex-1012, [0078] (“the reflecting layer can be located on the semiconductor substrate *opposite* the incoming electromagnetic radiation”); Ex-1021, Fig. 9.

A POSITA would have had a reasonable expectation of success because a reflecting layer was routinely placed on the side of a semiconductor layer opposite the light incident side. Ex-1012, [0078] (“the reflecting layer can be located on the semiconductor substrate *opposite* the incoming electromagnetic radiation”); Ex-1021, Fig. 9; *see also* Ex-1004 ¶116. And a support substrate was routinely placed on either side of a device. Ex-1012, [0086] (“the carrier substrate can be disposed on any surface of the device”); *see also* Ex-1004 ¶116.

Other than having an additional reflector layer, Alie’s device disclosed in Figure 3 is similar to Alie’s device disclosed in Figure 5 discussed above regarding claims 1 and 2 (from which claim 6 depends) and meets claims 1 and 2 for the same reason. Ex-1004 ¶117.

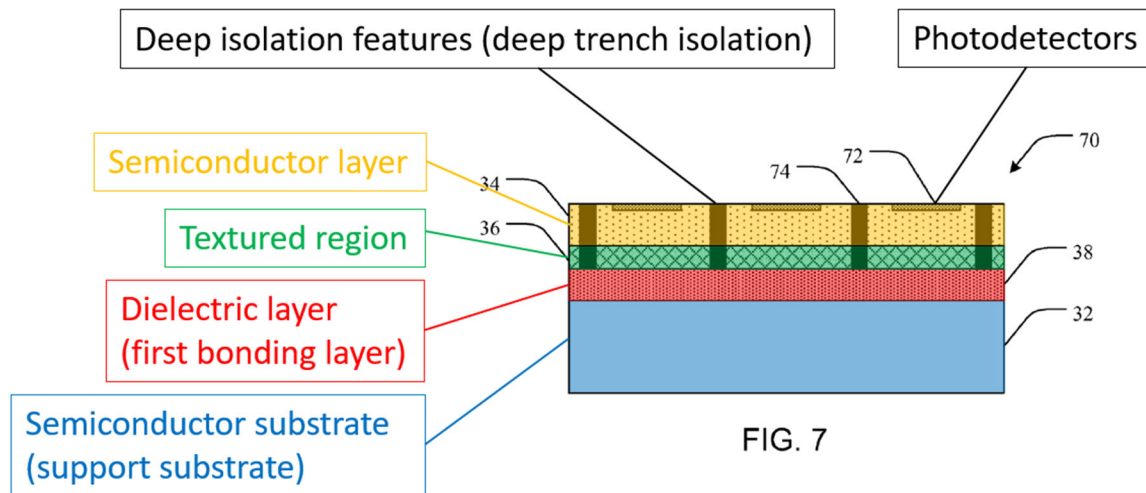
7. Claim 7

a) “The device of claim 1, further comprising deep trench isolation for isolating the device.”

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶119-25.

Figure 7 discloses deep isolation features (i.e., the claimed deep trench isolation) isolating each photodetector 72. Alie, [0097]; *see also* Ex-1004 ¶120.



Alie, Fig. 7 (annotated).

Other than having deep isolation features, Alie’s device disclosed in Figure 7 is similar to Alie’s device disclosed in Figure 5 discussed above regarding claim 1 (from which claim 7 depends) and meets claim 1 for the same reason. Ex-1004 ¶121.

It would also have been obvious to use the deep isolation features of Figure 7 to isolate Alie’s device disclosed in Figure 5. Ex-1004 ¶122. Alie teaches that “[t]he isolation features isolate each photodetector electrically, optically, or both

electrically and optically” and “[i]solation features can thus maintain uniformity across an array by reducing optical and electrical crosstalk between the photodetectors.” Alie, [0097]; *see also KSR*, 550 U.S. at 418; Ex-1004 ¶122. A POSITA would have recognized the benefits of the deep isolation features of Figure 7 and used them to isolate Alie’s device disclosed in Figure 5. Ex-1004 ¶122.

It would have been a use of known technique (i.e., deep isolation features) to improve similar devices in the same way. *KSR*, 550 U.S. at 417; Ex-1004 ¶123. Alie’s Figure 5 device and Figure 7 device share the same semiconductor layer 34, textured region 36, dielectric layer 38, and semiconductor substrate 32. *Compare* Alie, Fig. 5 *with* Alie, Fig. 7.

A POSITA would have had a reasonable expectation of success. Ex-1004 ¶124. It would have been well within the abilities of a POSITA to use deep trench isolation features to isolate the Figure 5 device, given that it would have involved routine manufacturing steps that Alie was already using for the embodiment depicted in Figure 7. Ex-1004 ¶124.

8. Claim 8

a) “The device of claim 7, wherein said deep trench isolation provides light trapping functionality.”

Alie discloses this limitation. Ex-1004 ¶¶126-27.

Alie discloses that its “isolation features isolate each photodetector ... optically,” i.e., the isolation features provide the claimed light trapping functionality.

Alie, [0006]; *see also* Ex-1004 ¶127. Specifically, Alie discloses that its “isolation features regions can be configured to reflect incident electromagnetic radiation until it is absorbed, thereby increas[ing] the effective absorption length of the device.” Alie, [0099].

9. Claim 9

- a) “The device of claim 1, wherein the semiconductor layer is single crystal silicon.”**

Alie discloses this limitation. Ex-1004 ¶¶128-29.

Alie discloses that “[a] variety of semiconductor materials are contemplated for use,” including “monocrystalline silicon” (i.e., the claimed single crystal silicon). Alie, [0060]; *see also* Ex-1004 ¶129.

10. Claim 10

- a) “The device of claim 1, wherein the semiconductor layer comprises silicon and germanium.”**

Alie discloses this limitation. Ex-1004 ¶¶130-31.

Alie discloses that “[a] variety of semiconductor materials are contemplated for use,” including “silicon,” “germanium,” and “silicon germanium.” Alie, [0060].

11. Claim 11

- a) “The device of claim 1, wherein the surface features are formed in the semiconductor layer.”**

Alie discloses this limitation. Ex-1004 ¶¶132-33.

Alie discloses that its textured region “can include surface features to further increase the effective absorption length of the device.” Alie, [0068]. Specifically, Alie discloses that its textured region “can be formed by wet etching the semiconductor material,” producing the claimed surface features. Alie, [0105]; *see also* Alie, [0104] (“a method of making a semiconductor device can include wet etch texturing at least a portion of a surface of a semiconductor layer to form a textured region”), [0072] (“a substrate such as the semiconductor layer can be textured and patterned across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch or a laser process to define a specific structure or pattern”); Ex-1004 ¶133. Alie also discloses chemically and/or structurally altering the surface of the substrate, “result[ing] in the formation of surface features appearing as structures or patterned areas on the surface.” Alie, [0077].

12. Claim 13

- a) **“The device of claim 1, wherein the surface features are not uniform in height.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶134-40.

Alie discloses that its surface features, for example, “cones, pyramids, protrusions, and the like can have an *average height*.” Alie, [0068]. That the surface

features have an “average height” rather than one height shows that the surface features are not uniform in height, as required by this limitation. Ex-1004 ¶136.

Moreover, U.S. Patent No. 7,442,629 (Mazur), which Alie incorporates by reference in paragraph [0076], discloses “spikes” (i.e., the claimed surface features) with “a *typical* height of about 500 nm” in Figures 5A and 5B. Ex-1025, 6:3-8; *see also* Ex-1004 ¶137.

FIG. 5A

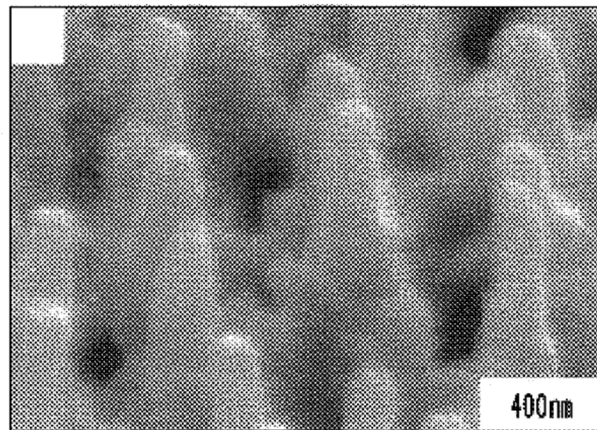
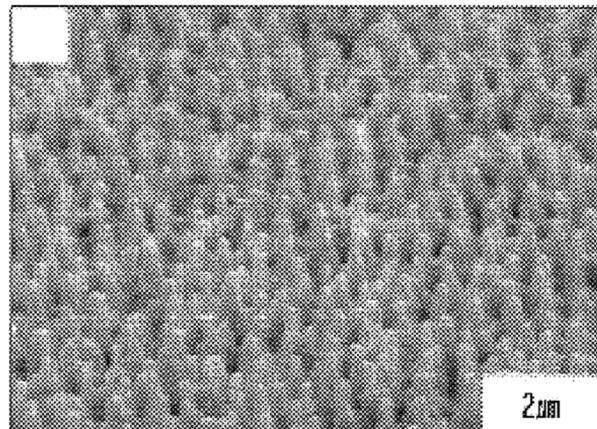
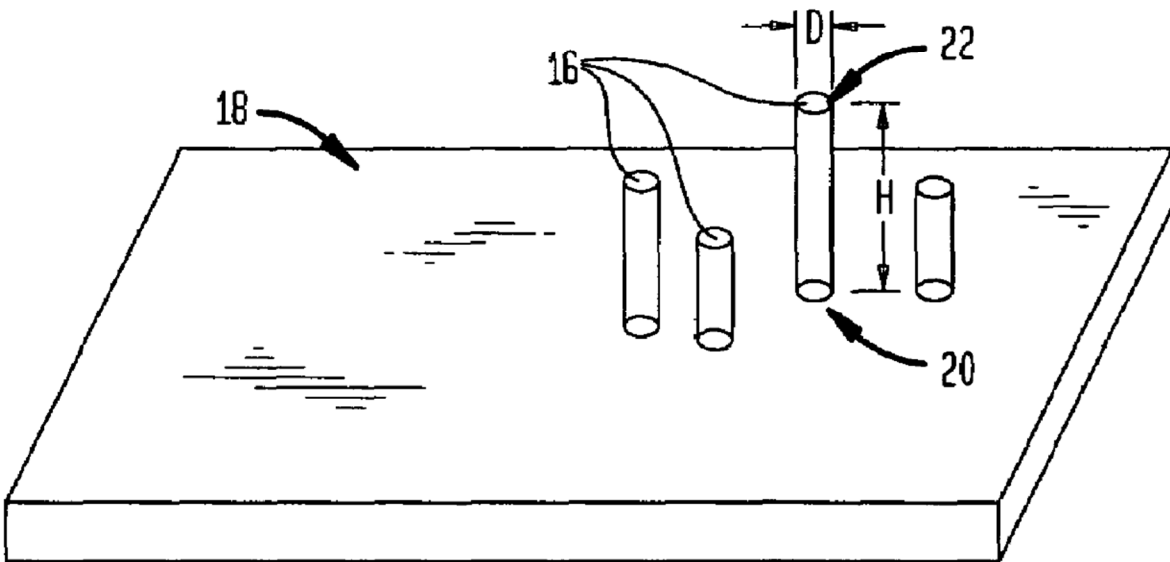


FIG. 5B



Ex-1025, Figs. 5A & 5B. As shown in Figures 5A and 5B, the surface features exhibit subtle variations in height, i.e., the surface features are not uniform in height, as required by this limitation. Ex-1004 ¶138. Figure 2 of Mazur schematically depicts these surface features. Ex-1025, 4:19-21.

FIG. 2



Ex-1025, Fig. 2. Although the spikes are “shown only for illustrative purposes and are not intended to indicate actual density, size or shape,” Ex-1025, 4:21-24, they accurately depict the variations in height, Ex-1025, 4:30-33 (disclosing that the surface features have an “average height” in a “range of about 200 nm to about 1 micrometer”); *see also* Ex-1004 ¶139.

13. Claim 14

- a) **“The device of claim 1, wherein said first bonding layer comprises any of silicon oxide, silicon nitride and amorphous silicon.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶141-46.

Alie discloses that its dielectric layer (i.e., the claimed first bonding layer) can include “oxides” and “nitrides.” Alie, [0088]. A POSITA would have understood that silicon oxides and silicon nitrides are one of the most common oxides and nitrides used for bonding. *See, e.g.*, Ex-1027, [0032]; Ex-1026, 228; *see also KSR*, 550 U.S. at 416; Ex-1004 ¶142.

It would also have been obvious to use silicon oxide or silicon nitride as the bonding layer because they can be easily polished and bonded. Ex-1026, 228 (“Materials that are too rough or difficult to polish may be covered by process-compatible intermediate layers such as spun-on or chemical vapor-deposited *silicon dioxide or silicon nitride, which may be easily polished and bonded.*”); *see also KSR*, 550 U.S. at 418; Ex-1004 ¶143.

It would also have been obvious to apply the known technique of using silicon oxide or silicon nitride as bonding layers to Alie’s device to yield predictable results. *KSR*, 550 U.S. at 417; Ex-1004 ¶144. Silicon oxide and silicon nitride were routinely used as bonding layers. Ex-1026, 216 (“SOI [silicon-on-insulator] structures consist

of a thin, top layer of single-crystal silicon, a layer of silicon dioxide (SiO₂), and a silicon handle substrate that acts as mechanical support.”); Ex-1027, [0032] (“The bonding layer 9 is, for example, formed of at least any one of a silicon oxide film (SiO₂), a silicon nitride film (SiN_x) ... as a single layer or a plurality of stacked layers.”); Ex-1028, 317; *see also* Ex-1004 ¶144. The use of silicon oxide and silicon nitride would have yielded predictable results because they were commonly used in semiconductor manufacturing and their properties were well known. Ex-1026, 228; Ex-1020, 155-162; *see also* Ex-1004 ¶144.

A POSITA would have had a reasonable expectation of success. Ex-1004 ¶145. It would have been well within the abilities of a POSITA to use silicon oxide and silicon nitride because the manufacturing methods were well known. Ex-1020, 155-162; *see also* Ex-1004 ¶145. Using silicon oxide and silicon nitride for bonding would have involved routine semiconductor manufacturing steps. Ex-1020, 155-162; *see also* Ex-1004 ¶145.

14. Claim 15

- a) **“The device of claim 1, wherein said semiconductor layer has a thickness in a range of about 1 micron to about 10 microns.”**

Alie discloses this limitation. Ex-1004 ¶¶147-48.

Alie discloses a semiconductor material (i.e., the claimed semiconductor layer) with “a thickness of from about 1 μm to about 10 μm.” Alie, [0063].

15. Claim 16

- a) **“The device of claim 15, wherein the device exhibits a quantum efficiency of at least about 35% for electromagnetic radiation at a wavelength of about 940 nm.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶149-53.

Like the '737 patent, Alie discloses using a textured region in a photodetector to increase quantum efficiency, particularly for infrared light, Alie, [0070], which includes light with a wavelength of 940 nm, Ex-1029, 807. A POSITA would have known that the increased quantum efficiency is at least about 35% for electromagnetic radiation at a wavelength of about 940 nm, as required by this limitation. Ex-1004 ¶150. At a minimum, it would have been obvious for a POSITA to ensure that Alie's device achieves a quantum efficiency of at least about 35% for electromagnetic radiation at a wavelength of about 940 nm, because as Alie teaches, an increase in the quantum efficiency “lead[s] to an improved signal to noise ratio.” Alie, [0070]; *see also* Ex-1012, [0050] (“Any increase in the quantum efficiency makes a large difference in the signal to noise ratio.”); *KSR*, 550 U.S. at 418; Ex-1004 ¶150.

A POSITA would have had a reasonable expectation of success in achieving a quantum efficiency of at least about 35% for electromagnetic radiation at a wavelength of about 940 nm. Ex-1004 ¶151. First, this understanding is consistent

with the disclosure of the '737 patent, which does not identify any exact combination of the disclosed features that achieves the required quantum efficiency, but rather, assumes that a POSITA would know how to achieve the claimed quantum efficiency. Ex-1004 ¶151.

Second, Jiang shows that a similar device has a quantum efficiency well over the claimed 35%, at around 70% for electromagnetic radiation at a wavelength of about 940 nm. Jiang, 1:32-35, 16:19-23; *see also* Ex-1004 ¶152.

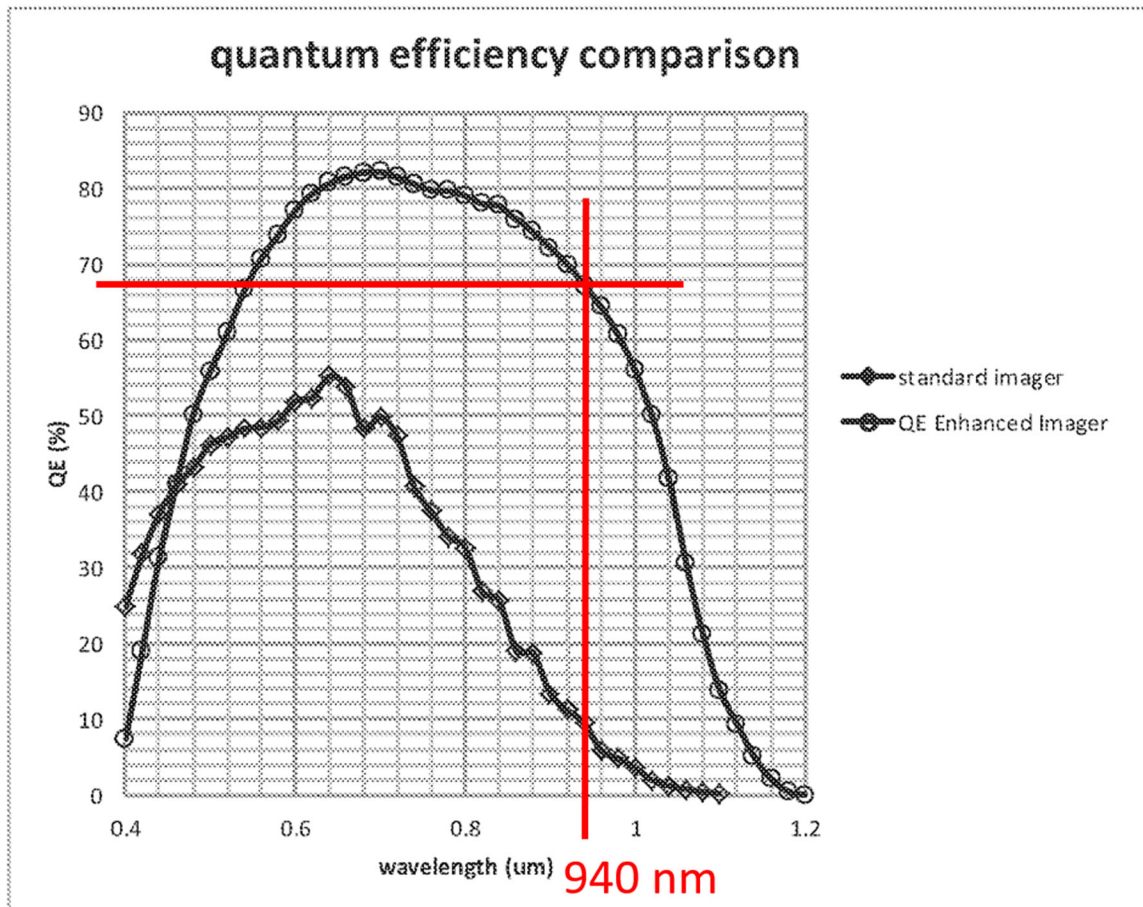


FIG. 15

Jiang, Fig. 15 (annotated). Like Alie, Jiang discloses enhancing quantum efficiency

by using a textured region. Jiang, 1:30-34. Like Alie's textured region, Jiang's textured region can be on the light incident side. Jiang, 19:15-19. And like Alie's textured region, Jiang's textured region can be formed by chemical etching. Jiang, 5:13-17.

16. Claim 17

- a) **“The device of claim 1, wherein said bonding layer has a thickness in a range of about 30 nm to about 3 microns.”**

Alie discloses this limitation. Ex-1004 ¶¶154-55.

Alie discloses a dielectric layer (i.e., the claimed bonding layer) with “a thickness of from about 500 nm to about 2 microns,” which is fully encompassed by the claimed range of about 30 nm to about 3 microns. Alie, [0088]; *see also* Ex-1004 ¶155.

17. Claim 18

- a) **“The device of claim 1, wherein said plurality of surface features have a height in a range of about 50 nm to about 2 microns.”**

Alie discloses this limitation. Ex-1004 ¶¶156-57.

Alie discloses surface features with “a height of from about 50 nm to about 2 μm .” Alie, [0068].

18. Claim 19

- a) **“The device of claim 1, wherein said plurality of surface features have a height in a range from about 0.35 microns to about 0.7 microns.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶158-59.

Alie discloses surface features with “a height of from about 50 nm to about 2 μm .” Alie, [0068]. This height range of 0.05 microns to 2 microns fully encompasses the claimed range of from about 0.35 microns to about 0.7 microns and the claimed range does not produce any new and unexpected result. Ex-1004 ¶159.

19. Claim 20

- a) **“The device of claim 1, wherein said plurality of surface features are formed by using a patterned mask and photolithography followed by etching.”**

Alie discloses this limitation. Ex-1004 ¶¶160-61.

Alie discloses that “a substrate such as the semiconductor layer can be textured and patterned [to form surface features] across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch ... to define a specific structure or pattern.” Alie, [0072]; *see also* Ex-1004 ¶161.

20. Claim 21

- a) **“The device of claim 1, wherein said plurality of surface features comprise multiple etched levels.”**

Alie discloses this limitation. Ex-1004 ¶¶162-63.

As discussed above regarding claim 13, Alie discloses that its surface features are not uniform in height. Alie, [0068]. And as discussed above regarding claim 20, Alie discloses that its surface features can be formed by etching. Alie, [0072]. That Alie's surface features formed by etching have differing heights shows that the surface features comprise multiple etched levels, as required by this limitation. Ex-1004 ¶163.

21. Claim 22

- a) “The device of claim 1, wherein said textured region increases optical absorption of the semiconductor layer over an electromagnetic spectrum range of at least about 700 nm to about 1100 nm.”**

Alie discloses this limitation. Ex-1004 ¶¶164-65.

Alie discloses a textured region that “allow[s] a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared).” Alie, [0070]. Infrared includes the claimed electromagnetic spectrum range of at least about 700 nm to about 1100 nm. Ex-1029, 807 (“The region of the near infrared spectrum extends from about 700 nm ($14,000\text{ cm}^{-1}$) near the end of the visible region, to 2500 nm ($4,000\text{ cm}^{-1}$), which is the beginning of the infrared fundamental region.”); *see also* Ex-1004 ¶165. Alie further discloses that “[s]uch internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor layer.” Alie, [0070]. An increase in the effective absorption length increases the optical absorption of the

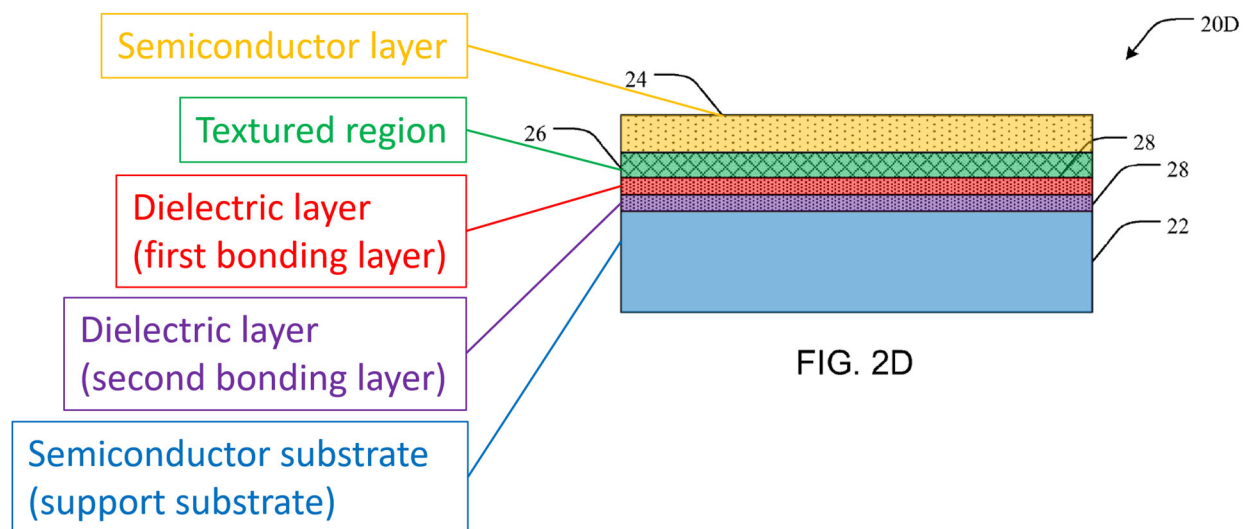
semiconductor layer, as required by this limitation. Alie, [0070] (“This increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.”); *see also* Ex-1004 ¶165.

22. Claim 23

- a) **“The device of claim 1, further comprising a second bonding layer positioned between the first bonding layer and the support substrate.”**

Alie discloses this limitation. Ex-1004 ¶¶166-70.

Alie discloses that, instead of using just one dielectric layer for bonding, two dielectric layers can be used. Alie, [0059]. Figure 2D depicts two dielectric layers (i.e., the claimed first and second bonding layers) placed between a semiconductor layer 24 and a textured region 26 on the one side and a semiconductor substrate 22 (i.e., the claimed support substrate) on the other side. Alie, [0055], [0059]; *see also* Ex-1004 ¶167.



Alie, Fig. 2D (annotated).

The top dielectric layer adjacent to the semiconductor layer 24 and textured region 26 corresponds to the claimed first bonding layer (red), whereas the bottom dielectric layer adjacent to the support substrate corresponds to the claimed second bonding layer (purple). Ex-1004 ¶168. As depicted in Figure 2D, the second bonding layer (purple) is positioned between the first bonding layer (red) and the support substrate (blue).

Other than having the second bonding layer, Alie's device disclosed in Figure 2D is similar to Alie's device disclosed in Figure 5 discussed above regarding claim 1 (from which claim 23 depends) and meets claim 1 for the same reason. Ex-1004 ¶169.

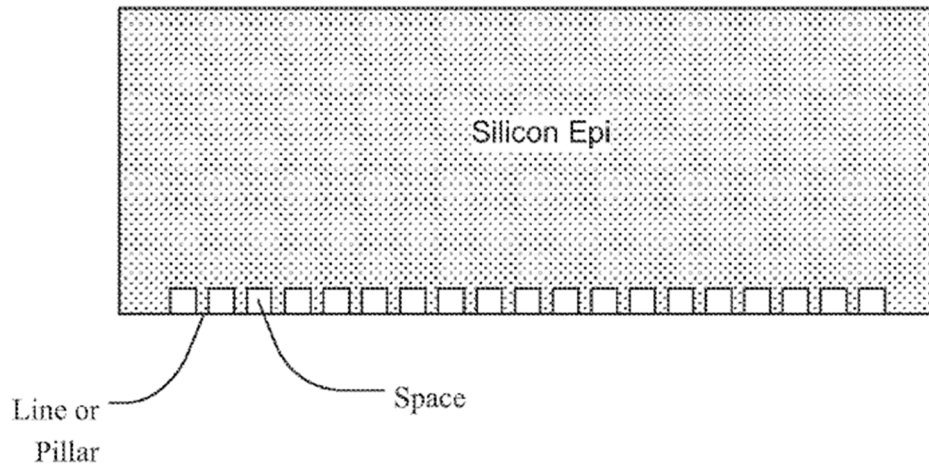
23. Claim 24

- a) “The device of claim 1, wherein the pattern is an at least substantially uniform grid.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious. Ex-1004 ¶¶171-72.

Alie discloses that “[n]on-limiting examples of shapes and configurations of surface features include ... gratings.” Alie, [0068]. The gratings could be uniform or non-uniform. It would have been obvious to try uniform gratings, i.e., the claimed substantially uniform grid, given the limited number of options, i.e., two, uniform or non-uniform. *KSR*, 550 U.S. at 421; Ex-1004 ¶172. The provisional application for the '737 patent identifies such gratings as an example of a “uniform grid pattern.”

Ex-1003, 13:3-4 (“[A]s is shown in FIG. 5 for example, the shallow trench isolation can be a ***uniform grid pattern*** comprised of [trenches] that form ***a series of spaces and lines*** or pillars.”).



Ex-1003, Fig. 5.

24. Claim 25

- a) **“The device of claim 1, wherein the pattern is a non-uniform arrangement.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶173-74.

Mazur, which Alie incorporates by reference in paragraph [0076], discloses “submicrometer beads” (i.e., the claimed surface features) that are “randomly distributed.” Ex-1025, 7:39-42. Ex-1004 ¶174.

25. Claim 26

- a) 26[pre]: “A method of making a photosensitive image device, comprising:”**

Alie discloses this preamble to the extent it is limiting. Ex-1004 ¶¶175-76.

Figures 11A and 11B depict a method of making Alie’s photosensitive image device. Alie, [0105] (“FIGS. 11A-C show one method of manufacturing a semiconductor device”); *see also* Alie, Abstract (“Photosensitive semiconductor devices and associated methods are provided.”); Ex-1004 ¶176.

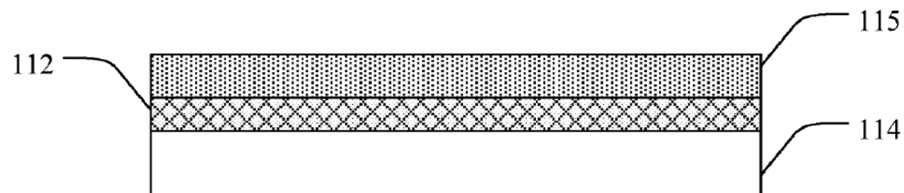


FIG. 11A

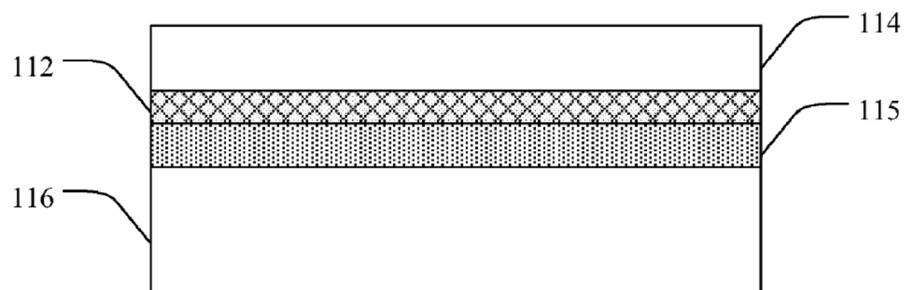


FIG. 11B

Alie, Figs. 11A-B.

- b) **26[a]: “providing a semiconductor layer having a light incident side and an opposed side, said semiconductor layer having multiple doped regions forming at least one junction;”**

Alie discloses this limitation. Ex-1004 ¶¶177-81.

Figure 11B depicts a semiconductor material 114 (i.e., the claimed semiconductor layer). Alie, [0105]; *see also* Ex-1004 ¶178.

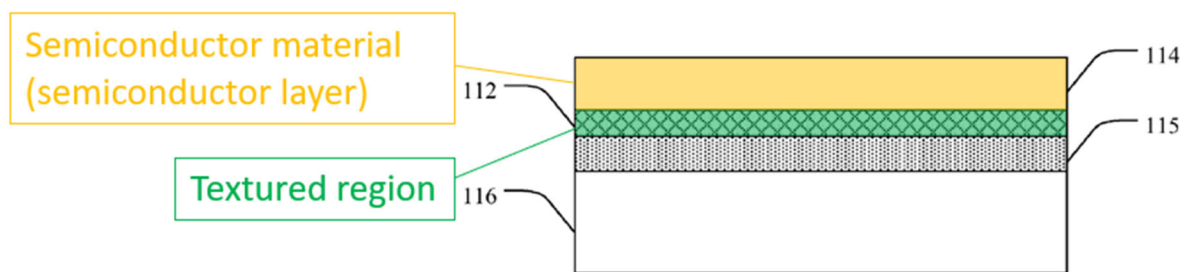


FIG. 11B

Alie, Fig. 11B (annotated).

As shown in Figure 11B, the semiconductor material 114 has a top side and a bottom side. Alie discloses “forming a p-i-n semiconductor material stack that creates a junction.” Alie, [0066]; *see also* Alie, [0066] (“the semiconductor material may include multiple junctions”). Such a photodiode junction would be formed on the top side of the semiconductor material 114 because the photodiode junction needs to be connected to a metallization layer above it (not shown in Figure 11B) to send out electrical signals representing the detected light. Ex-1004 ¶179.

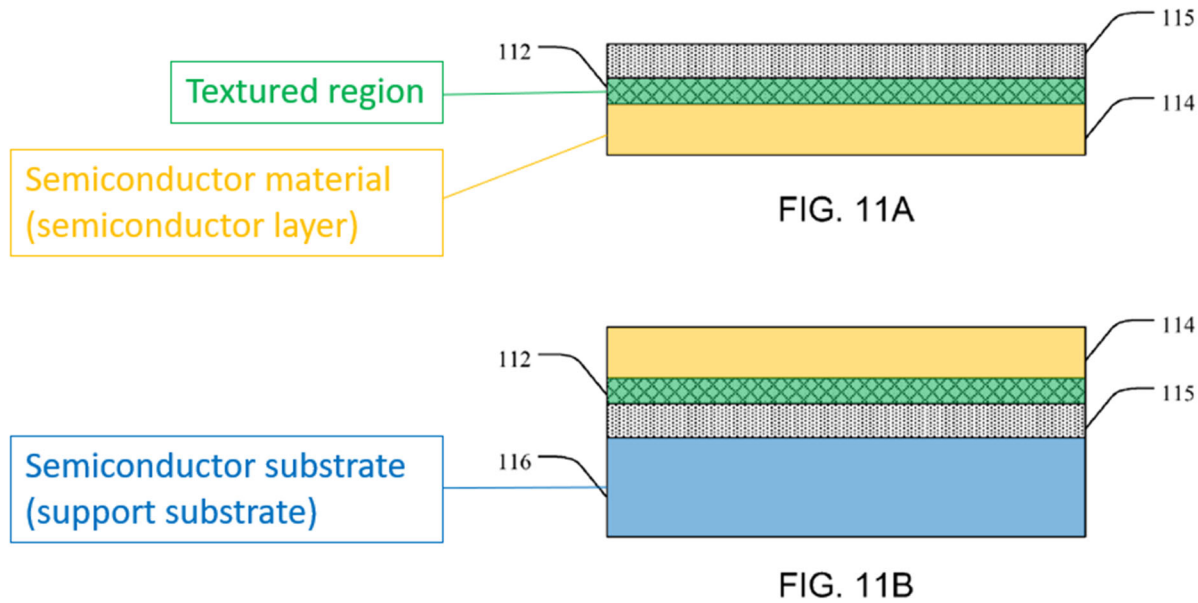
As discussed above regarding claim 2, either the top side and the bottom side can correspond to the claimed light incident side, where the other side corresponds

to the claimed opposed side. Ex-1004 ¶180. Specifically, in a front side illuminated architecture, the top side corresponds to the claimed light incident side because incident light enters the device from the top, whereas in a backside illuminated architecture, the bottom side corresponds to the claimed light incident side because incident light enters the device from the bottom. *See* discussion above regarding claim 2.

c) 26[b]: “providing a support substrate;”

Alie discloses this limitation. Ex-1004 ¶¶182-83.

Alie discloses that “[t]he resulting structure [shown in Figure 11A and including a semiconductor material 114, i.e., the claimed semiconductor layer] can then be wafer bonded to a semiconductor substrate 116 [i.e., the claimed support substrate], as is shown rotated 180° in FIG. 11B.” Alie, [0105]; *see also* Ex-1004 ¶183.

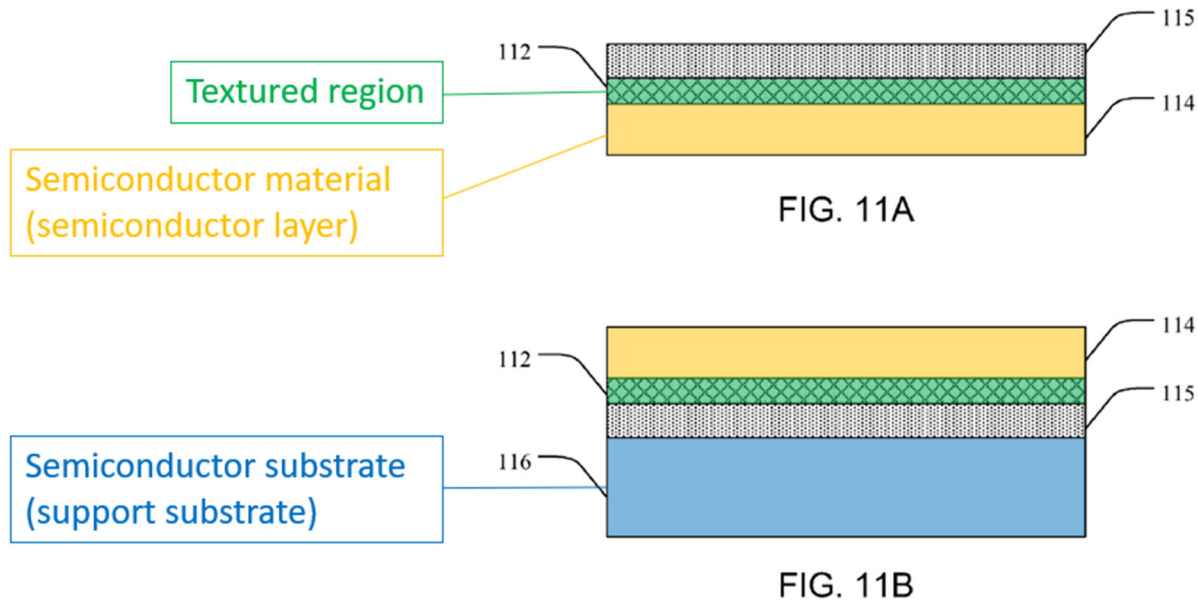


Alie, Figs. 11A-B (annotated).

d) 26[c]: “bonding the semiconductor layer to the support substrate;”

Alie discloses this limitation. Ex-1004 ¶¶184-85.

Alie discloses that “[t]he resulting structure [shown in Figure 11A and including a semiconductor material 114, i.e., the claimed semiconductor layer] can then be *wafer bonded* to a semiconductor substrate 116 [i.e., the claimed support substrate], as is shown rotated 180° in FIG. 11B.” Alie, [0105]; *see also* Ex-1004 ¶185.



Alie, Figs. 11A-B (annotated).

- e) **26[d]: “creating a plurality of surface features on one of the semiconductor layer and the support substrate, wherein the surface features are formed via etching;”**

Alie discloses this limitation. Ex-1004 ¶¶186-87. Claim 26 allows limitations 26[d]-[f] to be performed before limitation 26[c] because it does not require those limitations to be performed after limitation 26[c].

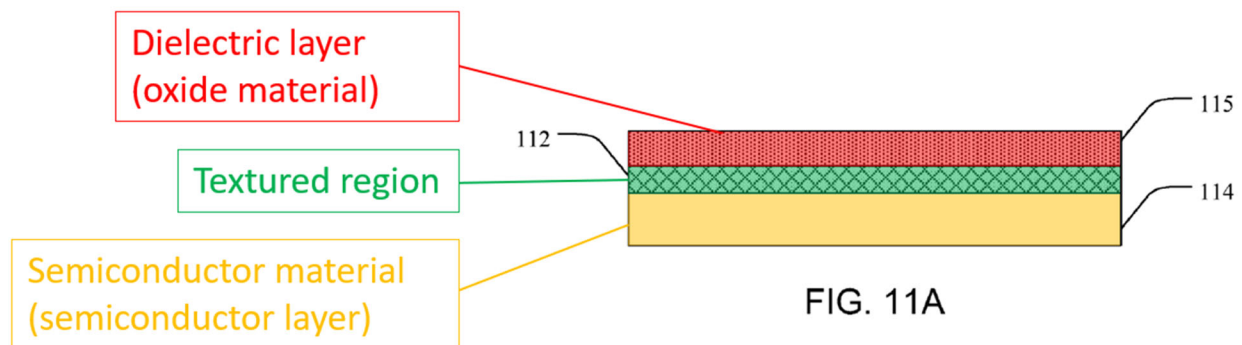
Alie discloses that its textured region “can include surface features to further increase the effective absorption length of the device.” Alie, [0068]. Specifically, Alie discloses that its textured region “can be formed by wet etching the semiconductor material,” producing the claimed surface features. Alie, [0105]; *see also* Alie, [0104] (“a method of making a semiconductor device can include wet etch texturing at least a portion of a surface of a semiconductor layer to form a textured region”), [0072] (“a substrate such as the semiconductor layer can be textured and

patterned across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch or a laser process to define a specific structure or pattern”); Ex-1004 ¶187.

- f) **26[e]: “depositing an oxide material within at least a portion of the semiconductor layer or support substrate removed during etching; and”**

Alie discloses this limitation. Ex-1004 ¶¶188-89.

Figure 11A depicts depositing a dielectric layer 115 (i.e., the claimed oxide material) over the textured region (i.e., the claimed portion of the semiconductor layer or support substrate removed during etching). Alie, [0105]; *see also* Ex-1004 ¶189. Alie discloses the dielectric layer can be made of “oxides.” Alie, [0088].



Alie, Figs. 11A (annotated).

- g) **26[f]: “processing the region of the semiconductor layer or support substrate comprising the surface features with CMP after depositing the oxide material.”**

Alie discloses this limitation under Patent Owner’s proposed construction in the Related Case. Ex-1004 ¶¶190-93.

In the Related Case, Petitioner proposed that this term is indefinite because of missing antecedent basis. Ex-1013, 5. Patent Owner proposed that the term has a plain and ordinary meaning and that, to the extent a construction is required, it means “a polishing step or series of polishing steps in the fabrication of the imager device performed after the deposition of the oxide material.” Ex-1014, 4.

Alie discloses that, after depositing the dielectric layer 115 (i.e., the claimed oxide material) over the textured region (i.e., the claimed region of the semiconductor layer or support substrate comprising the surface features), “[t]he dielectric layer can then be polished until smooth with a process such as CMP processing.” Alie, [0105]; *see also* Ex-1004 ¶192.

26. Claim 27

- a) 27[pre]: “The method of claim 26, wherein bonding the semiconductor layer to the support substrate comprises:”**

Alie discloses this preamble to the extent it is limiting. Ex-1004 ¶¶194-95.

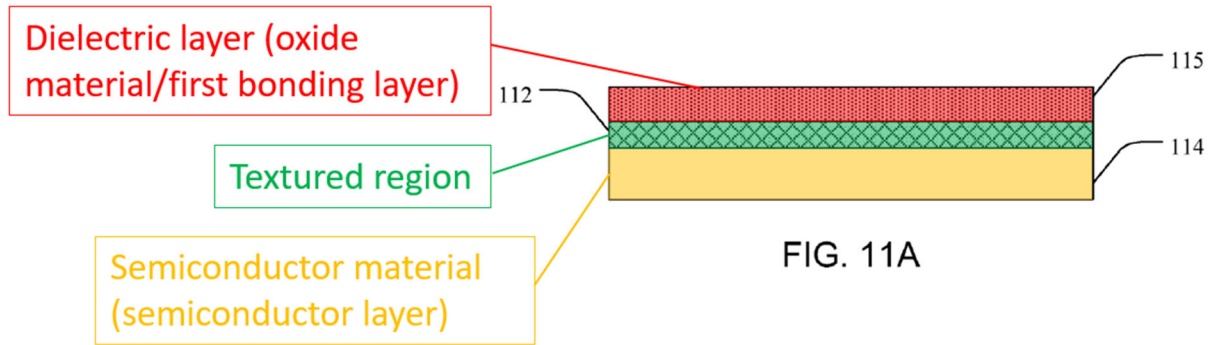
See claim 26.

- b) 27[a]: “depositing a first bonding layer onto the semiconductor layer; and”**

Alie discloses this limitation. Ex-1004 ¶¶196-97.

Figure 11A depicts depositing a dielectric layer 115 (i.e., the claimed oxide material and the first bonding layer) onto the semiconductor material 114 (i.e., the claimed semiconductor layer). Alie, [0105]; *see also* Ex-1004 ¶197; *Google LLC v.*

Pers. Audio, LLC, 743 F. App'x 978, 985 (Fed. Cir. 2018) (“a single element, feature, or mechanism can ordinarily satisfy multiple claim limitations”); *Kea Cloud, Inc. v. Valyant Ai, Inc.*, No. IPR2023-00450, Paper 12 at (P.T.A.B. July 19, 2023).



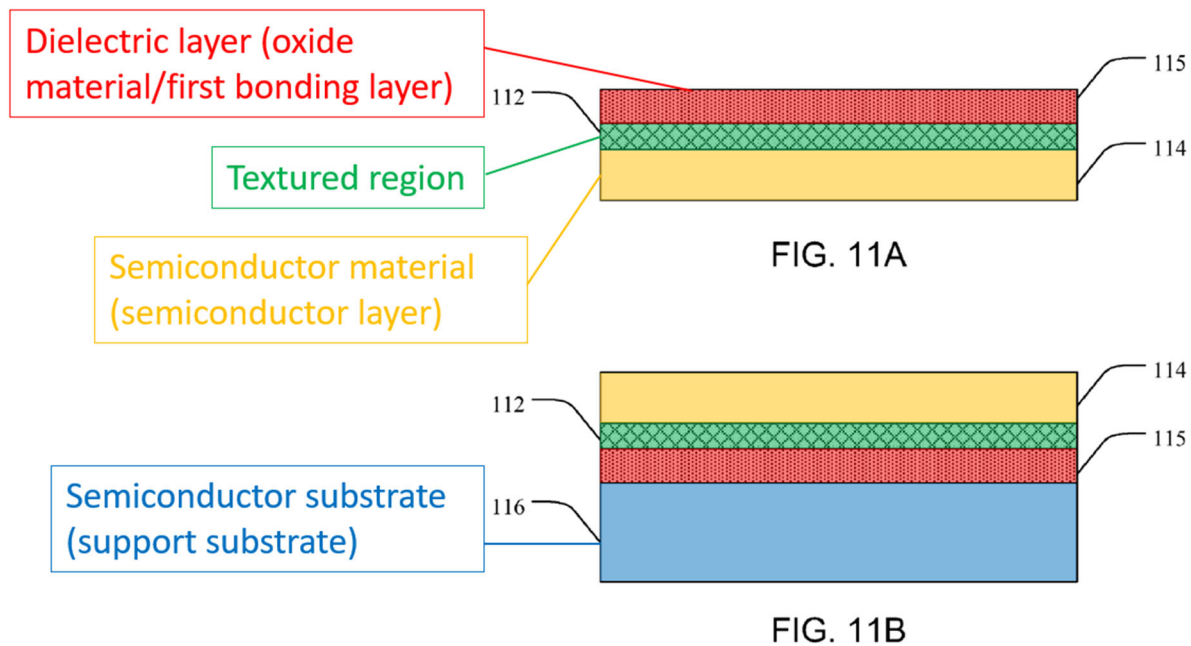
Alie, Fig. 11A (annotated).

Alternatively, if the Board finds that the dielectric layer 115 cannot both be the claimed oxide material and the first bonding layer, Alie discloses depositing a polysilicon layer (i.e., the alternative first bonding layer) on the dielectric layer. Alie, [0095] (“By depositing a thin dielectric layer followed by a thick polysilicon layer it can be possible to create a surface that can be polished.”); *see also* Ex-1004 ¶197. The polysilicon layer is a bonding layer because it facilitates bonding. Alie, [0095] (“the polysilicon layer can be planarized and polished until smooth, and the resulting surface can be *wafer bonded*”); *see also* Ex-1004 ¶197.

c) 27[b]: “bonding the first bonding layer to a second bonding layer disposed on the support substrate.”

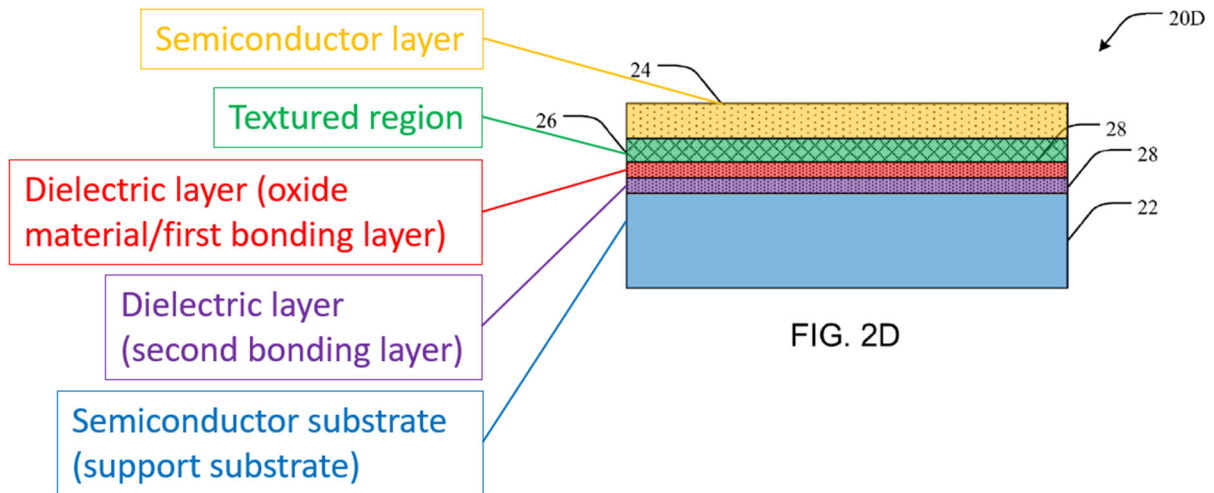
Alie discloses this limitation. Ex-1004 ¶¶198-201.

Alie discloses that “[t]he dielectric layer [i.e., the claimed first bonding layer] can be bonded directly to the semiconductor substrate [after being rotated 180° as shown in Figure 11B], *or to a second dielectric layer [i.e., the claimed second bonding layer] formed on the semiconductor substrate (not shown).*” Alie, [0105]; *see also* Ex-1004 ¶199.



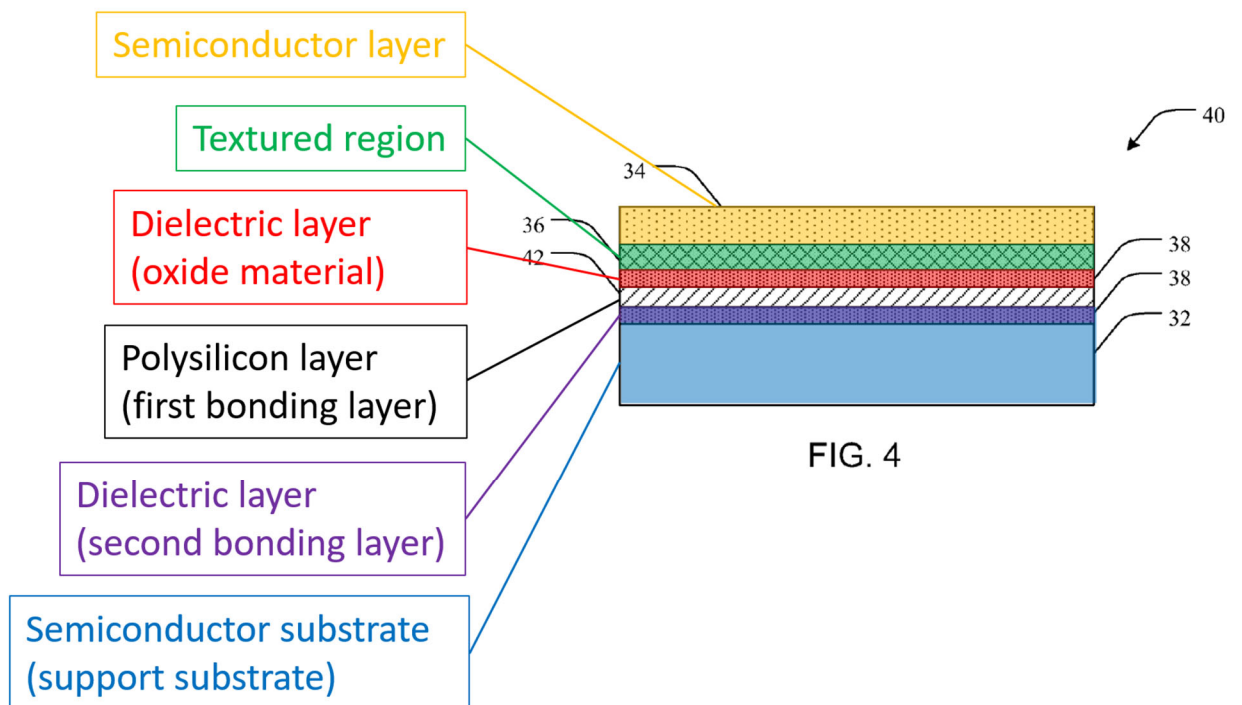
Alie, Figs. 11A-B (annotated).

Figure 2D illustrates Alie’s device with two bonding layers:



Alie, Fig. 2D (annotated); *see also* Ex-1004 ¶200.

Alternatively, Figure 4 illustrates Alie's device with a polysilicon layer bonded to the second bonding layer on top of the support substrate. Alie, [0095]; *see also* Ex-1004 ¶200.



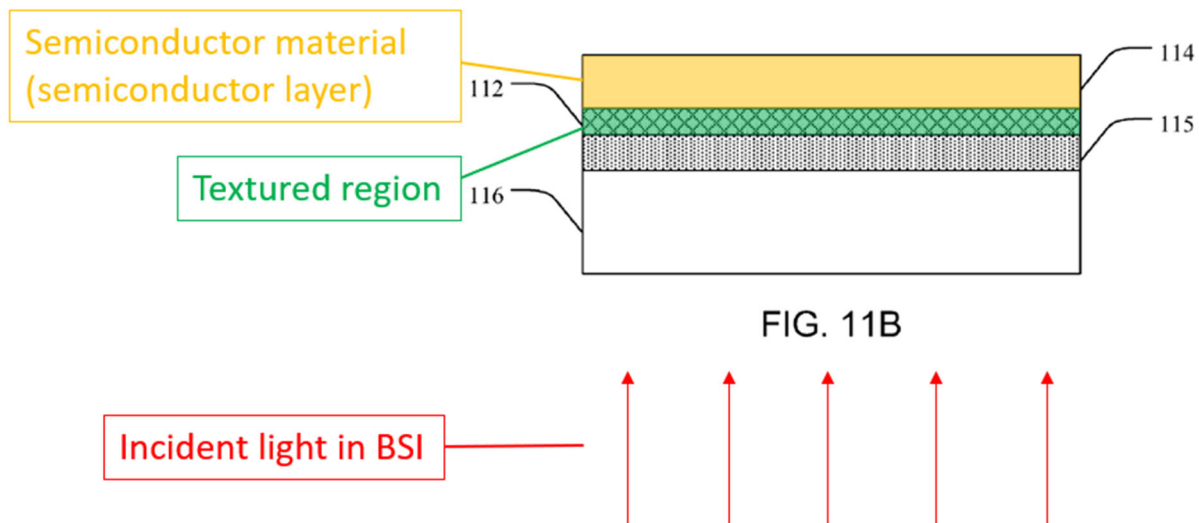
Alie, Fig. 4 (annotated).

27. Claim 28

- a) **“The method of claim 26, wherein the plurality of surface features are formed on the light incident side of the semiconductor layer.”**

Alie discloses this limitation. Ex-1004 ¶¶202-05.

As discussed above regarding limitation 26[a], the bottom side of the semiconductor material 114 (i.e., the claimed semiconductor layer) corresponds to the claimed light incident side in a backside illuminated architecture. Ex-1004 ¶203. Figure 11B depicts the textured region 112 formed on the bottom side of the semiconductor material 114.



Alie, Fig. 11B (annotated).

See discussion above regarding claim 2 for how devices such as the one depicted in Figure 11B would be modified for a backside illuminated architecture so

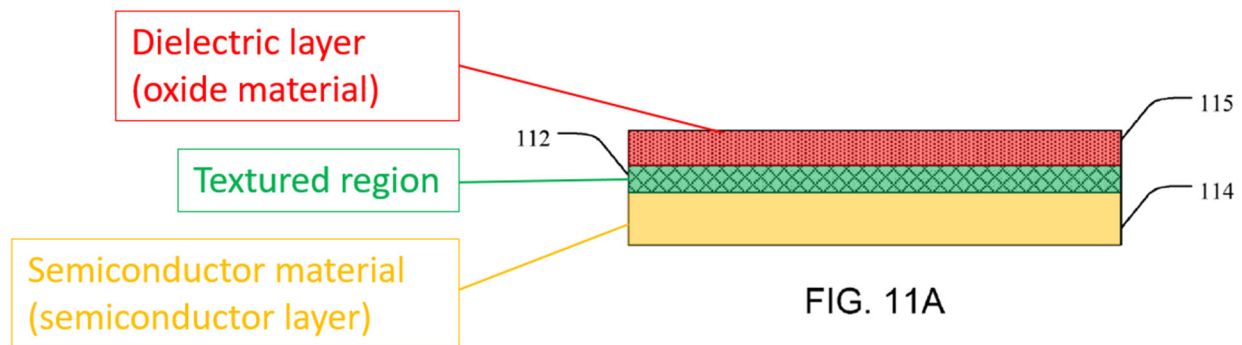
that the substrate 116 and the dielectric layer 115 are placed on the top side. Ex-1004 ¶204.

28. Claim 29

- a) **“The method of claim 26, wherein depositing the oxide material comprises at least partially filling one of trenches, holes, pits, and cones formed in the semiconductor layer during etching.”**

Alie discloses this limitation. Ex-1004 ¶¶206-09.

Figure 11A depicts depositing a dielectric layer 115 (i.e., the claimed oxide material) over the textured region. Alie, [0105]; *see also* Ex-1004 ¶207.



Alie, Figs. 11A (annotated).

Alie discloses textured regions with surface features such as “cones,” Alie, [0068], that are formed in the semiconductor layer during etching, Alie, [0072]. Ex-1004 ¶208.

29. Claim 30

- a) **“The method of claim 26, wherein the surface features are formed by shallow trench isolation etching.”**

Alie discloses this limitation under Patent Owner’s proposed construction in the Related Case. Ex-1004 ¶¶210-13.

In the Related Case, Petitioner proposed that the term “shallow trench isolation etching” is indefinite. Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning, and to the extent a construction is required, it means, “etching a pattern of shallow trenches.” Ex-1014, 4; Ex-1015, 2-3.

As discussed above regarding limitation 1[b] in Ground 1, Alie discloses a photodetector with a textured region. Alie, [0052], [0096], [0006]. Alie discloses that its textured region can include surface features. Alie, [0068]. “Non-limiting examples of shapes and configurations of surface features include ... gratings,” Alie, [0068], which are a series of trenches. *See* Baggenstoss, [0038] (discussing trenches that form a grated interface); *see also* Ex-1004 ¶212. Alie discloses that its surface features can be formed by chemical etching, Alie, [0074], and can have a height of 0.35 microns. Alie, [0068]; *see also* Ex-1004 ¶212. The ’737 patent states 0.35 microns is associated with “standard STI [shallow trench isolation] processes.” ’737 patent, 11:24-26; *see also* Ex-1004 ¶212.

30. Claim 31

- a) **“The method of claim 26, wherein the surface features are formed in the semiconductor layer.”**

Alie discloses this limitation. Ex-1004 ¶¶214-15.

See claims 11 and 26.

31. Claim 32

- a) **32[pre]: “A photosensitive imager device capable of detecting visible and infrared electromagnetic radiation, comprising:”**

Alie discloses this preamble under both Petitioner’s and Patent Owner’s proposed constructions in the Related Case. Ex-1004 ¶¶216-17.

See 1[pre].

- b) **32[a]: “a semiconductor layer having a light incident side and an opposed side, said semiconductor layer having multiple doped regions forming at least one junction,”**

Alie discloses this limitation. Ex-1004 ¶¶218-19.

See limitation 1[a].

- c) **32[b]: “a textured region comprising a plurality of surface features configured to interact with incident electromagnetic radiation so as to increase the quantum efficiency of the device,”**

Alie discloses this limitation under Patent Owner’s proposed construction in the Related Case. Ex-1004 ¶¶220-21.

See limitation 1[b].

- d) **32[c]: “a support substrate coupled to said semiconductor layer, and”**

Alie discloses this limitation. Ex-1004 ¶¶222-23.

See limitation 1[c].

- e) **32[d]: “a first bonding layer disposed between the semiconductor layer and the support substrate,”**

Alie discloses this limitation. Ex-1004 ¶¶224-25.

See limitation 1[d].

- f) **32[e]: “wherein the device exhibits a quantum efficiency of at least about 35% for electromagnetic radiation at a wavelength of about 940.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶226-27.

See claim 16.

32. Claim 33

- a) **“The device of claim 32, wherein the textured region is located on the light incident side of the semiconductor layer.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶228-29.

See claims 2 and 32.

33. Claim 34

- a) **“The device of claim 33, further comprising a device layer coupled to the semiconductor layer on said side opposed to the light incident side.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶230-31.

See claims 3 and 32.

34. Claim 35

- a) **“The device of claim 33, wherein the textured region is formed by etching.”**

Alie discloses this limitation. Ex-1004 ¶¶232-33.

See claims 4 and 32.

35. Claim 36

- a) **“The device of claim 35, wherein said surface features comprise pyramids.”**

Alie discloses this limitation. Ex-1004 ¶¶234-35.

See claims 5 and 32.

36. Claim 37

- a) **“The device of claim 33, further comprising a reflector layer disposed between the textured layer and the support substrate.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious under Patent Owner’s proposed construction in the Related Case. Ex-1004 ¶¶236-37.

See claims 6 and 32.

37. Claim 38

- a) **“The device of claim 32, further comprising deep trench isolation for isolating the device.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶238-39.

See claims 7 and 32.

38. Claim 39

- a) **“The device of claim 38, wherein said deep trench isolation provides light trapping functionality.”**

Alie discloses this limitation. Ex-1004 ¶¶240-41.

See claims 8 and 32.

39. Claim 40

- a) **“The device of claim 32, wherein the semiconductor layer is single crystal silicon.”**

Alie discloses this limitation. Ex-1004 ¶¶242-43.

See claims 9 and 32.

40. Claim 41

- a) **“The device of claim 32, wherein the semiconductor layer comprises silicon and germanium.”**

Alie discloses this limitation. Ex-1004 ¶¶244-45.

See claims 10 and 32.

41. Claim 42

- a) **“The device of claim 32, wherein the surface features are formed in the semiconductor layer.”**

Alie discloses this limitation. Ex-1004 ¶¶246-47.

See claims 11 and 32.

42. Claim 44

- a) **“The device of claim 32, wherein the surface features are not uniform in height.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶248-51.

See claims 13 and 32.

43. Claim 45

- a) **“The device of claim 32, wherein said first bonding layer comprises any of silicon oxide, silicon nitride and amorphous silicon.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶252-53.

See claims 14 and 32.

44. Claim 46

- a) **“The device of claim 32, wherein said semiconductor layer has a thickness in a range of about 1 micron to about 10 microns.”**

Alie discloses this limitation. Ex-1004 ¶¶254-55.

See claims 15 and 32.

45. Claim 47

- a) **“The device of claim 32, wherein said bonding layer has a thickness in a range of about 30 nm to about 3 microns.”**

Alie discloses this limitation. Ex-1004 ¶¶256-57.

See claims 17 and 32.

46. Claim 48

- a) **“The device of claim 32, wherein said plurality of surface features have a height in a range of about 50 nm to about 2 microns.”**

Alie discloses this limitation. Ex-1004 ¶¶258-59.

See claims 18 and 32.

47. Claim 49

- a) **“The device of claim 32, wherein said plurality of surface features have a height in a range from about 0.35 microns to about 0.7 microns.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶260-61.

See claims 19 and 32.

48. Claim 50

- a) **“The device of claim 32, wherein said plurality of surface features are formed by using a patterned mask and photolithography followed by etching.”**

Alie discloses this limitation. Ex-1004 ¶¶262-63.

See claims 20 and 32.

49. Claim 51

- a) **“The device of claim 32, wherein said plurality of surface features comprise multiple etched levels.”**

Alie discloses this limitation. Ex-1004 ¶¶264-65.

See claims 21 and 32.

50. Claim 52

- a) **“The device of claim 32, wherein said textured region increases optical absorption of the semiconductor layer over an electromagnetic spectrum range of at least about 700 nm to about 1100 nm.”**

Alie discloses this limitation. Ex-1004 ¶¶266-67.

See claims 22 and 32.

51. Claim 53

- a) **“The device of claim 32, further comprising a second bonding layer positioned between the first bonding layer and the support substrate.”**

Alie discloses this limitation. Ex-1004 ¶¶268-69.

See claim 23 and 32.

52. Claim 54

- a) **“The device of claim 32, wherein the surface features are arranged according to a pattern that is an at least substantially uniform grid.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶270-71.

See claims 24 and 32.

53. Claim 55

- a) **“The device of claim 32, wherein the surface features are arranged according to a pattern that is a non-uniform arrangement.”**

Alie discloses this limitation, or at a minimum, renders this limitation obvious.

Ex-1004 ¶¶272-73.

See claims 25 and 32.

B. Ground 2: Claims 1, 12-13, 21, 24, 30, 43-44, 51, and 54 Are Obvious Based on Alie and Baggenstoss

1. Claim 1

To the extent the Board finds that Alie does not anticipate or render obvious claim 1 because it does not disclose that “the surface features are arranged according to a pattern,” Alie in view of Baggenstoss renders claim 1 obvious under Patent Owner’s proposed construction in the Related Case. Ex-1004 ¶¶274-80.

In the Related Case, Petitioner proposed that the term “the surface features are arranged according to a pattern” is indefinite. Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning and that, to the extent a construction is required, it means “features coincident with at least one surface that are arranged in a repeating manner.” Ex-1014, 4.

As discussed above regarding limitation 1[b] in Ground 1, Alie discloses a photodetector with a textured region. Alie, [0052], [0096], [0006]; *see also* Ex-1004 ¶276. Alie discloses that its textured region can include surface features. Alie, [0068].

“Non-limiting examples of shapes and configurations of surface features include ... gratings” Alie, [0068].

Similarly, Baggenstoss discloses a photodetector with a grated interface formed by trenches 144 (i.e., the claimed surface features arranged according to a pattern). Baggenstoss, [0031]-[0032], [0009]; Ex-1004 ¶277.

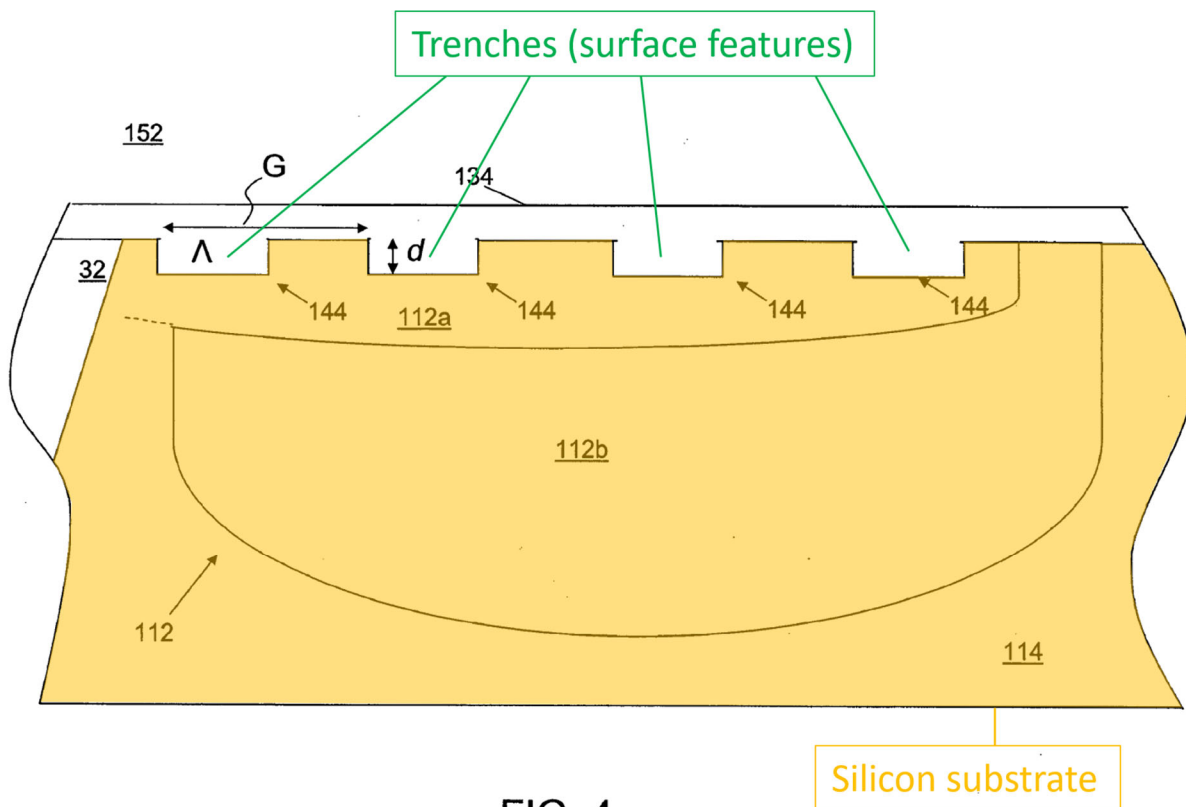


FIG. 4

Baggenstoss, Fig. 4 (annotated).

“Each grating (measured as the distance from the beginning of one trench 144 to the beginning of the next trench 144 (shown by arrow G)) has a predetermined period that is represented by Λ .” Baggenstoss, [0032]. The predetermined period Λ can be, for example, 340 nm. Baggenstoss, [0034]. Baggenstoss’s trenches are

features coincident with at least one surface that are arranged in a repeating manner, and are an example of a pattern provided by the provisional application for the '737 patent. Ex-1003, 13:3-4 (“[A]s is shown in FIG. 5 for example, the shallow trench isolation can be a ***uniform grid pattern*** comprised of [trenches] that form ***a series of spaces and lines*** or pillars.”); *see also* Ex-1004 ¶278.

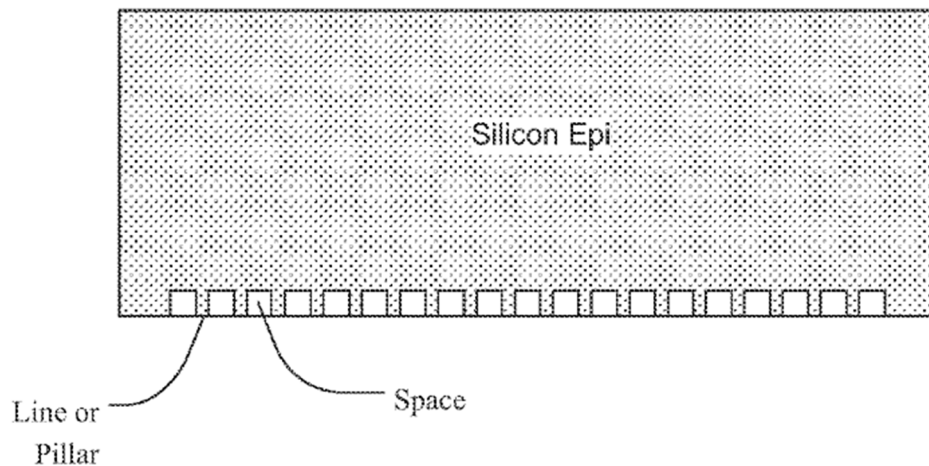


FIG. 5

Ex-1003, Fig. 5.

It would have been obvious to use Baggenstoss's trenches 144 as Alie's surface features, with a reasonable expectation of success, as discussed in Section VIII.B.11 below. Ex-1004 ¶279.

2. Claim 12

- a) “The device of claim 1, wherein the surface features have a substantially uniform height.”

Alie in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶281-85.

As discussed above regarding claim 1, Figure 4 of Baggenstoss depicts a grating interface formed by trenches 144 (i.e., the claimed surface features). Baggenstoss, [0031]-[0032]; *see also* Ex-1004 ¶282.

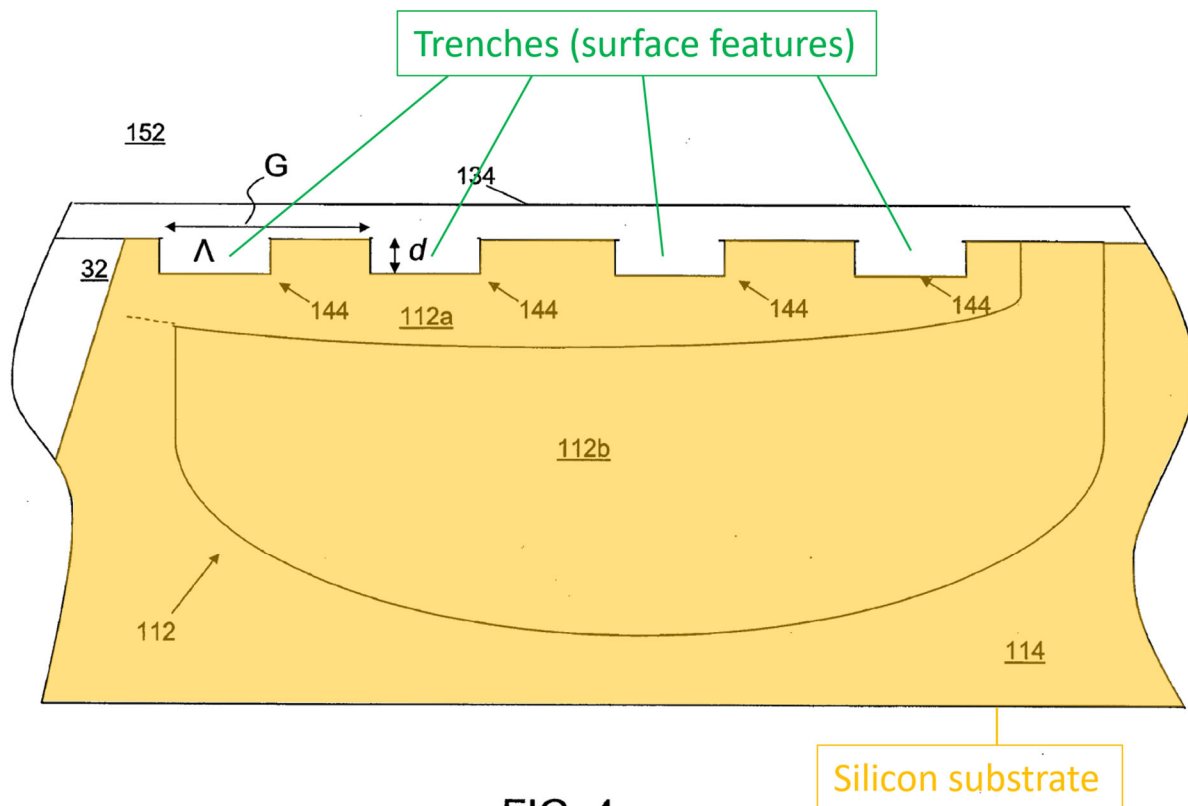


FIG. 4

Baggenstoss, Fig. 4 (annotated).

Baggenstoss discloses that the trenches 144 have a predetermined depth (i.e., the claimed height), represented by d in Figure 4. Baggenstoss, [0032]. The predetermined depth d can be, for example, a constant depth of 100 nm. Baggenstoss, [0034]-[0035]. Baggenstoss's surface features, therefore, have a substantially uniform height, as required by this limitation. Ex-1004 ¶283.

It would have been obvious to use Baggenstoss's trenches 144 as Alie's surface features, with a reasonable expectation of success, as discussed in Section VIII.B.11 below. Ex-1004 ¶284.

3. Claim 13

- a) **“The device of claim 1, wherein the surface features are not uniform in height.”**

Alie in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶286-91.

In another embodiment, Baggenstoss discloses a pixel cell with a “blazed (or step-wise)” gratings formed of trenches 244 (i.e., the claimed surface features). Baggenstoss, [0042]; *see also* Ex-1004 ¶287.

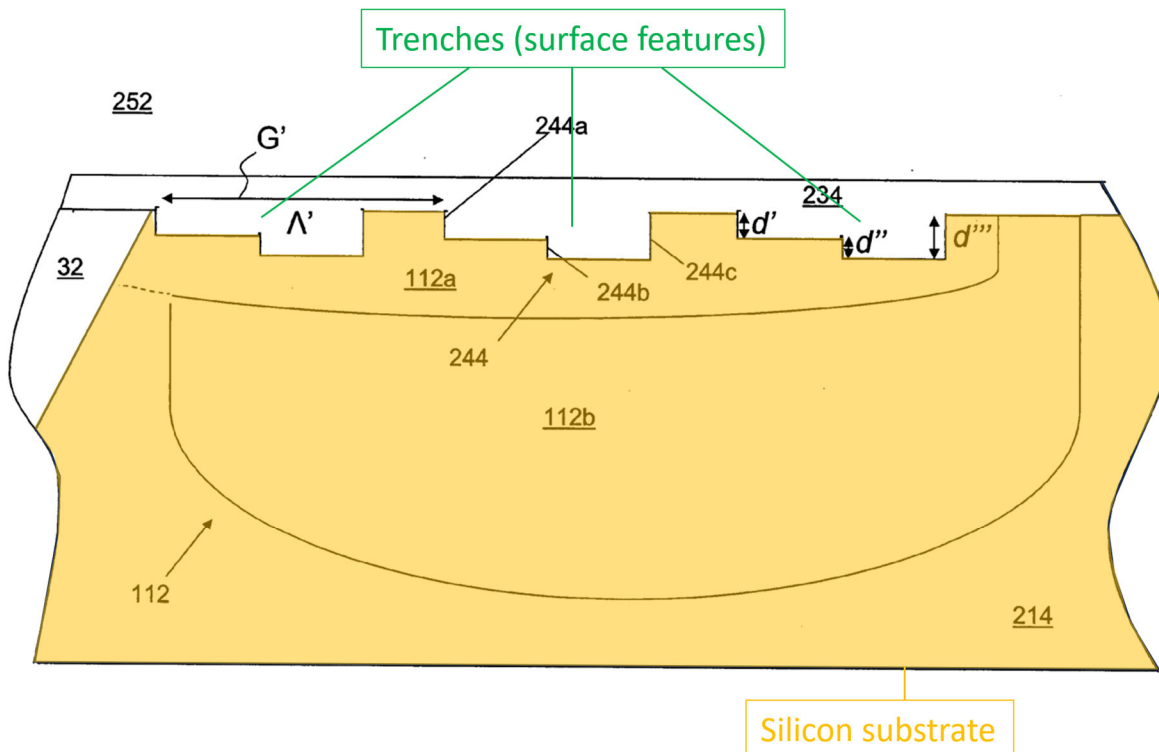


FIG. 11

Baggenstoss, Fig. 11 (annotated).

As shown in Figure 11, the trenches 244 have two different depths (i.e., the claimed heights). Baggenstoss, [0043]. Thus, the surface features are not uniform in height, as required by this limitation. Ex-1004 ¶288.

Baggenstoss discloses that its trenches can be formed by chemical etching. Baggenstoss, [0038], [0043]; *see also* Ex-1004 ¶289. Typically, two masks would be required to etch the two different depths of the trenches 244. Ex-1004 ¶289.

It would have been obvious to use Baggenstoss's trenches 244 as Alie's surface features, with a reasonable expectation of success, as discussed in Section VIII.B.11 below. Ex-1004 ¶290.

4. Claim 21

a) “The device of claim 1, wherein said plurality of surface features comprise multiple etched levels.”

Alie in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶292-96.

As discussed above regarding claim 13, Baggenstoss discloses trenches 244 (i.e., the claimed surface features) with two different depths. Baggenstoss, [0043]; *see also* Ex-1004 ¶293.

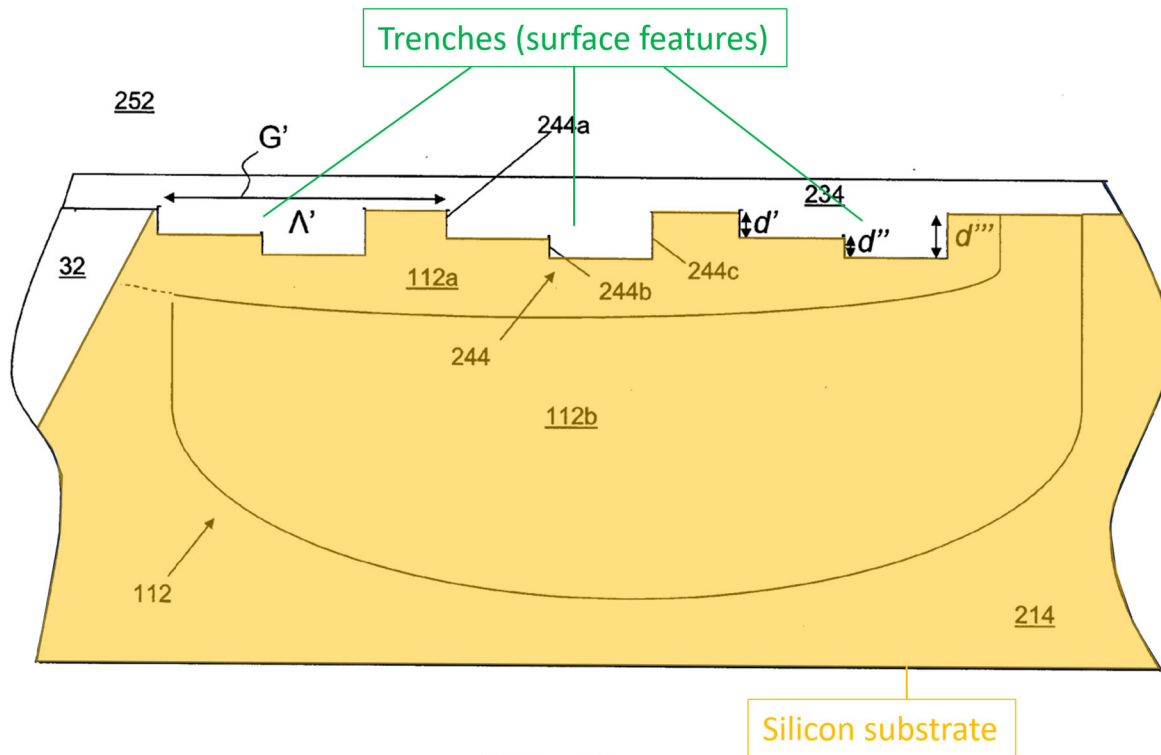


FIG. 11

Baggenstoss, Fig. 11 (annotated).

The different depths correspond to the claimed multiple etched levels because Baggenstoss's trenches 244 can be formed via chemical etching. Baggenstoss, [0038], [0043]; *see* Ex-1004 ¶294. Typically, two masks would be required to etch the two different depths of the trenches 244. Ex-1004 ¶294.

It would have been obvious to use Baggenstoss's trenches 244 as Alie's surface features, with a reasonable expectation of success, as discussed in Section VIII.B.11 below. Ex-1004 ¶295.

5. **Claim 24**

- a) **“The device of claim 1, wherein the pattern is an at least substantially uniform grid.”**

Alie in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶297-301.

As discussed above regarding claim 1, Figure 4 of Baggenstoss depicts a grated interface formed by trenches 144 (i.e., the claimed surface features). Baggenstoss, [0031]-[0032]; *see also* Ex-1004 ¶298.

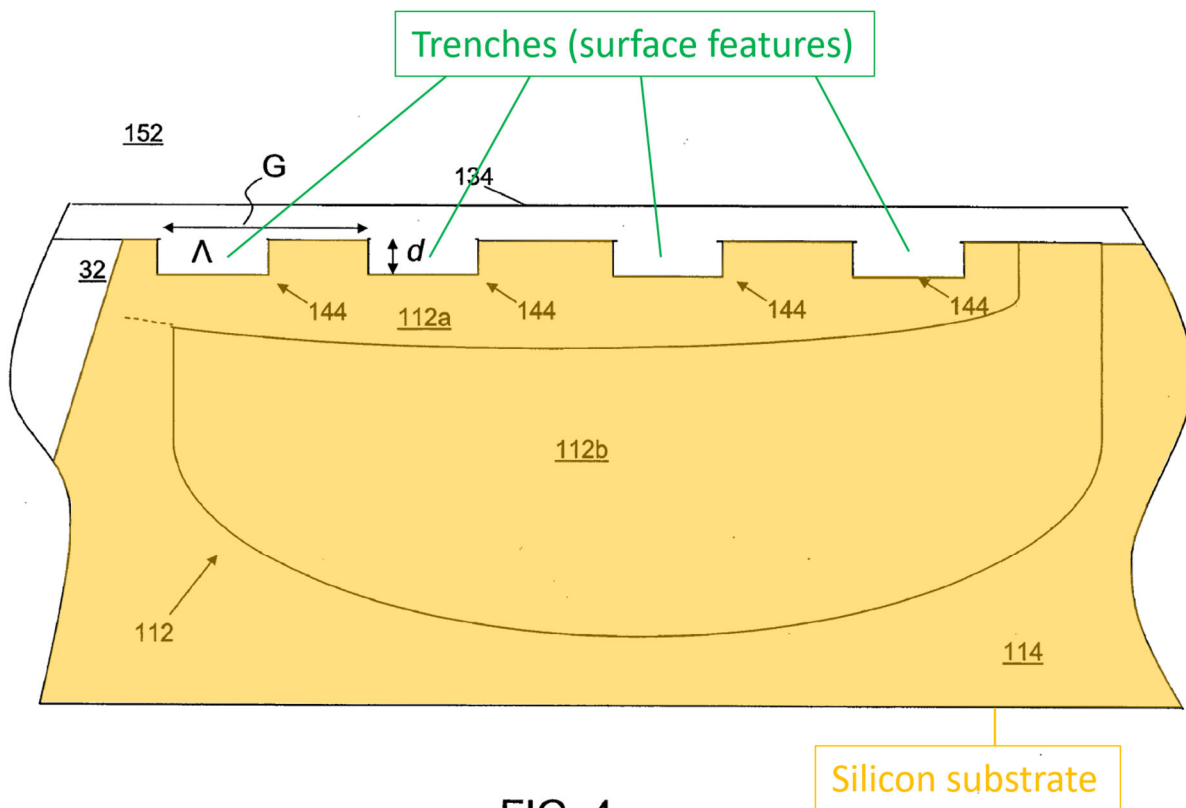


FIG. 4

Baggenstoss, Fig. 4 (annotated).

“Each grating (measured as the distance from the beginning of one trench 144 to the beginning of the next trench 144 (shown by arrow G) has a predetermined period that is represented by Λ ,” i.e., the trenches form the claimed substantially uniform grid. Baggenstoss, [0032]; *see also* Ex-1004 ¶299. The provisional application for the ’737 patent identifies such gratings as an example of a “uniform grid pattern.” Ex-1003, 13:3-4 (“[A]s is shown in FIG. 5 for example, the shallow trench isolation can be a *uniform grid pattern* comprised of [trenches] that form *a series of spaces and lines* or pillars.”).

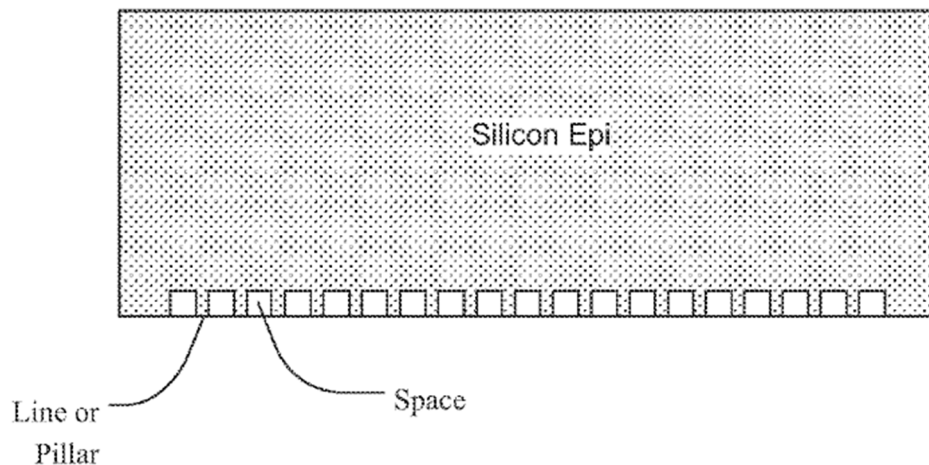


FIG. 5

Ex-1003, Fig. 5.

It would have been obvious to use Baggenstoss’s trenches 144 as Alie’s surface features, with a reasonable expectation of success, as discussed in Section VIII.B.11 below. Ex-1004 ¶300.

6. Claim 30

- a) “The method of claim 26, wherein the surface features are formed by shallow trench isolation etching.”**

Alie in view of Baggenstoss renders this limitation obvious under Patent Owner’s proposed construction in the Related Case. Ex-1004 ¶¶302-07.

In the Related Case, Petitioner proposed that the term “shallow trench isolation etching” is indefinite. Ex-1013, 4. Patent Owner proposed that the term has a plain and ordinary meaning, and to the extent a construction is required, it means, “etching a pattern of shallow trenches.” Ex-1014, 4; Ex-1015, 2-3.

As discussed above regarding claim 1, Figure 4 of Baggenstoss depicts a grated interface formed by trenches 144 (i.e., the claimed surface features). Baggenstoss, [0031]-[0032]; *see also* Ex-1004 ¶304.

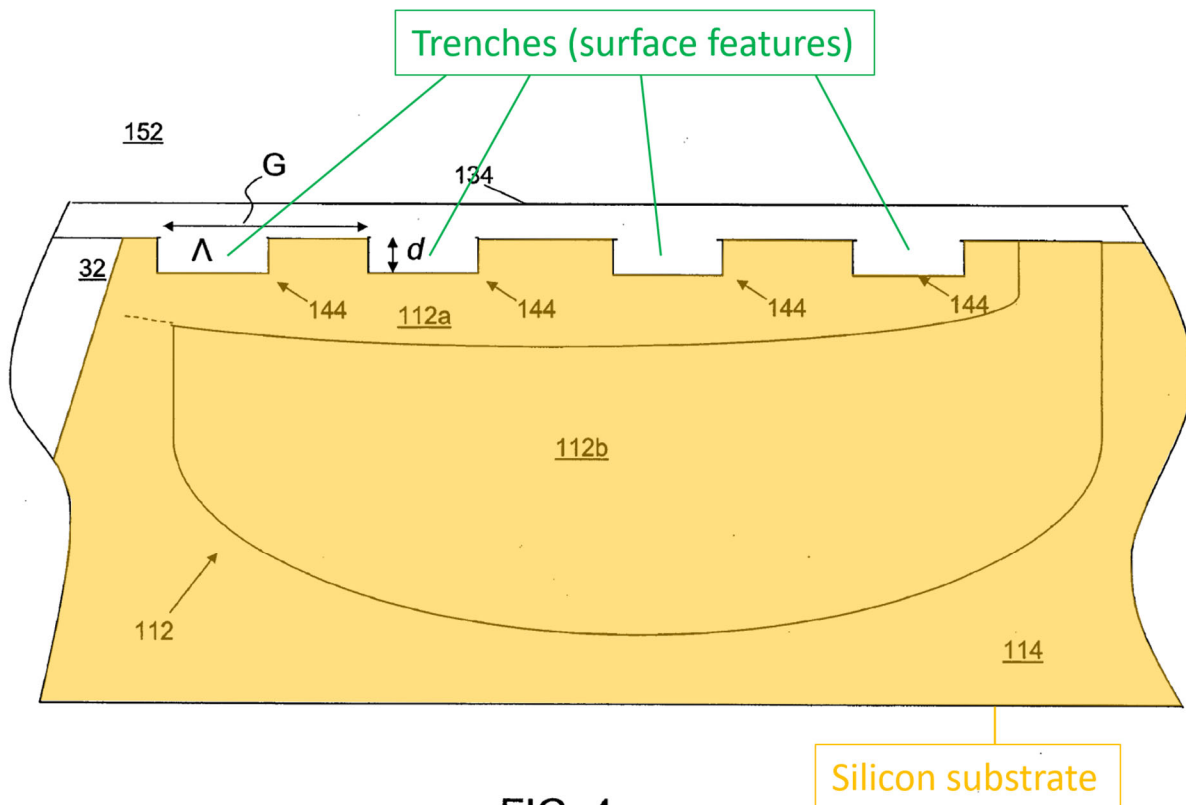


FIG. 4

Baggenstoss, Fig. 4 (annotated).

Baggenstoss discloses that its trenches can be formed by chemical etching, Baggenstoss, [0038], and have a depth of 100 nm. Baggenstoss, [0034]. 100 nm or 0.1 micron is even shallower than 0.35 microns that the '737 patent states is associated with “standard STI [shallow trench isolation] processes.” '737 patent, 11:24-26; *see also* Ex-1004 ¶305.

It would have been obvious to use Baggenstoss's trenches 144 (that is formed by etching) as Alie's surface features, with a reasonable expectation of success, as discussed in Section VIII.B.11 below. Ex-1004 ¶306.

7. Claim 43

- a) **“The device of claim 32, wherein the surface features have a substantially uniform height.”**

Alie in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶308-

09.

See claims 12 and 32.

8. Claim 44

- a) **“The device of claim 32, wherein the surface features are not uniform in height.”**

Alie in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶310-

11.

See claims 13 and 32.

9. Claim 51

- a) **“The device of claim 32, wherein said plurality of surface features comprise multiple etched levels.”**

Alie in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶312-

13.

See claims 21 and 32.

10. Claim 54

- a) **“The device of claim 32, wherein the surface features are arranged according to a pattern that is an at least substantially uniform grid.”**

Alie in view of Baggenstoss renders this limitation obvious. Ex-1004 ¶¶314-

15.

See claims 24 and 32.

11. Motivation to combine Alie and Baggenstoss

It would have been obvious to combine Alie with Baggenstoss. Ex-1004 ¶¶316-20.

A POSITA would have been motivated to use Baggenstoss's trenches for Alie's surface features. Ex-1004 ¶317. Baggenstoss teaches that its grated interface formed of trenches "allows a greater percentage of incident light to be captured, which is a vast improvement over the art." Baggenstoss, [0014]; *see also KSR*, 550 U.S. at 418. Baggenstoss explains that its grated interface "serves to create a hybrid index of refraction ... thereby decreasing the percentage of incident light reflection." Baggenstoss, [0031]. With the grated interface formed of trenches 144, the incident light reflection is "nearly eliminated" with a trench depth d of 100 nm. Baggenstoss, [0035]. The "blazed" gratings formed of trenches 244 can decrease the incident light reflection even further. Baggenstoss, [0042]-[0043]. Whether to use Baggenstoss's trenches 144 or 244 would have depended on the particular design needs regarding the cost of manufacture and the desired amount of reduction in incident light reflection. Ex-1004 ¶317.

Using Baggenstoss's trenches would have been a use of known technique to improve similar devices in the same way. *KSR*, 550 U.S. at 417; Ex-1004 ¶318. Both Alie and Baggenstoss disclose photodetectors. Alie, Abstract, [0006]; Baggenstoss,

[0014], [0009]. Both Alie and Baggenstoss have the same goal of improving the efficiency of photodetectors in capturing incident light. Alie, [0068]; Baggenstoss, [0014]. Both Alie and Baggenstoss achieve that goal by using a textured region including surface features arranged as gratings. Alie, [0068]; Baggenstoss, [0031]-[0032], [0042]. Both Alie and Baggenstoss disclose placing the textured region on the light incident side. Alie, [0094] (“Additional scattering can be provided by positioning a textured forward scattering layer on the side of the device that receives incident electromagnetic radiation.”); Baggenstoss, [0038], Fig. 3 (depicting light source 38 on the side of the grated interface). Both Alie and Baggenstoss disclose forming the surface features using chemical etching. Alie, [0074]; Baggenstoss, [0038].

It would have been a simple substitution of one known element (i.e., Alie’s surface features) for another (Baggenstoss’s trenches) to obtain predictable results. *KSR*, 550 U.S. at 417; Ex-1004 ¶319. Baggenstoss teaches that incident light reflection is decreased due to its grated interface formed of trenches serving to create a “hybrid index of refraction.” Baggenstoss, [0031]. Baggenstoss even provides measurements of incident light reflection based on various dimensions of its trenches and their arrangements into gratings. Baggenstoss, Figs. 5A & 5B.

A POSITA would have had a reasonable expectation of success. Ex-1004 ¶320. It would have been well within the abilities of a POSITA to use Baggenstoss’s

trenches for Alie's surface features, given that it would have involved routine manufacturing steps, such as chemical etching, that Alie was already using for its surface features. Alie, [0074]; *see also* Ex-1004 ¶320.

C. Ground 3: Claims 16, 32-42, and 44-55 Are Obvious Based on Alie and Jiang

To the extent that the Board finds that Alie does not disclose or render obvious a device exhibiting “a quantum efficiency of at least about 35% for electromagnetic radiation at a wavelength of about 940 nm,” and that therefore, Alie does not disclose or render obvious claims 16, 32-42, and 44-55, Alie in view of Jiang renders them obvious. Ex-1004 ¶¶321-25.

Like the '737 patent, Alie discloses using a textured region in a photodetector to increase quantum efficiency, particularly for infrared light, Alie, [0070], which includes light with a wavelength of 940 nm, Ex-1029, 807. A POSITA would have known that the increased quantum efficiency is at least about 35% for electromagnetic radiation at a wavelength of about 940 nm, as required by this limitation. Ex-1004 ¶322. At a minimum, it would have been obvious for a POSITA to ensure that Alie's device achieves a quantum efficiency of at least about 35% for electromagnetic radiation at a wavelength of about 940 nm, because as Alie teaches, an increase in the quantum efficiency “lead[s] to an improved signal to noise ratio.” Alie, [0070]; *see also* Ex-1012, [0050] (“Any increase in the quantum efficiency makes a large difference in the signal to noise ratio.”); *KSR*, 550 U.S. at 418; Ex-

1004 ¶322. A POSITA would have looked to Jiang's teaching that a device similar to Alie's device achieves a quantum efficiency well over the claimed 35%, at around 70% for electromagnetic radiation at a wavelength of about 940 nm. Jiang, 1:32-35, 16:19-23; *see also* Ex-1004 ¶322.

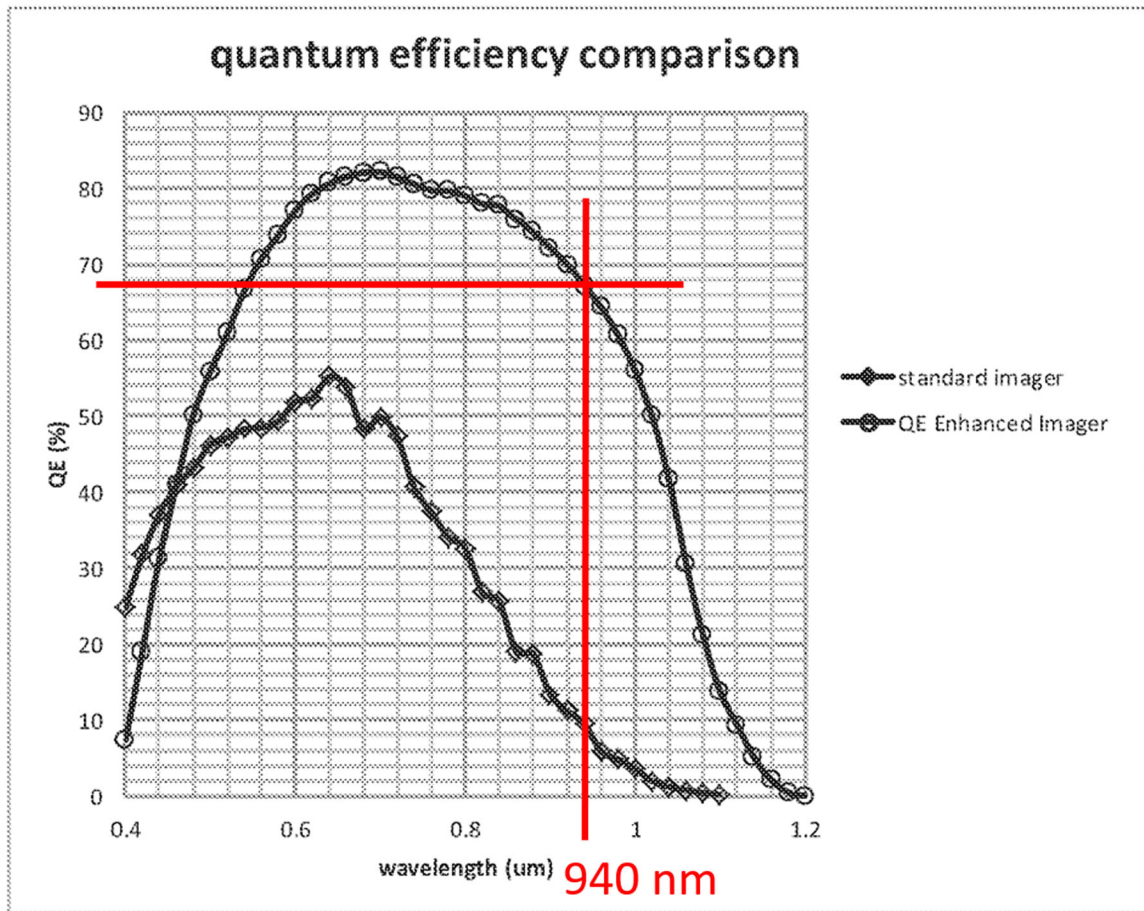


FIG. 15

Jiang, Fig. 15 (annotated).

Matching Jiang's quantum efficiency numbers would have involved a use of known technique to improve similar devices in the same way. *KSR*, 550 U.S. at 417; Ex-1004 ¶323. Alie discloses using a textured region in a photodetector to increase

quantum efficiency, particularly for infrared light, Alie, [0070], which includes light with a wavelength of 940 nm. Similarly, Jiang discloses using a textured region in a photodetector to increase quantum efficiency for infrared light. Jiang, 1:25-34, 11:1-4. Like Alie's textured region, Jiang's textured region can be on the light incident side. Jiang, 19:15-19. And like Alie's textured region, Jiang's textured region can be formed by chemical etching. Jiang, 5:13-17.

A POSITA would have had a reasonable expectation of success in achieving a quantum efficiency of at least about 35% for electromagnetic radiation at a wavelength of about 940 nm. Ex-1004 ¶324. First, this understanding is consistent with the disclosure of the '737 patent, which does not identify any exact combination of the disclosed features that achieves the required quantum efficiency, but rather, assumes that a POSITA would know how to achieve the claimed quantum efficiency. Ex-1004 ¶324. Second, as discussed above, Jiang has shown that a device similar to Alie's device achieves a quantum efficiency well over the claimed 35%. Jiang, 13:32-14:2, Fig. 15; *see* Ex-1004 ¶324.

D. Ground 4: Claims 25 and 55 Are Obvious Based on Alie and Haddad204

1. Claim 25

- a) **“The device of claim 1, wherein the pattern is a non-uniform arrangement.”**

Alie in view of Haddad204 renders this limitation obvious. Ex-1004 ¶¶326-32.

As discussed above regarding limitation 1[b] in Ground 1, Alie discloses a photodetector with a textured region. Alie, [0052], [0096], [0006]; *see also* Ex-1004 ¶327. Alie discloses that its textured region can include surface features such as pillars. Alie, [0068].

Similarly, Haddad204 discloses a photodetector with a textured region including surface features such as pillars. Haddad204, [0073], [0053]. Importantly, Haddad204 discloses “a plurality of pillars of variable sizes ... arranged in a non-uniform array.” Haddad204, [0112]; *see also* Ex-1004 ¶328. Figure 9a shows a top view and Figure 9b shows a cross-sectional view of such “pillars etched into a semiconductor material.” Haddad204, [0112].

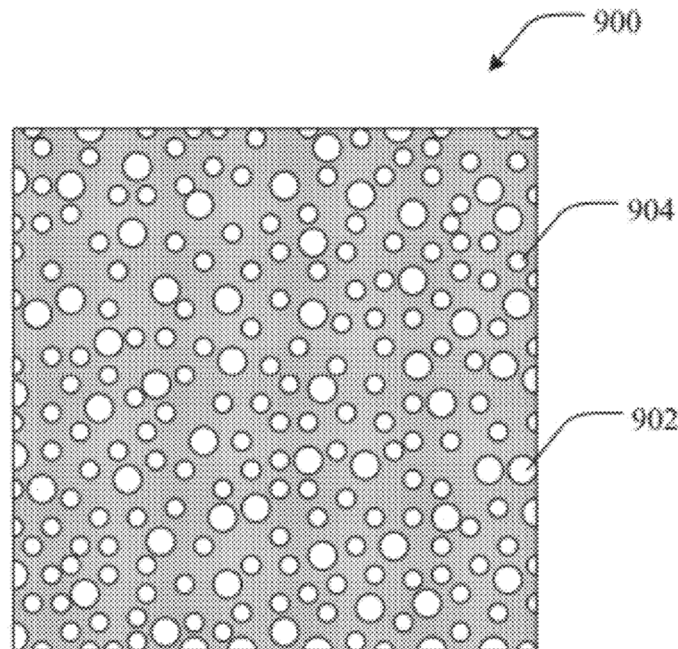


FIG. 9a

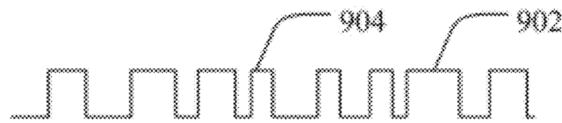


FIG. 9b

Haddad204, Figs. 9a-b.

It would have been obvious to use Haddad204's non uniform arrangement of pillars for Alie's arrangement of pillars because Haddad204 teaches that its surface features "increase the effective absorption length of the photosensitive pixel," which in turn, increases the quantum efficiency. Haddad204, [0073], [0076]; *see also* KSR, 550 U.S. at 418; Ex-1004 ¶329. Increasing quantum efficiency using surface features is the same goal shared by Alie. Alie, [0070]. Haddad204 teaches that "[a]ny increase in the quantum efficiency makes a large difference in the signal to noise ratio." Haddad204, [0058]. Alie similarly teaches that an increase in the quantum efficiency "lead[s] to an improved signal to noise ratio." Alie, [0070].

It would also have been a use of known technique (i.e., Haddad204's non uniform arrangement) to improve similar devices in the same way. KSR, 550 U.S. at 417; Ex-1004 ¶330. Both Alie and Haddad204 are SiOnyx's patent applications that share the same two joint inventors: Jeffrey McKee and Chintamani Palsule. Both Alie and Haddad204 concern photodetectors with textured regions that increase quantum efficiency. Alie, [0068], [0006]; Haddad204, [0073], [0053]. The textured regions in both references include similarly shaped surface features such as pillars.

Alie, [0068]; Haddad204, [0073]. The textured regions in both references can be formed by chemical etching. Alie, [0074]; Haddad204, [0093].

A POSITA would have had a reasonable expectation of success. Ex-1004 ¶331. It would have been well within the abilities of a POSITA to use Haddad204's non uniform arrangement of pillars for Alie's arrangement of pillars, given that it would have involved routine manufacturing steps that Haddad204 had already used in its device with predictable results. Ex-1004 ¶331.

2. Claim 55

- a) **“The device of claim 32, wherein the surface features are arranged according to a pattern that is a non-uniform arrangement.”**

Alie in view of Haddad204 renders this limitation obvious. Ex-1004 ¶¶333-34.

See claims 25 and 32.

E. Ground 5: Claims 25 and 55 Are Obvious Based on Alie and Park

1. Claim 25

- a) **“The device of claim 1, wherein the pattern is a non-uniform arrangement.”**

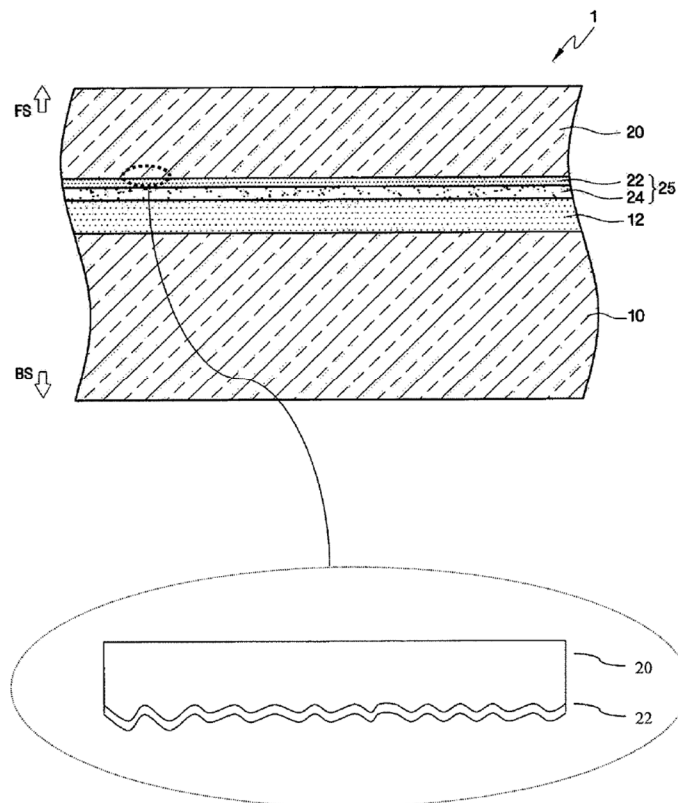
Alie in view of Park renders this limitation obvious. Ex-1004 ¶¶335-41.

As discussed above regarding limitation 1[b] in Ground 1, Alie discloses a photodetector with a textured region. Alie, [0052], [0096], [0006]; *see also* Ex-1004

¶336. Alie discloses that its textured region can include surface features such as protrusions. Alie, [0068].

Similarly, Park discloses a photodetector with a textured region including surface features with protrusions. Park, [0072] (“Referring to the inset in FIG. 1 ... reflections may also be reduced by processing the second substrate 20 to have an *uneven surface* facing the oxide layer 22.”), Fig. 8D-2(f); Ex-1004 ¶337.

FIG. 1



Park, Fig. 1. “The oxide layer 22 may have an uneven surface where it meets the second substrate 20.” Park, [0072]. “The oxide layer 22 may also have an uneven surface at the opposing surface.” Park, [0072]. As its name suggests, and as depicted

in Figure 1, Park's uneven surface has protrusions in a non-uniform arrangement. Ex-1004 ¶337.

It would have been obvious to use Park's uneven surface in place of, or in addition to, Alie's surface features because Park teaches that the uneven surface helps with absorbing incident light by reducing reflection. Park, [0072]; *see also KSR*, 550 U.S. at 418; Ex-1004 ¶338. Decreasing reflection of incident light means more light entering the silicon substrate to be absorbed. Ex-1004 ¶338. Alie teaches that increased absorption of incident light increases quantum efficiency, Alie, [0068], and that an increase in the quantum efficiency "lead[s] to an improved signal to noise ratio." Alie, [0070]. Based on the teachings of Park and Alie, a POSITA would have been motivated to use Park's uneven surface. Ex-1004 ¶338.

It would have been a use of known technique (i.e., Park's uneven surface) to improve similar devices in the same way. *KSR*, 550 U.S. at 417; Ex-1004 ¶339. Both Alie and Park concern increasing quantum efficiency of photodetectors. Alie, [0068], [0070], [0006]; Park, [0004]-[0005], Fig. 8D-2(f). To achieve this goal, Alie uses a textured region with protrusions and Park similarly uses an uneven surface with protrusions. Alie, [0068]; Park, [0072]. Both Alie and Park disclose placing the textured region or the uneven surface on the light incident side. Alie, [0094] ("Additional scattering can be provided by positioning a textured forward scattering

layer on the side of the device that receives incident electromagnetic radiation.”); Park, Figs. 1, 7.

A POSITA would have had a reasonable expectation of success. Ex-1004 ¶340. It would have been well within the abilities of a POSITA to use Park’s non uniform arrangement of protrusions for Alie’s arrangement of protrusions, given that it would have involved routine manufacturing steps that Park had already used in its device with predictable results. Ex-1004 ¶340.

2. Claim 55

- a) **“The device of claim 32, wherein the surface features are arranged according to a pattern that is a non-uniform arrangement.”**

Alie in view of Park renders this limitation obvious. Ex-1004 ¶¶342-43.

See claims 25 and 32.

IX. SECONDARY CONSIDERATIONS

Petitioner is unaware of evidence of secondary considerations of non-obviousness. Petitioner reserves the right to rebut any purported objective evidence of non-obviousness raised by SiOnyx.

X. THE BOARD SHOULD NOT USE ITS DISCRETION TO DENY INSTITUTION

A. 35 U.S.C. § 314(a)

The Board should not exercise its discretion to deny institution under 35 U.S.C. §314(a). No other petitions have been filed against the ’737 patent and thus the

General Plastic factors for serial petitions do not weigh against institution. The existence of a parallel ITC proceeding should not be a factor for consideration in determining whether the Board may exercise its discretion to deny institution. *See* Vidal, K., Memorandum—Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, USPTO (June 21, 2022) (“Interim Procedure”) at 6-7, https://www.ptabbar.org/docs/USPTO_Guidance_on_Discretionary_Denials_2_June_30_2022.pdf (“The PTAB will not discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding”). As for the parallel district court case, it has been stayed. Discretionary denial is further inappropriate here because this petition presents compelling evidence of unpatentability. Accordingly, the *Fintiv* factors should not be applied to deny institution of this proceeding.

B. 35 U.S.C. § 325(d)

The Board likewise should not deny institution under §325(d). When evaluating discretionary denial arguments under §325(d), the Board reviews: “(1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.” *Advanced Bionics, LLC v. Med-El*

Elektromedizinische Geräte GmbH, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020) (precedential). In applying this test, the Board considers the “*Becton, Dickinson*” factors, *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017) (precedential as to § III.C.5, first paragraph) (“*Becton, Dickinson*”).

Here, the first prong of *Advanced Bionics* is not satisfied. The primary reference Alie was not listed on an IDS or otherwise cited in the file history. Alie is not the same or substantially the same art previously presented to the Office, and also does not involve the same or substantially the same arguments previously presented to the Office. (The secondary reference Haddad204 and a parent application of the secondary reference Baggenstoss were listed in an IDS along with over 1,000 other documents, but were not substantively argued or otherwise meaningfully addressed during examination.³) Accordingly, any analysis by the Board of 325d issues should end with prong 1. *See, e.g., Fusion Orthopedics, LLC*

³ The Office has proposed changing this aspect of the §325(d) analysis. *See USPTO Notice of Proposed Rulemaking* [including Rules for 325(d) Considerations], 89 Fed. Reg. 28,693, 28,705 (Apr. 19, 2024) (“An initialed Information Disclosure Statement, without more, does not satisfy [the proposed §325(d) discretionary denial] standard.”).

v. Extremity Medical, LLC, IPR2023-00894, Paper 15 at 34-35 (P.T.A.B. Nov. 17, 2023).

Even were the Board to reach the second prong, it too is not met. The petition reflects the examiner's errors in a manner material to the patentability of the Challenged Claims. Under *Becton, Dickinson* factor (c), the secondary reference Haddad204 and a parent application of the secondary reference Baggenstoss were listed in an IDS but were not the basis for rejection. The examiner did not and could not have substantively considered them in connection with the primary reference Alie. Furthermore, under *Becton, Dickinson* factor (f), the examiner erred by overlooking the materiality of the secondary reference Haddad204 and a parent application of the secondary reference Baggenstoss to the Challenged Claims during examination. *See, e.g., STMicroelectronics, Inc. v. Trustees of Purdue Univ.*, IPR2022-00309, Paper 14 at 12–13 (P.T.A.B. July 6, 2022).

XI. CONCLUSION

Petitioner respectfully requests *inter partes* review and cancellation of the Challenged Claims of the '737 patent.

Date: September 24, 2024

Respectfully submitted,

By: /Scott C. Weidenfeller/

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Petition for *Inter Partes* Review of U.S. Pat. No. 11,069,737

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CERTIFICATION OF WORD COUNT

I certify that the foregoing complies with the type-volume limitation of 37 C.F.R. § 42.24 and contains 13,936 words based on the word count indicated by the word-processing system used to prepare the paper, and excluding those portions exempted by § 42.24(a).

Date: September 24, 2024

/Scott C. Weidenfeller/

Scott C. Weidenfeller (Reg. No. 54,531)

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6 and 42.105, I hereby certify that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 11,069,737 under U.S.C. §§ 311–319 and 37 C.F.R. § 42.100 *et seq.*, together with its supporting exhibits, and Power of Attorney was served by Federal Express, a means at least as fast and reliable as Priority Mail Express®, on the following correspondence address of record for patent owner:

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