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(54) **PROCESS MODULE FOR INCREASING THE RESPONSE OF BACKSIDE ILLUMINATED PHOTOSENSITIVE IMAGERS AND ASSOCIATED METHODS**

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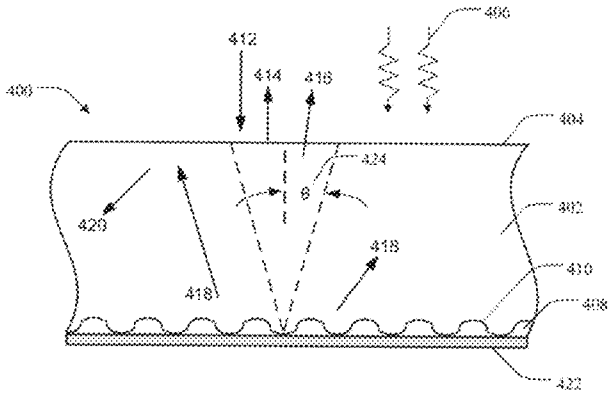
(57) **ABSTRACT**

Backside illuminated photosensitive devices and associated methods are provided. In one aspect, for example, a backside-illuminated photosensitive imager device can include a semiconductor substrate having multiple doped regions forming a least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation where the textured region includes surface features sized and positioned to facilitate tuning to a preselected wavelength of light, and a dielectric region positioned between the textured region and the at least one junction. The dielectric region is positioned to isolate the at least one junction from the textured region, and the semiconductor substrate and the textured region are positioned such that incoming electromagnetic radiation passes through the semiconductor substrate before contacting the textured region. Additionally, the device includes an electrical transfer element coupled to the semiconductor substrate to transfer an electrical signal from the at least one junction.

15 Claims, 10 Drawing Sheets



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* cited by examiner

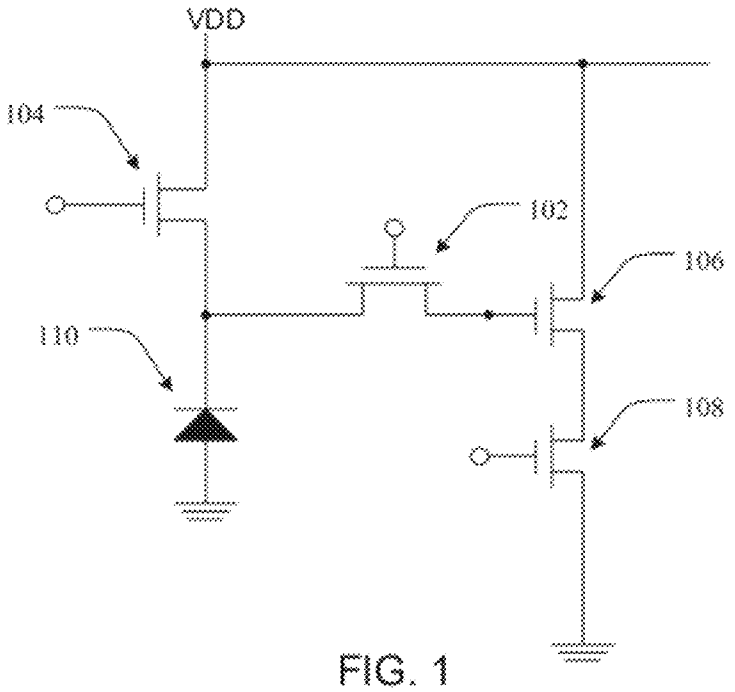


FIG. 1

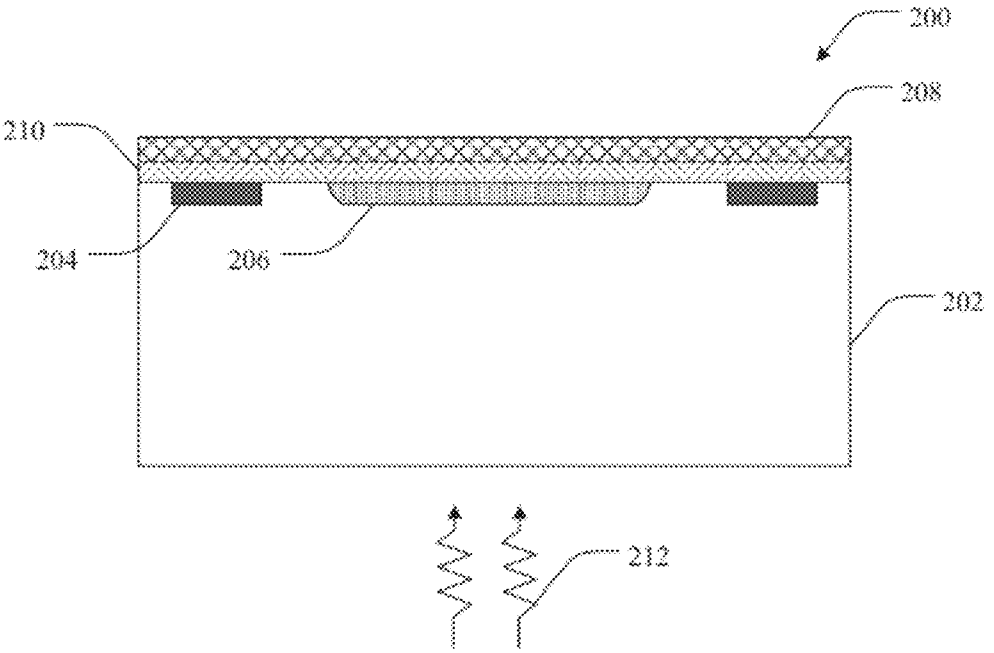


FIG. 2

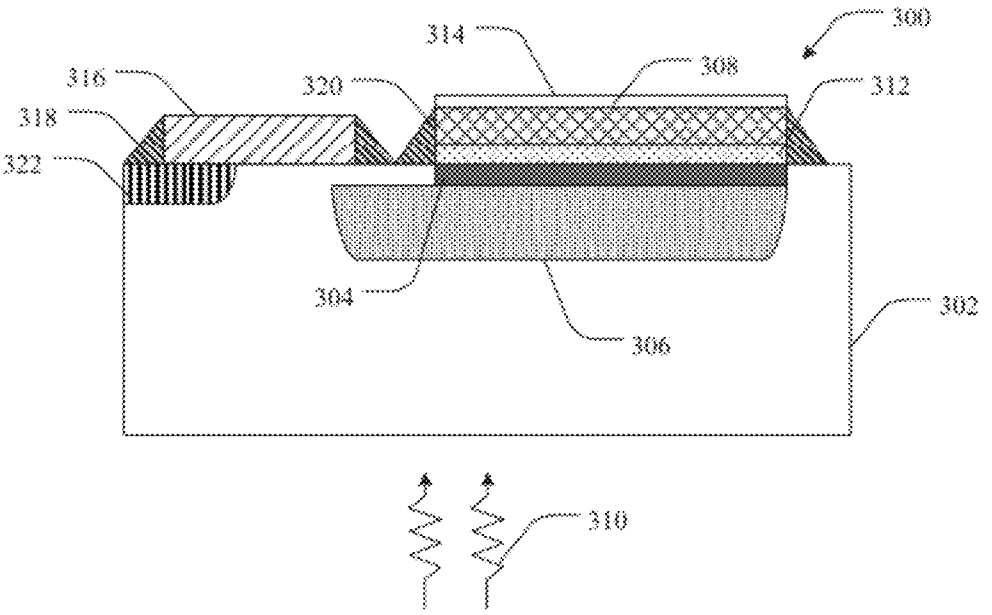

300
314
308
316
320
312
318
322
304
306
302
310

FIG. 3

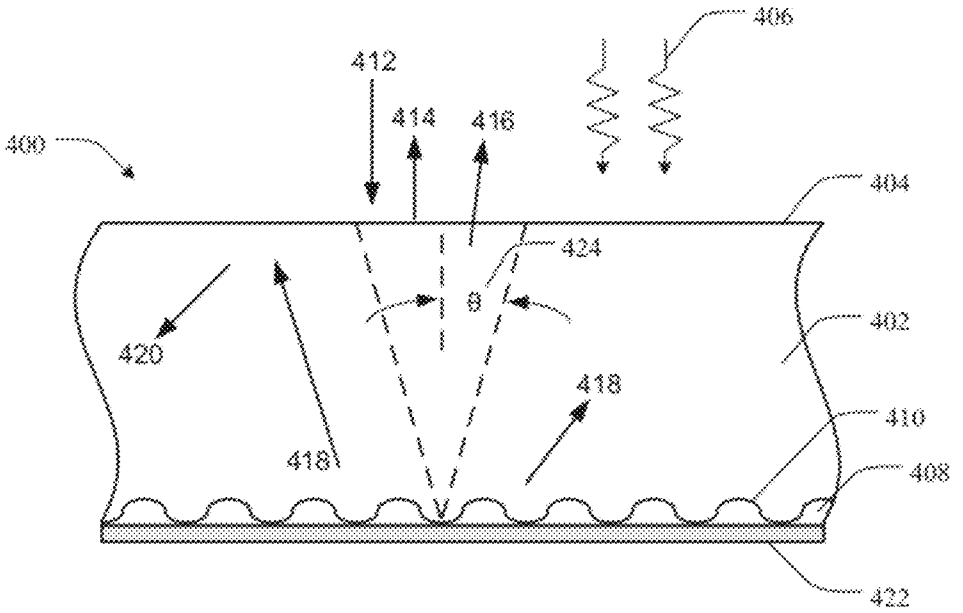

406
412
414
416
400
404
424
θ
402
420
418
418
410
408
422

FIG. 4

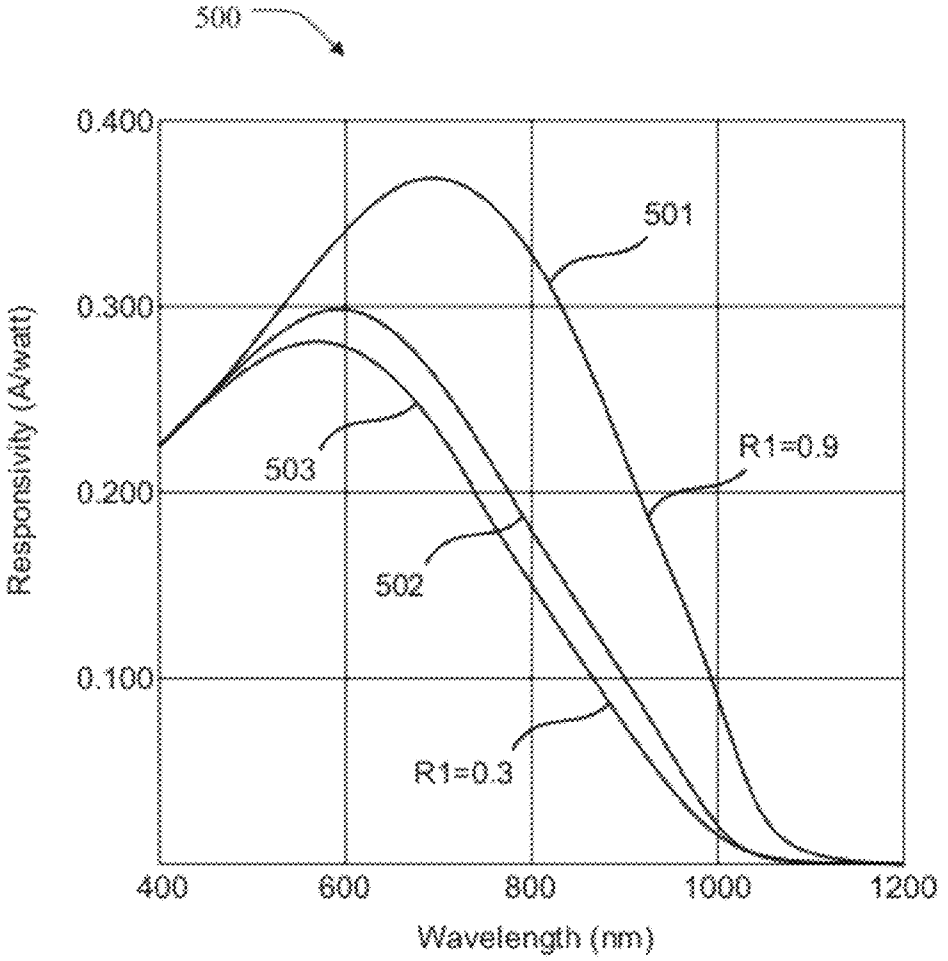
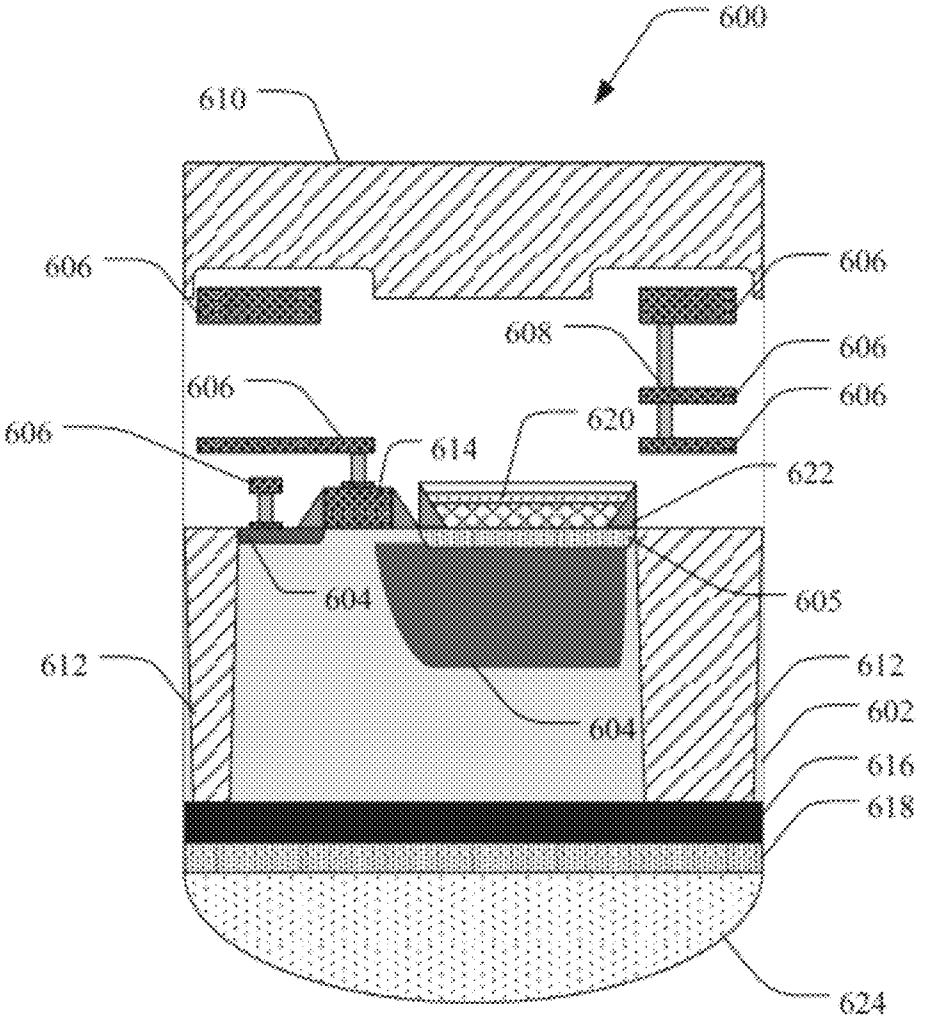

500
0.400
0.300
0.200
0.100
Responsivity (A/watt)
501
503
502
R1=0.9
R1=0.3
400
600
800
1000
1200
Wavelength (nm)

FIG. 5


600
610
606
606
608
606
606
606
606
614
620
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604
605
612
612
604
602
616
618
624

FIG. 6

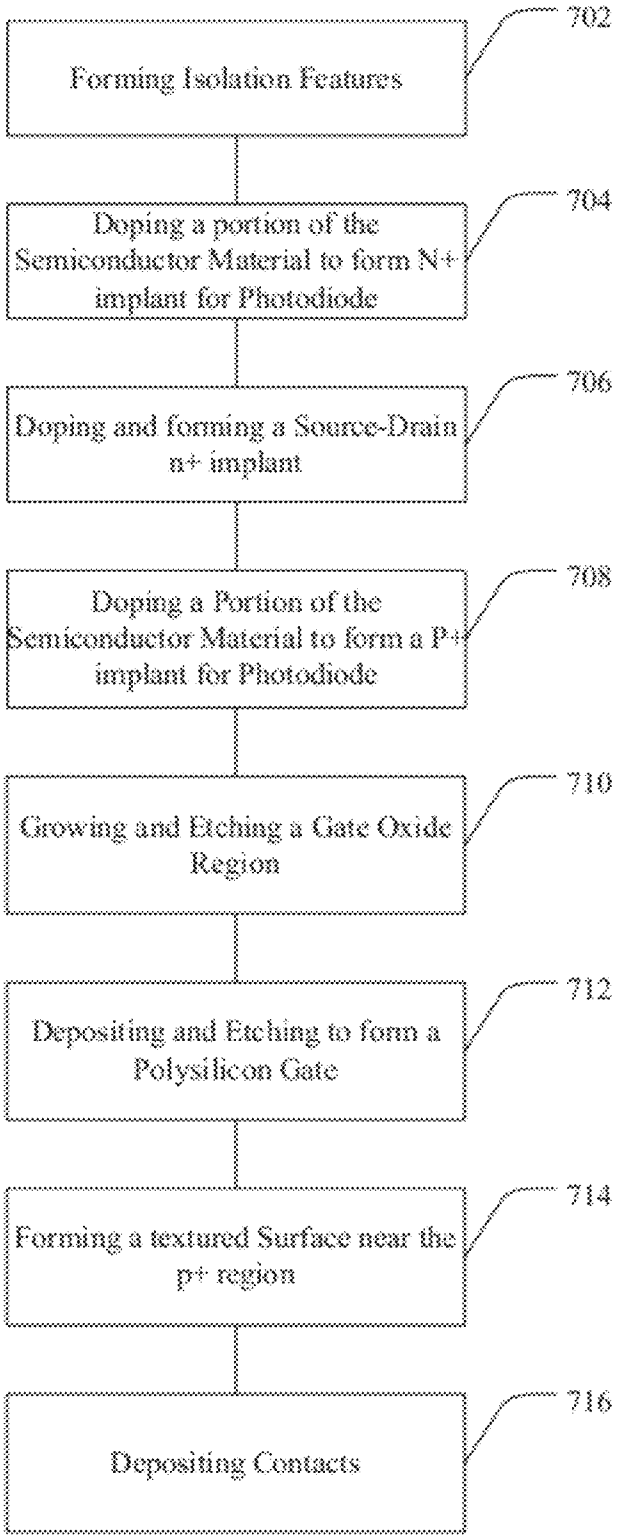
Forming Isolation Features
702
Doping a portion of the Semiconductor Material to form N+ implant for Photodiode
704
Doping and forming a Source-Drain n+ implant
706
Doping a Portion of the Semiconductor Material to form a P+ implant for Photodiode
708
Growing and Etching a Gate Oxide Region
710
Depositing and Etching to form a Polysilicon Gate
712
Forming a textured Surface near the p+ region
714
Depositing Contacts
716

FIG. 7

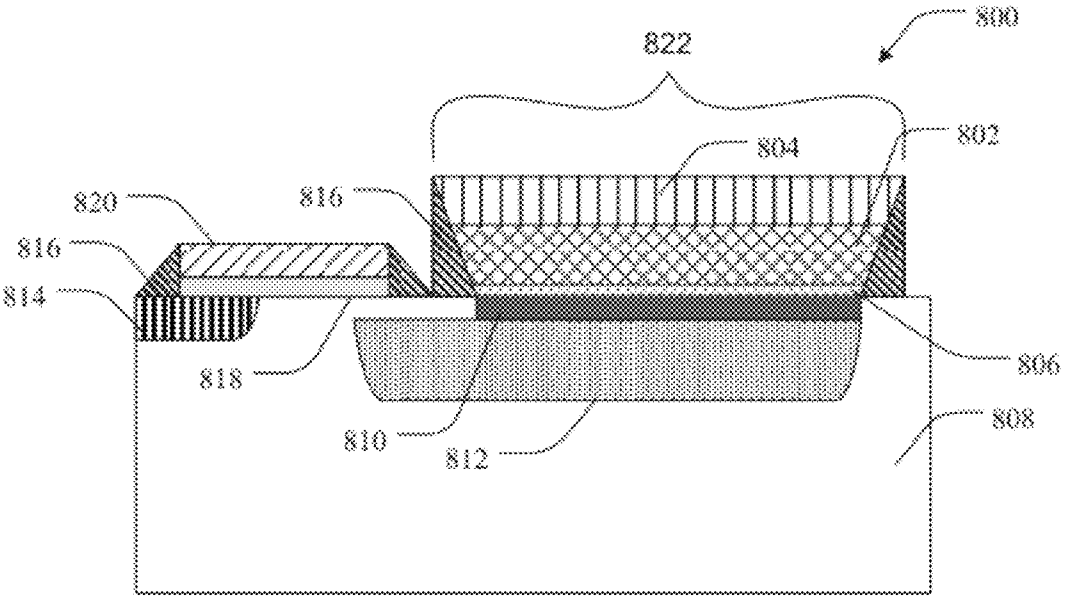
800
822
804
802
820
816
816
814
818
806
808
810
812

FIG. 8a

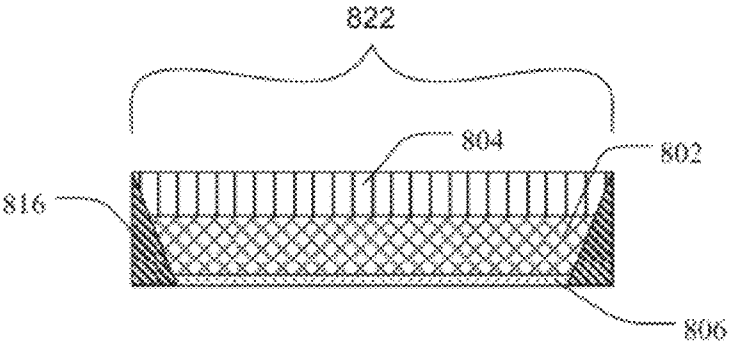
822
804
802
816
806

FIG. 8b

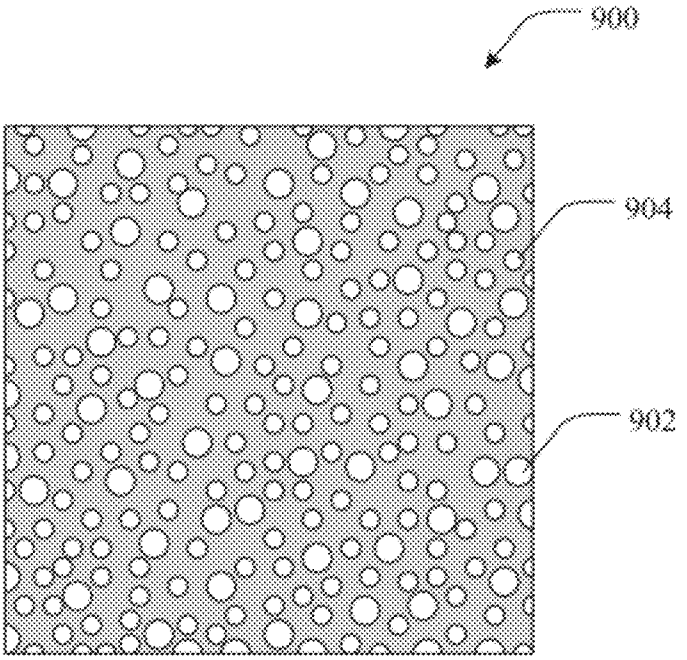

FIG. 9a

FIG. 9b

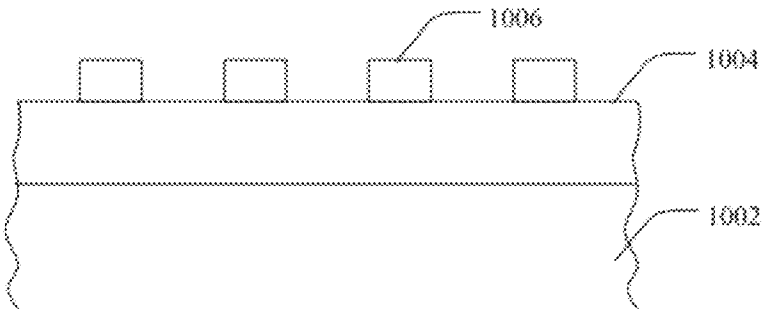

FIG. 10a

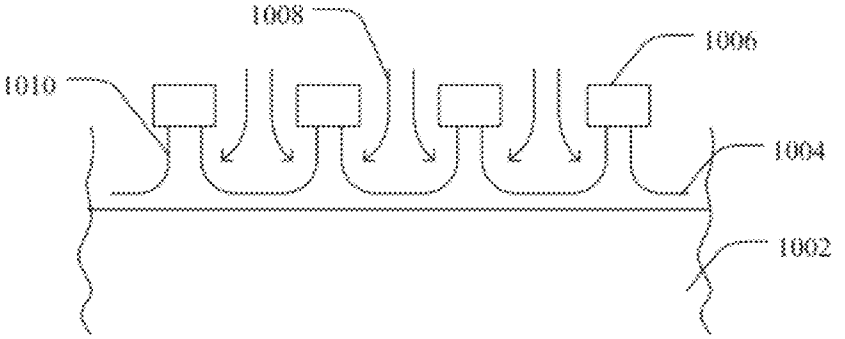

FIG. 10b

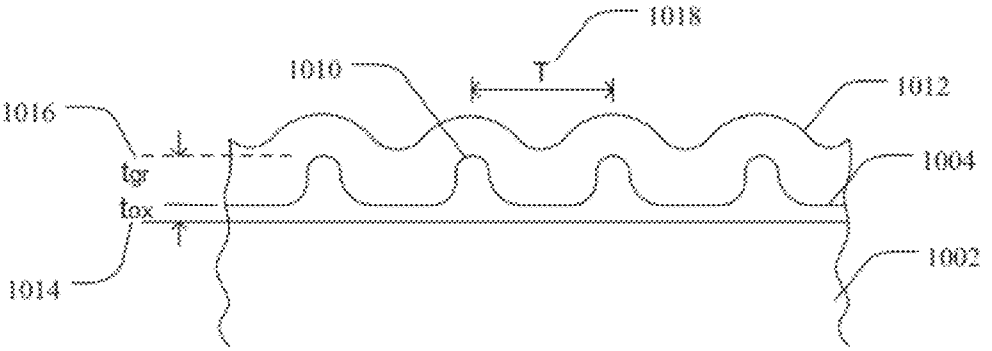

FIG. 10c

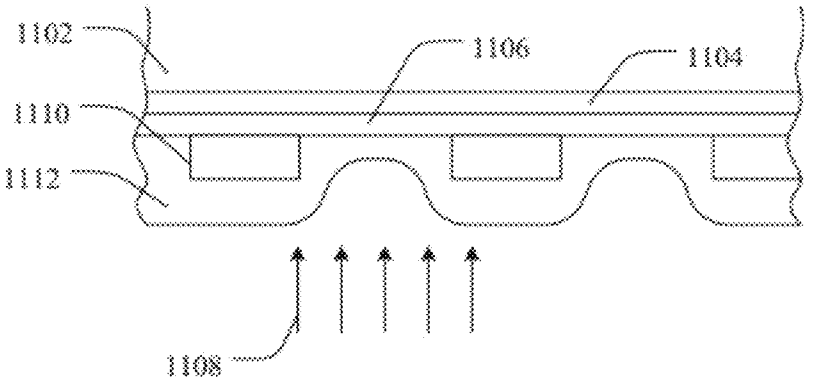

FIG. 11a

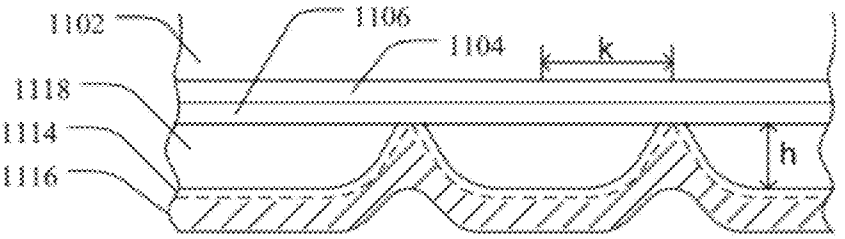

FIG. 11b

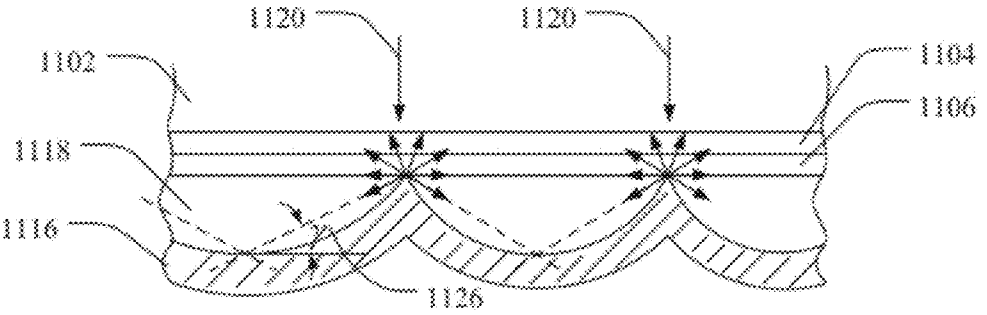

FIG. 11c

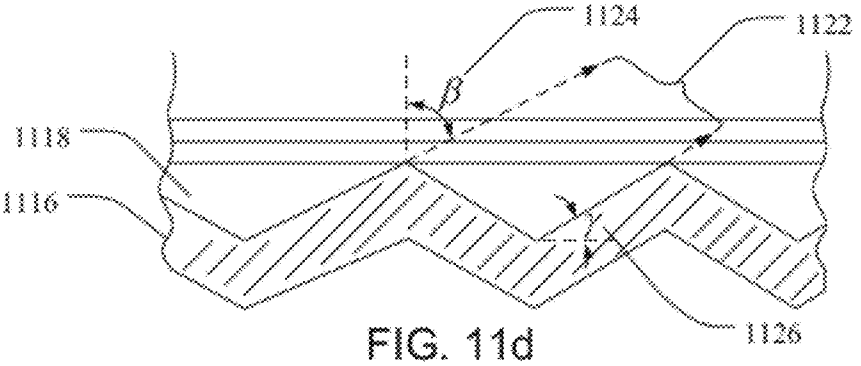

FIG. 11d

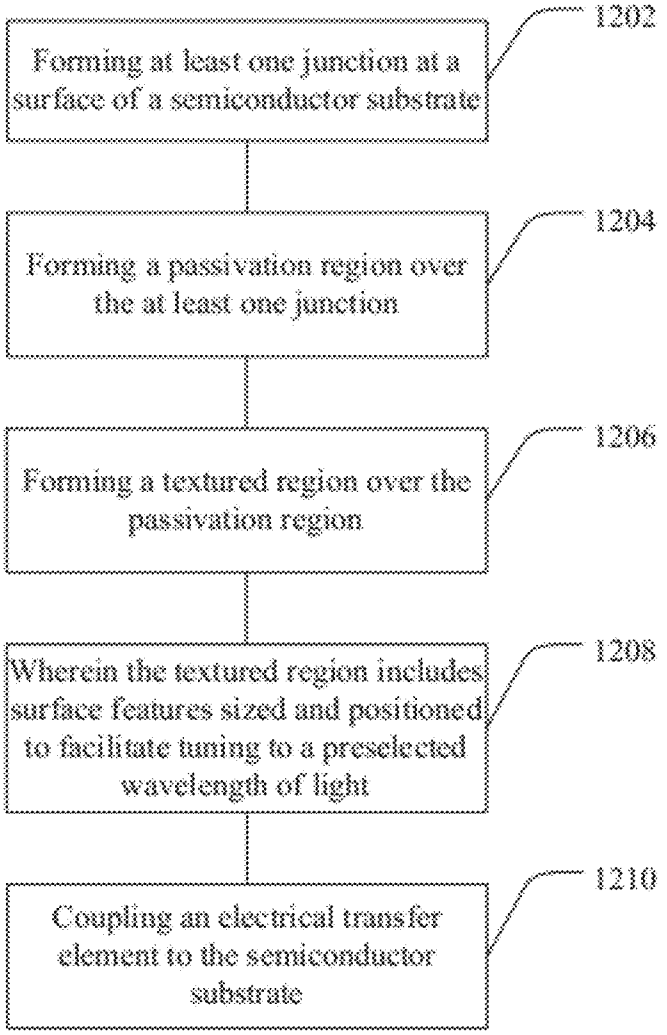
Forming at least one junction at a surface of a semiconductor substrate
1202
Forming a passivation region over the at least one junction
1204
Forming a textured region over the passivation region
1206
Wherein the textured region includes surface features sized and positioned to facilitate tuning to a preselected wavelength of light
1208
Coupling an electrical transfer element to the semiconductor substrate
1210

FIG. 12

PROCESS MODULE FOR INCREASING THE RESPONSE OF BACKSIDE ILLUMINATED PHOTOSENSITIVE IMAGERS AND ASSOCIATED METHODS

PRIORITY DATA

This application claims the benefit of U.S. Provisional Application Ser. No. 61/495,243, filed on Jun. 9, 2011, which is incorporated herein by reference.

BACKGROUND

The interaction of light with semiconductor materials has been a significant innovation. Silicon imaging devices are used in various technologies, such as digital cameras, optical mice, video cameras, cell phones, and the like. Charge-coupled devices (CCDs) were widely used in digital imaging, and were later improved upon by complementary metal-oxide-semiconductor (CMOS) imagers having improved performance. Many traditional CMOS imagers utilize front side illumination (FSI). In such cases, electromagnetic radiation is incident upon the semiconductor surface containing the CMOS devices and circuits. Backside illumination CMOS imagers have also been used, and in many designs electromagnetic radiation is incident on the semiconductor surface opposite the CMOS devices and circuits. CMOS sensors are typically manufactured from silicon and can covert visible incident light into a photocurrent and ultimately into a digital image. Silicon-based technologies for detecting infrared incident electromagnetic radiation have been problematic, however, because silicon is an indirect bandgap semiconductor having a bandgap of about 1.1 eV. Thus the absorption of electromagnetic radiation having wavelengths of greater than about 1100 nm is, therefore, very low in silicon.

SUMMARY

The present disclosure provides backside-illuminated photosensitive imager devices and associated methods. In one aspect, for example, a backside-illuminated photosensitive imager device can include a semiconductor substrate having multiple doped regions forming a least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, wherein the textured region includes surface features sized and positioned to facilitate tuning to a preselected wavelength of light, and a dielectric region positioned between the textured region and the at least one junction. The dielectric region is positioned to isolate the at least one junction from the textured region, and the semiconductor substrate and the textured region are positioned such that incoming electromagnetic radiation passes through the semiconductor substrate before contacting the textured region. Additionally, the device includes an electrical transfer element coupled to the semiconductor substrate to transfer an electrical signal from the at least one junction. In some aspects, the dielectric region is positioned to physically isolate the textured region from the at least one junction. In other aspects, the dielectric region is positioned to electrically isolate the textured region from the at least one junction.

In one aspect, the surface features have an average center-to-center distance of one half wavelength of the preselected wavelength of light, multiples of one half wavelength of the preselected wavelength of light, or at least one half wavelength of the preselected wavelength of light, wherein the preselected wavelength in this context is scaled by the refractive index of the surrounding material. In another aspect, the center-to-center distance of the features is substantially uniform across the textured region. In a further aspect, the surface features have an average height of about a multiple of a quarter wavelength of the preselected wavelength of light, wherein the preselected wavelength is scaled by the refractive index of the surrounding material. In another aspect, the surface features can be sized and positioned to reduce specular reflection.

Additional regions and/or structures can be included in various devices according to aspects of the present disclosure. In some aspects, for example, the device can include a reflecting region coupled to the textured region opposite the dielectric region and positioned to reflect electromagnetic radiation passing through the textured region back through the textured region. Various reflective materials can be included in the reflecting region including, without limitation, a Bragg reflector, a metal reflector, a metal reflector over a dielectric material, and the like, including combinations thereof. In some aspects, one or more dielectric layers are positioned between the reflecting region and the textured region. In another aspect, a lens can be optically coupled to the semiconductor substrate and positioned to focus incident electromagnetic radiation into the semiconductor substrate.

The preselected wavelength of light can be any wavelength or wavelength distribution. In one aspect, for example, the preselected wavelength of light can be in the near infrared or infrared range. In another aspect, the preselected wavelength of light can be greater than or equal to about 800 nm.

In another aspect, one or more anti-reflective layers can be deposited on the semiconductor substrate at a surface opposite the at least one junction such that incident light passes through the anti-reflective layer prior to contacting the semiconductor substrate. Additionally, in a further aspect at least one isolation feature can be formed in the semiconductor substrate, where the at least one isolation feature is positioned to reflect light impinging thereon back into the semiconductor substrate.

The present disclosure additionally provides various methods of making a backside-illuminated photosensitive imager device. One such method can include forming at least one junction at a surface of a semiconductor substrate, forming a dielectric region over the at least one junction, and forming a textured region over the dielectric region. The textured region can include surface features sized and positioned to facilitate tuning to a preselected wavelength of light. The dielectric region isolates the at least one junction from the textured region, and the semiconductor substrate and the textured region are positioned such that incoming electromagnetic radiation passes through the semiconductor substrate before contacting the textured region. The method can also include coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction.

Various techniques are contemplated for forming the textured region, and any technique useful for such a process is considered to be within the present scope. Non-limiting examples of such techniques include plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, lithography, and the like, including combinations thereof In one specific aspect, the forming of the textured region can include depositing a mask on the dielec-

tric region, etching the dielectric region through the mask to form surface features, and removing the mask from the dielectric region. The surface features can be further etched to round exposed edges. In yet another specific aspect, forming the textured region further includes depositing a first semiconductor material on the dielectric region, texturing the first semiconductor material to form a mask, depositing a second semiconductor material on the mask, and etching the second semiconductor material to form the textured region. In one specific aspect, texturing the second semiconductor material further includes etching the second semiconductor material to form a plurality of scallops pointing toward the semiconductor substrate. A variety of first and second semiconductor materials are contemplated, and any suitable material is considered to be within the present scope. In one aspect, however, the first and second semiconductor materials include silicon, polysilicon, amorphous silicon, or the like, including combinations thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the nature and advantage of the present invention, reference is being made to the following detailed description of preferred embodiments and in connection with the accompanying drawings, in which:

FIG. **1** is a schematic diagram of a four transistor active pixel sensor (APS) of a CMOS imager in accordance with one aspect of the present disclosure;

FIG. **2** is a schematic view of a photosensitive device in accordance with another aspect of the present disclosure;

FIG. **3** is a schematic view of a pixel of a photosensitive device with a BSI photodiode in accordance with yet another aspect of the present disclosure;

FIG. **4** illustrates light trapping in a thin semiconductor layer with a planar illuminated side and a textured opposing side in accordance with a further aspect of the present disclosure;

FIG. **5** is a graph showing calculated absorptance of infrared radiation in a thin silicon photodetector with light trapping and different amounts of light reflected back from the illuminated surface;

FIG. **6** is a schematic view of a photosensitive device in accordance with another aspect of the present disclosure;

FIG. **7** is a depiction of a method of making a photosensitive imager device in accordance with another aspect of the present disclosure;

FIG. **8***a* is a schematic view of a photosensitive device in accordance with yet another aspect of the present disclosure;

FIG. **8***b* is a schematic view of a photosensitive device in accordance with yet another aspect of the present disclosure;

FIG. **9***a* is a top view of a textured region in accordance with one aspect of the present disclosure;

FIG. **9***b* is a cross-sectional view of a textured surface in accordance with an aspect of the present disclosure;

FIG. **10***a* is a cross-sectional view of a photosensitive device during manufacture in accordance with another aspect of the present disclosure;

FIG. **10***b* is a cross-sectional view of a photosensitive device during manufacture in accordance with another aspect of the present disclosure;

FIG. **10***c* is a cross-sectional view of a photosensitive device during manufacture in accordance with another aspect of the present disclosure;

FIG. **11***a* is a cross-sectional view of a photosensitive device during manufacture in accordance with yet another aspect of the present disclosure;

FIG. **11***b* is a cross-sectional view of a photosensitive device during manufacture in accordance with yet another aspect of the present disclosure;

FIG. **11***c* is a cross-sectional view of a photosensitive device during manufacture in accordance with yet another aspect of the present disclosure;

FIG. **11***d* is a cross-sectional view of a photosensitive device during manufacture in accordance with yet another aspect of the present disclosure; and

FIG. **12** is a depiction of a method of making a photosensitive imager device in accordance with another aspect of the present disclosure.

DETAILED DESCRIPTION

Before the present disclosure is described herein, it is to be understood that this disclosure is not limited to the particular structures, process steps, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting.

Definitions

The following terminology will be used in accordance with the definitions set forth below.

It should be noted that, as used in this specification and the appended claims, the singular forms "a," and, "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a dopant" includes one or more of such dopants and reference to "the layer" includes reference to one or more of such layers.

As used herein, "tuning" refers to selectively enhancing a device for a property of light at a desired wavelength or range of wavelengths. In one aspect, a property of light can be absorptance, quantum efficiency, polarization, and the like.

As used herein, the term "textured surface" refers to a surface having a topology with nano- to micron-sized surface variations formed by the irradiation of laser pulses or other texturing methods. One non-limiting example of other texturing methods can include chemical etching. While the characteristics of such a surface can be variable depending on the materials and techniques employed, in one aspect such a surface can be several hundred nanometers thick and made up of nanocrystallites (e.g. from about 10 to about 50 nanometers) and nanopores. In another aspect, such a surface can include micron-sized structures (e.g. about 500 nm to about 60 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 500 μm.

As used herein, the terms "surface modifying" and "surface modification" refer to the altering of a surface of a semiconductor material using a variety of surface modification techniques. Non-limiting examples of such techniques include plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, selective epitaxial growth, and the like, including combinations thereof. In one specific aspect, surface modification can include processes using primarily laser radiation or laser radiation in combination with a dopant, whereby the laser radiation facilitates the incorporation of the dopant into a surface of the semiconductor material. Accordingly, in one aspect surface modification includes doping of a substrate such as a semiconductor material.

As used herein, the term "target region" refers to an area of a substrate that is intended to be doped or surface modified. The target region of the substrate can vary as the surface modifying process progresses. For example, after a first target region is doped or surface modified, a second target region may be selected on the same substrate.

As used herein, the term "fluence" refers to the amount of energy from a single pulse of laser radiation that passes through a unit area. In other words, "fluence" can be described as the energy surface density of one laser pulse.

As used herein, the term "detection" refers to the sensing, absorption, and/or collection of electromagnetic radiation.

As used herein, the term "backside illumination" refers to a device architecture design whereby electromagnetic radiation is incident on a surface of a semiconductor material that is opposite a surface containing the device circuitry. In other words, electromagnetic radiation is incident upon and passes through a semiconductor material prior to contacting the device circuitry.

As used herein, the term "substantially" refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is "substantially" enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use of "substantially" is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is "substantially free of" particles would either completely lack particles, or so nearly completely lack particles that the effect would be the same as if it completely lacked particles. In other words, a composition that is "substantially free of" an ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

As used herein, the term "about" is used to provide flexibility to a numerical range endpoint by providing that a given value may be "a little above" or "a little below" the endpoint.

As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of "about 1 to about 5" should be interpreted to include not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

The Disclosure

Electromagnetic radiation can be present across a broad wavelength range, including visible range wavelengths (approximately 350 nm to 800 nm) and non-visible wavelengths (longer than about 800 nm or shorter than 350 nm). The infrared spectrum is often described as including a near infrared portion of the spectrum including wavelengths of approximately 800 nm to 1300 nm, a short wave infrared portion of the spectrum including wavelengths of approximately 1300 nm to 3 micrometers, and a mid to long wave infrared (or thermal infrared) portion of the spectrum including wavelengths greater than about 3 micrometers up to about 30 micrometers. These are generally and collectively referred to herein as "infrared" portions of the electromagnetic spectrum unless otherwise noted.

Traditional silicon photodetecting imagers have limited light absorption/detection properties. For example, such silicon based detectors are mostly transparent to infrared light. While other mostly opaque materials (e.g. InGaAs) can be used to detect infrared electromagnetic radiation having wavelengths greater than about 1000 nm, silicon is still commonly used because it is relatively cheap to manufacture and can be used to detect wavelengths in the visible spectrum (i.e. visible light, 350 nm-800 nm). Traditional silicon materials require substantial path lengths to detect photons having wavelengths longer than approximately 700 nm. While visible light can be absorbed at relatively shallow depths in silicon, absorptance of longer wavelengths (e.g. 900 nm) in silicon of a standard wafer depth (e.g. approximately 750 μm) is poor if at all.

The devices of the present disclosure increase the absorptance of semiconductor materials by increasing the propagation path length for longer wavelengths as compared to traditional materials. The absorption depth in conventional silicon detectors is the depth into silicon at which the radiation intensity is reduced to about 36% of the value at the surface of the semiconductor. The increased propagation path length results in an apparent reduction in the absorption depth, or a reduced apparent or effective absorption depth. For example, the effective absorption depth of silicon can be reduced such that these longer wavelengths can be absorbed in material thicknesses of less than or equal to about 850 μm. In other words, by increasing the propagation path length, these devices are able to absorb longer wavelengths (e.g. >1000 nm for silicon) within a thinner semiconductor material. In addition to decreasing the effective absorption depth, the response rate or response speed can also be increased by using thinner semiconductor materials.

Accordingly, backside-illuminated (BSI) photosensitive imager devices and associated methods are provided. Such devices provide, among other things, enhanced response in the infrared light portion of the electromagnetic spectrum and improved response and quantum efficiency in converting electromagnetic radiation to electrical signals. Quantum efficiency can be defined as the percentage of photons that are converted into electrons and collected by a sensing circuit. There are two types of QE, Internal QE (IQE) and External QE (EQE). The EQE is always lower than the IQE since there will inevitably be recombination effects and optical losses (e.g. transmission and reflection losses). One

reason for improved performance with BSI is a higher fill factor or, in other words, the percentage if incident light that is incident on a photosensitive region of the device. The various metal layers on top of a front side-illuminated sensor (FSI) limit the amount of light that can be collected in a pixel. As pixel sizes get smaller, the fill factor gets worse. BSI provides a more direct path for light to travel into the pixel, thus avoiding light blockage by the metal interconnect and dielectric layers on the top-side of the semiconductor substrate.

The present disclosure additionally provides BSI broadband photosensitive diodes, pixels, and imagers capable of detecting visible as well as infrared electromagnetic radiation, including associated methods of making such devices. A photosensitive diode can include a semiconductor substrate having multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation where the textured region includes surface features sized and positioned to facilitate tuning to a preselected wavelength of light, and a dielectric region positioned between the textured region and the at least one junction. The dielectric region is positioned to isolate the at least one junction from the textured region, and the semiconductor substrate and the textured region are positioned such that incoming electromagnetic radiation passes through the semiconductor substrate before contacting the textured region. It should be noted that, in some aspects, the dielectric region can be a passivation region.

In one aspect the multiple doped regions can include at least one cathode region and at least one anode region. In some aspects, doped regions can include an n-type dopant and/or a p-type dopant as is discussed below, thereby creating a p-n junction. In other aspects, a photosensitive device can include an i-type region to form a p-i-n junction.

A photosensitive pixel can include a semiconductor substrate having multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation where the textured region includes surface features sized and positioned to facilitate tuning to a preselected wavelength of light, and a dielectric region positioned between the textured region and the at least one junction. The dielectric region is positioned to isolate the at least one junction from the textured region, and the semiconductor substrate and the textured region are positioned such that incoming electromagnetic radiation passes through the semiconductor substrate before contacting the textured region. Additionally, the photosensitive pixel also includes an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. A photosensitive imager can include multiple photosensitive pixels. Additionally, an electrical transfer element can include a variety of devices, including without limitation, transistors, sensing nodes, transfer gates, transfer electrodes, and the like.

Photosensitive or photo detecting imagers include photodiodes or pixels that are capable of absorbing electromagnetic radiation within a given wavelength range. Such imagers can be passive pixel sensors (PPS), active pixel sensors (APS), digital pixel sensor imagers (DPS), or the like, with one difference being the image sensor read out architecture. For example, a semiconducting photosensitive imager can be a three or four transistor active pixel sensor (3T APS or 4T APS). Various additional components are also contemplated, and would necessarily vary depending on the particular configuration and intended results. As an example, a 4T configuration as is shown in FIG. **1** can additionally include, among other things, a transfer gate **102**, a reset transistor **104**, a source follower **106**, a row select transistor **108**, and a photodiode sensor **110**. Additionally, devices having greater than 4 transistors are also within the present scope. In one aspect, photosensor diode **110** can be a conventional pinned photodiode as used in current state of the art complimentary metal-oxide-semiconductor (CMOS) imagers.

Photosensitive imagers can be front side illumination (FSI) or back side illumination (BSI) devices. In a typical FSI imager, incident light enters the semiconductor device by first passing by transistors and metal circuitry. The light, however, can scatter off of the transistors and circuitry prior to entering the light sensing portion of the imager, thus causing optical loss and noise. A lens can be disposed on the topside of a FSI pixel to direct and focus the incident light to the light sensing active region of the device, thus partially avoiding the circuitry. In one aspect the lens can be a micro-lens. In one aspect, for example, incident light enters the device via the light sensing portion and is mostly absorbed prior to reaching the circuitry. BSI designs allow for smaller pixel architecture and a higher fill factor for the imager. It should also be understood that devices according to aspects of the present disclosure can be incorporated into CMOS imager architectures, charge-coupled device (CCD) imager architectures, and the like.

In one aspect, as is shown in FIG. **2**, a BSI photosensitive diode **200** can include a semiconductor substrate **202** having multiple doped regions **204**, **206** forming at least one junction, and a textured region **208** coupled to the semiconductor substrate **202** and positioned to interact with electromagnetic radiation **212**. The multiple doped regions **204**, **206** can have the same doping profile or different doping profiles, depending on the device. While the device shown in FIG. **2** contains three doped regions, it should be noted that other aspects containing one or more doped regions are considered to be within the present scope. Additionally, the semiconductor substrate **202** can be doped, and thus can be considered to be a doped region in some aspects. A dielectric region **210** is positioned between the textured region **208** and the at least one junction. In one aspect, the dielectric region can have a thickness in the range of about 1 nm to about 2 μm. In another aspect, the dielectric region can have a thickness in the range of about 10 nm to about 100 nm. In yet another aspect the dielectric region can have a thickness of less than about 50 nm. The dielectric region **210** can be positioned to isolate the at least one junction from the textured region **208**, and the semiconductor substrate **202** and the textured region **208** can be positioned such that incoming electromagnetic radiation **212** passes through the semiconductor substrate **202** before contacting the textured region **208**. The photosensitive diode is backside illuminated by electromagnetic radiation **212** that is incident on the side of the semiconductor substrate **202** opposite the multiple doped regions **204**, **206**.

In another aspect, as is shown in FIG. **3**, a BSI photosensitive imager device **300** is provided. The BSI photosensitive imager device can include a semiconductor substrate **302** having multiple doped regions **304**, **306** forming a least one junction, and a textured region **308** coupled to the semiconductor substrate **302** and positioned to interact with electromagnetic radiation **310**. A dielectric region **312** can be positioned between the textured region **308** and the at least one junction to isolate the at least one junction from the textured region. The semiconductor substrate **302** and the textured region **308** are positioned such that incoming

electromagnetic radiation **310** passes through the semiconductor substrate **302** before contacting the textured region **308**. Additionally, in some aspects an optional dielectric region or reflecting region **314** can be coupled to the textured region **308**. An electrical transfer element **316** can be coupled to the semiconductor substrate **302** to transfer an electrical signal from the at least one junction. Side wall insulators **318** and **320** can also be formed about the transfer element **316** and also around the dielectric and textured regions **312**, **314**, respectively, to facilitate proper spacing away from the transfer element **316**. Additionally, a drain junction region **322** can be electrically coupled to the transfer element **316** to receive charge transferred thereto by the transfer element.

The various devices according to aspects of the present disclosure can exhibit increased quantum efficiency over traditional photosensitive devices. Any increase in the quantum efficiency makes a large difference in the signal to noise ratio. More complex structures can provide not only increased quantum efficiency but also good uniformity from pixel to pixel. In addition, devices of the present disclosure exhibit increased responsivity as compared to traditional photosensitive devices. For example, in one aspect the responsivity can be greater than or equal to 0.8 A/W for wavelengths greater than 1000 nm for semiconductor substrate that is less than 100 μm thick. In other embodiment the responsivity can be greater than 0.5 A/W for wavelengths greater than 1100 nm for semiconductor substrate that is less than 50 μm thick.

A variety of semiconductor materials are contemplated for use with the devices and methods according to aspects of the present disclosure. Non-limiting examples of such semiconductor materials can include group IV materials, compounds and alloys comprised of materials from groups II and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can include silicon carbide (SiC) and silicon germanium (SiGe). In one specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum gallium arsenide, and combinations thereof.

Exemplary combinations of group II-VI materials can include cadmium selenide (CdSe), cadmium sulfide (CdS), cadmium telluride (CdTe), zinc oxide (ZnO), zinc selenide (ZnSe), zinc sulfide (ZnS), zinc telluride (ZnTe), cadmium zinc telluride (CdZnTe, CZT), mercury cadmium telluride (HgCdTe), mercury zinc telluride (HgZnTe), mercury zinc selenide (HgZnSe), and combinations thereof.

Exemplary combinations of group III-V materials can include aluminum antimonide (AlSb), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum phosphide (AlP), boron nitride (BN), boron phosphide (BP), boron arsenide (BAs), gallium antimonide (GaSb), gallium arsenide (GaAs), gallium nitride (GaN), gallium phosphide (GaP), indium antimonide (InSb), indium arsenide (InAs), indium nitride (InN), indium phosphide (InP), aluminum gallium arsenide (AlGaAs, $Al_xGa_{1-x}As$), indium gallium arsenide (InGaAs, $In_xGa_{1-x}As$), indium gallium phosphide (InGaP), aluminum indium arsenide (AlInAs), aluminum indium antimonide (AlInSb), gallium arsenide nitride (GaAsN), gallium arsenide phosphide (GaAsP), aluminum gallium nitride (AlGaN), aluminum gallium phosphide (AlGaP), indium gallium nitride (InGaN), indium arsenide antimonide (InAsSb), indium gallium antimonide (InGaSb), aluminum gallium indium phosphide (AlGaInP), aluminum gallium arsenide phosphide (AlGaAsP), indium gallium arsenide phosphide (InGaAsP), aluminum indium arsenide phosphide (AlInAsP), aluminum gallium arsenide nitride (AlGaAsN), indium gallium arsenide nitride (InGaAsN), indium aluminum arsenide nitride (InAlAsN), gallium arsenide antimonide nitride (GaAsSbN), gallium indium nitride arsenide antimonide (GaInNAsSb), gallium indium arsenide antimonide phosphide (GaInAsSbP), and combinations thereof.

The semiconductor substrate can be of any thickness that allows electromagnetic radiation detection and conversion functionality, and thus any such thickness of semiconductor material is considered to be within the present scope. In some aspects, the textured region increases the efficiency of the device such that the semiconductor substrate can be thinner than has previously been possible. Decreasing the thickness of the semiconductor substrate reduces the amount of semiconductor material required to make such a device. In one aspect, for example, the semiconductor substrate has a thickness of from about 500 nm to about 50 μm. In another aspect, the semiconductor substrate has a thickness of less than or equal to about 100 μm. In yet another aspect, the semiconductor substrate has a thickness of from about 1 μm to about 10 μm. In a further aspect, the semiconductor substrate can have a thickness of from about 5 μm to about 50 μm. In yet a further aspect, the semiconductor substrate can have a thickness of from about 5 μm to about 10 μm.

Additionally, various types of semiconductor materials are contemplated, and any such material that can be incorporated into an electromagnetic radiation detection device is considered to be within the present scope. In one aspect, for example, the semiconductor material is monocrystalline. In another aspect, the semiconductor material is multicrystalline. In yet another aspect, the semiconductor material is microcrystalline. It is also contemplated that the semiconductor material can be amorphous. Specific nonlimiting examples include amorphous silicon or amorphous selenium.

The semiconductor materials of the present disclosure can also be made using a variety of manufacturing processes. In some cases the manufacturing procedures can affect the efficiency of the device, and may be taken into account in achieving a desired result. Exemplary manufacturing processes can include Czochralski (Cz) processes, magnetic Czochralski (mCz) processes, Float Zone (FZ) processes, epitaxial growth or deposition processes, and the like. It is contemplated that the semiconductor materials used in the present invention can be a combination of monocrystalline material with epitaxially grown layers formed thereon.

A variety of dopant materials are contemplated for the formation of the multiple doped regions, and any such dopant that can be used in such processes to surface modify a material is considered to be within the present scope. It should be noted that the particular dopant utilized can vary depending on the material being doped, as well as the intended use of the resulting material. For example, the selection of potential dopants may differ depending on whether or not tuning of the photosensitive device is desired.

A dopant can be either charge donating or accepting dopant species. More specifically, an electron donating or a hole donating species can cause a region to become more

positive or negative in polarity as compared to the semiconductor substrate. In one aspect, for example, the doped region can be p-doped. In another aspect the doped region can be n-doped. A highly doped region can also be formed on or near the doped region to create a pinned diode. In one non-limiting example, the semiconductor substrate can be negative in polarity, and a doped region and a highly doped region can be doped with p+ and n dopants respectively. In some aspects, variations of n(−−), n(−), n(+), n(++), p(−−), p(−), p(+), or p(++) type doping of the regions can be used.

In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof. It should be noted that the scope of dopant materials should include, not only the dopant materials themselves, but also materials in forms that deliver such dopants (i.e. dopant carriers). For example, S dopant materials includes not only S, but also any material capable being used to dope S into the target region, such as, for example, H_2S, SF_6, SO_2, and the like, including combinations thereof. In one specific aspect, the dopant can be S. Sulfur can be present at an ion dosage level of between about 5×10^{14} ions/cm^2 and about 1×10^{16} ions/cm^2. Non-limiting examples of fluorine-containing compounds can include ClF_3, PF_5, F_2 SF_6, BF_3, GeF_4, WF_6, SiF_4, HF, CF_4, CHF_3, CH_2F_2, CH_3F, C_2F_6, C_2HF_5, C_3F_8, C_4F_8, NF_3, and the like, including combinations thereof. Non-limiting examples of boron-containing compounds can include $B(CH_3)_3$, BF_3, BCl_3, BN, $C_2B_{10}H_{12}$, borosilica, B_2H_6, and the like, including combinations thereof. Non-limiting examples of phosphorous-containing compounds can include PF_5, PH_3, and the like, including combinations thereof. Non-limiting examples of chlorine-containing compounds can include Cl_2, SiH_2Cl_2, HCl, $SiCl_4$, and the like, including combinations thereof Dopants can also include arsenic-containing compounds such as AsH_3 and the like, as well as antimony-containing compounds. Additionally, dopant materials can include mixtures or combinations across dopant groups, i.e. a sulfur-containing compound mixed with a chlorine-containing compound. In one aspect, the dopant material can have a density that is greater than air. In one specific aspect, the dopant material can include Se, H_2S, SF_6, or mixtures thereof. In yet another specific aspect, the dopant can be SF_6 and can have a predetermined concentration range of about 5.0×10^{-8} mol/cm^3 to about 5.0×10^{-4} mol/cm^3. As one non-limiting example, SF_6 gas is a good carrier for the incorporation of sulfur into the semiconductor material via a laser process without significant adverse effects on the material. Additionally, it is noted that dopants can also be liquid solutions of n-type or p-type dopant materials dissolved in a solution such as water, alcohol, or an acid or basic solution. Dopants can also be solid materials applied as a powder or as a suspension dried onto the wafer.

As a further processing note, the semiconductor substrate can be annealed for a variety of reasons, including dopant activation, semiconductor damage repair, and the like. The semiconductor substrate can be annealed prior to texturing, following texturing, during texturing, or any combination thereof. Annealing can enhance the semiconductive properties of the device, including increasing the photoresponse properties of the semiconductor materials by reducing any imperfections in the material. Additionally, annealing can reduce damage that may occur during the texturing process. Although any known anneal can be beneficial and would be considered to be within the present scope, annealing at lower temperatures can be particularly useful. Such a "low temperature" anneal can greatly enhance the external quantum efficiency of devices utilizing such materials. In one aspect, for example, the semiconductor substrate can be annealed to a temperature of from about 300° C. to about 1100 C.°. In another aspect, the semiconductor substrate can be annealed to a temperature of from about 500° C. to about 900° C. In yet another aspect, the semiconductor substrate can be annealed to a temperature of from about 700° C. to about 800° C. In a further aspect, the semiconductor substrate can be annealed to a temperature that is less than or equal to about 850° C.

The duration of the annealing procedure can vary according to the specific type of anneal being performed, as well as according to the materials being used. For example, rapid annealing processes can be used, and as such, the duration of the anneal may be shorter as compared to other techniques. Various rapid thermal anneal techniques are known, all of which should be considered to be within the present scope. In one aspect, the semiconductor substrate can be annealed by a rapid annealing process for a duration of greater than or equal to about 1 μs. In another aspect, the duration of the rapid annealing process can be from about 1 μs to about 1 ms. As another example, a baking or furnace anneal process can be used having durations that may be longer compared to a rapid anneal. In one aspect, for example, the semiconductor substrate can be annealed by a baking anneal process for a duration of greater than or equal to about 1 ms to several hours.

Various types of dielectric region configurations are contemplated, and any configuration that can be incorporated into a photosensitive device is considered to be within the present scope. One benefit to such a dielectric region pertains to the isolation provided between the textured region and the doped regions that form the junction. In one aspect, for example, the dielectric region can be positioned to physically isolate the textured region from the junction. In this way, the creation of the textured region can be isolated from the doped regions, thus precluding undesirable effects of the texturing process from affecting the junction. In another aspect, the dielectric region can be a dielectric material, and thus the dielectric region could be used to electrically isolate the textured region from the junction. In some cases, the dielectric region is coupled directly to at least one of the doped regions forming the junction.

The dielectric region can be made from a variety of materials, and such materials can vary depending on the device design and desired characteristics. Non-limiting examples of such materials can include oxides, nitrides, oxynitrides, and the like, including combinations thereof. In one specific aspect, the dielectric region includes an oxide. Additionally, the dielectric region can be of various thicknesses. In one aspect, for example, the dielectric region has a thickness of from about 100 nm to about 1 micron. In another aspect, the dielectric region has a thickness of from about 5 nm to about 100 nm. In yet another aspect, the dielectric region has a thickness of from about 20 nm to about 50 nm. It should be noted that, in cases where the textured region is a portion of the dielectric region (e.g. a dielectric layer) that has been textured, the thickness of the dielectric material would be increased to account for the texturing. Thus the thickness ranges for the dielectric region provided here would be measured as the thickness of the dielectric region not including the textured portion.

The textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, to absorb electromagnetic radiation, and the like, thus increasing the quantum efficiency of the device. In the present BSI devices, electromagnetic radiation passing through the semiconductor substrate can contact the textured region. The

textured region can include surface features to thus increase the effective absorption length of the photosensitive pixel. Such surface features can be to micron-sized and/or nano-sized, and can be any shape or configurations. Non-limiting examples of such shapes and configurations include cones, pillars, pyramids, micolenses, quantum dots, inverted features, gratings, protrusions, scallops, and the like, including combinations thereof. Additionally, factors such as manipulating the feature sizes, dimensions, material type, dopant profiles, texture location, etc. can allow the diffusing region to be tunable for a specific wavelength. In one aspect, tuning the device can allow specific wavelengths or ranges of wavelengths to be absorbed. In another aspect, tuning the device can allow specific wavelengths or ranges of wavelengths to be reduced or eliminated via filtering.

Tuning can also be accomplished through the relative location of the texture region within the device, modifying the dopant profile(s) of regions within the device, dopant selection, and the like. Additionally, material composition near the textured region can create a wavelength specific photosensing pixel device. It should be noted that a wavelength specific photosensing pixel can differ from one pixel to the next, and can be incorporated into an imaging array. For example a 4×4 array can include a blue pixel, a green pixel, a red pixel, and infrared light absorbing pixel, or a blue pixel, two green pixels, and a red pixel.

The textured regions can also be made to be selective to polarized light and light of particular polarizations. In one specific example, if the textured region includes a one dimensional grating of grooves on a high index of refraction material then the scattering of the light will depend upon the polarization of the light and the pixels can select light of specific linear polarizations.

Textured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared). Such internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor substrate. This increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.

The materials used for producing the textured region can vary depending on the design and the desired characteristics of the device. As such, any material that can be utilized in the construction of a textured region is considered to be within the present scope. Non-limiting examples of such materials include semiconductor materials, dielectric materials, conductive materials (e.g. metals), silicon, polysilicon, amorphous silicon, transparent conductive oxides, and the like, including composites and combinations thereof. In one specific aspect, the textured layer can be a textured polysilicon layer. Thus a polysilicon layer can be deposited onto the dielectric region and then textured to form the textured region. In another aspect, the textured layer can be a textured dielectric layer. In this case the textured region can be a portion of the dielectric layer making up the dielectric region. In yet another aspect the textured layer can be a transparent conductive oxide or another semiconductor material. In the case of dielectric layers, the textured region can be a textured portion of the dielectric region or the textured region can be formed from other dielectric material deposited over the dielectric region. In the case of semiconductor materials, forming the textured region can include depositing a semiconductor material on the dielectric region and texturing the semiconductor material to form the textured region. In another aspect, the semiconductor material can be bonded or adhered to the dielectric region. The texturing process can texture the entire semiconductor material or only a portion of the semiconductor material. In one specific aspect, a polysilicon layer can be deposited over the dielectric region and textured and patterned by an appropriate technique (e.g. a porous silicon etch) to form the textured region. In yet another aspect, a polysilicon layer can be deposited over the dielectric region and textured and patterned by using a mask, photolithography, and an etch to define a specific structure or pattern.

In addition to surface features, the textured region can have a surface morphology that is designed to focus or otherwise direct electromagnetic radiation, thus enhancing the quantum efficiency of the device. For example, in one aspect the textured region has a surface morphology operable to direct electromagnetic radiation into the semiconductor substrate. Non-limiting examples of various surface morphologies include sloping, pyramidal, inverted pyramidal, spherical, square, rectangular, parabolic, ellipsoidal, asymmetric, symmetric, scallops, gratings, pillars, cones, microlenses, quantum dots, and the like, including combinations thereof.

One example of such a surface morphology is shown in FIG. **4**. Without intending to be limited to any operational theory, the following description provides one possible explanation for the effects of surface morphology in tuning a textured region for specific wavelengths of electromagnetic radiation. FIG. **4** shows a textured device **400** having a surface morphology that affects the near infrared wavelength response. A semiconductor substrate **402** is shown having an illuminated surface **404** to receive incident electromagnetic radiation **406**. The semiconductor substrate **402** further has a textured region **408** (e.g. dielectric) coupled thereto at a surface that is opposite to the illuminated surface **404**. The textured region **408** has a surface morphology configured in an undulating pattern **410** with grooves, ridges, or similar patterns to produce an internal reflection that is not specular. In the near infrared, the index of refraction of silicon is about $\eta=3.42$ and the reflectance is about R=30% from a single planar surface, and transmittance through a single planar surface is T=70% for normally incident waves. The absorption coefficient of silicon is very low in the near infrared. Electromagnetic radiation under normal incidence, represented by arrow **412**, is reflected from the illuminated surface **404**, and this is shown as arrow **414**. There are successive reflections from both the illuminated surface and the opposing side, represented by arrows **416** and **418**, and internal reflections from the illuminated surface **404**, represented by arrow **420**, resulting in a total internal reflection. If there is neither a reflective metal layer **422** nor textured region, the total transmittance, T_{tot}, is as shown in Equation (I) as:

$$T_{tot}=(TT)(1+R^2+R^4+\ldots)=(TT)/(1-R^2) \quad \text{(I)}$$

This result has been obtained using the sum of a geometric series. If both surfaces are just polished silicon—air, then the total transmittance is 54% and the reflectance is 46%.

If the increase in the individual path lengths caused by the diffuse scattering is neglected and if the absorption coefficient is very low then the total effective path length is determined by just the number of reflections, and the total absorptance can be as shown in Equation (II):

$$A=\alpha d(1R_2)(1+R_1R_2+R_1^2R_2^2+\ldots)=\alpha d(1+R_2)/(1-R_1R_2) \quad \text{(II)}$$

Here, α is the absorption coefficient in reciprocal cm, d is the thickness of the sample in cm, and the effective increase in

path length is $Enh=(1+R_2)/(1-R_1 R_2)$. The internal quantum efficiency (IQE) in the infrared where the absorption in silicon is low is thus $IQE=\alpha d(Enh)$. The external quantum efficiency (EQE) is $EQE=T_1 IQE$ and $EQE=T_1 \alpha d(Enh)$.

If both sides of an infrared photo detector are polished then $T_1=T_2=0.70$ and $R_1=R_2=0.3$, which gives Enh=1.4, IQE=1.4αd, and EQE=αd. If one side is polished and the other side has an oxide and a metal reflector, then $R_1=0.3$ and $R_2=1.0$, yielding an enhancement in infrared absorptance or Enh=3. T_1 is the transmittance of radiation incident on the first surface. T_2 is the transmittance of radiation striking the second surface from the semiconductor side. R_1 is the amount of radiation reflected back into the semiconductor for radiation striking the first surface from the semiconductor side. R_2 is the amount of radiation reflected back into the semiconductor for radiation striking the second surface from the semiconductor side.

In one aspect that can improve the infrared response, the illuminated side **404** is polished but the opposing side **410** is a textured dielectric material **408** with a reflecting region **422** (see FIG. **4**). The texturing can be realized in a fashion to produce a true diffuse scattering (i.e. a Lambertian scattering) at the infrared wavelengths. This diffuse scattering layer/reflecting layer combination, in essence yields an $R_2=100\%$, which is a diffuse reflector. The reflectance of the polished front side to the scattered light radiation is determined by solid angle considerations. Any incident light with an angle of incidence greater than the critical angle θ_c, **424**, will be totally internally reflected **420**. If the backside scattering is totally diffused in a half sphere or Lambertian, the transmittance is then determined by the area of the surface (π^2) within the critical angle θ_c, **424**, in this case 17° for silicon and air. The radius of the circle is $r=d\cdot\sin(17°)$, where d is the thickness of the sample. This area is divided by the area of the half sphere ($2\pi d^2$). If the backside scattering is totally diffuse, the transmittance of the front planar surface is then roughly $T_1=3\%$ and the reflectance $R_1=97\%$. The path length enhancement factor can be very large, as is shown in Equation (III):

$$Enh=(1+R_2)/(1-R_1R_2)=66 \quad \text{(III)}$$

This would result in an IQE=66αd and an EQE=46. If the backside includes a textured region and a truly diffusive scattering surface, and a mirror-like surface is used behind the back side, a very large enhancement of absorptance in the near infrared can be achieved. If the absorption in the semiconductor substrate is not assumed to be small but rather is taken into account, it can be shown that the enhancement factor for the IQE due to multiple reflections is modified from Equation (I) and as is shown in Equation (IV):

$$Enh=(1-\exp(-\alpha d))(1+R_2\exp(-\alpha d))/(1-R_1R_2\exp(-2\alpha d)) \quad \text{(IV)}$$

This allows a calculation of the responsivity in terms of the electrical current in Amperes per incident light power in Watts of photo detectors of different thickness d for different wavelengths λ, since the absorption coefficient α(λ) is a function of wavelength (see FIG. **5**). If it is assumed that the textured side is an ideal reflector (i.e. $R_2=1.0$) and the amount of diffusive scattering of the textured surface varies from that of a planar surface, then the fraction of light reflected back from the opposing illuminated surface may vary. If the textured surface is planar, then there is only specular reflection, and $R_1=0.3$ and the enhancement in responsivity, as indicated by curve **600**, is not large. If the textured surface is an ideal Lambertian diffusive surface then the fraction of light reflected back from the front surface may be very large, $R_1=0.97$. Several values of R_1 as illustrated by curves, **601**, **602**, and **603** are discussed herein and illustrated in FIG. **5**, for a diffuse reflector, and these represent the fraction of light internally reflected back at the front surface. For purposes of the present disclosure, values of $R_1\geq0.9$ (curve **601**) are deemed useful. The enhancement in absorptance described by Equation (IV) then varies with the fraction of light radiation reflected back from the illuminated surface and thickness of the sample, as is illustrated in FIG. **5**. It should be noted that, while the techniques described herein have been used to enhance the absorptance at infrared and red light radiation, they are also applicable to visible light as the thickness of the silicon layer becomes thinner. Scattering and multiple internal reflections can also be used to increase the absorptance at yellow, green and even blue light that will not be totally absorbed in single passes within thin silicon layers. These techniques can be applied then to visible imagers with thin silicon absorption layers.

In another aspect, FIG. **6** shows a cross-section of a BSI photosensitive pixel device **600**. The photosensitive pixel device can include a semiconductor substrate **602** that can be referred to as bulk semiconductor material. The semiconductor substrate **602** includes at least one doped region **604**, **605**, that can be doped with a charge donating species, such as an electron donating or hole donating species, to cause the region to become more n-type or p-type as compared to the semiconductor substrate. In one aspect, for example, the doped region can be p-doped. In another aspect the doped region can be n-doped. The device can further include various metal regions **606**, at least one via **608**, a dielectric region **610**, isolation element(s) **612**, such as trench isolation elements, and an electrical transfer element **614**.

Trench isolation elements can maintain pixel to pixel uniformity by reducing optical and electrical crosstalk. The isolation elements can be shallow or deep trench isolation. The trench isolation elements of FIG. **6** are shown as deep trench isolation elements. The isolation elements can include various materials, including, without limitation, dielectric materials, reflective materials, conductive materials, light diffusing features, and the like. These isolation regions can be configured to reflect incident light until it is absorbed, thereby increase the effective absorption length of the device.

A lens **624** and an anti-reflective coating **616** can be disposed on the backside of the pixel following thinning and trench isolation. A color filter **618** can be optically coupled to the lens to allow specific wavelength filtering of the electromagnetic radiation. A textured region **620** can be coupled to the semiconductor substrate **602** opposite the lens **624** in order to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes through to the front side of the pixel. Thus the electromagnetic radiation can be focused within the semiconductor substrate **602** to the combined action of the textured region **620** and the isolation features **612**. Additionally, side wall insulators **622** can be formed about the transfer element **606** and also around textured region **620** to facilitate proper spacing.

In general, isolation features can maintain pixel to pixel uniformity when multiple pixels are used in association by reducing optical and electrical crosstalk there between. The isolation feature can be shallow or deep, depending on the desired design. The isolation features can be generated using various materials including, without limitation, dielectric materials, reflective materials, conductive materials, light diffusing features, and the like. Additionally, in some aspects the isolation feature can be a void in the semiconductor

substrate. In one aspect, isolation features can also be configured to reflect incident electromagnetic radiation until it is absorbed, thereby increasing the effective absorption length of the incident light and reducing optical crosstalk into neighboring devices. Furthermore, the devices according to aspects of the present disclosure can also independently include one or more vias, dielectric regions, and the like.

In other aspects of the present disclosure, various methods of making a photosensitive device as described herein are contemplated. In one aspect, as is shown in FIG. **7**, a method of making a backside-illuminated photosensitive imager device can include traditional fabrication steps along with additional steps of forming isolation features **702**, doping a portion of the semiconductor material to form n+ implant **704**, doping a portion with an n+ implant to form a source-drain **706**, doping a portion of the semiconductor substrate with a p+ dopant to form p+ implant **708**, and growing and etching a gate oxide region **710**. The method can also include depositing and etching to form a polysilicon gate **712**, forming a textured surface near the p+ implant region **714**, and depositing the contacts **716**. It should be noted that the present scope is not limited to the above described doping scheme. Thus, this process can be applied in modular form to the steps involved in the fabrication of a conventional BSI CMOS imager pixel arrays. In other words, this modular processing method can be an insert of a process module in the process flow of the fabrication of a conventional BSI imager. In one aspect, the conventional process can be stopped just before the first via etch but after the deposition of the interlayer dielectric. At this point, rather than etch a via, the mask that was used to define the p-type implantation on top of the n-type diode can be used to mask and open the area over the p-type layer. A sidewall spacer process can be employed on the inside border of this opening to insure adequate spacing of the textured layers to be deposited away from the transfer device. A dielectric region, a textured region, and in some cases a metal or oxide reflector can be deposited in the area over the p-type region. As such, this module can be introduced into a conventional process flow with minimal changes. Subsequently, an interlayer dielectric similar to the first interlayer dielectric can be deposited over the metal reflector, and the combined interlayer dielectrics can be chemically and mechanically polished to planarize the surface. The normal contact mask can then be used to open vias resulting in minimal changes to the conventional process flow. A via can be opened to the metal reflector layer to control the potential of this layer and if appropriate, the textured layer to avoid charging during processing or for the region, can act as an MOS gate.

CMOS imagers are commonly used as visible light cell phone, still frame and video cameras, with BSI devices becoming a common structure. Cameras for use as infrared imagers for security and surveillance are, however, not commonly available. The present methods allow the conversion of visible light imagers to include the capability for imaging in the near infrared. Thus, the texture processing methods described can be adapted to a traditional fabrication process for visible imagers to provide an additional capability for near infrared imaging. The CMOS imagers can employ any pixel design including more than one transistor or transfer device. In some aspects, the transfer device can be a p-channel transfer gate or an n-channel transfer gate and associated implant polarities.

Conventional CCD imagers employ photodiode detectors similar to those used in CMOS imagers, and as such, the present methods can also be applied to the fabrication of CCD imagers to form devices capable of detecting infrared wavelengths in appreciable amounts and with appreciable enhancement.

The photodetecting diode used in the imager pixel can also include MOS diodes rather than doped junction diodes. MOS diodes use a pulsed bias to form a depletion region and light collecting region near the surface rather than a junction diode. The method described herein can equally be applied and inserted into imager pixels with MOS diodes or CCD imagers where the light generated carriers are collected in a surface depletion region. In these latter cases the metal reflecting gate can be driven with a voltage to act as a MOS or CCD gate.

In one aspect, as is shown in FIG. **8***a*, a BSI photosensitive imager device **800**, can include a textured region **802**, a reflecting layer **804**, and a dielectric layer **806** disposed between the semiconductor substrate **808** and the textured region **802**. The device can further include doped regions **810**, **812**, a drain region **814**, sidewall spacers **816**, and a transfer device having a gate insulator **818** and a polysilicon gate **820**, as has been described. The reflecting/diffusing region **822**, shown separately in FIG. **8***b*, is thus effectively a process module that can be inserted into a standard CMOS imager manufacturing process as has been described. In one aspect, this process module of forming the reflective/diffusing region can be inserted after deposition of the first dielectric spacer layer and before a contact etch step in a CMOS image sensor manufacturing process. A mask can be used to create the implantation of the P+ surface region on the photodiode, which can also be used to etch an aperture in the newly formed dielectric layer. The spacers **816** can be formed on the inside of this hole using conventional techniques to space the textured region **802** away from the edge of the P+ region. The hole can then be filled with any one of a variety of "process modules" to form the textured region **802**. After completion of the textured region, the conventional process can be continued starting with the contact etch mask. It should be noted that the present scope also includes aspects having a lens without an anti-reflecting coating, and aspects having an anti-reflecting coating associated with the semiconductor substrate without a lens. Additionally, a color filter (not shown) can be optically coupled to the lens to allow specific wavelength filtering of the electromagnetic radiation. Incident electromagnetic radiation passing through the color filter prior to contacting the semiconductor substrate can be filtered according to the characteristics of the filter.

One simple aspect to enhance the infrared response of photo detecting pixels can include a module consisting essentially of a dielectric region, an oxide, and a metal reflector region without texture. Even this simple structure can provide, by virtue of Equation III with R_2=1.0, R_1=0.3, an enhancement in the infrared response over that of a single pass of radiation by a factor of about 2.

The textured region, including surface features as well as surface morphologies, can be formed by various techniques, including plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, selective epitaxial growth, and the like. In one aspect, the texturing process can be performed during the manufacture of the photosensitive device. In another aspect, the texturing process can be performed on a photosensitive device that has previously been made. For example, a CMOS, CCD, or other photosensitive element can be textured following manufacture. In this case, material layers may be removed

from the photosensitive element to expose the semiconductor substrate or the dielectric region upon which a textured region can be formed.

Additionally, it is contemplated that the textured region can be formed having surface features with a size and position distribution that allows tuning to a desired light wavelength or range of wavelengths. As such, a given textured region can contain an arrangement of surface features that facilitate tuning of the textured region to a preselected wavelength of light. Any wavelength that can be selectively tuned via surface features in the textured region is considered to be within the present scope. In one aspect, for example, the preselected wavelength or wavelengths of light can be in the near infrared or infrared range. In another aspect, the preselected wavelength of light can be greater than or equal to about 800 nm.

In one aspect, tuning can be accomplished by generating a texture with sufficient long-range lateral order such that interference directs the photons within a certain wavelength range in such a direction that they will experience total internal reflection (TIR) on the surface opposite the texture. This will enhance absorptance and QE. In another aspect, the texture will be additionally tuned to minimize photons reflected into the range of angles where TIR will not occur. This further enhances absorptance and QE. In another aspect, the texture will be additionally tuned to keep the angle at which the photons at the preselected wavelength impinge on the surface opposite the texture as close to normal as possible while still maintaining TIR. This maximized the propagation path, thereby further increasing absorptance and QE, and simultaneously minimizing the optical crosstalk at that preselected wavelength.

For texture with poor long-range lateral order, the texture can be tuned for wavelength selection. In one aspect, the average lateral modulation spatial frequency will be large enough compared to the diffraction limited spot size at the preselected wavelength that effective index descriptions are inaccurate and scattering is substantial. In another aspect, the average modulation amplitude will not be much smaller than the preselected wavelength, so that the surface will not substantially behave as though it were planar.

Regardless of the degree of long-range lateral order, the individual features that make up the texture can be adjusted in shape so as to maximize the number of photons that are incident on the opposite surface at an angle beyond the critical angle, θ_c. In another aspect, these individual features are adjusted to minimize the number of photons that are incident on the opposite surface at an angle less than the critical angle, θ_c.

The texture can also be tuned to provide polarization selectivity. In one aspect, the rotational symmetry in the plane of the texture can be maximized, thereby leading to uniform behavior over the maximum polarization states. In another aspect, the rotational symmetry in the plane of the texture can be minimized, thereby leading to maximal difference in the behavior for differing polarization states.

One effective method of producing a textured region is through laser processing. Such laser processing allows discrete locations of the dielectric region or other substrate to be textured. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope. Laser treatment or processing can allow, among other things, enhanced absorptance properties and thus increased electromagnetic radiation focusing and detection. The laser treated region can be associated with the surface nearest the impinging electromagnetic radiation or, in the case of BSI devices, the laser treated surface can be associated with a surface opposite in relation to impinging electromagnetic radiation, thereby allowing the radiation to pass through the semiconductor substrate before it hits the laser treated region.

In one aspect, for example, a target region of the semiconductor material can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Pat. Nos. 7,057,256, 7,354,792 and 7,442,629, which are incorporated herein by reference in their entireties. Briefly, a surface of a substrate material is irradiated with laser radiation to form a textured or surface modified region. Such laser processing can occur with or without a dopant material. In those aspects whereby a dopant is used, the laser can be directed through a dopant carrier and onto the substrate surface. In this way, dopant from the dopant carrier is introduced into the target region of the substrate material. Such a region incorporated into a substrate material can have various benefits in accordance with aspects of the present disclosure. For example, the target region typically has a textured surface that increases the surface area of the laser treated region and increases the probability of radiation absorption via the mechanisms described herein. In one aspect, such a target region is a substantially textured surface including micron-sized and/or nano-sized surface features that have been generated by the laser texturing. In another aspect, irradiating the surface of the substrate material includes exposing the laser radiation to a dopant such that irradiation incorporates the dopant into the substrate. Various dopant materials are known in the art, and are discussed in more detail herein.

Thus the surface of the substrate or dielectric region is chemically and/or structurally altered by the laser treatment, which may, in some aspects, result in the formation of surface features appearing as microstructures or patterned areas on the surface and, if a dopant is used, the incorporation of such dopants into the substrate material. In some aspects, the features or microstructures can be on the order of 50 nm to 20 μm in size (i.e. size at the base, or in some cases center-to-center) and can assist in the absorption of electromagnetic radiation. In other words, the textured surface can increase the probability of incident radiation being absorbed.

The type of laser radiation used to surface modify a material can vary depending on the material and the intended modification. Any laser radiation known in the art can be used with the devices and methods of the present disclosure. There are a number of laser characteristics, however, that can affect the surface modification process and/or the resulting product including, but not limited to the wavelength of the laser radiation, pulse duration, pulse fluence, pulsing frequency, polarization, laser propagation direction relative to the semiconductor material, etc. In one aspect, a laser can be configured to provide pulsatile lasing of a material. A short-pulsed laser is one capable of producing femtosecond, picosecond and/or nanosecond pulse durations. Laser pulses can have a central wavelength in a range of about from about 10 nm to about 8 μm, and more specifically from about 200 nm to about 1200 nm. The pulse duration of the laser radiation can be in a range of from about tens of femtoseconds to about hundreds of nanoseconds. In one aspect, laser pulse durations can be in the range of from about 50 femtoseconds to about 50 picoseconds. In another aspect, laser pulse durations can be in the range of from about 50 picoseconds to 100 nanoseconds. In another aspect, laser pulse durations are in the range of from about 50 to 500 femtoseconds.

The number of laser pulses irradiating a target region can be in a range of from about 1 to about 2000. In one aspect, the number of laser pulses irradiating a target region can be from about 2 to about 1000. Further, the repetition rate or pulsing frequency can be selected to be in a range of from about 10 Hz to about 10 μHz, or in a range of from about 1 kHz to about 1 MHz, or in a range from about 10 Hz to about 1 kHz. Moreover, the fluence of each laser pulse can be in a range of from about 1 kJ/m^2 to about 20 kJ/m^2, or in a range of from about 3 kJ/m^2 to about 8 kJ/m^2.

As has been described, the devices according to aspects of the present disclosure can additionally include one or more reflecting regions. The reflecting region can be deposited over the entire textured region or only over a portion of the textured region. In some aspects, the reflecting region can be deposited over a larger area of the device than the textured region. The reflecting region can be positioned to reflect electromagnetic radiation passing through the texture region back through the textured region. In other words, as electromagnetic radiation passes into the semiconductor substrate, a portion that is not absorbed contacts the textured region. Of that portion that contacts the textured region, a smaller portion may pass though the textured region to strike the reflecting region and be reflected back through the textured region toward the semiconductor substrate.

A variety of reflective materials can be utilized in constructing the reflecting region, and any such material capable of incorporation into a photosensitive device is considered to be within the present scope. Non-limiting examples of such materials include a Bragg reflector, a metal reflector, a metal reflector over a dielectric material, a transparent conductive oxide such as zinc oxide, indium oxide, or tin oxide, and the like, including combinations thereof. Non-limiting examples of metal reflector materials can include silver, aluminum, gold, platinum, reflective metal nitrides, reflective metal oxides, and the like, including combinations thereof. In one aspect, a BSI photosensitive imager device can include a dielectric layer positioned between the reflecting region and the textured region. In one specific aspect, the dielectric layer can include an oxide layer and the reflecting region can include a metal layer. The surface of the metal layer on an oxide acts as a mirror-like reflector for the incident electromagnetic radiation from the backside. It should be noted that the reflective region is not biased with a voltage.

In another aspect, the textured region can include a hemispherical grained polysilicon or coarse grained polysilicon material and the reflective region can include a metal layer. The hemispherical grained or coarse grained silicon can act as a diffusive scattering site for the incident optical radiation and the dielectric layer and the reflective region together can act as a reflector.

In still another aspect, the photosensitive imager can include selective epitaxial silicon growth for generating the textured region on top of the junction formed by the doped regions (e.g. a photodiode) without the dielectric region being present (not shown). An oxide and metal reflector, for example, can be coupled to the textured region. The epitaxial growth places the textured region away from the top of the junction, and the rapid etch characteristics of grain boundaries can be used to create texturing.

Additionally, the textured surface of a metal on a roughened oxide can act as a diffusive scattering site for the incident electromagnetic radiation and also as a mirror-like reflector. Other aspects can utilize porous materials for the texturing. Porous polysilicon, for example, can be oxidized or oxide deposited and a reflective region such as a metal reflector can be associated therewith to provide a scattering and reflecting surface. In another aspect, aluminum can be subjected to anodic oxidation to provide porous aluminum oxide, a high dielectric constant insulator. This insulator can be coated with aluminum or other metals to provide a scattering and reflecting surface.

In one specific aspect, a reflective region can include a transparent conductive oxide, an oxide, and a metal layer. The transparent oxide can be textured and a metal reflector deposited thereupon. The textured surface of the metal on a roughened transparent conductive oxide can act as a diffusive scattering site for the incident electromagnetic radiation.

In another specific aspect, a Bragg reflector can be utilized as a reflective region. A Bragg reflector is a structure formed from multiple layers of alternating materials with varying refractive indexes, or by some other method of inducing a periodic variation in the propagation constant. Each layer boundary causes a partial reflection of an optical wave. For waves whose wavelength is close to four times the optical thickness of the layers, the many reflections combine with constructive interference, and the layers act as a high-quality reflector. Thus the coherent super-positioning of reflected and transmitted light from multiple interfaces in the structure interfere so as to provide the desired reflective, transmissive, and absorptive behavior. In one aspect, the Bragg reflector layers can be alternating layers of silicon dioxide and silicon. Because of the high refractive index difference between silicon and silicon dioxide, and the thickness of these layers, this structure can be fairly low loss even in regions where bulk silicon absorbs appreciably. Additionally, because of the large refractive index difference, the optical thickness of the entire layer set can be thinner, resulting in a broader-band behavior and fewer fabrications steps.

In another aspect, texturing can be applied to the light-incident surface of the semiconductor substrate in order to facilitate additional scattering as light enters the device. In some aspects it can be useful to also include trench isolation to preclude optical crosstalk between pixels due to this forward scattering. By also texturing the trench isolation, light can be reflected back into the semiconductor from the edges of the pixel. It is noted that, for a BSI architecture, the light-incident surface is on the back side of the semiconductor substrate opposite the photodiode.

In another embodiment of the present disclosure, a backside texture surface an imager pixel is shown in FIGS. **9***a,b*. Specifically, FIG. **9***a* shows a top view and FIG. **9***b* shows a cross sectional view of a textured region **900** including pillars etched into a semiconductor material. In one aspect, the textured region can include a plurality of pillars having a uniform size. In another aspect, the textured region can include a plurality of pillars in a regular (ordered pattern) array. In yet another aspect, the textured region can include a plurality of pillars of variable sizes (**902**, **904** in FIG. **9**). In a further aspect, the textured region can be arranged in a non-uniform array (see FIG. **9**). Similarly, holes of uniform or variable sizes can be etched into the silicon and covered by a thin layer of oxide and metal to achieve similar effects as the pillars. Moreover, the pillar or hole features can be etched into a thin layer of oxide and metal, or they can be etched into a thicker oxide on the semiconductor substrate and covered by a reflective material, such as silver or aluminum. In the former case the minimum oxide thickness between the semiconductor substrate and metal can be in the range of about 5 nm to 100 nm. In another aspect, the thickness can be about 40 nm.

The height of the pillars, shown in the cross sectional view of FIG. **9***b*, can vary depending on the design and desired use of the device. In one aspect, however, the average pillar height can be a multiple of a quarter wavelength of the desired light wavelength selectivity in the medium to which they are etched (e.g., the semiconductor material or the dielectric material. In another aspect, the average center-to-center distance between pillars can be about one half the wavelength of light desired to be absorbed (½ λ), multiples of one half the wavelength, or larger than half the wavelength of desired light selectivity. The pillars can also be designed to be anti-reflecting to the specular reflection of light or the zeroth order diffraction from the texture. The higher order diffractions of light from the texture can be designed to optimize the reflection of light at any particular oblique angle. In this manner most of the incident light can be reflected at angles to maximize light trapping in the imager pixel. Light scattered by the front side textured region and striking the semiconductor side of the back interface can be totally internally reflected if it is outside of the critical angle as defined by Snell's law.

One exemplary method of creating a textured region such as a diffraction grating is shown in FIGS. **10***a-c*. In this case, a semiconductor substrate **1002** having an oxide layer **1004** is provided. A mask **1006** as a 2-dimensional grating is formed on the oxide layer **1004**, as is shown in FIG. **10***a*. The oxide layer **1004** can then be etched with an isotropic etch **1008** to form a plurality of pillars **1010**, as shown in FIG. **10***b*. In one aspect, undercutting of the pillars by the isotropic etch **1008** can results in pillars **1010** that are narrow at the top of the pillar than the bottom. The mask **1006** can be removed and a rinse etch used to round off sharp corners and tops of the pillars **1010**, as is shown in FIG. **10***c*. A reflecting material **1012** (e.g. a metal) can be deposited as a reflector. The rounded surfaces can reduce the amplitude of the specular reflection or zeroth order diffraction of light from the diffraction grating (i.e., the textured region). Thus, the light will be scattered more effectively at oblique angles. FIG. **10***c* also shows the thickness (t_{ox}) **1014** of oxide layer **1004**, the grating thickness (t_{gr}) **1016**, and the distance from pillar peak-to-peak (T) **1018**. While the dimensions of the grating can vary depending on the design of the device and the desired usage, in one aspect the average thickness of t_{ox} can have a range of from about 10 nm to about 100 nm. In another aspect, the t_{ox} can have a thickness of less than about 50 nm. The average grating thickness t_{gr}, measured from the base of the oxide layer **1004** to a pillar peak **1010**, can be about a quarter of the wavelength of the desired light wavelength selectivity in the oxide layer (~¼λ). For example, light having a wavelength of about 1000 nm can dictate t_{gr} having a thickness of greater than about 175 nm. The average distance (T) from pillar peak-to-peak can be greater than 300 nm for light having a wavelength of greater than 1000 nm.

Another exemplary method of creating a textured region such as a diffraction grating is shown in FIGS. **11***a-d*, which are cross-sectional views of a photosensitive device at different stages of manufacturing. In one specific aspect, the semiconductor material can be amorphous silicon, which can have a texture surface with a high index of refraction because amorphous silicon can be deposited at low temperatures.

Specifically, FIGs. **11***a-d* show a one dimensional grating, such as a plurality of grooves, or in two dimensions an array of pyramidal structures being formed on or in the photosensitive device. In FIG. **11***a*, a semiconductor material **1102** can be coupled to a thin layer of oxide **1104** and a layer of nitride **1106**. In this aspect, the front side **1102** of the pixel in the P+ diode surface area has been opened in the first interlayer dielectric. The semiconductor material **1102** can be etched **1108** to form a mask **1110** using standard techniques on an opposite side where incident light enters the device. Furthermore, in some aspects another layer of a semiconductor material **1112** such as amorphous silicon can be deposited, and an anisotropic etch can be used in a "sidewall" like process. A reflecting region comprising a dielectric layer **1114** and metallic layer **1116** can be deposited on the etched surface. In one dimensional arrays this produces a series lines of material **1118** and grooves in the semiconductor material that functions as a diffraction grating **1120** (FIG. **11***c*). The distance from one groove to the neighboring groove (2k, FIG. **11***b*) can be determined by the diffraction angle for different orders (m) of diffraction. The first order diffraction, **1122**, can be selected to be a large angle βeta ((β) **1124**, thereby maximizing light trapping effects. The height of the original pillars are measured from the valley to the peak of the pillar identified as h, which determines the "blaze" angle gamma (γ) **1126** of the grating and the efficiency of the diffraction into different diffraction orders. In two dimensions, the semiconductor structure can have pillars rather than lines and the final structure is a two dimensional grating. Similar one dimensional grating design considerations can also be applied.

In yet another aspect, fully sub-wavelength pillars and grating structures can be used to form anti-reflecting structures for zeroth order diffraction or to form plasmonic structures. The zeroth order diffraction from such sub-wavelength structures can result in evanescent waves in the imager pixel. These evanescent waves will result in efficient absorption of the light striking the back in the imager pixel. Higher order diffractions in these structures will result in guided waves along the back surface but theses will be reflected by the isolation areas. In this manner efficient light trapping and absorption of infrared light can be achieved.

In other aspects of the present disclosure, various methods of making photosensitive diodes, pixels, and imagers, are contemplated. In one aspect, as is shown in FIG. **12**, a method of making a BSI photosensitive imager device can include forming at least one junction at a surface of a semiconductor substrate **1202**, forming a dielectric region over the at least one junction **1204**, and forming a textured region over the dielectric region **1206**, where the textured region includes surface features sized and positioned to facilitate tuning to a preselected wavelength of light **1208**. The dielectric region thus isolates the at least one junction from the textured region, and the semiconductor substrate and the textured region are positioned such that incoming electromagnetic radiation passes through the semiconductor substrate before contacting the textured region. The method also includes coupling an electrical transfer element to the semiconductor substrate **118** such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction. In one aspect, multiple pixels can be associated together to form an imager. A dielectric region can also be disposed on the backside of the photosensitive imager device to protect and/or reduce the dark current of the device. The method can also include coupling an electrical transfer element to the semiconductor substrate **1210** such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction.

Of course, it is to be understood that the above-described arrangements are only illustrative of the application of the principles of the present disclosure. Numerous modifications and alternative arrangements may be devised by those

skilled in the art without departing from the spirit and scope of the present disclosure and the appended claims are intended to cover such modifications and arrangements. Thus, while the present disclosure has been described above with particularity and detail in connection with what is presently deemed to be the most practical embodiments of the disclosure, it will be apparent to those of ordinary skill in the art that numerous modifications, including, but not limited to, variations in size, materials, shape, form, function and manner of operation, assembly and use may be made without departing from the principles and concepts set forth herein.

What is claimed is:

1. A backside-illuminated photosensitive image device, comprising:

a semiconductor substrate having multiple doped regions forming at least one junction;

a textured region coupled to the semiconductor substrate and positioned such that incoming electromagnetic radiation passes through the semiconductor substrate before contacting the textured region, wherein the textured region interacts with the electromagnetic radiation so as to redirect at least a portion of the electromagnetic radiation back into the semiconductor substrate,

a dielectric region positioned between the textured region and the at least one junction, the dielectric region being positioned to isolate the at least one junction from the textured region,

a reflecting region coupled to the textured region for reflecting electromagnetic radiation passing through the textured region back to the textured region, wherein the textured region is disposed between the dielectric region and the reflecting region, and

an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction.

2. The device of claim **1**, wherein the textured region includes surface features having an average center-to-center distance of one half wavelength of a preselected wavelength of light, multiples of one half wavelength of the preselected wavelength of light, or at least one half wavelength of the preselected wavelength of light.

3. The device of claim **2**, wherein the center-to-center distance distribution is a substantially uniform distance distribution.

4. The device of claim **2**, wherein the surface features have an average height of about a multiple of a quarter wavelength of the preselected wavelength of light.

5. The device of claim **2**, wherein the preselected wavelength of light is in the near infrared or infrared range.

6. The device of claim **2**, wherein the preselected wavelength of light is greater than or equal to about 800 nm.

7. The device of claim **1**, further comprising a dielectric layer positioned between the reflecting region and the textured region.

8. The device of claim **1**, wherein the reflecting region includes a member selected from the group consisting of a Bragg reflector, a metal reflector, a metal reflector over a dielectric material, and combinations thereof.

9. The device of claim **1**, wherein the textured region includes surface features selected from the group consisting of sloping, pyramidal, inverted pyramidal, spherical, square, rectangular, parabolic, ellipsoidal, asymmetric, symmetric, scallops, gratings, pillars, cones, microlenses, quantum dots, and combinations thereof.

10. The device of claim **1**, wherein the textured region includes surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof.

11. The device of claim **1**, wherein the textured region has been formed by a process selected from the group consisting of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.

12. The device of claim **1**, wherein the textured region includes surface features that are sized and positioned to reduce specular reflection in the zeroth order direction.

13. The device of claim **1**, further comprising an anti-reflective layer deposited on the semiconductor substrate at a surface opposite the at least one junction such that incident light passes through the anti-reflective layer prior to contacting the semiconductor substrate.

14. The device of claim **13**, further comprising at least one isolation feature in the semiconductor substrate, the at least one isolation feature being positioned to reflect light impinging thereon back into the semiconductor substrate.

15. A backside-illuminated photosensitive image device, comprising:

a semiconductor substrate having multiple doped regions forming at least one junction;

a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, wherein the textured region includes a plurality of grooves;

a dielectric region positioned between the textured region and the at least one junction, the dielectric region being positioned to isolate the at least one junction from the textured region, wherein the semiconductor substrate and the textured region are positioned such that incoming electromagnetic radiation passes through the semiconductor substrate and the dielectric region before contacting the textured region; and

an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction.

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