

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
24 January 2008 (24.01.2008)

PCT

(10) International Publication Number
WO 2008/009421 A2

(51) International Patent Classification: **Not classified**

(21) International Application Number:
PCT/EP2007/006334

(22) International Filing Date: 17 July 2007 (17.07.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0614299.6 17 July 2006 (17.07.2006) GB
60/807,509 17 July 2006 (17.07.2006) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

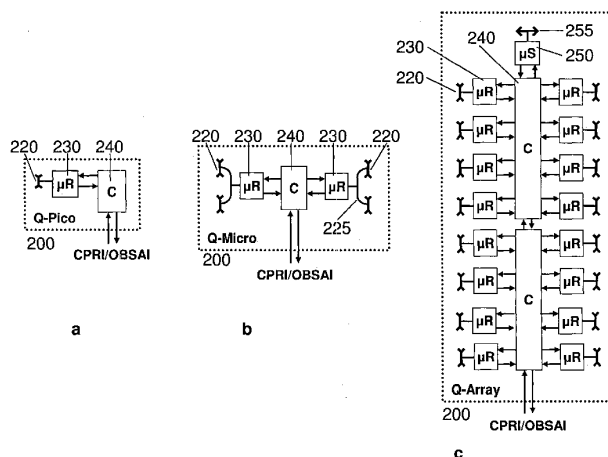
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— without international search report and to be republished upon receipt of that report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: ANTENNA ARRAY SYSTEM



(57) Abstract: Antenna system connectable to a base station, the antenna system comprising a digital radio unit (200) connectable to at least one antenna element (220), wherein the digital radio unit (200) comprises: at least one micro radio (230) for receiving/sending digital radio signals having a digital down-converter (350) / a digital up-converter (310) and a digital signal converter (234; 235). The at least one micro radio (230) converts the digital radio signals to analogue RF (radio frequency) signals and vice versa. The at least one micro radio (23) has at least one hub (240) for processing digital radio signals and control signals and for routing said digital radio signals and control signals via at least one serial link (260) and at least one interface (258, 259). The at least one serial link (260) is provided between the at least one hub (240) and the at least one micro radio (230).

WO 2008/009421 A2

Antenna Array System

Field of the Invention

The present invention relates to radio transceivers and antenna systems. In particular, the present invention relates to base transceiver stations and antennas for mobile communication systems.

Background of the Invention

Mobile communication technology has greatly advanced in recent years, as evident by the high performance digital mobile phones currently available. Mobile communication has been made available with almost 100% coverage area in many regions of the world following the demand of the users. Users wish to be able to communicate via their mobile phone (mobile stations) from anywhere they are.

As a consequence, the number of mobile stations and the number of communications links established is increasing. In addition, the amount of data transferred over a communication link is steadily increasing as it is not only desired to transfer voice messages or short messages with high quality but also increasing amounts of data, i.e. for images, movies or music etc.

In order to be reachable, a base transceiver station (BTS) has to be within the range of the mobile station. A communications link is then established between the mobile station and the BTS in which communications data are sent and received from the mobile stations and the BTS by an RF signal. The BTS transfers the communications data further into telephony or other communication networks.

Mobile service providers have to ensure that their clients can have access to a BTS almost everywhere they are. Therefore BTSs have to be distributed in order to achieve a high

-2-

coverage area. In addition, a sufficient number of BTS has to be installed in urban areas in which large numbers of mobile communication have to be performed concurrently.

Modern BTS have to cover a wide frequency bandwidth and a high dynamic range.

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In order to provide good access, antennas of BTS are usually placed in exposed places such as roof tops, tower tops or on masts, so that they are not shielded by walls or the landscape itself and the area covered can be maximized.

10 Prior Art

Base transceiver stations (BTS) known in the art usually comprise tower-top equipment and a base station.

15 The tower-top equipment mainly consists of a plurality of antenna elements forming an antenna that is mounted on exposed places such as roof tops, masts or the like, whereto and from which the RF signal can be transmitted to the mobile station with as few barriers as possible. When mounted exposed, antennas can also be widely seen. This, however, is not always wanted and frequently raises concerns with residents living close to the antennas.

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The antennas of the tower-top equipment known in the prior art are connected to radio units for transceiving the RF signals via the antenna elements of the antenna. The radio units serve as converters of RF signals into a digital base-band signal and are usually located together with further electronic equipment necessary for the BTS in a base station.

25 At present the base station requires a considerable amount of space, usually of the size of a small room. This room or container may be located in the basement or on the roof of the building on which the antenna is mounted. The base station and the radio unit are at some distance from the antenna, thus requiring a connection between them.

30 The radio unit and the antenna elements are connected with coaxial cables in order to shield them from electrical noise as far as possible. These coaxial cables are at present about 10 – 50 m in length because of the distance between the antenna and the radio unit.

-3-

The cable length has the inherent disadvantages of energy and signal to noise loss. The coaxial cable often runs along the outside of the building and is as a result unsightly.

The United Kingdom Patent Application GB 2 393 580 A describes an active antenna array with linear power amplifiers coupled proximate to the antenna elements. The connection between the base station and the radio unit is digital. The up-conversion and the down-conversion between the base-band and the carrier-band is performed in the analogue domain. The the amplification of the up-link signals and down-link signals is carried out by analogue components, such as a linear power amplifier or a low noise amplifier.

The European Patent Application EP 0 924 864 A3 relates to an automotive digital radio system that supports integration of cell phone functionality into the automotive digital radio. As such, the cell phone portion of the radio system corresponds to a mobile station (MS) in a mobile communications system. The radio system is digital because distributed components (AM/FM antenna, cellular antenna, loudspeaker, microphones etc) are connected to a digital radio signal processor via digital connections. However, within the distributed components signal processing is performed in an analogue manner. For example the antenna module located at the antenna processes much of tuning functions in analogue and then converts the signal to digital and sends it to the digital radio signal processor.

The United States Patent Application Publication US 2004/0198451 describes an intermediate frequency (IF) fibre optic communications link that communicates receive signals and transmit signals between a distributed active antenna and base station electronics in an antenna installation. Within the so-called tower top antenna structure the only digital signal processing relates to the communications link to the base station. Further signal processing, in particular up-conversion/down-conversion and amplification is performed on analogue signals.

Therefore, a system is required that minimizes or avoids the electrical losses of the RF signal and makes use of the advantages of extensive digital signal processing.

-4-

There is also a need for a BTS that requires less space and that is easier to install and maintain.

Summary of the Invention

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It is therefore an object of the present invention to provide a base transceiver station that avoids the use of coaxial cables for transferring a signal.

10 It is another object of the invention to provide a base transceiver station with low space requirements.

It is furthermore an object of the invention to provide a base transceiver station with low power electronics.

15 It is further an object of the invention to provide a digital radio unit that can be installed at the tower top equipment of a BTS in close proximity of the antenna.

It is yet a further object of the invention to provide a digital radio-unit for an all-digital antenna.

20

These and other objects of the invention are solved by an antenna system connectable to a base station. The antenna system comprises a digital radio unit connectable to at least one antenna element, wherein the digital radio unit comprises: at least one micro radio for receiving and/or sending digital radio signals having a digital down-converter and/or a digital up-converter and a digital signal converter, whereby the at least one micro radio converts the digital radio signals to analogue RF (radio frequency) signals and vice versa; at least one hub for processing digital radio signals and control signals and for routing said digital radio signals and control signals via at least one digital link and at least one interface, the at least one digital link (260) being provided between the at least one hub and

30 the at least one micro radio (230).

-5-

The radio communications stationary transmission/receiving apparatus can be used in mobile communications networks but can also be used in other communication networks.

The radio communications transmission/receiving apparatus can be stationary. A stationary apparatus is in this respect an apparatus that is used as a base station or as antenna for a base station to enable the communication with e.g. mobile communications devices. The term stationary apparatus also includes, but is not limited to, radio communications transmission/receiving apparatus that can be moved from one place to another, such as base stations that are mounted on a vehicle to be placed in areas with temporarily high access request, e.g. of events or the like.

The digital radio unit may be connected proximately to the at least one antenna element. It should be understood that the term "proximate" means that the digital radio unit and the at least one antenna element are closely located to each other. This avoids the use of long coaxial cables which would otherwise be necessary and are known in the art. The antenna element and the digital radio unit may be mounted on a single circuit board or the antenna element may be directly connected to the digital radio unit. One or more of the antenna elements may be connected to a single digital radio unit.

The digital radio signals can be digital base-band signals, digital band-pass signals or the like that can be modulated.

In a preferred embodiment, the at least one micro radio is operable in FDD mode and comprises: a FDD filter unit connected at a receive output to an input of a low noise analogue-to-digital converter (ADC) and further connected at a transmit input to an output of a power digital-to-analog converter (PDAC); a digital transceiver (DTRX) connected at an output for signal (I_{DL}) to an input of the PDAC and further connected at an input for signal (R_S) to an output of the ADC, the digital transceiver DTRX having a receive section and a transmit section, the digital up-converter being part of the transmit section and the digital down-converter being part of the receive section; a receive clock oscillator unit (RCLK) for providing a sampling clock for the ADC and for the receive section of the DTRX and for further providing a sub-sampling pulse for said receive section; a transmit

-6-

clock oscillator unit (TCLK) for providing a sampling clock for the PDAC and for the transmit section of the DTRX.

In an alternative preferred embodiment, the at least one micro radio is operable in the TDD mode and comprises: a TDD filter unit followed by a TDD switch connected at a receive output to an input of a low noise analogue-to-digital converter (ADC) and further connected at a transmit input to an output of a power digital-to-analog converter (PDAC); a digital transceiver (DTRX) connected at an output for signal (I_{DL}) to an input of the PDAC and further connected at an input for signal (R_S) to an output of the ADC, the DTRX having a receive section and a transmit section, the digital up-converter being part of the transmit section and the digital down-converter being part of the receive section; at least one clock oscillator unit (TRCLK) for providing a sampling clock for the ADC, the PDAC and the DTRX and for further providing a sub-sampling pulse for the receive section of the DTRX and a time control signal for the TDD switch.

The at least one clock oscillator unit may be a single transceiver clock oscillator unit. Alternatively, a plurality of clock oscillators may each provide sampling pulses to components of the digital radio unit.

In one embodiment, the analogue-to-digital converter (ADC) is a low noise analogue-to-digital converter. The (ADC) can comprises a low noise amplifier followed by a continuous-time sigma-delta band-pass modulator converting the RF signal at the input directly into a single/1.5 bit band-pass output signal (R_S).

In further embodiments of the antenna system as described above the power digital-to-analog converter (PDAC) utilizes 2 or 3 voltage levels to convert a single/1.5 bit band-pass input signal (I_{DL}) directly into a RF output signal.

In a further preferred embodiment, the micro radio is monolithically integrated by micro-electronic means or as a multi-chip module.

-7-

The digital radio unit comprising the at least one micro radio and the at least one hub may also be integrated by micro-electronic means or as a multi-chip module.

5 In a further embodiment of the invention, one digital radio unit is provided for each antenna element.

Description of the Drawings

10 The features of the present invention may be better understood when reading the detailed description and the figures, wherein identical numbers identify identical or similar objects.

Fig. 1 shows a mobile communications network

15 Fig. 2 shows base station configurations according to prior art and according to the present invention.

Fig. 3a to 3c shows different configurations of the all-digital antenna system according to the present invention.

20 Fig. 4a shows in detail the components of a digital radio unit for FDD radio links according to the invention.

Fig. 4b shows an example of the data frame format used between the μ -radio and the C-Hub in Fig 4a.

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Fig. 4c shows in detail the components of a micro radio for TDD radio links according to the invention.

30 Fig. 5 depicts a functional block diagram of a digital transceiver (DTRX) according to the invention in 4:1 mode.

-8-

Fig. 6a and 6b show functional block diagrams of two embodiments of a digital transceiver (DTRX) in 4:3 mode.

Fig. 7a shows the block diagram of a generic digital quadrature modulator with 1:2 over-sampling pre-stage having the identical functionality as the quadrature modulation by multiplexing and cyclic negation block of the DUC of Fig. 5.

Fig 7b shows illustrative examples of signals of the generic digital quadrature modulator with 1:2 over-sampling pre-stage of Fig. 7a.

10

Figs. 8a – 8i show examples of signals at different lines of the digital quadrature modulator in in-phase version shown in Fig. 7a.

Fig. 9 shows a pipelined realization of the quadrature modulation by 2:1 multiplexing and cyclic negation block of the DUC of Fig. 5.

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Fig. 10 shows the structure of a generic digital quadrature de-modulator followed by low-pass decimators having together the identical functionality as the quadrature de-modulation by de-multiplexing and cyclic negation block and low-pass decimators of the DDC of Fig. 5.

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Fig. 11 shows illustrative examples of signals at different lines of Fig 10.

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Fig. 12 shows the block diagram of a systolic N:1 decimator for digital down conversion.

Fig. 13 shows a systolic DDC block realizing N:1 decimation of an 1.5 bit signal

Fig. 14 shows a bit-slice of the convolution unit in a systolic DDC block for N:1 decimation.

Detailed Description

Fig. 1 shows an overview of a mobile communications network. A mobile station 2 can communicate via radio links with a base transceiver station (BTS) 100 when the mobile station 2 is within the range 4 of the BTS 100. A mobile station 2 is any mobile or immobile communication device that enables communication via radio links, usually at radio frequencies (RF) in the range of 800 MHz up to several GHz. Common examples for mobile stations are, but are not limited to, mobile telephones, pocket PC, data cards etc.

If a mobile station 2 is in the range of the BTS 100 data communication may be established between the mobile station 2 and the BTS 100. The data communication may be used to transfer voice and/or data. During communication the BTS 100 sends RF signals that are received by the mobile station 2 via a radio downlink and receives RF signals sent by the mobile station 2 via a radio uplink. In the Frequency Division Duplex (FDD) mode two different frequency bands are utilized to separate the radio downlink from the radio uplink. In the Time Division Duplex (TDD) mode, however, only one frequency band is used in both directions downlink and uplink. The separation is performed in the time domain by using the same frequency band alternately in downlink and uplink direction. Thus, in TDD mode the antenna plus band-pass filter is periodically switched either to the transmit path or to the receive path. Both modes are utilized in different mobile radio standards, although FDD is more widespread than TDD.

From the BTS 100, data (which includes data communication data and voice data) are transferred to a base station controller 12. The base station controller (BSC) 12 separates voice data and data communication data and sends the voice data and the SMS data to a mobile switching centre (MSC) 16 from which the voice data and the SMS data are further transferred to a telephony network 30 to which the MSC 16 is linked. Other data are sent by the BSC 12 to a Serving and Gateway GPRS Support Node (GSN) 18 and are further transferred to a data network 40, such as the Internet. It is understood that all communications flow may be in both directions. Data are also sent from the data network 40 and/or the telephony network 30 in the opposite direction to the BTS 100 from which

-10-

the data are sent by radio waves as RF signal to the mobile station 2. Several mobile stations 2 may be communicating with a single BTS 12 at the same time.

Fig. 2 shows three different configurations of base transceiver stations (BTS) 100. All BTS
5 100 comprise tower-top equipment 102 that is usually mounted – as discussed in the introduction - in an elevated position, such as on roof tops or towers, in order to maximize the coverage area of the BTS 100. The tower-top equipment 102 is connected to a base station 104 that may be in a specific housing beside or at some distance from the tower-top equipment.

10

In a first configuration (A) known in the art, a set of antennas or antenna elements 120 for receiving and sending radio signals from and to the mobile station 2 is linked with a coaxial cable 122 to a collocated radio unit 124. An analogue RF is received at the set of antennas or antenna elements 120 and passed to the collocated radio unit 124. In the
15 collocated radio unit 124, the analogue radio RF signal is amplified, separated from a carrier frequency and converted into a digital signal. The digital signal is then further transferred to a digital radio server 128 from which the digital signal is passed on to the BSC 12 shown in Fig. 1 or vice versa. The length of the coaxial cable affects the signal-to-noise ratios and the efficiency of the BTS 100 as well as for the electrical power consumed
20 and the configuration of electronics components necessary.

25

As discussed above, the tower-top equipment is in many cases located at exposed places such as tower tops, roofs or on the top of masts in order to maximize the area covered by the antennas. The length of the coaxial cable 122 may therefore become inefficiently long.

In a second configuration (B), a remote radio unit 134 is mounted at the tower top equipment 102. In that way a shorter coaxial cable 132 can be used to connect antennas or antenna elements 130 to the remote radio unit 134. The remote radio unit 134 converts modulated RF signals to communications signals in digital data format according to the
30 CPRI or OBSAI standard. The communications signals are then transferred via optical fibres 136 to a digital radio server 138 that may be essentially identical or similar to digital radio server 128.

-11-

In configuration (A) and (B), the plurality of antenna elements form an antenna 120; 130 that is connected via one coaxial cable 122; 132 to the single radio unit 124; 134. The radio unit 124, 134 must then separate signals received from the plurality of antenna elements in order to separate different communications links handled in parallel.

In a third configuration (C) according to the present invention, a digital radio unit 200 is directly connected to the plurality of antenna elements 220 forming the antenna. Each one of the antenna elements 220 is thereby directly connected to the digital radio unit or its components. In this embodiment no coaxial cable is required in order to couple the digital radio unit 200 to the antenna elements 220. The digital radio unit 200 converts RF signals received and transmitted via the antenna elements 220 from/to the mobile station 2 into signals according to CPRI or OBSAI standard/interface. These signals are then transferred via optical fibres to a digital radio server 208 located at base station 104. The optical fibre may thereby be up to 40 km long enabling the remote location of the base station 104 with respect to the tower-top equipment.

It is an advantage of the present invention that only the antenna elements 220 together with the digital radio unit 200 have to be installed at the location of the antenna. The base station 104 may be at some distance away. It is also possible, especially in urban areas with high antenna density, to connect several tower top equipments to a single one of the base stations 104.

The digital radio servers 128; 138; 208 may thereby be of the same type in all configurations (A) (B) and (C).

Fig. 3a to 3c show different embodiments of the digital radio units 200 according to the present invention. The digital radio unit 200 comprises at least one antenna element 220, at least one micro radio 230, and at least one hub 240, also referred to as "C-hub".

30

In the embodiment shown in Fig. 3a, the digital radio unit 200 comprises a single antenna element 220 directly connected to one micro radio 230 and one C-hub 240. The micro

-12-

radio 230 communicates with the C-hub 240 in a receiving and sending direction. The bi-directional serial interface between micro radio and C-hub is based on the well known standard termed 'SerDes'. The C-hub 230 is further connected to the digital radio server 208, i.e. via an optical fibre as shown in Fig. 2.

5

A plurality of the embodiments of Fig. 3a may be arranged and coupled in an array.

In the embodiment shown in Fig. 3b, a C-hub 240 is connected to two micro radios 230. Each of the micro radios 230 communicates in sending and receiving direction with the C-hub 240. Further, each micro radio 230 is connected to two antenna elements 220 via a so called Wilkinson splitter 225 known in the art.

10

Fig. 3c shows another embodiment of the present invention. In this embodiment a plurality of micro radios 230 are connected to one C-hub 240 whereby each of the micro radios 230 communicate in sending and receiving direction with the C-hub 240. Sixteen micro radios 230 are shown in Fig. 3c but this is not limiting the invention. In this example, each one of the micro radios 230 is connected to a antenna element 220. Several C-hubs 240 each with 8 micro radios 230 and 8 antenna elements 240 may be linked together to form arrays of 16 or more antenna elements 220.

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It will be obvious to a person skilled in the art that the embodiments shown are examples only and that any number of micro radios 230 may be connected to a C-hub 240. It is also obvious to a person skilled in the art that the number of antenna elements 220 per micro radio 230 can vary according to the needs of a particular application, although it is preferred to have one or two antenna elements 220 per micro radio 230. In addition, a plurality of C-hubs 240 can be coupled together (as is shown in Fig. 3c which includes two C-hubs 240).

25

In addition, a so called 'micro-sniffer' (μ S) 250 can be connected to one of the C-Hubs 240 for monitoring and calibrating purposes. The micro-sniffer 250 is a special micro radio having inverse receive and transmit frequency band. The micro-sniffer 250 can be connected to the C-Hub 240 via the same or a similar interface. The micro-sniffer 250

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-13-

additionally has an antenna 255 that may have the form of an antenna element or another form. The micro-sniffer 250 transmits pilot signals towards and detects the radiation emitted from the antenna elements 220, thus providing the C-Hubs 240 with feedback control information as required by the micro radios 230 for calibration purposes.

5

Fig. 4a shows in greater detail a micro radio 230 and a C-hub 240 connected via a digital bi-directionally serial link (260) forming together a digital radio unit 200 according to the invention. The antenna element 220 is directly connected to the micro radio 230. The antenna element 220 may, for example, be mounted on an antenna board or another circuit board onto which the micro radio 230 is arranged or attached. In an alternative
10 embodiment, the micro radio 230 may be realized directly on the printed board.

The micro radio 230 shown in Fig. 4a is operated in FDD mode, thus comprising a FDD filter unit 232 at its antenna element entry which separates the RF signals in uplink and downlink direction by utilizing a combination of two band-pass filters embedded in the
15 filter unit 232.

In uplink direction, a RF (radio frequency) signal received via the antenna element 220 and filtered by the FDD filter unit 232 is converted into a digital band-pass signal R_S by the low-noise analogue-to-digital converter (ADC) 235. The ADC 235 and the digital down
20 converter DDC 350 are clocked by a receive clock oscillator (RCLK) 237. The digital band-pass signal R_S is down converted into a digital base-band signal by the digital down converter (DDC) 350 integrated in a digital transceiver (DTRX) 300. The DTRX 300 is arranged at the digital port of the micro-radio 230 from where the digital base-band signal
25 is transferred to the C-hub 240.

The ADC 235 comprises a low-noise amplifier followed by a continuous-time sigma-delta band-pass modulator, both known in the art. The continuous-time sigma-delta band-pass modulator converts the incoming RF signal into the digital band-pass signal R_S by utilizing
30 a 2 or 3 level quantizer at a sample rate being 4 or 4/3 times the RF carrier frequency. Thus, the digital band-pass signal R_S comprises the representative levels +1, -1 or +1, 0, -1 coded by one or two bits, respectively. This digital signal format is further on termed as

-14-

'single/1.5bit' or 'bi-serial' in contrast to a 'multi-bit' format comprising more than 3 representative levels.

In downlink direction, a digital base-band signal received from the C-hub 240 is input into the DTRX 300 of the micro-radio 230 where it is up-converted into a digital band-pass signal I_{DL} by a digital up-converter (DUC) 310. The digital band-pass signal I_{DL} is then transferred to a power digital-to-analog converter (PDAC) 234 where it is converted into a RF signal. The PDAC 234 and DUC 310 are clocked by the transmit clock oscillator (TCLK) 236 at a sample rate being 4 or 4/3 times the RF carrier frequency. The RF signal is then passed through the FDD filter unit 232 and radiated via the antenna element 220. A separate power amplifier normally used in RF transmitters is not necessary because the power digital-to-analog converter (PDAC) 234 provides a sufficiently powered RF signal to be radiated via the antenna element 220.

The micro radio 230 shown in Fig. 4c is operated in TDD mode, thus comprising a TDD filter unit 233 at its antenna element entry followed by a TDD switch 239 which separates the RF signals in uplink and downlink direction within the time domain. The TDD switch 239 is controlled by a periodic signal 238 which is generated within the transceive clock oscillator (TRCLK) unit 2367 utilizing a synchronous counter which derives the periodic signal 238 from the transmit clock signal, a method well known in the art. The TRCLK unit 2367 further provides a common sampling clock for the transmit path as well as the receive path of the micro radio 230 plus a sub-sampling pulse (3781) for the DDC (350) utilizing another synchronous counter. The common sampling clock is sufficient because in TDD mode the same carrier frequency is used uplink and downlink, thus the sampling clock frequency being 4 or 4/3 times the carrier frequency (as discussed above) is also the same used uplink and downlink. All other elements and functions of the micro radio 230 operated in TDD mode are the same as shown in Fig. 4a for the micro radio 230 operated in FDD mode.

The digital up-converter (DUC) 310 contains one time-discrete sigma-delta band-pass modulator or alternatively two time-discrete sigma-delta low-pass modulators. In both cases, the modulators perform coarse quantization by use of 2 or 3 levels only providing a

-15-

single/1.5bit signal at the output. Thus, the digital band-pass signal I_{DL} being generated by the digital up-converter (DUC) 310 only comprises the representative levels +1, -1 or +1, 0, -1 coded by one or two bits, respectively. Therefore, the power digital-to-analog converter (PDAC) 234 utilizes only 2 or 3 voltage levels, respectively, to represent the
5 digital band-pass signal I_{DL} in the analog domain.

The transmit clock oscillator (TCLK) unit 236 and the receive clock oscillator (RCLK) unit 237 are each comprising mainly a voltage controlled oscillator (VCO) embedded in a phase-locked loop (PLL) used for synchronization purposes. Clock oscillators utilizing a
10 VCO plus PLL are known in the art and standard components or architectures may be applied.

It should be noted here, that those embodiments of the invention where the samples of signals I_{DL} and R_S are represented in the 2-level format can be interpreted as a special case
15 of the major embodiments of the invention utilizing the 3-level format to represent the samples of signals I_{DL} and R_S . In both cases, two's complement arithmetic is applied. In case of the major embodiments, the representative levels +1, 0, -1 are coded by two bits where the upper bit denotes the sign-bit whilst the lower bit denotes the zero-bit being cleared (low state) when a zero-sample occurs. Thus, the major embodiments of the
20 invention can be operated also in a special mode using the 2-level format by keeping the zero-bit always at high state (non-zero).

The micro-radio 230 is connected to the C-hub 240. A bi-directional serial link (260) between the micro-radio 230 and the C-hub 240 is based on the well known standard
25 termed 'SerDes'.

As known in the art, SerDes utilizes a self-clocking and DC-free channel code termed '8B/10B' representing each data byte by a code word comprising 10 bits whilst dedicated sequences of 10 bits are provided for synchronization. The SerDes functionality basically
30 comprises parallel-to-serial as well as serial-to-parallel conversion, channel coding and decoding plus clock recovery and synchronization.

-16-

In low-cost CMOS technologies, SerDes supports symbol rates up to 2.5 Giga Baud representing a gross data rate of 2.0 Giga bits per second equivalent to 250 Mega bytes per second due to code rate 0.8 of the 8B/10B channel code.

- 5 An example of the data format used on the bi-directional serial link (260) between the micro radio 230 and the C-Hub 240 is shown in Fig. 4b and described in detail below.

The C-hub 240 comprises an amplitude and phase aligner (APA) 241 including a frame buffer and a serializer/de-serializer. APA 241 has N-ports for connecting N micro-radios.

- 10 A plurality of micro-radios 230, 231 may be connected to one of the C-Hubs 240 as described with respect to Fig. 3c. In total N of the micro radios 230, 231 may be each connected to a port of the N-port phase aligner 241 and the signals received and transmitted from each one of the micro radios 230, 231 are treated in parallel and/or series by the subsequent components of C-Hub 240. The additional first and next micro-radios
15 231, may be identical to micro-radio 230, shown in greater detail in Fig. 4a.

- The C-hub 240 comprises as further components a sample rate converter (SRC) 242 for adjusting the sampling frequency of the complex base-band signal to the RF carrier frequency, a frequency multiplexer/de-multiplexer (FMDX) 243, a unit 244 comprising
20 time multiplexer/de-multiplexers (TMDX) around a hub and finally a master serializer/de-serializer (SerDes) 249 plus one or more serializers/de-serializers (SerDes) 248.

- The TMDX and hub unit 244 performs packet data handling and distribution of data streams in CPRI and/or OBSAI format controlled by adjacent signalling information. Thus,
25 only those data packets which are dedicated to be received and transmitted by the connected micro-radios 230, 231 are handed over from/to the FMDX unit 243 for further processing. Other data packets are passed through via the CPRI and/or OBSAI links supporting the so called cascading. The data packets contain I and Q samples of base-band signals in a given packet format which is identified by the adjacent signalling information.
30 The packet format defines the number and word length of the samples, the bandwidth of the base-band signal being represented by said samples and the frequency of its sub-carrier.

-17-

The frequency multiplexer/de-multiplexer (FMDX) unit 243 comprises several digital modulators and de-modulators for simultaneously up and down converting a variety of base-band signals to/from its respective sub-carrier frequencies. The modulated signals can be easily combined in the frequency domain by use of a simple adder stage, thus enabling multi-carrier operation.

All components of the C-hub 240 are controlled by a micro-controller (μ CTRL) 245 to whom they are connected via a control bus 247 and clocked by a master clock oscillator (MCLK) unit 246 comprising a voltage controlled oscillator (VCO) embedded in a phase-locked loop (PLL) used for synchronization purposes. The master clock oscillator 246 must be synchronized to the clock frequency of the CPRI and/or OBSAI transport signal (both of which formats utilize the self-clocking SerDes protocol) derived by the clock recovery unit within the master serializer/de-serializer (SerDes) 249. The master clock oscillator (MCLK) 246 also synchronizes the transmit clock oscillator 236 and the receive clock oscillator 237 of the micro radios 230/231.

All components of the C-hub 240 can be commercially available components known to a person skilled in the art.

A small form-factor module (SFF) 250 comprising one or more electro-optical converters (E/O) 258 and 259 is connected to the SerDes 248 and 249, respectively. Electro-optical converters are known in the art and are applied to convert the digital electrical signal into an optical signal that can be transferred with known standards such as CPRI (common public radio IF) or OBSAI, i.e. via optical fibres to a digital radio server as shown in Fig. 2.

Fig. 4b shows the data format of the bi-directional serial interface between the micro-radio 230 and the C-Hub 240. A data frame format comprising FL bytes is used in either direction. As depicted in Fig. 4b, the header contains a frame synchronization byte and a control byte followed by K data bytes and some non-dedicated residual bytes free for arbitrary use. Thus, the frame is only partially pay-loaded. This partially pay-loaded frame format combined with frame data buffering enables the tuning of the carrier frequencies

-18-

used in both transmit and receive paths of the micro-radio 230 whereas the over-sampling ratios N_T and N_R within the DTRX 300 remain constant as well as the clock rate of the bi-directional serial interface being always 2.5 GHz.

- 5 Assuming a preferred format of 16 bits or 2 bytes per sample for each in-phase and quadrature component of the complex base-band signal, the sample rate (SR) being transmitted over each serial 2.5 GHz link is given in MHz by $SR = 125 \cdot K/FL$.

In practice, FL comprises several hundred bytes whereas SR is in the range of 120 MHz.

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Thus, the carrier frequencies used in the micro radio 230 in 4:1 mode can be tuned by a step size $\Delta f_{CT} = \frac{1}{4}N_T \cdot SR_T/FL_T$ in the transmit path and by a step size $\Delta f_{CR} = \frac{1}{4}N_R \cdot SR_R/FL_R$ in the receive path.

- 15 When the micro radio 230 is used in 4:1 mode utilizing a DTRX 300 as described in detail with respect to Fig. 5, the micro radio 230 supports complex base-band signals having a bandwidth of 60 MHz at carrier frequencies around 2 GHz. According to Shannon's sampling theorem, each component of this complex base-band signal requires a sampling rate being at least 60 MHz.

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Thus, a fine-tuneable over-sampling ratio of approximately 2 is applied by a sample rate converter (SRC) 242 within the C-Hub 240 adapting the base-band sampling rate to those sampling rates SR_T and SR_R utilized on the bi-directional serial interface.

- 25 Fig. 5 shows a functional block diagram of a DTRX 300 in a 4:1 operating mode. The DTRX 300 may work over a 60 MHz bandwidth at carrier frequencies around 2 GHz. The DTRX 300 is divided into two parts, the DUC 310 and the DDC 350, that respectively provide base-band to carrier frequency up-conversion and carrier frequency to base-band down-conversion.

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In the 4:1 mode and in the transmitting direction, a data signal from C-Hub 240 according to the data format shown in Fig. 4b being based on the SerDes standard is applied to the

-19-

DUC 310 as an I-signal (in-phase signal) and a Q-signal (quadrature signal). The data signal may be input at rates of 2.5 Gbps. Both signals are first decoded and buffered at a SerDes Decoder and Buffer 312 and 313 for the I-signal I_0 and the Q-signal Q_0 , respectively. The data signals are then further transferred as 16 bit word length signals to units 314 and 315, respectively, comprising sample-and-hold stages plus FIR low-pass filters where the I-signal and the Q-signal are over-sampled by $1\frac{1}{2} \cdot N_T$. The SerDes Decoders and Buffers 312 and 313 and the over-sampling by sample-and-hold plus FIR low-pass filter units 314 and 315 are known in the art and standard components or architectures may be applied.

Both the I-signal and the Q-signal are then further transferred to systolic sigma-delta low-pass modulators 316 and 317, respectively, which are described in our co-pending US provisional patent (Attorney Docket Number: 90561US) and UK Patent Application No. GB 0611096.9., both filed on 2 June 2006. The teachings of this patent application are incorporated herein by reference.

The sigma-delta low pass modulator 316 outputs a 3 level signal I_{SD} and the sigma-delta low pass modulator 317 outputs a 3 level signal Q_{SD} . Both 3 level signals comprising the values +1, 0, -1 are each represented by 2 bits, thus being further addressed as '2-bit signals'.

Both 2-bit signals I_{SD} and Q_{SD} are applied to a quadrature modulation by multiplexing and cyclic negation block 340 in which the signal I_{SD} and the signal Q_{SD} are over-sampled by 1:2, cyclically negated and 2:1 multiplexed to a single 2-bit output signal I_{DL} applied to the PDAC 234 shown in Fig. 4a. The function of the quadrature modulation by multiplexing and cyclic negation block 340 will be described in detail with respect to Figs. 7a, 7b and 8a-i.

In receiving direction a 2-bit signal R_S also representing 3 levels (+1, 0, -1) is received at the DTRX 300 from the ADC 235 shown in Fig. 4a and applied to a quadrature demodulation by de-multiplexing and cyclic negation block 360 of DDC 350 in DTRX 300. The 2-bit signal R_S is 1:2 de-multiplexed, cyclically negated and 2:1 sub-sampled to a 2-bit

-20-

I-signal I_{DM} and a 2-bit Q-signal Q_{DM} . The function of the quadrature de-modulation by de-multiplexing and cyclic negation block 360 will be explained in detail with respect to Figs. 10 and 11.

- 5 The signals I_{DM} and Q_{DM} are further passed on to systolic FIR decimator blocks 356 and 357, respectively, where the signals are decimated by FIR filtering and $\frac{1}{4} \cdot N_R:1$ sub-sampling and output as a 16-bit I-signal and a 16-bit Q-signal. The systolic FIR decimator blocks 356 and 357 will be described in detail with respect to Figs. 12, 13 and 14.
- 10 From the systolic FIR decimator blocks 356 and 357 the I-signal and the Q-signal are further transferred as 16-bit signals to FIR low-pass and sub-sampling blocks 354 and 355, respectively, where the I-signal and the Q-signal are 2:1 sub-sampled. Both the I-signal and the Q-signal are then passed on to a SerDes encoder and buffer 352 and 353, respectively, from where the I-signal and the Q-signal are output from the DDC 350 and
- 15 sent to C-hub 240 as shown in Fig. 4a. The FIR low-pass and sub-sampling blocks 354 and 355 and the SerDes encoders and buffers 352 and 353 are known in the art and standard components or architecture may be applied.

Figs. 6a and 6b show a functional block diagram of two different alternative embodiments of DTRX 300 in 4:3 operating mode (4:3 mode). In 4:3 mode, the DTRX 300 may work at a 20 MHz bandwidth at carrier frequencies around 2 GHz.

20

In 4:3 mode the DTRX 300 and its component may be the same or similar to the DTRX used in 4:1 mode as described with respect to Fig. 5. Thus, the DTRX in 4:3 mode is divided into two parts, the DUC 310 and the DDC 350, that provide base-band to carrier frequency up-conversion and carrier frequency to base-band down-conversion, respectively.

25

In contrast to the 4:1 mode, a data signal from C-Hub 240 in 4:3 mode is applied to the DUC 310 as a single bit stream only. The data signal may be input at rates of 2.5 Gbps. The incoming signal is first decoded, buffered, and de-multiplexed into an I-signal and a Q-signal by a SerDes decoder, frame buffer and de-multiplexer block 311. The de-

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-21-

5 multiplexed and separated I-signal and Q-signal are further transferred separately as 16-bit word length signals to over-sampling by sample-and-hold plus FIR low-pass filter units 314 and 315, respectively, as described above with respect to Fig. 5. All further signal treatment of this embodiment is identical to the 4:1 mode described above. I-signal and Q-signal are further passed from over-sampling by sample-and-hold plus FIR low-pass filter units 314 and 315 to systolic sigma-delta low-pass modulators 316 and 317, respectively.

Each of the sigma-delta low pass modulators 316 and 317 outputs a 3 level signal (+1, 0, -1) represented by 2 bits, thus being addressed as '2-bit signal'. Both 2-bit output signals of the sigma-delta low-pass modulators 316 and 317 are connected to the quadrature modulation by multiplexing and cyclic negation block 340, where the I-signal and Q-signal are over-sampled by 1:2, cyclically negated and 2:1 multiplexed into a single 2-bit output signal applied to the PDAC 234 shown in Fig. 4a. In 4:3 mode however, the sampling rate is $f_{\text{Sampling}} = 4/3 \cdot f_{\text{Carrier}}$.

15 In receiving direction of the embodiment shown in Fig. 6a and analogous to the embodiment of Fig. 5, a 2-bit signal is received from the ADC 235 shown in Fig. 4a and applied to a quadrature de-modulation by de-multiplexing and cyclic negation block 360 of DDC 350 in DTRX 300 working in 4:3 mode. The signal is 1:2 de-multiplexed, cyclically negated and 2:1 sub-sampled into an I-signal (in-phase signal) and a Q-signal (quadrature signal) at $f_{\text{Sampling}} = 4/3 \cdot f_{\text{Carrier}}$. The 2-bit I-signal and the 2-bit Q-signal are further passed on to systolic FIR decimators 356 and 357, respectively, and then transferred as 16-bit signals to FIR low-pass and sub-sampling blocks 354 and 355, respectively.

25 In contrast to the 4:1 mode embodiment shown in Fig. 5, in the 4:3 mode both 16-bit signals are then applied to one multiplexer, frame buffer, and SerDes encoder 351, from where the multiplexed signal is output from the DDC 350 and sent to C-hub 240 as shown in Fig. 4a.

30 Fig. 6b illustrated yet another example of a DTRX 300 in 4:3 mode. In this embodiment and in transmitting direction of the DUC 310, the quadrature modulation by multiplexing and cyclic negation block 340, which may be comparable to the quadrature modulation by

-22-

5 multiplexing and cyclic negation block 340 of the embodiment of Fig. 5 and 6a, is connected directly to both over-sampling by sample-and-hold plus FIR low-pass filter units 314 and 315. The I-signal and Q-signal provided at the outputs of units 314 and 315 are over-sampled by 1:2, cyclically negated and 2:1 multiplexed into a single 16-bit output signal that is applied to a single systolic sigma-delta band-pass modulator 318, which is described in our co-pending US provisional patent (Attorney Docket Number: 90561US) and UK Patent Application No. GB 0611096.9., both filed on 2 June 2006. The 2-bit output signal of the single systolic sigma-delta band-pass modulator 318 is then applied to the PDAC 234.

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The receiving DDC 350 may in this embodiment be identical to that described with respect to Fig. 6a.

15 Fig. 7a shows a unit 3400 comprising a generic digital quadrature modulator 3410 combined with a 1:2 over-sampling pre-stage 3200. The over-sampling pre-stage 3200 consists of two equally tapped FIR low-pass filters 3360 and 3370 as well as two interpolating blocks 3260 and 3270 which are fed by the input signals I_{SD} and Q_{SD} . Over-sampling 1:2 prior to the quadrature modulator is needed because the signals I_{SD} and Q_{SD} are output by sigma-delta low-pass modulators generating significant out-of-band quantization noise. Without the over-sampling pre-stage 3200 the out-of-band quantization noise would be shifted by the quadrature modulation process into the pass-band of the band-pass signal I_{DL} at the modulator output. Fig 7b shows illustrative examples of corresponding signals.

25 In a first step below, the functionality of the unit 3400 will be explained in detail referring to Figs. 7a and 7b. In a second step, it will be shown for a special case being relevant for the embodiments of this invention that the functionality of the unit 3400 is equivalent to the functionality of the quadrature modulation by multiplexing and cyclic negation block 340 of the DUC 310 of the DTRX 300 of Fig. 5. However, the realization of the quadrature modulation by multiplexing and cyclic negation block 340 is much simpler compared to a realization of the unit 3400.

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-23-

The 2-bit I-signal I_{SD} from the systolic sigma-delta low-pass modulator 316 as depicted in Fig. 5 is assumed to be applied to an interpolating block 3260 of the over-sampling pre-stage 3200. In parallel, the 2-bit Q-signal Q_{SD} from the systolic sigma-delta low-pass modulator 317 is assumed to be applied to an interpolating block 3270 of the over-sampling pre-stage 3200. Examples of sequences of input signals I_{DS} and Q_{DS} are shown in Fig. 8a and 8b, respectively.

At the interpolating blocks 3260 and 3270, I_{SD} and Q_{SD} are 1:2 over-sampled respectively. First, the clock rate is doubled and zero samples are inserted in signals I_{SD} and Q_{SD} obtaining signals $I_{SD\uparrow 2z}$ and $Q_{SD\uparrow 2z}$. Examples for the signals Q_{SD} and $Q_{SD\uparrow 2z}$ are shown in Fig 7b. The signals $I_{SD\uparrow 2z}$ and $Q_{SD\uparrow 2z}$ are then applied to low-pass filters 3360 and 3370, respectively where the signals $I_{SD\uparrow 2z}$ and $Q_{SD\uparrow 2z}$ are each divided into two lines. One line is directly applied to adders 3340 and 3350, respectively, while the other line is passed through registers 3320 and 3330, respectively. In registers 3320 and 3330, the signal is delayed by one clock cycle and then applied to the adders 3340 and 3350, respectively, resulting in signals $I_{DS\uparrow 2}$ and $Q_{DS\uparrow 2}$ showing duplicated adjacent samples, examples of which are shown in Figs. 7b, 8d and 8e.

It should be noted that the duplication of adjacent samples as a result of an interpolation by equally tapped FIR low-pass filtering can be performed also by use of a sample-and-hold stage. In case of higher over-sampling ratios, the use of a sample-and-hold stage is much more economic compared to equally tapped FIR low-pass filters. Therefore, sample-and-hold stages are utilized within the over-sampling blocks 314 and 315 as depicted in Figs. 5, 6a and 6b.

The signals $I_{DS\uparrow 2}$ and $Q_{DS\uparrow 2}$ are further applied to the quadrature modulator 3410. In the generic digital quadrature modulator 3410 the over-sampled input signals $I_{SD\uparrow 2}$ and $Q_{SD\uparrow 2}$ are pair wise multiplied in multipliers 3460 and 3470 by the two components I_0 and Q_0 , respectively, of a complex carrier signal (I denotes the respective in-phase component and Q denotes the respective quadrature component). Examples of signals I_0 and Q_0 are illustrated in Figs. 8c and 8f, respectively. Feeding the resulting signal products $I_0 \cdot I_{DS\uparrow 2}$ as shown in Fig. 8g and $Q_0 \cdot Q_{DS\uparrow 2}$ as shown negated in Fig. 8i into a comparator stage 3480

-24-

yields at the output of the quadrature modulator 3410 the in-phase component I_{DL} of the complex digital band-pass signal for the down-link channel. The resulting example signal I_{DL} is shown in Fig. 8h.

5 A preferred choice of the sampling frequency being four times the carrier frequency is demonstrated by the signal diagrams in Fig. 8. In this particular case, the quadrature modulator 3410 and the over-sampling pre-stage 3200 together are interlacing both input signals I_{SD} and Q_{SD} whilst the input signals I_{SD} and Q_{SD} signals are cyclically negated to generate the output signal I_{DL} as illustrated in Fig 8h.

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Therefore, the generic digital quadrature modulator 3410 together with the over-sampling pre-stage 3200 of Fig. 7a can be replaced by a much simpler circuitry 340 illustrated in Fig. 9 comprising only a multiplexer 348 to interlace the input signals I_{SD} and Q_{SD} and cyclically controlled inverters, provided that the 2-bit input signals I_{SD} and Q_{SD} are
15 generated in two's complement notation. Thus, the cyclic negation can be performed by inverting the upper bit denoting the sign of the 3 level signal (+1, 0, -1) but only in the non-zero case whilst the lower bit denoting a zero remains unchanged in any case.

Fig. 9 shows the unit 340 performing quadrature modulation in 4:3 mode by 2:1
20 multiplexing and cyclic inversion. 2-bit input signals I_{SD} and Q_{SD} are first read into register 341, transferred to a cyclic negation block 343 clocked by clock the divider 342. In the cyclic negation block 343 the I- and Q-signals are cyclically negated by inverting the upper bit but only in the non-zero case. Subsequently, the cyclically negated I- and Q-signals are transferred into register 344 before they are interlaced by a 2:1 multiplexer 348. Interlacing
25 I and Q by the 2:1 multiplexer 348 is triggered by second clock divider 347. Thus, at a duplicated clock cycle both I and Q signals are 1:2 over-sampled in course of being interlaced by multiplexing to one 2-bit signal that is transferred to register 349 from where it is output as I_{DL} signal towards PDAC 234.

30 Quadrature modulation by 2:1 multiplexing and cyclic negation according to Fig. 9 can be realized as pipelined logic using exclusively low cost CMOS technology even in high speed applications being clocked at several GHz.

-25-

A generic digital quadrature de-modulator 3600 followed by two low-pass decimators 356 and 357 is depicted in Fig. 10. The incoming receiver signal R_S is multiplied by two components I_0 and Q_0 of the conjugated complex carrier signal by multipliers 3660 and 3670, respectively, where I_0 denotes the in-phase component and Q_0 denotes the quadrature component. Each output signal I_{DM} and Q_{DM} of quadrature de-modulator 3600 passes a low-pass decimator 356 and 357 comprising a low-pass filter followed by a sub-sampler to achieve two components I_{BB} and Q_{BB} of the complex base-band signal at the outputs of the low-pass decimators 356 and 357.

10

A preferred choice of the sampling frequency being four times the carrier frequency is demonstrated by the signal diagrams shown in Fig. 11. In this particular case the samples of signal R_S illustrated as example in Fig 11b are alternately passed to the de-modulator outputs I_{DM} and Q_{DM} illustrated as examples in Fig 11d and e, respectively, whilst being cyclically negated by the process of de-modulation. Therefore, the two multipliers 3660 and 3670 can be economically replaced by a simple de-multiplexer and cyclically controlled inverters, provided that the 2-bit input signal R_S is given in two's complement notation. Thus, the cyclic negation is performed by inverting the upper bit denoting the sign of the 3 level signal R_S (+1, 0, -1) but only in the non-zero case whilst the lower bit denoting a zero remains unchanged in any case.

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As a preferred embodiment of this invention, the functionality of a generic digital quadrature de-modulator 3600 according to Fig. 10 is implemented as quadrature de-modulation by de-multiplexing and cyclic negation within block 360 followed by low-pass decimators 356 and 357 of the DDC 350 of DTRX 300 of Fig. 5. Block 360 can be realized as simple pipelined logic using exclusively low cost CMOS technology even in high speed applications being clocked at several GHz.

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Furthermore, the low-pass decimators 356 and 357 can be operated at half the sampling frequency of the sampled receiver signal R_S because every second sample of both decimator input signals I_{DM} and Q_{DM} has alternately a zero value.

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-26-

Fig. 12 shows a block diagram of a systolic FIR decimator utilized for digital down conversion. The example shown is adapted for digital decimation of a 1.5 bit signal. The systolic FIR decimator comprises a FIR filter having $N \times M$ coefficients combined with $N:1$ sub-sampling and can be applied as sub-sampling unit 356 and 357, respectively,
5 within the DDC 350 of Fig 5.

A decimation process performing FIR filtering plus sub-sampling is realized using a number of M systolic DDC blocks 3701, 3702 up to 3706. A plurality of the M DDC blocks 3701, 3702 up to 3706 may be arranged and work in parallel. Each one of the M
10 DDC blocks 3701, 3702 up to 3706 performs a convolution of the bi-serial input signal by a subset of N filter coefficients plus sub-sampling. Thus, all of the M DDC blocks 3701, 3702 up to 3706 work simultaneously in consecutive windows of length N to jointly carry out the convolution.

15 The 1.5 bit signal, a bi-serial input signal representing 3 levels (+1, 0, -1), is applied to the DDC blocks 3701, 3702 up to 3706 at inputs 3721, 3722 up to 3726 as a parallel set of a zero-bit signal and a sign-bit signal.

Each one of the consecutive windows comprises N filter coefficients of word length L and
20 N samples of the input signal being aligned in time by the shift registers 3712 up to 3716 being arranged between the signal inputs 3721, 3722 up to 3726 of each of the DDC blocks 3701, 3702 up to 3706.

The convolution plus sub-sampling is executed by multiplying each one of the N filter
25 coefficients by the associated one of the N samples of the input signal and accumulating the resulting products within the window of length N .

Finally, the parallel output signals of all of the M DDC blocks 3701, 3702 up to 3706 have to be added by a pipelined cascade 390 of parallel adder stages. The values for M and N
30 are arbitrary integers, however, the output word length of the DDC blocks should not exceed N .

-27-

Fig. 13 shows the systolic realisation of a DDC block 370 that can be an embodiment of DDC blocks 3701, 3702 up to 3706 of Fig. 12 for $N = 6$. The systolic DDC block 370 realizes a 6:1 decimation of a 1.5 bit signal which represents 3 levels (+1, 0, -1) being coded by 2 bits per sample utilizing two's complement arithmetic. In this context, systolic realisation denotes a 2-dimensional pipelining in the flow direction of the coefficient bits (i. e. "horizontal pipelining") as well as in the flow direction of the carry bits (i. e. "vertical pipelining"). By definition, a "systolic array" comprises only binary logic elements like AND gates, EXOR gates and multiplexers plus one-bit full adders, flip-flops and wiring as depicted in Figs. 13 and 14.

In two's complement arithmetic always utilized in every embodiment of the invention, MSB denotes the Most Significant Bit representing the sign of a value A. A is negative when the MSB is set (high state) and positive when the MSB is cleared (low state). LSB denotes the Least Significant Bit representing in a codeword of n bits the value of 2^{-n} when the LSB is set (high state).

Furthermore a Representative Notation Bit (RNB) is included following the LSB. The RNB is always set (high state) representing the constant value of $2^{-(n+1)}$. This representative level notation achieved by introducing the RNB is used for enabling a systolic realization of the DDC block 370 because it inhibits the so called "carry ripple through effect". As known in the art, this effect normally occurs when in two's complement arithmetic a codeword is negated. When representative level notation by introducing a RNB is provided a given codeword for A can simply be negated by inverting all the bits from MSB to LSB whilst the RNB remains unchanged.

As depicted in Fig. 13, the systolic DDC Block 370 comprises a convolution plus sub-sampling unit composed of a plurality of L bit-slices 381, 382, 383 up to 386 followed by an output storage register 380 having a parallel output. Usually, $L < N$ bit-slices are arranged in parallel but the invention is not limited to the number of $L < N$ bit-slices. All flip-flops FF shown in Fig. 13 and the output storage register 380 are clocked at the sampling rate of the bi-serial input signal 3720 representing 3 levels (+1, 0, -1).

-28-

The bit-slices 381, 382, 383 up to 386 jointly perform the convolution plus sub-sampling process by multiplying the bi-serial input signal 3720 sample wise by FIR filter coefficients of word length L (including the RNB) and accumulating the resulting products over N sampling clock pulses. The FIR filter coefficients for each of the bit-slices 382, 383
5 up to 386 are loaded bit wise into shift registers with feed-back termed 'FIR coefficients revolver' where the coefficient bits are rotated. Within the RNB-slice 381, however, the FIR coefficients revolver and a following EXOR gate are replaced by a static high signal 3812 because the RNB is always set as stated above.

10 The convolution plus sub-sampling process is running simultaneously in all of the bit-slices 381, 382, 383 up to 386 but mutually delayed due to a vertical pipelining caused by flip-flops FF in the direction from RNB via LSB to MSB. Therefore, the first part of the convolution result per sub-sampling cycle is obtained in the RNB-slice 381 whilst the last part of the convolution result per sub-sampling cycle is obtained L-1 clock pulses later in
15 the MSB-slice 386. Thus, the result of a convolution plus sub-sampling cycle per bit-slice is intermediately stored in a sample & hold flip-flop equipped with feed-back via a multiplexer. This enables a permanently running convolution plus sub-sampling process within anyone of the bit-slices 381, 382, 383 up to 386 without the need to wait until the next bit-slices have finished.

20 As depicted in Fig. 13 for N=6, a convolution plus sub-sampling cycle is executed per bit-slice after N clock pulses when the sub-sampling pulse 3781 goes low. Finally, all of the intermediately per bit-slice stored results of a total convolution plus sub-sampling cycle calculated with delay by all of the bit-slices 381, 382, 383 up to 386 are taken over in
25 parallel by the output storage register 380 after the MSB-slice 386 has finished its cycle of the convolution and sub-sampling process.

All of the bit-slices 381, 382, 383 up to 386 have the same elements to carry out their respective part of the convolution and sub-sampling process. Within the RNB-slice 381,
30 however, the FIR coefficients revolver and the following EXOR gate are replaced by a static high signal 3812 because the RNB is always set as stated above.

-29-

Fig. 14 shows an example of one bit-slice 382,383 up to 386 of the convolution plus sub-sampling unit within the systolic DDC block 370 in greater detail. As depicted for one bit level and $N=6$, a bit-slice of the convolution plus sub-sampling unit comprises 4 consecutive functional sub-units. A shift register equipped with feed-back termed 'FIR coefficients revolver' 3730 is loaded with bits of N coefficients being rotated within the FIR coefficients revolver 3730.

The bits of N coefficients are consecutively multiplied in the 1×1.5 bit multiplier unit 3740 by the samples of the bi-serial input signal 3720 representing 3 levels (+1, 0, -1) wherein the 'sign-bit' is set (high state) in case of negative input samples whilst the 'zero-bit' is set for non-zero input samples. The multiplication is simply executed by passing, inhibiting or inverting the coefficient bits using an EXOR gate 3742 and an AND gate 3744. The FIR filter coefficients usually are given in two's complement representative level notation including the RNB (as discussed above). Thus, inverting all of the bits of a given FIR filter coefficient from LSB to MSB performs the negation of the respective coefficient.

The results of these consecutive 1×1.5 bit multiplications are accumulated in a synchronously cleared accumulator 3760 until the sub-sampling pulse 3781 goes low. As depicted in Fig. 4a, the sub-sampling pulse 3781 is generated within the receive clock oscillator unit 237 utilizing a synchronous counter which derives the pulse 3781 from the receive clock signal, a method well known in the art.

The sub-sampling pulse 3781 is only in 1 out of N (in the example illustrated here: $N=6$) consecutive sampling intervals at low state causing at the rising edge of the next clock pulse the take-over of the content of the accumulator 3760 by the following sub-sample & hold stage 3780 whilst the accumulator 3760 is synchronously cleared and the next cycle of the convolution plus sub-sampling process is started immediately. In this arrangement, no extra clearing or read-out cycle is necessary, thus keeping the convolution plus sub-sampling and read-out process straight forward and strictly synchronous.

-30-

It should be noted that the RNB of the coefficients being always set is also included in the convolution plus sub-sampling process. This is done by a special RNB-slice 381 wherein the coefficients revolver and the following EXOR gate are replaced by a static high signal 3812.

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-31-

Claims

1. Antenna system connectable to a base station, the antenna system comprising a digital radio unit (200) connectable to at least one antenna element (220), wherein
5 the digital radio unit (200) comprises:
 - at least one digital micro radio (230) for receiving/sending digital radio signals having a digital down-converter (350) / a digital up-converter (310) and a digital signal converter (234; 235); whereby the at least one micro radio (230) converts the digital radio signals to analogue RF (radio frequency) signals and vice versa;
 - 10 - at least one hub (240) for processing digital radio signals and control signals and for routing said digital radio signals and control signals via at least one digital link (260) and at least one interface (258, 259), the at least one digital link (260) being provided between the at least one hub (240) and the at least one micro radio (230).
- 15 2. Antenna system according to claim 1, wherein the at least one micro radio (230) is operable in FDD mode and comprises:
 - a FDD filter unit (232) connected at a receive output to an input of a low noise analogue-to-digital converter (ADC) (235) and further connected at a transmit input to an output of a power digital-to-analogue converter (PDAC) (234);
 - 20 - a digital transceiver (DTRX) (300) connected at an output for signal (I_{DL}) to an input of the PDAC (234) and further connected at an input for signal (R_S) to an output of the ADC (235), the digital transceiver DTRX having a receive section and a transmit section, the digital up-converter (310) being part of the transmit section and the digital down-converter (350) being part of the receive section;
 - 25 - a receive clock oscillator unit (RCLK) (237) for providing a sampling clock for the ADC (235) and for the receive section of the digital transceiver (300) and for further providing a sub-sampling pulse (3781) for said receive section;
 - a transmit clock oscillator unit (TCLK) (236) for providing a sampling clock for the PDAC (234) and for the transmit section of the DTRX (300).
- 30 3. Antenna system according to claim 1, wherein the at least one micro radio (230) is operable in TDD mode and comprises:

-32-

- a TDD filter unit (233) followed by a TDD switch (239) connected at a receive output to an input of a analogue-to-digital converter (ADC) (235) and further connected at a transmit input to an output of a power digital-to-analogue converter (PDAC) (234);
 - 5 - a digital transceiver (DTRX) (300) connected at an output for signal (I_{DL}) to an input of the PDAC (234) and further connected at an input for signal (R_S) to an output of the ADC (235), the DTRX having a receive section and a transmit section, the digital up-converter (310) being part of the transmit section and the digital down-converter (350) being part of the receive section;
 - 10 - at least one clock oscillator unit (TRCLK) (2367) for providing a sampling clock for the ADC (235), the PDAC (234), and the DTRX (300) and for further providing a sub-sampling pulse (3781) for the receive section of the DTRX (300) and a time control signal (238) for the TDD switch (239).
- 15 4. Antenna system according to claim 2 or 3, wherein the analogue-to-digital converter (ADC) (235) comprises a low noise amplifier followed by a continuous-time sigma-delta band-pass modulator converting the RF signal at the input directly into a digital single/1.5 bit band-pass output signal (R_S).
- 20 5. Antenna system according to any of the claims 2 to 4, wherein the power digital-to-analog converter (PDAC) (234) utilizes 2 or 3 voltage levels to convert a digital single/1.5 bit band-pass input signal (I_{DL}) directly into an analogue RF output signal.
- 25 6. Antenna system according to any of the claims claim 1 to 5, wherein the DUC (310) utilizes a unit (340) performing quadrature modulation by 2:1 multiplexing and cyclic negation in combination with a time-discrete sigma-delta band-pass modulator (318) or two time-discrete sigma-delta low-pass modulators (316, 317) to output a digital single/1.5bit band-pass signal (I_{DL}) being directly up-converted
- 30 from a digital base-band signal; and wherein the DDC (350) utilizes a unit (360) performing quadrature demodulation by 1:2 de-multiplexing and cyclic negation

-33-

followed by two systolic FIR decimators (356, 357) to down-convert the digital single/1.5bit band-pass input signal (R_S) directly into a digital base-band signal.

- 5 7. Antenna system according to claim 6 wherein the time-discrete sigma-delta band-pass modulator (318) is realized as a systolic array.
8. Antenna system according to claim 6 wherein the two time-discrete sigma-delta low-pass modulators (316, 317) are realized as systolic arrays.
- 10 9. Antenna system according to any of claims 1 to 8, wherein digital base-band signals are processed by the at least one hub (240) within time and frequency domain.
- 15 10. Antenna system according to any of claims 1 to 9, wherein at least one micro controller (245) and at least one control bus (247) are embedded in the at least one hub (240); whereby processing and routing of digital base-band signals and control signals by the at least one hub (240) is controlled and monitored by said micro controller (245).
- 20 11. Antenna system according to any of claims 1 to 10, wherein the at least one hub (240) comprises at least one Frequency Multiplexer & De-Multiplexer (FMDX) unit (243) comprising:
 - 25 - at least one digital quadrature modulator for combining a plurality of digital base-band signals to a digital multi-carrier signal;
 - at least one digital quadrature demodulator for splitting a digital multi-carrier signal into a plurality of digital base-band signals.
- 30 12. Antenna system according to any of claims 1 to 11, wherein the at least one hub (240) comprises at least one Sampling Rate Converter (SRC) unit (242) for synchronizing the sampling frequency of digital multi-carrier signals within the at least one FMDX (243) with the sampling frequencies of digital band-pass signals

-34-

(R_S) and (I_{DL}) within the at least one micro radio (230) utilizing a variable over-sampling ratio.

13. Antenna system according to any of claims 1 to 12, wherein the at least one hub
5 (240) comprises at least one Amplitude & Phase Aligner (APA) unit (241) comprising at least one complex digital multiplier stage for adjusting amplitude and phase of digital band-pass signals (R_S) and (I_{DL}) within the at least one micro radio (230) under software control.
- 10 14. Antenna system according to any of claims 1 to 13, wherein the at least one hub (240) comprises at least one Time Multiplexer & De-Multiplexer (TMDX) and Hub unit (244) for handling the routing of incoming and outgoing data streams via at least one SerDes interface unit (248, 249) under software control.
- 15 15. Antenna system according to any of claims 1 to 14, wherein the at least one hub (240) comprises at least one Master Clock Oscillator (MCLK) unit (246) being synchronized to the time reference of the Digital Radio Server (208) by the at least one Master SerDes interface unit (249) for providing clock signals for all units of the at least one hub (240) and for synchronizing the clock units (236, 237, 2367) of
20 the at least one micro radio (230).
16. Antenna system according to any of claims 1 to 15, wherein the at least one serial link (260) between the at least one hub (240) and the at least one micro radio (230) is a digital bi-directionally serial link transporting digital base-band signals and
25 adjacent control information as packet data in a partially filled frame format, wherein an adjustment of frame length and format and further the number of samples per frame is software controllable.
17. Antenna system according to any of claims 2 to 16, wherein the at least one micro
30 radio (230) further comprises an additional power amplifier being inserted between an output of the PDAC and a receive input of the FDD filter unit (232) or the TDD switch (239).

-35-

18. Antenna system according to any of the claims 2 to 17 wherein the at least one micro radio (230) utilizes a sampling rate of digital band-pass signals (R_S) and (I_{DL}) being 4 times or $4/3$ times the RF carrier frequency.
- 5
19. Antenna system according to any of the claims 2 to 18 wherein the at least one micro radio (230) utilizes a multi-bit format of digital band-pass signals (R_S) and/or (I_{DL}).
- 10
20. Antenna system according to any of the claims 2 to 19 wherein at least one of the functional sub-units ADC (235), PDAC (234), TCLK (236), TRCLK (2367), RCLK (237), and DTRX (300) of the at least one micro radio (230) are monolithically integrated by micro-electronic means.
- 15
21. Antenna system according to any of the claims 2 to 19 wherein the at least one micro radio (230) is monolithically integrated by micro-electronic means or as a multi-chip module.
- 20
22. Antenna system according to any of the preceding claims wherein the digital radio unit (200) comprising the at least one micro radio (230) and the at least one hub (240) is monolithically integrated by micro-electronic means or as a multi-chip module.
- 25
23. Antenna system according to any of the preceding claims wherein the at least one micro radio (230) is proximately connected to one or two antenna elements (220).
- 30
24. Antenna system according to any of the preceding claims wherein the digital radio unit (200) comprises a plurality of micro radios (230) each being proximately connected to one or two antenna elements (220).
25. Antenna system according to claim 24 wherein the digital radio unit (200) further comprises at least one micro sniffer (250) being proximately connected to at least

-36-

one monitoring antenna (255), the micro sniffer (250) being useable for antenna calibration.

5 26. Antenna system according to any of the preceding claims wherein the digital radio unit (200) is connected to a digital radio server (208) by at least one optical fibre (206).

10 27. Antenna system according to any of the preceding claims wherein the digital radio unit (200) and the at least one antenna element (220) are integrated on a single circuit board.

 28. Antenna system according to any of the preceding claims, whereby said processing and routing of digital radio signals and control signals performed by said hub is software controllable.

15

 29. The use of an antenna system according to any of the preceding claims within a mobile communications network.

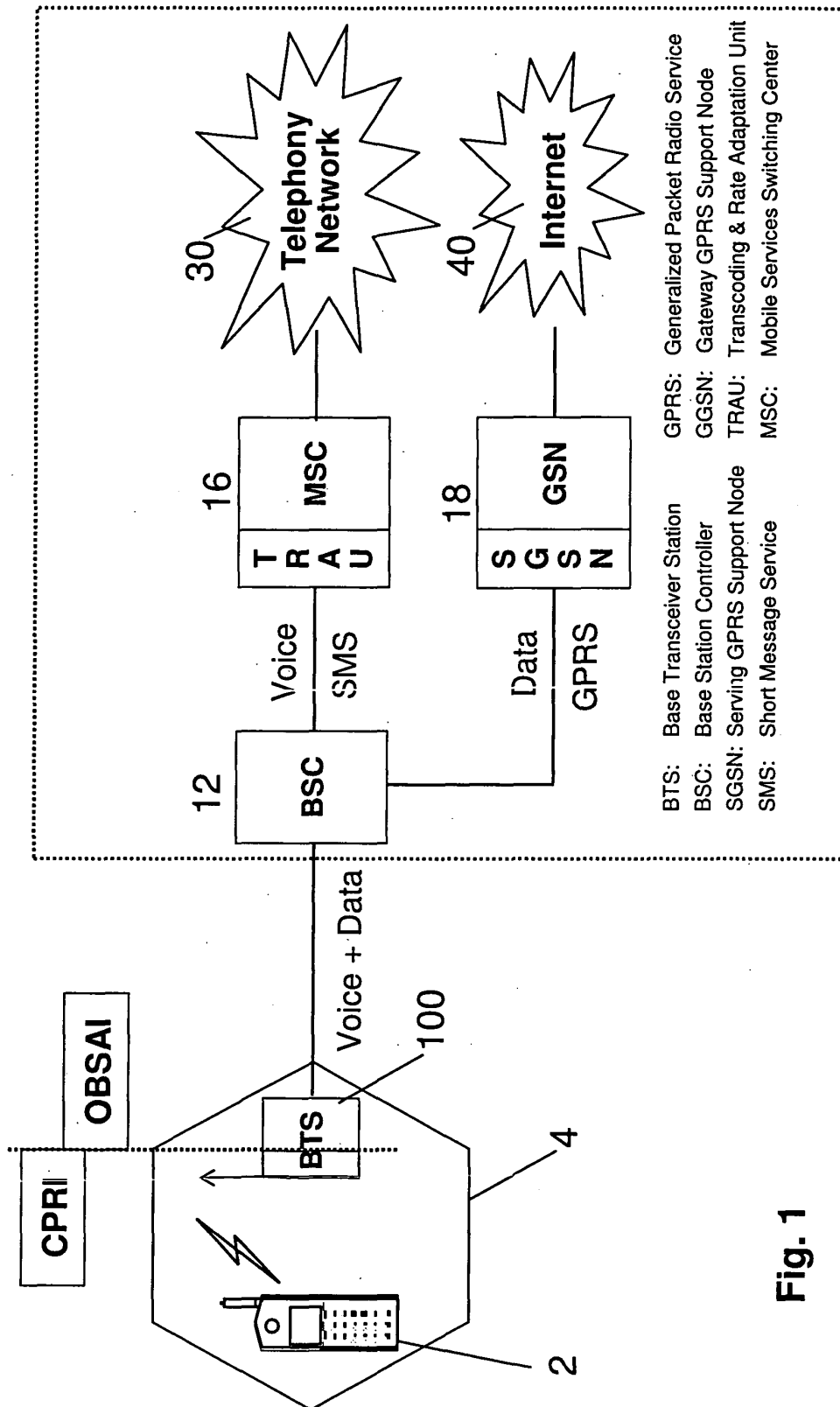


Fig. 1

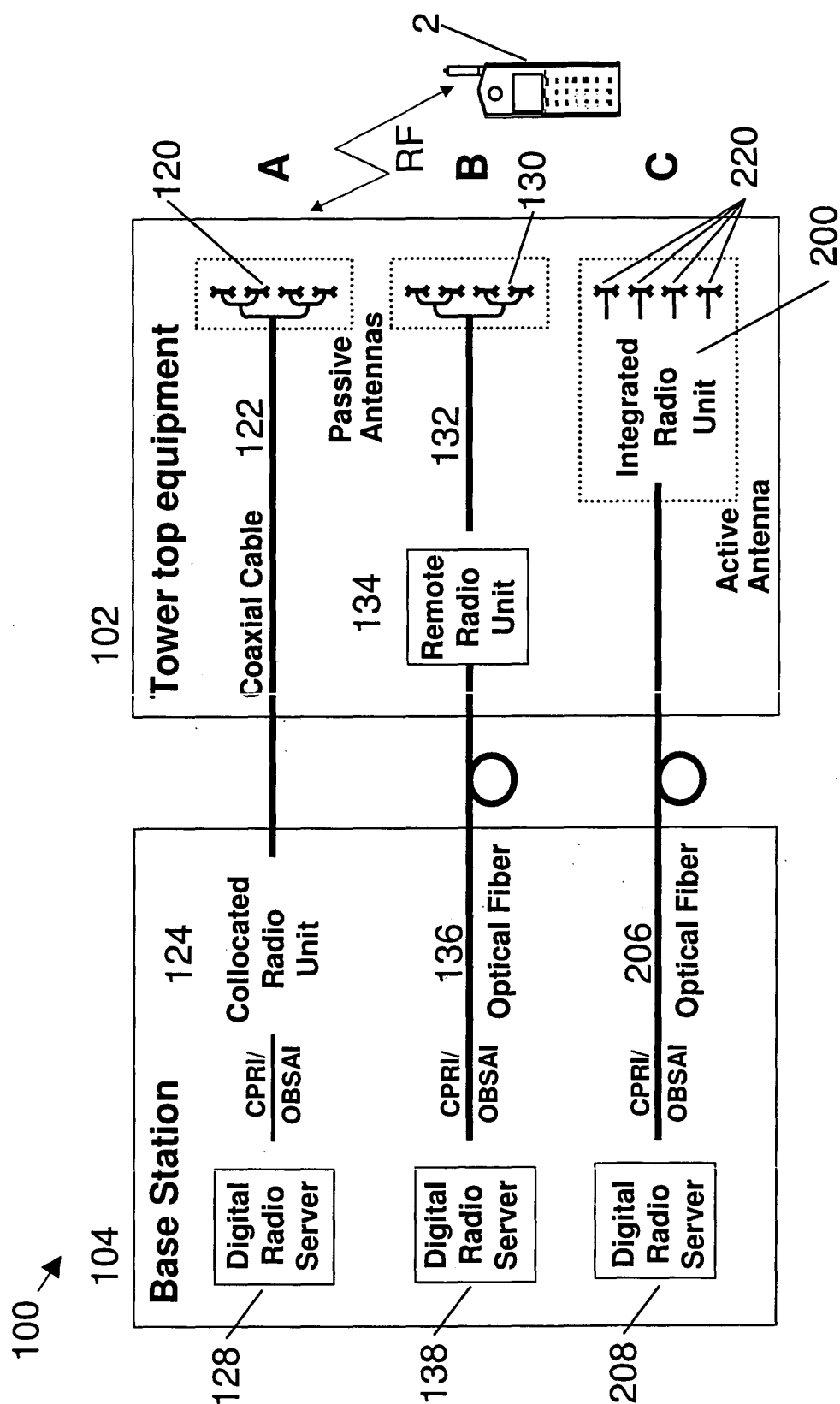


Fig. 2

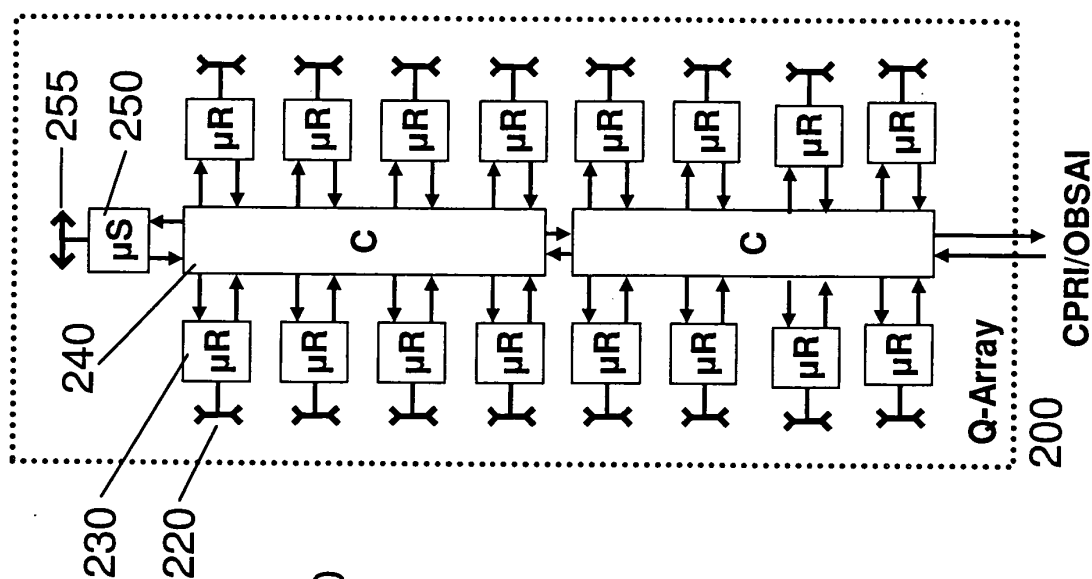


Fig. 3c

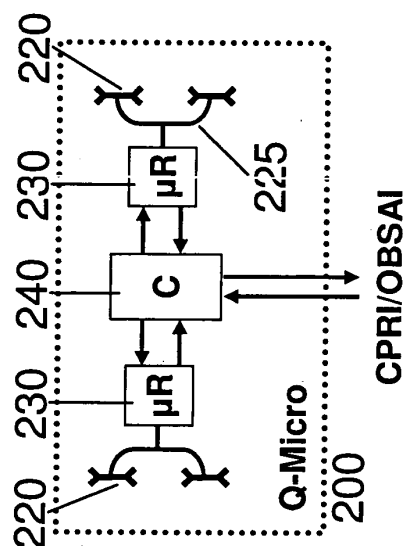


Fig. 3b

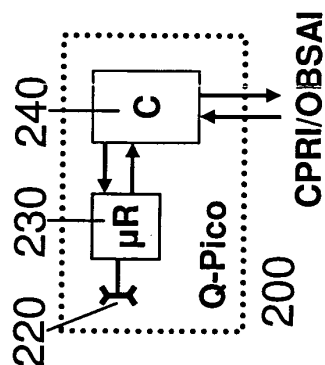


Fig. 3a

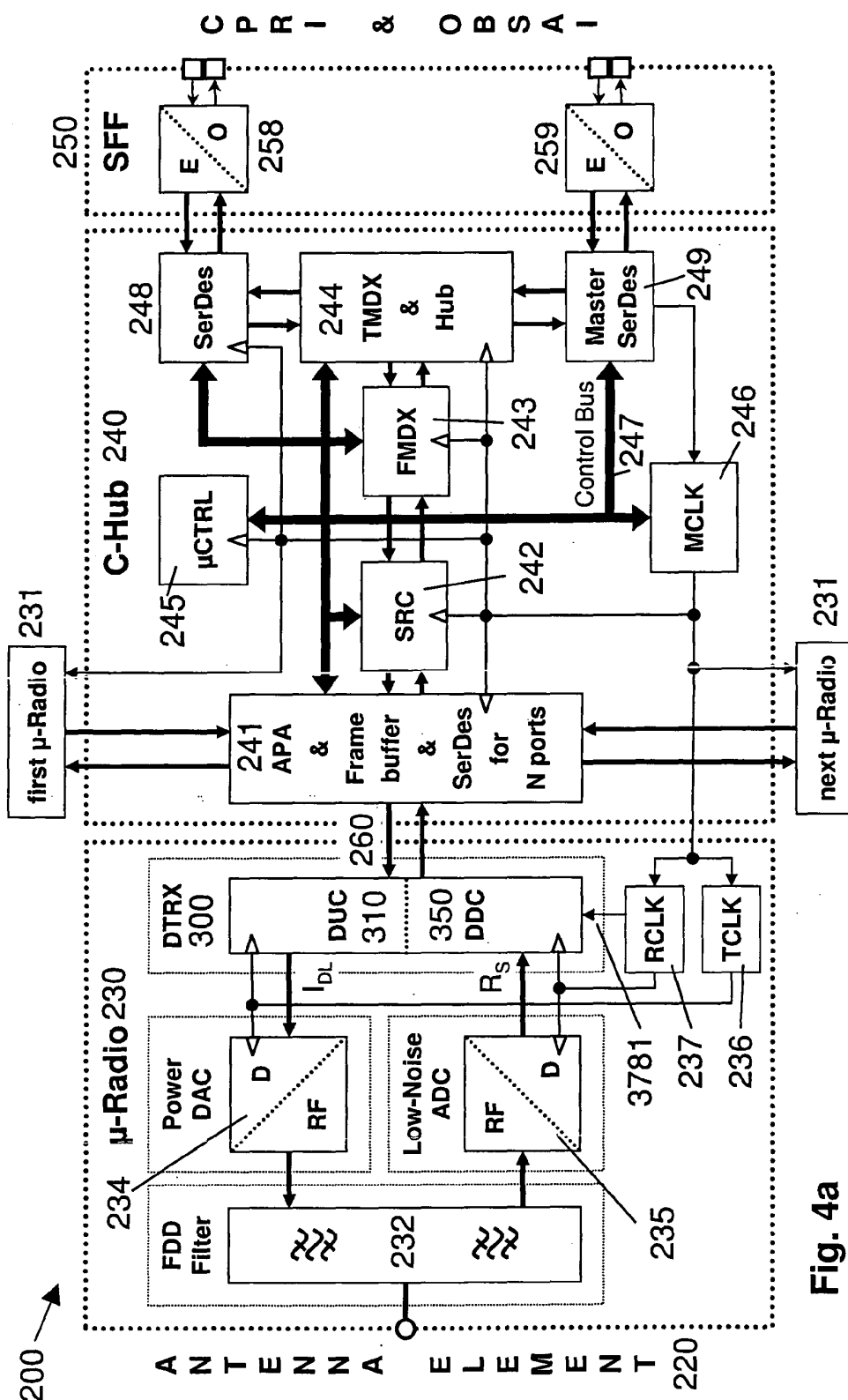


Fig. 4a

D/RF:	Digital-to-HF Converter	DTRX:	Digital Transceiver	FMDX:	Frequency Multiplexer & De-Multiplexer
RF/D:	RF-to-Digital Converter	APA:	Amplitude & Phase Aligner	TMDX:	Time Multiplexer & De-Multiplexer
DUC:	Digital Up-Converter	SerDes:	Serializer & De-serializer	SFF:	Small Form-Factor Modules
DDC:	Digital Down-Converter	SRC:	Sampling Rate Converter	E/O:	Electrical-to-Optical Converter
TCLK:	Transmit Clock Oscillator	μ -Controller:	Microcontroller	CPRI:	Common Public Radio Interface
RCLK:	Receive Clock Oscillator	MCLK:	Master Clock Oscillator	OBSAI:	Open Base-Station Architecture Interface
FDD:	Frequency Division Duplex	ADC:	Analog-to-Digital Converter	DAC:	Digital-to-Analog Converter

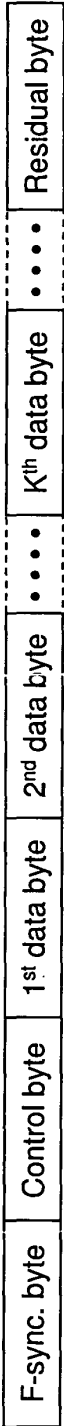


Fig. 4b

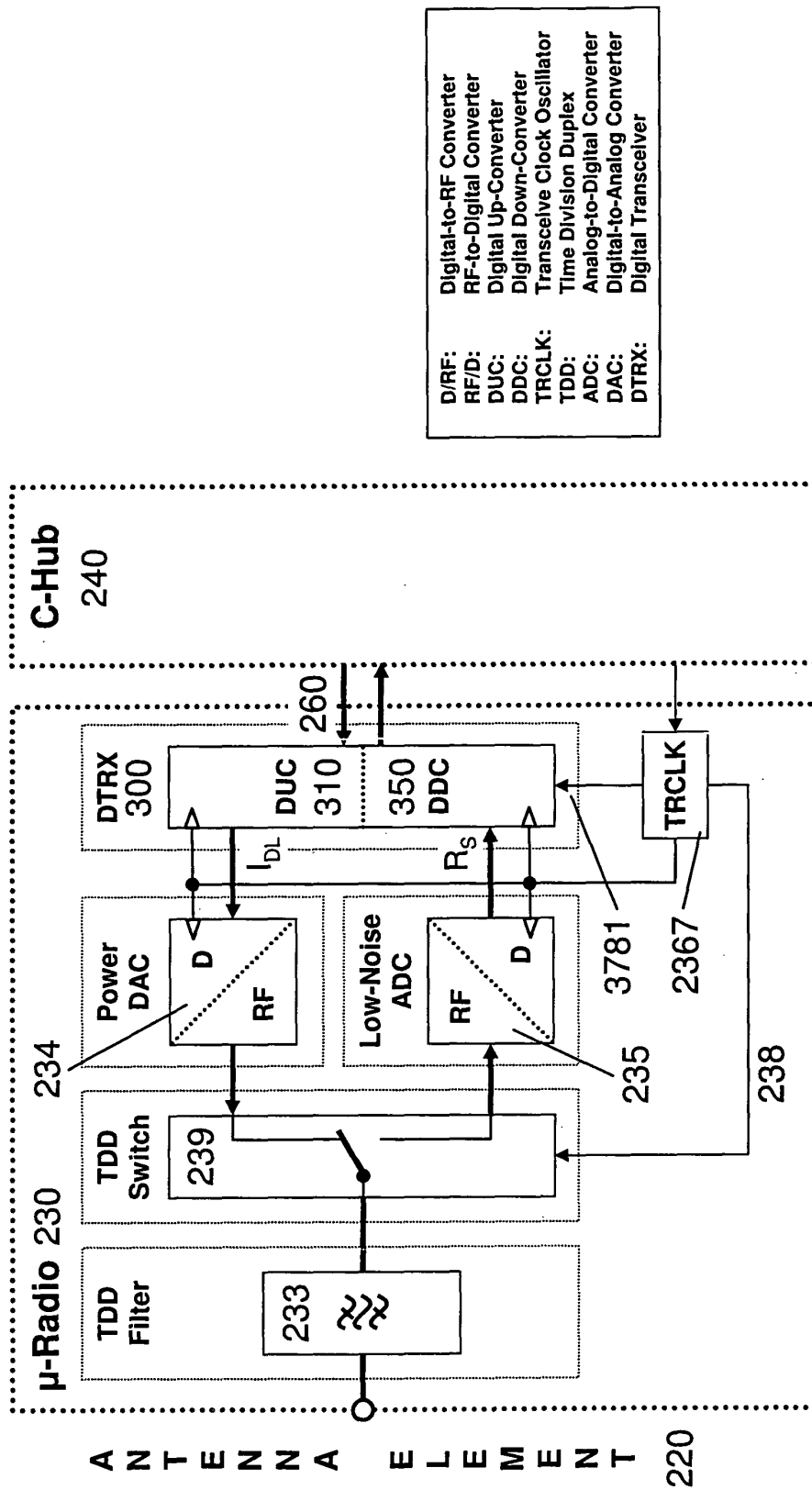


Fig. 4c

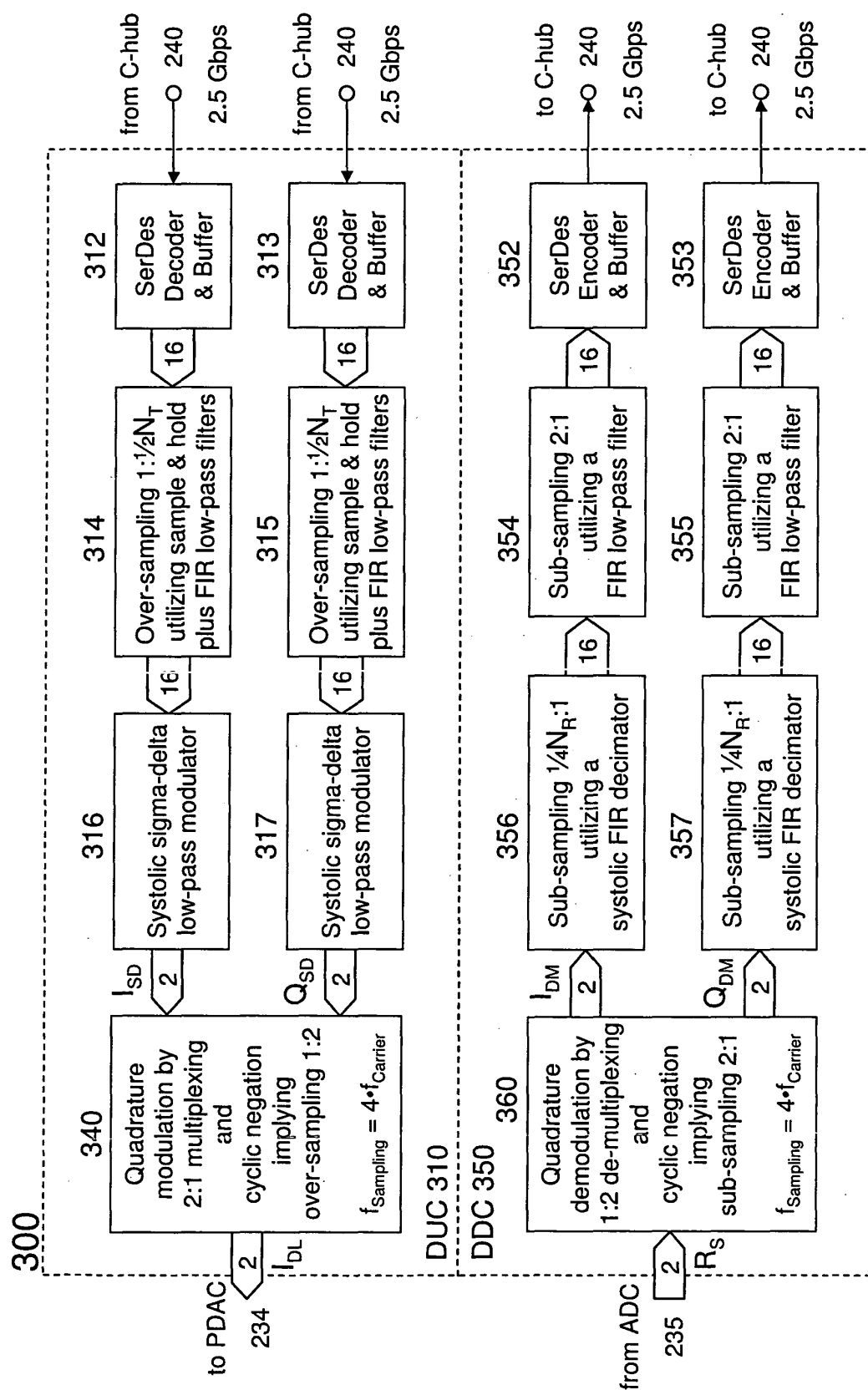


Fig. 5

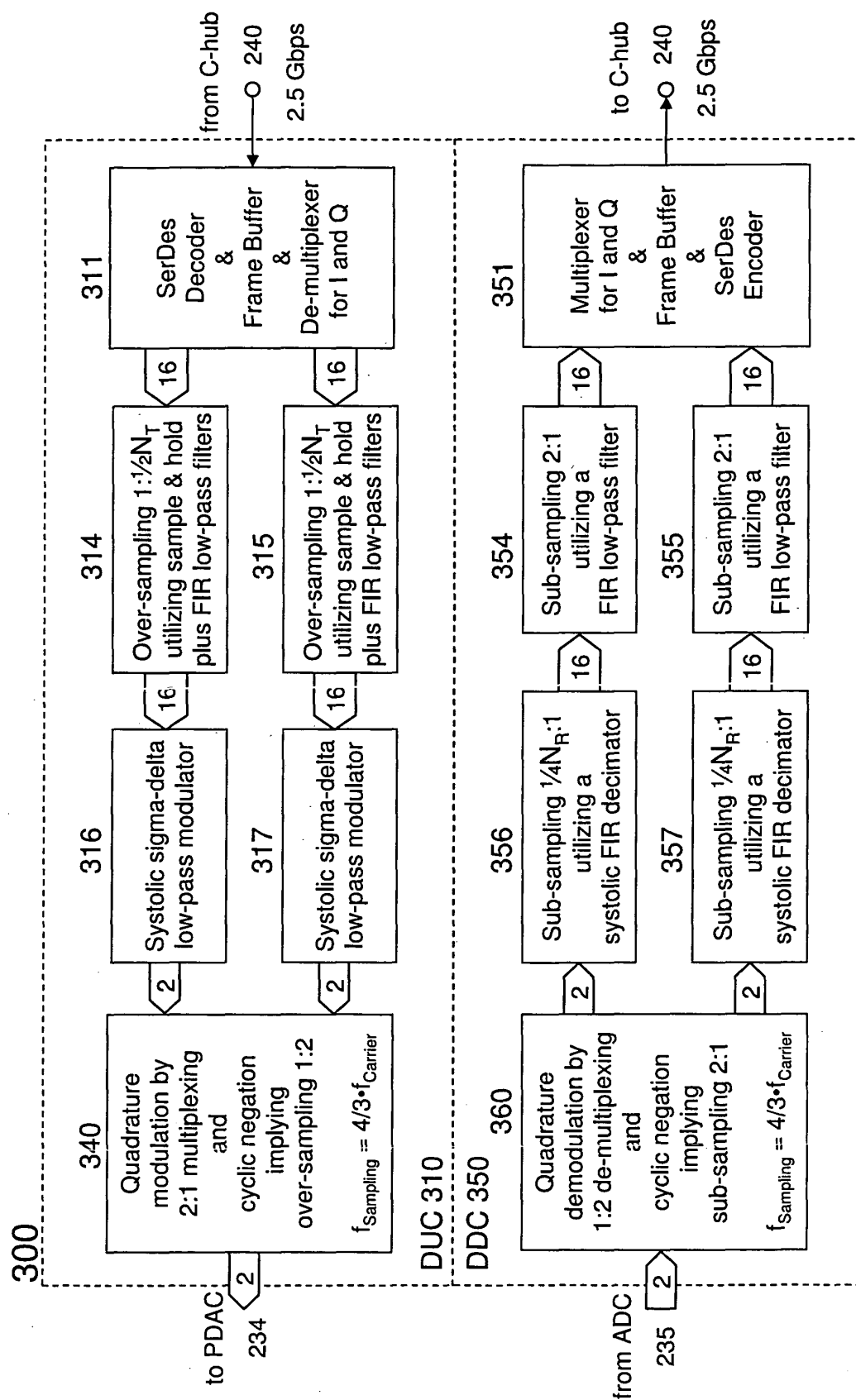


Fig. 6a

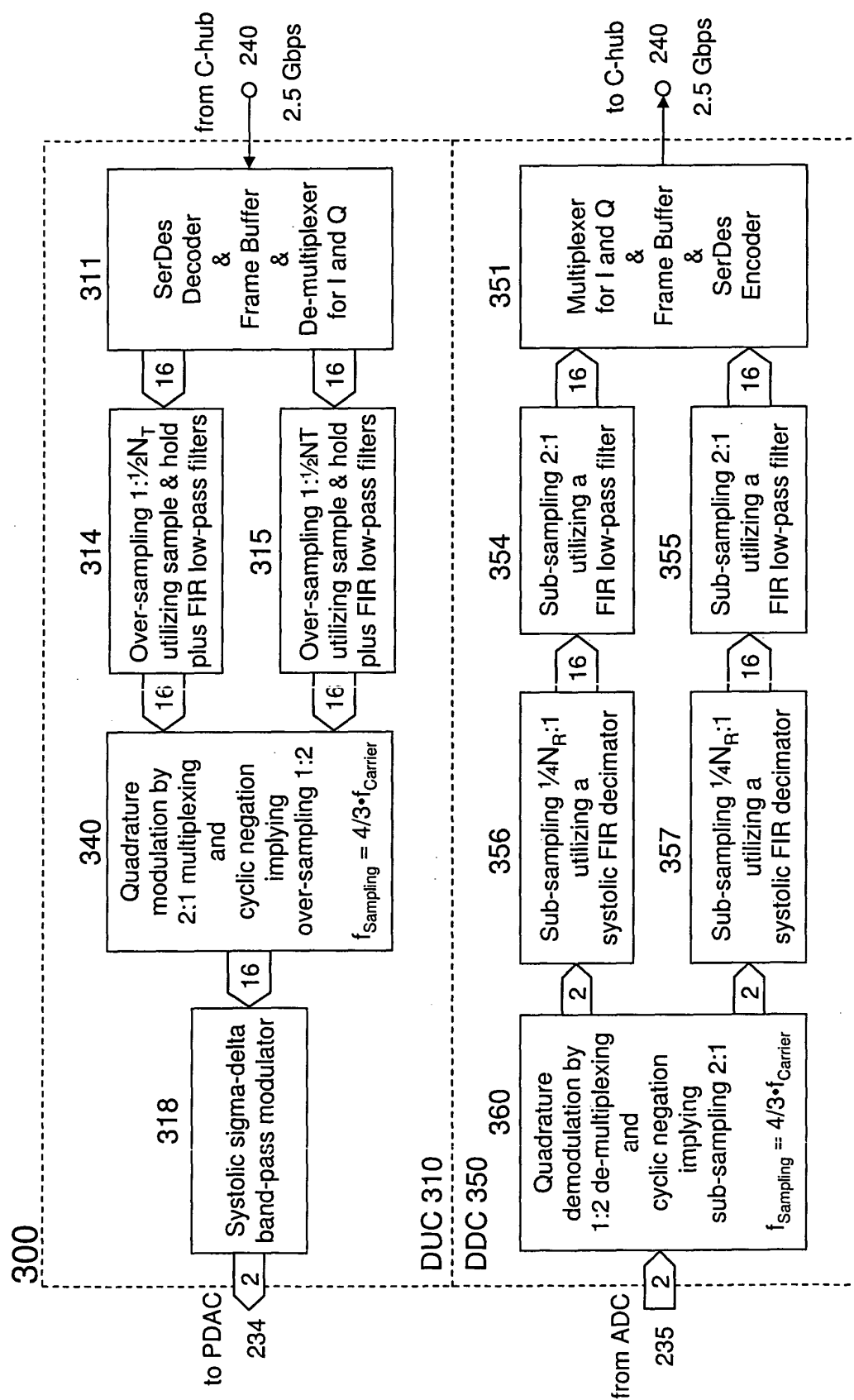


Fig. 6b

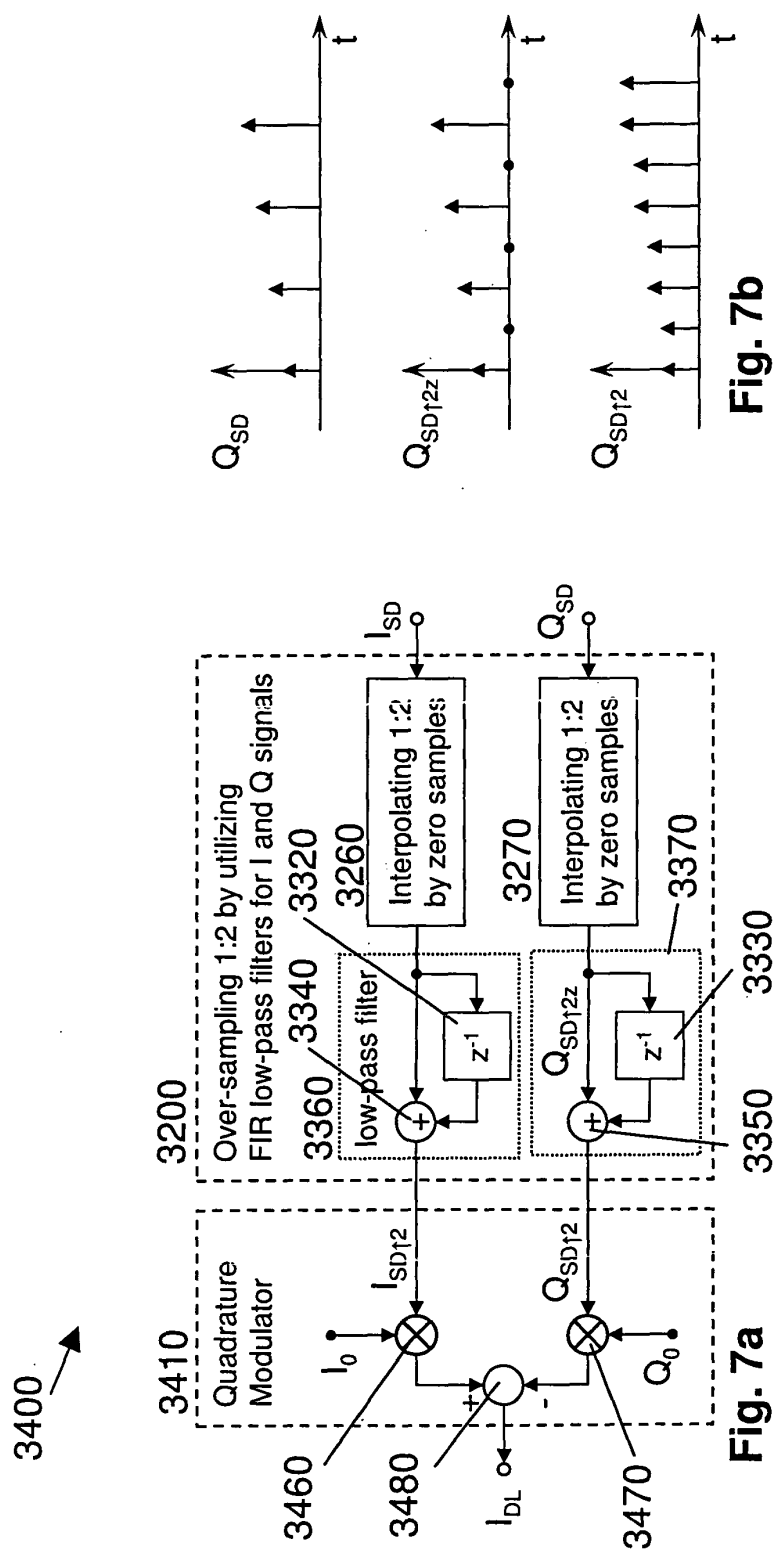


Fig. 7b

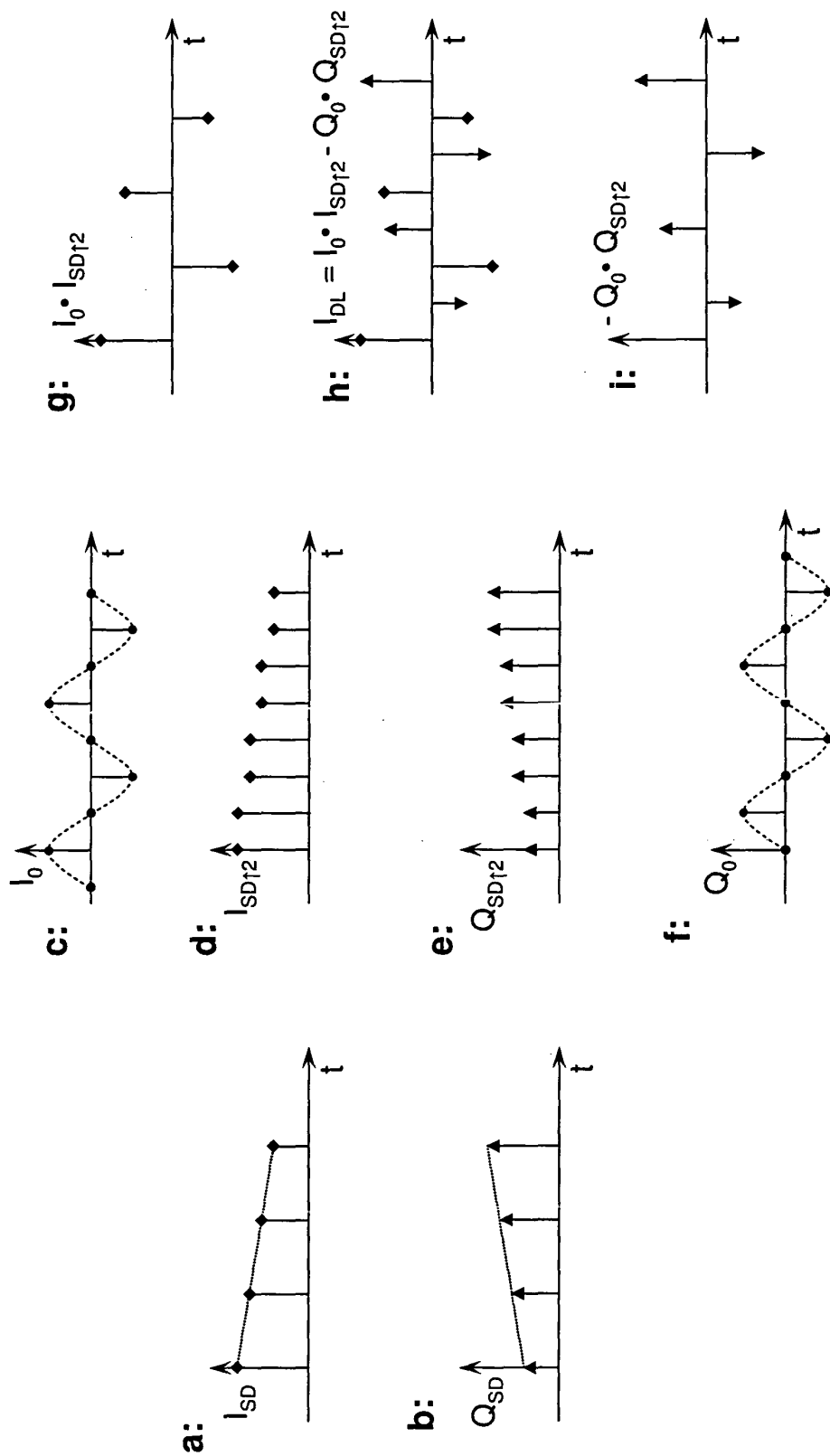


Fig. 8

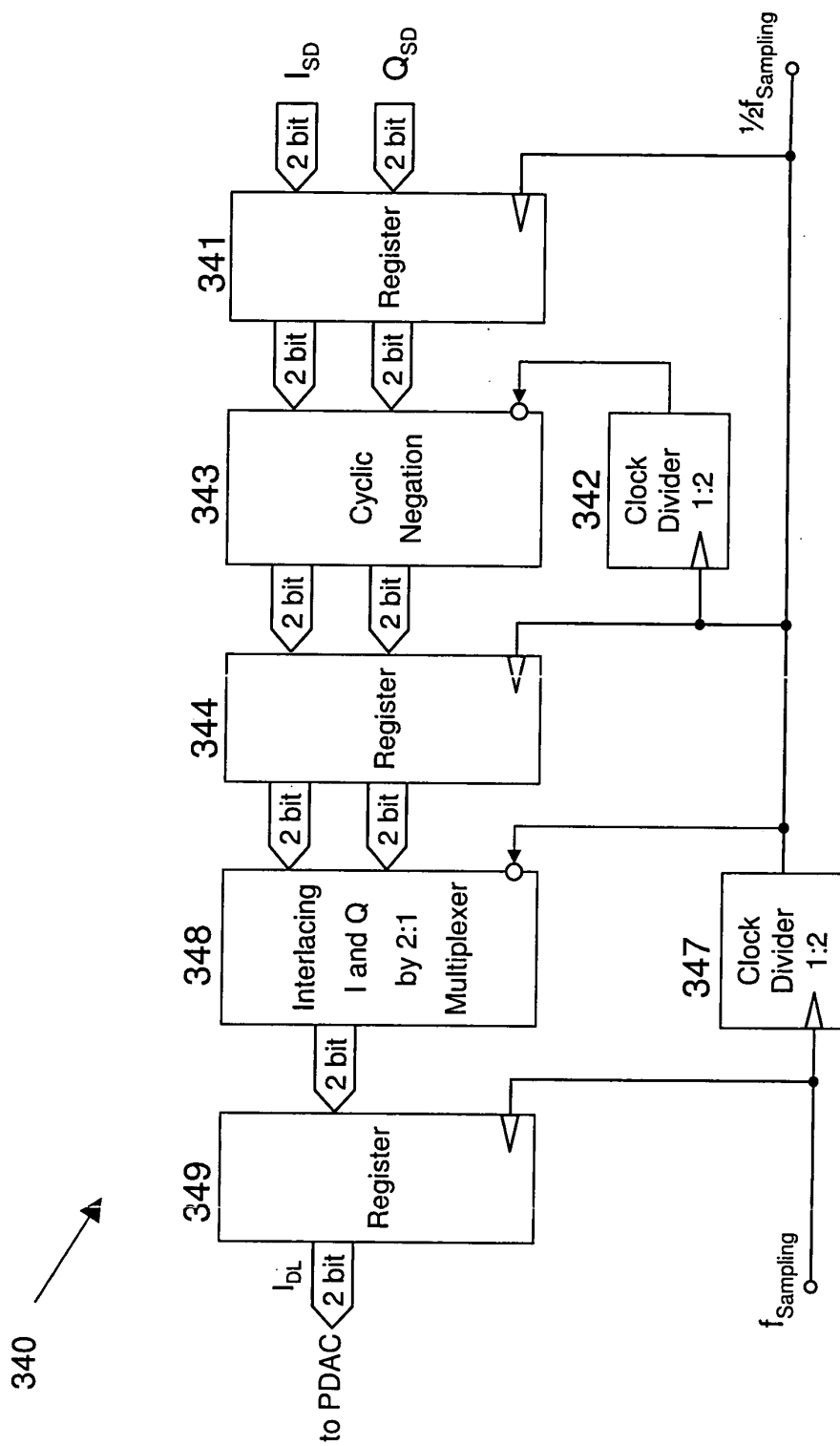


Fig. 9

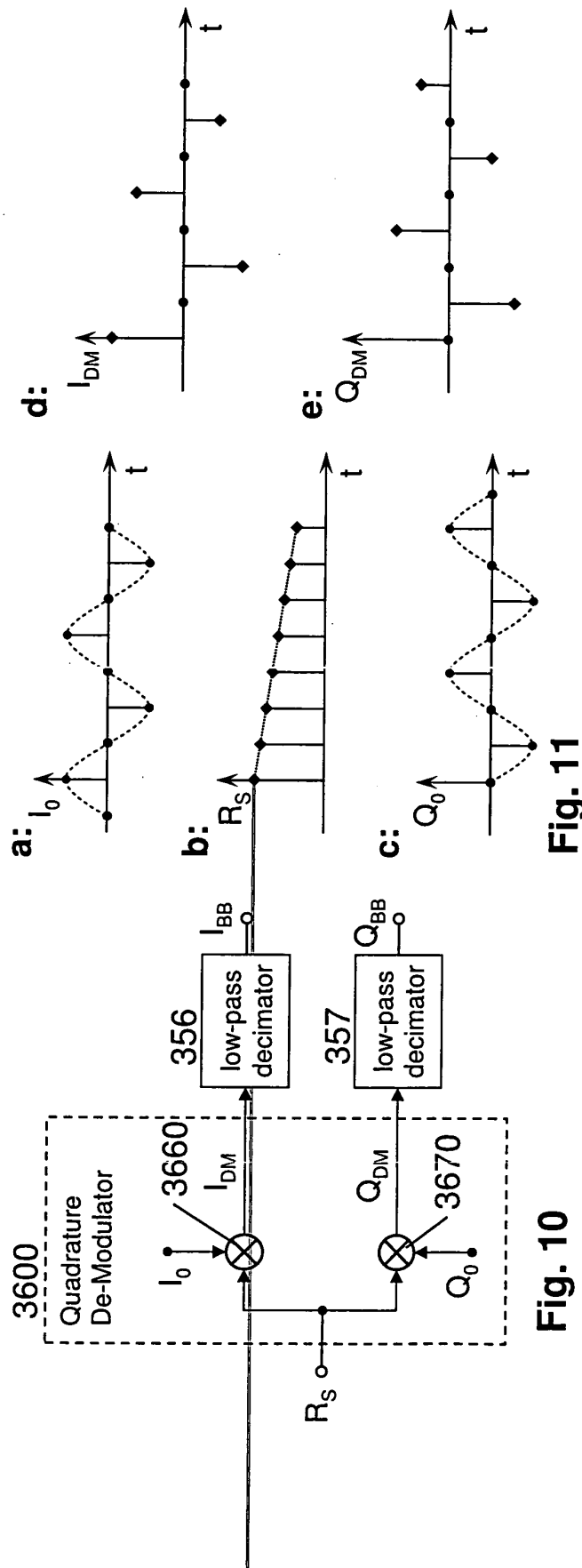


Fig. 11

Fig. 10

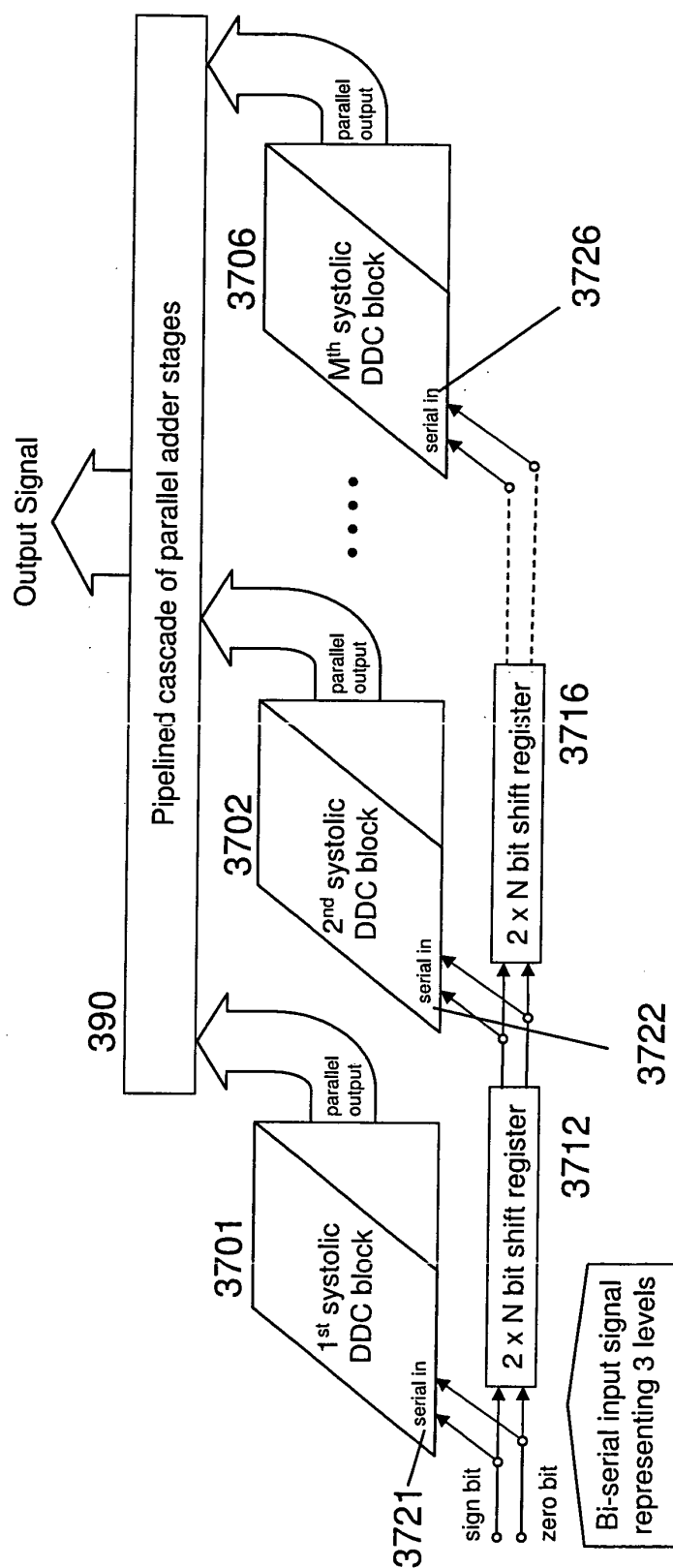


Fig. 12

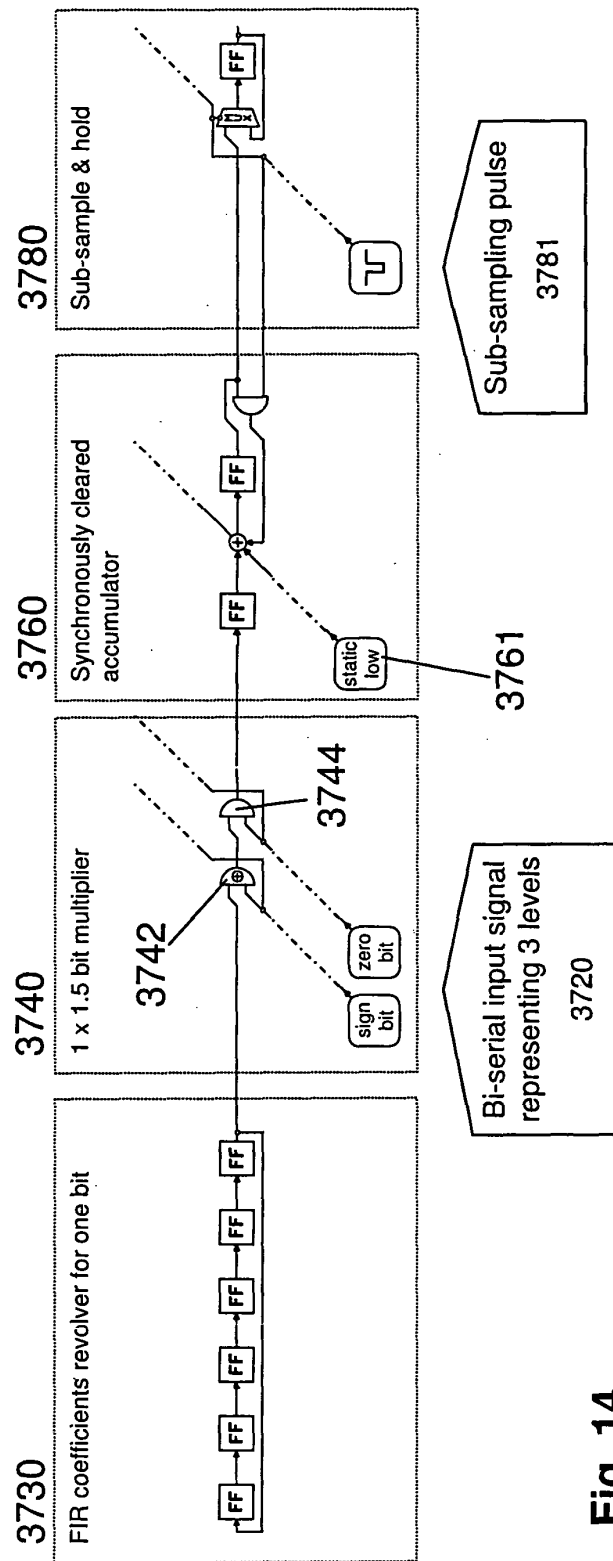


Fig. 14