

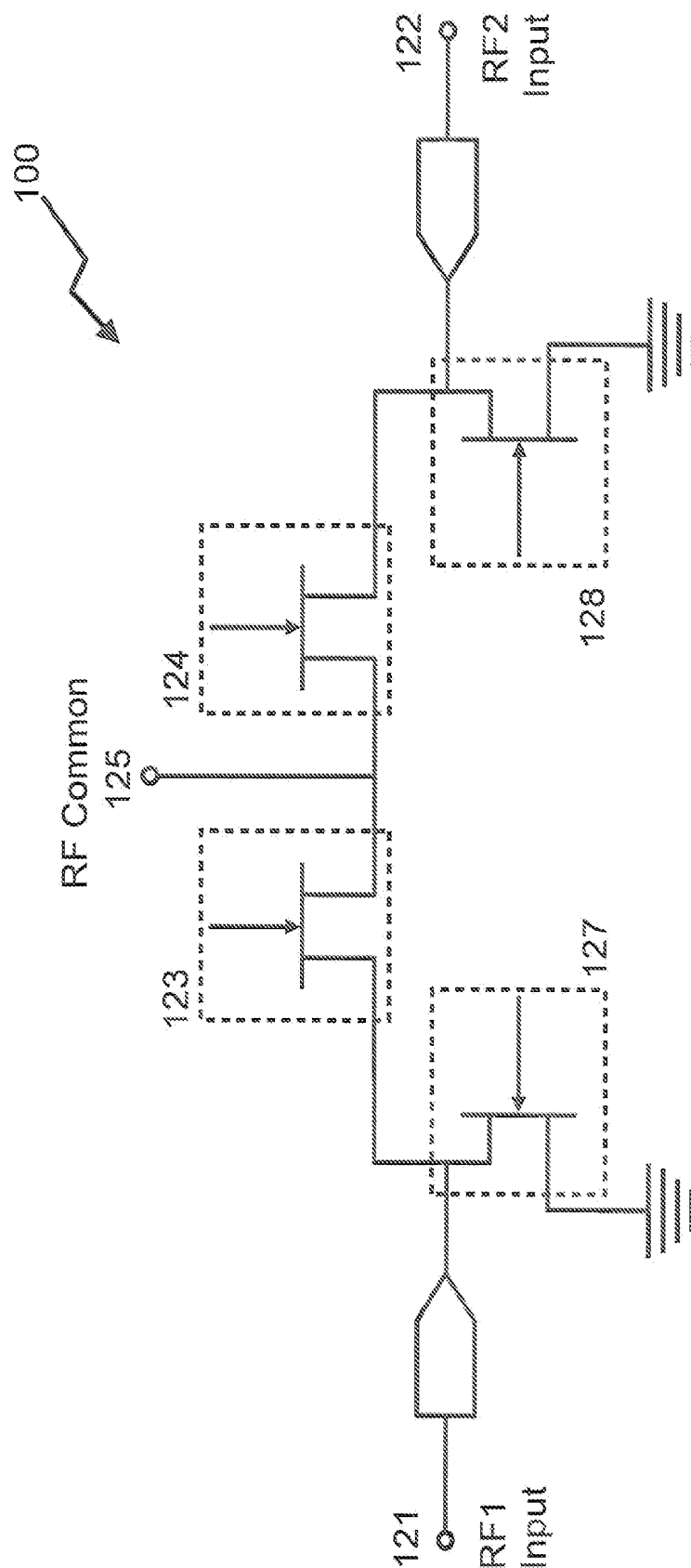


Fig. 1A Prior Art

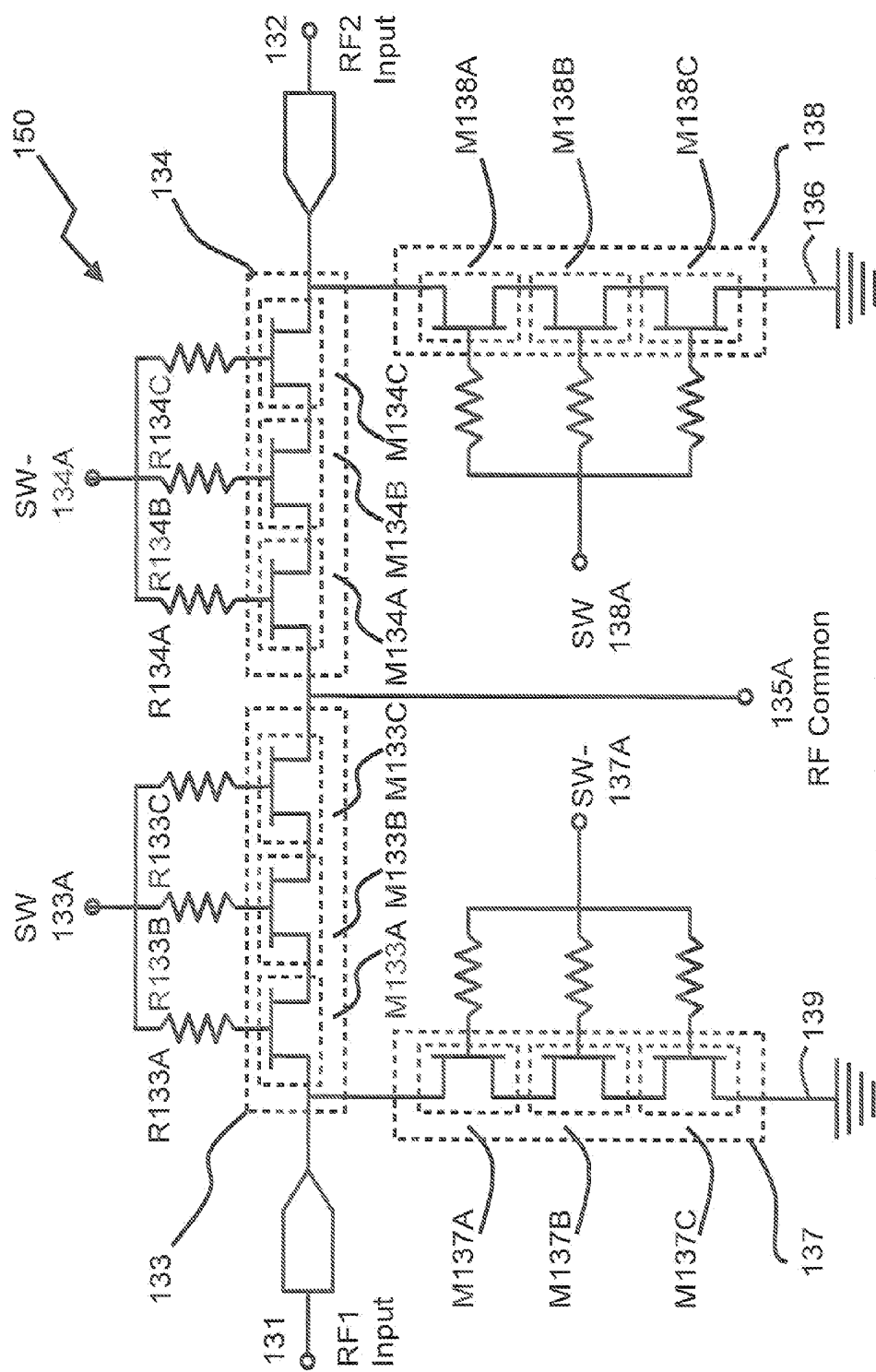


Fig. 1B Prior Art

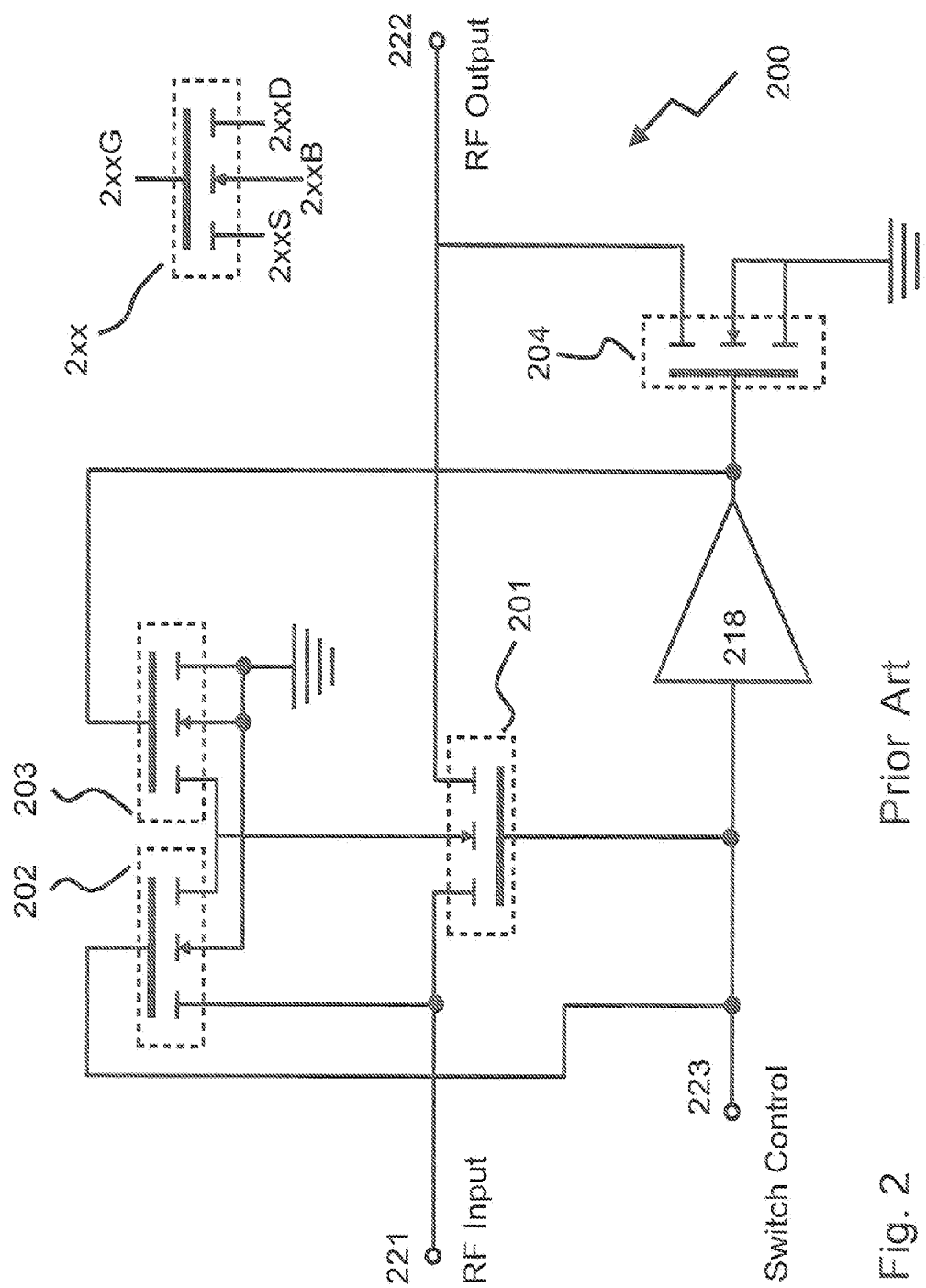
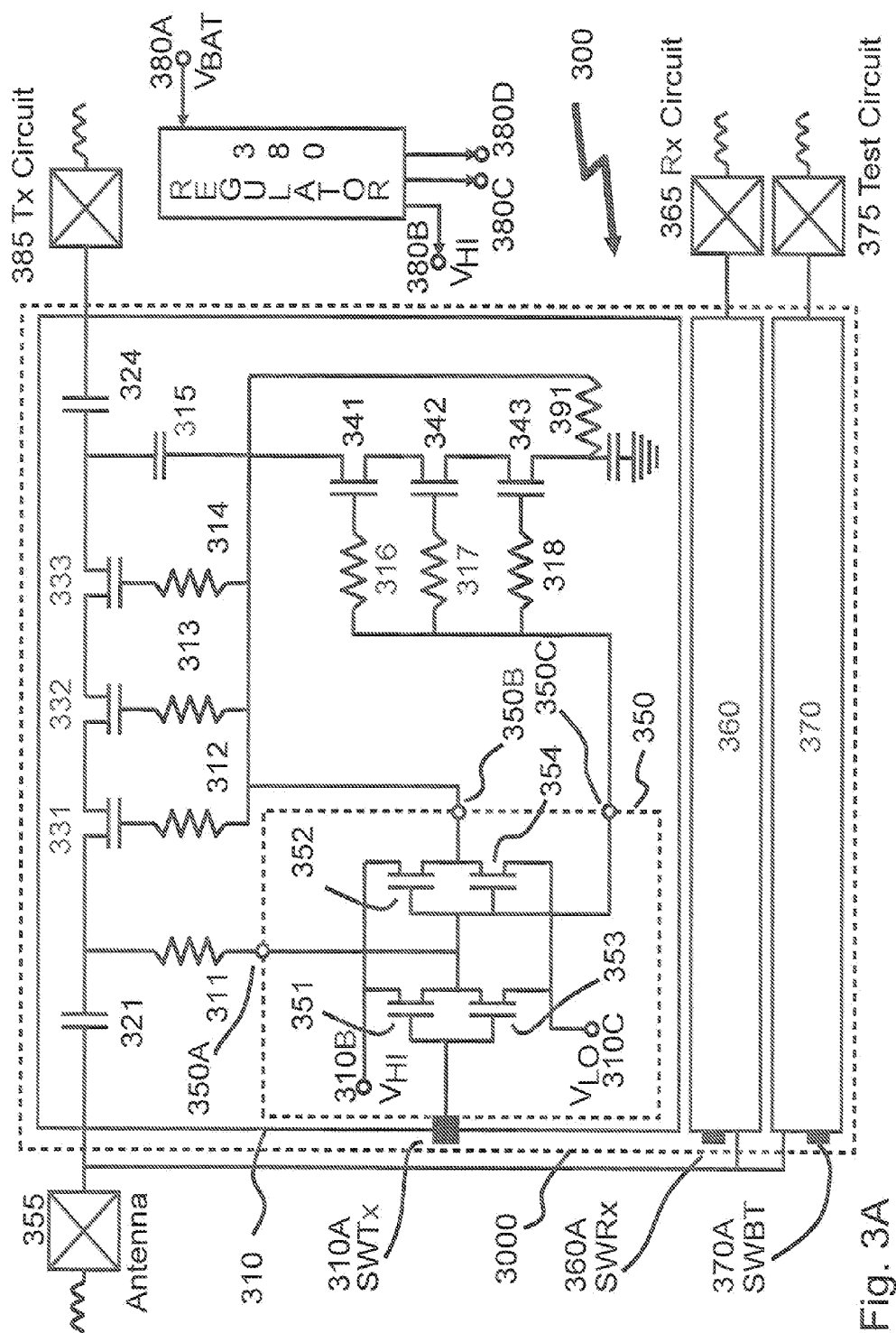


Fig. 2

Prior Art



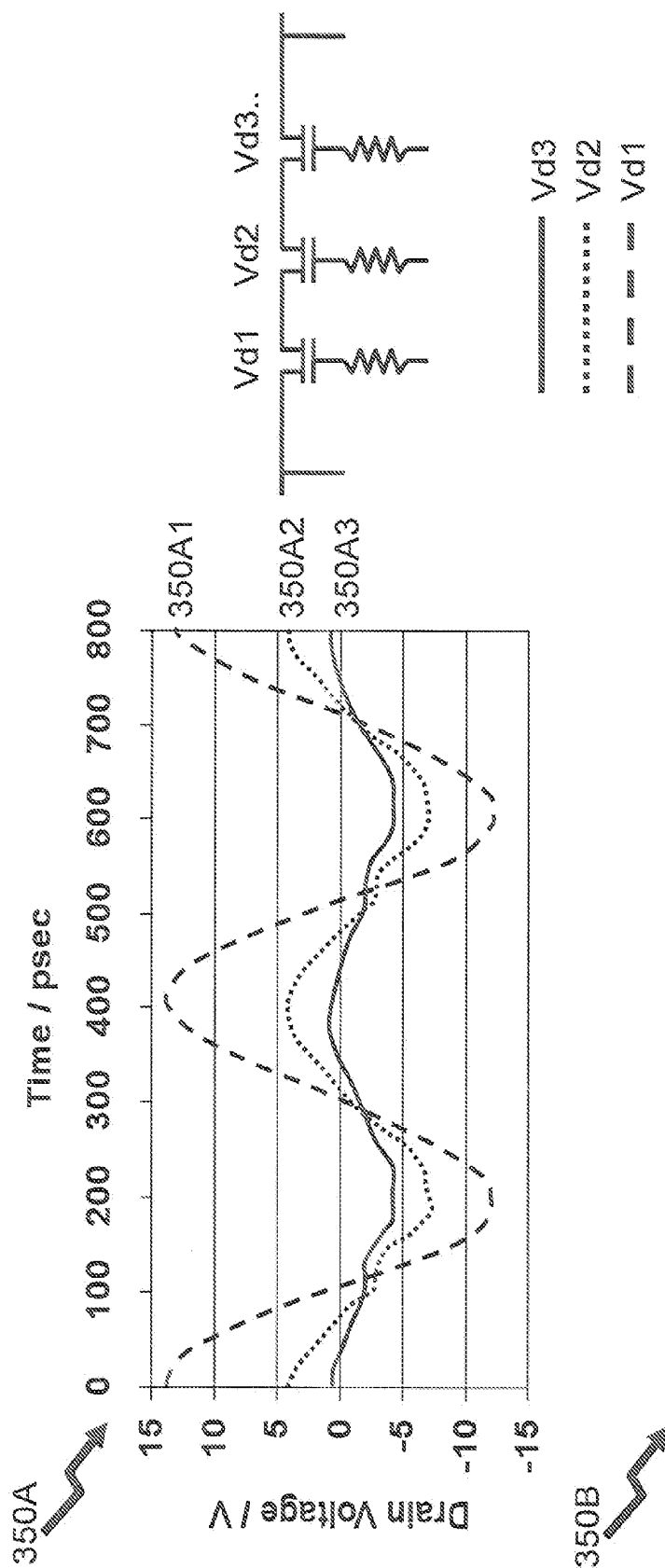


Fig. 3B

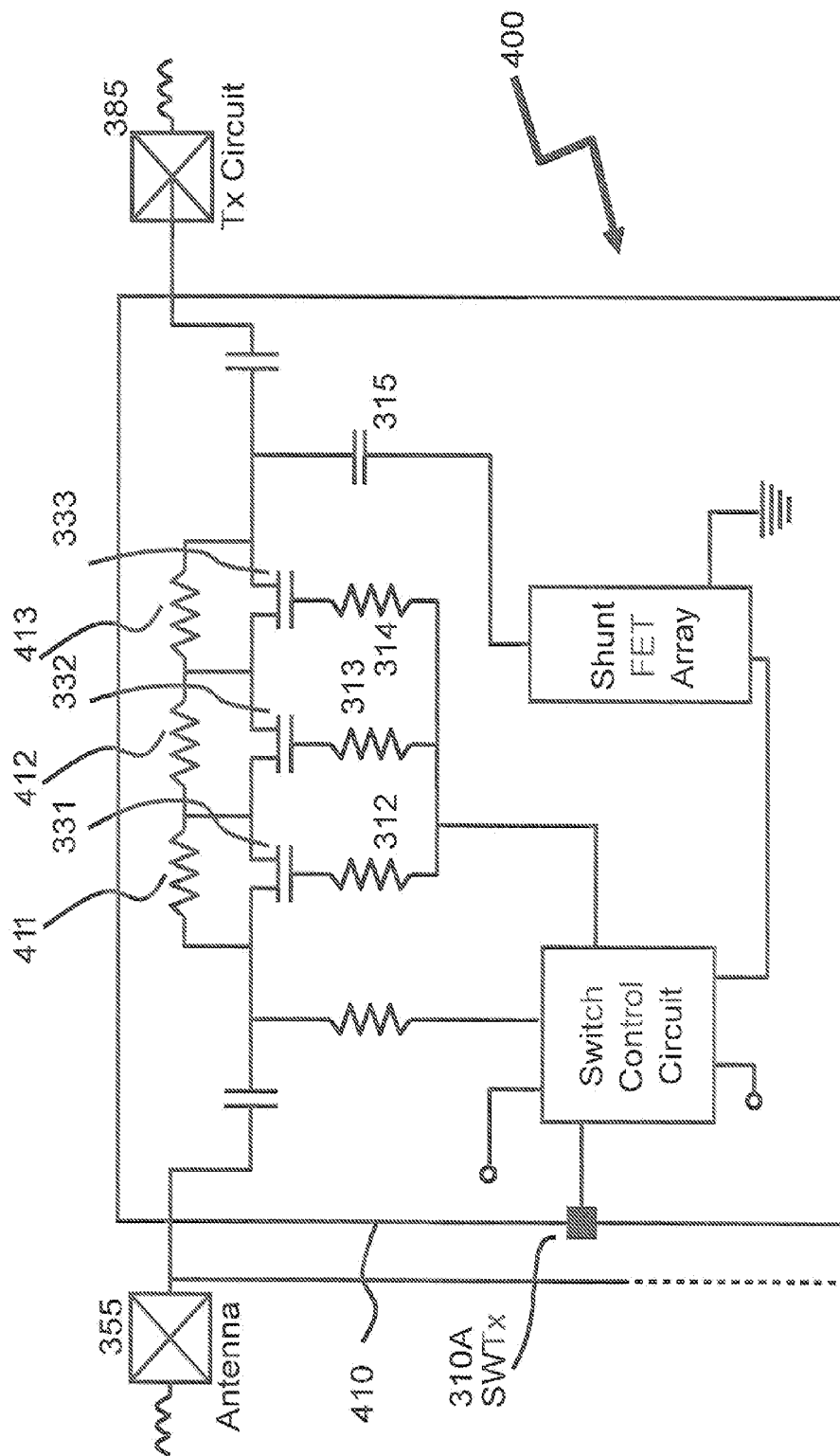


Fig. 4

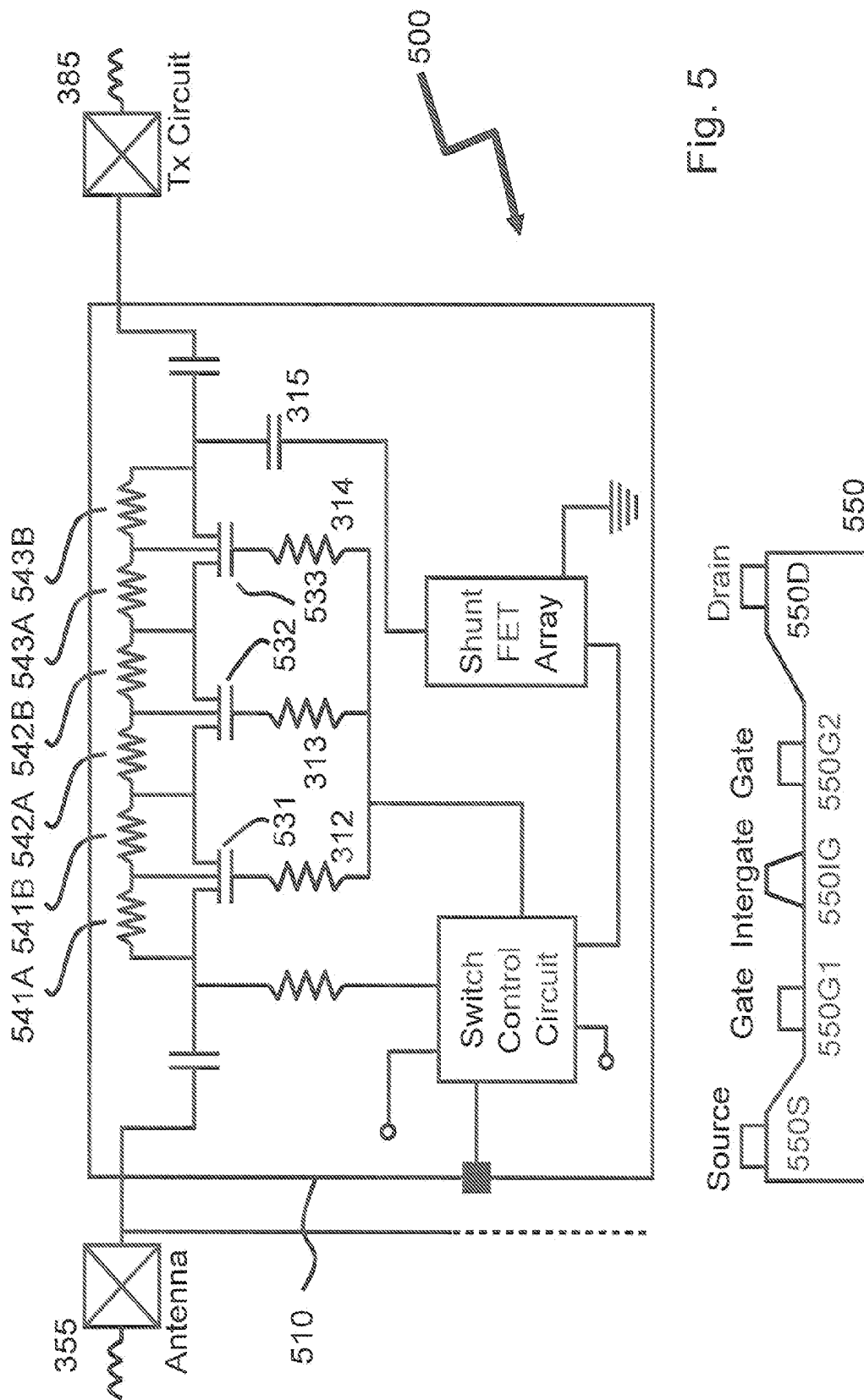


Fig. 5

SWITCHING CIRCUIT

FIELD OF THE INVENTION

[0001] The invention relates to microwave integrated circuits, and more particularly to an enhancement of microwave switch circuits.

BACKGROUND OF THE INVENTION

[0002] In recent years, the use of wireless and RF technology has increased dramatically. The number of cellular telephone subscribers alone worldwide is expected to reach 3 billion by the end of 2008 according to the International Telecommunication Union (ITU). Similarly the devices incorporating wireless technology have expanded, and continue to so. It is anticipated that the overall market for other wireless devices will exceed cellular telephone units as consumers procure multiple devices per household.

[0003] Wireless devices interface to wireless infrastructures that support data, voice and other services via one or more standards. Some examples of wireless standards in significant deployment today include:

[0004] WiFi [ANSI/IEEE Standard 802.11];

[0005] WiMAX [IEEE Standard 802.16];

[0006] Bluetooth [IEEE Standard 802.15.1];

[0007] Industrial, Scientific and Medical (ISM) [International Telecommunications Union Recommendations 5.138, 5.150, and 5.280]; and

[0008] GSM 850/900/1800/1900 [European Telecommunications Standards Institute (ETSI)] and its extensions General Packet Radio Service (GPRS) and Enhanced Data Rates for GSM Evolution (EDGE).

[0009] Pricing of finished products is often a major factor in the commercial success of products. Accordingly, monolithic integration of the electronics to result in devices with low parts count—a small number of integrated circuits (ICs)—is common practice. In fact, a typical RF system will comprise a baseband controller IC, a radio receiver and transmitter, and an RF signal front-end that may include power amplifiers, low-noise amplifiers, switches, and filters amongst other possible signal conditioning blocks. These integrated circuits are manufactured using a silicon-based technology platform for baseband elements of the circuit that are ‘logic’ intensive and, typically from silicon germanium, gallium arsenide, and indium phosphide for many RF circuit elements that condition the incoming or outgoing radio signal primarily in the analog or RF domain. The RF circuit elements form a microwave circuit path from the RF signal mixers that are upconverting or downconverting the RF signals via amplifiers, microwave filters, circulators, etc. The RF signal is, of course, received from or transmitted to an RF antenna or other load such as a co-axial cable. An RF antenna or cable is an RF load for the transmitting circuit or RF signal front-end. Moreover, a collection of RF circuit elements might be manifested in the form of a monolithic microwave integrated circuit (MMIC) and may be part of the RF front-end in the form of a module.

[0010] Within many wireless consumer electronics products that are intended to receive or transmit information is a transmit/receive switch circuit that selectively connects a microwave transmission circuit to the RF load of the consumer electronics product and a microwave receiver circuit to the antenna or cable, such a switch circuit being a Single Pole Double Throw (SPDT) switch. The microwave transmission circuit and microwave receiver circuit are often a single bidi-

rectional transmit/receive circuit. In other instances where the wireless consumer electronic product operates with multiple wireless standards there may be a separate microwave transmission circuit and microwave receiver circuit for each of the wireless standards supported. For example a wireless device supporting two wireless standards requiring different MMIC technologies for each, such as IEEE 802.11a at 5 GHz and IEEE 802.16 at 2.4 GHz, would have a Single Pole Quadruple Throw (SPQT) wherein a single common antenna or cable port is selectively coupled to one of two possible transmitter connections and a corresponding one of two receiver connections.

[0011] Conventionally, high-performance RF/microwave switches are implemented with depletion-mode GaAs MES-FETs or PHEMTs. These devices are chosen because they offer very low R_{on} and C_{off} per unit gate width; these parameters determine switch insertion loss and isolation. The transistor is turned on by biasing $V_{gs} > V_p$, where V_p is the pinch-off voltage and $V_p < 0$ for a depletion-mode device. The transistor is turned off by biasing $V_{gs} < V_p$, where a typical value of V_p might be -1.0 V. So $V_{gs_{on}}$ might be 0 V and $V_{gs_{off}}$ might be -2 V. This is accomplished, for example, by biasing the source and drain at 2 V and switching the gate to 0 V (off) or 2 V (on).

[0012] The D-mode GaAs FET or PHEMT has three major disadvantages for use as a high-performance switch. First is the tendency of gate current to flow when $V_{gs} > 0$; the gate forms a Schottky diode to the channel which can turn on for large signal levels or inappropriate bias. Gate current flow leads to sharply increased loss and distortion in the switch. A second disadvantage is the absence of a complementary device type (p-channel FET); without a PFET, logic functions consume more power and die area. In some circuits it is difficult to control the switch using standard low-voltage CMOS levels. A third disadvantage is resulting higher die cost per unit area, which is aggravated by the relatively primitive and area-intensive ESD protection structures available in most GaAs FET processes.

[0013] Silicon-based RF/microwave switches that use the CMOS device as the core switch element are attractive because of the integration potential of combining both logic and RF functionality. In addition, the relatively low cost when compared to GaAs-based devices makes such Silicon-based RF/microwave switches attractive for the consumer electronics market. The conventional biasing arrangement and topology of an RF/microwave switch is, however, similar when the switch is manufactured using a Silicon-based CMOS technology or GaAs.

[0014] It is therefore a goal of the invention to overcome at least some of the limitations of the prior art.

SUMMARY OF THE INVENTION

[0015] In accordance with the invention there is provided a circuit comprising: a first RF switch operable in a first mode and in a second other mode, the RF switch comprising: an input port for receiving an RF signal, an output port for in the first mode providing the RF signal and in the second other mode other than providing the RF signal, a shunt switch for in the second other mode shunting the RF signal to ground and in the first mode for other than shunting the RF signal to ground, and a switch for in the first mode conducting the RF signal between the input port and the output port and in the second other mode other than conducting the RF signal between the input port and the output port; and a controller

comprising a switching circuit for providing simultaneously a plurality of control signals comprising: a first signal for biasing the switch between the first mode and the second other mode; an approximately complimentary signal for biasing the shunt switch between the second other mode and the first mode; and a biasing signal for biasing one of a source and a drain of the switch approximately in accordance with the approximately complimentary signal.

[0016] In accordance with another embodiment of the invention there is provided a method comprising: providing a switching circuit for switching a signal from an input port to an output port thereof, providing a shunting circuit for switchably shunting the signal from the input port to ground; providing a control signal for biasing a control port of the shunting circuit and an approximately complimentary control signal for biasing a control port of the switching circuit to either shunt a signal received at the input port or to switch the signal to the output port; and, providing a bias signal for biasing a port within the switching circuit along the signal path between the input port and the output port.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Exemplary embodiments of the invention will now be described in conjunction with the following drawings, in which:

[0018] FIG. 1A illustrates a simple prior art microwave switch circuit according to Bergener et al.

[0019] FIG. 1B illustrates a typical prior art microwave switch circuit according to Bergener et al.

[0020] FIG. 2 illustrates a prior art microwave switch according to Burghartz.

[0021] FIG. 3A illustrates an exemplary embodiment of the invention for applying full ON/OFF drive to the RF FETs.

[0022] FIG. 3B illustrates a typical performance of the design of FIG. 3A.

[0023] FIG. 4 illustrates an exemplary embodiment of the invention applying drain-source resistors to the series FETs of FIG. 3A.

[0024] FIG. 5 illustrates an exemplary embodiment of the invention wherein the series FETs of the microwave switch are modified to include inter-gate electrodes.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0025] Referring to FIG. 1A there is shown a simple prior art microwave switch circuit 100 according to Bergener et al (U.S. Pat. No. 6,804,502). The microwave switch circuit 100 comprises four MOSFET transistors 123, 124, 127 and 128. The transistors 123 and 124 act as “pass” or “switching” transistors, and are configured to couple respective RF input nodes RF1 Input 121 and RF2 Input 122 to a common RF node RF Common 125. For example, when enabled—switched “on,” the switching transistor 123 couples a first RF signal applied to RF node RF1 Input port 121 to the RF common node RF Common 125. Similarly, when enabled, the switching transistor 124 couples a second RF signal applied to second RF node RF2 Input port 122, to the RF common node RF Common 125. The shunting transistors, 127 and 128, when enabled, act to shunt the respective RF signals to ground when their associated RF nodes are uncoupled from the RF common node RF Common 125. This uncoupling occurs when the respective switching transistor, switching

transistor 123 or switching transistor 124, is electrically connected to the associated node RF1 Input 121 or RF2 Input 122 is turned “off.”

[0026] Such a microwave switch circuit 100 when implemented using bulk silicon CMOS RF switches disadvantageously exhibits high insertion loss, low compression, and poor linearity performance characteristics. In contrast, implementing microwave switch circuit 100 with gallium arsenide (GaAs) semiconductor technology overcomes this as the semi-insulating GaAs substrate material results in parasitic substrate resistances being greatly reduced, thereby reducing RF switch insertion loss. Similarly, the semi-insulating GaAs substrate improves switch isolation. GaAs whilst offering improved performance compared with Si CMOS disadvantageously has higher manufacturing costs. As such it would be beneficial to enhance the performance of Si CMOS RF microwave switches. Referring to FIG. 1B illustrated is a prior art microwave switch circuit 150 according to Bergener et al that attempts to redress the performance issues of Si CMOS.

[0027] The microwave switch circuit 150 comprises four clusters or “groupings” of MOSFET transistors, identified in FIG. 1B as transistor groupings 133, 134, 137 and 138. Two transistor groupings comprise “pass” or “switching” transistor groupings 133 and 134, and two transistor groupings comprise shunting transistor groupings 137 and 138. Each transistor grouping comprises three MOSFET transistors arranged in a serial configuration. For example, in the embodiment shown in FIG. 1B, the switching grouping 133 includes three switching transistors, M133A, M133B, and M133C. Similarly, the switching grouping 134 includes three switching transistors, M134A, M134B, and M134C. The shunting grouping 137 includes three transistors M137A, M137B, and M137C. Similarly, the shunting grouping 138 includes three transistors, M138A, M138B, and M138C.

[0028] As shown in FIG. 1B, microwave switch circuit 150 is controlled by two control signals, SW, and its inverse, SW-. These control signals are coupled to the gates of their respective transistors through gate resistors. For example, the control signal SW controls the operation of the three transistors in the switching transistor grouping 133, M133A, M133B, and M133C, through gate resistors, R133A, R133B, and R133C, respectively. The control signal SW propagates to the switching transistor grouping 133 via input node 133A, and is also provided to input node 138A to control the shunting transistor grouping 138. Similarly, the inverse of SW, SW-, controls the switching transistor grouping 134 via input node 134. SW- is also provided to input node 137A to control the shunting transistor grouping 137. SW- is similarly applied to the transistors M134A, M134B, and M134C of switching transistor grouping 134 via three gate resistors, R134A, R134B, and R134C, respectively.

[0029] The switching transistor groupings 133 and 134 act as pass or switching transistors, and are configured to alternatively couple RF nodes, RF1 Input port 131 and RF2 Input port 132, to a common RF node RF Common 135. For example, when enabled, the switching transistor grouping 133 couples an RF signal applied to RF input node RF1 Input port 131 to the RF common node RF Common 135. Similarly, when enabled, the switching transistor grouping 134 couples a RF signal from the RF node RF2 Input port 132 to the RF common node RF Common 135. The shunting transistor groupings, 137 and 138, when enabled, act to shunt signals from the RF input nodes to ground when their associated RF nodes are uncoupled from the RF common node, i.e., when

the switching transistor grouping, **133** or **134**, that is electrically connected to the associated input node is turned “off.”

[0030] As taught by Bergener the microwave switch circuit **150** is not manufactured using a conventional Si CMOS manufacturing methodology. Rather the MOSFET transistors within the transistors groupings **133**, **134**, **137** and **138** are implemented using a fully insulating substrate silicon-on-insulator (SOI) technology. More specifically, Bergener teaches using “Ultra-Thin-Silicon” (UTSi), which is also known as Ultrathin Silicon-on-Sapphire due to the use of thin film silicon on a sapphire substrate rather than a silicon wafer. The fully insulating sapphire substrate enhances the performance characteristics of the RF switch by reducing the deleterious substrate coupling effects associated with non-insulating and partially insulating substrates. For example, improvements in insertion loss are realized by lowering the transistor “on” resistances and by reducing parasitic substrate resistances. In addition, switch isolation is improved using the fully insulating substrates provided by UTSi technology. Owing to the fully insulating nature of silicon-on-sapphire technology, the parasitic capacitance between the nodes of the microwave switch circuit **150** is greatly reduced as compared with bulk CMOS and other traditional integrated circuit manufacturing technologies.

[0031] However, whilst Bergener teaches a CMOS circuit, it is still one manufactured using unconventional manufacturing technology different from the bulk of low cost Si CMOS, which employs a low resistivity silicon substrate. An alternative approach is shown in respect of FIG. 2, which illustrates a prior art microwave switch **200** according to Burghartz. The microwave switch **200** as shown is an SPST switch that includes a port, RF input port **221**, where an RF signal is applied to the microwave switch **200**, an output port, RF Output port **222**, and a switch control port **223** which receives a bias signal for controlling an ON and OFF status of the switch. The RF signal appears at output port **222** with low insertion loss in the ON state, and with high insertion loss in the OFF state.

[0032] First FET **201** is electrically connected to both the RF Input port **221** and RF Output port **222** and includes gate **201G**, source **201S**, drain **201D**, and back gate contact **201B**. First FET **201** as well as the other FETs **202**, **203**, and **204** are silicon MOSFETs operating in depletion mode. Gate **201G** of first FET **201** is electrically connected to switch control port **223**, the source **201S** to the RF input port **221**, and the drain **201D** to the RF output port **222**. The back gate contact **201B** is coupled to source **203S** and drain **204D** of second and third FETs **202** and **203**. Drain **202D** of second FET **202** is electrically connected to RF Input port **221**, while the source **203S** of third FET is electrically connected to ground potential. The respective back gate contacts **202B** and **203B** of the second and third FETs **202** and **203** are commonly electrically connected to ground.

[0033] The gate **202G** of second FET **202** is electrically connected to switch control port **223**, while gate **203G** of third FET **203** is electrically connected to the output port of inverter **218**. The input signal port of the inverter **218** is electrically connected to switch control port **223**. The output port of the inverter **218** is electrically connected to the gate **204G** of the fourth FET **204**, the shunt FET, which has its source **204S** and back gate **204B** at ground and its drain **204D** coupled to RF output **222**. In the ON-state of the microwave switch **200**, a bias control signal applied to switch control port **223** is in a first state, e.g., $V_{GS}=OV$, thereby turning first and second

FETs **201** and **202** ON. Also, third and fourth FETs **203** and **204** are each OFF, since inverter **118** provides bias of opposite state to the gates **203G** and **204G** of third and fourth FETs **203** and **204**, respectively. With second FET **202** ON, the back gate **201B** and source **201S** of the first FET **201** are electrically connected together through the second FET **202**. This electrical connection of source **201S** and back gate **201B** regions minimizes the on-resistance of first FET **201**. Also, in the ON state, third FET **203** is off and thus presents high shunt impedance, which limits additional loss for the microwave switch **200**. In the OFF state of the microwave switch **200**, the bias control signal applied to switch control port **223** is in the opposite state, and hence first and second FETs **201** and **202** are OFF while third and fourth FETs **203** and **204** are ON. As a result, back gate contact **201B** is connected via third FET **203** to ground potential, as source **203S** is at ground potential. This maximizes the off-resistance of the series FET, first FET **201**. Also fourth FET **204** is ON, which increases the isolation, insertion loss, of the overall microwave switch **200** in the OFF state, since an RF short to ground is provided for coupling most of the power that leaks through first FET **201** to ground and not the RF output port **222**.

[0034] Insertion loss within a microwave switch such as prior art switch **200** is least when the FETs within the switching group, i.e. first FET **201**, are driven to their hardest ON state. Similarly highest isolation occurs when the FETs within the switching group are driven to their hardest OFF state and the shunt group, i.e. fourth FET **204**, are driven to their hardest ON state. An exemplary embodiment of the invention for applying ON/OFF drive to the switching and shunt FETs is shown by microwave switch circuit **300**. As shown an antenna **355** is intended for connection to one of three circuits, namely Tx circuit **385**, Rx circuit **365**, and test circuit **375**. Disposed between each of these three circuits and the antenna **355** are switching circuits **310**, **360** and **370**, respectively.

[0035] Considering the first switching circuit **310**, which is often typical of all three switching circuits **310**, **360** and **370**, then the switching path between the antenna **355** and Tx circuit **385** comprises first decoupling capacitor **321**, first through third switching FETs **331** through **333**, and second decoupling capacitor **324**. The first through third switching FETs **331**, **332**, and **333** are cascaded drain to source, and for each their gate contact is electrically coupled to a second output port **350B** of a switch controller **350** via resistors **312**, **313**, and **314**, respectively. The drain of the FET **331** is also electrically coupled via a resistor **311** to a first output port **350A** of the switch controller **350**. The third switching FET **333** has its source capacitively coupled via capacitor **315** to the drain contact of upper FET **341** of shunt transistor grouping comprising upper FET **341**, middle FET **342**, and lower FET **343**. As with the switching transistor grouping, the shunt transistor grouping of FETs **341**, **342**, and **343** are electrically coupled source contact to drain contact, whilst the source contact of lower FET **343** is capacitively coupled to ground and resistively coupled to port **350B** via resistor **391**. The gate contacts of upper FET **341**, middle FET **342**, and lower FET **343** are all electrically coupled to a third output port **350C** of the switch controller **350** via resistors **316**, **317**, and **318**, respectively.

[0036] The switch controller **350** is controlled from an input port Switch Tx (SWTx) **310A**. Also electrically coupled to the switch controller **350** are lower voltage rail V_{LO} at lower voltage port **310C** and upper voltage rail V_{HI} at upper voltage

port 310B. V_{HI} is provided from a regulator 380 to which upper voltage port 310B is electrically connected via regulator output port 380B. The other regulator output ports 380C and 380D are interconnected to equivalent upper voltage ports within the switching circuits 360 and 370, respectively. Switching circuit 360 is interfaced to the antenna 355 and Rx circuit 365 is controlled via Switch Rx (SWRx) port 360A. Similarly switching circuit 370 disposed between the antenna 355 and test circuit 375 is controlled via Switch (SWBT) port 370A. The regulator 380 is provided with a voltage to be regulated from regulator input port 380A, for example from a battery of a wireless handheld device V_{BAT} .

[0037] SWTx 310A is electrically coupled to the gates of first and second controller transistors 351 and 353. The drain of first controller transistor 351 is electrically coupled to the upper voltage rail V_{HI} , the source of first controller transistor 351 is electrically coupled to the drain of second controller transistor 353, and the drain of second controller transistor 353 is electrically coupled to the lower voltage rail V_{LO} . Similarly third and fourth controller transistors 352 and 354, respectively, are disposed between the upper voltage rail V_{HI} and lower voltage rail V_{LO} . The gates of the third and fourth controller transistors are electrically coupled to the mid-point drain-source connection between the first and second controller transistors 351 and 353, respectively. First controller output port 350A is also electrically coupled to this mid-point drain-source connection, as is the third controller output port 350C. The second controller output port 350B is electrically coupled to the mid-point drain-source connection between the third and fourth controller transistors 352 and 354, respectively.

[0038] Accordingly in operation, if a SWTx low signal is applied to SWTx port 310A this results in the switching FETs 331, 332, and 333 being turned off with source-drain voltage at V_{HI} from first controller output port 350A, and the gates at V_{LO} or ground from second controller output port 350B. In this state, the shunt FETs 341, 342, and 343 are turned on with gate-voltage at V_{HI} from third controller output port 350C, and the source-drain voltage at V_{LO} or ground from second controller output port 350B. If SWTx is high, V_{HI} , then the switching FETs are turned on with the source-drain voltage at V_{LO} and the gates biased at V_{HI} ; the shunt FETs are turned off with gates—at V_{LO} or ground and the source-drain voltage at V_{HI} .

[0039] As shown in schematic, the drain of a last shunt FET 343 is coupled to a signal complementary to that provided to the gate thereof. Here, the complementary signal is a signal provided to the gates of the switching FETs 331, 332, and 333. This provides a similar advantage for the shunt FET switching as is provided and explained for the switching FET.

[0040] Advantageously, each switching circuit, such as first switching circuit 310, provides approximately maximum possible "on" and "off" drive voltages to the FETs in switching and shunt paths. Additionally AC coupling of the switching circuit with respect of the antenna 355 and electrically coupled circuit, i.e. Tx circuit 385, is inherently provided. Optionally the capacitors 321 and 324 are chosen to be resonant with the bond wires interconnecting the switch circuit 300, comprising switching circuit 310, 360 and 370, to the antenna 355, Tx circuit 385, Rx circuit 365, and test circuit 375. For example, for a switch circuit designed to operate at 2.45 GHz where a typical bond wire inductance is 500 pH then these capacitors would be specified at nominal 8.4 pF.

[0041] As described supra in respect of microwave switch circuit 300 the regulator 380 provides a regulated output voltage V_{HI} to the regulator output ports 380B, 380C, and 380D which are electrically coupled to the switching circuits 310, 360, and 370, respectively. Optionally, regulator 380 is also interfaced to circuitry that determines whether a switching circuit has been enabled, i.e. has one of SWTx, SWRx, and SWBT been set to enable a respective switching circuit. If none of these three control signals has been enabled, this obviates regulation of voltage such that V_{HI} generated is directly supplied without regulation and the control logic operates with the circuit working at the same voltage levels, namely ground or V_{LO} and V_{HI} , so as to ensure no latch-up within the circuit and unwanted power dissipation. Since no average current is drawn from V_{HI} it merely serves as a power supply for static CMOS inverters within the controller circuits such as controller circuit 350.

[0042] Referring to FIG. 3B illustrated is a typical performance according to the design of FIG. 3A. As shown, there is first time-voltage graph 350A depicting voltage at each drain contact within the switching FETs 331, 332, and 333. Hence there is shown first curve 350A1 representing drain voltage V_{d1} from first switching FET 331, second curve 350A2 representing drain voltage V_{d2} from the second switching FET 332, and third curve 350A3 representing drain voltage V_{d3} from the third switching FET 333. The voltage appearing at each drain voltage is reduced from first switching curve 350A1, a swing of approximately 26V, to third switching curve 350A3, with a swing of approximately 5V.

[0043] Referring to FIG. 4 there is illustrated an exemplary embodiment of the invention wherein drain-source resistors are provided to the switching FETs 331, 332 and 333 of FIG. 3A. As shown in microwave switch circuit 400, a single switching circuit 410 is depicted between antenna 355 and Tx circuit 385 and is controlled from SWTx port 310A. The single switching circuit 410 now has resistors 411, 412, and 413 disposed between the drain and source contacts of each of switching FETs 331, 332 and 333, respectively. Properly selected resistors act to reduce harmonic distortion.

[0044] Referring to FIG. 5 there is illustrated an exemplary embodiment of the invention wherein the switching FETs of the microwave switch are modified to include inter-gate electrodes. As shown microwave switch circuit 500 comprises a switching circuit 510 disposed between antenna 355 and Tx circuit 385. Now each of the switching FETs 531 through 533 is implemented as shown by FET structure 550. As such, the FET structure 550 comprises source contact 550S, drain contact 550D, and gate contacts 550G1 and 550G2. However, now disposed between the gate contacts 550G1 and 550G2 is intergate contact 550IG.

[0045] Accordingly, resistors between the drain-source of the switching FETs, such as resistors 411, 412, and 413 of FIG. 4, are replaced by pairs of resistors. Hence first switching FET 531 has first resistor 541A between drain and intergate electrode and second resistor 541B between the intergate electrode and source. Second switching FET 532 has third and fourth resistors 542A and 542B disposed to connect the intergate contact 550G to the drain and source contacts, and third switching FET 533 has fifth and sixth resistors 543A and 543B disposed to connect the intergate contact 550G to the drain and source contacts. Whilst each switching FET 531 through 533 is depicted with a single resistor 312 through 314 between the gate contacts and the switch control circuit, each gate contact 550G1 and 550G2 optionally is electrically

coupled via a separate resistor (not shown for clarity). Biasing the intergate electrode changes the pinch-off voltage, thereby improving suppression of harmonics further within the switching FETs.

[0046] Optionally the switching FET configurations of FIGS. 4 and 5 are applied to the shunt FETs even though harmonic suppression whilst shunting RF power to ground is not typically as important as it is within the switching path. The embodiments herein described are applicable to silicon CMOS based FETs thereby allowing for low cost manufacturing as well as offering integration of the switching circuits with standard Si CMOS transmit/receive circuits.

[0047] Numerous other embodiments may be envisaged without departing from the spirit or scope of the invention.

What is claimed is:

1. A circuit comprising:
 - a first RF switch operable in a first mode and in a second other mode, the RF switch comprising:
 - an input port for receiving an RF signal,
 - an output port for in the first mode providing the RF signal and in the second other mode other than providing the RF signal,
 - a shunt switch for in the second other mode shunting the RF signal to ground and in the first mode other than shunting the RF signal to ground, and
 - a switch for in the first mode conducting the RF signal between the input port and the output port and in the second other mode other than conducting the RF signal between the input port and the output port; and
 - a controller comprising a switching circuit for providing simultaneously a plurality of control signals comprising:
 - a first signal for biasing the switch between the first mode and the second other mode;
 - an approximately complementary signal for biasing the shunt switch between the second other mode and the first mode; and
 - a biasing signal for biasing one of a source and a drain of the switch approximately in accordance with the approximately complementary signal.
2. A circuit according to claim 1 wherein the biasing signal is provided proximate the output port.
3. A circuit according to claim 1 wherein in use the biasing signal and the first signal cooperate to provide a larger voltage across the gate-channel of the switch.
4. A circuit according to claim 1 wherein the controller is for providing a second biasing signal for biasing one of a source and a drain of the shunt switch proximate a ground port approximately in accordance with the first signal.
5. A circuit according to claim 1 wherein
 - the shunt switch comprises at least a shunt FET;
 - the switch comprises at least a switching FET; and
 - the controller comprises:
 - a control port for receiving a switch control signal;
 - an upper voltage supply rail for supplying a first supply voltage to the controller; and
 - a plurality of control switches for driving the gate of the at least a shunt FET for turning on the shunt FET in the second other mode and for turning off the shunt FET in the first mode of operation, for driving the gate of the at least a switching FET for turning off the switching FET in the second other mode and for turning on the switching FET in the first mode of operation, and for biasing a

drain of the at least a switching FET for increasing a voltage difference between the gate and the drain of the at least a switching FET.

6. A circuit according to claim 5 wherein the plurality of control switches comprises a first control switch and a second control switch arranged in series between the upper voltage supply rail and a lower voltage supply rail, a drain of the first control switch coupled to a source of the second control switch and a third control switch and a fourth control switch arranged in series between the upper voltage supply rail and a lower voltage supply rail, a drain of the third control switch coupled to a source of the fourth control switch, the gates of the third and fourth control switches coupled to the drain of the first control switch and the gates of the first and second control switches coupled to a control signal input port.

7. A circuit according to claim 6 wherein the first signal for biasing is provided at the drain of the third control switch, the approximately complementary signal is provided at the drain of the third control switch and the biasing signal is provided at the drain of the first control switch.

8. A circuit according to claim 7 wherein the drain of the switching FET is biased with an approximately complementary signal to that provided at the gate thereof.

9. A circuit according to claim 1 wherein

- the shunt switch comprises at least a shunt FET;
- the switch comprises at least a switching FET; and
- the controller comprises:
 - a control port for receiving a switch control signal;
 - an upper voltage supply rail for supplying a first supply voltage to the controller;
 - a plurality of control switches for driving the gate of the at least a shunt FET for turning on the shunt FET in the second other mode and for turning off the shunt FET in the first mode of operation, for driving the gate of the at least a switching FET for turning off the switching FET in the second other mode and for turning on the switching FET in the first mode of operation, for biasing a drain of the at least a switching FET for increasing a voltage difference between the gate and the drain of the at least a switching FET, and for biasing a drain of the at least a shunt FET for increasing a voltage difference between the gate and the drain of the at least a shunt FET.

10. A circuit according to claim 9 wherein the plurality of control switches comprises a first control switch and a second control switch arranged in series between the upper voltage supply rail and a lower voltage supply rail, a drain of the first control switch coupled to a source of the second control switch and a third control switch and a fourth control switch arranged in series between the upper voltage supply rail and a lower voltage supply rail, a drain of the third control switch coupled to a source of the fourth control switch, the gates of the third and fourth control switches coupled to the drain of the first control switch and the gates of the first and second control switches coupled to a control signal input port.

11. A circuit according to claim 10 wherein the first signal for biasing is provided at the drain of the third control switch, the approximately complementary signal is provided at the drain of the third control switch and the biasing signal is provided at the drain of the first control switch.

12. A circuit according to claim 11 wherein the drain of the switching FET is biased with an approximately complementary signal to that provided at the gate thereof.

13. A circuit according to claim 1 wherein the switch comprises a plurality of switching FETs coupled in series, a

drain of a preceding switching FET coupled to a source of a subsequent switching FET, each switching FET having a gate thereof resistively coupled to the first signal.

14. A circuit according to claim 1 wherein, each switching FET comprises:

- an intergate electrode disposed between a pair of switching FET gate contacts for biasing an intergate region to adjust a characteristic of the switching FET;
- a first feed-forward resistor electrically coupled to the switching FET drain contact and the intergate electrode; and
- a second feed-forward resistor electrically coupled to the switching FET source contact and the intergate electrode.

15. A circuit according to claim 1 wherein the circuit consists of an integrated circuit manufactured using at least one of a silicon CMOS process, a GaAs process, and a SiGe process.

16. A method comprising:

- providing a switching circuit for switching a signal from an input port to an output port thereof,
- providing a shunting circuit for switchably shunting the signal from the input port to ground;
- providing a control signal for biasing a control port of the shunting circuit and an approximately complimentary

control signal for biasing of a control port of the switching circuit to either shunt a signal received at the input port or to switch the signal to the output port; and, providing a bias signal for biasing a port within the switching circuit along the signal path between the input port and the output port.

17. A method according to claim 16 wherein the bias signal is approximately a same signal as the control signal provided to the shunting circuit.

18. A method according to claim 17 wherein the bias signal is for increasing a gate-drain voltage difference across a FET of the switching circuit.

19. A method according to claim 18 wherein the bias signal is provided from a drain source junction between two first transistors coupled in series between an upper voltage supply rail and a lower voltage supply rail.

20. A method according to claim 18 wherein the approximately complimentary control signal provided to the switching circuit is provided from a drain source junction between two second transistors coupled in series between an upper voltage supply rail and a lower voltage supply rail, the gates of the two second transistors coupled to the source drain junction of the two first transistors.

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