Fully Integrated Switch-LNA Front-End IC Design in CMOS: A Systematic Approach for WLAN

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***Abstract*—A fully integrated front-end IC is demonstrated for 802.11b/g transceivers with integrated power amplifiers. The SP3T-LNA architecture integrates Bluetooth® functionality with transmit and receive for wireless LAN. The transmit switch achieves a P_{1dB} greater than 33.0 dBm at 2.5 GHz by employing a cross-biasing approach, transistor stacking and deep n-well process. Power handling techniques used for the switches and the associated performance tradeoffs are discussed. The measured noise figure of the LNA and the receive chain comprising both an LNA and a switch is 1.5 dB and 3.0 dB, respectively. The LNA achieves an IIP3 of 7.0 dBm while consuming 7.0 mA of current. The measured switching times are less than 350 ns. The front-end IC employs a 3.3 V supply and occupies 0.64 mm^2 in 0.18 μm bulk CMOS technology.**

***Index Terms*—CMOS, FEIC, switched LNA, T/R switch, wireless LAN.**

I. Introduction

WIRELESS LOCAL AREA NETWORK (WLAN) systems switch between transmit and receive functionality using a single-pole double-throw (SPDT) RF switch at the front-end. However, most of the modern WLAN module architectures have settled on the use of a SP3T switch in order to also incorporate Bluetooth® (BT) functionality [1], [2]. This allows the common blocks such as crystal oscillator, bandgap reference, and power management units to be shared between WLAN and Bluetooth®, thus saving die size, I/O count, and cost. To keep the overall solution cost down, the transceiver should be highly integrated with the baseband PHY and MAC as a System-on-Chip (SoC) solution, preferably in a low-complexity pure CMOS process [3]–[6]. Due to extensive CMOS scaling (sub-100 nm) and integration of the WLAN transceiver with baseband, it has become extremely difficult to integrate the RF front-end on the same chip to obtain the desired performance. Thus, a standalone front-end module is typically used, which includes performance critical blocks such as the RF switch, the low-noise amplifier on the receive side, and the power amplifier on the transmit side [7], [8]. Lately, standalone WLAN power amplifiers, and a power amplifier integrated with the WLAN transceiver have been demonstrated in highly scaled 65 nm CMOS technology [9], [10]. This approach necessitates RF front-end modules with only switch and LNA functionality for use with WLAN chipsets with integrated PAs.

Therefore, integrated SP3T and LNA as flip-chip die using GaAs pHEMT processes have been reported [11], [12]. WLAN switches have been historically dominated by GaAs platforms because of their superior high power handling capability and semi-insulating substrate. Owing to low mobility, high substrate conductivity, low breakdown voltage, and various parasitic parameters of CMOS processes, it is very challenging to design CMOS switches and LNA to simultaneously achieve low-insertion loss, high isolation, wide bandwidth, high power handling and low-noise comparable to their GaAs counterparts [13]. However, in the present work, the first implementation of a single-chip fully integrated SP3T and LNA front-end on 0.18 μm CMOS is reported for 802.11b/g WLAN applications at 2.5 GHz. The integrated solution includes on-chip dc blocking, bypass-mode, matching network and ESD protection and drives the die-size (0.64 mm^2) towards a low-cost, fully integrated solution.

One of the key constraints for a WLAN (or any portable) system is power dissipation. The most efficient technological approach for reducing power consumption is power-supply voltage. However, front-end power supply voltage (V_{DD}) is usually constrained by transceiver architecture and system requirements. In a typical radio receiver front-end, the low-noise amplifier (LNA) is one of the key components since it dominates the radio sensitivity. The LNA design involves tradeoffs between noise figure (NF), gain, power dissipation, input matching and harmonic content. With the added power dissipation constraint inherent in portable applications, the primary goal for LNA design is to achieve simultaneous noise and input matching at any given amount of power dissipation. The amplifier's compression point requirement also imposes a limitation on the LNA device size, thus making the simultaneous noise and input match harder to achieve. When the mobile device is close to a base station, the input signal can be high enough to overdrive the amplifier and thereby cause distortion [14]. A bypass mode is incorporated into the receive functionality which allows the amplifier to be switched into a low gain mode when the device is close to a base station [15]. While the switching and LNA functions are mostly achieved

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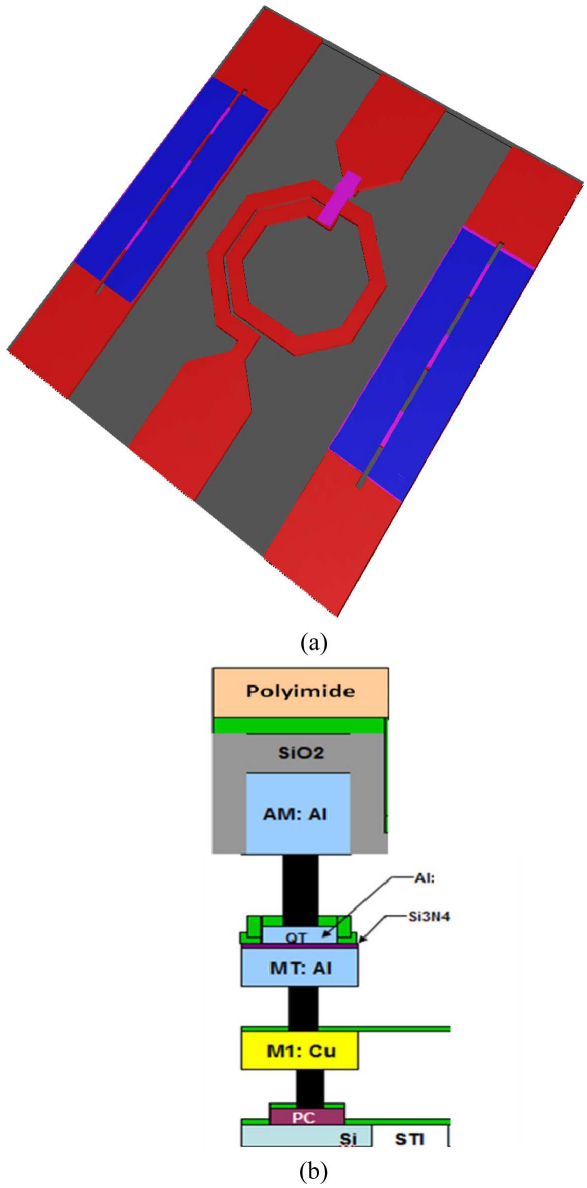

Fig. 1. (a) 3-D EM view of the inductor. (b) Back-end-of-line metal layers used in the three metal layer process.

using two separate devices, this work presents a fully integrated single-chip RF front-end solution for WLAN chipsets with integrated power amplifier. The power-handling techniques, as described in Section IV, allow one to achieve record power handling performance while maintaining competitive insertion loss with state-of-the-art CMOS T/R switches at 2.4 GHz without Bluetooth® functionality.

II. 180-nm CMOS Technology

The front-end integrated circuit (FEIC) has been fabricated in IBM's 180-nm bulk CMOS process. IBM's 7RF starting wafer is lightly doped p-type Si with a resistivity of 11–16 Ω-cm [16]. A low resistivity substrate can be detrimental for RF applications since it provides an extra capacitive component to the substrate. To verify the nature of the substrate in an RF context, an inductor's S-parameters were measured and substrate resistivity

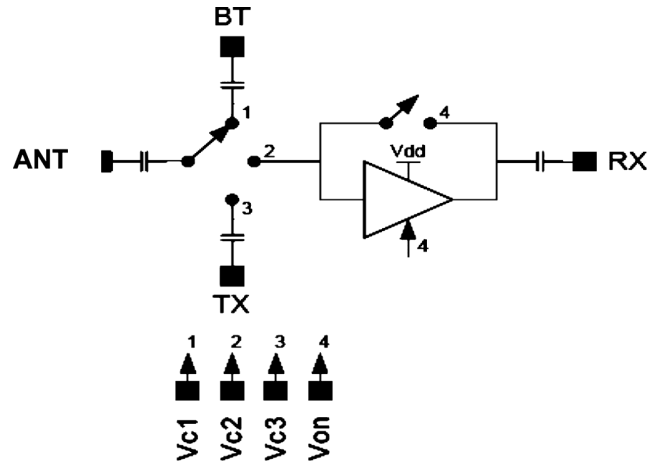

Fig. 2. Architecture of a switch-LNA WLAN front-end with integrated Bluetooth® functionality.

was used as a back-fit parameter in EM simulations, as shown in Fig. 1(a). The substrate resistivity was verified to be 13 Ω-cm.

The technology utilizes a twin-well CMOS process with shallow-trench isolation to provide isolation between FETs and other devices. Both thin and thick gate-oxide FETs are available in the technology, with an operating voltage of 1.8 V and 3.3 V, respectively. Triple-well isolation is provided for both types of FETs for improved substrate isolation. MIM caps, spiral inductors and transmission lines for RF interconnects are also provided as back-end passives. Finally, this technology uses copper wiring at the first metal level and aluminum wiring at the subsequent metal levels, as shown in Fig. 1(b). A three-layer metal stack is used for the present design.

III. RF Front-End IC Architecture

The FEIC is a single-chip solution with a Bluetooth® port to complement WLAN chipsets with integrated power amplifier. The FEIC integrates a SP3T switch and a low-noise amplifier with bypass mode. It is capable of switching between WLAN receive, WLAN transmit and Bluetooth®, as illustrated in Fig. 2.

When the transmit mode is ON, the signal from the PA is fed into the TX pin and the transmit throw of the switch is turned on. This allows the signal to be switched and propagated through to the antenna (ANT). In view of this architecture, one of the most critical specifications for the transmit and Bluetooth® switch is insertion loss. The maximum transmitted power of the system is reduced by the insertion loss of the transmit switch. Similarly, on the receive side, the insertion loss of the switch adds directly to the noise figure of the receiver. The number of shunt devices (for the on-throw) and series devices (for two off-throws) are critical to meet the isolation specification. Moreover, the Federal Communications Commission (FCC) imposes strict regulations for out-of-band RF emission, thus limiting the maximum modulated harmonics from the switch.

The FEIC is controlled by a logic decoder with four inputs and five modes, as shown in Table I. When the RX mode is enabled, Vc2 is set to high and the LNA is cascaded with the switch to improve the sensitivity of the receiver. The LNA shares a 3.3 V supply voltage with the switches and is turned on when

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TABLE I
CONTROLLER LOGIC FOR FEIC OPERATION

Mode#	Description	Vc1	Vc2	Vc3	Von
0	All Off	0	0	0	0
1	TX	0	0	1	0
2	BT	1	0	0	0
3	RX – high gain	0	1	0	1
4	RX – bypass	0	1	0	0

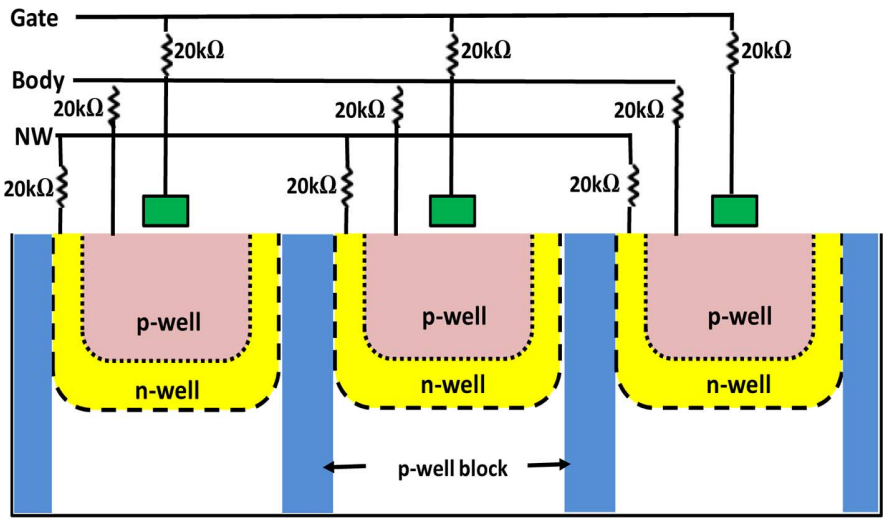

Fig. 3. A stack of three series transistors with isolated gate, p-well and n-well using 20 kΩ polysilicon resistors.

both Vc2 and Von are high. To avoid overdriving the LNA and causing distortion from a strong RF input signal, a bypass mode is provided in the LNA. The bypass mode is turned on when Vc2 is high and Von is low. The LNA is matched on-chip and all necessary paths are dc blocked with MIM caps. The sizes of series dc blocking MIM caps are chosen to provide optimum match at the frequency of interest.

IV. DESIGN METHODOLOGY

Key figures-of-merit of a RF switch include insertion loss, isolation, and power-handling capability, as measured by the power 1-dB compression point (P_{1dB}). CMOS switches usually have a lower power-handling capability compared to III-V pHEMT switches due to their lower breakdown voltage and the parasitic diodes between source/drain and the body. To improve the power handling capability and linearity of the switches, the following methods are used, as shown in Fig. 3:

i) the bulk and n-well terminals of triple-well nMOS are kept floating (from a RF standpoint) to avoid forward biasing of parasitic diodes under large input signal [17],
ii) the series and shunt transistors are stacked to sustain higher voltage swings and therefore improve the power handling of the switch [18]–[20], and
iii) a cross-biasing arrangement is used in a series-shunt switch topology to dc bias the source and drain terminals for maximum swing across each transistor. The source and drain are kept at the same dc potential by means of a polysilicon resistor tied between the two terminals.

Isolated triple-well nMOS devices use deep n-well to isolate the p-well and divide the voltage swing in a stack of devices. The deep n-well separates the bulk of the nMOS transistors from the p-substrate. The p-well and deep n-well are left floating, thus reducing the parasitic loss by increasing the effective impedance in the body of the device, as shown in Fig. 3. The p-well is biased at 0 V, and the deep n-well is biased at 3.3 V through 20 kΩ polysilicon resistors to reverse bias the p-n junctions, reducing the parasitic capacitance associated with the diodes. The channel length of nMOS devices used is 0.32 μm.

At high frequency, the power handling of switch FETs is limited by voltage swing in the 'off' state (capacitive state) and current saturation in the 'on' state (resistive state). The series and shunt stacks are composed of two to three FETs each, so that the voltage across the stack is evenly divided among these FETs. Even though a three FET switch stack multiplies the voltage handling capability ideally by 3x, it also increases the insertion loss by adding the on-resistance of the three transistors in series. Thus, the increased power handling typically comes at the cost of higher insertion loss.

In a cross-biased approach, the source and drain of shunt transistors are connected to the gate of the series transistors and vice versa. This allows for more voltage headroom (higher linearity) across the shunt arm by biasing the source and drain of the transistor higher than the gate.

A. TX Switch Topology

A series-shunt topology was chosen for the TX switch, as shown in Fig. 4. The transmit mode needs to handle more than one-watt (30 dBm) of RF power while maintaining minimal insertion loss. When the transmit switch is on, the shunt (off) devices limit the maximum voltage swing before the parasitic diodes in the shunt transistors turn on and the switch starts to operate in compression. To minimize insertion loss of the transmit

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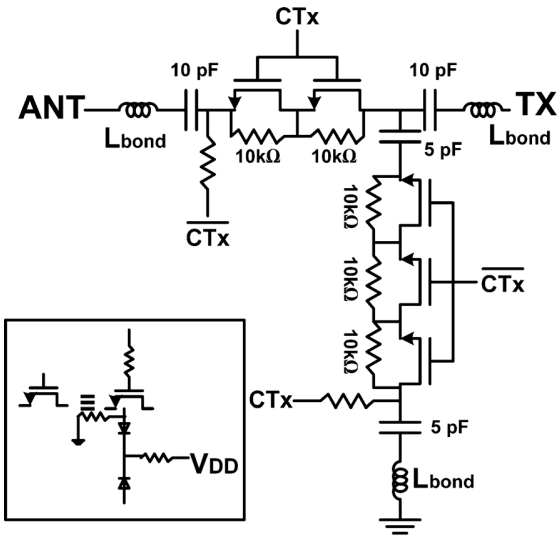

Fig. 4. Series-shunt stacked FET switch topology with cross-biasing for the transmit switch.

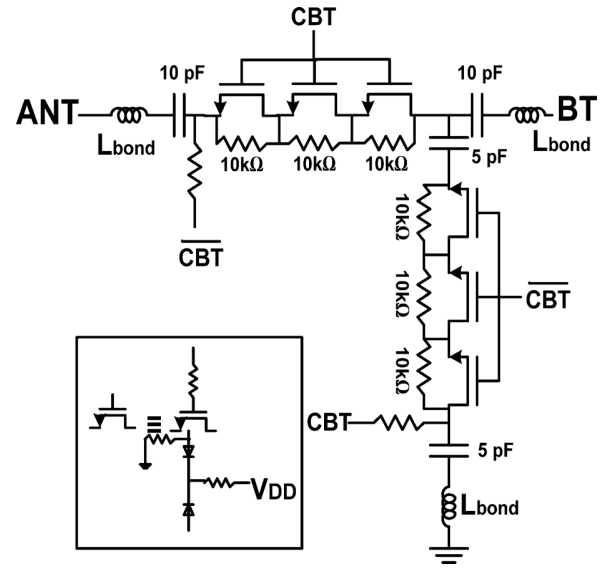

Fig. 5. Series-shunt stack topology of the Bluetooth® switch with 3-series and 3-shunt stack of FETs.

path, an asymmetrical switch design is used [14], [19]. An asymmetrical topology uses different switch stack designs for each switch throw, whereas a symmetrical topology adopts the same configuration in all throws with the most commonly used series-shunt configuration.

The correct balance between the on-resistance, parasitic capacitance and harmonics requirement must be established to size the devices correctly. While a bigger device allows lower on-resistance (and thus smaller insertion loss), it also has higher capacitance in off-state, leading to a higher insertion loss for other 'on' switch paths (Bluetooth® and receive) in the SP3T. In this case, the width of the series transistors was chosen to be 1000 μm, while the width of the shunt transistors was chosen to be 400 μm. This geometry optimizes the performance of the RF switches at 2.5 GHz. Since cross biasing is used to bias the series-arm and shunt-leg, on-chip dc blocking MIM capacitors are required, as shown in Fig. 4. In the final analysis, the dc power dissipated by the switch FET is only due to the leakage current in the device.

B. BT Switch Topology

The voltage swings 20 V peak-to-peak when a signal of 30 dBm is transmitted into 50 Ω on the transmit throw. Thus, the BT switch in "off" state should be able to tolerate this voltage swing without any of the series FETs turning "on". A stack of three series FETs is used in the Bluetooth® throw to withstand the high transmit voltage swing, as shown in Fig. 5. Additionally, it should not dissipate significant signal power and should maintain good isolation between transmit and Bluetooth® ports. The transmit throw also needs to have a good isolation in the BT mode so as not to draw power from the antenna (ANT), which would increase insertion loss.

C. RX Design

The switching part of the receive path uses a three-stack of series FETs. The shunt transistors are eliminated by adding a switch S1, which protects the LNA input from turning on due to

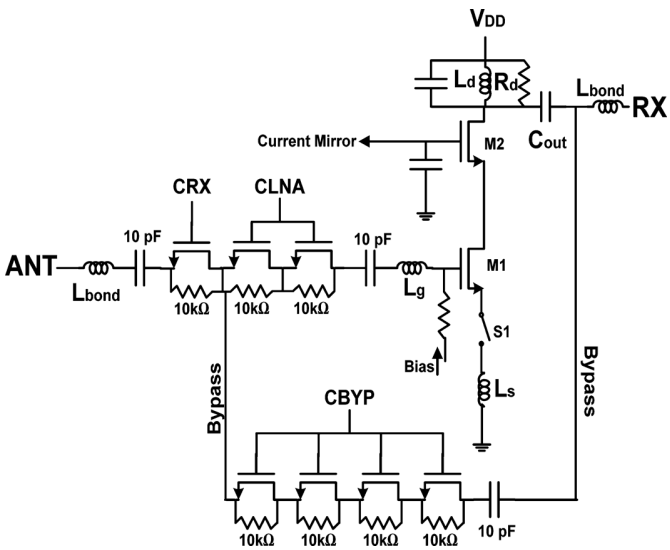

Fig. 6. Schematic of the receive path with high-gain mode (switch + LNA) and bypass mode.

the large voltage swing at the transmit output. Thus, S1 is turned on only during normal operation of the high-gain receive mode. The logic state CRX is set to high when either high-gain or bypass mode are enabled. The CLNA or CBYP are set to high when the high-gain or the bypass modes are enabled, respectively. The bypass switch uses a stack of four series transistors to maintain the required gain (-3 dB), as well as to provide sufficient isolation between the input and the output of the LNA. To minimize feedback and maintain stable operation of the LNA, the bypass path is tapped after the first series transistor, as shown in Fig. 6 below.

The LNA employs a cascode topology to realize high-gain and provide good isolation between the receive port and antenna. The 3.3 V thick-oxide cascode device (M2) enables direct operation with a 3.3 V rail, while the thin-oxide input device

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(M1) helps to minimize noise figure with a minimum channel length of 0.18 μm. The cascode is biased using a p-FET based current mirror and an on-chip constant-g_m source. The gates of both transistors are biased in such a way that the bias across input device M1 is 1.2 V. All of the matching elements are on-chip, and all the capacitors are implemented as MIM capacitors. The spiral inductor L_g utilizes a patterned ground shield structure, while the spiral inductor L_d is implemented without a ground shield to reduce the number of bondpads and hence the die area. The Q-factor of the output inductor L_d is less significant because of the resistance R_d, added to de-Q the output match for stable operation of the amplifier. The source degeneration inductance is implemented as a double bond-wire with an inductance of about 200 pH.

Once the drain current is fixed to 7 mA, the device width is scaled in order to move the real part of noise matching impedance close to 50 Ω. The gate widths of the FETs, M1 and M2, are both 300 μm. It is noteworthy that the devices cannot be sized too small due to the input $P_{1\ dB}$ constraint. Hence, there is a three-fold tradeoff between dc power consumption, minimal noise figure and power handling requirements. The next step is to match the input impedance to 50 Ω, which is accomplished by the addition of bond wire degeneration inductor. The value for this inductor, L_s is given by

$$L_s = \frac{50}{2\pi f_T} \tag{1}$$

where f_T is the cut-off frequency of the device at its operating point. Once the source degeneration inductance has been selected, the remaining portion of the input matching network, L_g, serves to resonate out the C_{GS} capacitance and conjugate match the reactive portion of the noise impedance. The following equation can be used to determine the value of L_g:

$$L_g = 1/(\omega^2 C_{GS}) - L_s. \tag{2}$$

Typically, this type of matching network is very narrow band, and therefore is suitable for 802.11 b/g WLAN applications with less than 100 MHz bandwidth.

D. Controller Design

A simplified schematic of the logic controller is shown in Fig. 7. Vc1 and Vc3 are buffered using NAND gates to provide enable signals for Bluetooth® and transmit throws, respectively. As shown in Table I, when Vc2 is high, either high-gain or bypass mode are enabled on the receive throw. Thus, the receive enable signal (CRx) is buffered from Vc2. Additional NAND logic is designed to enable the LNA in the high-gain mode, when both Vc2 and Von are high.

V. Circuit Implementation

The IC was fabricated on 180-nm CMOS technology provided by IBM using a standard resistivity ($\rho \sim 13$ Ω-cm) substrate. The active devices used in the design are 1.8 V and 3.3 V nMOS transistors with triple-well isolation. The geometry of the active devices was chosen to minimize the contribution from substrate coupling, which cannot be ignored in a low-resistivity bulk CMOS process. The values of the on-chip spiral inductors,

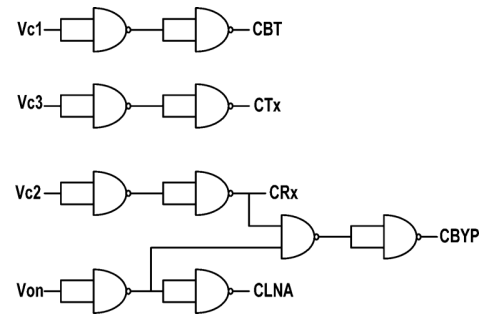

Fig. 7. NAND gate based logic decoder for switching between FEIC states.

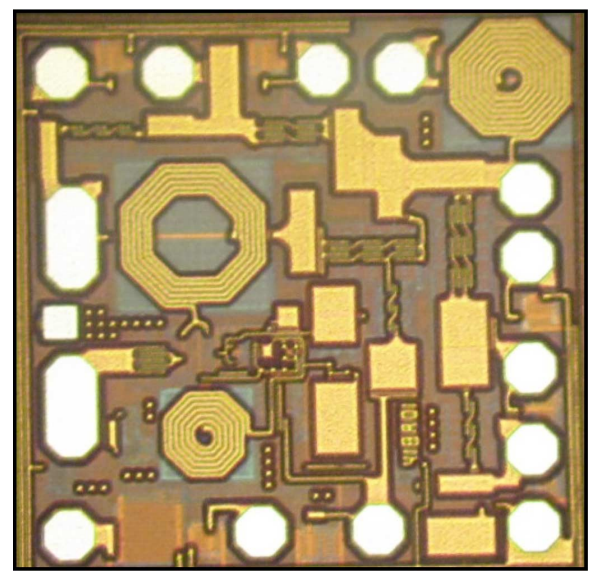

Fig. 8. Die micrograph of the FEIC.

L_g and L_d, have been optimized to 7.1 nH and 3 nH, respectively, as explained in Section IV.

A micrograph of the fabricated die is shown in Fig. 8. The chip dimensions are 0.8 mm × 0.8 mm including on-chip dc blocking and decoupling MIM capacitors. The LNA draws 7 mA current from a 3.3 V supply.

VI. Results and Discussion

For all measurements, the die were mounted directly on a FR-4 evaluation board and wire-bonded onto the respective traces. The reference plane for measurements is at the edge of the RF traces on the board.

A. Small-Signal

The measured S-parameters of transmit and Bluetooth® switches are shown in Fig. 9(a) and (b), respectively. The 10 pF on-chip series MIM capacitor not only serves as a dc blocking capacitor, but it also helps improve return loss (and, in turn, insertion loss) of the switch. The measured insertion loss between the transmit port and antenna is 1.3 dB at 2.4 GHz, while between the antenna port and Bluetooth® port is 1.45 dB. The return loss is about 20 dB in both the cases. Thus, the higher insertion loss for the Bluetooth® throw can be attributed to the extra series transistor in the Bluetooth®

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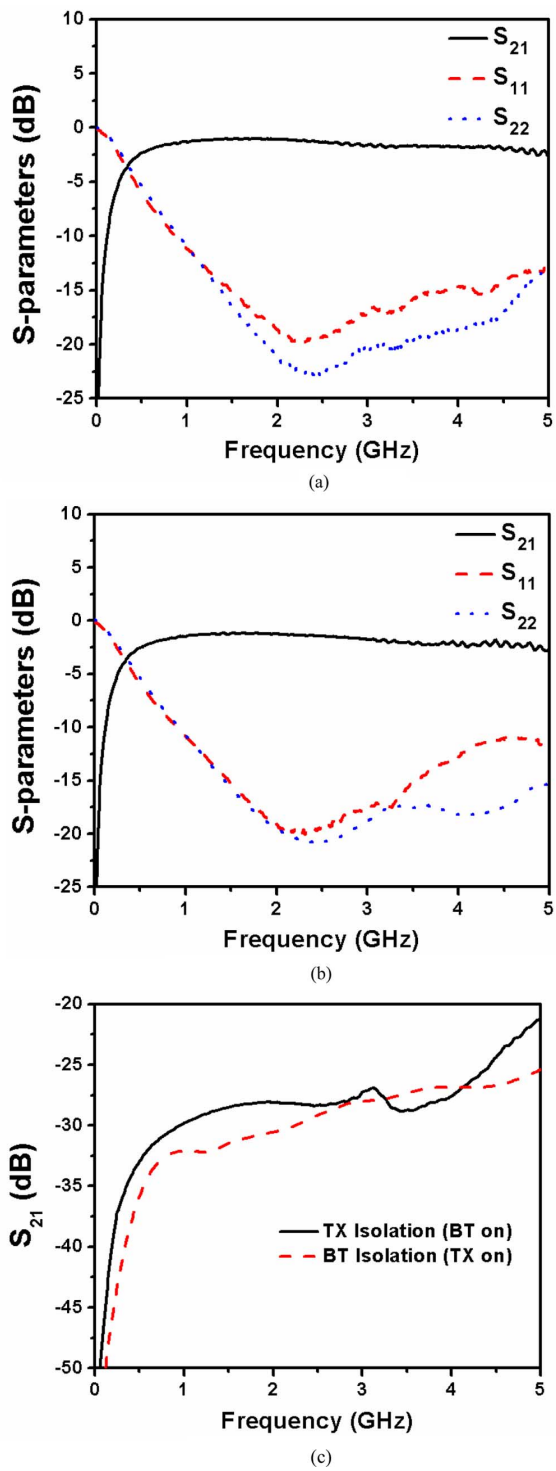

Fig. 9. (a) S-parameters of the transmit switch, (b) Bluetooth® switch, and (c) isolation between transmit and Bluetooth® throws.

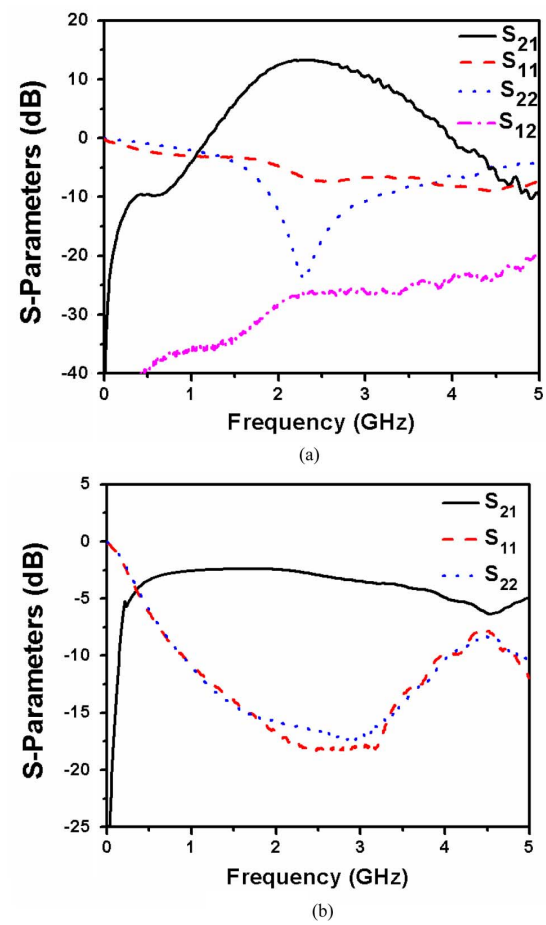

Fig. 10. Measured small-signal parameters of the receive path in (a) high gain mode, and (b) bypass or low-gain mode.

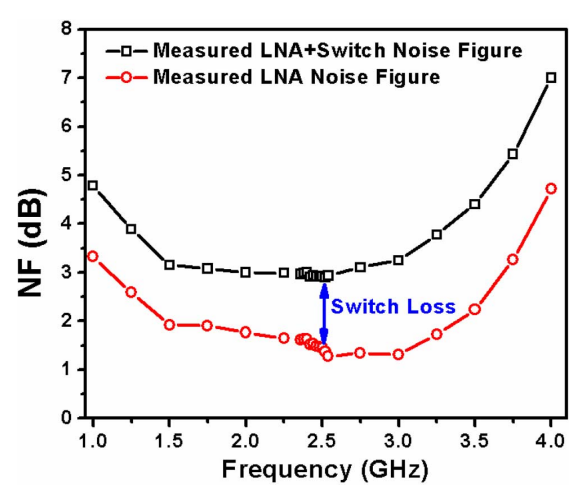

Fig. 11. Noise figure of the full receive path and the LNA. The LNA NF is 1.5 dB at 2.4 GHz.

path. It is noteworthy that the S-parameters are measured after terminating the remaining ports with 50 Ω load. The isolation between Bluetooth® and transmit throws is shown in Fig. 9(c). The measured in-band isolation between transmit and Bluetooth® port is better than 28 dB. This prevents the transmit signal from leaking into the Bluetooth® path, and vice versa.

The measured S-parameters of the LNA are shown in Fig. 10. In the high-gain mode, the LNA has a power gain of 13 dB at 2.4 GHz and a good output matching ($S_{22} \sim -20$ dB). The LNA draws 7.0 mA current from a 3.3 V supply. In the low-gain mode, the measured LNA gain is −2.7 dB (Fig. 10(b)), which meets the desired specification. The measured noise figure is plotted versus frequency in Fig. 11. The in-band receive noise figure is 3 dB, which includes the switch loss and the LNA noise figure. The noise figure is also plotted after de-embedding

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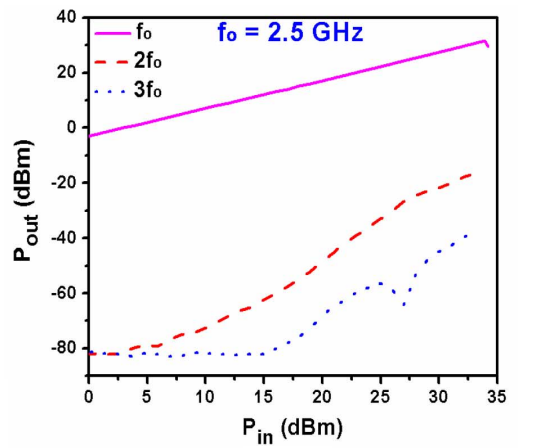
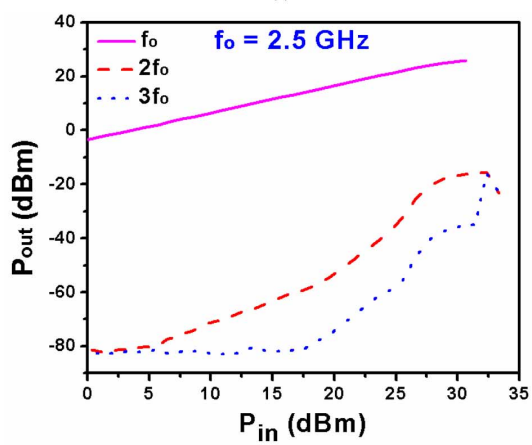


(a)



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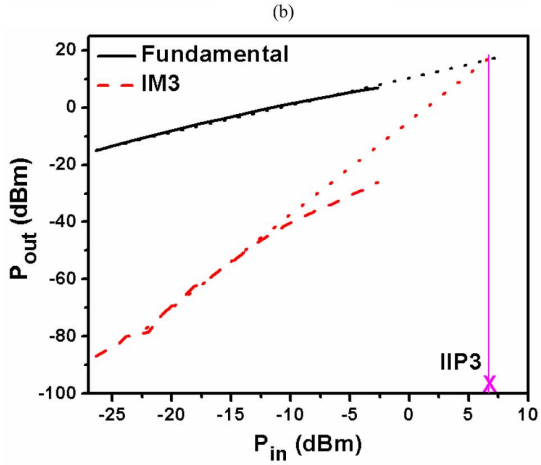
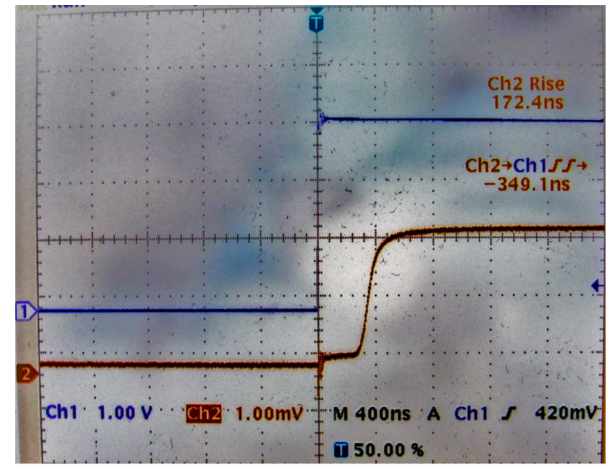
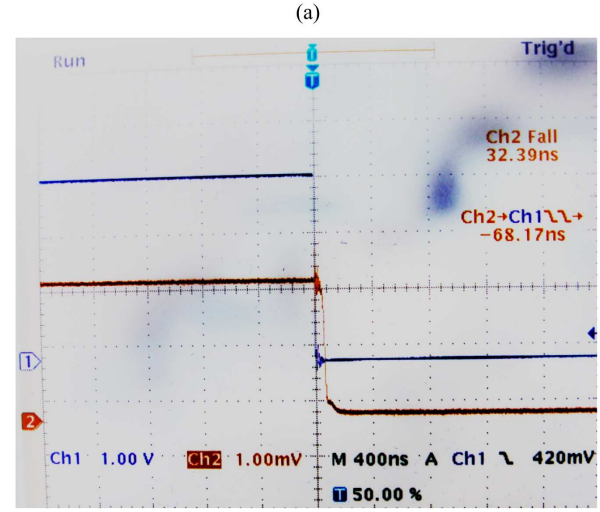


(c)

Fig. 12. Measured 1-dB compression point and harmonics of the (a) transmit switch, (b) Bluetooth® switch, and (c) receive path.



(a)



(b)

Fig. 13. (a) Turn-on and (b) turn-off time measurements for the switch paths at 2.5 GHz with an input power of +5 dBm.

the noise added by the switch FETs. The inductively degenerated cascode LNA has a noise figure of about 1.5 dB between 2.4 GHz and 2.5 GHz.

B. Large-Signal and Harmonics

Fig. 12(a) and (b) shows the measured 1-dB compression point of the transmit and Bluetooth® switches. From the measured data, 33 dBm of linear input power can be transmitted to the antenna through the transmit path. Thus, input power handling greater than 2 W in a standard 0.18 μm CMOS switch has been reported with 1.3 dB insertion loss. The less stringent requirements of the Bluetooth® throw allow for 30 dBm (1 W) linear power from the antenna to the Bluetooth® port. Second harmonics dominate the harmonic response of both the transmit and Bluetooth® switches. Fig. 12(c) shows the two-tone measurement on the receive side with a tone-spacing of 1 MHz at a center frequency of 2.5 GHz. At 2.5 GHz, the IIP3 is measured to be 7 dBm. Therefore, the output IP3 of the LNA is 20 dBm. The input 1-dB compression point of the LNA is measured to be −6 dBm after de-embedding the board loss.

C. Switching Time

The switching times for both transmit and Bluetooth® throws were measured at 2.5 GHz with an input power of +5 dBm, as shown in Fig. 13. The enable pin for the corresponding switch is triggered and the output of the switch is monitored on the scope. The turn-on time includes the delay and rise-times, while the turn-off time includes the delay and fall-times. The turn-on and turn-off times of the switch are dominated by the R-C time

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TABLE II
SUMMARY OF 2.4 GHZ CMOS SWITCHES

Freq	Switch	Tx IL (dB)	Iso (dB)	Linearity (dBm)	NF (dB)	Switching Time (ns)	Supply Voltage (V)	CMOS Tech (μm)	Ref
2.4 GHz	SP3T	1.3	28	33	3	350	3.3	0.18	This work
2.4 GHz	SPDT	1.5	32	28.5	-	-	1.8	0.18	[17]
2.4 GHz	SPDT	1.5	24	11	4.5	-	3.3	0.18	[22]
2.4 GHz	SPDT	1.1	20.6	20.6	-	-	1.8	0.18	[23]
2.4 GHz	SPDT	1.8	15	-	6	-	1.8	0.18	[24]
2.4 GHz	SPDT	0.4	30	30	5.5	150	1.2	0.09	[21]

constant of the circuit, which is determined by the dc blocking capacitor, gate-isolation resistor and the cross-biasing resistor. The turn-on time is measured to be 350 ns while the turn-off time is about 70 ns.

Table II compares the results of this work with state-of-the-art CMOS switches. It is noteworthy that a SP3T switch is expected to have higher insertion loss compared to SPDT, due to the off-state capacitance from the extra throw. The insertion loss of the SP3T switch presented in this work is better or comparable to most of SPDT designs at a similar technology node. The highest power handling and lowest NF is obtained due to the cross-biasing approach, the body isolation, the transistor stacking, and carefully optimized cascode topology for LNA, respectively. The reported NF for [21], [24] includes mixer and balun loss in the receive chain as well.

VII. CONCLUSION

We have presented a systematic approach for designing fully integrated, switch-LNA based front-end ICs for wireless applications in bulk CMOS technology. A detailed analysis of the switch and LNA design and topology tradeoffs has been presented. A cross-biasing approach is combined with the benefits of body isolation technique and transistor stacking to achieve transmit P_{1dB} greater than 33 dBm, while maintaining 1.3 dB insertion loss. The receive switch is cascaded with the LNA architecture which degrades the noise figure by 1.5 dB. The integrated switch-LNA achieves a total noise figure of 3 dB with moderate quality on-chip matching inductors and dc blocking. The fully integrated 802.11b/g/n solution includes on chip dc blocking capacitors, bypass-mode, matching network and hence, does not require any external components. The switch exhibits better than 28 dB isolation between transmit and Bluetooth® ports.

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