Solid State RF/Microwave Switch Technology: Part 2

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Introduction

In part 1 we discussed an overview of RF/microwave switch topologies, PIN diode theory of operation, and some simple PIN diode switch implementations. In part 2 we will discuss more complex PIN diode switches, the theory of operation of RF/microwave field effect transistors (FETs) -- with emphasis on the pseudomorphic high electron mobility transistor (pHEMT) -- and its implementation in RF/microwave switches. We will also describe criteria with which the relative advantages of PIN diode switches and pHEMT switches compare for specific types of applications.

Compound and Tuned Switches

In practice, it is usually difficult to achieve more than 40 dB isolation using a single PIN diode, either in shunt or series, at RF and higher frequencies. The causes of this limitation are generally radiation effects in the transmission medium, inadequate shielding and in some cases, the parasitic reactances of the diode's package. To overcome this, there are switch designs that employ combinations of series and shunt diodes (compound switches), and switches that employ resonant structures (tuned switches) affecting improved isolation performance.

The two most common compound switch configurations are PIN diodes mounted in either ELL (series-shunt) or TEE designs, as shown in Figures 1 and 2. In the insertion loss state for a compound switch, the series diode is forward biased and the shunt diode is at zero or reverse bias. The reverse is true for the isolation state. This adds some complexity to the bias circuitry in comparison to simple switches. A summary of formulas used for calculating insertion loss and isolation for compound and simple switches is given in Table 1.

It is important to note that the equations in Table 1 are valid only if the PIN diode presents a pure resistance when forward biased and a pure capacitive reactance when zero or reverse biased. This is not exactly the case for a practical packaged diode, since there is always some inductance present as well. The equations in Table 1 can be modified to apply to the general case by replacing R_S with the real part of the total impedance produced by the packaged diode, and by replacing C_T with the imaginary part of the packaged diode's total impedance.

Tuned Switches

A tuned switch may be constructed by spacing two series diodes or two shunt diodes a quarter wavelength apart, as shown in Figures 3 and 4. The resulting value of isolation in the tuned switch is twice that obtainable in a single diode switch. The insertion loss of the tuned series switch is higher than that of the simple series switch and may be computed using the sum of the diode resistance as the R_S value in Equation 8 of part 1 of this article. In the tuned shunt switch the insertion loss may even be lower than in a simple shunt switch because of a resonant effect of the spaced diode capacitances.

Quarter-wave spacing need not be limited to frequencies where the wavelength is short enough to install a discrete length of line. There is a lumped circuit equivalent which simulates the quarter wave section and may be used in RF band. This is shown in Figure 5. These tuned circuit techniques are effective in applications having bandwidths on the order of 10 percent of the center frequency.

Transmit-Receive Switches

There is a class of switches, commonly known as transmit-receive (T-R) switches, used in transceiver applications whose function is to connect the antenna to the transmitter (exciter) in the transmit state and to the receiver during the receiver state. When PIN diodes are used as elements in these switches, they offer higher reliability, better mechanical ruggedness and faster switching speed than electro-mechanical designs.

The basics circuit for one electronic T-R switch consists of a PIN diode connected in series with the transmitter, and a shunt diode connected a quarter wavelength from the antenna-TX-RX node, as shown in Figure 6.

When switched into the transmit state, each diode becomes

Skyworks, Con't on pg 38

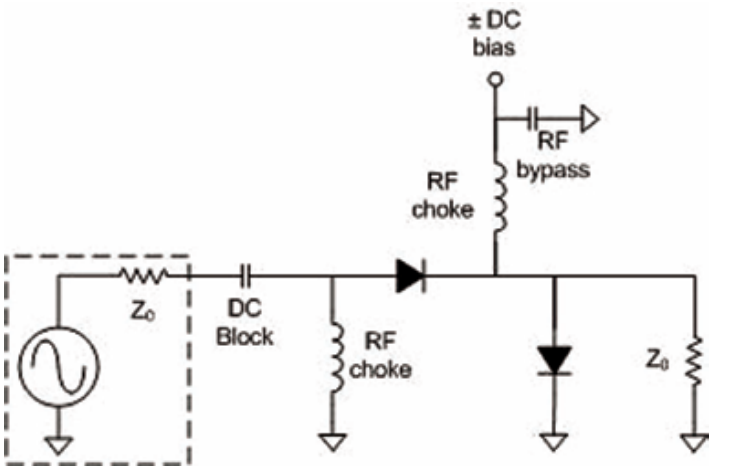

Figure 1: SPST with Series and Shunt Connected PIN Diodes

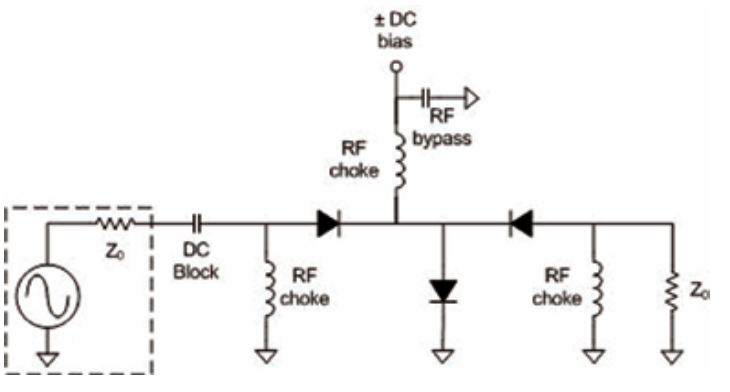

Figure 2: SPST with TEE-Connected PIN Diodes

Switch Type	Isolation	Insertion Loss
Series	$10\log_{10}\left[1+\frac{1}{(4\cdot\pi\cdot C\cdot Z_0)^2}\right]$	$20\log_{10}\left[1+\left(\frac{R_S}{2Z_0}\right)\right]$
Shunt	$20\log_{10}\left[1+\frac{Z_0}{2R_S}\right]$	$10\log_{10}\left[1+(\pi\cdot f\cdot C\cdot Z_0)^2\right]$
Series-shunt	$10\log_{10}\left[\left(1+\frac{Z_0}{2R_S}\right)^2+\left(\frac{X_C}{2Z_0}\right)^2\left(1+\frac{Z_0}{R_S}\right)^2\right]$	$10\log_{10}\left[\left(1+\frac{R_S}{2Z_0}\right)^2+\left(\frac{Z_0+R_S}{2X_C}\right)^2\right]$
TEE	$10\log_{10}\left[1+\left(\frac{X_C}{Z_0}\right)^2\right]+10\log_{10}\left[\left(1+\frac{Z_0}{2R_S}\right)^2+\left(\frac{X_C}{2R_S}\right)^2\right]$	$10\log_{10}\left[1+\left(\frac{X_C}{Z_0}\right)^2\right]+10\log_{10}\left[\left(1+\frac{Z_0}{2R_S}\right)^2+\left(\frac{X_C}{2R_S}\right)^2\right]$

Table 1: Summary of Formulae for SPST Switches

EX-1024
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.
001

Skyworks, Con't from pg 34

forward biased. The series diode appears as a low impedance to the signal heading toward the antenna, and the shunt diode effectively shorts the receiver's antenna terminals to prevent overloading.

Transmitter insertion loss and receiver isolation depend on the diode resistance. If R_S is 1 Ω, greater than 30 dB isolation and less than 0.2 dB, insertion loss can be expected. This performance is achievable over a 10 percent bandwidth. In the receive condition, the diodes are at zero or reverse bias and present essentially a low capacitance, C_T, which creates a direct low insertion loss path between the antenna and receiver. The off transmitter is isolated from this path by the high impedance series diode. The amount of power, P_A, this switch can handle depends on the power rating of the PIN diode, P_D, and the diode resistance, R_S. The equation showing this relationship is as follows for an antenna maximum SWR of σ:

$$P_A = \frac{P_D Z_0}{R_S} \times \left(\frac{\sigma + 1}{2\sigma}\right)^2$$

Equation 1

In a 50 Ω system in which the worst-case condition of a totally mismatched antenna must be considered, this becomes

$$P_A = \frac{12.5 \times P_D}{R_S}$$

Equation 2

The SMP1322-011LF is a surface mount PIN diode rated at 0.25 W dissipation to a 25°C contact. The resistance of this diode is a 0.50 Ω (max) at 10 mA. A quarter-wave switch using SMP1322-011LF may then be computed to handle 6.25 W with a totally mismatched antenna. It should be pointed out that the shunt diode of the quarter-wave antenna switch dissipates about as much power as the series diode. This may not be apparent from Figure 6; however, it may be shown that the RF current in both the series and shunt diode is practically identical.

Broadband antenna switches using PIN diodes may be designed using the series connected diode circuit shown in Figure 7. The frequency limitation of this switch results primarily from the capacitance of D2. In this case, forward bias is applied either to D1 during the transmit or D2 during the receive state. In high power applications (> 5 W) it may be necessary to apply reverse voltage on D2 during the transmit state. This may be accomplished either by a negative polarity power supply at Bias 2, or by having the forward bias current of D1 flow through resistor R to develop the required negative voltage.

The selection of diode D1 is based primarily on its power handling capability. It need not have a high voltage rating since it is always forward biased in its low resistance state when high RF power is applied. Diode D2 does not pass high RF current but must be able to hold off the RF voltage generated by the transmitter. It is primarily selected on the basis of its capacitance, which determines the upper frequency limit and its ability to operate at low distortion.

Using the SMP1322-011LF

Skyworks, Con't on pg 60

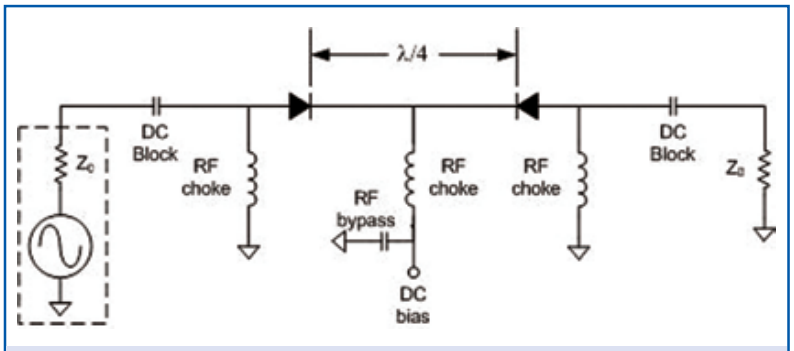

Figure 3: Quarter-Wavelength-Spaced Series PIN diode SPST

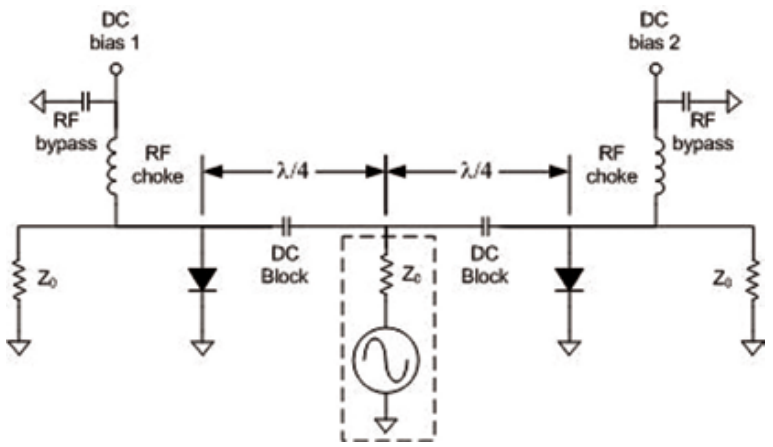

Figure 4: Quarter-Wavelength-Spaced Shunt PIN Diode SPST

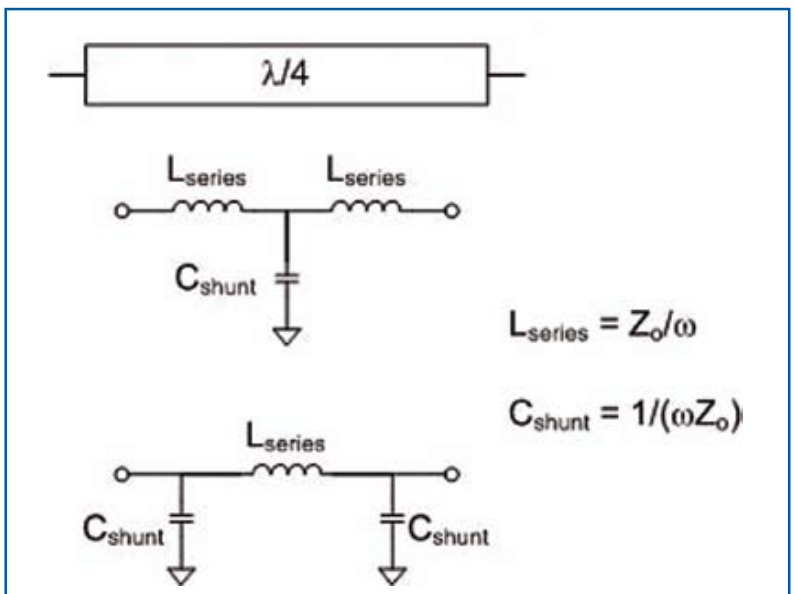

Figure 5: Lumped-Components Equivalent Circuits of a Quarter-Wavelength Transmission Line

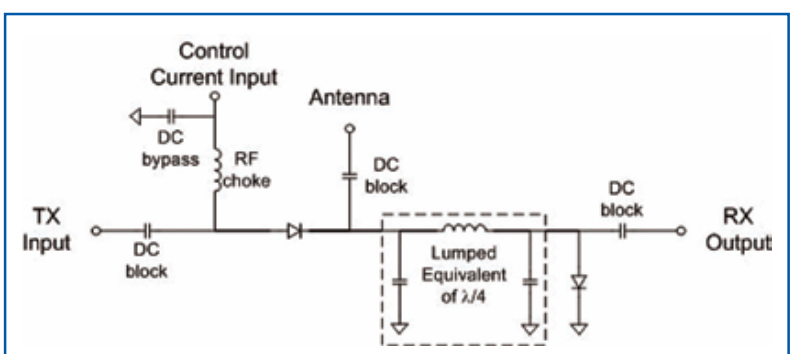

Figure 6: PIN Diode T-R Switch

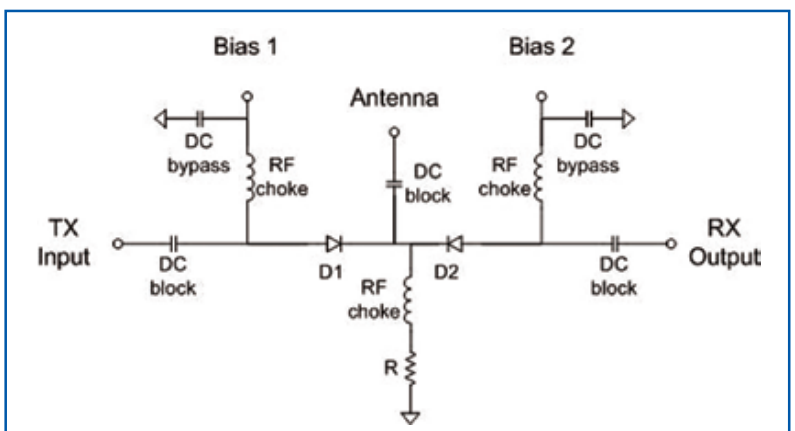

Figure 7: Broadband PIN Diode T-R Switch

EX-1024
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.
002

Skyworks, Con't from pg 38

for its low series resistance as D1, and an SMP1302-001LF for its low capacitance (rated at 0.3 pF maximum) and its thicker I layer (50 µm nominal) as D2, greater than 25 dB receiver isolation may be achieved up to 400 MHz. The expected transmit and receive insertion loss with the PIN diodes biased at 10 mA are 0.1 dB and 0.3 dB, respectively. This switch can handle RF power levels up to 6.25 W.

A Practical Design Hint

PIN diode circuit performance at RF frequencies is predictable and should conform closely to the design equations. RF/microwave modeling software can perform exacting simulations, but it is important to remember that the equations presented in this article and computer simulations have associated assumptions which may or may not be met by physical implementations of circuits. When a switch is not performing satisfactorily or as predicted in a real circuit, the fault is often not due to the PIN diode but to other circuit limitations -- such as circuit loss, inductance of printed circuit board vias, bias circuit interaction, or lead length problems -- especially when shunt PIN diodes are employed.

It is good practice in a new design to first evaluate the circuit loss exclusive of the PIN diode loss by substituting alternatively a wire short or open in place of the PIN diode. This will simulate the real circuit's performance with "ideal" PIN diodes. Any deficiency in the real circuit design and implementation may then be identified and corrected before inserting the PIN diodes.

GaAs pHEMT Switch Theory of Operation

The control field effect transistor (FET) or switching FET functions as a three port device, where the channel between source and drain ports forms a conduction path for the RF signal and the gate port, controls whether an RF signal is blocked or may pass. A DC control voltage applied between the gate and channel is required to create this function. Most control FETs use a depletion mode configuration, which means that the channel is normally in its low impedance state with no control voltage applied and in its high impedance, pinched off state when a negative voltage with respect to the channel is applied (thus the term "pinch off voltage"). See Figure 8.

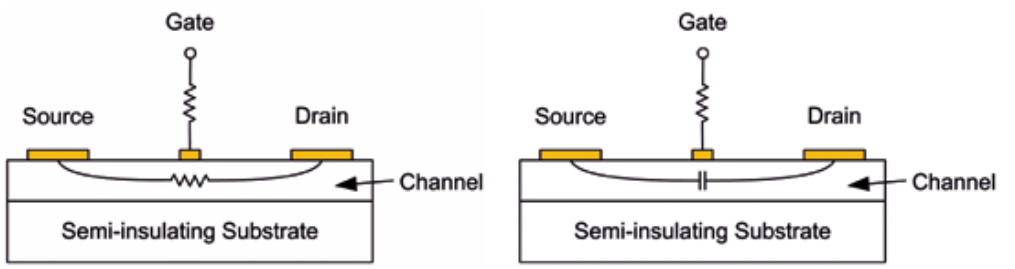

Figure 8: FET Equivalent Circuits – "On" and "Off" States

FET Switch Configurations

Figure 9 shows a single FET configured as a simplified single pole, single throw (SPST) switch. The first challenge in fabricating a switch using a GaAs FET is to isolate the DC gate control from the RF path. This is done by using a 5 kΩ to 10 kΩ resistor in series with the gate of the FET. This is a very simple bias network that has many advantages which will be discussed later. The next step is to DC block the RF source and drain ports using a capacitor with adequately low capacitive reactance at the desired frequency of operation. This creates an SPST switch. The insertion loss of the "ON" path of the switch will be affected by the channel resistance. Likewise the isolation of the "OFF" path is limited by the capacitance created by the source and drain spacing as well as FET physical size (periphery). Hence a balance of channel resistance (R_S) and off capacitance (C_{off}) must be met. The following equations show the relationship of the R_S and C_{off} as expressed in insertion loss (dB) and isolation loss (dB) for a single series FET SPST switch. The following is an example of a simple switch.

Assume the FET has the following characteristics: $R_S = 3\ \Omega$ and $C_{off} = 0.25$ pF ($X_C = 636\ \Omega$ at f = 1 GHz)

$$IL = 20\ log\left(1 + \frac{R_S}{2Z_0}\right) = 20\ log\left(1 + \frac{3}{2 \times 50}\right) = 0.257\ dB$$

where Z_0 is the system characteristic impedance (normally 50 Ω).

$$Isolation = 20\ log\left(1 + \frac{X_C}{2Z_0}\right) = 20\ log\left(1 + \frac{636}{2 \times 50}\right) = 17.34\ dB$$

Note: These equations are good first order approximations and are not intended for modeling purposes. As is the case with PIN diodes, the FET's parasitic reactances -- including inductive reactance -- must be considered in a rigorous analysis of insertion loss and isolation.

Applying the values of 3 Ω and 0.25 pF would result in an insertion loss of 0.257 dB and an isolation of 17.34 dB at 1 GHz. However if the frequency is lowered to 100 MHz then an isolation of 36.2 dB is achieved. This is due to the fact that the isolation of the series FET is a result of its capacitive reactance which is frequency dependent, an important feature when selecting FET parameters.

To improve the isolation at higher frequencies, a shunt FET can be used following the series FET. In this position the FET must be "ON" in order to increase isolation and "OFF" to put it in the insertion loss state. This requires two separate control voltages for the switch. See Figure 10.

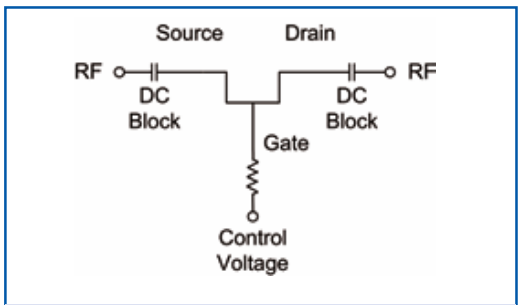

Figure 9: Single-FET SPST Switch

The resulting isolation would be an additional 19.4 dB. Since the shunt FET has no appreciable reactive component when it is biased to its "ON" state, isolation will stay relatively unchanged over frequency. Note: Again this equation provides a good approximation of the shunt FET additional isolation, assuming ideal conditions. Phase length, ground coupling, etc., will impact actual results.

The negative gate voltage required for this switch can be viewed as a drawback, since in most applications only positive voltage supplies are available. Also in this series/shunt configuration one FET must be "ON" while the other FET is "OFF". A solution to this problem is the addition of two capacitors applied to the shunt FET which provide DC blocks to the RF path and allow the gate port of the shunt FET to be grounded. An additional reference voltage port must also be added (see Figure 11.) This technique also allows for a single positive voltage to be applied to the switch. The selection of the capacitor value is critical to insure proper frequency operation and bandwidth. The values can be quite small (5 to 15 pF), since the series FET can provide most of the isolation at the lower frequencies.

This SPST switch is reflective, which means that the output when in the isolation state will have a substantial VSWR. A class of switches, known as "matched" or "absorptive" will terminate the output into a 50 Ω load when switched to the isolation state (see Figure 12).

A good example of a single throw switch is the AS130-73LF which is reflective on

Skyworks, Con't on pg 62

EX-1024
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.
003

Skyworks, Con't from pg 60

one port and absorptive on the other port. Since the switch is reciprocal, either port can be input or output giving the designer flexibility in their application.

Power Handling Capabilities

FET based devices can handle several Watts while consuming very little D.C. current. This feature is very attractive for mobile applications with handsets having the largest market opportunity for switches. The "ON" condition of the FET can handle typically more power than the "OFF" state. This is due to the voltage breakdown (V_B) created by gate/source and gate/drain spacing limitations. A simple way to rationalize this is to compare the "ON" limitation being channel current (I_{dss}), which can be increased significantly by making the channel wider. This can be done by adding periphery to the FET, however if the gate spacing is increased significantly the R_S becomes greatly affected and a significant loss penalty will result. A way to overcome voltage limitation is by adding FETs in series (see Figure 13). Doing so distributes the voltage across many FETs and thus reduces the voltage on the individual devices. This technique can increase power handling quite significantly. The SKY13290-313LF is a good example of this feature. This SPDT can handle 10 Watts with only 0.1 dB of compression. Another way of distributing voltage is by using multi gate FETs. Double and triple gates are commonly used, especially in applications where small size and cost are critical. This stacking of the FETs is not only beneficial for the series devices but also for the shunt FETs as well.

When using FETs at low frequencies, it must be noted that power handling will be reduced. To understand this effect, let's use our example FET device that has an "OFF" capacitance of 0.35 pF and a 5k Ω gate bias resistor. This FET will have a capacitive reactance of 454 Ω at 1.0 GHz. Since the gate resistance is much higher (by a factor of 10) it remains isolated. However, at 100 MHz the capacitive reactance is now 4540 Ω and is almost the same magnitude as the resistance of the gate resistor; at 1 MHz the reactance is significantly higher. Now the gate is no longer isolated and will result in distortion, or worse, RF failure. Figure 14 illustrates this effect. Increasing the value of the gate resistor will help, however, switching speed will be compromised. As significant, fabricating large resistor values will require more die area and thus is not recommended. Also large value resistors will display their own non linear characteristics, since they are created using very small geometries.

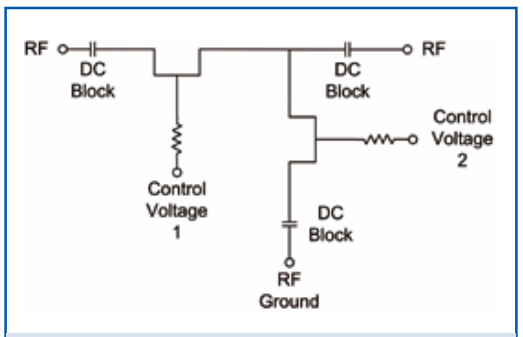

Figure 10: Series/Shunt FET SPST

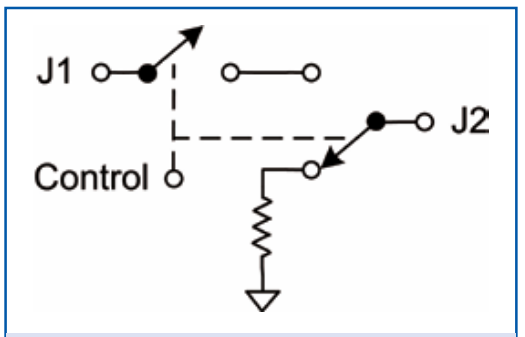

Figure 12: Absorptive SPST Switch

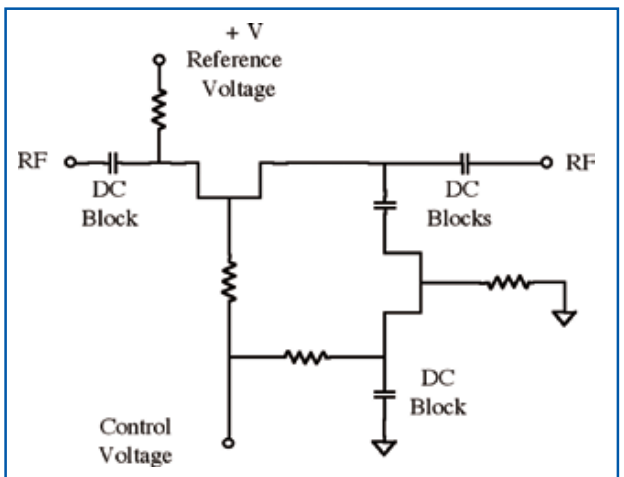

Figure 11: Single Positive Voltage Control SPST

Now that a SPST switch has been created, this function can be duplicated to form two throw, three throw, and even four throw switches without altering the basic series/shunt configuration. To go beyond a SP4T does require much more optimization in the FET selection as well as blocking capacitor and bias resistor values and even circuit topologies. Figure 15 shows a typical SP2T switch using dual control. Single control is possible, but has a drawback since an additional series capacitor needs to be added to one of arms resulting in a loss imbalance. A good example is the AS179-92LF. When designing multi throw switches a lot of attention must be focused on the capacitive size of the first series FET at the common junction. Too small will result in high insertion loss due to the high Rs in the "ON" state. Too large will impact isolation and poor VSWR. Therefore, a careful tradeoff must be met for optimum performance. The SKY13277-355LF is a good example of a SP3T while the SKY13296-340 LF is a solid performing high isolation SP4T. Both switches are absorptive and low insertion loss, less than 1.2 dB at 1.0 GHz.

PIN vs. FET Switches – Which One to Use?

PIN diodes and FETs have relative advantages and disadvantages to each other for use in switching applications. The performance attributes which should be compared when the selection of one of these technologies is undertaken are more numerous than one might think at first glance. Table 2 lists the foremost of these attributes, but is by no means intended to be complete.

"Integratability"

The wafer processing required for modern FET structures such as pHEMTs is largely lateral with respect to the top surface of the wafer; it lends itself quite well to the inclusion of passive component structures -- such as metal-insulator-metal (MIM) capacitors, spiral inductors, and thin film resistors -- all of which can be formed on or near the top-most layer of the wafer. The bottom-most layer of a FET wafer is semi-insulating material, which inherently isolates one FET structure from another. In comparison, PIN diode wafer processing is vertical with respect to the top surface of the wafer; the majority of the physical thickness of a PIN diode wafer is the cathode of the diode. It is very difficult to isolate the cathodes of PIN diodes that are on the same die. Consequently, with the exception of common-cathode pairs of PIN diodes, they are inherently discrete devices.

Power Handling

The vertical structure of a PIN diode is a relative advantage for power handling. The heat that is generated by Joule heating within the I layer of the diode can easily be conducted downwards through the diode's cathode layer to the system heat sink. RF FET structures such as pHEMTs and MESFETs are typically fabricated from III-V materials, such as GaAs, that has lower thermal conductivity than Si, which is the material utilized for most switching PIN diodes.

Switching Time

The FET is a majority carrier device whose drain-source impedance is con-

Skyworks, Con't on pg 66

EX-1024
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.
004

Skyworks, Con't from pg 62

trolled by the thickness of a depletion layer that extends into the channel from the gate-source interface. The thickness of this depletion layer can be modulated very rapidly in response to a change in the gate-source control voltage. By contrast, a PIN diode stores minority carriers in its I layer when it is under forward bias. These charge carriers must be primarily conducted out of the I layer to change its impedance from low to high. This process is inherently slower than the change in drain-source impedance for a pHEMT or MESFET device.

Control Current

The FET is a voltage-controlled device. In a practical pHEMT or MESFET, the only current that flows into the control port of the transistor is the reverse leakage current of the gate-source junction, which is very small, typically less than 10 microamps. On the other hand, a PIN diode can require a significant injection of charge carriers into its I layer to lower its impedance to the required level. The typical bias current for a PIN diode in a switch is 10 to 20 milliamps.

Distortion Performance

The PIN diodes produce nearly ideal, very linear series resistance when the amount of charge in its I layer -- as a result of DC forward bias current -- is at least ten times that of the charge that is alternately injected and removed by the RF signal. When the diode is non-conducting, it presents a very high resistance in parallel with its junction capacitance. This junction capacitance is independent of applied voltage for signals with sufficiently high frequency (typically greater than 100 MHz). Consequently, the PIN diode produces excellent distortion performance.

An FET structure responds very quickly to the magnitude of its applied gate-source voltage, because the gate-source junction in a MESFET and a pHEMT structure is a Schottky diode. The Schottky diode's very nonlinear impedance with respect to applied bias conditions can be a comparatively efficient distortion generation mechanism, which results in input third order intercept for a FET switch that is roughly an order of magnitude or more lower than that of a PIN diode switch.

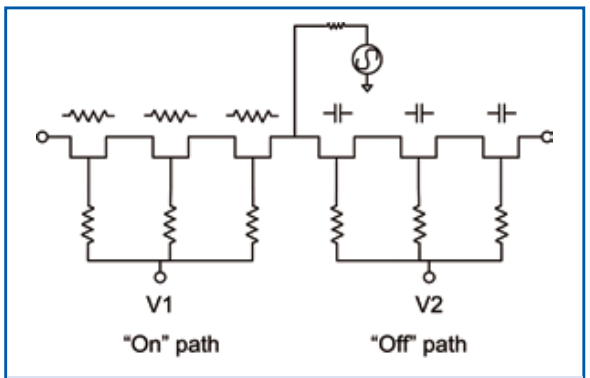

Figure 13: High Power SPDT Switch

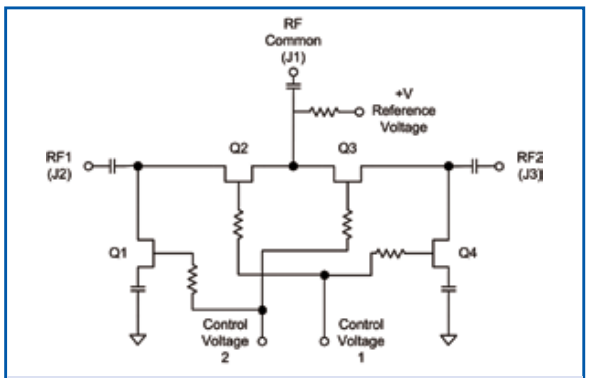

Figure 15: Single Pole Two Throw Switch

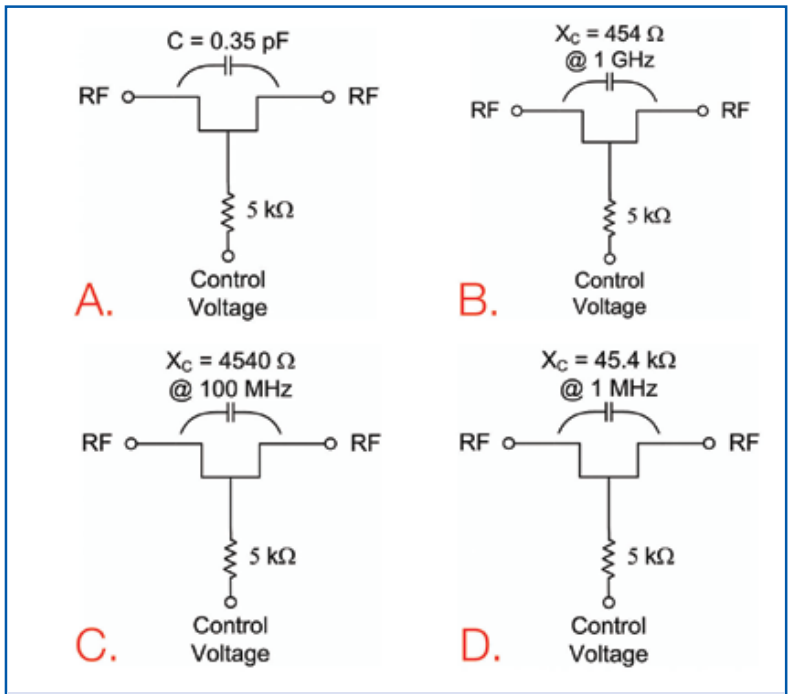

Figure 14a Series "Off" FET; 14b: Reactance of Series "Off" FET at 1 GHz; 14c: Reactance of Series "Off" FET at 100 MHz; 14d: Reactance of Series "Off" FET at 1 MHz

Conclusion

RF switches may comprise PIN diodes or FET structures such as MESFETs and pHEMTs. These two approaches to the design of the switch offer advantages and disadvantages. A PIN diode switch typically can handle greater power and produce less distortion, at the expense of longer switching time and much larger control current requirements. The very low bias current needs of MESFET and pHEMT switches makes them very well suited for battery powered applications. These devices can also be integrated into complex, multi-throw integrated circuit switches. These relative advantages for what would appear to be competing technologies, assures a bright future for them both.

Table 2: Comparison of Attributes for PIN Diodes and FETs for Switching Applications

Attribute	PIN Diode	FET
"Integratability" with other components	Poor	Excellent
Power handling	Very high (to greater than 1 kW CW)	Moderate (10 W CW or less)
Switching time	A few tens of nanoseconds to several microseconds	Tens to a few hundred of nanoseconds
Control current	Up to 100 milliamps	Less than 100 microamps
Distortion performance	Input third order intercepts in the +45 dBm or higher range	Input third order intercepts in the +30 to low +40's dBm range

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EX-1024
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.
005