

Single-Pole Double-Throw CMOS Switches for 900-MHz and 2.4-GHz Applications on p⁺ Silicon Substrates

Feng-Jung Huang, *Member, IEEE*, and Kenneth K. O, *Member, IEEE*

Abstract—A 900-MHz single-pole double-throw (SPDT) switch with an insertion loss of 0.5 dB and a 2.4-GHz SPDT switch with an insertion loss of 0.8 dB were implemented using 3.3-V 0.35- μm NMOS transistors in a 0.18- μm bulk CMOS process utilizing 20- $\Omega\cdot\text{cm}$ p^- substrates. Impedance transformation was used to reduce the source and load impedances seen by the switch to increase the power handling capability. SPDT switches with 30- Ω impedance transformation networks exhibit 0.97-dB insertion loss and 24.3-dBm output $P_{1\text{ dB}}$ when tuned for 900-MHz operation, and 1.10-dB insertion loss and 20.6-dBm output $P_{1\text{ dB}}$ when tuned for 2.4-GHz operation. The 2.4-GHz switch is the first bulk CMOS switch which can be used for 802.11b wireless local area network applications.

Index Terms—CMOS integrated circuits, impedance matching, microwave switches, MOSFET switches.

I. INTRODUCTION

RECENT studies have shown that it is feasible to implement radio-frequency (RF) single-pole double-throw (SPDT) switches operating at 900 MHz in 0.5- μm CMOS technologies using p^+ substrates (with a p^- epitaxial layer) [1]. Insertion loss of 0.8 dB and 1-dB power compression point ($P_{1\text{dB}}$) of ~ 18 dBm have been achieved [1]. The insertion loss is ~ 0.3 dB higher and $P_{1\text{dB}}$ is ~ 10 dB lower than those of commercially available transmit/receive (T/R) switches [2]–[4]. It has also been shown that RF components and circuits implemented on 10- $\Omega\cdot\text{cm}$ p^- substrates exhibit superior characteristics than those fabricated on p^+ substrates [5]. However, using a p^- substrate might increase insertion loss of integrated RF switches due to increased substrate resistances [6]. To examine the impact of this and the possibility of lowering insertion loss at 900 MHz, as well as applicability of CMOS SPDT switches at frequencies above 900 MHz, SPDT RF switches were fabricated using 3.3-V 0.35- μm MOS transistors in a foundry 0.18- μm CMOS process utilizing 20- $\Omega\cdot\text{cm}$ p^- substrates. Furthermore, to enhance power handling capabilities ($P_{1\text{dB}}$), uses of impedance transformation as well as their effects on isolation and insertion loss have been investigated. Through these efforts, 900-MHz and 2.4-GHz CMOS SPDT

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F.-J. Huang is with Maxim Integrated Products, Inc., Boston Design Center, North Chelmsford, MA 01863 USA (e-mail: fjj@ieee.org).

K. K. O is with the Department of Electrical and Computer Engineering, Silicon Microwave Integrated Circuits and Systems Research Group, University of Florida, Gainesville, FL 32611 USA.

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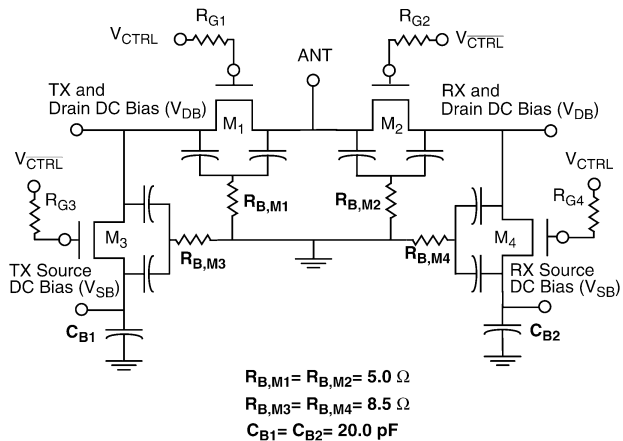


Fig. 1. Circuit schematic of an SPDT RF switch including key substrate resistances. (R_B : substrate resistance).

switches achieving low insertion loss with $P_{1\text{dB}}$ greater than 20 dBm have been demonstrated [7].

This paper consists of four sections, including this introduction section. The basic switch design and impedance transformation as well as the measurement results are presented in Sections II and III. Finally, this work is summarized in Section IV.

II. DESIGN OF RF SWITCH

Key figures of merit of an RF switch are insertion loss and $P_{1\text{ dB}}$. Transistor on-resistance is one of the dominant factors determining insertion loss (IL). Because of this, only n-channel MOS transistors are utilized in the design. The drain-to-body and source-to-body junction capacitances (C_{DB} and C_{SB}) of the transistors, and the associated parasitic resistances (R_{B}) due to the conductive nature of bulk silicon substrates are also critical factors determining insertion loss [1]. Fig. 1 is a schematic of an SPDT RF switch including critical substrate resistances. The widths of $M_{1,2}$ have been chosen to be $660\text{ }\mu\text{m}$ to minimize IL at 900 MHz. Compared to the previously reported 900-MHz switch [1], this switch has wider $M_{1,2}$ with lower on-resistance. This is critical to achieve low IL especially when impedance transformation networks (Section III) are added to the same switch core. If the on-resistance is not lowered, due to the reduced source/load impedances with impedance transformation, the IL could be high. The width of $M_{3,4}$ is $330\text{ }\mu\text{m}$. This width is chosen to improve isolation without noticeable degradation on

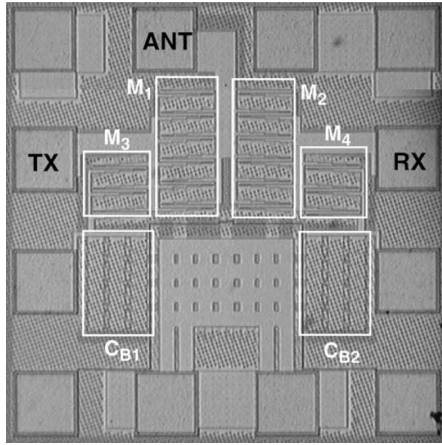


Fig. 2. Microphotograph of the 0.35- μm 900-MHz SPDT switch.

insertion loss. This switch also integrates two 20-pF capacitors, C_{B1} and C_{B2} , which allow dc biasing of the TX and RX nodes of the switch. By applying the same dc voltage on the top plates of the bypass capacitors, C_{B1} and C_{B2} , as the dc voltage for TX and RX nodes, dc power consumption is made negligible, while the insertion loss and power handling capability of the switch are improved [6].

Fig. 2 is a microphotograph of the 0.35- μm SPDT switch. To increase the maximum allowed voltage swing and thus $P_{1\text{ dB}}$, 0.35- μm CMOS transistors in a 0.18- μm CMOS process are chosen to implement the SPDT switches instead of the 0.18- μm MOS transistor even though the insertion loss can be lowered by using the transistors with smaller feature size at the frequencies of interest [8], [9]. Using 0.35- μm transistors in the 0.18- μm process instead of those in a 0.35- μm process also reduces the source/drain-to-body capacitances because of the more aggressive design rules, which in turn decreases substrate loss and insertion loss. The die area is $531 \times 531 \mu\text{m}^2$. Substrate contacts have been carefully laid out to ensure the impact of p^- substrates on IL is reduced. The measured substrate resistances of 5.0Ω for $R_{B,M1} = R_{B,M2}$ and 8.5Ω for $R_{B,M3} = R_{B,M4}$ are sufficiently low to make the substrate loss small. The low substrate resistances are achieved by fully surrounding the transistors with large area p^+ substrate contacts and filling in any open spaces with substrate contacts. Approximately, 63% of the die area is occupied by substrate contacts to reduce the substrate resistances. The resistances are measured using a test circuit identical to the switch except that the source/drain-to-body junctions are replaced with p^+ substrate contacts [10].

Fig. 3 shows the measured insertion loss, return loss and isolation of the 900-MHz switch without impedance transformation. Table I summarizes the measured characteristics of the switch near 900 MHz. The switch was packaged in an SOIC-like test package with an exposed paddle shown in Fig. 4. IL is about 0.5 dB, return loss is more than 15 dB, and isolation is more than 39 dB for operating frequencies up to 1 GHz at V_{CTRL} or $V_{\text{GB}} = 6.0 \text{ V}$, and drain/source-to-body reverse bias (V_{DB} and V_{SB}) of 3.0 V. The IL for the 0.35- μm SPDT switch is 0.3 dB lower than that of the 0.5- μm bulk CMOS 900-MHz SPDT switch [1]. The 0.5-dB IL is excellent. When $V_{\text{CTRL}} = 6.0 \text{ V}$

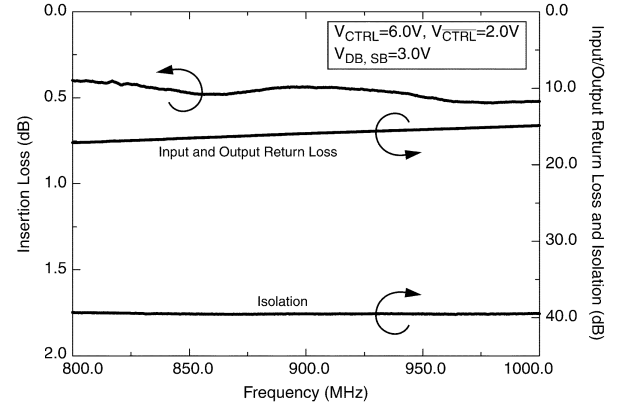


Fig. 3. Measured insertion loss, on-state return loss and isolation of the 0.35- μm 900-MHz SPDT switch.

TABLE I
SUMMARY OF 0.35- μm SPDT SWITCH CHARACTERISTICS WITH AND WITHOUT IMPEDANCE TRANSFORMATION NETWORKS (ITN)

	0.5- μm SPDT Switch [1]	0.35- μm SPDT Switch	0.35- μm SPDT Switch with 900-MHz ITN	0.35- μm SPDT Switch with 2.4-GHz ITN
Frequency (MHz)	928	928	928	2490
Insertion Loss (dB)	0.73	0.46	0.97	1.10
Isolation (dB)	41.3	39.5	35.4	20.6
$P_{1\text{ dB}}$ (dBm)	17.2	17.7	24.3	20.6
IP_3 (dBm)	38.2	40.1	37.7	29.8

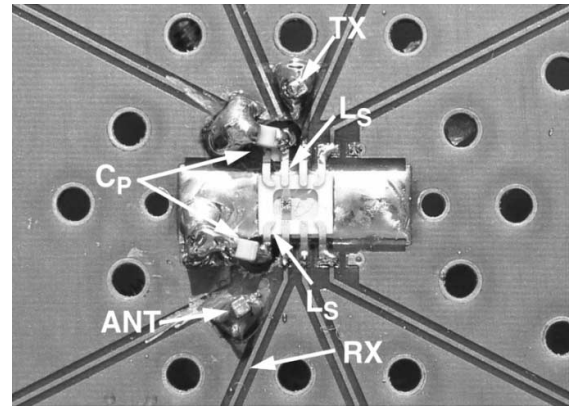


Fig. 4. Photograph of the test fixture for the 0.35- μm RF switch with 2.4-GHz impedance transformation networks.

and $V_{\text{CTRL}} = 2.0 \text{ V}$, TX and ANT nodes are connected (see Fig. 1), and output $P_{1\text{ dB}}$ is 17.7 dBm. The compression point is limited by turning on of transistor M_3 when an RF voltage with an amplitude larger than 2.7 V is applied due to the voltage divider formed by C_{GD} , C_{GS} , and C_{GB} of M_3 . The measured output third-order intercept point (IP_3) is 40.1 dBm, which is excellent. The measured third-order intermodulation products (IM3) for this switch deviate from the slope of 3 at the input power levels of $\sim 5 \text{ dB}$ below the input $P_{1\text{ dB}}$ point and above. The bias and control voltages, V_{CTRL} , V_{CTRL} , V_{DB} , and V_{SB} ,

are chosen for optimum insertion loss and $P_{1\text{dB}}$, as well as for long-term reliability [6]. The 6.0-V V_{CTRL} can be attained by using a voltage doubler [11], [12].

Another switch for operation up to 2.5-GHz without impedance transformation is also implemented in the same process [13]. As mentioned, the width of transistors M_1 and M_2 is a crucial factor determining insertion loss. Under a given bias condition, as the transistor width is increased, on-resistance decreases and insertion loss decreases. However, if the transistor width is excessively increased, the signal loss through capacitive coupling to the substrate becomes significant and insertion loss increases with the increasing width [6]. This is especially important for high-frequency applications. The minimum insertion loss at 2.4 GHz is achieved when the widths of $M_{1,2}$ and $M_{3,4}$ are about 300 and 100 μm , respectively. For this switch, the measured substrate resistances are 8.2 Ω for $R_{B,M1} = R_{B,M2}$ and 20.0 Ω for $R_{B,M3} = R_{B,M4}$.

Fig. 5 shows the measured insertion loss, return loss, and isolation of the 2.4-GHz switch. Insertion loss is about 0.8 dB, return loss is more than 19 dB, and isolation is more than 24 dB for operating frequencies up to 2.4 GHz at V_{CTRL} or $V_{\text{GB}} = 6.0$ V, and drain/source-to-body reverse bias (V_{DB} and $V_{\text{SB}} = 3.0$ V. Fig. 6 shows the power measurement results of the switch at 2.4 GHz. When $V_{\text{CTRL}} = 6.0$ V and $V_{\text{CTRL}} = 2.0$ V, TX and ANT nodes are connected, output $P_{1\text{dB}}$ is 17.4 dBm.

III. IMPEDANCE TRANSFORMATION

To enhance power-handling capabilities of switches, the GaAs community has utilized techniques such as multiple series transistors for the shunt arm of the transmitting path and the series arm of the receiving path [14], [15], and LC resonant switches [16] in order to reduce the voltage drop across drain-to-gate, V_{GD} , and drain-to-source, V_{DS} , of a transistor. For bulk CMOS switches, in addition to the similar factors limiting the power handling capability of GaAs FET-based switches, due to the conductive nature of silicon substrates, maintaining reverse bias across source/drain-to-substrate junctions (i.e., V_{SB} and V_{DB}) is a critical factor. Forward biasing the junctions can limit $P_{1\text{dB}}$ as well as trigger latchup [17]. In addition, the voltage across the gate oxide of the transistors should not exceed the time-dependent dielectric-breakdown (TDDb) limitations to prevent degradation of the long-term reliability. The voltage limit set by these requirements is usually lower than the transistor breakdown voltage, BV_{DSS} , and gate-to-drain breakdown voltage, BV_{GD} . Because of this, using multiple series transistors will result only marginal improvement of power handling capability. Use of resonant switches is problematic for CMOS switches operating in the 1–2 GHz frequency range due to higher on-resistance of MOS switches compared to GaAs FETs and low quality factors of integrated inductors. Because of these, impedance transformation networks (ITNs) were utilized to reduce the source and load impedances seen by the switches to increase the power-handling capability.

In order to deliver higher than 20 dBm of power to a 50- Ω antenna, the peak-to-peak voltage swing at the antenna must be about 6.3 V. This voltage swing is higher than the voltage swing

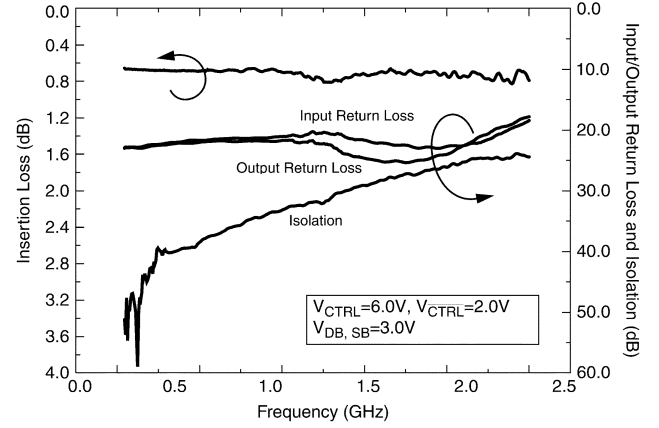


Fig. 5. Measured insertion loss, on-state return loss, and isolation of the 0.35- μm 2.4-GHz SPDT switch.

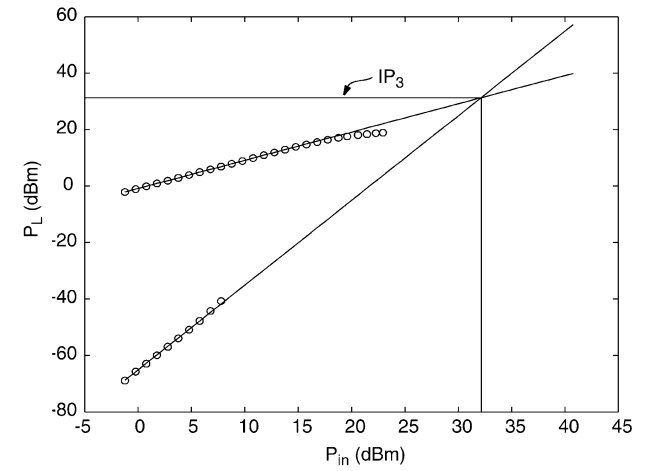


Fig. 6. The output 1-dB compression point measurement and IP_3 measurement when $V_{\text{CTRL}} = 6.0$ V, $V_{\text{CTRL}} = 2.0$ V and $V_{\text{DB}} = V_{\text{SB}} = 3.0$ V at 2.4 GHz.

at the $P_{1\text{dB}}$ points of the switches presented in the previous section. In addition, this voltage swing is potentially too high to guarantee long-term reliability. As discussed earlier, a technique to overcome these limitations is using impedance transformations to convert 50- Ω source/load impedances (Z_S and Z_L) to approximately $Z = (50 \Omega / [6.3 / (2X)]^2)$, where X is the maximum amplitude of the signal that can appear at the TX node of the switch without being significantly distorted. Assuming insertion loss of a switch is negligible, the voltage amplitude of X at the input of the switch would result in delivering 20 dBm of power to the load when the transformed impedance is Z . As will be discussed shortly, it is important to keep Z or X to be reasonably high in order to reduce the degradation of IL associated with utilizing impedance transformation.

The largest voltage amplitude that could appear at the TX node of the switch, X in the previously discussed impedance equation, is about 2.7 V, which limits the $P_{1\text{dB}}$ of the 0.35- μm switches without ITNs, as mentioned in Section II. To add some margin, X of 2.5-V is used to determine the transformed source/load impedances. For a 2.5-V RF signal amplitude at the output of the switch, the load impedance seen by the transistor

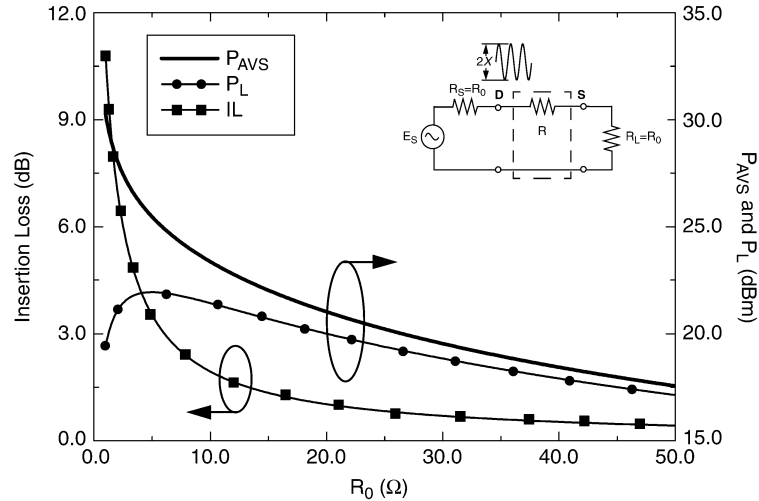


Fig. 7. P_{AVS} , P_L , and insertion loss versus the transformed source/load impedances (R_0) for the two-port network shown in the figure with a $5\text{-}\Omega$ R .

should be reduced to about $30\text{ }\Omega$ or less to achieve more than 20-dBm $P_{1\text{dB}}$. The $30\text{-}\Omega$ transformed impedance can be obtained by using a shunt C-series L network or a shunt L-series C network. The shunt C-series L network is preferred due to the fact that bondwire and package lead inductances present in a packaged SPDT switch can be more readily incorporated into the network.

The use of impedance transformation networks unfortunately increases the insertion loss of the switch due to the loss of capacitors and inductors used in the network, and due to the reduced source/load impedances seen by the switch. Thus, high quality factor (Q) inductors and capacitors are needed for the network to minimize the extra insertion loss introduced by the impedance transformation network. Generally, integrated inductors on bulk silicon substrates have low Q at 1 GHz [18], [19], and discrete off-chip inductors, and as mentioned, bondwire and package lead inductances are more suitable. If the source/load impedance is excessively transformed to a low value which is comparable to the on-resistance of the transistors, insertion loss can be greatly increased. For a two-port resistive network, shown in Fig. 7, insertion loss in decibels can be obtained from $1/|S_{21}|^2$

$$IL = 20 \times \log \left| \frac{2R_0 + R}{2R_0} \right| = 20 \times \log \left| \frac{2 + (R/R_0)}{2} \right|. \quad (1)$$

This IL expression clearly illustrates that for a given insertion loss, if R_0 is scaled, on-resistance R must be scaled along with R_0 . Because of this, the switch transistors need to have a wider width than that of the previously reported switches [1], [13]. P_{AVS} , P_L and insertion loss are plotted in Fig. 7 against the transformed source/load impedances (R_0). R of $5\text{ }\Omega$ is used to generate this plot. As shown in Fig. 7, when R_0 decreases, P_L increases and insertion loss also increases. However, if R_0 is transformed below R ($5\text{ }\Omega$ in this case), P_L decreases even though P_{AVS} is increased. This is due to the sharp increase of insertion loss and thus degrading the power handling capability of the network. In this analysis, the 22.0-dBm maximum P_L can be achieved when $R_0 = R = 5\text{ }\Omega$ ($IL = 3.5\text{ dB}$) with a P_{AVS}

of 25.5 dBm . However, the 3.5-dB insertion loss is high for an RF T/R switch. From (1), R_0 should not be lower than $20\text{ }\Omega$ for the $5\text{-}\Omega$ resistive network to maintain IL lower than 1 dB . The maximum $P_{1\text{dB}}$ that can be achieved while satisfying the less than 1-dB IL requirement is about 20 dBm in this case.

Fig. 8 shows simulated and measured IL and $P_{1\text{dB}}$ versus the transformed Z_S and Z_L of the 900-MHz $0.35\text{-}\mu\text{m}$ switch in a $50\text{-}\Omega$ system. The switch with ITN's is also shown in the figure. The switch core is represented as a two-port network. R_S and R_L are $50\text{-}\Omega$ source and load impedances, and Z_S and Z_L are the transformed source and load impedances seen by the switch. L_S 's and C_P 's are components for impedance transformation. For clarity, the bondwire and package lead inductances which are about 2.0 to 2.5 nH are included as part of L_S 's. As shown in the simulation, Z_S and Z_L should be higher than $30\text{ }\Omega$ to maintain IL less than 1 dB . The maximum $P_{1\text{dB}}$ that can be achieved while satisfying the IL less than 1-dB requirement is about 23.5 dBm . When Z_S and Z_L are further decreased, IL increases and $P_{1\text{dB}}$ also increases. If Z_S and Z_L are excessively lowered, a sharp increase of IL can actually decrease $P_{1\text{dB}}$. Using this switch, the highest $P_{1\text{dB}}$ of 26.6 dBm can be obtained when Z_S and Z_L are transformed to about $10\text{ }\Omega$. Again, the corresponding 2.6-dB IL is high. Thus, in order to maintain less than 1-dB IL with more than 20-dBm $P_{1\text{dB}}$, Z_S and Z_L should not be lower than $\sim 30\text{ }\Omega$ when using this particular MOS switch core.

To transform the $50\text{-}\Omega$ R_S and R_L to $30\text{-}\Omega$ Z_S and Z_L at 900 MHz , the required C_P and L_S are 2.8 pF and 4.4 nH , respectively. However, in order to properly transform the source/load impedance, the parasitic inductance and capacitance of SMA connectors used to connect RF cables to the test fixture need to be taken into account. An SMA connector used in this work can be represented by a series inductor followed by a shunt capacitor. The extracted series inductance and shunt capacitance from measurements are about 2.2 nH and 1.0 pF , respectively. In order to obtain Z_S and Z_L of $30\text{ }\Omega$ including the parasitics of SMA connectors, a 5.3-nH L_S and a 2.8-pF C_P are needed. A 3.3-nH off-chip inductor in series with the bondwire and package lead

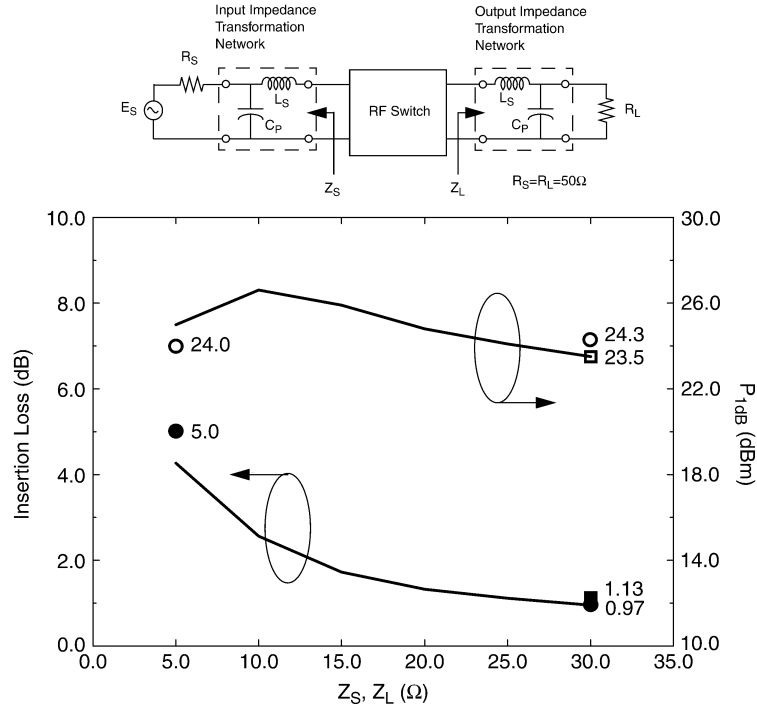


Fig. 8. Simulation and measured results of insertion loss and $P_{1\text{dB}}$ versus the transformed Z_S and Z_L of the 0.35- μm 900-MHz switch. The block diagram of the switch with impedance transformation networks is shown. Measured data are plotted using symbols.

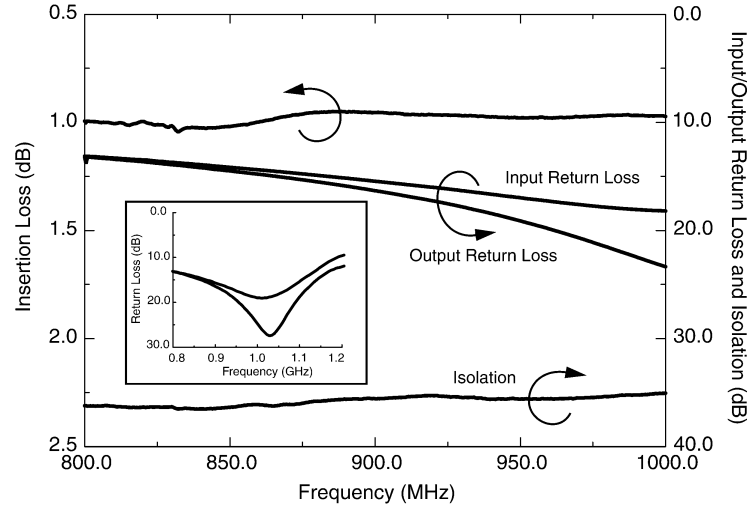


Fig. 9. Measured insertion loss, on-state return loss, and isolation for the 0.35- μm RF switch with 900-MHz 30- Ω Z_S and Z_L impedance transformation networks. Return loss is also plotted in a wider bandwidth to show the tuned responses.

inductances and a 2.7-pF off-chip capacitor are used to implement the transformation network. The choice of L_S is about 0.6 nH higher than the estimated 4.7 nH in order to compensate the ~ 0.7 -pF C_{DB} 's of M_1 and M_3 at the TX node and C_{SB} 's of M_1 and M_2 at the ANT node of the SPDT switch.

Fig. 9 shows the measured insertion loss, return loss, and isolation of the switch with impedance transformation networks. The measured insertion loss is less than 1 dB, return loss is more than 14 dB, and isolation is more than 35 dB for frequencies between 860 MHz and 1 GHz. At 928 MHz, the measured IL is 0.97 dB, return loss is more than 16.3 dB, and isolation

is 35.4 dB. Fig. 10 shows P_L versus P_{in} plots for the switch. When $V_{\text{CTRL}} = 6.0$ V and $V_{\text{CTRL}} = 2.0$ V, or when TX and ANT nodes are connected, output $P_{1\text{dB}}$ is 24.3 dBm and $\text{IP}_{1\text{dB}}$ (input referred $P_{1\text{dB}}$) is 26.3 dBm. The measured output IP_3 is 37.7 dBm and IIP_3 (input referred IP_3) is 38.7 dBm. Output $P_{1\text{dB}}$ is increased from 17.7 to 24.3 dBm with a less than 0.5-dB increase of IL.

IP_3 is higher than 10 dB above $P_{1\text{dB}}$. This is due to the fact that the mechanisms determining IP_3 and $P_{1\text{dB}}$ are different in a switch. IP_3 is measured at low input power levels and is mainly determined by the nonlinearity of the reverse-bi-

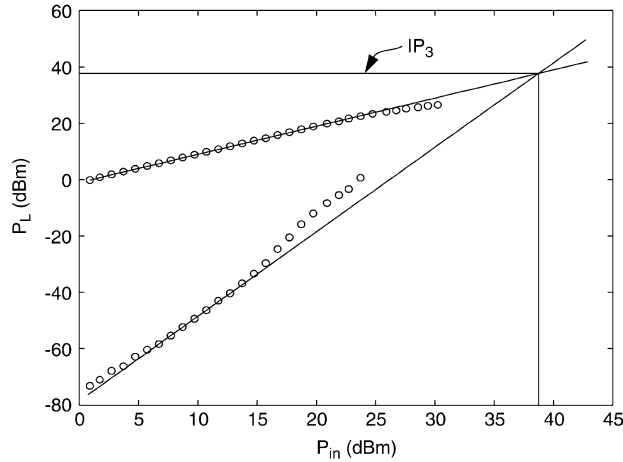


Fig. 10. Output 1-dB compression point measurement and IP3 measurement when $V_{CTRL} = 6.0$ V, $V_{CTRL} = 2.0$, and $V_{DB} = V_{SB} = 3.0$ V at 928 MHz of the 0.35- μ m RF switch with 900-MHz 30- Ω Z_S and Z_L impedance transformation networks.

ased drain/source-to-body junctions. On the other hand, P_{1dB} is measured at high input power levels and is determined by the turning on of the shunt transistor, M_3 , for this design. Because of this and the ~ 7 -dB increase of output P_{1dB} , the difference between P_{1dB} and IP3 is ~ 13 dB for this switch instead of more than 20 dB for the switch without ITNs. The use of ITNs using off-chip components has only small effects on IM3 for the switch. The reduction of the difference between P_{1dB} and IP3 is mainly due to the increase of P_{1dB} . The measured isolation is about 4 dB lower than the switch without impedance transformation networks. This is mainly due to the fact that when the source impedance is transformed down, M_3 in shunt with the transformed impedance is less effective for improving isolation. The measured characteristics of this 900-MHz switch with impedance transformation are summarized in Table I.

Another SPDT switch tuned for 20-dBm 2.4-GHz wireless local-area network (LAN) applications has also been implemented [7]. The same switch core used to implement the 900-MHz switch with impedance transformation is used for this purpose, because it has lower on-resistance for the switch core than that for the switch core designed for operation up to 2.5 GHz [13]. A photograph of the test fixture for this switch is shown in Fig. 4. A 2.2-nH L_S and a 0.8-pF C_P are estimated to transform the 50- Ω source/load impedance to 30 Ω at 2.4 GHz. For this circuit, L_S is entirely implemented with bondwire and package lead inductances, and the circuit does not require an off-chip inductor. The actual L_S is about 2.0–2.5 nH and C_P is 1.0 pF, which is the closest available value for the off-chip capacitors. This 0.2-pF additional C_P and the variation of L_S and C_P introduce mistuning of Z_S and Z_L .

Fig. 11 shows the measured insertion loss, return loss, and isolation for the 0.35- μ m RF switch with the 2.4-GHz impedance transformation networks. The measured insertion loss is less than 1.2 dB for frequencies between 2.32–2.60 GHz. At 2.49 GHz, the measured insertion loss is 1.1 dB, return loss is more than 17 dB, and isolation is 20.6 dB. Output P_{1dB} is 20.6 dBm at 2.4 GHz, which is lower than that for the

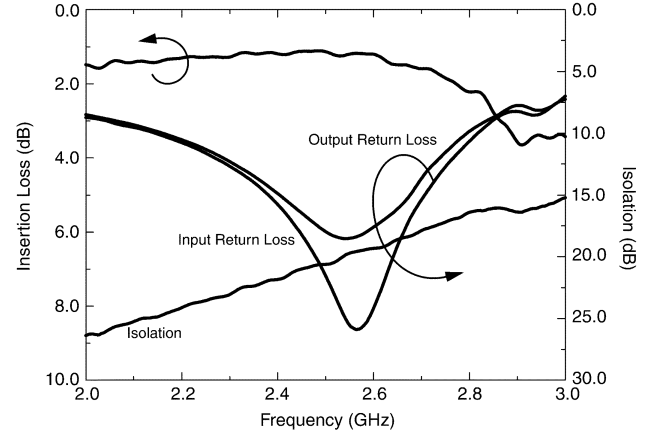


Fig. 11. Measured insertion loss, on-state return loss and isolation for the 0.35- μ m RF switch with 2.4-GHz 30- Ω Z_S and Z_L impedance transformation networks.

900-MHz switch due to the mistuning mentioned earlier caused by C_P and L_S not being the same as the design. The measured output IP3 is 29.8 dBm. The measured characteristics are also summarized in Table I.

Finally, the switches have been stressed at 20-dBm P_{AVS} with the output open and have also been stressed at 26 dBm P_{AVS} with a 50- Ω output load, and no degradation of the switch characteristics has been observed. These suggest that the switch can operate all the way up to P_{1dB} without being limited by reliability concerns [13].

IV. SUMMARY

SPDT switches implemented using 3.3-V 0.35- μ m NMOS transistors in a 0.18- μ m CMOS process on p⁺ silicon substrates for 900-MHz and 2.4-GHz wireless applications have been presented. In particular, a 900-MHz switch with an insertion loss of 0.5 dB and a 2.4-GHz switch with an insertion loss of 0.8 dB was demonstrated. These are the first bulk CMOS switches to attain such low insertion loss at 900 MHz and 2.4 GHz [13]. This work has also demonstrated that substrate resistances can be sufficiently lowered even when p⁺ silicon substrates are used. By using impedance transformation, power-handling capabilities as measured by output P_{1dB} have been increased to 24.3 and 20.6 dBm for 0.9 and 2.4-GHz operation while attaining insertion losses of 0.97 and 1.1 dB, respectively. The 2.4-GHz switch [7] is the first bulk CMOS switch which can be used for 802.11b wireless LAN applications. The use of a bulk CMOS process should enable integration of RF switches with other CMOS circuits.

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Feng-Jung Huang (S'98–M'01) was born in Taipei, Taiwan. He received the B.S. degree in electrical engineering from National Tsing Hua University, Hsinchu, Taiwan, in 1993, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Florida, Gainesville, in 1998 and 2001, respectively.

From 1995 to 1996, he was a Research Assistant developing intelligent power integrated circuits at National Tsing Hua University. From 1997 to 2001, he was with the Silicon Microwave Integrated Circuits and System Research Group (SiMICS), University of Florida. His research focused on developing devices and circuits to implement RF analog and digital systems using silicon IC technologies. Since June 2001, he has been with Maxim Integrated Products, Inc., Boston Design Center, North Chelmsford, MA, where he has developed several high-performance IF and RF integrated circuits such as the MAX2027, the MAX2055, and the MAX2056 family for wireless communication systems.



Kenneth K. O. (S'86–M'89) received the S.B., S.M., and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT), Cambridge, in 1984, 1984, and 1989, respectively.

From 1989 to 1994, he was with Analog Devices Inc., developing submicron CMOS processes for mixed-signal applications and high-speed bipolar and BiCMOS processes for RF and mixed-signal applications. He is currently a Professor at the University of Florida, Gainesville. He was also the Chief Technology Officer of Global Communications Devices Inc. from 2002 to 2003. His research group (Silicon Microwave Integrated Circuits and Systems Research Group) is developing circuits and components required to implement analog and digital systems operating between 1 and 100 GHz using silicon IC technologies. In 2001, he was a Visiting Professor in the Department of Electrical Engineering and Computer Science at MIT.

Dr. O was the General Chair of the 2001 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM). He has served as an Associate Editor for IEEE TRANSACTIONS ON ELECTRON DEVICES from 1999 to 2001. He also served as the Publication Chairman of the 1999 International Electron Device Meeting. He has authored or co-authored about 95 journal and conference publications, and holds four patents. He has received the 1995, 1997, and 2000 IBM Faculty Development Awards and the 1996 National Science Foundation Early Career Development Award.