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(54) TITLE OF THE INVENTION: SEMICONDUCTOR SWITCHING CIRCUIT

(57) ABSTRACT

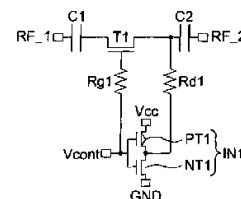
PROBLEM

To enhance maximum permissible input power and suppress an increase in ON-resistance.

SOLUTION

The semiconductor switching circuit includes: an enhancement n-channel MOSFET T1; first and second terminals RF_1, RF_2; a control terminal Vcont to which a control signal for controlling the switching of the MOSFET T1 is input; a first capacitive element C1 connected between the drain or the source of the MOSFET T1 and the first terminal RF_1; a second capacitive element C2 connected between the source or the drain of the MOSFET T1 and the second terminal RF_2; a first resistor Rg1 connected between the gate of the MOSFET T1 and the control terminal Vcont; a logic circuit IN1 for switching the control of the MOSFET T1, the logic circuit having an input side connected to the control terminal Vcont; and a second resistor Rd1 connected between either of the source and the drain of the MOSFET T1 and an output side of the logic circuit IN1.

SELECTED DRAWING: FIG. 1



CLAIMS

[Claim 1]

A semiconductor switching circuit comprising:
an enhancement n-channel MOSFET;
first and second terminals;
a control terminal to which a control signal for controlling the switching of the MOSFET is input;
a first capacitive element connected between the drain or source of the MOSFET and the first terminal;
a second capacitive element connected between the source or drain of the MOSFET and the second terminal;
a first resistor connected between the gate of the MOSFET and the control terminal;
a logic circuit for controlling the switching of the MOSFET, the logic circuit having an input side connected to the control terminal; and
a second resistor connected between the source or drain of the MOSFET and an output side of the logic circuit.

[Claim 2]

A semiconductor switching circuit comprising:
first and second enhancement n-channel MOSFETs;
first, second and third terminals;
a control terminal to which a control signal for controlling the switching of each of the first and second MOSFETs is input;
a first capacitive element connected between the drain or source of the first MOSFET and the first terminal;
a second capacitive element connected between the source or drain of the first MOSFET and the second terminal;
a third capacitive element connected between the drain or source of the second MOSFET and the second terminal;
a fourth capacitive element connected between the source or drain of the second MOSFET and the third terminal;
a first resistor connected between the gate of the first MOSFET and the control terminal;
a logic circuit for controlling the switching of the MOSFET, the logic circuit having an input side connected to the control terminal;
a second resistor connected between the source or drain of the first MOSFET and an output side of the logic circuit;
a third resistor connected between the source or drain of the second MOSFET and the control terminal; and
a fourth resistor connected between the gate of the second MOSFET and an output side of the logic circuit.

[Claim 3]

The semiconductor switching circuit according to claim 2, further comprising an inductor element connected in parallel to the source and drain of at least one of the first and second MOSFETs.

[Claim 4]

A semiconductor switching circuit comprising:
first, second, third and fourth enhancement n-channel MOSFETs;
first, second, third, fourth and fifth terminals;
a control terminal to which a control signal for controlling the switching of each of the first to fourth MOSFETs is input;
a first capacitive element connected between the drain or source of the first MOSFET and the first terminal;
a second capacitive element connected between the source or drain of the first MOSFET and the second terminal;
a third capacitive element connected between the drain or source of the second MOSFET and the

second terminal;

a fourth capacitive element connected between the source or drain of the second MOSFET and the third terminal;

a fifth capacitive element connected between the drain or source of the third MOSFET and the first terminal;

a sixth capacitive element connected between the source or drain of the third MOSFET and the fourth terminal;

a seventh capacitive element connected between the drain or source of the fourth MOSFET and the third terminal;

an eighth capacitive element connected between the source or drain of the fourth MOSFET and the fifth terminal;

a first resistor connected between the gate of the first MOSFET and the control terminal;

a logic circuit for controlling the switching of the first to fourth MOSFETs, the logic circuit having an input side connected to the control terminal;

a second resistor connected between the source or drain of the first MOSFET and an output side of the logic circuit;

a third resistor connected between the source or drain of the second MOSFET and the control terminal;

a fourth resistor connected between the gate of the second MOSFET and an output side of the logic circuit;

a fifth resistor connected between the gate of the third MOSFET and an output side of the logic circuit;

a sixth resistor connected between the source or drain of the third MOSFET and the control terminal;

a seventh resistor connected between the gate of the fourth MOSFET and the control terminal; and

an eighth resistor connected between the source or drain of the fourth MOSFET and an output side of the logic circuit.

[Claim 5]

The semiconductor switching circuit according to any one of claims 1 to 4, wherein the logic circuit is an inverter circuit having a CMOS configuration

DETAILED DESCRIPTION OF THE INVENTION

TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor switching circuit, and is particularly suitable for a high-frequency semiconductor switching circuit including a MOSFET formed on a silicon substrate.

BACKGROUND ART

[0002]

Compound semiconductors with a semi-insulating substrate having high electron mobility have been widely used as high-frequency semiconductor switching circuits that provide excellent switching properties in the high frequency range of 1 GHz or higher.

[0003]

However, in recent years, there has been active development of high-frequency semiconductor switching circuits using CMOS processes. The main reason therefor is that a CMOS switch can be integrated into another CMOS RF IC.

[0004]

However, when attempting to achieve a high-frequency semiconductor switching circuit using a MOSFET formed on a silicon substrate, the substrate is conductive, which causes insertion loss due to the resistance of the substrate in addition to insertion loss due to the ON-resistance of the MOSFET.

[0005]

Furthermore, when a high-frequency semiconductor switching circuit is used as a transmission/reception changeover switch, a considerably large maximum permissible input power is required. In order to achieve this, MOSFETs must be vertically stacked, or a multi-gate structure

must be used. However, this means that an increase in the ON-resistance occurs, which leads to an increase in insertion loss. There is a method of increasing the gate width in order to suppress the increase in ON-resistance caused by stacking such MOSFETs vertically or using a plurality of gates. However, this leads to an increase in the chip area and a deterioration in isolation. Optimization is performed within this kind of trade-off relationship, but the properties of CMOS switches are significantly inferior to switching circuits using a compound semiconductor.

[0006]

The following documents disclose conventional high-frequency semiconductor switching circuits.

Patent Document 1: Japanese Unexamined Patent Document H10-242836

Patent Document 2: Japanese Unexamined Patent Application H11-46101

Patent Document 3: Japanese Unexamined Patent Document H09-289443

Patent Document 4: Japanese Unexamined Patent Application H08-70245

Patent Document 5: Japanese Unexamined Patent Application H09-214201 Patent Document 6:

Japanese Unexamined Patent Application H10-284901 Patent Document 7: Japanese Unexamined

Patent Application 2003-37521 Patent Document 8: Japanese Unexamined Patent Application 2000-

261302

DISCLOSURE OF THE INVENTION

PROBLEM TO BE SOLVED BY THE INVENTION [0007]

[0007]

In view of the foregoing, an object of the present invention is to provide a semiconductor switching circuit capable of improving the maximum permissible input power while suppressing an increase in ON-resistance.

MEANS FOR SOLVING THE PROBLEM [0008]

[0008]

A semiconductor switching circuit according to one aspect of the present invention includes:

- an enhancement n-channel MOSFET;
- first and second terminals;
- a control terminal to which a control signal for controlling the switching of the MOSFET is input;
- a first capacitive element connected between the drain or source of the MOSFET and the first terminal;
- a second capacitive element connected between the source or drain of the MOSFET and the second terminal;
- a first resistor connected between the gate of the MOSFET and the control terminal;
- a logic circuit for controlling the switching of the MOSFET, the logic circuit having an input side connected to the control terminal; and
- a second resistor connected between the source or drain of the MOSFET and an output side of the logic circuit.

[0009]

Furthermore, a semiconductor switching circuit according to an aspect of the present invention includes:

- first and second enhancement n-channel MOSFETs;
- first, second and third terminals;
- a control terminal to which a control signal for controlling the switching of each of the first and second MOSFETs is input;
- a first capacitive element connected between the drain or source of the first MOSFET and the first terminal;
- a second capacitive element connected between the source or drain of the first MOSFET and the second terminal;
- a third capacitive element connected between the drain or source of the second MOSFET and the second terminal;
- a fourth capacitive element connected between the source or drain of the second MOSFET and the third terminal;

- a first resistor connected between the gate of the first MOSFET and the control terminal;
- a logic circuit for controlling the switching of the MOSFET, the logic circuit having an input side connected to the control terminal;
- a second resistor connected between the source or drain of the first MOSFET and an output side of the logic circuit;
- a third resistor connected between the source or drain of the second MOSFET and the control terminal; and
- a fourth resistor connected between the gate of the second MOSFET and an output side of the logic circuit.

[0010]

Alternatively, a semiconductor switching circuit according to an aspect of the present invention includes:

- first, second, third and fourth enhancement n-channel MOSFETs;
- first, second, third, fourth and fifth terminals;
- a control terminal to which a control signal for controlling the switching of each of the first to fourth MOSFETs is input;
- a first capacitive element connected between the drain or source of the first MOSFET and the first terminal;
- a second capacitive element connected between the source or drain of the first MOSFET and the second terminal;
- a third capacitive element connected between the drain or source of the second MOSFET and the second terminal;
- a fourth capacitive element connected between the source or drain of the second MOSFET and the third terminal;
- a fifth capacitive element connected between the drain or source of the third MOSFET and the first terminal;
- a sixth capacitive element connected between the source or drain of the third MOSFET and the fourth terminal;
- a seventh capacitive element connected between the drain or source of the fourth MOSFET and the third terminal;
- an eighth capacitive element connected between the source or drain of the fourth MOSFET and the fifth terminal;
- a first resistor connected between the gate of the first MOSFET and the control terminal;
- a logic circuit for controlling the switching of the first to fourth MOSFETs, the logic circuit having an input side connected to the control terminal;
- a second resistor connected between the source or drain of the first MOSFET and an output side of the logic circuit;
- a third resistor connected between the source or drain of the second MOSFET and the control terminal;
- a fourth resistor connected between the gate of the second MOSFET and an output side of the logic circuit;
- a fifth resistor connected between the gate of the third MOSFET and an output side of the logic circuit;
- a sixth resistor connected between the source or drain of the third MOSFET and the control terminal;
- a seventh resistor connected between the gate of the fourth MOSFET and the control terminal; and
- an eighth resistor connected between the source or drain of the fourth MOSFET and an output side of the logic circuit.

EFFECT OF THE INVENTION

[0011]

The semiconductor switching circuit of the present invention can improve the maximum permissible input power and suppress an increase in ON-resistance.

PREFERRED EMBODIMENT OF THE INVENTION

[0012]

Embodiments of the present invention will be described below with reference to the drawings.

[0013]

(1) Embodiment 1

FIG. 1 is a diagram depicting a configuration of a high-frequency semiconductor switching circuit according to Embodiment 1 of the present invention.

[0014]

The present Embodiment 1 includes: an enhancement n-channel MOSFET T1; capacitors C1 and C2 for DC component removal, in which first ends are connected to a source and drain of the MOSFET T1, respectively; a high-value resistor Rg1 in which a first end is connected to a gate of the MOSFET T1; a high-value resistor Rd1 in which a first end is connected to the source or drain of the MOSFET T1; and a CMOS inverter circuit IN1 including a p-channel MOSFET PT1 and an n-channel MOSFET NT1 with input/output terminals thereof connected between a second end of the resistor Rg1 and a second end of the resistor Rd1.

[0015]

Terminals RF_1, RF_2 for connecting to a high-frequency signal line are connected to second ends of the capacitors C1 and C2, respectively.

[0016]

A terminal GND connected to the CMOS inverter circuit IN1 is a grounding terminal and a terminal Vcc is a power supply voltage Vcc terminal.

[0017]

A control terminal Vcont, to which a control voltage Vcont for switching control is supplied, is connected to an input terminal of the CMOS inverter circuit IN1.

[0018]

Note that the resistors Rg1, Rd1 are large enough to prevent leaking of high-frequency signals and have a value of approximately 10 k Ω , for example.

[0019]

An operation of present Embodiment 1 having the abovementioned configuration will be described below.

[0020]

A1) When the control voltage Vcont is 0 V

A control voltage Vcont of 0 V is input to the input terminal of the CMOS inverter circuit IN1, and the power supply voltage Vcc is output from an output terminal.

[0021]

0 V is applied to a gate of the n-channel MOSFET T1, and the power supply voltage Vcc is applied to a drain or source, in this case the source, to which an output terminal of the CMOS inverter circuit IN1 is connected.

[0022]

If the power supply voltage Vcc is now 3 V, the gate-source voltage Vgs of the MOSFET T1 is -3 V.

[0023]

Furthermore, if a threshold voltage Vth of the MOSFET T1 is 0.7 V, the MOSFET T1 is at this time in an OFF state.

[0024]

As a result, a non-conductive state is established between the terminal RF_1 and terminal RF_2.

[0025]

B1) When the control voltage Vcont is 3 V

3 V is applied to the gate of the MOSFET T1 and 0 V is applied to the source. As a result, the gate-source voltage Vgs of the MOSFET T1 = 3 V, and the MOSFET T1 turns ON.

[0026]

Herein, when the MOSFET T1 is ON, the voltage $V_{gs} - V_{th} = 2.3$ V, thereby achieving a

sufficiently low ON-resistance.

[0027]

On the other hand, when the abovementioned MOSFET T1 is OFF, the voltage $V_{gs} - V_{th} = -3.7$ V, and the OFF state can be maintained even for a sufficiently large input amplitude.

[0028]

With the terminal RF_2 grounded and a sine wave voltage being applied to the terminal RF_1, the MOSFET T1 can remain OFF until the voltage amplitude reaches 7.4 V (14.8 V_{pp} at peak to peak values).

[0029]

The voltage amplitude of 7.4 V in a 50 Ω system is converted to power, which is 27.38 dBm. Therefore, it is possible to achieve a maximum permissible input power that is sufficiently usable as a transmission/reception switch for a PHS (Personal Handy-phone System), for example.

[0030]

As described above, according to the present Embodiment 1, not only is the gate voltage swung between 0 V and 3 V, but the source-drain voltage is also swung between 0 V and 3 V, such that the gate-source voltage V_{gs} can be made to swing with an amplitude (6 V) that is relatively twice that of the power supply voltage V_{cc} .

[0031]

This makes it possible to increase the maximum permissible input amplitude to maintain an OFF state, while at the same time lowering the ON-resistance of the MOSFET to approach the ON-resistance of a GaAs-based FET.

[0032]

In the circuit configuration depicted in FIG. 1, the input terminal of the CMOS inverter circuit IN1 is connected to the resistor Rg1, and the output terminal is connected to the resistor Rd1.

However, the input terminal may be connected to the resistor Rd1, and the output terminal may be connected to the resistor Rg1. In this case, the polarity of the operation with respect to the control voltage V_{cont} is simply reversed, and the same effect as that of the circuit configuration depicted in FIG. 1 can be achieved.

[0033]

(2) Embodiment 2

FIG. 2 is a diagram depicting a configuration of a high-frequency semiconductor switching circuit according to Embodiment 2 of the present invention.

[0034]

Assuming that the circuit indicated in Embodiment 1 above is considered as one unit, the present Embodiment 2 uses two of the units, and two more spiral inductors L1, L2 are connected between the source and drain of the MOSFET T1 and between a source and drain of a MOSFET T2, which corresponds to a so-called resonant SPDT (Single-Pole Double-Throw) switch.

[0035]

The present Embodiment 2 includes: enhancement type n-channel MOSFETs T1 and T2; capacitors C1 and C2 for DC component removal, in which first ends are connected to a source and drain of the MOSFET T1; capacitors C3 and C4 for DC component removal, in which first ends are connected to a source and drain of the MOSFET T2; a high-value resistor Rg1 in which a first end is connected to a gate of the MOSFET T1; a high-value resistor Rd1 in which a first end is connected to the source or drain of the MOSFET T1; a high-value resistor Rg2 in which a first end is connected to a gate of the MOSFET T2; a high-value resistor Rd2 in which a first end is connected to the source or drain of the MOSFET T1; a CMOS inverter circuit IN1 including a p-channel MOSFET PT1 and an n-channel MOSFET NT1 with an input terminal connected to a second end of the resistor Rg1 and a second end of the resistor Rg2 and an output terminal connected between the second end of the resistor Rd1 and the second end of the resistor Rg2; and as described above, spiral inductors L1 and L2 connected between the source and drain of the MOSFET T1 and the source and drain of the MOSFET T2, respectively.

[0036]

A second end of the capacitor C1 is connected to a terminal RF_1 for connecting a high-frequency signal line, and a second end of the capacitor C4 is connected to a terminal RF_2 for connecting a high-frequency signal line.

[0037]

A common terminal RF_COM is connected to a connection point between a second end of the capacitor C2 and a second end of the capacitor C3.

[0038]

A terminal GND connected to the CMOS inverter circuit IN1 is a grounding terminal and a terminal Vcc is a power supply voltage Vcc terminal.

[0039]

A control terminal Vcont, to which a control voltage Vcont for switching control is supplied, is connected to an input terminal of the CMOS inverter circuit IN1.

[0040]

Note that the resistors Rg1, Rg2, Rd1 and Rd2 are large enough to prevent leaking of high-frequency signals and have a value of approximately 10 k Ω , for example.

[0041]

An operation of present Embodiment 2 having the abovementioned configuration will be described below.

[0042]

In the present Embodiment 2, a signal path is switched between the common terminal RF_COM and the high-frequency signal terminal RF_1 or between the common terminal RF_COM and the high-frequency signal terminal RF_2 on the basis of the control voltage Vcont.

[0043]

The spiral inductor L1 is designed to resonate in parallel with the off-capacitance of the MOSFET T1 and the frequency of the high-frequency signal RF, and similarly, the spiral inductor L2 is designed to resonate in parallel with the off-capacitance of the MOSFET T2 and the frequency of the high-frequency signal RF.

[0044]

Herein, it is assumed that the power supply voltage Vcc is 3 V and the threshold voltages Vth of the MOSFETs T1, T2 are each 0.7 V.

[0045]

A2) When the control voltage Vcont is 0 V

A voltage of 0 V on the input terminal side of the CMOSFET inverter circuit IN1 is applied to a gate of a transistor T1 and a source of a transistor T2, and a voltage Vcc = 3V on the output terminal side is applied to a gate of the transistor T2 and a source of the transistor T1, such that the MOSFET T1 is in the OFF state and T2 is in the On state.

[0046]

The terminals RF_1 and RF_COM are in a cutoff state, and the terminals RF_2 and RF_COM are in a conductive state.

[0047]

Herein, the off-capacitance of the MOSFET T1 and the spiral inductor L1 are designed to resonate in parallel at the frequency of the high-frequency signal RF, such that sufficiently high isolation is achieved in the OFF state.

[0048]

B2) When the control voltage Vcont is 3 V

The MOSFET T1 is in the ON state, and the MOSFET T2 is in the OFF state. As a result, a conductive state is established between the terminals RF_1 and RF_COM, and a cutoff state is established between the terminals RF_2 and RF_COM.

[0049]

The off-capacitance of the MOSFET T2 and the spiral inductor L2 are designed to resonate in parallel at the frequency of the high-frequency signal RF, thereby achieving sufficiently high isolation.

[0050]

According to the present Embodiment 2, as in Embodiment 1, when either one of the MOSFETs T1, T2 is in an ON state, the $V_g - V_{th}$ thereof is as high as 2.3 V, thereby achieving a small ON-resistance.

[0051]

On the other hand, the $V_g - V_{th}$ of the MOSFET in an OFF state is -3.7 V, which is sufficiently low, and the maximum permissible input power is sufficiently high (27.38 dBm).

[0052]

If a larger maximum permissible input power is required, the MOSFETs T1, T2 can be stacked vertically or a multi-gate structure can be used.

[0053]

Note that the spiral inductors L1, L2 may be configured as external components.

[0054]

(3) Embodiment 3

FIG. 3 is a diagram depicting a configuration of a high-frequency semiconductor switching circuit according to Embodiment 3 of the present invention.

[0055]

Embodiment 3 is a so-called shunt SPDT switch where, assuming that the MOSFET T1, capacitors C1 and C2, resistors Rg1 and Rd1, and inverter circuit IN1 indicated in Embodiment 1 are considered as one unit, four units are used in a state in which the inverter circuit IN1 is shared.

[0056]

In other words, provided are: a first unit having a MOSFET T1, capacitors C1 and C2, and resistors Rg1 and Rd1 and sharing an inverter circuit IN1; a second unit having a MOSFET T2, capacitors C3 and C4, and resistors Rg2 and Rd2 and sharing the inverter circuit IN1; a second unit having a MOSFET T3, capacitors C5 and C6, and resistors Rg3 and Rd3 and sharing the inverter circuit IN1; and a second unit having a MOSFET T4, capacitors C7 and C8, and resistors Rg4 and Rd4 and sharing the inverter circuit IN1.

[0057]

Terminals RF_1 and RF_2 to which high-frequency signal lines are input are connected, respectively, to a connection point of first ends of the capacitors C1 and C5, and to a connection point of first ends of the capacitors C4 and C7.

[0058]

First ends of the capacitors C6 and C8 are connected to grounding terminals GND_1, GND_2.

[0059]

A terminal GND connected to the CMOS inverter circuit IN1 is a grounding terminal and a terminal Vcc is a power supply voltage Vcc terminal.

[0060]

A control terminal Vcont, to which a control voltage Vcont for switching control is supplied, is connected to an input terminal of the CMOS inverter circuit IN1.

[0061]

Note that the resistors Rg1 to Rg4 and Rd1 to Rd4 are large enough to prevent leaking of high-frequency signals, and have a value of approximately 10 k Ω , for example.

[0062]

An operation of Embodiment 4 having the abovementioned configuration will be described below.

[0063]

For one common high-frequency signal input terminal RF_COM, a signal path is switched between the two high-frequency signal input terminals RF_1, RF_2.

[0064]

As in the abovementioned Embodiments 1 and 2, the power supply voltage Vcc is set to 3 V, and the threshold voltage Vth of each of the MOSFETs T1 to T4 is set to 0.7 V.

[0065]

A3) When the control voltage Vcont is 0 V

A control voltage Vcont of 0 V is input to an input terminal of the inverter circuit IN1, turning

OFF the MOSFETs T1, T4. A power supply voltage V_{cc} of 3 V is output from an output terminal of the inverter circuit IN1, turning ON the MOSFETs T2, T3.

[0066]

As a result, a cutoff state is established between the terminals RF_1 and RF_COM, and a conductive state is established between the terminals RF_2 and RF_COM.

[0067]

B3) When the control voltage V_{cont} is 3 V

The MOSFETs T1, T4 are in an ON state, and the MOSFETs T2, T3 are in an OFF state.

[0068]

As a result, a conductive state is established between the terminals RF_1 and RF_COM, and a cutoff state is established between the terminals RF_2 and RF_COM.

[0069]

Similar to the abovementioned Embodiment 1, in the present Embodiment 3, $V_{gs} - V_{th}$ of the MOSFET in the ON state is sufficiently high at 2.3 V, and a small ON-resistance is achieved.

[0070]

Furthermore, the $V_g - V_{th}$ of the MOSFET in an OFF state is -3.7 V, which is sufficiently low, and the maximum permissible input power is sufficiently high (27.38 dBm).

[0071]

If an even larger maximum permissible input power is required, the MOSFETs T1 to T4 can be stacked vertically or a multi-gate structure can be used.

[0072]

Herein, the present Embodiment 3 will be compared with an example of a high-frequency semiconductor switching circuit as a comparative example.

[0073]

FIG. 4 depicts a shunt SPDT switch configuration according to a comparative example.

[0074]

A source and drain of a switching MOSFET T1 are connected between a common high-frequency input terminal RF_COM and one of the high-frequency input terminals RF_1, and the source and drain of the switching MOSFET T1 are connected between the high-frequency input terminal RF_COM and one of the high-frequency input terminals RF_1.

[0075]

A source and drain of a shunt MOSFET T3 are connected between a terminal RF_1 and a ground terminal GND_1, and a source and drain of a shunt MOSFET T4 are connected between a terminal RF_2 and a ground terminal GND_2.

[0076]

Gates of the MOSFETs T1, T4 are connected through resistors R_{g1} , R_{g4} to an input terminal of an inverter circuit IN1 to which a control voltage V_{cont} is input, and gates of the MOSFETs T2, T3 are connected through resistors R_{g2} , R_{g3} to an output terminal of the inverter circuit IN1.

[0077]

Capacitors C1 to C5 are connected between the terminals RF_1, RF_2, RF_COM, GND_1, GND_2 and a first end of the respective MOSFETs.

[0078]

Furthermore, in this comparative example, an intermediate potential V_{bias} is applied to a first end of each of transistors T1 to T4 as a bias potential via resistors R_{dd1} to R_{dd3} .

[0079]

Similar to the abovementioned Embodiments 1 to 3, when the power supply voltage $V_{cc} = 3$ V, the threshold voltage $V_{th} = 0.7$ V, and the intermediate potential $V_{bias} = 1.5$ V, the value of $V_{gs} - V_{th}$ is calculated as follows:

[0080]

A0) When in ON state

$$V_{gs} - V_{th} = 3 - 1.5 - 0.7 = 0.8 \text{ V}$$

This value is lower than 2.3 V in the abovementioned Embodiments 1 to 3, and thus the ON-

resistance increases in accordance with Embodiments 1 to 3.

[0081]

B0) When in OFF state

$$V_{gs} - V_{th} = 0 - 1.5 - 0.7 = -2.2 \text{ V}$$

The value in the abovementioned Embodiments 1 to 3 is -3.7 V, and the maximum permissible input power is reduced in the comparative example.

[0082]

As described above, according to the Embodiments 1 to 3, the ON-resistance is reduced and the maximum permissible input power is increased.

[0083]

The three Embodiments 1 to 3 have been described above, but the same effect can be achieved using the circuit indicated in Embodiment 1 as one unit and combining a plurality thereof to form a switch.

[0084]

Furthermore, a CMOS switch formed using a SOI (Silicon On Insulator) substrate generally has excellent high-frequency properties, and thus the use of SOI is also effective in the present invention.

[0085]

Furthermore, in the abovementioned Embodiments 1 to 3, the power supply voltage V_{cc} is 3 V as an example. However, when a higher power supply voltage is used, the maximum permissible input power increases accordingly.

[0086]

It is also effective to increase the maximum permissible input power by boosting the power supply voltage V_{cc} supplied externally by a separately provided charge pump circuit and supplying the power supply voltage V_{cc} to the power supply terminal V_{cc} .

[0087]

The capacitors used in Embodiments 1 to 3 above are not limited in terms of the configurations thereof, or the high-frequency properties can be improved by using a MIM (metal-insulator-metal) structure, which has excellent high-frequency properties.

Furthermore, in consideration of the parasitic inductance of bonding wires and the like, the value is preferably set such that resonance occurs in series.

[0088]

Furthermore, when configuring an SPnT (n is an integer equal to or greater than 3) switch, in order to reduce the number of control terminals, the inverter circuit and other logic circuits in Embodiments 1 to 3 may be configured as CMOS circuits and integrated on the same semiconductor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0089]

FIG. 1 is a circuit diagram depicting a configuration of a high-frequency semiconductor switching circuit according to Embodiment 1 of the present invention;

FIG. 2 is a circuit diagram depicting a configuration of a high-frequency semiconductor switching circuit according to Embodiment 2 of the present invention;

FIG. 3 is a circuit diagram depicting a configuration of a high-frequency semiconductor switching circuit according to Embodiment 3 of the present invention; and

FIG. 4 is a circuit diagram depicting a configuration of a high-frequency semiconductor switching circuit according to a comparative example.

DESCRIPTION OF CODES

[0090]

Rg1 to Rg4, Rd1 to Rd4: High-frequency signal blocking resistor C1 to C8: Component removal capacitor T1 to T4: Enhancement n-channel MOSFET RF_COM: High-frequency signal input terminal RF_1, RF_2: Common high-frequency signal input terminal GND_1, GND_2: High-frequency ground terminal GND: Ground terminal 10

V_{cc} : Power supply voltage terminal

V_{cont} : Control terminal PT1: p-channel MOSFET

NT1: n-channel MOSFET
IN1: CMOS inverter circuit

FIG. 1

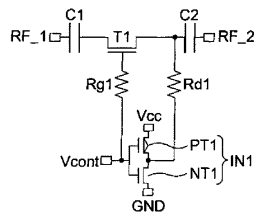


FIG. 2

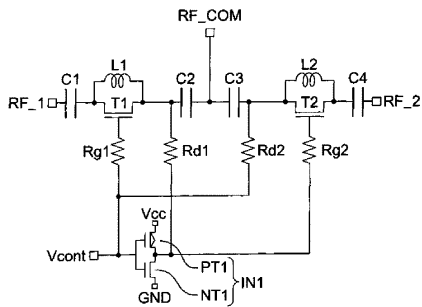


FIG. 3

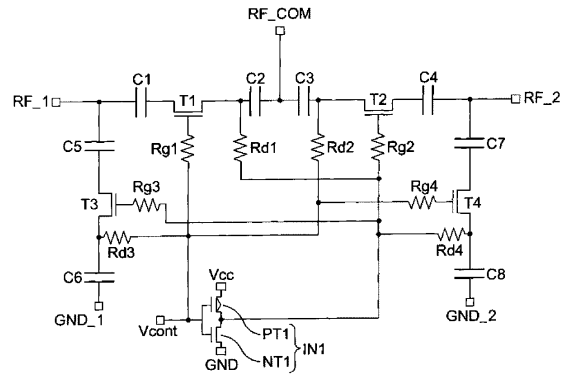
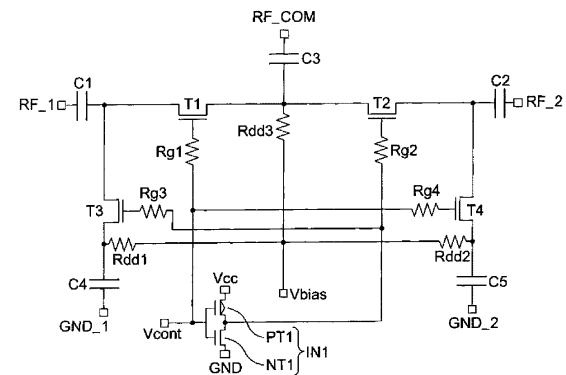


FIG. 4



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GX01



TRANSLATOR'S CERTIFICATE OF TRANSLATION

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I, Dwaine Palmer, a translator fluent in the Japanese and English languages, on behalf of Questel, do solemnly and sincerely declare that the following is, to the best of my knowledge and belief, a true and correct translation of the document(s) listed below in a form that best reflects the intention and meaning of the original text.

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