

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KANGXI COMMUNICATION TECHNOLOGIES (SHANGHAI) CO., LTD.
Petitioner,

v.

SKYWORKS SOLUTIONS, INC.,
Patent Owner.

U.S. Patent No. 9,450,579
Issue Date: SEPTEMBER 20, 2016

Title: RADIO FREQUENCY DEVICES HAVING REDUCED
INTERMODULATION DISTORTION

Inter Partes Review No.: IPR2024-01456

**PETITION FOR *INTER PARTES* REVIEW OF PATENT NO. 9,450,579
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. §§ 42.1-.80, 42.100-.107**

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PETITIONER'S EXHIBIT LIST

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EX-1002	Prosecution History of U.S. Patent No. 9,450,579.
EX-1003	Declaration of Dr. Larry Larson under 37 C.F.R. § 1.68.
EX-1004	<i>Curriculum Vitae</i> of Larry Larson.
EX-1005	U.S. Patent Publication No. 2011/0254614 A1 to C-W Huang, et al., Filing Date of April 16, 2010 and Publication Date of October 20, 2011 (“Huang”).
EX-1006	Japanese Patent Publication No. JP 2006-121217 to Seshimo, Toshiko et al., Publication Date of May 11, 2006 (“Seshimo”).
EX-1007	Certified English Translation of Japanese Patent Publication No. JP 2006-121217 (EX-1006).
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EX-1018	U.S. Patent No. 6,698,082 to Crenshaw, et al., filed August 28, 2001 and issued on March 2, 2004.
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EX-1024	Rick Cory, et al., “Solid State RF/Microwave Switch Technology: Part 2”, June 2009, Skyworks Solutions, Inc., www.mpdigest.com , archived at Internet Archive’s Wayback Machine at https://web.archive.org/web/20090906040150/http://www.skyworksinc.com/Press_Published_Articles.aspx .
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EX-1044	G. Breed, "There's Nothing Magic About 50 Ohms", High Frequency Electronics magazine, Summit Technical Media, LLC, June 2007, archived at Internet Archive's Wayback Machine on August 24, 2009 at https://web.archive.org/web/20090824090425/http://www.highfrequencyelectronics.com/Archives/Jun07/HFE0607_Editorial.pdf .
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EX-1049	Skyworks Solutions, Inc., “SKY13399-468LF: 0.7 – 2.7 GHz DPx3T Switch”, Data Sheet, accessible through Internet Archive’s Wayback Machine link archived on August 14, 2011 at https://web.archive.org/web/20111007155745/http://www.skyworksinc.com/Products_Documents.aspx and also accessible through Internet Archive’s Wayback Machine link archived on August 29, 2011 at https://web.archive.org/web/20110829193217/www.skyworksinc.com/categories.aspx?CategoryID=495

I. INTRODUCTION

Pursuant to 35 U.S.C. §§311 *et seq.* and 37 C.F.R. §§42.1 *et seq.*, Kangxi Communications Technologies (Shanghai) Co., Ltd. (“Petitioner”) petitions for *inter partes* review (“IPR”) of Patent No. 9,450,579 (the “’579 Patent”) (EX-1001). Petitioner submits that ’579 Patent claims 1-3, 7-9, and 13-15 (the “Challenged Claims”) are unpatentable under (pre-AIA) 35 U.S.C. §103(a) in view of the prior art discussed herein. This Petition demonstrates by a preponderance of the evidence that there is a reasonable likelihood that Petitioner will prevail with respect to at least one of the Challenged Claims. Accordingly, Petitioner requests that the Board institute the ’579 Patent IPR pursuant to 37 C.F.R. §42.108.

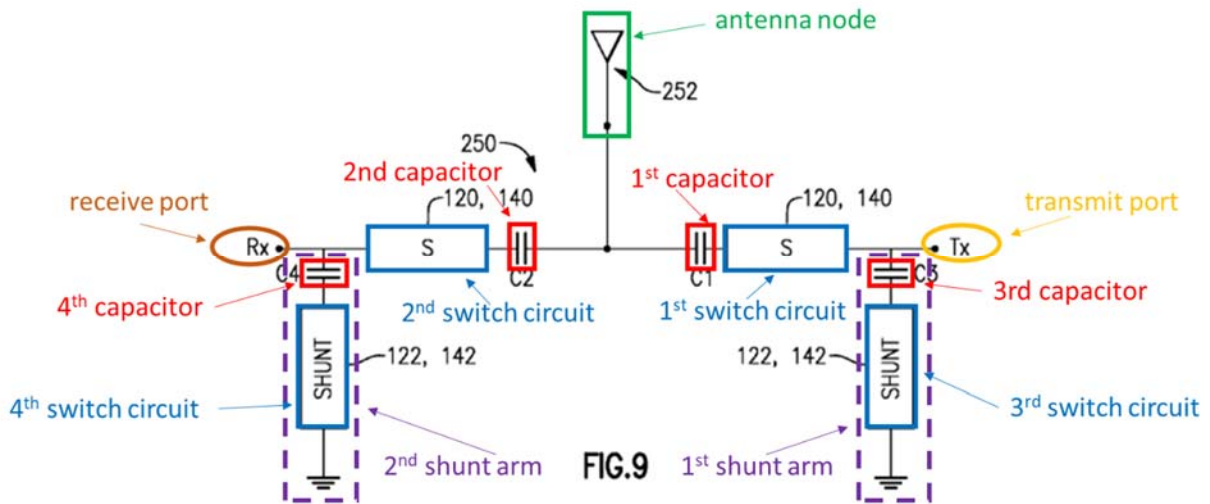
II. OVERVIEW

The ’579 Patent is directed to RF switches that can be used to “switch” signals between one or more “poles” (antenna) and one or more “throws” (transmit or receive circuits). During operation, at any given point in time, the “pole” may be used to transmit, or receive, a desired RF signal, where the transmit signal frequency may be different than the receive signal frequency. Accordingly, the RF switch is used to “switch” the “throw” that is communicatively/electrically connected to the “pole” based on the desired operating mode (transmit or receive). For example, if “transmitting” is desired, the path between the transmit “throw” and antenna is “switched” to a closed (“ON”) state, while the path between the receive “throw” and antenna is “switched” to

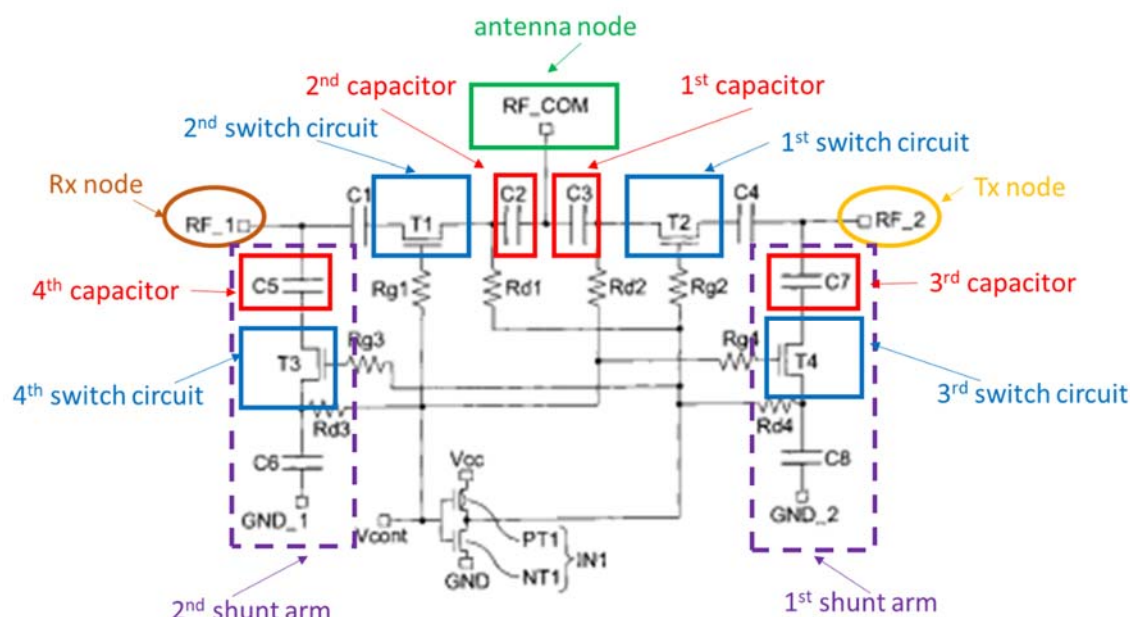
an open (“OFF”) state.

The Patent is directed to a well-known problem in designing RF switches in wireless devices, especially those operating in a “multi-band and/or multi-mode environment”, namely “the susceptibility of a [RF switch] system to interference” from unwanted signals. For example, when an unwanted signal (*e.g.*, “blocker” signals) mixes with a desired (“fundamental”) RF signal in an RF switch, the desired transmitted/received information may be degraded, and further unwanted signals may be created. These created unwanted signals may be at frequencies that are multiples of a desired RF signal frequency (f_1) (*e.g.*, $2f_1$, $3f_1$, etc.) called “harmonic frequencies”, or at non-harmonic frequencies (*e.g.*, $f_1 \pm f_{\text{blocker}}$, $2f_1 \pm f_{\text{blocker}}$, etc.) called “intermodulation distortion (IMD)” products.

The Patent’s disclosed solution to this “interference susceptibility” problem involved (i) including a “shunt arm” in each RF switch “throw”, and (ii) positioning capacitors in each “arm” of each RF switch “throw.” Specifically, the Patent states the particular arrangement of RF switch components depicted in Figure 9 (annotated below) provides this solution:



'579 Patent FIG. 9 (above-annotated) shows a SPDT switching configuration 250. The single pole is connected to antenna 252. One throw is coupled to transmit port (Tx) via 1st switch circuit S. The Tx port is coupled to ground via a first shunt arm, including 3rd switch circuit ("Shunt") and capacitor C3. Similarly, the other throw is coupled to receive port (Rx) via 2nd switch circuit S. The Rx port is coupled to ground via a second shunt arm, including 4th switch circuit ("Shunt") and capacitor C4. Capacitor C1 is provided between antenna node (252) and TX throw 1st switch S. Similarly, capacitor C2 is provided between antenna node (252) and RX throw 2nd switch S. For the shunt arms, capacitor C3 is provided between the TX node and 3rd switch ("Shunt") and, similarly, capacitor C4 is provided between the RX node and 4th switch ("Shunt") (although the Patent states the RX node shunt arm is optional). "With the foregoing capacitors, a low-frequency jammer signal can be blocked or reduced from mixing with any ON or OFF paths. This can lead to improvement in IMD performance, especially for low-frequency blocker signals." EX-1001, 9:39-59, FIG. 9;



EX-1007, FIG. 3 (above-annotated).

A well-known, fundamental characteristic of all capacitors (with a given capacitance value, which designers can select as appropriate) is that they have a **much** higher opposition (impedance) to low-frequency signals than high-frequency signals, *i.e.*, capacitors block low-frequency signals and pass high-frequency signals. As such, outside of specifying the arrangement of the capacitors in the SPDT switch, the Patent unsurprisingly leaves the particular size of the capacitors to design choices of POSITAs.

Indeed, the Patent does not provide **any** details as to, *e.g.*, (i) **how** the positioning of capacitors in the FIG. 9 SPDT switch “prevent[s] a low-frequency blocker signal from mixing with a fundamental frequency signal”, (ii) **what value** the capacitors must have to perform this function, (iii) **where** the “low-frequency blocker signal” originates from, or (iv) **what** constitutes a “low” frequency “blocker” signal relative to a

“fundamental” frequency. In other words, the Patent recognizes that this low-frequency-blocking-high-frequency-passing characteristic of capacitors was well-within the knowledge of POSITAs, and leaves the other implementation and operation details to design choices of POSITAs.

Likewise, Huang and Seshimo provide the same level of detail as the ’579 Patent and show the identical arrangement of capacitors in series and shunt arms of an RF switch of a wireless device to solve the well-known problem posed by undesired low-frequency signals in such RF switches and to achieve known and predictable benefits.

III. GROUNDS FOR STANDING (37 C.F.R. §42.104(A))

Petitioner certifies the ’579 Patent is eligible for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the grounds identified herein. 37 C.F.R. §42.104(a). This Petition is filed pursuant to 37 C.F.R. §42.106(a).

IV. RELIEF REQUESTED (37 C.F.R. §42.22(A))

Petitioner respectfully requests institution of an IPR pursuant to 37 C.F.R. §42.108 and cancellation of the Challenged Claims.

V. REASONS FOR THE RELIEF REQUESTED

As explained in §II and §V-§VII of this Petition and in the Declaration of Petitioner’s Expert, Dr. Larry Larson (EX-1003), the apparatus and methods recited in

the Challenged Claims are obvious over the prior art in view of the knowledge, skill and creativity (“Knowledge”) of POSITAs in July 2012.¹

A. Summary of the ’579 Patent

The ’579 Patent is directed to RF switches usable to “switch” signals between one or more “poles” (antenna) and one or more “throws” (receive (Rx) node and transmit (Tx) node) of a wireless device. EX-1001, 1:20-38, 9:22-30. EX-1003, ¶28.

The Patent describes exemplary RF transistor switches, “based on one or more field-effect transistors (FETs)” arranged, for example, in a “single-pole-double-throw (SPDT or SP2T) configuration”, *e.g.*, FIG. 3 (below-annotated):

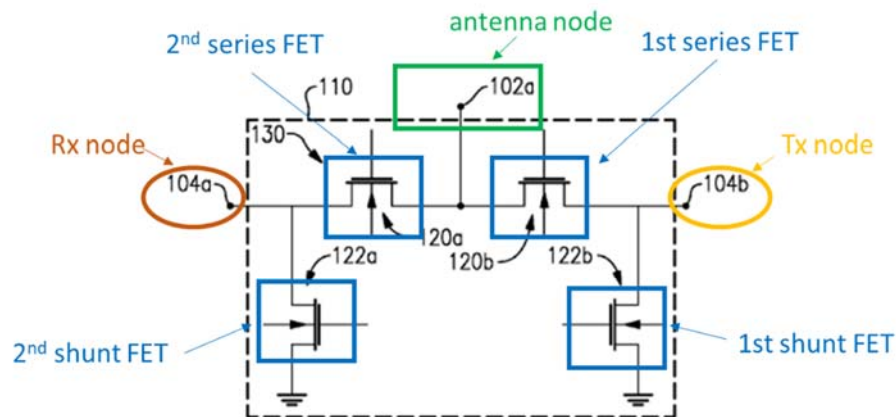
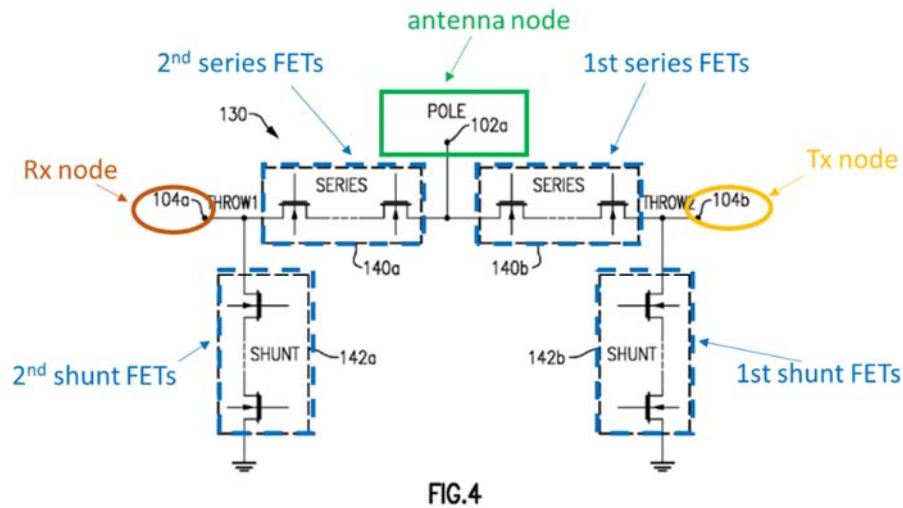


FIG.3

¹ All emphasis in quoted materials, and figure annotations, in the Petition were added by Petitioner.

EX-1001, 1:34-37, 3:33-37, 3:56-66, FIG. 3. EX-1003, ¶30. Using multiple FETs per switch arm, *e.g.*, FIG. 4 (below-annotated), in lieu of single FETs (*e.g.*, FIG. 3), “enables improved power-handling capability of the switching device”, but, “in some embodiments,... degrades the switching device insertion loss² performance”:



EX-1001, 4:25-56, 7:15-31, 8:31-53; EX-1003, ¶31.

These RF switches (including FETs) optionally “can be fabricated with silicon or silicon-on-insulator (SOI) technology”, where using SOI technology could “reduce[] power consumption of device circuitry due to decreased parasitic capacitance of

² “Insertion loss” was well-known as “measured as a ratio of the [respective] power or voltage of an RF signal” between “an input port”, and “an output port”, “of the switching device”, with “[d]ecreased... insertion loss” being “desirable”. EX-1001, 5:48-63; EX-1036, 1; EX-1039, 5, 9-11; EX-1008, 3; EX-1003, ¶31.

transistors and interconnect metallization to a silicon substrate”; “reduce junction capacitance or use of high resistivity substrate, enabling reduced substrate related RF losses” from the “[p]resence of a buried oxide layer”; and “decrease[] chip size” because “[e]lectrically isolated SOI transistors can facilitate stacking.” EX-1001, 7:34-59, 1:41-42, 1:58-61, 3:36-38; EX-1003, ¶32.

For both the single-, and multi-, transistor-per-switch-arm arrangements, the “[o]perations of such FETs can be controlled and/or facilitated by... gate bias/coupling circuit 150a,... body bias/coupling circuit 150c, and/or... source/drain coupling circuit 150b”, and the “design or features” of each such control circuit (150a, 150b, 150c, FIG. 6) “can improve performance of the switch arm... includ[ing]... device insertion loss, isolation performance³, power handling capability and/or switching device linearity.” EX-1001, 5:5-55, FIGS. 5-6, 10:11-27, FIGS. 11A-11D. The Patent provides **no** other details on **any** of such control circuits, nor explains **how** any of their “design or features” could result in any of the stated switching performance improvements; thus acknowledging that these implementation details were well-within the knowledge of

³ “Isolation” was well-known as “measure[d]... while the switching device is in a state where an input port and... output port are electrically isolated”, *e.g.*, “an OFF state”, and “[i]ncreased switching device isolation can improve RF signal integrity.” EX-1001, 6:7-18; EX-1036, 1; EX-1039, 5-6, 10-11, FIG. 5; EX-1003, ¶33.

POSITAs. *Id.*; EX-1003, ¶33.

The Patent is directed to a well-known problem in designing RF switches in wireless devices, especially those operating in a “multi-band and/or multi-mode environment”, namely “the susceptibility of a [RF switch] system to interference” from unwanted signals. EX-1001, 6:42-7:13, 9:8-21, 6:9-18; EX-1003, ¶34. For example, as was well-known to POSITAs⁴, when an unwanted signal (*e.g.*, “blocker” signal) mixes with a desired (“fundamental”) RF signal in an RF switch, the desired transmitted/received information may be degraded, and further unwanted signals may be created. *Id.*; EX-1001, 6:19-41, 9:1-7; EX-1003, ¶34. These created unwanted signals may be at frequencies that are multiples of a desired RF signal frequency (f_1) (*e.g.*, $2f_1$, $3f_1$, etc.) called “harmonic frequencies”, or at non-harmonic frequencies (*e.g.*, $f_1 \pm f_{\text{blocker}}$, $2f_1 \pm f_{\text{blocker}}$, etc.) called “intermodulation distortion (IMD)” products. *Id.*; EX-1003, ¶34.

The Patent describes a multi-pronged solution to this “interference susceptibility” problem. First, since “[a] given system’s linearity can govern how much IMD will occur within it, which in turn can create interferences”, “[s]ystem designers typically

⁴ Patent Owner’s (“PO’s”) own articles and whitepapers evidence that this same problem was well-known to POSITAs. §V.F.2 (EX-1039, 2-6, 8-12 (*citing* EX-1040, 3-6); EX-1036, 1-2).

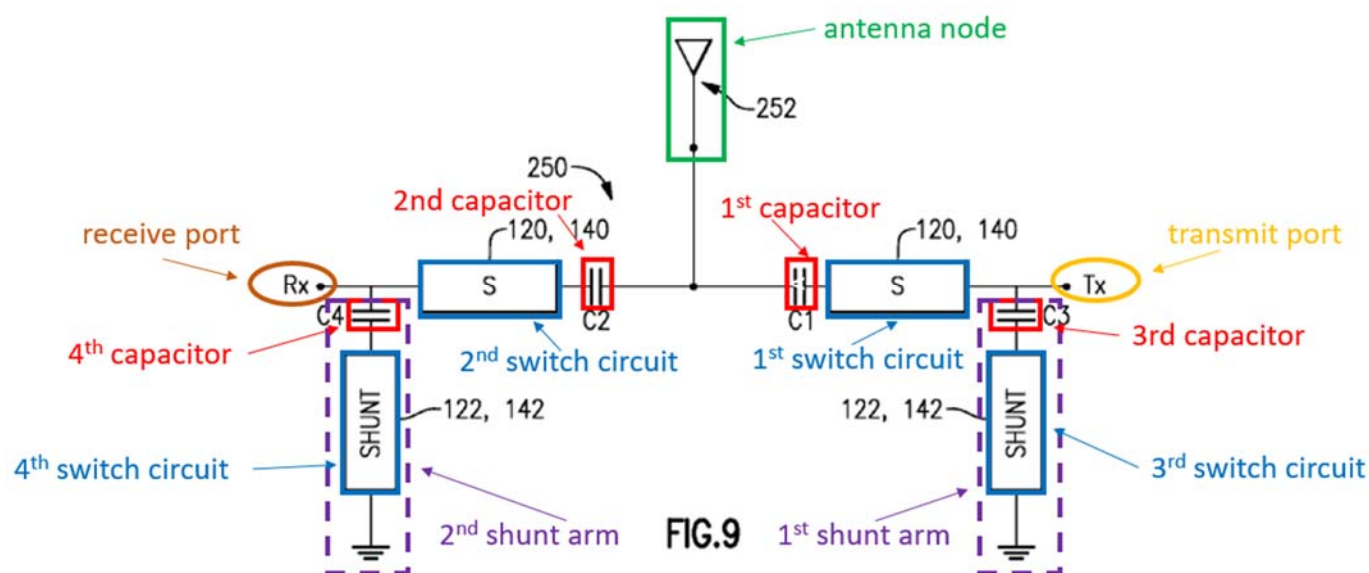
strive to reduce interference susceptibility through, for example, improved linearity... of the system building blocks, such as an RF switch.” EX-1001, 9:8-14, 5:21-55, 6:47-53, 7:5-8, FIG. 6; EX-1003, ¶35.

Second, the Patent discloses how including a “shunt arm” in each “throw” of the RF switch (e.g., SPDT switch of FIGS. 3-4, 9) is used to address this “interference susceptibility” problem. Referring to FIGS. 3 and 4 (above-annotated), the Patent describes “single pole 102a” [antenna] is “coupled to first and second throw nodes 104a, 104b [receive and transmit nodes respectively] via first and second... FETs[] 120a, 120b.” EX-1001, 3:45-50, 3:59-66, 4:31-36, 1:41-47, 9:22-30, FIGS. 2-4. Each “throw” node (104a, 104b) is “coupled to... RF ground” via a respective shunt FET (122a, 122b) to “provide shunting capability for the node.” EX-1001, 3:66-4:4, 4:37-41, FIGS. 3-4. During operation, “where an RF signal is being passed between... pole 102a and... first throw 104a”, (i) “FET 120a between... pole 102a and... first throw node 104a... [is]... ON”; (ii) “FET 120b between... pole 102a and... second throw node 104b... [is]... OFF”; (iii) Rx “shunt FET 122a... [is]... OFF... so that the RF signal is not shunted to ground as it travels from... pole 102a to... first throw node 104a”; and (iv) Tx “shunt FET 122b... [is]... ON... so that any RF signals or noise arriving... through the second throw node 104b is shunted to... ground so as to reduce

undesirable interference effects to the pole-to-first-throw operation.”⁵ EX-1001, 3:36-42, 4:5-18, 4:42-56; *see id.*, 9:22-38, 9:54-59, FIGS. 9-10; EX-1003, ¶36.

Third, the Patent states that the particular arrangement of RF switch components depicted in Figure 9 (below-annotated), and, specifically, the positioning of (i) “capacitor C1... between the antenna node and... switch arm S of the TX throw”; (ii) “capacitor C2... between the antenna node and... switch arm S of the RX throw”; (iii) “capacitor C3... between the TX node and its shunt switch”; and, (iv) “capacitor C4... between the RX node and its shunt switch”, “can lead to improvement in IMD performance, especially for low-frequency blocker signals”:

⁵ The same FIG. 3 and FIG. 4 configuration and operation of series and shunt FETs in SPDT RF switches, and described benefits and tradeoffs, were well-known to POSITAs (as evidenced by Patent Owner’s (“PO’s”) own article/whitepapers). EX-1024, 1, 3-4, FIG. 15; EX-1008, 3, Figure 1; EX-1039, 10, Figure 12; §V.F.2-§V.F.4; EX-1003, ¶36.



EX-1001, FIG. 9, 9:22-53, 9:64-10:3; 5:5-55, FIGS. 5-6, 10:11-27, FIGS. 11A-11D; EX-1003, ¶37. “With the foregoing capacitors, a low-frequency jammer signal can be blocked or reduced from mixing with any ON or OFF paths”, which “can provide improved IMD performance, by preventing a low-frequency blocker signal from mixing with a fundamental frequency signal.” EX-1001, 9:49-53, 9:39-41, 9:64-10:3; EX-1003, ¶37.

Unsurprisingly, given that a well-known, fundamental characteristic of all capacitors (with a given capacitance value, which designers can vary as appropriate) is that they have a **much** higher opposition (impedance) to low-frequency signals than high-frequency signals, outside of the positioning of the capacitors in the FIG. 9 SPDT switch, the '579 Patent leaves the remaining implementation details of this solution to design choices of POSITAs. *Id.*; §V.F.1-§V.F.3; EX-1003, ¶38. Indeed, the Patent does not provide **any** details as to, for example, (i) **how** the positioning of capacitors in

the FIG. 9 SPDT switch “prevent[s] a low-frequency blocker signal from mixing with a fundamental frequency signal”, (ii) **what value** the capacitors must have to perform this function, (iii) **where** the “low-frequency blocker signal” originates from, nor (iv) **what** constitutes a “low” frequency “blocker” signal relative to a “fundamental” frequency. *E.g.*, EX-1001, 6:19-7:13, 9:1-10:9; EX-1003, ¶39. Accordingly, and unsurprisingly, the Patent recognizes that this low-frequency-blocking-high-frequency-passing characteristic of capacitors was well-within the knowledge of POSITAs, and leaves the other implementation and operation details to design choices of POSITAs. *Id.*

The Patent states (i) “capacitors C1-C4 described in reference to FIGS. 9 and 10 can be implemented on the same die as their respective switch circuits, off of the die, or any combination thereof” (EX-1001, 9:60-63, 2:20-25), and (ii) “bias/coupling circuit 150” (*id.*, 5:5-55, FIGS. 5-6) “can be implemented” entirely/partially on the same die, or entirely/partially on a different die, as the die on which the SPDT switch is implemented (*id.*, 10:10-27, FIGS. 11A-11D). However, the Patent does not identify any benefits or tradeoffs associated with such design choices. Again, this lack of detail is not surprising as these were well-known design choices, with well-known advantages and tradeoffs, to POSITAs. §V.F.2-§V.F.4; EX-1003, ¶40.

B. Summary of the Prosecution History

As filed in August 2015, '579 Patent claim 1 originally recited:

A semiconductor die comprising:

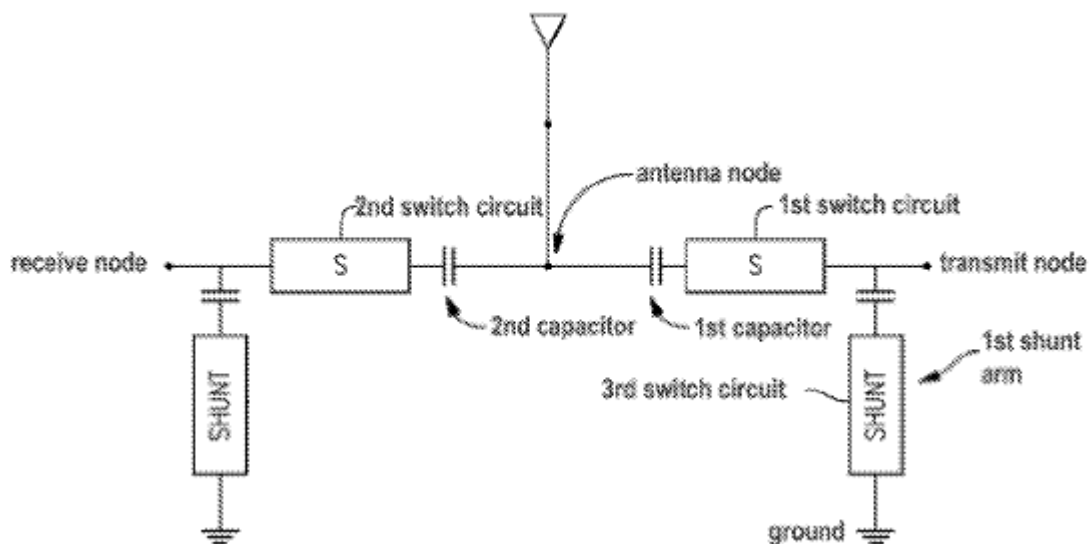
a semiconductor substrate;

a switch formed on the semiconductor substrate and including a stack of field effect transistors (FETs) connected in series; and

a capacitor formed on the semiconductor substrate and connected in series with the switch, the capacitor configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

EX-1002, 339-341 (“switch” and “capacitor” limitations are representative of original independent claims 9, 15); EX-1003, ¶43. All independent claims were rejected as obvious over Patent 7,265,604 (EX-1030) and Patent Publication 2011/0260773 (“Granger-Jones”, EX-1026), with the Examiner relying on Granger-Jones’ disclosure of “the capacitor configured to inhibit a low-frequency blocker signal...” limitation. EX-1002, 47-52; EX-1026, FIG. 2, [0033], [0040], [0049], [0063]; EX-1003, ¶44. In response, Applicant amended the independent claims, and specifically argued:

The features of [the] amended claim[s] can be understood with reference to Figure 9, which is provided in annotated form below:



The Applicant submits that the cited references fail to disclose or render obvious **the particular configuration** claimed in [the] amended claim[s], **particularly with respect to the positioning of the first and second capacitors with respect to the antenna node, and further with respect to the shunt arm.**

EX-1002, 37-39 (emphasis added). The amendments to claim 1 (below-reproduced with bracketed notations added) are representative of Applicant's amendments and arguments over the prior art of record:

[1.0] A semiconductor die comprising:

[1.1] a semiconductor substrate;

[1.2] a first switch circuit formed on the semiconductor substrate ~~and including a stack of field effect transistors (FETs) connected in series~~ connected between an antenna node and a transmit node; [[and]]

[1.3] a second switch circuit formed on the semiconductor substrate and connected between the antenna node and a receive node;

[1.4] a first capacitor formed on the semiconductor substrate and connected in series with the first switch circuit between the first switch circuit and the antenna node;

[1.5] a second, the capacitor formed on the semiconductor substrate and connected in series with the second switch circuit between the second switch circuit and the antenna node; and ~~configured to inhibit a low-frequency blocker signal from mixing with a fundamental frequency signal in the switch;~~⁶

⁶ Applicant deleted the “configured to inhibit a low frequency blocker...” limitation,

[1.6.1] a first shunt arm formed on the semiconductor substrate and connected to the first switch circuit and the transmit node, [1.6.2] the first shunt arm including a third switch circuit connected to ground.

EX-1002, 31-34.

The Examiner allowed the claims based on these amendments, and without providing any reasons for allowance, and the Patent issued September 20, 2016. EX-1002, 5, 11-18, EX-1003, ¶46.

C. Claim Construction

Petitioner proposes that each claim term in the Challenged Claims be given its plain and ordinary meaning in this proceeding, and that no specific construction of any claim term is required because the prior art relied on in this Petition meets each of the claim terms under any reasonable construction. EX-1003, ¶¶47-49.

D. Priority Date of the Challenged Claims

The '579 Patent was filed August 22, 2015, as a divisional of Patent No. 9,148,194, filed July 6, 2013, claiming priority to July 7, 2012. Therefore,

and added limitations reciting “the particular... positioning of the first and second capacitors with respect to the antenna node” depicted in '579 Patent Figure 9. As discussed in §V.A and §V.F.1-§V.F.2, the deleted limitation merely recites a fundamental characteristic of capacitors that was textbook knowledge toPOSITAs. §V.A (pp.13-14); §V.F.1-§V.F.2; EX-1003, ¶45.

Petitioner assumes the priority date is July 7, 2012.

E. Person of Ordinary Skill in the Art

A POSITA in July 2012 would have been someone knowledgeable and familiar with RF electronics, including RF switches and electrical components of such switches, and semiconductor manufacturing processes. POSITAs would have gained knowledge of these concepts through a mixture of training and work experience, such as by having a Bachelor's degree in electrical engineering, or related field, and approximately two to three years of related experience; or by obtaining a Master's degree in electrical engineering, or related field, but having only a year of related experience; or by having no formal education but experience in RF electronics and semiconductor packaging of at least six to eight years. EX-1003, ¶¶51.

F. State of the Art

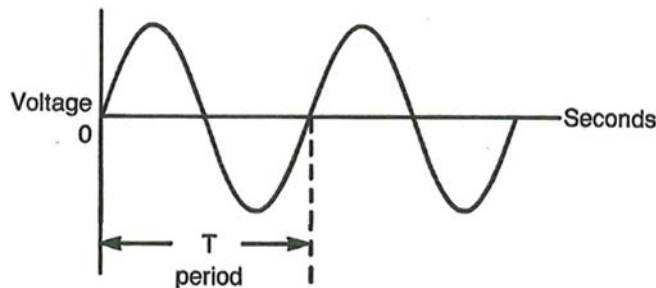
The following section describes the state of the art (*see* §V.E) as of July 2012. EX-1003 ¶42. The prior art references, and the discussions of what was known to POSITAs, provide the factual support for the general description of the state of the art in July 2012, and provide additional motivation to modify or combine teachings in the references and/or to make design choices given a reference's teachings. Accordingly, these references should be considered by the Board.

**1. Textbook EE Concepts Regarding Radio Frequency
Electrical Circuits and Capacitors in such Circuits**

There are several basic, textbook-type electrical engineering (EE) concepts

relevant to the state of the art. EX-1003, ¶55.

First, RF communications waveforms are routinely represented by an alternating current (AC) signal in which a single complete waveform is known as a “cycle”, and the number of cycles occurring in one second is the “frequency”, *i.e.*, frequency (f) is the rate at which a given waveform repeats, and is measured in hertz (1 Hz= 1 cycle/second):

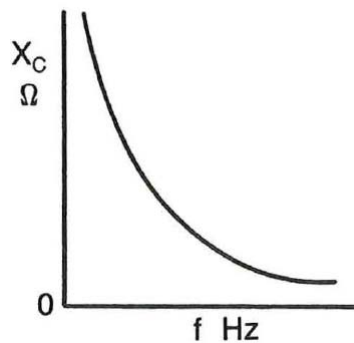


EX-1012, 200-201; EX-1027, 83; EX-1014, 30-31. The time interval taken by a complete cycle—“period” (T)—is the reciprocal value of frequency, measured in second(s). For example, a waveform with a frequency of 60Hz has a period of $1/60^{\text{th}}$ seconds. *Id.*; EX-1003 ¶56.

Second, capacitors “[t]o a first approximation... are devices that might be considered simply frequency-dependent resistors.” EX-1014, 20, 30; EX-1027, 82-83; EX-1012, 231-234; EX-1003 ¶¶57.⁷ A fundamental characteristic of all capacitors is

⁷ The classical construction of capacitors is two conductors near each other (but not touching), often with a thin insulating material (“dielectric”) therebetween; for greater

that their opposition to the flow of an AC waveform (*e.g.*, RF), called “capacitive reactance” (X_c) or, more generally, “impedance”, measured in ohms (Ω), is “*inversely* determined by the product of the frequency and the capacitance”, with this fundamental characteristic expressed in the equation $X_c = \frac{1}{2\pi fC}$ and shown in the below graph of X_c versus AC signal frequency (f):



EX-1012, 231-234 (original emphasis); EX-1027, 83; EX-1014, 29-32, 37 (Figure 1.56(A)); EX-1043, 128-129; EX-1024, 3-4; EX-1003 ¶58. Accordingly, all capacitors, regardless of capacitance value, have an essentially infinite opposition to DC current ($f=0\text{Hz}$); in other words, all capacitors block (*i.e.*, are essentially an open circuit to) the very low frequency that is DC current. EX-1012, 231-232, 175-176; EX-1027, 83, 50; EX-1014, 32, 36-37, 42; EX-1043, 128-129, 137-139; EX-1032, 1-2; EX-1033, 1; EX-1011, 2616-2617; EX-1026, [0049]; EX-1024, 3-4; EX-1031, 8-9, FIG. 13; EX-1003

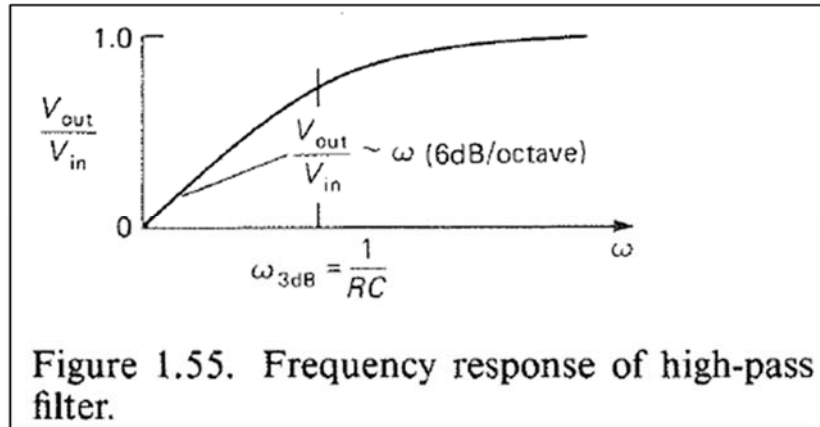
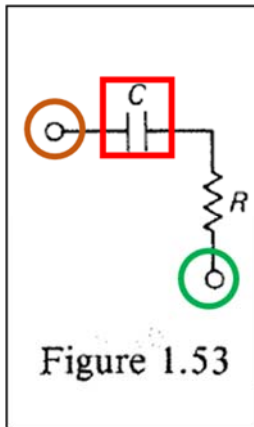
capacitance, larger sized conductors (more area), and closer spacing between conductors, is needed. EX-1014, 21, EX-1012, 158; EX-1027, 48-51; EX-1003 ¶57.

¶59. As the frequency of the in-series current increases, the impedance drops; at a sufficiently high frequency signal (for a given size capacitor) the impedance drops to the point where the capacitor approximates a conductor. *Id.*; EX-1003 ¶59.

As a simple example of the fundamental low-frequency-blocking, and high-frequency-passing, characteristic of typical capacitors used in typical RF switches, a 10pF capacitor has an impedance X_c of $\sim 16,000\Omega$ to 1MHz signals, $\sim 84\Omega$ to 190MHz signals, and $\sim 7\Omega$ to 2.4GHz signals. *Id.*; EX-1011, 2616-2617 (10pf); EX-1024, 3 (5-15pf); EX-1010, [0040] (8.4pF); EX-1029, 36-39 (20pF, 2.7pF); EX-1017, [0025]; EX-1014, 32; EX-1027, 83; EX-1012, 232-234; EX-1003 ¶60.

Third, due to this fundamental characteristic of capacitors, a basic high-pass filter (having the “desirable property of passing [high] signal frequencies of interest while rejecting undesired [low] signal frequencies”) was, as shown in the EE textbook figure reproduced below left (and annotated), simply a capacitor connected in series between the RF waveform source node and output node, and in series with a resistor (where the “50-ohm standard impedance for RF circuits” is commonly used as this resistor value), and with the fundamental “-3dB ‘breakpoint’” of this filter expressed in the equation $f_{3dB} = \frac{1}{2\pi RC}$ and shown in the graph (below right) of signal amplitude reduction (as a fractional ratio) versus AC signal frequency (in radians (ω ⁸):

⁸ Radians (ω) were a well-known shorthand expression of $2\pi f$. EX-1014, 30, 36-37;



EX-1014, 36-37 (Figures 1.52-1.55), 39-40; EX-1043, 137-139, 236-238, FIGS. 5-17(A), 8-17(B), 8-17(D), 8-18(B), 8-18(D); EX-1044, 1-2; EX-1011, 2617-2618 (FIG. 9(a)), 2x10pF capacitors/throw, $f_{3dB}=636.9\text{MHz}$); EX-1024, 3 (“system characteristic impedance (normally 50Ω)”), Figure 15 (2x 5-15pF capacitors/throw, $f_{3dB}=1.27\text{GHz}$ to 424.MHz); EX-1036, 2; EX-1040, 4-5; EX-1019, [0179]; EX-1017, 2:55-58; EX-1007, [0029]; EX-1010, [0040] (2x8.4pF capacitors/throw, $f_{3dB}=757.9\text{MHz}$); EX-1003 ¶61.

The EE-textbook-type “-3dB ‘breakpoint’” (f_{3dB}) of this fundamental high-pass filter is the low-frequency value at which the input AC signal amplitude “is reduced to 0.707 of its maximum” and where, if an even more-attenuated filter fall-off point was desired for the particular application, POSITAs understood such amplitude “is reduced to 0.45 of its maximum at $f_{[3dB]}/2\dots$, to 0.25 of its maximum at $f_{[3dB]}/4\dots$, to 0.125 of its maximum at $f_{[3dB]}/8\dots$ ” and so on. *Id.*; EX-1003 ¶62.

Selecting a capacitance value of capacitors in RF switches based on, for example,

EX-1003 ¶61.

desired (fundamental) frequency values (for which designers want capacitors to essentially act as short circuits, *i.e.*, pass through as very low-impedance resistors), practical size constraints, and low frequencies of undesired, potentially interfering signals (for which designers want capacitors to essentially act as open circuits, *i.e.*, block as very high-impedance resistors), was widely known to, and well-within the skill and creativity of, POSITAs. EX-1014, 36-37; EX-1043, 137-139, EX-1026, FIG. 2, [0002], [0040], [0049], [0051], [0063]; EX-1011, 2615-2618; EX-1009, FIG. 2, [0083]-[0084]; EX-1024, 3; EX-1032, 1-2, FIG. 1; EX-1031, 8-9, FIG. 13; EX-1035, 5; EX-1042, 294, 298, 308, 312; EX-1003 ¶63.

Accordingly, given these well-known factors, typical capacitance values were well-known to be in picofarads (pF) or nanofarads (nF) for use in semiconductor-based RF switches. *Id.*; EX-1024, 3 (5-15pF); EX-1011, 2616-2617 (10pF); EX-1010, [0040]; EX-1033, 1 (47pF); EX-1029, 36-39 (20pF, 2.7pF); EX-1042, 96, 172, 180, 227, 275, 286 (22pF, 47pF, 4.7pF); EX-1031, 8-9 (100pF); EX-1017, [0025]; *see* EX-1014, 21; EX-1012, 158-159; EX-1003 ¶64.

2. Well-Known Operation and Performance Evaluation of Single-Pole-Multi-Throw (SPnT) Transistor Switches

Single-Pole-Multi-Throw (“SPnT”) (*e.g.*, SPDT) switches, including those using semiconductor-based FETs, were well-known and widely used in RF applications. EX-1024, 1, 4; EX-1021, 1; EX-1010, [0002]-[0009]; EX-1023, 1:13-24, 3:43-47; EX-1039, 1, 9-10; EX-1041, 1; EX-1003, ¶65.

PO's June 2009 article ("Cory") states "[t]here is a class of switches, commonly known as transmit-receive (T-R) switches, used in transceiver applications whose function is to connect the antenna to the transmitter... in the transmit state and to the receiver during the receiver state", and describes the operation of widely-used SPnT switches for such transceiver applications. EX-1024, 1, 3-4; EX-1003, ¶66.

Cory, and other prior art PO publications, explain that "typical" SPnT switches, used in high-power, multi-mode, high-fundamental-RF-frequency applications, included (i) series and shunt FET switch circuits to shunt "OFF" path high-power, high-frequency signals to ground to prevent them from "leaking into" the "ON" path, (ii) FET control circuitry whose design impacted "isolation", "insertion loss", and "linearity" performance parameters, (iii) "stack[ed]... FETs" for increased power handling, and (iv) capacitors with "quite small (5 to 15pf)" "capacitor values" where "[t]he selection of the capacitor values is critical to insure proper frequency operation and bandwidth":

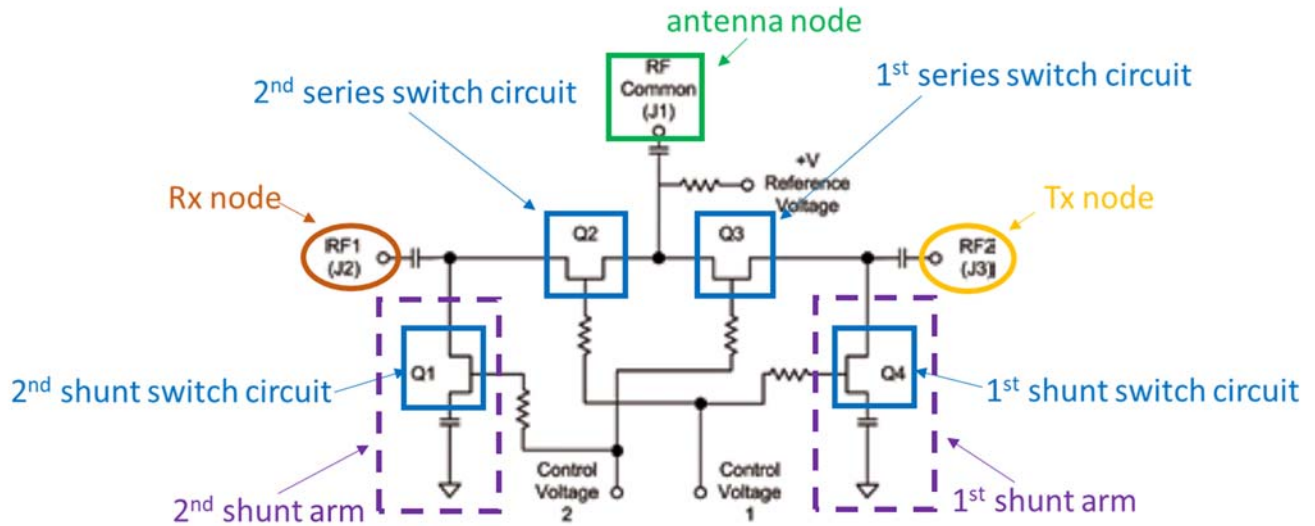
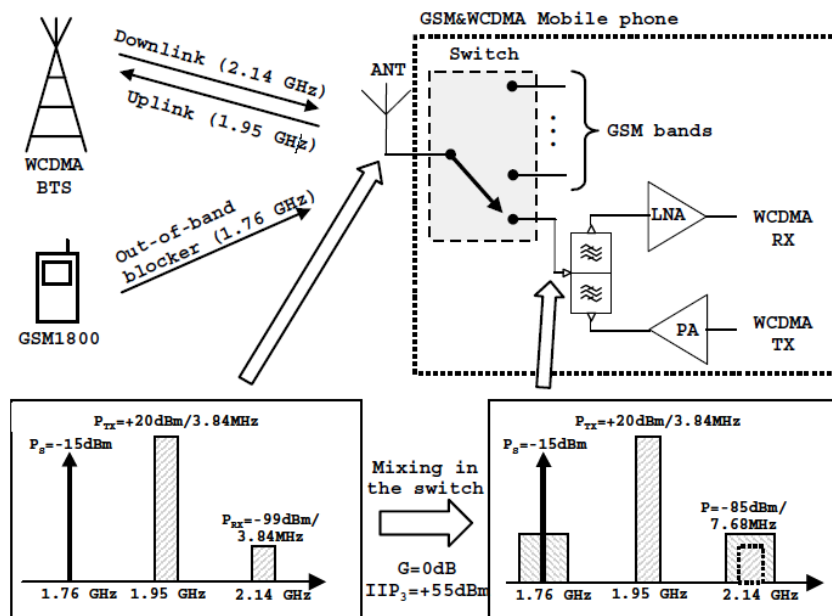


Figure 15: Single Pole Two Throw Switch

EX-1024, 1, 3-5; EX-1039, 4-6, 9-11; EX-1041, 1-2; EX-1008, 3; EX-1023, 5:44-53; §V.F.1; §V.F.4; EX-1003, ¶67.

PO's May 2011 whitepaper (and relied-on 2005 paper) explain that another well-known consideration in designing RF switches in wireless devices, especially those operating in “multi-mode and multiband” environments, was that, if an “unwanted” signal (*e.g.*, “out-of-band blocking” signal at $f_{blocker}$) is allowed to mix with a “wanted” (“fundamental”) RF signal (*e.g.*, f_{TX} , f_{RX}) in an RF switch, the desired transmitted/received information may be degraded, further “unwanted” signals (*e.g.*, IMD products (*e.g.*, $f_{TX}-f_{blocker}$ (IMD₂), $2f_{TX}-f_{blocker}$ (IMD₃)), “harmonics” (*e.g.*, $2f_{TX}$, $3f_{RX}$), etc.) may be created, and calls could be dropped. EX-1039, 2-6, 8-12 *citing* EX-1040, 3-6; *see also* EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1049, p.3; EX-1003, ¶68.

In the below-illustrated example, a phone's antenna ("ANT") may pick-up "out-of-band blocker" signals transmitted in the area (e.g., $f_{blocker}=1760\text{MHz}$) and, if the RF switch's "linearity is poor", those antenna-picked-up-signals would "mix" with "fundamental" frequency signals (e.g., $f_{TX}=1950\text{MHz}$) inside the switch, and produce IMD_2 (e.g., $f_{TX}-f_{blocker}=190\text{MHz}$) and IMD_3 (e.g., $2f_{TX}-f_{blocker}=2140\text{MHz}$) products, where the IMD_2 product mixing with the same "fundamental" frequency signal (e.g., $1950\text{MHz}+190\text{MHz}=2140\text{MHz}$), or the IMD_3 product (e.g., 2140MHz), could be "right at the" phone's desired Rx/downlink fundamental frequency causing interference (and possibly dropped calls):



Band	TX f_{TX}	RX f_{RX}	IMD2 low	IMD3	IMD2 high
			Blocker 1 $f_{TX} + f_{S1} = f_{RX}$	Blocker 2 $2f_{TX} - f_{S2} = f_{RX}$	Blocker 3 $f_{S3} - f_{TX} = f_{RX}$
850	836.5	881.5	45	791.5	1718
1900	1880	1960	80	1800	3840
2100	1950	2140	190	1760	4090

Fig. 4. Dominating out-of-band blocking mechanisms and center frequencies for the 850, 1900 and 2100 WCDMA bands.

Id.; EX-1003, ¶69. As explained therein and illustrated above, the same result could occur in the same example for antenna-picked-up-blocker signals at 190MHz, *e.g.*, “TV transmission” signals. *Id.*; EX-1045, 1 (“174.0-216.0MHz” is “Broadcasting (TV Channels 7-13)” spectrum); EX-1046, 23-24 (“[T]he radio system... must be able to reject signals outside the band without loss of performance. These signals may be very large (*e.g.* TV transmissions)... [N]on-linearities in the receiver... will allow unwanted signals to intermodulate... [which] may result in a distortion product falling onto the wanted signal...”); EX-1003, ¶70.

As further explained therein, typical solutions to “minimize[]” the “distortion products for current dependent nonlinearity” in RF switches, *e.g.*, “nonlinear series resistance[]... of the OFF paths”, involved “adjusting the phase so... the switch sees an open circuit at the blocker frequency.” *Id.*; EX-1040, 5; EX-1046, 23-24; EX-1003, ¶71.

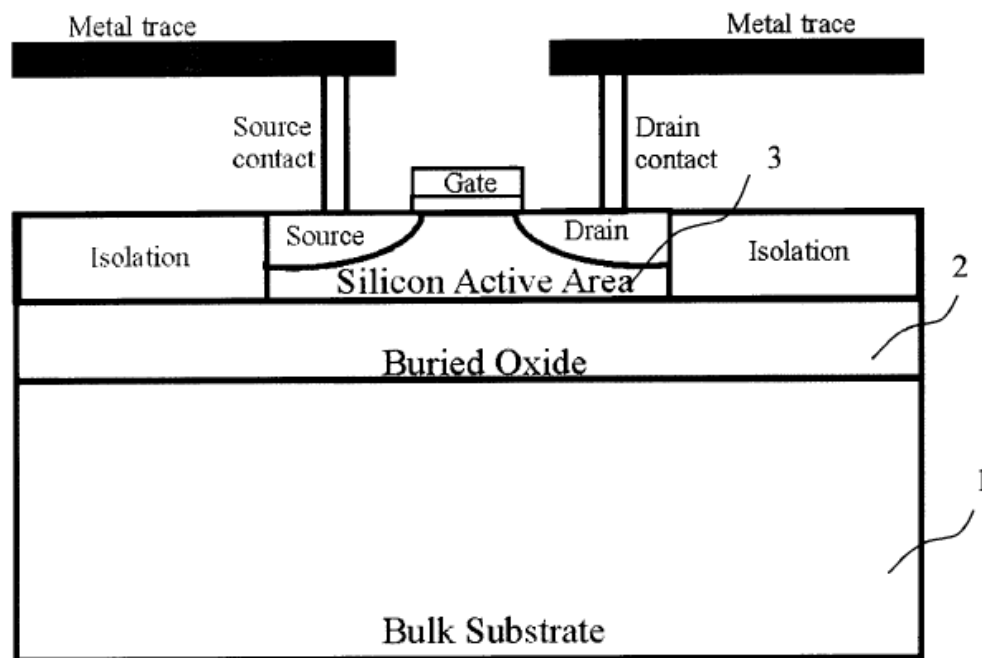
3. Well-Known Manufacturing Processes to Form SPnT Components on Semiconductor Substrates/Wafers of Semiconductor Dies and Well-Known Monolithic Integrated Circuits Incorporating the Same

Regarding well-known manufacturing processes and packaging of RF Transmit-

Receive switches (including SPDT switches), Cory discloses examples of pHEMT FETs, for which fabricating semiconductor material, *e.g.*, GaAs, is grown on a “semi-insulating substrate” that “inherently isolates one FET structure from another,” and whereby the switch components (“FET structures”, “metal-insulator-metal (MIM) capacitors”, etc.) are formed “on or near the top-most layer” of **the same** wafer. EX-1024, 1, 3-4, Figure 8; EX-1039, 9-10; EX-1003, ¶72.

A well-known design choice to POSITAs involved selecting whether to form the SPnT switch capacitors on the same semiconductor substrate of the same die/chip as the FETs, or to incorporate (*e.g.*, in a packaged RF switch module, FEM, etc.) “external” capacitors in the packaging design, where such capacitors would be off of the die/chip on which the FETs were formed (*e.g.*, formed on a separate substrate of a separate die, surface-mounted to a packaging substrate, etc.). EX-1032, 1-2; EX-1034, FIG. 2; EX-1035, 2-5 (for HEMT-FET-SPDT switch: “It is desirable to use... On chip MIM... capacitor[s] instead of... external capacitor[s]... **It is possible to use... external capacitor[s], but since multiple capacitors are required,** the cost of the external capacitor[s]... and **the cost** of connecting [them] to the switch **increase significantly...** **On chip MIM capacitor[s] can be easily manufactured through a semiconductor process and do[] not require additional work.”); EX-1023, 10:13-17, 8:29-37, 5:59-6:21, FIG. 5; EX-1011, 2616-2617, FIG. 4; EX-1029, FIGS. 1-2, pp.35-36, 40; EX-1003, ¶73.**

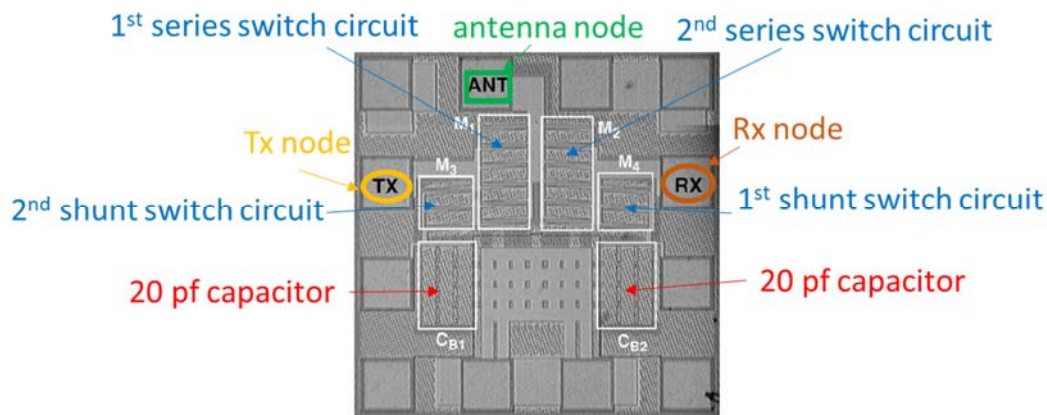
A well-known alternative to using pHEMT FETs—fabricating the SPnT switch components, including series and shunt FETs, in silicon, including silicon-on-insulator (SOI), grown over a substrate (example below)—had well-understood benefits (*e.g.*, lower cost, higher “thermal conductivity”, reduced “degradation in bandwidth associated with the stacking of FET devices”, “reduce[d] dielectric losses associated with the silicon substrate”, allowing monolithic (same die/chip) integration of SPnT switch and control components and other front-end module (FEM) components, etc.), and trade-offs requiring additional design considerations (*e.g.*, silicon substrates are conductive, accumulated charge in off-state MOSFETs, etc.):



EX-1020, 7:17-18, 8:17-25, 10:5-11, 8:28-29, 1:10-14, 12:27-31, FIGS. 1, 4, 16; , EX-1026, [0030]; EX-1039, 9-10; EX-1005 [0040], [0043]; EX-1009, FIG. 2, [0004]-[0005], [0050], [0054], [0058], [0074], [0126], [0142], FIGS. 8-10, 12-14; EX-1018,

4:27-41, 3:50-54, FIGS. 3-4; EX-1010, [0009], [0013], FIG. 3A, [0034]-[0036], [0046]; EX-1022, [0028], FIG. 7, [0046]-[0050]; EX-1025, Abstract, 16:11-18, 16:56-61, 20:57-67, FIGS. 12, 17; EX-1019, [0001], [0004], FIGS. 1, 9, 19, [0013]-[0021], [0073]-[0079], [0148]-[0149], [0159], [0184]-[0191], [0199]-[0200], 68:36-69:21, 70:10-24; §V.B (EX-1002, 47-52); EX-1003, ¶74.

A few examples of the monolithic (same die/chip) integration benefits resulting from forming SPnT switches on silicon substrates, including SOI, are provided below:



EX-1029, FIGS. 1-2, pp.35-36, 40; *see* EX-1039, FIG. 12;

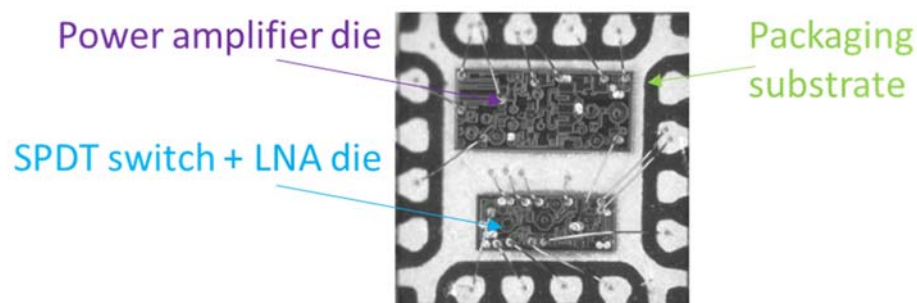


Fig.2. The high linearity 4.9-5.9 GHz FEM in a 3 x 3 mm QFN package.

EX-1028, FIGS. 2, 4, 5, pp.2-3; EX-1036, 1-2 (“RF testing is performed at the package level... RF wafer probe [testing] is performed on 100% of the RF switch

die used in Skyworks FEMs.”);

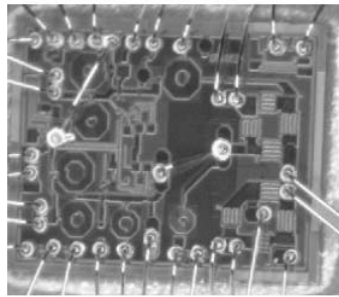


Fig. 1. Die photo for the SP4T T/R switch with dual-band LNA and bypass attenuators. The die size is 1.2x1.6 mm².

EX-1021, FIGS. 1-2, 4-5, pp.2-3;

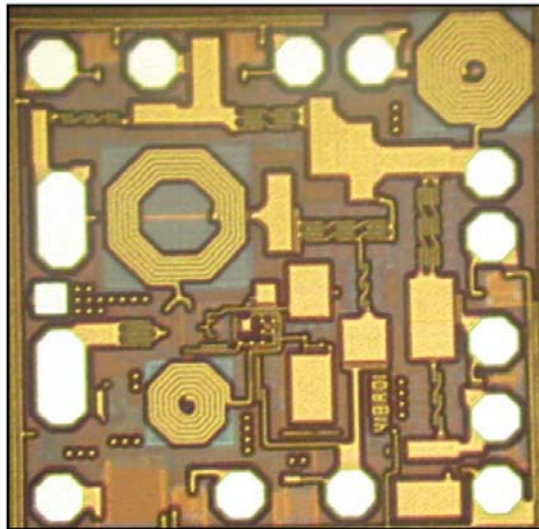


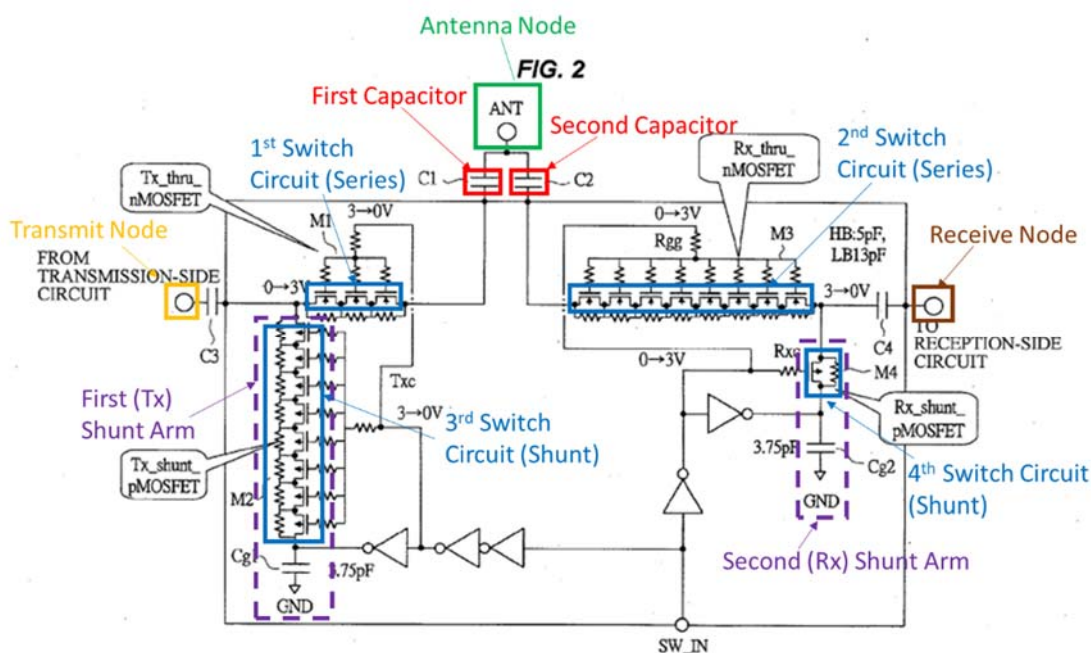
Fig. 8. Die micrograph of the FEIC.

The front-end integrated circuit (FEIC)... **integrates a SP3T switch and a low-noise amplifier with bypass mode**... [T]he fabricated die... shown in Fig. 8... include[es] **on-chip** dc blocking and decoupling MIM capacitors.
EX-1011, FIGS. 1-2, 4-6, 8, 2613-2617; *see* §V.F.4; EX-1003, ¶75.

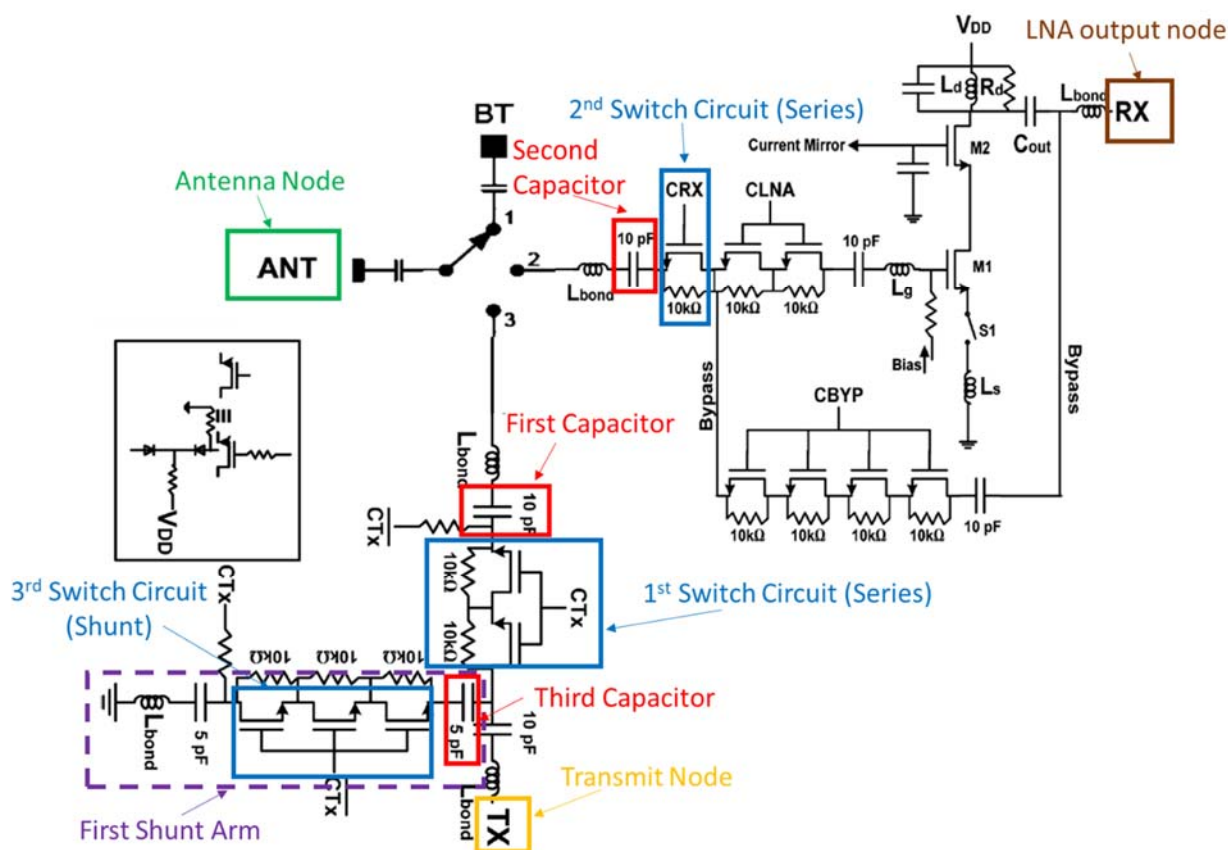
4. Exemplary Known Component Configurations in Series and Shunt Switch Arms of SPnT Transmit-Receive Switches in RF Transceiver Applications

By July 2012, as detailed in the Grounds (§VI-§VII below), and shown and

described in the below additional examples, the “particular configuration” of components in SPnT transmit-receive switches of wireless devices—including the positioning of capacitors with respect to the antenna, transmit and receive nodes, and the use of shunt arms, as recited in the Challenged Claims—and for purposes of reducing well-known interference susceptibility, and improving other well-known switch performance parameters, were well-known:



EX-1009, FIG. 2 (annotated), [0005], [0060]-[0067], [0074]-[0078], [0083]-[0084];



EX-1011, FIGS. 2, 4, 6 (combined/annotated above), 2613-2617, FIG. 8 (§V.F.3); *see* EX-1010, FIG. 3A, [0034]-[0036]; EX-1003, ¶76.

5. Transistor SPnT Switches Were Widely Used in RF Transceiver Applications

Numerous prior art references (examples below) confirm Cory's described configuration—a Transmit-Receive switch module (*e.g.*, SPDT module) interconnected between an antenna and a transceiver configured to process RF signals (*see* §V.F.2)—was the conventional, well-known, widely-used configuration for RF applications (*e.g.*, mobile devices):

FIG. 3 depicts... WLAN front-end module (FEM)... 10... coupled to... antenna 20 and... transceiver 30... Within... FEM 10 are both a transmit

path and receive path... In a preferred implementation of... FEM 10...
switch 90 is a SPDT T/R switch...

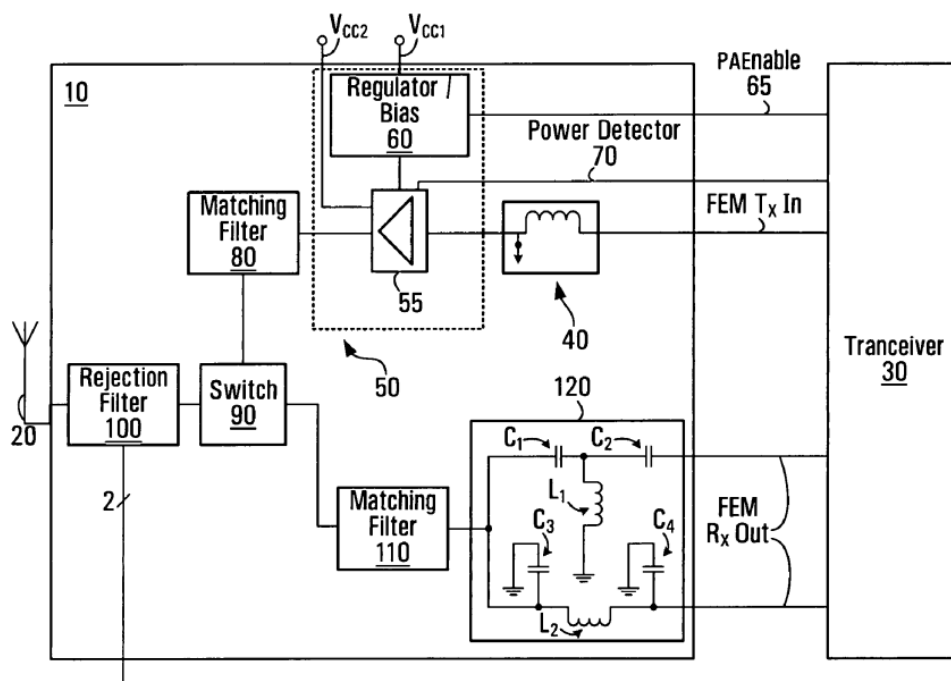


FIG. 3

EX-1023, FIG. 3, 1:43-67; 1:7-9, 1:13-24, FIG. 6, 7:50-52;

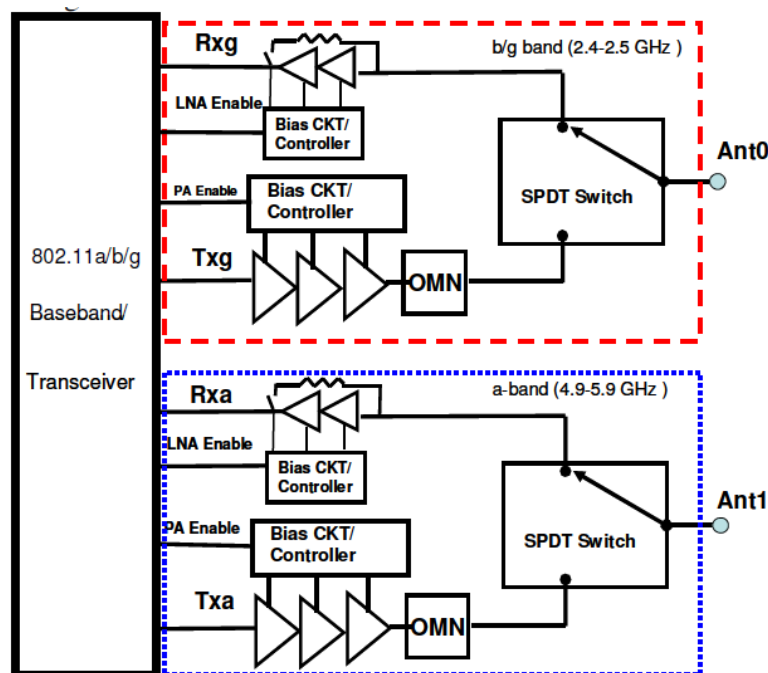


Fig. 1. Block diagram of a dual-band WLAN radio.

EX-1028, 1, FIG. 1;

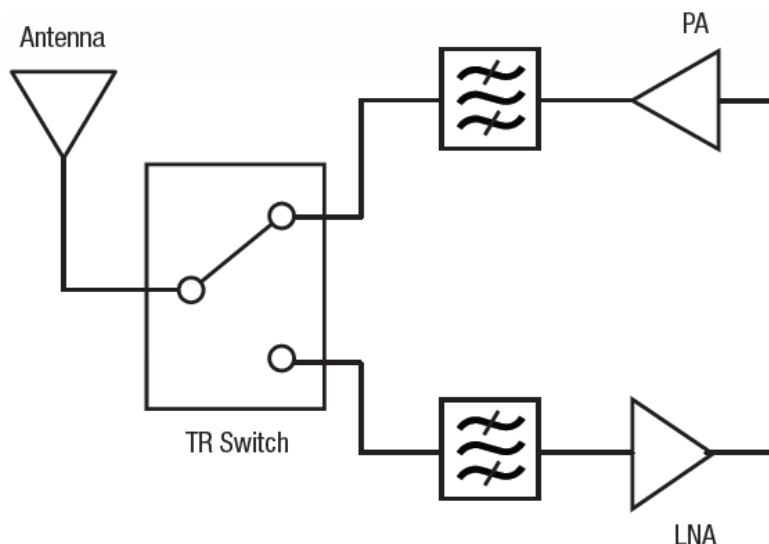


Figure 3. Simplified TR Switching Block Diagram

EX-1008, 3; *see* EX-1041, 1; EX-1039, 1, 3-4, Figures 3-4; EX-1017, FIG. 5, [0027], [0001], [0016], [0018]; EX-1022, [0004]; EX-1025, FIG. 12, 15:24-33, 16:19-18:7, Abstract; EX-1003, ¶77.

VI. IDENTIFICATION OF CHALLENGES

A. Challenged Claims

This Petition challenges '579 Patent claims 1-3, 7-9, and 13-15.

B. Statutory Grounds for Challenges

The Challenges are set forth in detail below and summarized as follows:

Ground	Claims	Basis	Reference(s)
1	1-3, 7-9, 13-15	§103	Huang in view of the knowledge, skill and creativity ("Knowledge") of POSITAs
2	1-3, 7-9, 13-15	§103	Seshimo in view of the Knowledge of POSITAs

Huang (EX-1005) is Patent Publication No. 2011/0254614, filed April 16, 2010 and published October 20, 2011. Huang is prior art at least under (pre-AIA) §102(a).

Seshimo (EX-1006/EX-1007) is Patent Publication No. JP2006-121217A, filed October 19, 2004 and published May 11, 2006. EX-1007 is the certified English translation of EX-1006, and all citations to Seshimo are to EX-1007. Seshimo is prior art at least under (pre-AIA) §102(b).

Neither reference was cited, nor applied by the Examiner, during the '579 Patent prosecution.

VII. IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE

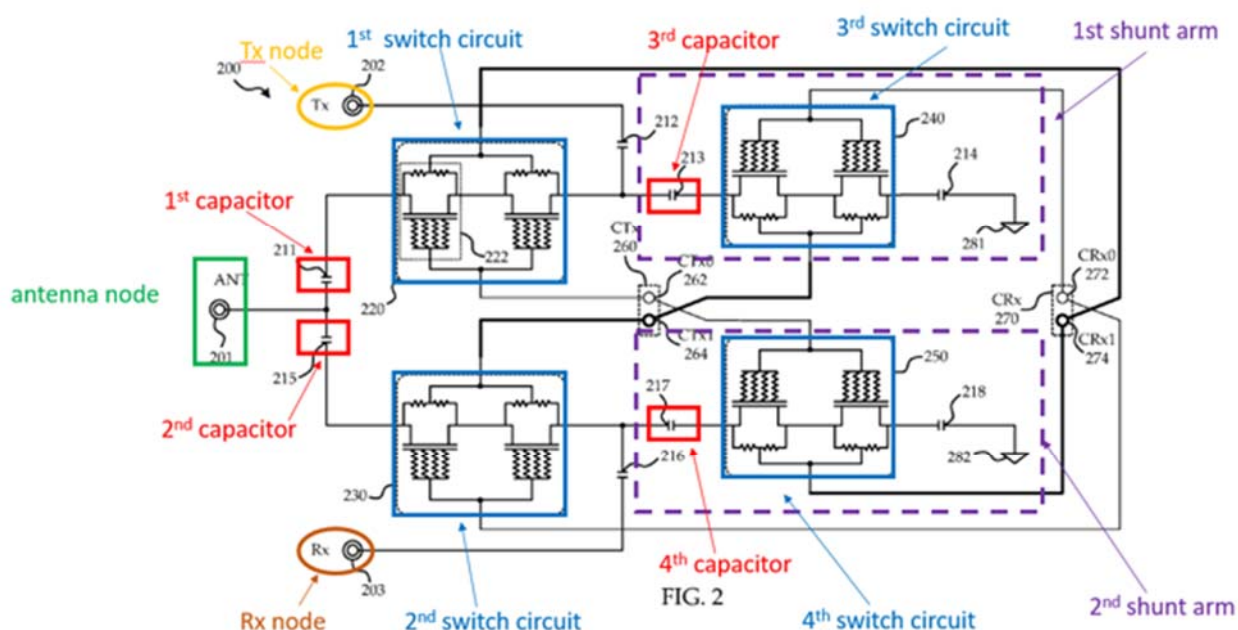
A. Ground 1: Claims 1-3, 7-9, and 13-15 are obvious under §103(a) over Huang in view of the Knowledge of POSITAs

1. Huang

Huang discloses the identical “particular configuration” of components as '579 Patent FIG. 9, in a “semiconductor-based high power switch” of a wireless device (*e.g.*, “WLAN radio”), specifically a “SPDT... transmit-receive switch” formed “using... SOI” technology:

- “first series FET group switch 220” connected between “antenna 201” and “transmit terminal 202”;
- “second series FET group switch 230” connected between “antenna 201” and “receive terminal 203”;
- “blocking capacitor 211” “coupled in series with... first series FET group

- switch 220” and connected between Tx-series-switch 220 and antenna 201;
- “blocking capacitor 215” “coupled in series with... second series FET group switch 230” and connected between Rx-series-switch 230 and antenna 201;
 - first shunt arm connected to Tx-series-switch 220 and transmit terminal 202, including (i) “first shunt FET group switch 240” connected to ground, and (ii) “blocking capacitor 213” connected “in series with... first shunt FET group switch 240” and connected between this shunt switch 240 and transmit terminal 202; and
 - second shunt arm connected to Rx-series-switch 230 and receive terminal 203, including (i) “second shunt FET group switch 250” connected to ground, and (ii) “blocking capacitor 217” connected “in series with... second shunt FET group switch 250” and connected between this shunt switch 250 and receive terminal 203:



EX-1005, Abstract, [0001]-[0002], [0122], [0040], [0042]-[0043], claims 5, 19, [0044]-[0045], FIG. 2 (above-annotated), [0051]; §V.A-§V.B; EX-1003, ¶79.

Huang also discloses the identical operation of the semiconductor-based, series and shunt FET switches in SPDT switch 200 as the '579 Patent. EX-1005, [0056] (transmission), [0058] (reception), Annotated FIG. 2; §V.A; EX-1003, ¶80.

Like the '579 Patent, Huang discloses that the particular configuration of the above-identified series and shunt components in the high-power SPDT transmit-receive switch, formed using SOI technology, and controlled FET biasing when the SPDT is in transmit, or receive, modes, achieves desirable switching performance parameters including “low insertion loss along the signal path”, “high isolation from the off paths”, “improved signal quality”, “reduce[d] spurious harmonic transmissions”, and “good linearity.” EX-1005, [0002]-[0003], [0039]-[0040], [0043], [0056]; §V.A; EX-1003,

¶81.

2. Detailed Application of Huang in View of the Knowledge of POSITAs to the Challenged Claims

a. Claim 1

i. [1.0] A semiconductor die comprising:

To the extent the preamble is limiting, Huang discloses a semiconductor die, including a semiconductor substrate on which the components of the disclosed single-pole-dual-throw (SPDT) transmit-receive switch are formed, to POSITAs. EX-1003, ¶82. Huang states “[t]he invention relates to high power semiconductor switches”, and discloses the “transistor switches” in such high power, “semiconductor-based transmit-receive switches”, including SPDT switch 200, can be “silicon-on-insulator FET switches.” EX-1005, [0001]-[0003], Abstract, [0040], [0042]-[0043], [0122], claims 5, 19, FIG. 2; EX-1003, ¶83. Accordingly, POSITAs reading Huang would understand Huang discloses that all of the components of the SPDT switch 200 are formed on a semiconductor substrate of a semiconductor die, where, in some embodiments, the semiconductor die is a silicon-on-insulator (SOI) die in which the SPDT switch 200 components would be formed on an insulator layer. *Id.*

To the extent PO asserts that Huang does not explicitly state that the SPDT switch 200 components are formed on a semiconductor substrate of a semiconductor die, it would have been obvious to POSITAs to do so, as this was the well-known and widely-implemented approach to provide a stable foundation for fabrication of

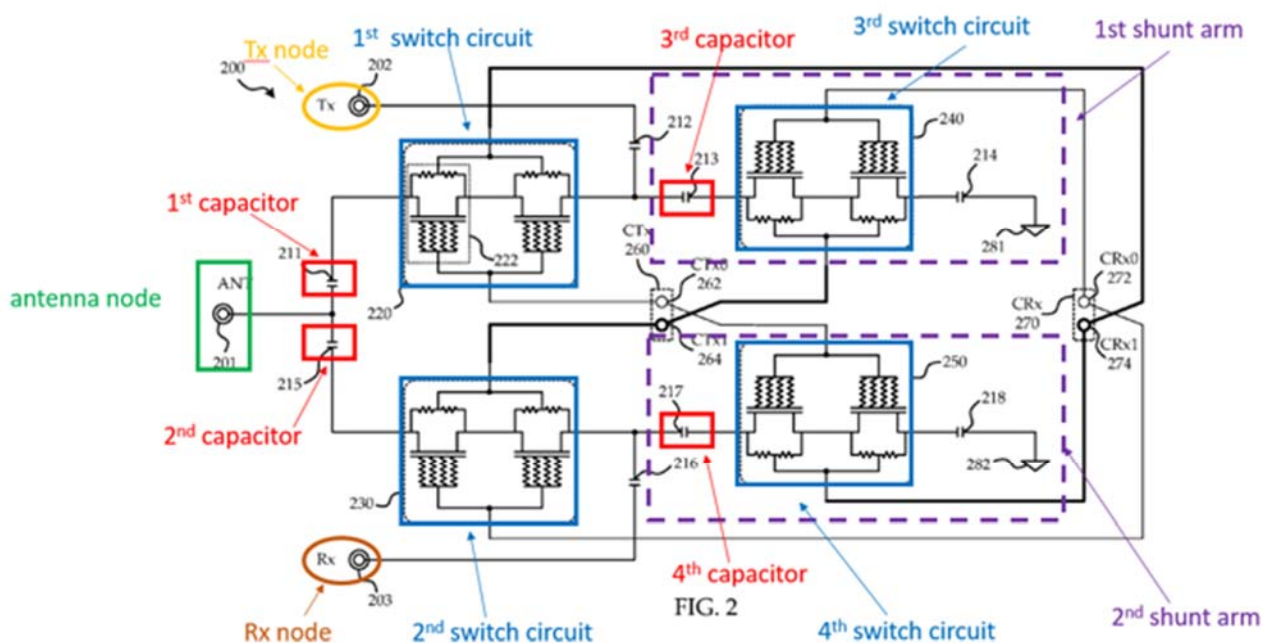
components of high-power, semiconductor-based, transmit/receive switches, and in order to make manufacturing, testing and production of integrated circuits (“ICs”) (including such switches and related circuits (*e.g.*, LNAs)) easier and less costly as discussed in the State of the Art section. *Id.*; §V.F.3 (EX-1018, 4:27-41; EX-1010, [0009], [0013], FIG. 3A, [0046]; EX-1019, [0001], [0004], FIG. 1; EX-1039, 9-10, FIG. 12; EX-1020, FIGS. 1, 4; EX-1009, [0004]-[0005], [0058], FIG. 2; EX-1022, FIG. 7, [0046]-[0050]; EX-1024, 1, 3-4, FIG. 8; EX-1029, FIGS. 1-2, 35-36, 40; EX-1028, 2-3, FIGS. 2, 4, 5; EX-1021, 2-3, FIGS. 1-2, 4-5; EX-1019, [0001], [0004], FIG. 1; EX-1011, 2613-2617, FIGS. 1-2, 4-6, 8; EX-1036, 1-2); EX-1003, ¶84.

ii. [1.1] a semiconductor substrate;

Huang discloses this limitation for the reasons discussed regarding [1.0].

iii. [1.2] a first switch circuit formed on the semiconductor substrate connected between an antenna node and a transmit node;

Huang discloses SPDT switch 200 includes “[first series FET group switch 220](#)” that may be a “silicon-on-insulator FET switch” (*first switch circuit formed on the semiconductor substrate*), and is connected between [antenna 201](#) (*antenna node*) and [transmit terminal 202](#) (*transmit node*) as illustrated in FIG. 2 as annotated below (“Annotated FIG. 2”):



EX-1005, [0045], [0122], claims 5, 19; EX-1003, ¶86. Huang also discloses that each “FET group switch” (220, 230, 240, 250) includes multiple FETs connected in series to each other. *Id.*; EX-1005, [0003], [0040].

iv. [1.3] a second switch circuit formed on the semiconductor substrate and connected between the antenna node and a receive node;

Huang discloses SPDT switch 200 includes “second series FET group switch 230” that may be a “silicon-on-insulator FET switch” (*second switch circuit formed on the semiconductor substrate*), and is connected between antenna 201 (*antenna node*) and receive terminal 203 (*receive node*) as shown in Annotated FIG 2. EX-1005, [0045], [0122], claims 5, 19; EX-1003, ¶87.

- v. *[1.4] a first capacitor formed on the semiconductor substrate and connected in series with the first switch circuit between the first switch circuit and the antenna node;*

Huang discloses “semiconductor-based” SPDT switch 200 includes “**blocking capacitor 211**” (*first capacitor formed on the semiconductor substrate*) that is “coupled in series with... **first series FET group switch 220**” (*first switch circuit*) and connected between the **first series FET group switch 220** and **antenna 201** (*antenna node*) as shown in Annotated FIG. 2. EX-1005, [0045]; *id.*, [0001]-[0003], Abstract, [0040], [0042]-[0043], [0122]; EX-1003, ¶88.

To the extent PO asserts that Huang does not explicitly disclose forming “**blocking capacitor 211**” (and, *e.g.*, “**blocking capacitor 213**”) on the same semiconductor (*e.g.*, SOI) substrate of the same semiconductor die as the other components (*e.g.*, SOI FETs) of SPDT switch 200, as discussed in the State of the Art sections, POSITAs would have been motivated to do so as a mere design choice to achieve known and predictable benefits, including making manufacturing, testing, and production of SPDT switch 200 (and ICs incorporating the same) easier and less costly, with a reasonable expectation of success, including because low capacitance value (picofarad) capacitors are small in size and typically used in RF switches since, as was well-known to POSITAs, they would pass (with very low impedance) the high frequencies-of-interest (*e.g.*, 2.4GHz associated with “traditional WLAN radio[s]”) while impeding low, out-of-band-blocker frequencies. *Id.*; §V.F.3 (EX-1034, FIG. 2;

EX-1035, 2-5; EX-1023, 10:13-17, FIG. 5; EX-1011, 2616-2617, FIG. 4; EX-1029, FIGS. 1-2, pp.35-36, 40; EX-1022, [0028], FIG. 7, [0046]-[0050]; EX-1010, [0009], [0013], FIG. 3A, [0046]); §V.F.1 (EX-1012, 231-234, 175-176; EX-1027, 82-83, 50; EX-1014, 29-32, 36-37, 42; EX-1043, 128-129, 137-139, 236-238; EX-1032, 1-2; EX-1033, 1; EX-1011, 2615-2618; EX-1026, [0049]; EX-1024, 3-4; EX-1031, 8-9; EX-1044, 1-2; EX-1010, [0040]; EX-1009, FIG. 2, [0083]-[0084], EX-1035, 5; EX-1042, 96, 172, 180, 227, 275, 286; EX-1029, 36-39; EX-1017, [0025]); §V.F.2 (EX-1024, 1, 3-4; EX-1039, FIG. 5, 2-6, 9-12 (*citing* EX-1040, 3-6, FIGS. 3-4); EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1045, 1, EX-1049, p.3); *see* [7.3] (below); EX-1003, ¶89.

vi. [1.5] a second capacitor formed on the semiconductor substrate and connected in series with the second switch circuit between the second switch circuit and the antenna node; and

Per [1.4] (above), Huang discloses SPDT switch 200 includes “**blocking capacitor 215**” (*second capacitor formed on the semiconductor substrate*) that is “coupled in series with a **second series FET group switch 230**” (*second switch circuit*), and connected between **second series FET group switch 230** (*second switch circuit*) and **antenna 201** (*antenna node*) as shown in Annotated FIG. 2. EX-1005, [0045]; *id.*, [0001]-[0003], Abstract, [0040], [0042]-[0043], [0122]; *see* [1.4]; EX-1003, ¶90.

- vii. [1.6.1] a first shunt arm formed on the semiconductor substrate and connected to the first switch circuit and the transmit node,**

Huang discloses “[a]long a shunt path from the transmit terminal 202 to... transmit branch ground connection 281, the transmit terminal 202 is coupled to... a blocking capacitor 213 in series with a first shunt FET group switch 240...” as shown in Annotated FIG. 2. EX-1005, [0045]; §V.B (EX-1002, 37-39); EX-1003, ¶91.

Accordingly, POSITAs would understand Huang discloses SPDT switch 200 including, as shown in Annotated FIG. 2, a first shunt arm that (i) is formed on the semiconductor substrate (see [1.0], [1.4]), (ii) is connected to the first series FET group switch 220 (first switch circuit) and transmit terminal 202 (transmit node), and (iii) includes (among other components) a first shunt FET group switch 240, that may be a “silicon-on-insulator FET switch”, and that is connected to “the transmit branch ground connection 281” (third switch circuit connected to ground). *Id.*, EX-1005, [0001]-[0003], Abstract, [0040], [0042]-[0043], [0122], claims 5, 19; §VII.A.2 [1.0]; EX-1003, ¶92.

- viii. [1.6.2] the first shunt arm including a third switch circuit connected to ground.**

Huang discloses this limitation for the reasons discussed regarding [1.6.1].

b. Claim 2

- i. The semiconductor die of claim 1 further comprising an insulator layer disposed between the first and**

second switch circuits and the semiconductor substrate.

As explained in [1.0], Huang discloses SPDT switch 200 is a “semiconductor-based”, “high-power transmit-receive switch”, that may be “implement[ed]... using silicon on insulator (SOI)” technology, with its “transistor switches” (220, 230, 240, 250) being “silicon on insulator FET switches.” EX-1005, [0001]-[0003], Abstract, [0040], [0042]-[0043], [0122], claims 5, 19; EX-1003, ¶94.

Unsurprisingly, Huang does not disclose the well-known details of implementing SOI technology to manufacture the SOI FET switches of the “semiconductor-based high power switches”, *e.g.*, SPDT switch 200, of “the invention.” *Id.* Indeed, as described in the State of the Art section, it was well-known that, in using SOI technology to create ICs, an insulator layer is deposited onto a semiconductor substrate of a semiconductor die, silicon is grown on top of this insulator layer, and then the silicon is patterned and etched to create the various components of the IC (*e.g.*, FETs, capacitors, etc. of SPDT switch 200). §V.F.3 (EX-1020, FIGS. 1, 4, 8:17-25, 7:12, 7:17-18, 10:5-11, 8:28-29, 1:10-14, 12:27-13:8, FIG. 16; EX-1026, [0030]; EX-1018, 4:27-41, 3:50-54, FIGS. 3-4; EX-1039, 9-10, FIG. 10); EX-1003, ¶95. Accordingly, POSITAs understood Huang’s implementation of SOI included an insulator layer disposed between the SOI **first (220)** and **second (230)** series FET group switches (*first and second switch circuits*) and the semiconductor substrate. *Id.*; EX-1005, [0001]-[0003], Abstract, [0040], [0042]-[0043], [0122], claims 5, 19; EX-1003, ¶96.

To the extent PO asserts that Huang does not expressly disclose an insulator layer disposed between the SOI **first** (220) and **second** (230) series FET group switches and the semiconductor substrate, it would have been obvious to POSITAs to do so as this was the well-known and widely-implemented approach to using the disclosed SOI technology to manufacture “semiconductor-based high power switches”, such as SPDT switch 200, with well-known and predictable benefits including, for example, lower cost, higher “thermal conductivity”, reduced “degradation in bandwidth associated with the stacking of FET devices”, “reduce[d] dielectric losses associated with the silicon substrate”, allowing monolithic (same die/chip) integration of SPnT switch and control components and other front-end module (FEM) components, etc. *Id.*; §V.F.3 (EX-1018, 4:37-41; EX-1026, [0030]; EX-1021, 2; EX-1009, [0005]; EX-1010, [0013]); EX-1003, ¶97.

c. Claim 3

- i. The semiconductor die of claim 2 wherein the semiconductor die is a silicon-on-insulator (SOI) die.*

Huang discloses this limitation for the reasons discussed regarding claim 2.

d. Claim 7

- i. [7.0] A method for operating a radio-frequency (RF) device, the method comprising:*

To the extent the preamble is limiting, Huang discloses that SPDT switch 200 may be “utilized in a traditional WLAN radio”, which POSITAs understood refers to “wireless LAN radio”, and that, “[i]n modern RF communication systems a

semiconductor-based transmit receive switch is often the last/first component encountered by a transmitted/received signal before/after encountering an antenna.” EX-1005, [0051], [0002], [0044]-[0045], FIG. 2; [1.0]. Huang also discloses methods for operating SPDT switch 200 in such RF/wireless devices (“WLAN radio”, “modern RF communication system”). *Id.*; EX-1005, [0055]-[0059]. Accordingly, Huang discloses a method for operating a radio-frequency (RF) device to POSITAs. *Id.*; EX-1003, ¶99.

ii. [7.1.1] providing an RF device including

Huang discloses this limitation for the reasons discussed regarding [7.0].

iii. [7.1.2] a first switch circuit connected between an antenna node and a transmit node, [7.1.3] a second switch circuit connected between the antenna node and a receiver node, [7.1.4] a first capacitor connected in series with the first switch circuit⁹ between the first switch circuit and the antenna node, [7.1.5] a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node, and [7.1.6] a first shunt arm connected to the first switch circuit and the transmit node, [7.1.7] the first shunt arm including a third switch circuit connected to ground;

Huang discloses these limitations for the reasons discussed regarding [1.2]-

⁹ Petitioner assumes “first switch circuity” is a typographical error and, solely for purposes of this petition, interprets this limitation as “first switch circuit.” *See* [7.1.2], [7.1.6], [7.2].

[1.6.2].

- iv. *[7.2] controlling an RF switch of the RF device by placing the first switch circuit in an ON state and placing the third switch circuit in an OFF state; and*

Huang discloses controlling SPDT switch 200 (*an RF switch*) of the RF device (see [7.0]) by: “when... antenna 201 is utilized for transmission, the first series FET group switch 220 [*first switch circuit*] and... second shunt FET group switch 250 are provided with on-state Vgsd... while the second series FET group switch 230 and... first shunt FET group switch 240 [*third switch circuit*] are provided off-state Vgsd wherein no channel is established.” EX-1005, [0056], Annotated FIG. 2; EX-1003, ¶108.

- v. *[7.3] inhibiting a low-frequency blocker signal from mixing with a fundamental-frequency signal in the RF switch using the first capacitor.*

Huang discloses this limitation to POSITAs. EX-1003 ¶109. As discussed in [1.4]-[1.5], Huang discloses positioning, in SPDT switch 200 (*the RF switch*) as shown in Annotated FIG. 2 (see [1.2]), (i) blocking capacitor 211 (*the first capacitor*) between antenna 201 and Tx series FET group switch 220, and (ii) blocking capacitor 215 between antenna 201 and Rx series FET group switch 230. Huang’s disclosure is identical to the ’579 Patent’s disclosed positioning in its FIG. 9 SPDT switch 250, (i) capacitor C1 between antenna node 252 and Tx series switch circuit 120/140, and (ii) capacitor C2 between antenna node 252 and Rx series switch circuit 120/140. EX-

1005, [0045], §V.B (EX-1002, 31-34, 37-39, 47-48, 339-341); §V.A (EX-1001, 9:39-53, FIG. 9); EX-1003, ¶¶109-110.

Huang also discloses the importance of selecting the “arrange[ment]” of “groups of FETs” and “judiciously chosen... capacitors”, and of selecting the biasing voltages of the FETs when in “on” and “off” states, in “a high power transmit-receive switch using... SOI” to achieve, for example, “low insertion loss along the signal path”, “high isolation from the off paths”, “reduce[d] spurious harmonic emissions”, and “improve[d] linearity” for the switch. EX-1005, [0002]-[0003], [0039]-[0040], [0043]-[0045], [0055]-[0059]; EX-1003, ¶111. Moreover, Huang expressly refers to capacitor 211 (*the first capacitor*) as “**blocking capacitor 211**” and, as discussed in [1.2], [1.4] and [7.0], Huang discloses, in SPDT switch 200 intended for use in “modern RF communication systems” (e.g., “WLAN radio”) (*the RF device*), that “**antenna 201** is coupled to... **blocking capacitor 211** coupled in series with... **first series FET group switch 220**” “**along a signal path** from... **antenna 201** to... **transmit terminal 202**.” *Id.*; EX-1005, [0051]; *see* [1.2], [1.4], [7.0]; EX-1003, ¶112.

Unsurprisingly, just like the ’579 Patent, given the fundamental, frequency-dependent impedance characteristic of capacitors—capacitors allow high frequencies to pass through (essentially acting as short circuits) while blocking low frequencies (essentially acting as open circuits)—outside of specifying the identical arrangement of **blocking capacitor 211** (*the first capacitor*) in SPDT switch 200 as the Applicant’s

relied-on arrangement, Huang leaves the particular capacitor value implementation details to design choices of POSITAs. *Id.*

Moreover, given this fundamental, frequency-dependent impedance characteristic of capacitors, the typical (picofarad) capacitor values selected for RF switches in Huang’s disclosed use cases, and the known solution—having “the switch see[] an open circuit at the blocker frequencies”—to the well-known low-frequency, “out-of-band blocker” signal problem in non-linear RF switches, POSITAs understood Huang’s disclosed implementation of **blocking capacitor 211** in SPDT switch 200 as being a high-pass filter that would “inhibit[] a low-frequency blocker signal from mixing with a fundamental frequency signal in the RF switch.” *Id.*, §V.F.1 (EX-1012, 231-234, 175-176; EX-1027, 82-83, 50; EX-1014, 20, 30, 29-32, 36-37, 39-40, 42, FIGS. 1.52-1.55, 1.56(A); EX-1043, 128-129, 137-139, 236-238, FIGS. 5-17(A), 8-17(B), 8-17(D), 8-18(B), 8-18(D); EX-1011, 2615-2618, FIG. 9A; EX-1024, 3-4; EX-1026, [0049]; EX-1031, 8-9, FIG. 13; EX-1010, [0040]; EX-1044, 1-2; EX-1029, 36-39; EX-1032, 1-2; EX-1033, 1; EX-1042, 96, 172, 180, 227, 275, 286; EX-1017, [0025]); §V.F.2 (EX-1039, FIG. 5, 2-6, 8-12 (*citing* EX-1040, 3-6, FIGS. 3-4); EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1045, 1, EX-1049, p.3); EX-1003, ¶114.

Furthermore, to the extent PO asserts that Huang does not expressly disclose **blocking capacitor 211** performing this step in SPDT switch 200, with the SPDT switch 200 components arranged as shown in Annotated FIG. 2, and opposing series and shunt

switches placed in ON and OFF states depending on the transmit or receive mode of SPDT switch 200 as disclosed by Huang, POSITAs understood **this capacitor's** inhibition of low-frequency blocker signals from mixing with fundamental frequency signals in SPDT switch 200 to merely be a matter of design choice. *Id.*; EX-1003, ¶115.

As discussed in the State of the Art section, because blocking capacitor 211 is a fundamentally frequency-dependent circuit element (with decreasing impedance with increasing frequency), POSITAs understood that tuning the resulting high-pass filter, *i.e.*, setting the frequency range above which **blocking capacitor 211** permits frequencies (*e.g.* the desired RF frequency) to pass essentially unimpeded, and below which (*e.g.*, the “-3dB breakpoint”) it impedes lower frequencies (*e.g.*, low-frequency “out-of-band blocker” signals), is simply a matter of picking the size capacitor that yields the desired pass/inhibit thresholds within the practical size constraints for the RF device (*e.g.*, “traditional WLAN radio”) with a reasonable expectation of success. *Id.*; *see also* §V.F.1 (EX-1009, FIG. 2, [0083], [0084]; EX-1035, 5; EX-1032, FIG. 1; EX-1026, FIG. 2, [0002], [0040], [0049], [0051], [0063]; EX-1042, 294, 298, 308, 312); EX-1049, p.3; EX-1003, ¶116. Filtering **antenna-201**-picked-up, low-frequency, out-of-band-blocker signals was a well-known problem in RF radios, with a well-known solution (*i.e.*, a series capacitor sized to yield the desired frequency-dependent response as a high-pass filter within the practical size constraints for the RF device). *Id.*; EX-1003, ¶117.

Accordingly, POSITAs would have been motivated to select an appropriately-sized **blocking capacitor 211** to pass (with very low impedance) the high frequencies-of-interest (*e.g.*, 2.4Ghz associated with “traditional WLAN radio[s]”), while impeding low, out-of-band frequencies, within the practical size constraints of such radios, to achieve the known and predictable benefits of improved switch performance (including improved IMD performance) with a reasonable expectation of success given that this involves nothing more than the conventional and routine use of Huang’s **blocking capacitors**. *Id.*; EX-1003, ¶118.

e. Claim 8

- i. The method of claim 7 wherein the first switch circuit is formed on an insulator layer disposed between the first switch circuit and a semiconductor substrate.*

Huang discloses this limitation for the reasons discussed regarding claim 2 and [1.0], [1.1].

f. Claim 9

- i. The method of claim 7 wherein the RF switch is a silicon-on-insulator (SOI) switch.*

Huang discloses this limitation for the reasons discussed regarding claims 2, 3.

g. Claim 13

- i. [13.0] A wireless device comprising:*

To the extent the preamble is limiting, Huang discloses this limitation for the reasons discussed regarding [7.0]-[7.1.1].

ii. [13.1] a transceiver configured to process RF signals;

As discussed in [7.0], Huang discloses incorporating SPDT switch 200 (*switch module*) into an RF/wireless device (e.g., “WLAN radio”), in which such switch “is often the last/first component encountered by a transmitted/received signal before/after encountering an antenna” (e.g., **antenna 201**) (*antenna*). EX-1005, [0051], [0002], [0044]-[0045], [0051], FIG. 2. Huang also discloses methods for operating SPDT switch 200 (*switch module*) when incorporated into such wireless devices, “when the [antenna 201/SPDT switch 200] is utilized for transmission” and, separately, “when the SPDT switch 200 is utilized for reception.” *Id.*; EX-1005, [0055]-[0059].

Accordingly, POSITAs reading Huang would understand it discloses *a transceiver* configured to process RF signals, which is in communication with **antenna 201** (*antenna*) via, in part, SPDT switch 200 (*a switch module*), which is interconnected to **antenna 201** and the transceiver and configured to selectively route RF signals to and from the antenna. *Id.*; see also §V.F.5 (EX-1023, FIG. 3, 1:43-67, 1:7-9, 1:13-24, FIG. 6, 7:50-52; EX-1028, 1, FIG. 1; EX-1008, 3; EX-1041, 1; EX-1039, 1, 3-4, Figures 3-4; EX-1017, FIG. 5, [0027], [0001], [0016], [0018]; EX-1022, [0004]; EX-1025, FIG. 12, 15:24-33, 16:19-18:7, Abstract); EX-1003, ¶¶122-123.

iii. [13.2] an antenna in communication with the transceiver; and

Huang discloses this limitation for the reasons discussed regarding [13.1].

- iv. *[13.3] a switch module interconnected to the antenna and the transceiver and configured to selectively route RF signals to and from the antenna,*

Huang discloses this limitation for the reasons discussed regarding [13.1].

- v. *[13.4.1] the switch module including a first switch connected between the antenna and a transmit node, [13.4.2] a second switch connected between the antenna and a receive node, [13.4.3] a first capacitor connected in series with the first switch between the first switch and the antenna, [13.4.4] a second capacitor connected in series with the second switch between the second switch and the antenna, and [13.4.5] a first shunt arm connected to the first switch and the transmit node, [13.4.6] the first shunt arm including a third switch connected to ground.*

Huang discloses these limitations for the reasons discussed regarding [1.2]-[1.6.2].

h. Claim 14

- i. *The wireless device of claim 13 wherein the first switch is formed on a silicon-on-insulator (SOI) die of the wireless device.*

Huang discloses this limitation for the reasons discussed regarding claims 2, 3 and [1.0], [1.1].

i. Claim 15

- i. *The wireless device of claim 13 wherein the first capacitor is part of the same semiconductor die as the first switch.*

Huang discloses this limitation for the reasons discussed regarding [1.4], [1.0], [1.1].

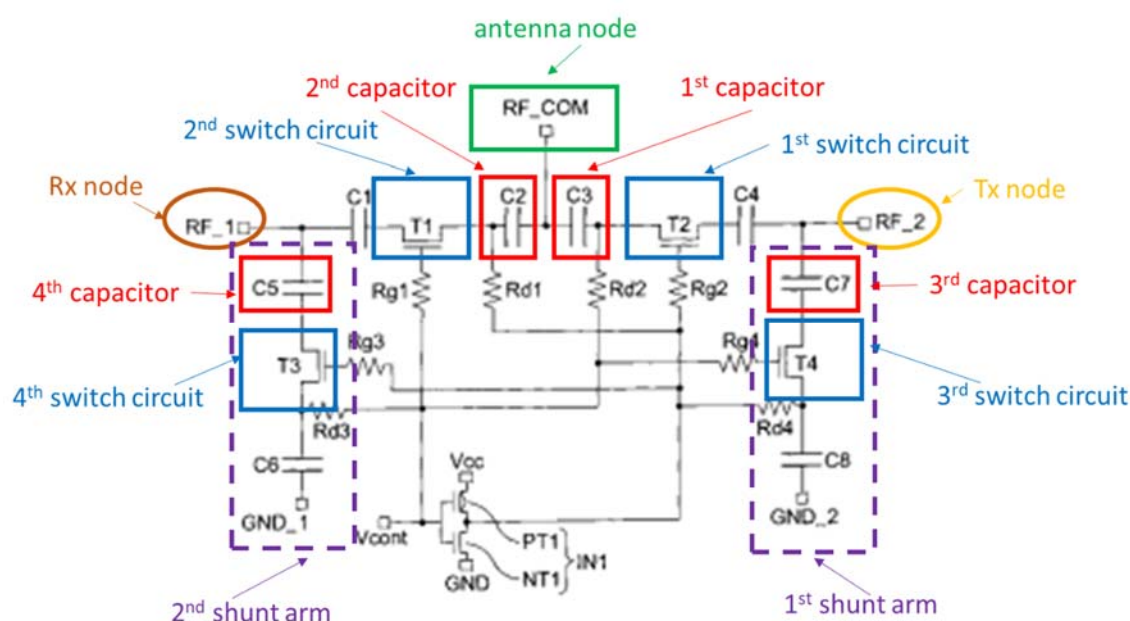
B. Ground 2: Claims 1-3, 7-9, and 13-15 are obvious under 35 U.S.C. §103(a) over Seshimo in view of the Knowledge of POSITAs

1. Seshimo

Seshimo discloses the same “particular configuration” of components as ’579 Patent FIG. 9, in a “high frequency semiconductor switching circuit... used as a transmission/reception changeover switch” (FIG. 3 “shunt SPDT switch”) of a wireless device (*e.g.*, “PHS (Personal Handyphone System)”):

- “MOSFET T2” connected between “common terminal RF_COM” (*antenna node*) and “high-frequency signal terminal RF_2” (*transmit node*);
- “MOSFET T1” connected between common terminal RF_COM and “high-frequency signal terminal RF_1” (*receive node*);
- “capacitor C3” connected in series with MOSFET T2, and connected between MOSFET T2 and common terminal RF_COM;
- “capacitor C2” connected in series with MOSFET T1, and positioned between MOSFET T1 and common terminal RF_COM;
- first shunt arm (i) connected to MOSFET T2 and high-frequency signal terminal RF_2 (*transmit node*), includes (ii) “MOSFET T4” connected to “high-frequency ground terminal GND” (*ground*), and includes (iii) “capacitor C7” connected in series with MOSFET T4 and positioned between MOSFET T4 and high-frequency signal terminal RF_2;

- **second shunt arm** (i) connected to **MOSFET T1** and **high-frequency signal terminal RF_1** (receive node), includes (ii) “**MOSFET T3**” connected to “high-frequency ground terminal GND”, and includes (iii) “**capacitor C5**” connected in series with **MOSFET T3** and positioned between **MOSFET T3** and **high-frequency signal terminal RF_1**:



EX-1007, [0001], [0003], [0005], [0007], [0029], [0037], [0042], [0054]-[0056], [0065]-[0072], [0090], FIG. 3 (above-annotated); §V.A-§V.B; EX-1003, ¶135.

Seshimo also discloses the identical operation of its series and shunt MOSFETs “formed on a silicon substrate” in the “high frequency semiconductor switching circuit... used as a transmission/reception changeover switch” (FIG. 3 SPDT switch) as the ’579 Patent. *Id.*; EX-1007, [0065]-[0066] (e.g., transmission), [0067]-[0068] (e.g., reception); §V.A; EX-1003, ¶136.

Like the '579 Patent, Seshimo discloses that the particular configuration of the above-identified series and shunt components in the “high frequency semiconductor switching circuit... used as a transmission/reception changeover switch”, formed using CMOS processes and SOI, and controlled FET biasing when the SPDT is in transmit, or receive, modes, achieves desirable switching performance parameters including “improving the maximum permissible input [power/amplitude] to maintain an OFF state” (*e.g.*, power usable by PHS), and “suppressing an increase in ON resistance” (that, without suppression, would “lead to an increase in insertion loss” and a “deterioration in isolation”). EX-1007, [0002]-[0005], [0007], [0011], [0026]-[0030], [0037], [0039]-[0040], [0042]-[0043], [0054]-[0056], [0065]-[0072], [0090]; §V.A; EX-1003, ¶137.

2. Detailed Application of Seshimo in View of the Knowledge of POSITAs to the Challenged Claims

a. Claim 1

i. [1.0] A semiconductor die comprising:

To the extent the preamble is limiting, Seshimo discloses a semiconductor die, including a semiconductor (*e.g.*, silicon, “SOI (Silicon on Insulator)”, etc.) substrate on which the components of the disclosed “high-frequency semiconductor switching circuit” (*e.g.*, FIG. 3 SPDT switch) are formed. EX-1003 ¶138.

Seshimo discloses “[t]he present invention... is particularly suitable for high-frequency semiconductor switching circuit including a MOSFET formed on a silicon

substrate”, “the use of SOI is also effective in the present invention”, that the SPDT components and control circuits all “may be configured as CMOS circuits and integrated on the same semiconductor substrate”, and identifies well-known benefits of “develop[ing] high-frequency semiconductor switching circuits using CMOS processes”, namely “that a CMOS switch can be integrated into another CMOS RF IC.” EX-1007, [0001], [0003], [0007], [0054], [0084], [0088]; EX-1003 ¶139. Accordingly, POSITAs would have understood Seshimo discloses that all of components of the FIG. 3 SPDT switch are formed on a semiconductor substrate of a semiconductor die, where, in some embodiments, the semiconductor die is a SOI die in which the SPDT switch components would be formed on an insulator layer. *Id.*; EX-1003, ¶139.

To the extent PO asserts that Seshimo does not explicitly disclose the FIG. 3 SPDT switch components are formed on a semiconductor substrate of a semiconductor die, it would have been obvious to POSITAs to do so, because, as discussed in the State of the Art section, this was the well-known and widely implemented approach to provide a stable foundation for fabrication of components of high-power, semiconductor-based, transmit/receive switches, and in order to make manufacturing, testing and production of ICs (including such switches and related circuits (*e.g.*, LNAs) easier and less costly. *Id.*; §V.F.3 (EX-1018, 4:27-41; EX-1010, [0009], [0013], FIG. 3A, [0046]; EX-1019, [0001], [0004], FIG. 1; EX-1039, 9-10, FIG. 12; EX-1020, FIGS. 1, 4; EX-1009, [0004]-[0005], [0058], FIG. 2; EX-1022, FIG. 7, [0046]-[0050]; EX-

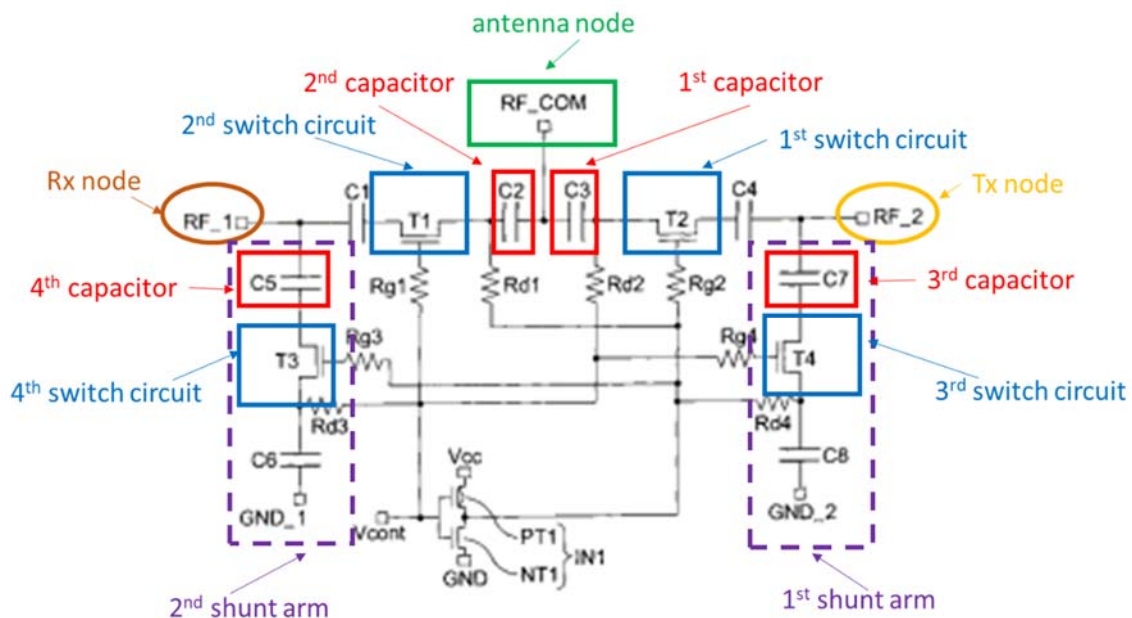
1024, 1, 3-4, FIG. 8; EX-1029, FIGS. 1-2, 35-36, 40; EX-1028, 2-3, FIGS. 2, 4, 5; EX-1021, 2-3, FIGS. 1-2, 4-5; EX-1019, [0001], [0004], FIG. 1; EX-1011, 2613-2617, FIGS. 1-2, 4-6, 8; EX-1036, 1-2); EX-1003, ¶140.

ii. [1.1] a semiconductor substrate;

Seshimo discloses this limitation for the reasons discussed regarding [1.0].

iii. [1.2] a first switch circuit formed on the semiconductor substrate connected between an antenna node and a transmit node;

Seshimo discloses a “shunt SPDT switch”, formed “using a CMOS process” (e.g., “using a SOI... substrate”) (see [1.0]), includes MOSFET T2 (first switch circuit formed on the semiconductor substrate) connected between “common terminal RF_COM” (antenna node) and “high-frequency signal terminal RF_2” (transmit node) as shown in annotated FIG. 3 (“Annotated FIG. 3”):



EX-1007, FIG. 3, [0001], [0003], [0005], [0007], [0029], [0037], [0042], [0054]-[0056], [0065]-[0072], [0084]; EX-1003, ¶142. Seshimo discloses that “MOSFETs T1[, T2, T3 and] T4 can be stacked vertically or a multi-gate structure can be used.” EX-1007, [0071], FIG. 3; *see also* [1.3], [1.6.1].

Given Seshimo’s disclosure that, for example, the SPDT switch (FIG. 3) could achieve the “maximum permissible input power... usable by a PHS (Personal Handyphone System)” where it would be “used as a transmission/reception changeover switch” (EX-1007, [0029], [0070]-[0071], [0005], [0007]), and emphasis on the disclosed “high-frequency semiconductor switching circuit[s]” (e.g., FIG. 3) being “developed... using CMOS processes” so that the “CMOS switch can be integrated into another CMOS RF IC” (EX-1007, [0003], [0084], [0087]-[0088]), POSITAs understood Seshimo discloses “common terminal RF_COM” as an antenna, and “high-frequency signal terminal RF_2” and “high-frequency signal terminal RF_1” as a transmit node and receive node respectively. EX-1003, ¶¶142-143.

iv. [1.3] a second switch circuit formed on the semiconductor substrate and connected between the antenna node and a receive node;

Seshimo discloses SPDT switch (FIG. 3), formed “using a CMOS process” (e.g., “using a SOI... substrate”) (*see* [1.0]), includes MOSFET T1 (*second switch circuit formed on the semiconductor substrate*) connected between common terminal RF_COM (*antenna node*) and “high-frequency signal terminal RF_1” (*receive node*) as illustrated

in Annotated FIG. 3 (*see* [1.2]). EX-1007, FIG. 3, [0001], [0003], EX-1003, ¶144.

- v. ***[1.4] a first capacitor formed on the semiconductor substrate and connected in series with the first switch circuit between the first switch circuit and the antenna node;***

Seshimo discloses **capacitor C3**, that, (i) like the other capacitors (**C2, C5, C7**, etc.), may have a “MIM (metal-insulator-metal) structure” and is “integrated on the same semiconductor substrate” as the other SPDT components (*first capacitor formed on the semiconductor substrate*), and (ii) is connected in series with **MOSFET T2** (*first switch circuit*) and between **MOSFET T2** and **common terminal RF_COM** (*antenna node*) as illustrated in Annotated FIG. 3. EX-1007, [0065]-[0071], FIG. 3; *see* [1.0]; EX-1003, ¶145. POSITAs understood Seshimo discloses resistor Rd2 (and likewise Rd1 and the other resistors in the FIG. 3 circuit) are used for DC biasing only, such that the depicted Rd2 contact to the series path between **MOSFET T2** and **RF_COM** via **capacitor C3** is a “y-junction”, which POSITAs understood does not alter the series connection between **MOSFET T2** and **capacitor C3**. EX-1007, [0055]-[0056], [0059]-[0061]; EX-1003, ¶146.

To the extent PO asserts that Seshimo does not explicitly disclose forming “**capacitor C3**” (and, *e.g.*, “**capacitor C2**”) on the same semiconductor substrate of the same semiconductor die as the other components (*e.g.*, SOI FETs) of FIG. 3 SPDT switch, as discussed in the State of the Art sections, POSITAs would have been motivated to do so as a mere design choice to achieve known and predictable benefits,

including making manufacturing, testing, and production of FIG. 3 SPDT switch (and ICs incorporating the same) easier and less costly, with a reasonable expectation of success, including because low capacitance value (*e.g.*, picofarad) capacitors are small in size and typically used in RF switches since, as was well-known to POSITAs, they would pass (with very low impedance) the high RF frequencies-of-interest (*e.g.*, 1.88-1.93GHz associated with “PHS”) while impeding low, out-of-band blocker frequencies. *Id.*; §V.F.3 (EX-1034, FIG. 2; EX-1035, 2-5; EX-1023, 10:13-17, FIG. 5; EX-1011, 2616-2617, FIG. 4; EX-1029, FIGS. 1-2, pp.35-36, 40; EX-1022, [0028], FIG. 7, [0046]-[0050]; EX-1010, [0009], [0013], FIG. 3A, [0046]); §V.F.1 (EX-1012, 231-234, 175-176; EX-1027, 82-83, 50; EX-1014, 29-32, 36-37, 42; EX-1043, 128-129, 137-139, 236-238; EX-1032, 1-2; EX-1033, 1; EX-1011, 2615-2618; EX-1026, [0049]; EX-1024, 3-4; EX-1031, 8-9; EX-1044, 1-2; EX-1010, [0040]; EX-1009, FIG. 2, [0083]-[0084], EX-1035, 5; EX-1042, 96, 172, 180, 227, 275, 286; EX-1029, 36-39; EX-1017, [0025]); §V.F.2 (EX-1024, 1, 3-4; EX-1039, FIG. 5, 2-6, 9-12 (*citing* EX-1040, 3-6, FIGS. 3-4); EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1045, 1; EX-1049, p.3); EX-1047, 1; EX-1048, 4, 9-11; EX-1003 ¶147.

- vi. [1.5] a second capacitor formed on the semiconductor substrate and connected in series with the second switch circuit between the second switch circuit and the antenna node; and**

Per [1.4], Seshimo discloses a capacitor C2 that, (i) like the other capacitors (C1, C5, C7, etc.), may have a “MIM (metal-insulator-metal) structure” and is “integrated on

the same semiconductor substrate” as the other SPDT components (*second capacitor formed on the semiconductor substrate*), and (ii) is connected in series with MOSFET T1 (*second switch circuit*) and between MOSFET T1 and common terminal RF_COM (*antenna node*) as illustrated in Annotated FIG. 3. EX-1007, [0001], [0003], [0007], [0065]-[0071], [0082], [0084], [0087]-[0088], [0090], FIG. 3; *see* [1.0], [1.4]; EX-1003, ¶148. Per [1.4], POSITAs understood resistor Rd1’s contact to the series path between MOSFET T1 and RF_COM via capacitor C2 is a “y-junction”, does not alter the series connection between MOSFET T1 and capacitor C2. *Id.*; EX-1007, [0055]-[0056], [0059]-[0061]; EX-1003, ¶149.

vii. [1.6.1] a first shunt arm formed on the semiconductor substrate and connected to the first switch circuit and the transmit node,

Seshimo discloses, “in a state in which the inverter circuit IN1 is shared”, one of “four units” of FIG. 3 “shunt SPDT switch” includes “MOSFET T4, capacitors C7 and C8...” and discloses, during operation of this SPDT switch:

A... Vcont of 0 V is input to... inverter circuit IN1, **turning OFF...** MOSFETs T1, T4. A... Vcc of 3 V is output from... inverter circuit IN1, **turning ON...** MOSFETs T2, T3. As a result, a cutoff state is established between... RF_1 and RF_COM, and a conductive state is established between... RF_2 and RF_COM. When... Vcont is 3 V The MOSFETs T1, T4 are in an ON state, and... MOSFETs T2, T3 are in an OFF state. As a result, a conductive state is established between... RF_1 and RF_COM, and a cutoff state is established between... RF_2 and RF_COM.

EX-1007, [0054]-[0056], [0065]-[0066] (*e.g.*, transmission), [0067]-[0068] (*e.g.*, reception); EX-1003, ¶150. Accordingly, and as discussed in [1.0], [1.2] and [1.4] and illustrated in Annotated FIG. 3, POSITAs understood Seshimo discloses a **first shunt arm** that (i) is formed on the semiconductor substrate, (ii) is connected to **MOSFET T2** (*first switch circuit*) and to **high-frequency signal terminal RF_2** (*transmit node*), and (iii) includes (among other components) **MOSFET T4** connected to “high-frequency ground terminal GND” (*third switch circuit connected to ground*). *Id.*; EX-1007, [0001], [0003], [0007], [0065]-[0071], [0082], [0084], [0087]-[0088], [0090]; EX-1003, ¶151.

viii. [1.6.2] the first shunt arm including a third switch circuit connected to ground.

Seshimo discloses this limitation for the reasons discussed regarding [1.6.1].

b. Claim 2

i. *The semiconductor die of claim 1 further comprising an insulator layer disposed between the first and second switch circuits and the semiconductor substrate.*

As explained in [1.0], Seshimo discloses FIG. 3 SPDT switch is “a high-frequency semiconductor switching circuit including... MOSFET[s] formed on a silicon substrate”, and may include “CMOS switch[es] formed using a SOI... substrate” due to, for example, their “excellent high frequency properties” and ease of “integrat[ion] into another CMOS RF IC.” EX-1007, [0001], [0003], [0007], [0054], [0084], [0088]; EX-

1003, ¶153.

Unsurprisingly, Seshimo does not disclose the well-known details of implementing SOI technology to manufacture the “CMOS switch[es] formed using a SOI... substrate” of the FIG. 3 SPDT switch. *Id.* Indeed, as described in the State of the Art section, it was well-known that, in using SOI technology to create ICs, an insulator layer is deposited onto a semiconductor substrate of a semiconductor die, silicon is grown on top of this insulator layer, and then the silicon is patterned and etched to create the various components of the IC (*e.g.*, MOSFETs, capacitors, etc. of SPDT switch (FIG. 3)). §V.F.3 (EX-1020, FIGS. 1, 4, 8:17-25, 7:12, 7:17-18, 10:5-11, 8:28-29, 1:10-14, 12:27-13:8, FIG. 16; EX-1026, [0030]; EX-1018, 4:27-41, 3:50-54, FIGS. 3-4; EX-1039, 9-10, FIG. 10); EX-1003, ¶154. Accordingly, POSITAs understood Seshimo’s disclosed implementation of SOI included an insulator layer disposed between the SOI **first (T2)** and **second (T1)** MOSFETs (*first and second switch circuits*) and the semiconductor substrate. *Id.*; EX-1007, [0001], [0003], [0007], [0054], [0084], [0088]; EX-1003, ¶155.

To the extent PO asserts that Seshimo does not expressly disclose an insulator layer disposed between the **first (T2)** and **second (T1)** MOSFETs (*first and second switch circuits*) and the semiconductor substrate, it would have been obvious to POSITAs to do so because, as described in the State of the Art section, this was the well-known and widely implemented approach to using the disclosed SOI technology to

manufacture “the CMOS switch[es] formed using a SOI... substrate” of the “high-frequency semiconductor switching circuit” (e.g., FIG. 3 SPDT switch), with well-known and predictable benefits including, for example, lower cost, higher “thermal conductivity”, reduced “degradation in bandwidth associated with the stacking of FET devices”, “reduce[d] dielectric losses associated with the silicon substrate”, allowing monolithic (same die/chip) integration of SPnT switch and control components and other FEM components, etc. *Id.*; §V.F.3 (EX-1009, [0005]; EX-1018, 4:37-41; EX-1024, 4; EX-1021, 2; EX-1010, [0013]); EX-1003, ¶156.

c. Claim 3

- i. The semiconductor die of claim 2 wherein the semiconductor die is a silicon-on-insulator (SOI) die.*

Seshimo discloses this limitation for the reasons discussed regarding [1.0], claim 2.

d. Claim 7

- i. [7.0] A method for operating a radio-frequency (RF) device, the method comprising:*

To the extent the preamble is limiting, Seshimo discloses FIG. 3 SPDT switch, including high-frequency signal terminal RF_2, high-frequency signal terminal RF_1, and common terminal RF_COM, could achieve the “maximum permissible input power... usable by a PHS (Personal Handyphone System)” where it would be “used as a transmission/reception changeover switch” (EX-1007, [0029], [0070]-[0071], [0005], [0007]), and emphasizes the disclosed “high-frequency semiconductor switching

circuit” (*e.g.*, FIG. 3) being “developed... using CMOS processes... [to] be integrated into another CMOS RF IC” (EX-1007, [0003], [0084], [0087]-[0088]). Seshimo also discloses methods for operating the FIG. 3 SPDT switch in such RF/wireless devices (PHS). *Id.*; EX-1007, [0065]-[0071], EX-1003, ¶158. Accordingly, Seshimo discloses a method for operating a radio-frequency (RF) device to POSITAs. *Id.*; *see* EX-1047, 1; EX-1048, 4, 9-11; EX-1003, ¶159.

ii. [7.1.1] providing an RF device including

Seshimo discloses this limitation for the reasons discussed regarding [7.0].

iii. [7.1.2] a first switch circuit connected between an antenna node and a transmit node, [7.1.3] a second switch circuit connected between the antenna node and a receiver node, [7.1.4] a first capacitor connected in series with the first switch circuit¹⁰ between the first switch circuit and the antenna node, [7.1.5] a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node, and [7.1.6] a first shunt arm connected to the first switch circuit and the transmit node, [7.1.7] the first shunt arm including a third switch circuit connected to ground;

Seshimo discloses these limitations for the reasons discussed regarding [1.2]-[1.6.2].

iv. [7.2] controlling an RF switch of the RF device by placing the first switch circuit in an ON state and placing the third switch circuit in an OFF state; and

¹⁰ See footnote 9.

Seshimo discloses controlling the FIG. 3 SPDT switch (*controlling an RF switch*) of the RF device (*see* [7.0]) by: “[a] control voltage... is input to... inverter circuit IN1, **turning OFF the MOSFETs T1, T4** [*third switch circuit*]. A power supply voltage... is output from... inverter circuit IN1, **turning ON the MOSFETs T2** [*first switch circuit*], **T3**. As a result, a cutoff state is established between... **RF_1** and **RF_COM**, and a conductive state is established between... **RF_2** and **RF_COM**.” EX-1007, [0065]-[0066] (*e.g.*, transmission), FIG. 3; [0067]-[0068] (*e.g.*, reception); §VII.A.2 [1.2]-[1.6.2]; EX-1003, ¶167.

v. [7.3] inhibiting a low-frequency blocker signal from mixing with a fundamental-frequency signal in the RF switch using the first capacitor.

Seshimo discloses this limitation to POSITAs. EX-1003, ¶169. As discussed in [1.4]-[1.5], Seshimo discloses, in FIG. 3 SPDT switch (*the RF switch*) as shown in Annotated FIG. 3, positioning (i) **capacitor C3** (*first capacitor*) between **common terminal RF_COM** and **Tx series MOSFET T2**, and (ii) **capacitor C2** between **RF_COM** and **Rx series MOSFET T1**. Seshimo’s disclosure is identical to the ’579 Patent’s disclosed positioning in its FIG. 9 SPDT switch 250, (i) **capacitor C1** (*first capacitor*) between **antenna node 252** and **Tx series switch circuit 120/140**, and (ii) **capacitor C2** between **antenna node 252** and **Rx series switch circuit 120/140**. EX-1007, [0055]-[0056], FIG. 3; §V.B (EX-1002, 31-34, 37-39, 47-48, 339-341); §V.A (EX-1001, 9:39-53, FIG. 9); EX-1003, ¶¶169-170.

Seshimo also discloses the importance of selecting (i) substrates (*e.g.*, SOI) and capacitor structures (*e.g.*, MIM) with “excellent high frequency properties”, (ii) biasing voltages of the MOSFETs when in “ON” and “OFF” states, and (iii) the FIG. 3 SPDT switch configuration (with identical C3, C2, C7 and C5 capacitor positioning as the ’579 Patent FIG. 9 C1, C2, C3 and C4 positioning) instead of the FIG. 4 SPDT switch configuration (with shared capacitor C3 between RF_COM and MOSFET T2 and MOSFET T1, and no top capacitor in either the first shunt arm or the second shunt arm), in order to be able to “provide a semiconductor switching circuit capable of improving the maximum permissible input power while suppressing an increase in ON-resistance” (that, without suppression, would “lead to an increase in insertion loss” and a “deterioration in isolation”). EX-1007, FIG. 3 ([0054]-[0056], [0064]-[0071]), FIG. 4 ([0072]-[0073], [0077], [0079]-[0081]), [0082], [0084], [0087]; [0001], [0004]-[0005], [0007]; EX-1003, ¶171.

Unsurprisingly, just like the ’579 Patent, given the fundamental, frequency-dependent impedance characteristic of capacitors—capacitors allow high frequencies to pass through (essentially acting as short circuits) while blocking low frequencies (essentially acting as open circuits)—outside of specifying the identical arrangement of capacitor C3 (*the first capacitor*) in FIG. 3 SPDT switch (*the RF switch*) as the Applicant’s relied-on arrangement, Seshimo leaves the particular capacitor value implementation details to design choices of POSITAs. *Id.*

Moreover, given this fundamental, frequency-dependent impedance characteristic of capacitors, the typical (picofarad) capacitor values selected for RF switches in Seshimo's disclosed use cases, and the known solution—having “the switch see[] an open circuit at the blocker frequencies”—to the well-known low-frequency, “out-of-band blocker” signal problem in non-linear RF switches, POSITAs would understand Seshimo's disclosed implementation of **capacitor C3** as being a high-pass filter that would “inhibit[] a low-frequency blocker signal from mixing with a fundamental frequency signal in the RF switch.” *Id.*, §V.F.1 (EX-1012, 231-234, 175-176; EX-1027, 82-83, 50; EX-1014, 20, 30, 29-32, 36-37, 39-40, 42, FIGS. 1.52-1.55, 1.56(A); EX-1043, 128-129, 137-139, 236-238, FIGS. 5-17(A), 8-17(B), 8-17(D), 8-18(B), 8-18(D); EX-1011, 2615-2618, FIG. 9A; EX-1024, 3-4; EX-1026, [0049]; EX-1031, 8-9, FIG. 13; EX-1010, [0040], EX-1044, 1-2; EX-1029, 36-39; EX-1032, 1-2; EX-1033, 1; EX-1042, 96, 172, 180, 227, 275, 286; EX-1017, [0025]); §V.F.2 (EX-1039, FIG. 5, 2-6, 8-12 (*citing* EX-1040, 3-6, FIGS. 3-4); EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1045, 1; EX-1049, p.3); EX-1003, ¶¶172-173.

Furthermore, to the extent PO asserts that Seshimo does not expressly disclose **capacitor C3** performing this step, with the FIG. 3 SPDT switch components arranged as shown in Annotated FIG. 3, and opposing series and shunt switches placed in ON and OFF states depending on the transmit or receive mode of such switch as disclosed by Seshimo, POSITAs understood **this capacitor's** inhibition of low-frequency blocker

signals from mixing with fundamental frequency signals in FIG. 3 SPDT switch to merely be a matter of design choice. *Id.*; EX-1003, ¶174.

As discussed in the State of the Art section, because capacitor C3 is fundamentally a frequency-dependent circuit element (with decreasing impedance with increasing frequency), POSITAs understood that tuning the resulting high-pass filter, *i.e.*, setting the frequency range above which this capacitor permits frequencies (*e.g.* the desired RF frequency) to pass essentially unimpeded, and below which (*e.g.*, the “- 3dB breakpoint”) it impedes lower frequencies (*e.g.*, low-frequency “out-of-band-blocker” signals), is simply a matter of picking the size capacitor that yields the desired pass/inhibit thresholds within the practical size constraints for the RF device (*e.g.*, “PHS”) with a reasonable expectation of success. *Id.*; *see also* §V.F.1 (EX-1009, FIG. 2, [0083]-[0084]; EX-1035, 5; EX-1032, FIG. 1; EX-1026, FIG. 2, [0002], [0040], [0049], [0051], [0063]; EX-1042, 294, 298, 308, 312); EX-1003, ¶175. Filtering RF_COM-picked-up, low-frequency, out-of-band-blocker signals was a well-known problem in RF radios, with a well-known solution (*i.e.*, a series capacitor sized to yield the desired frequency-dependent response as a high-pass filter within the practical size constraints for the RF device). *Id.*; EX-1003, ¶176.

Accordingly, POSITAs would have been motivated to selecting an appropriately-sized capacitor C3 to pass (with very low impedance) the high frequencies-of-interest (*e.g.*, 1.88-1.93GHz associated with PHS ([1.0])), while impeding low, out-of-band

frequencies, within the practical size constraints of such radios, to achieve the known and predictable benefits of improved switch performance (including improved IMD performance) with a reasonable expectation of success given that this involves nothing more than the conventional and routine use of Seshimo's capacitors. *Id.*; *see also* EX-1047, 1; EX-1048, 4, 9-11; EX-1003, ¶177.

e. Claim 8

- i. The method of claim 7 wherein the first switch circuit is formed on an insulator layer disposed between the first switch circuit and a semiconductor substrate.*

Seshimo discloses this limitation for the reasons discussed regarding claim 2 and [1.0].

f. Claim 9

- i. The method of claim 7 wherein the RF switch is a silicon-on-insulator (SOI) switch.*

Seshimo discloses this limitation for the reasons discussed regarding claim 2.

g. Claim 13

- i. [13.0] A wireless device comprising:*

To the extent the preamble is limiting, Seshimo discloses this limitation for the reasons discussed regarding [7.0], [7.1].

- i. [13.1] a transceiver configured to process RF signals;*

As discussed in [7.0] and [7.1.1], Seshimo discloses to POSITAs incorporation of a “high-frequency semiconductor switching circuit” (*e.g.*, FIG. 3 SPDT switch) into an

RF/wireless device (*e.g.*, PHS), in which such switch module would (i) be “used as a transmission/reception changeover switch”, (ii) include high-frequency signal terminal RF_2 (*transmit node*), high-frequency signal terminal RF_1 (*receive node*), and common terminal RF_COM (*antenna*), (iii) have its SPDT components and control circuits all “configured as CMOS circuits and integrated on the same semiconductor substrate”, and (iv) be “developed... using CMOS processes” so that the “CMOS switch can be integrated into another CMOS RF IC.” EX-1007, [0029], [0070]-[0071], [0003], [0005], [0007], [0084], [0087]-[0088]. Seshimo also discloses methods for operating the FIG. 3 SPDT switch (*switch module*) in such wireless devices, in which the RF signal path is switched between having “a conductive state established between... RF_2 and RF_COM” and, separately, having “a conductive state established between... RF_1 and RF_COM.” EX-1007, [0065]-[0071], FIG. 3.

Accordingly, POSITAs reading Seshimo would understand it discloses a transceiver configured to process RF signals, which is in communication with RF_COM (*antenna*) via, in part, the FIG. 3 SPDT switch, formed for use as a component incorporated into (*e.g.*, in a packaged RF switch module, etc.) (*switch module*) an RF/wireless device (*e.g.*, “PHS”), which is interconnected to RF_COM (*antenna*) and the transceiver and configured to selectively route RF signals to and from RF_COM (*antenna*). *Id.*; see also §V.F.5 (EX-1023, FIG. 3, 1:43-67, 1:7-9, 1:13-24, FIG. 6, 7:50-52; EX-1028, 1, FIG. 1; EX-1008, 3; EX-1041, 1; EX-1039, 1, 3-4, Figures 3-4; EX-

1017, FIG. 5, [0027], [0001], [0016], [0018]; EX-1022, [0004]; EX-1025, FIG. 12, 15:24-33, 16:19-18:7, Abstract); EX-1003, ¶¶181-183.

- ii. [13.2] an antenna in communication with the transceiver; and*

Seshimo discloses this limitation for the reasons discussed regarding [13.1].

- iii. [13.3] a switch module interconnected to the antenna and the transceiver and configured to selectively route RF signals to and from the antenna,*

Seshimo discloses this limitation for the reasons discussed regarding [13.1].

- iv. [13.4.1] the switch module including a first switch connected between the antenna and a transmit node, [13.4.2] a second switch connected between the antenna and a receive node, [13.4.3] a first capacitor connected in series with the first switch between the first switch and the antenna, [13.4.4] a second capacitor connected in series with the second switch between the second switch and the antenna, and [13.4.5] a first shunt arm connected to the first switch and the transmit node, [13.4.6] the first shunt arm including a third switch connected to ground.*

Seshimo discloses these limitations for the reasons discussed regarding [1.2]-[1.6.2].

h. Claim 14

- i. The wireless device of claim 13 wherein the first switch is formed on a silicon-on-insulator (SOI) die of the wireless device.*

Seshimo discloses this limitation for the reasons discussed regarding claims 2, 3, and [1.0].

i. Claim 15

- i. *The wireless device of claim 13 wherein the first capacitor is part of the same semiconductor die as the first switch.***

Seshimo discloses this limitation for the reasons discussed regarding [1.0], [1.2], [1.4].

VIII. DISCRETIONARY DENIAL WOULD BE INAPPROPRIATE

A. Discretionary denial under the *Fintiv* factors is not appropriate.

Under *Fintiv*, the Board takes a holistic view of whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel district court proceeding. *Apple Inc. v. Fintiv, Inc.*, PR2020-00019, Paper 11, at 6. Pursuant to the Director’s June 2022 Guidance Memo:

The plain language of the *Fintiv* factors is directed to district court litigation and does **not** apply to parallel U.S. International Trade Commission (ITC) proceedings, as the ITC lacks authority to invalidate a patent and the ITC's invalidity rulings are not binding on the Office or on district courts ... For the foregoing reasons, the PTAB **no longer** discretionarily denies petitions based on applying *Fintiv* to a parallel ITC proceeding. This memorandum memorializes that practice. The PTAB will **not** discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding.

K. Vidal, *Interim Procedure For Discretionary Denials in AIA Post-Grant Proceedings With Parallel District Court Litigation*, June 21, 2022. Here, the district court case was filed in C.D. California on May 6, 2024, a co-pending ITC proceeding was filed on July

16, 2024 and investigation instituted on August 16, 2024, and, on September 13, 2024, pursuant to 28 U.S.C. §1659, the district court granted Petitioner's motion to stay the district court proceeding until the ITC determination becomes final.

B. Discretionary denial under 35 U.S.C. §325(d) is not appropriate.

Petitioner is unaware of any authority holding *Advanced Bionics* to be satisfied where (like here) the prosecution history lacks discussion of any reference relied upon in this petition. In such situations, the Board routinely does not decline institution on §325(d) grounds. Moreover, the challenges in this petition are non-cumulative because the prior art presented describes the claim limitations that were added to gain allowance (including those acknowledged by the Patent/Applicant to be well-known). See §V.A-§VII.B.2.

IX. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Party-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner certifies that the real party-in-interest in this Petition is Kangxi Communications Technologies (Shanghai) Co., Ltd.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

1. Judicial Matters

As of the filing date of this Petition and to the best knowledge of Petitioner, the '579 Patent is involved in the following litigation:

Case Heading	Number	Court	Date
<i>Skyworks Solutions, Inc. v. Kangxi Communication Technologies Shanghai Co., Ltd et al.</i>	CDCA-8-24-cv-00974	CDCA	May 6, 2024
<i>Wireless Front-End Modules, Devices Containing the Same, and Components Thereof</i>	Inv. No. 337-TA-3762	ITC	July 17, 2024

2. Administrative Matters

As of this Petition's filing date and to the best knowledge of Petitioner, the '579 Patent has not been subject to any *inter partes* reviews, reissues, or reexaminations.

3. Related Patents

To the best knowledge of Petitioner, U.S. patent applications and U.S. patents related to the '579 Patent include U.S. Patent No. 9,148,194.

C. Lead/Back-up Counsel (37 C.F.R. § 42.8(b)(3)):

Petitioner provides the following designation of counsel:

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In a concurrently filed Power of Attorney, Petitioner has granted Power of Attorney to Practitioners at Duane Morris LLP.

D. Notice of Service Information (37 C.F.R. § 42.8(b)(4)):

Please direct all correspondence to lead and back-up counsel at the above addresses. Petitioner consents to electronic service at the email addresses above.

X. CONCLUSION

Petitioner requests the Board institute IPR and cancel the Challenged Claims.

Respectfully submitted,

DUANE MORRIS LLP

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Dated: November 12, 2024

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. §42.24 *et seq.*, the undersigned certifies that this document complies with the type-volume limitations. This document contains 13854 words as calculated by the “Word Count” feature of Microsoft Word 2016, the word processing program used to create it. Pursuant to 37 C.F.R. § 42.24(d), this word count excludes the table of contents, table of authorities, mandatory notices under § 42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing.

Dated: November 12, 2024

/Christopher J. Tyson/

Christopher J. Tyson
Lead Counsel for Petitioner
Registration No. 63,850

CERTIFICATION OF SERVICE ON PATENT OWNER

Pursuant to 37 C.F.R. §§42.6(e), 42.8(b)(4) and 42.105, the undersigned certifies that on the November 12, 2024, a complete and entire copy of this Petition for *Inter Partes* Review of U.S. Patent 9,450,579 and all supporting exhibits were served via Federal Express, postage prepaid, to the correspondence address of record for the '579 Patent:

Date of service November 12, 2024

Manner of service FEDERAL EXPRESS

Documents served Petition for *Inter Partes* Review Under 35 U.S.C. § 312 and 37 C.F.R. § 42.104 of U.S. 8,446,823; Petitioner's Exhibit List; All Exhibits; Petitioner's Power of Attorney.

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