

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KANGXI COMMUNICATION TECHNOLOGIES (SHANGHAI) CO., LTD.
Petitioner,

v.

SKYWORKS SOLUTIONS, INC.,
Patent Owner.

U.S. Patent No. 9,148,194
Issue Date: SEPTEMBER 29, 2015

Title: RADIO FREQUENCY DEVICES HAVING REDUCED
INTERMODULATION DISTORTION

Inter Partes Review No.: IPR2024-01457

DECLARATION OF LAWRENCE E. LARSON, Ph.D,

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I, Lawrence E. Larson, Ph.D., declare as follows:

I. INTRODUCTION

1. I am over the age of eighteen (18) and otherwise competent to make this Declaration.

2. I have been retained by Kangxi Communication Technologies (Shanghai) Co., Ltd. (“Petitioner” or “KCT”) as an independent, technical expert consultant in this proceeding before the United States Patent and Trademark Office (“USPTO”). I am being compensated at my rate of \$600 per hour for my services. No part of my compensation is dependent on my opinions or on the outcome of this proceeding. I have no financial interest in any of the parties to this proceeding.

3. This Declaration is in support of the petition for inter partes review (“IPR”) No. IPR2024-01457 (the “Petition”) involving U.S. Patent No. 9,148,194 (the “’194 Patent” or “the Patent”) (EX-1001), entitled “Radio-Frequency Switch System Having Improved Intermodulation Distortion Performance” and listing Anuj Madan, Fikret Altunkilic, and Guillaume Alexandre Blin as the inventors.

4. For the purposes of this inter partes review as I discuss later (in Section IV.B of my Declaration below), I have been instructed to assume that the effective filing date of the claims of the ’194 Patent challenged by the Petitioner in this *inter partes* review is the earliest identified priority date on the face of the ’194 Patent,

i.e., the July 7, 2012 filing date of U.S. Provisional Patent Application No. 61/669,045.

5. I understand that, according to USPTO records, the '194 Patent is currently assigned to Skyworks Solutions, Inc. ("Skyworks" or "Patent Owner"). I assume for purposes of this proceeding that Skyworks is the patent owner.

6. The '194 Patent is generally directed to a radio-frequency (RF) switch that can be used to "switch" signals between one or more "poles" (*e.g.*, an antenna) and one or more "throws" (*e.g.*, an internal receive (Rx) node and an internal transmit (Tx) node) of a wireless device (*e.g.*, a cellular phone). EX-1001, 1:17-19, 1:31-34, 1:41-45, 2:22-30, 9:8-16, 11:2-10. I am familiar with the technology described in the '194 Patent as of the earliest identified priority date of July 7, 2012.

7. In preparing this Declaration, I have reviewed the '194 Patent (EX-1001) and its prosecution history (EX-1002), as well as the patents and documents cited herein, and I have considered these documents in light of the general knowledge in the art as of July 7, 2012. In formulating my opinions, I have relied upon my experience in the relevant art. I have also considered the viewpoint of a person of ordinary skill in the art ("POSITA") in the relevant field, as of July 7, 2012, who I describe below (*see* Section VI.A of my Declaration). For convenience,

the materials I considered in arriving at my opinions are listed in Appendix A of this Declaration.

8. I have been asked to provide my technical expertise, analysis, insights, and opinions regarding the '194 Patent and relevant references that form the basis of the grounds of rejection set forth in the accompanying Petition for *inter partes* review of the '194 Patent. As described in detail below, I offer the following opinions in this Declaration:

- A POSITA would have found Claims 1-11 of the '194 Patent to be obvious over U.S. Patent Publication No. 2011/0254614 to Chun-Wen Huang, et al. ("*Huang*") in view of the knowledge, skill, and creativity of a POSITA.¹ *Huang*, in view of the knowledge, skill, and creativity of a POSITA, teaches each element of these claims to a POSITA; and
- A POSITA would have found Claims 1-11 of the '194 Patent to be obvious over Japanese Patent Publication No. 2006-121217 to Seshimo, et al. ("*Seshimo*") in view of the knowledge, skill, and creativity of a POSITA.² *Seshimo*, in view of the knowledge, skill, and

¹ A copy of *Huang* can be found in Exhibit 1005.

² A Japanese language copy of *Seshimo* can be found in Exhibit 1006, and a copy

creativity of a POSITA, teaches each element of these claims to a POSITA.

9. Unless otherwise indicated, I have added the emphasis in quotations to which I have cited (and reproduced) in this Declaration.

II. QUALIFICATIONS

10. My qualifications and professional experience are described in my *Curriculum Vitae*, a copy of which can be found in Exhibit 1004. The following is a brief summary of my relevant qualifications and professional experience.

11. I hold the title of Chairman of the Board of Slater Technology Fund, where I specialize in advancing early-stage technology ventures in Rhode Island, with the overall objective of economic growth and workforce development.

12. I received a B.S. (1979) in Electrical Engineering from Cornell University; an M.S. (1980) in Electrical Engineering from Cornell University; a Ph.D. in Electrical Engineering from the University of California of Los Angeles; and an Executive M.B.A. (1996) from the University of California of Los Angeles.

of a certified English translation of EX-1006 can be found in Exhibit 1007.

Generally, in my Declaration, when I am referencing the disclosure of Seshimo, I make a citation to Exhibit 1007.

13. Prior to and during my Ph.D. program, I worked at Hughes Aircraft and their Research Laboratories in Malibu, California, from 1980 to 1996 where I directed the development of high-frequency microelectronics in GaAs, InP, and Si/SiGe and MEMS technologies. I also led the development of analog integrated circuits and new generations of low-noise high-electron mobility transistors (HEMTs). In 1996, I joined the faculty at University of California, San Diego (“UCSD”) and served as the director of the UCSD Center for Wireless Communications from 2001 to 2006. From 2007 to 2011, I chaired the Electrical and Computer Engineering Department at UCSD’s Jacobs School of Engineering and was the first faculty member to hold the Communications Industry Chair. I stayed in my position at UCSD until 2011, when I left to accept the position of Dean at the newly opened Brown University School of Engineering.

14. From 2011 to 2022, I worked as Founding Dean of Engineering at Brown University as well as a Professor of Engineering. During that time, I oversaw the faculty and students within the School of Engineering and taught courses in a range of technology-related subjects. The courses I have taught include Wireless Communication Devices and Circuits, Microwave Circuit Design, Introduction to Digital Circuit Design and Introduction to Active Circuit Design.

15. During the second-half of the 2022-2023 academic year (from January 2023 to July 2023), I held the title of Interim Provost at Brown University, where I was responsible for academic and research excellence; sound budgetary practices; and oversight for all programs in all academic departments, research centers, and interdisciplinary institutes.

16. I am currently a Life Fellow of the IEEE and a member of IEEE Microwave Theory and Techniques Society, and I have held the following professional memberships and affiliations:

- Fellow, IEEE (1999), Life Fellow, IEEE (2022)
- Member, Eta Kappa Nu, Sigma Xi, Tau Beta Pi

17. I have co-authored over four hundred publications and over ten books including:

- W. W. Cheng and L. E. Larson, "A Low-Frequency CMOS Triangle Wave Generator", IEEE J. Solid-State Circuits, SC-20 (2), 649-652 (1985).
- Design of Linear RF Outphasing Power Amplifiers (2003);
- CDMA Mobile Radio Design (2000); and
- RF and Microwave Circuit Design for Wireless Communications (1996)

18. I am a named co-inventor on over 40 U.S. patents including: U.S. Pat. No. 4,682,149; U.S. Pat. No. 4,872,010; and U.S. Pat. No. 4,896,121.

19. My *Curriculum Vitae*, a copy of which can be found in Exhibit 1004, also includes my testimony in prior cases.

III. RELEVANT LEGAL STANDARDS

20. I am not a lawyer. In preparing and expressing my opinions and considering the subject matter of the '194 Patent, I am relying on certain basic legal principles that counsel have explained to me. These principles are discussed below.

21. I have been asked to provide my opinions regarding whether the claims of the '194 Patent would have been obvious to a person of ordinary skill in the art ("POSITA") at the time of the claimed invention, in light of the prior art. I understand that prior art to the '194 Patent includes patents and printed publications in the relevant art that predate the priority date of the claimed invention recited in the '194 Patent. As I identified above (and in Section IV.B of my Declaration below), for purposes of this Declaration, I am applying July 7, 2012 as the earliest identified priority date of the '194 Patent.

22. I have been informed by counsel and understand that a patent claim is not patentable as obvious (a requirement I understand to be governed by a statute, 35 U.S.C. § 103) if the differences between the patent claim and the prior art are such that the claimed subject matter as a whole would have been obvious at the time the claimed invention was made to a person of ordinary skill in the relevant art

(“POSITA”). I have also been informed by counsel and understand that the obviousness analysis takes into account factual inquiries including the level of ordinary skill in the art, the scope and content of the prior art, and the differences between the prior art and the claimed subject matter.

23. I have been informed by counsel and I understand that whether there are any relevant differences between the prior art and the claimed invention is to be analyzed from the view of a person of ordinary skill in the relevant art (“POSITA”) at the time of the invention (here, July 2012). As such, my opinions below as to a person of ordinary skill in the art (“POSITA”) are as of the time of the invention, even if not expressly stated as such; for example, even if stated in the present tense.

24. In analyzing the relevance of the differences between the claimed invention and the prior art, I have been informed by counsel and I understand that I must consider the impact, if any, of such differences on the obviousness or non-obviousness of the invention as a whole, not merely some portion of it. The person of ordinary skill in the art (“POSITA”) faced with a problem is able to apply his or her experience and ability to solve the problem and also look to any available prior art to help solve the problem.

25. I have also been informed by counsel and I understand that a precise teaching in the prior art directed to the subject matter of the claimed invention is not

needed. I have been informed by counsel and I understand that one may take into account the inferences and creative steps that a person of ordinary skill in the art (“POSITA”) would have employed in reviewing the prior art at the time of the invention. For example, if the claimed invention combined elements known in the prior art and the combination yielded results that were predictable to a person of ordinary skill in the art (“POSITA”) at the time of the invention, then this evidence would make it more likely that the claim was obvious. On the other hand, if the combination of known elements yielded unexpected or unpredictable results, or if the prior art teaches away from combining the known elements, then this evidence would make it more likely that the claim that successfully combined those elements was not obvious.

26. I have been informed by counsel and I understand that the U.S. Supreme Court has recognized several rationales for combining the teachings of different references or modifying the teaching of a reference to show obviousness of claimed subject matter. Some of these rationales include the following: (a) combining prior art elements according to known methods to yield predictable results; (b) simple substitution of one known element for another to obtain predictable results; (c) use of a known technique to improve a similar device (method, or product) in the same way; (d) applying a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e)

choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and (f) some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

27. I have been informed by counsel and I understand that objective indicia can be important evidence regarding whether a patent claim is obvious or nonobvious, if it has an appropriate nexus to the claimed invention, *i.e.*, if it is a result of the merits of a claimed invention (rather than the result of design needs or market-pressure advertising or similar activities). Such indicia include: (a) commercial success of products covered by the patent claims; (b) a long-felt need for the invention; (c) failed attempts by others to make the invention; (d) copying of the invention by others in the field; (e) unexpected results achieved by the invention as compared to the closest prior art; (f) praise of the invention by the infringer or others in the field; (g) the taking of licenses under the patent by others; (h) expressions of surprise by experts and those skilled in the art at the making of the invention; (i) the patentee proceeded contrary to the accepted wisdom of the prior art, and, (j) the contemporaneous development of the subject matter claimed by others.

IV. BACKGROUND

A. Overview of the '194 Patent

28. The '194 Patent is directed to a radio-frequency (RF) switch that can be used to “switch” signals between one or more “poles” (*e.g.*, an antenna) and one or more “throws” (*e.g.*, an internal receive (Rx) node and an internal transmit (Tx) node) of a wireless device (*e.g.*, a cellular phone). EX-1001, 1:17-19, 9:8-16.

29. The '194 Patent acknowledges that radio-frequency (RF) switches, including “transistor switches”, were in existence, could “be used to switch signals between one or more poles and one or more throws.” EX-1001, 1:21-23. The '194 Patent also acknowledges that such transistor switches were known to be “controlled through transistor bias and/or coupling” where the “[d]esign and/or use of bias and/or coupling circuits in connection with RF switches can affect switching performance.” EX-1001, 1:23-27.

30. The '194 Patent describes examples of RF transistor switches, which can be “based on one or more field-effect transistors (FETs)” arranged, for example, in a “single-pole-double-throw (SPDT or SP2T) configuration”, such as depicted in FIG. 3 (which I have reproduced and annotated below):

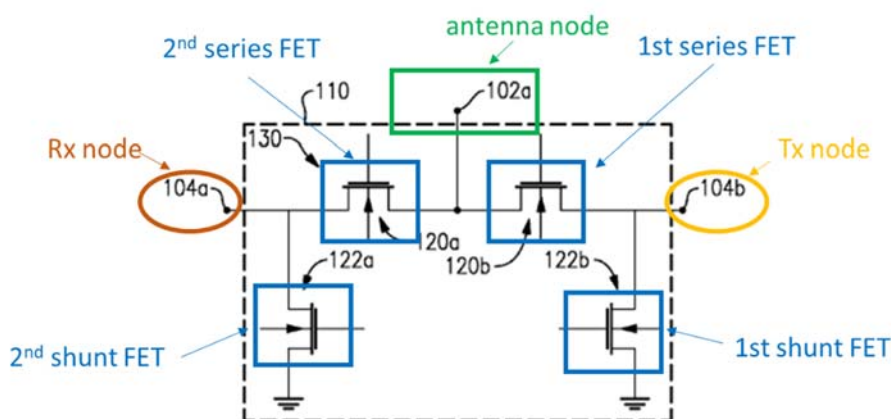


FIG.3

EX-1001, 1:31-34, 3:26-30, 3:49-59, FIG. 3.

31. The '194 Patent states that using multiple FETs per switch arm, *e.g.*, FIG. 4 (which I have reproduced and annotated below), in lieu of single FETs (*e.g.*, FIG. 3 above), “enables improved power-handling capability of the switching device”, but, “in some embodiments,... degrades the switching device insertion loss³ performance”:

³ The '194 Patent describes well-known “switching device insertion loss” as being “measured as a ratio of the power or voltage of an RF signal at an input port to the power or voltage of the RF signal at an output port of the switching device”, with “[d]ecreased switching device insertion loss” being “desirable”. EX-1001, 5:48-63; *see also, e.g.*, EX-1036, 1 (Skyworks’ May 2010 paper describing, in part,

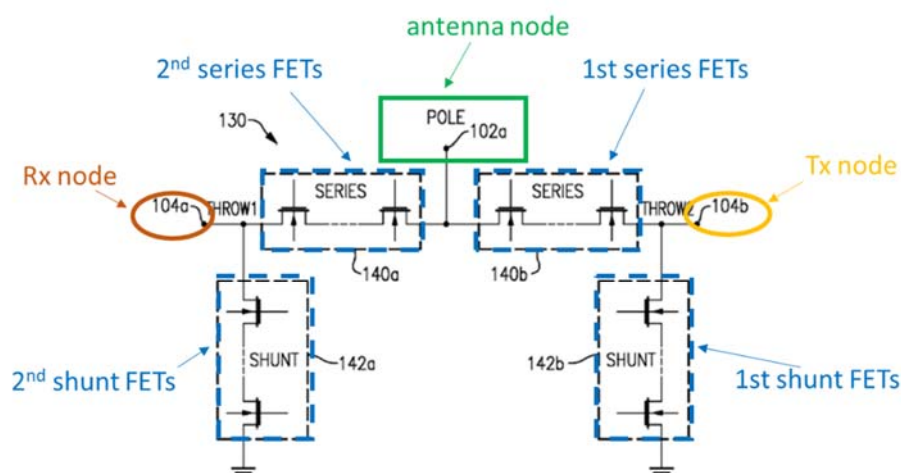


FIG. 4

EX-1001, 4:18-48, 7:5-19, 8:18-39.

32. The '194 Patent states that these RF switches (including FETs) optionally “can be fabricated with silicon or silicon-on-insulator (SOI) technology”, where using SOI technology could “reduce[] power consumption of device circuitry due to decreased parasitic capacitance of transistors and interconnect metallization to a silicon substrate”; “reduce junction capacitance or use of high resistivity substrate, enabling reduced substrate related RF losses” from the “[p]resence of a

“insertion loss” wafer level RF tests); EX-1039, 5, 9-11 (Skyworks’ May 2011 whitepaper describing “important RF switch specification parameters” including “insertion loss”); EX-1008, 2-3 (Skyworks January 2011 brochure describing “insertion loss” measurements); EX-1024, 3 (Skyworks June 2009 article describing “insertion loss” measurements).

buried oxide layer”; and “decrease[] chip size” because “[e]lectrically isolated SOI transistors can facilitate stacking.” EX-1001, 7:23-47, 1:38-39, 1:55-57, 3:28-30.

33. For both the single-, and multi-, transistor-per-switch-arm arrangements, the '194 Patent states that “[o]perations of such FETs can be controlled and/or facilitated by... gate bias/coupling circuit 150a,... body bias/coupling circuit 150c, and/or... source/drain coupling circuit 150b”, and the “design or features” of each such control circuit (150a, 150b, 150c, FIG. 6) “can improve performance of the switch arm... includ[ing]... device insertion loss, isolation performance⁴, power handling capability and/or switching device

⁴ The '194 Patent describes well-known “[s]witching device isolation” as being “measure[d]... while the switching device is in a state where an... input port and... an output port are electrically isolated”, such as “in an OFF state”, and where “[i]ncreased switching device isolation can improve RF signal integrity.” EX-1001, 5:65-6:10; *see also, e.g.*, EX-1036, 1 (Skyworks’ May 2010 paper describing, in part, “isolation” wafer level RF tests); EX-1039, 5-6, 10-11, FIG. 5 (Skyworks’ May 2011 paper describing “important RF switch specification parameters” including “isolation”); EX-1008, 2-3 (Skyworks January 2011 brochure describing “isolation” measurements); EX-1024, 3 (Skyworks June 2009

linearity.” EX-1001, 4:65-5:45, FIGS. 5-6, 9:63-10:11, FIGS. 11A-11D. The ’194 Patent provides **no** other details on **any** of such control circuits, nor explains **how** any of their “design or features” could result in any of the stated switching performance improvements; thus acknowledging that these implementation details were well within the knowledge of POSITAs. *Id.*

34. The ’194 Patent is directed to a well-known problem in designing RF switches in wireless devices, especially wireless devices that operate in a “multi-band and/or multi-mode environment”, namely “the susceptibility of a [RF switch] system to interference” from unwanted signals. EX-1001, 6:33-7:3, 8:61-9:7, 5:66-6:8. For example, as was well-known in the art⁵, when an unwanted signal (*e.g.*, “blocker” signal) mixes with a desired (“fundamental”) RF signal in an RF switch, the desired transmitted/received information may be degraded, and further unwanted signals may be created. *Id.*; EX-1001, 6:9-32, 8:55-60. These created unwanted signals may be at frequencies that are multiples of a desired RF signal frequency (f_1)

article describing “isolation” measurements).

⁵ Patent Owner’s own articles and whitepapers evidence that this same problem was well-known to POSITAs. *See, e.g.*, State of the Art section §VI.B.2 of my Declaration (EX-1039, 2-6, 8-12 (Skyworks’ May 2011 whitepaper) (*citing* EX-1040, 3-6 (Nokia 2005 article)); EX-1036, 1-2 (Skyworks’ May 2010 paper)).

(e.g., $2f_1$, $3f_1$, etc.) called “harmonic frequencies”, or at non-harmonic frequencies (e.g., $f_1 \pm f_{\text{blocker}}$, $2f_1 \pm f_{\text{blocker}}$, etc.) called “intermodulation distortion (IMD)” products. *Id.*

35. The '194 Patent describes a multi-pronged solution to this “interference susceptibility” problem. First, since “[a] given system’s linearity can govern how much IMD will occur within it, which in turn can create interferences”, the Patent states “[s]ystem designers typically strive to reduce interference susceptibility through, for example, improved linearity... of the system building blocks, such as an RF switch.” EX-1001, 8:61-67; *see also* EX-1001 6:38-44, 6:62-65, 5:13-45, FIG. 6.

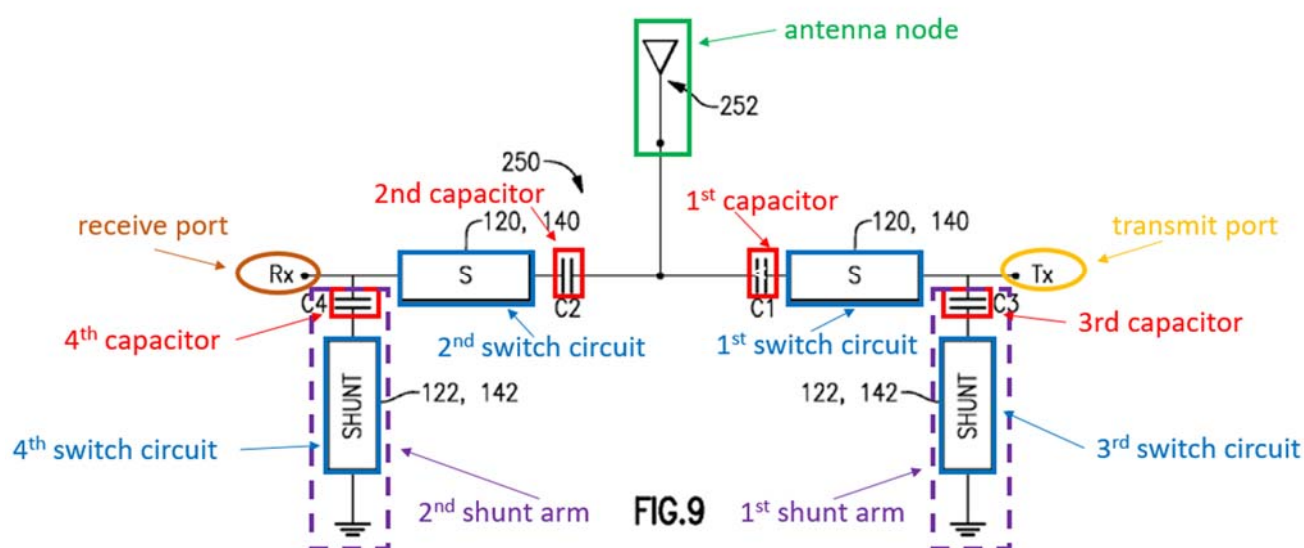
36. Second, the '194 Patent discloses how including a “shunt arm” for each “throw” of the RF switch (e.g., SPDT switch of FIGS. 3-4, 9) is used to address this “interference susceptibility” problem. Referring to FIGS. 3 and 4 (which I reproduced and annotated above), the '194 Patent describes “single pole 102a” is “coupled to first and second ‘throw’ nodes 104a, 104b [e.g., receive and transmit nodes respectively] via first and second... FETs[] 120a, 120b.” EX-1001, 3:38-43, 3:52-59, 4:24-29, 1:38-45, 9:8-16, FIGS. 2-4. Each “throw” node (104a, 104b) is “coupled to an RF ground” via a respective shunt FET (122a, 122b) to “provide shunting capability for the node” (104a, 104b). EX-1001, 3:59-64, 4:30-34, FIGS. 3-4. During operation, “where an RF signal is being passed between... pole 102a

[e.g., antenna] and... first throw 104a [e.g., receive node]”, (i) “FET 120a between... pole 102a and... first throw node 104a can be in an ON state”; (ii) “FET 120b” between... pole 102a and... second throw node 104b [e.g., transmit node] can be in an OFF state”; (iii) Rx “shunt FET 122a can be in an OFF state so that the RF signal is not shunted to ground as it travels from... pole 102a to... first throw node 104a”; and (iv) Tx “shunt FET 122b... can be in an ON state so that any RF signals or noise arriving at the RF core 110 through the second throw node 104b is shunted to the ground so as to reduce undesirable interference effects to the pole-to-first-throw operation.”⁶ EX-1001, 3:28-35, 3:65-4:11, 4:35-48; *see also, e.g.*, EX-1001, 9:8-24, 9:39-44, FIGS. 9-10.

37. Third, the '194 Patent states that the particular arrangement of RF switch components depicted in Figure 9 (which I have reproduced and annotated below) — specifically, the positioning of (i) “capacitor C1... between the antenna

⁶ Patent Owner’s own article and whitepapers evidence that the same FIG. 3 and FIG. 4 configuration and operation of series and shunt FETs in SPDT RF switches, and described benefits and tradeoffs, were well-known to POSITAs. EX-1024, 1, 3-4, FIG. 15 (Skyworks’ June 2009 article); EX-1008, 3, Figure 1 (Skyworks’ January 2011 brochure); EX-1039, 10, Figure 12 (Skyworks’ May 2011 whitepaper); *see also* State of the Art Sections of my Declaration §VI.B.2-§VI.B.4 (in which I identify other examples).

node and the switch arm S of the TX throw”; (ii) “capacitor C2... between the antenna node and the switch arm S of the RX throw”; (iii) “capacitor C3... between the TX node and its shunt switch”; and (iv) “capacitor C4... between the RX node and its shunt switch” — “can lead to improvement in IMD performance, especially for low-frequency blocker signals”:



EX-1001, FIG. 9, 9:8-38, 9:49-54, 4:64-5:45, FIGS. 5-6, 10:11-27, FIGS. 11A-11D.

The '194 Patent explains that, “[w]ith the foregoing capacitors, a low-frequency jammer signal can be blocked or reduced from mixing with any ON or OFF paths”, which “can provide improved IMD performance by preventing a low-frequency blocker signal from mixing with a fundamental frequency signal.” EX-1001, 9:35-38, 9:49-55, 9:25-27.

38. Unsurprisingly, given that a well-known, fundamental characteristic of all capacitors (with a given capacitance value, which a designer can vary as

appropriate) is that they have a **much** higher opposition (X_c : capacitive reactance) to low frequency signals than high frequency signals, outside of the positioning of the capacitors in the FIG. 9 SPDT switch, the '194 Patent leaves the remaining implementation details of this solution to the design choices of POSITAs. *Id.*; see State of the Art Sections of my Declaration §VI.B.1-§VI.B.3.

39. Indeed, the '194 Patent does not provide **any** details as to, for example, (i) **how** the positioning of capacitors in the FIG. 9 SPDT switch “prevent[s] a low-frequency blocker signal from mixing with a fundamental frequency signal”, (ii) **what value** the capacitors must have to perform this function, (iii) **where** the “low-frequency blocker signal” originates from, nor (iv) **what** constitutes a “low” frequency “blocker” signal relative to a “fundamental” frequency. *E.g.*; EX-1001, 6:11-7:3, 8:55-9:55. Accordingly, and unsurprisingly, the '194 Patent recognizes that this low-frequency-blocking-high-frequency-passing characteristic of capacitors was well-within the knowledge of POSITAs, and leaves the other implementation details to design choices of POSITAs. *Id.*

40. The '194 Patent also states (i) “capacitors C1-C4 described in reference to FIGS. 9 and 10 can be implemented on the same die as their respective switch circuits, off of the die, or any combination thereof” (EX-1001, 9:45-49, 2:15-21), and (ii) “bias/coupling circuit 150” (*id.*, 4:64-5:55, FIGS. 5-6) “can be implemented” entirely/partially on the same die, or entirely/partially on a different die, as the die

on which the SPDT switch is implemented (*id.*, 9:62-10:11, FIGS. 11A-11D). However, the '194 Patent does not identify any benefits or tradeoffs associated with such design choices. *Id.* Again, this lack of detail is not surprising as these were well-known design choices, with well-known advantages and tradeoffs, to POSITAs. *See* State of the Art Sections §VI.B.2-§VI.B.4 of my Declaration.

B. Priority Date of the '194 Patent Claims

41. The application that issued as the '194 Patent was filed July 6, 2013, and claims priority to U.S. Provisional Application No. 61/669,045 filed July 7, 2012. EX-1001, 1; EX-1002, 319. I have been instructed to assume, for the purpose of this *inter partes* review proceeding, that the priority date of claims 1-11 of the '194 Patent is the July 7, 2012 filing date of U.S. Provisional Application No. 61/669,045 ("Priority Date").

C. Prosecution History

42. As I discussed in section IV.B of my Declaration (above), the application that eventually led to the '194 Patent was filed July 6, 2013 and claims a Priority Date of July 7, 2012. *See* §IV.B of my Declaration; EX-1001, 1. Original claim 1 of the '194 Patent application recited:

A radio-frequency (RF) switch system comprising:

a switch having a stack of field-effect transistors (FETs)

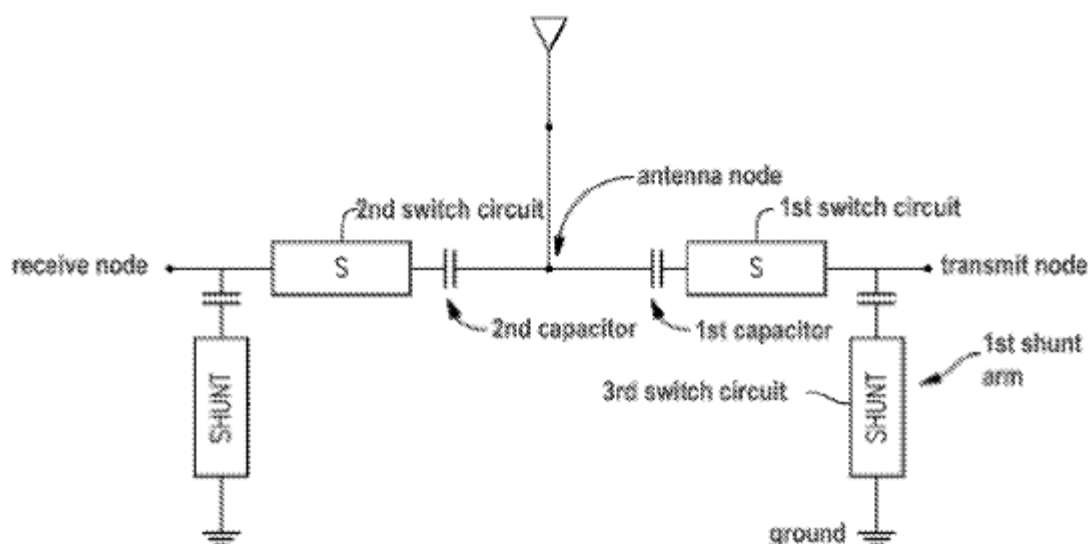
connected in series between first and second nodes; and

a capacitor connected in series with the switch and configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

EX-1002, 345-347, 303-305 (“switch” and “capacitor” limitations are representative of original independent claims 10, 12). The Examiner finally rejected all pending claims, except dependent claims 4-6, as obvious over Patent No. 7,848,712 (“Fu”) and Patent No. 7,885,614 (“Jedeloo”), with claims 4-6 being objected to as each containing allowable subject matter but dependent upon rejected claims. EX-1002, 40-45, 57-60. In response, Applicant “amended independent claims 1, 10 and 12 to include the limitations of dependent claims 3 and 4” (*see* Grounds §VII ([1.5.1]-[1.5.2], [1.6.1]-[1.6.2])) and “rewr[ote] claim 6 [*see* Grounds §VII ([4.5.2])] in independent form including the limitations of” claims 1 and 3. EX-1002, 28-34. The Examiner allowed the claims based on these amendments, and without providing any reasons for allowance, and the Patent issued on September 29, 2015. EX-1002, 1, 7-14.

43. To achieve subsequent allowance of the claims of related U.S. Patent No. 9,450,579, Applicant amended the independent claims and specifically argued:

The features of [the] amended claim[s] can be understood with reference to Figure 9, which is provided in annotated form below:



The Applicant submits that the cited references fail to disclose or render obvious **the particular configuration** claimed in [the] amended claim[s], **particularly with respect to the positioning of the first and second capacitors with respect to the antenna node, and further with respect to the shunt arm.**

EX-1037, 37-39 (emphasis added), 31-34, 15-18.

V. CLAIM CONSTRUCTION

44. I have been advised that, in order to properly evaluate the Challenged Claims of the '194 Patent, the terms of the claims must first be interpreted. I am informed and understand that the terms in the '194 Patent are to be given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art ("POSITA", defined below in Section §VI.A of my Declaration) as of the Priority Date (*see* Section IV.B (above) of my Declaration) in view of the

specification and prosecution history, unless the inventor has set forth a special meaning for a term. That is the meaning I have applied in my analysis.

45. I have been informed by counsel that no court or administrative board has construed any of the claims of the '194 Patent. If a board or court construes any term of the '194 Patent, I reserve the right to supplement my opinions in view of such construction. I have also been informed by counsel that the Board does not construe claim terms unless the terms are in controversy, and then only to the extent necessary to resolve the controversy.

46. I have followed these principles in my analysis throughout this Declaration. It is my opinion that no specific construction of any term is required because the relied-upon prior art meets each of the claimed terms under any proper construction.

VI. STATE OF THE ART

A. Level of Ordinary Skill in the Art

47. I have been informed by counsel and understand that a person of ordinary skill in the relevant art ("POSITA") is a hypothetical person who is presumed to be aware of all pertinent prior art, thinks along conventional wisdom in the art, and is a person of ordinary creativity. I have also been informed by counsel and understand that there are multiple factors relevant to determining the level of

ordinary skill in the pertinent art, including (1) the levels of education and experience of persons working in the field at the time of the invention; (2) the sophistication of the technology; (3) the types of problems encountered in the field; and (4) the prior art solutions to those problems.

48. In my opinion, a person of ordinary skill in the art (“POSITA”) in the field of the ’194 Patent, as of its Priority Date (*see* Section IV.B (above) of my Declaration), would have been someone knowledgeable and familiar with RF electronics, including RF switches and electrical components of such switches, and semiconductor manufacturing processes. A POSITA would have gained knowledge of these concepts through a mixture of training and work experience, such as by having a Bachelor’s degree in electrical engineering, or related field, and approximately two to three years of related experience; or by obtaining a Master’s degree in electrical engineering, or related field, but having only a year of related experience; or by having no formal education but experience in RF electronics and semiconductor packaging of at least six to eight years.

49. A POSITA may work as part of a multi-disciplinary team and draw upon not only his or her own skills, but also take advantage of certain specialized skills of others on the team to solve a given problem.

50. For purposes of this Declaration, in general, and unless otherwise noted, my statements and opinions, such as those regarding my experience and the understanding of a POSITA generally (and specifically related to the references I consulted herein), reflect the knowledge that existed in the field as of the Priority Date of the '194 Patent. Unless otherwise stated, when I provide my understanding and analysis below, it is consistent with the level of a POSITA prior to the Priority Date of the '194 Patent (*see* Section IV.B above – July 7, 2012).

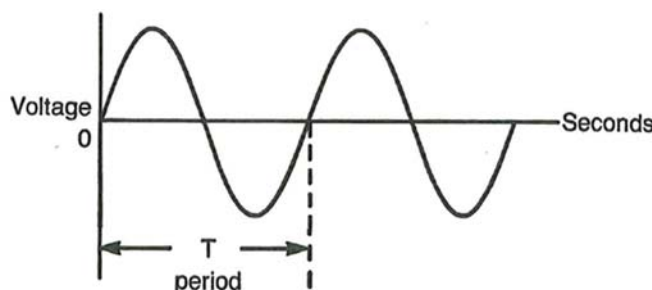
B. State of the Art and the General Knowledge of a POSITA

51. In this section, I describe the state of the art (*see* Section VI.A (above) of my Declaration), including the general knowledge, skill, and creativity possessed by a POSITA as of July 2012. The prior art references that I discuss in this section, and my discussions of what was known to a POSITA during this timeframe, provide the factual support for my general description of the state of the art as of July 2012, and informs the motivations and reasonable expectations of success for the Grounds (that I detail in Section VII of my Declaration below).

1. Textbook EE Concepts Regarding Radio Frequency Electrical Circuits and Capacitors in such Circuits

52. There are several basic, textbook-type electrical engineering (EE) concepts that are relevant to the state of the art of RF switches.

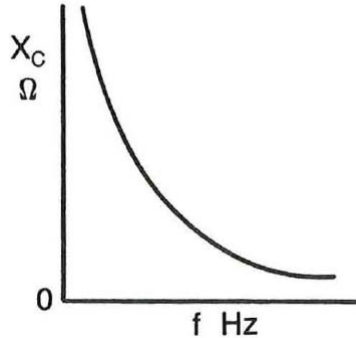
53. First, the RF communications waveform is routinely represented by an alternating current (AC) sinusoidal signal (example depicted below) in which a single complete waveform is known as a “cycle”, and the number of cycles occurring in one second is the “frequency”, *i.e.*, frequency (f) is the rate at which a given waveform repeats, and is measured in hertz (1 Hz = 1 cycle/second):



EX-1012, 200-201 (Veley 1987 Textbook); EX-1027, 83 (Boylestead 1977 Textbook); EX-1014, 30-31 (Horowitz 1989 Textbook). The time interval taken by a complete cycle is the “period” (T), is equal to the reciprocal of the frequency, and is measured in second(s). For example, a waveform with a frequency of 60Hz has a period of $1/60^{\text{th}}$ of a second. *Id.* As frequency (f) increases, the period (T) decreases, and vice versa. *Id.*

54. Second, capacitors “[t]o a first approximation... are devices that might be considered simply frequency-dependent resistors.” EX-1014, 20, 30; EX-1027, 82-83; EX-1012, 231-234.⁷

55. A fundamental characteristic of all capacitors is that their opposition to the flow of an AC waveform (*e.g.*, RF), called “capacitive reactance” (X_c) or, more generally, impedance and measured in ohms (Ω), is “*inversely* determined by the product of the frequency and the capacitance”, with this fundamental characteristic expressed in the equation $X_c = \frac{1}{2\pi fC}$ and shown in the below graph of X_c versus AC signal frequency (f) (which I reproduced below for purposes of my Declaration):



EX-1012, 231-234 (original emphasis); EX-1027, 83; EX-1014, 29-32, 37 (Figure

⁷ The classical construction of a capacitor is two conductors near each other (but not touching), often with a thin insulating material (“dielectric”) therebetween; for greater capacitance, larger sized conductors (more area) and closer spacing between conductors is needed. EX-1014, 21, EX-1012, 158; EX-1027, 48-51.

1.56(A)); EX-1043, 128-129 (Horowitz 1986 Textbook); EX-1024, 3-4 (Skyworks' June 2009 article).

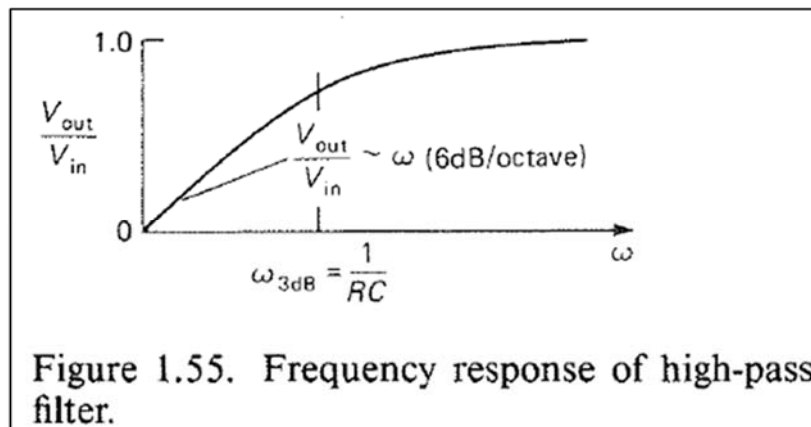
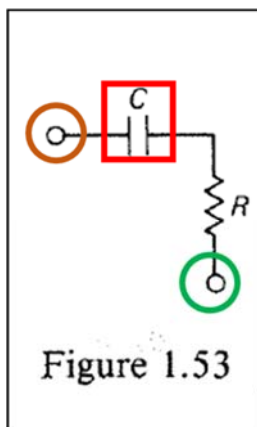
56. Accordingly, all capacitors, regardless of capacitance value, have an essentially infinite opposition to DC current ($f=0\text{Hz}$); in other words, all capacitors block (*i.e.*, are essentially an open circuit to) the very low frequency that is DC current. EX-1012, 231-232, 175-176 (Veley 1987 Textbook); EX-1027, 83, 50 (Boylestead 1977 Textbook); EX-1014, 32, 36-37, 42 (Horowitz 1989 Textbook); EX-1043, 128-129, 137-139 (Horowitz 1986 Textbook); EX-1032, 1-2 (Skyworks' 2005 "MIS Chip Capacitors" data sheet); EX-1033, 1 (Skyworks' 2006 "GaAs... SPDT Switch 0.1-4 GHz data sheet); EX-1011, 2616-2617 (Skyworks' November 2011 article); EX-1026, [0049] (Granger-Jones patent publication); EX-1024, 3-4 (Skyworks' June 2009 article); EX-1031, 8-9, FIG. 13 (Skyworks' 2010 "SP4T... Switch with Decoder" data sheet). As the frequency of the in-series current increases, the impedance X_c drops; at a sufficiently high frequency signal (for a given size capacitor) the impedance drops to the point where the capacitor approximates a conductor. *Id.*

57. As a simple example of the fundamental low-frequency-blocking, and high-frequency-passing, characteristic of typical capacitors used in typical RF switches, a 10pF capacitor would have an impedance X_c of $\sim 16,000\Omega$ to a 1MHz signal, an impedance X_c of $\sim 84\Omega$ to a 190MHz signal, and an impedance X_c of $\sim 7\Omega$

to a 2.4GHz signal. *Id.*; EX-1011, 2616-2617 (10pf); EX-1024, 3 (5-15pf); EX-1010, [0040] (8.4pF) (Nisbet patent publication); EX-1029, 36-39 (20pF, 2.7pF) (FJHuang January 2004 article); EX-1017, [0025] (Ilkov patent publication); *see also* EX-1014, 32; EX-1027, 83; EX-1012, 232-234.

58. Third, due to this fundamental characteristic of capacitors, a basic high-pass filter (having the “desirable property of passing [high] signal frequencies of interest while rejecting undesired [low] signal frequencies”) was, as shown in the EE textbook figure that I reproduced below left (and annotated), simply a capacitor connected in series between the RF waveform source node (which I annotated brown) and output node (which I annotated green), and in series with a resistor (where the “50-ohm standard impedance for RF circuits” is commonly used as this resistor value), and with the fundamental “-3dB ‘breakpoint’” of this filter expressed in the equation $f_{3dB} = \frac{1}{2\pi RC}$ and shown in the graph (which I reproduced below right) of signal amplitude reduction (as a fractional ratio) versus AC signal frequency (in radians (ω^8)):

⁸ POSITAs understood radians (ω) were a shorthand expression of $2\pi f$ (with f being frequency expressed in Hz). EX-1014, 30, 36-37.



EX-1014, 36-37 (Figures 1.52-1.55), 39-40; EX-1043, 137-139, 236-238, FIGS. 5-17(A), 8-17(B), 8-17(D), 8-18(B), 8-18(D); EX-1044, 1-2 (High Frequency Electronics June 2007 article describing “[t]he deeply entrenched 50-ohm standard impedance for RF circuits”); EX-1011, 2617-2618 (Skyworks November 2011 article, FIG. 9(a), “the S-measurements are measured after terminating the remaining ports with 50Ω load.”), 2x10pF capacitors/throw (FIG. 4), $f_{3dB}=636.9\text{MHz}$); EX-1024, 3 (Skyworks June 2009 article, “system characteristic impedance (normally 50Ω)”, Figure 15 (2x “5 to 15pF” capacitors/throw, $f_{3dB}=1.27\text{GHz}$ to 424.MHz)); EX-1036, 2 (Skyworks May 2010 article); EX-1040, 4-5 (Nokia 2005 article); EX-1019, [0179] (Brindle EP patent publication); EX-1017, 2:55-58 (Ilkov patent publication); EX-1007, [0029] (Seshimo patent publication); EX-1010, [0040] (Nisbet patent publication, 2x8.4pF capacitors/throw, FIG. 3A, $f_{3dB}=757.9\text{MHz}$).

59. The EE-textbook-type “- 3dB ‘breakpoint’” (f_{3dB}) of this fundamental high-pass filter is the low frequency value at which the input AC signal amplitude

“is reduced to 0.707 of its maximum” and where, if an even more-attenuated filter fall-off point was desired for the particular application, POSITAs understood such amplitude “is reduced to 0.45 of its maximum at $f_{[3\text{dB}]}/2\dots$, to 0.25 of its maximum at $f_{[3\text{dB}]}/4\dots$, to 0.125 of its maximum at $f_{[3\text{dB}]}/8\dots$ ” and so on. *Id.*

60. Selecting a capacitance value of capacitors in RF switches based on, for example, desired (fundamental) frequency values (for which designers want capacitors to essentially act as a short circuit, *i.e.*, pass through as a very low impedance resistor), practical size constraints, and low frequencies of undesired, potentially interfering signals (for which designers wanted capacitors to essentially act as an open circuit, *i.e.*, block as a very high impedance resistor), was widely known to, and well-within the skill and creativity of, POSITAs. EX-1014, 36-37; EX-1043, 137-139; EX-1026, FIG. 2, [0002], [0040], [0049], [0051], (in “shunt and series coupled RF switches where the input terminal... is connected to an RF line” and “the output terminal... is an RF port” [0063], and using “stacked FET switches” [0002], [0063], “capacitor[s]... behave as high-pass filters” including “presenting a low impedance to the time-variant input signal” [0049]); EX-1011, 2615 (“The sizes of series dc blocking MIM caps are chosen to provide optimum match at the frequency of interest.”), 2617 (“The 10 pf on-chip series MIM capacitor not only serves as a dc blocking capacitor, but it also helps improve return loss (and, in turn, insertion loss) of the switch.”); EX-1009, FIG. 2 (which I reproduce and annotate in

Section VI.B.4 of my Declaration below), [0083]-[0084] (“[The capacitance value of the incremental capacitor C1 [positioned between ANT and Tx series switch M1] is determined according to the frequency and transmission/reception method to be used.”); EX-1024, 3 (“FET Switch Configurations... us[e] a capacitor with adequately low capacitive reactance at the desired frequency of operation” to “DC block the RF source and drain ports.”), 3 (“The selection of the capacitor value is critical to insure proper frequency operation and bandwidth. The values can be quite small (5 to 15 pF), since the series FET can provide most of the isolation at the lower frequencies.”); EX-1032, 1-2 (Skyworks 2005 data sheet for “MIS Chip Capacitors”: “A typical insertion loss versus frequency graph is shown in Figure 1... The apparent higher loss at lower frequencies on the lower capacitance units is strictly due to the capacitive reactance of the capacitor.”), FIG. 1; EX-1031, 8-9, FIG. 13 (Skyworks October 2010 data sheet for “20MHZ-2.5GHz High Power SP4T Switch”: “DC blocking capacitors C1, C2, C7, C8, and C9 determine the low frequency operation of the switch. Increase the capacitor values to lower operation frequency.”); EX-1035, 5 (“The size of the capacitance varies depending on the specifications such as the frequency of use...”); EX-1042, 294, 298 (Skyworks 2007 data sheet for “20MHz-2.5GHz” SP4T switch: “1000pF for operating frequency > 20 MHz” but “use cap appropriate for minimum freq. of operation”), 308, 312 (Skyworks 2008

data sheet for for “0.1-3GHz” SP3T switch: “ $C_{BL}=47$ pF for operation > 500 MHz”, “ $C_{BL}=220$ pF for operation down to 50 MHz”).

61. Accordingly, given these well-known factors, typical capacitance values were well-known to be in picofarads (pF) or nanofarads (nF) for use in semiconductor-based RF switches. *Id.*; EX-1024, 3 (5-15pF); EX-1011, 2616-2617 (10pF, $f_{3dB}=636.9$ MHz (2x10pF capacitors/throw, FIG. 4); EX-1010, [0040] (8.4pF, $f_{3dB}=757.9$ MHz (2x8.4pF capacitors/throw, FIG. 3A); EX-1033, 1 (47pF); EX-1029, 36-39 (20pF, 2.7pF); EX-1042, 96 (22pF for C9, C10), 172 (47pF), 180 (47pF), 227 (47pF), 275 (4.7pF), 286 (47pF); EX-1031, 8-9 (100pF); EX-1017, [0025]; *see also* EX-1014, 21; EX-1012, 158-159.

2. Well-Known Operation and Performance Evaluation of Single-Pole-Multi-Throw (SPnT) Transistor Switches

62. Single-Pole-Multi-Throw (“SPnT”), including Single-Pole-Double-Throw (“SPDT” or “SP2T”), switches, including those using semiconductor-based field-effect transistors (FETs), were well-known and widely used in RF applications and on wireless devices (*e.g.*, mobile phones, WLAN radios, smart phones, etc.). EX-1024, 1, 4; EX-1021, 1; EX-1010, [0002]-[0009]; EX-1023, 1:13-24, 3:43-47; EX-1039, 1, 9-10; EX-1041, 1.

63. For example, Patent Owner’s June 2009 article (EX-1024, “Cory”) states “[t]here is a class of switches, commonly known as transmit-receive (T-R)

switches, used in transceiver applications whose function is to connect the antenna to the transmitter (exciter) in the transmit state and to the receiver during the receiver state”, and describes the operation of SPnT switches that were widely used in such transceiver applications and on wireless devices. EX-1024, 1, 3-4.

64. Cory (EX-1024), and other prior art Patent Owner publications, explain that “typical” SPnT switches, used in high power, multi-mode, high fundamental RF frequency applications, included (i) series and shunt FET switch circuits in order to shunt “OFF” path high power, high frequency signals to ground to prevent them from “leaking into” the “ON” path, (ii) FET control circuitry whose design impacted “isolation”, “insertion loss”, and “linearity” performance parameters, (iii) “stack[ed]... FETs” for increased power handling, and (iv) capacitors with “quite small (5 to 15pf)” “capacitor values” where “[t]he selection of the capacitor values is critical to insure proper frequency operation and bandwidth”:

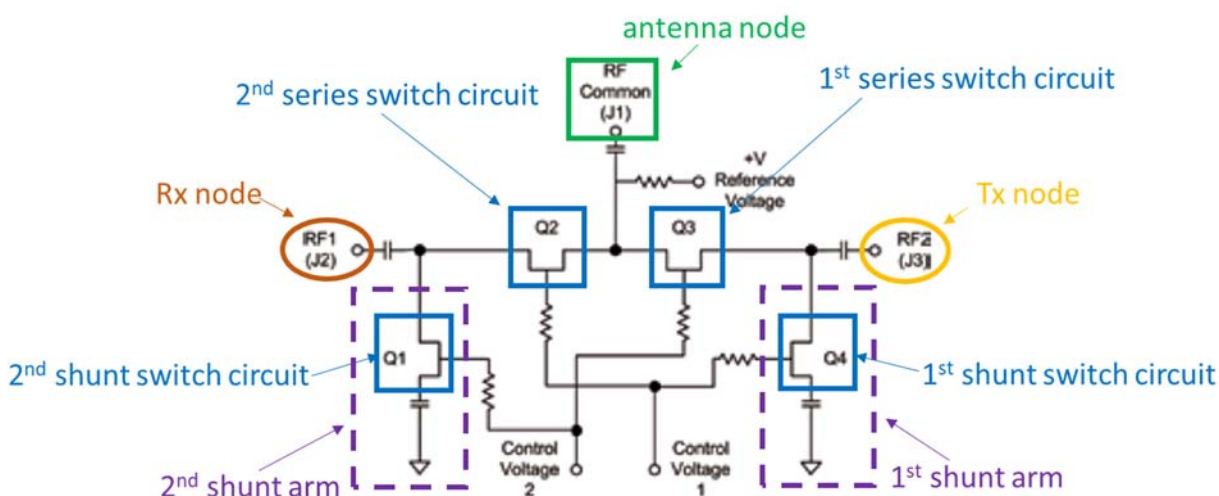


Figure 15: Single Pole Two Throw Switch

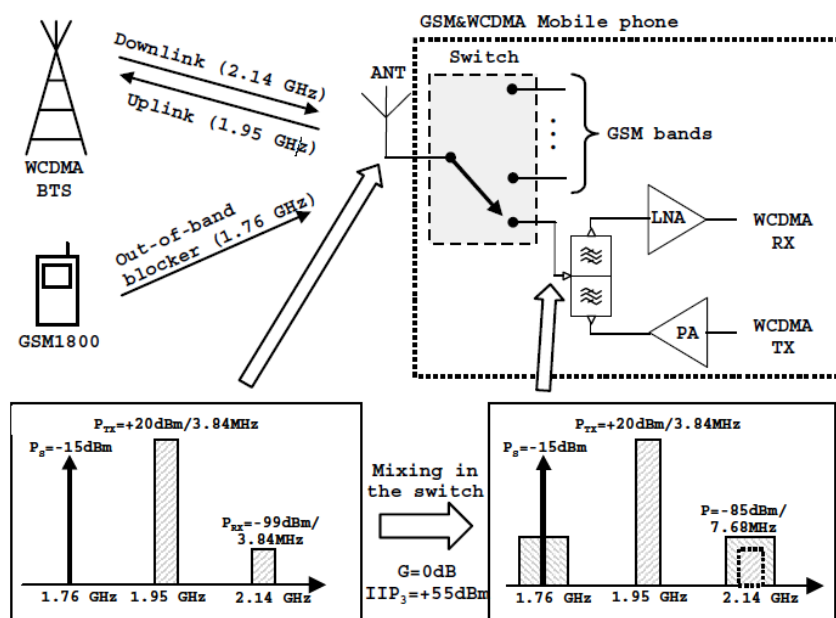
EX-1024, 1, 3-5 (Skyworks’ June 2009 article); EX-1039, 4-6, 9-11 (Skyworks’ May 2011 whitepaper); EX-1041, 1-2 (Skyworks’ July/August 2009 article); EX-1008, 3 (Skyworks’ January 2011 “General Purpose RF Switches” brochure); EX-1023, 5:44-53 (CW-Huang (SiGe Semiconductor) June 2005-filed patent); *see also* State of the Art Sections §VI.B.1 and §VI.B.4 of my Declaration (other examples included).

65. Patent Owner’s May 2011 whitepaper (and the relied-on Nokia 2005 paper therein) explain that another well-known consideration in designing RF switches in wireless devices, especially wireless devices that operate in “multi-mode and multiband” environments, was that if an “unwanted” signal (*e.g.*, “out-of-band blocking” signal at $f_{blocker}$) is allowed to mix with a “wanted” (or “fundamental”) RF signal (*e.g.*, f_{TX} , f_{RX}) in an RF switch, the desired transmitted/received information may be degraded, further “unwanted” signals (*e.g.*, IMD products (*e.g.*, $f_{TX} - f_{blocker}$

(IMD_2), $2f_{TX} - f_{blocker}$ (IMD_3)), “harmonics” (*e.g.*, $2f_{TX}$, $3f_{RX}$), etc.) may be created, and calls may even be dropped. EX-1039, 2-6, 8-12 *citing* EX-1040, 3-6; *see also, e.g.*, EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24 (“[T]he radio system never operates in isolation... In any system, a band is defined in which the receiver may receive signals. The receiver must be able to reject signals outside the band without loss of performance. These signals may be very large (*e.g.* TV transmissions) and quite capable of overloading a sensitive receiver... [T]he non-linearities in the receiver that are excited by the overload will allow unwanted signals to intermodulate. This may result in a distortion product falling onto the wanted signal and effectively masking it.”); EX-1049, p.3 (disclosing examples of low, “out-of-band” blocking frequencies of (i) $f_{\text{blocking}}=45.1718\text{MHz}$ for fundamental frequencies of $f_{TX}=836.5\text{MHz}$ and $f_{RX}=881.5\text{MHz}$, (ii) $f_{\text{blocking}}=45\text{MHz}$ for fundamental frequencies of $f_{TX}=897.5\text{MHz}$ and $f_{RX}=942.5\text{MHz}$, (iii) $f_{\text{blocking}}=30\text{MHz}$ for fundamental frequencies of $f_{TX}=710\text{MHz}$ and $f_{RX}=740\text{MHz}$).

66. In the below-illustrated example, a phone’s antenna (“ANT”) may pick-up “out-of-band blocker” signals transmitted in the area of the phone (*e.g.*, $f_{blocker}=1760\text{MHz}$) and, if the phone’s RF switch’s “linearity is poor”, those antenna-picked-up-signals would “mix” with “fundamental” frequency signals (*e.g.*, $f_{TX} = 1950\text{MHz}$) inside the switch, and produce IMD_2 (*e.g.*, $f_{TX} - f_{blocker}=190\text{MHz}$) and IMD_3 (*e.g.*, $2f_{TX} - f_{blocker}=2140\text{MHz}$) products, where the IMD_2 product mixing with

the same “fundamental” frequency signal (e.g., 1950MHz+190MHz=2140MHz), or the IMD₃ product (e.g., 2140MHz), could be “right at the” phone’s desired Rx/downlink fundamental frequency causing interference (and possibly dropped calls):



Band	TX f_{TX}	RX f_{RX}	IMD2 low	IMD3	IMD2 high
			Blocker 1 $f_{TX} + f_{S1} = f_{RX}$	Blocker 2 $2f_{TX} - f_{S2} = f_{RX}$	Blocker 3 $f_{S3} - f_{TX} = f_{RX}$
850	836.5	881.5	45	791.5	1718
1900	1880	1960	80	1800	3840
2100	1950	2140	190	1760	4090

Fig. 4. Dominating out-of-band blocking mechanisms and center frequencies for the 850, 1900 and 2100 WCDMA bands.

Id.

67. As explained therein and illustrated in the figures that I reproduced above, the same result could occur in the same example for antenna-picked-up-

blocker signals at 190MHz, *e.g.*, a “very large... TV transmission” signal. EX-1039, 2-6, 9-12 *citing* EX-1040, 3-6; EX-1045, 1 (“174.0-216.0MHz” is “Broadcasting (TV Channels 7-13)” spectrum); EX-1046, 23-24 (“[T]he radio system never operates in isolation... In any system, a band is defined in which the receiver may receive signals. The receiver must be able to reject signals outside the band without loss of performance. These signals may be very large (*e.g.* TV transmissions) and quite capable of overloading a sensitive receiver... [T]he non-linearities in the receiver that are excited by the overload will allow unwanted signals to intermodulate. This may result in a distortion product falling onto the wanted signal and effectively masking it.”); *see also, e.g.*, EX-1019, FIG. 19, [0191], [0199].

68. As further explained therein, typical solutions to “minimize[]” the “distortion products for current dependent nonlinearity” in RF switches, *e.g.*, nonlinear series resistance[]... of the OFF paths”, involved “adjusting the phase so that the switch sees an open circuit at the blocker frequency.” *Id.*; EX-1040, 5; EX-1046, 23-24 (“In any system, a band is defined in which the receiver may receive signals. The receiver must be able to reject signals outside the band without loss of performance. These signals may be very large (*e.g.* TV transmissions)... It is therefore imperative that these signals [outside the band] are heavily filtered before the input to the receiver.”).

3. Well-Known Manufacturing Processes to Form SPnT Components on Semiconductor Substrates/Wafers of Semiconductor Dies and Well-Known Monolithic Integrated Circuits and Packages Incorporating the Same

69. Regarding well-known manufacturing processes and packaging of RF Transmit-Receive switches (including SPDT switches), Patent Owner's Cory article (EX-1024) discloses examples of "pseudomorphic high electron mobility transistor (pHEMT)" FETs, which are "typically fabricated from III-V [semiconductor] materials, such as GaAs", which is grown on a "semi-insulating substrate" that "inherently isolates one FET structure from another," and whereby all the switch components (pHEMT "FET structures", "passive component structures – such as metal-insulator-metal (MIM) capacitors", etc.) are formed "on or near the top-most layer" of **the same** wafer EX-1024, 1, 3-4, Figure 8; *see also* EX-1039, 9-10.

70. A well-known design choice to POSITAs (especially with HEMT FETs) involved a selection as to whether to form capacitors of the SPnT switch on the same semiconductor substrate of the same die/chip as the FETs or to incorporate (*e.g.*, in a packaged RF switch module, FEM, etc.) "external" capacitors formed in the packaging design, where such capacitors would be off of the die/chip on which the FETs were formed (*e.g.*, formed on a separate substrate of a separate die, surface mounted to a packaging substrate, etc.). EX-1032, 1-2 (external MIS Chip Capacitors usable in SPDT switches); EX-1033 (pHEMT-GaAs-FET-SPDT switch

datasheet stating “DC blocking capacitors (C_{BL}) must be supplied externally.”); EX-1034, FIG. 2; EX-1035, 2-5 (for HEMT-FET-SPDT switch: “It is desirable to use an On-chip MIM (metal insulator metal) capacitor instead of bonding an external capacitor for the DC blocking capacitor [BC1, BC2, BC3, BC4, BC5, BC6]. It is **possible to use an external capacitor**, but **since multiple capacitors are required**, **the cost of the external capacitor itself and the cost of connecting it to the switch increase significantly**, and **the pad area for capacitor bonding in the switch IC becomes very large**, which can be a problem. **An On-chip MIM capacitor can be easily manufactured** through a semiconductor process **and does not require additional work** such as capacitor bonding from an external user.”); EX-1023, 10:13-17 (“blocking capacitors... are also integrated into the [semiconductor-based DPDT] switch... this simplifies construction and/or assembly of the switch-filter.”), 8:29-37, 5:59-6:21, FIG. 5; EX-1011, 2616-2617, FIG. 4 (CMOS-integrated-SP3T-PA-LNA-die: “[s]ince cross-biasing is used to bias the series-arm and shunt-leg, **on-chip** dc blocking MIM capacitors are required”) ”); EX-1029, FIGS. 1-2 (which I reproduce below), pp. 35-36, 40; EX-1032, 1-2 (Skyworks datasheet describing external MIS Chip Capacitors usable in SPDT switches); EX-1033 (Skyworks pHEMT-GaAs-FET-SPDT switch datasheet stating “DC blocking capacitors (C_{BL}) must be supplied externally”).

71. Regardless of this design choice selection, the well-known, and widely implemented approach, for packaging a die (or a plurality of dies) for commercial sale, testing, shipment, etc. of the SPnT switch (and any other components that are incorporated into the packaged module (*e.g.*, external capacitors, control circuitry, LNA, etc.)), was to mount each separate die (and/or surface mountable component) on, and electrically connect (*e.g.*, wire-bond) each separate die (and/or surface mountable component) to, a packaging substrate (*e.g.*, printed circuit board (PCB)) to electrically interconnect the components of the packaged module. EX-1008, 1-3 (“All switches are packaged in industry-standard, plastic surface-mount packages...”, *citing* EX-1041, 2 (“The Package”)); EX-1029, 36-39 (“SPDT switch... was packaged in an SOIC-like test package...shown in Fig. 4 with “off-chip inductor” (Ls) and “off-chip capacitor” (Cp)), Figures 4, 8; EX-1031, 1 (“SP4T switch... in a compact Quad Flat No-Lead (QFN)... package”); EX-1028, 1, 4, Fig. 2 (annotated below) (depicting PA die and SPDT-LNA die mounted on packaging substrate of “QFN package”); EX-1038, [0010], [0027], [0029], [0030]-[0032] (separate “capacitor die” and “integrated circuit die” mounted on “packaging substrate”), [0036]-[0037], [0045], FIGS. 2-3; EX-1042, 80-82 (WLAN 802.11b, g, n InterTM Front-End Module Single Antenna), 95-97 (WLAN 802.11b, g, n InterTM Front-End Module), 105-106 (WLAN 802.11a, b, g, n Dual-Band, Front-End Module Single Antenna), 171-172 (GaAs SPDT Switch 100 MHz–2.5 GHz),

180-181 (GaAs IC High-Isolation Positive Control SPDT Switch 300 kHz–3 GHz), 192-193 (GaAs SPDT Switch 300 kHz–3 GHz Medium Power), 210 (PHEMT GaAs IC SPDT Switch LF–4 GHz), 221-222 (GaAs SPDT 7 W Switch 100 MHz–4 GHz), 226-227 (GaAs IC High-Isolation SPDT Nonreflective Switch with Driver LF–6 GHz), 237-238 (PHEMT SP2T Switch 0.5–6.0 GHz), 242 (PHEMT GaAs IC 1 W Low Loss 0.1–6 GHz SPDT Switch), 274-275 (GaAs T/R Diversity Switch LF–6 GHz), 285-286 (GaAs SP3T Absorptive Switch 500 MHz–2.5 GHz), 298-299 (PHEMT GaAs IC High-Power SP4T Switch 0.1–2.5 GHz), 312-313 (PHEMT GaAs IC SP3T Switch 0.1–3.0 GHz); EX-1021, 1-3; EX-1033, 1 (“SPDT switch in a SOT-6 plastic package”), 3, 9-11; EX-1032, 1-2; EX-1022, [0028].

72. A well-known alternative to using pHEMT FETs in SPnT switches, with well-understood benefits (*e.g.*, lower cost, higher “thermal conductivity”, reduced “degradation in bandwidth associated with the stacking of FET devices”, “reduce[d] dielectric losses associated with the silicon substrate”, allowing monolithic (same die/chip) integration of SPnT switch and control components and other front-end module (FEM) components, etc.), and trade-offs requiring additional design considerations (*e.g.*, silicon substrates are conductive, accumulated charge in off-state MOSFETs, etc.), was fabricating the SPnT switch components, including the series and shunt FETs, in silicon, including silicon-on-insulator (SOI), grown over a substrate, as shown in the examples below:

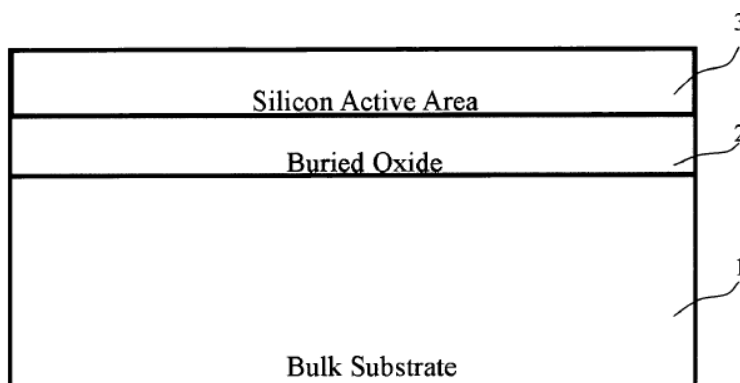
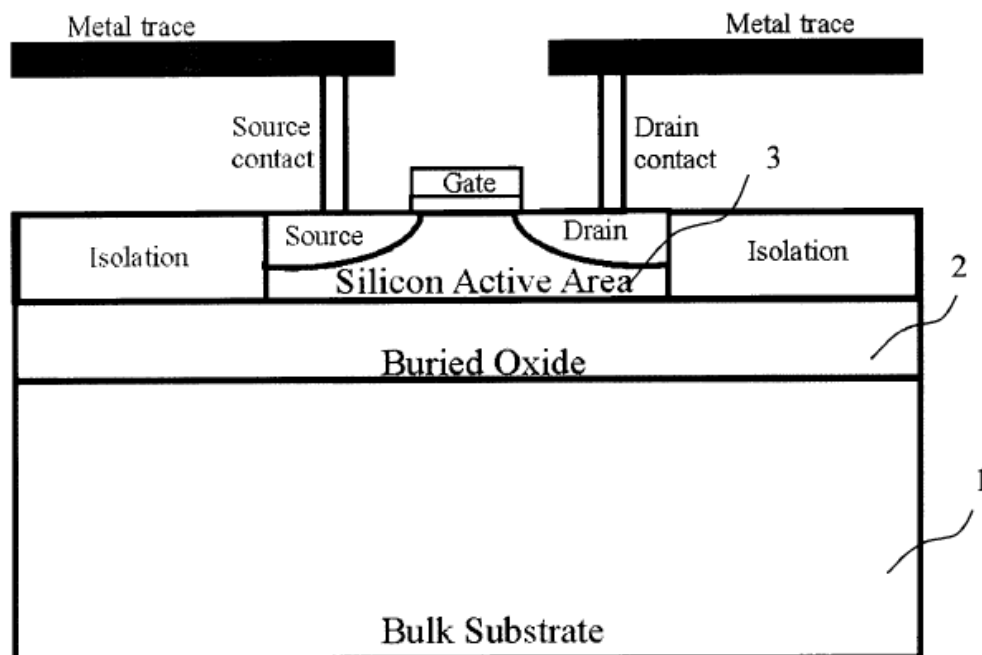


Figure 1

Figure 1 illustrates a cross section of the principle elements of a typical SOI process. The SOI process consists of a thin silicon active area above an insulating layer. This insulating layer sits on top of a silicon substrate. A typical material for the insulating layer is silicon dioxide. In general SOI technologies consist of a bulk substrate 1, a buried oxide layer 2 and another thin active silicon layer 3. The bulk substrate 1 is generally a high resistivity substrate.

EX-1020, FIG. 1, 8:17-25;

As shown in Figure 4 transistors are made in the thin active layer of the process... The source and drain regions are created in this thin silicon layer using a suitable heavy dopant. The channel region is the area of active silicon between the source and drain. The gate dielectric is formed over the channel region. Isolation implants can also be implanted in areas of unused active silicon.



EX-1020, FIG. 4, 7:17-18; *see id.*, 10:5-11, 8:28-29 (“The RF switch 10 shown is a single pole two throw (SP2T) switch.”), 1:10-14, 12:27-31, FIG. 16; EX-1039, 9-10; EX-1005 [0040], [0043]; EX-1009, FIG. 2, [0004]-[0005], [0050], [0054], [0058], [0074], [0126], [0142], FIGS. 8-10, 12-14 (discloses SPDT switch in which, **“to achieve a reduction in cost,... silicon[] (CMOS)”** instead of “pHEMT” is used to fabricate the FETs, and as part of an **“integrated on one chip SOICMOS integrated circuit.”**); EX-1018, 4:27-41, 3:50-54, FIGS. 3-4 (in fabricating SPDT switch, “an anchor material such as SiO₂ is grown (or deposited) on a microwave quality wafer or substrate... [of] silicon... [or] silicon on sapphire,... silicon on insulator, etc. Formation of the switch on a **thick oxide layer on a silicon substrate permits control circuitry for control electrodes to be integrated on the same die as the switch.** The oxide also helps **reduce dielectric losses** associated with the

silicon substrate.”); EX-1010, [0009], [0013], FIG. 3A, [0034]-[0036], [0046] (disclosing SP3T switch includes “silicon CMOS based FETs [to] allow[] for **low cost manufacturing** [and] offer[] **integration of the switching circuits with standard Si CMOS transmit/receive circuits**”); EX-1022, [0028] (“Typically, the package size of a pHEMT-based device is significantly larger and consequently more expensive than a similar device implemented in CMOS.”), FIG. 7, [0046]-[0050] (“Integrated Circuit (IC) chip layout” of example SPDT switch and control circuitry); EX-1025, Abstract, 16:11-18, 16:56-61, 20:57-67, FIGS. 12, 17 (“a single IC that includes all devices from a PA, through an antenna switch, and to an antenna connection” provides “substantial savings in device area... as compared to combining discrete ICs to fabricate a comparably-performing transceiver”); EX-1019, [0001], [0004], FIGS. 1, 9, 19, [0013]-[0021], [0073]-[0079], [0148]-[0149], [0159], [0184]-[0191], [0199]-[0200], 68:36-69:21, 70:10-24 (disclosing examples of “MOSFETs fabricated on... SOI... substrates”, with all SPnT switch components integrated on the same wafer, and techniques to control “accumulated charge... in off-state MOSFETs”, which, without such control, can “adversely affect the linearity of the SOI MOSFETs and thereby increasing harmonic distortion and intermodulation distortion...”); *see* Prosecution History Section of my Declaration §IV.C (EX-1002, 61-62; EX-1037, 47-52; Examiner *citing to* EX-1026, [0030] (“The FET device stack 34 may be formed, for example, on a silicon-on-insulator

(SOI) type substrate... Each of the plurality of FET devices 32 in the FET device stack may be a... MOSFET... Utilizing SOI type substrates... may be advantageous in some applications because of the high degree of insulation provided by their internal layers... [I]n an SOI type substrate, the FET devices are formed on a device layer and an insulating layer (also known as a Buried Oxide layer ‘BOX’) may be provided between a handle layer and the device layer. The insulating layer is typically made from an insulating or dielectric type oxide material such as SiO₂ while the handle layer is typically made from a semiconductor, such as silicon (Si)... The degradation in bandwidth normally associated with the stacking of FET devices 32 and the increased parasitic capacitances of the extra components can be reduced utilizing SOI... type substrates.”).

73. It was well-known to POSITAs that monolithic (same die/chip) integration benefits result from forming RF SPnT switches on silicon substrates, with examples provided below (with reproduced images that I have annotated):

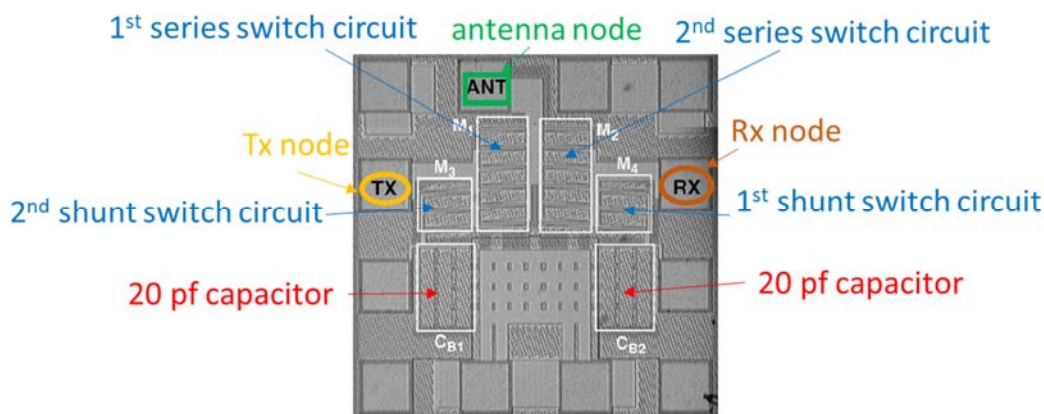


Fig. 2 is a microphotograph of the 0.35 μ m SPDT switch... The die area is 531x531 μ m... SPDT switches implemented using 3.3-V 0.35 μ m NMOS transistors in a 0.18 μ m CMOS process on p silicon substrates for 900-MHz and 2.4-GHz wireless applications have been presented.

EX-1029, FIGS. 1-2, pp. 35-36, 40; *see also* EX-1039, FIG. 12 (“Typical SPDT Switch with Series and Shunt FETs” on the same substrate of the same die);

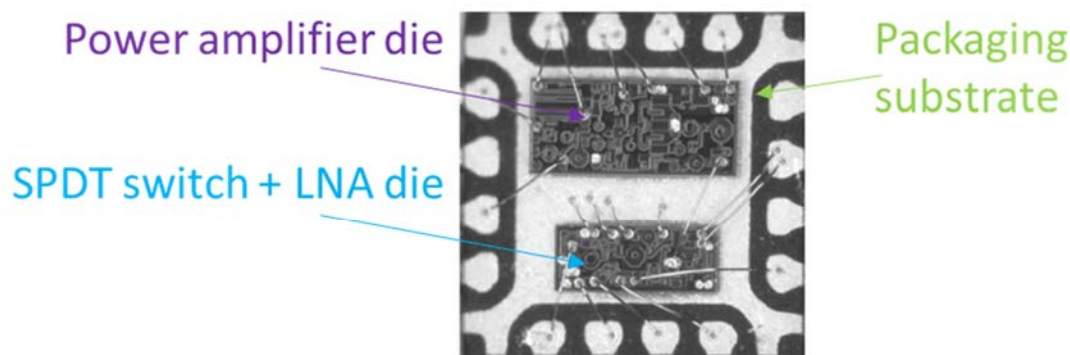


Fig.2. The high linearity 4.9-5.9 GHz FEM in a 3 x 3 mm QFN package.

[For] WLAN radios in portable electronic devices... [a]s shown in Fig. 2, the FEM design consists of two die: a power amplifier (based on SiGe BiCMOS) and a **[dual-band SPDT] switched low noise amplifier (based on Silicon-on-Insulator, SOI)**.

EX-1028, FIGS. 2, 4, 5 (circuit schematics showing components integrated on dual-band-SPDT-LNA die based on SOI), pp. 2-3;

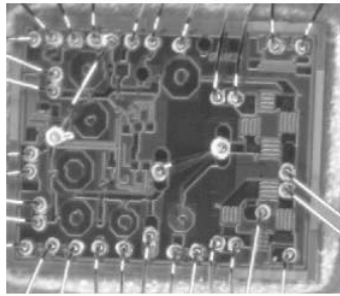


Fig. 1. Die photo for the SP4T T/R switch with dual-band LNA and bypass attenuators. The die size is 1.2x1.6 mm².

In this paper, a novel dual-band, single-pole, 4-throw (**SP4T**) T/R switch with an integrated dual-band LNA and bypass attenuators is presented as shown in Fig. 1. The design is based on SOI technology... **Using SOI technology**, analogue circuitry such as temperature/voltage compensated bias circuits, enable/disable controls, bypass attenuator controllers, and switch logic decoder **can be easily integrated onto the same die.**

EX-1021, FIGS. 1-2, 4-5, pp. 2-3;

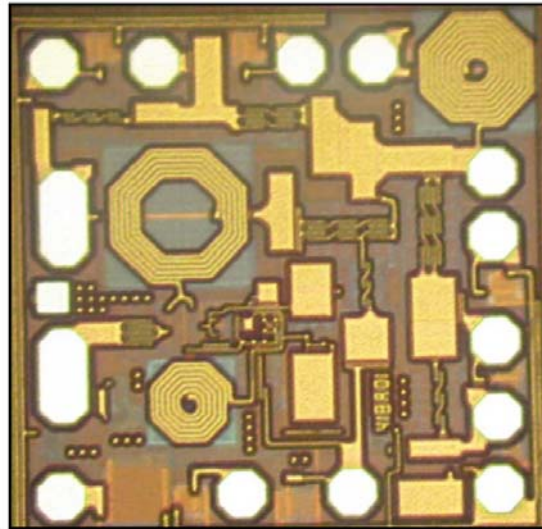


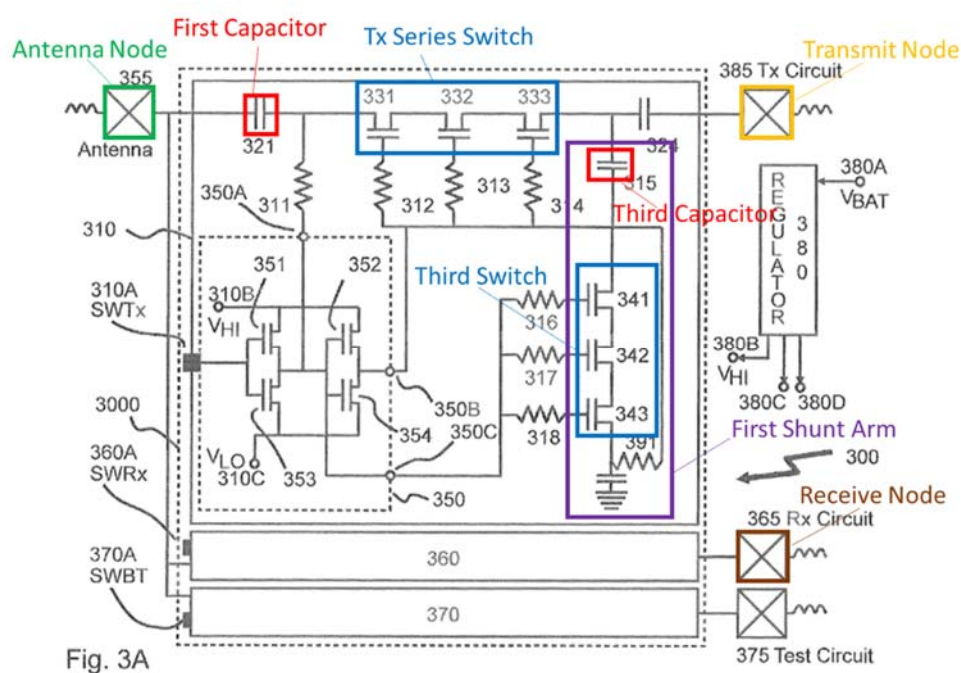
Fig. 8. Die micrograph of the FEIC.

The front-end integrated circuit (FEIC) has been fabricated in IBM's 180-nm bulk **CMOS process**. IBM's 7RF **starting wafer** is lightly

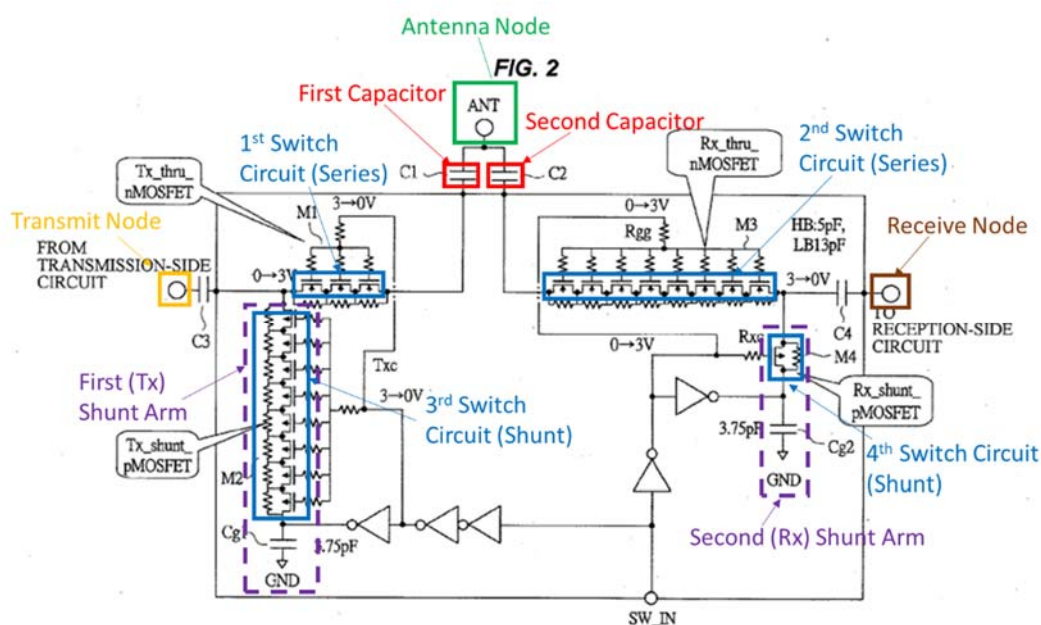
doped p-type Si... The FEIC... **integrates a SP3T switch and a low-noise amplifier with bypass mode**... A micrograph of the fabricated die is shown in Fig. 8. The chip dimensions are 0.8 mm 0.8 mm including **on-chip** dc blocking and decoupling MIM capacitors. EX-1011, FIGS. 1-2, 4-6, 8, 2613-2617; *see* State of the Art Section §VI.B.4 (below) (in which I reproduce, combine and annotate EX-1011, FIGS. 2, 4, 6 as described therein) of my Declaration.

4. Exemplary Known Component Configurations in Series and Shunt Switch Arms of SPnT Transmit-Receive Switches in RF Transceiver Applications

74. By July of 2012, as detailed in the Grounds (*see* Section §VII of my Declaration below) and also shown and described in the below additional examples, the “particular configuration” of components in a SPnT transmit-receive switch of a wireless device—including the positioning of capacitors with respect to the antenna, transmit node and receive node, and the use of shunt arms, as recited in the Challenged Claims—and for purposes of reducing well-known interference susceptibility, and improving other well-known switch performance parameters, were well-known:



EX-1010, FIG. 3A, [0034]-[0036] (“[Tx] switching circuit 310 [depicted and annotated above]... is **often typical** of all three switching circuits [Tx switching circuit] 310, [Rx switching circuit] 360, and [Test switching circuit] 370”), which, in my opinion, POSITAs would understand EX-1010 to disclose the same “particular configuration” of components as ’194 Patent FIG. 9; EX-1010, [0009], [0046] (disclosing SP3T switch formed using silicon CMOS processes and as a “monolithic microwave integrated circuit (MMIC)”); *see* Prosecution History Section §IV.C (EX-1002, 61-62; EX-1037, 37-39), *see* Overview of the ’194 Patent Section §IV.A (FIG. 9, 9:8-35);



EX-1009, FIG. 2 (annotated), [0005], [0060]-[0067], [0074]-[0078], [0083]-[0084] (disclosing an SPDT switch formed using SOI technology with the same “particular configuration” of components as ’194 Patent FIG. 9 except for the 3rd capacitor and 4th capacitor); *see also* Prosecution History Section §IV.C (EX-1002, 61-62; EX-1037, 37-39) of my Declaration; *see also* Overview of the ’194 Patent Section §IV.A (FIG. 9, 9:8-35) of my Declaration;

Transceiver Applications

75. Numerous prior art references (examples which I provide below) confirm that Patent Owner's Cory article's (EX-1024) described configuration—a Transmit-Receive switch module (*e.g.*, SPDT module) interconnected between an antenna and a transceiver configured to process RF signals (*see* State of the Art section §VI.B.2 of my Declaration)—was the conventional, well-known, widely used configuration for RF applications (*e.g.*, mobile devices):

Using a single pole double throw (SPDT) switch and a single antenna is a more practical approach for a WLAN multi-radio architecture when it is desirable to have a small handset... FIG. 3 [reproduced below] depicts an architecture for a WLAN front-end module (FEM), generally indicated at 10, of a wireless portable device. **The FEM 10 is shown coupled to an antenna 20 and a transceiver 30.** Within the FEM 10 are both a transmit path and receive path... **In a preferred implementation of the FEM 10, the switch 90 is a SPDT T/R switch...**

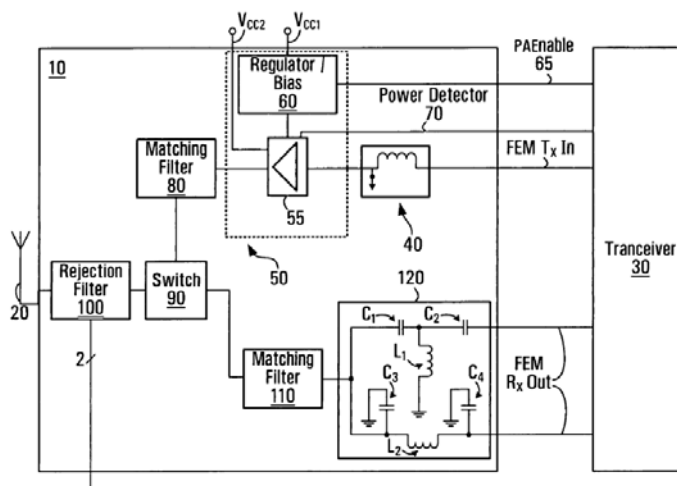


FIG. 3

EX-1023, FIG. 3, 1:43-67, 1:7-9; *see also* EX-1023, 1:13-24, FIG. 6, 7:50-52;

Recently, applications of Wireless LAN (WLAN) radios beyond traditional computer networking to many other electronic appliances, such as cellular phones... [A] commonly used topology for a dual-band WLAN front-end (FE) circuit is seen in Fig. 1, which consists of two Tx and Rx paths where the output ports Ant0 and Ant1 can be connected to individual single band antennas.

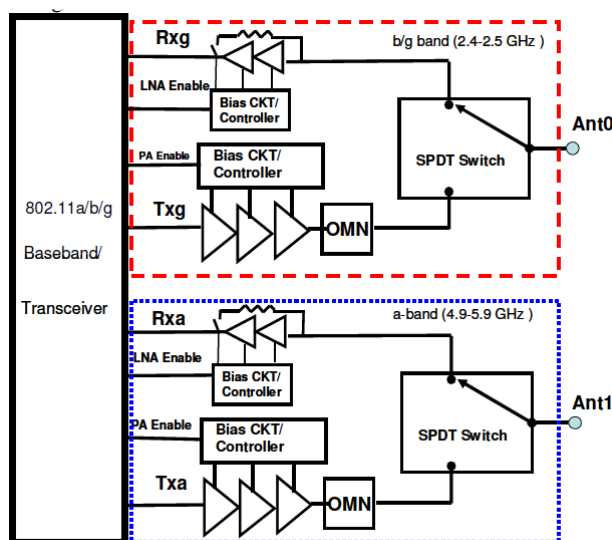


Fig. 1. Block diagram of a dual-band WLAN radio.

EX-1028, 1, FIG. 1;

A **SPDT switch** can be used as a transmit-receive (Tx/Rx) switch, to **alternately connect a transmitter and a receiver to a common single antenna** in a single duplex system, as shown in Figure 3.

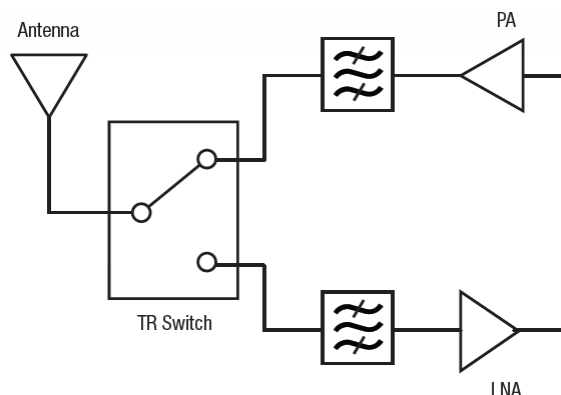


Figure 3. Simplified TR Switching Block Diagram

EX-1008, 3; *see also*, e.g., EX-1041, 1; EX-1039, 1, 3-4, Figures 3-4; EX-1017, FIG. 5, [0027] (“mobile device 500... has mobile processor 504, which is coupled to antenna 536 via transceivers... [t]hese transceivers are further coupled through [SPnT] switches”), [0001], [0016], [0018]; EX-1022, [0004] (“Mobile communication devices... having a transceiver for transmitting and receiving communication signals generally include a radio frequency (RF) switch to switch the antenna between a receive path and a transmit path.”); EX-1025, FIG. 12, 15:24-33, 16:19-18:7, Abstract.

VII. GROUND 1: CLAIMS 1-11 ARE OBVIOUS UNDER 35 U.S.C. §103(A) OVER *HUANG* (EX-1005) IN VIEW OF THE KNOWLEDGE, SKILL, AND CREATIVITY OF A POSITA

A. Identification of Ground

76. Based on my understanding of the law of obviousness that I discuss in Section III of my Declaration (above), it is my opinion that Claims 1-11 of the '194 Patent are obvious over U.S. Patent Publication No. 2011/0254614 to Chun-Wen Huang, et al. ("*Huang*") (EX-1005) in view of the knowledge, skill and creativity of a POSITA.

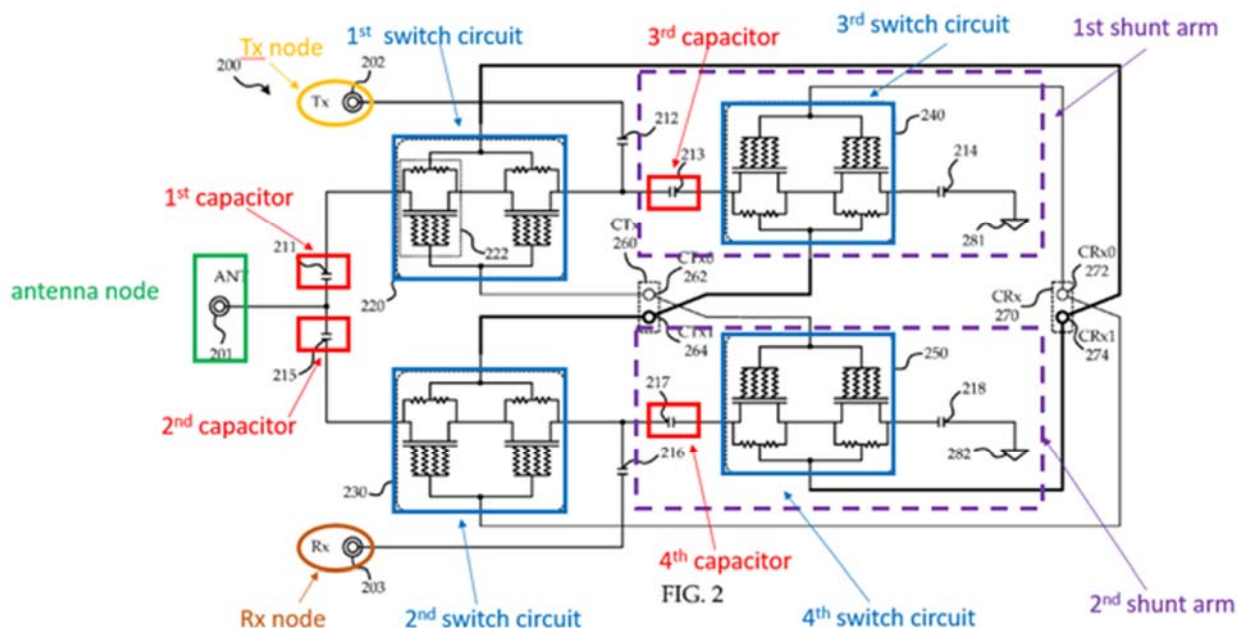
B. Summary of the Huang Reference (EX-1005)

77. Huang discloses the identical "particular configuration" of electrical components as the '194 Patent FIG. 9, in a "semiconductor-based high power switch" of a wireless device (*e.g.*, "WLAN radio"), specifically in a "single pole dual throw (SPDT) transmit-receive switch" formed "using silicon on insulator (SOI)" technology, in which:

- a "**first series FET group switch 220**" (*1st switch circuit*) is connected between "**antenna 201**" (*antenna node*) and "**transmit terminal 202**" (*transmit node*);
- a "**second series FET group switch 230**" (*2nd switch circuit*) is connected between "**antenna 201**" (*antenna node*) and a "**receive terminal 203**" (*receive node*);
- a first "**blocking capacitor 211**" (*1st capacitor*) is "coupled in series with [the] **first series FET group switch 220**" (*1st switch circuit*) and connected

- between the first series FET group switch 220 (*1st switch circuit*) and the antenna 201 (*antenna node*);
- a second “blocking capacitor 215” (*2nd capacitor*) is “coupled in series with [the] second series FET group switch 230” (*2nd switch circuit*) and connected between the second series FET group switch 230 (*2nd switch circuit*) and the antenna 201 (*antenna node*);
 - a first shunt arm is connected to the first series FET group switch 220 (*1st switch circuit*) and the transmit terminal 202 (*transmit node*) via blocking capacitor 212, the first shunt arm including (i) a “first shunt FET group switch 240” (*3rd switch circuit*) connected to ground via blocking capacitor 214; and (ii) a third “blocking capacitor 213” (*3rd capacitor*) that is connected “in series with [the] first shunt FET group switch 240” (*3rd switch circuit*) and connected between the first shunt FET group switch 240 (*3rd switch circuit*) and the transmit terminal 202 (*transmit node*) via blocking capacitor 212; and
 - a second shunt arm is connected to the second series FET group switch 230 (*2nd switch circuit*) and the receive terminal 203 (*receive node*) via blocking capacitor 216, the second shunt arm including (i) a “second shunt FET group switch 250” (*4th switch circuit*) connected to ground via blocking capacitor 218; and (ii) a fourth “blocking capacitor 217” (*4th*

capacitor) that is connected “in series with [the] **second shunt FET group switch 250**” (*4th switch circuit*) and connected between the **second shunt FET group switch 250**” (*4th switch circuit*) and the **receive terminal 20** (*receive node*) via blocking capacitor 216:



EX-1005, Abstract, [0001]-[0002], [0122], [0040], [0042]-[0043], claims 5, 19, [0044]-[0045], FIG. 2 (which I reproduced and annotated above), [0051]; *see* Overview of the '194 Patent Section §IV.A of my Declaration (above); *see* Prosecution History Section §IV.C of my Declaration (above).

78. Huang also discloses the identical operation of the semiconductor-based FET switches in the high-power, SPDT transmit-receive switch as the '194 Patent:

[W]hen the antenna 201 is utilized for **transmission**, the first series FET group switch 220 and the second shunt FET group switch 250 are provided with **on-state** V_{gsd} such that a strong inversion layer creates a low resistance path between source and drain diffusions while the second series FET group switch 230 and the first shunt FET group switch 240 are provided **off-state** V_{gsd} wherein no channel is established.

EX-1005, [0056]; *id.*, [0058] (reception); *see* Overview of the '194 Patent Section §IV.A.

79. Like the '194 Patent, Huang also discloses that the particular disclosed and depicted configuration of the above-identified (and annotated) series and shunt components in the high-power SPDT transmit-receive switch, formed using SOI technology, and controlled FET biasing when the SPDT is in transmit or receive modes, achieves desirable switching performance parameters including “low insertion loss along the signal path”, “high isolation from the off paths”, “improved signal quality”, “reduce[d] spurious harmonic transmissions”, and “good linearity”.

EX-1005, [0002]-[0003], [0039]-[0040], [0043], [0056]; *see* Overview of the '194 Patent Section §IV.A.

C. Detailed Invalidity Analysis of Huang (EX-1005) in View of the Knowledge, Skill and Creativity of a POSITA to the Challenged Claims

a. Claim 1

i. [1.0] A radio-frequency (RF) switch system comprising:

80. To the extent the preamble is limiting, in my opinion, Huang discloses a RF switch system to a POSITA.

81. Huang discloses to POSITAs incorporating a “high power”, “semiconductor-based transmit-receive switch” (*e.g.*, SPDT switch 200) (*switch module*) into an RF/wireless device (*e.g.*, WLAN radio) in which such switch “is often the last/first component encountered by a transmitted/received signal before/after encountering an antenna” (*e.g.*, antenna 201) (*antenna*). EX-1005, [0051], [0002], [0044]-[0045], [0051], FIG. 2. Also, in my opinion, Huang discloses that SPDT switch 200 includes a respective plurality of “series FET group switches” (*e.g.*, 220, 230) and of “shunt FET group switches” (*e.g.*, 240, 250), where each “FET group switch” includes multiple FETs connected in series to each other. EX-1005, *Id.*; [0003], FIG. 2, [0120].

82. In my opinion, POSITAs understood Huang’s disclosure of SPDT switch 200 (including as packaged in a “WLAN radio”) to constitute an *RF switch system*. *Id.*; *see also* my analysis of limitation [7.0] below.

ii. [1.1] a first switch circuit connected between an antenna node and a transmit node;

84. As I show in Annotated FIG. 2 (*see* [1.1] above), Huang discloses SPDT switch 200 includes “a second series FET group switch 230” (*second switch circuit*), that is connected between antenna 201 (*antenna node*) and receive terminal 203 (*receive node*). EX-1005, [0045], [0122], claims 5, 19; *see also* my analysis of limitations [1.0], [1.1] above.

iv. [1.3] a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node;

85. As I show in Annotated FIG. 2 (*see* [1.1] above), Huang discloses the “semiconductor-based” SPDT switch 200 includes a “blocking capacitor 211” (*first capacitor*) that is “coupled in series with a first series FET group switch 220” (*first switch circuit*) and further connected between the first series FET group switch 220 (*first switch circuit*) and the antenna 201 (*antenna node*). EX-1005, [0045], FIG. 2; *id.*, [0001]-[0003], Abstract, [0040], [0042]-[0043], [0122]; *see also* my analysis of limitations [1.0], [1.1] above.

v. [1.4] a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node;

86. As I show in Annotated FIG. 2 (*see* [1.1] above), Huang discloses the “semiconductor-based” SPDT switch 200 includes a “blocking capacitor 215” (*second capacitor*) that is “coupled in series with a second series FET group switch

230” (*second switch circuit*), and further connected between **second series FET group switch 230** (*second switch circuit*) and **antenna 201** (*antenna node*). EX-1005, [0045]; *id.*, [0001]-[0003], Abstract, [0040], [0042]-[0043], [0122]; *see also* my analysis of limitations [1.0], [1.1], [1.2] above.

vi. [1.5.1] a first shunt arm connected to the first switch circuit and the transmit node,

87. As I show in Annotated FIG. 2 (*see* [1.1] above), Huang discloses “[a]long a **shunt path** from the **transmit terminal 202** to the transmit branch ground connection 281, the **transmit terminal 202** is coupled to the blocking capacitor 212, a **blocking capacitor 213** in series with a **first shunt FET group switch 240** and another blocking capacitor 214.” EX-1005, [0045]; *see also* Prosecution History Section §IV.C (EX-1002, 61-62, EX-1037, 37-39) of my Declaration (above).

88. Accordingly, in my opinion POSITAs reading Huang would understand it discloses “semiconductor-based” SPDT switch 200 including, as I show in Annotated FIG. 2 (*see* [1.1] above), a **first shunt arm** that (i) is connected to the **first series FET group switch 220** (*first switch circuit*) and **transmit terminal 202** (*transmit node*) via capacitor 212, and includes (ii) a **first shunt FET group switch 240**, that is connected to “the transmit branch ground connection 281” via capacitor 214 (*third switch circuit connected to ground*), and (iii) also includes **blocking capacitor 213** (*third capacitor*) that is connected in series with **first shunt FET group**

switch 240 (*third switch circuit*) between first shunt FET group switch 240 and transmit terminal 202 (*transmit node*) via capacitor 212. *Id.*, EX-1005, [0001]-[0003], Abstract, [0040], [0042]-[0043], [0122], claims 5, 19; *see* [3.1]; *see also* my analysis of limitation [1.0] above; *see also* Patent Prosecution Section §IV.C (EX-1002, 61-62; EX-1037, 37-39) of my Declaration (above).

vii. [1.5.2] the first shunt arm including a third switch circuit connected to ground;

89. Huang discloses this limitation for the reasons that I discussed regarding claim element [1.5.1].

i. [1.6.1] and a second shunt arm connected to the second switch circuit and the receive node,

90. As I show in Annotated FIG. 2 (*see* [1.1] above), Huang discloses “[a]long a shunt path from the receive terminal 203 to the receive branch ground connection 282, the receive terminal 203 is coupled to the blocking capacitor 216, a blocking capacitor 217 in series with a second shunt FET group switch 250 ...” EX-1005 [0045], FIG. 2.

91. Accordingly, in my opinion, POSITAs reading Huang would understand that it discloses “semiconductor-based” SPDT switch 200 including a second shunt arm that (i) is connected to second series FET group switch 230 (*second switch circuit*) and receive terminal 203 (*receive node*) via capacitor 216,

and includes (ii) a **second shunt FET group switch 250** connected to “receive branch ground connection 282” via capacitor 218 (*fourth switch circuit connected to ground*), and (iii) also includes **blocking capacitor 217** (*fourth capacitor*) that is connected in series with **second shunt FET group switch 250** (*fourth switch circuit*) between **switch 250** and **receive terminal 203** (*receive node*) via capacitor 216. *Id.*, see my analysis of limitation [3.2], below; see also Patent Prosecution Section §IV.C (EX-1002, 61-62; EX-1037, 37-39) of my Declaration (above).

ii. [1.6.2] the second shunt arm including a fourth switch circuit connected to ground.

Huang discloses this limitation for the reasons that I discussed regarding claim element [1.6.1].

b. Claim 2

i. The switch system of claim 1 wherein at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

92. In my opinion, Huang discloses this claim limitation to POSITAs. As discussed in my analysis of claim elements [1.3]-[1.4] (above), and as shown and described in my Annotated FIG. 2 (see [1.1] above), Huang discloses positioning, in SPDT switch 200 (the *switch*), of (i) **blocking capacitor 211** (*first capacitor*) between **antenna 201** (*antenna node*) and **Tx series FET group switch 220** (*first switch circuit*)

and (ii) **blocking capacitor 215** (*second capacitor*) between **antenna 201** (*antenna node*) and **Rx series FET group switch 230** (*second switch circuit*). EX-1005, [0045], Annotated FIG. 2 (*see my analysis of limitation [1.1] above*).

93. In my opinion, Huang's disclosure is identical to the '194 Patent's disclosure positioning, in SPDT switch 250 depicted and described in '194 Patent FIG. 9, of (i) **capacitor C1** between **antenna node 252** and **Tx series switch circuit 120/140** and (ii) **capacitor C2** between **antenna node 252** and **Rx series switch circuit 120/140**. *Id.*; *see* Overview of the '194 Patent §IV.A (EX-1001, 9:25-38, FIG. 9) of my Declaration (above); *see* Patent Prosecution Section §IV.C (EX-1002, 61-62; EX-1037, 31-34, 37-39, 47-48, 339-341) of my Declaration (above).

94. Huang also discloses the importance of selecting the “arrange[ment]” of “groups of FETs” and “judiciously chosen... capacitors”, and of selecting the biasing voltages of the FETs when in “on” and “off” states, in “a high power transmit-receive switch using... SOI” to achieve, for example, “low insertion loss along the signal path”, “high isolation from the off paths”, “reduce[d] spurious harmonic emissions”, and “improve[d] linearity” for the switch. EX-1005, [0002]-[0003], [0039]-[0040], [0043]-[0045], [0055]-[0059].

95. Huang also expressly refers to capacitor 211 (*the first capacitor*) and capacitor 215 as “**blocking capacitor 211**” and “**blocking capacitor 215**”

respectively, and, as I discussed in my analysis of claim elements [1.0]-[1.4] above, Huang discloses, in transmit-receive SPDT switch 200 (*the RF switch*) intended for use in “modern RF communication systems” such as a “WLAN radio”, that (i) “antenna 201 is coupled to [the] blocking capacitor 211 coupled in series with [the] first series FET group switch 220” “along a signal path from the antenna 201 to the transmit terminal 202”, and (ii) “antenna 201 is coupled to [the] blocking capacitor 215 coupled in series with [the] first series FET group switch 230” “along a signal path from the antenna 201 to the receive terminal 203.” *Id.*, EX-1005, [0051]; see my analysis of limitations [1.0]-[1.4].

96. Unsurprisingly, just like the '194 Patent, in my opinion, given the fundamental, frequency-dependent impedance characteristic of capacitors—capacitors allow high frequencies to pass through (essentially acting as short circuits) while blocking low frequencies (essentially acting as open circuits)—outside of specifying the identical arrangement of blocking capacitor 211 (*first capacitor*) and blocking capacitor 215 (*second capacitor*) in SPDT switch 200 as the Applicant’s relied-on arrangement of capacitor C1 and capacitor C2 in SPDT switch 250 (*see* §IV.A-IV.B of my Declaration (above)), Huang leaves the particular capacitor value implementation details to design choices of POSITAs. *Id.*; *see also* my analysis of claim elements [1.0]-[1.4]; State of the Art sections §VI.B.1-§VI.B.2 of my Declaration; *see also* my analysis of claim element [5.4] (below).

97. Moreover, given this fundamental, frequency-dependent impedance characteristic of capacitors, the typical (picofarad) capacitor values selected for RF switches in Huang’s disclosed use cases, and the known solution—having “the switch see[] an open circuit at the blocker frequencies”—to the well-known low frequency, “out-of-band blocker” signal problem in non-linear RF switches, which I discussed in State of the Art sections §VI.B.1-§VI.B.2 of my Declaration, in my opinion, POSITAs would understand Huang’s disclosed implementation of **blocking capacitor 211** and **blocking capacitor 215** in SPDT switch 200 as being high-pass filters “configured to inhibit a low-frequency blocker signal from mixing with a fundamental frequency signal in the RF switch.” *Id.*; *see also* State of the Art section §VI.B.1 (EX-1012, 231-234, 175-176; EX-1027, 82-83, 50; EX-1014, 20, 30, 29-32, 36-37, 39-40, 42, FIGS. 1.52-1.55, 1.56(A); EX-1043, 128-129, 137-139, 236-238, FIGS. 5-17(A), 8-17(B), 8-17(D), 8-18(B), 8-18(D); EX-1011, 2615-2618, FIG. 9A; EX-1024, 3-4; EX-1026, [0049]; EX-1031, 8-9, FIG. 13; EX-1010, [0040], EX-1044, 1-2; EX-1029, 36-39; EX-1032, 1-2; EX-1033, 1; EX-1042, 96, 172, 180, 227, 275, 286, 308, 312; EX-1017, [0025]) of my Declaration (above); *see also* State of the Art section §VI.B.2 (EX-1039, FIG. 5, 2-6, 8-12 (*citing* EX-1040, 3-6, FIGS. 3-4); EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1045, 1; EX-1049, p.3) of my Declaration (above); *see also* my analysis of claim element [5.4] (below).

98. Furthermore, to the extent that the Patent Owner asserts that Huang does not expressly disclose **blocking capacitor 211**, and/or **blocking capacitor 215**, as being configured as claimed, with the SPDT switch 200 components arranged as shown in Annotated FIG. 2 (*see* [1.1] above), and opposing series and shunt switches placed in ON and OFF states depending on the transmit or receive mode of SPDT switch 200 as disclosed by Huang (*see* EX-1005, [0056] (transmission), [0058] (reception)), POSITAs understood these capacitors' inhibition of low-frequency blocker signals from mixing with fundamental frequency signals in SPDT switch 200 to merely be a matter of design choice. *Id.*

99. As I discuss in the State of the Art Sections (§VI.B.1-§VI.B.2) of my Declaration and in my analysis of claim element [5.4] (below), in my opinion, because **blocking capacitor 211** and **blocking capacitor 215**, are fundamentally frequency-dependent circuit elements (with decreasing impedance with increasing frequency), POSITAs understood that tuning the resulting high-pass filters, *i.e.*, setting the frequency range above which **blocking capacitor 211** and **blocking capacitor 215** permit frequencies (*e.g.*, the desired RF frequency) to pass essentially unimpeded, and below which (*e.g.*, the “-3dB breakpoint”) they impede lower frequencies (*e.g.*, low-frequency “out-of-band blocker” signals), is simply a matter of picking the size capacitor that yields the desired pass/inhibit thresholds within the practical size constraints for the RF device (*e.g.*, “traditional WLAN radio”) with a

reasonable expectation of success. *Id. see also* State of the Art Section §VI.B.1 (EX-1009, FIG. 2, [0083], [0084]; EX-1035, 5; EX-1032, FIG. 1; EX-1026, FIG. 2, [0002], [0040], [0049], [0051], [0063]; EX-1042, 294, 298, 308, 312; EX-1049, p.3).

100. As I discussed in the State of the Art sections (§VI.B.1-§VI.B.2) of my Declaration, filtering antenna-201-picked-up, low-frequency, out-of-band-blocker signals was a well-known problem in RF radios, with a well-known solution (*i.e.*, a series capacitor sized to yield the desired frequency-dependent response as a high-pass filter within the practical size constraints for the RF device). *Id.*; *see also* State of the Art section §VI.B.2 (EX-1039, FIG. 5, 2-6, 8-12 (*citing* EX-1040, 3-6, FIGS. 3-4); EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1045, 1; EX-1049, p.3).

101. Accordingly, in my opinion, POSITAs would have been motivated to select appropriately-sized blocking capacitors 211 and 215 to pass (with very low impedance) the high RF frequencies of interest (*e.g.*, 2.4Ghz associated with “traditional WLAN radio[s]”), while impeding low, out-of-band frequencies, within the practical size constraints of such radios, to achieve the known and predictable benefits of improved switch performance (including improved IMD performance) with a reasonable expectation of success given that this involves nothing more than the conventional and routing use of Huang’s blocking capacitors. *Id.*

c. **Claim 3**

- i. ***[3.1] The switch system of claim 1 wherein the first shunt arm includes a third capacitor connected between the third switch circuit and the transmit node, and***

102. As I explained in my analysis of claim elements [1.5.1]-[1.5.2] (above), and as I show in Annotated FIG. 2 (see [1.1] above), Huang discloses that the *first shunt arm*, of the “semiconductor-based” SPDT switch 200, also includes “**blocking capacitor 213**” (*third capacitor*) that is connected to the *first shunt FET group switch 240* (*third switch circuit*) between *switch 240* (*third switch circuit*) and *transmit terminal 202* (*transmit node*). EX-1005, [0045]; see also my analysis of limitations [1.5.1]-[1.5.2].

- ii. ***[3.2] the second shunt arm includes a fourth capacitor connected between the fourth switch circuit and the receive node.***

103. As I explained in my analysis of claim elements [1.6.1]-[1.6.2] (above), and as I show in Annotated FIG. 2 (see [1.1] above), Huang discloses the *second shunt arm*, of the “semiconductor-based” SPDT switch 200 further includes a “**blocking capacitor 217**” (*fourth capacitor*) that is connected to the “*second shunt FET group switch 250*” (*fourth switch circuit*) between *switch 250* (*fourth switch circuit*) and the “**receive terminal 203**” (*receive node*). EX-1005, [0045]; see also my analysis of limitations [1.6.1]-[1.6.2].

d. **Claim 4**

i. ***[4.0] A radio-frequency (RF) switch system comprising:***

104. Huang discloses this limitation for the reasons that I discussed regarding claim element [1.0].

ii. ***[4.1] a first switch circuit connected between an antenna node and a transmit node;***

105. Huang discloses this limitation for the reasons that I discussed regarding claim element [1.1].

iii. ***[4.2] a second switch circuit connected between the antenna node and a receive node;***

106. Huang discloses this limitation for the reasons that I discussed regarding claim element [1.2].

iv. ***[4.3] a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node;***

107. Huang discloses this limitation for the reasons that I discussed regarding claim element [1.3].

v. ***[4.4] a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node;***

108. Huang discloses this limitation for the reasons that I discussed regarding claim element [1.4].

vi. [4.5.1] a first shunt arm connected to the first switch circuit and the transmit node,

109. Huang discloses this limitation for the reasons that I discussed regarding claim element [1.5.1].

vii. [4.5.2] the first shunt arm including a third switch circuit connected to ground and a third capacitor connected between the third switch circuit and the transmit node.

110. Huang discloses this limitation for the reasons that I discussed claim elements [1.5.1]-[1.5.2], [3.1].

e. Claim 5

i. [5.0] A method for fabricating a semiconductor die, the method comprising:

111. To the extent the preamble is limiting, in my opinion, Huang discloses a method for fabricating a semiconductor die, including forming the components of the disclosed single pole dual throw (SPDT) transmit-receive switch (SPDT switch 200) on (*e.g.*, fabricated on, attached to) a semiconductor substrate of a semiconductor die, to POSITAs.

112. Huang states “[t]he invention relates to high power semiconductor switches”, and discloses that the “transistor switches” in such high power, “semiconductor-based transmit-receive switches”, including the SPDT switch 200,

can be “silicon-on-insulator FET switches.” EX-1005, [0001]-[0003], Abstract, [0040], [0042]-[0043], [0122], claims 5, 19, FIG. 2.

113. Accordingly, in my opinion, POSITAs reading Huang would understand Huang discloses providing a semiconductor substrate, and forming the SPDT switch 200 components on the semiconductor substrate to fabricate a semiconductor die, where, in some embodiments, the semiconductor die is a silicon-on-insulator die in which the SPDT switch 200 components would be formed on an insulator layer. EX-1005, [0001]-[0003], Abstract, [0040], [0042]-[0043], [0122], claims 5, 19, FIG. 2.

114. To the extent Patent Owner asserts that Huang does not explicitly disclose providing a semiconductor substrate, and forming the SPDT switch 200 components on the semiconductor substrate to fabricate a semiconductor die, in my opinion, it would have been obvious to POSITAs to do so, as this was the well-known and widely implemented approach to provide a stable foundation for fabrication of components of high power, semiconductor-based, transmit/receive switches, and in order to make manufacturing, testing and production of integrated circuits (including such switches and related circuits (*e.g.*, low noise amplifiers (LNAs), etc.) easier and less costly as I discussed in the State of the Art section §VI.B.3 of my Declaration. *See* State of the Art Section §VI.B.3 (EX-1018, 4:27-

41; EX-1010, [0009], [0013], FIG. 3A, [0046]; EX-1019, [0001], [0004], FIG. 1; EX-1039, 9-10, FIG. 12; EX-1020, FIGS. 1, 4; EX-1009, [0004]-[0005], [0058], FIG. 2; EX-1022, FIG. 7, [0046]-[0050]; EX-1024, 1, 3-4, FIG. 8; EX-1029, FIGS. 1-2, 35-36, 40; EX-1028, 2-3, FIGS. 2, 4, 5; EX-1021, 2-3, FIGS. 1-2, 4-5; EX-1019, [0001], [0004], FIG. 1; EX-1011, 2613-2617, FIGS. 1-2, 4-6, 8).

ii. [5.1] providing a semiconductor substrate;

115. Huang discloses this limitation for the reasons that I discussed regarding claim element [5.0].

iii. [5.2] forming a first switch circuit on the semiconductor substrate so as to be connected between an antenna node and a transmit node;

116. Huang discloses this limitation for the reasons that I discussed regarding claim elements [1.1], [5.0]-[5.1].

iv. [5.3] forming a second switch circuit on the semiconductor substrate so as to be connected between the antenna node and a receive node;

117. Huang discloses this limitation for the reasons that I discussed regarding claim elements [1.2], [5.0]-[5.1].

i. [5.4] forming a first capacitor on the semiconductor substrate so as to be connected in series with the first switch circuit between the first switch circuit and the antenna node;

118. As I show in Annotated FIG. 2 (*see* my analysis of claim element [1.1] (above)), Huang discloses this limitation for the reasons discussed regarding elements [1.3], [5.0].

119. To the extent that Patent Owner asserts that Huang does not explicitly disclose forming “**blocking capacitor 211**” (*first capacitor*) (and, *e.g.*, “**blocking capacitor 213**” (*second capacitor*), *see* [5.5] (below)) on the same semiconductor (*e.g.*, SOI) substrate of the same semiconductor die as the other components (*e.g.*, SOI FETs) of SPDT switch 200, as I discussed in State of the Art sections §VI.B.1-§VI.B.3 of my Declaration, in my opinion, POSITAs would have been motivated to do so as a mere design choice to achieve known and predictable benefits, including making manufacturing, testing, and production of SPDT switch 200 (and integrated circuits (ICs) incorporating the same) easier and less costly, with a reasonable expectation of success, including because low capacitance value (*e.g.*, picofarad) capacitors are small in size and typically used in RF switches since, as was well-known to POSITAs, they would pass (with very low impedance) the desired high frequencies of interest (*e.g.*, 2.4 Ghz associated with “traditional WLAN radio[s]”) while impeding low, out-of-band blocker frequencies. *Id.*; State of the Art section §VI.B.3 (EX-1034, FIG. 2; EX-1035, 2-5; EX-1023, 10:13-17, FIG. 5; EX-1011, 2616-2617, FIG. 4; EX-1029, FIGS. 1-2, pp.35-36, 40; EX-1022, [0028], FIG. 7, [0046]-[0050]; EX-1010, [0009], [0013], FIG. 3A, [0046]) of my Declaration; State

of the Art section §VI.B.1 (EX-1012, 231-234, 175-176; EX-1027, 82-83, 50; EX-1014, 29-32, 36-37, 42; EX-1043, 128-129, 137-139, 236-238; EX-1032, 1-2; EX-1033, 1; EX-1011, 2615-2618; EX-1026, [0049]; EX-1024, 3-4; EX-1031, 8-9; EX-1044, 1-2; EX-1010, [0040]; EX-1009, FIG. 2, [0083]-[0084], EX-1035, 5; EX-1042, 96, 172, 180, 227, 275, 286; EX-1029, 36-39; EX-1017, [0025]) of my Declaration; State of the Art section §VI.B.2 (EX-1024, 1, 3-4; EX-1039, FIG. 5, 2-6, 9-12 (*citing* EX-1040, 3-6, FIGS. 3-4); EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1045, 1; EX-1049, p.3) of my Declaration; *see* [5.0], claim 2.

ii. [5.5] forming a second capacitor on the semiconductor substrate so as to be connected in series with the second switch circuit between the second switch circuit and the antenna node;

120. Huang discloses this limitation for the reasons that I discussed regarding claim elements [1.4], [5.0], [5.4].

iii. [5.6.1] forming a first shunt arm connected to the first switch circuit and the transmit node,

121. Huang discloses this limitation for the reasons that I discussed regarding claim elements [1.5.1].

iv. [5.6.2] the first shunt arm including a third switch circuit connected to ground; and

122. Huang discloses this limitation for the reasons that I discussed regarding claim elements [1.5.1]-[1.5.2], [3.1].

- v. ***[5.7.1] forming a second shunt arm connected to the second switch circuit and the receive node,***

123. Huang discloses this limitation for the reasons that I discussed regarding claim elements [1.6.1].

- vi. ***[5.7.2] the second shunt arm including a fourth switch circuit connected to ground.***

124. Huang discloses this limitation for the reasons that I discussed regarding claim elements [1.6.1]-[1.6.2], [3.2].

f. **Claim 6**

- i. ***The method of claim 5 further comprising forming an insulator layer between the first switch circuit and the semiconductor substrate.***

125. As I explained in my analysis of claim element [5.0] (above), Huang discloses SPDT switch 200 is a “semiconductor-based”, “high-power transmit-receive switch”, that may be “implement[ed]... using silicon on insulator (SOI)” technology, and where each of the “transistor switches” (220, 230, 240, 250) (*first switch circuit, second switch circuit, third switch circuit, fourth switch circuit* respectively) included therein may be “silicon on insulator FET switches.” EX-

1005, [0001]-[0003], Abstract, [0040], [0042]-[0043], [0122], claims 5, 19; *see also* my analysis of limitation [5.0] (above).

126. Unsurprisingly, Huang does not disclose the well-known details of implementing SOI technology to manufacture the “silicon on insulator FET switches” of the “semiconductor-based high power switches”, such as SPDT switch 200, of “the invention.” *Id.* Indeed, as I discussed in State of the Art section §VI.B.3 of my Declaration, it was well-known to POSITAs that, in using SOI technology to create integrated circuits (ICs), an insulator layer is deposited onto a semiconductor substrate of a semiconductor die, silicon is grown on top of this insulator layer, and then the silicon is patterned and etched to create the various components of the integrated circuit (such as the FETs, capacitors, etc. of SPDT switch 200). *Id.*; *see* State of the Art Section §VI.B.3 (EX-1020, FIGS. 1, 4, 8:17-25, 7:17-18, 7:12, 10:5-11, 8:28-29, 1:10-14, 12:27-31, FIG. 16; EX-1026, [0030]; EX-1018, 4:27-41, 3:50-54, FIGS. 3-4; EX-1039, 9-10, FIG. 10).

127. Accordingly, in my opinion, POSITAs understood Huang’s implementation of SOI included an insulator layer disposed between the SOI *first series FET group switch 220* (*first switch circuit*) and the semiconductor substrate. *Id.*; EX-1005, [0001]-[0003], Abstract, [0040], [0042]-[0043], [0122], claims 5, 19.

128. To the extent the Patent Owner asserts that Huang does not expressly disclose an insulator layer disposed between the SOI **first series FET group switch 220** and the semiconductor substrate, in my opinion, it would have been obvious to POSITAs to do so as this was the well-known and widely implemented approach to using the disclosed SOI technology to manufacture “semiconductor-based high power switches”, such as Huang’s SPDT switch 200, with well-known and predictable benefits including, for example, lower cost, higher “thermal conductivity”, reduced “degradation in bandwidth associated with the stacking of FET devices”, “reduce[d] dielectric losses associated with the silicon substrate”, allowing monolithic (same die/chip) integration of SPnT switch and control components and other front-end module (FEM) components, etc. *Id.*; see State of the Art Section §VI.B.3 (EX-1018, 4:37-41; EX-1026, [0030]; EX-1021, 2; EX-1009, [0005]; EX-1010, [0013]).

g. Claim 7

i. [7.0] A radio-frequency (RF) switch module comprising:

129. To the extent the preamble is limiting, as I discussed in claim elements [1.0] and [5.0], in my opinion, Huang discloses to POSITAs forming the components of SPDT switch 200 on a semiconductor substrate of a semiconductor die, and incorporating SPDT switch 200 into an RF/wireless device (*e.g.*, “WLAN radio”) in

which such switch “is often the last/first component encountered by a transmitted/received signal before/after encountering an antenna” (*e.g.*, antenna 201) (*antenna*). EX-1005, [0001]-[0003], Abstract, [0040], [0042]-[0045], [0051], 0122], claims 5, 19, FIG. 2. In my opinion, POSITAs understood that Huang’s disclosure of SPDT switch 200, formed for use as a component incorporated into (*e.g.*, in a packages RF switch module, FEM, etc.) RF/wireless devices, to constitute an *RF switch module*. *Id.*

130. Unsurprisingly, Huang does not disclose the well-known details of packaging the components of SPDT switch 200 for testing, shipment, commercial sale, etc., for such use in such RF/wireless devices. *Id.* Indeed, as I discussed in State of the Art section §VI.B.3 of my Declaration, given that the well-known, and widely implemented approach to package a semiconductor die (or plurality of dies) for testing, shipment, commercial sale, etc. of an SPnT switch, and of any other components that are incorporated into the packaged module (*e.g.*, external capacitors, control circuitry, LNA, etc.), was to mount each separate die (and/or surface mountable component) on, and electrically connect (*e.g.*, wire-bond) each separate die (and/or surface mountable component) to, a packaging substrate (*e.g.*, printed circuit board (PCB)), in my opinion, POSITAs would have been motivated to do so as a mere design choice with a high likelihood of success of achieving well-known benefits, such as making packaging, testing, production, shipment, and

commercial sales of packaged products (*e.g.*, RF switch module, FEM, etc.) easier, less costly, and more attractive to customers. *Id.*; see State of the Art Section §VI.B.3 (EX-1008, 1-3; EX-1041, 2; EX-1029, 36-39, Figures 4, 8; EX-1033, 1; EX-1028, 1, 4, Fig. 2; EX-1038, [0010], [0027], [0029], [0030]-[0032], [0036]-[0037], [0045], FIGS. 2-3; EX-1042, 80-82 (WLAN 802.11b, g, n Intera™ Front-End Module Single Antenna); 95-97 (WLAN 802.11b, g, n Intera™ Front-End Module); 105-106 (WLAN 802.11a, b, g, n Dual-Band, Front-End Module Single Antenna); 171-172 (GaAs SPDT Switch 100 MHz–2.5 GHz); 180-181 (GaAs IC High-Isolation Positive Control SPDT Switch 300 kHz–3 GHz); 192-193 (GaAs SPDT Switch 300 kHz–3 GHz Medium Power); 210 (PHEMT GaAs IC SPDT Switch LF–4 GHz); 221-222 (GaAs SPDT 7 W Switch 100 MHz–4 GHz); 226-227 (GaAs IC High-Isolation SPDT Nonreflective Switch with Driver LF–6 GHz); 237-238 (PHEMT SP2T Switch 0.5–6.0 GHz); 242 (PHEMT GaAs IC 1 W Low Loss 0.1–6 GHz SPDT Switch); 274-275 (GaAs T/R Diversity Switch LF–6 GHz); 285-286 (GaAs SP3T Absorptive Switch 500 MHz–2.5 GHz); 298-299 (PHEMT GaAs IC High-Power SP4T Switch 0.1–2.5 GHz); 312-313 (PHEMT GaAs IC SP3T Switch 0.1–3.0 GHz); EX-1021, 1-3; EX-1031, 1, 3, 9-11; EX-1032, 1-2; EX-1022, [0028]) of my Declaration.

- ii. [7.1] a packaging substrate configured to receive a plurality of components;*

131. POSITAs reading Huang would have been motivated to implement this limitation as discussed in claim elements [1.0], [5.0], [7.0].

iii. [7.2] a semiconductor die mounted on the packaging substrate,

132. Huang discloses this limitation for the reasons that I discussed regarding claim elements [5.0], [7.0].

iv. [7.3.1] the die including a first switch circuit connected between an antenna node and a transmit node and

133. Huang discloses this limitation for the reasons that I discussed regarding claim elements [1.1]-[1.2], [5.0], [7.0].

v. [7.3.2] a second switch circuit connected between the antenna node and a receive node;

Huang discloses this limitation for the reasons that I discussed regarding [1.1]-[1.2], [5.0], [7.0].

vi. [7.4] a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node;

134. Huang discloses this limitation for the reasons that I discussed regarding claim element [1.3].

vii. [7.5] a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node;

135. Huang discloses this limitation for the reasons that I discussed regarding claim element [1.4].

viii. [7.6.1] a first shunt arm connected to the first switch circuit and the transmit node,

136. Huang discloses this limitation for the reasons that I discussed regarding claim element [1.5.1].

ix. [7.6.2] the first shunt arm including a third switch circuit connected to ground; and

137. Huang discloses this limitation for the reasons that I discussed regarding claim elements [1.5.1]-[1.5.2].

x. [7.7.1] a second shunt arm connected to the second switch circuit and the receive node,

138. Huang discloses this limitation for the reasons that I discussed regarding claim element [1.6.1].

xi. [7.7.2] the second shunt arm including a fourth switch circuit connected to ground.

139. Huang discloses this limitation for the reasons that I discussed regarding claim elements [1.6.1]-[1.6.2].

h. Claim 8

i. The switch module of claim 7 wherein at least one of the first and second capacitors is configured to inhibit a low-frequency blocker

signal from mixing with a fundamental-frequency signal in the switch.

140. Huang discloses this limitation for the reasons that I discussed regarding Claim 2.

i. **Claim 9**

i. ***The switch module of claim 7 wherein the first capacitor is part of the same semiconductor die as the first switch circuit.***

141. Huang discloses this limitation for the reasons that I discussed regarding claim elements [7.0], [5.4].

j. **Claim 10**

i. ***The switch module of claim 7 wherein the first capacitor is part of a second die mounted on the packaging substrate.***

142. As the '194 Patent itself acknowledges, and as I discussed in my analysis of claim elements [7.0], [5.0], and [5.4] and in State of the Art sections §VI.B.3, §VI.B.1 of my Declaration, POSITAs understood this limitation to be obvious as a mere (and well-known) design choice—selecting between forming Huang's **blocking capacitor 211** (and the other blocking capacitors) on the same die as the **FET group switches**, or on a separate capacitor die (*second capacitor die mounted on the packaging substrate*), or mounting them as surface mountable components on the same packaging substrate on which the FET-group-switch-die is

mounted (claim 11)—based on, for example, size/space constraints, the RF application, the fundamental frequency values, and blocking frequency values, associated with such application, performance requirements, etc., and with well-known benefits and tradeoffs. *See* [7.0], [5.0], [5.4], EX-1005, [0045], Annotated FIG. 2, [0001]-[0002], [0120]-[0124]; *see* State of the Art section §VI.B.3 (EX-1035, 2-5; EX-1034, FIG. 2; EX-1032, 1-2; EX-1033, 1; EX-1023, 10:13-17, 8:29-37, 5:59-6:21, FIG. 5; EX-1011, 2616-2617, FIGS. 4, 8; EX-1029, 35-36, 40, Figures 1-2) of my Declaration; State of the Art section §VI.B.1 (EX-1014, 36-37; EX-1043, 137-139; EX-1026, [0049], [0063]; EX-1011, 2615-2618; EX-1009, FIG. 2, [0083]-[0084]; EX-1024, 3; EX-1031, 8-9, EX-1032, FIG. 1; EX-1042 96 (WLAN 802.11b, g, n Intera™ Front-End Module), 172 (GaAs SPDT Switch 100 MHz–2.5 GHz), 180 (PHEMT 10 W SPDT Switch 500 MHz–2.5 GHz), 227 (GaAs IC High-Isolation SPDT Nonreflective Switch with Driver LF–6 GHz), 275 (GaAs T/R Diversity Switch LF–6 GHz), 286 (GaAs SP3T Absorptive Switch 500 MHz–2.5 GHz), 298 (GaAs SP4T Absorptive Switch 20 MHz–2.5 GHz), 312 (PHEMT GaAs IC SP3T Switch 0.1–3.0 GHz) of my Declaration; *see also* Overview of the '194 Patent Section §IV.A (EX-1001, 9:45-49, 2:15-21, 9:62-10:11, FIGS. 11A-11D).

k. Claim 11

- i. The switch module of claim 7 wherein the first capacitor is disposed at a location outside of the semiconductor die.*

143. Huang discloses this limitation for the reasons that I discussed regarding claim element [7.0], claim 10.

VIII. GROUND 2: CLAIMS 1-11 ARE OBVIOUS UNDER 35 U.S.C. §103(A) OVER SESHIMO IN VIEW OF THE KNOWLEDGE, SKILL, AND CREATIVITY OF A POSITA

A. Identification of Ground

144. Based on my understanding of the law of obviousness that I discuss in Section III of my Declaration (above), it is my opinion that Claims 1-11 of the '194 Patent are obvious over Japanese Patent Publication No. JP2006-121217A to Seshimo, et al. ("*Seshimo*") (EX-1006/EX-10079) in view of the knowledge, skill and creativity of a POSITA.

B. Summary of the Seshimo Reference (EX-1007)

145. Seshimo discloses the same "particular configuration" of components as '194 Patent FIG. 9, in a "high frequency semiconductor switching circuit... used

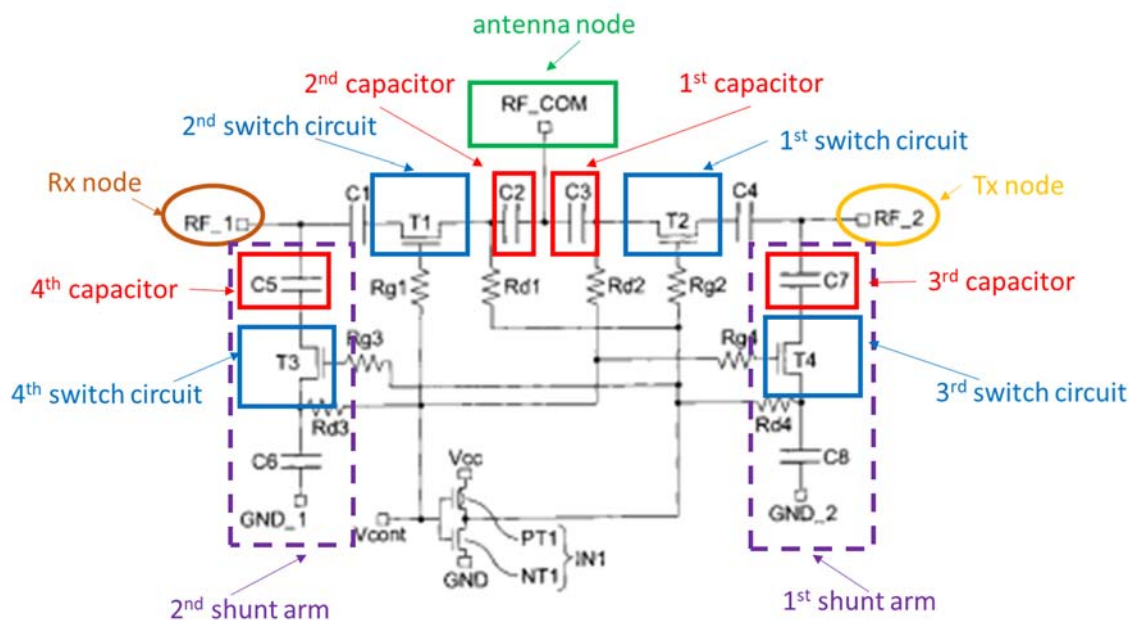
⁹ A Japanese language copy of *Seshimo* can be found in Exhibit 1006, and a copy of a certified English translation of EX-1006 can be found in Exhibit 1007. Generally, in my Declaration, when I am referencing the disclosure of Seshimo, I will cite to Exhibit 1007.

as a transmission/reception changeover switch” (FIG. 3 “shunt SPDT switch”) of a wireless device (e.g., “PHS (Personal Handyphone System)”):

- a “MOSFET T2” (*1st switch circuit*) is connected between the “common terminal RF_COM” (*antenna node*) and a “high-frequency signal terminal RF_2” (*transmit node*);
- a “MOSFET T1” (*2nd switch circuit*) is connected between the common terminal RF_COM (*antenna node*) and a “high-frequency signal terminal RF_1” (*receive node*);
- a first “capacitor C3” (*1st capacitor*) is connected in series with MOSFET T2 (*1st switch circuit*), and connected between MOSFET T2 (*1st switch circuit*) and common terminal RF_COM (*antenna node*);
- a second “capacitor C2” (*2nd capacitor*) is connected in series with MOSFET T1 (*2nd switch circuit*), and connected between MOSFET T1 (*2nd switch circuit*) and common terminal RF_COM (*antenna node*);
- a first shunt arm (i) is connected to MOSFET T2 (*1st switch circuit*) via capacitor C4 and to high-frequency signal terminal RF_2 (*transmit node*), includes (ii) “MOSFET T4” (*3rd switch circuit*) connected to “high-frequency ground terminal GND” (*ground*) via capacitor C8, and includes (iii) a third “capacitor C7” (*3rd capacitor*) connected between

MOSFET T4 (3rd switch circuit) and high-frequency signal terminal RF_2 (transmit node);

- a second shunt arm (i) is connected to MOSFET T1 (2nd switch circuit) via capacitor C1 and to high-frequency signal terminal RF_1 (receive node), includes (ii) “MOSFET T3” (4th switch circuit) connected to “high-frequency ground terminal GND” (ground)) via capacitor C6, and includes (iii) a fourth “capacitor C5” (4th capacitor) between MOSFET T3 (4th switch circuit) and high-frequency signal terminal RF_1 (receive node):



EX-1007, [0001], [0003], [0005], [0007], [0029], [0037], [0042], [0054]-[0056], [0065]-[0072], [0090], FIG. 3 (which I reproduced and annotated above); see Overview of the '194 Patent section §IV.A of my Declaration (above) (EX-1001,

9:8-35, FIG. 9); *see also* Prosecution History section §IV.C of my Declaration (above).

146. Seshimo also discloses the identical operation of its MOSFETs, “formed on a silicon substrate” in the “high frequency semiconductor switching circuit... used as a transmission/reception changeover switch” as the ’194 Patent:

A control voltage V_{cont} of 0 V is input to an input terminal of the inverter circuit IN1, **turning OFF the MOSFETs T1, T4**. A power supply voltage V_{cc} of 3 V is output from an output terminal of the inverter circuit IN1, **turning ON the MOSFETs T2, T3**. As a result, a cutoff state is established between the terminals RF_1 and RF_COM, and a conductive state is established between the terminals RF_2 and RF_COM.

Id.; EX-1007, [0065]-[0066] (*e.g.*, transmission), [0067]-[0068] (*e.g.*, reception); *see also* Overview of the ’194 Patent section §IV.A (EX-1001, 9:44-49; *id.*, FIG. 10, 3:65-5:11, FIG. 3, 4:35-48, FIG. 4) of my Declaration.

147. Like the ’194 Patent, Seshimo discloses that the particular configuration of the above-identified (and annotated) series and shunt components in the “high frequency semiconductor switching circuit... used as a transmission/reception changeover switch”, formed using CMOS processes and SOI, and controlled FET biasing when the SPDT is in transmit mode or receive mode, achieves desirable switching performance parameters including “improving

the maximum permissible input [power/amplitude] to maintain an OFF state” (*e.g.*, power usable by a “PHS (Personal Handyphone System)”), and “suppressing an increase in ON resistance” (that, without suppression, would “lead to an increase in insertion loss” and a “deterioration in isolation”). EX-1007, [0002]-[0005], [0007], [0011], [0026]-[0030], [0037], [0039]-[0040], [0042]-[0043], [0054]-[0056], [0065]-[0072], [0090]; *see also* Overview of the ’194 Patent Section §IV.A.

C. Detailed Invalidity Analysis of Seshimo (EX-1007) in View of the Knowledge, Skill and Creativity of a POSITA to the Challenged Claims

a. Claim 1

i. [1.0] A radio-frequency (RF) switch system comprising:

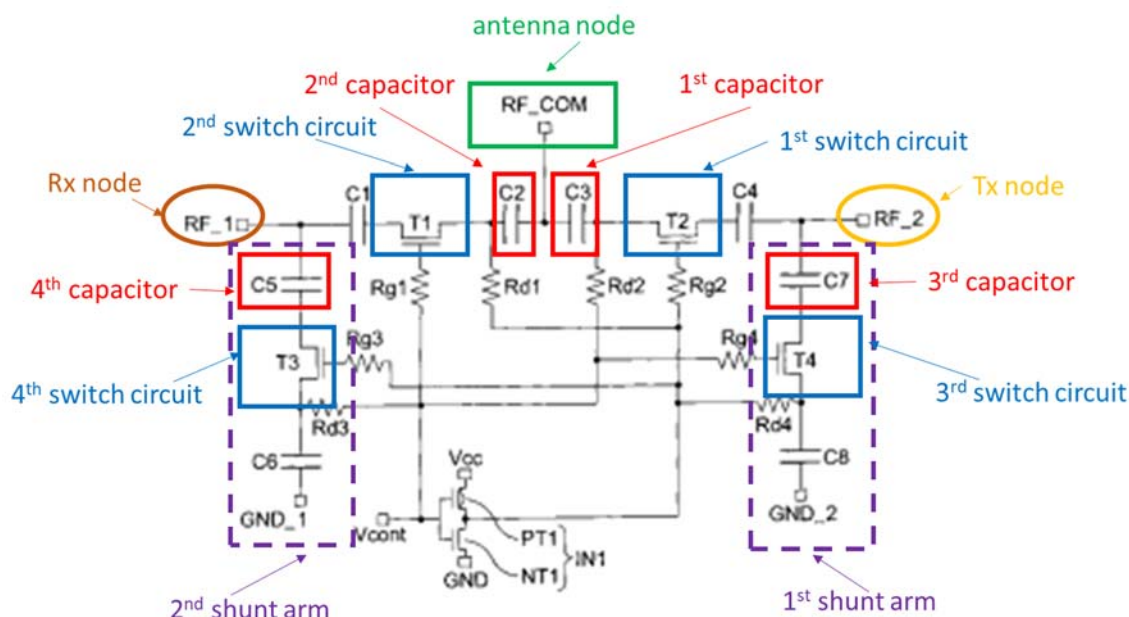
148. To the extent the preamble is limiting, in my opinion, Seshimo discloses a “high frequency semiconductor switching circuit... used as a transmission/reception changeover switch” of a wireless device (*e.g.*, “PHS (Personal Handyphone System)”), specifically in a FIG. 3 “shunt SPDT switch” formed “using a CMOS process” (*e.g.*, “using a SOI... substrate”). EX-1007, FIG. 3, [0001], [0003], [0005], [0007], [0029], [0037], [0042], [0054]-[0056], [0065]-[0072], [0084].

149. Seshimo discloses this “transmission/reception changeover [SPDT] switch” can include vertically “stacking” MOSFETs or “multi-gate structures” to

achieve an even larger maximum permissible input power. EX-1007, [0005], [0071]. POSITAs understood Seshimo's disclosure of FIG. 3 shunt SPDT switch (including as packaged in a PHS) to constitute an *RF switch system*. *Id.*

ii. [1.1] a first switch circuit connected between an antenna node and a transmit node;

150. In my opinion, POSITAs understood that Seshimo discloses FIG. 3 “shunt SPDT switch” includes “MOSFET T2” (*first switch circuit*) connected between “common terminal RF_COM” (*antenna node*) and “high-frequency signal terminal RF_2” (*transmit node*) as illustrated in FIG. 3 as I have annotated below (which I will refer to in Section VIII.C of my Declaration as “Annotated FIG. 3”):



EX-1007, FIG. 3, [0001], [0003], [0005], [0007], [0029], [0037], [0042], [0054]-[0056]. Seshimo discloses that “the MOSFETs T1[, T2, T3 and] T4 can be stacked

vertically or a multi-gate structure can be used.” EX-1007, [0071], FIG. 3; *see* my analysis of claim elements [1.2], [1.5.1]-[1.5.2], [1.6.1]-[1.6.2] (below).

151. In my opinion, given Seshimo’s disclosure that, for example, the FIG. 3 SPDT switch could achieve the “maximum permissible input power... usable by a PHS (Personal Handyphone System)” where it would be “used as a transmission/reception changeover switch” (EX-1007, [0029], [0070]-[0071], [0005], [0007]), and emphasis on the disclosed “high-frequency semiconductor switching circuit[s]” (*e.g.*, FIG. 3) being “developed... using CMOS processes” so the “CMOS switch can be integrated into another CMOS RF IC” (EX-1007, [0003], [0084], [0087]-[0088]), POSITAs understood Seshimo discloses “common terminal RF_COM” as an *antenna node*, and “high-frequency signal terminal RF_2” and “high-frequency signal terminal RF_1” may be a *transmit node* and a *receive node*, respectively.

iii. ***[1.2] a second switch circuit connected between the antenna node and a receive node;***

152. As I show in Annotated FIG. 3 (*see* my analysis of [1.1] above), Seshimo discloses shunt SPDT switch (FIG. 3) includes MOSFET T1 (*second switch circuit*) that is connected between common terminal RF_COM (*antenna node*) and “high-frequency signal terminal RF_1” (*receive node*). EX-1007, FIG. 3, [0054]-[0056]; [1.1].

iv. ***[1.3] a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node;***

153. As I show in Annotated FIG. 3 (see my analysis of [1.1] above), Seshimo discloses a **capacitor C3** (*first capacitor*), that, (i) like the other capacitors (**C2, C5, C7**, etc.), may have a “MIM (metal-insulator-metal) structure”, and (ii) is connected in series with **MOSFET T2** (*first switch circuit*) and between **MOSFET T2** (*first switch circuit*) and **common terminal RF_COM** (*antenna node*). EX-1007, [0054]-[0056], [0065]-[0071], FIG. 3.

154. In my opinion, POSITAs understood that Seshimo discloses resistor Rd2 (and likewise Rd1 and the other resistors in the FIG. 3 circuit) are used for DC biasing only, such that the depicted Rd2 contact to the series path between **MOSFET T2** and **RF_COM** via **capacitor C3** is a “y-junction”, which, in my opinion, a POSITA understood does not alter the series connection between **MOSFET T2** and **capacitor C3**. EX-1007, [0055]-[0056], [0059]-[0061].

v. ***[1.4] a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node;***

155. As I discussed in my analysis of claim element [1.3] (above), Seshimo discloses a **capacitor C2** (*second capacitor*) that, (i) like the other capacitors (**C1, C5, C7**, etc.), may have a “MIM (metal-insulator-metal) structure”, and (ii) is

connected in series between MOSFET T1 (second switch circuit) and common terminal RF_COM (antenna node) as illustrated in Annotated FIG. 3 (see [1.1]). EX-1007, [0054]-[0056], [0065]-[0071].

156. As I also discussed in my analysis of claim element [1.3] (above), POSITAs understood that resistor Rd1's contact to the series path between MOSFET T1 and RF_COM via capacitor C2 is a "y-junction", which, in my opinion, does not alter the series connection between MOSFET T1 and capacitor C2. *Id.*; EX-1007, [0055]-[0056], [0059]-[0061].

vi. ***[1.5.1] a first shunt arm connected to the first switch circuit and the transmit node,***

157. Seshimo discloses, "in a state in which the inverter circuit IN1 is shared", one of "four units" of "shunt SPDT switch" (FIG. 3) includes "a MOSFET T4, capacitors C7 and C8..." and discloses, during, for example, receive operations (see my analysis of claim elements [1.1]-[1.2] (above)) of this SPDT switch:

A control voltage Vcont of 0 V is input to ... inverter circuit IN1, **turning OFF the MOSFETs T1, T4.** A power supply voltage Vcc of 3 V is output from an output terminal of the inverter circuit IN1, **turning ON the MOSFETs T2, T3.** As a result, a cutoff state is established between the terminals RF_1 and RF_COM, and a conductive state is established between the terminals RF_2 and RF_COM. When the control voltage Vcont is 3 V The MOSFETs T1,

T4 are in an ON state, and the MOSFETs T2, T3 are in an OFF state. As a result, a conductive state is established between the terminals RF_1 and RF_COM, and a cutoff state is established between the terminals RF_2 and RF_COM.

EX-1007, [0054]-[0056], [0065]-[0066] (e.g., transmission), [0067]-[0068] (e.g., reception).

158. Accordingly, in my opinion, POSITAs understood Seshimo discloses a *first shunt arm* that is connected to MOSFET T2 (*first switch circuit*) via capacitor C4 and to high-frequency signal terminal RF_2 (*transmit node*), and includes (i) MOSFET T4 connected to “high-frequency ground terminal GND” via capacitor C8 (*third switch circuit connected to ground*), and (ii) capacitor C7 (*third capacitor connected between MOSFET T4 (third switch circuit) and high-frequency signal terminal RF_2 (transmit node)*) as illustrated in Annotated FIG. 3 (*see my analysis of element [1.1] (above)*). *Id.*; EX-1007, [0001], [0003], [0007], [0065]-[0071], [0082], [0084], [0087]-[0088], [0090]; *see also, e.g.,* Prosecution History section §IV.C of my Declaration (EX-1002, 61-62; EX-1037, 37-39).

vii. ***[1.5.2] the first shunt arm including a third switch circuit connected to ground;***

159. Seshimo discloses this limitation for the reasons that I discussed regarding claim element [1.5.1].

viii. *[1.6.1] and a second shunt arm connected to the second switch circuit and the receive node,*

160. Seshimo discloses, “in a state in which the inverter circuit IN1 is shared”, another of “four units” of FIG. 3 “**shunt** SPDT switch” includes “**MOSFET T3**, **capacitors C5** and C6...”, and during, for example, transmit operations (*see my analysis of claim elements [1.1]-[1.2] (above)*) of this SPDT switch:

A control voltage V_{cont} of 0 V is input to ... inverter circuit IN1, **turning OFF the MOSFETs T1, T4**. A power supply voltage V_{cc} of 3 V is output from an output terminal of the inverter circuit IN1, **turning ON the MOSFETs T2, T3**. As a result, a cutoff state is established between the terminals RF_1 and RF_COM, and a conductive state is established between the terminals RF_2 and RF_COM. When the control voltage V_{cont} is 3 V The **MOSFETs T1, T4** are in **an ON state**, and the **MOSFETs T2, T3** are in **an OFF state**. As a result, a conductive state is established between the terminals **RF_1** and **RF_COM**, and a cutoff state is established between the terminals **RF_2** and **RF_COM**.

EX-1007, [0054]-[0056], [0065]-[0066] (*e.g.*, transmission), [0067]-[0068] (*e.g.*, reception); *see also* my analysis of claim elements [1.5.1]-[1.5.2] (above).

161. Accordingly, in my opinion, POSITAs would understand that Seshimo discloses the SPDT switch (FIG. 3) includes a *second shunt arm* that is connected to **MOSFET T1** (*second switch circuit*) via capacitor C1 and to **high-frequency signal terminal RF_1** (*receive node*), and includes (i) **MOSFET T3** connected to high-

frequency ground terminal GND via capacitor C6 (*fourth switch circuit connected to ground*), and (ii) capacitor C5 (*fourth capacitor*) connected between MOSFET T3 (*fourth switch circuit*) and high-frequency signal terminal RF_1 (*receive node*) as illustrated in Annotated FIG. 3 (*see my analysis of claim element [1.1] (above)*). *Id.*, *see also, e.g.*, Prosecution History section §IV.C of my Declaration (EX-1002, 61-62; EX-1037, 37-39).

ix. [1.6.2] the second shunt arm including a fourth switch circuit connected to ground.

162. Seshimo discloses this limitation for the reasons that I discussed regarding element claim element [1.6.1].

b. Claim 2

i. The switch system of claim 1 wherein at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

163. In my opinion, Seshimo discloses this limitation to POSITAs. As I discussed in my analysis of claim elements [1.3]-[1.4] (*above*), and as shown and described in my Annotated FIG. 3 (*see my analysis of claim element [1.1] (above)*), Seshimo discloses positioning, in shunt SPDT switch (FIG. 3) (*the switch*), of (i) capacitor C3 (*first capacitor*) between common terminal RF_COM (*antenna node*) and Tx series MOSFET T2 (*first switch circuit*), and (ii) capacitor C2 (*second*

capacitor) between common terminal RF_COM (antenna node) and Rx series MOSFET T1 (second switch circuit). EX-1007, [0055]-[0056], FIG. 3.

164. In my opinion, Seshimo's disclosure is identical to the '194 Patent's disclosure of positioning, in SPDT switch 250 depicted and described in '194 Patent FIG. 9 (and relied on for allowance of the claims), of (i) capacitor C1 (first capacitor) between antenna node 252 and Tx series switch circuit 120/140 (first switch circuit), and (ii) capacitor C2 (second capacitor) between antenna node 252 and Rx series switch circuit 120/140 (second switch circuit). EX-1007, [0055]-[0056], FIG. 3; see Patent Prosecution section §IV.C (EX-1002, 61-62; EX-1037, 31-34, 37-39, 47-48, 339-341) of my Declaration; see also Overview of the '194 Patent section §IV.A (EX-1001, 9:25-38, FIG. 9) of my Declaration.

165. Seshimo also discloses the importance of selecting substrates (e.g., SOI) and capacitor structures (e.g., MIM) with “excellent high frequency properties”, of selecting biasing voltages of the MOSFETs when in “ON” and “OFF” states, and of selecting the FIG. 3 “shunt SPDT switch” configuration (with identical C3, C2, C7 and C5 capacitor positioning as the '194 Patent FIG. 9 C1, C2, C3 and C4 positioning) instead of the FIG. 4 “shunt SPDT switch” configuration (with shared capacitor C3 between RF_COM and MOSFET T2 and MOSFET T1, and no top capacitor in either the first shunt arm or the second shunt arm), in order to be

able to “provide a semiconductor switching circuit capable of improving the maximum permissible input power while suppressing an increase in ON-resistance” (that, without suppression, would “lead to an increase in insertion loss” and a “deterioration in isolation”). EX-1007, FIG. 3 ([0054]-[0056], [0064]-[0071]), FIG. 4 ([0072]-[0073], [0077], [0079]-[0081]), [0082], [0084], [0087], [0001], [0004]-[0005], [0007].

166. Unsurprisingly, just like the '194 Patent, given the fundamental, frequency-dependent impedance characteristic of capacitors—capacitors allow high frequencies to pass through (essentially acting as short circuits) while blocking low frequencies (essentially acting as open circuits)—outside of specifying the identical arrangement of **capacitor C3** (*first capacitor*) and **capacitor C2** (*second capacitor*) in FIG. 3 shunt SPDT switch, as the Applicant’s relied-on arrangement of **capacitor C1** and **capacitor C2** in SPDT switch 250 (*see* §IV.A-IV.B of my Declaration (above)), Seshimo leaves the particular capacitor value implementation details to the design choice of a POSITA. *Id.*; *see also* State of the Art sections §VI.B.1-§VI.B.2 of my Declaration.

167. Moreover, given this fundamental, frequency-dependent impedance characteristic of capacitors, the typical (picofarad) capacitor values selected for RF switches in Seshimo’s disclosed use cases, and the known solution—having “the

switch see[] an open circuit at the blocker frequencies”—to the well-known low frequency, “out-of-band blocker” signal problem in non-linear RF switches, which I discuss in State of the Art sections §VI.B.1-§VI.B.2 of my Declaration, in my opinion, POSITAs would understand Seshimo’s implementation of **capacitor C3** and **capacitor C2** as being high-pass filters “configured to inhibit a low-frequency blocker signal from mixing with a fundamental frequency signal in the RF switch.” *Id.*; State of the Art Section §VI.B.1 (EX-1012, 231-232, 175-176; EX-1027, 82-83, 50; EX-1014, 20, 30, 29-32, 36-37, 39-40, 42, FIGS. 1.52-1.55, 1.56(A); EX-1043, 128-129, 137-139, 236-238, FIGS. 5-17(A), 8-17(B), 8-17(D), 8-18(B), 8-18(D); EX-1011, 2615-2618, FIG. 9A; EX-1024, 3-4; EX-1026, [0049]; EX-1031, 8-9, FIG. 13; EX-1010, [0040], EX-1044, 1-2; EX-1029, 36-39; EX-1032, 1-2; EX-1033, 1; EX-1042, 96, 172, 180, 227, 275, 286; EX-1017, [0025]) of my Declaration; State of the Art Section §VI.B.2 (EX-1039, FIG. 5, 2-6, 8-12 (*citing* EX-1040, 3-6, FIGS. 3-4); EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1045, 1; EX-1049, p.3) of my Declaration.

168. Furthermore, to the extent that the Patent Owner asserts that Seshimo does not expressly disclose **capacitor C3** and/or **capacitor C2** as being configured as claimed, with the FIG. 3 SPDT switch components arranged as shown in Annotated FIG. 3 (*see* [1.1] above), and opposing series and shunt switches placed in ON and OFF states depending on the transmit or receive mode of FIG. 3 SPDT switch as

disclosed by Seshimo (*see* [1.5.1]-[1.61] above), POSITAs would understand these capacitors' inhibition of low-frequency blocker signals from mixing with fundamental frequency signals in FIG. 3 SPDT switch to merely be a matter of design choice. *Id.*

169. As I discussed in State of the Art sections §VI.B.1-§VI.B.2 of my Declaration, because capacitors C3 and C2 are fundamentally frequency-dependent circuit elements (with decreasing impedance with increasing frequency), in my opinion, POSITAs would understand that tuning the resulting high-pass filters, *i.e.*, setting the frequency range above which these capacitors permit frequencies (*e.g.* the desired RF frequency) to pass essentially unimpeded, and below which (*e.g.*, the “- 3dB breakpoint”) they impede lower frequencies (*e.g.*, low-frequency “out-of-band blocker” signals), is simply a matter of picking the size capacitor that yields the desired pass/inhibit thresholds within the practical size constraints for the RF device (*e.g.*, “PHS”) with a reasonable expectation of success. *Id.*; *see also* State of the Art Section §VI.B.1 of my Declaration (EX-1009, FIG. 2, [0083]-[0084]; EX-1035, 5; EX-1032, FIG. 1; EX-1026, FIG. 2, [0002], [0040], [0049], [0051], [0063]; EX-1042, 294, 298, 308, 312; EX-1049, p.3).

170. As I discussed in State of the Art sections §VI.B.1-§VI.B.2 of my Declaration, filtering RF_COM-picked-up, low-frequency, out-of-band-blocker

signals was a well-known problem in RF radios, with a well-known solution (*i.e.*, a series capacitor sized to yield the desired frequency-dependent response as a high-pass filter within the practical size constraints for the RF device). *Id.*; *see also* State of the Art section §VI.B.2 (EX-1039, FIG. 5, 2-6, 8-12 (*citing* EX-1040, 3-6, FIGS. 3-4); EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1045, 1; EX-1049, p.3) of my Declaration.

171. Accordingly, in my opinion, POSITAs would have been motivated to select appropriately-sized capacitors C3 and C2 to pass (with very low impedance) the high RF frequencies of interest (*e.g.*, 1.88-1.93GHz associated with PHS (*see* [1.0] above)), while impeding low, out-of-band frequencies, within the practical size constraints of such radios, to achieve the known and predictable benefits of improved switch performance (including improved IMD performance) with a reasonable expectation of success given that this involves nothing more than the conventional and routine use of Seshimo's capacitors. *Id.*; *see also* EX-1047, 1; EX-1048, 4, 9-11.

c. **Claim 3**

- i. ***[3.1] The switch system of claim 1 wherein the first shunt arm includes a third capacitor connected between the third switch circuit and the transmit node, and***

172. As I explained in my analysis of claim elements [1.5.1]-[1.5.2] (above), Seshimo discloses the **first shunt arm** of SPDT switch (FIG. 3) includes **capacitor C7** (*third capacitor*) *connected between MOSFET T4* (*third switch circuit*) and **high-frequency signal terminal RF_2** (*transmit node*) as illustrated in Annotated Figure 3 (see my analysis of claim element [1.1] (above)). EX-1007, [0055]-[0057]; see also my analysis of limitations [1.5.1]-[1.5.2] (above).

ii. [3.2] the second shunt arm includes a fourth capacitor connected between the fourth switch circuit and the receive node.

173. As I explained in my analysis of claim elements [1.6.1]-[1.6.2] (above), Seshimo discloses the **second shunt arm** of SPDT switch (FIG. 3) includes **capacitor C5** (*fourth capacitor*) *connected between MOSFET T3* (*fourth switch circuit*) and **high-frequency signal terminal RF_1** (*receive node*) as illustrated in Annotated Figure 3 (see my analysis of claim element [1.1] (above)). EX-1007 [0055]-[0057], see also my analysis of limitations [1.6.1]-[1.6.2] (above).

d. Claim 4

i. [4.0] A radio-frequency (RF) switch system comprising:

174. Seshimo discloses this limitation for the reasons that I discussed regarding claim element [1.0].

ii. [4.1] a first switch circuit connected between an antenna node and a transmit node;

175. Seshimo discloses this limitation for the reasons that I discussed regarding claim element [1.1].

iii. [4.2] a second switch circuit connected between the antenna node and a receive node;

176. Seshimo discloses this limitation for the reasons that I discussed regarding claim element [1.2].

iv. [4.3] a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node;

177. Seshimo discloses this limitation for the reasons that I discussed regarding [1.3].

v. [4.4] a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node;

178. Seshimo discloses this limitation for the reasons that I discussed regarding claim element [1.4].

vi. [4.5.1] a first shunt arm connected to the first switch circuit and the transmit node,

179. Seshimo discloses this limitation for the reasons that I discussed regarding claim element [1.5.1].

- vii. ***[4.5.2] the first shunt arm including a third switch circuit connected to ground and a third capacitor connected between the third switch circuit and the transmit node.***

180. Seshimo discloses this limitation for the reasons that I discussed regarding claim element [1.5.2], [3.1].

e. **Claim 5**

- i. ***[5.0] A method for fabricating a semiconductor die, the method comprising:***

181. To the extent the preamble is limiting, in my opinion, Seshimo discloses a method for fabricating a semiconductor die, including forming components of the disclosed “high-frequency semiconductor switching circuit” (*e.g.*, “SPDT switch” (FIG. 3)) on a semiconductor substrate of a semiconductor die to POSITAs.

182. Seshimo discloses “[t]he present invention... is particularly suitable for a high-frequency semiconductor switching circuit including a MOSFET formed on a silicon substrate”, “the use of SOI is also effective in the present invention”, that the SPDT components and control circuits all “may be configured as CMOS circuits and integrated on the same semiconductor substrate”, and identifies a well-known benefit of “develop[ing] high-frequency semiconductor switching circuits using CMOS processes”, namely “that a CMOS switch can be integrated into another CMOS RF IC.” EX-1007, [0001], [0003], [0007], [0054], [0084], [0088].

183. Accordingly, in my opinion, POSITAs would understand that Seshimo discloses providing a semiconductor substrate, and forming the SPDT switch components on the semiconductor substrate to fabricate a semiconductor die, where, in some embodiments, the semiconductor die is a SOI die in which the SPDT switch components would be formed on an insulator layer. EX-1007, [0001], [0003], [0007], [0054], [0084], [0088].

184. To the extent that Patent Owner asserts that Seshimo does not explicitly disclose forming SPDT switch components on the semiconductor substrate to fabricate a semiconductor die, in my opinion, it would have been obvious to POSITAs to do so, as this was the well-known and widely implemented approach to provide a stable foundation for fabrication of components of high power, semiconductor-based, transmit/receive switches, and in order to make manufacturing, testing and production of integrated circuits (including such switches and related circuits (*e.g.*, low noise amplifiers (LNAs)) easier and less costly. *Id.*; *See* State of the Art Section §VI.B.3 (EX-1018, 4:27-41; EX-1010, [0009], [0013], FIG. 3A, [0046]; EX-1019, [0001], [0004], FIG. 1; EX-1039, 9-10, FIG. 12; EX-1020, FIGS. 1, 4; EX-1009, [0004]-[0005], [0058], FIG. 2; EX-1022, FIG. 7, [0046]-[0050]; EX-1024, 1, 3-4, FIG. 8; EX-1029, FIGS. 1-2, 35-36, 40; EX-1028, 2-3, FIGS. 2, 4, 5; EX-1021, 2-3, FIGS. 1-2, 4-5; EX-1019, [0001], [0004], FIG. 1; EX-1011, 2613-2617, FIGS. 1-2, 4-6, 8).

ii. [5.1] providing a semiconductor substrate;

185. Seshimo discloses this limitation for the reasons that I discussed regarding claim element [1.0].

iii. [5.2] forming a first switch circuit on the semiconductor substrate so as to be connected between an antenna node and a transmit node;

186. Seshimo discloses this limitation for the reasons that I discussed regarding claim elements [1.1], [5.0]-[5.1].

iv. [5.3] forming a second switch circuit on the semiconductor substrate so as to be connected between the antenna node and a receive node;

187. Seshimo discloses this limitation for the reasons that I discussed regarding claim elements [1.2], [5.0]-[5.1].

v. [5.4] forming a first capacitor on the semiconductor substrate so as to be connected in series with the first switch circuit between the first switch circuit and the antenna node;

188. As I show in Annotated FIG. 3 (*see* my analysis of [1.3] above), Seshimo discloses a **capacitor C3**, that, (i) like the other capacitors (**C2, C5, C7**, etc.), may have a “MIM (metal-insulator-metal) structure” and is “integrated on the same semiconductor substrate” as the other SPDT components (*forming a first capacitor on the semiconductor substrate*), and (ii) is connected in series with **MOSFET T2** (*first switch circuit*) and between **MOSFET T2** (*first switch circuit*) and **common**

terminal RF_COM (antenna node). EX-1007, [0065]-[0071], FIG. 3; *see also* my analysis of limitations[1.3], [5.0] above

189. In my opinion, POSITAs understood that Seshimo discloses resistor Rd2 (and likewise Rd1 and the other resistors in the FIG. 3 circuit) are used for DC biasing only, such that the depicted Rd2 contact to the series path between MOSFET T2 and RF_COM via capacitor C3 is a “y-junction”, which, in my opinion, a POSITA understood does not alter the series connection between MOSFET T2 and capacitor C3. *Id.*; EX-1007, [0055]-[0056], [0059]-[0061].

190. To the extent Patent Owner asserts that Seshimo does not explicitly disclose forming “capacitor C3” (and, *e.g.*, “capacitor C2”, *see* [5.5] (below)) on the same semiconductor (*e.g.*, SOI) substrate of the same semiconductor die as the other components (*e.g.*, SOI FETs) of FIG. 3 SPDT switch, as I discussed in State of the Art sections §VI.B.1-§VI.B.3 of my Declaration, in my opinion, POSITAs would have been motivated to do so as a mere design choice to achieve known and predictable benefits, including making manufacturing, testing, and production of FIG. 3 SPDT switch (and integrated circuits (“ICs”) incorporating the same) easier and less costly, with a reasonable expectation of success, including because low capacitance value (*e.g.*, picofarad) capacitors are small in size and typically used in RF switches since, as was well-known to POSITAs, they would pass (with very low

impedance) the high RF frequencies of interest (*e.g.*, 1.88-1.93GHz associated with “PHS”) while impeding low, out-of-band blocker frequencies. *Id.*; *see also* State of the Art section §VI.B.3 of my Declaration (EX-1034, FIG. 2; EX-1035, 2-5; EX-1023, 10:13-17, FIG. 5; EX-1011, 2616-2617, FIG. 4; EX-1029, FIGS. 1-2, pp.35-36, 40; EX-1022, [0028], FIG. 7, [0046]-[0050]; EX-1010, [0009], [0013], FIG. 3A, [0046]) of my Declaration; State of the Art section §VI.B.1 (EX-1012, 231-234, 175-176; EX-1027, 82-83, 50; EX-1014, 29-32, 36-37, 42; EX-1043, 128-129, 137-139, 236-238; EX-1032, 1-2; EX-1033, 1; EX-1011, 2615-2618; EX-1026, [0049]; EX-1024, 3-4; EX-1031, 8-9; EX-1044, 1-2; EX-1010, [0040]; EX-1009, FIG. 2, [0083]-[0084], EX-1035, 5; EX-1042, 96, 172, 180, 227, 275, 286; EX-1029, 36-39; EX-1017, [0025]); State of the Art section §VI.B.2 (EX-1024, 1, 3-4; EX-1039, FIG. 5, 2-6, 9-12 (*citing* EX-1040, 3-6, FIGS. 3-4); EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1045, 1; EX-1049, p.3) of my Declaration; EX-1047, 1; EX-1048, 4, 9-11.

vi. [5.5] forming a second capacitor on the semiconductor substrate so as to be connected in series with the second switch circuit between the second switch circuit and the antenna node;

191. Seshimo discloses this limitation for the reasons that I discussed regarding claim elements [1.4], [5.0], [5.4].

vii. [5.6.1] forming a first shunt arm connected to the first switch circuit and the transmit node,

192. Seshimo discloses this limitation for the reasons that I discussed regarding claim elements [1.5.1].

viii. [5.6.2] the first shunt arm including a third switch circuit connected to ground; and

193. Seshimo discloses this limitation for the reasons that I discussed regarding claim elements [1.5.1]-[1.5.2].

ix. [5.7.1] forming a second shunt arm connected to the second switch circuit and the receive node,

194. Seshimo discloses this limitation for the reasons that I discussed regarding claim element [1.6.1].

x. [5.7.2] the second shunt arm including a fourth switch circuit connected to ground.

195. Seshimo discloses this limitation for the reasons that I discussed regarding claim elements [1.6.1]-[1.6.2].

f. Claim 6

i. The method of claim 5 further comprising forming an insulator layer between the first switch circuit and the semiconductor substrate.

196. As I explained in my analysis of claim element [5.0] (above), Seshimo discloses “[t]he present invention... is particularly suitable for a high-frequency

semiconductor switching circuit including a MOSFET formed on a silicon substrate”, because “CMOS switch[es] formed using a SOI... substrate generally [have] excellent high frequency properties,... the use of SOI is also effective in the present invention”, that the SPDT components and control circuits all “may be configured as CMOS circuits and integrated on the same semiconductor substrate”, and identifies a well-known benefit of “develop[ing] high-frequency semiconductor switching circuits using CMOS processes”, namely “that a CMOS switch can be integrated into another CMOS RF IC.” EX-1007, [0001], [0003], [0007], [0054], [0084], [0088].

197. Unsurprisingly, Seshimo does not disclose the well-known details of implementing SOI technology to manufacture the “CMOS switch[es] formed using a SOI... substrate” of the “high-frequency semiconductor switching circuit”, such as SPDT switch (FIG. 3). EX-1007, [0001], [0003], [0007], [0054], [0084], [0088]. Indeed, as I discuss in State of the Art section §VI.B.3 of my Declaration, it was well-known that, in using SOI technology to create integrated circuits (“ICs”), an insulator layer is deposited onto a semiconductor substrate of a semiconductor die, silicon is grown on top of this insulator layer, and then the silicon is patterned and etched to create the various components of the IC (*e.g.*, MOSFETs, capacitors, etc. of SPDT switch (FIG. 3)). *Id.*; see State of the Art section §VI.B.3 (EX-1020, FIGS. 1, 4, 8:17-25, 7:12, 7:17-18, 10:5-11, 8:28-29, 1:10-14, 12:27-31, FIG. 16; EX-1026,

[0030]; EX-1018, 4:27-41, 3:50-54, FIGS. 3-4, EX-1039, 9-10, FIG. 10) of my Declaration.

198. Accordingly, in my opinion, POSITAs understood that Seshimo's implementation of SOI included forming an insulator layer between the SOI MOSFET T2 (*first switch circuit*) and the semiconductor substrate. *Id.*; EX-1007, [0001], [0003], [0007], [0054], [0084], [0088].

199. To the extent that the Patent Owner asserts that Seshimo does not expressly disclose an insulator layer disposed between MOSFET T2 (*first switch circuit*) and the semiconductor substrate, in my opinion, it would have been obvious to POSITAs to do so as this was the well-known and widely implemented approach to using the disclosed SOI technology to manufacture "CMOS switch[es] formed using a SOI... substrate" of the "high-frequency semiconductor switching circuit", such as SPDT switch (FIG. 3), with well-known and predictable benefits including, for example, lower cost, higher "thermal conductivity", reduced "degradation in bandwidth associated with the stacking of FET devices", "reduce[d] dielectric losses associated with the silicon substrate", allowing monolithic (same die/chip) integration of SPnT switch and control components and other front-end module (FEM) components, etc. *Id.*; see State of the Art Section §VI.B.3 (EX-1009, [0005];

EX-1018, 4:37-41; EX-1026, [0030]; EX-1021, 2; EX-1009, [0005]; EX-1010, [0013]).

g. Claim 7

i. [7.0] A radio-frequency (RF) switch module comprising:

200. To the extent the preamble is limiting, as I discussed in my analysis of claim elements [1.0]-[1.1] and [5.0], in my opinion, Seshimo discloses to POSITAs incorporation of a “high-frequency semiconductor switching circuit” (e.g., FIG. 3 SPDT switch) into an RF/wireless device (e.g., “PHS (Personal Handyphone System)”), in which such switch would (i) be “used as a transmission/reception changeover switch”, (ii) include **high-frequency signal terminal RF_2** (*transmit node*), **high-frequency signal terminal RF_1** (*receive node*), and **common terminal RF_COM** (*antenna*), (iii) have its SPDT components and control circuits all “configured as CMOS circuits and integrated on the same semiconductor substrate”, and (iv) be “developed... using CMOS processes” so that the “CMOS switch can be integrated into another CMOS RF IC.” EX-1007, [0029], [0070]-[0071], [0003], [0005], [0007], [0084], [0087]-[0088]. In my opinion, POSITAs understood Seshimo’s disclosure of FIG. 3 SPDT switch, formed for use as a component incorporated into (e.g., in a packaged RF switch module, FEM, etc.) RF/wireless devices (e.g., “PHS”), to constitute an *RF switch module*. *Id.*

201. Unsurprisingly, Seshimo does not disclose the well-known details of packaging the components of SPDT switch (FIG. 3) for testing, shipment, commercial sale, etc., for such use in such RF/wireless devices. *Id.* Indeed, as I discussed in State of the Art section §VI.B.3 of my Declaration,, given that the well-known, and widely implemented approach to package a semiconductor die (or plurality of dies) for testing, shipment, commercial sale, etc. of a SPnT switch, and of any other components that are incorporated into the packaged module (*e.g.*, external capacitors, control circuitry, LNA, etc.)), was to mount each separate die (and/or surface mountable component) on, and electrically connect (*e.g.*, wire-bond) each separate die and/or surface mountable component) to, a packaging substrate (*e.g.*, printed circuit board (PCB)), in my opinion, POSITAs would have been motivated to do so as a mere design choice with a high likelihood of success of achieving well-known benefits, such as making packaging, testing, production, shipment, and commercial sales of packaged products (*e.g.*, RF switch module, FEM, etc.) easier, less costly, and more attractive to customers. *Id.*; *see* State of the Art Section §VI.B.3 (EX-1008, 1-3; EX-1041, 2; EX-1029, 36-39, Figures 4, 8; EX-1033, 1; EX-1028, 1, 4, Fig. 2; EX-1038, [0010], [0027], [0029], [0030]-[0032], [0036]-[0037], [0045], FIGS. 2-3; EX-1042, 80-82 (WLAN 802.11b, g, n Intera™ Front-End Module Single Antenna); 95-97 (WLAN 802.11b, g, n Intera™ Front-End Module); 105-106 (WLAN 802.11a, b, g, n Dual-Band, Front-End Module

Single Antenna); 171-172 (GaAs SPDT Switch 100 MHz–2.5 GHz); 180-181 (GaAs IC High-Isolation Positive Control SPDT Switch 300 kHz–3 GHz); 192-193 (GaAs SPDT Switch 300 kHz–3 GHz Medium Power); 210 (PHEMT GaAs IC SPDT Switch LF–4 GHz); 221-222 (GaAs SPDT 7 W Switch 100 MHz–4 GHz); 226-227 (GaAs IC High-Isolation SPDT Nonreflective Switch with Driver LF–6 GHz); 237-238 (PHEMT SP2T Switch 0.5–6.0 GHz); 242 (PHEMT GaAs IC 1 W Low Loss 0.1–6 GHz SPDT Switch); 274-275 (GaAs T/R Diversity Switch LF–6 GHz); 285-286 (GaAs SP3T Absorptive Switch 500 MHz–2.5 GHz); 298-299 (PHEMT GaAs IC High-Power SP4T Switch 0.1–2.5 GHz); 312-313 (PHEMT GaAs IC SP3T Switch 0.1–3.0 GHz); EX-1021, 1-3; EX-1031, 1, 3, 9-11; EX-1032, 1-2; EX-1022, [0028]) of my Declaration.

ii. [7.1] a packaging substrate configured to receive a plurality of components;

202. POSITAs reading Seshimo would have been motivated to implement this limitation as I discussed in claim elements [1.0]-[1.1], [5.0], [7.0].

iii. [7.2] a semiconductor die mounted on the packaging substrate,

203. Seshimo discloses this limitation for the reasons that I discussed regarding claim elements [5.0], [7.0].

- iv. ***[7.3.1] the die including a first switch circuit connected between an antenna node and a transmit node and***

204. Seshimo discloses this limitation for the reasons that I discussed regarding claim elements [1.1], [5.0], [7.0].

- v. ***[7.3.2] a second switch circuit connected between the antenna node and a receive node;***

205. Seshimo discloses this limitation for the reasons that I discussed regarding claim elements [1.2], [5.0], [7.0].

- vi. ***[7.4] a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node;***

206. Seshimo discloses this limitation for the reasons that I discussed regarding claim element [1.3].

- vii. ***[7.5] a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node;***

207. Seshimo discloses this limitation for the reasons that I discussed regarding claim element [1.4].

- viii. ***[7.6.1] a first shunt arm connected to the first switch circuit and the transmit node,***

208. Seshimo discloses this limitation for the reasons that I discussed regarding claim element [1.5.1].

- ix. ***[7.6.2] the first shunt arm including a third switch circuit connected to ground; and***

209. Seshimo discloses this limitation for the reasons that I discussed regarding claim elements [1.5.1]-[1.5.2].

- x. ***[7.7.1] a second shunt arm connected to the second switch circuit and the receive node,***

210. Seshimo discloses this limitation for the reasons that I discussed regarding claim element [1.6.1].

- xi. ***[7.7.2] the second shunt arm including a fourth switch circuit connected to ground.***

211. Seshimo discloses this limitation for the reasons that I discussed regarding claim elements [1.6.1]-[1.6.2].

h. Claim 8

- i. ***The switch module of claim 7 wherein at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.***

212. Seshimo discloses this limitation for the reasons that I discussed regarding Claim 2.

i. Claim 9

- i. ***The switch module of claim 7 wherein the first capacitor is part of the same semiconductor die as the first switch circuit.***

213. Seshimo discloses this limitation for the reasons that I discussed regarding claim elements [7.0], [5.4].

j. **Claim 10**

i. ***The switch module of claim 7 wherein the first capacitor is part of a second die mounted on the packaging substrate.***

214. As the '194 Patent itself acknowledges, and as I discussed in my analysis of claim elements [7.0], [5.0], and [5.4] (above) and in State of the Art sections §VI.B.3, §VI.B.1 of my Declaration, POSITAs understood this limitation to be obvious as a mere (and well-known) design choice—selecting between forming Seshimo's capacitor C3 (and the other capacitors) on the same die as the MOSFETs, or on a separate capacitor die (*second capacitor die mounted on the packaging substrate*), or mounting them as surface mountable components on the same packaging substrate on which the MOSFET-die is mounted (claim 11)—based on, for example, size/space constraints, the RF application, the fundamental frequency values, and blocking frequency values, associated with such application, performance requirements, etc., and with well-known benefits and tradeoffs. *See* [7.0], [5.0], [5.4], EX-1007, [0054]-[0056], Annotated FIG. 3, [0001], [0003], [0005], [0007], [0029], [0070]-[0071], [0084]-[0087]; *see* State of the Art Section §VI.B.3 (EX-1035, 2-5; EX-1034, FIG. 2; EX-1032, 1-2; EX-1033, 1; EX-1023, 10:13-17, 8:29-37, 5:59-6:21, FIG. 5; EX-1011, 2616-2617, FIGS. 4, 8; EX-1029,

35-36, 40, Figures 1-2) of my Declaration; State of the Art Section §VI.B.1 (EX-1014, 36-37; EX-1043, 137-139; EX-1026, [0049], [0063]; EX-1011, 2615-2618; EX-1009, FIG. 2, [0083]-[0084]; EX-1024, 3; EX-1031, 8-9, EX-1032, FIG. 1; EX-1042, 96 (WLAN 802.11b, g, n Intera™ Front-End Module), 172 (GaAs SPDT Switch 100 MHz–2.5 GHz), 180 (PHEMT 10 W SPDT Switch 500 MHz–2.5 GHz), 227 (GaAs IC High-Isolation SPDT Nonreflective Switch with Driver LF–6 GHz), 275 (GaAs T/R Diversity Switch LF–6 GHz), 286 (GaAs SP3T Absorptive Switch 500 MHz–2.5 GHz), 298 (GaAs SP4T Absorptive Switch 20 MHz–2.5 GHz), 312 (PHEMT GaAs IC SP3T Switch 0.1–3.0 GHz) of my Declaration; *see also* Overview of the '194 Patent section §IV.A (EX-1001, 9:45-49, 2:15-21, 9:62-10:11, FIGS. 11A-11D) of my Declaration.

k. Claim 11

- i. The switch module of claim 7 wherein the first capacitor is disposed at a location outside of the semiconductor die.*

215. Seshimo discloses this limitation for the reasons that I discussed regarding Claim 10.

CONCLUSION AND DECLARATION

My findings and opinions set forth in this Declaration are based on my work and examination to date. I may continue my examinations in view of additional

documents or other factual evidence over the course of this proceeding that may necessitate supplementing and/or refining my opinions. I reserve the right to add to, alter, or delete my opinions and my Declaration upon discovery of additional information. I reserve the right to make such changes as necessary.

In signing this Declaration, I understand that the Declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed at

By:

A handwritten signature in black ink, appearing to be 'L. E. Larson', written over a horizontal line.

Lawrence E. Larson, Ph.D.

APPENDIX A – MATERIALS RELIED UPON

<i>Exhibit #</i>	<i>Description</i>
EX-1001	U.S. Patent No. 9,148,194 to Madan et al. (“194 Patent”), filing date of July 6, 2013, and claiming priority to U.S. Provisional Patent App. No. 61/669,045 filed on July 7, 2012.
EX-1002	Prosecution History of U.S. Patent No. 9,148,194.
EX-1005	U.S. Patent Publication No. 2011/0254614 A1 to C-W Huang, et al., Filing Date of April 16, 2010 and Publication Date of October 20, 2011 (“Huang”).
EX-1006	Japanese Patent Publication No. JP 2006-121217 to Seshimo, Toshiko et al., Publication Date of May 11, 2006 (“Seshimo”).
EX-1007	Certified English Translation of Japanese Patent Publication No. JP 2006-121217 (EX-1006).
EX-1008	“General Purpose RF Switches”, Skyworks Solutions., Inc., archived at Internet Archive’s Wayback Machine on January 6, 2011 at https://web.archive.org/web/20110106070051/http://www.skyworksi nc.com/uploads/documents/BR0378_10B.pdf .
EX-1009	U.S. Patent Pub. No. 2012/0081262 to Tanaka, et al. filed July 12, 2011 and published April 5, 2012.
EX-1010	U.S. Patent Pub. No. 2010/0327948 to Nisbet, et al., filed June 29, 2009 and published December 30, 2010.
EX-1011	Madan, et al., “Fully Integrated Switch-LNA Front-End IC Design in CMOS: A Systematic Approach for WLAN”, IEEE Journal of Solid State Circuits, Vol. 46, No. 11, November 2011 (also available, and identified as published in October 2011, on Skyworks’ web page archived on November 4, 2011 at Internet Archive’s Wayback Machine at https://web.archive.org/web/20111104120653/http://www.skyworksi nc.com/Press_Published_Articles.aspx).
EX-1012	Excerpts from V. Veley, “The Benchtop Electronics Reference Manual,” Tab Books Inc., 1987.

EX-1013	U.S. Patent Pub. No. 2004/0251952 to Nakatsuka et al. filed June 10, 2004 and published December 16, 2004.
EX-1014	Excerpts from Paul Horowitz, et al., “The Art of Electronics” (2d ed. 1989).
EX-1015	Japanese Patent Publication No. JP2011-166663A to Takashi et al., published August 24, 2011.
EX-1016	English Machine Translation of Japanese Patent Publication No. JP2011-166663A (EX-1015).
EX-1017	U.S. Patent Publication No. 2013/0154761 to Ilkov, filed December 14, 2011, and published June 20, 2013.
EX-1018	U.S. Patent No. 6,698,082 to Crenshaw, et al., filed August 28, 2001 and issued on March 2, 2004.
EX-1019	EP Pat. No. 2348532 to Brindle, et al., filed July 11, 2006 and published July 27, 2011.
EX-1020	International Patent Publication WO 2011/045442 to Heaney, et al., filed on October 18, 2010 with a priority claim to October 16, 2009, and published April 21, 2011.
EX-1021	C-W Huang, et al., “Highly Linear SOI Single-Pole, 4-Throw Switch with an Integrated Dual-band LNA and Bypass Attenuators”, SiGe Semiconductor, 2010 IEEE Radio Frequency Integrated Circuits Symposium, May 23-25, 2010.
EX-1022	U.S. Patent Pub. No. 2011/0294443 to Nohra, et al., filed May 26, 2010 and published December 1, 2011.
EX-1023	U.S. Patent No. 7,359,677 to C-W Huang, et al., filed June 10, 2005 and published April 15, 2008.
EX-1024	Rick Cory, et al., “Solid State RF/Microwave Switch Technology: Part 2”, June 2009, Skyworks Solutions, Inc., www.mpdigest.com , archived at Internet Archive’s Wayback Machine at https://web.archive.org/web/20090906040150/http://www.skyworksinc.com/Press_Published_Articles.aspx .
EX-1025	U.S. Patent No. 7,088,971 to Burgener, et al., filed June 22, 2005 and issued August 8, 2006.
EX-1026	U.S. Patent Pub. No. 2011/0260773 to Granger-Jones et al., filed

	April 27, 2011 with priority claim to April 27, 2010, and published October 27, 2011 (“Granger-Jones”).
EX-1027	Excerpts from R. Boylestead, et al., “Electricity, Electronics and Electromagnetics Principles and Applications,” Prentice-Hall, Inc., 1977.
EX-1028	C-W Huang, et al., “Highly Linear 4.9-5.9 GHz WLAN Front-End Module Based on SiGe BiCMOS and SOI”, 2011 IEEE MTT-S International Microwave Symposium, Baltimore, MD, USA, August 4, 2011, pp. 1-4.
EX-1029	F-J Huang, et al., “Single-Pole Double-Throw CMOS Switches for 900-MHz and 2.4-GHz Applications on p Silicon Substrates”, IEEE Journal of Solid-State Circuits, Vol. 39, No. 1, January 2004.
EX-1030	U.S. Patent No. 7,265,604 to Yasuda et al., filed November 23, 2005 with priority claim to November 26, 2004, and issued September 4, 2007 (“Yasuda”).
EX-1031	Skyworks Solutions, Inc., “SKY14151-350LF High-Power Single Pole Four Throw (SP4T) Switch with Decoder”, Data Sheet, October 6, 2010, archived at Internet Archive’s Wayback Machine at https://web.archive.org/web/20110106074932/http://www.skyworksinc.com/uploads/documents/200983H.pdf .
EX-1032	Skyworks Solutions, Inc., “SC Series: MIS Chip Capacitors”, Data Sheet, November 1, 2005, archived at Internet Archive’s Wayback Machine at https://web.archive.org/web/20060322024053/http://www.skyworksinc.com/products_display_item.asp?did=742&filename=/200136B.pdf .
EX-1033	Skyworks Solutions, Inc., “AS191-73, AS191-73LF: PHEMT GaAs IC High-Linearity 3 V Control SPDT Switch 0.1–4 GHz”, Data Sheet, August 2, 2006, archived at Internet Archive’s Wayback Machine on June 2, 2010 at https://web.archive.org/web/20100602013954/http://www.skyworksinc.com/uploads/documents/200185B.pdf .
EX-1034	Korean Patent Publication No. KR100967847B1, filed on March 31, 2008, published on July 5, 2010

EX-1035	English Machine Translation of Korean Patent Publication No. KR100967847B1 (EX-1034).
EX-1036	J. Oerth, et al., “Evaluating pHEMT Process Improvements Using Wafer Level RF Tests”, Skyworks Solutions, Inc., identified as published in May 2010 at the “GaAs Mantech 2010 Conference” at https://web.archive.org/web/20110104205915/http://www.skyworksinc.com/Press_Published_Articles.aspx , archived at Internet Archive’s Wayback Machine on January 5, 2011 at https://web.archive.org/web/20110105002236/http://www.skyworksinc.com/downloads/press_room/published_articles/GaAs_Mantech_052010_4.pdf .
EX-1037	Prosecution History of U.S. Patent No. 9,450,579.
EX-1038	U.S. Patent Pub. No. 2010/0123215 to Pan et al., filed November 18, 2009, with priority claim to November 20, 2008, and published May 20, 2010 (“Pan”).
EX-1039	“Choosing the Right RF Switches for Smart Mobile Device Applications” White Paper, Skyworks Solutions, Inc., May 9, 2011, accessible as archived at Internet Archive’s Wayback Machine on June 12, 2011 at https://web.archive.org/web/20110612215106/http://www.skyworksinc.com/TechnicalDocuments.aspx?DocTypeID=16 ; on December 29, 2011 at https://web.archive.org/web/20111229234636/http://www.everythingrf.com/Profiles/7_Skyworks ; on July 26, 2011 at https://web.archive.org/web/20110726081257/http://www.mwjournals.com/BuyersGuide/ ; on December 16, 2011 at https://web.archive.org/web/20111216112526/https://www.rfcafe.com/references/magazine-articles/magazine-articles-2011.htm ; on December 4, 2011 at https://web.archive.org/web/20111204155405/http://www.mpdigest.com/
EX-1040	T. Ranta et al., “Antenna Switch Linearity Requirements for GSM/WCDMA Mobile Phone Front-Ends,” presented at “The European Conference on Wireless Technology” in Paris, France, October 3-4, 2005, published in 2005 Wireless Technology Conference Proceedings, Horizon House Publications Ltd., pp. 23-

	36, 2005; <i>cited in</i> EX-1039, 5-6, 12.
EX-1041	S. Bellette, “Top Considerations When Buying or Specifying an RF Switch”, Skyworks Solutions, Inc., July/August 2009, wirelessdesignmag.com, archived at Internet Archive’s Wayback Machine on January 5, 2011 at https://web.archive.org/web/20110105004915/http://www.skyworksinc.com/downloads/press_room/published_articles/WDD_082009.pdf , and as linked from the web page archived at Internet Archive’s Wayback Machine on January 4, 2011 at https://web.archive.org/web/20110104205915/http://www.skyworksinc.com/Press_Published_Articles.aspx .
EX-1042	Excerpts of “Linear Products 2008”, Skyworks Solutions, Inc., Fall 2008, archived at Internet Archive’s Wayback Machine on June 28, 2011 at https://web.archive.org/web/20110628193600/http://www.skyworksinc.com/downloads/literature/LinearProductsCatalog.zip , and as linked from the web page archived at Internet Archive’s Wayback Machine on May 9, 2011 at https://web.archive.org/web/20110509050519/http://www.skyworksinc.com/ProductLiterature.aspx .
EX-1043	Excerpts of M. Horowitz, “Elementary Electricity and Electronics”, TAB BOOKS Inc., 1986.
EX-1044	G. Breed, “There’s Nothing Magic About 50 Ohms”, High Frequency Electronics magazine, Summit Technical Media, LLC, June 2007, archived at Internet Archive’s Wayback Machine on August 24, 2009 at https://web.archive.org/web/20090824090425/http://www.highfrequencyelectronics.com/Archives/Jun07/HFE0607_Editorial.pdf .
EX-1045	“United States Frequency Allocations – The Radio Spectrum”, National Telecommunications and Information Administration Office of Spectrum Management, October 2003, archived at Internet Archive’s Wayback Machine on June 1, 2004 at https://web.archive.org/web/20040601230908/http://www.ntia.doc.gov/osmhome/allochrt.pdf .
EX-1046	P. J. Mole, “Integration of RF Systems on a Chip”, Chapter 3 of “Circuits and Systems for Wireless Communications”, Helfenstein,

	M., Moschytz, G.S. (eds), Springer, Boston, MA, 2002.
EX-1047	“Personal Handy-phone System”, Wikipedia, archived at Internet Archive’s Wayback Machine on November 25, 2007 at https://web.archive.org/web/20071125082123/https://en.wikipedia.org/wiki/Personal_Handy-phone_System .
EX-1048	“Extension of Frequency Band Allocations for Personal Handy-phone systems (PHS),” PHS MoU Document A-GN3.00-01-TS, Version 1, (April 20, 1999), archived at Internet Archive’s Wayback Machine on December 7, 2003 at https://web.archive.org/web/20031207100524/http://www.phsmou.or.jp/documents/pdf/A-GN3.00-01-TS.pdf , and as linked from the web page archived at Internet Archive’s Wayback Machine on March 11, 2003 at https://web.archive.org/web/20030311143954/http://www.phsmou.or.jp/documents/ and as further linked from the web page archived at Internet Archive’s Wayback Machine on April 8, 2003 at https://web.archive.org/web/20030408234423/http://www.phsmou.or.jp/documents/TECH_June2000.html
EX-1049	Skyworks Solutions, Inc., “SKY13399-468LF: 0.7 – 2.7 GHz DPx3T Switch”, Data Sheet, accessible through Internet Archive’s Wayback Machine link archived on August 14, 2011 at https://web.archive.org/web/20111007155745/http://www.skyworksinc.com/Products_Documents.aspx and also accessible through Internet Archive’s Wayback Machine link archived on August 29, 2011 at https://web.archive.org/web/20110829193217/www.skyworksinc.com/categories.aspx?CategoryID=495