IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KANGXI COMMUNICATION TECHNOLOGIES (SHANGHAI) CO., LTD.
Petitioner,

v.

SKYWORKS SOLUTIONS, INC.,
Patent Owner.

U.S. Patent No. 9,148,194
Issue Date: SEPTEMBER 29, 2015

Title: RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION

Inter Partes Review No.: IPR2024-01457

PETITION FOR *INTER PARTES* REVIEW OF PATENT NO. 9,148,194 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. §§ 42.1-.80, 42.100-.107

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i. [1.0] A radio-frequency (RF) switch system comprising: 33

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iii. [1.2] a second switch circuit connected between the antenna node and a receive node; 34

iv. [1.3] a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node; 35

v. [1.4] a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node; 35

vi. [1.5.1] a first shunt arm connected to the first switch circuit and the transmit node, [1.5.2] the first shunt arm including a third switch circuit connected to ground; . 35

vii. [1.6.1] and a second shunt arm connected to the second switch circuit and the receive node, [1.6.2] the second

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b. Claim 2 37

i. The switch system of claim 1 wherein at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch. 37

c. Claim 3 41

i. [3.1] The switch system of claim 1 wherein the first shunt arm includes a third capacitor connected between the third switch circuit and the transmit node, and 41

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h. Claim 8.....50

i. The switch module of claim 7 wherein at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch. 50

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i. The switch module of claim 7 wherein the first capacitor is part of the same semiconductor die as the first switch circuit.....50

j. Claim 10.....50

i. The switch module of claim 7 wherein the first capacitor is part of a second die mounted on the packaging substrate. 50

k. Claim 11 51

i. The switch module of claim 7 wherein the first capacitor is disposed at a location outside of the semiconductor die. 51

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i. [1.0] A radio-frequency (RF) switch system comprising: 54

ii. [1.1] a first switch circuit connected between an antenna node and a transmit node; 55

iii. [1.2] a second switch circuit connected between the antenna node and a receive node; 56

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vi. [1.5.1] a first shunt arm connected to the first switch circuit and the transmit node, [1.5.2] the first shunt arm including a third switch circuit connected to ground; . 57

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b. Claim 2.....59

i. The switch system of claim 1 wherein at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch. 59

c. Claim 3.....63

i. [3.1] The switch system of claim 1 wherein the first shunt arm includes a third capacitor connected between the third switch circuit and the transmit node, and.....63

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d. Claim 4.....64

i. [4.0] A radio-frequency (RF) switch system comprising: [4.1] a first switch circuit connected between an antenna node and a transmit node; [4.2] a second switch circuit connected between the antenna node and a receive node; [4.3] a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node; [4.4] a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node; [4.5.1] a first shunt arm connected to the first switch circuit and the transmit node, [4.5.2] the first shunt arm including a third switch circuit connected to ground and a third capacitor connected between the third switch circuit and the transmit node.....64

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i. [5.4] forming a first capacitor on the semiconductor substrate so as to be connected in series with the first switch circuit between the first switch circuit and the antenna node; 66

ii. [5.5] forming a second capacitor on the semiconductor substrate so as to be connected in series with the second switch circuit between the second switch circuit and the antenna node; 67

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f. Claim 6 68

i. The method of claim 5 further comprising forming an insulator layer between the first switch circuit and the semiconductor substrate. 68

g. Claim 7 70

i. [7.0] A radio-frequency (RF) switch module comprising: 70

ii. [7.1] a packaging substrate configured to receive a plurality of components; 71

iii. [7.2] a semiconductor die mounted on the packaging

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iv. [7.3.1] the die including a first switch circuit connected between an antenna node and a transmit node and [7.3.2] a second switch circuit connected between the antenna node and a receive node; 72

v. [7.4] a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node; [7.5] a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node; [7.6.1] a first shunt arm connected to the first switch circuit and the transmit node, [7.6.2] the first shunt arm including a third switch circuit connected to ground; and [7.7.1] a second shunt arm connected to the second switch circuit and the receive node, [7.7.2] the second shunt arm including a fourth switch circuit connected to ground.72

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PETITIONER'S EXHIBIT LIST

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EX-1002	Prosecution History of U.S. Patent No. 9,148,194.
EX-1003	Declaration of Dr. Larry Larson under 37 C.F.R. § 1.68.
EX-1004	*Curriculum Vitae* of Larry Larson.
EX-1005	U.S. Patent Publication No. 2011/0254614 A1 to C-W Huang, et al., Filing Date of April 16, 2010 and Publication Date of October 20, 2011 ("Huang").
EX-1006	Japanese Patent Publication No. JP 2006-121217 to Seshimo, Toshiko et al., Publication Date of May 11, 2006 ("Seshimo")
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EX-1008	"General Purpose RF Switches", Skyworks Solutions., Inc., archived at Internet Archive's Wayback Machine on January 6, 2011 at https://web.archive.org/web/20110106070051/http//www.skyworksinc.com/uploads/documents/BR0378_10B.pdf.
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EX-1011	Madan, et al., "Fully Integrated Switch-LNA Front-End IC Design in CMOS: A Systematic Approach for WLAN", IEEE Journal of Solid State Circuits, Vol. 46, No. 11, November 2011 (also available, and identified as published in October 2011, on Skyworks' web page archived on November 4, 2011 at Internet Archive's Wayback Machine at https://web.archive.org/web/20111104120653/http:/www.skyworksinc.com/Press_Published_Articles.aspx.)

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EX-1017	U.S. Patent Publication No. 2013/0154761 to Ilkov, filed December 14, 2011, and published June 20, 2013.
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EX-1019	EP Pat. No. 2348532 to Brindle, et al., filed July 11, 2006 and published July 27, 2011.
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EX-1024	Rick Cory, et al., "Solid State RF/Microwave Switch Technology: Part 2", June 2009, Skyworks Solutions, Inc., www.mpdigest.com, archived at Internet Archive's Wayback Machine at https://web.archive.org/web/20090906040150/http://www.skyworksinc.com/Press_Published_Articles.aspx.
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EX-1037	Prosecution History of U.S. Patent No. 9,450,579.
EX-1038	U.S. Patent Pub. No. 2010/0123215 to Pan et al., filed November 18, 2009, with priority claim to November 20, 2008, and published May 20, 2010 ("Pan").
EX-1039	"Choosing the Right RF Switches for Smart Mobile Device Applications" White Paper, Skyworks Solutions, Inc., May 9, 2011, accessible as archived at Internet Archive's Wayback Machine on June 12, 2011 at https://web.archive.org/web/20110612215106/http://www.skyworksinc.com/TechnicalDocuments.aspx?DocTypeID=16; on December 29, 2011 at https://web.archive.org/web/20111229234636/http://www.everythingrf.com/Profiles/7_Skyworks; on July 26, 2011 at https://web.archive.org/web/20110726081257/http://www.mwjournal.com/BuyersGuide/; on December 16, 2011 at https://web.archive.org/web/20111216112526/https://www.rfcafe.com/references/magazine-articles/magazine-articles-2011.htm; on December 4, 2011 at https://web.archive.org/web/20111204155405/http://www.mpdigest.com/.
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EX-1041	S. Bellette, "Top Considerations When Buying or Specifying an RF Switch", Skyworks Solutions, Inc., July/August 2009, wirelessdesignmag.com, archived at Internet Archive's Wayback Machine on January 5, 2011 at https://web.archive.org/web/20110105004915/http://www.skyworksinc.com/downloads/press_room/published_articles/WDD_082009.pdf, and as linked from the web page archived at Internet Archive's Wayback Machine on January 4, 2011 at https://web.archive.org/web/20110104205915/http://www.skyworksinc.com/Press_Published_Articles.aspx.
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I. INTRODUCTION

Pursuant to 35 U.S.C. §§311 *et seq*. and 37 C.F.R. §§42.1 *et seq*., Kangxi Communications Technologies (Shanghai) Co., Ltd. ("Petitioner") petitions for *inter partes* review ("IPR") of Patent No. 9,148,194 (the "'194 Patent") (EX-1001). Petitioner submits that '194 Patent claims 1-11 (the "Challenged Claims") are unpatentable under (pre-AIA) 35 U.S.C. §103(a) in view of the prior art discussed herein. This Petition demonstrates by a preponderance of the evidence that there is a reasonable likelihood that Petitioner will prevail with respect to at least one of the Challenged Claims. Accordingly, Petitioner requests that the Board institute the '194 Patent IPR pursuant to 37 C.F.R. §42.108.

II. OVERVIEW

The '194 Patent is directed to RF switches that can be used to "switch" signals between one or more "poles" (antenna) and one or more "throws" (transmit or receive circuits). During operation, at any given point in time, the "pole" may be used to transmit, or receive, a desired RF signal, where the transmit signal frequency may be different than the receive signal frequency. Accordingly, the RF switch is used to "switch" the "throw" that is communicatively/electrically connected to the "pole" based on the desired operating mode (transmit/receive). For example, if "transmitting" is desired, the path between the transmit "throw" and antenna is "switched" to a closed ("ON") state, while the path between the receive "throw" and antenna is "switched" to

an open ("OFF") state.

The Patent is directed to a well-known problem in designing RF switches in wireless devices, especially those operating in a "multi-band and/or multi-mode environment", namely "the susceptibility of a [RF switch] system to interference" from unwanted signals. For example, when an unwanted signal (*e.g.*, "blocker" signals) mixes with a desired signal in an RF switch, the desired transmitted/received information may be degraded, and further unwanted signals may be created. These created unwanted signals may be at frequencies that are multiples of a desired signal frequency (f_1) (*e.g.*, $2f_1$, $3f_1$, etc.) called "harmonic frequencies", or at non-harmonic frequencies (*e.g.*, f_1+/-$f_{blocker}$, $2f_1$+/-$f_{blocker}$, etc.) called "intermodulation distortion (IMD)" products.

The Patent's disclosed solution to this "interference susceptibility" problem involved (i) including a "shunt arm" in each RF switch "throw", and (ii) positioning capacitors in each arm of each RF switch throw. Specifically, the Patent states that the particular arrangement of RF switch components depicted in Figure 9 (annotated below) provides this solution:

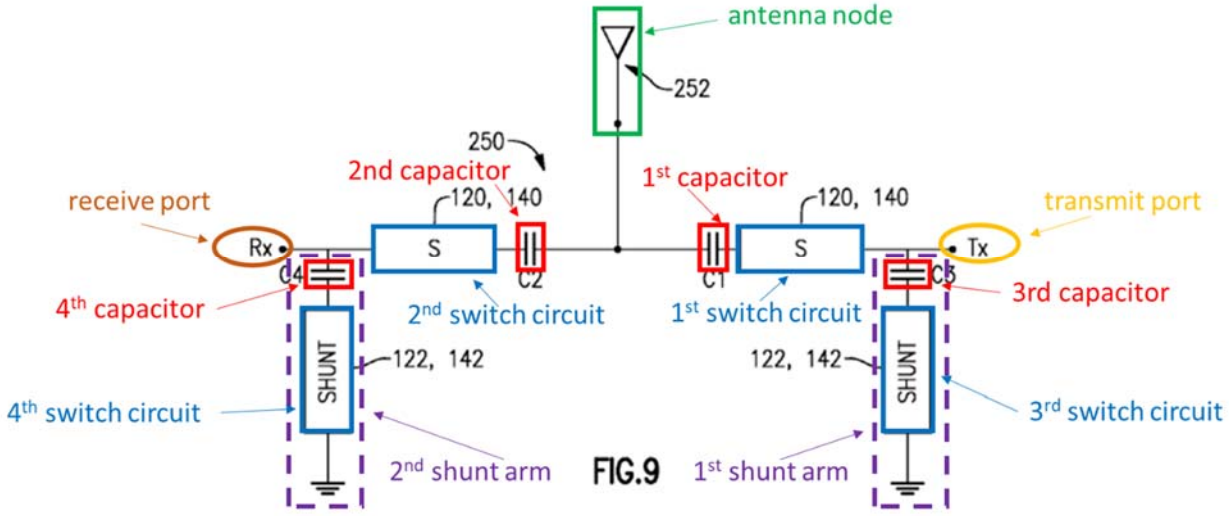


FIG.9

However, this same problem and same solution were well-known in the prior art. For example, Huang (EX-1005) and Seshimo (EX-1007) each describe using the identical configuration of shunt arms and capacitors in an SPDT RF switch of a wireless device, as '194 Patent FIG. 9:

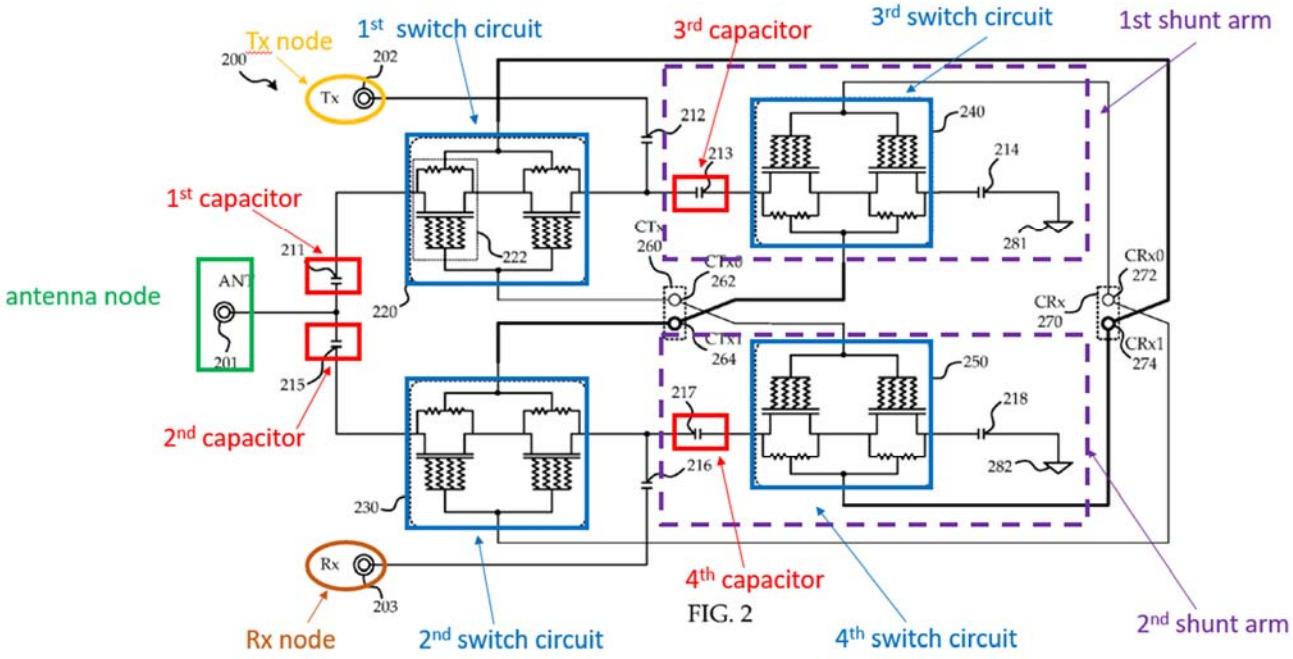
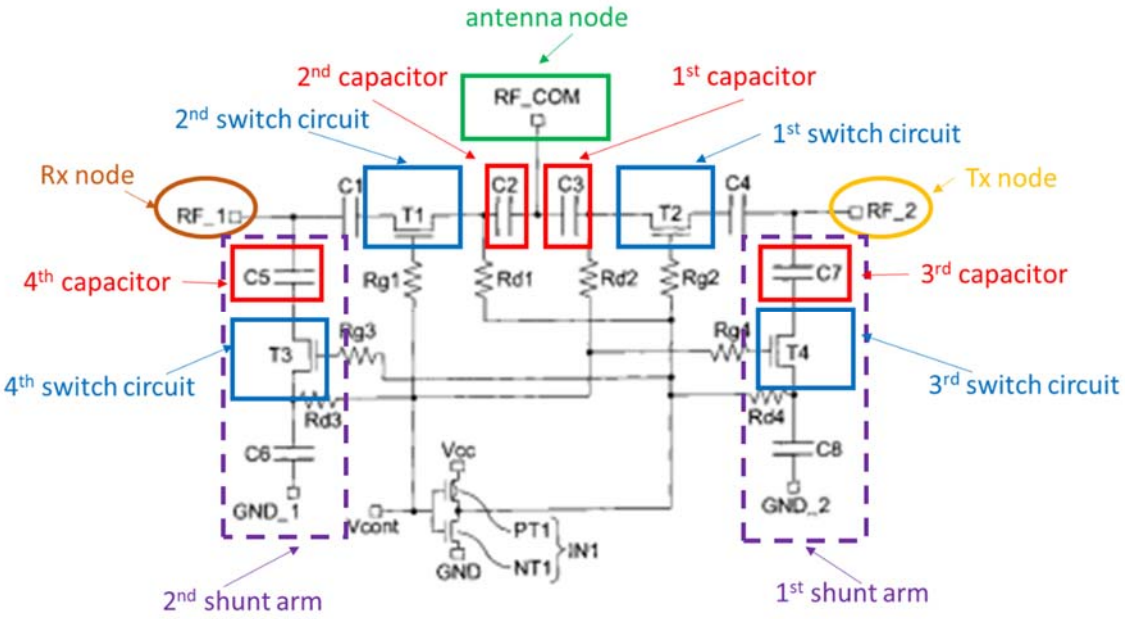


FIG. 2

EX-1005, FIG. 2 (above-annotated).



EX-1007, FIG. 3 (above-annotated).

III. GROUNDS FOR STANDING (37 C.F.R. §42.104(A))

Petitioner certifies the '194 Patent is eligible for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the grounds identified herein. 37 C.F.R. §42.104(a). This Petition is filed pursuant to 37 C.F.R. §42.106(a).

IV. RELIEF REQUESTED (37 C.F.R. §42.22(A))

Petitioner respectfully requests institution of an IPR pursuant to 37 C.F.R. §42.108 and cancellation of the Challenged Claims.

V. REASONS FOR THE RELIEF REQUESTED

As explained in §II and §V-§VII of this Petition and in the Declaration of Petitioner's Expert, Dr. Larry Larson (EX-1003), the systems and methods recited in the

Challenged Claims are obvious over the prior art in view of the knowledge, skill and creativity of POSITAs in July 2012.[1]

A. Summary of the '194 Patent

The '194 Patent is directed to RF switches usable to "switch" signals between a "pole" and one or more "throws" of a wireless device. EX-1001, 1:17-19, 9:8-16. The Patent describes exemplary RF transistor switches, "based on one or more… FETs", arranged in a SPDT configuration, *e.g.*, FIG. 3 (below-annotated):

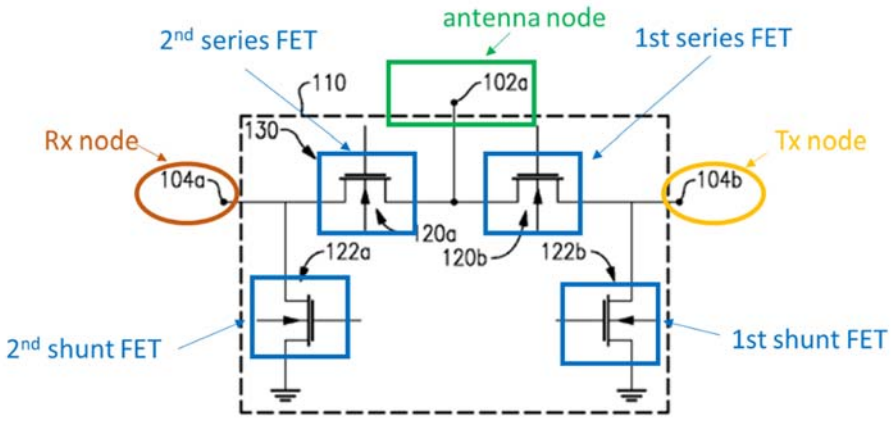


FIG.3

EX-1001, 1:31-34, 3:26-30, 3:49-59, FIG. 3; EX-1003, ¶¶28-30. Using multiple FETs per switch arm, *e.g.*, FIG. 4 (below-annotated), in lieu of single FETs (*e.g.*, FIG. 3),

[1] All emphasis in quoted materials, and figure annotations, in the Petition were added by Petitioner.

"enables improved power-handling capability of the switching device", but, "in some embodiments,… degrades the switching device insertion loss[2] performance":

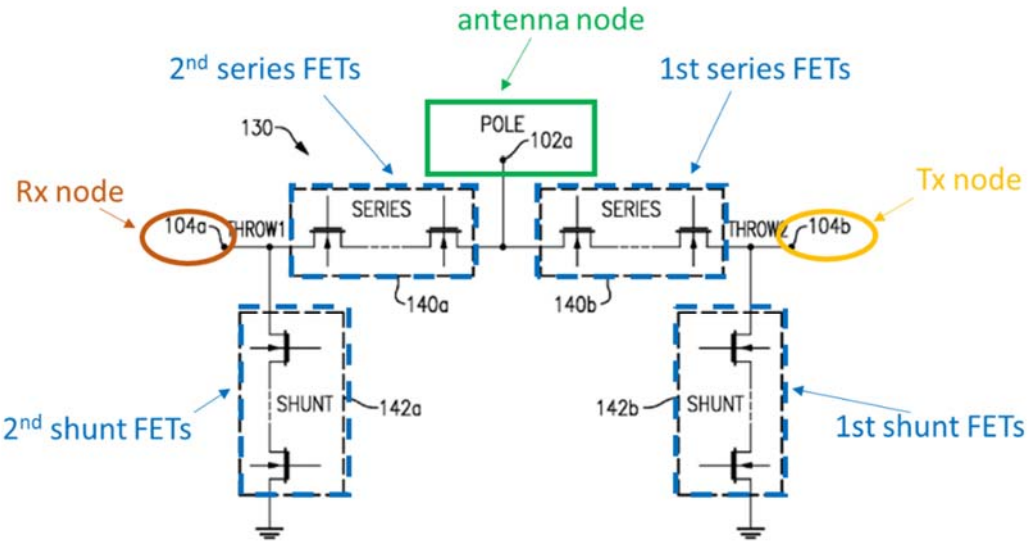


FIG.4

EX-1001, 4:18-48, 7:5-19, 8:18-39; EX-1003, ¶31.

These RF switches (including FETs) optionally "can be fabricated with silicon or silicon-on-insulator (SOI) technology", where using SOI technology could "reduce[] power consumption of device circuitry due to decreased parasitic capacitance of transistors and interconnect metallization to a silicon substrate"; "reduce junction

[2] "[I]nsertion loss" was well-known as "measured as a ratio of the [respective] power or voltage of an RF signal" between "an input port", and "an output port", "of the switching device", with "[d]ecreased… insertion loss" being "desirable". EX-1001, 5:48-63; EX-1036, 1; EX-1039, 5, 9-11; EX-1009, 3; EX-1003, ¶31.

capacitance or use of high resistivity substrate, enabling reduced substrate related RF losses" from the "[p]resence of a buried oxide layer"; and "decrease[] chip size" because "[e]lectrically isolated SOI transistors can facilitate stacking." EX-1001, 7:23-47, 1:38-39, 1:55-57, 3:28-30; EX-1003, ¶32.

For both the single-, and multi-, transistor-per-switch-arm arrangements, the "[o]perations of such FETs can be controlled and/or facilitated by… gate bias/coupling circuit 150a,… body bias/coupling circuit 150c, and/or… source/drain coupling circuit 150b", and the "design or features" of each such control circuit (150a, 150b, 150c, FIG. 6) "can improve performance of the switch arm… includ[ing]… device insertion loss, isolation performance[3], power handling capability and/or switching device linearity." EX-1001, 4:65-5:45, FIGS. 5-6, 9:63-10:11, FIGS. 11A-11D. The Patent provides **no** other details on **any** of such control circuits, nor explains **how** any of their "design or features" could result in any of the stated switching performance improvements; thus acknowledging that these implementation details were well-within the knowledge of POSITAs. *Id.*; EX-1003, ¶33.

[3] "[I]solation" was well-known as "measure[d]… while the switching device… input port and… output port are electrically isolated", *e.g.*, "OFF state", where "[i]ncreased… isolation can improve RF signal integrity." EX-1001, 5:65-6:10; EX-1036, 1; EX-1039, 5-6, 10-11, FIG. 5; EX-1009, 3; EX-1003, ¶33.

The Patent is directed to a well-known problem in designing RF switches in wireless devices, especially those operating in a "multi-band and/or multi-mode environment", namely "the susceptibility of a [RF switch] system to interference" from unwanted signals. EX-1001, 6:33-7:3, 8:61-9:7, 5:66-6:8; EX-1003, ¶34. For example, as was well-known to POSITAs[4], when an unwanted signal (*e.g.*, "blocker" signal) mixes with a desired ("fundamental") RF signal in an RF switch, the desired transmitted/received information may be degraded, and further unwanted signals may be created. *Id*.; EX-1001, 6:9-32, 8:55-60; EX-1003, ¶34. These created unwanted signals may be at frequencies that are multiples of a desired RF signal frequency (f_1) (*e.g.*, $2f_1$, $3f_1$, etc.) called "harmonic frequencies", or at non-harmonic frequencies (*e.g.*, f_1+/-$f_{blocker}$, $2f_1$+/-$f_{blocker}$, etc.) called "intermodulation distortion (IMD)" products. *Id*.; EX-1003, ¶34.

The Patent describes a multi-pronged solution to this "interference susceptibility" problem. First, since "[a] given system's linearity can govern how much IMD will occur within it, which in turn can create interferences", "[s]ystem designers typically strive to reduce interference susceptibility through, for example, improved linearity…

[4] Patent Owner's ("PO's") own articles and whitepapers evidence that this same problem was well-known to POSITAs. §V.F.2 (EX-1039, 2-6, 8-12 (*citing* EX-1040, 3-6); EX-1036, 1-2).

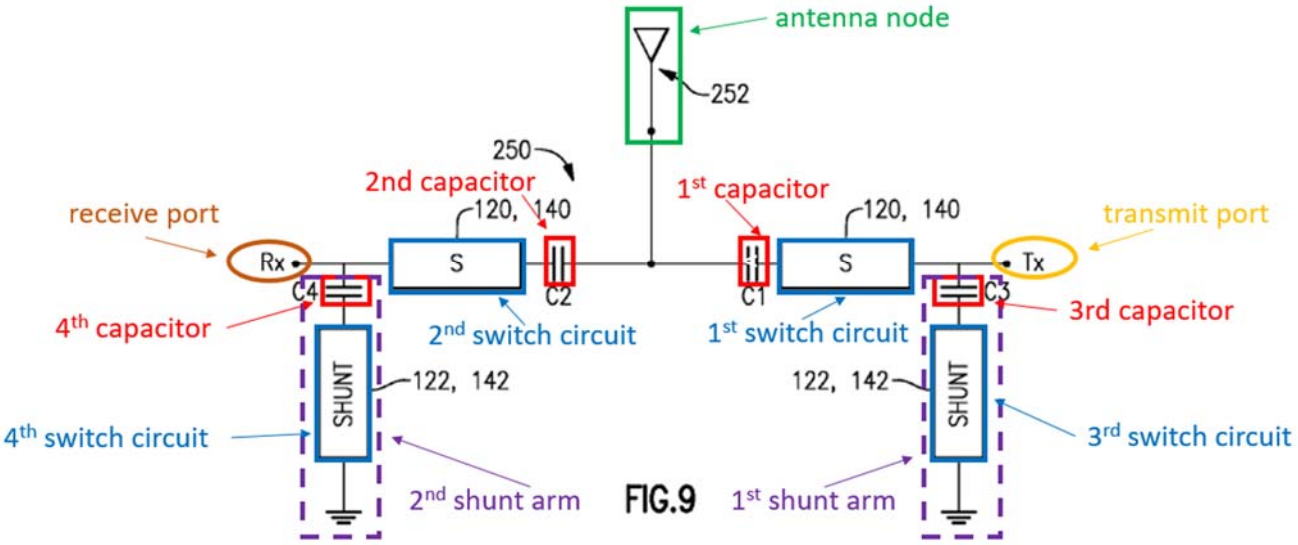
of the system building blocks, such as an RF switch." EX-1001, 8:61-67, 6:38-44, 6:62-65, 5:13-45, FIG. 6; EX-1003, ¶35.

Second, the Patent discloses how including a "shunt arm" in each RF switch "throw" addresses this "interference susceptibility" problem. Referring to FIGS. 3 and 4 (above-annotated), the Patent describes "single pole 102a" (antenna) is "coupled to first and second throw nodes 104a, 104b [receive and transmit nodes respectively] via first and second… FETs[] 120a, 120b." EX-1001, 3:38-43, 3:52-59, 4:24-29, 1:38-45, 9:8-16, FIGS. 2-4. Each throw node (104a, 104b) is "coupled to… RF ground" via a respective shunt FET (122a, 122b) to "provide shunting capability for the node." EX-1001, 3:59-64, 4:30-34, FIGS. 3-4. During operation, when "an RF signal is being passed between… pole 102a and… first throw 104a", (i) "FET 120a" is "ON"; (ii) "FET 120b" is "OFF"; (iii) "shunt FET 122a… [is]… OFF… so that the RF signal is not shunted to ground as it travels from… pole 102a to… first throw node 104a"; and (iv) "shunt FET 122b… [is]… ON… so that any RF signals or noise arriving at the RF core 110 through the second throw node 104b is shunted to… ground so as to reduce undesirable interference effects to the pole-to-first-throw operation."[5] EX-1001, 3:28-

[5] The same FIGS. 3, 4 and 9 configuration and operation of series and shunt FETs in SPDT RF switches, and described benefits and tradeoffs, were well-known to POSITAs (as evidenced by Patent Owner's ("PO's") own article/whitepapers). EX-1024, 1, 3-4,

35, 3:65-4:11, 4:35-48; *see id*., 9:8-24, 9:39-44, FIGS. 9-10; EX-1003, ¶36.

Third, the Patent states that the particular arrangement of RF switch components depicted in Figure 9 (below-annotated)—specifically, the positioning of (i) "capacitor C1… between the antenna node and… switch arm S of the TX throw"; (ii) "capacitor C2… between the antenna node and… switch arm S of the RX throw"; (iii) "capacitor C3… between the TX node and its shunt switch"; and (iv) "capacitor C4… between the RX node and its shunt switch"—"can lead to improvement in IMD performance, especially for low-frequency blocker signals":



EX-1001, FIG. 9, 9:8-38, 9:49-54, 4:64-5:45, FIGS. 5-6, 10:11-27, FIGS. 11A-11D; EX-1003, ¶37.

Unsurprisingly, given that a well-known, fundamental characteristic of all

FIG. 15; EX-1008, 3, Figure 1; EX-1039, 10, Figure 12; §V.F.2-§V.F.3; EX-1003, ¶36.

capacitors (with a given capacitance value, which designers can select as appropriate) is that they have a **much** higher opposition (impedance) to low-frequency signals than high-frequency signals, outside of the positioning of the capacitors in the FIG. 9 SPDT switch, the Patent leaves the remaining implementation details of this solution to design choices of POSITAs. *Id*.; §V.F.1-§V.F.3; EX-1003, ¶38.

Indeed, the Patent does not provide **any** details as to, for example, (i) **how** the positioning of capacitors in the FIG. 9 SPDT switch "prevent[s] a low-frequency blocker signal from mixing with a fundamental frequency signal", (ii) **what value** the capacitors must have to perform this function, (iii) **where** the "low-frequency blocker signal" originates from, nor (iv) **what** constitutes a "low" frequency "blocker" signal relative to a "fundamental" frequency. *Id*.; EX-1001, 6:11-7:3, 8:55-9:55; EX-1003, ¶39. Accordingly, the Patent recognizes the low-frequency-blocking-high-frequency-passing characteristic of capacitors was well-within the knowledge of POSITAs, and leaves the other implementation details to design choices of POSITAs. *Id*.

The Patent states (i) "capacitors C1-C4 described in reference to FIGS. 9 and 10 can be implemented on the same die as their respective switch circuits, off of the die, or any combination thereof" (EX-1001, 9:45-49, 2:15-21), and (ii) "bias/coupling circuit 150" (*id*., 4:64-5:55, FIGS. 5-6) "can be implemented" entirely/partially on the same die, or entirely/partially on a different die, as the die on which the SPDT switch is implemented (*id*., 9:62-10:11, FIGS. 11A-11D). However, the Patent does not identify

any benefits or tradeoffs associated with such design choices. Again, this lack of detail is not surprising as these were well-known design choices, with well-known advantages and tradeoffs, to POSITAs. §V.F.2-§V.F.4; EX-1003, ¶40.

B. Summary of the Prosecution History

As filed July 6, 2013, original claim 1 recited:

A radio-frequency (RF) switch system comprising:

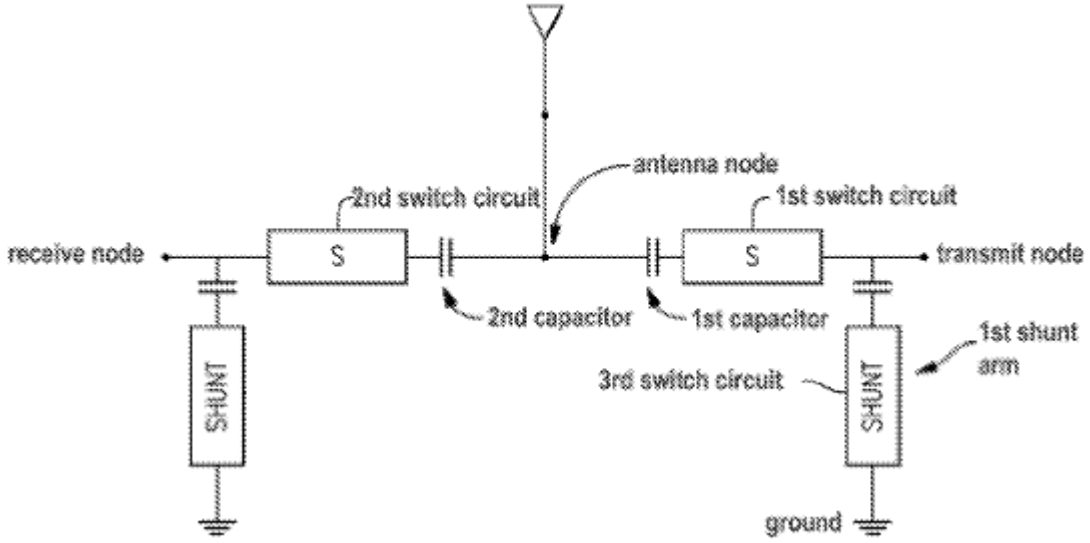
a switch having a stack of field-effect transistors (FETs) connected in series between first and second nodes; and

a capacitor connected in series with the switch and configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

EX-1002, 345-347, 303-305 (all original independent claims include "switch"/"capacitor" limitations); EX-1003, ¶42. All pending claims, except dependent claims 4-6 (objected to as allowable except for dependency on rejected claims), were finally rejected as obvious. EX-1002, 40-45, 57-60. In response, Applicant "amended independent claims 1, 10 and 12 to include the limitations of dependent claims 3 and 4" (*see* §VII ([1.5.1]-[1.5.2], [1.6.1]-[1.6.2])) and "rewr[ote] claim 6 [*id*., ([4.5.2])] in independent form including the limitations of" claims 1 and 3. EX-1002, 28-34. The claims were then allowed, and the '194 Patent issued. EX-1002, 1, 7-14.

To achieve subsequent allowance of related Patent 9,450,579, Applicant amended the independent claims and argued:

The features of [the] amended claim[s] can be understood with reference to Figure 9, which is provided in annotated form below:



Applicant submits that the cited references fail to disclose or render obvious **the particular configuration** claimed in [the] amended claim[s], **particularly with respect to the positioning of the first and second capacitors with respect to the antenna node, and further with respect to the shunt arm**.

EX-1037, 37-39, 31-34, 15-18; EX-1003, ¶43.

C. Claim Construction

Petitioner proposes that each claim term in the Challenged Claims be given its plain and ordinary meaning in this proceeding, and that no specific construction of any claim term is required because the prior art relied on in this Petition meets each of the claim terms under any reasonable construction. EX-1003, ¶¶44-46.

D. Priority Date of the Challenged Claims

The '194 Patent was filed July 6, 2013, claiming priority to July 7, 2012;

therefore, Petitioner assumes the priority date is July 7, 2012.

E. Person of Ordinary Skill in the Art

A POSITA in July 2012 would have been someone knowledgeable and familiar with RF electronics, including RF switches and electrical components of such switches, and semiconductor manufacturing processes. POSITAs would have gained knowledge of these concepts through a mixture of training and work experience, such as by having a Bachelor's degree in electrical engineering, or related field, and approximately two to three years of related experience; or by obtaining a Master's degree in electrical engineering, or related field, but having only a year of related experience; or by having no formal education but experience in RF electronics and semiconductor packaging of at least six to eight years. EX-1003, ¶48.

F. State of the Art

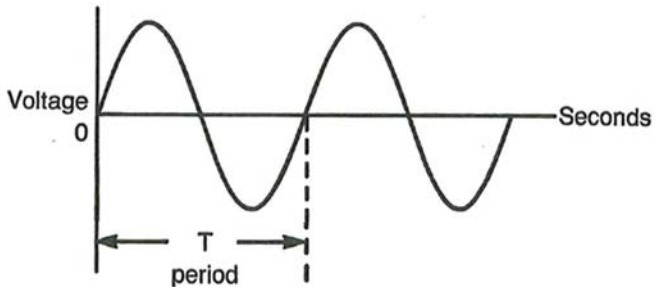
The following section describes the state of the art as of July 2012. EX-1003 ¶51. The prior art references, and discussions of what was known to POSITAs, provide the factual support for the general description of the state of the art in July 2012, and provide additional motivation to modify or combine teachings in the references and/or to make design choices given a reference's teachings. Accordingly, these references should be considered by the Board.

1. Textbook EE Concepts Regarding Radio Frequency Electrical Circuits and Capacitors in such Circuits

There are several basic, textbook-type electrical engineering (EE) concepts

relevant to the state of the art.

First, RF communications waveforms are routinely represented by an alternating current (AC) signal in which a single complete waveform is known as a "cycle", and the number of cycles occurring in one second is the "frequency", *i.e.*, frequency (*f*) is the rate at which a given waveform repeats, and is measured in hertz (1 Hz=1 cycle/second):

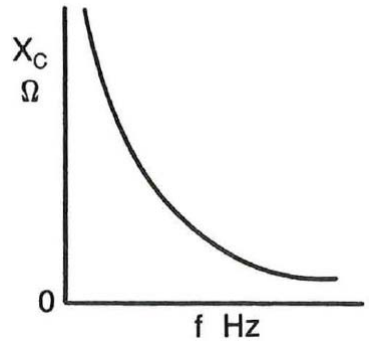


EX-1012, 200-201; EX-1027, 83; EX-1014, 30-31. The complete cycle time interval—"period" (T)—is the reciprocal value of frequency, measured in second(s). *Id*.; EX-1003 ¶53.

Second, capacitors "[t]o a first approximation… are devices that might be considered simply frequency-dependent resistors." EX-1014, 20, 30; EX-1027, 82-83; EX-1012, 231-234; EX-1003 ¶54.

A fundamental characteristic of all capacitors is that their opposition to the flow of an AC waveform (*e.g.*, RF), called "capacitive reactance" (X_c) or, more generally, "impedance", measured in ohms (Ω), is "*inversely* determined by the product of the frequency and the capacitance", with this fundamental characteristic expressed in the

equation $Xc = \frac{1}{2\pi fC}$ and shown in the below graph of X_c versus AC signal frequency (f):



EX-1012, 231-234; EX-1027, 83; EX-1014, 29-32, 37 (Figure 1.56(A)); EX-1043, 128-129; EX-1024, 3-4; EX-1003 ¶55.

Accordingly, all capacitors, regardless of capacitance value, have an essentially infinite opposition to DC current (f=0Hz); in other words, all capacitors block (*i.e.*, are essentially open circuits to) the very low frequency that is DC current. EX-1012, 231-232, 175-176; EX-1027, 83, 50; EX-1014, 32, 36-37, 42; EX-1043, 128-129, 137-139; EX-1032, 1-2; EX-1033, 1; EX-1011, 2616-2617; EX-1026, [0049]; EX-1024, 3-4; EX-1031, 8-9, FIG. 13; EX-1003 ¶56. As the frequency of the in-series current increases, the impedance drops; at a sufficiently high frequency signal (for a given size capacitor) the impedance drops to the point where the capacitor approximates a conductor. *Id*.; EX-1003 ¶56.

As a simple example of the fundamental low-frequency-blocking, and high-frequency-passing, characteristic of typical capacitors used in typical RF switches, a 10pF capacitor has an impedance X_c of ~16,000Ω to 1MHz signals, ~84Ω to 190MHz

signals, and ~7Ω to 2.4GHz signals. *Id.*; EX-1011, 2616-2617 (10pf); EX-1024, 3 (5-15pf); EX-1010, [0040] (8.4pF); EX-1029, 36-39 (20pF, 2.7pF); EX-1017, [0025]; EX-1014, 32; EX-1027, 83; EX-1012, 232-234; EX-1003 ¶57.

Third, due to this fundamental characteristic of capacitors, a basic high-pass filter (having the "desirable property of passing [high] signal frequencies of interest while rejecting undesired [low] signal frequencies") was, as shown in the EE textbook figure (below-left-annotated), simply a capacitor connected in series between the RF waveform source node and output node, and in series with a resistor ("50-ohm standard impedance for RF circuits" is commonly used), and with the fundamental "-3dB 'breakpoint'" of this filter expressed in the equation $f_{3dB} = \frac{1}{2\pi RC}$ and shown in the graph (below-right) of signal amplitude reduction (as a fractional ratio) versus AC signal frequency (in radians (ω[6])):

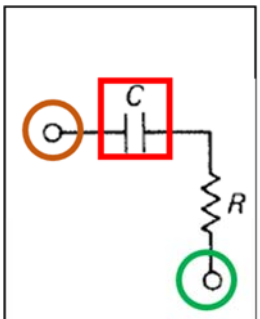


Figure 1.53

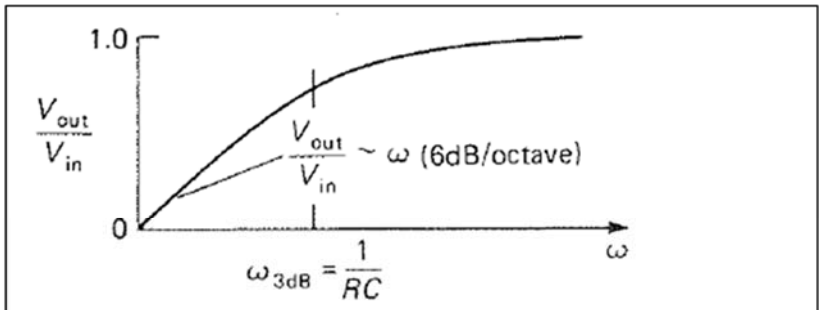


Figure 1.55. Frequency response of high-pass filter.

[6] Radians (ω) were a well-known shorthand for 2π*f*. EX-1014, 30, 36-37; EX-1003 ¶58.

EX-1014, 36-37 (Figures 1.52-1.55), 39-40; EX-1043, 137-139, 236-238, FIGS. 5-17(A), 8-17(B), 8-17(D), 8-18(B), 8-18(D); EX-1044, 1-2; EX-1011, 2617-2618 (FIG. 9(a), 2x10pF capacitors/throw, f_{3dB}=636.9MHz); EX-1009, 3 ("system characteristic impedance (normally 50Ω)"); EX-1036, 2; EX-1040, 4-5; EX-1019, [0179]; EX-1017, 2:55-58; EX-1007, [0029]; EX-1010, [0040] (2x8.4pF capacitors/throw, f_{3dB}=757.9MHz); EX-1024, 3, Figure 15 (2x 5-15pF capacitors/throw, f_{3dB}=1.27GHz to 424.MHz); EX-1003 ¶58.

The EE-textbook-type "-3dB 'breakpoint'" (f_{3dB}) of this fundamental high-pass filter is the low-frequency value at which the input AC signal amplitude "is reduced to 0.707 of its maximum" and where, if an even more-attenuated filter fall-off point was desired for the particular application, POSITAs understood such amplitude "is reduced to 0.45 of its maximum at $f_{[3dB]}/2$…, to 0.25 of its maximum at $f_{[3dB]}/4$…, to 0.125 of its maximum at $f_{[3dB]}/8$…" and so on. *Id*.; EX-1003 ¶59.

Selecting a capacitance value of capacitors in RF switches based on, for example, fundamental frequency values (for which designers want capacitors to essentially act as short circuits (very low-impedance resistors)), practical size constraints, and low frequencies of undesired, potentially interfering signals (for which designers want capacitors to essentially act as open circuits (very high-impedance resistors)), was widely known to, and well-within the skill and creativity of, POSITAs. EX-1014, 36-37; EX-1043, 137-139; EX-1026, FIG. 2, [0002], [0040], [0049], [0051], [0063]; EX-

1011, 2615-2618; EX-1009, FIG. 2, [0083]-[0084]; EX-1024, 3; EX-1032, 1-2, FIG. 1; EX-1031, 8-9, FIG. 13; EX-1035, 5; EX-1042, 294, 298, 308, 312; EX-1003 ¶60.

Accordingly, given these well-known factors, typical capacitance values were well-known to be in picofarads (pF) or nanofarads (nF) for use in semiconductor-based RF switches. *Id.*; EX-1024, 3 (5-15pF); EX-1011, 2616-2617 (10pF); EX-1010, [0040] (8.4pF); EX-1033, 1 (47pF); EX-1029, 36-39 (20pF, 2.7pF); EX-1042, 96, 172, 180, 227, 275, 286 (22pF, 47pF, 4.7pF); EX-1031, 8-9 (100pF); EX-1017, [0025]; EX-1014, 21; EX-1012, 158-159; EX-1003 ¶61.

2. Well-Known Operation and Performance Evaluation of Single-Pole-Multi-Throw (SPnT) Transistor Switches

Single-Pole-Multi-Throw ("SPnT") (*e.g.*, SPDT) switches, including those using semiconductor-based FETs, were well-known and widely used in RF applications. EX-1024, 1, 4; EX-1021, 1; EX-1010, [0002]-[0009]; EX-1023, 1:13-24, 3:43-47; EX-1039, 1, 9-10; EX-1041, 1; EX-1003, ¶62.

PO's June 2009 article ("Cory") describes the "class of switches, commonly known as transmit-receive (T-R) switches, used in transceiver applications whose function is to connect the antenna to the transmitter… in the transmit state and to the receiver during the receiver state", and describes the operation of widely-used SPnT switches for such transceiver applications. EX-1024, 1, 3-4; EX-1003, ¶63.

Cory, and other prior art PO publications, explain that "typical" SPnT switches,

used in high-power, multi-mode, high-fundamental-RF-frequency applications, included (i) series and shunt FET switch circuits to shunt "OFF" path high-power, high-frequency signals to ground to prevent them from "leaking into" the "ON" path, (ii) FET control circuitry whose design impacted "isolation", "insertion loss", and "linearity" performance parameters, (iii) "stack[ed]… FETs" for increased power handling, and (iv) capacitors with "quite small (5 to 15pf)" "capacitor values" where "[t]he selection of the capacitor values is critical to insure proper frequency operation and bandwidth":

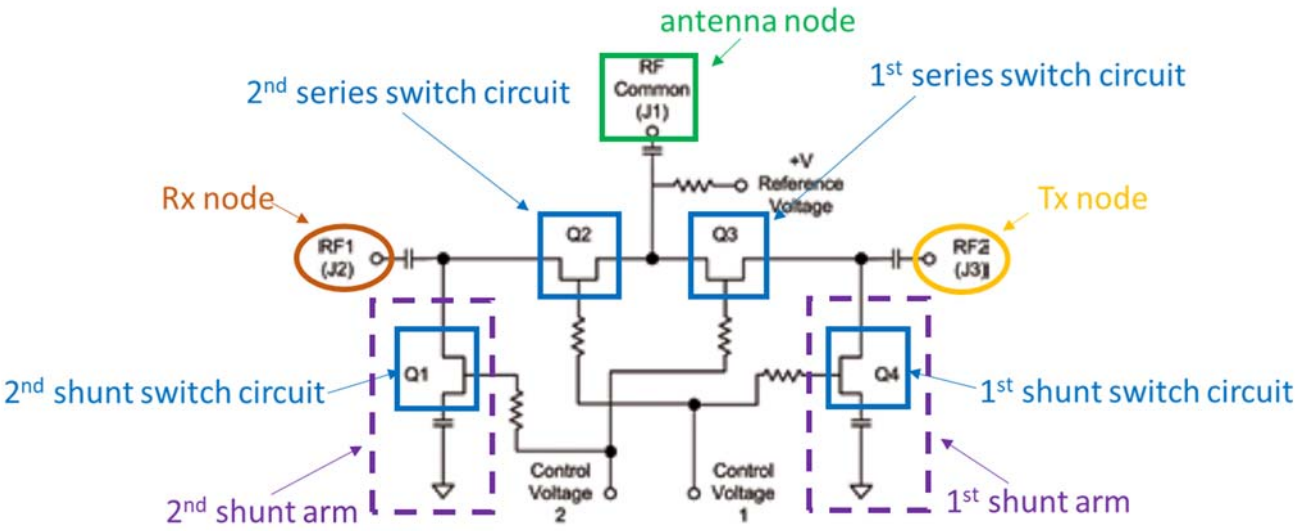


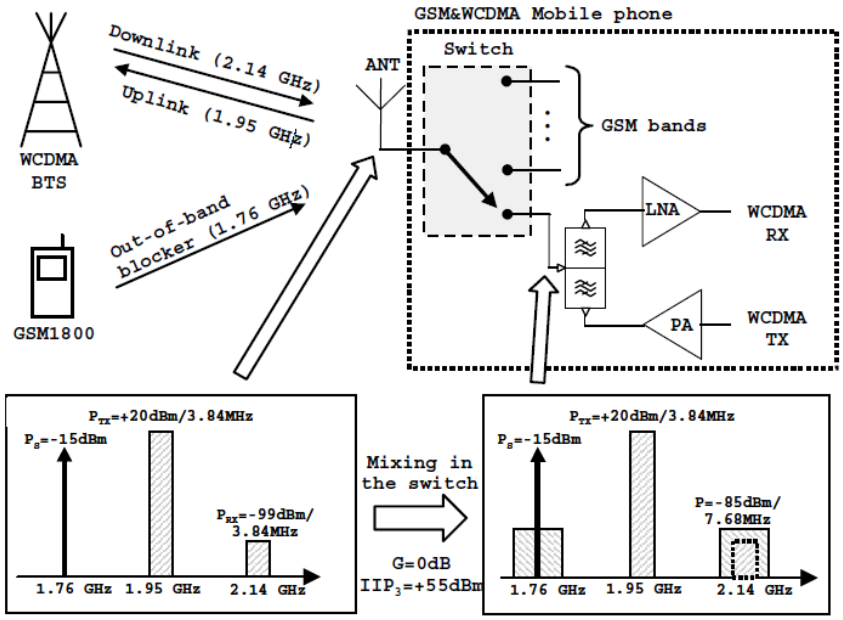
Figure 15: Single Pole Two Throw Switch

EX-1024, 1, 3-5; EX-1039, 4-6, 9-11; EX-1041, 1-2; EX-1008, 3; EX-1023, 5:44-53; §V.F.1; §V.F.4; EX-1003, ¶64.

PO's May 2011 whitepaper (and relied-on 2005 paper) explain that another well-known consideration in designing RF switches in wireless devices, especially those

operating in "multi-mode and multiband" environments, was that if "unwanted" signals (*e.g.*, "out-of-band blocking" signal ($f_{blocker}$)) is allowed to mix with a "wanted" ("fundamental") RF signal (f_{TX}, f_{RX}) in an RF switch, the desired transmitted/received information may be degraded, further "unwanted" signals (*e.g.*, IMD products (*e.g.*, f_{TX}-$f_{blocker}$ (IMD_2), $2f_{TX}$-$f_{blocker}$ (IMD_3)), "harmonics" (*e.g.*, $2f_{TX}$, $3f_{RX}$), etc.) may be created, and calls could be dropped. EX-1039, 2-6, 8-12 *citing* EX-1040, 3-6; *see* EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1049, p.3; EX-1003, ¶65.

In the below-illustrated example, a phone's antenna may pick-up "out-of-band blocker" signals transmitted in the area (*e.g.*, $f_{blocker}$=1760MHz) and, if the RF switch's "linearity is poor", those antenna-picked-up-signals would "mix" with "fundamental" frequency signals (*e.g.*, f_{TX}=1950MHz) inside the switch, and produce IMD_2 (*e.g.*, f_{TX}-$f_{blocker}$=190MHz) and IMD_3 (*e.g.*, $2f_{TX}$-$f_{blocker}$=2140Mhz) products, where the IMD_2 product mixing with the same "fundamental" frequency signal (*e.g.*, 1950MHz+190MHz=2140MHz), or the IMD_3 product (*e.g.*, 2140MHz), could be "right at the" phone's Rx/downlink fundamental frequency causing interference (and possibly dropped calls):



			IMD2 low	IMD3	IMD2 high
Band	**TX** f_{TX}	**RX** f_{RX}	**Blocker 1** $f_{TX}+f_{S1}=f_{RX}$	**Blocker 2** $2f_{TX}-f_{S2}=f_{RX}$	**Blocker 3** $f_{S3}-f_{TX}=f_{RX}$
850	836.5	881.5	45	791.5	1718
1900	1880	1960	80	1800	3840
2100	1950	2140	190	1760	4090

Fig. 4. Dominating out-of-band blocking mechanisms and center frequencies for the 850, 1900 and 2100 WCDMA bands.

Id.; EX-1003, ¶66.

As explained therein and illustrated above, the same result could occur in the same example for antenna-picked-up-blocker signals at 190MHz, *e.g.*, "TV transmission" signals. *Id.*; EX-1045, 1 ("174.0-216.0MHz" is "Broadcasting (TV Channels 7-13)" spectrum); EX-1046, 23-24 ("[T]he radio system… must be able to reject signals outside the band without loss of performance. These signals may be very large (e.g. TV transmissions)… [N]on-linearities in the receiver… will allow unwanted signals to intermodulate… [which] may result in a distortion product falling onto the

wanted signal…"); EX-1003, ¶67.

As further explained therein, typical solutions to "minimize[]" the "distortion products for current dependent nonlinearity" in RF switches, *e.g.*, "nonlinear series resistance[]… of the OFF paths", involved "adjusting the phase so… the switch sees an open circuit at the blocker frequency." *Id*.; EX-1040, 5; EX-1046, 23-24; EX-1003, ¶68.

3. Well-Known Manufacturing Processes to Form SPnT Components on Semiconductor Substrates/Wafers of Semiconductor Dies and Well-Known Monolithic Integrated Circuits and Packages Incorporating the Same

Regarding well-known manufacturing processes and packaging of RF Transmit-Receive SPnT switches, Cory discloses examples of pHEMT FETs, for which fabricating semiconductor material, *e.g.*, GaAs, is grown on a "semi-insulating substrate" that "inherently isolates one FET structure from another," and whereby the switch components ("FET structures", "metal-insulator-metal (MIM) capacitors", etc.) are formed "on or near the top-most layer" of **the same** wafer. EX-1024, 1, 3-4, Figure 8; EX-1039, 9-10; EX-1003, ¶69.

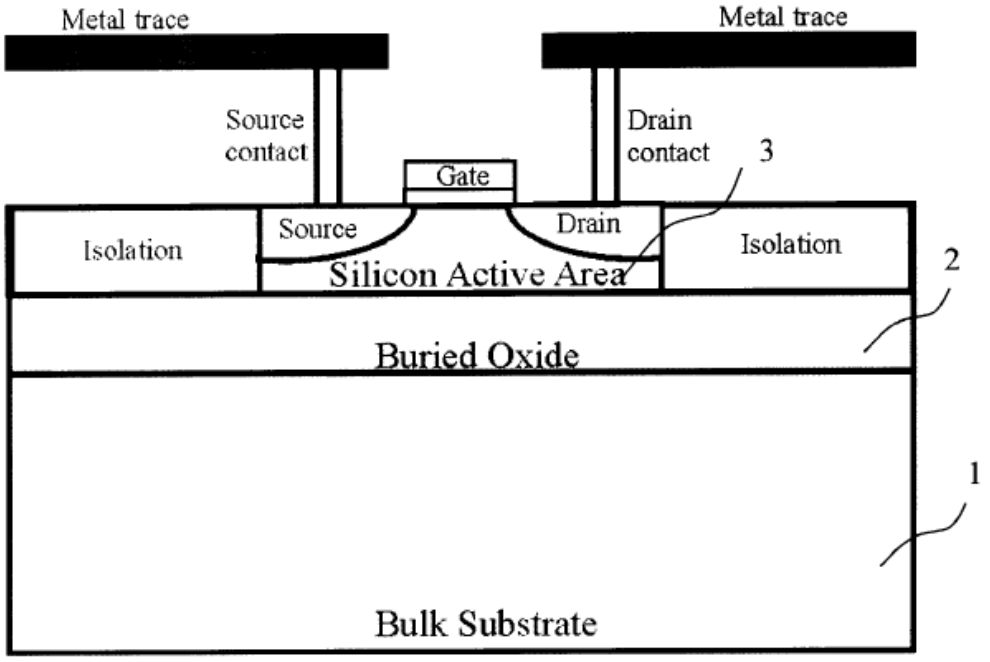
A well-known design choice to POSITAs involved selecting whether to form the SPnT switch capacitors on the same semiconductor substrate of the same die/chip as the FETs, or to incorporate (*e.g.*, in a packaged RF switch module, FEM, etc.) "external" capacitors in the packaging design, where such capacitors would be off of the die/chip

on which the FETs were formed (*e.g.*, formed on a separate substrate of a separate die, surface-mounted to a packaging substrate, etc.). EX-1032, 1-2; EX-1033, 1; EX-1034, FIG. 2; EX-1035, 2-5 ("It is desirable to use… On chip MIM… capacitor[s] instead of… external capacitor[s]… **It is possible to use… external capacitor[s]**, but since multiple capacitors are required, the cost of the external capacitor[s]… and **the cost** of connecting [them] to the switch **increase significantly**… **On chip MIM capacitors[s] can be easily manufactured through a semiconductor process and do[] not require additional work**…."); EX-1023, 10:13-17, 8:29-37, 5:59-6:21, FIG. 5; EX-1011, 2616-2617, FIG. 4; EX-1029, FIGS. 1-2, pp.35-36, 40; EX-1003, ¶70.

Regardless of this design choice selection, the well-known, and widely-implemented, approach for packaging a die (or plurality of dies) for commercial sale, testing, shipment, etc. of the SPnT switch (and other components that are incorporated into the packaged module (*e.g.*, external capacitors, control circuitry, LNA, etc.)), was to mount each separate die (and/or surface-mountable component) on, and electrically connect (*e.g.*, wire-bond) each separate die (and/or surface-mountable component) to, a packaging substrate (*e.g.*, printed circuit board ("PCB")) to electrically interconnect the components of the packaged module. EX-1008, 1-3 ("All switches are packaged in industry-standard, plastic surface-mount packages…" *citing* EX-1041, 2); EX-1029, 36-39, Figures 4, 8; EX-1031, 1; EX-1028, 1, 4, Fig. 2 (below-annotated); EX-1038, [0010], [0027], [0029], [0030]-[0032], [0036]-[0037], [0045], FIGS. 2-3; EX-1042, 80-

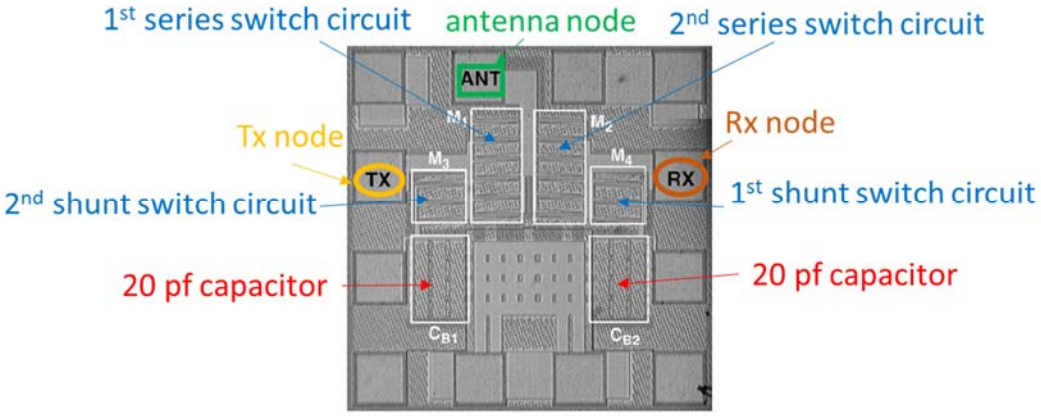
82, 95-97, 105-106, 171-172, 180-181, 192-193, 210, 221-222, 226-227, 237-238, 242, 274-275, 285-286, 298-299, 312-313; EX-1021, 1-3; EX-1033, 1, 3, 9-11; EX-1032, 1-2; EX-1022, [0028]; EX-1036, 1-2 ("RF testing is performed at the package level… RF wafer probe [testing] is performed on 100% of the RF switch die used in Skyworks FEMs."); EX-1003, ¶71.

A well-known alternative to using pHEMT FETs—fabricating the SPnT switch components, including the series and shunt FETs, in silicon, including silicon-on-insulator (SOI), grown over a substrate—had well-understood benefits (*e.g.*, lower cost, higher "thermal conductivity", reduced "degradation in bandwidth associated with the stacking of FET devices", "reduce[d] dielectric losses associated with the silicon substrate", allowing monolithic (same die/chip) integration of SPnT switch and control components and other front-end module (FEM) components, etc.), and trade-offs requiring additional design considerations (*e.g.*, silicon substrates are conductive, accumulated charge in off-state MOSFETs, etc.):



EX-1020, 7:17-18, 8:17-25, 10:5-11, 8:28-29, 1:10-14, 12:27-31, FIGS. 1, 4, 16; EX-1026, [0030]; EX-1039, 9-10; EX-1005, [0040], [0043]; EX-1009, FIG. 2, [0004]-[0005], [0050], [0054], [0058], [0074], [0126], [0142], FIGS. 8-10, 12-14; EX-1018, 4:27-41, 3:50-54, FIGS. 3-4; EX-1010, [0009], [0013], FIG. 3A, [0034]-[0036], [0046]; EX-1022, [0028], FIG. 7, [0046]-[0050]; EX-1025, Abstract, 16:11-18, 16:56-61, 20:57-67, FIGS. 12, 17; EX-1019, [0001], [0004], FIGS. 1, 9, 19, [0013]-[0021], [0073]-[0079], [0148]-[0149], [0159], [0184]-[0191], [0199]-[0200], 68:36-69:21, 70:10-24; §V.B (EX-1002, 61-62; EX-1037, 47-52); EX-1003, ¶72.

A few examples of the monolithic (same die/chip) integration benefits resulting from forming SPnT switches on silicon substrates, including SOI, are provided below:



EX-1029, FIGS. 1-2, pp.35-36, 40; *see* EX-1039, FIG. 12; EX-1021, FIG. 1;

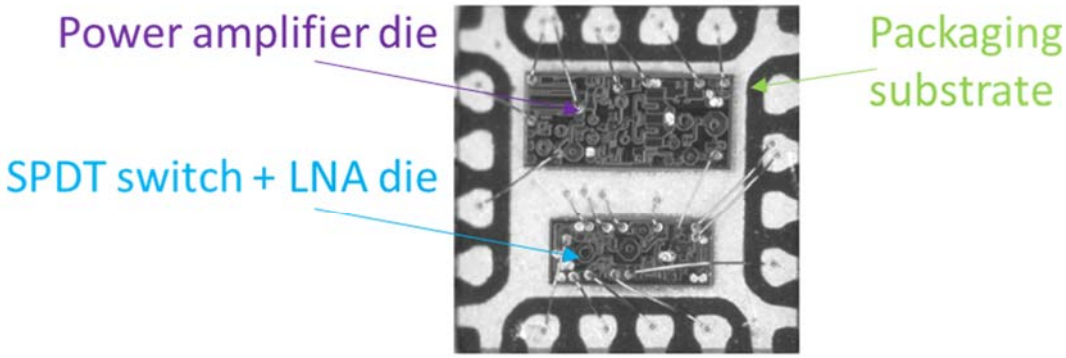


Fig.2. The high linearity 4.9-5.9 GHz FEM in a 3 x 3 mm QFN package.

EX-1028, FIGS. 2, 4, 5, pp.2-3;

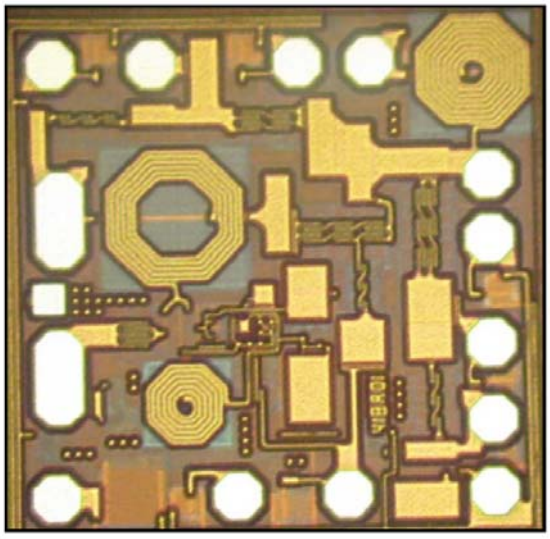


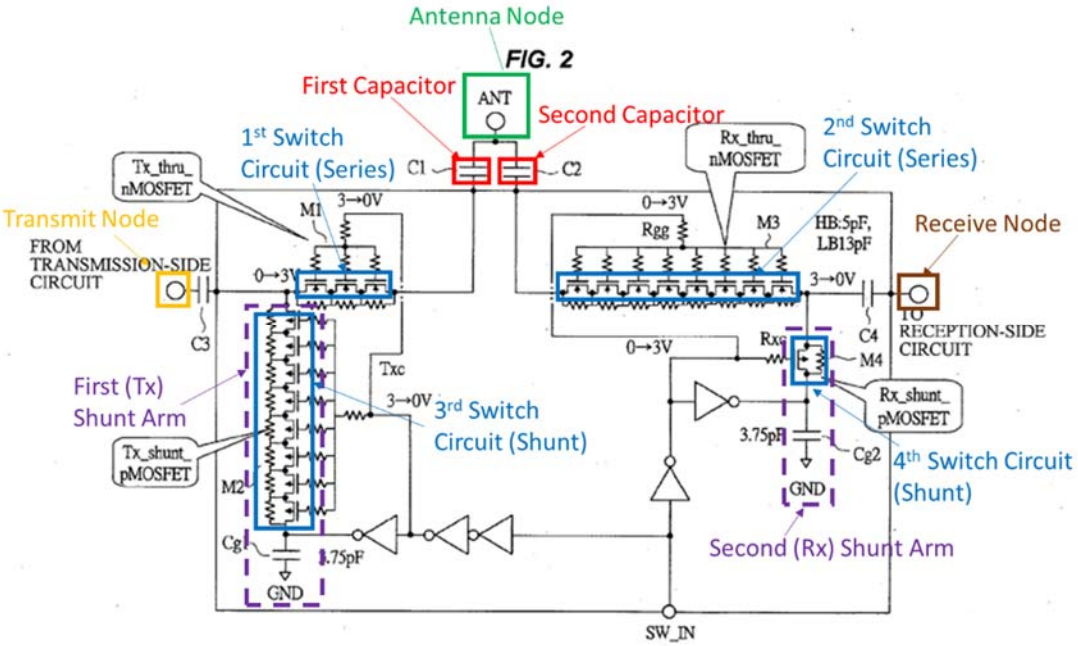
Fig. 8. Die micrograph of the FEIC.

> The front-end integrated circuit (FEIC)… **integrates a SP3T switch and a low-noise amplifier with bypass mode**… [T]he fabricated die… shown in Fig. 8… includ[es] **on-chip** dc blocking and decoupling MIM capacitors.

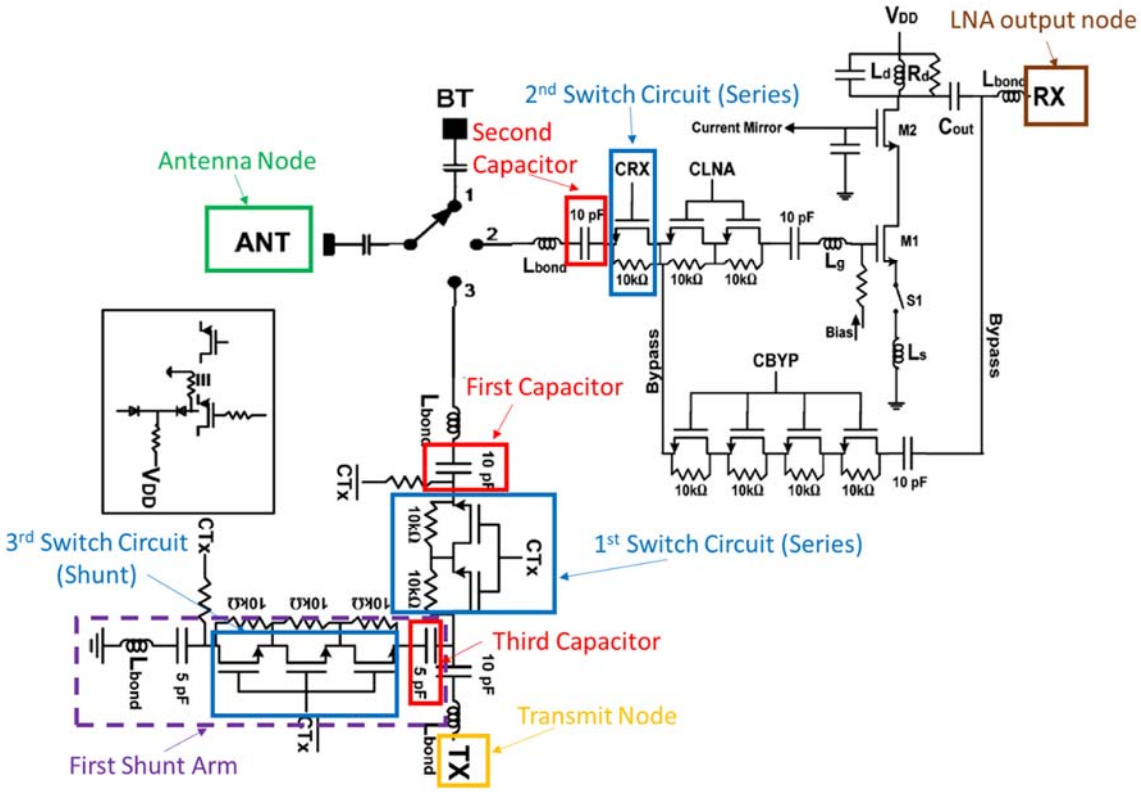
EX-1011, FIGS. 1-2, 4-6, 8, 2613-2617; *see* §V.F.4; EX-1003, ¶73.

4. Exemplary Known Component Configurations in Series and Shunt Switch Arms of SPnT Transmit-Receive Switches in RF Transceiver Applications

By July 2012, as detailed in the Grounds (§VI-§VII below) and shown and described in the below additional examples, the "particular configuration" of components in SPnT transmit-receive switches of wireless devices—including the positioning of capacitors with respect to the antenna, transmit and receive nodes, and the use of shunt arms, as recited in the Challenged Claims—and for purposes of reducing well-known interference susceptibility, and improving other well-known switch performance parameters, were well-known:



EX-1009, FIG. 2 (above-annotated), [0005], [0060]-[0067], [0074]-[0078], [0083]-[0084];



EX-1011, FIGS. 2, 4, 6 (above-combined/annotated), 2613-2617, FIG. 8 (§V.F.3); EX-1010, FIG. 3A, [0034]-[0036]; EX-1003, ¶74.

VI. IDENTIFICATION OF CHALLENGES

A. Challenged Claims

This Petition challenges '194 Patent claims 1-11.

B. Statutory Grounds for Challenges

The Challenges are set forth in detail below and summarized as follows:

Ground	Claims	Basis	Reference(s)
1	1-11	§103	Huang in view of the knowledge, skill and creativity ("Knowledge") of POSITAs
2	1-11	§103	Seshimo in view of the Knowledge of POSITAs

Huang (EX-1005) is Patent Publication 2011/0254614, filed April 16, 2010 and published October 20, 2011. Huang is prior art at least under (pre-AIA) §102(a).

Seshimo (EX-1006/EX-1007) is Patent Publication JP2006-121217A, filed October 19, 2004 and published May 11, 2006. EX-1007 is the certified English translation of EX-1006, and all citations to Seshimo are to EX-1007. Seshimo is prior art at least under (pre-AIA) §102(b).

Neither reference was cited, nor applied by the Examiner, during the '194 Patent prosecution.

VII. IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE

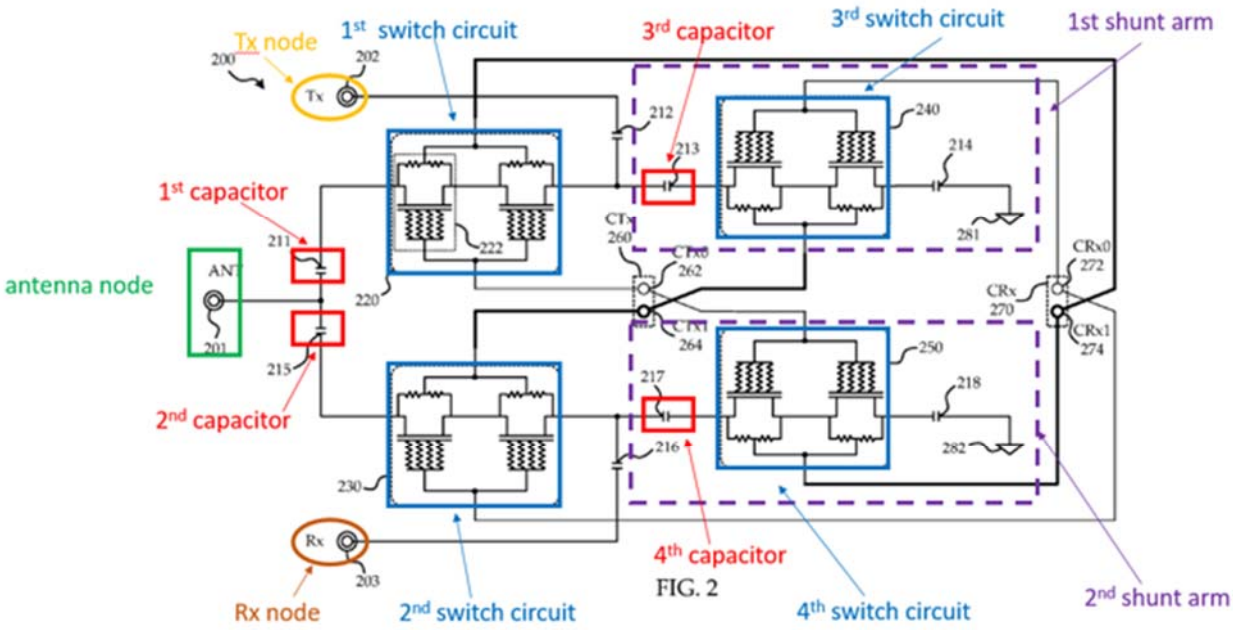
A. Ground 1: Claims 1-11 are obvious under §103(a) over Huang in view of the Knowledge of POSITAs

1. Huang

Huang discloses the identical "particular configuration" of components as '194 Patent FIG. 9, in a "semiconductor-based high power switch" of a wireless device, specifically a "SPDT… transmit-receive switch" formed "using… SOI" technology:

- "first series FET group switch 220" connected between "antenna 201" and "transmit terminal 202";
- "second series FET group switch 230" connected between "antenna 201" and "receive terminal 203";
- "blocking capacitor 211" "coupled in series with… first series FET group switch 220" and connected between Tx-series-switch 220 and antenna 201;
- "blocking capacitor 215" "coupled in series with… second series FET group switch 230" and connected between Rx-series-switch 230 and antenna 201;
- first shunt arm connected to Tx-series-switch 220 and transmit terminal 202, including (i) "first shunt FET group switch 240" connected to ground and (ii) "blocking capacitor 213" connected between this shunt switch 240 and transmit terminal 202; and
- second shunt arm connected to Rx-series-switch 230 and receive terminal 203,

including (i) "second shunt group switch 250" connected to ground and (ii) "blocking capacitor 217" connected between this shunt switch 250 and receive terminal 203:



EX-1005, Abstract, [0001]-[0002], [0122], [0040], [0042]-[0043], claims 5, 19, [0044]-[0045], FIG. 2 (above-annotated), [0051]; §V.A-§V.B; EX-1003, ¶77. Huang also discloses the identical operation of the semiconductor-based, series and shunt FET switches in SPDT switch 200 as the '194 Patent. EX-1005, [0056], [0058]; §V.A; EX-1003, ¶78.

Like the '194 Patent, Huang discloses that the particular configuration of the above-identified series and shunt components in the high-power SPDT transmit-receive switch, formed using SOI technology, and controlled FET biasing when the SPDT is in

transmit, or receive, modes, achieves desirable switching performance parameters including "low insertion loss along the signal path", "high isolation from the off paths", "improved signal quality", "reduce[d] spurious harmonic transmissions", and "good linearity." EX-1005, [0002]-[0003], [0039]-[0040], [0043], [0056]; §V.A; EX-1003, ¶79.

2. Detailed Application of Huang in View of the Knowledge of POSITAs to the Challenged Claims

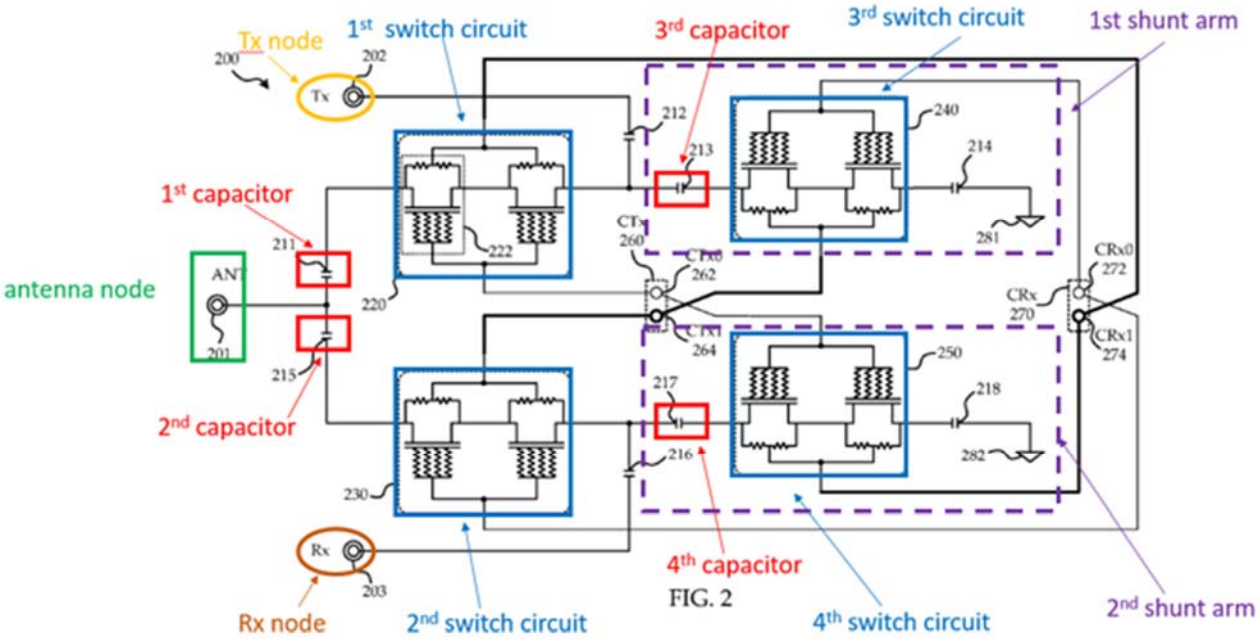
a. Claim 1

i. [1.0] A radio-frequency (RF) switch system comprising:

To the extent the preamble is limiting, Huang discloses incorporating SPDT switch 200 into an RF/wireless device (*e.g.*, "WLAN radio") in which such switch "is often the last/first component encountered by a transmitted/received signal before/after encountering an antenna" (*e.g.*, antenna 201). EX-1005, [0002], [0044]-[0045], [0051], FIG. 2. Huang discloses that SPDT switch 200 includes a respective plurality of "series FET group switches" (*e.g.*, 220, 230) and of "shunt FET group switches" (*e.g.*, 240, 250), where each "FET group switch" includes multiple FETs connected in series to each other. *Id*., EX-1005, [0003], [0120]; EX-1003, ¶¶80-81. POSITAs understood Huang's disclosure of SPDT switch 200 (including as packaged in a "WLAN radio") to constitute an *RF switch system*. *Id*.; *see* [7.0]; EX-1003, ¶82.

ii. [1.1] a first switch circuit connected between an antenna node and a transmit node;

Huang discloses SPDT switch 200 includes "first series FET group switch 220" (*first switch circuit*) connected between antenna 201 (*antenna node*) and transmit terminal 202 (*transmit node*) as illustrated in FIG 2 as annotated ("Annotated FIG. 2"):



EX-1005, [0045]; EX-1003, ¶83. Huang also discloses that each "FET **group** switch" (220, 230, 240, 250) includes multiple FETs connected in series to each other. *Id.*; EX-1005, [0003], [0040]; *see* [1.2], [1.5.1]-[1.5.2], [1.6.1]-[1.6.2].

iii. [1.2] a second switch circuit connected between the antenna node and a receive node;

Huang discloses SPDT switch 200 includes "second series FET group switch 230" (*second switch circuit*) connected between antenna 201 (*antenna node*) and receive terminal 203 (*receive node*) as shown in Annotated FIG. 2. EX-1005, [0045]; EX-1003, ¶84.

iv. [1.3] a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node;

Huang discloses SPDT switch 200 includes "blocking capacitor 211" (*first capacitor*) "coupled in series with… first series FET group switch 220" (*first switch circuit*) and connected between this *first switch circuit* 220 and antenna 201 (*antenna node*) as shown in Annotated FIG. 2. EX-1005, [0045]; EX-1003, ¶85.

v. [1.4] a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node;

Huang discloses SPDT switch 200 includes "blocking capacitor 215" (*second capacitor*) "coupled in series with a second series FET group switch 230" (*second switch circuit*), and connected between this *second switch circuit* 230 and antenna 201 (*antenna node*) as shown in Annotated FIG. 2. EX-1005, [0045]; EX-1003, ¶86.

vi. [1.5.1] a first shunt arm connected to the first switch circuit and the transmit node, [1.5.2] the first shunt arm including a third switch circuit connected to ground;

Huang discloses "[a]long **a shunt path** from… transmit terminal 202 to… transmit branch ground connection 281,… transmit terminal 202 is coupled to… blocking capacitor 213 in series with… first shunt FET group switch 240…" as shown in Annotated FIG. 2. EX-1005, [0045]; EX-1003, EX-1003, ¶87.

Accordingly, POSITAs understood Huang discloses SPDT switch 200 includes *a*

first shunt arm connected to first series FET group switch 220 (*first switch circuit*) and transmit terminal 202 (*transmit node*), and including (i) first shunt FET group switch 240 connected to "transmit branch ground connection 281" (*third switch circuit connected to ground*), and (ii) blocking capacitor 213 (*third capacitor*) connected between first shunt FET group switch 240 and transmit terminal 202. *Id.*; *see* [3.1]; EX-1003, ¶¶88-89.

vii. *[1.6.1] and a second shunt arm connected to the second switch circuit and the receive node, [1.6.2] the second shunt arm including a fourth switch circuit connected to ground.*

Huang discloses "[a]long **a shunt path** from… receive terminal 203 to… receive branch ground connection 282,… receive terminal 203 is coupled to… blocking capacitor 217 in series with… second shunt FET group switch 250…" as shown in Annotated FIG. 2. EX-1005, [0045]; EX-1003, ¶90.

Accordingly, POSITAs understood Huang discloses SPDT switch 200 includes *a second shunt arm* connected to second series FET group switch 230 (*second switch circuit*) and receive terminal 203 (*receive node*), and including (i) second shunt FET group switch 250 connected to "receive branch ground connection 282" (*fourth switch circuit connected to ground*), and (iii) blocking capacitor 217 (*fourth capacitor*) connected between second shunt FET group switch 250 and receive terminal 203. *Id.*; *see* [3.2]; EX-1003, ¶91.

b. Claim 2

i. The switch system of claim 1 wherein at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

Huang discloses this limitation to POSITAs. EX-1003, ¶92. As discussed in [1.3]-[1.4], Huang discloses positioning, in SPDT switch 200 (*the switch*) as shown in Annotated FIG. 2, (i) blocking capacitor 211 (*first capacitor*) between antenna 201 and Tx-series FET group switch 220, and (ii) blocking capacitor 215 (*second capacitor*) between antenna 201 and Rx-series FET group switch 230. Huang's disclosure is identical to the '194 Patent's disclosed positioning in FIG. 9 SPDT switch 250, (i) capacitor C1 between antenna node 252 and Tx-series switch circuit 120/140, and (ii) capacitor C2 between antenna node 252 and Rx-series switch circuit 120/140. EX-1005, [0045]; §V.A (EX-1001, 9:25-38, FIG. 9); §V.B (EX-1002, 61-62; EX-1037, 31-34, 37-39, 47-48, 339-341); EX-1003, ¶93.

Huang discloses the importance of selecting the "arrange[ment]" of "groups of FETs" and "judiciously chosen… capacitors", and of selecting the biasing voltages of the FETs when in "on" and "off" states, in "a high power transmit-receive switch using… SOI" to achieve, for example, "low insertion loss along the signal path", "high isolation from the off paths", "reduce[d] spurious harmonic emissions", and "improve[d] linearity" for the switch. EX-1005, [0002]-[0003], [0039]-[0040], [0043]-

[0045], [0055]-[0059], EX-1003, ¶94. Moreover, Huang expressly refers to capacitors 211 and 215 as "**blocking** capacitor 211" and "**blocking** capacitor 215" respectively, and, as discussed in [1.0]-[1.4], Huang discloses, in SPDT switch 200 intended for use in "modern RF communication systems" (*e.g.*, "WLAN radio[s]"), that (i) "antenna 201 is coupled to… **blocking** capacitor 211 coupled in series with… first series FET group switch 220" "**along a signal path** from… antenna 201 to… transmit terminal 202", and (ii) "antenna 201 is coupled to… **blocking** capacitor 215 coupled in series with… first series FET group switch 230" "**along a signal path** from… antenna 201 to… receive terminal 203." *Id.*, EX-1005, [0051]; *see* [1.0]-[1.4]; EX-1003, ¶95.

Unsurprisingly, just like the '194 Patent, given the fundamental, frequency-dependent impedance characteristic of capacitors—capacitors allow high frequencies to pass through (essentially acting as short circuits) while blocking low frequencies (essentially acting as open circuits)—outside of specifying the identical arrangement of blocking capacitor 211 (*first capacitor*) and blocking capacitor 215 (*second capacitor*) in SPDT switch 200 as the Applicant's relied-on arrangement, Huang leaves the particular capacitor value implementation details to design choices of POSITAs. *Id.*

Moreover, given this fundamental, frequency-dependent impedance characteristic of capacitors, the typical (picofarad) capacitor values selected for RF switches in Huang's disclosed use cases, and the known solution—having "the switch see[] an open circuit at the blocker frequencies"—to the well-known low-frequency, "out-of-band

blocker" signal problem in non-linear RF switches, POSITAs understood Huang's disclosed implementation of blocking capacitor 211 and blocking capacitor 215 in SPDT switch 200 as being high-pass filters "configured to inhibit a low-frequency blocker signal from mixing with a fundamental frequency signal in the RF switch." *Id*., §V.F.1 (EX-1012, 231-234, 175-176; EX-1027, 82-83, 50; EX-1014, 20, 30, 29-32, 36-37, 39-40, 42, FIGS. 1.52-1.55, 1.56(A); EX-1043, 128-129, 137-139, 236-238, FIGS. 5-17(A), 8-17(B), 8-17(D), 8-18(B), 8-18(D); EX-1011, 2615-2618, FIG. 9A; EX-1024, 3-4; EX-1026, [0049]; EX-1031, 8-9, FIG. 13; EX-1010, [0040], EX-1044, 1-2; EX-1029, 36-39; EX-1032, 1-2; EX-1033, 1; EX-1042, 96, 172, 180, 227, 275, 286; EX-1017, [0025]); §V.F.2 (EX-1039, FIG. 5, 2-6, 8-12 (*citing* EX-1040, 3-6, FIGS. 3-4); EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1045, 1; EX-1049, p.3); EX-1003, ¶¶96-97.

Furthermore, to the extent PO asserts Huang does not expressly disclose blocking capacitor 211, and/or blocking capacitor 215, as being configured as claimed, with the SPDT switch 200 components arranged as shown in Annotated FIG. 2, and opposing series and shunt switches placed in ON and OFF states depending on the transmit or receive mode of SPDT switch 200 as disclosed by Huang, POSITAs understood these capacitors' inhibition of low-frequency blocker signals from mixing with fundamental frequency signals in SPDT switch 200 to merely be a matter of design choice. *Id*.; EX-1003, ¶98.

As discussed in the State of the Art section, because blocking capacitors 211 and 215 are fundamentally frequency-dependent circuit elements (with decreasing impedance with increasing frequency), POSITAs understood that tuning the resulting high-pass filters, *i.e.*, setting the frequency range above which these capacitors permit frequencies (*e.g.* the desired RF frequency) to pass essentially unimpeded, and below which (*e.g.*, the "-3dB breakpoint") they impede lower frequencies (*e.g.*, low-frequency "out-of-band blocker" signals), is simply a matter of picking the size capacitor that yields the desired pass/inhibit thresholds within the practical size constraints for the RF device (*e.g.*, "traditional WLAN radio") with a reasonable expectation of success. *Id.*; *see also* §V.F.1 (EX-1009, FIG. 2, [0083], [0084]; EX-1035, 5; EX-1032, FIG. 1; EX-1026, FIG. 2, [0002], [0040], [0049], [0051], [0063]; EX-1042, 294, 298, 308, 312; EX-1049, p.3); EX-1003, ¶99. Filtering antenna-201-picked-up, low-frequency, out-of-band-blocker signals was a well-known problem in RF radios, with a well-known solution (*i.e.*, a series capacitor sized to yield the desired frequency-dependent response as a high-pass filter within the practical size constraints for the RF device). *Id.*; EX-1003, ¶100.

Accordingly, POSITAs would have been motivated to select appropriately-sized blocking capacitors 211 and 215 to pass (with very low impedance) the high frequencies-of-interest (*e.g.,* 2.4Ghz associated with "traditional WLAN radio[s]"), while impeding low, out-of-band frequencies, within the practical size constraints of

such radios, to achieve the known and predictable benefits of improved switch performance (including improved IMD performance) with a reasonable expectation of success given that this involves nothing more than the conventional and routine use of Huang's blocking capacitors. *Id*., EX-1003, ¶101.

c. Claim 3

i. [3.1] The switch system of claim 1 wherein the first shunt arm includes a third capacitor connected between the third switch circuit and the transmit node, and

As discussed in [1.5.1]-[1.5.2], Huang discloses the *first shunt arm*, of SPDT switch 200, includes "blocking capacitor 213" (*third capacitor*) connected between first shunt FET group switch 240 (*third switch circuit*) and transmit terminal 202 (*transmit node*). EX-1005, [0045], Annotated Figure 2; EX-1003, ¶102.

ii. [3.2] the second shunt arm includes a fourth capacitor connected between the fourth switch circuit and the receive node.

As discussed in [1.6.1]-[1.6.2], Huang discloses the *second shunt arm*, of SPDT switch 200, includes "blocking capacitor 217" (*fourth capacitor*) connected between "second shunt FET group switch 250" (*fourth switch circuit*) and "receive terminal 203" (*receive node*). EX-1005 [0045], Annotated Figure 2; EX-1003, ¶103.

d. Claim 4

i. [4.0] A radio-frequency (RF) switch system comprising: [4.1] a first switch circuit connected between an antenna node and a transmit node; [4.2] a

second switch circuit connected between the antenna node and a receive node; [4.3] a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node; [4.4] a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node; [4.5.1] a first shunt arm connected to the first switch circuit and the transmit node, [4.5.2] the first shunt arm including a third switch circuit connected to ground and a third capacitor connected between the third switch circuit and the transmit node.

Huang discloses these limitations for the reasons discussed regarding [1.0]-[1.5.2], and [3.1].

e. <u>Claim 5</u>

i. [5.0] A method for fabricating a semiconductor die, the method comprising:

To the extent the preamble is limiting, Huang discloses a method for fabricating a semiconductor die, including forming the components of the disclosed SPDT transmit-receive switch (SPDT switch 200) on a semiconductor substrate of a semiconductor die, to POSITAs. Huang states "[t]he invention relates to high power semiconductor switches", and discloses that the "transistor switches" in such high power, "semiconductor-based transmit-receive switches", including SPDT switch 200, can be "silicon-on-insulator FET switches." EX-1005, [0001]-[0003], Abstract, [0040], [0042]-[0043], [0122], claims 5, 19, FIG. 2. Accordingly, POSITAs understood Huang discloses providing a semiconductor substrate, and forming the SPDT switch 200

components on the semiconductor substrate to fabricate a semiconductor die, where, in some embodiments, the semiconductor die is a silicon-on-insulator (SOI) die in which the SPDT switch 200 components would be formed on an insulator layer. *Id*.; EX-1003, ¶¶111-113.

To the extent PO asserts Huang does not explicitly disclose providing a semiconductor substrate, and forming the SPDT switch 200 components on the semiconductor substrate, to fabricate a semiconductor die, it would have been obvious to POSITAs to do so, as this was the well-known and widely-implemented approach to provide a stable foundation for fabrication of components of high-power, semiconductor-based, transmit/receive switches, and in order to make manufacturing, testing and production of integrated circuits ("ICs"), including such switches and related circuits (*e.g.*, LNAs)), easier and less costly. *Id*.; §V.F.3 (EX-1018, 4:27-41; EX-1010, [0009], [0013], FIG. 3A, [0046]; EX-1019, [0001], [0004], FIG. 1; EX-1039, 9-10, FIG. 12; EX-1020, FIGS. 1, 4; EX-1009, [0004]-[0005], [0058], FIG. 2; EX-1022, FIG. 7, [0046]-[0050]; EX-1024, 1, 3-4, FIG. 8; EX-1029, FIGS. 1-2, 35-36, 40; EX-1028, 2-3, FIGS. 2, 4, 5; EX-1021, 2-3, FIGS. 1-2, 4-5; EX-1019, [0001], [0004], FIG. 1; EX-1011, 2613-2617, FIGS. 1-2, 4-6, 8; EX-1036, 1-2); EX-1003, ¶114.

ii. [5.1] providing a semiconductor substrate; [5.2] forming a first switch circuit on the semiconductor substrate so as to be connected between an antenna node and a transmit node; [5.3] forming a second switch circuit on the semiconductor substrate so as to

be connected between the antenna node and a receive node;

Huang discloses these limitations for the reasons discussed regarding [5.0], [1.1]-[1.2].

iii. [5.4] forming a first capacitor on the semiconductor substrate so as to be connected in series with the first switch circuit between the first switch circuit and the antenna node;

Huang discloses this limitation for the reasons discussed regarding [1.3], [5.0]. To the extent PO asserts that Huang does not explicitly disclose forming "blocking capacitor 211" (and, *e.g.*, "blocking capacitor 213") on the same semiconductor (*e.g.*, SOI) substrate of the same semiconductor die as the other components (*e.g.*, SOI FETs) of SPDT switch 200, as discussed in the State of the Art sections, POSITAs would have been motivated to do so as a mere design choice to achieve known and predictable benefits, including making manufacturing, testing, and production of SPDT switch 200 (and ICs incorporating the same) easier and less costly, with a reasonable expectation of success, including because low capacitance value (picofarad) capacitors are small in size and typically used in RF switches since, as was well-known to POSITAs, they would pass (with very low impedance) the high frequencies-of-interest (*e.g.,* 2.4Ghz associated with "traditional WLAN radio[s]") while impeding low, out-of-band-blocker frequencies. §V.F.3 (EX-1034, FIG. 2; EX-1035, 2-5; EX-1023, 10:13-17, FIG. 5; EX-1011, 2616-2617, FIG. 4; EX-1029, FIGS. 1-2, pp.35-36, 40; EX-1022, [0028], FIG. 7,

[0046]-[0050]; EX-1010, [0009], [0013], FIG. 3A, [0046]); §V.F.1 (EX-1012, 231-234, 175-176; EX-1027, 82-83, 50; EX-1014, 29-32, 36-37, 42; EX-1043, 128-129, 137-139, 236-238; EX-1032, 1-2; EX-1033, 1; EX-1011, 2615-2618; EX-1026, [0049]; EX-1024, 3-4; EX-1031, 8-9; EX-1044, 1-2; EX-1010, [0040]; EX-1009, FIG. 2, [0083]-[0084], EX-1035, 5; EX-1042, 96, 172, 180, 227, 275, 286; EX-1029, 36-39; EX-1017, [0025]); §V.F.2 (EX-1024, 1, 3-4; EX-1039, FIG. 5, 2-6, 9-12 (*citing* EX-1040, 3-6, FIGS. 3-4); EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1045, 1; EX-1049, p.3); *see* [5.0], claim 2; EX-1003, ¶¶118-119.

iv. [5.5] forming a second capacitor on the semiconductor substrate so as to be connected in series with the second switch circuit between the second switch circuit and the antenna node;

Huang discloses this limitation for the reasons discussed regarding [1.4], [5.0], [5.4].

v. [5.6.1] forming a first shunt arm connected to the first switch circuit and the transmit node, [5.6.2] the first shunt arm including a third switch circuit connected to ground; and [5.7.1] forming a second shunt arm connected to the second switch circuit and the receive node, [5.7.2] the second shunt arm including a fourth switch circuit connected to ground.

Huang discloses these limitations for the reasons discussed regarding [1.5.1]-[1.5.2], [1.6.1]-[1.6.2], [5.0].

f. Claim 6

i. The method of claim 5 further comprising forming an insulator layer between the first switch circuit and the semiconductor substrate.

As explained in [5.0], Huang discloses SPDT switch 200 is a "semiconductor-based", "high-power transmit-receive switch", that may be "implement[ed]… using silicon on insulator (SOI)" technology, with its "transistor switches" (222, 230, 240, 250) being "silicon on insulator FET switches." EX-1005, [0001]-[0003], Abstract, [0040], [0042]-[0043], [0122], claims 5, 19; EX-1003, ¶125.

Unsurprisingly, Huang does not disclose the well-known details of implementing SOI technology to manufacture the SOI FET switches of SPDT switch 200. *Id*. Indeed, as described in the State of the Art section, it was well-known that, in using SOI technology to create ICs, an insulator layer is deposited onto a semiconductor substrate of a semiconductor die, silicon is grown on top of this insulator layer, and then the silicon is patterned and etched to create the various components of the IC (*e.g.*, FETs, capacitors, etc. of SPDT switch 200). §V.F.3 (EX-1020, FIGS. 1, 4, 8:17-25, 7:12, 7:17-18, 10:5-11, 8:28-29, 1:10-14, 12:27-13:8, FIG. 16; EX-1026, [0030]; EX-1018, 4:27-41, 3:50-54, FIGS. 3-4; EX-1039, 9-10, FIG. 10); EX-1003, ¶126.

Accordingly, POSITAs understood Huang's implementation of SOI included an insulator layer disposed between the SOI first series FET group switch 220 (*first switch circuit*) and the semiconductor substrate. *Id*.; EX-1005, [0001]-[0003], Abstract,

[0040], [0042]-[0043], [0122], claims 5, 19; EX-1003, ¶127.

To the extent PO asserts Huang does not expressly disclose an insulator layer disposed between the SOI first series FET group switch 220 and the semiconductor substrate, it would have been obvious to POSITAs to do so as this was the well-known and widely-implemented approach to using the disclosed SOI technology to manufacture "semiconductor-based high power switches" (*e.g.*, SPDT switch 200) with well-known and predictable benefits including, for example, lower cost, higher "thermal conductivity", reduced "degradation in bandwidth associated with the stacking of FET devices", "reduce[d] dielectric losses associated with the silicon substrate", allowing monolithic (same die/chip) integration of SPnT switch and control components and other front-end module (FEM) components, etc. *Id.*; §V.F.3 (EX-1018, 4:37-41; EX-1026, [0030]; EX-1021, 2; EX-1009, [0005]; EX-1010, [0013]); EX-1003, ¶128.

g. Claim 7

i. [7.0] A radio-frequency (RF) switch module comprising:

To the extent the preamble is limiting, as discussed in [1.0] and [5.0], Huang discloses to POSITAs forming the SPDT switch 200 components on a semiconductor substrate of a semiconductor die, and incorporating SPDT switch 200 into an RF/wireless device (*e.g.*, "WLAN radio") in which such switch "is often the last/first component encountered by a transmitted/received signal before/after encountering an

antenna" (*e.g.*, antenna 201). EX-1005, [0001]-[0003], Abstract, [0040], [0042]-[0045], [0051], [0122], claims 5, 19, FIG. 2; EX-1003, ¶129. POSITAs understood Huang's disclosure of SPDT switch 200, formed for use as a component incorporated into (*e.g.*, in a packaged RF switch module, FEM, etc.) RF/wireless devices, to constitute an *RF switch module*. *Id*.; EX-1003, ¶129.

Unsurprisingly, Huang does not disclose the well-known details of packaging the components of SPDT switch 200 for testing, shipment, commercial sale, etc., for such use in such RF/wireless devices. *Id*. Indeed, as discussed in the State of the Art section, given that the well-known, and widely-implemented approach to package a semiconductor die (or plurality of dies) for testing, shipment, commercial sale, etc. of an SPnT switch, and of any other components that are incorporated into the packaged module (*e.g.*, external capacitors, control circuitry, LNA, etc.), was to mount each separate die (and/or surface-mountable component) on, and electrically connect (*e.g.*, wire-bond) each separate die (and/or surface-mountable component) to, a packaging substrate (*e.g.*, PCB), POSITAs would have been motivated to do so as a mere design choice with a high likelihood of success of achieving well-known benefits, such as making packaging, testing, production, shipment, and commercial sales of packaged products (*e.g.*, RF switch module, FEM, etc.) easier, less costly, and more attractive to customers. *Id*.; §V.F.3 (EX-1008, 1-3; EX-1041, 2; EX-1029, 36-39, Figures 4, 8; EX-1033, 1; EX-1028, 1, 4, Fig. 2; EX-1038, [0010], [0027], [0029], [0030]-[0032], [0036]-

[0037], [0045], FIGS. 2-3; EX-1042, 80-82, 95-97, 105-106, 171-172, 180-181, 192-193, 210, 221-222, 226-227, 237-238, 242, 274-275, 285-286, 298-299, 312-313; EX-1021, 1-3; EX-1033, 1, 3, 9-11; EX-1032, 1-2; EX-1022, [0028]; EX-1036, 1-2); EX-1003, ¶130.

ii. [7.1] a packaging substrate configured to receive a plurality of components;

POSITAs reading Huang would have been motivated to implement this limitation as discussed in [1.0], [5.0], [7.0].

iii. [7.2] a semiconductor die mounted on the packaging substrate,

Huang discloses this limitation for the reasons discussed regarding [5.0], [7.0].

iv. [7.3.1] the die including a first switch circuit connected between an antenna node and a transmit node and [7.3.2] a second switch circuit connected between the antenna node and a receive node;

Huang discloses these limitations for the reasons discussed regarding [1.1]-[1.2], [5.0], [7.0].

v. [7.4] a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node; [7.5] a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node; [7.6.1] a first shunt arm connected to the first switch circuit and the transmit node, [7.6.2] the first shunt arm including a third switch circuit connected to ground; and [7.7.1] a second shunt arm connected to the second switch circuit and the receive node, [7.7.2] the

second shunt arm including a fourth switch circuit connected to ground.

Huang discloses these limitations for the reasons discussed regarding [1.3]-[1.6.2].

h. Claim 8

i. The switch module of claim 7 wherein at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

Huang discloses this limitation for the reasons discussed regarding Claim 2.

i. Claim 9

i. The switch module of claim 7 wherein the first capacitor is part of the same semiconductor die as the first switch circuit.

Huang discloses this limitation for the reasons discussed regarding [7.0], [5.4].

j. Claim 10

i. The switch module of claim 7 wherein the first capacitor is part of a second die mounted on the packaging substrate.

As the '194 Patent acknowledges, and as explained in [7.0], [5.0], and [5.4], POSITAs understood this limitation to be obvious as a mere (and well-known) design choice—selecting between forming Huang's blocking capacitor 211 (and the other blocking capacitors) on the same die as the FET group switches, or on a separate capacitor die (*second capacitor die mounted on the packaging substrate*), or mounting

them as surface-mountable components on the same packaging substrate on which the FET-group-switch-die is mounted (claim 11)—based on, for example, size/space constraints, the RF application, the fundamental frequency values, and blocking frequency values, associated with such application, performance requirements, etc., and with well-known benefits and tradeoffs. EX-1005, [0045], Annotated FIG. 2, [0001]-[0002], [0120]-[0124], §V.A (EX-1001, 9:45-49, 2:15-21, 9:62-10:11, FIGS. 11A-11D); §V.F.3 (EX-1035, 2-5; EX-1034, FIG. 2; EX-1032, 1-2; EX-1033, 1; EX-1023, 10:13-17, 8:29-37, 5:59-6:21, FIG. 5; EX-1011, 2616-2617, FIGS. 4, 8; EX-1029, 35-36, 40, Figures 1-2); §V.F.1 (EX-1014, 36-37; EX-1043, 137-139; EX-1026, [0049], [0063]; EX-1011, 2615-2618; EX-1009, FIG. 2, [0083]-[0084]; EX-1024, 3; EX-1031, 8-9, EX-1032, FIG. 1; EX-1042, 294, 298, 308, 312); EX-1003 ¶142.

k. Claim 11

i. The switch module of claim 7 wherein the first capacitor is disposed at a location outside of the semiconductor die.

Huang discloses this limitation for the reasons discussed regarding [7.0], claim 10.

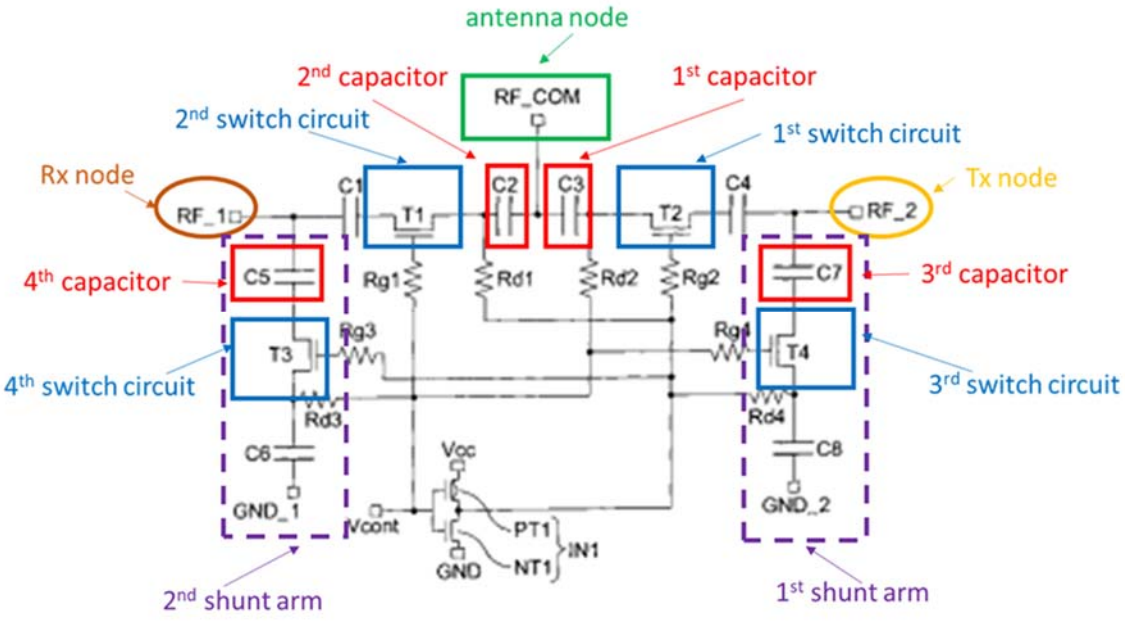
B. Ground 2: Claims 1-11 are obvious under 35 U.S.C. §103(a) over Seshimo in view of the Knowledge of a POSITA.

1. Seshimo

Seshimo discloses the same "particular configuration" of components as '579 Patent FIG. 9, in a "high frequency semiconductor switching circuit… used as a

transmission/reception changeover switch" (FIG. 3 "shunt SPDT switch") of a wireless device (*e.g.*, "PHS (Personal Handyphone System)"):

- "MOSFET T2" connected between "common terminal RF_COM" (*antenna node*) and "high-frequency signal terminal RF_2" (*transmit node*);
- "MOSFET T1" connected between common terminal RF_COM and "high-frequency signal terminal RF_1" (*receive node*);
- "capacitor C3" connected in series with MOSFET T2, and connected between MOSFET T2 and common terminal RF_COM;
- "capacitor C2" connected in series with MOSFET T1, and connected between MOSFET T1 and common terminal RF_COM;
- first shunt arm connected to MOSFET T2 and high-frequency signal terminal RF_2, includes (i) "MOSFET T4" connected to "high-frequency ground terminal GND", and (ii) "capacitor C7" connected between MOSFET T4 and high-frequency signal terminal RF_2;
- second shunt arm connected to MOSFET T1 and high-frequency signal terminal RF_1, includes (i) "MOSFET T3" connected to "high-frequency ground terminal GND", and (ii) "capacitor C5" connected between MOSFET T3 and high-frequency signal terminal RF_1:



EX-1007, [0001], [0003], [0005], [0007], [0029], [0037], [0042], [0054]-[0056], [0065]-[0072], [0090], FIG. 3 (above-annotated); §VII.B.2 ([1.1]); §V.A-§V.B; EX-1003, ¶145.

Seshimo also discloses the identical operation of its series and shunt MOSFETs, in the "high frequency semiconductor switching circuit… used as a transmission/reception changeover switch" (FIG. 3 SPDT switch), as the '194 Patent. *Id.*; EX-1007, [0065]-[0066] (*e.g.*, transmission), [0067]-[0068] (*e.g.*, reception); §VII.B.2 ([1.1]); §V.A; EX-1003, ¶146.

Like the '194 Patent, Seshimo discloses that the particular configuration of the above-identified series and shunt components in the "high frequency semiconductor switching circuit… used as a transmission/reception changeover switch", formed using CMOS processes and SOI, and controlled FET biasing when the SPDT is in transmit, or

receive, modes, achieves desirable switching performance parameters including "improving the maximum permissible input [power/amplitude] to maintain an OFF state" (*e.g.*, power usable by PHS), and "suppressing an increase in ON resistance" (that, without suppression, would "lead to an increase in insertion loss" and a "deterioration in isolation"). EX-1007, [0002]-[0005], [0007], [0011], [0026]-[0030], [0037], [0039]-[0040], [0042]-[0043], [0054]-[0056], [0065]-[0072], [0090]; §V.A; EX-1003, ¶147.

2. Detailed Application of Seshimo in View of the Knowledge of POSITAs to the Challenged Claims

a. Claim 1

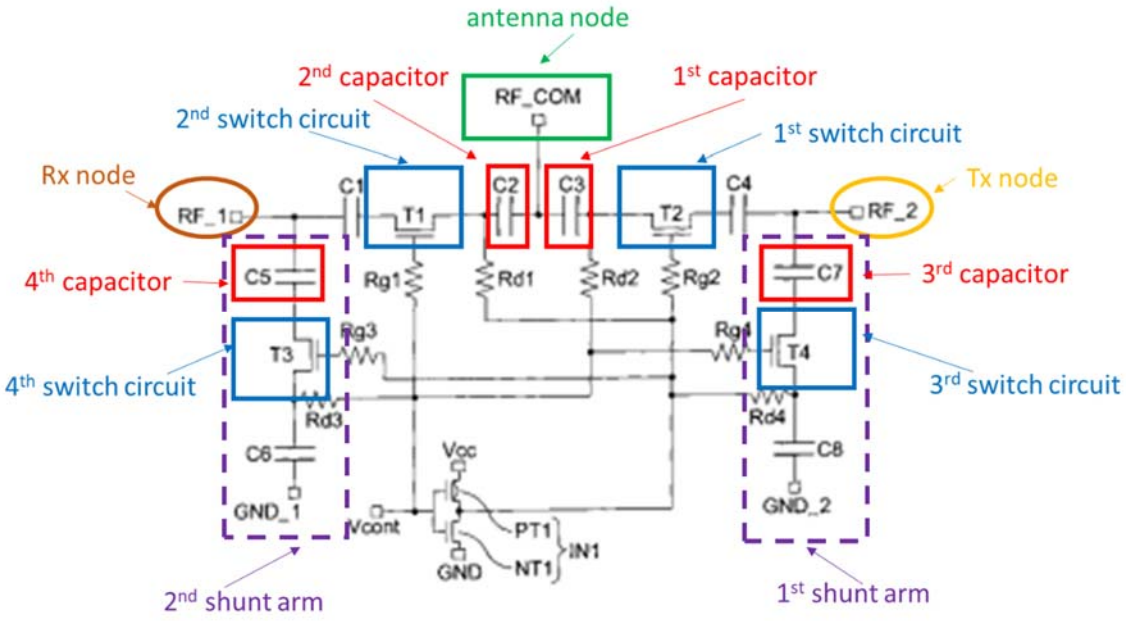
i. [1.0] A radio-frequency (RF) switch system comprising:

To the extent the preamble is limiting, Seshimo discloses a "high frequency semiconductor switching circuit… used as a transmission/reception changeover switch" (*e.g.*, FIG. 3 SPDT switch), formed "using CMOS processes… [to] be integrated into another CMOS RF IC", of a wireless device (*e.g.*, "PHS (Personal Handyphone System)"). EX-1007, FIG. 3, [0001], [0003], [0005], [0007], [0029], [0037], [0042], [0054]-[0056], [0065]-[0072], [0084]; EX-1003, ¶148. Seshimo discloses this "transmission/reception changeover [SPDT] switch" can include vertically "stacking" MOSFETs or "multi-gate structures" to achieve "an even larger maximum permissible input power." *Id.*; EX-1007, [0005], [0071]; EX-1003, ¶149. POSITAs understood

Seshimo's disclosure of FIG. 3 SPDT switch (including as packaged in a PHS) to constitute an *RF switch system*. EX-1003, ¶149.

ii. [1.1] a first switch circuit connected between an antenna node and a transmit node;

POSITAs understood Seshimo discloses FIG. 3 SPDT switch includes "MOSFET T2" (*first switch circuit*) connected between "common terminal RF_COM" (*antenna node*) and "high-frequency signal terminal RF_2" (*transmit node*) as shown in below-annotated FIG. 3 ("Annotated FIG. 3"):



EX-1007, [0001], [0003], [0005], [0007], [0029], [0037], [0042], [0054]-[0056]; EX-1003, ¶150. Seshimo discloses "MOSFETs T1[, T2, T3 and] T4 can be stacked vertically or a multi-gate structure can be used." EX-1007, [0071]; *see* [1.2], [1.5.1]-[1.5.2], [1.6.1]-[1.6.2]; EX-1003, ¶150.

Given Seshimo's disclosure of FIG. 3 SPDT switch achieving the "maximum permissible input power… usable by a PHS (Personal Handyphone System)" where it would be "used as a transmission/reception changeover switch" (EX-1007, [0029], [0070]-[0071], [0005], [0007]), and emphasis on "high-frequency semiconductor switching circuit[s]" (*e.g.*, FIG. 3 SPDT switch) being "developed… using CMOS processes" so the "CMOS switch can be integrated into another CMOS RF IC" (EX-1007, [0003], [0084], [0087]-[0088]), POSITAs understood Seshimo discloses "common terminal RF_COM" as an antenna node, and "high-frequency signal terminal RF_2" and "high-frequency signal terminal RF_1" may be transmit and receive nodes, respectively. EX-1003, ¶151.

iii. [1.2] a second switch circuit connected between the antenna node and a receive node;

Per [1.1], and illustrated in Annotated FIG. 3, Seshimo discloses SPDT switch (FIG. 3) includes MOSFET T1 (*second switch circuit*) connected between common terminal RF_COM (*antenna node*) and "high-frequency signal terminal RF_1" (*receive node*). EX-1007, [0054]-[0056]; [1.1]; EX-1003, ¶152.

iv. [1.3] a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node;

Seshimo discloses capacitor C3 (*first capacitor*), that, (i) like the other capacitors (C2, C5, C7, etc.), may have a "MIM (metal-insulator-metal) structure", and (ii) is

connected in series with MOSFET T2 (*first switch circuit*) and between MOSFET T2 and common terminal RF_COM (*antenna node*) as illustrated in Annotated FIG. 3. EX-1007, [0054]-[0056], [0065]-[0071]; EX-1003, ¶153. POSITAs understood Seshimo discloses resistor Rd2 (and likewise Rd1, and the other resistors in FIG. 3) are used for DC biasing only, such that the depicted Rd2 contact to the series path between MOSFET T2 and RF_COM via capacitor C3 is a "y-junction", which POSITAs understood does not alter the series connection between MOSFET T2 and capacitor C3. EX-1007, [0055]-[0056], [0059]-[0061]; EX-1003, ¶154.

v. [1.4] a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node;

Per [1.3], Seshimo discloses capacitor C2 (*second capacitor*) connected in series with MOSFET T1 (*second switch circuit*) and between MOSFET T1 and RF_COM (*antenna node*) as illustrated in Annotated FIG. 3. EX-1007, [0054]-[0056], [0065]-[0071]; EX-1003, ¶155. Per [1.3], POSITAs understood resistor Rd1's contact to the series path between MOSFET T1 and RF_COM via capacitor C2 is a "y-junction", and does not alter the series connection between MOSFET T1 and capacitor C2. *Id.*; EX-1007, [0055]-[0056], [0059]-[0061]; EX-1003, ¶156.

vi. [1.5.1] a first shunt arm connected to the first switch circuit and the transmit node, [1.5.2] the first shunt arm including a third switch circuit connected to ground;

Seshimo discloses, "in a state in which the inverter circuit IN1 is shared", one of "four units" of FIG. 3 "**shunt** SPDT switch" includes "MOSFET T4, capacitors C7 and C8…", and during, *e.g.*, receive (*see* [1.1]-[1.2]) operations:

> When… Vcont is 3 V The MOSFETs T1, **T4** are… **ON**…, and… MOSFETs **T2**, T3 are… **OFF**… As a result, a conductive state is established between… RF_1 and RF_COM, and **a cutoff state is established between… RF_2 and RF_COM**.

EX-1007, [0054]-[0056], [0067]-[0068], [0060], [0064], [0069]-[0071]; EX-1003, ¶157.

Accordingly, as illustrated in Annotated FIG. 3, POSITAs understood Seshimo discloses *a first shunt arm* connected to MOSFET T2 (*first switch circuit*) and to high-frequency signal terminal RF_2 (*transmit node*), and including (i) MOSFET T4 connected to "high-frequency ground terminal GND" (*third switch circuit connected to ground*), and (ii) capacitor C7 (*third capacitor*) *connected between* MOSFET T4 and high-frequency signal terminal RF_2. *Id.*; EX-1003, ¶158-159.

vii. [1.6.1] and a second shunt arm connected to the second switch circuit and the receive node, [1.6.2] the second shunt arm including a fourth switch circuit connected to ground.

Seshimo discloses, "in a state in which the inverter circuit IN1 is shared", another of "four units" of FIG. 3 "**shunt** SPDT switch" includes "MOSFET T3, capacitors C5 and C6…", and during, *e.g.*, transmit (*see* [1.1]-[1.2]) operations:

> A…Vcont of 0 V is input to… inverter circuit IN1, **turning OFF**… **MOSFETs T1**, T4. A… Vcc of 3 V is output from… inverter circuit IN1,

> **turning ON**… **MOSFETs T2, T3**. **As a result, a cutoff state is established between… terminals RF_1 and RF_COM**, and a conductive state is established between the terminals… RF_2 and RF_COM.

EX-1007, [0054]-[0056], [0065]-[0066], [0060], [0064], [0069]-[0071]; *see* [1.5.1]-[1.5.2]; EX-1003, ¶160.

Accordingly, as illustrated in Annotated FIG. 3, POSITAs understood Seshimo discloses *a second shunt arm* connected to MOSFET T1 (*second switch circuit*) and high-frequency signal terminal RF_1 (*receive node*), and including (i) MOSFET T3 connected to high-frequency ground terminal GND (*fourth switch circuit connected to ground*), and (ii) capacitor C5 (*fourth capacitor*) *connected between* MOSFET T3 and high-frequency signal terminal RF_1. *Id*.; EX-1003, ¶161-162.

b. Claim 2

i. The switch system of claim 1 wherein at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

Seshimo discloses this limitation to POSITAs. EX-1003, ¶163. As discussed in [1.3]-[1.4], Seshimo discloses, in FIG. 3 SPDT switch (*the switch*) as shown in Annotated FIG. 3, positioning (i) capacitor C3 (*first capacitor*) between common terminal RF_COM and Tx series MOSFET T2, and (ii) capacitor C2 (*second capacitor*) between common terminal RF_COM and Rx series MOSFET T1. Seshimo's disclosure is identical to the '194 Patent's disclosed positioning in FIG. 9 SPDT switch 250, (i)

capacitor C1 between antenna node 252 and Tx series switch circuit 120/140, and (ii) capacitor C2 between antenna node 252 and Rx series switch circuit 120/140. EX-1007, [0054]-[0056]; §V.A (EX-1001, 9:25-38, FIG. 9); §V.B; EX-1003, ¶¶163-164.

Seshimo also discloses the importance of selecting (i) substrates (*e.g.*, SOI) and capacitor structures (*e.g.*, MIM) with "excellent high frequency properties", (ii) biasing voltages of the MOSFETs when in "ON" and "OFF" states, and (iii) the FIG. 3 SPDT switch configuration (with identical C3, C2, C7 and C5 capacitor positioning as the '194 Patent FIG. 9 C1, C2, C3 and C4 positioning) instead of the FIG. 4 SPDT switch configuration (with shared capacitor C3 between RF_COM and MOSFET T2 and MOSFET T1, and no top capacitor in either the first shunt arm or the second shunt arm), in order to be able to "provide a semiconductor switching circuit capable of improving the maximum permissible input power while suppressing an increase in ON-resistance" (that, without suppression, would "lead to an increase in insertion loss" and "deterioration in isolation"). EX-1007, FIG. 3 ([0054]-[0056], [0064]-[0071]), FIG. 4 ([0072]-[0073], [0077], [0079]-[0081]), [0082], [0084], [0087], [0001], [0004]-[0005], [0007]; EX-1003, ¶165.

Unsurprisingly, just like the '194 Patent, given the fundamental, frequency-dependent impedance characteristic of capacitors—capacitors allow high frequencies to pass through (essentially acting as short circuits) while blocking low frequencies (essentially acting as open circuits)—outside of specifying the identical arrangement of

capacitor C3 (*first capacitor*) and capacitor C2 (*second capacitor*) in FIG. 3 SPDT switch as the Applicant's relied-on arrangement, Seshimo leaves the particular capacitor value implementation details to design choices of POSITAs. *Id.*

Moreover, given this fundamental, frequency-dependent impedance characteristic of capacitors, the typical (picofarad) capacitor values selected for RF switches in Seshimo's disclosed use cases, and the known solution—having "the switch see[] an open circuit at the blocker frequencies"—to the well-known low-frequency, "out-of-band blocker" signal problem in non-linear RF switches, POSITAs understood Seshimo's implementation of capacitor C3 and capacitor C2 as being high-pass filters "configured to inhibit a low-frequency blocker signal from mixing with a fundamental frequency signal in the RF switch." *Id.*, §V.F.1 (EX-1012, 231-234, 175-176; EX-1027, 82-83, 50; EX-1014, 20, 30, 29-32, 36-37, 39-40, 42, FIGS. 1.52-1.55, 1.56(A); EX-1043, 128-129, 137-139, 236-238, FIGS. 5-17(A), 8-17(B), 8-17(D), 8-18(B), 8-18(D); EX-1011, 2615-2618, FIG. 9A; EX-1024, 3-4; EX-1026, [0049]; EX-1031, 8-9, FIG. 13; EX-1010, [0040], EX-1044, 1-2; EX-1029, 36-39; EX-1032, 1-2; EX-1033, 1; EX-1042, 96, 172, 180, 227, 275, 286; EX-1017, [0025]; EX-1049, p.3); §V.F.2 (EX-1039, FIG. 5, 2-6, 8-12 (*citing* EX-1040, 3-6, FIGS. 3-4); EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1045, 1); EX-1003, ¶166-167.

To the extent PO asserts Seshimo does not expressly disclose capacitor C3 and/or capacitor C2 as being configured as claimed, with the FIG. 3 SPDT switch components

arranged as shown in Annotated FIG. 3, and opposing series and shunt switches placed in ON and OFF states depending on the transmit or receive mode of such switch as disclosed by Seshimo, POSITAs understood these capacitors' inhibition of low-frequency blocker signals from mixing with fundamental frequency signals in FIG. 3 SPDT switch to merely be a matter of design choice. *Id.*; EX-1003, ¶168.

As discussed in the State of the Art section, because capacitors C3 and C2 are fundamentally frequency-dependent circuit elements (with decreasing impedance with increasing frequency), POSITAs understood that tuning the resulting high-pass filters, *i.e.*, setting the frequency range above which these capacitors permit frequencies (*e.g.* the desired RF frequency) to pass essentially unimpeded, and below which (*e.g.*, the "-3dB breakpoint") they impede lower frequencies (*e.g.*, low-frequency, out-of-band-blocker signals), is simply a matter of picking the size capacitor that yields the desired pass/inhibit thresholds within the practical size constraints for the RF device (*e.g.*, "PHS") with a reasonable expectation of success. *Id.*; *see also* §V.F.1 (EX-1009, FIG. 2, [0083]-[0084]; EX-1035, 5; EX-1032, FIG. 1; EX-1026, FIG. 2, [0002], [0040], [0049], [0051], [0063]; EX-1042, 294, 298, 308, 312; EX-1049, p.3); EX-1003, ¶169. Filtering RF_COM-picked-up, low-frequency, out-of-band-blocker signals was a well-known problem in RF radios, with a well-known solution (*i.e.*, a series capacitor sized to yield the desired frequency-dependent response as a high-pass filter within the practical size constraints for the RF device). *Id.*; EX-1003, ¶170.

Accordingly, POSITAs would have been motivated to select appropriately-sized capacitors C3 and C2 to pass (with very low impedance) the high frequencies-of-interest (*e.g.*, 1.88-1.93GHz associated with PHS ([1.0])), while impeding low, out-of-band frequencies, within the practical size constraints of such radios, to achieve the known and predictable benefits of improved switch performance (including improved IMD performance) with a reasonable expectation of success given that this involves nothing more than the conventional and routine use of Seshimo's capacitors. *Id.*; *see also* EX-1047, 1; EX-1048, 4, 9-11; EX-1003, ¶171.

c. Claim 3

i. [3.1] The switch system of claim 1 wherein the first shunt arm includes a third capacitor connected between the third switch circuit and the transmit node, and

As discussed in [1.5.1]-[1.5.2], as illustrated in Annotated Figure 3, Seshimo discloses the first shunt arm of SPDT switch (FIG. 3) includes capacitor C7 (*third capacitor*) *connected between* MOSFET T4 (*third switch circuit*) and high-frequency signal terminal RF_2 (*transmit node*). EX-1007, [0055]-[0057]; EX-1003, ¶172.

ii. [3.2] the second shunt arm includes a fourth capacitor connected between the fourth switch circuit and the receive node.

As discussed in [1.6.1]-[1.6.2], as illustrated in Annotated Figure 3, Seshimo discloses the second shunt arm of SPDT switch (FIG. 3) includes capacitor C5 (*fourth*

capacitor) *connected between* MOSFET T3 (*fourth switch circuit*) and high-frequency signal terminal RF_1 (*receive node*). EX-1007, [0055]-[0057]; EX-1003, ¶173.

d. Claim 4

i. [4.0] A radio-frequency (RF) switch system comprising: [4.1] a first switch circuit connected between an antenna node and a transmit node; [4.2] a second switch circuit connected between the antenna node and a receive node; [4.3] a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node; [4.4] a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node; [4.5.1] a first shunt arm connected to the first switch circuit and the transmit node, [4.5.2] the first shunt arm including a third switch circuit connected to ground and a third capacitor connected between the third switch circuit and the transmit node.

Seshimo discloses these limitations for the reasons discussed regarding [1.0]-[1.5.2], [3.1].

e. Claim 5

i. [5.0] A method for fabricating a semiconductor die, the method comprising:

To the extent the preamble is limiting, Seshimo discloses a method for fabricating a semiconductor die, including forming components of the disclosed "high-frequency semiconductor switching circuit" (*e.g.*, FIG. 3 SPDT switch) on a semiconductor substrate of a semiconductor die to POSITAs. Seshimo discloses "[t]he present invention… is particularly suitable for a high-frequency semiconductor switching

circuit including a MOSFET formed on a silicon substrate", "the use of SOI is… effective in the present invention", the SPDT components and control circuits all "may be configured as CMOS circuits and integrated on the same semiconductor substrate", and well-known benefits of "develop[ing] high-frequency semiconductor switching circuits using CMOS processes", *e.g.*, "a CMOS switch can be integrated into another CMOS RF IC." EX-1007, [0001], [0003], [0007], [0054], [0084], [0088]. Accordingly, POSITAs understood Seshimo discloses providing a semiconductor substrate, and forming the SPDT switch components on the semiconductor substrate to fabricate a semiconductor die, where, in some embodiments, the semiconductor die is a SOI die in which the SPDT switch components would be formed on an insulator layer. *Id.*; EX-1003, ¶¶181-183.

To the extent PO asserts Seshimo does not explicitly disclose forming SPDT switch components on the semiconductor substrate to fabricate a semiconductor die, it would have been obvious to POSITAs to do so, as this was the well-known and widely-implemented approach to provide a stable foundation for fabrication of components of high-power, semiconductor-based, transmit/receive switches on a stable foundation, and in order to make manufacturing, testing and production of ICs (including such switches and related circuits (*e.g.*, LNAs)) easier and less costly. *Id.*; §V.F.3 (EX-1018, 4:27-41; EX-1010, [0009], [0013], FIG. 3A, [0046]; EX-1019, [0001], [0004], FIG. 1; EX-1039, 9-10, FIG. 12; EX-1020, FIGS. 1, 4; EX-1009, [0004]-[0005], [0058], FIG. 2; EX-1022,

FIG. 7, [0046]-[0050]; EX-1024, 1, 3-4, FIG. 8; EX-1029, FIGS. 1-2, 35-36, 40; EX-1028, 2-3, FIGS. 2, 4, 5; EX-1021, 2-3, FIGS. 1-2, 4-5; EX-1019, [0001], [0004], FIG. 1; EX-1011, 2613-2617, FIGS. 1-2, 4-6, 8; EX-1036, 1-2); EX-1003, ¶184.

ii. [5.1] providing a semiconductor substrate; [5.2] forming a first switch circuit on the semiconductor substrate so as to be connected between an antenna node and a transmit node; [5.3] forming a second switch circuit on the semiconductor substrate so as to be connected between the antenna node and a receive node;

Seshimo discloses these limitations for the reasons discussed regarding [1.0]-[1.2], [5.0].

i. [5.4] forming a first capacitor on the semiconductor substrate so as to be connected in series with the first switch circuit between the first switch circuit and the antenna node;

Seshimo discloses this limitation for the reasons discussed regarding [1.3], [5.0]. To the extent PO asserts that Seshimo does not explicitly disclose forming "capacitor C3" (and, *e.g.*, "capacitor C2") on the same semiconductor substrate of the same semiconductor die as the other components (*e.g.*, SOI FETs) of FIG. 3 SPDT switch, as discussed in the State of the Art sections, POSITAs would have been motivated to do so as a mere design choice to achieve known and predictable benefits, including making manufacturing, testing, and production of such switch (and ICs incorporating the same) easier and less costly, with a reasonable expectation of success, including because low

capacitance value (*e.g.*, picofarad) capacitors are small in size and typically used in RF switches since, as was well-known to POSITAs, they would pass (with very low impedance) the high frequencies-of-interest (*e.g.*, 1.88-1.93GHz associated with "PHS") while impeding low, out-of-band-blocker frequencies. *Id.*; §V.F.3 (EX-1034, FIG. 2; EX-1035, 2-5; EX-1023, 10:13-17, FIG. 5; EX-1011, 2616-2617, FIG. 4; EX-1029, FIGS. 1-2, pp.35-36, 40; EX-1022, [0028], FIG. 7, [0046]-[0050]; EX-1010, [0009], [0013], FIG. 3A, [0046]); §V.F.1 (EX-1012, 231-234, 175-176; EX-1027, 82-83, 50; EX-1014, 29-32, 36-37, 42; EX-1043, 128-129, 137-139, 236-238; EX-1032, 1-2; EX-1033, 1; EX-1011, 2615-2618; EX-1026, [0049]; EX-1024, 3-4; EX-1031, 8-9; EX-1044, 1-2; EX-1010, [0040]; EX-1009, FIG. 2, [0083]-[0084], EX-1035, 5; EX-1042, 96, 172, 180, 227, 275, 286; EX-1029, 36-39; EX-1017, [0025]); §V.F.2 (EX-1024, 1, 3-4; EX-1039, FIG. 5, 2-6, 9-12 (*citing* EX-1040, 3-6, FIGS. 3-4); EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1045, 1; EX-1049, p.3); EX-1047, 1; EX-1048, 4, 9-11; EX-1003 ¶¶188-190.

ii. [5.5] forming a second capacitor on the semiconductor substrate so as to be connected in series with the second switch circuit between the second switch circuit and the antenna node;

Seshimo discloses this limitation for the reasons discussed regarding [1.4], [5.0], [5.4].

iii. [5.6.1] forming a first shunt arm connected to the first switch circuit and the transmit node, [5.6.2] the first

shunt arm including a third switch circuit connected to ground; and [5.7.1] forming a second shunt arm connected to the second switch circuit and the receive node, [5.7.2] the second shunt arm including a fourth switch circuit connected to ground.

Seshimo discloses these limitations for the reasons discussed regarding [1.5.1]-[1.5.2], [1.6.1]-[1.6.2], [5.0].

f. Claim 6

i. The method of claim 5 further comprising forming an insulator layer between the first switch circuit and the semiconductor substrate.

As explained in [5.0], Seshimo discloses FIG. 3 SPDT switch is "a high-frequency semiconductor switching circuit including… MOSFET[s] formed on a silicon substrate", and may include "CMOS switch[es] formed using a SOI… substrate" due to, *e.g.*, their "excellent high frequency properties" and ease of "integrat[ion] into another CMOS RF IC." EX-1007, [0001], [0003], [0007], [0054], [0084], [0088]; EX-1003 ¶196.

Unsurprisingly, Seshimo does not disclose the well-known details of implementing SOI technology to manufacture the "CMOS switch[es] formed using a SOI… substrate" of the FIG. 3 SPDT switch. *Id*. Indeed, as described in the State of the Art section, it was well-known that, in using SOI technology to create ICs, an insulator layer is deposited onto a semiconductor substrate of a semiconductor die, silicon is grown on top of this insulator layer, and then the silicon is patterned and

etched to create the various components of the IC (*e.g.*, MOSFETs, capacitors, etc. of SPDT switch (FIG. 3)). §V.F.3 (EX-1020, FIGS. 1, 4, 8:17-25, 7:12, 7:17-18, 10:5-11, 8:28-29, 1:10-14, 12:27-13:8, FIG. 16; EX-1026, [0030]; EX-1018, 4:27-41, 3:50-54, FIGS. 3-4; EX-1039, 9-10, FIG. 10); EX-1003, ¶197.

Accordingly, POSITAs understood Seshimo's implementation of SOI included forming an insulator layer between SOI MOSFET T2 (*first switch circuit*) and the semiconductor substrate. *Id.*; EX-1007, [0001], [0003], [0007], [0054], [0084], [0088]; EX-1003, ¶198.

To the extent PO asserts Seshimo does not expressly disclose an insulator layer disposed between SOI MOSFET T2 and the semiconductor substrate, it would have been obvious to POSITAs to do so as this was the well-known and widely implemented approach to using the disclosed SOI technology to manufacture "CMOS switch[es] formed using a SOI… substrate" of the "high-frequency semiconductor switching circuit" (*e.g.*, FIG. 3 SPDT switch), with well-known and predictable benefits including, for example, lower cost, higher "thermal conductivity", reduced "degradation in bandwidth associated with the stacking of FET devices", "reduce[d] dielectric losses associated with the silicon substrate", allowing monolithic (same die/chip) integration of SPnT switch and control components and other FEM components, etc. *Id.*; §V.F.3 (EX-1009, [0005]; EX-1018, 4:37-41; EX-1024, 4; EX-1021, 2; EX-1010, [0013]); EX-1003, ¶199.

g. Claim 7

i. [7.0] A radio-frequency (RF) switch module comprising:

To the extent the preamble is limiting, as discussed in [1.0]-[1.1] and [5.0], Seshimo discloses to POSITAs incorporation of a "high-frequency semiconductor switching circuit" (*e.g.*, FIG. 3 SPDT switch) into an RF/wireless device (*e.g.*, PHS), in which such switch would (i) be "used as a transmission/reception changeover switch", (ii) include high-frequency signal terminal RF_2 (*transmit node*), high-frequency signal terminal RF_1 (*receive node*), and common terminal RF_COM (*antenna node*), (iii) have its SPDT components and control circuits "configured as CMOS circuits and integrated on the same semiconductor substrate", and (iv) be "developed… using CMOS processes" so the "CMOS switch can be integrated into another CMOS RF IC." EX-1007, [0029], [0070]-[0071], [0003], [0005], [0007], [0084], [0087]-[0088]; EX-1003, ¶199. POSITAs understood Seshimo's disclosure of FIG. 3 SPDT switch, formed for use as a component incorporated into (*e.g.*, in a packaged RF switch module, FEM, etc.) RF/wireless devices (*e.g.*, "PHS"), to constitute an *RF switch module*. *Id.*; *see* EX-1047, 1; EX-1048, 4, 9-11; EX-1003, ¶200.

Unsurprisingly, Seshimo does not disclose the well-known details of packaging the components of SPDT switch (FIG. 3) for testing, shipment, commercial sale, etc., for such use in such RF/wireless devices. *Id.* Indeed, as discussed in the State of the

Art section, given that the well-known, and widely-implemented approach to package a semiconductor die (or plurality of dies) for testing, shipment, commercial sale, etc. of a SPnT switch, and of any other components that are incorporated into the packaged module (*e.g.*, external capacitors, control circuitry, LNA, etc.), was to mount each separate die (and/or surface-mountable component) on, and electrically connect (*e.g.*, wire-bond) each separate die (and/or surface-mountable component) to, a packaging substrate (*e.g.*, PCB), POSITAs would have been motivated to do so as a mere design choice with a high likelihood of success of achieving well-known benefits, such as making packaging, testing, production, shipment, and commercial sales of packaged products (*e.g.*, RF switch module , FEM, etc.) easier, less costly, and more attractive to customers. *Id*.; §V.F.3 (EX-1008, 1-3; EX-1041, 2; EX-1029, 36-39, Figures 4, 8; EX-1033, 1; EX-1028, 1, 4, Fig. 2; EX-1038, [0010], [0027], [0029], [0030]-[0032], [0036]-[0037], [0045], FIGS. 2-3; EX-1042, 80-82, 95-97, 105-106, 171-172, 180-181, 192-193, 210, 221-222, 226-227, 237-238, 242, 274-275, 285-286, 298-299, 312-313; EX-1021, 1-3; EX-1033, 1, 3, 9-11; EX-1032, 1-2; EX-1022, [0028]; EX-1036, 1-2); EX-1003, ¶201.

ii. [7.1] a packaging substrate configured to receive a plurality of components;

POSITAs reading Seshimo would have been motivated to implement this limitation as discussed in [1.0]-[1.1], [5.0], [7.0].

iii. [7.2] a semiconductor die mounted on the packaging substrate,

Seshimo discloses this limitation for the reasons discussed regarding [5.0], [7.0].

iv. [7.3.1] the die including a first switch circuit connected between an antenna node and a transmit node and [7.3.2] a second switch circuit connected between the antenna node and a receive node;

Seshimo discloses these limitations for the reasons discussed regarding [1.1]-[1.2], [5.0], [7.0].

v. [7.4] a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node; [7.5] a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node; [7.6.1] a first shunt arm connected to the first switch circuit and the transmit node, [7.6.2] the first shunt arm including a third switch circuit connected to ground; and [7.7.1] a second shunt arm connected to the second switch circuit and the receive node, [7.7.2] the second shunt arm including a fourth switch circuit connected to ground.

Seshimo discloses these limitations for the reasons discussed regarding [1.3]-[1.6.2].

h. <u>Claim 8</u>

i. The switch module of claim 7 wherein at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

Seshimo discloses this limitation for the reasons discussed regarding Claim 2.

i. Claim 9

i. The switch module of claim 7 wherein the first capacitor is part of the same semiconductor die as the first switch circuit.

Seshimo discloses this limitation for the reasons discussed regarding [7.0], [5.4].

j. Claim 10

i. The switch module of claim 7 wherein the first capacitor is part of a second die mounted on the packaging substrate.

As the '194 Patent itself acknowledges, and as discussed in [7.0], [5.0], and [5.4], POSITAs understood this limitation to be obvious as a mere (and well-known) design choice—selecting between forming Seshimo's capacitor C3 (and the other capacitors) on the same die as the MOSFETs, or on a separate capacitor die (*second capacitor die mounted on the packaging substrate*), or mounting them as surface-mountable components on the same packaging substrate on which the MOSFET-die is mounted (claim 11)—based on, for example, size/space constraints, the RF application, the fundamental frequency values, and blocking frequency values, associated with such application, performance requirements, etc., and with well-known benefits and tradeoffs. *See* [7.0], [5.0], [5.4], EX-1007, [0054]-[0056], Annotated FIG. 3, [0001], [0003], [0005], [0007], [0029], [0070]-[0071], [0084]-[0087]; §V.A (EX-1001, 9:45-49, 2:15-21, 9:62-10:11, FIGS. 11A-11D); §V.F.3 (EX-1035, 2-5; EX-1034, FIG. 2; EX-1032, 1-2; EX-1033, 1; EX-1023, 10:13-17, 8:29-37, 5:59-6:21, FIG. 5; EX-1011,

2616-2617, FIGS. 4, 8; EX-1029, 35-36, 40, Figures 1-2); §V.F.1 (EX-1014, 36-37; EX-1043, 137-139; EX-1026, [0049], [0063]; EX-1011, 2615-2618; EX-1009, FIG. 2, [0083]-[0084]; EX-1024, 3; EX-1031, 8-9, EX-1032, FIG. 1; EX-1042, 294, 298, 308, 312); EX-1003 ¶214.

k. Claim 11

i. The switch module of claim 7 wherein the first capacitor is disposed at a location outside of the semiconductor die.

Seshimo discloses this limitation for the reasons discussed regarding Claim 10.

VIII. DISCRETIONARY DENIAL WOULD BE INAPPROPRIATE

A. Discretionary denial under the *Fintiv* factors is not appropriate.

Under *Fintiv*, the Board takes a holistic view of whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel district court proceeding. *Apple Inc. v. Fintiv, Inc*., IPR2020-00019, Paper 11, at 6. Pursuant to the Director's June 2022 Guidance Memo:

> The plain language of the *Fintiv* factors… does **not** apply to parallel U.S. International Trade Commission (ITC) proceedings, as the ITC lacks authority to invalidate a patent and the ITC's invalidity rulings are not binding on the Office or on district courts … For the foregoing reasons, the PTAB **no longer** discretionarily denies petitions based on applying *Fintiv* to a parallel ITC proceeding. This memorandum memorializes that practice. The PTAB will **not** discretionarily deny petitions based on applying ***Fintiv*** to a parallel ITC proceeding.

K. Vidal, *Interim Procedure For Discretionary Denials in AIA Post-Grant Proceedings With Parallel District Court Litigation*, June 21, 2022. Here, the district court case was filed in C.D. California on May 6, 2024, a co-pending ITC proceeding was filed on July 16, 2024 and investigation instituted on August 16, 2024, and, on September 13, 2024, pursuant to 28 U.S.C. §1659, the district court granted Petitioner's motion to stay the district court proceeding until the ITC determination becomes final.

B. Discretionary denial under 35 U.S.C. §325(d) is not appropriate.

Petitioner is unaware of any authority holding *Advanced Bionics* to be satisfied where (like here) the prosecution history lacks discussion of any reference relied upon in this petition. In such situations, the Board routinely does not decline institution on Section 325 grounds. Moreover, the challenges in this petition are non-cumulative because the prior art presented describes the claim limitations that were added to gain allowance (including those acknowledged by the Patent/Applicant to be well-known). *See* §V.A-§VII.B.2.

IX. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Party-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner certifies that the real party-in-interest in this Petition is Kangxi Communications Technologies (Shanghai) Co., Ltd.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

1. Judicial Matters

As of the filing date of this Petition and to the best knowledge of Petitioner, the '194 Patent is involved in the following litigation and investigation:

Case Heading	Number	Tribunal	Date
Skyworks Solutions, Inc. v. Kangxi Communication Technologies Shanghai Co., Ltd et al.	CDCA-8-24-cv-00974	CDCA	May 6, 2024
Wireless Front-End Modules, Devices Containing the Same, and Components Thereof	Inv. No. 337-TA-3762	ITC	July 17, 2024

2. Administrative Matters

As of this Petition's filing date and to the best knowledge of Petitioner, the '194 Patent has not been subject to any *inter partes* reviews, reissues, or reexaminations.

3. Related Patents

To the best knowledge of Petitioner, U.S. patent applications and U.S. patents related to the '194 Patent include U.S. Patent No. 9,450,579.

C. Lead/Back-up Counsel (37 C.F.R. § 42.8(b)(3)):

Petitioner provides the following designation of counsel:

Lead Counsel: Christopher J. Tyson, USPTO Reg. No. 63,850 DUANE MORRIS LLP, 901 New York Ave. NW, Suite 700 East Washington, DC 20001-4795 P: 202-776-7851; F: 202-478-2620; Email: CJTyson@duanemorris.com
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In a concurrently filed Power of Attorney, Petitioner has granted Power of Attorney to Practitioners at Duane Morris LLP.

D. Notice of Service Information (37 C.F.R. § 42.8(b)(4)):

Please direct all correspondence to lead and back-up counsel at the above addresses. Petitioner consents to electronic service at the email addresses above.

X. CONCLUSION

Petitioner requests the Board institute IPR and cancel the Challenged Claims.

Respectfully submitted,

DUANE MORRIS LLP

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ATTORNEY FOR PETITIONER

Dated: November 12, 2024

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. §42.24 *et seq*., the undersigned certifies that this document complies with the type-volume limitations. This document contains 13878 words as calculated by the "Word Count" feature of Microsoft Word 2016, the word processing program used to create it. Pursuant to 37 C.F.R. § 42.24(d), this word count excludes the table of contents, table of authorities, mandatory notices under § 42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing.

Dated: November 12, 2024

/*Christopher J. Tyson*/
Christopher J. Tyson
Lead Counsel for Petitioner
Registration No. 63,850

CERTIFICATION OF SERVICE ON PATENT OWNER

Pursuant to 37 C.F.R. §§42.6(e), 42.8(b)(4) and 42.105, the undersigned certifies that on November 12, 2024, a complete and entire copy of this Petition for *Inter Partes* Review of U.S. Patent 9,148,194 and all supporting exhibits were served via Federal Express, postage prepaid, to the correspondence address of record for the '194 Patent:

Date of service	November 12, 2024
Manner of service	FEDERAL EXPRESS
Documents served	Petition for *Inter Partes* Review Under 35 U.S.C. § 312 and 37 C.F.R. § 42.104 of U.S. 9,148,194; Petitioner's Exhibit List; All Exhibits; Petitioner's Power of Attorney.
Persons served	James Chang Chang and Hale LLP 4199 Campus Drive Suite 550, #115 Irvine, CA 92612 James M. Dowd Wilmer Cutler Hale Pickering and Dorr LLP 350 South Grand Avenue Suite 2400 Los Angeles, CA 90071

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