PTO/SB/47 (03-09)
Approved for use through 07/31/2018. OMB 0651-0016
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

- OR -

Fax to:
571-273-6500

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below**: If you have a Customer Number to represent the fee address. **When to check the second box below**: If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☒ Customer Number: 96879

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
9,450,579	14/833,076

Completed by (check one):

☐ Applicant/Inventor

☒ Attorney or Agent of record 52,718 (Reg. No.)

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☐ Assignee recorded at Reel Frame

/James W. Chang/
Signature

James W. Chang
Typed or printed name

(949) 336-1454
Requester's telephone number

July 16, 2018
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

☐ * Total of forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1. 11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313- 1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	33189034
Application Number:	14833076
International Application Number:	
Confirmation Number:	3042
Title of Invention:	RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION
First Named Inventor/Applicant Name:	Anuj Madan
Customer Number:	115870
Filer:	James W. Chang
Filer Authorized By:	
Attorney Docket Number:	75900-50031D1
Receipt Date:	16-JUL-2018
Filing Date:	22-AUG-2015
Time Stamp:	15:59:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Change of Address	2018-07-16_Fee-Address_75900-50031D1.pdf	133095 db0a0eb6da3f1a32d279b1c162c13b25fd2b5827	no	2

Warnings:

Information:	
Total Files Size (in bytes):	133095

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/833,076	09/20/2016	9450579	75900-50031D1	3042

115870 7590 08/31/2016

Chang & Hale LLP
4199 Campus Drive
Suite 550, #115
Irvine, CA 92612

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Anuj Madan, Cambridge, MA;
SKYWORKS SOLUTIONS, INC., Woburn, MA
Fikret Altunkilic, North Andover, MA;
Guillaume Alexandre Blin, Carlisle, MA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

115870 7590 05/27/2016
Fernando Hale & Chang LLP
4199 Campus Drive
Suite 550, #115
Irvine, CA 92612

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/833,076	08/22/2015	Anuj Madan	75900-50031D1	3042

TITLE OF INVENTION: RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	08/29/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, TUAN HOANG	2647	455-083000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 Chang & Hale LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Skyworks Solutions, Inc.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Woburn, MA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
☐ A check is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached.
☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Alan T. Hale/ Date 2016-08-24
Typed or printed name Alan T. Hale Registration No. 68,226

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

EX-1037
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.
0006

Electronic Patent Application Fee Transmittal

Application Number:	14833076
Filing Date:	22-Aug-2015
Title of Invention:	RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION
First Named Inventor/Applicant Name:	Anuj Madan
Filer:	Alan Troy Hale
Attorney Docket Number:	75900-50031D1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**960**

Electronic Acknowledgement Receipt	
EFS ID:	26735661
Application Number:	14833076
International Application Number:	
Confirmation Number:	3042
Title of Invention:	RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION
First Named Inventor/Applicant Name:	Anuj Madan
Customer Number:	115870
Filer:	Alan Troy Hale
Filer Authorized By:	
Attorney Docket Number:	75900-50031D1
Receipt Date:	24-AUG-2016
Filing Date:	22-AUG-2015
Time Stamp:	14:55:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$960
RAM confirmation Number	082516INTEFSW14564700
Deposit Account	0585
Authorized User	Alan Hale
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	2016-08-24_IssueFeePaid.pdf	161932 5d5f7f4e4147fc4351f8eeb9955bb96cdc90b90e	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30467 27a24e59b8c0d4ec65df1fb6788eb7c5b3bb259b	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	192399		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

115870 7590 05/27/2016

Fernando Hale & Chang LLP
4199 Campus Drive
Suite 550, #115
Irvine, CA 92612

EXAMINER
NGUYEN, TUAN HOANG

ART UNIT	PAPER NUMBER
2647	

DATE MAILED: 05/27/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/833,076	08/22/2015	Anuj Madan	75900-50031D1	3042

TITLE OF INVENTION: RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	08/29/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

115870 7590 05/27/2016
Fernando Hale & Chang LLP
4199 Campus Drive
Suite 550, #115
Irvine, CA 92612

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/833,076	08/22/2015	Anuj Madan	75900-50031D1	3042

TITLE OF INVENTION: RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	08/29/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, TUAN HOANG	2647	455-083000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
❑ Issue Fee
❑ Publication Fee (No small entity discount permitted)
❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
❑ A check is enclosed.
❑ Payment by credit card. Form PTO-2038 is attached.
❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
❑ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____
Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

EX-1037
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.
0012

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/833,076	08/22/2015	Anuj Madan	75900-50031D1	3042

115870 7590 05/27/2016

Fernando Hale & Chang LLP
4199 Campus Drive
Suite 550, #115
Irvine, CA 92612

EXAMINER	
NGUYEN, TUAN HOANG	
ART UNIT	PAPER NUMBER
2647	

DATE MAILED: 05/27/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

EX-1037
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.
0013

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/833,076	Applicant(s) MADAN ET AL.	
	Examiner TUAN H. NGUYEN	Art Unit 2647	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *04/04/2016*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-6 and 9-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/Tuan H. Nguyen/
Primary Examiner
Art Unit 2647

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

1. The applicant's remarks, filed on 04/04/2016, have been carefully reviewed with updated search. Claims 1-6 and 9-20 are allowed over the prior art record. Claims 7 and 8 are canceled.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

2. Any response to this action should be mailed to:

Mail Stop_____ (Explanation, e.g., Amendment or After-final, etc.)

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Facsimile responses should be faxed to:

(571) 273-8300

Hand-delivered responses should be brought to:

Customer Service Window

Randolph Building

401 Dulany Street

Alexandria, VA 22313

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Nguyen whose telephone number is (571) 272-8329. The examiner can normally be reached on 8:00Am - 5:00Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Maung Nay A. can be reached on (571) 272-7882. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Tuan H. Nguyen/
Primary Examiner
Art Unit 2647

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14833076	MADAN ET AL.
	Examiner	Art Unit
	TUAN H NGUYEN	2647

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/28/2015	05/16/2016							
1	1	✓	=							
2	2	✓	=							
3	3	✓	=							
4	4	✓	=							
5	5	✓	=							
6	6	✓	=							
	7	✓	-							
	8	✓	-							
7	9	✓	=							
8	10	✓	=							
9	11	✓	=							
10	12	✓	=							
11	13	✓	=							
12	14	✓	=							
13	15	✓	=							
14	16	✓	=							
15	17	✓	=							
16	18	✓	=							
17	19	✓	=							
18	20	✓	=							

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14833076	MADAN ET AL.
	Examiner	**Art Unit**
	TUAN H NGUYEN	2647

CPC							
Symbol						**Type**	**Version**
H03K		17	/	687		F	2013-01-01
H04B		1	/	44		I	2013-01-01
H04B		1	/	48		I	2013-01-01
H03K		17	/	693		I	2013-01-01
H03K		2217	/	0018		A	2013-01-01
H03K		2217	/	0054		A	2013-01-01
H01L		21	/	84		I	2013-01-01
H01L		27	/	0629		I	2013-01-01
H01L		27	/	1203		I	2013-01-01
			/				
			/				
			/				
			/				
			/				
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CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 18	
/TUAN H NGUYEN/ Primary Examiner.Art Unit 2647 (Primary Examiner)	05/16/2016 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

U.S. Patent and Trademark Office — Part of Paper No. 20160516

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14833076	MADAN ET AL.
	Examiner	**Art Unit**
	TUAN H NGUYEN	2647

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
455	83	H	0	4	B	1 / 44 (2006.01.01)						
CROSS REFERENCE(S)												
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											

NONE (Assistant Examiner) (Date)	**Total Claims Allowed:** 18	
/TUAN H NGUYEN/ Primary Examiner.Art Unit 2647 (Primary Examiner)	05/16/2016 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

U.S. Patent and Trademark Office

Part of Paper No. 20160516

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14833076	MADAN ET AL.
	Examiner	**Art Unit**
	TUAN H NGUYEN	2647

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	15	17												
2	2	16	18												
3	3	17	19												
4	4	18	20												
5	5														
6	6														
	7														
	8														
7	9														
8	10														
9	11														
10	12														
11	13														
12	14														
13	15														
14	16														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 18	
/TUAN H NGUYEN/ Primary Examiner.Art Unit 2647 (Primary Examiner)	05/16/2016 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	62969	semiconductor$1 near3 die	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:07
L2	593168	semiconductor$1 near3 substrate	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:08
L3	27463	1 and L2	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:08
L4	6464	(stack$3 near3 (field adj2 effect$3 adj2 transistor$1) FET) near3 (connect$3 coupl$3) near3 ser$3	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:24
L5	5843	capacitor$1 near3 form$3 near3 semiconductor$1 near3 substrate	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:45
L6	1587	switch$3 near3 form$3 near3 semiconductor$1 near3 substrate	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:45
L7	100	L5 and L6	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:45
L8	9	4 and L7	US-PGPUB; USPAT	OR	ON	2016/05/16 14:45
L9	96	2 and L7	US-PGPUB; USPAT	OR	ON	2016/05/16 14:46
L10	23297	(H04B1/44 OR H04B1/48 OR H04B15/005 OR H04B15/00 OR H04B15/02 OR H04B1/10 OR H04B1/04 OR H04B7/0602 OR H03H19/004 OR H03H2210/025).CPC.	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:46
L11	3	9 and L10	US-PGPUB; USPAT	OR	ON	2016/05/16 14:46

L12	3	(shunt adj2 arm) same (semiconductor$1 near3 substrate)	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:47
L13	1687	(shunt adj2 arm)	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:48
L14	7	7 and 13	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:48
L15	33	Anuj near3 Madan.in.	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:48
L16	35	Fikret near3 Altunkilic.in.	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:49
L17	37	Guillaume near3 Alexandre near3 Blin.in.	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:49
L18	10	3 and 7	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:51
L19	6	15 and 18	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:51
L20	7	16 and 18	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:51
L21	6	17 and 18	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 14:51
L22	4	(capacitor$1 near3 form$3 near3 semiconductor$1 near3 substrate) same ((connect$3 coupl$3) near3 ser$3) same (switch$3 near3 circuit$3)	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2016/05/16 15:10
S2	5745	capacitor$1 near3 form$3 near3 semiconductor$1 near3 substrate	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:21

S3	1538	switch$3 near3 form$3 near3 semiconductor$1 near3 substrate	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:21
S4	97	S2 and S3	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:21
S6	22620	(H04B1/44 OR H04B1/48 OR H04B15/005 OR H04B15/00 OR H04B15/02 OR H04B1/10 OR H04B1/04 OR H04B7/0602 OR H03H19/004 OR H03H2210/025).CPC.	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:47
S7	3	S4 and S6	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:47
S14	26464	((radio adj2 frequenc$3) RF) adj3 switch$3	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:48
S15	8	S4 and S14	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:48
S16	29	Anuj near3 Madan.in.	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:48
S17	5	S4 and S16	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:48
S18	28	Fikret near3 Altunkilic.in.	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:48
S19	6	S4 and S18	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:48
S20	31	Guillaume near3 Alexandre near3 Blin.in.	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:48
S21	5	S4 and S20	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:48

S22	1342	(reduc$3 decreas$3 lower) near3 intermodulat$3 near3 distort$3	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:19
S23	5745	capacitor$1 near3 form$3 near3 semiconductor$1 near3 substrate	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:19
S24	1538	switch$3 near3 form$3 near3 semiconductor$1 near3 substrate	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:19
S25	97	S23 and S24	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:19
S26	1	S22 and S25	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:19
S27	4	S22 and S24	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:20
S28	6292	((stack$3 near3 field adj2 effect$3 adj2 transistor$1) FET) near3 (connect$3 coupl$3) near3 ser$3	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:42
S29	8	S25 and S28	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:42
S30	17	S23 and S28	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:51
S31	41	S24 and S28	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:51
S32	7756	capacit$4 near3 (connect$3 coupl$3) near3 antenna$3	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:53
S33	2	S31 and S32	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:53

S34	24	S31 and ((transmi$6 receiv$3 transceiv$3) near3 (device$1 unit$1 module$1 apparatus))	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 14:45
S35	333011	((radio adj2 frequenc$3) RF) near3 signal$1	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 14:47
S36	19	S34 and S35	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 14:47
S37	3450708	((transmi$6 receiv$3 transceiv$3) near3 (device$1 unit$1 module$1 apparatus))	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 15:16
S38	202701	S35 and S37	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 15:16
S39	6	S25 and S38	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 15:17
S40	64	S24 and S38	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 15:18
S41	35	S23 and S38	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 15:18
S42	4	S22 and S40	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 15:18
S43	19	S28 and S40	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 16:26
S44	576222	semiconductor$1 near3 substrate	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 16:32
S45	218001	(silicon near3 insulat$3)	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 16:33

S46	13	S31 and S45	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 16:34
S47	78209	((field adj2 effect$3 adj2 transistor$1) FET) same insulat$3	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 16:47
S48	18	S40 and S47	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 16:47
S49	18	S38 and S48	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 16:48
S50	279250	(silicon near3 insulat$3) SOI	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 17:41
S51	592	S28 and S50	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 17:41
S52	175	S37 and S51	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 17:42
S53	10	S24 and S52	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 17:42

5/ 16/ 2016 3:31:13 PM
C:\ Users\ tnguyen90\ Documents\ EAST\ Workspaces\ 14833076.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14833076	MADAN ET AL.
	Examiner	Art Unit
	TUAN H NGUYEN	2647

CPC- SEARCHED		
Symbol	Date	Examiner
H04B1/44.	5/16/2016	T.N

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner
H04B1/48,H04B15/005.	5/16/2016	T.N

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
All searches are on EAST data base.	5/16/2016	T.N
Updated search above.	5/16/2016	T.N

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	See search above.	5/16/2016	T.N

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Skyworks Solutions, Inc.
App. No.	:	14/833,076
Filed	:	August 22, 2015
Title	:	*RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION*
Examiner	:	Tuan H. Nguyen
Art Unit	:	2647
Conf No.	:	3042

RESPONSE TO FINAL OFFICE ACTION DATED JANUARY 4, 2016

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the pending Office Action, the Applicant requests that the above-identified application be considered in view of the following amendments and remarks:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 7 of this paper.

AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions thereof. Changes are shown below in highlighted form, where insertions appear as underlined text (e.g., insertions) while deletions appear as strikethrough text (e.g., ~~deletions~~) or double brackets (e.g., [[~~deletions~~]]).

1. (Currently amended) A semiconductor die comprising:

a semiconductor substrate;

a first switch circuit formed on the semiconductor substrate ~~and including a stack of field-effect transistors (FETs) connected in series~~ connected between an antenna node and a transmit node; [[and]]

a second switch circuit formed on the semiconductor substrate and connected between the antenna node and a receive node;

a first capacitor formed on the semiconductor substrate and connected in series with the first switch circuit between the first switch circuit and the antenna node;

a second~~, the~~ capacitor formed on the semiconductor substrate and connected in series with the second switch circuit between the second switch circuit and the antenna node; and ~~configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch~~

a first shunt arm formed on the semiconductor substrate and connected to the first switch circuit and the transmit node, the first shunt arm including a third switch circuit connected to ground.

2. (Currently amended) The semiconductor die of claim 1 further comprising an insulator layer disposed between the first and second switch circuits ~~stack of FETs~~ and the semiconductor substrate.

3. (Currently amended) The semiconductor die of claim 2 wherein the semiconductor die is a silicon-on-insulator (SOI) die.

4. (Currently amended) The semiconductor die of claim 1 wherein the ~~stack of FETs~~ first shunt arm includes a third capacitor connected in series with the first switch circuit between the first switch circuit and the transmit node ~~silicon-on-insulator (SOI) FETs~~.

5. (Currently amended) The semiconductor die of claim [[1]] 4 further comprising a second shunt arm connected to the second switch circuit and the receive node, the second shunt arm including a fourth switch circuit connected to ground ~~wherein the capacitor is connected to an antenna node~~.

6. (Currently amended) The semiconductor die of claim 5 wherein the second shunt arm includes a fourth capacitor connected in series with the second switch circuit ~~is disposed~~ between the second switch circuit and the receive ~~antenna~~ node.

7. (Cancelled)

8. (Cancelled)

9. (Currently amended) A method for operating a radio-frequency (RF) device, the method comprising:

providing an RF device including a first switch circuit connected between an antenna node and a transmit node, a second switch circuit connected between the antenna node and a receiver node, a first capacitor connected in series with the first switch circuity between the first switch circuit and the antenna node, a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node, and a first shunt arm

connected to the first switch circuit and the transmit node, the first shunt arm including a third switch circuit connected to ground;

controlling an RF switch of the RF device by placing the first switch circuit ~~including a plurality of field-effect transistors (FETs) connected in series between first and second nodes so that the FETs are collectively~~ in an ON state [[or]] and placing the third switch circuit in an OFF state; and

inhibiting a low-frequency blocker signal from mixing with a fundamental-frequency signal in the RF switch using [[a]] the first capacitor ~~connected in series with the switch between the switch and the first node~~.

10. (Currently amended) The method of claim 9 wherein the first switch circuit is ~~plurality of FETs is~~ formed on an insulator layer disposed between the first switch circuit ~~FETs~~ and a semiconductor substrate.

11. (Currently amended) The method of claim 9 wherein the RF switch is a silicon-on-insulator (SOI) switch.

12. (Currently amended) The method of claim 9 wherein the first shunt arm includes a third capacitor connected in series with the first switch circuit between the first switch circuit and the transmit node ~~first node is an antenna node~~.

13. (Currently amended) The method of claim [[9]] 12 wherein the RF device further includes a second shunt arm connected to the second switch circuit and the receive node, the second shunt arm including a fourth switch circuit connected to ground ~~the switch is part of a receive path such that the second node of the switch is an output node for an RF signal received from the antenna~~.

14. (Currently amended) The method of claim [[9]] 13 wherein the second shunt arm includes a fourth capacitor connected in series with the second switch circuit

between the second switch circuit and the receive node ~~switch is part of a transmit path such that the second node of the switch is an input node for an amplified RF signal~~.

15. (Currently amended) A wireless device comprising:

a transceiver configured to process RF signals;

an antenna in communication with the transceiver; and

a switch module interconnected to the antenna and the transceiver and configured to selectively route RF signals to and from the antenna, the switch module including a first switch ~~including a stack of field-effect transistors (FETs)~~ connected between the antenna and a transmit node, a second switch connected between the antenna and a receive node, a first ~~in series, the switch module further including a~~ capacitor connected in series with the first switch between the first switch and the antenna, a second capacitor connected in series with the second switch between the second switch and the antenna, and a first shunt arm connected to the first switch and the transmit node, the first shunt arm including a third switch connected to ground~~, the capacitor configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch~~.

16. (Currently amended) The wireless device of claim 15 wherein the first switch is formed on a silicon-on-insulator (SOI) die of the wireless device.

17. (Currently amended) The wireless device of claim 15 wherein the first capacitor is part of the same semiconductor die as the first switch ~~stack of FETs~~.

18. (Currently amended) The wireless device of claim 15 wherein the first shunt arm includes a third capacitor connected in series with the first switch between the first switch and the transmit node ~~capacitor is disposed between the switch and the antenna~~.

19. (Currently amended) The wireless device of claim [[15]] 18 wherein the switch module further includes a second shunt arm connected to the second switch and the receive node, the second shunt arm including a fourth switch connected to ground ~~switch is part of a receive path, the switch being connected to an output node for an RF signal received from the antenna~~.

20. (Currently amended) The wireless device of claim [[15]] 19 wherein the second shunt arm includes a fourth capacitor connected in series with the second switch between the second switch and the receive node ~~switch is part of a transmit path, the switch being connected to an input node for an amplified RF signal~~.

REMARKS

By way of summary, claims 1-20 were pending in this application. In the present amendment, the Applicant has amended claims 1-6 and 9-20 without prejudice or disclaimer to previously pending versions thereof and cancelled claims 7 and 8. Accordingly, claims 1-6 and 9-20 remain pending for consideration.

Rejection of Claims Under 35 U.S.C. § 101

The Office Action rejected claims 1-20 under 35 U.S.C. § 101 as allegedly being directed to non-statutory subject matter. The Office Action asserts that the claims "are not significantly more than an abstract idea." Office Action at pp. 2-3. However, the Office Action does not present a *prima facie* case of patent ineligibility. The Applicant references the USPTO's "July 2015 Update: Interim Eligibility Guidance Quick Reference Sheet" (Alice Update), which states that:

> a *prima facie* case of eligibility requires the examiner to explain why a claim or claims are unpatentable clearly and specifically, so that applicant has sufficient notice and is able to effectively respond. For subject matter eligibility, the examiner's burden is met by clearly articulating the reason(s) why the claimed invention is not eligible, for example by **providing a reasoned rationale that identifies the judicial exception recited in the claim and why it is considered an exception**, and that **identifies the additional elements in the claim (if any) and explains why they do not amount to significantly more than the exception**.

(emphasis added). The Office Action fails to identify what the abstract idea is (see Alice Update at p. 2, identifying four categories of abstract ideas: (1) "fundamental economic practices," (2) "methods of organizing human activity," (3) "mathematical relationships/formulas," (4) "ideas 'of themselves' that can be performed in the human mind"). The Applicant asserts that the claimed "semiconductor dies," methods for operating radio-frequency devices," and "wireless devices" are not directed to any of the recognized categories of abstract ideas.

Furthermore, the Office Action fails to identify the remaining elements of the claims and explain why they do not amount to significantly more than the abstract idea, whatever it may be. The claims recited switches, transistors, and capacitors in various configurations. The Applicant submits that such elements amount to significantly more than any abstract idea. In addition, the Applicant has amended the claims herein to include additional elements that further clarify the subject matter eligibility of the claims. Therefore, the Applicant asserts that the claims satisfy the requirements of § 101, and requests that the rejection of the claims under § 101 be withdrawn.

Rejection of Claims Under 35 U.S.C. § 103

The Office Action rejected claims 1-6, 9-12 and 15-18 as allegedly being unpatentable over U.S. Pat. No. 7,265,604 (Yasuda) in view of U.S. Pub. No. 2011/0260773 (Granger-Jones). The Applicant respectfully traverse the rejections of the claims for the reasons set forth below.

Independent Claim 1

The Applicant has amended claim 1 herein to recite, among other things:

> a **first switch circuit** formed on the semiconductor substrate **connected between an antenna node and a transmit node**;
> a **second switch circuit** formed on the semiconductor substrate and **connected between the antenna node and a receive node**;
> a **first capacitor** formed on the semiconductor substrate and connected in series with the first switch circuit **between the first switch circuit and the antenna node**;
> a **second capacitor** formed on the semiconductor substrate and connected in series with the second switch circuit **between the second switch circuit and the antenna node**; and
> a **first shunt arm** formed on the semiconductor substrate and connected to the first switch circuit and the transmit node, the first shunt arm including a **third switch circuit connected to ground**.

(emphasis added). The features of amended claim 1 can be understood with reference to Figure 9, which is provided in annotated form below:

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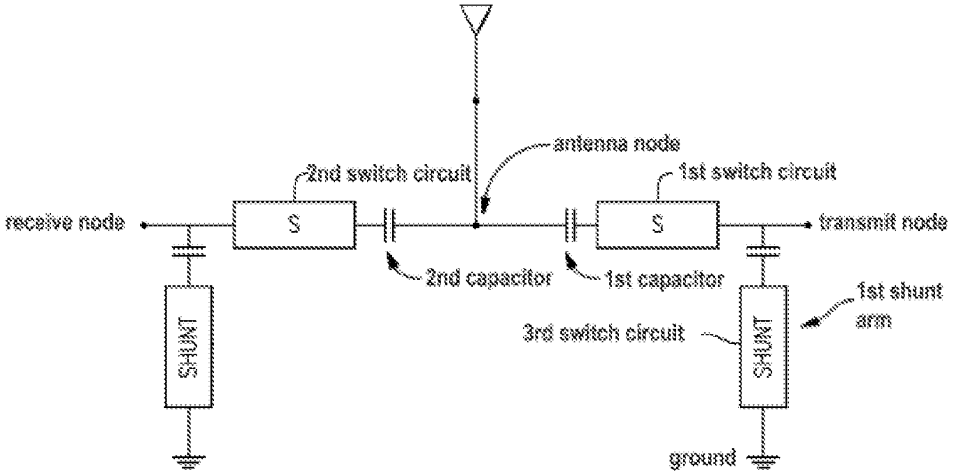
0037



The Applicant submits that the cited references fail to disclose or render obvious the particular configuration claimed in amended claim 1, particularly with respect to the positioning of the first and second capacitors with respect to the antenna node, and further with respect to the shunt arm. Therefore, the Applicant respectfully requests that the rejection of claim 1 be withdrawn.

Independent Claim 9

The Applicant has amended claim 9 to recite, among other things:

> providing an RF device including a **first switch circuit** connected between an antenna node and a transmit node, a **second switch circuit** connected between the antenna node and a receiver node, a **first capacitor** connected in series with the first switch circuity between the first switch circuit and the antenna node, a **second capacitor** connected in series with the second switch circuit between the second switch circuit and the antenna node, and a **first shunt arm** connected to the first switch circuit and the transmit node, the first shunt arm including a **third switch circuit** connected to ground;
>
> controlling an RF switch of the RF device by placing the first switch circuit in an ON state and placing the third switch circuit in an OFF state; and
>
> inhibiting a low-frequency blocker signal from mixing with a fundamental-frequency signal in the RF switch using the first capacitor.

(emphasis added). For at least reasons similar to those discussed above with respect to claim 1, the Applicant submits that the cited references fail to disclose or render obvious the features of independent claim 9. Therefore, the Applicant respectfully requests that the rejection of independent claim 9 be withdrawn.

Independent Claim 15

The Applicant has amended claim 15 to recite, among other things, one or more processors configured to:

> a switch module interconnected to the antenna and the transceiver and configured to selectively route RF signals to and from the antenna, the switch module including a **first switch** connected between the antenna and a transmit node, a **second switch** connected between the antenna and a receive node, a **first capacitor** connected in series with the first switch between the first switch and the antenna, a **second capacitor** connected in series with the second switch between the second switch and the antenna, and a **first shunt arm** connected to the first switch and the transmit node, the first shunt arm including a **third switch** connected to ground.

(emphasis added). For at least reasons similar to those discussed above with respect to claim 1, the Applicant submits that the cited references fail to disclose or render obvious the features of independent claim 15. Therefore, the Applicant respectfully requests that the rejection of independent claim 15 be withdrawn.

Dependent Claims

Claims 2-6, which depend from claim 1; claim 10-14, which depend from claim 9; and claims 16-20, which depend from claim 20, are believed to be patentable for the same reasons articulated above with respect to claims 1, 9 and 15, respectively, and because of the additional features recited therein.

No Disclaimers or Disavowals

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the Applicant is not

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conceding in this application that previously pending claims are not patentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application. The Applicant reserves the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that the Applicant has made any disclaimers or disavowals of any subject matter supported by the present application.

Respectfully submitted,

FERNANDO HALE & CHANG LLP

Dated: April 4, 2016

By: /Alan T. Hale/

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Registration No. 68,226
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(949) 229-8045

Electronic Acknowledgement Receipt

EFS ID:	25386509
Application Number:	14833076
International Application Number:	
Confirmation Number:	3042
Title of Invention:	RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION
First Named Inventor/Applicant Name:	Anuj Madan
Customer Number:	115870
Filer:	Alan Troy Hale
Filer Authorized By:	
Attorney Docket Number:	75900-50031D1
Receipt Date:	04-APR-2016
Filing Date:	22-AUG-2015
Time Stamp:	13:56:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2016-04-04_Amendment.pdf	90366 80c474e02078483df5f4e7f825104152e0ab6768	yes	11

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	11
Warnings:			
Information:			
	Total Files Size (in bytes):	90366	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/833,076	Filing Date 08/22/2015	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	04/04/2016	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/PARTHENIA D. MERRILL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/833,076	08/22/2015	Anuj Madan	75900-50031D1	3042

115870 7590 01/04/2016

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EXAMINER	
NGUYEN, TUAN HOANG	

ART UNIT	PAPER NUMBER
2647	

NOTIFICATION DATE	DELIVERY MODE
01/04/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mail@fhcip.com

Office Action Summary	Application No. 14/833,076	Applicant(s) MADAN ET AL.	
	Examiner TUAN H. NGUYEN	Art Unit 2647	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/22/2015*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *08/22/2015* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 08/22/2015 has been considered by Examiner and made of record in the application file.

Claim Rejections - 35 U$C § 101

2. 35 U.S.C. 101 reads as follows: Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. The claimed invention is directed to a judicial exception (i.e., a law of nature, a natural phenomenon, or an abstract idea) without significantly more. Claims 1-20 are directed to a semiconductor die comprising: a semiconductor substrate; a switch formed on the semiconductor substrate and including a stack of field-effect transistors (FETs) connected in series; and a capacitor formed on the semiconductor substrate and connected in series with the switch, the capacitor configured to inhibit a low- frequency blocker signal from mixing with a fundamental-frequency signal in the switch. The claims do not include additional elements that are sufficient to amount to significantly

more than the judicial exception because the claims 1-20 are not significantly more than the abstract idea.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6, 9-12 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasuda et al. (US PAT. 7,265,604 hereinafter, “Yasuda”) in view of Granger-Jones et al. (U.S PUB. 2011/0260773 hereinafter, “Fu”).

Consider claim 1, Yasuda teaches a semiconductor die comprising: a semiconductor substrate (col. 5 line 55 through col. 6 line 7); a switch formed on the semiconductor substrate and including a stack of field-effect transistors (FETs) connected in series (Abstract, col. 13 lines 16-41).

Yasuda does not explicitly show that a capacitor formed on the semiconductor substrate and connected in series with the switch, the capacitor configured to inhibit a low- frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

In the same field of endeavor, Granger-Jones teaches a capacitor formed on the semiconductor substrate and connected in series with the switch, the capacitor

configured to inhibit a low- frequency blocker signal from mixing with a fundamental-frequency signal in the switch (page 3 [0033]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, a capacitor formed on the semiconductor substrate and connected in series with the switch, the capacitor configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch, as taught by Granger-Jones, in order to provide a stacked field effect transistor (FET) switch having a plurality of FET devices coupled in series to form an FET device stack. The FET device stack is configured to operate in an open state and in closed state. During the closed state, the plurality of FET devices is turned on and thus a time-variant input signal can be transmitted through the FET device stack. On the other hand, in the closed state, the plurality of FET devices is turned off and the time-variant input signal is blocked from being transmitted through the FET device stack.

Consider claim 2, Yasuda further teaches an insulator layer disposed between the stack of FETs and the semiconductor substrate (col. 5 line 55 through col. 6 line 7).

Consider claim 3, Granger-Jones further teaches wherein the die is a silicon-on-insulator (SOI) die (page 3 [0030]).

Consider claim 4, Granger-Jones further teaches wherein the stack of FETs includes silicon-on-insulator (SOI) FETs (page 3 [0030]).

Consider claim 5, Granger-Jones further teaches wherein the capacitor is connected to an antenna node (page 8 [0063]).

Consider claim 6, Granger-Jones further teaches wherein the capacitor is disposed between the switch and the antenna node (page 8 [0063]).

Consider claim 9, Yasuda teaches a method for operating a radio-frequency (RF) device, the method comprising: controlling an RF switch including a plurality of field-effect transistors (FETs) connected in series between first and second nodes so that the FETs are collectively in an ON state or an OFF state (Abstract, col. 10 lines 25-46 and col. 13 lines 16-41).

Yasuda does not explicitly show that inhibiting a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch using a capacitor connected in series with the switch between the switch and the first node.

In the same field of endeavor, Granger-Jones teaches inhibiting a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch using a capacitor connected in series with the switch between the switch and the first node (col. 2 lines 32-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, inhibiting a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch using a capacitor connected in series with the switch between the switch and the first node, as taught by Granger-Jones, in order to provide a stacked field effect transistor (FET) switch having a plurality

of FET devices coupled in series to form an FET device stack. The FET device stack is configured to operate in an open state and in closed state. During the closed state, the plurality of FET devices is turned on and thus a time-variant input signal can be transmitted through the FET device stack. On the other hand, in the closed state, the plurality of FET devices is turned off and the time-variant input signal is blocked from being transmitted through the FET device stack.

Consider claim 10, the previous rejections of claim 2 apply mutatis mutandis to corresponding claim 10.

Consider claim 11, Granger-Jones further teaches wherein the switch is a silicon-on-insulator (SOI) switch (page 3 [0030]).

Consider claim 12, Granger-Jones further teaches wherein the first node is an antenna node (page 8 [0063]).

Consider claim 15, Yasuda teaches a wireless device comprising: a transceiver configured to process RF signals (col. 1 lines 12-17); an antenna in communication with the transceiver (col. 1 lines 12-17); and a switch module interconnected to the antenna (col. 1 lines 12-17) and the transceiver and configured to selectively route RF signals to and from the antenna, the switch module including a switch including a stack of field-effect transistors (FETs) connected in series (Abstract, col. 1 lines 12-17 and col. 13 lines 16-41).

Yasuda does not explicitly show that the switch module further including a capacitor connected in series with the switch, the capacitor configured to inhibit a low-frequency blocker signal from mixing with a fundamental- frequency signal in the switch.

In the same field of endeavor, Granger-Jones teaches the switch module further including a capacitor connected in series with the switch, the capacitor configured to inhibit a low-frequency blocker signal from mixing with a fundamental- frequency signal in the switch (col. 2 lines 32-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use, the switch module further including a capacitor connected in series with the switch, the capacitor configured to inhibit a low-frequency blocker signal from mixing with a fundamental- frequency signal in the switch, as taught by Granger-Jones, in order to provide a stacked field effect transistor (FET) switch having a plurality of FET devices coupled in series to form an FET device stack. The FET device stack is configured to operate in an open state and in closed state. During the closed state, the plurality of FET devices is turned on and thus a time-variant input signal can be transmitted through the FET device stack. On the other hand, in the closed state, the plurality of FET devices is turned off and the time-variant input signal is blocked from being transmitted through the FET device stack.

Consider claim 16, Granger-Jones further teaches wherein the switch is formed on a silicon-on-insulator (SOI) die of the wireless device (page 3 [0030]).

Consider claim 17, Granger-Jones further teaches wherein the capacitor is part of the same semiconductor die as the stack of FETs (page 3 [0030]).

Consider claim 18, the previous rejections of claim 6 apply mutatis mutandis to corresponding claim 18.

6. Claims 7, 8, 13, 14, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasuda in view of Granger-Jones and further in view of Brindle et al. (U.S PAT. 8,129,787 hereinafter, “Brindle”).

Consider claim 7, Yasuda and Granger-Jones in combination fail to teach wherein the switch is part of a receive path, the switch being connected to an output node for an RF signal received from the antenna.

However, Brindle teaches wherein the switch is part of a receive path, the switch being connected to an output node for an RF signal received from the antenna (col. 11 lines 48-59).

Therefore, it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate the disclosing of Brindle into view of Yasuda and Granger-Jones, in order to control accumulated charge in SOI MOSFETs, thereby improving nonlinear responses and harmonic and intermodulaton distortion effects in the operation of the SOI MOSFETs.

Consider claim 8, Brindle further teaches wherein the switch is part of a transmit path, the switch being connected to an input node for an amplified RF signal (col. 17 line 57 through col. 18 line 8).

Consider claim 13, the previous rejections of claim 7 apply mutatis mutandis to corresponding claim 13.

Consider claim 14, the previous rejections of claim 8 apply mutatis mutandis to corresponding claim 14.

Consider claim 19, the previous rejections of claim 7 apply mutatis mutandis to corresponding claim 19.

Consider claim 20, the previous rejections of claim 8 apply mutatis mutandis to corresponding claim 20.

Conclusion

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Maung Nay A. can be reached on (571)272-7882. The fax phone number for the organization where this application or proceeding is assigned is (571)273-8300.

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/Tuan H. Nguyen/
Primary Examiner
Art Unit 2647

Notice of References Cited	Application/Control No. 14/833,076	Applicant(s)/Patent Under Reexamination MADAN ET AL.	
	Examiner TUAN H. NGUYEN	Art Unit 2647	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-7,265,604 B2	09-2007	Yasuda; Eiji	H03K17/693	327/427
*	B	US-8,129,787 B2	03-2012	Brindle; Christopher N.	H01L29/78609	257/347
*	C	US-2011/0260773 A1	10-2011	Granger-Jones; Marcus	H03K17/102	327/427
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

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	N					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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CONFIRMATION NO. 3042

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/833,076	08/22/2015	455	2647	75900-50031D1

APPLICANTS

SKYWORKS SOLUTIONS, INC., Woburn, MA

INVENTORS

Anuj Madan, Cambridge, MA;
Fikret Altunkilic, North Andover, MA;
Guillaume Alexandre Blin, Carlisle, MA;

**** CONTINUING DATA **************************

This application is a DIV of 13/936,175 07/06/2013 PAT 9148194
which claims benefit of 61/669,045 07/07/2012

**** FOREIGN APPLICATIONS **************************

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09/04/2015

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /TUAN HOANG NGUYEN/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		MA	9	20	3

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Fernando Hale & Chang LLP
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UNITED STATES

TITLE

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BIB (Rev. 05/07).

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14833076	MADAN ET AL.
	Examiner	Art Unit
	TUAN H NGUYEN	2647

CPC- SEARCHED		
Symbol	Date	Examiner
H04B1/44.	12/28/2015	T.N

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner
H04B1/48,H04B15/005.	12/28/2015	T.N

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
455	78,87,,252.1,296.	12/28/2015	T.N
438	178,197,381.	12/28/2015	T.N
327	427,434,436,437.	12/28/2015	T.N

SEARCH NOTES		
Search Notes	Date	Examiner
All searches are on EAST data base.	12/28/2015	T.N

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	See search above.	12/28/2015	T.N

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	6292	((stack$3 near3 field adj2 effect$3 adj2 transistor$1) FET) near3 (connect$3 coupl$3) near3 ser$3	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:21
S2	5745	capacitor$1 near3 form$3 near3 semiconductor$1 near3 substrate	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:21
S3	1538	switch$3 near3 form$3 near3 semiconductor$1 near3 substrate	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:21
S4	97	S2 and S3	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:21
S5	8	S1 and S4	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:21
S6	22620	(H04B1/44 OR H04B1/48 OR H04B15/005 OR H04B15/00 OR H04B15/02 OR H04B1/10 OR H04B1/04 OR H04B7/0602 OR H03H19/004 OR H03H2210/025).CPC.	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:47
S7	3	S4 and S6	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:47
S8	5176	455/78,87,252.1,296.ccls.	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:47
S9	1	S4 and S8	US-PGPUB; USPAT; USOCR;	OR	ON	2015/12/22 10:47

			FPRS			
S10	7160	438/178,197,381.ccls.	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:47
S11	3	S4 and S10	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:47
S12	3021	327/427,434,436,437.ccls.	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:47
S13	11	S4 and S12	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:47
S14	26464	((radio adj2 frequenc$3) RF) adj3 switch$3	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:48
S15	8	S4 and S14	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:48
S16	29	Anuj near3 Madan.in.	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:48
S17	5	S4 and S16	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:48
S18	28	Fikret near3 Altunkilic.in.	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:48
S19	6	S4 and S18	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:48
S20	31	Guillaume near3 Alexandre near3 Blin.in.	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 10:48
S21	5	S4 and S20	US-PGPUB;	OR	ON	2015/12/22

			USPAT; USOCR; FPRS			10:48
S22	1342	(reduc$3 decreas$3 lower) near3 intermodulat$3 near3 distort$3	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:19
S23	5745	capacitor$1 near3 form$3 near3 semiconductor$1 near3 substrate	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:19
S24	1538	switch$3 near3 form$3 near3 semiconductor$1 near3 substrate	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:19
S25	97	S23 and S24	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:19
S26	1	S22 and S25	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:19
S27	4	S22 and S24	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:20
S28	6292	((stack$3 near3 field adj2 effect$3 adj2 transistor$1) FET) near3 (connect$3 coupl$3) near3 ser$3	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:42
S29	8	S25 and S28	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:42
S30	17	S23 and S28	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:51
S31	41	S24 and S28	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:51
S32	7756	capacit$4 near3 (connect$3 coupl$3) near3 antenna$3	US-PGPUB; USPAT; USOCR;	OR	ON	2015/12/22 13:53

			FPRS			
S33	2	S31 and S32	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 13:53
S34	24	S31 and ((transmi$6 receiv$3 transceiv$3) near3 (device$1 unit$1 module$1 apparatus))	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 14:45
S35	333011	((radio adj2 frequenc$3) RF) near3 signal$1	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 14:47
S36	19	S34 and S35	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 14:47
S37	3450708	((transmi$6 receiv$3 transceiv$3) near3 (device$1 unit$1 module$1 apparatus))	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 15:16
S38	202701	S35 and S37	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 15:16
S39	6	S25 and S38	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 15:17
S40	64	S24 and S38	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 15:18
S41	35	S23 and S38	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 15:18
S42	4	S22 and S40	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 15:18
S43	19	S28 and S40	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 16:26
S44	576222	semiconductor$1 near3 substrate	US-PGPUB;	OR	ON	2015/12/22

EX-1037
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.
0061

			USPAT; USOCR; FPRS			16:32
S45	218001	(silicon near3 insulat$3)	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 16:33
S46	13	S31 and S45	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 16:34
S47	78209	((field adj2 effect$3 adj2 transistor$1) FET) same insulat$3	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 16:47
S48	18	S40 and S47	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 16:47
S49	18	S38 and S48	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 16:48
S50	279250	(silicon near3 insulat$3) SOI	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 17:41
S51	592	S28 and S50	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 17:41
S52	175	S37 and S51	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 17:42
S53	10	S24 and S52	US-PGPUB; USPAT; USOCR; FPRS	OR	ON	2015/12/22 17:42

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14833076	MADAN ET AL.
	Examiner	**Art Unit**
	TUAN H NGUYEN	2647

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/28/2015								
	1	✓								
	2	✓								
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	19	✓								
	20	✓								

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(Not for submission under 37 CFR 1.99)

Application Number	14/833,076
Filing Date	08/22/2015
First Named Inventor	Anuj Madan
Art Unit	2647
Examiner Name	Tuan H. Nguyen
Attorney Docket Number	75900-50031D1

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8779840		2014-07-15	Sugiura, et al.	
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	3	8514008		2013-08-20	Yan, et al.	
	4	8461903		2013-06-11	Granger-Jones	
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	First Named Inventor	Anuj Madan
	Art Unit	2647
	Examiner Name	Tuan H. Nguyen
	Attorney Docket Number	75900-50031D1

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	14	7619462		2009-11-17	Kelly, et al.	
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	First Named Inventor	Anuj Madan
	Art Unit	2647
	Examiner Name	Tuan H. Nguyen
	Attorney Docket Number	75900-50031D1

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	27	4999585		1991-03-12	Burt, et al.	
	28	4255756		1981-03-10	Shimotori, et al.	

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	Examiner Name	Tuan H. Nguyen
	Attorney Docket Number	75900-50031D1

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	2	20110148501		2011-06-23	Granger-Jones, et al.	
	3	20110025403		2011-02-03	Cassia	
	4	20100060377		2010-03-11	Takahashi	
	5	20050239415		2005-10-27	Sagae, et al.	
	6	20140009214		2014-01-09	Altunkilic, et al.	
	7	20140009208		2014-01-09	Smith	
	8	20140009203		2014-01-09	Cebi, et al.	
	9	20130009725		2013-01-10	Heaney, et al.	
	10	20110169550		2011-07-14	Brindle, et al.	
	11	20050195037		2005-09-08	Dupuis, et al.	

EFS Web 2.1.17

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14/833,076
	Filing Date	08/22/2015
	First Named Inventor	Anuj Madan
	Art Unit	2647
	Examiner Name	Tuan H. Nguyen
	Attorney Docket Number	75900-50031D1

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2011045442	WO	A2	2011-04-21	Heaney, et al.		☐
	2	2005-515657	JP	A	2005-05-26	Peregrine Semiconductor corporation		☒

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	International Search Report and Written Opinion for PCT/US2013/049500 issued on December 23, 2013.	☐

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EXAMINER SIGNATURE

Examiner Signature	/Tuan Nguyen/	Date Considered	12/22/2015

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/833,076	08/22/2015	Anuj Madan	75900-50031D1

CONFIRMATION NO. 3042

115870
Fernando Hale & Chang LLP
4199 Campus Drive
Suite 550, #115
Irvine, CA 92612

PUBLICATION NOTICE

OC000000079444455

Title:RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION

Publication No.US-2015-0365088-A1
Publication Date:12/17/2015

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The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/833,076

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/833,076	08/22/2015	2649	1600	75900-50031D1	20	3

CONFIRMATION NO. 3042

115870
Fernando Hale & Chang LLP
4199 Campus Drive
Suite 550, #115
Irvine, CA 92612

FILING RECEIPT

OC000000077275539

Date Mailed: 09/08/2015

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Inventor(s)

Anuj Madan, Cambridge, MA;
Fikret Altunkilic, North Andover, MA;
Guillaume Alexandre Blin, Carlisle, MA;

Applicant(s)

SKYWORKS SOLUTIONS, INC., Woburn, MA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a DIV of 13/936,175 07/06/2013
which claims benefit of 61/669,045 07/07/2012

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/833,076**
Projected Publication Date: 12/17/2015
Non-Publication Request: No

Early Publication Request: No
Title

RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION

Preliminary Class

455

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	
	Filing Date	
	First Named Inventor	Anuj Madan
	Art Unit	
	Examiner Name	
	Attorney Docket Number	75900-50031D1

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8779840		2014-07-15	Sugiura, et al.	
	2	8723260		2014-05-13	Carroll, et al.	
	3	8514008		2013-08-20	Yan, et al.	
	4	8461903		2013-06-11	Granger-Jones	
	5	8441304		2013-05-14	Kinoshita, et al.	
	6	8054143		2011-11-08	Takahashi	
	7	7928794		2011-04-19	Balboni	
	8	7910993		2011-03-22	Brindle, et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Anuj Madan
	Art Unit	
	Examiner Name	
	Attorney Docket Number	75900-50031D1

	9	7898297		2011-03-01	Kapoor, et al.	
	10	7890063		2011-02-15	Ahn, et al.	
	11	7683433		2010-03-23	Kapoor, et al.	
	12	7659770		2010-02-09	Teraguchi, et al.	
	13	7659765		2010-02-09	Ito	
	14	7619462		2009-11-17	Kelly, et al.	
	15	7385436		2008-06-10	Itoh, et al.	
	16	7236044		2007-06-26	Talwalkar, et al.	
	17	7095266		2006-08-22	Miske	
	18	6989706		2006-01-24	Sekigawa, et al.	
	19	6281737		2001-08-28	Kuang, et al.	

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	Filing Date	
	First Named Inventor	Anuj Madan
	Art Unit	
	Examiner Name	
	Attorney Docket Number	75900-50031D1

	20	5969564		1999-10-19	Komatsu, et al.	
	21	5753955		1998-05-19	Fechner	
	22	5748016		1998-05-05	Kurosawa	
	23	5644266		1997-07-01	Chen, et al.	
	24	5382826		1995-01-17	Mojaradi, et al.	
	25	7885614		2011-02-08	Jedeloo	
	26	7848712		2010-12-07	Fu, et al.	
	27	4999585		1991-03-12	Burt, et al.	
	28	4255756		1981-03-10	Shimotori, et al.	

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	Filing Date	
	First Named Inventor	Anuj Madan
	Art Unit	
	Examiner Name	
	Attorney Docket Number	75900-50031D1

	1	20140002171		2014-01-02	Nohra	
	2	20110148501		2011-06-23	Granger-Jones, et al.	
	3	20110025403		2011-02-03	Cassia	
	4	20100060377		2010-03-11	Takahashi	
	5	20050239415		2005-10-27	Sagae, et al.	
	6	20140009214		2014-01-09	Altunkilic, et al.	
	7	20140009208		2014-01-09	Smith	
	8	20140009203		2014-01-09	Cebi, et al.	
	9	20130009725		2013-01-10	Heaney, et al.	
	10	20110169550		2011-07-14	Brindle, et al.	
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	Attorney Docket Number	75900-50031D1

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2011045442	WO	A2	2011-04-21	Heaney, et al.		☐
	2	2005-515657	JP	A	2005-05-26	Peregrine Semiconductor corporation		☒

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	1	International Search Report and Written Opinion for PCT/US2013/049500 issued on December 23, 2013.	☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	
	First Named Inventor	Anuj Madan
	Art Unit	
	Examiner Name	
	Attorney Docket Number	75900-50031D1

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Alan T. Hale/	Date (YYYY-MM-DD)	2015-08-22
Name/Print	Alan T. Hale	Registration Number	68226

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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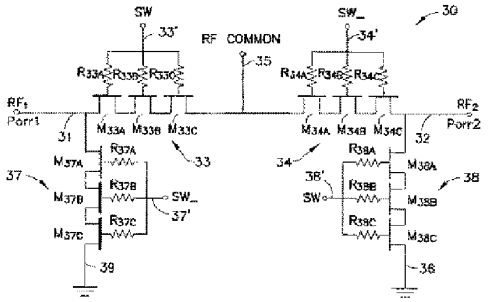
(54)【発明の名称】スイッチ回路および高周波信号のスイッチング方法

(57)【要約】
新規なＲＦスイッチ回路およびＲＦ信号をスイッチングするための方法について記載している。ＲＦスイッチ回路は、シリコンオンインシュレータ（ＳＯＩ）技術で製造する。ＲＦスイッチには、ＲＦ入力信号を交互に共通ＲＦノードに結合するために使用する、スイッチングトランジスタ・グループおよび分路トランジスタグループの組が含まれる。スイッチングトランジスタ・グループおよび分路トランジスタグループの組は、スイッチング制御電圧（ＳＷ）およびその逆の（ＳＷ＿）によって制御される。スイッチングトランジスタ・グループおよび分路トランジスタグループには、「積層」または直列構成にともに接続された１つまたは複数のＭＯＳＦＥＴトランジスタが含まれる。トランジスタ・グループデバイスの積層および関連するゲート抵抗器は、直列に接続されたスイッチトランジスタ全体の降伏電圧を増加し、ＲＦスイッチ圧縮を改善するように働く。ＲＦスイッチ素子とともに集積されたデジタル制御論理および負電圧発生器を含む、完全に集積化されたＲＦスイッチについて記載している。一実施形態では、完全に集積化された



【特許請求の範囲】
【請求項1】
（ａ）　第１のＲＦ入力信号を受信する第１の入力ポートと、
（ｂ）　第２のＲＦ入力信号を受信する第２の入力ポートと、
（ｃ）　ＲＦ共通ポートと、
（ｄ）　前記第１の入力ポートに結合された第１のノードと、前記ＲＦ共通ポートに結合された第２のノードとを有し、スイッチ制御信号（ＳＷ）によって制御される第１のスイッチトランジスタ・グループと、
（ｅ）　前記第２の入力ポートに結合された第１のノードと、前記ＲＦ共通ポートに結合された第２のノードとを有し、前記スイッチ制御信号（ＳＷ）の反転信号（ＳＷ＿）によって制御される第２のスイッチトランジスタ・グループと、
（ｆ）　前記第２の入力ポートに結合された第１のノードと、グラウンドに結合された第２のノードとを有し、前記スイッチ制御信号（ＳＷ）によって制御される、第１の分路トランジスタグループと、
（ｇ）　前記第１の入力ポートに結合された第１のノードと、グラウンドに結合された第２のノードとを有し、前記スイッチ制御信号（ＳＷ）の反転信号（ＳＷ＿）によって制御される、第２の分路トランジスタグループと、
を含む、ＲＦ信号をスイッチングするためのＲＦスイッチ回路であって、
前記スイッチ制御信号ＳＷが有効であるとき、前記第１のスイッチトランジスタ・グループおよび前記第１の分路トランジスタグループが作動する一方、前記第２のスイッチトランジスタ・グループおよび前記第２の分路トランジスタグループは不作動となり、それにより、前記第１のＲＦ入力信号を前記ＲＦ共通ポートへ通過させて、前記第２のＲＦ入力信号をグラウンドへ分路し、前記スイッチ制御信号ＳＷが非有効であるときには、前記第２のスイッチトランジスタ・グループおよび前記第２の分路トランジスタグループが作動する一方、前記第１のスイッチトランジスタ・グループおよび前記第１の分路トランジスタグループは不作動となり、それにより、前記第２のＲＦ入力信号を前記ＲＦ共通ポートへ通過させて、前記第１のＲＦ入力信号をグラウンドへ分路するＲＦスイッチ回路。
【請求項2】
シリコンオンインシュレータ（ＳＯＩ）技術において製造される、請求項１に記載のＲＦスイッチ回路。
【請求項3】
極薄シリコン（「ＵＴＳｉ」）基板上に製造される、請求項１に記載のＲＦスイッチ回路。
【請求項4】
前記トランジスタグループが、完全絶縁性サファイアウエハ上の薄いシリコン層に形成されるＭＯＳＦＥＴトランジスタを含み、前記完全絶縁性サファイアウエハが、基板の結合効果を減少することによって、前記ＲＦスイッチの性能特性を向上させる、請求項３に記載のＲＦスイッチ回路。
【請求項5】
スイッチ挿入損失が、前記ＭＯＳＦＥＴトランジスタのオン抵抗を減少することにより減少される、請求項４に記載のＲＦスイッチ回路。
【請求項6】
前記ＲＦスイッチのスイッチ分離特性が、前記ＭＯＳＦＥＴトランジスタのノード間の寄生容量を減少することにより改善される、請求項４に記載のＲＦスイッチ回路。
【請求項7】
前記トランジスタグループが、積層構成に配置された複数のＭＯＳＦＥＴトランジスタを含む、請求項３に記載のＲＦスイッチ回路。
【請求項8】
前記積層ＭＯＳＦＥＴトランジスタが、それぞれの関連するゲート抵抗器に結合された

ゲートノードを含み、前記ゲート抵抗器が、通常、スイッチング電圧によって制御される、請求項７に記載のＲＦスイッチ回路。

【請求項9】

前記第１のスイッチトランジスタ・グループおよび前記第１の分路トランジスタグループのトランジスタゲート・ノードに結合された前記ゲート抵抗器が、通常、前記スイッチ制御信号ＳＷによって制御される、請求項８に記載のＲＦスイッチ回路。

【請求項10】

前記第２のスイッチトランジスタ・グループおよび前記第２の分路トランジスタグループのトランジスタゲート・ノードに結合された前記ゲート抵抗器が、通常、前記反転スイッチ制御信号ＳＷ＿によって制御される、請求項８に記載のＲＦスイッチ回路。

【請求項11】

前記ＭＯＳＦＥＴトランジスタが関連するゲート容量を有し、前記トランジスタグループ内の各ＭＯＳＦＥＴトランジスタに関連するＲＣ時定数が、前記ゲート抵抗器および関連する前記ゲート容量の関数であり、各トランジスタの前記ＲＣ時定数が、前記ＲＦ入力信号の周期をはるかに超え、それによって、ＲＦ電圧が、前記ＭＯＳＦＥＴトランジスタ全体で等しく共用される、請求項８に記載のＲＦスイッチ回路。

【請求項12】

選択したトランジスタグループの、前記複数の積層ＭＯＳＦＥＴトランジスタ全体の降伏電圧が、前記選択したトランジスタグループの個別ＭＯＳＦＥＴトランジスタの降伏電圧のｎ倍に効果的に増加され、ｎが、前記選択したトランジスタグループにおけるＭＯＳＦＥＴトランジスタの総計を含む、請求項８に記載のＲＦスイッチ回路。

【請求項13】

関連する１ｄＢ圧縮ポイントを有し、前記１ｄＢ圧縮ポイントを、前記積層ＭＯＳＦＥＴトランジスタ構成を用いて増加する、請求項１２に記載のＲＦスイッチ回路。

【請求項14】

前記第１のＲＦ入力信号および前記第２のＲＦ入力信号が、関連する入力電力レベルを有し、増加した入力電力レベルを、トランジスタグループごとのＭＯＳＦＥＴトランジスタの数を増加することによって、前記ＲＦスイッチ回路で調節できる、請求項７に記載のＲＦスイッチ回路。

【請求項15】

前記第１のＲＦ入力信号および前記第２のＲＦ入力信号が、関連する入力電力レベルを有し、増加した入力電力レベルを、トランジスタグループの実現に使用するトランジスタの物理的サイズを変えることによって、前記ＲＦスイッチ回路で調節できる、請求項７に記載のＲＦスイッチ回路。

【請求項16】

（ａ）　請求項３に記載のＲＦスイッチ回路と、

（ｂ）　前記スイッチ制御信号（ＳＷ）および前記反転スイッチ制御信号（ＳＷ＿）を出力する、前記ＲＦスイッチ回路に結合された制御論理ブロックと、

（ｃ）　クロック入力信号および外部電源からの正の電源電圧を受取り、負の電源電圧を出力する、前記制御論理ブロックに結合された負電圧発生器と、

を含む、完全に集積化されたＲＦスイッチ回路。

【請求項17】

前記ＲＦスイッチ回路が、複数のデジタル回路およびアナログ回路とともに、集積回路（ＩＣ）に集積されている、請求項１６に記載の完全に集積化されたＲＦスイッチ回路。

【請求項18】

（ａ）　クロック入力信号を出力する発振器と、

（ｂ）　前記クロック入力信号を入力する前記発振器に結合され、負の電源電圧を出力する電荷ポンプと、

（ｃ）　前記電荷ポンプに結合され、前記スイッチトランジスタ・グループおよび前記分路トランジスタグループの制御に使用する制御信号を出力する論理回路ブロックと、

（ｄ）　前記論理回路ブロックおよび前記ＲＦスイッチ回路に結合され、前記トランジスタグループを実現するために使用するＭＯＳＦＥＴトランジスタのゲート－ドレイン、ゲート－ソースおよびドレイン－ソース電圧を減少するレベルシフト回路と、
（ｅ）　前記ＲＦスイッチ回路に結合され、ＲＦ信号エネルギを、前記電荷ポンプブロックおよび前記論理回路ブロックから分離するＲＦバッファ回路と、
をさらに含む、請求項１６に記載の完全に集積化されたＲＦスイッチ回路。
【請求項19】
前記電荷ポンプが、
（ａ）　少なくとも２つのＰチャネルＭＯＳＦＥＴトランジスタと、
（ｂ）　少なくとも２つのＮチャネルＭＯＳＦＥＴトランジスタであって、それぞれが、それぞれの関連するＰチャネルＭＯＳＦＥＴトランジスタと直列に結合され、それによって、前記電荷ポンプのそれぞれのレッグを形成するＮチャネルＭＯＳＦＥＴトランジスタと、
（ｃ）　連続レッグに結合された前記電荷ポンプの各レッグを結合する、少なくとも１つの結合キャパシタと、
（ｄ）　前記電荷ポンプの出力レッグに結合された出力キャパシタと、
を含み、
前記負の電源電圧を、前記ＰチャネルＭＯＳＦＥＴトランジスタおよび前記ＮチャネルＭＯＳＦＥＴトランジスタを駆動するための、非重複入力クロック信号を用い、前記結合キャパシタおよび前記出力キャパシタを交互に充電および放電することによって、前記電荷ポンプで発生する、請求項１８に記載の完全に集積化されたＲＦスイッチ回路。
【請求項20】
前記非重複入力クロック信号が、２つの非重複クロック制御信号を含み、第１の非重複クロック制御信号がＰチャネルトランジスタを制御し、第２の非重複クロック制御信号がＮチャネルトランジスタを制御する、請求項１９に記載の完全に集積化されたＲＦスイッチ回路。
【請求項21】
前記Ｐチャネルトランジスタおよび前記Ｎチャネルトランジスタが、単一閾値トランジスタである、請求項１９に記載の完全に集積化されたＲＦスイッチ回路。
【請求項22】
前記非重複入力クロック信号が、パルスシフト回路によって発生される、請求項１９に記載の完全に集積化されたＲＦスイッチ回路。
【請求項23】
前記非重複入力クロック信号が、前記発振器クロック入力信号から引き出される、請求項１９に記載の完全に集積化されたＲＦスイッチ回路。
【請求項24】
前記発振器が、弛張発振器を含む、請求項１９に記載の完全に集積化されたＲＦスイッチ回路。
【請求項25】
前記非重複入力クロック信号が、－Ｖｄｄから＋Ｖｄｄまでの電圧振幅で変化する、請求項１９に記載の完全に集積化されたＲＦスイッチ回路。
【請求項26】
前記レベルシフト回路が、フィードバック構成でともに結合された複数のインバータを含む、請求項１８に記載の完全に集積化されたＲＦスイッチ回路。
【請求項27】
前記インバータが、第１の差動入力と、第２の差動入力と、論理入力と、論理出力とを含み、前記レベルシフト回路が、
（ａ）　２つの入力差動インバータを含む入力インバータグループであって、第１の入力差動インバータが論理入力信号（ｉｎｐｕｔ）を受信して、第１の論理入力信号（ｉｎ）を出力し、第２の入力差動インバータが、前記第１の論理入力信号（ｉｎ）を受信し、

前記第１の論理入力信号の逆（ｉｎ＿）を出力する入力インバータグループと、
（ｂ）　３つの差動インバータを含む第１のインバータグループであって、前記第１のインバータグループにおける第１のインバータの前記論理出力が、前記第１の論理入力信号（ｉｎ）に結合され、前記第１のインバータの前記論理出力が、前記第１のインバータグループにおける出力インバータの第１の差動入力に結合され、前記第１のインバータグループにおける第２のインバータの前記論理出力が、前記第１のインバータグループにおける前記出力インバータの第２の差動入力に結合され、前記第１のインバータグループの前記出力インバータが、第１の出力信号（ｏｕｔ）を出力する第１のインバータグループと、
（ｃ）　３つの差動インバータを含む第２のインバータグループであって、前記第２のインバータグループの第１のインバータの前記論理出力が、前記第１の論理入力信号の前記逆（ｉｎ＿）に結合され、前記第２のインバータグループにおける前記第１のインバータの前記論理出力が、前記第２のインバータグループにおける出力インバータの第１の差動入力に結合され、前記第２のインバータグループにおける第２のインバータの前記論理出力が、前記第２のインバータグループにおける前記出力インバータの第２の差動入力に結合され、前記第２のインバータグループにおける前記出力インバータが、第２の出力信号（ｏｕｔ＿）を出力する前記第２のインバータグループと、を含み、
前記第１の出力信号（ｏｕｔ）がフィードバックとして供給されて、前記第２のインバータグループにおける前記第２のインバータの論理入力部に入力され、前記第２の出力信号（ｏｕｔ＿）が、フィードバックとして供給されて、前記第１のインバータグループにおける前記第２のインバータの論理入力部に入力される請求項２６に記載の完全に集積化されたＲＦスイッチ回路。
【請求項28】
前記第１の出力信号および前記第２の出力信号が、前記ＲＦスイッチの、前記スイッチトランジスタ・グループおよび前記分路トランジスタグループを制御する、請求項２７に記載の完全に集積化されたＲＦスイッチ回路。
【請求項29】
前記レベルシフト回路が、前記入力信号の周波数応答に影響を与えずに、前記論理入力信号（ｉｎｐｕｔ）の直流レベルをシフトする、請求項２６に記載の完全に集積化されたＲＦスイッチ回路。
【請求項30】
前記ＲＦバッファ回路が、第１段階レベルシフト回路および第２段階ＲＦバッファ回路を含む２段階回路を含み、前記第１段階レベルシフト回路が、請求項２７で定義されたレベルシフト回路を含み、前記第２段階ＲＦバッファ回路が、第２の複数の差動インバータを含み、前記第２の複数の差動インバータが、それぞれ、第１の差動入力と、第２の差動入力と、論理入力と、論理出力とを有し、前記第２段階ＲＦバッファ回路が、さらに、
（ａ）　３つの差動インバータを含む第１のＲＦバッファインバータ・グループであって、前記第１のＲＦバッファインバータ・グループにおける第１のインバータと第２のインバータの前記論理入力が、前記レベルシフト回路によって、前記第１の出力信号（ｏｕｔ）出力に結合され、前記第１のＲＦバッファインバータ・グループにおける前記第１のインバータの前記論理出力が、前記第１のＲＦバッファインバータ・グループにおける出力インバータの第１の差動入力に結合され、前記第１のＲＦバッファインバータ・グループにおける、前記第２のインバータの前記論理出力が、前記第１のＲＦバッファインバータ・グループにおける前記出力インバータの第２の差動入力に結合され、前記第１のＲＦバッファインバータ・グループの前記出力インバータが、第１の出力信号（ＯＵＴ）を出力する第１のＲＦバッファインバータ・グループと、
（ｂ）　３つの差動インバータを含む第２のＲＦバッファインバータ・グループであって、前記第２のＲＦバッファインバータ・グループにおける第１のインバータと第２のインバータの前記論理入力が、前記レベルシフト回路によって、前記第２の出力信号（ｏｕｔ＿）出力に結合され、前記第２のＲＦバッファインバータ・グループにおける前記第１

のインバータの前記論理出力が、前記第２のＲＦバッファインバータ・グループにおける出力インバータの第１の差動入力に結合され、前記第２のＲＦバッファインバータ・グループにおける前記第２のインバータの前記論理出力が、前記第２のＲＦバッファインバータ・グループにおける前記出力インバータの第２の差動入力に結合され、前記第２のＲＦバッファインバータ・グループの前記出力インバータが、第２の出力信号（ＯＵＴ＿）を出力する第２のＲＦバッファインバータ・グループと、
を含む、請求項１８に記載の完全に集積化されたＲＦスイッチ回路。
【請求項31】
前記ＲＦバッファ回路が、デジタル論理信号を前記ＲＦスイッチ回路から分離する、請求項３０に記載の完全に集積化されたＲＦスイッチ回路。
【請求項32】
前記第２段階ＲＦバッファ回路が、前記出力信号ＯＵＴおよびＯＵＴ＿のフィードバックを、前記第１段階レベルシフト回路に供給せず、それによって、前記デジタル論理信号からの、前記ＲＦスイッチの分離を改善する、請求項３１に記載の完全に集積化されたＲＦスイッチ回路。
【請求項33】
前記第１段階レベルシフト回路を実現するために使用するトランジスタが、前記第２段階ＲＦバッファ回路を実現するために使用するトランジスタよりも小さい、請求項３０に記載の完全に集積化されたＲＦスイッチ回路。
【請求項34】
前記出力信号（ｏｕｔ）および（ｏｕｔ＿）に結合された分圧器回路をさらに含み、前記分圧器回路が、前記出力信号の電圧レベルを制限し、その後、前記出力信号が、前記第１インバータグループおよび前記第２インバータグループの前記第２のインバータにフィードバックとして供給される、請求項２７に記載の完全に集積化されたＲＦスイッチ回路。
【請求項35】
前記分圧器回路が、前記電圧レベルを、ほぼＶｄｄに制限する、請求項３４に記載の完全に集積化されたＲＦスイッチ回路。
【請求項36】
前記分圧器が、直列構成にともに結合された複数のＭＯＳＦＥＴデバイスを含み、出力ＭＯＳＦＥＴデバイスが、バラスト抵抗器を介してグラウンドノードに結合され、前記ＭＯＳＦＥＴデバイスが、ダイオード機能を果たす、請求項３４に記載の完全に集積化されたＲＦスイッチ回路。
【請求項37】
前記ＲＦバッファ回路が、第１段階レベルシフト回路と第２段階ＲＦバッファ回路とを含む２段階回路を含み、前記第１段階レベルシフト回路が、請求項３４で定義されたレベルシフト回路を含み、前記第２段階ＲＦバッファ回路が、第２の複数の差動インバータを含み、前記第２の複数の差動インバータが、それぞれ、第１の差動入力と、第２の差動入力と、論理入力と、論理出力とを含み、前記第２段階ＲＦバッファ回路が、さらに、
（ａ）　３つの差動インバータを含む第１のＲＦバッファインバータ・グループであって、前記第１のＲＦバッファインバータ・グループにおける第１のインバータの前記論理入力が、前記レベルシフト回路によって、第１の出力信号（ｏｕｔ＿ｐｏｓ１）出力に結合され、前記第１のＲＦバッファインバータ・グループにおける第２のインバータの前記論理入力が、前記レベルシフト回路によって、第２の出力信号（ｏｕｔ＿ｎｅｇ１）出力に結合され、前記第１のＲＦバッファインバータ・グループにおける前記第１のインバータの前記出力が、前記第１のＲＦバッファインバータ・グループにおける出力インバータの第１の差動入力に結合され、前記第１のＲＦバッファインバータ・グループにおける前記第２のインバータの前記論理出力が、前記第１のＲＦバッファインバータ・グループにおける前記出力インバータの第２の差動入力に結合され、前記第１のＲＦバッファインバータ・グループの前記出力インバータが、第１の出力信号（ＯＵＴ）を出力する第１のＲ

ＲＦバッファインバータ・グループと、
（ｂ）　３つの差動インバータを含む第２のＲＦバッファインバータ・グループであって、前記第２のＲＦバッファインバータ・グループにおける第１のインバータの前記論理入力が、前記レベルシフト回路によって、第３の出力信号（ｏｕｔ＿ｐｏｓ２）出力に結合され、前記第２のＲＦバッファインバータ・グループにおける第２のインバータの前記論理入力が、前記レベルシフト回路によって、第４の出力信号（ｏｕｌ＿ｎｅｇ２）出力に結合され、前記第２のＲＦバッファインバータ・グループにおける前記第１のインバータの前記出力が、前記第２のＲＦバッファインバータ・グループにおける出力インバータの第１の差動入力に結合され、前記第２のＲＦバッファインバータ・グループにおける、前記第２のインバータの前記論理出力が、前記第２のＲＦバッファインバータ・グループにおける前記出力インバータの第２の差動入力に結合され、前記第２のＲＦバッファインバータ・グループの前記出力インバータが、第２の出力信号（ＯＵＴ＿）を出力する第２のＲＦバッファインバータ・グループと、を含み、
前記第１の出力信号（ｏｕｔ＿ｐｏｓ１）が、前記レベルシフト回路の前記第１のインバータグループにおける前記第１のインバータのバッファされた出力を含み、前記第２の出力信号（ｏｕｔ＿ｎｅｇ１）が、前記レベルシフト回路の前記第１のインバータグループにおける前記第２のインバータのバッファされた出力を含み、前記第３の出力信号（ｏｕｔ＿ｐｏｓ２）が、前記レベルシフト回路の前記第２のインバータグループにおける前記第１のインバータのバッファされた出力を含み、前記第４の出力信号（ｏｕｔ＿ｎｅｇ２）が、前記レベルシフト回路の前記第２のインバータグループにおける前記第２のインバータのバッファされた出力を含む、請求項１８に記載の完全に集積化されたＲＦスイッチ回路。
【請求項38】
前記非重複入力クロック信号が、請求項３４で定義されるレベルシフト回路へ入力され、その後前記電荷ポンプへ入力される、請求項２０に記載の完全に集積化されたＲＦスイッチ回路。
【請求項39】
前記レベルシフト回路が、第１のレベルシフト回路と第２のレベルシフト回路とを含み、前記第１のレベルシフト回路と前記第２のレベルシフト回路が請求項３４で定義され、前記第１のレベルシフト回路が、その第１のインバータグループにおける前記第１のインバータの前記論理出力から第１の出力信号（ｃｌｋ１ｐｏｓ）を出力し、その第１のインバータグループにおける前記第２のインバータの前記論理出力から第２の出力信号（ｃｌｋ１ｎｅｇ）を出力し、その第２のインバータグループにおける前記第１のインバータの前記論理出力から第３の出力信号（ｃｌｋ１ｐｏｓ＿）を出力し、その第２のインバータグループにおける前記第２のインバータの前記論理出力から第４の出力信号（ｃｌｋ１ｎｅｇ＿）を出力し、前記第２のレベルシフト回路が、その第１のインバータグループにおける前記第１のインバータの前記論理出力から第５の出力信号（ｃｌｋ２ｐｏｓ）を出力し、その第１のインバータグループにおける前記第２のインバータの前記論理出力から第６の出力信号（ｃｌｋ２ｎｅｇ）を出力し、その第２のインバータグループにおける前記第１のインバータの前記論理出力から第７の出力信号（ｃｌｋ２ｐｏｓ＿）を出力し、その第２のインバータグループにおける前記第２のインバータの前記論理出力から第８の出力信号（ｃｌｋ２ｎｅｇ＿）を出力する、請求項３８に記載の完全に集積化されたＲＦスイッチ回路。
【請求項40】
前記第３の出力信号（ｃｌｋ１ｐｏｓ＿）が、前記電荷ポンプの第１のＰチャネルＭＯＳＦＥＴトランジスタを制御し、前記第４の出力信号（ｃｌｋ１ｎｅｇ＿）が、前記電荷ポンプの第２のＰチャネルＭＯＳＦＥＴトランジスタを制御し、前記第５の出力信号（ｃｌｋ２ｐｏｓ）が、前記第１のＰチャネルＭＯＳＦＥＴトランジスタに関連する第１のＮチャネルＭＯＳＦＥＴトランジスタを制御し、前記第６の出力信号（ｃｌｋ２ｎｅｇ）が、前記第２のＰチャネルＭＯＳＦＥＴトランジスタに関連する第２のＮチャネルＭＯＳＦ

ＥＴトランジスタを制御する、請求項３９に記載の完全に集積化されたＲＦスイッチ回路。

【請求項41】

（ａ）　第１の高周波信号を受信するための第１の入力手段と、

（ｂ）　第２の高周波信号を受信するための第２の入力手段と、

（ｃ）　高周波共通ポート手段と、

（ｄ）　前記第１の入力手段に結合された第１のノードと前記高周波共通ポート手段に結合された第２のノードとを有し、スイッチ制御信号（ＳＷ）によって制御される第１の積層トランジスタスイッチング手段と、

（ｅ）　前記第２の入力手段に結合された第１のノードと前記高周波共通ポート手段に結合された第２のノードとを有し、前記スイッチ制御信号（ＳＷ）の反転信号（ＳＷ＿）によって制御される第２の積層トランジスタスイッチング手段と、

（ｆ）　前記第２の入力手段に結合された第１のノードと接地に結合された第２のノードとを有し、前記スイッチ制御信号（ＳＷ）によって制御される第１の積層トランジスタ分路手段と、

（ｇ）　前記第１の入力手段に結合された第１のノードと接地に結合された第２のノードとを有し、前記スイッチ制御信号（ＳＷ）の反転信号（ＳＷ＿）によって制御される第２の積層トランジスタ分路手段と、を備え、

前記スイッチング制御信号ＳＷが有効であるときに、前記第１の積層トランジスタスイッチング手段及び及び前記第１の積層トランジスタ分路手段が有効となり、前記第２の積層トランジスタスイッチング手段及び前記第２の積層トランジスタ分路手段が非有効となって、前記第１の高周波入力信号を高周波共通ポート手段に通過させ、前記第２の高周波入力信号を接地に分流させ、

前記スイッチング制御信号ＳＷが非有効であるときに、前記第２の積層トランジスタ分路手段が有効となり、前記第１の積層トランジスタ及び第１の積層トランジスタ分路手段が非有効となって、前記第２の高周波入力信号を前記高周波共通ポート手段に通過させ、前記第１の高周波入力信号を接地に分流させる、

高周波信号を切替える高周波スイッチング回路。

【請求項42】

（ａ）　複数の積層トランジスタを含む第１のスイッチトランジスタ・グループおよび第１の分路トランジスタグループに、第１のＲＦ入力信号を入力するステップと、

（ｂ）　複数の積層トランジスタを含む第２のスイッチトランジスタ・グループおよび第２の分路トランジスタグループに、第２のＲＦ入力信号を入力するステップと、

（ｃ）　前記第１のスイッチトランジスタ・グループを作動する一方、前記第１の分路トランジスタグループを不作動にし、同時に、前記第２のスイッチトランジスタ・グループを不作動にする一方、前記第２の分路トランジスタグループを作動し、それによって、前記第１のＲＦ入力信号を通過させ、前記第２のＲＦ入力信号を分路させるステップと、

（ｄ）　前記第２のスイッチトランジスタ・グループを作動する一方、前記第２の分路トランジスタグループを不作動にし、同時に、前記第１のスイッチトランジスタ・グループを不作動にする一方、前記第１の分路トランジスタグループを作動し、それによって、前記第２のＲＦ入力信号を通過させ、前記第１のＲＦ入力信号を分路させるステップと、

を含む、ＲＦ信号をスイッチングする方法。

【発明の詳細な説明】

【技術分野】

【0001】

発明の背景

発明の分野

本発明はスイッチに関し、特に、集積回路内のスイッチ回路および高周波（ＲＦ）信号のスイッチング方法に関する。一実施形態では、このスイッチ回路には、無線通信設備、

衛星およびケーブルテレビなどＲＦの適用分野において使用するための、シリコンオンインシュレータ（ＳＯＩ）上に実現するＣＭＯＳデバイスが含まれる。

【背景技術】

【0002】

関連技術の説明

周知のように、高周波（ＲＦ）スイッチは、多くの無線通信システムにおいて、重要な構成ブロックとなっている。ＲＦスイッチは、携帯電話機、無線ページャ、無線インフラ設備、衛星通信設備およびケーブルテレビ設備などの多くの異なる通信設備に使用されている。周知のように、ＲＦスイッチの性能は、３つの主な動作性能パラメータ、すなわち挿入損失、スイッチ分離および「１ｄＢ圧縮ポイント」によって決められる。これら３つの性能パラメータは緊密に結びついており、ＲＦスイッチ構成要素の設計において、いずれか１つのパラメータを重視すると、他のパラメータを犠牲にすることになる。ＲＦスイッチ設計において時々考慮される第４のパラメータは、通常、スイッチング時間またはスイッチング速度（スイッチの片側をオンにし、反対側をオフにするのに必要な時間と定義される）と呼ばれている。ＲＦスイッチの設計において重要な他の指標には、ＲＦスイッチ集積の容易さと程度（レベル）、複雑さ、歩留まり、返品損失および製造コストが含まれる。

【0003】

これらのＲＦスイッチの性能パラメータは、図１ａ～１ｃの簡易回路図に示す、先行技術によるＲＦスイッチ設計を参照して、より簡単に説明できる。図１ａに、先行技術の単極単投（ＳＰＳＴ）ＲＦスイッチ１０の簡易回路図を示す。先行技術のＳＰＳＴスイッチ１０には、スイッチングトランジスタＭ１（５）および分路トランジスタＭ２（７）が含まれる。ここで図１ａを参照すると、２つのＭＯＳＦＥＴトランジスタＭ１（５）およびＭ２（７）の制御電圧の状態に依存して（すなわち、ＭＯＳＦＥＴスイッチングトランジスタＭ１および分路トランジスタＭ２のゲート入力部にそれぞれ印加される直流バイアスに依存して）、ＲＦ信号は、ＲＦ入力ノード１からＲＦ出力ノード３へ送られるか、または分路トランジスタＭ２（７）を介してグラウンドへ分路される。直流バイアス電圧の実際の値は、ＭＯＳＦＥＴトランジスタＭ１（５）およびＭ２（７）の極性と閾値次第である。ＲＦ電源信号と直列の抵抗器Ｒ０（９）は、電源信号からバイアスを分離するものであり、最高のスイッチ性能にとって必須である。図１ｂに、図１ａにおけるＲＦスイッチ１０の「オン」状態を示す（すなわち、図１ｂには、ＲＦスイッチ１０が「オン」、スイッチングトランジスタＭ１（５）がオンおよび分路トランジスタＭ２（７）がオフのときの、トランジスタＭ１およびＭ２の等価小信号値を示す）。図１ｃに、図１ａのスイッチ１０の「オフ」状態を示す（すなわち、図１ｃには、ＲＦスイッチ１０が「オフ」、スイッチングトランジスタＭ１（５）がオフおよび分路トランジスタＭ２（７）がオンのときの、トランジスタＭ１およびＭ２の等価小信号値を示す）。

【0004】

図１ｂに示すように、ＲＦスイッチ１０がオンのとき、スイッチングトランジスタＭ１（５）は主に抵抗性であり、一方、分路トランジスタＭ２（７）は主に容量性である。ＲＦスイッチ１０の「挿入損失」は、入力ノード１における最大利用可能電力と出力ノード３の負荷に供給される電力間の差異から決定される。低周波においては、スイッチ１０がオンのとき（図１ｂを参照されたい）、電力損失はいずれも、スイッチングトランジスタＭ１（５）の有限なオン抵抗「ｒ」１３に起因する。オン抵抗ｒ１３（図１ｂ）は、典型的には、電源抵抗器Ｒ０（９）よりもずっと小さい。したがって、挿入損失「ＩＬ」は、以下に示す式１のような特徴がある。

式１：ＩＬはほぼ、１０ｒ／Ｒ０ｌｎ（１０）－０．０８７ｒ（ｄＢ）に等しい。

【0005】

したがって、低周波で、ｒの値が３Ωでは、結果として約０．２５ｄＢの挿入損失となる。挿入損失は、ＲＦスイッチ送信機のオン抵抗に大きく左右されるので、トランジスタ・オン抵抗を下げ、寄生基板抵抗を減少させることにより、挿入損失を改善できる。

【0006】
一般に、ＲＦスイッチの入力－出力分離（または簡単にスイッチ分離）は、入力ポートと出力ポートを接続しているトランジスタがオフのとき、入力ポートから出力ポートへ「流出」する電力量を測ることによって決定する。分離特性は、ＲＦスイッチの切断の程度はどれくらいか（すなわち、スイッチが、入力信号を出力からどの程度ブロックするか）を示す。特に、ここで図１ｃにおけるＲＦスイッチ１０の「オフ」状態を参照すると、スイッチＭ１（５）のオフ状態は、入力１を出力３からブロックする働きをする。分路トランジスタＭ２（７）もまた、スイッチ１０の入力－出力分離を向上させる働きをする。
【0007】
ターンオフすると（すなわち、ＲＦスイッチ１０およびスイッチングトランジスタＭ１（５）がターンオフするとき）、Ｍ１（５）は、主に容量性であり、入力信号の「フィードスルー」（ＲＦ入力信号が、入力ノード１から出力ノード３へ通ること）は、キャパシタＣＧＤオフ１５（スイッチングトランジスタＭ１がターンオフしたときのゲート－ドレインキャパシタンス）、キャパシタＣＧＳオフ１７（スイッチングトランジスタＭ１がターンオフしたときのゲート－ソースキャパシタンス）およびキャパシタＣＤＳ１（１９）（スイッチングトランジスタＭ１がターンオフしたときのドレイン－ソースキャパシタンス）の直列／並列値によって決定される。入力信号のフィードスルーは望ましくなく、ＲＦスイッチ１０の入力－出力分離に直接関連する。分路トランジスタＭ２（７）を使用してフィードスルーの大きさを減少し、それによってＲＦスイッチの分離特性を向上させる。
【0008】
図１ｃの分路トランジスタＭ２（７）を、スイッチングトランジスタＭ１（５）がターンオフのとき、ターンオンさせる。この条件では、分路トランジスタＭ２（７）は、主に、値ｒの抵抗器として働く。設計によっては、ｒの値は、ＲＦ電源特有のインピーダンスよりずっと小さい。結果として、ｒは、スイッチングトランジスタＭ１（５）の入力部の電圧を著しく減少させる。ｒの値が、電源抵抗Ｒ０（９）および分路トランジスタＭ２（７）のフィードスルー容量性抵抗よりもずっと小さいとき、分離は簡単に計算できる。ＲＦスイッチ１０のオフ状態のスイッチ分離は、入力部の最大利用可能電力と出力部の電力間の差異で決定する。
【0009】
ＲＦスイッチの挿入損失および分離に加えて、別の重要なＲＦスイッチ性能特性は、大きな入力電力を処理する能力である。これは、スイッチをターンオンしたとき、一定の周波数で、挿入損失が入力電力の関数とならないことを、確実なものとすることである。スイッチが、「スイッチオン」したスイッチを通して送られる電力をゆがめないことが、多くの適用分野で求められている。たとえば、２つの近接した音が、同時にＲＦスイッチを通過する場合には、スイッチの非線形性のために、相互変調（ＩＭ）を起こす可能性があり、それにより隣接するチャネルで擬似音声を生成する可能性がある。たとえば、これらの隣接するチャネルを、情報信号のために確保しておく場合には、擬似音声の電力は、できる限り小さく維持しなければならない。スイッチ圧縮または「１ｄＢ圧縮ポイント」（「Ｐ１ｄＢ」）は、電力を処理する能力を示す。Ｐ１ｄＢは、挿入損失がその低電力値から１ｄＢだけ増加したときの入力電力として定義される。または別の言い方をすると、１ｄＢ圧縮ポイントは、出力電力が、入力電力との線形的関係から１ｄＢだけ逸脱する前に、入力ポートでＲＦスイッチに入力できる電力量の程度である。
【0010】
スイッチ圧縮は、２つの道筋のいずれか１つで発生する。スイッチ圧縮がどのように発生するかを理解するために、図１ａ～１ｃのＲＦスイッチ１０に示すＭＯＳＦＥＴトランジスタの動作について説明する。トランジスタ設計分野においては周知のように、ＭＯＳＦＥＴは、ターンオンするために、閾値電圧V_tを超えるゲート－ソースバイアスが必要である。同様に、ゲート　ソースバイアスは、スイッチがオフになるためには、V_tより小さくなければならない。V_tは、「Ｎ型」ＭＯＳＦＥＴでは正であり、「Ｐ型」ＭＯＳ

ＦＥＴでは、負である。図１ａ～１ｃのＲＦスイッチ１０には、Ｎ型ＭＯＳＦＥＴが、選択されている。Ｎ型ＭＯＳＦＥＴのソースは、最も低い電位のノードである。
再び図１ｃを参照すると、分路トランジスタＭ２（７）の過渡電圧の結果、入力信号サイクルの一部期間に、分路トランジスタＭ２（７）がターンオンすると、入力電力はグラウンドへ送られ、出力に対しては失われる。この電力の損失は、入力電力が増加（すなわち、増加した電力の入力信号）すると増加し、それにより第１のタイプの圧縮を引き起こす。ＲＦスイッチ１０の１ｄＢ圧縮ポイントは、ターンオフした分路トランジスタＭ２（７）がオフのままでいられなくなるポイントにおける入力の信号振動によって決定される。結局、入力の負振動は、グラウンドより低く、同様にＭ２ゲート電位より低くなる（したがってソース化する）。この差異がV_tに等しくなると、トランジスタＭ２（７）がターンオンし始め、圧縮が始まる。この第１のタイプの圧縮は、ＲＦスイッチの分路レッグにおけるノーマリオフ型ゲートのターンオン現象によって引き起こされる。ひとたび分路トランジスタＭ２（７）がターンオンすると、出力ノード３の電力は、もはや、線形にスイッチ入力部の電力に従うことはない。第２のタイプのＲＦスイッチ圧縮は、分路トランジスタＭ２（７）のソースおよびドレインが過度の電圧でブレークダウンするときに発生する。サブミクロンのシリコンオンインシュレータ（ＳＯＩ）デバイスに対して、この電圧は、供給電圧を直流約＋１Ｖ超えるだけの可能性がある。ブレークダウンでは、分路デバイスは大量の電力を導通し始め、それにより出力で利用できる電力が減少する。

【0011】

図２に、先行技術による単極双投（ＳＰＤＴ）ＲＦスイッチ２０の簡易図を示す。図２に示すように、先行技術のＲＦスイッチ２０には、最低限、４つのＭＯＳＦＥＴトランジスタ２３、２４、２７および２８が含まれる。トランジスタ２３および２５は、「パス」または「スイッチング」トランジスタとして働き（図１ａ－１ｃのスイッチングＭＯＳＦＥＴトランジスタＭ１（５）と同様に）、これらの関連したそれぞれのＲＦ入力ノードを二者択一的に共通のＲＦノード２５に結合するように構成されている。たとえば、作動している場合（すなわち、「オン」にスイッチされたとき）、スイッチングトランジスタ２３は、第１のＲＦ入力ノード２１への入力である第１の入力信号「RF_1」をＲＦ共通ノード２５へ結合する。同様に、作動している場合、スイッチングトランジスタ２４は、第２のＲＦ入力ノード２２への入力である第２のＲＦ入力信号「RF_2」を、ＲＦ共通ノード２５へ結合する。分路トランジスタ２７および２８は、作動している場合で、それらの関連したＲＦ入力ノードが、ＲＦ共通ノード２５と結合していないとき（すなわち、それらの関連する入力ノードへ接続されているスイッチングトランジスタ（２３または２４）がターンオフされているとき）、それぞれの関連したＲＦ入力ノードを二者択一的にグラウンドへ分路するために働く。

【0012】

図２に示すように、先行技術のＲＦスイッチの動作を制御するために、２つの制御電圧を用いている。「ＳＷ」およびその逆の「ＳＷ＿」の名称がついた制御電圧は、トランジスタ２３、２４、２７および２８の動作を制御する。制御電圧は、選択したトランジスタの対を、二者択一的に作動（ターンオン）または不作動（ターンオフ）にするように調整されている。たとえば、図２に示すように、ＳＷがオン（いくつかの実施形態では、これは、制御電圧を、論理的に「高い」電圧レベル、たとえば、「＋Ｖｄｄ」に設定することによって決定される）のとき、スイッチングトランジスタ２３が作動となり、その関連する分路トランジスタ２８も作動する。しかしながら、ＳＷの逆のＳＷ＿は、第２のスイッチングトランジスタ２４の動作とその関連する分路トランジスタ２７を制御し、また、制御信号ＳＷ＿は、ＳＷがオン（いくつかの実施形態では、これは、ＳＷ＿を－Ｖｄｄに設定することによって決定する）の間、オフなので、これら２つのトランジスタは、この同じ期間には不作動またはターンオフされている。この状態（ＳＷがオンでＳＷ＿がオフ）では、RF_1入力信号は、（作動しているスイッチングトランジスタ２３を介して）ＲＦ共通ポート２５に結合される。第２のスイッチングトランジスタ２４はターンオフされているので、RF_2入力信号は、ＲＦ共通ポート２５からはブロックされる。その上、ＲＦ

$_2$入力信号は、作動している分路トランジスタ２８を介してグラウンドへ分路されるので、ＲＦ共通ポート２５からさらに分離される。トランジスタ設計分野の当業者は容易に理解されるであろうように、ＳＷ制御信号が「オフ」（およびＳＷ＿が「オン」）のときには、ＲＦ$_2$信号は、同じような方法で、ＲＦ共通ポート２５に結合される（そしてＲＦ$_1$信号はブロックさレッグラウンドへ分路される）。

【0013】

様々な性能上の結果を伴って、図２のＳＰＤＦ・ＲＦスイッチ２０などのＲＦスイッチが、バルク相補型金属酸化膜半導体（ＣＭＯＳ）およびガリウムヒ素（ＧａＡｓ）技術を始めとする、異なる素子技術においてこれまで実現されてきた。実は、ほとんどの高性能高周波スイッチは、ＧａＡｓ技術を使用している。先行技術によるＲＦスイッチの実現において、上記のＲＦスイッチ性能特性を改善しようと試みているが、それらの結果は種々雑多であり、集積回路の複雑さと歩留まりの程度も様々である。たとえば、バルクＣＭＯＳ・ＲＦスイッチは、不利なことに、高い挿入損失性能特性、低い圧縮性能特性および不十分な線形性能特性を示す。対照的に、ＧａＡｓ材料の半絶縁性のために、寄生基板抵抗は著しく減少でき、それにより、スイッチ挿入損失を減少できる。同様に、半絶縁ＧａＡｓ基板は、スイッチ分離を改善する。

【0014】

ＧａＡｓＲＦスイッチの実現により、性能特性の向上がもたらされるが、この技術にはいくつかの欠点がある。たとえば、ＧａＡｓ技術では、正常に機能する集積回路の歩留まりが比較的低い。ＧａＡｓＲＦスイッチは、設計および製造が比較的高価になりがちである。加えて、ＧａＡｓスイッチは、上記のように、挿入損失特性を改善するが、ＧａＡｓ基板に存在する遅い表面準位のために、周波数制限が低くなる可能性がある。また、この技術は高いレベルの集積化に向いていないので、ＲＦスイッチに関連するデジタル制御回路をスイッチから「オフチップ」で実現する必要がある。スイッチに関連する低電力回路は、集積するのが困難だと分かっている。これは、全体的なシステムコストまたは製造コスト、サイズおよび複雑さを増加させ、同様に、システムのスループット速度を減少させるので不利である。

【発明の開示】

【発明が解決しようとする課題】

【0015】

したがって、改善した性能特性を有する、ＲＦスイッチおよびＲＦ信号をスイッチングする方法を提供することが望ましい。特に、挿入損失、分離および圧縮が改善したＲＦスイッチを提供することが望ましい。このようなＲＦスイッチは、容易に設計製造ができ、比較的安価に製造され、高いレベルの集積に向いており、低周波から高周波まで適用できるのが望ましい。電力制御回路は、スイッチ機能とともに簡単にオンチップに集積できるようにすべきである。このような集積は、これまで、Ｓｉ基板およびＧａＡｓ基板を用いて実現するのが困難だった。本発明は、このようなＲＦスイッチおよびＲＦ信号のスイッチング方法を提供する。

【課題を解決するための手段】

【0016】

発明の概要

新規なＲＦスイッチ回路およびＲＦ信号のスイッチング方法について説明する。ＲＦスイッチは無線用途に使用可能で、シリコンオンインシュレータ技術で製造できる。一実施形態において、ＲＦスイッチは、極薄シリコン（「ＵＴＳｉ」）基板上に製造する。一実施形態において、ＲＦスイッチには、つぎのものが含まれる。すなわち、ＲＦ信号を受信するための入力部と、ＲＦ信号を受信するための入力部およびＲＦ共通ポートに接続され、スイッチング電圧（ＳＷ）によって制御される第１のスイッチングトランジスタ・グループと、第１のスイッチングトランジスタ・グループおよびＲＦ共通ポートに接続され、スイッチング電圧（ＳＷ＿）によって制御される第２のスイッチングトランジスタ・グループとが含まれ、またＳＷ＿はＳＷの逆であり、第１のスイッチングトランジスタ・グル

ープがオンのとき、第２のスイッチングトランジスタ・グループがオフになる。スイッチングトランジスタ・グループは、作動しているとき、それぞれのＲＦ入力信号を、ＲＦ共通ポートへ二者択一的に接続する。この実施形態において、ＲＦスイッチにはまた、スイッチングトランジスタ・グループに結合され、スイッチング電圧ＳＷおよびＳＷ＿によって制御される分路トランジスタグループが含まれる。分路トランジスタグループは、作動しているとき、それらの関連するＲＦ入力ノードを二者択一的にグラウンドに分路するように働き、それによってＲＦスイッチ分離を改善する。

【0017】

スイッチングおよび分路トランジスタグループには、積層または直列構成でともに接続された１つまたは複数のＭＯＳＦＥＴトランジスタが含まれる。各トランジスタグループ内では、積層トランジスタのゲートは、通常、スイッチング電圧（ＳＷまたはＳＷ＿）によって制御され、このスイッチング電圧は、それぞれのゲート抵抗器を介して各トランジスタゲートに結合される。トランジスタグループ・デバイスの積層およびゲート抵抗器によって、スイッチの圧縮ポイントが増加する。ＭＯＳＦＥＴのゲート抵抗器およびゲート容量によって形成されるＲＣ時定数は、ＲＦ信号の周期よりもずっと長くなるように設計され、ＲＦ電圧が、直列接続デバイス全体で等しく共用されるようにする。この構成によって、ＲＦスイッチの１ｄＢ圧縮ポイントが増加する。

【0018】

完全に集積化されたＲＦスイッチについて説明する。このＲＦスイッチには、デジタルスイッチ制御論理回路と、本発明のＲＦスイッチとともに集積された負の電源電圧発生器とが含まれる。一実施形態では、完全に集積化されたＲＦスイッチによって、先行技術のＲＦスイッチには存在しない、いくつかの機能が提供される。たとえば、一実施形態では、完全に集積化されたＲＦスイッチには、電荷ポンプ回路にクロック入力信号を供給する内蔵式発振器と、他のＲＦスイッチ回路が必要とする負の電源電圧を発生する集積された電荷ポンプ回路と、ＲＦスイッチトランジスタを制御する制御信号を発生するＣＭＯＳ論理回路と、スイッチデバイスの信頼性を増加する、レベルシフト回路および低電流分圧器回路と、ＲＦ信号エネルギを、電荷ポンプ回路およびデジタル制御論理回路から分離するＲＦバッファ回路とが含まれる。電荷ポンプ回路、レベルシフト回路、分圧器およびＲＦバッファ回路のいくつかの実施形態について説明する。本発明のＲＦスイッチによって、挿入損失、スイッチ分離およびスイッチ圧縮が改善される。さらに、本発明のＲＦスイッチによって利用可能となる、より高いレベルの集積のおかげで、本発明を用いることにより、ＲＦシステムの設計および製造コストは減少し、信頼性が高まる。

なお、以下の図面の簡単な説明において、様々な図面の同じ参照符号は、同じ構成要素を示す。

【発明を実施するための最良の形態】

【0019】

発明の詳細な説明

この明細書を通して、明らかにする好適な実施形態および実施例は、本発明に対する限定というよりも、例示的なものとして考えるべきである。

本発明のＲＦスイッチ

本発明は、新規なＲＦスイッチ設計およびＲＦ回路をスイッチングするための方法である。本発明のＲＦスイッチ３０の第１の例示的な実施形態を、図３に示す。図３に示すように、一実施形態において、本発明のＲＦスイッチ３０には、ＭＯＳＦＥＴトランジスタの４つのクラスタまたは「グループ」が含まれる。これらを、トランジスタグループ３３、３４、３７および３８として図３に示す。２つのトランジスタグループには、「パス」または「スイッチング」トランジスタグループ３３および３４が含まれ、２つのトランジスタグループには、分路トランジスタグループ３７および３８が含まれる。各トランジスタグループには、直列構成に配置された１つまたは複数のＭＯＳＦＥＴトランジスタが含まれる。たとえば、図３に示す実施形態では、スイッチンググループ３３には、３つのスイッチングトランジスタM_{33A}、M_{33B}およびM_{33C}が含まれる。同様に、スイッ

チンググループ３４には、３つのスイッチングトランジスタM_{34A}、M_{34B}およびM_{34C}が含まれる。分路グループ３７には、３つのトランジスタM_{37A}、M_{37B}およびM_{37C}が含まれる。同様に、分路グループ３８には、３つのトランジスタM_{38A}、M_{38B}およびM_{38C}が含まれる。トランジスタグループ３３、３４、３７および３８は、３つのＭＯＳＦＥＴトランジスタを含むものとして、図３には示してあるが、ＲＦスイッチ設計分野の当業者は、本発明の範囲または趣旨から逸脱することなく、代替のグループ構成が使用できることを、理解されるであろう。たとえば、以下により詳細に説明するように、本発明の範囲から逸脱することなく、任意の都合のよい数のトランジスタを使用して、図３に示すグループを実現することができる。

【0020】

本発明のＲＦスイッチの一実施形態において、ＭＯＳＦＥＴトランジスタ（たとえば、トランジスタM_{37A}、M_{37B}およびM_{37C}）は、完全に絶縁された基板シリコンオンインシュレータ（ＳＯＩ）技術を用いて実現する。特に、以下により詳細に説明するように、本発明のＲＦスイッチのＭＯＳＦＥＴトランジスタは、「極薄シリコン（Ｕｌｔｒａ－Ｔｈｉｎ－Ｓｉｌｉｃｏｎ）（ＵＴＳｉ）」（本明細書においては、また「極薄シリコンオンサファイア（ｕｌｔｒａｔｈｉｎ　ｓｉｌｉｃｏｎ－ｏｎ－ｓａｐｐｈｉｒｅ）」と呼ぶ）技術を用いて実現する。ＵＴＳｉ製造方法に従い、本発明のＲＦスイッチを実現するために使用するトランジスタは、絶縁サファイアウエハにおけるシリコンの極薄層に形成する。完全な絶縁性のサファイア基板は、非絶縁基板および半絶縁基板に関連する、有害な、基板の結合効果を減少させることにより、本発明によるＲＦスイッチの性能特性を向上させる。たとえば、挿入損失の改善は、トランジスタのオン抵抗を下げ、寄生基板抵抗を減少させることにより実現する。さらに、スイッチ分離は、ＵＴＳｉ技術によって提供される、完全な絶縁基板を用いて改善する。シリコンオンサファイア技術の完全な絶縁性のおかげで、バルクＣＭＯＳおよび他の、従来の集積回路製造技術と比較して、ＲＦスイッチ３０のノード間の寄生キャパシタンスは、著しく減少する。その結果、本発明のＲＦスイッチでは、先行技術のＲＦスイッチ設計と比較して、スイッチ分離が改善される。

【0021】

図３に示すように、図２に関連して上記に説明したスイッチと同様に、トランジスタグループは、２つの制御信号ＳＷおよびその逆のＳＷ＿によって制御される。制御信号は、関連するそれぞれのゲート抵抗器を介して、それぞれのトランジスタのゲートに結合される。たとえば、制御信号ＳＷは、スイッチングトランジスタ・グループ３３における３つのトランジスタ（M_{33A}、M_{33B}およびM_{33C}）の動作を、３つのそれぞれに関連するゲート抵抗器（R_{33A}、R_{33B}およびR_{33C}）を介して制御する。制御信号ＳＷは、入力ノード３３’へ入力され、スイッチングトランジスタ・グループ３３を制御する。ＳＷはまた、入力ノード３８’へ入力され、分路トランジスタグループ３８を制御する。同様に、ＳＷの逆のＳＷ＿は、入力ノード３４’を介して、スイッチングトランジスタ・グループ３４を制御する。ＳＷ＿はまた、入力ノード３７’へ入力され、分路トランジスタグループ３７を制御する。

【0022】

一実施形態において、トランジスタグループの抵抗器には、約３０ＫΩの抵抗器が含まれるが、本発明の趣旨または範囲から逸脱せずに、代替の抵抗値を用いることができる。さらに、本発明のいくつかの実施形態において、ゲート抵抗器には、比較的高い抵抗値を有する任意の抵抗素子が含まれる。たとえば、一実施形態では、逆バイアスダイオードを用いて、ゲート抵抗器を実現してもよい。以下により詳細に説明するように、ゲート抵抗器は、直列接続トランジスタ全体の実効降伏電圧を増加するのに役立つ。

【0023】

制御信号は、トランジスタグループ３３、３４、３７および３８の作動および不作動について制御するように機能し、ＲＦスイッチ３０は、一般に、図２におけるスイッチのアナログトランジスタを制御するのと同様の方法で、ＲＦ信号を通過させるかまたはブロッ

クするように機能する。特に、スイッチングトランジスタ・グループ３３および３４は、パストランジスタまたはスイッチングトランジスタとして機能し、二者択一的に、それぞれの関連するＲＦ入力ノードを共通のＲＦノード３５に結合するように構成されている。たとえば、スイッチングトランジスタ・グループ３３は、作動すると、第１のＲＦ入力ノード３１への入力である第１のＲＦ入力信号「RF_1」を、ＲＦ共通ノード３５に結合する。同様に、スイッチングトランジスタ・グループ３４は、作動すると、第２のＲＦ入力ノード３２への入力である第２のＲＦ入力信号「RF_2」を、ＲＦ共通ノード３５へ結合する。分路トランジスタグループ３７および３８は、作動すると、それらの関連するＲＦ入力ノードが、ＲＦ共通ノード３５と結合していないとき（すなわち、関連する入力ノードに接続されているスイッチングトランジスタ・グループ（３３または３４）がターンオフされているとき）、それぞれの関連するＲＦ入力ノードを、二者択一的にグラウンドへ分路するように働く。

【0024】

制御電圧は、トランジスタグループの選択した組を、二者択一的に作動または不作動にするために接続されている。たとえば、図３に示すように、ＳＷがオンのとき（いくつかの実施形態では、これは、制御電圧ＳＷが、論理的に「高い」電圧レベルに設定されるときに決定される）、スイッチングトランジスタ・グループ３３は作動し（すなわち、グループ３３の全てのトランジスタがターンオンする）、その関連する分路トランジスタグループ３８もまた作動する（すなわち、グループ３８の全てのトランジスタが、ターンオンする）。しかしながら、図２におけるスイッチの動作と同様に、ＳＷの逆のＳＷ＿が、第２のスイッチングトランジスタ・グループ３４およびその関連する分路トランジスタグループ３７を制御するので、これら２つのトランジスタグループは、この期間には不作動になる（すなわち、グループ３４および３７のトランジスタは全て、ターンオフする）。したがって、ＳＷがオンのとき、RF_1 入力信号は、ＲＦ共通ノード３５に結合される。RF_2 入力信号は、スイッチングトランジスタ・グループ３４がオフなので、ＲＦ共通ノード３５からブロックされる。RF_2 入力信号は、作動された分路トランジスタグループ３８を介してグラウンドに分路されるので、ＲＦ共通ノード３５からさらに分離される。ＲＦスイッチ設計分野の当業者は理解されるであろうように、RF_2 信号は、ＳＷ制御信号がオフ（そしてＳＷ＿制御信号がオン）のとき、同様の方法で、ＲＦ共通ノード３５に結合される（そしてRF_1 信号はブロックさレッグラウンドへ分路される）。

【0025】

図３における本発明のＲＦスイッチ３０に示すように、ＭＯＳＦＥＴトランジスタを積層し、ゲート抵抗器を使用する目的の１つは、直列接続トランジスタ全体の降伏電圧を高くすることである。ゲート抵抗器およびＭＯＳＦＥＴのゲート容量によって形成されるＲＣ時定数は、ＲＦ信号の周期よりもずっと長くなるように設計する。それゆえに、ＲＦエネルギは、ゲート抵抗器を介して消散することがほとんどない。この配置により、ＲＦ電圧は、効果的に、直列接続トランジスタ全体で等しく共用される。正味効果として、直列接続デバイス全体の降伏電圧が、個別ＦＥＴの降伏電圧のｎ倍に増加する。この場合、ｎは、直列に接続されるトランジスタの数である。この構成により、本発明のＲＦスイッチ３０の１ｄＢ圧縮ポイントが増加する。

【0026】

スイッチ性能を改善するために、ＲＣ時定数は、ＲＦ信号周期に対して大きなサイズにしなければならない。このことは、主として、ゲートトランジスタ（ゲート抵抗器）を実現するのに使用できるＲの最小値に制約を課すことになる。上記のように、本発明の一実施形態では、Ｒの典型的な値は３０ｋΩであるが、本発明の範囲から逸脱することなく、他の抵抗値を用いることもできる。ＭＯＳＦＥＴゲート入力部は、直流電流を引き寄せないので、この抵抗全体のＩＲ降下のために、デバイスにおけるバイアスが変更されることはない。

【0027】

有利なことに、本発明のＲＦスイッチ３０は、増大した電力レベルの入力信号に対応で

きる。トランジスタグループ（３３、３４、３７および３８）を含むＭＯＳＦＥＴトランジスタの直列配置のおかげで、増大した電力信号を、スイッチ動作に有害な影響を与えることなく、ＲＦ入力ノード（すなわち、入力ノード３１および３２）に供給することができる。トランジスタ設計分野の当業者は、より大きな入力電力レベルには、トランジスタグループごとにトランジスタの数を増やすこと、またはトランジスタの物理的構成を変えることによって対応できることを、理解されるであろう。たとえば、一実施形態において、トランジスタの寸法は、約０．５×２，１００μｍである。しかしながら、本発明の範囲または趣旨から逸脱することなく、代替の構成を用いることができる。

シリコンオンインシュレータ（ＳＯＩ）技術

図３におけるＲＦスイッチの説明において上記で言及したように、ＳＯＩ技術は、絶縁基板の完全な絶縁性のために、ＲＦスイッチの実現においては、魅力がある。周知のように、ＳＯＩは、高性能マイクロエレクトロニクスデバイスの実現、主に、放射線耐性および高速動作を必要とする用途に使用されてきた。ＳＯＩ技術には、たとえば、ＳＩＭＯＸ、絶縁層に接合された薄いシリコン層を有する接合ウエハおよびシリコンオンサファイアが含まれる。上記の望ましいスイッチ性能特性を達成するために、一実施形態において、本発明のＲＦスイッチは、サファイア基板上に製造される。

【0028】

絶縁基板上にデバイスを製造するには、絶縁基板上にシリコンＣＭＯＳデバイスを形成するための効果的な方法を用いる必要がある。サファイアなどの絶縁性支持基板にエピタキシャル堆積した、シリコンなどの単結晶半導体層を含む複合基板を用いることの利点がよく認識され、これらの利点は、サファイア（Al_2O_3）、スピネルまたは他の周知の高絶縁材料などの絶縁材料を基板として用い、デバイス間リーク電流の導電経路が基板を必ず通過するようにすることによって、実現できる。

【0029】

「理想的」なシリコンオンサファイア・ウエハは、その中に能動素子を製造できる十分な厚さを有した、完全単結晶で欠陥のないシリコン層を含む、と定義できる。このシリコン層は、絶縁基板に隣接し、シリコン－絶縁体界面における結晶格子の乱れは最小限であろう。この「理想的」なシリコンオンサファイア・ウエハを製造しようとする初期の試みは、多くの際立った問題のために挫折した。これらの問題は、（１）最初のエピタキシャルシリコン堆積に使用する高温、およびその後、シリコン層をアニールして、その中の欠陥を減少するために使用する高温の結果として、汚染物、特にｐ型ドーパントのアルミニウムがかなりエピタキシャル堆積シリコン層に侵入するすること、ならびに（２）様々な打込み、アニールおよび／または再成長の方法を通して問題となる高温を避けたときの、エピタキシャルシリコン層の不十分な結晶特性として要約できる。

【0030】

要求の厳しいデバイス用途に適した高品質のシリコン薄膜を、サファイア基板上に製造できることが分かっているが、このときの方法には、サファイア基板上におけるシリコン層のエピタキシャル堆積、シリコン層に埋込みアモルファス領域を形成するための低温イオン打込みおよび約９５０℃未満の温度における複合物のアニールが含まれる。

【0031】

このようなシリコンオンサファイア・デバイスを製造する例および方法が、以下の明細書に記載されている。それらは、米国特許第５，４１６，０４３号明細書（「超薄膜シリコンオンサファイアウエハ上に製造される最小電荷ＦＥＴ」（Ｍｉｎｉｍｕｍ ｃｈａｒｇｅ ＦＥＴ ｆａｂｒｉｃａｔｅｄ ｏｎ ａｎ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｗａｆｅｒ））、米国特許第５，４９２，８５７号明細書（「単一の極薄膜シリコンオンサファイアチップ上の高周波ワイヤレス通信システム」（Ｈｉｇｈ－ｆｒｅｑｕｅｎｃｙ ｗｉｒｅｌｅｓｓ ｃｏｍｍｕｎｉｃａｔｉｏｎ ｓｙｓｔｅｍ ｏｎ ａ ｓｉｎｇｌｅ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｃｈｉｐ））、米国特許第５，５７２，０４０号明細書（「単一の極薄膜シリコンオンサファイアチップ上の高周波ワイヤレス通信システム」（Ｈｉｇｈ－ｆｒｅ

ｑｕｅｎｃｙ ｗｉｒｅｌｅｓｓ ｃｏｍｍｕｎｉｃａｔｉｏｎ ｓｙｓｔｅｍ ｏｎ ａ ｓｉｎｇｌｅ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｃｈｉｐ））、米国特許第５，５９６，２０５号明細書（「単一の極薄膜シリコンオンサファイアチップ上の高周波ワイヤレス通信システム」（Ｈｉｇｈ－ｆｒｅｑｕｅｎｃｙ ｗｉｒｅｌｅｓｓ ｃｏｍｍｕｎｉｃａｔｉｏｎ ｓｙｓｔｅｍ ｏｎ ａ ｓｉｎｇｌｅ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｃｈｉｐ））、米国特許第５，６００，１６９号明細書（「超薄膜シリコンオンサファイアウエハ上に製造される最小電荷ＦＥＴ」（Ｍｉｎｉｍｕｍ ｃｈａｒｇｅ ＦＥＴ ｆａｂｒｉｃａｔｅｄ ｏｎ ａｎ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｗａｆｅｒ））、米国特許第５，６６３，５７０号明細書（「単一の極薄膜シリコンオンサファイアチップ上の高周波ワイヤレス通信システム」（Ｈｉｇｈ－ｆｒｅｑｕｅｎｃｙ ｗｉｒｃｌｅｓｓ ｃｏｍｍｕｎｉｃａｔｉｏｎ ｓｙｓｔｃｍ ｏｎ ａ ｓｉｎｇｌｃ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｃｈｉｐ））、米国特許第５，８６１，３３６号明細書（「単一の極薄膜シリコンオンサファイアチップ上の高周波ワイヤレス通信システム」（Ｈｉｇｈ－ｆｒｅｑｕｅｎｃｙ ｗｉｒｅｌｅｓｓ ｃｏｍｍｕｎｉｃａｔｉｏｎ ｓｙｓｔｅｍ ｏｎ ａ ｓｉｎｇｌｅ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｃｈｉｐ））、米国特許第５，８６３，８２３号明細書（「シリコンオンインシュレータにおける自己整合されたエッジ制御」（Ｓｅｌｆ－ａｌｉｇｎｅｄ ｅｄｇｅ ｃｏｎｔｒｏｌ ｉｎ ｓｉｌｉｃｏｎ ｏｎ ｉｎｓｕｌａｔｏｒ））、米国特許第５，８８３，３９６号明細書（「単一の極薄膜シリコンオンサファイアチップ上の高周波ワイヤレス通信システム」（Ｈｉｇｈ－ｆｒｅｑｕｅｎｃｙ ｗｉｒｅｌｅｓｓ ｃｏｍｍｕｎｉｃａｔｉｏｎ ｓｙｓｔｅｍ ｏｎ ａ ｓｉｎｇｌｅ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｃｈｉｐ））、米国特許第５，８９５，９５７号明細書（「超薄膜シリコンオンサファイアウエハ上に製造される最小電荷ＦＥＴ」（Ｍｉｎｉｍｕｍ ｃｈａｒｇｅ ＦＥＴ ｆａｂｒｉｃａｔｅｄ ｏｎ ａｎ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｗａｆｅｒ））、米国特許第５，９２０，２３３号明細書（「擬似側波帯を減少するためのサンプリング回路を含む位相同期ループ」Ｐｈａｓｅ ｌｏｃｋｅｄ ｌｏｏｐ ｉｎｃｌｕｄｉｎｇ ａ ｓａｍｐｌｉｎｇ ｃｉｒｃｕｉｔ ｆｏｒ ｒｅｄｕｃｉｎｇ ｓｐｕｒｉｏｕｓ ｓｉｄｅ ｂａｎｄ）、米国特許第５，９３０，６３８号明細書（「極薄シリコンオンインシュレータ上に低寄生抵抗を製造する方法」（Ｍｅｔｈｏｄ ｏｆ ｍａｋｉｎｇ ａ ｌｏｗ ｐａｒａｓｔｉｃ ｒｅｓｉｓｔｏｒ ｏｎ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｉｎｓｕｌａｔｏｒ））、米国特許第５，９７３，３６３号明細書（「極薄シリコンオンインシュレータ上の、短縮されたＰチャネル長を有するＣＭＯＳ回路」（ＣＭＯＳ ｃｉｒｃｕｉｔｒｙ ｗｉｔｈ ｓｈｏｒｔｅｎｅｄ Ｐ－ｃｈａｎｎｅｌ ｌｅｎｇｔｈ ｏｎ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｉｎｓｕｌａｔｏｒ））、米国特許第５，９７３，３８２号明細書（「絶縁体上における極薄半導体上のキャパシタ」（Ｃａｐａｃｉｔｏｒ ｏｎ ｕｌｔｒａｔｈｉｎ ｓｅｍｉｃｏｎｄｕｃｔｏｒ ｏｎ ｉｎｓｕｌａｔｏｒ））および米国特許第６，０５７，５５５号明細書（「超薄膜シリコンオンサファイアウエハ上に製造される最小電荷ＦＥＴ」（Ｈｉｇｈ－ｆｒｅｑｕｅｎｃｙ ｗｉｒｅｌｅｓｓ ｃｏｍｍｕｎｉｃａｔｉｏｎ ｓｙｓｔｅｍ ｏｎ ａ ｓｉｎｇｌｅ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｃｈｉｐ））である。これらの参照特許は全て、極薄シリコンオンサファイア集積回路設計および製造に関するその教示全体において、本明細書に援用している。

【００３２】

上記で参照した特許に記載された方法を用いて、電子デバイスを、絶縁合成サファイアウエハ上のシリコン極薄層に形成することができる。シリコン層の厚さは、典型的には、１５０ｎｍ未満である。このような「極薄」シリコン層により、絶縁サファイア基板の利点が最大化され、単一集積回路上に多数の機能を集積することが可能となる。厚いシリコ

ンでは必要とされる従来のトランジスタ分離ウェルが必要でなくなり、トランジスタ処理が簡略化され、回路密度が増大する。これらの、上記で参照した方法およびデバイスを、以前の厚いシリコン実施形態と区別するために、本明細書では、これらを一括して「極薄シリコンオンサファイア」と呼ぶ。

【0033】

本発明のいくつかの好適な実施形態では、ＭＯＳトランジスタは、米国特許第５，４１６，０４３号、第５，４９２，８５７号、第５，５７２，０４０号、第５，５９６，２０５号、第５，６００，１６９号、第５，６６３，５７０号、第５，８６１，３３６号、第５，８６３，８２３号、第５，８８３，３９６号、第５，８９５，９５７号、第５，９２０，２３３号、第５，９３０，６３８号、第５，９７３，３６３号、第５，９７３，３８２号および第６，０５７，５５５号の各明細書に開示された方法により、極薄シリコンオンサファイアに形成する。しかしながら、本発明の趣旨または範囲から逸脱することなしに、極薄シリコンオンサファイア集積回路を製造する他の周知の方法を用いることができる。

【0034】

これらの特許に記載され、特許請求されているように、要求の厳しいデバイス用途に適した高品質のシリコン薄膜が、絶縁基板上へのシリコン層のエピタキシャル堆積、シリコン層に埋込みアモルファスを形成するための低温イオン打込みおよび約９５０℃未満の温度での複合物のアニールを含む方法により、絶縁基板上に製造することができる。約９５０℃を超える温度にシリコン層をさらすどのような処理も、酸化周囲環境において実施する。トランジスタを形成するシリコン薄膜には、意図的ではなくドープされた領域に、約$5\times10^{11}\ cm^{-2}$未満の電気的に活性状態の面積密度がある。

【0035】

上記で言及したように、ＵＴＳｉ基板は、ＲＦ用途には特に望ましい。なぜなら、完全な絶縁基板は、従来の基板（すなわち、完全には絶縁性でない）に関連した基板結合の有害な影響を減少するからである。結果として、一実施形態では、図３のＲＦスイッチ３０は、ＵＴＳｉ基板上に製造する。

ＲＦスイッチ設計トレードオフ

図３に関連して上記で説明した、本発明のＲＦスイッチ３０を設計し実現するときに、いくつかの設計パラメータおよびトレードオフを考慮すべきである。本発明のＲＦスイッチは、所望のシステム設計要求およびＲＦスイッチ性能目標を満たすか超えるように仕立てることができる。ＲＦスイッチ設計に影響を与える設計トレードオフおよび考慮すべきことについて、ここで説明する。

【0036】

図３に関連して上記で説明したように、ＲＦスイッチ３０は、「Ｎ型」でも「Ｐ型」でもよいが、ＭＯＳＦＥＴトランジスタを用いて実現する。しかしながら、ＣＭＯＳ技術においてＲＦスイッチを実現するには、Ｎチャネルトランジスタが好ましい。Ｎチャネルトランジスタが好ましいのは、一定のトランジスタサイズに対して、Ｎチャネルトランジスタの「オン」抵抗が、Ｐチャネルトランジスタの場合よりも、ずっと小さいからである。これは、正孔に対して電子の、シリコンにおける移動度が高いことによる。制御電圧は、「オン」トランジスタのオン抵抗が確実に減少するように選択する。制御電圧はまた、「オフ」トランジスタが、不作動にされたとき、確実にオフとどまるように選択する。

【0037】

トランジスタ設計分野においては周知のように、ＮチャネルＭＯＳトランジスタにおいては、「オン」抵抗は、トランジスタゲートに印加する電圧とトランジスタソースに印加する電圧間の差異に反比例する。この電圧は、通常、「Ｖｇｓ」（ゲートーソース電圧）と呼ばれる。容易に気づくことだが、入力ポート（たとえば、図３における第１のＲＦ入力ノード３１）において、したがって、ＲＦ共通ポート３５においてＲＦ信号（Ｖｓ）の大きさが増すにつれて、オントランジスタのＶｇｓが減少する（たとえば、ＲＦ１信号の大きさが増加するにつれて、スイッチングトランジスタ・グループ３３におけるトランジ

スタＭ３３$_A$のＶｇｓが減少する）。このために、ゲート制御電圧（たとえば、入力ノードＳＳ’のＳＷ）を可能な限り正にすべきだというになる。しかし残念ながら、信頼性の懸念から、ゲート制御電圧を正にできる程度が制限される。

【0038】

同様の懸念が「オフ」トランジスタに対しても存在する。典型的なＲＦスイッチの適用では、ＲＦ入力信号（たとえば、ＲＦ１入力信号）が一般にゼロ基準電圧をめぐって振動することに注目することは大切である。オフトランジスタ（たとえば、シャントトランジスタグループ３７のトランジスタ）は、ＲＦ入力信号の正および負の電圧偏移の間、不作動またはターンオフのままにとどまらなくてはならない。このことから、オフトランジスタのゲート制御電圧（たとえば、ＳＷ＿制御電圧信号）をできる限り負にすべきだということになる。再び、信頼性の懸念から、ゲート制御電圧を負にできる程度が制限される。

【0039】

ＣＭＯＳスイッチにとって、オフトランジスタの設計によって、また、スイッチの１ｄＢ圧縮ポイントが制限される。トランジスタ設計分野においては周知のように、ＭＯＳトランジスタでは、そのソースとドレイン間に基本的な降伏電圧がある。デバイス両端の電位がこの降伏電圧を超えると、トランジスタをオフ状態に維持しようとしているゲート電位が存在するときでも、ソースとドレイン間に高電流が流れる。スイッチにおける圧縮の改善は、トランジスタの降伏電圧を増加することによっと、達成することができる。高降伏電圧を有するＭＯＳトランジスタを製造する方法の１つは、ゲート長を増加することである。残念なことに、ゲート長の増加により、デバイスのチャネル抵抗が不都合にも増加し、それにより、デバイスの挿入損失が増加する。チャネル抵抗は、デバイスの幅を広くすることによって減少できるが、これはまた、スイッチ分離を低下させる。したがって、ＭＯＳスイッチに、トレードオフが存在する。

【0040】

図３における本発明のＲＦスイッチ３０に関連して上記に説明したように、トランジスタを直列構成に積層して、スイッチの１ｄＢ圧縮ポイントを改善する。比較的高い値のゲート抵抗器と、トランジスタグループにおけるトランジスタの積層構成との組み合わせにより、直列接続トランジスタ全体の実効降伏電圧を増加する。スイッチ素子の設計および製造においては、ＲＣ時定数（ゲート抵抗器の抵抗値およびＭＯＳＦＥＴのゲート容量によって決定される）が、ＲＦスイッチ３０が処理するＲＦ信号の周期よりもずっと長くなるようにする。上記のように、積層構成および比較的高抵抗のゲート抵抗器の正味効果として、直列接続トランジスタ全体の降伏電圧が、個別トランジスタにおける降伏電圧のｎ倍の率で増加する（ここで、ｎは、トランジスタグループにおいて、直列に接続したトランジスタの数に等しい）。

【0041】

設計上さらに考慮すべきことは、従来のバルクＣＭＯＳトランジスタにおいて使用されている「ボディタイ」に関する。トランジスタ設計分野においては周知のように、ボディタイは、デバイスをウェルまたは基板のどちらかに結合する。ウェル－基板接合部は、常に逆バイアスをかけられたままにしなければならない。ソース－ボディおよびドレイン－ボディ接合部は、常に逆バイアスをかけられたままにしなければならない。一般に、バルクＣＭＯＳ設計において、ウェル（Ｎウェル技術の）は、回路に印加される最大の正の電位に結合される。基板（Ｐウェル技術の）は、回路に印加される最大の負の電位に結合される。ＲＦ入力信号は、グラウンドの上下を対称的に振動するので、ＣＭＯＳスイッチ設計は、挿入損失、分離および１ｄＢ圧縮ポイントについて、不十分な性能を示す。これらおよび上記の理由で、本発明のＲＦスイッチ３０は、絶縁基板上に実現するのが好ましい。

【0042】

本発明のＲＦスイッチを絶縁基板上に実現することにより、スイッチ分離の改善および挿入損失の減少などいくつかの利点が提供される。ＵＴＳｉ技術を用いて本発明のＲＦスイッチを実現することにより、さらなる利点が得られる。たとえば、先行技術のＲＦスイ

ッチをＧａＡｓに実現することと比較して、ＵＴＳｉを用いることにより、集積回路歩留まりの改善、製造コストの減少および集積レベルの増加が達成される。集積回路設計分野において周知のように、ＧａＡｓは、高レベルの集積化には向いていない。したがって、ＲＦスイッチの動作および機能に関連したデジタル制御回路および他の回路（負電圧電力供給発生器回路、レベルシフト回路、低電流分圧器回路およびＲＦバッファ回路など）は、オフチップで実現しなければならないことがしばしばある（すなわち、これらの機能は、ＲＦスイッチと簡単には集積できない）。これは、コストの増加および先行技術により実現したＲＦスイッチの性能低下へとつながる。

【0043】

対照的に、本ＲＦスイッチの発明に従い、ＵＴＳｉ技術を用いて、ＲＦスイッチの正常な動作および機能のために必要な回路を、スイッチ自体と同じ集積回路に一緒に実現できる。たとえば、以下により詳細に説明するように、ＵＴＳｉ技術でＲＦスイッチを実現することにより、ＲＦスイッチは、負電圧発生器およびＲＦスイッチの動作を制御するのに必要なＣＭＯＳ制御論理回路とともに同じ集積回路に集積できる。スイッチの動作を制御するのに必要な制御線の減少のおかげで、ＲＦスイッチの複雑さもまた減少する。有利なことに、ＲＦスイッチ制御論理回路は、低電圧ＣＭＯＳトランジスタを用いて実現できる。さらに、高電力ＲＦスイッチ実現のためであっても、比較的低電力の外部電源を用いて、本発明のＲＦスイッチに電力を供給することができる。この特徴は、先行技術によるＧａＡｓの実現に比較して有利である。ＧａＡｓの場合には、比較的高電力の外部電源ならびに正および負両方の電力供給を実現するのに必要な電力発生回路を使用することが必要だからである。たとえば、図４～１２に関連して以下に説明する例示的な実施形態では、本発明のＲＦスイッチは、単一の３Ｖ外部電源を１つ必要とするだけである。先行技術によるスイッチでは、典型的に、少なくとも１つの６Ｖ外部電源ならびに正および負の電力供給を実現するための外部電圧発生回路が必要である

完全に集積化されたＲＦスイッチ

図４に、本発明に従って製造し、例示的で、完全に集積化されたＲＦスイッチ１００の簡易ブロック図を示す。図４に示すように、完全に集積化されたＲＦスイッチ１００には、上記において図３で説明した本発明のＲＦスイッチ３０（図４においては、簡略化した図式表現で示す）ＣＭＯＳ制御論理回路１１０および負電圧発生器回路１２０（「電荷ポンプ」回路を用いて、一実施形態において実現する）が含まれる。制御信号１３０は、ＣＭＯＳ論理回路ブロック１１０入力する。一実施形態では、制御信号１３０は、０ボルトから＋Ｖｄｄの範囲におよぶが、デジタル論理回路設計分野の当業者は、本発明の範囲または趣旨から逸脱することなく、他の論理回路レベルが使用できることを理解されるであろう。上記に提示した理由で、一実施形態では、完全に集積化されたＲＦスイッチ１００は、ＵＴＳｉ基板上に製造する。しかし、他の絶縁基板技術を用いることもできる。

【0044】

以下により詳細に説明するように、完全に集積化されたＲＦスイッチ１００には、図２における先行技術のＲＦスイッチにはないいくつかの機能および特徴が含まれる。たとえば、本発明のＲＦスイッチ３０（図３に関連して上記に説明したように、新規な、トランジスタの積層およびゲートトランジスタ（ゲート抵抗）構成を用いる）に加えて、完全に集積化されたＲＦスイッチ１００では、本発明のスイッチと同じ集積回路上に、負電圧発生器およびＲＦスイッチ制御機能を一緒に集積する。以下により詳細に説明するように、完全に集積化されたＲＦスイッチ１００には、クロック入力信号を電荷ポンプ回路に供給する内蔵式発振器、他のＲＦスイッチ回路が必要とする負の電源電圧を発生する集積化電荷ポンプ回路、ＲＦスイッチトランジスタを制御する制御信号を発生するＣＭＯＳ論理回路、スイッチトランジスタの、ゲートードレイン、ゲートーソースおよびドレインーソース電圧を減少することにより、信頼性を増加させるレベルシフト回路ならびに電荷ポンプ回路およびデジタル制御論理回路からＲＦ信号エネルギを分離するＲＦバッファ回路が含まれる。これらの各回路は、関連する図を参照して、以下により詳細に説明する。

負電圧発生器－電荷ポンプ－第１の実施形態

図４に示すように、完全に集積化されたＲＦスイッチ１００の一実施形態には、負電圧発生器すなわち電荷ポンプ１２０が含まれる。負電圧発生器１２０によって、完全に集積化されたＲＦスイッチ１００の他の回路が必要とする負の電源電圧（以下、「－Ｖｄｄ」と記す）を発生する。２つの入力セット、すなわち、正の直流電源電圧信号（Ｖｄｄ）１２２およびクロック入力（単一の入力信号「Ｃｌｋ」として図に示す）１２４を、負電圧発生器１２０に供給する。クロック入力１２４は、図４で単一の入力信号として示してあるが、以下に図５ｂに関連して説明するように、本発明におけるＲＦスイッチのいくつかの実施形態では、クロック入力１２４は、２つまたはそれを超えるクロック入力信号を含むことができる。

【0045】

さらに、図４に示す実施形態では、負電圧発生器回路１２０への入力である正の供給電圧には、直流３Ｖ電力供給源が含まれる。しかしながら、本発明の範囲または趣旨から逸脱することなく、他の電力供給レベルを用いてもよい。たとえば、所望ならば、直流３．５Ｖ、直流５Ｖまたは任意の他の都合のよい正の電力供給を、図４の負電圧発生器回路１２０への入力とすることができる。正の電力供給信号は、典型的には、外部の低電力供給源により発生する。

【0046】

本発明の一実施形態において、図４の負電圧発生器１２０は、電荷ポンプ回路を用いて実現する。図５ａに、図４の負電圧発生器１２０における例示的な一実施形態の簡易ブロック図を示す。図５ａの簡易ブロック図に示すように、負電圧発生器には、発振器２０２、クロック発生器回路２０４および本発明の電荷ポンプ回路２０６が含まれる。発振器２０２の出力は、クロック発生器回路２０４に入力される。クロック発生器回路２０４の出力は、電荷ポンプ回路２０６に入力される。負電圧発生器１２０により、完全に集積化されたＲＦスイッチ１００の他の回路が使用する負の電源電圧を供給する。

【0047】

先行技術によるＲＦスイッチの多くでは、不利なことに、負の電源電圧は、ＲＦスイッチ回路に対して外部の回路で発生しなければならない。他のＲＦスイッチの実現では、ＲＦ入力信号の直流値を、印加したバイアス電圧の中間点にシフトするために必要な結合アプローチを用いる。このアプローチでは一般に、ＦＥＴゲートドライブがこのレベルシフトのために実効的に半分になるため、比較的高いバイアス電圧を印加する必要がある。バイアス電圧を増加しない場合、このことにより、スイッチ挿入損失に否定的な影響がもたらされる。なぜなら、これによりゲートドライブが減少し、それによってＦＥＴチャネル抵抗が増加するからである。

【0048】

これらの問題に対処するために、完全に集積化されたＲＦスイッチ１００の一実施形態では、図５ｂに詳細に示す、本発明の電荷ポンプ回路２０６を使用する。図５ｂに示すように、電荷ポンプ回路２０６の第１の実施形態には、２つのＰチャネルＭＯＳＦＥＴトランジスタ２０８および２１０が含まれ、これらは、２つのＮチャネルＭＯＳＦＥＴトランジスタ２１２および２１４に直列に接続されている。電荷ポンプ回路２０６の左レッグ（第１のＮチャネルトランジスタ２１２に直列に接続された、第１のＰチャネルトランジスタ２０８を含む）は、電荷ポンプ回路の右レッグ（第２のＮチャネルトランジスタ２１４に直列に接続された、第２のＰチャネルトランジスタ２１０を含む）に、第１のキャパシタＣｐ２１６を用いて結合されている。図示のように、第２のＮチャネルトランジスタ２１４のソースは、出力キャパシタである第２のキャパシタＣ２１８に結合されている。２つの非重複クロック制御信号「Ｃｌｋ１」および「Ｃｌｋ２」は、トランジスタ２０８、２１０、２１２および２１４の動作を制御するために用いる。たとえば、図５ｂに示すように、「Ｃｌｋ１」の逆の「Ｃｌｋ１＿」は、Ｐチャネルトランジスタ２０８および２１０のゲートを制御する。他方の非重複クロック制御信号「Ｃｌｋ２」は、図示のように、Ｎチャネルトランジスタ２１２および２１４のゲートを制御する。

【0049】

電荷ポンプ２０６は、トランジスタゲートを駆動する非重複クロック制御信号Ｃ１ｋ１およびＣ１ｋ２を用いて、２つのキャパシタ（Ｃｐ２１６および出力キャパシタＣ２１８）を交互に充電および放電することにより、負の電源電圧（－Ｖｄｄ）を発生する。負の電源電圧－Ｖｄｄは、キャパシタＣ２１８に充電した電荷から発生する。一実施形態では、パルスシフト回路（図示せず）を用いて、電荷ポンプを駆動するパルス列（すなわち、パルス列は、クロック入力信号Ｃ１ｋ１およびＣ１ｋ２として入力される）を発生する。パルス列が、電荷ポンプ２０６に印加されるので、キャパシタＣｐ２１６は、正の電力供給Ｖｄｄを印加され、つぎにキャパシタＣ２１８を越えて反対方向に放電され、負の電源電圧－Ｖｄｄを生成する。電荷ポンプのどのトランジスタも、いずれのソース／ドレインノード間でも、Ｖｄｄを超えるものを避ける必要がなく、したがって、電荷ポンプ２０６の信頼性が大いに高まる。

【0050】

本発明の電荷ポンプ回路２０６の一実施形態において、出力Ｃ２１８のキャパシタンスは約２００ｐＦであり、Ｃｐ２１６のキャパシタンスは約５０ｐＦである。電荷ポンプ設計分野の当業者は、本発明の範囲または趣旨から逸脱することなく、他のキャパシタンス値を使用できることを、理解されるであろう。

図５ａの簡易ブロック図に示すように、一実施形態において、２つの非重複クロック信号は、内部発振器２０２が発生する発振信号から派生する。図５ａに示すように、発振器２０２は、発振信号を、クロック発生器回路２０４に入力し、今度はこの回路が、電荷ポンプトランジスタゲートを制御する２つの非重複クロック信号を（任意で便利な、周知の方法で）発生する。本発明の完全に集積化されたＲＦスイッチ１００の一実施形態では、発振器２０２には、（数ＭＨｚのオーダの）比較的低周波の発振器が含まれる。この実施形態では、発振器には、簡単な弛張発振器が含まれる。しかしながら、集積回路分野の当業者は、本発明の趣旨または範囲から逸脱することなく、他のタイプの発振器を用いて本発明を実施できることを、理解されるであろう。

【0051】

図５ｃに、経時的に変化する、２つの非重複クロック信号Ｃ１ｋ１およびＣ１ｋ２の電圧振幅を示す。図５ｃに示すように、２つの非重複クロック信号は、－ＶｄｄからＶｄｄまでの電圧振幅で変化する。一実施形態において、クロック信号は、直流－３Ｖから直流＋３Ｖまで変化する。このように調整することによって、電荷ポンプ２０６の効率を改善する。

【0052】

電荷ポンプトランジスタ２０８、２１０、２１２および２１４には、有利なことに、単一閾値のＮチャネル（２１２および２１４）およびＰチャネル（２０８および２１０）デバイスが含まれる。従来の電荷ポンプ回路は、複数閾値レベルデバイスの使用を必要とする。したがって、これら従来のものを実現するには、図５ｂにおける本発明の電荷ポンプ回路２０６よりも、設計が複雑でコストがかかった。本発明の電荷ポンプ２０６の一実施形態において、Ｐチャネルトランジスタ２０８および２１０の幅は約２０μｍ、長さは約０．８μｍである。Ｎチャネルトランジスタ２１２および２１４の幅は約８μｍ、長さは約０．８μｍである。集積回路設計分野の当業者は、本発明の範囲または趣旨から逸脱することなく、他の寸法のトランジスタが使用できることを、理解されるであろう。本発明の電荷ポンプ回路２０６は、非常に効率的であり、温度およびプロセスの変動にもかかわらず、申し分なく動作する。

レベルシフト回路

電荷ポンプ回路は、この回路に印加された電源電圧を効率的に２倍にするので、これらの高い電圧に関連した、電位の信頼性問題に注意を払わなければならない。トランジスタの信頼性を高めるような方法で電荷ポンプを実現するために、レベルシフト回路を用いて、トランジスタのゲート－ソース電圧、ゲート－ドレイン電圧およびドレイン－ソース電圧を、許容できるレベルに制限する。

【0053】

本発明に従って作成された発明的なレベルシフト回路３００を図６ａに示す。レベルシフト回路３００を用いて、典型的または「普通の」デジタル入力信号（デジタル信号は、典型的にはグラウンド（ＧＮＤ）から＋Ｖｄｄの範囲におよぶ）を、－Ｖｄｄから＋Ｖｄｄの範囲におよぶように変換またはシフトする。それにより、完全に集積化されたＲＦスイッチの信頼性が高まる。本発明の一実施形態では、制御信号は、直流－３Ｖから直流＋３Ｖの範囲へシフトされるが、ＲＦスイッチ制御分野の当業者は、本発明の趣旨または範囲から逸脱することなく、他のレベルシフト電圧範囲が使用できることを理解されるであろう。

【0054】

図６ａに示すように、本発明のレベルシフト回路３００（以後は、レベルシフタ３００と呼ぶ）には、フィードバック構造に結合された複数のインバータが含まれる。特に、図６ａに示す実施形態では、レベルシフタ３００には、２つのグループのインバータが含まれ、これらのインバータを用いて、第１および第２のシフトした出力信号、すなわち、第１の出力ノード３１４の「ｏｕｔ」およびその逆の、第２の出力ノード３１６の「ｏｕｔ＿」を発生する。第１のインバータグループには、インバータ３０２、３０４および３０６が含まれる。第２のインバータグループには、インバータ３０８、３１０および３１２が含まれる。典型的または「普通の」デジタル入力信号（すなわち、ＧＮＤから＋Ｖｄｄの範囲にわたるデジタル入力信号）は、第１のインバータ３２０の入力ノード３１８で、レベルシフタ３００へ入力される。第１のインバータ３２０は、（出力ノード３２４で）第１の入力信号「ｉｎ」を発生し、この信号が、第２のインバータ３２２へ入力される。第２のインバータ３２２は、第１の入力信号「ｉｎ」の逆である第２の入力信号「ｉｎ＿」を、出力ノード３２６で発生する。したがって、第１および第２のインバータ３２０および３２２は、上記の２つのインバータグループへ入力される信号を発生する。たとえば、第１の入力信号「ｉｎ」は、インバータ３０２の入力部３２８に結合される。同様に、第２の入力信号「ｉｎ＿」は、インバータ３０８の入力部３３０に結合される。

【0055】

第１のインバータグループの出力「ｏｕｔ」は、第１の出力インバータ３０６によって発生され、第１の出力ノード３１４へ供給される。第２のインバータグループの出力「ｏｕｔ＿」は、第２の出力インバータ３１２によって発生され、第２の出力ノード３１６に供給される。２つのレベルシフタ出力「ｏｕｔ」および「ｏｕｔ＿」は、図４の完全に集積化されたＲＦスイッチ１００の他の回路へ入力される。たとえば、一実施形態では、第１の出力「ｏｕｔ」は、スイッチングトランジスタ・グループ３３および分路トランジスタグループ３８におけるデバイスのゲートに結合される（すなわち、図６ａの第１の出力ノード３１４における「ｏｕｔ」信号は、入力ノード３３’および３８’で、図３の「ＳＷ」制御入力信号に結合され、それにより、図３に関連して上記で説明したように、スイッチングトランジスタ・グループ３３および分路トランジスタグループ３８の動作を制御する）。同様に、この実施形態では、第２のレベルシフタ出力「ｏｕｔ＿」は、図３の「ＳＷ＿」制御入力信号に（入力ノード３４’および３８’で）結合され、それにより、上記のように、スイッチングトランジスタ・グループ３４および分路トランジスタグループ３７を制御する

図６ａのレベルシフタ３００は、入力信号（すなわち、入力ノード３１８で供給される入力信号）の直流レベルをシフトし、一方、入力信号の周波数応答を不変にする。レベルシフタ３００は、完全に集積化されたＲＦスイッチ１００のシリコンオンインシュレータ基板での実現によって提供されるフローティング技術を十分に利用する。レベルシフタ３００のインバータは、差動バイアスに基づいて動作する。すなわち、レベルシフタは、２つの電圧信号の差異に基づいてデジタル入力信号をシフトする。特に、インバータ（たとえば、出力インバータ３０６および３１２など）に供給される電力供給信号間の差異が、Ｖｄｄのオーダである限りは、レベルシフタ３００は、確実に機能して、入力信号を－Ｖｄｄと＋Ｖｄｄ間の範囲でシフトする。一実施形態では、Ｖｄｄは直流３Ｖに等しい。この実施形態において、レベルシフタ３００のインバータ（たとえば、出力インバータ３０

６および３１２）を構成するトランジスタでは、それらのソース／ドレインノード間に印加される電圧は、直流３Ｖよりも大きくはならない。このことによって、トランジスタデバイスの信頼性が増加する。

【0056】

再び図６ａを参照すると、レベルシフタはフィードバック法を用いて、デジタル入力信号を、－ＶｄｄからＶｄｄの範囲の電圧レベルにシフトする。特に、第２の出力ノード３１６における、第２のインバータグループ（３０８、３１０および３１２）の出力（すなわち、「ｏｕｔ＿」信号）が、インバータ３０４の入力部で、第１のインバータグループの入力部へのフィードバックとして供給される。同様に、第１の出力ノード３１４における、第１のインバータグループ（３０２、３０４および３０６）の出力（すなわち、「ｏｕｔ」出力信号）が、第２のインバータグループ、特に、インバータ３１０への入力として供給される。

【0057】

入力ノード３１８におけるデジタル入力信号が論理的に「高い」状態になるとき（すなわち、いくつかの実施形態では、入力信号がＧＮＤから＋ＶｄｄＶに遷移するとき）、「ｉｎ」信号（ノード３２４における）および「ｉｎ＿」信号（ノード３２６における）は、それぞれレッグラウンド（たとえば、直流０Ｖ）およびＶｄｄ（たとえば、直流３Ｖ）になる。第１の出力ノード３１４の「ｏｕｔ」信号は、＋Ｖｄｄになる。同時に、第２の出力ノード３１６の「ｏｕｔ＿」信号は、－Ｖｄｄになる。（インバータ３０４の入力部へフィードバックされる「ｏｕｔ＿」およびインバータ３１０の入力部へフィードフォワードされる「ｏｕｔ」の）フィードバック構成により、レベルシフタ３００における状態の迅速な変化を確実にする。レベルシフタ３００は、入力信号が論理的に高い状態から論理的に低い状態に遷移（すなわち、＋ＶｄｄからＧＮＤに遷移）するときにも、同様に働く。入力ノード３１８のデジタル入力信号が、論理的に「低い」状態になると、「ｉｎ」信号（ノード３２４における）および「ｉｎ＿」信号（ノード３２６における）は、それぞれ、Ｖｄｄ（たとえば、直流３Ｖ）およびグラウンドになる。第１の出力ノード３１４における「ｏｕｔ」信号は、－Ｖｄｄになる。同時に、第２の出力ノード３１６における「ｏｕｔ＿」信号は、＋Ｖｄｄになる。再びフィードバックにより、レベルシフタ３００における状態の迅速な変化を確実にする。接地により、レベルシフタインバータにおいては、インバータのＭＯＳＦＥＴトランジスタにおけるソース／ドレインノード間の、完全なＶｄｄ電圧以上の降下は確実になくなる。

【0058】

図６ｂに、図６ａのレベルシフタ３００を実現するために使用するインバータ（たとえば、インバータ３０２、３０４および３０６）の一実施形態を示す。図６ｂに示すように、インバータ３４０には、２つのＭＯＳＦＥＴデバイス、すなわちＰチャネルトランジスタ３４２およびＮチャネルトランジスタ３４４が含まれる。図示のように、これらのデバイスは直列に接続され、そのゲートをともに結合し、入力ノード３４６に供給される入力信号によって制御される。Ｐチャネルトランジスタ３４２のソースは、ノード３５０で、第１の電源電圧へ結合され、一方、Ｎチャネルトランジスタ３４４ソースは、ノード３５２で、第２の電源電圧へ結合される。図示のように、デバイスのドレインは、共に結合され、出力ノード３４８で、インバータの出力を生成する。本発明のインバータ３４０の一実施形態では、Ｐチャネルトランジスタ３４２は、幅が５μｍであり、長さが０．８μｍである。この実施形態では、Ｎチャネルトランジスタは、幅が２μｍであり、長さが０．８μｍである。トランジスタ設計分野の当業者は、本発明の範囲または趣旨から逸脱することなく、インバータ３４０のトランジスタとして、他の物理的寸法のものを使用できることを、理解されるであろう。インバータ３４０の論理表現を、また、図６ｂにおいて記号３６０として示してある。

【0059】

このように、本発明のレベルシフタ３００を用いることによって、当初ＧＮＤからＶｄｄの範囲におよぶデジタル入力信号が、－ＶｄｄからＶｄｄの範囲におよぶようにシ

フトされる。図７ａに、デジタル入力信号の、電圧振幅対時間のプロットおよび図６ａの本発明のレベルシフタ３００が発生する、対応する出力信号を示す。図７ａに示すように、デジタル入力信号は、グラウンドまたは直流０ＶからＶｄｄの範囲におよぶ。本発明のレベルシフタ３００の出力は、－ＶｄｄからＶｄｄの範囲におよぶ。本発明におけるＲＦスイッチの一実施形態では、入力信号は、直流０Ｖから直流＋３Ｖの範囲におよび、レベルシフタ３００の出力は、直流－３Ｖから直流＋３Ｖの範囲におよぶ。本発明の範囲または趣旨から逸脱することなく、他の値の電源電圧を用いることができる。たとえば、一実施形態では、入力信号は、０から直流＋３．５Ｖまたは０から直流４Ｖの範囲とすることができる。この実施形態では、レベルシフタは、信号を、直流－３．５（または－４）Ｖから直流＋３．５（または＋４）Ｖにシフトする。

【0060】

図７ｂに、図６ａにおける本発明のレベルシフタ３００の簡易論理記号を示す。この論理記号は、後の図面で用いる。図７ｂに示すように、デジタル入力信号は、入力ノード３１８（図６ａに関連して上記で説明したのと同じ入力ノード３１８）で供給される。レベルシフタ３００は、２つのシフトした出力、すなわち「ｏｕｔ」およびその逆の「ｏｕｔ＿」を供給する。これらの出力は、それぞれ、出力ノード３１４および３１６（図６ａに関連して上記で説明したのと同じ出力ノード３１４および３１６）で供給される。

ＲＦバッファ回路

図８ａは、２段階レベルシフタ・バッファ回路４００の電気図である。図８ｂは、デジタル制御入力およびバッファ回路４００に対するインタフェースの簡易ブロック図である。図８ａの２段階レベルシフタ・ＲＦバッファ回路４００には、第１段階レベルシフタ３００および第２段階ＲＦバッファ回路４０２が含まれる。第１段階レベルシフタ３００は、図６ａ、６ｂ、７ａおよび７ｂに関連して上記で説明したものと同一であり、したがって、ここでより詳細に説明することはしない。上記で説明したように、レベルシフタ段階３００は、デジタル制御信号の論理レベルをシフトして、－ＶｄｄからＶｄｄの範囲におよぶようにする。回路４００の第２段階には、ＲＦバッファ回路４０２が含まれる。ＲＦバッファ回路４０２は、ドライバの役割のみ果たす（ＲＦバッファ回路は、レベルシフトを行わない）。

【0061】

ＲＦバッファは、図３に関連して上記に説明したＲＦスイッチ３０から、デジタル制御信号（図４のＣＭＯＳ論理ブロック１１０が発生するものなど）を電気的に分離する。ＲＦバッファ４０２は、ＲＦスイッチ３０におけるトランジスタの作動および不作動を制御する制御電圧（ＳＷおよびＳＷ＿のことだが、本明細書および図８ａではまた、それぞれ、制御信号「ｏｕｔ」および「ｏｕｔ＿」として示す）の垂下を抑制するように機能する。以下により詳細に説明するように、ＲＦバッファ４０２はまた、大電力ＲＦ信号が、負電力供給（すなわち、－Ｖｄｄ）に結合するのを防ぐように機能する。この負電力供給は、図５ａ～５ｃに関連して上記に説明したように、電荷ポンプ回路２０６が発生する。特に、ＲＦバッファ４０２は、ＲＦスイッチ３０における大電力ＲＦ信号の外延が、電荷ポンプ２０６（図５）が発生する負電力供給にＲＦ結合し、それにより、負電力供給から電流が排流するのを防ぐ。

【0062】

きわめて大電力のＲＦ入力信号が、本発明のＲＦスイッチ３０に入力されるとき、デジタル論理信号をＲＦスイッチから分離するために、バッファ回路を用いていない場合には、ＲＦ信号とデジタル論理信号の結合が起こる。ＲＦ結合は、ＲＦトランジスタ制御信号（ＳＷおよびＳＷ＿）に有害な影響を与える可能性があるし、通常は、有害な影響を与える。たとえば、約３０ｄＢのオーダのＲＦ入力信号が、１ワットのＲＦスイッチ３０に入力される場合、ＲＦ結合により、デジタル制御線で零点数ボルトの電圧振動の起こる可能性がある。これは、ＲＦ信号が、ＲＦスイッチからデジタル制御回路へフィードバックされるためである。このＲＦ結合効果が、ＲＦトランジスタグループの作動および不作動、したがって、ＲＦスイッチ３０の正常な動作に悪い影響を与える可能性がある。図８ａの

バッファ回路４０２によって、結合効果を防ぐ。

【0063】

図８ａに示すように、本発明のバッファ回路４０２は、２段階回路４００の第１段階として上記に説明し図示したレベルシフタ３００と、構成において非常に似ている。レベルシフタ３００と同様に、ＲＦバッファ４０２には、２つのインバータグループ、すなわち第１のインバータグループ（４０４、４０６および４０８）ならびに第２のインバータグループ（４１０、４１２および４１４）が含まれる。第１のインバータグループ（４０４、４０６および４０８）の出力は、第１の出力インバータ４０８によって発生され、図では「ｏｕｔ」の符号を付けてあり、第１の出力ノード４１６で供給される。第２のインバータグループ（４１０、４１２および４１４）の出力は、第２の出力インバータ４１４によって発生され、「ｏｕｔ＿」の符号を付けてあり、第２の出力ノード４１８で供給される。出力信号「ｏｕｔ＿」は、出力信号「ｏｕｔ」の逆である。

【0064】

重要なことだが、第１段階のレベルシフタ３００は、フィードバックを用いてレベルシフト機能を実行する（図６ａに関連して説明したように）が、ＲＦバッファ回路４０２は、その出力信号を入力へフィードバックしない。その結果、第１段階へ入力されるデジタル入力信号（すなわち、ノード３２８および３３０で、レベルシフタ３００に入力される制御入力信号）は、ＲＦスイッチトランジスタを制御するために使用する出力信号（すなわち、それぞれ、出力ノード４１６および４１８の制御出力信号「ｏｕｔ」およびその逆の「ｏｕｔ＿」であり、それぞれ、ＳＷおよびＳＷ＿制御信号線に結合される）から分離される。

【0065】

再び図８ａを参照すると、特に、レベルシフタ３００は、デジタル制御信号「ｉｎ」およびその逆の信号「ｉｎ＿」を、それぞれ、ノード３２８および３３０で入力する（図６ａに関連して上記により詳細に説明したように）。出力ノード３１４における、レベルシフタ３００の第１の出力「ｏｕｔ１」は、図示のようにインバータ３１０の入力部へフィードバックされる。同様に、出力ノード３１６における、レベルシフタ３００の第２の出力「ｏｕｔ１＿」は、インバータ３０４の入力部へフィードバックされる。上記のように、このフィードバックトポロジのせいでＲＦ結合（すなわち、レベルシフタ出力信号が、ＲＦ信号をその上に重ね合わせる）が起こるのは、レベルシフタの出力信号を、ＲＦスイッチトランジスタを直接制御するために用いる場合（すなわち、バッファ回路４０２がない場合）である。したがって、本発明のＲＦバッファ回路４０２は、出力信号のフィードバックなしに用いて、入力信号（すなわち、デジタル入力信号「ｉｎ」および「ｉｎ＿」）を、ＲＦスイッチに存在するＲＦ信号から分離する。図８ａに示すように、レベルシフタ３００の第１の出力信号「ｏｕｔ１」は、ＲＦバッファ回路のインバータ４０４および４０６へ入力する。同様に、レベルシフタ３００の第２の出力信号「ｏｕｔ１＿」は、バッファ回路のインバータ４１０および４１２へ入力する。ＲＦバッファ回路４０２の２つの制御出力（「ｏｕｔ」および「ｏｕｔ＿」）は、ＲＦスイッチにおけるトランジスタの作動および不作動を制御するが、レベルシフタへのフィードバックとしては供給されない。したがって、ＲＦスイッチとデジタル論理回路間における分離の改善が達成される。

【0066】

一実施形態において、２段階レベルシフタ・ＲＦバッファ回路４００を実現するインバータには、図６ｂに関連して上記に説明したインバータ３４０が含まれる。しかしながら、インバータ設計分野の当業者は、代替のインバータ設計を用いて、本発明の範囲または趣旨から逸脱することなく、２段階回路４００が実現できることを理解されるであろう。一実施形態では、第１段階レベルシフタ３００を実現するために使用するトランジスタは、第２段階ＲＦバッファ回路４０２を実現するため使用するトランジスタよりも物理的に小さい。より大きな寸法のトランジスタは、制御信号の効率的な増幅を達成するために、ＲＦバッファ回路４０２で用いる。たとえば、一実施形態では、ＲＦバッファを実現するために使用するトランジスタは、レベルシフタ３００を実現するために使用するトランジ

スタよりも、幅が３倍あり、その結果、電流の約３倍の増幅がもたらされる。トランジスタ設計分野の当業者は、デジタル制御信号における任意の望ましい増幅を達成するために、他の便利な寸法のトランジスタが使用できることを、理解されるであろう。

本発明の代替レベルシフト回路において使用する分圧器

図９ａは、低電流分圧器（「ＬＣＶＤ」）回路５００における一実施形態の電気図である。この回路は、図６ａに関連して上記に説明したレベルシフタ３００における一実施形態のフィードバック経路で使用する。図９ｂに、図９ａの分圧器５００を表すために使用する簡易論理記号を示す。分圧器５００を一実施形態で用いて、フィードバック・インバータトランジスタのゲート酸化物全体の過度の電圧振動に関連した潜在的なゲート酸化物信頼性問題と取り組む。レベルシフタ３００に関連して上記で説明したように、レベルシフタを実現するために使用する様々なＭＯＳＦＥＴのソース－ドレイン電圧は、Ｖｄｄより大きな電圧を印加されることは決してないが、レベルシフタの出力（すなわち、出力信号「ｏｕｔ」および「ｏｕｔ＿」）は、２×Ｖｄｄ（すなわち、－Ｖｄｄから＋Ｖｄｄまで）も振動する可能性があるので、フィードバックインバータ３０４および３１０のゲート酸化物は、２×Ｖｄｄの電圧を印加される可能性がある。これらのフィードバック電圧レベルは、フィードバックインバータ３０４および３１０のゲート酸化物全体に印加され、結果として、ゲート酸化物信頼性問題が生じる可能性がある。

【0067】

ゲート酸化物信頼性問題を回避できるようにするためには、フィードバックインバータ３０４および３１０のゲート酸化物全体に印加される最大電圧を、確実に、ほぼＶｄｄ（２×Ｖｄｄのゲート酸化物電圧ではなく）に低減する。したがって、本発明の完全に集積化されたＲＦスイッチにおける一実施形態では、図９ａの分圧器によって、レベルシフタ・フィードバックインバータ３０４および３１０のゲートに印加される電圧を制限する。この実施形態では、レベルシフタの出力（すなわち、出力ノード３１４および３１６におけるそれぞれの出力「ｏｕｔ」および「ｏｕｔ＿」）を、それぞれの、図６ａのレベルシフタに示すフィードバックインバータに直接フィードバックする代わりに、レベルシフタ出力信号を、最初に、図９ａの分圧器５００で調整して、その後、フィードバックインバータにフィードバックする。以下により詳細に説明するように、分圧器５００により、確実に、フィードバックインバータ３０４および３１０のゲート酸化物に印加される電圧が、Ｖｄｄと小さな電圧降下の合計（電圧降下は、分圧器５００を実現するために使用するトランジスタの数およびトランジスタ閾値電圧の関数である）を超えないようにする。一実施形態では、Ｖｄｄは直流３Ｖであり、電圧降下は直流０．９Ｖである。この実施形態では、分圧器５００のおかげで、ゲート酸化物は、直流約３．９Ｖ（すなわち、フィードバックインバータは、直流－３Ｖから直流０．９Ｖの範囲にわたる電圧を印加される）を超える電圧を決して印加されないことが確実になる。

【0068】

ここで図９ａを参照すると、分圧器５００には、直列構成（すなわち、図示のように、ソースードレイン配置で互いの上に重ねる）でともに結合された複数のＭＯＳＦＥＴデバイス（５０２、５０４、５０６および５０８）含まれる。一実施形態では、ＭＯＳＦＥＴ５０２、５０４、５０６および５０８のゲートおよびドレインが、ともに結合して、積層ダイオードを実現している。ダイオードを実現するＭＯＳＦＥＴを以後は「ダイオードデバイス」と称するが、これらは、図示のように、直列に積層されている。分圧器５００にはまた、ＭＯＳＦＥＴＭ３（５１０）および出力ＭＯＳＦＥＴＭ２（５１２）が含まれる。これら２つのトランジスタの機能は、以下でより詳細に説明する。

【0069】

ダイオードデバイスを使用して、入力ノード５１４で分圧器５００に供給される入力信号の電圧を分圧する。図９ａに示すように、分圧器５００に分圧される信号は、第１のデバイス５０２のドレイン（および接続されているゲート）に入力として供給される。入力信号が、ひとたび（ｎ×Ｖｔｈｎ）の正の電圧レベルを超えると、ここで「ｎ」は、分圧器５００を実現するために使用するダイオードデバイスの数で、Ｖｔｈｎは、デバイスの

閾値電圧（すなわち、デバイスのドレインからソースへの「ダイオード降下」）だが、ダイオードデバイス（５０２、５０４、５０６および５０８）は、大量の電流を導通し始める。図９ａに示す実施形態では、ｎ＝４、Ｖｔｈｎ＝０．７ボルトだが、本発明の範囲または趣旨から逸脱することなく、「ｎ」およびＶｔｈｎに対して、代替値を用いることができる。たとえば、他の実施形態では、分圧器に供給する入力信号は、分圧器５００を実現するために使用するダイオードデバイスの数を変えることにより（すなわち、「ｎ」の値を変えることにより）、任意で所望の電圧レベルに制限できる。図９ａに示す実施形態では、入力電圧が、（４×０．７）の電圧レベルすなわち２．８ボルトをひとたび超えると、積層ダイオードデバイスがさかんに導通し始める。

【0070】

バラスト抵抗器Ｒ５１６が、図示のように、出力ダイオードデバイス５０８のソースに接続されている。ひとたびダイオードデバイスが完全にターンオンすると、バラスト抵抗器Ｒ５１６のために、ｎ×Ｖｔｈｎの値を超える、任意の追加的入力電圧が降下する。図９ａに示す実施形態では、バラスト抵抗器Ｒ５１６のために、（入力電圧－（４×Ｖｔｈｎ））の値を超える、任意の追加的入力電圧が降下する。分圧器５００の出力は、出力ダイオードデバイス５０８の、接続されたゲートードレインから引き出す。分圧された出力信号は、出力ノード５２０で供給される。ダイオードデバイス５０２、５０４および５０６のダイオード電圧降下およびバラスト抵抗器Ｒ５１６全体で降下する電圧のために、出力ノード５２０の出力は、ほぼ（入力電圧－（３×Ｖｔｈｎ））を決して超えないことが保証される。Ｖｔｈｎ＝約０．７Ｖおよび約３Ｖの最大入力電圧に対して、出力ノード５２０は、（直流３Ｖ－（３×直流０．７Ｖ））すなわち直流０．９Ｖを決して超えない。このように、図９ａに示す実施形態では、直流－３Ｖと直流＋３Ｖ間の範囲におよぶ入力電圧に対して、分圧器５００は、出力ノード５２０の出力を、直流－３Ｖから直流＋０．９Ｖの範囲に制限する。

【0071】

出力ＭＯＳＦＥＴＭ２（５１２）はキャパシタとして構成され、分圧器５００のスイッチング時間の加速を支援するために使用する。入力が負電位に達したとき、ＭＯＳＦＥＴＭ３（５１０）は、出力ノード５２０が、入力ノード５１４における入力信号の電位に振動することを確実にする。これは、入力信号が負電位に達したとき、デバイスＭ３（５１０）がターンオンすることによって、達成される。したがって、入力信号が－Ｖｄｄ電位（たとえば、直流－３Ｖ）になるとき、出力ノード５２０の出力信号もまた－Ｖｄｄになる。出力デバイス５０８は、入力信号の負電圧振動の間、逆バイアスをかけられ、これにより、入力信号の負電圧振動の間、直流電流が、負の電力供給源から排流しないことが確実となる。分圧器の出力が直流約－３Ｖのとき、分圧器５００は、電流を少しも引き寄せない。このことは、重要である。なぜなら、電流は直流－３Ｖで、図５ｂに関連して上記に説明した電荷ポンプ回路を放電させるからである。分圧器の出力が約０．９Ｖのとき、バラスト抵抗器Ｒ５１６が比較的大きく選択されている場合には、引き寄せられる電流は、比較的少ない。しかしながら、この場合の電流は、正電圧（０．９Ｖ）とグラウンド間に生じるので、図９ａの分圧器５００の動作のために、追加的な電荷ポンプ電流が送られることはない。

【0072】

実施形態では、バラスト抵抗器Ｒ５１６の値は１００ｋΩである。　実施形態では、分圧器５００のデバイスは全て、同じ長さである。たとえば、一実施形態では、全てのデバイスは、長さが０．８μｍである。一実施形態では、全てのダイオードデバイス（５０２、５０４、５０６および５０８）の物理的寸法は同じである。一実施形態では、各ダイオードデバイスは、幅が２μｍであり、デバイスＭ３（５１０）は、幅が同じ２μｍであり、そして出力ＭＯＳＦＥＴＭ２（５１２）は、幅が１４μｍである。集積回路設計分野の当業者は、本発明の範囲または趣旨から逸脱することなく、図９ａに示すデバイスに対して、他の値および代替構成が使用できることを、理解されるであろう。たとえば、電気回路設計分野の当業者は、ダイオード素子の数「ｎ」を変えること、Ｖｔｈｎの値を変え

ること、またはダイオードデバイスの積層において、異なるポイントで出力ノード５２０を引き出すこと（たとえば、図示のように、デバイス５０８のドレインから引き出す代わりに、ダイオードデバイス５０６または５０４のドレインから出力を引き出すこと）によって、他の分圧器出力レベルが、簡単に調節できることを理解されるであろう。

分圧器を用いる修正レベルシフタ

ＲＦスイッチトランジスタのゲート酸化物に印加される電圧を減少することにより、図９ａおよび９ｂの分圧器５００を有利に使用して、上記のレベルシフタ３００および電荷ポンプ回路の両方におけるトランジスタの信頼性を高めることができる。たとえば、図１０に、図６ａのレベルシフタ３００と組み合わせて、図９ａの分圧器５００を使用する修正レベルシフタ６００を示す。図１０に示すように、レベルシフタ３００におけるインバータ３０６の出力（出力ノード３１４における）は、第１の分圧器５００’の入力部へ印加される。同様に、レベルシフタ３００のインバータ３１２の出力（出力ノード３１６における）は、第２の分圧器５００’’の入力部に印加される。分圧器の出力は、図１０に示すように、フィードバックインバータ３０４および３１０の入力部へフィードバックされる。特に、図１０を参照すると、出力ノード５２０’における、第１の分圧器の出力「ｏｕｔ」は、フィードバックインバータ３１０の入力部へフィードバックされる。同様に、出力ノード５２０’’における、第２の分圧器の出力「ｏｕｔ＿」は、フィードバックインバータ３０４の入力部へフィードバックされる。図９ａに関連して上記に説明したように、レベルシフタ５００’および５００’’により、フィードバック電圧を、－Ｖｄｄから直流約＋０．９Ｖの範囲に減少する。このフィードバック経路の減少した電圧振動のために、レベルシフタ６００の機能が変わることはない。

【0073】

ＲＦスイッチ制御信号「ＳＷ」および「ＳＷ＿」は、それらを分圧器５００’および５００’’へ入力する前に、レベルシフタ出力から引き出し、図３の本発明のＲＦスイッチ３０へ入力として供給できることに注目されたい。たとえば、図１０に示すように、出力ノード３１４における、インバータ３０６の出力は、スイッチ制御信号「ＳＷ」を発生するために、引き出して使用することができる。同様に、出力ノード３１６における、インバータ３１２の出力は、スイッチ制御信号「ＳＷ＿」を発生するために、引き出して使用することができる。一実施形態では、図８ａの２段階レベルシフタ・ＲＦバッファ回路４００に関連して上記で説明したように、ノード３１４および３１６から引き出した制御信号は、最初にバッファに格納され、その後ＲＦスイッチトランジスタに結合される。スイッチ制御信号ＳＷおよびＳＷ＿は、全域にわたる電圧振動が可能だが、これは、ＲＦスイッチにおける、ゲート酸化物の信頼性問題を引き起こさない。特に、スイッチ制御信号は、－Ｖｄｄから＋Ｖｄｄまでの範囲にわたる（すなわち、スイッチ制御信号の電圧レベルは、分圧器によって制限されない）。スイッチ制御信号の全面的な電圧振動は、ＲＦスイッチＭＯＳＦＥＴに関して、ゲート酸化物の信頼性問題を引き起こすことはない。なぜなら、ＲＦスイッチＭＯＳＦＥＴのソースが、接地されているからである。したがって、スイッチ入力信号は、ＲＦスイッチＭＯＳＦＥＴにおけるグラウンドに関連する。その結果、ＭＯＳＦＥＴは、グラウンドに対して正のＶｄｄ電圧を、ゲート酸化物全体に印加されるか、またはグラウンドに対して負のＶｄｄ電圧を、ゲート酸化物全体に印加される。

【0074】

図１０にまた、修正レベルシフタ６００における一部分の簡易記号表現６０１を示す。記号６０１は、図１０の破線領域６０１’が示す部分を表す。図１０に示すように、記号による修正レベルシフタ６０１には、入力ノード３２６（「ｉｎ＿」）に対応する第１の入力「ｉｎ＿」６３０が含まれる。記号による修正レベルシフタ６０１にはまた、フィードバックインバータ３１０への入力に対応する、第２の入力「ｏｕｔ」６３２が含まれる。この信号はまた、第１の分圧器５００’の出力部５２０’から出ていることに注意されたい。正の電源電圧は、＋Ｖｄｄ入力部６３４で入力される。負の電源電圧は、－Ｖｄｄ入力部６３６で入力される。修正レベルシフタ６０１には、３つの出力信号、すなわち、「ｏｕｔ＿ｐｏｓ」（出力部６３８における）、「ｏｕｔ＿ｎｅｇ」（出力部６４０にお

ける）および「ｏｕｔ＿」（出力部６４２における）がある。これらの出力部は、上記の出力ノード６０６、６０８および５２０’’に対応している。理解を容易にするために、レベルシフタ６０１の記号表現は、以下に説明する図面において使用する。

【0075】

図６ａに関連して上記に説明した、レベルシフタ３００に関連する潜在的なゲート酸化物信頼性問題は、修正レベルシフタ６００のフィードバック経路において、分圧器５００’および５００’’を用いて回避する。さらに、分圧器５００’および５００’’はまた、電荷ポンプ回路に関連する潜在的なゲート酸化物信頼性問題を減少するために機能することもできる。図１０に示すように、インバータ３０８および３１０の出力は、レベルシフタ３００から引き出され、２つの出力信号「ｏｕｔ＿ｐｏｓ」および「ｏｕｔ＿ｎｅｇ」を生成するために、２つの出力インターバルに入力として供給される。特に、インバータ３０８の出力は、第１の出力インバータ６０２への入力として供給される。同様に、フィードバックインバータ３１０の出力は、第２の出力インバータ６０４への入力として供給される。

【0076】

このような方法で出力インバータ６０２および６０４を結合することにより、修正レベルシフタ６００の出力信号は、決してＶｄｄ（または－Ｖｄｄ）を超えることがなくなる。特に、第１の出力インバータ６０２は、第１の出力ノード６０６において、ＧＮＤ（すなわち、直流０Ｖ）から＋Ｖｄｄの範囲にわたる出力信号「ｏｕｔ＿ｐｏｓ」を発生する。第２の出力インバータ６０４は、第２の出力ノード６０８において、－ＶｄｄからＧＮＤの範囲にわたる第２の出力信号「ｏｕｔ＿ｎｅｇ」を発生する。入力信号「ｉｎ＿」がＧＮＤになると、出力信号「ｏｕｔ＿ｐｏｓ」もまたＧＮＤになる。出力信号「ｏｕｔ＿ｎｅｇ」がＧＮＤから－Ｖｄｄに移る。入力信号「ｉｎ＿」が正の＋Ｖｄｄになると、「ｏｕｔ＿ｐｏｓ」もまたＶｄｄになり、「ｏｕｔ＿ｎｅｇ」が－ＶｄｄからＧＮＤに移る。このように、本発明の修正レベルシフタ６００を用いると、「ｏｕｔ＿ｐｏｓ」出力信号は、ＧＮＤから＋Ｖｄｄの範囲にわたり、一方、「ｏｕｔ＿ｎｅｇ」出力信号は、ＶｄｄからＧＮＤの範囲にわたる。以下により詳細に説明するように、２つの出力信号「ｏｕｔ＿ｐｏｓ」および「ｏｕｔ＿ｎｅｇ」を用いて、修正電荷ポンプ回路における潜在的なゲート酸化物信頼性問題に取り組む。ここで図１１ａおよび１１ｂに関連して説明するように、これらの出力信号を用いて、ＲＦバッファ回路における、潜在的なゲート酸化物信頼性問題に取り組むこともできる。

修正レベルシフタ・ＲＦバッファ回路

図８ａに関連して上記で説明した、２段階のレベルシフタ・ＲＦバッファ４００では、ＲＦバッファインバータ入力において、約２×Ｖｄｄの電圧振動を経験する可能性がある。すでに説明したように、このレベルの電圧振動では、ゲート酸化物信頼性問題が生じ、ＲＦバッファトランジスタの機能に有害な影響を与える可能性がある。

【0077】

図１１ａおよび１１ｂに、図８ａに関連して上記に説明した、２段階レベルシフタ・ＲＦバッファ回路４００の代替実施形態を示す。図１１ｂに示す、ＲＦバッファの代替実施形態では、上記に説明した分圧器回路を用いて、確実に、ＲＦバッファのゲート酸化物にかかる電圧が、Ｖｄｄを０．９ボルトより超えないようにする。図１１ｂに示すように、代替の２段階レベルシフタ・ＲＦバッファ回路４００’には、第１段階レベルシフタ回路６００およびそれに結合された第２段階ＲＦバッファ回路４０２’が含まれる。レベルシフタおよびＲＦバッファ回路４００’のこの実施形態では、図１１に関連して上記で説明した、修正レベルシフタの出力「ｏｕｔ＿ｐｏｓ」および「ｏｕｔ＿ｎｅｇ」を、ＲＦバッファインバータへの入力として用い、ＲＦバッファ出力信号「ｏｕｔ」および「ｏｕｔ＿」を発生する。たとえば、図１１ｂに示すように、第１の修正レベルシフタ７００が発生する「ｏｕｔ＿ｐｏｓ」および「ｏｕｔ＿ｎｅｇ」出力信号は、２つのＲＦバッファインバータ７０２および７０４へそれぞれ入力される。同様に、第２の修正レベルシフタ７０６が発生する「ｏｕｔ＿ｐｏｓ」および「ｏｕｔ＿ｎｅｇ」出力信号は、２つのＲＦバ

ッファインバータ７０８および７１０へそれぞれ入力される。図１１ａおよび１１ｂに示す代替の実施形態４００’に従い、入力信号「ｉｎ」が論理的に高い信号のとき、「ｏｕｔ＿ｐｏｓ」出力はＶｄｄになり、一方「ｏｕｔ＿ｎｅｇ」はＧＮＤになる。このように、入力信号「ｉｎ」が論理的に高い値のとき、インバータ７０２の出力はＧＮＤになり、インバータ７０４の出力は－Ｖｄｄになる。したがって、入力信号「ｉｎ」が高いとき、インバータ７１２の出力は（「ｏｕｌ」）－Ｖｄｄになる。入力信号「ｉｎ」が低いとき、反対の出力が生成される。

【0078】

ＲＦバッファインバータ７０２および７０４を用いて、第１のＲＦ出力インバータ７１２の電源電圧を制御する。同様に、ＲＦバッファインバータ７０８および７１０を用いて、第２のＲＦ出力インバータ７１４の電源電圧を制御する。この実施形態では、ＲＦバッファ出力信号「ｏｕｔ」および「ｏｕｔ＿」を用いてＲＦスイッチを制御する（すなわち、出力信号「ｏｕｌ」は、制御電圧「ＳＷ」として働き、一方、「ｏｕｌ＿」は制御電圧「ＳＷ＿」として働く）。

修正電荷ポンプ－代替実施形態

上記のように、図１０の修正レベルシフタ６００が発生する２つの出力信号「ｏｕｔ＿ｐｏｓ」および「ｏｕｔ＿ｎｅｇ」を、電荷ポンプ回路における代替の一実施形態で用いて、電荷ポンプに印加される過度の電圧に関連する、潜在的なゲート酸化物信頼性問題を減少または解消することができる。図５ｂおよび５ｃに関連して上記に説明したように、電荷ポンプトランジスタ（すなわち、Ｐチャネルトランジスタ２０８および２１０、ならびにＮチャネルトランジスタ２１２および２１４）のゲートを制御するために用いるクロック信号には、２×Ｖｄｄの電圧振動がある。たとえば、図５ｃに示すように、電荷ポンプクロック信号「Ｃｌｋ１」および「Ｃｌｋ２」は、負の電源電圧－Ｖｄｄから正の電源電圧＋Ｖｄｄの範囲にわたる。ＲＦバッファ回路およびレベルシフタ回路に関連して上記に説明したゲート酸化物信頼性問題と同様に、この全域にわたる電圧振動は、電荷ポンプ回路に酸化物信頼性問題を引き起こす可能性がある。したがって、ゲート酸化物に印加される電圧を、－Ｖｄｄから０．９Ｖの範囲に制限することにより、潜在的なゲート酸化物信頼性問題を減少または解消する修正電荷ポンプ回路を、図１２に示す。

【0079】

図１２に、修正電荷ポンプ８００を示す。これは、図１０に関連して上記に説明した修正レベルシフタ６００を使用する。図１２に示すように、修正電荷ポンプ８００には、電荷ポンプ回路２０６’および本発明の電荷ポンプクロック発生回路８０２が含まれる。電荷ポンプクロック発生回路８０２によって、電荷ポンプ回路２０６’が使用するクロック制御信号を発生する。電荷ポンプ回路２０６’は、図５ｂに関連して上記で説明した電荷ポンプ２０６に、設計が非常に似ている。たとえば、電荷ポンプ回路２０６’には、パスキャパシタＣｐ２１６および出力キャパシタＣ２１８に加えて、一対のＰチャネルトランジスタ２０８および２１０、ならびに一対のＮチャネルトランジスタ２１２および２１４が含まれる。電荷ポンプ回路２０６’の一実施形態では、出力キャパシタＣ２１８には、数百ｐＦのオーダのキャパシタンスがあり、キャパシタＣｐ２１６には、約５０ｐＦのキャパシタンスがある。電荷ポンプ設計分野の当業者は、本発明の範囲または趣旨から逸脱することなく、他のキャパシタンス値が使用できることを、理解されるであろう。

【0080】

電荷ポンプ２０６’の機能は、図５ａに関連して上記に説明した電荷ポンプ２０６と、非常に似ている。したがって、その動作を、ここで再び詳細に説明することはしない。図１２に示す電荷ポンプ２０６’が電荷ポンプ２０６と異なるのは、電荷ポンプ２０６’のトランジスタゲート（すなわち、トランジスタ２０８、２１０、２１２および２１４のゲート）を制御するために使用する制御信号が、電圧振動の半分の領域に制限されている点である（すなわち、－Ｖｄｄからグラウンドまたはグラウンドから Ｖｄｄの範囲に制限されている）。ゲート制御電圧が全域（すなわち、　Ｖｄｄから Ｖｄｄまで）を振動するときに生じる、潜在的なゲート酸化物信頼性問題は、したがって、減少するかまたは解消さ

れる。

【0081】

図１２に示すように、電荷ポンプクロック発生回路８０２には、フィードバック構成でともに結合された、４つの修正レベルシフタ８０４、８０６、８０８および８１０が含まれる。修正電荷ポンプの一実施形態では、４つの修正レベルシフタは、図１０に関連して上記に説明した修正レベルシフタ６００によって実現される。図１２に、図１０におけるレベルシフタ６００の記号表現６０１を用いたレベルシフタを示す。この実施形態では、レベルシフタ８０４、８０６、８０８および８１０は、図１０のレベルシフタ６００と同一の動作をする。２つの非重複クロック信号「Ｃｌｋ１」および「Ｃｌｋ２」（ならびに、それぞれの逆信号「Ｃｌｋ１＿」および「Ｃｌｋ２＿」）は、図１２に示すように、レベルシフタの「ｉｎ＿」入力部に入力される。２つの入力クロック信号「Ｃｌｋ１」および「Ｃｌｋ２」は、図５ａ～５ｃに関連して上記で説明した非重複クロック信号と同一である。図５ｃに関連して上記で示したように、２つの非重複クロック信号は、－Ｖｄｄから＋Ｖｄｄの電圧振幅で変化する。一実施形態では、クロック信号は、直流－３Ｖから直流＋３Ｖまで変化する。

【0082】

４つの修正レベルシフタにより、電荷ポンプ２０６’を制御するために使用する、半分の領域のクロック制御信号を発生する。特に、図１２に示すように、４つのレベルシフタにより、「ＣＬＫ１ＰＯＳ＿」、「ＣＬＫ１ＮＥＧ＿」、「ＣＬＫ２ＰＯＳ」および「ＣＬＫ２ＮＥＧ」制御信号を発生する。これらは、電荷ポンプ・トランジスタゲート制御ノード２５０、２５２、２５４および２５６へそれぞれ入力される。図１２に示す実施形態では、レベルシフタ８０５および８０８により、４つのトランジスタゲート制御信号「ＣＬＫ１ＰＯＳ＿」、「ＣＬＫ１ＮＥＧ＿」、「ＣＬＫ２ＰＯＳ」および「ＣＬＫ２ＮＥＧ」を発生する。レベルシフタ８０６により、「ＣＬＫ１ＰＯＳ＿」および「ＣＬＫ１ＮＥＧ＿」ゲート制御信号を発生し、一方、レベルシフタ８０８により、「ＣＬＫ２ＰＯＳ」および「ＣＬＫ２ＮＥＧ」ゲート制御信号を発生する。特に、図１２に示すように、レベルシフタ８０６の「ｏｕｔ＿ｐｏｓ」出力（「ＣＬＫ１ＰＯＳ＿」）は、トランジスタ２０８のトランジスタゲート入力部２５０を制御するために結合される。レベルシフタ８０６の「ｏｕｔ＿ｎｅｇ」出力（「ＣＬＫ１ＮＥＧ＿」）は、トランジスタ２１０のトランジスタゲート入力部２５２を制御するために結合される。同様に、レベルシフタ８０８の「ｏｕｔ＿ｐｏｓ」出力（「ＣＬＫ２ＰＯＳ」）は、トランジスタ２１４のトランジスタゲート入力部２５４を制御するために結合される。最後に、レベルシフタ８０８の「ｏｕｔ＿ｎｅｇ」出力（「ＣＬＫ２ＮＥＧ」）は、トランジスタ２１４のトランジスタゲート入力部２５６を制御するために結合される。クロック発生回路８０２は、電荷ポンプトランジスタにおけるゲート酸化物全体の過度の電圧を防ぐように機能する。

【0083】

トランジスタ設計分野の当業者は、本発明の趣旨または範囲から逸脱することなく、他の制御構成が使用できることを、理解されるであろう。たとえば、他の２つのレベルシフタ（８０４および８１０）を用い、修正電荷ポンプの代替実施形態において、制御信号を発生できる。また、電荷ポンプ回路２０６に関連して上記で説明したように、代替のトランジスタ構成（Ｎチャネルおよびｐチャネル）を用いて、本発明の修正電荷ポンプ２０６’を実現することができる。

【0084】

図１２に示すように、４つのレベルシフタ８０４、８０６、８０８および８１０は、図６ａに関連して上記で説明したレベルシフタのフィードバックトポロジと非常に似ているフィードバック構成において、ともにレベルシフタの組（８０４と８０６および８０８と８１０）に結合される。たとえば、レベルシフタ８０４の「ｏｕｔ＿」出力ノード（信号）は、その関連する組のレベルシフタ８０６の「ｏｕｔ」ノードへフィードバックとして供給される。同様に、レベルシフタ８０６の「ｏｕｔ＿」出力ノードは、その関連する組のレベルシフタ８０４の「ｏｕｔ」ノードへフィードバックとして供給される。同様に、

レベルシフタ８０８の「ｏｕｔ＿」出力ノードは、その関連する組のレベルシフタ８１０の「ｏｕｔ」ノードへのフィードバックとして供給される。レベルシフタ８１０の「ｏｕｔ＿」出力ノードは、その関連する組のレベルシフタ８０８の「ｏｕｔ」ノードへフィードバックとして供給される。フィードバック構成は、４つのトランジスタゲート制御信号「ＣＬＫ１ＰＯＳ＿」、「ＣＬＫ１ＮＥＧ＿」、「ＣＬＫ２ＰＯＳ」および「ＣＬＫ２ＮＥＧ」の発生において、クロック発生回路８０２が使用する。

概要

ＳＯＩ・ＣＭＯＳプロセスを用いて製造する新規なＲＦスイッチを提供する。ＳＯＩ基板の上にスイッチを製造すると、結果として、基板バイアスがなくなり、主なＣＭＯＳ回路構成ブロックを、ＲＦスイッチ素子とともに集積することが可能となる。ＣＭＯＳ構成ブロックをＲＦスイッチ素子と集積することにより、単一外部電源（すなわち、負の電源電圧は、ＲＦスイッチとともに集積された電荷ポンプ回路で内的に発生する）だけの使用が必要な、完全に集積化されたＲＦスイッチという解決法が提供される。この結果として、ＲＦスイッチ分離、挿入損失および圧縮が改善される。一実施形態では、ＲＦスイッチの１ｄＢ圧縮ポイントは約１ワットを超え、挿入損失は約０．５ｄＢ未満であり、スイッチ分離は約４０ｄＢほどの高さである。本発明スイッチにより、また、スイッチング時間が改善する。

【0085】

本発明のいくつかの実施形態について、説明してきた。しかしながら、本発明の趣旨および範囲から逸脱することなく、様々な修正が可能であることを理解されるであろう。

【0086】

したがって、本発明は、特定の、例示した実施形態によって限定されるのではなく、添付の特許請求の範囲によってのみ限定されることを理解されたい。

【図面の簡単な説明】

【0087】

【図1a】ＲＦスイッチの性能特性を説明するために使用する、先行技術による単極単投（ＳＰＳＴ）ＲＦスイッチの簡易電気回路図である。

【図1b】図１ａにおけるＳＰＳＴ・ＲＦスイッチの簡易電気回路図であり、このスイッチがターン「オン」され、ＲＦ信号が入力ノードから出力ノードへ通過可能となったときの、スイッチの主要な特性を示す。

【図1c】ＲＦスイッチがターン「オフ」され、それによってＲＦ信号を出力ノードからブロックするときの、図１ａおよび１ｂにおけるＲＦスイッチの、同等な小信号電気特性を示す。

【図2】先行技術による単極双投（ＳＰＤＴ）ＲＦスイッチの簡易電気回路図である。

【図3】本発明の一実施形態によるＲＦスイッチの電気回路図である。

【図4】本発明に従って製造した、例示的で、完全に集積化されたＲＦスイッチの、簡易ブロック図である。

【図5a】図４の簡易ブロック図に示す負電圧発生器における例示的な一実施形態の簡易ブロック図である。

【図5b】図４のＲＦスイッチへ負供給電圧を発生するために使用する電荷ポンプ回路における第１の実施形態の電気回路図である。

【図5c】図５ｂの電荷ポンプ回路を制御するために使用する、２つの、重なり合わず、経時的に変化するクロック信号の電圧振幅を示す、電圧振幅対時間のプロットである。

【図6a】本発明のレベルシフト回路における第１の実施形態の電気回路図である。

【図6b】図６ａのレベルシフタを実現するために使用するインバータにおける一実施形態の電気回路図である。

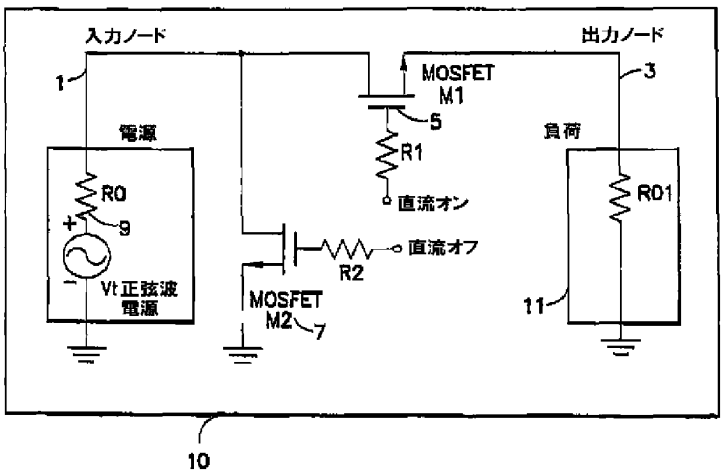
【図7a】デジタル入力信号およびそれに対応する、図６ａの本発明のレベルシフタが発生する出力信号の、電圧振幅対時間のプロットである。

【図7b】図６ａにおける本発明のレベルシフタの簡易論理記号である。

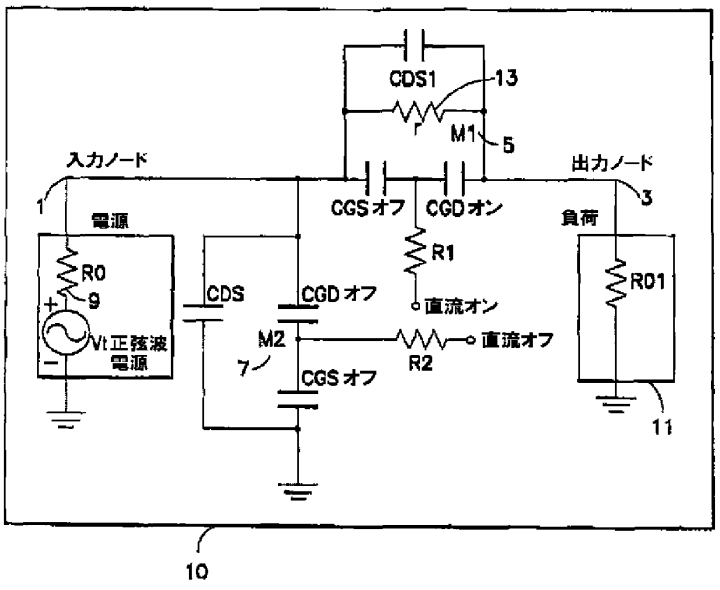
【図8a】第１段階のレベルシフタおよび第２段階のＲＦバッファ回路を含む２段階レベル

シフタ・ＲＦバッファ回路における一実施形態の電気回路図である。
【図8b】デジタル制御入力および図８ａのＲＦバッファ回路に対するインタフェースの簡易ブロック図である。
【図9a】本ＲＦスイッチの発明に従って製造した低電流分圧器（ＬＣＶＤ）回路における一実施形態の電気回路図である。
【図9b】図９ａの分圧器を表現するために使用する簡易論理記号である。
【図10】図６ａのレベルシフト回路と組み合わせて、図９ａの低電流分圧器回路を用いているレベルシフト回路における第２の実施形態の電気回路図である。
【図11a】図８ａの２段階レベルシフタ・ＲＦバッファ回路の代替実施形態を示す電気回路図である。
【図11b】図８ａの２段階レベルシフタ・ＲＦバッファ回路の代替実施形態を示す電気回路図である。
【図12】図１０のレベルシフト回路を使用する修正電荷ポンプの電気回路図である。

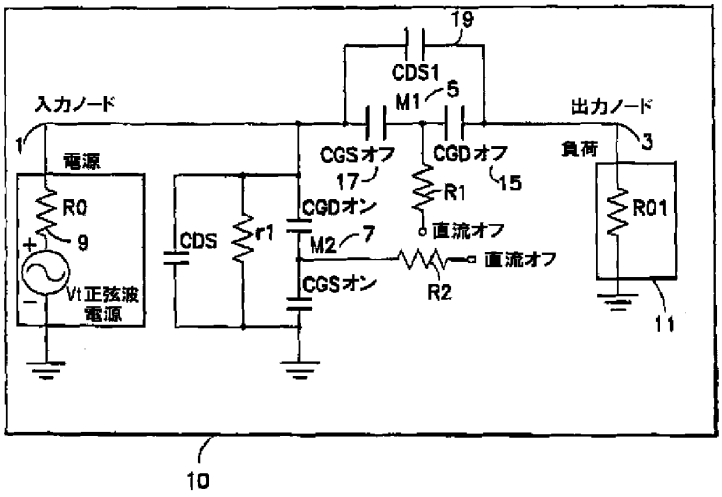
【図1A】



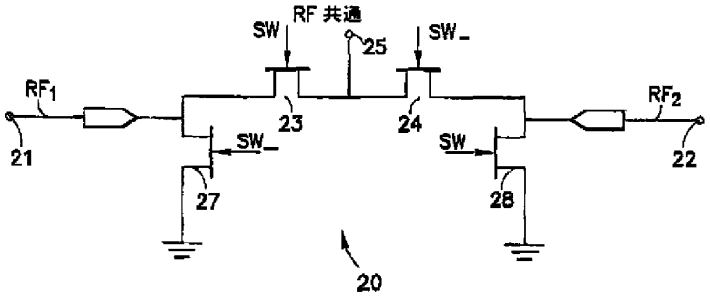
【図1B】


CDS1
13
M1
5
入力ノード
出力ノード
1
3
電源
CGSオフ
CGDオン
負荷
R1
R0
9
CDS
CGDオフ
直流オン
R01
M2
7
直流オフ
R2
Vt正弦波
電源
CGSオフ
11
10

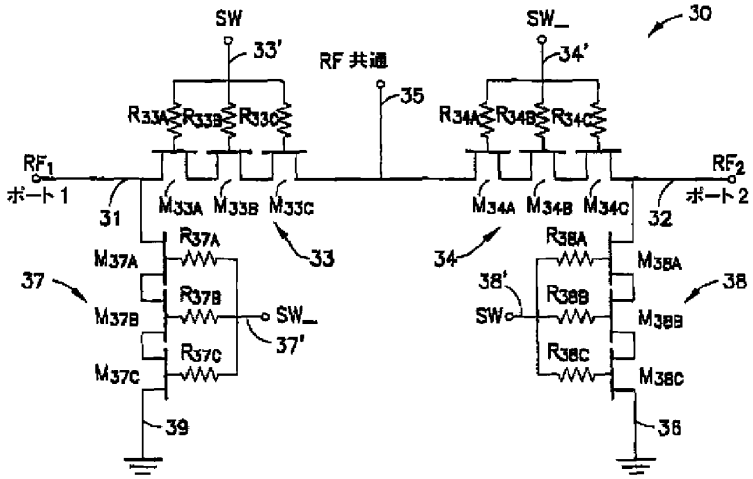
【図1C】


19
CDS1
5
M1
入力ノード
出力ノード
1
3
電源
CGSオフ
17
CGDオフ
15
負荷
R1
R0
9
CDS
r1
CGDオン
直流オフ
R01
M2
7
直流オフ
R2
Vt正弦波
電源
CGSオン
11
10

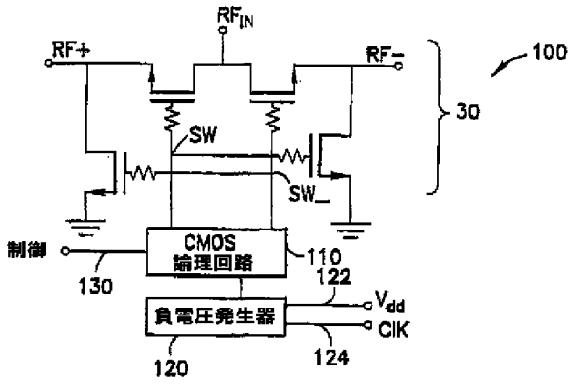
【図2】


SW
RF 共通
25
SW_
RF1
21
23
24
RF2
22
SW_
SW
27
28
20

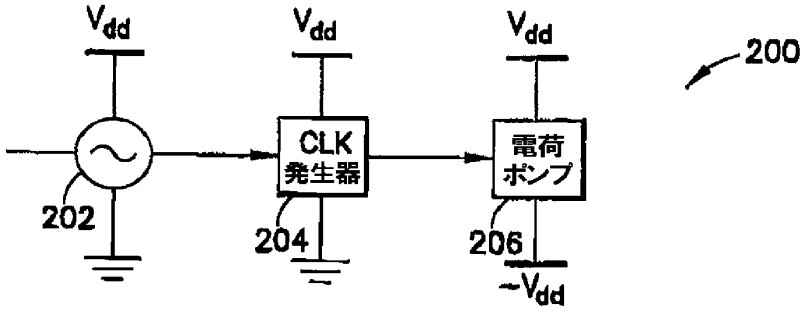
【図3】


SW
33'
RF 共通
35
SW_
34'
30
R33A R33B R33C
R34A R34B R34C
RF1
ポート1
31
M33A M33B M33C
33
M34A M34B M34C
32
RF2
ポート2
R37A
M37A
37
R37B
M37B
SW_
37'
R37C
M37C
39
34
R38A
M38A
38'
SW
R38B
M38B
38
R38C
M38C
36

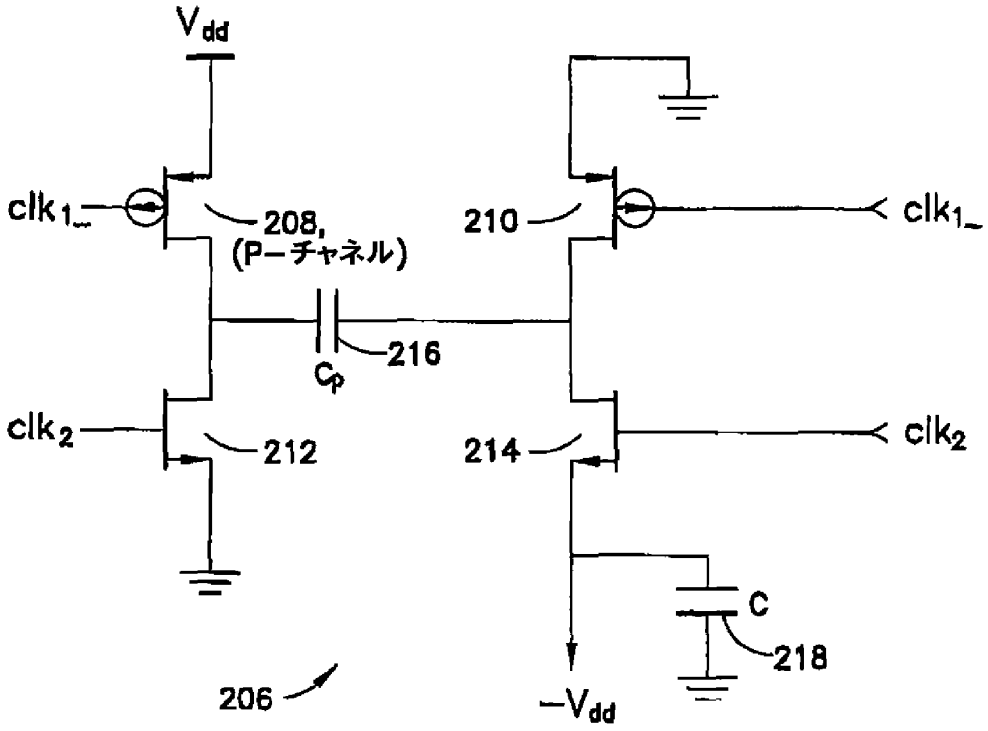
【図4】


RF_IN
RF+
RF−
100
30
SW
SW_
制御
CMOS
論理回路
110
130
122
負電圧発生器
V_dd
CIK
120
124

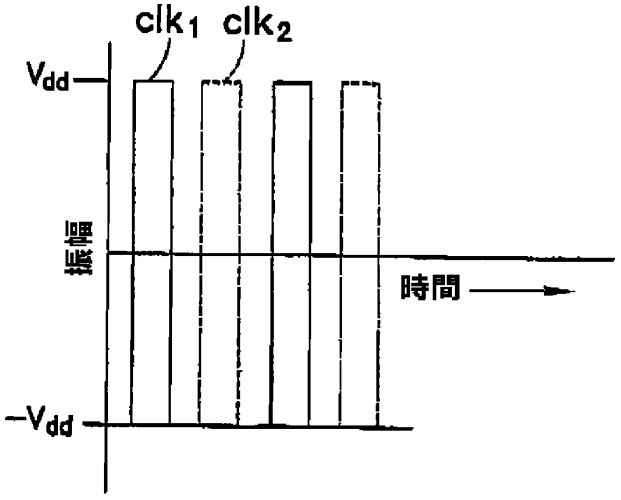
【図5A】


V_dd
V_dd
V_dd
200
CLK
発生器
電荷
ポンプ
202
204
206
−V_dd

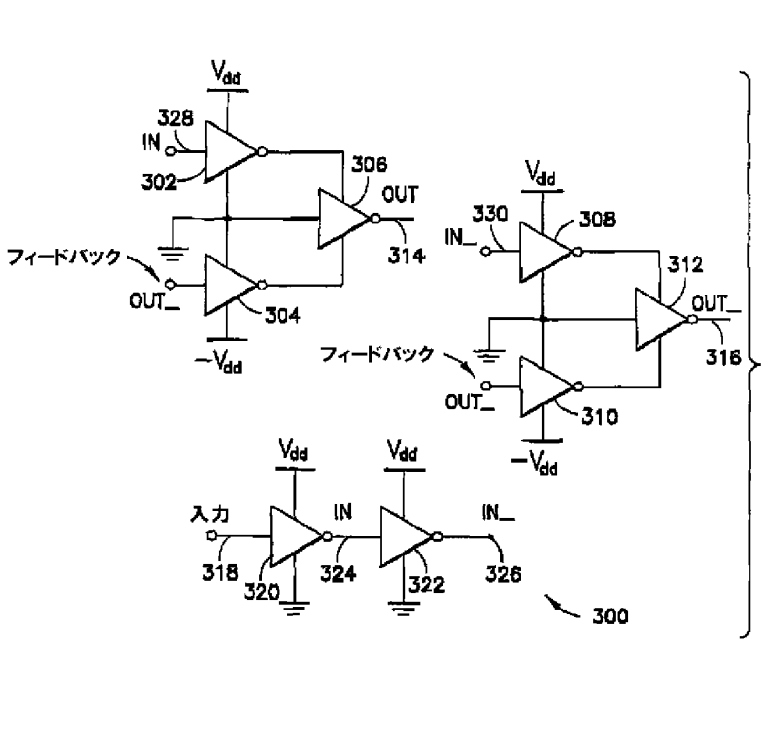
【図5B】


Vdd
clk1
208,
(P−チャネル)
210
clk1
216
Cp
clk2
212
214
clk2
C
218
206
−Vdd

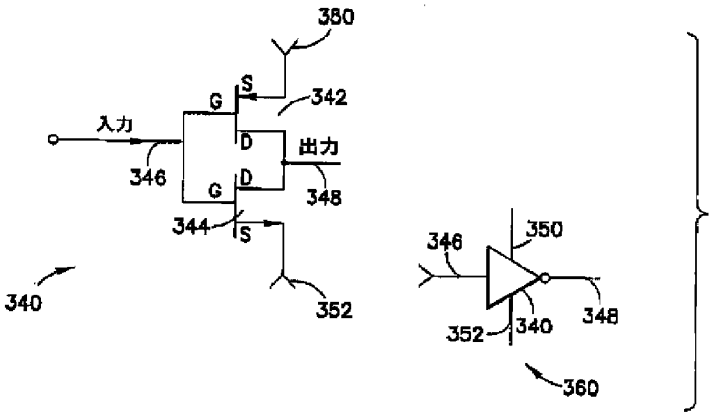
【図5C】


clk1 clk2
Vdd
電圧
時間
−Vdd

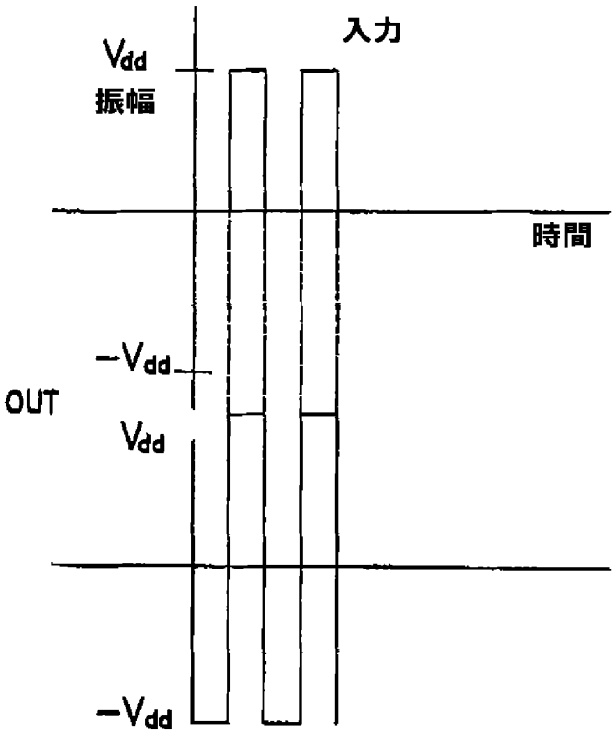
【図6A】


Vdd
328
IN
302
306
OUT
314
フィードバック
OUT_
304
−Vdd
Vdd
330
IN_
308
312
OUT_
316
フィードバック
OUT_
310
−Vdd
Vdd
Vdd
入力
IN
IN_
318
320
324
322
326
300

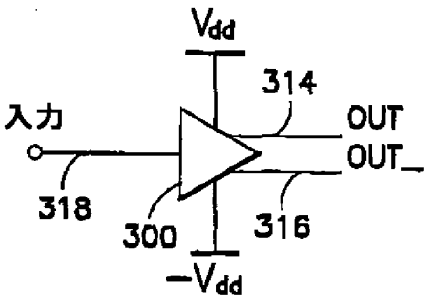
【図6B】


380
S
G
342
入力
D
出力
346
G
D
348
344
S
340
352
346
350
348
352
340
360

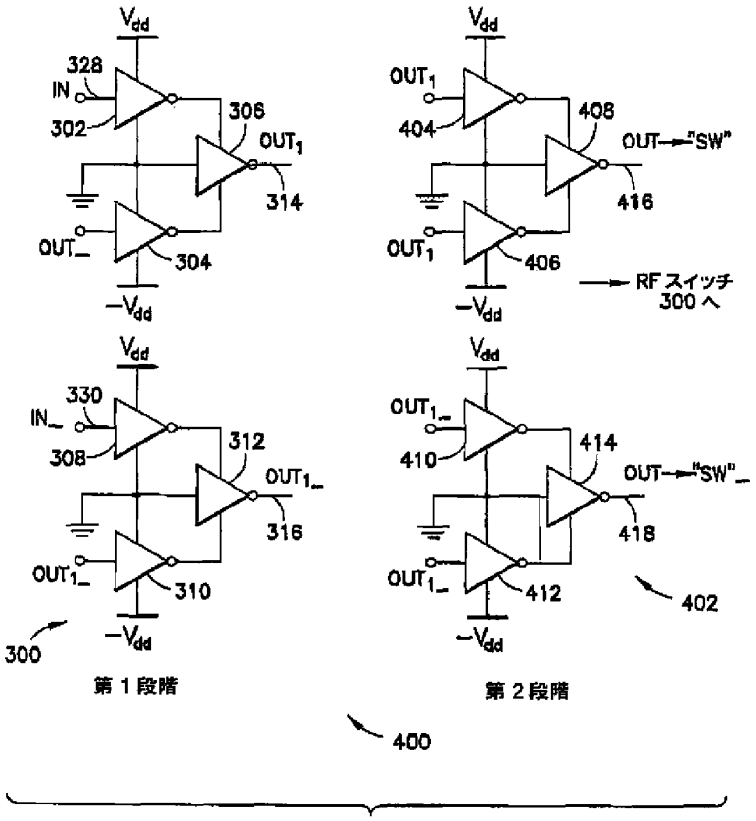
【図7A】


入力
Vdd
振幅
時間
−Vdd
OUT
Vdd
−Vdd

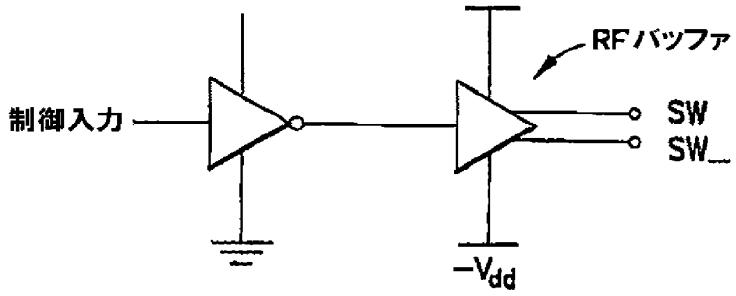
【図7B】


Vdd
314
入力
OUT
OUT_
318
300
316
-Vdd

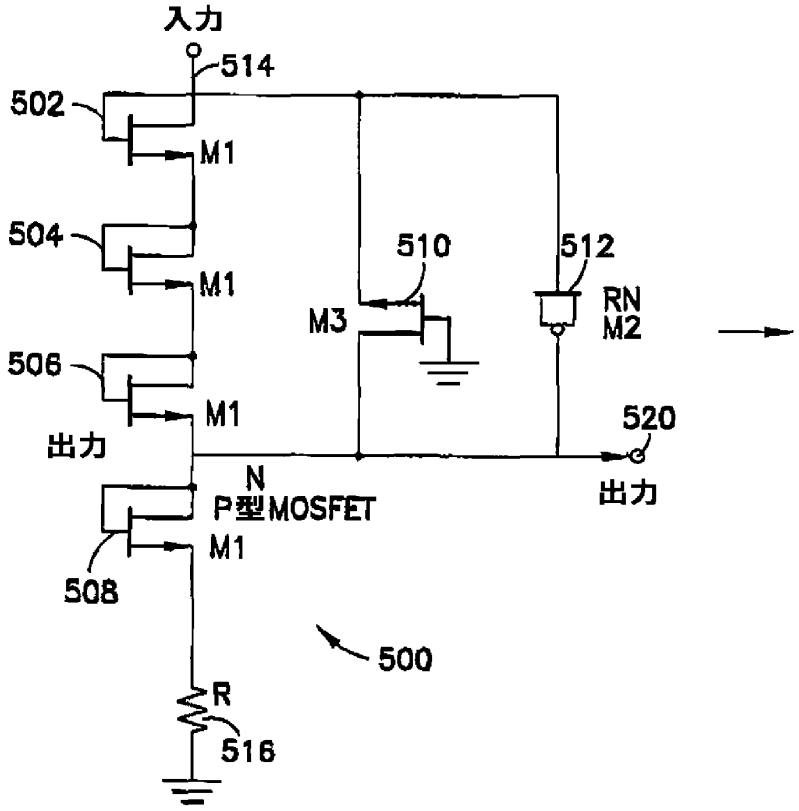
【図8A】


Vdd
328
IN
302
306
OUT1
314
OUT_
304
-Vdd
Vdd
OUT1
404
408
OUT→"SW"
416
OUT1
406
RF スイッチ 300 へ
-Vdd
Vdd
330
IN_
308
312
OUT1_
316
OUT1_
310
-Vdd
300
第１段階
Vdd
OUT1_
410
414
OUT→"SW"_
418
OUT1_
412
402
-Vdd
第２段階
400

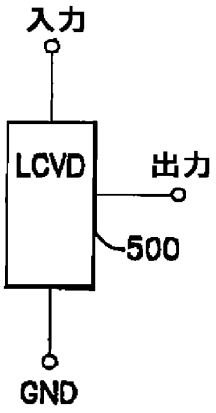
【図8B】


RFバッファ
制御入力
SW
SW_
$-V_{dd}$

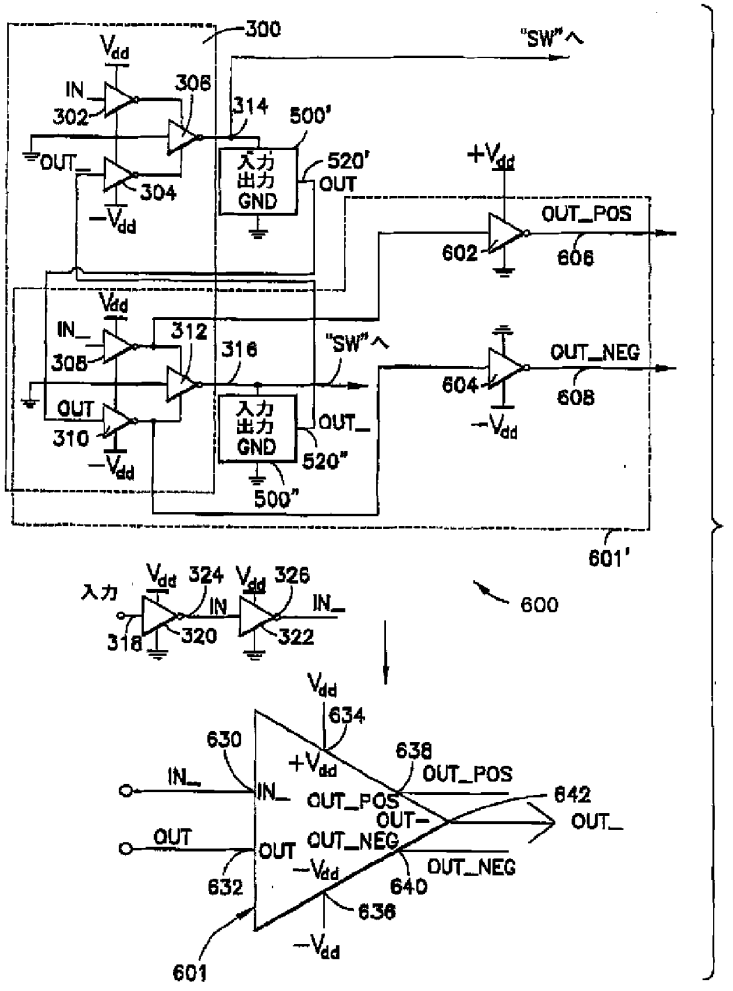
【図9A】


入力
514
502
M1
504
M1
510
512
M3
RN
M2
506
M1
520
出力
出力
N
P型MOSFET
M1
508
500
R
516

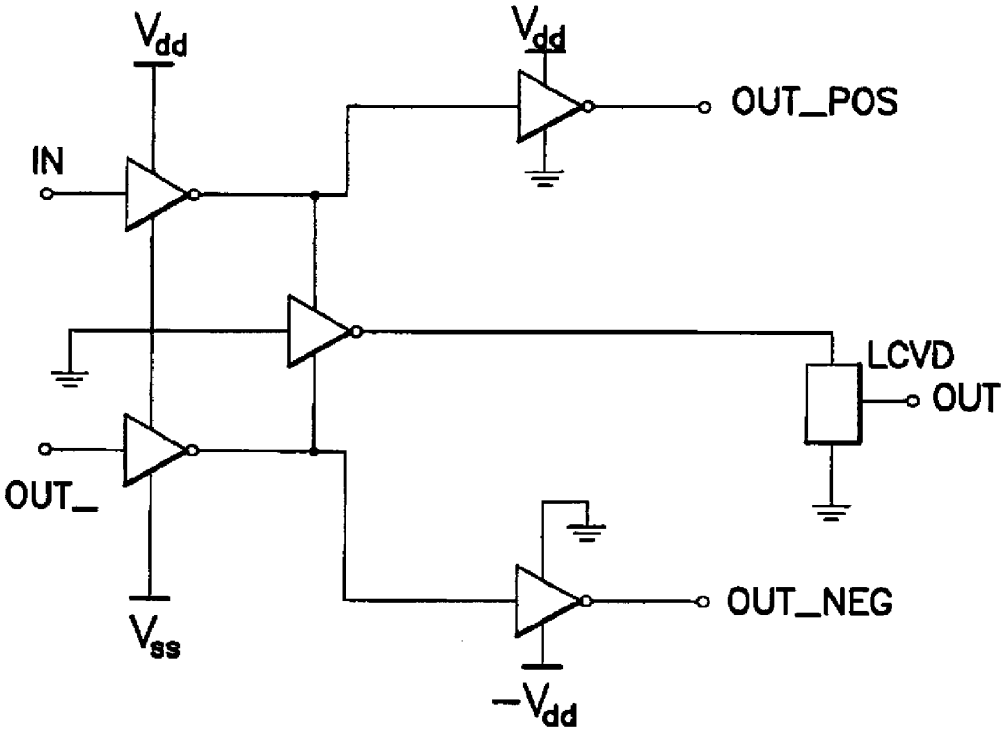
【図9B】



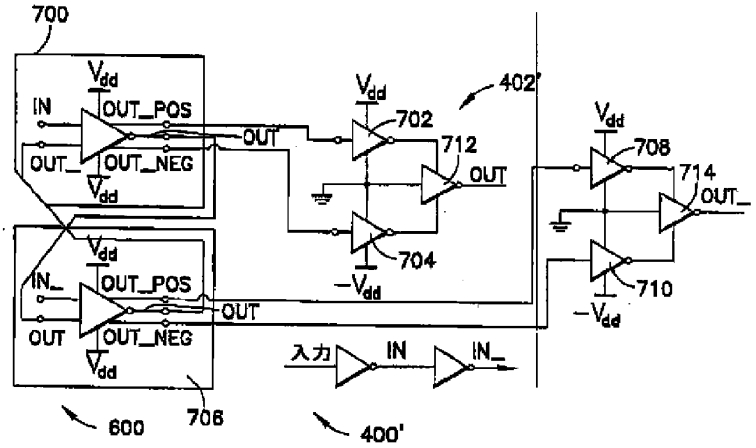
【図10】


300
"SW"へ
Vdd
IN
302
306
314
500'
OUT_
304
−Vdd
入力
出力
GND
520'
OUT
+Vdd
OUT_POS
602
606
IN_
308
312
316
"SW"へ
OUT_NEG
604
608
OUT
310
520"
500"
601'
入力
324
326
IN
IN_
318
320
322
600
630
634
638
IN_
OUT_POS
642
OUT
OUT_NEG
632
640
636
601

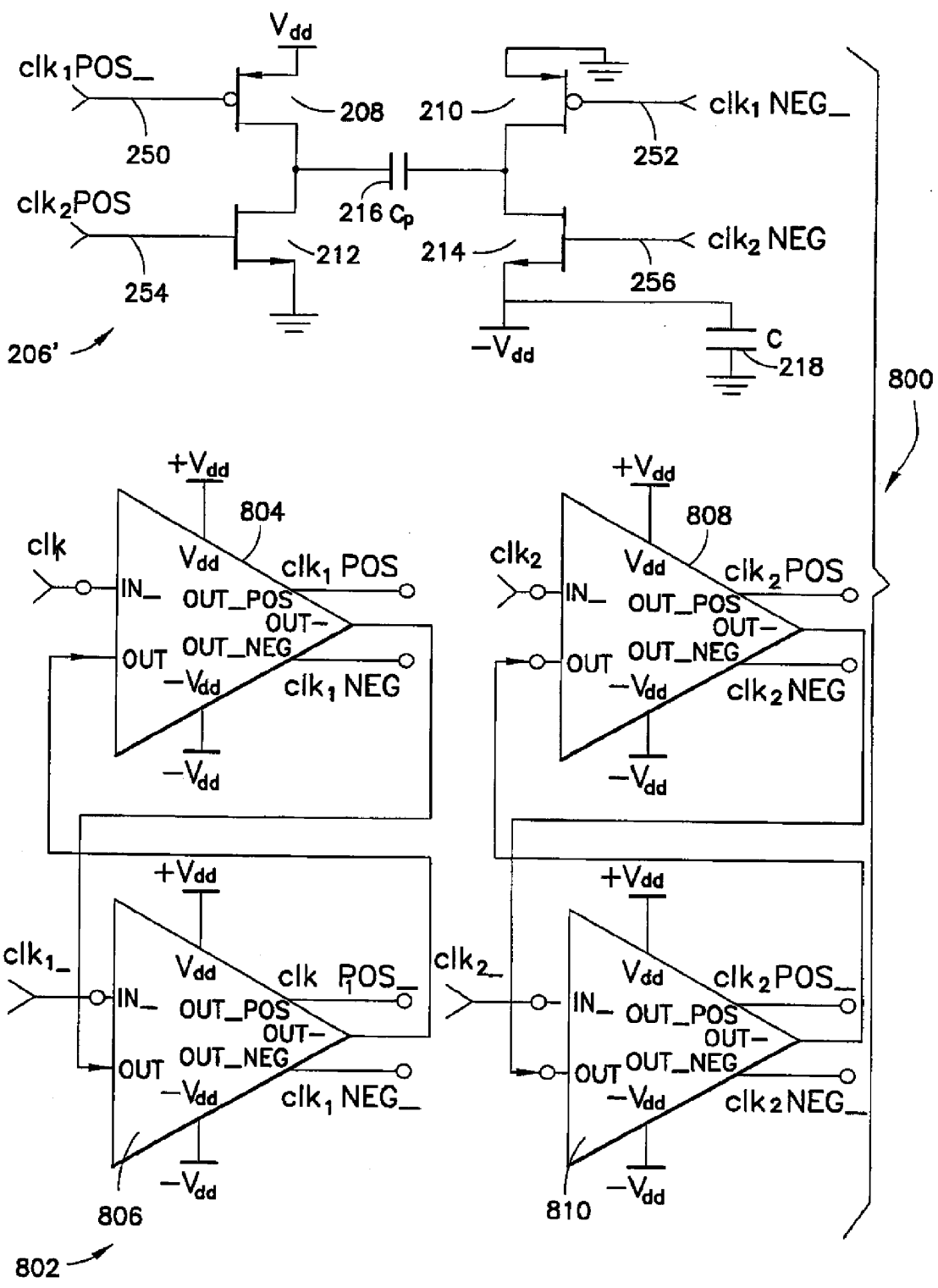
【図11A】


Vdd
Vdd
OUT_POS
IN
LCVD
OUT
OUT_
Vss
OUT_NEG
−Vdd

【図11B】


700
Vdd
IN
OUT_POS
OUT
OUT_
OUT_NEG
Vdd
Vdd
IN_
OUT_POS
OUT
OUT
OUT_NEG
Vdd
600
706
Vdd
402'
702
712
OUT
704
−Vdd
入力
IN
IN_
400'
Vdd
708
714
OUT_
710
−Vdd

【図12】



【手続補正書】
【提出日】平成15年11月3日(2003.11.3)

【手続補正1】
【補正対象書類名】特許請求の範囲
【補正対象項目名】全文
【補正方法】変更
【補正の内容】
【特許請求の範囲】
【請求項1】
（ａ）　第１のＲＦ入力信号を受信する第１の入力ポートと、
（ｂ）　第２のＲＦ入力信号を受信する第２の入力ポートと、
（ｃ）　ＲＦ共通ポートと、
（ｄ）　各トランジスタが少なくとも約３０ｋΩのゲート抵抗を有する、積層構成に配置された複数のトランジスタを含む第１のスイッチトランジスタ・グループであって、前記第１の入力ポートに結合された第１のノードと、前記ＲＦ共通ポートに結合された第２のノードとを有し、スイッチ制御信号（ＳＷ）によって制御される第１のスイッチトランジスタ・グループと、
（ｅ）　各トランジスタが少なくとも約３０ｋΩのゲート抵抗を有する、積層構成に配置された複数のトランジスタを含む第２のスイッチトランジスタ・グループであって、前記第２の入力ポートに結合された第１のノードと、前記ＲＦ共通ポートに結合された第２のノードとを有し、前記スイッチ制御信号（ＳＷ）の反転信号（ＳＷ＿）によって制御される第２のスイッチトランジスタ・グループと、
（ｆ）　各トランジスタが少なくとも約３０ｋΩのゲート抵抗を有する、積層構成に配置された複数のトランジスタを含む第１の分路トランジスタ・グループであって、前記第２の入力ポートに結合された第１のノードと、グラウンドに結合された第２のノードとを有し、前記スイッチ制御信号（ＳＷ）によって制御される、第１の分路トランジスタグループと、
（ｇ）　各トランジスタが少なくとも約３０ｋΩのゲート抵抗を有する、積層構成に配置された複数のトランジスタを含む第２の分路トランジスタ・グループであって、前記第１の入力ポートに結合された第１のノードと、グラウンドに結合された第２のノードとを有し、前記スイッチ制御信号（ＳＷ）の反転信号（ＳＷ＿）によって制御される、第２の分路トランジスタグループと、を含む、ＲＦ信号をスイッチングするためのＲＦスイッチ回路であって、
前記スイッチ制御信号ＳＷが有効であるとき、前記第１のスイッチトランジスタ・グループおよび前記第１の分路トランジスタグループが作動する一方、前記第２のスイッチトランジスタ・グループおよび前記第２の分路トランジスタグループは不作動となり、それにより、前記第１のＲＦ入力信号を前記ＲＦ共通ポートへ通過させて、前記第２のＲＦ入力信号をグラウンドへ分路し、前記スイッチ制御信号ＳＷが非有効であるときには、前記第２のスイッチトランジスタ・グループおよび前記第２の分路トランジスタグループが作動する一方、前記第１のスイッチトランジスタ・グループおよび前記第１の分路トランジスタグループは不作動となり、それにより、前記第２のＲＦ入力信号を前記ＲＦ共通ポートへ通過させて、前記第１のＲＦ入力信号をグラウンドへ分路するＲＦスイッチ回路。
【請求項2】
シリコンオンインシュレータ（ＳＯＩ）技術において製造される、請求項１に記載のＲＦスイッチ回路。
【請求項3】
極薄シリコン（「ＵＴＳｉ」）基板上に製造される、請求項１に記載のＲＦスイッチ回路。
【請求項4】
前記トランジスタグループが、完全絶縁性サファイアウエハ上の薄いシリコン層に形成される並列ＭＯＳＦＥＴトランジスタを含み、前記完全絶縁性サファイアウエハが、基板の結合効果を減少することによって、前記ＲＦスイッチの性能特性を向上させる、請求項

３に記載のＲＦスイッチ回路。
【請求項5】
スイッチ挿入損失が、前記ＭＯＳＦＥＴトランジスタのオン抵抗を減少することにより減少される、請求項４に記載のＲＦスイッチ回路。
【請求項6】
前記ＲＦスイッチのスイッチ分離特性が、前記ＭＯＳＦＥＴトランジスタのノード間の寄生容量を減少することにより改善される、請求項４に記載のＲＦスイッチ回路。
【請求項7】
前記トランジスタグループが、複数のＭＯＳＦＥＴトランジスタを含む、請求項３に記載のＲＦスイッチ回路。
【請求項8】
前記ＭＯＳＦＥＴトランジスタが、通常スイッチング電圧によって制御されるゲート抵抗器を含む、請求項７に記載のＲＦスイッチ回路。
【請求項9】
前記第１のスイッチトランジスタ・グループおよび前記第１の分路トランジスタグループのトランジスタゲート・ノードに結合された前記ゲート抵抗器が、通常、前記スイッチ制御信号ＳＷによって制御される、請求項８に記載のＲＦスイッチ回路。
【請求項10】
前記第２のスイッチトランジスタ・グループおよび前記第２の分路トランジスタグループのトランジスタゲート・ノードに結合された前記ゲート抵抗器が、通常、前記反転スイッチ制御信号ＳＷ＿によって制御される、請求項８に記載のＲＦスイッチ回路。
【請求項11】
前記トランジスタグループ内の各ＭＯＳＦＥＴトランジスタに関連する前記ＲＣ時定数が、前記ＲＦ入力信号の周期をはるかに超え、それによって、ＲＦ電圧が、前記ＭＯＳＦＥＴトランジスタ全体で等しく共用される、請求項８に記載のＲＦスイッチ回路。
【請求項12】
選択したトランジスタグループの、前記複数の積層ＭＯＳＦＥＴトランジスタ全体の降伏電圧が、前記選択したトランジスタグループの個別ＭＯＳＦＥＴトランジスタの降伏電圧のｎ倍に効果的に増加され、ｎが、前記選択したトランジスタグループにおけるＭＯＳＦＥＴトランジスタの総計を含む、請求項８に記載のＲＦスイッチ回路。
【請求項13】
関連する１ｄＢ圧縮ポイントを有し、前記１ｄＢ圧縮ポイントを、前記積層ＭＯＳＦＥＴトランジスタ構成を用いて増加する、請求項１２に記載のＲＦスイッチ回路。
【請求項14】
前記第１のＲＦ入力信号および前記第２のＲＦ入力信号が、関連する入力電力レベルを有し、増加した入力電力レベルを、トランジスタグループごとのＭＯＳＦＥＴトランジスタの数を増加することによって、前記ＲＦスイッチ回路で調節できる、請求項７に記載のＲＦスイッチ回路。
【請求項15】
前記第１のＲＦ入力信号および前記第２のＲＦ入力信号が、関連する入力電力レベルを有し、増加した入力電力レベルを、トランジスタグループの実現に使用するトランジスタの物理的サイズを変えることによって、前記ＲＦスイッチ回路で調節できる、請求項７に記載のＲＦスイッチ回路。
【請求項16】
（ａ）　請求項３に記載のＲＦスイッチ回路と、
（ｂ）　前記スイッチ制御信号（ＳＷ）および前記反転スイッチ制御信号（ＳＷ＿）を出力する、前記ＲＦスイッチ回路に結合された制御論理ブロックと、
（ｃ）　クロック入力信号および外部電源からの正の電源電圧を受取り、負の電源電圧を出力する、前記制御論理ブロックに結合された負電圧発生器と、
を含む、完全に集積化されたＲＦスイッチ回路。

【請求項17】
前記ＲＦスイッチ回路が、複数のデジタル回路およびアナログ回路とともに、集積回路（ＩＣ）に集積されている、請求項１６に記載の完全に集積化されたＲＦスイッチ回路。
【請求項18】
（ａ）（ｉ）　第１のＲＦ入力信号を受信する第１の入力ポートと、
（ｉｉ）　第２のＲＦ入力信号を受信する第２の入力ポートと、
（ｉｉｉ）　ＲＦ共通ポートと、
（ｉｖ）　前記第１の入力ポートに結合された第１のノードと、前記ＲＦ共通ポートに結合された第２のノードとを有し、スイッチ制御信号（ＳＷ）によって制御される第１のスイッチトランジスタ・グループと、
（ｖ）　前記第２の入力ポートに結合された第１のノードと、前記ＲＦ共通ポートに結合された第２のノードとを有し、前記スイッチ制御信号（ＳＷ）の反転信号（ＳＷ＿）によって制御される第２のスイッチトランジスタ・グループと、
（ｖｉ）　前記第２の入力ポートに結合された第１のノードと、グラウンドに結合された第２のノードとを有し、前記スイッチ制御信号（ＳＷ）によって制御される、第１の分路トランジスタグループと、
（ｖｉｉ）　前記第１の入力ポートに結合された第１のノードと、グラウンドに結合された第２のノードとを有し、前記スイッチ制御信号（ＳＷ）の反転信号（ＳＷ＿）によって制御される、第２の分路トランジスタグループと、
を含む、ＲＦスイッチ回路であって、ＳＷが作動しているとき、前記第１のスイッチトランジスタ・グループおよび前記第１の分路トランジスタグループが作動する一方、前記第２のスイッチトランジスタ・グループおよび前記第２の分路トランジスタグループは不作動となり、それにより、前記第１のＲＦ入力信号を前記ＲＦ共通ポートへ通過させて、前記第２のＲＦ入力信号をグラウンドへ分路し、ＳＷが不作動のときには、前記第２のスイッチトランジスタ・グループおよび前記第２の分路トランジスタグループが作動する一方、前記第１のスイッチトランジスタ・グループおよび前記第１の分路トランジスタグループは不作動となり、それにより、前記第２のＲＦ入力信号を前記ＲＦ共通ポートへ通過させて、前記第１のＲＦ入力信号をグラウンドへ分路し、また、極薄シリコン（「ＵＴＳｉ」）基板上に製造されるＲＦスイッチ回路と、
（ｂ）　前記ＲＦスイッチ回路に結合され、前記スイッチ制御信号（ＳＷ）および前記反転スイッチ制御信号（ＳＷ＿）を出力する制御論理ブロックと、
（ｃ）　前記制御論理ブロックに結合され、クロック入力信号と、外部電源からの正の電源電圧とを供給され、負の電源電圧を出力する負電圧発生器と、
（ｄ）　クロック入力信号を出力する発振器と、
（ｅ）　前記クロック入力信号を入力する前記発振器に結合され、負の電源電圧を出力する電荷ポンプと、
（ｆ）　前記電荷ポンプに結合され、前記スイッチトランジスタ・グループおよび前記分路トランジスタグループの制御に使用する制御信号を出力する論理回路ブロックと、
（ｇ）　前記論理回路ブロックおよび前記ＲＦスイッチ回路に結合され、前記トランジスタグループを実現するために使用するＭＯＳＦＥＴトランジスタのゲートードレイン、ゲートーソースおよびドレインーソース電圧を減少するレベルシフト回路と、
（ｈ）　前記ＲＦスイッチ回路に結合され、ＲＦ信号エネルギを、前記電荷ポンプブロックおよび前記論理回路ブロックから分離するＲＦバッファ回路と、
を含む完全に集積化されたＲＦスイッチ回路。
【請求項19】
前記電荷ポンプが、
（ａ）　少なくとも２つのＰチャネルＭＯＳＦＥＴトランジスタと、
（ｂ）　少なくとも２つのＮチャネルＭＯＳＦＥＴトランジスタであって、それぞれが、それぞれの関連するＰチャネルＭＯＳＦＥＴトランジスタと直列に結合され、それによって、前記電荷ポンプのそれぞれのレッグを形成するＮチャネルＭＯＳＦＥＴトランジス

タと、
（ｃ）　連続レッグに結合された前記電荷ポンプの各レッグを結合する、少なくとも１つの結合キャパシタと、
（ｄ）　前記電荷ポンプの出力レッグに結合された出力キャパシタと、
を含み、
前記負の電源電圧を、前記ＰチャネルＭＯＳＦＥＴトランジスタおよび前記ＮチャネルＭＯＳＦＥＴトランジスタを駆動するための、非重複入力クロック信号を用い、前記結合キャパシタおよび前記出力キャパシタを交互に充電および放電することによって、前記電荷ポンプで発生する、請求項１８に記載の完全に集積化されたＲＦスイッチ回路。
【請求項20】
前記非重複入力クロック信号が、２つの非重複クロック制御信号を含み、第１の非重複クロック制御信号がＰチャネルトランジスタを制御し、第２の非重複クロック制御信号がＮチャネルトランジスタを制御する、請求項１９に記載の完全に集積化されたＲＦスイッチ回路。
【請求項21】
前記Ｐチャネルトランジスタおよび前記Ｎチャネルトランジスタが、単一閾値トランジスタである、請求項１９に記載の完全に集積化されたＲＦスイッチ回路。
【請求項22】
前記非重複入力クロック信号が、パルスシフト回路によって発生される、請求項１９に記載の完全に集積化されたＲＦスイッチ回路。
【請求項23】
前記非重複入力クロック信号が、前記発振器クロック入力信号から引き出される、請求項１９に記載の完全に集積化されたＲＦスイッチ回路。
【請求項24】
前記発振器が、弛張発振器を含む、請求項１９に記載の完全に集積化されたＲＦスイッチ回路。
【請求項25】
前記非重複入力クロック信号が、－Ｖｄｄから＋Ｖｄｄまでの電圧振幅で変化する、請求項１９に記載の完全に集積化されたＲＦスイッチ回路。
【請求項26】
前記レベルシフト回路が、フィードバック構成でともに結合された複数のインバータを含む、請求項１８に記載の完全に集積化されたＲＦスイッチ回路。
【請求項27】
前記インバータが、第１の差動入力と、第２の差動入力と、論理入力と、論理出力とを含み、前記レベルシフト回路が、
（ａ）　２つの入力差動インバータを含む入力インバータグループであって、第１の入力差動インバータが論理入力信号（ｉｎｐｕｔ）を受信して、第１の論理入力信号（ｉｎ）を出力し、第２の入力差動インバータが、前記第１の論理入力信号（ｉｎ）を受信し、前記第１の論理入力信号の逆（ｉｎ＿）を出力する入力インバータグループと、
（ｂ）　３つの差動インバータを含む第１のインバータグループであって、前記第１のインバータグループにおける第１のインバータの前記論理出力が、前記第１の論理入力信号（ｉｎ）に結合され、前記第１のインバータの前記論理出力が、前記第１のインバータグループにおける出力インバータの第１の差動入力に結合され、前記第１のインバータグループにおける第２のインバータの前記論理出力が、前記第１のインバータグループにおける前記出力インバータの第２の差動入力に結合され、前記第１のインバータグループの前記出力インバータが、第１の出力信号（ｏｕｔ）を出力する第１のインバータグループと、
（ｃ）　３つの差動インバータを含む第２のインバータグループであって、前記第２のインバータグループの第１のインバータの前記論理出力が、前記第１の論理入力信号の前記逆（ｉｎ＿）に結合され、前記第２のインバータグループにおける前記第１のインバー

タの前記論理出力が、前記第２のインバータグループにおける出力インバータの第１の差動入力に結合され、前記第２のインバータグループにおける第２のインバータの前記論理出力が、前記第２のインバータグループにおける前記出力インバータの第２の差動入力に結合され、前記第２のインバータグループにおける前記出力インバータが、第２の出力信号（ｏｕｔ＿）を出力する前記第２のインバータグループと、を含み、

前記第１の出力信号（ｏｕｌ）がフィードバックとして供給されて、前記第２のインバータグループにおける前記第２のインバータの論理入力部に入力され、前記第２の出力信号（ｏｕｔ＿）が、フィードバックとして供給されて、前記第１のインバータグループにおける前記第２のインバータの論理入力部に入力される請求項２６に記載の完全に集積化されたＲＦスイッチ回路。

【請求項28】

前記第１の出力信号および前記第２の出力信号が、前記ＲＦスイッチの、前記スイッチトランジスタ・グループおよび前記分路トランジスタグループを制御する、請求項２７に記載の完全に集積化されたＲＦスイッチ回路。

【請求項29】

前記レベルシフト回路が、前記入力信号の周波数応答に影響を与えずに、前記論理入力信号（ｉｎｐｕｔ）の直流レベルをシフトする、請求項２６に記載の完全に集積化されたＲＦスイッチ回路。

【請求項30】

前記ＲＦバッファ回路が、第１段階レベルシフト回路および第２段階ＲＦバッファ回路を含む２段階回路を含み、前記第１段階レベルシフト回路が、請求項２７で定義されたレベルシフト回路を含み、前記第２段階ＲＦバッファ回路が、第２の複数の差動インバータを含み、前記第２の複数の差動インバータが、それぞれ、第１の差動入力と、第２の差動入力と、論理入力と、論理出力とを有し、前記第２段階ＲＦバッファ回路が、さらに、

（ａ）　３つの差動インバータを含む第１のＲＦバッファインバータ・グループであって、前記第１のＲＦバッファインバータ・グループにおける第１のインバータと第２のインバータの前記論理入力が、前記レベルシフト回路によって、前記第１の出力信号（ｏｕｔ）出力に結合され、前記第１のＲＦバッファインバータ・グループにおける前記第１のインバータの前記論理出力が、前記第１のＲＦバッファインバータ・グループにおける出力インバータの第１の差動入力に結合され、前記第１のＲＦバッファインバータ・グループにおける、前記第２のインバータの前記論理出力が、前記第１のＲＦバッファインバータ・グループにおける前記出力インバータの第２の差動入力に結合され、前記第１のＲＦバッファインバータ・グループの前記出力インバータが、第１の出力信号（ＯＵＴ）を出力する第１のＲＦバッファインバータ・グループと、

（ｂ）　３つの差動インバータを含む第２のＲＦバッファインバータ・グループであって、前記第２のＲＦバッファインバータ・グループにおける第１のインバータと第２のインバータの前記論理入力が、前記レベルシフト回路によって、前記第２の出力信号（ｏｕｔ＿）出力に結合され、前記第２のＲＦバッファインバータ・グループにおける前記第１のインバータの前記論理出力が、前記第２のＲＦバッファインバータ・グループにおける出力インバータの第１の差動入力に結合され、前記第２のＲＦバッファインバータ・グループにおける前記第２のインバータの前記論理出力が、前記第２のＲＦバッファインバータ・グループにおける前記出力インバータの第２の差動入力に結合され、前記第２のＲＦバッファインバータ・グループの前記出力インバータが、第２の出力信号（ＯＵＴ＿）を出力する第２のＲＦバッファインバータ・グループと、

を含む、請求項１８に記載の完全に集積化されたＲＦスイッチ回路。

【請求項31】

前記ＲＦバッファ回路が、デジタル論理信号を前記ＲＦスイッチ回路から分離する、請求項３０に記載の完全に集積化されたＲＦスイッチ回路。

【請求項32】

前記第２段階ＲＦバッファ回路が、前記出力信号ＯＵＴおよびＯＵＴ＿のフィードバッ

クを、前記第１段階レベルシフト回路に供給せず、それによって、前記デジタル論理信号からの、前記ＲＦスイッチの分離を改善する、請求項３１に記載の完全に集積化されたＲＦスイッチ回路。

【請求項33】

前記第１段階レベルシフト回路を実現するために使用するトランジスタが、前記第２段階ＲＦバッファ回路を実現するために使用するトランジスタよりも小さい、請求項３０に記載の完全に集積化されたＲＦスイッチ回路。

【請求項34】

前記出力信号（ｏｕｔ）および（ｏｕｔ＿）に結合された分圧器回路をさらに含み、前記分圧器回路が、前記出力信号の電圧レベルを制限し、その後、前記出力信号が、前記第１インバータグループおよび前記第２インバータグループの前記第２のインバータにフィードバックとして供給される、請求項２７に記載の完全に集積化されたＲＦスイッチ回路。

【請求項35】

前記分圧器回路が、前記電圧レベルを、ほぼＶｄｄに制限する、請求項３４に記載の完全に集積化されたＲＦスイッチ回路。

【請求項36】

前記分圧器が、直列構成にともに結合された複数のＭＯＳＦＥＴデバイスを含み、出力ＭＯＳＦＥＴデバイスが、バラスト抵抗器を介してグラウンドノードに結合され、前記ＭＯＳＦＥＴデバイスが、ダイオード機能を果たす、請求項３４に記載の完全に集積化されたＲＦスイッチ回路。

【請求項37】

前記ＲＦバッファ回路が、第１段階レベルシフト回路と第２段階ＲＦバッファ回路とを含む２段階回路を含み、前記第１段階レベルシフト回路が、請求項３４で定義されたレベルシフト回路を含み、前記第２段階ＲＦバッファ回路が、第２の複数の差動インバータを含み、前記第２の複数の差動インバータが、それぞれ、第１の差動入力と、第２の差動入力と、論理入力と、論理出力とを含み、前記第２段階ＲＦバッファ回路が、さらに、

（ａ）　３つの差動インバータを含む第１のＲＦバッファインバータ・グループであって、前記第１のＲＦバッファインバータ・グループにおける第１のインバータの前記論理入力が、前記レベルシフト回路によって、第１の出力信号（ｏｕｔ＿ｐｏｓ１）出力に結合され、前記第１のＲＦバッファインバータ・グループにおける第２のインバータの前記論理入力が、前記レベルシフト回路によって、第２の出力信号（ｏｕｔ＿ｎｅｇ１）出力に結合され、前記第１のＲＦバッファインバータ・グループにおける前記第１のインバータの前記出力が、前記第１のＲＦバッファインバータ・グループにおける出力インバータの第１の差動入力に結合され、前記第１のＲＦバッファインバータ・グループにおける前記第２のインバータの前記論理出力が、前記第１のＲＦバッファインバータ・グループにおける前記出力インバータの第２の差動入力に結合され、前記第１のＲＦバッファインバータ・グループの前記出力インバータが、第１の出力信号（ＯＵＴ）を出力する第１のＲＦバッファインバータ・グループと、

（ｂ）　３つの差動インバータを含む第２のＲＦバッファインバータ・グループであって、前記第２のＲＦバッファインバータ・グループにおける第１のインバータの前記論理入力が、前記レベルシフト回路によって、第３の出力信号（ｏｕｔ＿ｐｏｓ２）出力に結合され、前記第２のＲＦバッファインバータ・グループにおける第２のインバータの前記論理入力が、前記レベルシフト回路によって、第４の出力信号（ｏｕｔ＿ｎｅｇ２）出力に結合され、前記第２のＲＦバッファインバータ・グループにおける前記第１のインバータの前記出力が、前記第２のＲＦバッファインバータ・グループにおける出力インバータの第１の差動入力に結合され、前記第２のＲＦバッファインバータ・グループにおける、前記第２のインバータの前記論理出力が、前記第２のＲＦバッファインバータ・グループにおける前記出力インバータの第２の差動入力に結合され、前記第２のＲＦバッファインバータ・グループの前記出力インバータが、第２の出力信号（ＯＵＴ＿）を出力する第２

のＲＦバッファインバータ・グループと、を含み、
　前記第１の出力信号（ｏｕｔ＿ｐｏｓ１）が、前記レベルシフト回路の前記第１のインバータグループにおける前記第１のインバータのバッファされた出力を含み、前記第２の出力信号（ｏｕｔ＿ｎｅｇ１）が、前記レベルシフト回路の前記第１のインバータグループにおける前記第２のインバータのバッファされた出力を含み、前記第３の出力信号（ｏｕｌ＿ｐｏｓ２）が、前記レベルシフト回路の前記第２のインバータグループにおける前記第１のインバータのバッファされた出力を含み、前記第４の出力信号（ｏｕｔ＿ｎｅｇ２）が、前記レベルシフト回路の前記第２のインバータグループにおける前記第２のインバータのバッファされた出力を含む、請求項１８に記載の完全に集積化されたＲＦスイッチ回路。
【請求項38】
　前記非重複入力クロック信号が、請求項３４で定義されるレベルシフト回路へ入力され、その後前記電荷ポンプへ入力される、請求項２０に記載の完全に集積化されたＲＦスイッチ回路。
【請求項39】
　前記レベルシフト回路が、第１のレベルシフト回路と第２のレベルシフト回路とを含み、前記第１のレベルシフト回路と前記第２のレベルシフト回路が請求項３４で定義され、前記第１のレベルシフト回路が、その第１のインバータグループにおける前記第１のインバータの前記論理出力から第１の出力信号（ｃｌｋ１ｐｏｓ）を出力し、その第１のインバータグループにおける前記第２のインバータの前記論理出力から第２の出力信号（ｃｌｋ１ｎｅｇ）を出力し、その第２のインバータグループにおける前記第１のインバータの前記論理出力から第３の出力信号（ｃｌｋ１ｐｏｓ＿）を出力し、その第２のインバータグループにおける前記第２のインバータの前記論理出力から第４の出力信号（ｃｌｋ１ｎｅｇ＿）を出力し、前記第２のレベルシフト回路が、その第１のインバータグループにおける前記第１のインバータの前記論理出力から第５の出力信号（ｃｌｋ２ｐｏｓ）を出力し、その第１のインバータグループにおける前記第２のインバータの前記論理出力から第６の出力信号（ｃｌｋ２ｎｅｇ）を出力し、その第２のインバータグループにおける前記第１のインバータの前記論理出力から第７の出力信号（ｃｌｋ２ｐｏｓ＿）を出力し、その第２のインバータグループにおける前記第２のインバータの前記論理出力から第８の出力信号（ｃｌｋ２ｎｅｇ＿）を出力する、請求項３８に記載の完全に集積化されたＲＦスイッチ回路。
【請求項40】
　前記第３の出力信号（ｃｌｋ１ｐｏｓ＿）が、前記電荷ポンプの第１のＰチャネルＭＯＳＦＥＴトランジスタを制御し、前記第４の出力信号（ｃｌｋ１ｎｅｇ＿）が、前記電荷ポンプの第２のＰチャネルＭＯＳＦＥＴトランジスタを制御し、前記第５の出力信号（ｃｌｋ２ｐｏｓ）が、前記第１のＰチャネルＭＯＳＦＥＴトランジスタに関連する第１のＮチャネルＭＯＳＦＥＴトランジスタを制御し、前記第６の出力信号（ｃｌｋ２ｎｃｇ）が、前記第２のＰチャネルＭＯＳＦＥＴトランジスタに関連する第２のＮチャネルＭＯＳＦＥＴトランジスタを制御する、請求項３９に記載の完全に集積化されたＲＦスイッチ回路。
【請求項41】
　（ａ）　複数の積層トランジスタを含む第１のスイッチトランジスタ・グループおよび第１の分路トランジスタグループに、第１のＲＦ入力信号を入力するステップと、
　（ｂ）　複数の積層トランジスタを含む第２のスイッチトランジスタ・グループおよび第２の分路トランジスタグループに、第２のＲＦ入力信号を入力するステップと、
　（ｃ）　前記第１のスイッチトランジスタ・グループを作動する一方、前記第１の分路トランジスタグループを不作動にし、同時に、前記第２のスイッチトランジスタ・グループを不作動にする一方、前記第２の分路トランジスタグループを作動し、それによって、前記第１のＲＦ入力信号を通過させ、前記第２のＲＦ入力信号を分路させるステップと、
　（ｄ）　前記第２のスイッチトランジスタ・グループを作動する一方、前記第２の分路

トランジスタグループを不作動にし、同時に、前記第１のスイッチトランジスタ・グループを不作動にする一方、前記第１の分路トランジスタグループを作動し、それによって、前記第２のＲＦ入力信号を通過させ、前記第１のＲＦ入力信号を分路させるステップと、を含む、ＲＦ信号をスイッチングする方法。

【手続補正書】
【提出日】平成16年6月9日(2004.6.9)
【手続補正1】
【補正対象書類名】明細書
【補正対象項目名】全文
【補正方法】変更
【補正の内容】
【書類名】明細書
【０００１】
関連仮出願優先権主張の相互参照
本発明は、係属中の米国仮出願第６０／３２８，３５３号（２００１年１０月１０日出願、名称「シリコンオンインシュレータ（Ｓｉｌｉｃｏｎ－Ｏｎ－Ｉｎｓｕｌａｔｏｒ）ＲＦスイッチ」）について、米国法典第３５編１１９条（ｅ）項の利益を主張し、その内容を全体として、本明細書に援用している。
【技術分野】
【０００２】
発明の背景
発明の分野
本発明はスイッチに関し、特に、集積回路内のスイッチ回路および高周波（ＲＦ）信号のスイッチング方法に関する。一実施形態では、このスイッチ回路には、無線通信設備、衛星およびケーブルテレビなどＲＦの適用分野において使用するための、シリコンオンインシュレータ（ＳＯＩ）上に実現するＣＭＯＳデバイスが含まれる。
【背景技術】
【０００３】
関連技術の説明
周知のように、高周波（ＲＦ）スイッチは、多くの無線通信システムにおいて、重要な構成ブロックとなっている。ＲＦスイッチは、携帯電話機、無線ページャ、無線インフラ設備、衛星通信設備およびケーブルテレビ設備などの多くの異なる通信設備に使用されている。周知のように、ＲＦスイッチの性能は、３つの主な動作性能パラメータ、すなわち挿入損失、スイッチ分離および「１ｄＢ圧縮ポイント」によって決められる。これら３つの性能パラメータは緊密に結びついており、ＲＦスイッチ構成要素の設計において、いずれか１つのパラメータを重視すると、他のパラメータを犠牲にすることになる。ＲＦスイッチ設計において時々考慮される第４のパラメータは、通常、スイッチング時間またはスイッチング速度（スイッチの片側をオンにし、反対側をオフにするのに必要な時間と定義される）と呼ばれている。ＲＦスイッチの設計において重要な他の指標には、ＲＦスイッチ集積の容易さと程度（レベル）、複雑さ、歩留まり、返品損失および製造コストが含まれる。
【０００４】
これらのＲＦスイッチの性能パラメータは、図１ａ～１ｃの簡易回路図に示す、先行技術によるＲＦスイッチ設計を参照して、より簡単に説明できる。図１ａに、先行技術の単極単投（ＳＰＳＴ）ＲＦスイッチ１０の簡易回路図を示す。先行技術のＳＰＳＴスイッチ１０には、スイッチングトランジスタＭ１（５）および分路トランジスタＭ２（７）が含まれる。ここで図１ａを参照すると、２つのＭＯＳＦＥＴトランジスタＭ１（５）およびＭ２（７）の制御電圧の状態に依存して（すなわち、ＭＯＳＦＥＴスイッチングトランジスタＭ１および分路トランジスタＭ２のゲート入力部にそれぞれ印加される直流バイアス

に依存して）、ＲＦ信号は、ＲＦ入力ノード１からＲＦ出力ノード３へ送られるか、または分路トランジスタＭ２（７）を介してグラウンドへ分路される。直流バイアス電圧の実際の値は、ＭＯＳＦＥＴトランジスタＭ１（５）およびＭ２（７）の極性と閾値次第である。ＲＦ電源信号と直列の抵抗器Ｒ０（９）は、電源信号からバイアスを分離するものであり、最高のスイッチ性能にとって必須である。図１ｂに、図１ａにおけるＲＦスイッチ１０の「オン」状態を示す（すなわち、図１ｂには、ＲＦスイッチ１０が「オン」、スイッチングトランジスタＭ１（５）がオンおよび分路トランジスタＭ２（７）がオフのときの、トランジスタＭ１およびＭ２の等価小信号値を示す）。図１ｃに、図１ａのスイッチ１０の「オフ」状態を示す（すなわち、図１ｃには、ＲＦスイッチ１０が「オフ」、スイッチングトランジスタＭ１（５）がオフおよび分路トランジスタＭ２（７）がオンのときの、トランジスタＭ１およびＭ２の等価小信号値を示す）。

【０００５】

図１ｂに示すように、ＲＦスイッチ１０がオンのとき、スイッチングトランジスタＭ１（５）は主に抵抗性であり、一方、分路トランジスタＭ２（７）は主に容量性である。ＲＦスイッチ１０の「挿入損失」は、入力ノード１における最大利用可能電力と出力ノード３の負荷に供給される電力間の差異から決定される。低周波においては、スイッチ１０がオンのとき（図１ｂを参照されたい）、電力損失はいずれも、スイッチングトランジスタＭ１（５）の有限なオン抵抗「ｒ」１３に起因する。オン抵抗ｒ１３（図１ｂ）は、典型的には、電源抵抗器Ｒ０（９）よりもずっと小さい。したがって、挿入損失「ＩＬ」は、以下に示す式１のような特徴がある。

式１：ＩＬはほぼ、１０ｒ／Ｒ０ｌｎ（１０）＝０．０８７ｒ（ｄＢ）に等しい。

【０００６】

したがって、低周波で、ｒの値が３Ωでは、結果として約０．２５ｄＢの挿入損失となる。挿入損失は、ＲＦスイッチ送信機のオン抵抗に大きく左右されるので、トランジスタ・オン抵抗を下げ、寄生基板抵抗を減少させることにより、挿入損失を改善できる。

【０００７】

一般に、ＲＦスイッチの入力－出力分離（または簡単にスイッチ分離）は、入力ポートと出力ポートを接続しているトランジスタがオフのとき、入力ポートから出力ポートへ「流出」する電力量を測ることによって決定する。分離特性は、ＲＦスイッチの切断の程度はどれくらいか（すなわち、スイッチが、入力信号を出力からどの程度ブロックするか）を示す。特に、ここで図１ｃにおけるＲＦスイッチ１０の「オフ」状態を参照すると、スイッチＭ１（５）のオフ状態は、入力１を出力３からブロックする働きをする。分路トランジスタＭ２（７）もまた、スイッチ１０の入力－出力分離を向上させる働きをする。

【０００８】

ターンオフすると（すなわち、ＲＦスイッチ１０およびスイッチングトランジスタＭ１（５）がターンオフするとき）、Ｍ１（５）は、主に容量性であり、入力信号の「フィードスルー」（ＲＦ入力信号が、入力ノード１から出力ノード３へ通ること）は、キャパシタＣＧＤオフ１５（スイッチングトランジスタＭ１がターンオフしたときのゲート－ドレインキャパシタンス）、キャパシタＣＧＳオフ１７（スイッチングトランジスタＭ１がターンオフしたときのゲート－ソースキャパシタンス）およびキャパシタＣＤＳ１（１９）（スイッチングトランジスタＭ１がターンオフしたときのドレイン－ソースキャパシタンス）の直列／並列値によって決定される。入力信号のフィードスルーは望ましくなく、ＲＦスイッチ１０の入力－出力分離に直接関連する。分路トランジスタＭ２（７）を使用してフィードスルーの大きさを減少し、それによってＲＦスイッチの分離特性を向上させる。

【０００９】

図１ｃの分路トランジスタＭ２（７）を、スイッチングトランジスタＭ１（５）がターンオフのとき、ターンオンさせる。この条件では、分路トランジスタＭ２（７）は、主に、値ｒの抵抗器として働く。設計によっては、ｒの値は、ＲＦ電源特有のインピーダンスよりずっと小さい。結果として、ｒは、スイッチングトランジスタＭ１（５）の入力部の

電圧を著しく減少させる。ｒの値が、電源抵抗ＲＯ（９）および分路トランジスタＭ２（７）のフィードスルー容量性抵抗よりもずっと小さいとき、分離は簡単に計算できる。ＲＦスイッチ１０のオフ状態のスイッチ分離は、入力部の最大利用可能電力と出力部の電力間の差異で決定する。

【００１０】

ＲＦスイッチの挿入損失および分離に加えて、別の重要なＲＦスイッチ性能特性は、大きな入力電力を処理する能力である。これは、スイッチをターンオンしたとき、一定の周波数で、挿入損失が入力電力の関数とならないことを、確実なものとすることである。スイッチが、「スイッチオン」したスイッチを通して送られる電力をゆがめないことが、多くの適用分野で求められている。たとえば、２つの近接した音が、同時にＲＦスイッチを通過する場合には、スイッチの非線形性のために、相互変調（ＩＭ）を起こす可能性があり、それにより隣接するチャネルで擬似音声を生成する可能性がある。たとえば、これらの隣接するチャネルを、情報信号のために確保しておく場合には、擬似音声の電力は、できる限り小さく維持しなければならない。スイッチ圧縮または「１ｄＢ圧縮ポイント」（「Ｐ１ｄＢ」）は、電力を処理する能力を示す。Ｐ１ｄＢは、挿入損失がその低電力値から１ｄＢだけ増加したときの入力電力として定義される。または別の言い方をすると、１ｄＢ圧縮ポイントは、出力電力が、入力電力との線形的関係から１ｄＢだけ逸脱する前に、入力ポートでＲＦスイッチに入力できる電力量の程度である。

【００１１】

スイッチ圧縮は、２つの道筋のいずれか１つで発生する。スイッチ圧縮がどのように発生するかを理解するために、図１ａ～１ｃのＲＦスイッチ１０に示すＭＯＳＦＥＴトランジスタの動作について説明する。トランジスタ設計分野においては周知のように、ＭＯＳＦＥＴは、ターンオンするために、閾値電圧V_tを超えるゲート－ソースバイアスが必要である。同様に、ゲート－ソースバイアスは、スイッチがオフになるためには、V_tより小さくなければならない。V_tは、「Ｎ型」ＭＯＳＦＥＴでは正であり、「Ｐ型」ＭＯＳＦＥＴでは、負である。図１ａ～１ｃのＲＦスイッチ１０には、Ｎ型ＭＯＳＦＥＴが、選択されている。Ｎ型ＭＯＳＦＥＴのソースは、最も低い電位のノードである。

【００１２】

再び図１ｃを参照すると、分路トランジスタＭ２（７）の過渡電圧の結果、入力信号サイクルの一部期間に、分路トランジスタＭ２（７）がターンオンすると、入力電力はグラウンドへ送られ、出力に対しては失われる。この電力の損失は、入力電力が増加（すなわち、増加した電力の入力信号）すると増加し、それにより第１のタイプの圧縮を引き起こす。ＲＦスイッチ１０の１ｄＢ圧縮ポイントは、ターンオフした分路トランジスタＭ２（７）がオフのままでいられなくなるポイントにおける入力の信号振動によって決定される。結局、入力の負振動は、グラウンドより低く、同様にＭ２ゲート電位より低くなる（したがってソース化する）。この差異がV_tに等しくなると、トランジスタＭ２（７）がターンオンし始め、圧縮が始まる。この第１のタイプの圧縮は、ＲＦスイッチの分路レッグにおけるノーマリオフ型ゲートのターンオン現象によって引き起こされる。ひとたび分路トランジスタＭ２（７）がターンオンすると、出力ノード３の電力は、もはや、線形にスイッチ入力部の電力に従うことはない。第２のタイプのＲＦスイッチ圧縮は、分路トランジスタＭ２（７）のソースおよびドレインが過度の電圧でブレークダウンするときに発生する。サブミクロンのシリコンオンインシュレータ（ＳＯＩ）デバイスに対して、この電圧は、供給電圧を直流約＋１Ｖ超えるだけの可能性がある。ブレークダウンでは、分路デバイスは大量の電力を導通し始め、それにより出力で利用できる電力が減少する。

【００１３】

図２に、先行技術による単極双投（ＳＰＤＴ）ＲＦスイッチ２０の簡易図を示す。図２に示すように、先行技術のＲＦスイッチ２０には、最低限、４つのＭＯＳＦＥＴトランジスタ２３、２４、２７および２８が含まれる。トランジスタ２３および２５は、「パス」または「スイッチング」トランジスタとして働き（図１ａ　１ｃのスイッチングＭＯＳＦＥＴトランジスタＭ１（５）と同様に）、これらの関連したそれぞれのＲＦ入力ノードを

二者択一的に共通のＲＦノード２５に結合するように構成されている。たとえば、作動している場合（すなわち、「オン」にスイッチされたとき）、スイッチングトランジスタ２３は、第１のＲＦ入力ノード２１への入力である第１の入力信号「$ＲＦ_1$」をＲＦ共通ノード２５へ結合する。同様に、作動している場合、スイッチングトランジスタ２４は、第２のＲＦ入力ノード２２への入力である第２のＲＦ入力信号「$ＲＦ_2$」を、ＲＦ共通ノード２５へ結合する。分路トランジスタ２７および２８は、作動している場合で、それらの関連したＲＦ入力ノードが、ＲＦ共通ノード２５と結合していないとき（すなわち、それらの関連する入力ノードへ接続されているスイッチングトランジスタ（２３または２４）がターンオフされているとき）、それぞれの関連したＲＦ入力ノードを二者択一的にグラウンドへ分路するために働く。

【００１４】

図２に示すように、先行技術のＲＦスイッチの動作を制御するために、２つの制御電圧を用いている。「ＳＷ」およびその逆の「ＳＷ＿」の名称がついた制御電圧は、トランジスタ２３、２４、２７および２８の動作を制御する。制御電圧は、選択したトランジスタの対を、二者択一的に作動（ターンオン）または不作動（ターンオフ）にするように調整されている。たとえば、図２に示すように、ＳＷがオン（いくつかの実施形態では、これは、制御電圧を、論理的に「高い」電圧レベル、たとえば、「＋Ｖｄｄ」に設定することによって決定される）のとき、スイッチングトランジスタ２３が作動となり、その関連する分路トランジスタ２８も作動する。しかしながら、ＳＷの逆のＳＷ＿は、第２のスイッチングトランジスタ２４の動作とその関連する分路トランジスタ２７を制御し、また、制御信号ＳＷ＿は、ＳＷがオン（いくつかの実施形態では、これは、ＳＷ＿を－Ｖｄｄに設定することによって決定する）の間、オフなので、これら２つのトランジスタは、この同じ期間には不作動またはターンオフされている。この状態（ＳＷがオンでＳＷ＿がオフ）では、$ＲＦ_1$入力信号は、（作動しているスイッチングトランジスタ２３を介して）ＲＦ共通ポート２５に結合される。第２のスイッチングトランジスタ２４はターンオフされているので、$ＲＦ_2$入力信号は、ＲＦ共通ポート２５からはブロックされる。その上、$ＲＦ_2$入力信号は、作動している分路トランジスタ２８を介してグラウンドへ分路されるので、ＲＦ共通ポート２５からさらに分離される。トランジスタ設計分野の当業者は容易に理解されるであろうように、ＳＷ制御信号が「オフ」（およびＳＷ＿が「オン」）のときには、$ＲＦ_2$信号は、同じような方法で、ＲＦ共通ポート２５に結合される（そして$ＲＦ_1$信号はブロックさレッグラウンドへ分路される）。

【００１５】

様々な性能上の結果を伴って、図２のＳＰＤＦ・ＲＦスイッチ２０などのＲＦスイッチが、バルク相補型金属酸化膜半導体（ＣＭＯＳ）およびガリウムヒ素（ＧａＡｓ）技術を始めとする、異なる素子技術においてこれまで実現されてきた。実は、ほとんどの高性能高周波スイッチは、ＧａＡｓ技術を使用している。先行技術によるＲＦスイッチの実現において、上記のＲＦスイッチ性能特性を改善しようと試みているが、それらの結果は種々雑多であり、集積回路の複雑さと歩留まりの程度も様々である。たとえば、バルクＣＭＯＳ・ＲＦスイッチは、不利なことに、高い挿入損失性能特性、低い圧縮性能特性および不十分な線形性能特性を示す。対照的に、ＧａＡｓ材料の半絶縁性のために、寄生基板抵抗は著しく減少でき、それにより、スイッチ挿入損失を減少できる。同様に、半絶縁ＧａＡｓ基板は、スイッチ分離を改善する。

【００１６】

ＧａＡｓＲＦスイッチの実現により、性能特性の向上がもたらされるが、この技術にはいくつかの欠点がある。たとえば、ＧａＡｓ技術では、正常に機能する集積回路の歩留まりが比較的低い。ＧａＡｓＲＦスイッチは、設計および製造が比較的高価になりがちである。加えて、ＧａＡｓスイッチは、上記のように、挿入損失特性を改善するが、ＧａＡｓ基板に存在する遅い表面準位のために、周波数制限が低くなる可能性がある。また、この技術は高いレベルの集積化に向いていないので、ＲＦスイッチに関連するデジタル制御回路をスイッチから「オフチップ」で実現する必要がある。スイッチに関連する低電力回路

は、集積するのが困難だと分かっている。これは、全体的なシステムコストまたは製造コスト、サイズおよび複雑さを増加させ、同様に、システムのスループット速度を減少させるので不利である。

【発明の開示】

【発明が解決しようとする課題】

【００１７】

したがって、改善した性能特性を有する、ＲＦスイッチおよびＲＦ信号をスイッチングする方法を提供することが望ましい。特に、挿入損失、分離および圧縮が改善したＲＦスイッチを提供することが望ましい。このようなＲＦスイッチは、容易に設計製造ができ、比較的安価に製造され、高いレベルの集積に向いており、低周波から高周波まで適用できるのが望ましい。電力制御回路は、スイッチ機能とともに簡単にオンチップに集積できるようにすべきである。このような集積は、これまで、Ｓｉ基板およびＧａＡｓ基板を用いて実現するのが困難だった。本発明は、このようなＲＦスイッチおよびＲＦ信号のスイッチング方法を提供する。

【課題を解決するための手段】

【００１８】

発明の概要

新規なＲＦスイッチ回路およびＲＦ信号のスイッチング方法について説明する。ＲＦスイッチは無線用途に使用可能で、シリコンオンインシュレータ技術で製造できる。一実施形態において、ＲＦスイッチは、極薄シリコン（「ＵＴＳｉ」）基板上に製造する。一実施形態において、ＲＦスイッチには、つぎのものが含まれる。すなわち、ＲＦ信号を受信するための入力部と、ＲＦ信号を受信するための入力部およびＲＦ共通ポートに接続され、スイッチング電圧（ＳＷ）によって制御される第１のスイッチングトランジスタ・グループと、第１のスイッチングトランジスタ・グループおよびＲＦ共通ポートに接続され、スイッチング電圧（ＳＷ＿）によって制御される第２のスイッチングトランジスタ・グループとが含まれ、またＳＷ＿はＳＷの逆であり、第１のスイッチングトランジスタ・グループがオンのとき、第２のスイッチングトランジスタ・グループがオフになる。スイッチングトランジスタ・グループは、作動しているとき、それぞれのＲＦ入力信号を、ＲＦ共通ポートへ二者択一的に接続する。この実施形態において、ＲＦスイッチにはまた、スイッチングトランジスタ・グループに結合され、スイッチング電圧ＳＷおよびＳＷ＿によって制御される分路トランジスタグループが含まれる。分路トランジスタグループは、作動しているとき、それらの関連するＲＦ入力ノードを二者択一的にグラウンドに分路するように働き、それによってＲＦスイッチ分離を改善する。

【００１９】

スイッチングおよび分路トランジスタグループには、積層または直列構成でともに接続された１つまたは複数のＭＯＳＦＥＴトランジスタが含まれる。各トランジスタグループ内では、積層トランジスタのゲートは、通常、スイッチング電圧（ＳＷまたはＳＷ＿）によって制御され、このスイッチング電圧は、それぞれのゲート抵抗器を介して各トランジスタゲートに結合される。トランジスタグループ・デバイスの積層およびゲート抵抗器によって、スイッチの圧縮ポイントが増加する。ＭＯＳＦＥＴのゲート抵抗器およびゲート容量によって形成されるＲＣ時定数は、ＲＦ信号の周期よりもずっと長くなるように設計され、ＲＦ電圧が、直列接続デバイス全体で等しく共用されるようにする。この構成によって、ＲＦスイッチの１ｄＢ圧縮ポイントが増加する。

【００２０】

完全に集積化されたＲＦスイッチについて説明する。このＲＦスイッチには、デジタルスイッチ制御論理回路と、本発明のＲＦスイッチとともに集積された負の電源電圧発生器とが含まれる。一実施形態では、完全に集積化されたＲＦスイッチによって、先行技術のＲＦスイッチには存在しない、いくつかの機能が提供される。たとえば、一実施形態では、完全に集積化されたＲＦスイッチには、電荷ポンプ回路にクロック入力信号を供給する内蔵式発振器と、他のＲＦスイッチ回路が必要とする負の電源電圧を発生する集積された

電荷ポンプ回路と、ＲＦスイッチトランジスタを制御する制御信号を発生するＣＭＯＳ論理回路と、スイッチデバイスの信頼性を増加する、レベルシフト回路および低電流分圧器回路と、ＲＦ信号エネルギを、電荷ポンプ回路およびデジタル制御論理回路から分離するＲＦバッファ回路とが含まれる。電荷ポンプ回路、レベルシフト回路、分圧器およびＲＦバッファ回路のいくつかの実施形態について説明する。本発明のＲＦスイッチによって、挿入損失、スイッチ分離およびスイッチ圧縮が改善される。さらに、本発明のＲＦスイッチによって利用可能となる、より高いレベルの集積のおかげで、本発明を用いることにより、ＲＦシステムの設計および製造コストは減少し、信頼性が高まる。

【００２１】

なお、以下の図面の簡単な説明において、様々な図面の同じ参照符号は、同じ構成要素を示す。

【発明を実施するための最良の形態】

【００２２】

発明の詳細な説明

この明細書を通して、明らかにする好適な実施形態および実施例は、本発明に対する限定というよりも、例示的なものとして考えるべきである。

【００２３】

本発明のＲＦスイッチ

本発明は、新規なＲＦスイッチ設計およびＲＦ回路をスイッチングするための方法である。本発明のＲＦスイッチ３０の第１の例示的な実施形態を、図３に示す。図３に示すように、一実施形態において、本発明のＲＦスイッチ３０には、ＭＯＳＦＥＴトランジスタの４つのクラスタまたは「グループ」が含まれる。これらを、トランジスタグループ３３、３４、３７および３８として図３に示す。２つのトランジスタグループには、「パス」または「スイッチング」トランジスタグループ３３および３４が含まれ、２つのトランジスタグループには、分路トランジスタグループ３７および３８が含まれる。各トランジスタグループには、直列構成に配置された１つまたは複数のＭＯＳＦＥＴトランジスタが含まれる。たとえば、図３に示す実施形態では、スイッチンググループ３３には、３つのスイッチングトランジスタM_{33A}、M_{33B}およびM_{33C}が含まれる。同様に、スイッチンググループ３４には、３つのスイッチングトランジスタM_{34A}、M_{34B}およびM_{34C}が含まれる。分路グループ３７には、３つのトランジスタM_{37A}、M_{37B}およびM_{37C}が含まれる。同様に、分路グループ３８には、３つのトランジスタM_{38A}、M_{38B}およびM_{38C}が含まれる。トランジスタグループ３３、３４、３７および３８は、３つのＭＯＳＦＥＴトランジスタを含むものとして、図３には示してあるが、ＲＦスイッチ設計分野の当業者は、本発明の範囲または趣旨から逸脱することなく、代替のグループ構成が使用できることを、理解されるであろう。たとえば、以下により詳細に説明するように、本発明の範囲から逸脱することなく、任意の都合のよい数のトランジスタを使用して、図３に示すグループを実現することができる。

【００２４】

本発明のＲＦスイッチの一実施形態において、ＭＯＳＦＥＴトランジスタ（たとえば、トランジスタM_{37A}、M_{37B}およびM_{37C}）は、完全に絶縁された基板シリコンオンインシュレータ（ＳＯＩ）技術を用いて実現する。特に、以下により詳細に説明するように、本発明のＲＦスイッチのＭＯＳＦＥＴトランジスタは、「極薄シリコン（Ｕｌｔｒａ－Ｔｈｉｎ－Ｓｉｌｉｃｏｎ）（ＵＴＳｉ）」（本明細書においては、また「極薄シリコンオンサファイア（ｕｌｔｒａｔｈｉｎ　ｓｉｌｉｃｏｎ－ｏｎ－ｓａｐｐｈｉｒｅ）」と呼ぶ）技術を用いて実現する。ＵＴＳｉ製造方法に従い、本発明のＲＦスイッチを実現するために使用するトランジスタは、絶縁サファイアウエハにおけるシリコンの極薄層に形成する。完全な絶縁性のサファイア基板は、非絶縁基板および半絶縁基板に関連する、有害な、基板の結合効果を減少させることにより、本発明によるＲＦスイッチの性能特性を向上させる。たとえば、挿入損失の改善は、トランジスタのオン抵抗を下げ、寄生基板抵抗を減少させることにより実現する。さらに、スイッチ分離は、ＵＴＳｉ技術によっ

て提供される、完全な絶縁基板を用いて改善する。シリコンオンサファイア技術の完全な絶縁性のおかげで、バルクＣＭＯＳおよび他の、従来の集積回路製造技術と比較して、ＲＦスイッチ３０のノード間の寄生キャパシタンスは、著しく減少する。その結果、本発明のＲＦスイッチでは、先行技術のＲＦスイッチ設計と比較して、スイッチ分離が改善される。

【００２５】

図３に示すように、図２に関連して上記に説明したスイッチと同様に、トランジスタグループは、２つの制御信号ＳＷおよびその逆のＳＷ＿によって制御される。制御信号は、関連するそれぞれのゲート抵抗器を介して、それぞれのトランジスタのゲートに結合される。たとえば、制御信号ＳＷは、スイッチングトランジスタ・グループ３３における３つのトランジスタ（M_{33A}、M_{33B}およびM_{33C}）の動作を、３つのそれぞれに関連するゲート抵抗器（R_{33A}、R_{33B}およびR_{33C}）を介して制御する。制御信号ＳＷは、入力ノード３３’へ入力され、スイッチングトランジスタ・グループ３３を制御する。ＳＷはまた、入力ノード３８’へ入力され、分路トランジスタグループ３８を制御する。同様に、ＳＷの逆のＳＷ＿は、入力ノード３４’を介して、スイッチングトランジスタ・グループ３１を制御する。ＳＷ＿はまた、入力ノード３７’へ入力され、分路トランジスタグループ３７を制御する。

【００２６】

一実施形態において、トランジスタグループの抵抗器には、約３０ＫΩの抵抗器が含まれるが、本発明の趣旨または範囲から逸脱せずに、代替の抵抗値を用いることができる。さらに、本発明のいくつかの実施形態において、ゲート抵抗器には、比較的高い抵抗値を有する任意の抵抗素子が含まれる。たとえば、一実施形態では、逆バイアスダイオードを用いて、ゲート抵抗器を実現してもよい。以下により詳細に説明するように、ゲート抵抗器は、直列接続トランジスタ全体の実効降伏電圧を増加するのに役立つ。

【００２７】

制御信号は、トランジスタグループ３３、３４、３７および３８の作動および不作動について制御するように機能し、ＲＦスイッチ３０は、一般に、図２におけるスイッチのアナログトランジスタを制御するのと同様の方法で、ＲＦ信号を通過させるかまたはブロックするように機能する。特に、スイッチングトランジスタ・グループ３３および３４は、パストランジスタまたはスイッチングトランジスタとして機能し、二者択一的に、それぞれの関連するＲＦ入力ノードを共通のＲＦノード３５に結合するように構成されている。たとえば、スイッチングトランジスタ・グループ３３は、作動すると、第１のＲＦ入力ノード３１への入力である第１のＲＦ入力信号「RF_1」を、ＲＦ共通ノード３５に結合する。同様に、スイッチングトランジスタ・グループ３４は、作動すると、第２のＲＦ入力ノード３２への入力である第２のＲＦ入力信号「RF_2」を、ＲＦ共通ノード３５へ結合する。分路トランジスタグループ３７および３８は、作動すると、それらの関連するＲＦ入力ノードが、ＲＦ共通ノード３５と結合していないとき（すなわち、関連する入力ノードに接続されているスイッチングトランジスタ・グループ（３３または３４）がターンオフされているとき）、それぞれの関連するＲＦ入力ノードを、二者択一的にグラウンドへ分路するように働く。

【００２８】

制御電圧は、トランジスタグループの選択した組を、二者択一的に作動または不作動にするために接続されている。たとえば、図３に示すように、ＳＷがオンのとき（いくつかの実施形態では、これは、制御電圧ＳＷが、論理的に「高い」電圧レベルに設定されるときに決定される）、スイッチングトランジスタ・グループ３３は作動し（すなわち、グループ３３の全てのトランジスタがターンオンする）、その関連する分路トランジスタグループ３８もまた作動する（すなわち、グループ３８の全てのトランジスタが、ターンオンする）。しかしながら、図２におけるスイッチの動作と同様に、ＳＷの逆のＳＷ＿が、第２のスイッチングトランジスタ・グループ３４およびその関連する分路トランジスタグループ３７を制御するので、これら２つのトランジスタグループは、この期間には不作動に

なる（すなわち、グループ３４および３７のトランジスタは全て、ターンオフする）。したがって、ＳＷがオンのとき、$ＲＦ_1$入力信号は、ＲＦ共通ノード３５に結合される。$ＲＦ_2$入力信号は、スイッチングトランジスタ・グループ３４がオフなので、ＲＦ共通ノード３５からブロックされる。$ＲＦ_2$入力信号は、作動された分路トランジスタグループ３８を介してグラウンドに分路されるので、ＲＦ共通ノード３５からさらに分離される。ＲＦスイッチ設計分野の当業者は理解されるであろうように、$ＲＦ_2$信号は、ＳＷ制御信号がオフ（そしてＳＷ_制御信号がオン）のとき、同様の方法で、ＲＦ共通ノード３５に結合される（そして$ＲＦ_1$信号はブロックさレッグラウンドへ分路される）。

【００２９】

図３における本発明のＲＦスイッチ３０に示すように、ＭＯＳＦＥＴトランジスタを積層し、ゲート抵抗器を使用する目的の１つは、直列接続トランジスタ全体の降伏電圧を高くすることである。ゲート抵抗器およびＭＯＳＦＥＴのゲート容量によって形成されるＲＣ時定数は、ＲＦ信号の周期よりもずっと長くなるように設計する。それゆえに、ＲＦエネルギは、ゲート抵抗器を介して消散することがほとんどない。この配置により、ＲＦ電圧は、効果的に、直列接続トランジスタ全体で等しく共用される。正味効果として、直列接続デバイス全体の降伏電圧が、個別ＦＥＴの降伏電圧のｎ倍に増加する。この場合、ｎは、直列に接続されるトランジスタの数である。この構成により、本発明のＲＦスイッチ３０の１ｄＢ圧縮ポイントが増加する。

【００３０】

スイッチ性能を改善するために、ＲＣ時定数は、ＲＦ信号周期に対して大きなサイズにしなければならない。このことは、主として、ゲートトランジスタ（ゲート抵抗器）を実現するのに使用できるＲの最小値に制約を課すことになる。上記のように、本発明の一実施形態では、Ｒの典型的な値は３０ｋΩであるが、本発明の範囲から逸脱することなく、他の抵抗値を用いることもできる。ＭＯＳＦＥＴゲート入力部は、直流電流を引き寄せないので、この抵抗全体のＩＲ降下のために、デバイスにおけるバイアスが変更されることはない。

【００３１】

有利なことに、本発明のＲＦスイッチ３０は、増大した電力レベルの入力信号に対応できる。トランジスタグループ（３３、３４、３７および３８）を含むＭＯＳＦＥＴトランジスタの直列配置のおかげで、増大した電力信号を、スイッチ動作に有害な影響を与えることなく、ＲＦ入力ノード（すなわち、入力ノード３１および３２）に供給することができる。トランジスタ設計分野の当業者は、より大きな入力電力レベルには、トランジスタグループごとにトランジスタの数を増やすこと、またはトランジスタの物理的構成を変えることによって対応できることを、理解されるであろう。たとえば、一実施形態において、トランジスタの寸法は、約０．５×２，１００μｍである。しかしながら、本発明の範囲または趣旨から逸脱することなく、代替の構成を用いることができる。

【００３２】

シリコンオンインシュレータ（ＳＯＩ）技術

図３におけるＲＦスイッチの説明において上記で言及したように、ＳＯＩ技術は、絶縁基板の完全な絶縁性のために、ＲＦスイッチの実現においては、魅力がある。周知のように、ＳＯＩは、高性能マイクロエレクトロニクスデバイスの実現、主に、放射線耐性および高速動作を必要とする用途に使用されてきた。ＳＯＩ技術には、たとえば、ＳＩＭＯＸ、絶縁層に接合された薄いシリコン層を有する接合ウエハおよびシリコンオンサファイアが含まれる。上記の望ましいスイッチ性能特性を達成するために、一実施形態において、本発明のＲＦスイッチは、サファイア基板上に製造される。

【００３３】

絶縁基板上にデバイスを製造するには、絶縁基板上にシリコンＣＭＯＳデバイスを形成するための効果的な方法を用いる必要がある。サファイアなどの絶縁性支持基板にエピタキシャル堆積した、シリコンなどの単結晶半導体層を含む複合基板を用いることの利点がよく認識され、これらの利点は、サファイア（$Ａ１_2Ｏ_3$）、スピネルまたは他の周知の

高絶縁材料などの絶縁材料を基板として用い、デバイス間リーク電流の導電経路が基板を必ず通過するようにすることによって、実現できる。

【００３４】

「理想的」なシリコンオンサファイア・ウエハは、その中に能動素子を製造できる十分な厚さを有した、完全単結晶で欠陥のないシリコン層を含む、と定義できる。このシリコン層は、絶縁基板に隣接し、シリコン－絶縁体界面における結晶格子の乱れは最小限であろう。この「理想的」なシリコンオンサファイア・ウエハを製造しようとする初期の試みは、多くの際立った問題のために挫折した。これらの問題は、（１）最初のエピタキシャルシリコン堆積に使用する高温、およびその後、シリコン層をアニールして、その中の欠陥を減少するために使用する高温の結果として、汚染物、特にｐ型ドーパントのアルミニウムがかなりエピタキシャル堆積シリコン層に侵入するすること、ならびに（２）様々な打込み、アニールおよび／または再成長の方法を通して問題となる高温を避けたときの、エピタキシャルシリコン層の不十分な結晶特性として要約できる。

【００３５】

要求の厳しいデバイス用途に適した高品質のシリコン薄膜を、サファイア基板上に製造できることが分かっているが、このときの方法には、サファイア基板上におけるシリコン層のエピタキシャル堆積、シリコン層に埋込みアモルファス領域を形成するための低温イオン打込みおよび約９５０℃未満の温度における複合物のアニールが含まれる。

【００３６】

このようなシリコンオンサファイア・デバイスを製造する例および方法が、以下の明細書に記載されている。それらは、米国特許第５，４１６，０４３号明細書（「超薄膜シリコンオンサファイアウエハ上に製造される最小電荷ＦＥＴ」（Ｍｉｎｉｍｕｍ ｃｈａｒｇｅ ＦＥＴ ｆａｂｒｉｃａｔｅｄ ｏｎ ａｎ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｗａｆｅｒ））、米国特許第５，４９２，８５７号明細書（「単一の極薄膜シリコンオンサファイアチップ上の高周波ワイヤレス通信システム」（Ｈｉｇｈ ｆｒｅｑｕｅｎｃｙ ｗｉｒｅｌｅｓｓ ｃｏｍｍｕｎｉｃａｔｉｏｎ ｓｙｓｔｅｍ ｏｎ ａ ｓｉｎｇｌｅ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｃｈｉｐ））、米国特許第５，５７２，０４０号明細書（「単一の極薄膜シリコンオンサファイアチップ上の高周波ワイヤレス通信システム」（Ｈｉｇｈ－ｆｒｅｑｕｅｎｃｙ ｗｉｒｅｌｅｓｓ ｃｏｍｍｕｎｉｃａｔｉｏｎ ｓｙｓｔｅｍ ｏｎ ａ ｓｉｎｇｌｅ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｃｈｉｐ））、米国特許第５，５９６，２０５号明細書（「単一の極薄膜シリコンオンサファイアチップ上の高周波ワイヤレス通信システム」（Ｈｉｇｈ－ｆｒｅｑｕｅｎｃｙ ｗｉｒｅｌｅｓｓ ｃｏｍｍｕｎｉｃａｔｉｏｎ ｓｙｓｔｅｍ ｏｎ ａ ｓｉｎｇｌｅ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｃｈｉｐ））、米国特許第５，６００，１６９号明細書（「超薄膜シリコンオンサファイアウエハ上に製造される最小電荷ＦＥＴ」（Ｍｉｎｉｍｕｍ ｃｈａｒｇｃ ＦＥＴ ｆａｂｒｉｃａｔｃｄ ｏｎ ａｎ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｗａｆｅｒ））、米国特許第５，６６３，５７０号明細書（「単一の極薄膜シリコンオンサファイアチップ上の高周波ワイヤレス通信システム」（Ｈｉｇｈ－ｆｒｅｑｕｅｎｃｙ ｗｉｒｅｌｅｓｓ ｃｏｍｍｕｎｉｃａｔｉｏｎ ｓｙｓｔｅｍ ｏｎ ａ ｓｉｎｇｌｅ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｃｈｉｐ））、米国特許第５，８６１，３３６号明細書（「単一の極薄膜シリコンオンサファイアチップ上の高周波ワイヤレス通信システム」（Ｈｉｇｈ－ｆｒｅｑｕｅｎｃｙ ｗｉｒｅｌｅｓｓ ｃｏｍｍｕｎｉｃａｔｉｏｎ ｓｙｓｔｅｍ ｏｎ ａ ｓｉｎｇｌｅ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｃｈｉｐ））、米国特許第５，８６３，８２３号明細書（「シリコンオンインシュレータにおける自己整合されたエッジ制御」（Ｓｅｌｆ－ａｌｉｇｎｅｄ ｅｄｇｅ ｃｏｎｔｒｏｌ ｉｎ ｓｉｌｉｃｏｎ ｏｎ ｉｎｓｕｌａｔｏｒ））、米国特許第５，８８３，３９６号明細書（「単 の極薄膜シリコンオンサファイアチップ上の高周波ワイヤレス通信システム」（Ｈｉｇｈ－ｆｒｅｑｕ

ｅｎｃｙ ｗｉｒｅｌｅｓｓ ｃｏｍｍｕｎｉｃａｔｉｏｎ ｓｙｓｔｅｍ ｏｎ ａ ｓｉｎｇｌｅ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｃｈｉｐ））、米国特許第５，８９５，９５７号明細書（「超薄膜シリコンオンサファイアウエハ上に製造される最小電荷ＦＥＴ」（Ｍｉｎｉｍｕｍ ｃｈａｒｇｅ ＦＥＴ ｆａｂｒｉｃａｔｅｄ ｏｎ ａｎ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｗａｆｅｒ））、米国特許第５，９２０，２３３号明細書（「擬似側波帯を減少するためのサンプリング回路を含む位相同期ループ」Ｐｈａｓｅ ｌｏｃｋｅｄ ｌｏｏｐ ｉｎｃｌｕｄｉｎｇ ａ ｓａｍｐｌｉｎｇ ｃｉｒｃｕｉｔ ｆｏｒ ｒｅｄｕｃｉｎｇ ｓｐｕｒｉｏｕｓ ｓｉｄｅ ｂａｎｄ）、米国特許第５，９３０，６３８号明細書（「極薄シリコンオンインシュレータ上に低寄生抵抗を製造する方法」（Ｍｅｔｈｏｄ ｏｆ ｍａｋｉｎｇ ａ ｌｏｗ ｐａｒａｓｔｉｃ ｒｅｓｉｓｔｏｒ ｏｎ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｉｎｓｕｌａｔｏｒ））、米国特許第５，９７３，３６３号明細書（「極薄シリコンオンインシュレータ上の、短縮されたＰチャネル長を有するＣＭＯＳ回路」（ＣＭＯＳ ｃｉｒｃｕｉｔｒｙ ｗｉｔｈ ｓｈｏｒｔｅｎｅｄ Ｐ－ｃｈａｎｎｅｌ ｌｅｎｇｔｈ ｏｎ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｉｎｓｕｌａｔｏｒ））、米国特許第５，９７３，３８２号明細書（「絶縁体上における極薄半導体上のキャパシタ」（Ｃａｐａｃｉｔｏｒ ｏｎ ｕｌｔｒａｔｈｉｎ ｓｅｍｉｃｏｎｄｕｃｔｏｒ ｏｎ ｉｎｓｕｌａｔｏｒ））および米国特許第６，０５７，５５５号明細書（「超薄膜シリコンオンサファイアウエハ上に製造される最小電荷ＦＥＴ」（Ｈｉｇｈ－ｆｒｅｑｕｅｎｃｙ ｗｉｒｅｌｅｓｓ ｃｏｍｍｕｎｉｃａｔｉｏｎ ｓｙｓｔｅｍ ｏｎ ａ ｓｉｎｇｌｅ ｕｌｔｒａｔｈｉｎ ｓｉｌｉｃｏｎ ｏｎ ｓａｐｐｈｉｒｅ ｃｈｉｐ））である。これらの参照特許は全て、極薄シリコンオンサファイア集積回路設計および製造に関するその教示全体において、本明細書に援用している。

【００３７】

上記で参照した特許に記載された方法を用いて、電子デバイスを、絶縁合成サファイアウエハ上のシリコン極薄層に形成することができる。シリコン層の厚さは、典型的には、１５０ｎｍ未満である。このような「極薄」シリコン層により、絶縁サファイア基板の利点が最大化され、単一集積回路上に多数の機能を集積することが可能となる。厚いシリコンでは必要とされる従来のトランジスタ分離ウェルが必要でなくなり、トランジスタ処理が簡略化され、回路密度が増大する。これらの、上記で参照した方法およびデバイスを、以前の厚いシリコン実施形態と区別するために、本明細書では、これらを一括して「極薄シリコンオンサファイア」と呼ぶ。

【００３８】

本発明のいくつかの好適な実施形態では、ＭＯＳトランジスタは、米国特許第５，４１６，０４３号、第５，４９２，８５７号、第５，５７２，０４０号、第５，５９６，２０５号、第５，６００，１６９号、第５，６６３，５７０号、第５，８６１，３３６号、第５，８６３，８２３号、第５，８８３，３９６号、第５，８９５，９５７号、第５，９２０，２３３号、第５，９３０，６３８号、第５，９７３，３６３号、第５，９７３，３８２号および第６，０５７，５５５号の各明細書に開示された方法により、極薄シリコンオンサファイアに形成する。しかしながら、本発明の趣旨または範囲から逸脱することなしに、極薄シリコンオンサファイア集積回路を製造する他の周知の方法を用いることができる。

【００３９】

これらの特許に記載され、特許請求されているように、要求の厳しいデバイス用途に適した高品質のシリコン薄膜が、絶縁基板上へのシリコン層のエピタキシャル堆積、シリコン層に埋込みアモルファスを形成するための低温イオン打込みおよび約９５０℃未満の温度での複合物のアニールを含む方法により、絶縁基板上に製造することができる。約９５０℃を超える温度にシリコン層をさらすどのような処理も、酸化周囲環境において実施する。トランジスタを形成するシリコン薄膜には、意図的ではなくドープされた領域に、約

$5\times10^{11}\ cm^{-2}$未満の電気的に活性状態の面積密度がある。

【００４０】

上記で言及したように、ＵＴＳｉ基板は、ＲＦ用途には特に望ましい。なぜなら、完全な絶縁基板は、従来の基板（すなわち、完全には絶縁性でない）に関連した基板結合の有害な影響を減少するからである。結果として、一実施形態では、図３のＲＦスイッチ３０は、ＵＴＳｉ基板上に製造する。

【００４１】

ＲＦスイッチ設計トレードオフ

図３に関連して上記で説明した、本発明のＲＦスイッチ３０を設計し実現するときに、いくつかの設計パラメータおよびトレードオフを考慮すべきである。本発明のＲＦスイッチは、所望のシステム設計要求およびＲＦスイッチ性能目標を満たすか超えるように仕立てることができる。ＲＦスイッチ設計に影響を与える設計トレードオフおよび考慮すべきことについて、ここで説明する。

【００４２】

図３に関連して上記で説明したように、ＲＦスイッチ３０は、「Ｎ型」でも「Ｐ型」でもよいが、ＭＯＳＦＥＴトランジスタを用いて実現する。しかしながら、ＣＭＯＳ技術においてＲＦスイッチを実現するには、Ｎチャネルトランジスタが好ましい。Ｎチャネルトランジスタが好ましいのは、一定のトランジスタサイズに対して、Ｎチャネルトランジスタの「オン」抵抗が、Ｐチャネルトランジスタの場合よりも、ずっと小さいからである。これは、正孔に対して電子の、シリコンにおける移動度が高いことによる。制御電圧は、「オン」トランジスタのオン抵抗が確実に減少するように選択する。制御電圧はまた、「オフ」トランジスタが、不作動にされたとき、確実にオフとどまるように選択する。

【００４３】

トランジスタ設計分野においては周知のように、ＮチャネルＭＯＳトランジスタにおいては、「オン」抵抗は、トランジスタゲートに印加する電圧とトランジスタソースに印加する電圧間の差異に反比例する。この電圧は、通常、「Ｖｇｓ」（ゲート　ソース電圧）と呼ばれる。容易に気づくことだが、入力ポート（たとえば、図３における第１のＲＦ入力ノード３１）において、したがって、ＲＦ共通ポート３５においてＲＦ信号（Ｖｓ）の大きさが増すにつれて、オントランジスタのＶｇｓが減少する（たとえば、ＲＦ１信号の大きさが増加するにつれて、スイッチングトランジスタ・グループ３３におけるトランジスタ$M33_A$のＶｇｓが減少する）。このために、ゲート制御電圧（たとえば、入力ノード３３’のＳＷ）を可能な限り正にすべきだというになる。しかし残念ながら、信頼性の懸念から、ゲート制御電圧を正にできる程度が制限される。

【００４４】

同様の懸念が「オフ」トランジスタに対しても存在する。典型的なＲＦスイッチの適用では、ＲＦ入力信号（たとえば、ＲＦ１入力信号）が一般にゼロ基準電圧をめぐって振動することに注目することは大切である。オフトランジスタ（たとえば、シャントトランジスタグループ３７のトランジスタ）は、ＲＦ入力信号の正および負の電圧偏移の間、不作動またはターンオフのままにとどまらなくてはならない。このことから、オフトランジスタのゲート制御電圧（たとえば、ＳＷ＿制御電圧信号）をできる限り負にすべきだということになる。再び、信頼性の懸念から、ゲート制御電圧を負にできる程度が制限される。

【００４５】

ＣＭＯＳスイッチにとって、オフトランジスタの設計によって、また、スイッチの１ｄＢ圧縮ポイントが制限される。トランジスタ設計分野においては周知のように、ＭＯＳトランジスタでは、そのソースとドレイン間に基本的な降伏電圧がある。デバイス両端の電位がこの降伏電圧を超えると、トランジスタをオフ状態に維持しようとしているゲート電位が存在するときでも、ソースとドレイン間に高電流が流れる。スイッチにおける圧縮の改善は、トランジスタの降伏電圧を増加することによっと、達成することができる。高降伏電圧を有するＭＯＳトランジスタを製造する方法の１つは、ゲート長を増加することである。残念なことに、ゲート長の増加により、デバイスのチャネル抵抗が不都合にも増加

し、それにより、デバイスの挿入損失が増加する。チャネル抵抗は、デバイスの幅を広くすることによって減少できるが、これはまた、スイッチ分離を低下させる。したがって、ＭＯＳスイッチに、トレードオフが存在する。

【００４６】

図３における本発明のＲＦスイッチ３０に関連して上記に説明したように、トランジスタを直列構成に積層して、スイッチの１ｄＢ圧縮ポイントを改善する。比較的高い値のゲート抵抗器と、トランジスタグループにおけるトランジスタの積層構成との組み合わせにより、直列接続トランジスタ全体の実効降伏電圧を増加する。スイッチ素子の設計および製造においては、ＲＣ時定数（ゲート抵抗器の抵抗値およびＭＯＳＦＥＴのゲート容量によって決定される）が、ＲＦスイッチ３０が処理するＲＦ信号の周期よりもずっと長くなるようにする。上記のように、積層構成および比較的高抵抗のゲート抵抗器の正味効果として、直列接続トランジスタ全体の降伏電圧が、個別トランジスタにおける降伏電圧のｎ倍の率で増加する（ここで、ｎは、トランジスタグループにおいて、直列に接続したトランジスタの数に等しい）。

【００４７】

設計上さらに考慮すべきことは、従来のバルクＣＭＯＳトランジスタにおいて使用されている「ボディタイ」に関する。トランジスタ設計分野においては周知のように、ボディタイは、デバイスをウェルまたは基板のどちらかに結合する。ウェル－基板接合部は、常に逆バイアスをかけられたままにしなければならない。ソース－ボディおよびドレイン－ボディ接合部は、常に逆バイアスをかけられたままにしなければならない。一般に、バルクＣＭＯＳ設計において、ウェル（Ｎウェル技術の）は、回路に印加される最大の正の電位に結合される。基板（Ｐウェル技術の）は、回路に印加される最大の負の電位に結合される。ＲＦ入力信号は、グラウンドの上下を対称的に振動するので、ＣＭＯＳスイッチ設計は、挿入損失、分離および１ｄＢ圧縮ポイントについて、不十分な性能を示す。これらおよび上記の理由で、本発明のＲＦスイッチ３０は、絶縁基板上に実現するのが好ましい。

【００４８】

本発明のＲＦスイッチを絶縁基板上に実現することにより、スイッチ分離の改善および挿入損失の減少などいくつかの利点が提供される。ＵＴＳｉ技術を用いて本発明のＲＦスイッチを実現することにより、さらなる利点が得られる。たとえば、先行技術のＲＦスイッチをＧａＡｓに実現することと比較して、ＵＴＳｉを用いることにより、集積回路歩留まりの改善、製造コストの減少および集積レベルの増加が達成される。集積回路設計分野において周知のように、ＧａＡｓは、高レベルの集積化には向いていない。したがって、ＲＦスイッチの動作および機能に関連したデジタル制御回路および他の回路（負電圧電力供給発生器回路、レベルシフト回路、低電流分圧器回路およびＲＦバッファ回路など）は、オフチップで実現しなければならないことがしばしばある（すなわち、これらの機能は、ＲＦスイッチと簡単には集積できない）。これは、コストの増加および先行技術により実現したＲＦスイッチの性能低下へとつながる。

【００４９】

対照的に、本ＲＦスイッチの発明に従い、ＵＴＳｉ技術を用いて、ＲＦスイッチの正常な動作および機能のために必要な回路を、スイッチ自体と同じ集積回路に一緒に実現できる。たとえば、以下により詳細に説明するように、ＵＴＳｉ技術でＲＦスイッチを実現することにより、ＲＦスイッチは、負電圧発生器およびＲＦスイッチの動作を制御するのに必要なＣＭＯＳ制御論理回路とともに同じ集積回路に集積できる。スイッチの動作を制御するのに必要な制御線の減少のおかげで、ＲＦスイッチの複雑さもまた減少する。有利なことに、ＲＦスイッチ制御論理回路は、低電圧ＣＭＯＳトランジスタを用いて実現できる。さらに、高電力ＲＦスイッチ実現のためであっても、比較的低電力の外部電源を用いて、本発明のＲＦスイッチに電力を供給することができる。この特徴は、先行技術によるＧａＡｓの実現に比較して有利である。ＧａＡｓの場合には、比較的高電力の外部電源ならびに正および負両方の電力供給を実現するのに必要な電力発生回路を使用することが必要

だからである。たとえば、図４～１２に関連して以下に説明する例示的な実施形態では、本発明のＲＦスイッチは、単一の３Ｖ外部電源を１つ必要とするだけである。先行技術によるスイッチでは、典型的に、少なくとも１つの６Ｖ外部電源ならびに正および負の電力供給を実現するための外部電圧発生回路が必要である

【００５０】

完全に集積化されたＲＦスイッチ

図４に、本発明に従って製造し、例示的で、完全に集積化されたＲＦスイッチ１００の簡易ブロック図を示す。図４に示すように、完全に集積化されたＲＦスイッチ１００には、上記において図３で説明した本発明のＲＦスイッチ３０（図４においては、簡略化した図式表現で示す）ＣＭＯＳ制御論理回路１１０および負電圧発生器回路１２０（「電荷ポンプ」回路を用いて、一実施形態において実現する）が含まれる。制御信号１３０は、ＣＭＯＳ論理回路ブロック１１０入力する。一実施形態では、制御信号１３０は、０ボルトから＋Ｖｄｄの範囲におよぶが、デジタル論理回路設計分野の当業者は、本発明の範囲または趣旨から逸脱することなく、他の論理回路レベルが使用できることを理解されるであろう。上記に提示した理由で、一実施形態では、完全に集積化されたＲＦスイッチ１００は、ＵＴＳｉ基板上に製造する。しかし、他の絶縁基板技術を用いることもできる。

【００５１】

以下により詳細に説明するように、完全に集積化されたＲＦスイッチ１００には、図２における先行技術のＲＦスイッチにはないいくつかの機能および特徴が含まれる。たとえば、本発明のＲＦスイッチ３０（図３に関連して上記に説明したように、新規な、トランジスタの積層およびゲートトランジスタ（ゲート抵抗）構成を用いる）に加えて、完全に集積化されたＲＦスイッチ１００では、本発明のスイッチと同じ集積回路上に、負電圧発生器およびＲＦスイッチ制御機能を一緒に集積する。以下により詳細に説明するように、完全に集積化されたＲＦスイッチ１００には、クロック入力信号を電荷ポンプ回路に供給する内蔵式発振器、他のＲＦスイッチ回路が必要とする負の電源電圧を発生する集積化電荷ポンプ回路、ＲＦスイッチトランジスタを制御する制御信号を発生するＣＭＯＳ論理回路、スイッチトランジスタの、ゲートードレイン、ゲートーソースおよびドレインーソース電圧を減少することにより、信頼性を増加させるレベルシフト回路ならびに電荷ポンプ回路およびデジタル制御論理回路からＲＦ信号エネルギを分離するＲＦバッファ回路が含まれる。これらの各回路は、関連する図を参照して、以下により詳細に説明する。

【００５２】

負電圧発生器ー電荷ポンプー第１の実施形態

図４に示すように、完全に集積化されたＲＦスイッチ１００の一実施形態には、負電圧発生器すなわち電荷ポンプ１２０が含まれる。負電圧発生器１２０によって、完全に集積化されたＲＦスイッチ１００の他の回路が必要とする負の電源電圧（以下、「－Ｖｄｄ」と記す）を発生する。２つの入力セット、すなわち、正の直流電源電圧信号（Ｖｄｄ）１２２およびクロック入力（単一の入力信号「Ｃｌｋ」として図に示す）１２４を、負電圧発生器１２０に供給する。クロック入力１２４は、図４で単一の入力信号として示してあるが、以下に図５ｂに関連して説明するように、本発明におけるＲＦスイッチのいくつかの実施形態では、クロック入力１２４は、２つまたはそれを超えるクロック入力信号を含むことができる。

【００５３】

さらに、図４に示す実施形態では、負電圧発生器回路１２０への入力である正の供給電圧には、直流３Ｖ電力供給源が含まれる。しかしながら、本発明の範囲または趣旨から逸脱することなく、他の電力供給レベルを用いてもよい。たとえば、所望ならば、直流３．５Ｖ、直流５Ｖまたは任意の他の都合のよい正の電力供給を、図４の負電圧発生器回路１２０への入力とすることができる。正の電力供給信号は、典型的には、外部の低電力供給源により発生する。

【００５４】

本発明の一実施形態において、図４の負電圧発生器１２０は、電荷ポンプ回路を用いて

実現する。図５ａに、図４の負電圧発生器１２０における例示的な一実施形態の簡易ブロック図を示す。図５ａの簡易ブロック図に示すように、負電圧発生器には、発振器２０２、クロック発生器回路２０４および本発明の電荷ポンプ回路２０６が含まれる。発振器２０２の出力は、クロック発生器回路２０４に入力される。クロック発生器回路２０４の出力は、電荷ポンプ回路２０６に入力される。負電圧発生器１２０により、完全に集積化されたＲＦスイッチ１００の他の回路が使用する負の電源電圧を供給する。

【００５５】

先行技術によるＲＦスイッチの多くでは、不利なことに、負の電源電圧は、ＲＦスイッチ回路に対して外部の回路で発生しなければならない。他のＲＦスイッチの実現では、ＲＦ入力信号の直流値を、印加したバイアス電圧の中間点にシフトするために必要な結合アプローチを用いる。このアプローチでは一般に、ＦＥＴゲートドライブがこのレベルシフトのために実効的に半分になるため、比較的高いバイアス電圧を印加する必要がある。バイアス電圧を増加しない場合、このことにより、スイッチ挿入損失に否定的な影響がもたらされる。なぜなら、これによりゲートドライブが減少し、それによってＦＥＴチャネル抵抗が増加するからである。

【００５６】

これらの問題に対処するために、完全に集積化されたＲＦスイッチ１００の一実施形態では、図５ｂに詳細に示す、本発明の電荷ポンプ回路２０６を使用する。図５ｂに示すように、電荷ポンプ回路２０６の第１の実施形態には、２つのＰチャネルＭＯＳＦＥＴトランジスタ２０８および２１０が含まれ、これらは、２つのＮチャネルＭＯＳＦＥＴトランジスタ２１２および２１４に直列に接続されている。電荷ポンプ回路２０６の左レッグ（第１のＮチャネルトランジスタ２１２に直列に接続された、第１のＰチャネルトランジスタ２０８を含む）は、電荷ポンプ回路の右レッグ（第２のＮチャネルトランジスタ２１４に直列に接続された、第２のＰチャネルトランジスタ２１０を含む）に、第１のキャパシタＣｐ２１６を用いて結合されている。図示のように、第２のＮチャネルトランジスタ２１４のソースは、出力キャパシタである第２のキャパシタＣ２１８に結合されている。２つの非重複クロック制御信号「Ｃ１ｋ１」および「Ｃ１ｋ２」は、トランジスタ２０８、２１０、２１２および２１４の動作を制御するために用いる。たとえば、図５ｂに示すように、「Ｃ１ｋ１」の逆の「Ｃ１ｋ１＿」は、Ｐチャネルトランジスタ２０８および２１０のゲートを制御する。他方の非重複クロック制御信号「Ｃ１ｋ２」は、図示のように、Ｎチャネルトランジスタ２１２および２１４のゲートを制御する。

【００５７】

電荷ポンプ２０６は、トランジスタゲートを駆動する非重複クロック制御信号Ｃ１ｋ１およびＣ１ｋ２を用いて、２つのキャパシタ（Ｃｐ２１６および出力キャパシタＣ２１８）を交互に充電および放電することにより、負の電源電圧（－Ｖｄｄ）を発生する。負の電源電圧－Ｖｄｄは、キャパシタＣ２１８に充電した電荷から発生する。一実施形態では、パルスシフト回路（図示せず）を用いて、電荷ポンプを駆動するパルス列（すなわち、パルス列は、クロック入力信号Ｃ１ｋ１およびＣ１ｋ２として入力される）を発生する。パルス列が、電荷ポンプ２０６に印加されるので、キャパシタＣｐ２１６は、正の電力供給Ｖｄｄを印加され、つぎにキャパシタＣ２１８を越えて反対方向に放電され、負の電源電圧－Ｖｄｄを生成する。電荷ポンプのどのトランジスタも、いずれのソース／ドレインノード間でも、Ｖｄｄを超えるものを避ける必要がなく、したがって、電荷ポンプ２０６の信頼性が大いに高まる。

【００５８】

本発明の電荷ポンプ回路２０６の一実施形態において、出力Ｃ２１８のキャパシタンスは約２００ｐＦであり、Ｃｐ２１６のキャパシタンスは約５０ｐＦである。電荷ポンプ設計分野の当業者は、本発明の範囲または趣旨から逸脱することなく、他のキャパシタンス値を使用できることを、理解されるであろう。

【００５９】

図５ａの簡易ブロック図に示すように、一実施形態において、２つの非重複クロック信号

は、内部発振器２０２が発生する発振信号から派生する。図５ａに示すように、発振器２０２は、発振信号を、クロック発生器回路２０４に入力し、今度はこの回路が、電荷ポンプトランジスタゲートを制御する２つの非重複クロック信号を（任意で便利な、周知の方法で）発生する。本発明の完全に集積化されたＲＦスイッチ１００の一実施形態では、発振器２０２には、（数ＭＨｚのオーダの）比較的低周波の発振器が含まれる。この実施形態では、発振器には、簡単な弛張発振器が含まれる。しかしながら、集積回路分野の当業者は、本発明の趣旨または範囲から逸脱することなく、他のタイプの発振器を用いて本発明を実施できることを、理解されるであろう。

【００６０】

図５ｃに、経時的に変化する、２つの非重複クロック信号Ｃｌｋ１およびＣｌｋ２の電圧振幅を示す。図５ｃに示すように、２つの非重複クロック信号は、－ＶｄｄからＶｄｄまでの電圧振幅で変化する。一実施形態において、クロック信号は、直流－３Ｖから直流＋３Ｖまで変化する。このように調整することによって、電荷ポンプ２０６の効率を改善する。

【００６１】

電荷ポンプトランジスタ２０８、２１０、２１２および２１４には、有利なことに、単一閾値のＮチャネル（２１２および２１４）およびＰチャネル（２０８および２１０）デバイスが含まれる。従来の電荷ポンプ回路は、複数閾値レベルデバイスの使用を必要とする。したがって、これら従来のものを実現するには、図５ｂにおける本発明の電荷ポンプ回路２０６よりも、設計が複雑でコストがかかった。本発明の電荷ポンプ２０６の一実施形態において、Ｐチャネルトランジスタ２０８および２１０の幅は約２０μｍ、長さは約０．８μｍである。Ｎチャネルトランジスタ２１２および２１４の幅は約８μｍ、長さは約０．８μｍである。集積回路設計分野の当業者は、本発明の範囲または趣旨から逸脱することなく、他の寸法のトランジスタが使用できることを、理解されるであろう。本発明の電荷ポンプ回路２０６は、非常に効率的であり、温度およびプロセスの変動にもかかわらず、申し分なく動作する。

【００６２】

レベルシフト回路

電荷ポンプ回路は、この回路に印加された電源電圧を効率的に２倍にするので、これらの高い電圧に関連した、電位の信頼性問題に注意を払わなければならない。トランジスタの信頼性を高めるような方法で電荷ポンプを実現するために、レベルシフト回路を用いて、トランジスタのゲート－ソース電圧、ゲート－ドレイン電圧およびドレイン－ソース電圧を、許容できるレベルに制限する。

【００６３】

本発明に従って作成された発明的なレベルシフト回路３００を図６ａに示す。レベルシフト回路３００を用いて、典型的または「普通の」デジタル入力信号（デジタル信号は、典型的にはグラウンド（ＧＮＤ）から＋ＶｄｄのＶｄｄの範囲におよぶ）を、－Ｖｄｄから＋ＶｄｄのＶｄｄの範囲におよぶように変換またはシフトする。それにより、完全に集積化されたＲＦスイッチの信頼性が高まる。本発明の一実施形態では、制御信号は、直流－３Ｖから直流＋３Ｖの範囲へシフトされるが、ＲＦスイッチ制御分野の当業者は、本発明の趣旨または範囲から逸脱することなく、他のレベルシフト電圧範囲が使用できることを理解されるであろう。

【００６４】

図６ａに示すように、本発明のレベルシフト回路３００（以後は、レベルシフタ３００と呼ぶ）には、フィードバック構造に結合された複数のインバータが含まれる。特に、図６ａに示す実施形態では、レベルシフタ３００には、２つのグループのインバータが含まれ、これらのインバータを用いて、第１および第２のシフトした出力信号、すなわち、第１の出力ノード３１４の「ｏｕｔ」およびその逆の、第２の出力ノード３１６の「ｏｕｔ＿」を発生する。第１のインバータグループには、インバータ３０２、３０４および３０４が含まれる。第２のインバータグループには、インバータ３０８、３１０および３１２

が含まれる。典型的または「普通の」デジタル入力信号（すなわち、ＧＮＤから＋Ｖｄｄの範囲にわたるデジタル入力信号）は、第１のインバータ３２０の入力ノード３１８で、レベルシフタ３００へ入力される。第１のインバータ３２０は、（出力ノード３２４で）第１の入力信号「ｉｎ」を発生し、この信号が、第２のインバータ３２２へ入力される。第２のインバータ３２２は、第１の入力信号「ｉｎ」の逆である第２の入力信号「ｉｎ＿」を、出力ノード３２６で発生する。したがって、第１および第２のインバータ３２０および３２２は、上記の２つのインバータグループへ入力される信号を発生する。たとえば、第１の入力信号「ｉｎ」は、インバータ３０２の入力部３２８に結合される。同様に、第２の入力信号「ｉｎ＿」は、インバータ３０８の入力部３３０に結合される。

【００６５】

第１のインバータグループの出力「ｏｕｔ」は、第１の出力インバータ３０６によって発生され、第１の出力ノード３１４へ供給される。第２のインバータグループの出力「ｏｕｔ＿」は、第２の出力インバータ３１２によって発生され、第２の出力ノード３１６に供給される。２つのレベルシフタ出力「ｏｕｔ」および「ｏｕｔ＿」は、図４の完全に集積化されたＲＦスイッチ１００の他の回路へ入力される。たとえば、一実施形態では、第１の出力「ｏｕｔ」は、スイッチングトランジスタ・グループ３３および分路トランジスタグループ３８におけるデバイスのゲートに結合される（すなわち、図６ａの第１の出力ノード３１４における「ｏｕｔ」信号は、入力ノード３３’および３８’で、図３の「ＳＷ」制御入力信号に結合され、それにより、図３に関連して上記で説明したように、スイッチングトランジスタ・グループ３３および分路トランジスタグループ３８の動作を制御する）。同様に、この実施形態では、第２のレベルシフタ出力「ｏｕｔ＿」は、図３の「ＳＷ＿」制御入力信号に（入力ノード３４’および３８’で）結合され、それにより、上記のように、スイッチングトランジスタ・グループ３４および分路トランジスタグループ３７を制御する

【００６６】

図６ａのレベルシフタ３００は、入力信号（すなわち、入力ノード３１８で供給される入力信号）の直流レベルをシフトし、一方、入力信号の周波数応答を不変にする。レベルシフタ３００は、完全に集積化されたＲＦスイッチ１００のシリコンオンインシュレータ基板での実現によって提供されるフローティング技術を十分に利用する。レベルシフタ３００のインバータは、差動バイアスに基づいて動作する。すなわち、レベルシフタは、２つの電圧信号の差異に基づいてデジタル入力信号をシフトする。特に、インバータ（たとえば、出力インバータ３０６および３１２など）に供給される電力供給信号間の差異が、Ｖｄｄのオーダである限りは、レベルシフタ３００は、確実に機能して、入力信号を－Ｖｄｄと＋Ｖｄｄ間の範囲でシフトする。一実施形態では、Ｖｄｄは直流３Ｖに等しい。この実施形態において、レベルシフタ３００のインバータ（たとえば、出力インバータ３０６および３１２）を構成するトランジスタでは、それらのソース／ドレインノード間に印加される電圧は、直流３Ｖよりも大きくはならない。このことによって、トランジスタデバイスの信頼性が増加する。

【００６７】

再び図６ａを参照すると、レベルシフタはフィードバック法を用いて、デジタル入力信号を、－Ｖｄｄから＋Ｖｄｄの範囲の電圧レベルにシフトする。特に、第２の出力ノード３１６における、第２のインバータグループ（３０８、３１０および３１２）の出力（すなわち、「ｏｕｔ＿」信号）が、インバータ３０４の入力部で、第１のインバータグループの入力部へのフィードバックとして供給される。同様に、第１の出力ノード３１４における、第１のインバータグループ（３０２、３０４および３０６）の出力（すなわち、「ｏｕｔ」出力信号）が、第２のインバータグループ、特に、インバータ３１０への入力として供給される。

【００６８】

入力ノード３１８におけるデジタル入力信号が論理的に「高い」状態になるとき（すなわち、いくつかの実施形態では、入力信号がＧＮＤから＋Ｖｄｄに遷移するとき）、「ｉ

ｎ」信号（ノード３２４における）および「ｉｎ＿」信号（ノード３２６における）は、それぞれレッグラウンド（たとえば、直流０Ｖ）およびＶｄｄ（たとえば、直流３Ｖ）になる。第１の出力ノード３１４の「ｏｕｔ」信号は、＋Ｖｄｄになる。同時に、第２の出力ノード３１６の「ｏｕｔ＿」信号は、－Ｖｄｄになる。（インバータ３０４の入力部へフィードバックされる「ｏｕｔ＿」およびインバータ３１０の入力部へフィードフォワードされる「ｏｕｌ」の）フィードバック構成により、レベルシフタ３００における状態の迅速な変化を確実にする。レベルシフタ３００は、入力信号が論理的に高い状態から論理的に低い状態に遷移（すなわち、＋ＶｄｄからＧＮＤに遷移）するときにも、同様に働く。入力ノード３１８のデジタル入力信号が、論理的に「低い」状態になると、「ｉｎ」信号（ノード３２４における）および「ｉｎ＿」信号（ノード３２６における）は、それぞれ、Ｖｄｄ（たとえば、直流３Ｖ）およびグラウンドになる。第１の出力ノード３１４における「ｏｕｔ」信号は、－Ｖｄｄになる。同時に、第２の出力ノード３１６における「ｏｕｌ＿」信号は、＋Ｖｄｄになる。再びフィードバックにより、レベルシフタ３００における状態の迅速な変化を確実にする。接地により、レベルシフタインバータにおいては、インバータのＭＯＳＦＥＴトランジスタにおけるソース／ドレインノード間の、完全なＶｄｄ電圧以上の降下は確実になくなる。

【００６９】

図６ｂに、図６ａのレベルシフタ３００を実現するために使用するインバータ（たとえば、インバータ３０２、３０４および３０６）の一実施形態を示す。図６ｂに示すように、インバータ３４０には、２つのＭＯＳＦＥＴデバイス、すなわちＰチャネルトランジスタ３４２およびＮチャネルトランジスタ３４４が含まれる。図示のように、これらのデバイスは直列に接続され、そのゲートをともに結合し、入力ノード３４６に供給される入力信号によって制御される。Ｐチャネルトランジスタ３４２のソースは、ノード３５０で、第１の電源電圧へ結合され、一方、Ｎチャネルトランジスタ３４４ソースは、ノード３５２で、第２の電源電圧へ結合される。図示のように、デバイスのドレインは、共に結合され、出力ノード３４８で、インバータの出力を生成する。本発明のインバータ３４０の一実施形態では、Ｐチャネルトランジスタ３４２は、幅が５μｍであり、長さが０．８μｍである。この実施形態では、Ｎチャネルトランジスタは、幅が２μｍであり、長さが０．８μｍである。トランジスタ設計分野の当業者は、本発明の範囲または趣旨から逸脱することなく、インバータ３４０のトランジスタとして、他の物理的寸法のものを使用できることを、理解されるであろう。インバータ３４０の論理表現を、また、図６ｂにおいて記号３６０として示してある。

【００７０】

このように、本発明のレベルシフタ３００を用いることによって、当初ＧＮＤから＋Ｖｄｄの範囲におよぶデジタル入力信号が、－Ｖｄｄから＋Ｖｄｄの範囲におよぶようにシフトされる。図７ａに、デジタル入力信号の、電圧振幅対時間のプロットおよび図６ａの本発明のレベルシフタ３００が発生する、対応する出力信号を示す。図７ａに示すように、デジタル入力信号は、グラウンドまたは直流０ＶからＶｄｄの範囲におよぶ。本発明のレベルシフタ３００の出力は、－Ｖｄｄから＋Ｖｄｄの範囲におよぶ。本発明におけるＲＦスイッチの一実施形態では、入力信号は、直流０Ｖから直流＋３Ｖの範囲におよび、レベルシフタ３００の出力は、直流－３Ｖから直流＋３Ｖの範囲におよぶ。本発明の範囲または趣旨から逸脱することなく、他の値の電源電圧を用いることができる。たとえば、一実施形態では、入力信号は、０から直流＋３．５Ｖまたは０から直流４Ｖの範囲とすることができる。この実施形態では、レベルシフタは、信号を、直流－３．５（または－４）Ｖから直流＋３．５（または＋４）Ｖにシフトする。

【００７１】

図７ｂに、図６ａにおける本発明のレベルシフタ３００の簡易論理記号を示す。この論理記号は、後の図面で用いる。図７ｂに示すように、デジタル入力信号は、入力ノード３１８（図６ａに関連して上記で説明したのと同じ入力ノード３１８）で供給される。レベルシフタ３００は、２つのシフトした出力、すなわち「ｏｕｔ」およびその逆の「ｏｕｔ

＿」を供給する。これらの出力は、それぞれ、出力ノード３１４および３１６（図６ａに関連して上記で説明したのと同じ出力ノード３１４および３１６）で供給される。

【００７２】

ＲＦバッファ回路

図８ａは、２段階レベルシフタ・バッファ回路４００の電気図である。図８ｂは、デジタル制御入力およびバッファ回路４００に対するインタフェースの簡易ブロック図である。図８ａの２段階レベルシフタ・ＲＦバッファ回路４００には、第１段階レベルシフタ３００および第２段階ＲＦバッファ回路４０２が含まれる。第１段階レベルシフタ３００は、図６ａ、６ｂ、７ａおよび７ｂに関連して上記で説明したものと同一であり、したがって、ここでより詳細に説明することはしない。上記で説明したように、レベルシフタ段階３００は、デジタル制御信号の論理レベルをシフトして、－Ｖｄｄから＋Ｖｄｄの範囲におよぶようにする。回路４００の第２段階には、ＲＦバッファ回路４０２が含まれる。ＲＦバッファ回路４０２は、ドライバの役割のみ果たす（ＲＦバッファ回路は、レベルシフトを行わない）。

【００７３】

ＲＦバッファは、図３に関連して上記に説明したＲＦスイッチ３０から、デジタル制御信号（図４のＣＭＯＳ論理ブロック１１０が発生するものなど）を電気的に分離する。ＲＦバッファ４０２は、ＲＦスイッチ３０におけるトランジスタの作動および不作動を制御する制御電圧（ＳＷおよびＳＷ＿のことだが、本明細書および図８ａではまた、それぞれ、制御信号「ｏｕｔ」および「ｏｕｔ＿」として示す）の垂下を抑制するように機能する。以下により詳細に説明するように、ＲＦバッファ４０２はまた、大電力ＲＦ信号が、負電力供給（すなわち、－Ｖｄｄ）に結合するのを防ぐように機能する。この負電力供給は、図５ａ～５ｃに関連して上記に説明したように、電荷ポンプ回路２０６が発生する。特に、ＲＦバッファ４０２は、ＲＦスイッチ３０における大電力ＲＦ信号の外延が、電荷ポンプ２０６（図５）が発生する負電力供給にＲＦ結合し、それにより、負電力供給から電流が排流するのを防ぐ。

【００７４】

きわめて大電力のＲＦ入力信号が、本発明のＲＦスイッチ３０に入力されるとき、デジタル論理信号をＲＦスイッチから分離するために、バッファ回路を用いていない場合には、ＲＦ信号とデジタル論理信号の結合が起こる。ＲＦ結合は、ＲＦトランジスタ制御信号（ＳＷおよびＳＷ＿）に有害な影響を与える可能性があるし、通常は、有害な影響を与える。たとえば、約３０ｄＢのオーダのＲＦ入力信号が、１ワットのＲＦスイッチ３０に入力される場合、ＲＦ結合により、デジタル制御線で零点数ボルトの電圧振動の起こる可能性がある。これは、ＲＦ信号が、ＲＦスイッチからデジタル制御回路へフィードバックされるためである。このＲＦ結合効果が、ＲＦトランジスタグループの作動および不作動、したがって、ＲＦスイッチ３０の正常な動作に悪い影響を与える可能性がある。図８ａのバッファ回路４０２によって、結合効果を防ぐ。

【００７５】

図８ａに示すように、本発明のバッファ回路４０２は、２段階回路４００の第１段階として上記に説明し図示したレベルシフタ３００と、構成において非常に似ている。レベルシフタ３００と同様に、ＲＦバッファ４０２には、２つのインバータグループ、すなわち第１のインバータグループ（４０４、４０６および４０８）ならびに第２のインバータグループ（４１０、４１２および４１４）が含まれる。第１のインバータグループ（４０４、４０６および４０８）の出力は、第１の出力インバータ４０８によって発生され、図では「ｏｕｔ」の符号を付けてあり、第１の出力ノード４１６で供給される。第２のインバータグループ（４１０、４１２および４１４）の出力は、第２の出力インバータ４１４によって発生され、「ｏｕｔ＿」の符号を付けてあり、第２の出力ノード４１８で供給される。出力信号「ｏｕｔ＿」は、出力信号「ｏｕｔ」の逆である。

【００７６】

重要なことだが、第１段階のレベルシフタ３００は、フィードバックを用いてレベルシ

フト機能を実行する（図６ａに関連して説明したように）が、ＲＦバッファ回路４０２は、その出力信号を入力へフィードバックしない。その結果、第１段階へ入力されるデジタル入力信号（すなわち、ノード３２８および３３０で、レベルシフタ３００に入力される制御入力信号）は、ＲＦスイッチトランジスタを制御するために使用する出力信号（すなわち、それぞれ、出力ノード４１６および４１８の制御出力信号「ｏｕｔ」およびその逆の「ｏｕｔ＿」であり、それぞれ、ＳＷおよびＳＷ＿制御信号線に結合される）から分離される。

【００７７】

再び図８ａを参照すると、特に、レベルシフタ３００は、デジタル制御信号「ｉｎ」およびその逆の信号「ｉｎ＿」を、それぞれ、ノード３２８および３３０で入力する（図６ａに関連して上記により詳細に説明したように）。出力ノード３１４における、レベルシフタ３００の第１の出力「ｏｕｔ１」は、図示のようにインバータ３１０の入力部へフィードバックされる。同様に、出力ノード３１６における、レベルシフタ３００の第２の出力「ｏｕｔ１＿」は、インバータ３０４の入力部へフィードバックされる。上記のように、このフィードバックトポロジのせいでＲＦ結合（すなわち、レベルシフタ出力信号が、ＲＦ信号をその上に重ね合わせる）が起こるのは、レベルシフタの出力信号を、ＲＦスイッチトランジスタを直接制御するために用いる場合（すなわち、バッファ回路４０２がない場合）である。したがって、本発明のＲＦバッファ回路４０２は、出力信号のフィードバックなしに用いて、入力信号（すなわち、デジタル入力信号「ｉｎ」および「ｉｎ＿」）を、ＲＦスイッチに存在するＲＦ信号から分離する。図８ａに示すように、レベルシフタ３００の第１の出力信号「ｏｕｔ１」は、ＲＦバッファ回路のインバータ４０４および４０６へ入力する。同様に、レベルシフタ３００の第２の出力信号「ｏｕｔ１＿」は、バッファ回路のインバータ４１０および４１２へ入力する。ＲＦバッファ回路４０２の２つの制御出力（「ｏｕｔ」および「ｏｕｔ＿」）は、ＲＦスイッチにおけるトランジスタの作動および不作動を制御するが、レベルシフタへのフィードバックとしては供給されない。したがって、ＲＦスイッチとデジタル論理回路間における分離の改善が達成される。

【００７８】

一実施形態において、２段階レベルシフタ・ＲＦバッファ回路４００を実現するインバータには、図６ｂに関連して上記に説明したインバータ３４０が含まれる。しかしながら、インバータ設計分野の当業者は、代替のインバータ設計を用いて、本発明の範囲または趣旨から逸脱することなく、２段階回路４００が実現できることを理解されるであろう。一実施形態では、第１段階レベルシフタ３００を実現するために使用するトランジスタは、第２段階ＲＦバッファ回路４０２を実現するため使用するトランジスタよりも物理的に小さい。より大きな寸法のトランジスタは、制御信号の効率的な増幅を達成するために、ＲＦバッファ回路４０２で用いる。たとえば、一実施形態では、ＲＦバッファを実現するために使用するトランジスタは、レベルシフタ３００を実現するために使用するトランジスタよりも、幅が３倍あり、その結果、電流の約３倍の増幅がもたらされる。トランジスタ設計分野の当業者は、デジタル制御信号における任意の望ましい増幅を達成するために、他の便利な寸法のトランジスタが使用できることを、理解されるであろう。

【００７９】

本発明の代替レベルシフト回路において使用する分圧器

図９ａは、低電流分圧器（「ＬＣＶＤ」）回路５００における一実施形態の電気図である。この回路は、図６ａに関連して上記に説明したレベルシフタ３００における一実施形態のフィードバック経路で使用する。図９ｂに、図９ａの分圧器５００を表すために使用する簡易論理記号を示す。分圧器５００を一実施形態で用いて、フィードバック・インバータトランジスタのゲート酸化物全体の過度の電圧振動に関連した潜在的なゲート酸化物信頼性問題と取り組む。レベルシフタ３００に関連して上記で説明したように、レベルシフタを実現するために使用する様々なＭＯＳＦＥＴのソース－ドレイン電圧は、Ｖｄｄより大きな電圧を印加されることは決してないが、レベルシフタの出力（すなわち、出力信号「ｏｕｔ」および「ｏｕｔ＿」）は、２×Ｖｄｄ（すなわち、－Ｖｄｄから＋Ｖｄｄま

で）も振動する可能性があるので、フィードバックインバータ３０４および３１０のゲート酸化物は、２×Ｖｄｄの電圧を印加される可能性がある。これらのフィードバック電圧レベルは、フィードバックインバータ３０４および３１０のゲート酸化物全体に印加され、結果として、ゲート酸化物信頼性問題が生じる可能性がある。

【００８０】

ゲート酸化物信頼性問題を回避できるようにするためには、フィードバックインバータ３０４および３１０のゲート酸化物全体に印加される最大電圧を、確実に、ほぼＶｄｄ（２×Ｖｄｄのゲート酸化物電圧ではなく）に低減する。したがって、本発明の完全に集積化されたＲＦスイッチにおける一実施形態では、図９ａの分圧器によって、レベルシフタ・フィードバックインバータ３０４および３１０のゲートに印加される電圧を制限する。この実施形態では、レベルシフタの出力（すなわち、出力ノード３１４および３１６におけるそれぞれの出力「ｏｕｔ」および「ｏｕｔ＿」）を、それぞれの、図６ａのレベルシフタに示すフィードバックインバータに直接フィードバックする代わりに、レベルシフタ出力信号を、最初に、図９ａの分圧器５００で調整して、その後、フィードバックインバータにフィードバックする。以下により詳細に説明するように、分圧器５００により、確実に、フィードバックインバータ３０４および３１０のゲート酸化物に印加される電圧が、Ｖｄｄと小さな電圧降下の合計（電圧降下は、分圧器５００を実現するために使用するトランジスタの数およびトランジスタ閾値電圧の関数である）を超えないようにする。一実施形態では、Ｖｄｄは直流３Ｖであり、電圧降下は直流０．９Ｖである。この実施形態では、分圧器５００のおかげで、ゲート酸化物は、直流約３．９Ｖ（すなわち、フィードバックインバータは、直流－３Ｖから直流０．９Ｖの範囲にわたる電圧を印加される）を超える電圧を決して印加されないことが確実になる。

【００８１】

ここで図９ａを参照すると、分圧器５００には、直列構成（すなわち、図示のように、ソースードレイン配置で互いの上に重ねる）でともに結合された複数のＭＯＳＦＥＴデバイス（５０２、５０４、５０６および５０８）含まれる。　実施形態では、ＭＯＳＦＥＴ５０２、５０４、５０６および５０８のゲートおよびドレインが、ともに結合して、積層ダイオードを実現している。ダイオードを実現するＭＯＳＦＥＴを以後は「ダイオードデバイス」と称するが、これらは、図示のように、直列に積層されている。分圧器５００にはまた、ＭＯＳＦＥＴＭ３（５１０）および出力ＭＯＳＦＥＴＭ２（５１２）が含まれる。これら２つのトランジスタの機能は、以下でより詳細に説明する。

【００８２】

ダイオードデバイスを使用して、入力ノード５１４で分圧器５００に供給される入力信号の電圧を分圧する。図９ａに示すように、分圧器５００に分圧される信号は、第１のデバイス５０２のドレイン（および接続されているゲート）に入力として供給される。入力信号が、ひとたび（ｎ×Ｖｔｈｎ）の正の電圧レベルを超えると、ここで「ｎ」は、分圧器５００を実現するために使用するダイオードデバイスの数で、Ｖｔｈｎは、デバイスの閾値電圧（すなわち、デバイスのドレインからソースへの「ダイオード降下」）だが、ダイオードデバイス（５０２、５０４、５０６および５０８）は、大量の電流を導通し始める。図９ａに示す実施形態では、ｎ＝４、Ｖｔｈｎ＝０．７ボルトだが、本発明の範囲または趣旨から逸脱することなく、「ｎ」およびＶｔｈｎに対して、代替値を用いることができる。たとえば、他の実施形態では、分圧器に供給する入力信号は、分圧器５００を実現するために使用するダイオードデバイスの数を変えることにより（すなわち、「ｎ」の値を変えることにより）、任意で所望の電圧レベルに制限できる。図９ａに示す実施形態では、入力電圧が、（４×０．７）の電圧レベルすなわち２．８ボルトをひとたび超えると、積層ダイオードデバイスがさかんに導通し始める。

【００８３】

バラスト抵抗器Ｒ５１６が、図示のように、出力ダイオードデバイス５０８のソースに接続されている。ひとたびダイオードデバイスが完全にターンオンすると、バラスト抵抗器Ｒ５１６のために、ｎ×Ｖｔｈｎの値を超える、任意の追加的入力電圧が降下する。図

９ａに示す実施形態では、バラスト抵抗器Ｒ５１６のために、（入力電圧－（４×Ｖｔｈｎ））の値を超える、任意の追加的入力電圧が降下する。分圧器５００の出力は、出力ダイオードデバイス５０８の、接続されたゲート－ドレインから引き出す。分圧された出力信号は、出力ノード５２０で供給される。ダイオードデバイス５０２、５０４および５０６のダイオード電圧降下およびバラスト抵抗器Ｒ５１６全体で降下する電圧のために、出力ノード５２０の出力は、ほぼ（入力電圧－（３×Ｖｔｈｎ））を決して超えないことが保証される。Ｖｔｈｎ＝約０．７Ｖおよび約３Ｖの最大入力電圧に対して、出力ノード５２０は、（直流３Ｖ－（３×直流０．７Ｖ））すなわち直流０．９Ｖを決して超えない。このように、図９ａに示す実施形態では、直流－３Ｖと直流＋３Ｖ間の範囲におよぶ入力電圧に対して、分圧器５００は、出力ノード５２０の出力を、直流－３Ｖから直流＋０．９Ｖの範囲に制限する。

【００８４】

出力ＭＯＳＦＥＴＭ２（５１２）はキャパシタとして構成され、分圧器５００のスイッチング時間の加速を支援するために使用する。入力が負電位に達したとき、ＭＯＳＦＥＴＭ３（５１０）は、出力ノード５２０が、入力ノード５１４における入力信号の電位に振動することを確実にする。これは、入力信号が負電位に達したとき、デバイスＭ３（５１０）がターンオンすることによって、達成される。したがって、入力信号が－Ｖｄｄ電位（たとえば、直流－３Ｖ）になるとき、出力ノード５２０の出力信号もまた－Ｖｄｄになる。出力デバイス５０８は、入力信号の負電圧振動の間、逆バイアスをかけられ、これにより、入力信号の負電圧振動の間、直流電流が、負の電力供給源から排流しないことが確実となる。分圧器の出力が直流約－３Ｖのとき、分圧器５００は、電流を少しも引き寄せない。このことは、重要である。なぜなら、電流は直流－３Ｖで、図５ｂに関連して上記に説明した電荷ポンプ回路を放電させるからである。分圧器の出力が約０．９Ｖのとき、バラスト抵抗器Ｒ５１６が比較的大きく選択されている場合には、引き寄せられる電流は、比較的少ない。しかしながら、この場合の電流は、正電圧（０．９Ｖ）とグラウンド間に生じるので、図９ａの分圧器５００の動作のために、追加的な電荷ポンプ電流が送られることはない。

【００８５】

一実施形態では、バラスト抵抗器Ｒ５１６の値は１００ｋΩである。一実施形態では、分圧器５００のデバイスは全て、同じ長さである。たとえば、一実施形態では、全てのデバイスは、長さが０．８μｍである。一実施形態では、全てのダイオードデバイス（５０２、５０４、５０６および５０８）の物理的寸法は同じである。一実施形態では、各ダイオードデバイスは、幅が２μｍであり、デバイスＭ３（５１０）は、幅が同じ２μｍであり、そして出力ＭＯＳＦＥＴＭ２（５１２）は、幅が１４μｍである。集積回路設計分野の当業者は、本発明の範囲または趣旨から逸脱することなく、図９ａに示すデバイスに対して、他の値および代替構成が使用できることを、理解されるであろう。たとえば、電気回路設計分野の当業者は、ダイオード素子の数「ｎ」を変えること、Ｖｔｈｎの値を変えること、またはダイオードデバイスの積層において、異なるポイントで出力ノード５２０を引き出すこと（たとえば、図示のように、デバイス５０８のドレインから引き出す代わりに、ダイオードデバイス５０６または５０４のドレインから出力を引き出すこと）によって、他の分圧器出力レベルが、簡単に調節できることを理解されるであろう。

【００８６】

分圧器を用いる修正レベルシフタ

ＲＦスイッチトランジスタのゲート酸化物に印加される電圧を減少することにより、図９ａおよび９ｂの分圧器５００を有利に使用して、上記のレベルシフタ３００および電荷ポンプ回路の両方におけるトランジスタの信頼性を高めることができる。たとえば、図１０に、図６ａのレベルシフタ３００と組み合わせて、図９ａの分圧器５００を使用する修正レベルシフタ６００を示す。図１０に示すように、レベルシフタ３００におけるインバータ３０６の出力（出力ノード３１４における）は、第１の分圧器５００’の入力部へ印加される。同様に、レベルシフタ３００のインバータ３１２の出力（出力ノード３１６に

おける）は、第２の分圧器５００’’の入力部に印加される。分圧器の出力は、図１０に示すように、フィードバックインバータ３０４および３１０の入力部へフィードバックされる。特に、図１０を参照すると、出力ノード５２０’における、第１の分圧器の出力「ｏｕｔ」は、フィードバックインバータ３１０の入力部へフィードバックされる。同様に、出力ノード５２０’’における、第２の分圧器の出力「ｏｕｔ＿」は、フィードバックインバータ３０４の入力部へフィードバックされる。図９ａに関連して上記に説明したように、レベルシフタ５００’および５００’’により、フィードバック電圧を、－Ｖｄｄから直流約＋０．９Ｖの範囲に減少する。このフィードバック経路の減少した電圧振動のために、レベルシフタ６００の機能が変わることはない。

【００８７】

ＲＦスイッチ制御信号「ＳＷ」および「ＳＷ＿」は、それらを分圧器５００’および５００’’へ入力する前に、レベルシフタ出力から引き出し、図３の本発明のＲＦスイッチ３０へ入力として供給できることに注目されたい。たとえば、図１０に示すように、出力ノード３１４における、インバータ３０６の出力は、スイッチ制御信号「ＳＷ」を発生するために、引き出して使用することができる。同様に、出力ノード３１６における、インバータ３１２の出力は、スイッチ制御信号「ＳＷ＿」を発生するために、引き出して使用することができる。一実施形態では、図８ａの２段階レベルシフタ・ＲＦバッファ回路４００に関連して上記で説明したように、ノード３１４および３１６から引き出した制御信号は、最初にバッファに格納され、その後ＲＦスイッチトランジスタに結合される。スイッチ制御信号ＳＷおよびＳＷ＿は、全域にわたる電圧振動が可能だが、これは、ＲＦスイッチにおける、ゲート酸化物の信頼性問題を引き起こさない。特に、スイッチ制御信号は、－Ｖｄｄから＋Ｖｄｄまでの範囲にわたる（すなわち、スイッチ制御信号の電圧レベルは、分圧器によって制限されない）。スイッチ制御信号の全面的な電圧振動は、ＲＦスイッチＭＯＳＦＥＴに関して、ゲート酸化物の信頼性問題を引き起こすことはない。なぜなら、ＲＦスイッチＭＯＳＦＥＴのソースが、接地されているからである。したがって、スイッチ入力信号は、ＲＦスイッチＭＯＳＦＥＴにおけるグラウンドに関連する。その結果、ＭＯＳＦＥＴは、グラウンドに対して正のＶｄｄ電圧を、ゲート酸化物全体に印加されるか、またはグラウンドに対して負のＶｄｄ電圧を、ゲート酸化物全体に印加される。

【００８８】

図１０にまた、修正レベルシフタ６００における一部分の簡易記号表現６０１を示す。記号６０１は、図１０の破線領域６０１’が示す部分を表す。図１０に示すように、記号による修正レベルシフタ６０１には、入力ノード３２６（「ｉｎ＿」）に対応する第１の入力「ｉｎ＿」６３０が含まれる。記号による修正レベルシフタ６０１にはまた、フィードバックインバータ３１０への入力に対応する、第２の入力「ｏｕｔ」６３２が含まれる。この信号はまた、第１の分圧器５００’の出力部５２０’から出ていることに注意されたい。正の電源電圧は、＋Ｖｄｄ入力部６３４で入力される。負の電源電圧は、－Ｖｄｄ入力部６３６で入力される。修正レベルシフタ６０１には、３つの出力信号、すなわち、「ｏｕｔ＿ｐｏｓ」（出力部６３８における）、「ｏｕｔ＿ｎｅｇ」（出力部６４０における）および「ｏｕｔ＿」（出力部６４２における）がある。これらの出力部は、上記の出力ノード６０６、６０８および５２０’’に対応している。理解を容易にするために、レベルシフタ６０１の記号表現は、以下に説明する図面において使用する。

【００８９】

図６ａに関連して上記に説明した、レベルシフタ３００に関連する潜在的なゲート酸化物信頼性問題は、修正レベルシフタ６００のフィードバック経路において、分圧器５００’および５００’’を用いて回避する。さらに、分圧器５００’および５００’’はまた、電荷ポンプ回路に関連する潜在的なゲート酸化物信頼性問題を減少するために機能することもできる。図１０に示すように、インバータ３０８および３１０の出力は、レベルシフタ３００から引き出され、２つの出力信号「ｏｕｔ＿ｐｏｓ」および「ｏｕｔ＿ｎｅｇ」を生成するために、２つの出力インターバルに入力として供給される。特に、インバータ３０８の出力は、第１の出力インバータ６０２への入力として供給される。同様に、フ

ィードバックインバータ３１０の出力は、第２の出力インバータ６０４への入力として供給される。

【００９０】

このような方法で出力インバータ６０２および６０４を結合することにより、修正レベルシフタ６００の出力信号は、決してＶｄｄ（またはーＶｄｄ）を超えることがなくなる。特に、第１の出力インバータ６０２は、第１の出力ノード６０６において、ＧＮＤ（すなわち、直流０Ｖ）から＋ＶｄｄのＲＦ範囲にわたる出力信号「ｏｕｔ＿ｐｏｓ」を発生する。第２の出力インバータ６０４は、第２の出力ノード６０８において、－ＶｄｄからＧＮＤの範囲にわたる第２の出力信号「ｏｕｔ＿ｎｅｇ」を発生する。入力信号「ｉｎ＿」がＧＮＤになると、出力信号「ｏｕｔ＿ｐｏｓ」もまたＧＮＤになる。出力信号「ｏｕｔ＿ｎｅｇ」がＧＮＤから－Ｖｄｄに移る。入力信号「ｉｎ＿」が正の＋Ｖｄｄになると、「ｏｕｔ＿ｐｏｓ」もまたＶｄｄになり、「ｏｕｔ＿ｎｅｇ」が－ＶｄｄからＧＮＤに移る。このように、本発明の修正レベルシフタ６００を用いると、「ｏｕｔ＿ｐｏｓ」出力信号は、ＧＮＤから＋ＶｄｄのＲＦ範囲にわたり、一方、「ｏｕｔ＿ｎｅｇ」出力信号は、－ＶｄｄからＧＮＤの範囲にわたる。以下により詳細に説明するように、２つの出力信号「ｏｕｔ＿ｐｏｓ」および「ｏｕｔ＿ｎｅｇ」を用いて、修正電荷ポンプ回路における潜在的なゲート酸化物信頼性問題に取り組む。ここで図１１ａおよび１１ｂに関連して説明するように、これらの出力信号を用いて、ＲＦバッファ回路における、潜在的なゲート酸化物信頼性問題に取り組むこともできる。

【００９１】

修正レベルシフタ・ＲＦバッファ回路

図８ａに関連して上記で説明した、２段階のレベルシフタ・ＲＦバッファ４００では、ＲＦバッファインバータ入力において、約２×Ｖｄｄの電圧振動を経験する可能性がある。すでに説明したように、このレベルの電圧振動では、ゲート酸化物信頼性問題が生じ、ＲＦバッファトランジスタの機能に有害な影響を与える可能性がある。

【００９２】

図１１ａおよび１１ｂに、図８ａに関連して上記に説明した、２段階レベルシフタ・ＲＦバッファ回路４００の代替実施形態を示す。図１１ｂに示す、ＲＦバッファの代替実施形態では、上記に説明した分圧器回路を用いて、確実に、ＲＦバッファのゲート酸化物にかかる電圧が、Ｖｄｄを０．９ボルトより超えないようにする。図１１ｂに示すように、代替の２段階レベルシフタ・ＲＦバッファ回路４００’には、第１段階レベルシフタ回路６００およびそれに結合された第２段階ＲＦバッファ回路４０２’が含まれる。レベルシフタおよびＲＦバッファ回路４００’のこの実施形態では、図１１に関連して上記で説明した、修正レベルシフタの出力「ｏｕｔ＿ｐｏｓ」および「ｏｕｔ＿ｎｅｇ」を、ＲＦバッファインバータへの入力として用い、ＲＦバッファ出力信号「ｏｕｔ」および「ｏｕｔ＿」を発生する。たとえば、図１１ｂに示すように、第１の修正レベルシフタ７００が発生する「ｏｕｔ＿ｐｏｓ」および「ｏｕｔ＿ｎｅｇ」出力信号は、２つのＲＦバッファインバータ７０２および７０４へそれぞれ入力される。同様に、第２の修正レベルシフタ７０６が発生する「ｏｕｔ＿ｐｏｓ」および「ｏｕｔ＿ｎｅｇ」出力信号は、２つのＲＦバッファインバータ７０８および７１０へそれぞれ入力される。図１１ａおよび１１ｂに示す代替の実施形態４００’に従い、入力信号「ｉｎ」が論理的に高い信号のとき、「ｏｕｔ＿ｐｏｓ」出力はＶｄｄになり、一方「ｏｕｔ＿ｎｅｇ」はＧＮＤになる。このように、入力信号「ｉｎ」が論理的に高い値のとき、インバータ７０２の出力はＧＮＤになり、インバータ７０４の出力は－Ｖｄｄになる。したがって、入力信号「ｉｎ」が高いとき、インバータ７１２の出力は（「ｏｕｔ」）－Ｖｄｄになる。入力信号「ｉｎ」が低いとき、反対の出力が生成される。

【００９３】

ＲＦバッファインバータ７０２および７０４を用いて、第１のＲＦ出力インバータ７１２の電源電圧を制御する。同様に、ＲＦバッファインバータ７０８および７１０を用いて、第２のＲＦ出力インバータ７１４の電源電圧を制御する。この実施形態では、ＲＦバッ

ファ出力信号「ｏｕｔ」および「ｏｕｔ＿」を用いてＲＦスイッチを制御する（すなわち、出力信号「ｏｕｔ」は、制御電圧「ＳＷ」として働き、一方、「ｏｕｔ＿」は制御電圧「ＳＷ＿」として働く）。

【００９４】

修正電荷ポンプ－代替実施形態

上記のように、図１０の修正レベルシフタ６００が発生する２つの出力信号「ｏｕｌ＿ｐｏｓ」および「ｏｕｔ＿ｎｅｇ」を、電荷ポンプ回路における代替の一実施形態で用いて、電荷ポンプに印加される過度の電圧に関連する、潜在的なゲート酸化物信頼性問題を減少または解消することができる。図５ｂおよび５ｃに関連して上記に説明したように、電荷ポンプトランジスタ（すなわち、Ｐチャネルトランジスタ２０８および２１０、ならびにＮチャネルトランジスタ２１２および２１４）のゲートを制御するために用いるクロック信号には、２×Ｖｄｄの電圧振動がある。たとえば、図５ｃに示すように、電荷ポンプクロック信号「Ｃｌｋ１」および「Ｃｌｋ２」は、負の電源電圧－Ｖｄｄから正の電源電圧＋Ｖｄｄの範囲にわたる。ＲＦバッファ回路およびレベルシフタ回路に関連して上記に説明したゲート酸化物信頼性問題と同様に、この全域にわたる電圧振動は、電荷ポンプ回路に酸化物信頼性問題を引き起こす可能性がある。したがって、ゲート酸化物に印加される電圧を、－Ｖｄｄから０．９Ｖの範囲に制限することにより、潜在的なゲート酸化物信頼性問題を減少または解消する修正電荷ポンプ回路を、図１２に示す。

【００９５】

図１２に、修正電荷ポンプ８００を示す。これは、図１０に関連して上記に説明した修正レベルシフタ６００を使用する。図１２に示すように、修正電荷ポンプ８００には、電荷ポンプ回路２０６’および本発明の電荷ポンプクロック発生回路８０２が含まれる。電荷ポンプクロック発生回路８０２によって、電荷ポンプ回路２０６’が使用するクロック制御信号を発生する。電荷ポンプ回路２０６’は、図５ｂに関連して上記で説明した電荷ポンプ２０６に、設計が非常に似ている。たとえば、電荷ポンプ回路２０６’には、パスキャパシタＣｐ２１６および出力キャパシタＣ２１８に加えて、一対のＰチャネルトランジスタ２０８および２１０、ならびに一対のＮチャネルトランジスタ２１２および２１４が含まれる。電荷ポンプ回路２０６’の一実施形態では、出力キャパシタＣ２１８には、数百ｐＦのオーダのキャパシタンスがあり、キャパシタＣｐ２１６には、約５０ｐＦのキャパシタンスがある。電荷ポンプ設計分野の当業者は、本発明の範囲または趣旨から逸脱することなく、他のキャパシタンス値が使用できることを、理解されるであろう。

【００９６】

電荷ポンプ２０６’の機能は、図５ａに関連して上記に説明した電荷ポンプ２０６と、非常に似ている。したがって、その動作を、ここで再び詳細に説明することはしない。図１２に示す電荷ポンプ２０６’が電荷ポンプ２０６と異なるのは、電荷ポンプ２０６’のトランジスタゲート（すなわち、トランジスタ２０８、２１０、２１２および２１４のゲート）を制御するために使用する制御信号が、電圧振動の半分の領域に制限されている点である（すなわち、－Ｖｄｄからグラウンドまたはグラウンドから Ｖｄｄの範囲に制限されている）。ゲート制御電圧が全域（すなわち、－ＶｄｄからＶｄｄまで）を振動するときに生じる、潜在的なゲート酸化物信頼性問題は、したがって、減少するかまたは解消される。

【００９７】

図１２に示すように、電荷ポンプクロック発生回路８０２には、フィードバック構成でともに結合された、４つの修正レベルシフタ８０４、８０６、８０８および８１０が含まれる。修正電荷ポンプの一実施形態では、４つの修正レベルシフタは、図１０に関連して上記に説明した修正レベルシフタ６００によって実現される。図１２に、図１０におけるレベルシフタ６００の記号表現６０１を用いたレベルシフタを示す。この実施形態では、レベルシフタ８０４、８０６、８０８および８１０は、図１０のレベルシフタ６００と同一の動作をする。２つの非重複クロック信号「Ｃｌｋ１」および「Ｃｌｋ２」（ならびに、それぞれの逆信号「Ｃｌｋ１＿」および「Ｃｌｋ２＿」）は、図１２に示すように、レ

ベルシフタの「ｉｎ＿」入力部に入力される。２つの入力クロック信号「Ｃｌｋ１」および「Ｃｌｋ２」は、図５ａ～５ｃに関連して上記で説明した非重複クロック信号と同一である。図５ｃに関連して上記で示したように、２つの非重複クロック信号は、－Ｖｄｄから＋Ｖｄｄの電圧振幅で変化する。一実施形態では、クロック信号は、直流－３Ｖから直流＋３Ｖまで変化する。

【００９８】

４つの修正レベルシフタにより、電荷ポンプ２０６’を制御するために使用する、半分の領域のクロック制御信号を発生する。特に、図１２に示すように、４つのレベルシフタにより、「ＣＬＫ１ＰＯＳ＿」、「ＣＬＫ１ＮＥＧ＿」、「ＣＬＫ２ＰＯＳ」および「ＣＬＫ２ＮＥＧ」制御信号を発生する。これらは、電荷ポンプ・トランジスタゲート制御ノード２５０、２５２、２５４および２５６へそれぞれ入力される。図１２に示す実施形態では、レベルシフタ８０５および８０８により、４つのトランジスタゲート制御信号「ＣＬＫ１ＰＯＳ＿」、「ＣＬＫ１ＮＥＧ＿」、「ＣＬＫ２ＰＯＳ」および「ＣＬＫ２ＮＥＧ」を発生する。レベルシフタ８０６により、「ＣＬＫ１ＰＯＳ＿」および「ＣＬＫ１ＮＥＧ＿」ゲート制御信号を発生し、一方、レベルシフタ８０８により、「ＣＬＫ２ＰＯＳ」および「ＣＬＫ２ＮＥＧ」ゲート制御信号を発生する。特に、図１２に示すように、レベルシフタ８０６の「ｏｕｔ＿ｐｏｓ」出力（「ＣＬＫ１ＰＯＳ＿」）は、トランジスタ２０８のトランジスタゲート入力部２５０を制御するために結合される。レベルシフタ８０６の「ｏｕｔ＿ｎｅｇ」出力（「ＣＬＫ１ＮＥＧ＿」）は、トランジスタ２１０のトランジスタゲート入力部２５２を制御するために結合される。同様に、レベルシフタ８０８の「ｏｕｔ＿ｐｏｓ」出力（「ＣＬＫ２ＰＯＳ」）は、トランジスタ２１４のトランジスタゲート入力部２５４を制御するために結合される。最後に、レベルシフタ８０８の「ｏｕｔ＿ｎｅｇ」出力（「ＣＬＫ２ＮＥＧ」）は、トランジスタ２１４のトランジスタゲート入力部２５６を制御するために結合される。クロック発生回路８０２は、電荷ポンプトランジスタにおけるゲート酸化物全体の過度の電圧を防ぐように機能する。

【００９９】

トランジスタ設計分野の当業者は、本発明の趣旨または範囲から逸脱することなく、他の制御構成が使用できることを、理解されるであろう。たとえば、他の２つのレベルシフタ（８０４および８１０）を用い、修正電荷ポンプの代替実施形態において、制御信号を発生できる。また、電荷ポンプ回路２０６に関連して上記で説明したように、代替のトランジスタ構成（Ｎチャネルおよびｐチャネル）を用いて、本発明の修正電荷ポンプ２０６’を実現することができる。

【０１００】

図１２に示すように、４つのレベルシフタ８０４、８０６、８０８および８１０は、図６ａに関連して上記で説明したレベルシフタのフィードバックトポロジと非常に似ているフィードバック構成において、ともにレベルシフタの組（８０４と８０６および８０８と８１０）に結合される。たとえば、レベルシフタ８０４の「ｏｕｔ＿」出力ノード（信号）は、その関連する組のレベルシフタ８０６の「ｏｕｔ」ノードへフィードバックとして供給される。同様に、レベルシフタ８０６の「ｏｕｔ＿」出力ノードは、その関連する組のレベルシフタ８０４の「ｏｕｔ」ノードへフィードバックとして供給される。同様に、レベルシフタ８０８の「ｏｕｔ＿」出力ノードは、その関連する組のレベルシフタ８１０の「ｏｕｔ」ノードへのフィードバックとして供給される。レベルシフタ８１０の「ｏｕｔ＿」出力ノードは、その関連する組のレベルシフタ８０８の「ｏｕｔ」ノードへフィードバックとして供給される。フィードバック構成は、４つのトランジスタゲート制御信号「ＣＬＫ１ＰＯＳ＿」、「ＣＬＫ１ＮＥＧ＿」、「ＣＬＫ２ＰＯＳ」および「ＣＬＫ２ＮＥＧ」の発生において、クロック発生回路８０２が使用する。

【０１０１】

概要

ＳＯＩ・ＣＭＯＳプロセスを用いて製造する新規なＲＦスイッチを提供する。ＳＯＩ基板の上にスイッチを製造すると、結果として、基板バイアスがなくなり、主なＣＭＯＳ回

路構成ブロックを、ＲＦスイッチ素子とともに集積することが可能となる。ＣＭＯＳ構成ブロックをＲＦスイッチ素子と集積することにより、単一外部電源（すなわち、負の電源電圧は、ＲＦスイッチとともに集積された電荷ポンプ回路で内的に発生する）だけの使用が必要な、完全に集積化されたＲＦスイッチという解決法が提供される。この結果として、ＲＦスイッチ分離、挿入損失および圧縮が改善される。一実施形態では、ＲＦスイッチの１ｄＢ圧縮ポイントは約１ワットを超え、挿入損失は約０．５ｄＢ未満であり、スイッチ分離は約４０ｄＢほどの高さである。本発明スイッチにより、また、スイッチング時間が改善する。

【０１０２】

本発明のいくつかの実施形態について、説明してきた。しかしながら、本発明の趣旨および範囲から逸脱することなく、様々な修正が可能であることを理解されるであろう。

【０１０３】

したがって、本発明は、特定の、例示した実施形態によって限定されるのではなく、添付の特許請求の範囲によってのみ限定されることを理解されたい。

【図面の簡単な説明】

【０１０４】

【図１ａ】ＲＦスイッチの性能特性を説明するために使用する、先行技術による単極単投（ＳＰＳＴ）ＲＦスイッチの簡易電気図である。

【図１ｂ】図１ａにおけるＳＰＳＴ・ＲＦスイッチの簡易電気図であり、このスイッチがターン「オン」され、ＲＦ信号が入力ノードから出力ノードへ通過可能となったときの、スイッチの主要な特性を示す。

【図１ｃ】ＲＦスイッチがターン「オフ」され、それによってＲＦ信号を出力ノードからブロックするときの、図１ａおよび１ｂにおけるＲＦスイッチの、同等な小信号電気特性を示す。

【図２】先行技術による単極双投（ＳＰＤＴ）ＲＦスイッチの簡易電気図である。

【図３】本発明の一実施形態によるＲＦスイッチの電気図である。

【図４】本発明に従って製造した、例示的で、完全に集積化されたＲＦスイッチの、簡易ブロック図である。

【図５ａ】図４の簡易ブロック図に示す負電圧発生器における例示的な一実施形態の簡易ブロック図である。

【図５ｂ】図４のＲＦスイッチへ負供給電圧を発生するために使用する電荷ポンプ回路における第１の実施形態の電気図である。

【図５ｃ】図５ｂの電荷ポンプ回路を制御するために使用する、２つの、重なり合わず、経時的に変化するクロック信号の電圧振幅を示す、電圧振幅対時間のプロットである。

【図６ａ】本発明のレベルシフト回路における第１の実施形態の電気図である。

【図６ｂ】図６ａのレベルシフタを実現するために使用するインバータにおける一実施形態の電気図である。

【図７ａ】デジタル入力信号およびそれに対応する、図６ａの本発明のレベルシフタが発生する出力信号の、電圧振幅対時間のプロットである。

【図７ｂ】図６ａにおける本発明のレベルシフタの簡易論理記号である。

【図８ａ】第１段階のレベルシフタおよび第２段階のＲＦバッファ回路を含む２段階レベルシフタ・ＲＦバッファ回路における一実施形態の電気図である。

【図８ｂ】デジタル制御入力および図８ａのＲＦバッファ回路に対するインタフェースの簡易ブロック図である。

【図９ａ】本ＲＦスイッチの発明に従って製造した低電流分圧器（ＬＣＶＤ）回路における一実施形態の電気図である。

【図９ｂ】図９ａの分圧器を表現するために使用する簡易論理記号である。

【図１０】図６ａのレベルシフト回路と組み合わせて、図９ａの低電流分圧器回路を用いているレベルシフト回路における第２の実施形態の電気図である。

【図１１ａ】図８ａの２段階レベルシフタ・ＲＦバッファ回路の代替実施形態を示す電気図である。

【図１１ｂ】図８ａの２段階レベルシフタ・ＲＦバッファ回路の代替実施形態を示す電気図である。

【図１２】図１０のレベルシフト回路を使用する修正電荷ポンプの電気図である。

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/32266

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H01F 17/15; H02K 17/60
US CL : 327/306, 535; 333/81R, 104
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 327/306, 535, 534, 536, 333; 333/81R, 104

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO APS EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,777,530 A (NAKATUKA) 07 July 1998 (07.07.1998), Figures 2, 4, 9.	1-42
Y	US 5,012,123 A (AYASLI et al) 30 April 1991 (30.04.1991), Figures 1A-1D.	1-42
Y	US 5,801,577 A (TAILLIET) 01 September 1998 (01.09.1998), Figures 3, 5.	16-40
Y	US 5,553,295 A (PANTELAKIS et al) 03 September1996 (03.09.1996), Figures 4.	16-40

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"B" earlier document published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

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(81)指定国　　AP(GH,GM,KE,LS,MW,MZ,SD,SL,SZ,TZ,UG,ZM,ZW),EA(AM,AZ,BY,KG,KZ,MD,RU,TJ,TM),EP(AT,BE,BG,CH,CY,CZ,DE,DK,EE,ES,FI,FR,GB,GR,IE,IT,LU,MC,NL,PT,SE,SK,TR),OA(BF,BJ,CF,CG,CI,CM,GA,GN,GQ,GW,ML,MR,NE,SN,TD,TG),AE,AG,AL,AM,AT,AU,AZ,BA,BB,BG,BR,BY,BZ,CA,CH,CN,CR,CU,CZ,DE,DK,DM,DZ,EE,ES,FI,GB,GD,GE,GH,GM,HR,HU,ID,IL,IN,IS,JP,KE,KG,KP,KR,KZ,LC,LK,LR,LS,LT,LU,LV,MA,MD,MG,MK,MN,MW,MX,MZ,NO,NZ,PL,PT,RO,RU,SD,SE,SG,SI,SK,SL,TJ,TM,TR,TT,TZ,UA,UG,US,UZ,VN,YU,ZA,ZW

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Ｆターム(参考) 5F038 BG02 BG05 DF01 DF17 EZ05 EZ06 EZ20
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DX72 EY01 EY10 EY21 EZ07 EZ13 EZ20 EZ55 GX01 GX02
GX04

【要約の続き】
ＲＦスイッチには、内蔵式発振器、電荷ポンプ回路、ＣＭＯＳ論理回路、レベルシフト回路および分圧器回路ならびにＲＦバッファ回路が含まれる。電荷ポンプ回路、レベルシフト回路、分圧器回路およびＲＦバッファ回路のいくつかの実施形態について記載している。本発明のＲＦスイッチによって、挿入損失、スイッチ分離およびスイッチ圧縮における改善が実現する。

SWITCH CIRCUIT AND METHOD OF SWITCHING RADIO FREQUENCY SIGNALS

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Classification:

- **international:** ***H01L21/822; H01L27/04; H01P1/15; H03K17/693;*** *H03K17/06;* (IPC1-7): H01P1/15; H03K17/60

- **cooperative:** **H01P1/15**; **H03K17/063**; **H03K17/102**; **H03K17/693**; **H03K19/018521**; **H03K19/0944**; H03K2017/0803

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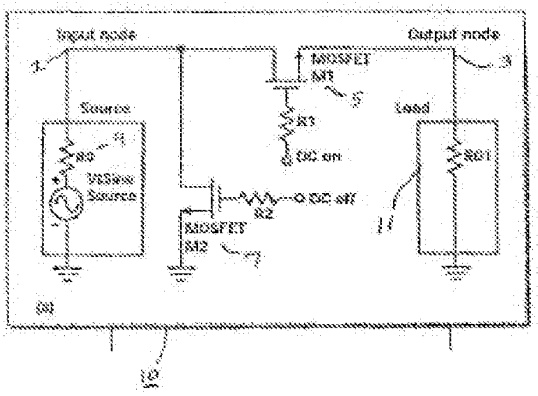

A RF switch circuit (20) is fabricated in a silicon-on-insulator "SOI" technology. The RF switch circuit (20) includes pairs of switching and shunting transistor grouping (33, 34, 37, 38) used to alternatively coupled RF input signals (RF1, RF2) to a common RF node (35). The switching and shunting transistor groupings (33, 34, 37, 38) comprise one or more MSFET transistors connected together in o "stacked" or serial configuration. The stacking of transistor groupings(33, 34), associated gate resistors increase the breakdown voltage across the series connected switch transistors and operate to improve RF switch compression. A fully integrated RF switch is described including digital control logic (110) and a negative voltage generator (120) integrated together with the RF switch elements (30).; In one embodiment, the fully integrated RF switch includes a built-in oscillator (202), a charge pump circuit (206), a level shifting, voltage divider circuits (500), and an RF buffer circuit (400). The inventive RF switch (20) provides improvements in insertion loss, switch isolation, and switch compression.

* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim 1]
(a) A first input port that receives a first RF input signal,
(b) A second input port which receives a second RF input signal,
(c) RF common port,
(d) A first switch transistor group who has a first node combined with said first input port, and the second node combined with the aforementioned RF common port, and is controlled by a switch control signal (SW),
(e) A second switch transistor group who has a first node combined with said second input port, and the second node combined with the aforementioned RF common port, and is controlled by an inversion signal (SW_) of the aforementioned switch control signal (SW),
(f) A first shunt transistor group who has a first node combined with said second input port, and the second node combined with a ground, and is controlled by the aforementioned switch control signal (SW),
(g) A second shunt transistor group who has a first node combined with said first input port, and the second node combined with a ground, and is controlled by an inversion signal (SW_) of the aforementioned switch control signal (SW),
It is an RF switching circuit for switching ****** and an RF signal,
When the aforementioned switch control signal SW is effective, while said first switch transistor group and said first shunt transistor group operate, Become non-operative [said second switch transistor group and said second shunt transistor group], and by that cause, Pass said first RF input signal to the aforementioned RF common port, shunt said second RF input signal to a ground, and when the aforementioned switch control signal SW is un-effective, While said second switch transistor group and said second shunt transistor group operate, An RF switching circuit which said first switch transistor group and said first shunt transistor group become non-operative, pass said second RF input signal to the aforementioned RF common port by that cause, and shunts said first RF input signal to a ground.
[Claim 2]
The RF switching circuit according to claim 1 manufactured in silicon on insulator (SOI) technology.
[Claim 3]
The RF switching circuit according to claim 1 manufactured on an ultra-thin silicon ("UTSi") substrate.
[Claim 4]

Said perfect insulation sapphire wafer the joint effect of a substrate by decreasing including an MOSFET transistor by which the aforementioned transistor group is formed in a thin silicon layer on a perfect insulation sapphire wafer, The RF switching circuit according to claim 3 which improves the performance characteristic of the aforementioned RF switch.
[Claim 5]
The RF switching circuit according to claim 4 which decrease in number when switch insertion loss decreases on resistance of the aforementioned MOSFET transistor.
[Claim 6]
The RF switching circuit according to claim 4 improved when the switch separation characteristics of the aforementioned RF switch decrease parasitic capacitance between nodes of the aforementioned MOSFET transistor.
[Claim 7]
The RF switching circuit according to claim 3 where the aforementioned transistor group contains two or more MOSFET transistors arranged at laminated constitution.
[Claim 8]
The RF switching circuit according to claim 7 where the aforementioned gate resistance machine is usually controlled by switching voltage including gate nodes by which the aforementioned lamination MOSFET transistor was combined with each related gate resistance machine.
[Claim 9]
The RF switching circuit according to claim 8 by which the aforementioned gate resistance machine combined with a transistor gate node of said first switch transistor group and said first shunt transistor group is usually controlled by the aforementioned switch control signal SW.
[Claim 10]
The RF switching circuit according to claim 8 where the aforementioned gate resistance machine combined with a transistor gate node of said second switch transistor group and said second shunt transistor group is usually controlled by aforementioned reversing-switch control signal SW_.
[Claim 11]
Have the gate capacitance to which the aforementioned MOSFET transistor relates, and a RC time constant relevant to each MOSFET transistor in the aforementioned transistor group, The RF switching circuit according to claim 8 where it is a function of the aforementioned gate resistance machine and the aforementioned related gate capacitance, the aforementioned RC time constant of each transistor exceeds a cycle of the aforementioned RF input signal far, and RF voltage is equally shared by it by the aforementioned whole MOSFET transistor.
[Claim 12]
Breakdown voltage of two or more aforementioned whole lamination MOSFET transistors of a selected transistor group, The RF switching circuit according to claim 8 where it is increased effectively [breakdown voltage of an individual MOSFET transistor of a transistor group who chose / aforementioned] n times, and n includes the total of an MOSFET transistor in a transistor group who chose [aforementioned].
[Claim 13]
The RF switching circuit according to claim 12 which has a related 1-dB compression point and increases the aforementioned 1-dB compression point using the aforementioned lamination MOSFET transistor composition.
[Claim 14]
Said first RF input signal and said second RF input signal have a related input power level, and

an input power level which increased by increasing the number of MOSFET transistors for every transistor group, The RF switching circuit according to claim 7 which can be adjusted in the aforementioned RF switching circuit.
[Claim 15]
Said first RF input signal and said second RF input signal have a related input power level, and by changing physical size of a transistor which uses an input power level which increased for a transistor group's realization, The RF switching circuit according to claim 7 which can be adjusted in the aforementioned RF switching circuit.
[Claim 16]
(a) An RF switching circuit of a description to Claim 3,
(b) A control logic block which outputs the aforementioned switch control signal (SW) and the aforementioned reversing-switch control signal (SW_) and which was combined with the aforementioned RF switching circuit,
(c) A negative voltage generator combined with the aforementioned control logic block which receives positive power supply voltage of a clock input signal and an external power, and outputs negative power supply voltage,
******, an RF switching circuit integrated completely.
[Claim 17]
The RF switching circuit according to claim 16 on which the aforementioned RF switching circuit is accumulated by integrated circuit (IC) with two or more digital circuits and analog circuitry and which was integrated completely.
[Claim 18]
(a) An oscillator which outputs a clock input signal,
(b) A charge pump which is combined with the aforementioned oscillator which inputs the aforementioned clock input signal, and outputs negative power supply voltage,
(c) A logic circuit block which outputs a control signal which is combined with the aforementioned charge pump and used for control of the aforementioned switch transistor group and the aforementioned shunt transistor group,
(d) A level shift circuit which decrease in number a gate drain, a gate source, and drain source voltage of an MOSFET transistor used in order to be combined with the aforementioned logic circuit block and the aforementioned RF switching circuit and to realize the aforementioned transistor group,
(e) An RF buffer circuit which is combined with the aforementioned RF switching circuit and separates RF signal energy from the aforementioned electric charge pump block and the aforementioned logic circuit block,
The RF switching circuit according to claim 16 which is included in a pan and which was integrated completely.
[Claim 19]
The aforementioned charge pump,
(a) At least two P channel MOS FET transistors,
(b) An N-channel metal oxide semiconductor FET transistor which it is at least two N-channel metal oxide semiconductor FET transistors, and each is combined with each related P channel MOS FET transistor and series, and forms each leg of the aforementioned charge pump by it,
(c) At least one joint capacitor which combines each leg of the aforementioned charge pump combined with a continuation leg,
(d) An output capacitor combined with an output leg of the aforementioned charge pump,

An implication,
Since the aforementioned P channel MOS FET transistor and the aforementioned N-channel metal oxide semiconductor FET transistor are driven for the aforementioned negative power supply voltage, The RF switching circuit according to claim 18 which is generated with the aforementioned charge pump by using a non-overlapping input clock signal, and charging and discharging alternately the aforementioned joint capacitor and the aforementioned output capacitor and which was integrated completely.
[Claim 20]
The RF switching circuit according to claim 19 where a first non-overlapping clock control signal controls P channel transistor including two non-overlapping clock control signals in the aforementioned non-overlapping input clock signal, and a second non-overlapping clock control signal controls N channel transistor and which was integrated completely.
[Claim 21]
The RF switching circuit according to claim 19 whose aforementioned P channel transistor and aforementioned N channel transistor are single threshold value transistors and which was integrated completely.
[Claim 22]
The RF switching circuit according to claim 19 where the aforementioned non-overlapping input clock signal is generated by pulse shift circuit and which was integrated completely.
[Claim 23]
The RF switching circuit according to claim 19 where the aforementioned non-overlapping input clock signal is pulled out from the aforementioned oscillator clock input signal and which was integrated completely.
[Claim 24]
The RF switching circuit according to claim 19 where the aforementioned oscillator contains a relaxation oscillator and which was integrated completely.
[Claim 25]
The RF switching circuit according to claim 19 where the aforementioned non-overlapping input clock signal changes by a voltage swing from -Vdd to +Vdd and which was integrated completely.
[Claim 26]
The RF switching circuit according to claim 18 where the aforementioned level shift circuit contains two or more inverters combined with both feedback composition and which was integrated completely.
[Claim 27]
In the aforementioned inverter, the aforementioned level shift circuit including a first difference input, a second difference input, a logic input, and fanout,
(a) Are an input inverter group containing two input differential inverters, and a first input differential inverter receives a logic-input signal (input), An input inverter group to whom a first logic-input signal (in) is outputted, and a second input differential inverter receives said first logic-input signal (in), and outputs reverse (in_) of said first logic-input signal,
(b) He is a first inverter group containing three differential inverters, The aforementioned fanout of a first inverter in said first inverter group, It is combined with said first logic-input signal (in), and the aforementioned fanout of said first inverter, It is combined with a first difference input of output inverters in said first inverter group, The aforementioned fanout of a second inverter in said first inverter group, A first inverter group to whom it is combined with a second difference

input of the aforementioned output inverters in said first inverter group, and said first inverter group's aforementioned output inverters output a first output signal (out),
(c) He is a second inverter group containing three differential inverters, The aforementioned fanout of said second inverter group's first inverter, It is combined with said reverse (in_) of said first logic-input signal, and the aforementioned fanout of said first inverter in said second inverter group, It is combined with a first difference input of output inverters in said second inverter group, The aforementioned fanout of a second inverter in said second inverter group, It is combined with a second difference input of the aforementioned output inverters in said second inverter group, and the aforementioned output inverters in said second inverter group contain said second inverter group who outputs a second output signal (out_),
Said first output signal (out) is supplied as feedback, It inputs into a logic-input part of said second inverter in said second inverter group, The RF switching circuit according to claim 26 which said second output signal (out_) is supplied as feedback, and is input into a logic-input part of said second inverter in said first inverter group and which was integrated completely.
[Claim 28]
The RF switching circuit according to claim 27 where said first output signal and said second output signal control the aforementioned switch transistor group and the aforementioned shunt transistor group of the aforementioned RF switch and which was integrated completely.
[Claim 29]
The RF switching circuit according to claim 26 which shifts direct current level of the aforementioned logic-input signal (input) without the aforementioned level shift circuit affecting a frequency response of the aforementioned input signal and which was integrated completely.
[Claim 30]
The aforementioned RF buffer circuit includes two stage circuits including the 1st step level shift circuit and the 2nd step RF buffer circuit, Said 1st step level shift circuit includes a level shift circuit defined by Claim 27, In said 2nd step RF buffer circuit, said two or more second differential inverters have a first difference input, a second difference input, a logic input, and fanout including two or more second differential inverters, respectively, and said 2nd step RF buffer circuit is further,
(a) He is a first RF buffer inverter group containing three differential inverters, The aforementioned logic input of a first inverter in said first RF buffer inverter group and a second inverter by the aforementioned level shift circuit, It is combined with said first output signal (out) output, and the aforementioned fanout of said first inverter in said first RF buffer inverter group, It is combined with a first difference input of output inverters in said first RF buffer inverter group, The aforementioned fanout of said second inverter in said first RF buffer inverter group, A first RF buffer inverter group to whom it is combined with a second difference input of the aforementioned output inverters in said first RF buffer inverter group, and said first RF buffer inverter group's aforementioned output inverters output a first output signal (OUT),
(b) He is a second RF buffer inverter group containing three differential inverters, The aforementioned logic input of a first inverter in said second RF buffer inverter group and a second inverter by the aforementioned level shift circuit, It is combined with said second output signal (out_) output, and the aforementioned fanout of said first inverter in said second RF buffer inverter group, It is combined with a first difference input of output inverters in said second RF buffer inverter group, The aforementioned fanout of said second inverter in said second RF buffer inverter group, A second RF buffer inverter group to whom it is combined with a second difference input of the aforementioned output inverters in said second RF buffer inverter group,

and said second RF buffer inverter group's aforementioned output inverters output a second output signal (OUT_),
******, the RF switching circuit according to claim 18 integrated completely.
[Claim 31]
The RF switching circuit according to claim 30 where the aforementioned RF buffer circuit separates a digital logic signal from the aforementioned RF switching circuit and which was integrated completely.
[Claim 32]
Said 2nd step RF buffer circuit does not supply feedback of the aforementioned output signal OUT and OUT_ to said 1st step level shift circuit, but it by it, The RF switching circuit according to claim 31 which improves separation of the aforementioned RF switch from the aforementioned digital logic signal and which was integrated completely.
[Claim 33]
The RF switching circuit according to claim 30 where a transistor used in order to realize said 1st step level shift circuit is smaller than a transistor used in order to realize said 2nd step RF buffer circuit and which was integrated completely.
[Claim 34]
A voltage divider circuit combined with the aforementioned output signal (out) and (out_) is included further, The RF switching circuit according to claim 27 where the aforementioned voltage divider circuit restricts a voltage level of the aforementioned output signal, and the aforementioned output signal is supplied to said second inverter of said 1st inverter group and said 2nd inverter group as feedback after that and which was integrated completely.
[Claim 35]
The RF switching circuit according to claim 34 where the aforementioned voltage divider circuit restricts the aforementioned voltage level to Vdd substantially and which was integrated completely.
[Claim 36]
The aforementioned voltage divider contains two or more MOSFET devices combined with both series constitution, The RF switching circuit according to claim 34 where an output MOSFET device is combined with a ground node via a ballast-resistances machine, and the aforementioned MOSFET device performs a diode function and which was integrated completely.
[Claim 37]
The aforementioned RF buffer circuit includes two stage circuits including the 1st step level shift circuit and the 2nd step RF buffer circuit, Said 1st step level shift circuit includes a level shift circuit defined by Claim 34, Said 2nd step RF buffer circuit contains two or more second differential inverters, said two or more second differential inverters include a first difference input, a second difference input, a logic input, and fanout, respectively, and said 2nd step RF buffer circuit is further,
(a) Are a first RF buffer inverter group containing three differential inverters, and the aforementioned logic input of a first inverter in said first RF buffer inverter group by the aforementioned level shift circuit, It is combined with a first output signal (out_pos1) output, and the aforementioned logic input of a second inverter in said first RF buffer inverter group by the aforementioned level shift circuit, It is combined with a second output signal (out_neg1) output, and the aforementioned output of said first inverter in said first RF buffer inverter group, It is combined with a first difference input of output inverters in said first RF buffer inverter group, The aforementioned fanout of said second inverter in said first RF buffer inverter group, A first

RF buffer inverter group to whom it is combined with a second difference input of the aforementioned output inverters in said first RF buffer inverter group, and said first RF buffer inverter group's aforementioned output inverters output a first output signal (OUT),
(b) Are a second RF buffer inverter group containing three differential inverters, and the aforementioned logic input of a first inverter in said second RF buffer inverter group by the aforementioned level shift circuit, It is combined with the 3rd output signal (out_pos2) output, and the aforementioned logic input of a second inverter in said second RF buffer inverter group by the aforementioned level shift circuit, It is combined with the 4th output signal (out_neg2) output, and the aforementioned output of said first inverter in said second RF buffer inverter group, It is combined with a first difference input of output inverters in said second RF buffer inverter group, The aforementioned fanout of said second inverter in said second RF buffer inverter group, It is combined with a second difference input of the aforementioned output inverters in said second RF buffer inverter group, and said second RF buffer inverter group's aforementioned output inverters contain a second RF buffer inverter group who outputs a second output signal (OUT_),
Said first output signal (out_pos1) includes an output to which the buffer of said first inverter in said first inverter group of the aforementioned level shift circuit was carried out, Said second output signal (out_neg1) includes an output to which the buffer of said second inverter in said first inverter group of the aforementioned level shift circuit was carried out, Said 3rd output signal (out_pos2) includes an output to which the buffer of said first inverter in said second inverter group of the aforementioned level shift circuit was carried out, The RF switching circuit according to claim 18 where said 4th output signal (out_neg2) includes an output to which the buffer of said second inverter in said second inverter group of the aforementioned level shift circuit was carried out and which was integrated completely.
[Claim 38]
The RF switching circuit according to claim 20 which the aforementioned non-overlapping input clock signal is input into a level shift circuit defined by Claim 34, and is input into the account charge pump of back to front and which was integrated completely.
[Claim 39]
The aforementioned level shift circuit includes a first level shift circuit and a second level shift circuit, Said first level shift circuit and said second level shift circuit are defined by Claim 34, Said first level shift circuit outputs a first output signal (clk1pos) from the aforementioned fanout of said first inverter in the first inverter group, A second output signal (clk1neg) is outputted from the aforementioned fanout of said second inverter in the first inverter group, The 3rd output signal (clk1pos_) is outputted from the aforementioned fanout of said first inverter in the second inverter group, The 4th output signal (clk1neg_) is outputted from the aforementioned fanout of said second inverter in the second inverter group, Said second level shift circuit outputs a fifth output signal (clk2pos) from the aforementioned fanout of said first inverter in the first inverter group, A sixth output signal (clk2neg) is outputted from the aforementioned fanout of said second inverter in the first inverter group, A seventh output signal (clk2pos_) is outputted from the aforementioned fanout of said first inverter in the second inverter group, The RF switching circuit according to claim 38 which outputs an eighth output signal (clk2neg_) from the aforementioned fanout of said second inverter in the second inverter group and which was integrated completely.
[Claim 40]
Said 3rd output signal (clk1pos_) controls a first P channel MOS FET transistor of the

aforementioned charge pump, Said 4th output signal (clk1neg_) controls a second P channel MOS FET transistor of the aforementioned charge pump, Said fifth output signal (clk2pos) controls a first N-channel metal oxide semiconductor FET transistor relevant to said first P channel MOS FET transistor, The RF switching circuit according to claim 39 where said sixth output signal (clk2neg) controls a second N-channel metal oxide semiconductor FET transistor relevant to said second P channel MOS FET transistor and which was integrated completely.
[Claim 41]
(a) A first input means for receiving a first high frequency signal,
(b) A second input means for receiving a second high frequency signal,
(c) A high frequency common port means,
(d) A first lamination transistor switching means that has a first node combined with said first input means, and the second node combined with the aforementioned high frequency common port means, and is controlled by a switch control signal (SW),
(e) A second lamination transistor switching means which has a first node combined with said second input means, and the second node combined with the aforementioned high frequency common port means, and is controlled by an inversion signal (SW_) of the aforementioned switch control signal (SW),

* NOTICES *

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damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[Field of the Invention]
[0001]
The background of invention
The field of invention
Especially the present invention relates to the switching circuit in an integrated circuit, and the switching method of a high frequency (RF) signal about a switch. According to one embodiment, the CMOS device realized on [for using it in the field of application of RF, such as a wireless communication equipment, a satellite, and cable TV,] a silicon on insulator (SOI) is contained in this switching circuit.
[Background of the Invention]
[0002]
The description of a pertinent art
As everyone knows, the high frequency (RF) switch serves as an important configuration block in many wireless communication systems. The RF switch is used for the communication equipment with which many, such as a cellular phone, a wireless pager, wireless infrastructure equipment, satellite communication equipment, and cable TV equipment, differ. As everyone knows, it opts for the performance of an RF switch by the three main performance parameters of operation, i.e., insertion loss, switch separation, and a "1-dB compression point." These three performance parameters are connected closely, and in the design of an RF switch component, when they think any one parameter as important, other parameters will be sacrificed for them. The 4th parameter sometimes taken into consideration in an RF switch design is usually called switching time or switching speed (one side of a switch is turned ON and defined as time required to turn OFF an opposite side). In the design of an RF switch, the ease of RF switch accumulation, a degree (level), complexity, the yield, a returned-goods loss, and a manufacturing cost are contained in other important indices.
[0003]
The performance parameter of these RF switches can be more easily described with reference to the RF switch design by the advanced technology shown in the simple circuit diagram of Fig.1 a - 1c. The simple circuit diagram of single-pole single-throw (SPST) RF switch 10 of the advanced technology is shown in Fig.1 a. The switching transistor M1 (5) and the shunt transistor M2 (7) are contained in SPST switch 10 of the advanced technology. If Fig.1 a is referred to here, it will be dependent on the state of two MOSFET transistors M1 (5) and the

control voltage of M2 (7) (). Namely, depending on the DC bias applied to the gate input part of the MOSFET switching transistor M1 and the shunt transistor M2, respectively an RF signal, It is sent to the RF output node 3 from the RF input node 1, or shunts via the shunt transistor M2 (7) in a ground. The actual value of DC bias voltage is dependent on MOSFET transistor M1 (5), and the polarity of M2 (7) and a threshold value. An RF power signal and the in-series resistor R0 (9) separate bias from a power supply signal.
It is indispensable for the highest switch performance.
"ON" state of RF switch 10 in Fig.1 a is shown in Fig.1 b (that is, to Fig.1 b). RF switch 10 shows the equivalent small signal value of the transistors M1 and M2 in case "ON" and the switching transistor M1 (5) are [ON and the shunt transistor M2 (7)] OFF. "OFF" state of the switch 10 of Fig.1 a is shown in Fig.1 c (that is, RF switch 10 shows the equivalent small signal value of the transistors M1 and M2 in case "OFF" and the switching transistor M1 (5) are [OFF and the shunt transistor M2 (7)] ON to Fig.1 c).
[0004]
As shown in Fig.1 b, when RF switch 10 is ON, the switching transistor M1 (5) is mainly resistance, and, on the other hand, its shunt transistor M2 (7) is mainly capacitive. "Insertion loss" of RF switch 10 is determined from the difference between the maximum available electric power in the input node 1, and the electric power supplied to the load of the output node 3. In a low frequency wave, when the switch 10 is ON (Fig.1 b should be referred to), each power loss originates in the on resistance 13 "r" with the limited switching transistor M1 (5). Typically, the on resistance r13 (Fig.1 b) is much smaller than the power-resistors machine R0 (9). Therefore, insertion loss "IL" has the characteristics like the formula 1 shown below.
Formula 1: IL is equal to 10 r/R0ln(10) =0.087r (dB) substantially.
[0005]
Therefore, the value of r serves as insertion loss of about 0.25 dB as a result at 3ohms by a low frequency wave. Since insertion loss is largely influenced by the on resistance of an RF switch transmitter, it lowers transistor on resistance and can improve insertion loss by decreasing parasitism board resistance.
[0006]
Generally, input-output separation (or simply switch separation) of an RF switch is determined by measuring the electric energy which "flows" out of an input port into an output port, when the transistor which has connected the input port and the output port is OFF. As for separation characteristics, the degree of cutting of an RF switch shows how much (that is, how much does a switch block an input signal from an output?). If "OFF" state of RF switch 10 in Fig.1 c is referred to especially here, the OFF state of the switch M1 (5) will serve to block the input 1 from the output 3. The shunt transistor M2 (7) serves to improve input-output separation of the switch 10.
[0007]
When a turn-off is carried out (namely, when RF switch 10 and the switching transistor M1 (5) carry out a turn-off) M1 (5), It is mainly capacitive and "feed through" (an RF input signal should pass from the input node 1 to the output node 3) of an input signal, The capacitor CGD OFF 15 (gate drain capacitance when the switching transistor M1 carries out a turn-off), Capacitor CGS OFF 17 (when the switching transistor M1 carries out a turn-off) The series / parallel value of a ** gate source capacitance, and capacitor CDS1 (19) and (a drain source capacitance when the switching transistor M1 carries out a turn-off) determine. The feed through of an input signal relates to input-output separation of RF switch 10 directly desirably. The size

of feed through is decreased using the shunt transistor M2 (7), and the separation characteristics of an RF switch are improved by it.
[0008]
When the switching transistor M1 (5) is a turn-off, turn-on of the shunt transistor M2 of Fig.1 c (7) is carried out. In this condition, the shunt transistor M2 (7) mainly works as a resistor of the value r. Depending on a design, the value of r is much smaller than impedance peculiar to RF power. As a result, r decreases remarkably the voltage of the input part of the switching transistor M1 (5). When the value of r is much smaller than the power resistors R0 (9) and feed-through capacitive resistance of the shunt transistor M2 (7), separation can be calculated easily. Switch separation of the OFF state of RF switch 10 is determined with the difference between the maximum available electric power of an input part, and the electric power of an outputting part.
[0009]
It is the capability to process the input power with another, important big RF switch performance characteristic in addition to the insertion loss of an RF switch, and separation. When turn-on of the switch is carried out, this is fixed frequency and is making for insertion loss not to serve as a function of input power into a positive thing. It is called for by many field of application that a switch cannot be distorted in the electric power sent through the switch which carried out "switch-on." For example, when two sounds which approached pass an RF switch simultaneously, they may start an intermodulation (IM) for the nonlinearity of a switch, and may generate a pseudo voice by the channel which adjoins by that cause. For example, when securing these adjoining channels for the information signal, the electric power of a pseudo voice must be maintained as small as possible. Switch compression or a "1-dB compression point" ("P1dB") shows the capability to process electric power. P1dB, it defines as input power when insertion loss increases only 1 dB from the low-electric-power value. Or when it has another way of speaking, a 1-dB compression point is a degree of the electric energy which can be input into an RF switch in an input port, before output power of only 1 dB deviates from linear relation with input power.
[0010]
Switch compression is generated in any one of the two routes. In order to understand how switch compression occurs, it describes about operation of the MOSFET transistor shown in RF switch 10 of Fig.1 a - 1c. In order to carry out turn-on of the MOSFET as everyone knows in the transistor design field, the gate source bias exceeding threshold voltage V_t is required. Similarly, gate source bias must be smaller than V_t, in order for a switch to be come by off. V_t is positive in "N type" MOSFET.
In "P type" MOSFET, it is negative.
N-channel MOS FET is chosen as RF switch 10 of Fig.1 a - 1c. The source of N-channel MOS FET is a node of the lowest electric potential.
If Fig.1 c is referred to again and the shunt transistor M2 (7) will carry out turn-on to the part period of an input signal cycle as a result of the transient voltage of the shunt transistor M2 (7), input power will be sent to a ground and will be lost to an output. The loss of this electric power will increase, if input power increases (namely, input signal of the electric power which increased), and thereby, it causes a first type of compression. The 1-dB compression point of RF switch 10 is determined by the signal vibration of the input in the point it stops in the shunt transistor M2 (7) which carried out the turn-off keeping [OFF / point] not been. After all, a negative vibration of an input is lower than a ground, and becomes lower than M2 gate potential in a similar manner (therefore, it source-izes). If this difference becomes equal to V_t, the

transistor M2 (7) will begin to carry out turn-on, and compression will start. This first type of compression is caused by the turn-on phenomenon of the no MARIOFU type gate in the shunt leg of an RF switch. Once the shunt transistor M2 (7) carries out turn-on, the electric power of the output node 3 will not follow the electric power of a switch input part any longer at linearity. A second type of RF switch compression is generated when the source and drain of the shunt transistor M2 (7) carry out breakdown on excessive voltage. This voltage has only the possibility exceeding service voltage direct-current abbreviation+1V to a submicron silicon on insulator (SOI) device. In breakdown, a shunt device begins to conduct a lot of electric power, and the electric power which can be used with an output by that cause decreases.

[0011]

The simple figure of single pole double throw (SPDT) RF switch 20 by the advanced technology is shown in Fig.2. As shown in Fig.2, four MOSFET transistors 23, 24, 27, and 28 are contained in RF switch 20 of the advanced technology at worst. The transistors 23 and 25 work as a "path" or a "switching" transistor (to switching MOSFET transistor M1 (5) and the appearance of drawing 1 a-1c), It is constituted so that each of these related RF input node may be combined with RF node 25 common in alternative. For example, when operating, the switching transistor 23 combines the first input signal "RF_1" that is an input to the first RF input node 21 to the RF common nodes 25 (namely, when switched to "ON"). Similarly, when operating, the switching transistor 24 combines the second RF input signal "RF_2" which is an input to the second RF input node 22 to the RF common nodes 25. The shunt transistors 27 and 28 by the case where it is operating those related RF input nodes, When not having combined with the RF common nodes 25, it works in order to shunt each related RF input node to a ground in alternative (namely, when the turn-off of the switching transistor (23 or 24) connected to those related input nodes is carried out).

[0012]

In order to control operation of the RF switch of the advanced technology to be shown in Fig.2, two control voltage is used. The control voltage with the name of "SW" and its reverse "SW_" controls operation of the transistors 23, 24, 27, and 28. control voltage is an alternative about the pair of the selected transistor ---like -- an operation (turn-on) -- or it is adjusted so that it may be made non-operative (turn-off). For example, as shown in Fig.2, SW turns on (according to some embodiments). When this is determined by setting control voltage to a voltage level logically "high", for example, "+Vdd", the switching transistor 23 is operating and the related shunt transistor 28 also operates. However, reverse SW_ of SW controls operation and its related shunt transistor 27 of the second switching transistor 24, and control signal SW_, during ON (according to some embodiments, this is determined by setting SW_ as -Vdd) of SW, since it is off, these two transistors are non-operative in this same period -- or the turn-off is carried out. RF_1input signal is combined with the RF (passing switching transistor 23 which is operating) common port 25 in this state (in SW, SW_ turns off by ON). Since the turn-off of the second switching transistor 24 is carried out, RF_2 input signal is blocked from the RF common port 25. Moreover, since an RF_2 input signal is shunted in a ground via the shunt transistor 28 which is operating, it is further separated from the RF common port 25. When [whose SW control signal is "OFF" (and SW_ "ON") like] it will be understood easily, the person skilled in the art of the transistor design field, RF_2 signal is the same method and is combined with the RF common port 25 (and RF_1signal is shunted to a block ** leg round).

[0013]

RF switches, such as SPDF, RF switch 20, etc. of Fig.2, have so far been realized with the result

on various performances in different element technology including a bulk complementary metal oxide semiconductor (CMOS) and gallium arsenide (GaAs) technology. In fact, GaAs technology is being used for almost all highly efficient high frequency switches. In realization of the RF switch by the advanced technology, although it has tried to improve the above-mentioned RF switch performance characteristic, those results are miscellaneous and are various. [of the complexity of an integrated circuit and the degree of the yield] For example, bulk CMOS and an RF switch show a high insertion loss performance characteristic, the low compression performance characteristic, and an insufficient linearity performance characteristic to a disadvantageous thing. By contrast, for semi insulating [of GaAs material], the parasitism board resistance can decrease remarkably and, thereby, can decrease switch insertion loss. Similarly, a half-insulation GaAs substrate improves switch separation.

[0014]

Although improvement in a performance characteristic is brought about by realization of a GaAsRF switch, this technology has some faults. For example, the yield of the integrated circuit which functions normally in GaAs technology is comparatively low. It tends to become expensive [a design and manufacture] comparatively [a GaAsRF switch]. In addition, although GaAs switches improve an insertion loss characteristic as mentioned above, frequency restrictions may become low for the slow surface state which exists in a GaAs substrate. Since this technology is not fit for integration of the high level, an "off-chip" needs to realize the digital control circuit relevant to an RF switch from a switch. It turns out that the low-electric-power circuit relevant to a switch is difficult to be accumulated. Since this makes overall system cost or manufacturing cost, size, and complexity increase and decreases the throughput speed of a system similarly, it is disadvantageous.

[Description of the Invention]

[Problem to be solved by the invention]

[0015]

Therefore, it is desirable to provide the method of switching the RF switch and RF signal which have an improved performance characteristic. It is desirable to provide the RF switch which insertion loss, separation, and compression have improved especially. Design manufacture of such an RF switch was completed easily, it was manufactured comparatively inexpensive, and is fit for accumulation of the high level, and it is desirable that it is applicable from a low frequency wave to high frequency. It should enable it to accumulate a power control circuit on chip simply with a switch function. Such accumulation was difficult to realize until now using a Si substrate and a GaAs substrate. The present invention provides such an RF switch and the switching method of an RF signal.

[Means for solving problem]

[0016]

The outline of invention

It describes about the switching method of a new RF switching circuit and an RF signal. An RF switch is usable for a wireless use, and can be manufactured with silicon on insulator technology. In one embodiment, an RF switch is manufactured on an ultra-thin silicon ("UTSi") substrate. The following thing is contained in an RF switch in one embodiment. Namely, the first switching transistor group who is connected to the input part for receiving an RF signal, the input part for receiving an RF signal, and RF common port, and is controlled by switching voltage (SW), It is connected to a first switching transistor group and RF common port, The second switching transistor group controlled by switching voltage (SW_) is contained, and SW_ is the reverse of

SW, and when a first switching transistor group is ON, a second switching transistor group is come by off. A switching transistor group connects each RF input signal to RF common port in alternative, while operating. In this embodiment, it is combined with an RF switch by the switching transistor group again, and the shunt transistor group controlled by the switching voltage SW and SW_ is contained. While operating, a shunt transistor group works so that those related RF input nodes may be shunted to a ground in alternative, and improves RF switch separation by it.

[0017]

One or more MOSFET transistors connected by lamination or series constitution are contained in both switching and a shunt transistor group. Within each transistor group, the gate of a lamination transistor is usually controlled by switching voltage (SW or SW_), and this switching voltage is combined with each transistor gate via each gate resistance machine. The compression point of a switch increases with lamination and the gate resistance machine of a transistor group device. The RC time constant formed of the gate resistance machine and gate capacitance of MOSFET is designed to become much longer than the cycle of an RF signal, and RF voltage is equally shared with the whole series-connection device. By this composition, the 1-dB compression point of an RF switch increases.

[0018]

It describes about the RF switch integrated completely. A digital switch control logic circuit and the negative power-supply-voltage generator accumulated with the RF switch of the present invention are contained in this RF switch. According to one embodiment, the RF switch of the advanced technology is provided with some functions not existing by the RF switch integrated completely. For example, in one embodiment, to the RF switch integrated completely. The built-in type oscillator which supplies a clock input signal to a charge pump circuit, and the charge pump circuit which generates the negative power supply voltage which other RF switching circuits need and which were accumulated, The CMOS logic circuit which generates the control signal which controls RF switch transistor, The level shift circuit and low current voltage divider circuit which increase the reliability of a switch device, and the RF buffer circuit which separates RF signal energy from a charge pump circuit and a digital control logic circuit are included. It describes about some embodiments of a charge pump circuit, a level shift circuit, a voltage divider, and an RF buffer circuit. By the RF switch of the present invention, insertion loss, switch separation, and switch compression are improved. Thanks to the accumulation of a higher level which becomes available with the RF switch of the present invention, by using the present invention, a design and manufacturing cost of RF system decrease, and reliability increases.

In the following brief explanation of the drawings, the same reference mark of various Drawings shows the same component.

[Best Mode of Carrying Out the Invention]

[0019]

DETAILED DESCRIPTION

It should let this Description pass and the preferable embodiment and working example to clarify should be considered as an illustration thing rather than the limitation to the present invention.

The RF switch of the present invention

The present invention is a method for switching a new RF switch design and RF circuit. The first illustration embodiment of RF switch 30 of the present invention is shown in Fig.3. As shown in Fig.3, in one embodiment, four clusters or a "group" of an MOSFET transistor is contained in RF switch 30 of the present invention. These are shown in Fig.3 as the transistor groups 33, 34,

37, and 38. A "path" or "switching" transistor groups 33 and 34 are contained in two transistor groups, and the shunt transistor groups 37 and 38 are contained in two transistor groups. One or more MOSFET transistors arranged at series constitution are contained in each transistor group. For example, in the embodiment shown in Fig.3, three switching transistor M_{33A}, M_{33B}, and M_{33C} are contained in the switching group 33. Similarly, three switching transistor M_{34A}, M_{34B}, and M_{34C} is contained in the switching group 34. Three transistor M_{37A}, M_{37B}, and M_{37C} are contained in the shunt group 37. Similarly, three transistor M_{38A}, M_{38B}, and M_{38C} are contained in the shunt group 38. Although the transistor groups 33, 34, 37, and 38 are shown in Fig.3 as a thing containing three MOSFET transistors, The person skilled in the art of the RF switch design field will be understood [that a substitute group configuration can be used and], without deviating from the range or the meaning of the present invention. For example, without deviating from the range of the present invention so that it may describe in detail by the following, any convenient number of transistors can be used and the group who shows Fig.3 can be realized.

[0020]

In one embodiment of the RF switch of the present invention, an MOSFET transistor (for example, transistor M_{37A}, M_{37B}, and M_{37C}) is realized using the substrate silicon on insulator (SOI) technology insulated completely. So that it may describe in detail by the following especially the MOSFET transistor of the RF switch of the present invention, It realizes using "ultra-thin silicon (Ultra-Thin-Silicon) (UTSi)" (in this Description, it is called "ultra-thin silicon on sapphire (ultrathin silicon-on-sapphire)") technology. In accordance with a UTSi manufacturing method, the transistor used in order to realize the RF switch of the present invention is formed in the ultra-thin layer of the silicon in an insulating sapphire wafer. Perfect insulating silicon on sapphire improves the performance characteristic of the RF switch by the present invention by decreasing the harmful joint effect of a substrate relevant to a non-insulating substrate and a semi insulating substrate. For example, an improvement of insertion loss lowers the on resistance of a transistor, and is realized by decreasing parasitism board resistance. Switch separation improves using the perfect insulating substrate provided by UTSi technology. Thanks to insulation with perfect silicon on sapphire technology, as compared with bulk CMOS and other conventional integrated circuit production technology, the parasitism capacitance between the nodes of RF switch 30 decreases remarkably. As a result, in the RF switch of the present invention, switch separation is improved as compared with the RF switch design of the advanced technology.

[0021]

A transistor group is controlled by the two control signals SW and reverse SW_ of those like the switch described above in relation to Fig.2 to be shown in Fig.3.A control signal is combined with the gate of each transistor via each related gate resistance machine. For example, three transistors [in / in the control signal SW / the switching transistor group 33] (M_{33A}) Operation of M_{33B} and M_{33C} is controlled via the gate resistance machine (R_{33A}, R_{33B}, and R_{33C}) relevant to three each. The control signal SW is input into input node 33', and controls the switching transistor group 33. SW is input into input node 38', and controls the shunt transistor group 38 again. Similarly, reverse SW_ of SW controls the switching transistor group 34 via input node 34'. SW_ is input into input node 37', and controls the shunt transistor group 37 again.

[0022]

In one embodiment, although about 30K ohm of a resistor is contained in a transistor group's resistor, substitute resistance can be used, without deviating from the meaning or the range of the present invention. In some embodiments of the present invention, any resistance element which

has comparatively high resistance is contained in a gate resistance machine. For example, in one embodiment, a gate resistance machine may be realized using a reverse bias diode. A gate resistance machine is useful to increase the effective breakdown voltage of the whole series-connection transistor so that it may describe in detail by the following.

[0023]

Function as controlling a control signal about the transistor groups' 33, 34, 37, and 38 operation, and un-operating, and RF switch 30, or [passing an RF signal in a way similar with controlling the analog transistor of the switch in Fig.2 generally] -- or it functions as blocking. Especially the switching transistor groups 33 and 34 function as a path transistor or a switching transistor, and in alternative, they are constituted so that each related RF input node may be combined with common RF node 35. For example, if the switching transistor group 33 operates, he will combine with the RF common nodes 35 the first RF input signal "RF_1" that is an input to the first RF input node 31. Similarly, if the switching transistor group 34 operates, he will combine the second RF input signal "RF_2" which is an input to the second RF input node 32 to the RF common nodes 35. The shunt transistor groups 37 and 38, If it operates, when those related RF input nodes will not have combined with the RF common nodes 35 () That is, when the turn-off of the switching transistor group (33 or 34) connected to the related input node is carried out, each related RF input node is committed so that it may shunt to a ground in alternative.

[0024]

In alternative, the group as which the transistor group chose control voltage is connected an operation or in order to make it non-operative. For example, as shown in Fig.3, when SW is ON (according to some embodiments) This is determined when the control voltage SW is set as a voltage level logically "high", The switching transistor group 33 operates (that is, all the transistors of the group 33 carry out turn-on), and the related shunt transistor group 38 also operates (that is, all the transistors of the group 38 carry out turn-on). However, like operation of the switch in Fig.2, since the second switching transistor group 34 and its related shunt transistor group 37 are controlled, reverse SW_ of SW, These two transistor groups become non-operative in this period (that is, the turn-off of all of the groups' 34 and 37 transistor is carried out). Therefore, when SW is ON, RF_1 input signal is combined with the RF common nodes 35. Since the switching transistor group 34 is off, RF_2 input signal is blocked from the RF common nodes 35. Since RF_2 input signal is shunted in a ground via the shunt transistor group 38 who operated, it is further separated from the RF common nodes 35. Like, RF_2 signal is the same method when [whose SW control signal is OFF (SW_control signal. and ON)] the person skilled in the art of the RF switch design field will be understood, and it is combined with the RF common nodes 35 (and RF_1 signal is shunted to a block ** leg round).

[0025]

As shown in RF switch 30 of the present invention in Fig.3, one to laminate an MOSFET transistor and use a gate resistance machine is making high breakdown voltage of the whole series-connection transistor. The RC time constant formed of the gate capacitance of a gate resistance machine and MOSFET is designed to become much longer than the cycle of an RF signal. So, RF energy does not almost have dissipating via a gate resistance machine. RF voltage is effectively shared equally with the whole series-connection transistor by this arrangement. As a net effect, the breakdown voltage of the whole series-connection device increases by n times the breakdown voltage of individual FET. In this case, n is the number of the transistors connected in series. By this composition, the 1-dB compression point of RF switch 30 of the present invention increases.

[0026]
In order to improve switch performance, the RC time constant must be made into big size to an RF signal cycle. This will impose restrictions on the minimum of R which can be used mainly for realizing gate transistors (gate resistance machine). As mentioned above, although the typical value for R is 30komega in one embodiment of the present invention, other resistance can also be used, without deviating from the range of the present invention. Since an MOSFET gate input part does not draw a direct current near, the bias in a device is not changed for the IR drop of this whole resistance.
[0027]
RF switch 30 of the present invention can respond to the input signal of the power level which increased at an advantageous thing. Thanks to the serial arrangement of an MOSFET transistor including a transistor group (33, 34, 37, and 38), the power signal which increased can be supplied to an RF input node (namely, input nodes 31 and 32), without having influence harmful to switching. The person skilled in the art of the transistor design field will be understood [that it can respond to a bigger input power level increasing the number of transistors for every transistor group, or by changing the physical configuration of a transistor, and]. For example, in one embodiment, the dimension of a transistor is about 0.5x2,100 micrometers. However, substitute composition can be used, without deviating from the range or the meaning of the present invention.
a silicon on insulator (SOI) -- PRIOR ART
As reference was made above in the description of the RF switch inFig.3, SOI technology is attractive in realization of an RF switch for insulation with a perfect insulating substrate. As everyone knows, a highly efficient microelectronics device is realized and SOI has mainly been used for the use which needs radiation resistance and high-speed operation. The junction wafer and silicon on sapphire which have the thin silicon layer joined to SIMOX and an insulating layer, for example are contained in SOI technology. In order to attain the above-mentioned desirable switch performance characteristic, in one embodiment, the RF switch of the present invention is manufactured on silicon on sapphire.
[0028]
In order to manufacture a device on an insulating substrate, it is necessary to use the effective method for forming a silicon CMOS device on an insulating substrate. It is well recognized by the advantage of using the composite board which contains single crystal semiconductor layers which carried out epitaxial deposition, such as silicon, in insulating supporting boards, such as sapphire, and these advantages, Using insulating materials, such as sapphire (aluminum$_2O_3$), a spinel, or a high insulating material of other well-known, as a substrate, when making it the electric conduction course of the leakage current between devices certainly pass a substrate, it is realizable.
[0029]
It can be defined as an "ideal" silicon on sapphire wafer containing a silicon layer without a defect in it with a perfect single crystal with sufficient thickness which can manufacture an active device. Probably this silicon layer adjoins an insulating substrate and the disorder of the crystalline lattice in a silicon insulator interface is the minimum. The early trial which is going to manufacture this "ideal" silicon on sapphire wafer suffered a setback for the problem for which many were conspicuous. these problems -- (1) -- the annealing of the silicon layer being carried out and the elevated temperature used for first epitaxial silicon deposition, and after that, The thing by which a contaminant, especially aluminum of a p type dopant enter into an epitaxial

deposited silicon layer considerably as a high temperature result used in order to decrease the defect in it and to do, (2) -- it can summarize as a crystal property with an insufficient epitaxial silicon layer when various elevated temperatures which devote themselves and pose a problem through the method of an annealing and/or re-growth are avoided. [and]

[0030]

Although it turns out that a quality silicon thin film suitable for the severe device use of a demand can be manufactured on silicon on sapphire, The annealing of the composite at the low-temperature ion implantation for embedding at epitaxial deposition of the silicon layer on silicon on sapphire and a silicon layer, and forming an amorphous region and the temperature below about 950 degrees C is contained in the method at this time.

[0031]

The example and method of manufacturing such a silicon on sapphire device are described in the following Descriptions. They, US,5,416,043,B Description ("minimum electric charge FET manufactured on a super-thin film silicon on sapphire wafer" (Minimum chargeFET fabricated on an ultrathin silicon)) on sapphire wafer, US,5,492,857,B Description ("high frequency wireless communication system on a single ultra-thin film silicon on sapphire chip" (High-frequency wireless communication system)) on asingle ultrathin silicon on sapphire chip, US,5,572,040,B Description ("high frequency wireless communication system on a single ultra-thin film silicon on sapphire chip" (High-frequency wirelesscommunication system)) on a single ultrathinsilicon on sapphire chip, US,5,596,205,B Description ("high frequency wireless communication system on a single ultra-thin film silicon on sapphire chip" (High-frequency wireless communicationsystem)) on a single ultrathin silicon on sapphire chip, US,5,600,169,B Description ("minimum electric charge FET manufactured on a super-thin film silicon on sapphire wafer" (Minimum charge FET fabricated on an ultrathin silicon)) on sapphire wafer, US,5,663,570,B Description ("high frequency wireless communication system on a single ultra-thin film silicon on sapphire chip" (High-frequency wireless communication system)) on a single ultrathin silicon on sapphire chip, US,5,861,336,B Description ("high frequency wireless communication system on a single ultra-thin film silicon on sapphire chip" (High-frequency wireless communication system)) on a single ultrathin silicon on sapphire chip, The US,5,863,823,B Description ("edge control in a silicon on insulator by which self align was carried out" (Self-aligned edge control in silicon on insulator)), US,5,883,396,B Description ("high frequency wireless communication system on a single ultra-thin film silicon on sapphire chip" (High-frequency wireless communication system)) on a single ultrathin silicon on sapphire chip, US,5,895,957,B Description ("minimum electric charge FET manufactured on a super-thin film silicon on sapphire wafer" (Minimum charge FET fabricated on an ultrathin silicon)) on sapphire wafer, US,5,920,233,B Description ("false side band) Phase-locked loop" Phase locked loop including a samplingcircuit for reducing spurious side band including the sampling circuit for decreasing, US,5,930,638,B Description ("how to manufacture low parasitic resistance on an ultra-thin silicon on insulator" (Method of making a low parastic resistor on ultrathin)) silicon on insulator, the US,5,973,363,B Description (on "ultra-thin silicon on insulator) The CMOS circuit which has the shortened P channel length" (CMOS circuitry with shortened P-channel length on ultrathin silicon on insulator), The US,5,973,382,B Description. ("The capacitor on the ultra-thin semiconductor on an insulator".) (Capacitor on ultrathin.) semiconductor on insulator and the US,6,057,555,B Description ("minimum electric charge FET manufactured on a super-thin film silicon on sapphire wafer" (High-frequency wireless)) It is communicationsystem on a single ultrathin silicon on sapphire chip. In the whole instruction about an ultra-thin silicon on sapphire

integrated circuit design and manufacture, all of these reference patents are used for this Description.

[0032]

An electron device can be formed in the silicon ultra-thin layer on an insulating synthesis sapphire wafer using the method described in the patent referred to above. Typically, silicon layer thickness is less than 150 nm. The advantage of insulating silicon on sapphire is maximized by such "ultra-thin" silicon layer, and it becomes possible to accumulate a many function on a single integrated circuit. With thick silicon, it is [the conventional transistor separation well needed] less necessary, transistor processing is simplified, and circuit density increases. In order to distinguish the method and device which were referred to by these above from a former thick silicon embodiment, in this Description, these are collectively called "ultra-thin silicon on sapphire."

[0033]

In some preferable embodiments of the present invention, a MOS transistor, US,5,416,043,B, No. 5,492,857, No. 5,572,040, No. 5,596,205, No. 5,600,169, No. 5,663,570, No. 5,861,336, No. 5,863,823, No. 5,883,396, It forms in ultra-thin silicon on sapphire by the method disclosed in each Description of No. 5,895,957, No. 5,920,233, No. 5,930,638, No. 5,973,363, No. 5,973,382, and No. 6,057,555. However, the method of other well-known which manufactures an ultra-thin silicon on sapphire integrated circuit can be used, without deviating from the meaning or the range of the present invention.

[0034]

A quality silicon thin film suitable for the severe device use of a demand as claim for patent is described and carried out to these patents, It can manufacture on an insulating substrate by the method containing the annealing of the low-temperature ion implantation for embedding at epitaxial deposition of the silicon layer to an insulating-substrate top, and a silicon layer, and forming AMORUFASU, and the composite in the temperature below about 950 degrees C. Any processings which expose a silicon layer to the temperature over about 950 degrees C are carried out in oxidation ambient environment. There is area density of an active state to the region which was not intentional to the silicon thin film which forms a transistor, and was doped electrically [less than abbreviation $5x10^{11}cm^{-2}$].

[0035]

As reference was made above, a UTSi substrate is desirable for especially RF use. A perfect insulating substrate is because the harmful influence of the substrate combination relevant to the conventional substrate (that is, it is not completely insulation) is decreased. As a result, RF switch 30 of Fig.3 is manufactured on a UTSi substrate by one embodiment.

RF switch design trade-off

When designing RF switch 30 of the present invention described above in relation to Fig.3 and realizing, some design parameters and a trade-off should be taken into consideration. The RF switch of the present invention can be prepared so that it may exceed whether a desired system design demand and RF switch performance objective are filled. It describes here about the design trade-off and the thing which should be taken into consideration which affect an RF switch design.

[0036]

As it described above in relation to Fig.3, RF switch 30 is realized using an MOSFET transistor, although "N type" or "P type" may be used. However, in order to realize an RF switch in a CMOS technology, N channel transistor is preferable. It is because one with preferable N

channel transistor has "ON" resistance of N channel transistor much smaller than the case of P channel transistor to fixed transistor size. This is because the mobility in electronic silicon is high to an electron hole. Control voltage is chosen so that the on resistance of an "on-" transistor may decrease reliably. the time of an "off-" transistor being made non-operative again as for control voltage -- reliably -- OFF and ****** -- it chooses like.

[0037]

In the transistor design field, "ON" resistance is in inverse proportion to the difference between the voltage applied to a transistor gate, and the voltage applied to a transistor source in an N-channel metal oxide semiconductor transistor as everyone knows. This voltage is usually called "Vgs" (gate source voltage). Although it is noticing easily, In an input port (for example, first RF input node 31 in Fig.3), Therefore, as the size of an RF signal (Vs) increases in the RF common port 35, Vgs of an on-transistor decreases (for example, Vgs of transistor $M33_A$ in the switching transistor group 33 decreases as the size of RF1 signal increases). For this reason, it becomes saying that gate control voltage (for example, SW of input node 33') should as just as possible be carried out. However, though regrettable, the degree which can just do gate control voltage is restricted due to concern of reliability.

[0038]

The same concern exists also to an "off-" transistor. It is important to note that an RF input signal (for example, RF1 input signal) generally vibrates involving zero reference voltage in application of a typical RF switch. The off-transistor (for example, the shunt transistor group's 37 transistor) must remain in as at non-operative or a turn-off between the voltage deviation of an RF input signal positive and negative. From this, it will be said that gate control voltage (for example, SW_control voltage signal) of an off-transistor should be made negative as much as possible. Again, the degree as for which gate control voltage is made negative is restricted due to concern of reliability.

[0039]

The 1-dB compression point of a switch is restricted by the design of an off-transistor for a CMOS switch again. In the transistor design field, there is breakdown voltage fundamental between the source and drain by a MOS transistor as everyone knows. If the electric potential of device both ends exceeds this breakdown voltage, even when the gate potential which is going to maintain the transistor to the OFF state exists, high electric current flows between a source and a drain. an improvement of the compression in a switch increases the breakdown voltage of a transistor -- it can attain. One of the methods which manufactures the MOS transistor which has high breakdown voltage is increasing gate length. Regrettably, by the increase in gate length, the channel resistance of a device increases also inconvenient and, thereby, the insertion loss of a device increases. Although the channel resistance can decrease by making width of a device wide, this makes switch separation be deteriorated again. Therefore, a trade-off exists in a MOS switch.

[0040]

As it described above in relation to RF switch 30 of the present invention in Fig.3, a transistor is laminated to series constitution and the 1-dB compression point of a switch is improved. The effective breakdown voltage of the whole series-connection transistor is increased with the combination of the comparatively high gate resistance machine of a value, and the laminated constitution of the transistor in a transistor group. It is made for a RC time constant (the resistance of a gate resistance machine and the gate capacitance of MOSFET determine) to become much longer than the cycle of the RF signal which RF switch 30 processes in a design

and manufacture of a switch element. As mentioned above, it increases by one n times the rate [laminated constitution and / in / as a net effect of the gate resistance machine of high resistance / comparatively / in the breakdown voltage of the whole series-connection transistor / an individual transistor] of breakdown voltage (here). n is equal to the number of the transistors connected to series in a transistor group.

[0041]

What should be further taken into consideration on a design is related with the "body tie" currently used in the conventional bulk CMOS transistor. In the transistor design field, a body tie combines a device with either a well or a substrate as everyone knows. The well substrate junction must always keep reverse bias applied. A source body and the drain body junction must always keep reverse bias applied. Generally, a well (N well technology) is combined with the greatest electropositive potential applied to a circuit in a bulk CMOS design. A substrate (P well technology) is combined with the greatest electronegative potential applied to a circuit. Since an RF input signal vibrates the upper and lower sides of a ground symmetrically, a CMOS switch design shows insufficient performance about insertion loss, separation, and a 1-dB compression point. It is preferable to realize RF switch 30 of the present invention on an insulating substrate for these and the above-mentioned Reason.

[0042]

By realizing the RF switch of the present invention on an insulating substrate, some advantages, such as an improvement of switch separation and reduction of insertion loss, are provided. The further advantage is acquired by realizing the RF switch of the present invention using UTSi technology. For example, as compared with realizing the RF switch of the advanced technology to GaAs, the improvement of the integrated circuit yield, reduction of a manufacturing cost, and the increase in an accumulation level are attained by using UTSi. In the integrated circuit design field, GaAs are not fit for integration of a high level as everyone knows. therefore, the digital control circuit relevant to operation and the function of the RF switch and other circuits (a negative voltage electric power supply generator circuit --) The level shift circuit, the low current voltage divider circuit, the RF buffer circuit, etc. must often realize with an off-chip (that is, these functions are easily [as an RF switch] umaccumulable). This is connected to the degradation of the RF switch realized with an increase in cost and the advanced technology.

[0043]

By contrast, according to invention of this RF switch, a circuit required for normal operation of an RF switch and a function is realizable for the same integrated circuit as the switch itself together using UTSi technology. For example, an RF switch is accumulable on the same integrated circuit by realizing an RF switch with UTSi technology with a CMOS control logic circuit required to control operation of a negative voltage generator and an RF switch so that it may describe in detail by the following. Thanks to reduction of the control line required to control operation of a switch, the complexity of an RF switch also decreases. An RF switch control logic circuit is realizable for an advantageous thing using a low-voltage CMOS transistor. Even if it is for high power RF switch realization, electric power can be comparatively supplied to the RF switch of the present invention using the external power of low electric power. These characteristics are advantageous as compared with realization of GaAs by the advanced technology. It is because it is required to use a power generation circuit required to realize an electric power supply the external power of high power, positive, and negative [both] comparatively in the case of GaAs. For example, in the illustration embodiment described below in relation to Fig.4 - 12, the RF switch of the present invention only needs one 3V single external

power. In the switch by the advanced technology, the external voltage generation circuit for realizing at least one 6V external power and a positive and negative electric power supply is required typically.

The RF switch integrated completely

To Fig.4, it manufactures according to the present invention, and it is illustration-like and the simple block diagram of RF switch 100 integrated completely is shown. As shown in Fig.4, to RF switch 100 integrated completely, The RF switch 30(simplified schematic representation shows Fig.4)CMOS control logic circuit 110 and the negative voltage generator circuit 120 (in one embodiment, it realizes using a "charge pump" circuit) of the present invention which were described by Fig.3 in the above are included.The control signal 130 is input CMOS logic circuit block 110. The control signal 130 will have it understood from 0 volt in one embodiment that other logic circuit levels can be used, without the person skilled in the art of the digital logic circuit design field deviating from the range or the meaning of the present invention in the range of +Vdd. For the Reason shown above, RF switch 100 integrated completely is manufactured on a UTSi substrate at one embodiment. However, other insulating-substrate technology can also be used.

[0044]

Some the functions and the characteristics which are not in the RF switch of the advanced technology in Fig.2 are included in RF switch 100 integrated completely so that it may describe in detail by the following. For example, RF switch 30 (as it described above in relation to Fig.3) of the present invention In addition, a negative voltage generator and an RF switch control facility are accumulated together on the same integrated circuit as the switch of the present invention with RF switch 100 integrated completely using new lamination and gate-transistors (gate resistance) composition of a transistor. To RF switch 100 integrated completely, so that it may describe in detail by the following, The built-in type oscillator which supplies a clock input signal to a charge pump circuit, the integration charge pump circuit which generates the negative power supply voltage which other RF switching circuits need, The gate drain of the CMOS logic circuit which generates the control signal which controls RF switch transistor, and a switch transistor, a gate source, and drain source voltage by decreasing, The RF buffer circuit which separates RF signal energy from the level shift circuit to which reliability is made to increase, a charge pump circuit, and a digital control logic circuit is included. Each of these circuits are described in detail by the following with reference to related figures.

A 1st embodiment of a negative voltage generator-charge pump

As shown in Fig.4, the negative voltage generator 120, i.e., a charge pump, is contained in one embodiment of RF switch 100 integrated completely. The negative power supply voltage (it is hereafter described as "-Vdd") which other circuits of RF switch 100 integrated completely need with the negative voltage generator 120 is generated. The two input sets (Vdd) 122, i.e., a positive DC-power-supply-voltage signal, and the clocked into (shown in a figure as a single input signal "Clk") 124 are supplied to the negative voltage generator 120. Although Fig.4 has shown the clocked into 124 as a single input signal, by some embodiments of the RF switch in the present invention, the clocked into 124 can include the clock input signal exceeding two or it so that it may describe in relation to Fig.5 b below.

[0045]

In the embodiment shown in Fig.4, direct-current 3V power supply source is included in the positive service voltage which is an input to the negative voltage generator circuit 120. However, other electric power supply levels may be used, without deviating from the range or the meaning

of the present invention. For example, if it is a request, a positive electric power supply with the sufficient direct current 3.5V, the direct current 5V, or other arbitrary convenience can be considered as the input to the negative voltage generator circuit 120 of Fig.4. Typically, a positive electric power supply signal is generated with an external low-electric-power supply source.

[0046]

In one embodiment of the present invention, the negative voltage generator 120 of Fig.4 is realized using a charge pump circuit. The simple block diagram of one illustration embodiment in the negative voltage generator 120 of Fig.4 is shown in Fig.5 a.As shown in the simple block diagram of Fig.5 a, the oscillator 202, the clock generation machine circuit 204, and the charge pump circuit 206 of the present invention are included in a negative voltage generator. The output of the oscillator 202 is input into the clock generation machine circuit 204. The output of the clock generation machine circuit 204 is input into the charge pump circuit 206. The negative power supply voltage which other circuits of RF switch 100 integrated completely use with the negative voltage generator 120 is supplied.

[0047]

The negative power supply voltage must be generated to an RF switching circuit in a disadvantageous thing in an external circuit in many of RF switches by the advanced technology. In realization of other RF switches, joint approach required in order to shift the direct-current value of an RF input signal to the halfway point of the applied bias voltage is used. In this approach, generally, since an FET gate drive becomes half effectively because of this level shift, it is necessary to apply comparatively high bias voltage. Negative influence is brought to switch insertion loss by this when not increasing bias voltage. It is because gate drives decrease in number by this and FET channel resistance increases by it.

[0048]

In order to cope with these problems, in one embodiment of RF switch 100 integrated completely, the charge pump circuit 206 of the present invention shown in detail is used for Fig.5 b. As shown in Fig.5 b, two P channel MOS FET transistors 208 and 210 are contained in the first embodiment of the charge pump circuit 206, and these are connected to two N-channel metal oxide semiconductor FET transistors 212 and 214 in series at it. The left leg (the first P channel transistor 208 connected to the first N channel transistor 212 in series is included) of the charge pump circuit 206, First capacitor Cp216 is used for the right leg (the second P channel transistor 210 connected to the second N channel transistor 214 in series is included) of a charge pump circuit, and it is combined with it. The source of the second N channel transistor 214 is combined with the illustrated second capacitor C218 which is an output capacitor like. Two non-overlapping clock control signals "Clk1" and "Clk2" are used in order to control operation of the transistors 208, 210, 212, and 214. For example, reverse "Clk1_" of "Clk1" controls the gate of the P channel transistors 208 and 210 to be shown in Fig.5 b. The non-overlapping clock control signal "Clk2" of another side controls the gate of the N channel transistors 212 and 214 like a graphic display.

[0049]

The charge pump 206 generates negative power supply voltage (-Vdd) by using the non-overlapping clock control signals Clk1 and Clk2 which drive a transistor gate, and charging and discharging alternately two capacitors (Cp216 and output capacitor C218). Negative power-supply-voltage-Vdd is generated from the electric charge which charged the capacitor C218. According to one embodiment, the train of impulses (that is, a train of impulses is input as the

clock input signals Clk1 and Clk2) which drives a charge pump is generated using a pulse shift circuit (not shown). Since a train of impulses is applied to the charge pump 206, capacitor Cp216 is applied in the positive electric power supply Vdd, then, is discharged by the counter direction over the capacitor C218, and generates negative power-supply-voltage-Vdd. No transistor of a charge pump needs to avoid the thing exceeding Vdd also between which source / drain node, therefore the reliability of the charge pump 206 increases dramatically.
[0050]
In one embodiment of the charge pump circuit 206 of the present invention, the capacitance of the output C218 is about 200 pF, and the capacitance of Cp216 is about 50 pF. The person skilled in the art of the charge pump design field will be understood [that other capacitance values can be used and], without deviating from the range or the meaning of the present invention.
As shown in the simple block diagram of Fig.5 a, in one embodiment, two non-overlapping clock signals are derived from the oscillation signal which the internal oscillator 202 generates. As shown in Fig.5 a, the oscillator 202 inputs an oscillation signal into the clock generation machine circuit 204, and generates shortly two non-overlapping clock signals with which this circuit controls a charge pump transistor gate (by the arbitrary and useful well-known method). According to one embodiment of RF switch 100 with which the present invention was integrated completely, the oscillator of a low frequency wave is contained comparatively (several MHz order) in the oscillator 202. According to this embodiment, an easy relaxation oscillator is contained in an oscillator. however, the person skilled in the art of the integrated circuit field is understood [that the present invention can be carried out using the oscillator of other types, and], without deviating from the meaning or the range of the present invention -- I will come out.
[0051]
The voltage swing of the two non-overlapping clock signals Clk1 and Clk2 which changes to Fig.5 c temporally is shown. As shown in Fig.5 c, two non-overlapping clock signals change by the voltage swing from -Vdd to Vdd. In one embodiment, a clock signal changes from direct-current-3V to direct-current+3V. The efficiency of the charge pump 206 is improved by adjusting in this way.
[0052]
The N channel (212 and 214) and P channel (208 and 210) device of a single threshold value are contained in being advantageous to the charge pump transistors 208, 210, 212, and 214. The conventional charge pump circuit needs use of two or more threshold level device. Therefore, in order to have realized the thing of these former, rather than the charge pump circuit 206 of the present invention in Fig.5 b, the design was complicated and cost started. In one embodiment of the charge pump 206 of the present invention, the width of the P channel transistors 208 and 210 is about 20 micrometers, and length is about 0.8 micrometer. The width of the N channel transistors 212 and 214 is about 8 micrometers, and length is about 0.8 micrometer. The person skilled in the art of the integrated circuit design field will be understood [that the transistor of other dimensions can be used, and], without deviating from the range or the meaning of the present invention. The charge pump circuit 206 of the present invention is dramatically efficient, and operates perfect in spite of change of temperature and a process.
Level shift circuit
Since a charge pump circuit doubles efficiently the power supply voltage applied to this circuit, it must pay attention to the integrity problems of electric potential relevant to such high voltage. In order to realize a charge pump by a method which improves the reliability of a transistor, a level

shift circuit is used and the gate source voltage, gate drain voltage, and drain source voltage of a transistor are restricted to a permissible level.

[0053]

The invention level shift circuit 300 created according to the present invention is shown in Fig.6 a. Using the level shift circuit 300, an "ordinary" digital input signal [typical or] (a digital signal ranges from a ground (GND) to the range of +Vdd typically) is converted or shifted so that the range of -Vdd to +Vdd may be attained to. Thereby, the reliability of the RF switch integrated completely increases. Although a control signal is shifted to the range of direct-current-3V to direct-current+3V, the person skilled in the art of the RF switch control field will have it understood in one embodiment of the present invention, without deviating from the meaning or the range of the present invention that other level-shifted-voltages ranges can be used.

[0054]

As shown in Fig.6 a, two or more inverters combined with feedback structure are contained in the level shift circuit 300 (henceforth, it is called the level shifter 300) of the present invention. Especially in the embodiment shown in Fig.6 a, to the level shifter 300, Two groups' inverter is contained and "out of the 1st and the shifted second output signal 314, i.e., a first output node," and its reverse "out_" of the second output node 316 are generated using these inverters. The inverters 302, 304, and 304 are contained in a first inverter group. The inverters 308, 310, and 312 are contained in a second inverter group. An "ordinary" digital input signal [typical or] (namely, digital input signal covering the range of GND to +Vdd) is the input node 318 of the first inverter 320, and is input into the level shifter 300. The first inverter 320 generates the first input signal "in" (with output node 324), and this signal is input into the second inverter 322. The second inverter 322 generates the second input signal "in_" which is the reverse of a first input signal "in" in the output node 326. Therefore, the 1st and the second inverters 320 and 322 generate the signal input into the two above-mentioned inverter groups. For example, the first input signal "in" is combined with the input part 328 of the inverter 302. Similarly, the second input signal "in_" is combined with the input part 330 of the inverter 308.

[0055]

It is generated by the first output inverters 306 and a first inverter group's output "out" is supplied to the first output node 314. It is generated by the second output inverters 312 and a second inverter group's output "out_" is supplied to the second output node 316. Two level-shifter outputs "out" and out_" are input into other circuits of RF switch 100 with which Fig.4 was integrated completely. For example, in one embodiment a first output "out", It is combined with the gate of the device in the switching transistor group 33 and the shunt transistor group 38 (). Namely, the "out" signal in the first output node 314 of Fig.6 a, It is combined with the "SW" control input signal of Fig.3, and this controls operation of the switching transistor group 33 and the shunt transistor group 38 by input node 33' and 38', as it described above in relation to Fig.3. Similarly, it is combined with "SW_" control input signal of Fig.3 (with input node 34' and 38'), and, thereby, a second level-shifter output "out_" controls the switching transistor group 34 and the shunt transistor group 37 by this embodiment as mentioned above.

The level shifter 300 of Fig.6 a shifts the direct current level of an input signal (namely, input signal supplied by the input node 318), and, on the other hand, makes the frequency response of an input signal eternal. The level shifter 300 uses sufficiently the floating technology provided by realization by the silicon on insulator substrate of RF switch 100 integrated completely. The inverter of the level shifter 300 operates based on differential bias. That is, a level shifter shifts a

digital input signal based on the difference between two voltage signals. As long as the difference between the electric power supply signals especially supplied to inverters (for example, output inverters 306 and 312 etc.) is the order of Vdd, the level shifter 300 functions reliably and shifts an input signal in the range between -Vdd and +Vdd. In one embodiment, Vdd is equal to the direct current 3V. In this embodiment, the voltage applied between those sources / drain nodes does not become larger than the direct current 3V with the transistor which constitutes the inverter (for example, output inverters 306 and 312) of the level shifter 300. The reliability of a transistor device increases by this.

[0056]

If Fig.6 a is referred to again, a level shifter will shift a digital input signal from -Vdd to the voltage level of the range of +Vdd using a feedback method. In particular, a second inverter group's (308, 310, and 312) output (namely, "out_" signal) in the second output node 316 is supplied as feedback to a first inverter group's input part by the input part of the inverter 304. Similarly, a first inverter group's (302, 304, and 306) output (namely, "out" output signal) in the first output node 314 is supplied as an input to a second inverter group, especially the inverter 310.

[0057]

When the digital input signal in the input node 318 will be in a state logically "high" (that is, in some embodiments) When an input signal changes from GND to +Vdd, it swerves and the "in" signal (it can set to the node 324) and "in_" signal (it can set to the node 326) are set to a ** leg round (for example, direct current 0V) and Vdd (for example, direct current 3V). The "out" signal of the first output node 314 is set to +Vdd. Simultaneously, the "out_" signal of the second output node 316 is set to -Vdd. ("out" which acts as feedforward to the input part of "out_" fed back to the input part of the inverter 304, and the inverter 310) By feedback composition, quick change of the state in the level shifter 300 is carried out reliably. The level shifter 300 works similarly, when an input signal changes in the low state logically from a high state (from +Vdd to namely, GND transition). If the digital input signal of the input node 318 will be in a state logically "low", the "in" signal (it can set to the node 324) and "in_" signal (it can set to the node 326) will become Vdd (for example, direct current 3V) and a ground, respectively. The "out" signal in the first output node 314 is set to -Vdd. Simultaneously, the "out_" signal in the second output node 316 is set to +Vdd. By feedback, quick change of the state in the level shifter 300 is carried out reliably again. According to grounding, the descent more than perfect Vdd voltage between the source / drain node in the MOSFET transistor of an inverter is reliably lost in a level-shifter inverter.

[0058]

One embodiment of the inverter (for example, inverters 302, 304, and 306) used for Fig.6 b in order to realize the level shifter 300 of Fig.6 a is shown. As shown in Fig.6 b, two MOSFET devices 342, i.e., P channel transistor, and the N channel transistor 344 are contained in the inverter 340. These devices are controlled by the illustrated input signal which is connected in series, combines the gate both, and is supplied to the input node 346 like. The source of the P channel transistor 342 is the node 350, and it is combined to first power supply voltage, and on the other hand, N channel transistor 344 source is the node 352, and is combined to second power supply voltage. It is combined, and both the illustrated drains that are devices like are the output nodes 348, and generate the output of an inverter. In one embodiment of the inverter 340 of the present invention, the P channel transistor 342 is 5 micrometers in width, and is 0 or 8 micrometers in length. In this embodiment, N channel transistor is 2 micrometers in width, and is

0.8 micrometer in length. The person skilled in the art of the transistor design field will be understood [that the thing of other physical sizes can be used as a transistor of the inverter 340, and], without deviating from the range or the meaning of the present invention. The logical expression of the inverter 340 is shown as the sign 360 in Fig.6 b again.

[0059]

Thus, by using the level shifter 300 of the present invention, the digital input signal which attains to the range of GND to +Vdd at the beginning is shifted so that the range of -Vdd to +Vdd may be attained to. The corresponding output signal which the level shifter 300 of the plot of a digital input signal of a voltage swing versus time and the present invention of Fig.6 a generates in Fig.7 a is shown. As shown in Fig.7 a, a digital input signal ranges from a ground or the direct current 0V to the range of Vdd. The output of the level shifter 300 of the present invention attains to the range of -Vdd to +Vdd. As for an input signal, according to one embodiment of the RF switch in the present invention, the output of the level shifter 300 ranges from the direct current 0V to the range of direct-current-3V to direct-current+3V in the range of direct-current+3V. The power supply voltage of other values can be used without deviating from the range or the meaning of the present invention. For example, in one embodiment, an input signal can be made into the range of the direct current 4V from 0 to direct-current+3.5V, or 0. According to this embodiment, a level shifter shifts a signal to direct-current+3.5(or +4)V from direct-current-3.5(or -4)V.

[0060]

The simple logical symbols of the level shifter 300 of the present invention in Fig.6 a are shown in Fig.7 b. These logical symbols are used with next Drawings. As shown in Fig.7 b, a digital input signal is supplied by the input node 318 (the same input node 318 as having described above in relation to Fig.6 a). The level shifter 300 supplies reverse "two shifted outputs, i.e., "out", and out_" of those. These outputs are supplied by the output nodes 314 and 316 (the same output nodes 314 and 316 as having described above in relation to Fig.6 a), respectively.

RF buffer circuit

Fig.8 a is an electric figure of the two-step level-shifter buffer circuit 400. Fig.8 b is a simple block diagram of an interface to a digital control input and the buffer circuit 400. The 1st step level shifter 300 and the 2nd step RF buffer circuit 402 are included in the two-step level shifter and the RF buffer circuit 400 of Fig.8 a. The 1st step level shifter 300 is the same as that of what was described above in relation to Fig.6 a, and 6b, 7a and 7b, therefore it does not carry out describing in details more here. The level-shifter stage 300 shifts the logical level of a digital control signal, and it is made to attain to the range of -Vdd to +Vdd, as described above. The RF buffer circuit 402 is included in the 2nd step of the circuit 400. The RF buffer circuit 402 performs only the role of a driver (an RF buffer circuit does not perform a level shift).

[0061]

An RF buffer separates electrically digital control signals (what the CMOS logical block 110 of Fig.4 generates) from RF switch 30 described above in relation to Fig.3.RF buffer 402 functions as inhibiting the sag of the control voltage (although it is SW and SW_, this Description and Fig.8 a shows as a control signal "out" and "out_" again, respectively) which controls the operation of a transistor and un-operating in RF switch 30. RF buffer 402 functions as a big-electric-power RF signal preventing combining with a negative electric power supply (namely, -Vdd) again so that it may describe in detail by the following. As it described above in relation to Fig.5 a - 5c, the charge pump circuit 206 generates this negative electric power supply. The extent of the big-electric-power RF signal in RF switch 30 carries out RF combination at the

negative electric power supply which the charge pump 206 (Fig.5) generates, and, thereby, especially RF buffer 402 protects that current carries out drainage from a negative electric power supply.
[0062]
When the RF input signal of big electric power is extremely input into RF switch 30 of the present invention, in order to separate a digital logic signal from an RF switch, when the buffer circuit is not used, combination of an RF signal and a digital logic signal takes place. RF combination may have harmful influence on an RF transistor control signal (SW and SW_), and usually has harmful influence. For example, when the RF input signal of order of about 30 dB is input into 1-W RF switch 30, there is a possibility that the voltage oscillation of a zero mark bolt will happen by a digital control line, by RF combination. This is because an RF signal is fed back to a digital control circuit from an RF switch. This RF joint effect may have bad influence on an RF transistor group's operation and non-operativeness, therefore normal operation of RF switch 30. The buffer circuit 402 of Fig.8 a protects the joint effect.
[0063]
As shown in Fig.8 a, in composition, the buffer circuit 402 of the present invention resembles dramatically the level shifter 300 which was described above as the 1st step of the two stage circuits 400, and was illustrated. Two inverter groups (404, 406, and 408), i.e., a first inverter group, and a second inverter group (410, 412, and 414) are contained in RF buffer 402 like the level shifter 300. It is generated by the first output inverters 408, and, by a diagram, the first inverter group's (404, 406, and 408) output has attached the code of "out", and is supplied by the first output node 416. It is generated by the second output inverters 414, and the second inverter group's (410, 412, and 414) output has attached the code of "out_", and is supplied by the second output node 418. The output signal "out_" is the reverse of an output signal "out."
[0064]
feedback is used for the level shifter 300 of the 1st step although it is important -- a level shift function -- performing (it described in relation to Fig.6 a -- as) -- the RF buffer circuit 402 does not feed back the output signal to an input. As a result, the digital input signal (namely, control input signal input into the level shifter 300 by the nodes 328 and 330) input into the 1st step, It separates from the output signal (that is, it is a control-output signal "out" of the output nodes 416 and 418, and its reverse "out_", and combined with SW and SW_controlling signal line, respectively) used in order to control RF switch transistor.
[0065]
If Fig.8 a is referred to again, especially the level shifter 300 will input a digital control signal "in" and its reverse signal "in_" by the nodes 328 and 330, respectively (in relation to Fig.6 a, it described in detail by the above like). The first output "out1" of the level shifter 300 in the output node 314 is fed back to the input part of the inverter 310 like a graphic display. Similarly, the second output "out1_" of the level shifter 300 in the output node 316 is fed back to the input part of the inverter 304. That as mentioned above, RF combination (that is, a level-shifter output signal piles up an RF signal on it) takes place because of this feedback topology, It is a case where the output signal of a level shifter is used in order to control RF switch transistor directly (namely, when there is no buffer circuit 402). Therefore, the RF buffer circuit 402 of the present invention is used without feedback of an output signal, and separates an input signal (namely, a digital input signal "in" and "in_") from the RF signal which exists in an RF switch. As shown in Fig.8 a, the first output signal "out1" of the level shifter 300 is input into the inverters 404 and 406 of an RF buffer circuit. Similarly, the second output signal "out1_" of the level shifter 300 is

input into the inverters 410 and 412 of a buffer circuit. Two control outputs ("out" and "out_") of the RF buffer circuit 402 are not supplied as feedback to a level shifter, although it controls the operation of a transistor and un-operating in an RF switch. Therefore, an improvement of separation between an RF switch and a digital logic circuit is attained.

[0066]

In one embodiment, the inverter 340 described above in relation to Fig.6 b is contained in the inverter which realizes a two-step level shifter and the RF buffer circuit 400. However, the person skilled in the art of the inverter design field will have it understood that the two stage circuits 400 are realizable, without deviating from the range or the meaning of the present invention using a substitute inverter design. In one embodiment, the transistor used in order to realize the 1st step level shifter 300 is more nearly physically [than the transistor used in order to realize the 2nd step RF buffer circuit 402] small. The transistor of a bigger dimension is used in the RF buffer circuit 402, in order to attain efficient amplification of a control signal. For example, in one embodiment, the amplification whose width is those with 3 times, as a result about 3 times the current is brought about rather than the transistor used in order that the transistor used in order to realize an RF buffer may realize the level shifter 300. The person skilled in the art of the transistor design field will be understood [that the transistor of other convenient dimensions can be used, and] in order to attain any desirable amplification in a digital control signal.

The voltage divider used in the alternative level shift circuit of the present invention

Fig.9 a is an electric figure of one embodiment in the low current voltage divider ("LCVD") circuit 500. This circuit is used by the feedback path of one embodiment in the level shifter 300 described above in relation to Fig.6 a. The simple logical symbols used since the voltage divider 500 of Fig.9 a is expressed to Fig.9 b are shown. The voltage divider 500 is used by one embodiment, and the potential gate oxide integrity problems relevant to the excessive voltage oscillation of the whole gate oxide of a feedback inverter transistor are tackled. Various source drain voltage of MOSFET used in order to realize a level shifter, as it described above in relation to the level shifter 300, Although bigger voltage than Vdd never is not applied, the output (namely, an output signal "out" and "out_") of a level shifter, since 2xVdd may also vibrate from -Vdd to +Vdd namely,, the gate oxide of the feedback inverters 304 and 310 may be applied in the voltage of 2xVdd. These feedback voltage levels are applied to the whole gate oxide of the feedback inverters 304 and 310, and gate oxide integrity problems may produce them as a result.

[0067]

In order to be able to avoid gate oxide integrity problems, the maximum voltage applied to the whole gate oxide of the feedback inverters 304 and 310 is reliably reduced substantially to Vdd (not being the gate oxide voltage of 2xVdd). Therefore, in one embodiment in the RF switch with which the present invention was integrated completely, the voltage divider of Fig.9 a restricts the voltage applied to the gate of the level-shifter feedback inverters 304 and 310. In this embodiment, the output (namely, each output "out" and "out_" in the output nodes 314 and 316) of a level shifter, Instead of feeding back to the feedback inverter shown in the level shifter of each Fig.6 a directly, first, a level-shifter output signal is adjusted with the voltage divider 500 of Fig.9 a, and is fed back to a feedback inverter after that. The voltage applied to the gate oxide of the feedback inverters 304 and 310 reliably with the voltage divider 500 so that it may describe in detail by the following, It is made not to exceed the sum total (a voltage drop is the number of transistors and the function of transistor threshold voltage which are used in order to realize the voltage divider 500) of Vdd and a small voltage drop. In one embodiment, Vdd is the direct

current 3V and a voltage drop is the direct current 0.9V. According to this embodiment, it becomes reliably that a gate oxide is never applied in the voltage exceeding the direct-current abbreviation 3.9V (that is, a feedback inverter is applied in the voltage covering the range of the direct current 0.9V from direct-current-3V), thanks to the voltage divider 500.
[0068]
two or more MOSFET devices (502, 504, 506, and 508) combined with both the voltage dividers 500 by series constitution (namely, -- being illustrated -- it puts on a mutual top by source drain arrangement like) when Fig.9 a was referred to here -- it is contained. According to both one embodiments, the gate and drain of MOSFETs 502, 504, 506, and 508 joined together, and have realized the lamination diode. Although MOSFET which realizes a diode is henceforth called a "diode device", these are laminated in series like a graphic display. MOSFETM3 (510) and output MOSFETM2 (512) are contained in the voltage divider 500 again. The function of these two transistors is described more in details below.
[0069]
A diode device is used and the partial pressure of the voltage of the input signal supplied to the voltage divider 500 by the input node 514 is carried out. As shown in Fig.9 a, the signal by which a partial pressure is carried out to the voltage divider 500 is supplied to the drain (and gate connected) of the first device 502 as an input. when an input signal exceeds a positive voltage level once (nxVthn), "n" is the number of the diode devices used in order to realize the voltage divider 500 here -- Vthn -- the threshold voltage (namely, "diode descent" to a source from the drain of a device) of a device -- but, A diode device (502, 504, 506, and 508) begins to conduct a lot of current. the embodiment shown in Fig.9 a -- n= 4 and Vthn= -- 0.7 volt of alternative values can be but used to "n" and Vthn, without deviating from the range or the meaning of the present invention. For example, in other embodiments, by changing the number of the diode devices used in order to realize the voltage divider 500, the input signal supplied to a voltage divider is arbitrary, and can be restricted to a desired voltage level (namely, thing for which the value of "n" is changed). According to the embodiment shown in Fig.9 a, once input voltage exceeds the voltage level of (4x0.7), i.e., 2.8 volts, a lamination diode device will begin to conduct briskly.
[0070]
The ballast-resistances machine R516 is connected to the source of the output diode device 508 like a graphic display. Once a diode device carries out turn-on completely, any additional input voltage which exceeds the value of nxVthn for the ballast-resistances machine R516 will descend. According to the embodiment shown in Fig.9 a, any additional input voltage which exceeds the value of (the input voltage - (4xVthn)) for the ballast-resistances machine R516 descends. The output of the voltage divider 500 is pulled out from the gate drain to which the output diode device 508 was connected. The output signal by which the partial pressure was carried out is supplied by the output node 520. It is guaranteed for the voltage which descends by the diode drop of the diode devices 502, 504, and 506, and the ballast-resistances machine R516 whole that the output of the output node 520 substantially (input voltage - (3xVthn)) never exceeds. about [Vthn=] -- about [0.7V and] -- the output node 520 never exceeds (direct-current 3V- (3x direct current 0.7V)) 0.9V, i.e., a direct current, to the maximum input voltage of 3V. Thus, in the embodiment shown in Fig.9 a, the voltage divider 500 restricts the output of the output node 520 to the range of direct-current-3V to direct-current+0.9V to the input voltage which attains to the range between direct-current-3V and direct-current+3V.
[0071]

Output MOSFETM2 (512) is constituted as a capacitor, and it is used in order to support acceleration of the switching time of the voltage divider 500. When an input reaches negative potential, MOSFETM3 (510) carries out reliably that the output node 520 vibrates to the electric potential of the input signal in the input node 514. This is attained when an input signal reaches negative potential, and the device M3 (510) carries out turn-on. Therefore, when an input signal becomes -Vdd electric potential (for example, direct-current-3V), the output signal of the output node 520 is also set to -Vdd. The output device 508 can apply reverse bias during negative voltage vibration of an input signal, and, thereby, becomes trustworthy [that a direct current does not carry out drainage from a negative power supply source] during negative voltage vibration of an input signal. When the output of a voltage divider is direct-current abbreviation-3V, the voltage divider 500 does not draw current near at all. This is important. Current is direct-current-3V and it is because the charge pump circuit described above in relation to Fig.5 b is made to discharge. When the output of a voltage divider is about 0.9v and the ballast-resistances machine R516 is chosen comparatively largely, there is comparatively little current which can be drawn near. However, since the current in this case is produced between positive voltage (0.9V) and a ground, charge pump current additional for operation of the voltage divider 500 of Fig.9 a is not sent.

[0072]

In one embodiment, the value of the ballast-resistances machine R516 is 100komega. In one embodiment, all the devices of the voltage divider 500 are the same length. For example, in one embodiment, all the devices are 0.8 micrometer in length. In one embodiment, the physical size of all the diode devices (502, 504, 506, and 508) is the same. In one embodiment, each diode device is 2 micrometers in width, and the device M3 (510) is the 2 micrometers with same width, and output MOSFETM2 (512) is 14 micrometers in width. the person skilled in the art of the integrated circuit design field is understood [that other values and alternative composition can be used and] to the device shown in Fig.9 a, without deviating from the range or the meaning of the present invention -- I will come out. for example, the person skilled in the art of the electric circuit design field in lamination of changing the number of diode elements "n", changing the value of Vthn, or a diode device, The output node 520 is pulled out on a different point (for example, like a graphic display). Instead of pulling out from the drain of the device 508, other voltage divider output levels will have it understood by what an output is pulled out for from the drain of the diode device 506 or 504 that it can adjust easily.

The correction level shifter using a voltage divider

By decreasing the voltage applied to the gate oxide of RF switch transistor, the voltage divider 500 of Fig.9 a and 9b can be used advantageously, and the reliability of the transistor in both the above-mentioned level shifter 300 and a charge pump circuit can be improved. For example, the correction level shifter 600 which uses the voltage divider 500 of Fig.9 a for Fig.10 in combination with the level shifter 300 of Fig.6 a is shown. As shown in Fig.10, the output (it can set to the output node 314) of the inverter 306 in the level shifter 300 is applied to the input part of the first voltage divider 500'. Similarly, the output (it can set to the output node 316) of the inverter 312 of the level shifter 300 is applied to the input part of second voltage divider 500". The output of a voltage divider is fed back to the input part of the feedback inverters 304 and 310, as shown in Fig.10. If Fig.10 is referred to especially, the output "out" of a first voltage divider in output node 520' will be fed back to the input part of the feedback inverter 310. Similarly, the output "out_" of a second voltage divider in output node 520" is fed back to the input part of the feedback inverter 304. As it described above in relation to Fig.9 a, feedback

voltage is decreased in the range of -Vdd to direct-current abbreviation+0.9V by the level shifter 500' and 500". The function of the level shifter 600 does not change for the voltage oscillation in which this feedback path decreased.

[0073]

Please pull out an RF switch control signal "SW" and "SW_" from a level-shifter output, and note being able to supply RF switch 30 of the present invention of Fig.3 as an input, before inputting them into the voltage divider 500' and 500". For example, as shown in Fig.10, since the switch control signal "SW" is generated, the output of the inverter 306 in the output node 314 can be pulled out and used. Similarly, since the switch control signal "SW_" is generated, the output of the inverter 312 in the output node 316 can be pulled out and used. According to one embodiment, as it described above in relation to the two-step level shifter and the RF buffer circuit 400 of Fig.8 a, the control signal pulled out from the nodes 314 and 316 is stored in a buffer first, and is combined with RF switch transistor after that. Although the voltage oscillation covering the whole region is possible for the switch control signal SW and SW_, this does not cause the integrity problems of a gate oxide in an RF switch. Especially a switch control signal is crossed to the range from -Vdd to +Vdd (that is, the voltage level of a switch control signal is not restricted by the voltage divider). The all-out voltage oscillation of a switch control signal does not cause the integrity problems of a gate oxide about RF switch MOSFET. The source of RF switch MOSFET is because it is grounded. Therefore, a switch input signal relates to the ground in RF switch MOSFET. As a result, MOSFET is applied to the whole gate oxide in positive Vdd voltage to a ground, or negative Vdd voltage is applied to the whole gate oxide to a ground.

[0074]

The simple graphic table expression 601 of the part in the correction level shifter 600 is shown in Fig.10 again. The sign 601 expresses the portion which the dashed line region 601' of Fig.10 shows. As shown in Fig.10, first ininput "_" 630 corresponding to the input node 326 ("in_") are contained in the correction level shifter 601 with a sign. The second input "out" 632 corresponding to the input to the feedback inverter 310 is included in the correction level shifter 601 with a sign again. This signal should be careful of having come out of the outputting part 520' of the first voltage divider 500' again. Positive power supply voltage is input by the +Vdd input part 634. Negative power supply voltage is input by the -Vdd input part 636. There are three output signals, i.e., "out_pos" (it can set to the outputting part 638), "out_neg" (it can set to the outputting part 640), and "out_" (it can set to the outputting part 642) in the correction level shifter 601. These outputting parts correspond to the above-mentioned output nodes 606 and 608 and 520". In order to understand easily, in the Drawings described below, graphic table expression of the level shifter 601 is used.

[0075]

The potential gate oxide integrity problems relevant to the level shifter 300 described above in relation to Fig.6 a are avoided in the feedback path of the correction level shifter 600 using the voltage divider 500' and 500". The voltage divider 500' and 500" can also function in order to decrease the potential gate oxide integrity problems relevant to a charge pump circuit. As shown in Fig.10, the output of the inverters 308 and 310 is supplied to two output intervals as an input, in order to be pulled out from the level shifter 300 and to generate two output signals "out_pos" and "out_neg." Especially the output of the inverter 308 is supplied as an input to the first output inverters 602. Similarly, the output of the feedback inverter 310 is supplied as an input to the second output inverters 604.

[0076]

By combining the output inverters 602 and 604 by such a method, never exceeding Vdd (or -Vdd) of the output signal of the correction level shifter 600 is lost. Especially the first output inverters 602 generate the output signal "out_pos" covering the range of GND (namely, direct current 0V) to +Vdd in the first output node 606. The second output inverters 604 generate the second output signal "out_neg" covering the range of -Vdd to GND in the second output node 608. If the input signal "in_" is set to GND, the output signal "out_pos" will be set to GND. The output signal "out_neg" moves from GND to -Vdd. If the input signal "in_" is set to positive +Vdd, "out_pos" will be set to Vdd and "out_neg" will move from -Vdd to GND. Thus, if the correction level shifter 600 of the present invention is used, the "out_pos" output signal will be crossed to the range of GND to +Vdd, and, on the other hand, the "out_neg" output signal will be crossed to the range of GND from -Vdd. The potential gate oxide integrity problems in a correction charge pump circuit are tackled using two output signals "out_pos" and "out_neg" so that it may describe in detail by the following. The potential gate oxide integrity problems in an RF buffer circuit can also be tackled using these output signals so that it may describe in relation to Fig.11 a and 11b here.

A correction level shifter and an RF buffer circuit

In two steps of the level shifter and RF buffers 400 described above in relation to Fig.8 a, the voltage oscillation of abbreviation 2xVdd may be experienced in an RF buffer inverter input. As already described, in the voltage oscillation of this level, gate oxide integrity problems arise and it may have harmful influence on the function of RF buffer transistor.

[0077]

The alternative embodiment of the two-step level shifter and the RF buffer circuit 400 described above in relation to Fig.8 a to Fig.11 a and 11b is shown. The voltage concerning the gate oxide of an RF buffer is kept from exceeding Vdd from 0.9 volt reliably in the alternative embodiment of an RF buffer shown in Fig.11 b using the voltage divider circuit described above. As shown in Fig.11 b, the 2nd step RF buffer circuit 402' combined with the 1st step level shifter circuit 600 and it is included in substitute two-step level shifter and RF buffer circuit 400'. In this embodiment of a level shifter and the RF buffer circuit 400', An RF buffer output signal "out" and "out_" are generated using the output "out_pos" and "out_neg" of a correction level shifter which were described above in relation to Fig.11 as an input to an RF buffer inverter. For example, as shown in Fig.11 b, "out_pos" and the "out_neg" output signal which the first correction level shifter 700 generates are input into the two RF buffer inverters 702 and 704, respectively. Similarly, "out_pos" and the "out_neg" output signal which the second correction level shifter 706 generates are input into the two RF buffer inverters 708 and 710, respectively. According to Embodiment 400' of the substitution shown in Fig.11 a and 11b, as for the "out_pos" output, the input signal "in" is logically set to Vdd at the time of a high signal, and, on the other hand, "out_neg" is set to GND. Thus, logically, at the time of a high value, the output of the inverter 702 is set to GND and, as for the output of the inverter 704, the input signal "in" is set to -Vdd. Therefore, as for the output of the inverter 712, the input signal "in" is set to ("out")-Vdd when high. When low, an opposite output is generated for an input signal "in."

[0078]

The power supply voltage of the first RF output inverter 712 is controlled using the RF buffer inverters 702 and 704. Similarly, the power supply voltage of the second RF output inverter 714 is controlled using the RF buffer inverters 708 and 710. An RF switch is controlled by this embodiment using an RF buffer output signal "out" and "out_" (that is, the output signal "out" works as control voltage "SW", and, on the other hand, commits "out_" as control voltage

"SW_").
Correction charge pump alternative embodiment
As mentioned above, two output signals "out_pos" and "out_neg" which the correction level shifter 600 of Fig.10 generates, It can use by one embodiment of the substitution in a charge pump circuit, and the potential gate oxide integrity problems relevant to the excessive voltage applied to a charge pump can be decreased or eliminated. As it described above in relation to Fig.5 b and 5c, it is a charge pump transistor (). That is, the voltage oscillation of 2xVdd is among the clock signals used in order to control the gate of the P channel transistors 208 and 210 and the N channel transistors 212 and 214. For example, as shown in Fig.5 c, a charge pump clock signal "Clk1" and "Clk2" are crossed to the range of positive power-supply-voltage +Vdd from negative power-supply-voltage-Vdd. The voltage oscillation covering this whole region may cause oxide integrity problems in a charge pump circuit like the gate oxide integrity problems described above in relation to the RF buffer circuit and the level shifter circuit. Therefore, by restricting the voltage applied to a gate oxide from -Vdd to the range of 0.9V shows to Fig.12 the correction charge pump circuit which decreases in number or eliminates potential gate oxide integrity problems.
[0079]
The correction charge pump 800 is shown in Fig.12. This uses the correction level shifter 600 described above in relation to Fig.10. As shown in Fig.12, the charge pump circuit 206' and the charge pump clock generation circuit 802 of the present invention are included in the correction charge pump 800. By the charge pump clock generation circuit 802, the clock control signal which the charge pump circuit 206' uses is generated. The design resembles dramatically the charge pump 206 which the charge pump circuit 206' described above in relation to Fig.5 b. For example, it adds to path capacitor Cp216 and the output capacitor C218, and the pair of P channel transistors 208 and 210 and the pair of N channel transistors 212 and 214 are contained in the charge pump circuit 206'. According to one embodiment of the charge pump circuit 206', there is a capacitance of hundreds of pF order in the output capacitor C218, and there is a capacitance of about 50 pF in capacitor Cp216. The person skilled in the art of the charge pump design field will be understood [that other capacitance values can be used and], without deviating from the range or the meaning of the present invention.
[0080]
The function of charge pump 206' resembles dramatically the charge pump 206 described above in relation to Fig.5 a. Therefore, it does not carry out describing the operation in detail again here. That charge pump 206' shown in Fig.12 differs from the charge pump 206, The control signal used in order to control the transistor gate (namely, gate of the transistors 208, 210, 212, and 214) of charge pump 206', It is the point restricted to the region of the half of a voltage oscillation (that is, restricted to the range of Vdd from the ground or the ground from -Vdd). the potential gate oxide integrity problems produced when gate control voltage vibrates the whole region from -Vdd to Vdd namely, -- -- or [therefore, / decreasing] -- or it eliminates.
[0081]
As shown in Fig.12, the four correction level shifters 804, 806, 808, and 810 combined with feedback composition are contained in both the charge pump clock generation circuits 802. According to one embodiment of a correction charge pump, four correction level shifters are realized by the correction level shifter 600 described above in relation to Fig.10. The level shifter using the graphic table expression 601 of the level shifter 600 in Fig.10 is shown inFig.12.According to this embodiment, the level shifters 804, 806, 808, and 810 carry out the

same operation as the level shifter 600 of Fig.10. Two non-overlapping clock signals "Clk1" and "Clk2" (and each reverse signal "Clk1_" and "Clk2_") are input into "in_" input part of a level shifter as shown in Fig.12. Two input clock signals "Clk1" and "Clk2" are the same as that of the non-overlapping clock signal described above in relation to Fig.5 a - 5c. As shown above in relation to Fig.5 c, two non-overlapping clock signals change by the voltage swing of -Vdd to +Vdd. According to one embodiment, a clock signal changes from direct-current-3V to direct-current+3V.

[0082]

The clock control signal of the half region used by four correction level shifters in order to control charge pump 206' is generated. As especially shown in Fig.12, "CLK1POS_", "CLK1NEG_", "CLK2POS", and a "CLK2NEG" control signal are generated by four level shifters. These are input into the charge pump transistor gate control nodes 250, 252, 254, and 256, respectively. According to the embodiment shown in Fig.12, four transistor gate control signals "CLK1POS_", "CLK1NEG_", "CLK2POS", and "CLK2NEG" are generated by the level shifters 805 and 808. By the level shifter 806, "CLK1POS_" and a "CLK1NEG_" gate control signal are generated, and, on the other hand, "CLK2POS" and a "CLK2NEG" gate control signal are generated by the level shifter 808. As especially shown in Fig.12, the "out_pos" output ("CLK1POS_") of the level shifter 806 is combined in order to control the transistor gate input part 250 of the transistor 208. The "out_neg" output ("CLK1NEG_") of the level shifter 806 is combined in order to control the transistor gate input part 252 of the transistor 210. Similarly, the "out_pos" output ("CLK2POS") of the level shifter 808 is combined in order to control the transistor gate input part 254 of the transistor 214. Finally, the "out_neg" output ("CLK2NEG") of the level shifter 808 is combined in order to control the transistor gate input part 256 of the transistor 214. It functions as the clock generation circuit 802 preventing the excessive voltage of the whole gate oxide in a charge pump transistor.

[0083]

The person skilled in the art of the transistor design field will be understood [that other control constitution can be used and], without deviating from the meaning or the range of the present invention. For example, in the alternative embodiment of a correction charge pump, a control signal can be generated using other two level shifters (804 and 810). As it described above in relation to the charge pump circuit 206, correction charge pump 206' of the present invention is realizable using substitute transistor composition (an N channel and a P channel).

[0084]

As shown in Fig.12, the four level shifters 804, 806, 808, and 810, It is combined with both the groups (804, 806, and 808 and 810) of a level shifter in the feedback composition which resembles dramatically the feedback topology of the level shifter described above in relation to Fig.6 a. For example, the "out_" output node (signal) of the level shifter 804 is supplied to the "out" node of the level shifter 806 of the related group as feedback. Similarly, the "out_" output node of the level shifter 806 is supplied to the "out" node of the level shifter 804 of the related group as feedback. Similarly, the "out_" output node of the level shifter 808 is supplied as feedback to the "out" node of the level shifter 810 of the related group. The "out_" output node of the level shifter 810 is supplied to the "out" node of the level shifter 808 of the related group as feedback. In generating of four transistor gate control signals "CLK1POS_", "CLK1NEG_", "CLK2POS", and "CLK2NEG", the clock generation circuit 802 uses feedback composition.

Outline

The new RF switch manufactured using SOI and a CMOS process is provided. If a switch is

manufactured on a SOI substrate, as a result, board bias will be lost and it will become possible to accumulate the main CMOS-circuit configuration blocks with an RF switch element. By accumulating a CMOS structure block with an RF switch element, the solution [need / only a single external power (that is, negative power supply voltage is generated inner in the charge pump circuit accumulated with the RF switch) / to be used] of the RF switch integrated completely is provided. As this result, RF switch separation, insertion loss, and compression are improved. In one embodiment, the 1-dB compression point of an RF switch exceeds about 1 W, insertion loss is less than about 0.5 dB, and switch separation is about about 40 dB in height. Switching time improves with a present invention switch again.

[0085]

It has described about some embodiments of the present invention. However, it will be understood that various corrections are possible, without deviating from the meaning and the range of the present invention.

[0086]

Therefore, the present invention should understand the specific thing which it is not limited by the illustrated embodiment but is limited by only attached Claims.

[Brief Description of the Drawings]

[0087]

[Fig.1 a] It is a simple electric diagram of the single-pole single-throw (SPST) RF switch by the advanced technology used in order to describe the performance characteristic of an RF switch.

[Fig.1 b] It is a simple electric diagram of SPST and the RF switch in Fig.1 a, and this switch turns "ON" and the characteristics with a main switch when passage of an RF signal is attained from an input node to an output node are shown.

[Fig.1 c] An RF switch turns "OFF" and the equivalent small signal electrical property of the RF switch in Fig.1 a when an RF signal is blocked with it from an output node, and 1b is shown.

[Drawing 2]It is a simple electric diagram of the single pole double throw (SPDT) RF switch by the advanced technology.

[Drawing 3]It is an electric diagram of the RF switch by one embodiment of the present invention.

[Drawing 4]It is a simple block diagram of the RF switch which was manufactured according to the present invention and which is illustration-like and was integrated completely.

[Fig.5 a] It is a simple block diagram of one illustration embodiment in the negative voltage generator shown in the simple block diagram of Fig.4.

[Fig.5 b] It is an electric diagram of the first embodiment in the charge pump circuit used since negative service voltage is generated to the RF switch of Fig.4.

[Fig.5 c] It is the plot of a voltage swing versus [which shows two voltage swings of a clock signal which do not overlap but change temporally] time used in order to control the charge pump circuit of Fig.5 b.

[Fig.6 a] It is an electric diagram of the first embodiment in the level shift circuit of the present invention.

[Fig.6 b] It is an electric diagram of one embodiment in the inverter used in order to realize the level shifter of Fig.6 a.

[Fig.7 a] It is the plot of a voltage swing versus time of the output signal which the level shifter of the present invention of Fig.6 a corresponding to a digital input signal and it generates.

[Fig.7 b] They are simple logical symbols of the level shifter of the present invention in Fig.6 a.

[Fig.8 a] It is an electric diagram of one embodiment in a two-step level shifter and RF buffer

circuit including the level shifter of the 1st step, and the RF buffer circuit of the 2nd step.
[Fig.8 b] It is a simple block diagram of an interface to the RF buffer circuit of a digital control input and Fig.8 a.
[Fig.9 a] It is an electric diagram of one embodiment in the low current voltage divider (LCVD) circuit which manufactured according to invention of this RF switch.
[Fig.9 b] They are simple logical symbols used in order to express the voltage divider of Fig.9 a.
[Drawing 10]It is an electric diagram of the second embodiment in the level shift circuit which uses the low current voltage divider circuit of Fig.9 a in combination with the level shift circuit of Fig.6 a.
[Fig.11 a] It is an electric diagram showing the alternative embodiment of the two-step level shifter and RF buffer circuit of Fig.8 a.
[Fig.11 b] It is an electric diagram showing the alternative embodiment of the two-step level shifter and RF buffer circuit of Fig.8 a.
[Drawing 12]It is an electric diagram of the correction charge pump which uses the level shift circuit of Fig.10.

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TECHNICAL FIELD

[Field of the Invention]
[0001]
The background of invention
The field of invention
Especially the present invention relates to the switching circuit in an integrated circuit, and the switching method of a high frequency (RF) signal about a switch. According to one embodiment, the CMOS device realized on [for using it in the field of application of RF, such as a wireless communication equipment, a satellite, and cable TV,] a silicon on insulator (SOI) is contained in this switching circuit.

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PRIOR ART

[Background of the Invention]
[0002]
The description of a pertinent art
As everyone knows, the high frequency (RF) switch serves as an important configuration block in many wireless communication systems. The RF switch is used for the communication equipment with which many, such as a cellular phone, a wireless pager, wireless infrastructure equipment, satellite communication equipment, and cable TV equipment, differ. As everyone knows, it opts for the performance of an RF switch by the three main performance parameters of operation, i.e., insertion loss, switch separation, and a "1-dB compression point." These three performance parameters are connected closely, and in the design of an RF switch component, when they think any one parameter as important, other parameters will be sacrificed for them. The 4th parameter sometimes taken into consideration in an RF switch design is usually called switching time or switching speed (one side of a switch is turned ON and defined as time required to turn OFF an opposite side). In the design of an RF switch, the ease of RF switch accumulation, a degree (level), complexity, the yield, a returned-goods loss, and a manufacturing cost are contained in other important indices.
[0003]
The performance parameter of these RF switches can be more easily described with reference to the RF switch design by the advanced technology shown in the simple circuit diagram of Fig.1 a - 1c. The simple circuit diagram of single-pole single-throw (SPST) RF switch 10 of the advanced technology is shown in Fig.1 a. The switching transistor M1 (5) and the shunt transistor M2 (7) are contained in SPST switch 10 of the advanced technology. If Fig.1 a is referred to here, it will be dependent on the state of two MOSFET transistors M1 (5) and the control voltage of M2 (7) (). Namely, depending on the DC bias applied to the gate input part of the MOSFET switching transistor M1 and the shunt transistor M2, respectively an RF signal, It is sent to the RF output node 3 from the RF input node 1, or shunts via the shunt transistor M2 (7) in a ground. The actual value of DC bias voltage is dependent on MOSFET transistor M1 (5), and the polarity of M2 (7) and a threshold value. An RF power signal and the in-series resistor R0 (9) separate bias from a power supply signal.
It is indispensable for the highest switch performance.
"ON" state of RF switch 10 in Fig.1 a is shown in Fig.1 b (that is, to Fig.1 b). RF switch 10 shows the equivalent small signal value of the transistors M1 and M2 in case "ON" and the switching transistor M1 (5) are [ON and the shunt transistor M2 (7)] OFF. "OFF" state of the switch 10 of Fig.1 a is shown in Fig.1 c (that is, RF switch 10 shows the equivalent small signal

value of the transistors M1 and M2 in case "OFF" and the switching transistor M1 (5) are [OFF and the shunt transistor M2 (7)] ON to Fig.1 c).

[0004]

As shown in Fig.1 b, when RF switch 10 is ON, the switching transistor M1 (5) is mainly resistance, and, on the other hand, its shunt transistor M2 (7) is mainly capacitive. "Insertion loss" of RF switch 10 is determined from the difference between the maximum available electric power in the input node 1, and the electric power supplied to the load of the output node 3. In a low frequency wave, when the switch 10 is ON (Fig.1 b should be referred to), each power loss originates in the on resistance 13 "r" with the limited switching transistor M1 (5). Typically, the on resistance r13 (Fig.1 b) is much smaller than the power-resistors machine R0 (9). Therefore, insertion loss "IL" has the characteristics like the formula 1 shown below.

Formula 1: IL is equal to 10 r/R0ln(10) =0.087r (dB) substantially.

[0005]

Therefore, the value of r serves as insertion loss of about 0.25 dB as a result at 3ohms by a low frequency wave. Since insertion loss is largely influenced by the on resistance of an RF switch transmitter, it lowers transistor on resistance and can improve insertion loss by decreasing parasitism board resistance.

[0006]

Generally, input-output separation (or simply switch separation) of an RF switch is determined by measuring the electric energy which "flows" out of an input port into an output port, when the transistor which has connected the input port and the output port is OFF. As for separation characteristics, the degree of cutting of an RF switch shows how much (that is, how much does a switch block an input signal from an output?). If "OFF" state of RF switch 10 in Fig.1 c is referred to especially here, the OFF state of the switch M1 (5) will serve to block the input 1 from the output 3. The shunt transistor M2 (7) serves to improve input-output separation of the switch 10.

[0007]

When a turn-off is carried out (namely, when RF switch 10 and the switching transistor M1 (5) carry out a turn-off) M1 (5), It is mainly capacitive and "feed through" (an RF input signal should pass from the input node 1 to the output node 3) of an input signal, The capacitor CGD OFF 15 (gate drain capacitance when the switching transistor M1 carries out a turn-off), Capacitor CGS OFF 17 (when the switching transistor M1 carries out a turn-off) The series / parallel value of a ** gate source capacitance, and capacitor CDS1 (19) and (a drain source capacitance when the switching transistor M1 carries out a turn-off) determine. The feed through of an input signal relates to input-output separation of RF switch 10 directly desirably. The size of feed through is decreased using the shunt transistor M2 (7), and the separation characteristics of an RF switch are improved by it.

[0008]

When the switching transistor M1 (5) is a turn-off, turn-on of the shunt transistor M2 of Fig.1 c (7) is carried out. In this condition, the shunt transistor M2 (7) mainly works as a resistor of the value r. Depending on a design, the value of r is much smaller than impedance peculiar to RF power. As a result, r decreases remarkably the voltage of the input part of the switching transistor M1 (5). When the value of r is much smaller than the power resistors R0 (9) and feed-through capacitive resistance of the shunt transistor M2 (7), separation can be calculated easily. Switch separation of the OFF state of RF switch 10 is determined with the difference between the maximum available electric power of an input part, and the electric power of an outputting part.

[0009]
It is the capability to process the input power with another, important big RF switch performance characteristic in addition to the insertion loss of an RF switch, and separation. When turn-on of the switch is carried out, this is fixed frequency and is making for insertion loss not to serve as a function of input power into a positive thing. It is called for by many field of application that a switch cannot be distorted in the electric power sent through the switch which carried out "switch-on." For example, when two sounds which approached pass an RF switch simultaneously, they may start an intermodulation (IM) for the nonlinearity of a switch, and may generate a pseudo voice by the channel which adjoins by that cause. For example, when securing these adjoining channels for the information signal, the electric power of a pseudo voice must be maintained as small as possible. Switch compression or a "1-dB compression point" ("P1dB") shows the capability to process electric power. P1dB, it defines as input power when insertion loss increases only 1 dB from the low-electric-power value. Or when it has another way of speaking, a 1-dB compression point is a degree of the electric energy which can be input into an RF switch in an input port, before output power of only 1 dB deviates from linear relation with input power.
[0010]
Switch compression is generated in any one of the two routes. In order to understand how switch compression occurs, it describes about operation of the MOSFET transistor shown in RF switch 10 of Fig.1 a - 1c. In order to carry out turn-on of the MOSFET as everyone knows in the transistor design field, the gate source bias exceeding threshold voltage Vt is required. Similarly, gate source bias must be smaller than Vt, in order for a switch to be come by off. Vt is positive in "N type" MOSFET.
In "P type" MOSFET, it is negative.
N-channel MOS FET is chosen as RF switch 10 of Fig.1 a - 1c. The source of N-channel MOS FET is a node of the lowest electric potential.
If Fig.1 c is referred to again and the shunt transistor M2 (7) will carry out turn-on to the part period of an input signal cycle as a result of the transient voltage of the shunt transistor M2 (7), input power will be sent to a ground and will be lost to an output. The loss of this electric power will increase, if input power increases (namely, input signal of the electric power which increased), and thereby, it causes a first type of compression. The 1-dB compression point of RF switch 10 is determined by the signal vibration of the input in the point it stops in the shunt transistor M2 (7) which carried out the turn-off keeping [OFF / point] not been. After all, a negative vibration of an input is lower than a ground, and becomes lower than M2 gate potential in a similar manner (therefore, it source-izes). If this difference becomes equal to Vt, the transistor M2 (7) will begin to carry out turn-on, and compression will start. This first type of compression is caused by the turn-on phenomenon of the no MARIOFU type gate in the shunt leg of an RF switch. Once the shunt transistor M2 (7) carries out turn-on, the electric power of the output node 3 will not follow the electric power of a switch input part any longer at linearity.
A second type of RF switch compression is generated when the source and drain of the shunt transistor M2 (7) carry out breakdown on excessive voltage. This voltage has only the possibility exceeding service voltage direct-current abbreviation+1V to a submicron silicon on insulator (SOI) device. In breakdown, a shunt device begins to conduct a lot of electric power, and the electric power which can be used with an output by that cause decreases.
[0011]

The simple figure of single pole double throw (SPDT) RF switch 20 by the advanced technology is shown in Fig.2. As shown in Fig.2, four MOSFET transistors 23, 24, 27, and 28 are contained in RF switch 20 of the advanced technology at worst. The transistors 23 and 25 work as a "path" or a "switching" transistor (to switching MOSFET transistor M1 (5) and the appearance of drawing 1 a-1c), It is constituted so that each of these related RF input node may be combined with RF node 25 common in alternative. For example, when operating, the switching transistor 23 combines the first input signal "RF1" that is an input to the first RF input node 21 to the RF common nodes 25 (namely, when switched to "ON"). Similarly, when operating, the switching transistor 24 combines the second RF input signal "RF2" which is an input to the second RF input node 22 to the RF common nodes 25. The shunt transistors 27 and 28 by the case where it is operating those related RF input nodes, When not having combined with the RF common nodes 25, it works in order to shunt each related RF input node to a ground in alternative (namely, when the turn-off of the switching transistor (23 or 24) connected to those related input nodes is carried out).

[0012]

In order to control operation of the RF switch of the advanced technology to be shown in Fig.2, two control voltage is used. The control voltage with the name of "SW" and its reverse "SW_" controls operation of the transistors 23, 24, 27, and 28. control voltage is an alternative about the pair of the selected transistor ---like -- an operation (turn-on) -- or it is adjusted so that it may be made non-operative (turn-off). For example, as shown in Fig.2, SW turns on (according to some embodiments). When this is determined by setting control voltage to a voltage level logically "high", for example, "+Vdd", the switching transistor 23 is operating and the related shunt transistor 28 also operates. However, reverse SW_ of SW controls operation and its related shunt transistor 27 of the second switching transistor 24, and control signal SW_, during ON (according to some embodiments, this is determined by setting SW_ as -Vdd) of SW, since it is off, these two transistors are non-operative in this same period -- or the turn-off is carried out. RF1 input signal is combined with the RF (passing switching transistor 23 which is operating) common port 25 in this state (in SW, SW_ turns off by ON). Since the turn-off of the second switching transistor 24 is carried out, RF2 input signal is blocked from the RF common port 25. Moreover, since an RF2 input signal is shunted in a ground via the shunt transistor 28 which is operating, it is further separated from the RF common port 25. When [whose SW control signal is "OFF" (and SW_ "ON") like] it will be understood easily, the person skilled in the art of the transistor design field, RF2 signal is the same method and is combined with the RF common port 25 (and RF1 signal is shunted to a block ** leg round).

[0013]

RF switches, such as SPDF, RF switch 20, etc. of Fig.2, have so far been realized with the result on various performances in different element technology including a bulk complementary metal oxide semiconductor (CMOS) and gallium arsenide (GaAs) technology. In fact, GaAs technology is being used for almost all highly efficient high frequency switches. In realization of the RF switch by the advanced technology, although it has tried to improve the above-mentioned RF switch performance characteristic, those results are miscellaneous and are various. [of the complexity of an integrated circuit and the degree of the yield] For example, bulk CMOS and an RF switch show a high insertion loss performance characteristic, the low compression performance characteristic, and an insufficient linearity performance characteristic to a disadvantageous thing. By contrast, for semi insulating [of GaAs material], the parasitism board

resistance can decrease remarkably and, thereby, can decrease switch insertion loss. Similarly, a half-insulation GaAs substrate improves switch separation.

[0014]

Although improvement in a performance characteristic is brought about by realization of a GaAsRF switch, this technology has some faults. For example, the yield of the integrated circuit which functions normally in GaAs technology is comparatively low. It tends to become expensive [a design and manufacture] comparatively [a GaAsRF switch]. In addition, although GaAs switches improve an insertion loss characteristic as mentioned above, frequency restrictions may become low for the slow surface state which exists in a GaAs substrate. Since this technology is not fit for integration of the high level, an "off-chip" needs to realize the digital control circuit relevant to an RF switch from a switch. It turns out that the low-electric-power circuit relevant to a switch is difficult to be accumulated. Since this makes overall system cost or manufacturing cost, size, and complexity increase and decreases the throughput speed of a system similarly, it is disadvantageous.

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TECHNICAL PROBLEM

[Problem to be solved by the invention]
[0015]
Therefore, it is desirable to provide the method of switching the RF switch and RF signal which have an improved performance characteristic. It is desirable to provide the RF switch which insertion loss, separation, and compression have improved especially. Design manufacture of such an RF switch was completed easily, it was manufactured comparatively inexpensive, and is fit for accumulation of the high level, and it is desirable that it is applicable from a low frequency wave to high frequency. It should enable it to accumulate a power control circuit on chip simply with a switch function. Such accumulation was difficult to realize until now using a Si substrate and a GaAs substrate. The present invention provides such an RF switch and the switching method of an RF signal.

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MEANS

[Means for solving problem]
[0016]
The outline of invention
It describes about the switching method of a new RF switching circuit and an RF signal. An RF switch is usable for a wireless use, and can be manufactured with silicon on insulator technology. In one embodiment, an RF switch is manufactured on an ultra-thin silicon ("UTSi") substrate. The following thing is contained in an RF switch in one embodiment. Namely, the first switching transistor group who is connected to the input part for receiving an RF signal, the input part for receiving an RF signal, and RF common port, and is controlled by switching voltage (SW), It is connected to a first switching transistor group and RF common port, The second switching transistor group controlled by switching voltage (SW_) is contained, and SW_ is the reverse of SW, and when a first switching transistor group is ON, a second switching transistor group is come by off. A switching transistor group connects each RF input signal to RF common port in alternative, while operating. In this embodiment, it is combined with an RF switch by the switching transistor group again, and the shunt transistor group controlled by the switching voltage SW and SW_ is contained. While operating, a shunt transistor group works so that those related RF input nodes may be shunted to a ground in alternative, and improves RF switch separation by it.
[0017]
One or more MOSFET transistors connected by lamination or series constitution are contained in both switching and a shunt transistor group. Within each transistor group, the gate of a lamination transistor is usually controlled by switching voltage (SW or SW_), and this switching voltage is combined with each transistor gate via each gate resistance machine. The compression point of a switch increases with lamination and the gate resistance machine of a transistor group device. The RC time constant formed of the gate resistance machine and gate capacitance of MOSFET is designed to become much longer than the cycle of an RF signal, and RF voltage is equally shared with the whole series-connection device. By this composition, the 1-dB compression point of an RF switch increases.
[0018]
It describes about the RF switch integrated completely. A digital switch control logic circuit and the negative power-supply-voltage generator accumulated with the RF switch of the present invention are contained in this RF switch. According to one embodiment, the RF switch of the advanced technology is provided with some functions not existing by the RF switch integrated completely. For example, in one embodiment, to the RF switch integrated completely. The built-

in type oscillator which supplies a clock input signal to a charge pump circuit, and the charge pump circuit which generates the negative power supply voltage which other RF switching circuits need and which were accumulated, The CMOS logic circuit which generates the control signal which controls RF switch transistor, The level shift circuit and low current voltage divider circuit which increase the reliability of a switch device, and the RF buffer circuit which separates RF signal energy from a charge pump circuit and a digital control logic circuit are included. It describes about some embodiments of a charge pump circuit, a level shift circuit, a voltage divider, and an RF buffer circuit. By the RF switch of the present invention, insertion loss, switch separation, and switch compression are improved. Thanks to the accumulation of a higher level which becomes available with the RF switch of the present invention, by using the present invention, a design and manufacturing cost of RF system decrease, and reliability increases.
In the following brief explanation of the drawings, the same reference mark of various Drawings shows the same component.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[0087]
[Fig.1 a] It is a simple electric diagram of the single-pole single-throw (SPST) RF switch by the advanced technology used in order to describe the performance characteristic of an RF switch.
[Fig.1 b] It is a simple electric diagram of SPST and the RF switch in Fig.1 a, and this switch turns "ON" and the characteristics with a main switch when passage of an RF signal is attained from an input node to an output node are shown.
[Fig.1 c] An RF switch turns "OFF" and the equivalent small signal electrical property of the RF switch in Fig.1 a when an RF signal is blocked with it from an output node, and 1b is shown.
[Drawing 2]It is a simple electric diagram of the single pole double throw (SPDT) RF switch by the advanced technology.
[Drawing 3]It is an electric diagram of the RF switch by one embodiment of the present invention.
[Drawing 4]It is a simple block diagram of the RF switch which was manufactured according to the present invention and which is illustration-like and was integrated completely.
[Fig.5 a] It is a simple block diagram of one illustration embodiment in the negative voltage generator shown in the simple block diagram of Fig.4.
[Fig.5 b] It is an electric diagram of the first embodiment in the charge pump circuit used since negative service voltage is generated to the RF switch of Fig.4.
[Fig.5 c] It is the plot of a voltage swing versus [which shows two voltage swings of a clock signal which do not overlap but change temporally] time used in order to control the charge pump circuit of Fig.5 b.
[Fig.6 a] It is an electric diagram of the first embodiment in the level shift circuit of the present invention.
[Fig.6 b] It is an electric diagram of one embodiment in the inverter used in order to realize the level shifter of Fig.6 a.
[Fig.7 a] It is the plot of a voltage swing versus time of the output signal which the level shifter of the present invention of Fig.6 a corresponding to a digital input signal and it generates.
[Fig.7 b] They are simple logical symbols of the level shifter of the present invention in Fig.6 a.
[Fig.8 a] It is an electric diagram of one embodiment in a two-step level shifter and RF buffer circuit including the level shifter of the 1st step, and the RF buffer circuit of the 2nd step.
[Fig.8 b] It is a simple block diagram of an interface to the RF buffer circuit of a digital control input and Fig.8 a.

[Fig.9 a] It is an electric diagram of one embodiment in the low current voltage divider (LCVD) circuit which manufactured according to invention of this RF switch.
[Fig.9 b] They are simple logical symbols used in order to express the voltage divider of Fig.9 a.
[Drawing 10]It is an electric diagram of the second embodiment in the level shift circuit which uses the low current voltage divider circuit of Fig.9 a in combination with the level shift circuit of Fig.6 a.
[Fig.11 a] It is an electric diagram showing the alternative embodiment of the two-step level shifter and RF buffer circuit of Fig.8 a.
[Fig.11 b] It is an electric diagram showing the alternative embodiment of the two-step level shifter and RF buffer circuit of Fig.8 a.
[Drawing 12]It is an electric diagram of the correction charge pump which uses the level shift circuit of Fig.10.

* NOTICES *

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damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

WRITTEN AMENDMENT

[Written Amendment]
[Filing date]Heisei 15(2003) November 3 (2003.11.3)
[Amendment 1]
[Document to be Amended]Claims
[Item(s) to be Amended]Whole sentence
[Method of Amendment]Change
[The contents of correction]
[Claim(s)]
[Claim 1]
(a) A first input port that receives a first RF input signal,
(b) A second input port which receives a second RF input signal,
(c) RF common port,
(d) Each transistor has the gate resistance of abbreviation 30komega at least, A first node that is a first switch transistor group containing two or more transistors arranged at laminated constitution, and was combined with said first input port, A first switch transistor group who has the second node combined with the aforementioned RF common port, and is controlled by a switch control signal (SW),
(e) Each transistor has the gate resistance of abbreviation 30komega at least, A first node that is a second switch transistor group containing two or more transistors arranged at laminated constitution, and was combined with said second input port, A second switch transistor group who has the second node combined with the aforementioned RF common port, and is controlled by an inversion signal (SW_) of the aforementioned switch control signal (SW),
(f) each transistor -- at least -- about -- with a first node that is a first shunt transistor group containing two or more transistors which have the gate resistance of 30komega, and which are arranged at laminated constitution, and was combined with said second input port, A first shunt transistor group who has the second node combined with a ground and is controlled by the aforementioned switch control signal (SW),
(g) each transistor -- at least -- about -- with a first node that is a second shunt transistor group containing two or more transistors which have the gate resistance of 30komega, and which are arranged at laminated constitution, and was combined with said first input port, It is an RF switching circuit for switching an RF signal which has the second node combined with a ground and is controlled by an inversion signal (SW_) of the aforementioned switch control signal (SW) and including a second shunt transistor group,

When the aforementioned switch control signal SW is effective, while said first switch transistor group and said first shunt transistor group operate, Become non-operative [said second switch transistor group and said second shunt transistor group], and by that cause, Pass said first RF input signal to the aforementioned RF common port, shunt said second RF input signal to a ground, and when the aforementioned switch control signal SW is un-effective, While said second switch transistor group and said second shunt transistor group operate, An RF switching circuit which said first switch transistor group and said first shunt transistor group become non-operative, pass said second RF input signal to the aforementioned RF common port by that cause, and shunts said first RF input signal to a ground.

[Claim 2]

The RF switching circuit according to claim 1 manufactured in silicon on insulator (SOI) technology.

[Claim 3]

The RF switching circuit according to claim 1 manufactured on an ultra-thin silicon ("UTSi") substrate.

[Claim 4]

Said perfect insulation sapphire wafer the joint effect of a substrate by decreasing including a parallel MOSFET transistor by which the aforementioned transistor group is formed in a thin silicon layer on a perfect insulation sapphire wafer, The RF switching circuit according to claim 3 which improves the performance characteristic of the aforementioned RF switch.

[Claim 5]

The RF switching circuit according to claim 4 which decrease in number when switch insertion loss decreases on resistance of the aforementioned MOSFET transistor.

[Claim 6]

The RF switching circuit according to claim 4 improved when the switch separation characteristics of the aforementioned RF switch decrease parasitic capacitance between nodes of the aforementioned MOSFET transistor.

[Claim 7]

The RF switching circuit according to claim 3 where the aforementioned transistor group contains two or more MOSFET transistors.

[Claim 8]

The RF switching circuit according to claim 7 where the aforementioned MOSFET transistor contains a gate resistance machine usually controlled by switching voltage.

[Claim 9]

The RF switching circuit according to claim 8 by which the aforementioned gate resistance machine combined with a transistor gate node of said first switch transistor group and said first shunt transistor group is usually controlled by the aforementioned switch control signal SW.

[Claim 10]

The RF switching circuit according to claim 8 where the aforementioned gate resistance machine combined with a transistor gate node of said second switch transistor group and said second shunt transistor group is usually controlled by aforementioned reversing-switch control signal SW_.

[Claim 11]

The RF switching circuit according to claim 8 where the aforementioned RC time constant relevant to each MOSFET transistor in the aforementioned transistor group exceeds a cycle of

the aforementioned RF input signal far, and RF voltage is equally shared by it by the aforementioned whole MOSFET transistor.
[Claim 12]
Breakdown voltage of two or more aforementioned whole lamination MOSFET transistors of a selected transistor group, The RF switching circuit according to claim 8 where it is increased effectively [breakdown voltage of an individual MOSFET transistor of a transistor group who chose / aforementioned] n times, and n includes the total of an MOSFET transistor in a transistor group who chose [aforementioned].
[Claim 13]
The RF switching circuit according to claim 12 which has a related 1-dB compression point and increases the aforementioned 1-dB compression point using the aforementioned lamination MOSFET transistor composition.
[Claim 14]
Said first RF input signal and said second RF input signal have a related input power level, and an input power level which increased by increasing the number of MOSFET transistors for every transistor group, The RF switching circuit according to claim 7 which can be adjusted in the aforementioned RF switching circuit.
[Claim 15]
Said first RF input signal and said second RF input signal have a related input power level, and by changing physical size of a transistor which uses an input power level which increased for a transistor group's realization, The RF switching circuit according to claim 7 which can be adjusted in the aforementioned RF switching circuit.
[Claim 16]
(a) An RF switching circuit of a description to Claim 3,
(b) A control logic block which outputs the aforementioned switch control signal (SW) and the aforementioned reversing-switch control signal (SW_) and which was combined with the aforementioned RF switching circuit,
(c) A negative voltage generator combined with the aforementioned control logic block which receives positive power supply voltage of a clock input signal and an external power, and outputs negative power supply voltage,
******, an RF switching circuit integrated completely.
[Claim 17]
The RF switching circuit according to claim 16 on which the aforementioned RF switching circuit is accumulated by integrated circuit (IC) with two or more digital circuits and analog circuitry and which was integrated completely.

[Claim 18]
(a) -- (i) -- a first input port that receives a first RF input signal,
(ii) A second input port which receives a second RF input signal,
(iii) RF common port,
(iv) A first switch transistor group who has a first node combined with said first input port, and the second node combined with the aforementioned RF common port, and is controlled by a switch control signal (SW),
(v) A second switch transistor group who has a first node combined with said second input port, and the second node combined with the aforementioned RF common port, and is controlled by an inversion signal (SW_) of the aforementioned switch control signal (SW),

(vi) A first shunt transistor group who has a first node combined with said second input port, and the second node combined with a ground, and is controlled by the aforementioned switch control signal (SW),
(vii) A second shunt transistor group who has a first node combined with said first input port, and the second node combined with a ground, and is controlled by an inversion signal (SW_) of the aforementioned switch control signal (SW),
While it is ****** and an RF switching circuit, the SW is operating and said first switch transistor group and said first shunt transistor group operate, Become non-operative [said second switch transistor group and said second shunt transistor group], and by that cause, Pass said first RF input signal to the aforementioned RF common port, shunt said second RF input signal to a ground, and when SW is non-operative, While said second switch transistor group and said second shunt transistor group operate, Become non-operative [said first switch transistor group and said first shunt transistor group], and by that cause, An RF switching circuit which passes said second RF input signal to the aforementioned RF common port, and shunts said first RF input signal to a ground, and is manufactured on an ultra-thin silicon ("UTSi") substrate,
(b) A control logic block which is combined with the aforementioned RF switching circuit and outputs the aforementioned switch control signal (SW) and the aforementioned reversing-switch control signal (SW_),
(c) A negative voltage generator which it is combined with the aforementioned control logic block, and a clock input signal and positive power supply voltage of an external power are supplied, and outputs negative power supply voltage,
(d) An oscillator which outputs a clock input signal,
(e) A charge pump which is combined with the aforementioned oscillator which inputs the aforementioned clock input signal, and outputs negative power supply voltage,
(f) A logic circuit block which outputs a control signal which is combined with the aforementioned charge pump and used for control of the aforementioned switch transistor group and the aforementioned shunt transistor group,
(g) A level shift circuit which decrease in number a gate drain, a gate source, and drain source voltage of an MOSFET transistor used in order to be combined with the aforementioned logic circuit block and the aforementioned RF switching circuit and to realize the aforementioned transistor group,
(h) An RF buffer circuit which is combined with the aforementioned RF switching circuit and separates RF signal energy from the aforementioned electric charge pump block and the aforementioned logic circuit block,
An RF switching circuit integrated by ****** completeness.
[Claim 19]
The aforementioned charge pump,
(a) At least two P channel MOS FET transistors,
(b) An N-channel metal oxide semiconductor FET transistor which it is at least two N-channel metal oxide semiconductor FET transistors, and each is combined with each related P channel MOS FET transistor and series, and forms each leg of the aforementioned charge pump by it,
(c) At least one joint capacitor which combines each leg of the aforementioned charge pump combined with a continuation leg,
(d) An output capacitor combined with an output leg of the aforementioned charge pump,
An implication,

Since the aforementioned P channel MOS FET transistor and the aforementioned N-channel metal oxide semiconductor FET transistor are driven for the aforementioned negative power supply voltage, The RF switching circuit according to claim 18 which is generated with the aforementioned charge pump by using a non-overlapping input clock signal, and charging and discharging alternately the aforementioned joint capacitor and the aforementioned output capacitor and which was integrated completely.
[Claim 20]
The RF switching circuit according to claim 19 where a first non-overlapping clock control signal controls P channel transistor including two non-overlapping clock control signals in the aforementioned non-overlapping input clock signal, and a second non-overlapping clock control signal controls N channel transistor and which was integrated completely.
[Claim 21]
The RF switching circuit according to claim 19 whose aforementioned P channel transistor and aforementioned N channel transistor are single threshold value transistors and which was integrated completely.
[Claim 22]
The RF switching circuit according to claim 19 where the aforementioned non-overlapping input clock signal is generated by pulse shift circuit and which was integrated completely.
[Claim 23]
The RF switching circuit according to claim 19 where the aforementioned non-overlapping input clock signal is pulled out from the aforementioned oscillator clock input signal and which was integrated completely.
[Claim 24]
The RF switching circuit according to claim 19 where the aforementioned oscillator contains a relaxation oscillator and which was integrated completely.
[Claim 25]
The RF switching circuit according to claim 19 where the aforementioned non-overlapping input clock signal changes by a voltage swing from -Vdd to +Vdd and which was integrated completely.
[Claim 26]
The RF switching circuit according to claim 18 where the aforementioned level shift circuit contains two or more inverters combined with both feedback composition and which was integrated completely.
[Claim 27]
In the aforementioned inverter, the aforementioned level shift circuit including a first difference input, a second difference input, a logic input, and fanout,
(a) Are an input inverter group containing two input differential inverters, and a first input differential inverter receives a logic-input signal (input), An input inverter group to whom a first logic-input signal (in) is outputted, and a second input differential inverter receives said first logic-input signal (in), and outputs reverse (in_) of said first logic-input signal,
(b) He is a first inverter group containing three differential inverters, The aforementioned fanout of a first inverter in said first inverter group, It is combined with said first logic-input signal (in), and the aforementioned fanout of said first inverter, It is combined with a first difference input of output inverters in said first inverter group, The aforementioned fanout of a second inverter in said first inverter group, A first inverter group to whom it is combined with a second difference

input of the aforementioned output inverters in said first inverter group, and said first inverter group's aforementioned output inverters output a first output signal (out),
(c) He is a second inverter group containing three differential inverters, The aforementioned fanout of said second inverter group's first inverter, It is combined with said reverse (in_) of said first logic-input signal, and the aforementioned fanout of said first inverter in said second inverter group, It is combined with a first difference input of output inverters in said second inverter group, The aforementioned fanout of a second inverter in said second inverter group, It is combined with a second difference input of the aforementioned output inverters in said second inverter group, and the aforementioned output inverters in said second inverter group contain said second inverter group who outputs a second output signal (out_),
Said first output signal (out) is supplied as feedback, It inputs into a logic-input part of said second inverter in said second inverter group, The RF switching circuit according to claim 26 which said second output signal (out_) is supplied as feedback, and is input into a logic-input part of said second inverter in said first inverter group and which was integrated completely.
[Claim 28]
The RF switching circuit according to claim 27 where said first output signal and said second output signal control the aforementioned switch transistor group and the aforementioned shunt transistor group of the aforementioned RF switch and which was integrated completely.
[Claim 29]
The RF switching circuit according to claim 26 which shifts direct current level of the aforementioned logic-input signal (input) without the aforementioned level shift circuit affecting a frequency response of the aforementioned input signal and which was integrated completely.
[Claim 30]
The aforementioned RF buffer circuit includes two stage circuits including the 1st step level shift circuit and the 2nd step RF buffer circuit, Said 1st step level shift circuit includes a level shift circuit defined by Claim 27, In said 2nd step RF buffer circuit, said two or more second differential inverters have a first difference input, a second difference input, a logic input, and fanout including two or more second differential inverters, respectively, and said 2nd step RF buffer circuit is further,
(a) He is a first RF buffer inverter group containing three differential inverters, The aforementioned logic input of a first inverter in said first RF buffer inverter group and a second inverter by the aforementioned level shift circuit, It is combined with said first output signal (out) output, and the aforementioned fanout of said first inverter in said first RF buffer inverter group, It is combined with a first difference input of output inverters in said first RF buffer inverter group, The aforementioned fanout of said second inverter in said first RF buffer inverter group, A first RF buffer inverter group to whom it is combined with a second difference input of the aforementioned output inverters in said first RF buffer inverter group, and said first RF buffer inverter group's aforementioned output inverters output a first output signal (OUT),
(b) He is a second RF buffer inverter group containing three differential inverters, The aforementioned logic input of a first inverter in said second RF buffer inverter group and a second inverter by the aforementioned level shift circuit, It is combined with said second output signal (out_) output, and the aforementioned fanout of said first inverter in said second RF buffer inverter group, It is combined with a first difference input of output inverters in said second RF buffer inverter group, The aforementioned fanout of said second inverter in said second RF buffer inverter group, A second RF buffer inverter group to whom it is combined with a second difference input of the aforementioned output inverters in said second RF buffer inverter group,

and said second RF buffer inverter group's aforementioned output inverters output a second output signal (OUT_),
******, the RF switching circuit according to claim 18 integrated completely.
[Claim 31]
The RF switching circuit according to claim 30 where the aforementioned RF buffer circuit separates a digital logic signal from the aforementioned RF switching circuit and which was integrated completely.
[Claim 32]
Said 2nd step RF buffer circuit does not supply feedback of the aforementioned output signal OUT and OUT_ to said 1st step level shift circuit, but it by it, The RF switching circuit according to claim 31 which improves separation of the aforementioned RF switch from the aforementioned digital logic signal and which was integrated completely.
[Claim 33]
The RF switching circuit according to claim 30 where a transistor used in order to realize said 1st step level shift circuit is smaller than a transistor used in order to realize said 2nd step RF buffer circuit and which was integrated completely.
[Claim 34]
A voltage divider circuit combined with the aforementioned output signal (out) and (out_) is included further, The RF switching circuit according to claim 27 where the aforementioned voltage divider circuit restricts a voltage level of the aforementioned output signal, and the aforementioned output signal is supplied to said second inverter of said 1st inverter group and said 2nd inverter group as feedback after that and which was integrated completely.
[Claim 35]
The RF switching circuit according to claim 34 where the aforementioned voltage divider circuit restricts the aforementioned voltage level to Vdd substantially and which was integrated completely.
[Claim 36]
The aforementioned voltage divider contains two or more MOSFET devices combined with both series constitution, The RF switching circuit according to claim 34 where an output MOSFET device is combined with a ground node via a ballast-resistances machine, and the aforementioned MOSFET device performs a diode function and which was integrated completely.
[Claim 37]
The aforementioned RF buffer circuit includes two stage circuits including the 1st step level shift circuit and the 2nd step RF buffer circuit, Said 1st step level shift circuit includes a level shift circuit defined by Claim 34, Said 2nd step RF buffer circuit contains two or more second differential inverters, said two or more second differential inverters include a first difference input, a second difference input, a logic input, and fanout, respectively, and said 2nd step RF buffer circuit is further,
(a) Are a first RF buffer inverter group containing three differential inverters, and the aforementioned logic input of a first inverter in said first RF buffer inverter group by the aforementioned level shift circuit, It is combined with a first output signal (out_pos1) output, and the aforementioned logic input of a second inverter in said first RF buffer inverter group by the aforementioned level shift circuit, It is combined with a second output signal (out_neg1) output, and the aforementioned output of said first inverter in said first RF buffer inverter group, It is combined with a first difference input of output inverters in said first RF buffer inverter group, The aforementioned fanout of said second inverter in said first RF buffer inverter group, A first

RF buffer inverter group to whom it is combined with a second difference input of the aforementioned output inverters in said first RF buffer inverter group, and said first RF buffer inverter group's aforementioned output inverters output a first output signal (OUT),
(b) Are a second RF buffer inverter group containing three differential inverters, and the aforementioned logic input of a first inverter in said second RF buffer inverter group by the aforementioned level shift circuit, It is combined with the 3rd output signal (out_pos2) output, and the aforementioned logic input of a second inverter in said second RF buffer inverter group by the aforementioned level shift circuit, It is combined with the 4th output signal (out_neg2) output, and the aforementioned output of said first inverter in said second RF buffer inverter group, It is combined with a first difference input of output inverters in said second RF buffer inverter group, The aforementioned fanout of said second inverter in said second RF buffer inverter group, It is combined with a second difference input of the aforementioned output inverters in said second RF buffer inverter group, and said second RF buffer inverter group's aforementioned output inverters contain a second RF buffer inverter group who outputs a second output signal (OUT_),
Said first output signal (out_pos1) includes an output to which the buffer of said first inverter in said first inverter group of the aforementioned level shift circuit was carried out, Said second output signal (out_neg1) includes an output to which the buffer of said second inverter in said first inverter group of the aforementioned level shift circuit was carried out, Said 3rd output signal (out_pos2) includes an output to which the buffer of said first inverter in said second inverter group of the aforementioned level shift circuit was carried out, The RF switching circuit according to claim 18 where said 4th output signal (out_neg2) includes an output to which the buffer of said second inverter in said second inverter group of the aforementioned level shift circuit was carried out and which was integrated completely.
[Claim 38]
The RF switching circuit according to claim 20 which the aforementioned non-overlapping input clock signal is input into a level shift circuit defined by Claim 34, and is input into the account charge pump of back to front and which was integrated completely.
[Claim 39]
The aforementioned level shift circuit includes a first level shift circuit and a second level shift circuit, Said first level shift circuit and said second level shift circuit are defined by Claim 34, Said first level shift circuit outputs a first output signal (clk1pos) from the aforementioned fanout of said first inverter in the first inverter group, A second output signal (clk1neg) is outputted from the aforementioned fanout of said second inverter in the first inverter group, The 3rd output signal (clk1pos_) is outputted from the aforementioned fanout of said first inverter in the second inverter group, The 4th output signal (clk1neg_) is outputted from the aforementioned fanout of said second inverter in the second inverter group, Said second level shift circuit outputs a fifth output signal (clk2pos) from the aforementioned fanout of said first inverter in the first inverter group, A sixth output signal (clk2neg) is outputted from the aforementioned fanout of said second inverter in the first inverter group, A seventh output signal (clk2pos_) is outputted from the aforementioned fanout of said first inverter in the second inverter group, The RF switching circuit according to claim 38 which outputs an eighth output signal (clk2neg_) from the aforementioned fanout of said second inverter in the second inverter group and which was integrated completely.
[Claim 40]

Said 3rd output signal (clk1pos_) controls a first P channel MOS FET transistor of the aforementioned charge pump, Said 4th output signal (clk1neg_) controls a second P channel MOS FET transistor of the aforementioned charge pump, Said fifth output signal (clk2pos) controls a first N-channel metal oxide semiconductor FET transistor relevant to said first P channel MOS FET transistor, The RF switching circuit according to claim 39 where said sixth output signal (clk2neg) controls a second N-channel metal oxide semiconductor FET transistor relevant to said second P channel MOS FET transistor and which was integrated completely.
[Claim 41]
(a) A step which inputs a first RF input signal into a first switch transistor group containing two or more lamination transistors and a first shunt transistor group,
(b) A step which inputs a second RF input signal into a second switch transistor group containing two or more lamination transistors and a second shunt transistor group,
(c) While operating said first switch transistor group, While making said second switch transistor group non-operative, make said first shunt transistor group non-operative, operate said second shunt transistor group simultaneously, and by it, A step which passes said first RF input signal and makes said second RF input signal shunt,
(d) While operating said second switch transistor group, While making said first switch transistor group non-operative, make said second shunt transistor group non-operative, operate said first shunt transistor group simultaneously, and by it, A step which passes said second RF input signal and makes said first RF input signal shunt,
How to switch ****** and an RF signal.

[A Written Amendment]
[Filing date]Heisei 16(2004) June 9 (2004.6.9)
[Amendment 1]
[Document to be Amended]Description
[Item(s) to be Amended]Whole sentence
[Method of Amendment]Change
[The contents of correction]
[Document Name]Description
[0001]
The cross-reference of a related provisional application claim of priority
The present invention is the U.S. provisional application 60th under pendency / No. 328,353 (on October 10, 2001). [and] About the name "silicon on insulator (Silicon-On-Insulator) RF switch", the profits of the 119 sections of U.S. code [35th piece] (e) item were asserted, and the contents are used for this Description as a whole.
[Field of the Invention]
[0002]
The background of invention
The field of invention
Especially the present invention relates to the switching circuit in an integrated circuit, and the switching method of a high frequency (RF) signal about a switch. According to one embodiment, the CMOS device realized on [for using it in the field of application of RF, such as a wireless communication equipment, a satellite, and cable TV,] a silicon on insulator (SOI) is contained in this switching circuit.

[Background of the Invention]
[0003]
The description of a pertinent art
As everyone knows, the high frequency (RF) switch serves as an important configuration block in many wireless communication systems. The RF switch is used for the communication equipment with which many, such as a cellular phone, a wireless pager, wireless infrastructure equipment, satellite communication equipment, and cable TV equipment, differ. As everyone knows, it opts for the performance of an RF switch by the three main performance parameters of operation, i.e., insertion loss, switch separation, and a "1-dB compression point." These three performance parameters are connected closely, and in the design of an RF switch component, when they think any one parameter as important, other parameters will be sacrificed for them. The 4th parameter sometimes taken into consideration in an RF switch design is usually called switching time or switching speed (one side of a switch is turned ON and defined as time required to turn OFF an opposite side). In the design of an RF switch, the ease of RF switch accumulation, a degree (level), complexity, the yield, a returned-goods loss, and a manufacturing cost are contained in other important indices.
[0004]
The performance parameter of these RF switches can be more easily described with reference to the RF switch design by the advanced technology shown in the simple circuit diagram of Fig.1 a - 1c. The simple circuit diagram of single-pole single-throw (SPST) RF switch 10 of the advanced technology is shown in Fig.1 a. The switching transistor M1 (5) and the shunt transistor M2 (7) are contained in SPST switch 10 of the advanced technology. If Fig.1 a is referred to here, it will be dependent on the state of two MOSFET transistors M1 (5) and the control voltage of M2 (7) (). Namely, depending on the DC bias applied to the gate input part of the MOSFET switching transistor M1 and the shunt transistor M2, respectively an RF signal, It is sent to the RF output node 3 from the RF input node 1, or shunts via the shunt transistor M2 (7) in a ground. The actual value of DC bias voltage is dependent on MOSFET transistor M1 (5), and the polarity of M2 (7) and a threshold value. An RF power signal and the in-series resistor R0 (9) separate bias from a power supply signal, and are indispensable for the highest switch performance. "ON" state of RF switch 10 in Fig.1 a is shown in Fig.1 b (that is, to Fig.1 b). RF switch 10 shows the equivalent small signal value of the transistors M1 and M2 in case "ON" and the switching transistor M1 (5) are [ON and the shunt transistor M2 (7)] OFF. "OFF" state of the switch 10 of Fig.1 a is shown in Fig.1 c (that is, RF switch 10 shows the equivalent small signal value of the transistors M1 and M2 in case "OFF" and the switching transistor M1 (5) are [OFF and the shunt transistor M2 (7)] ON to Fig.1 c).
[0005]
As shown in Fig.1 b, when RF switch 10 is ON, the switching transistor M1 (5) is mainly resistance, and, on the other hand, its shunt transistor M2 (7) is mainly capacitive. "Insertion loss" of RF switch 10 is determined from the difference between the maximum available electric power in the input node 1, and the electric power supplied to the load of the output node 3. In a low frequency wave, when the switch 10 is ON (Fig.1 b should be referred to), each power loss originates in the on resistance 13 "r" with the limited switching transistor M1 (5). Typically, the on resistance r13 (Fig.1 b) is much smaller than the power-resistors machine R0 (9). Therefore, insertion loss "IL" has the characteristics like the formula 1 shown below.
Formula 1: IL is equal to 10 r/R0ln(10) =0.087r (dB) substantially.
[0006]

Therefore, the value of r serves as insertion loss of about 0.25 dB as a result at 3ohms by a low frequency wave. Since insertion loss is largely influenced by the on resistance of an RF switch transmitter, it lowers transistor on resistance and can improve insertion loss by decreasing parasitism board resistance.

[0007]

Generally, input-output separation (or simply switch separation) of an RF switch is determined by measuring the electric energy which "flows" out of an input port into an output port, when the transistor which has connected the input port and the output port is OFF. As for separation characteristics, the degree of cutting of an RF switch shows how much (that is, how much does a switch block an input signal from an output?). If "OFF" state of RF switch 10 in Fig.1 c is referred to especially here, the OFF state of the switch M1 (5) will serve to block the input 1 from the output 3. The shunt transistor M2 (7) serves to improve input-output separation of the switch 10.

[0008]

When a turn-off is carried out (namely, when RF switch 10 and the switching transistor M1 (5) carry out a turn-off) M1 (5), It is mainly capacitive and "feed through" (an RF input signal should pass from the input node 1 to the output node 3) of an input signal, The capacitor CGD OFF 15 (gate drain capacitance when the switching transistor M1 carries out a turn-off), Capacitor CGS OFF 17 (when the switching transistor M1 carries out a turn-off) The series / parallel value of a ** gate source capacitance, and capacitor CDS1 (19) and (a drain source capacitance when the switching transistor M1 carries out a turn-off) determine. The feed through of an input signal relates to input-output separation of RF switch 10 directly desirably. The size of feed through is decreased using the shunt transistor M2 (7), and the separation characteristics of an RF switch are improved by it.

[0009]

When the switching transistor M1 (5) is a turn-off, turn-on of the shunt transistor M2 of Fig.1 c (7) is carried out. In this condition, the shunt transistor M2 (7) mainly works as a resistor of the value r. Depending on a design, the value of r is much smaller than impedance peculiar to RF power. As a result, r decreases remarkably the voltage of the input part of the switching transistor M1 (5). When the value of r is much smaller than the power resistors R0 (9) and feed-through capacitive resistance of the shunt transistor M2 (7), separation can be calculated easily. Switch separation of the OFF state of RF switch 10 is determined with the difference between the maximum available electric power of an input part, and the electric power of an outputting part.

[0010]

It is the capability to process the input power with another, important big RF switch performance characteristic in addition to the insertion loss of an RF switch, and separation. When turn-on of the switch is carried out, this is fixed frequency and is making for insertion loss not to serve as a function of input power into a positive thing. It is called for by many field of application that a switch cannot be distorted in the electric power sent through the switch which carried out "switch-on." For example, when two sounds which approached pass an RF switch simultaneously, they may start an intermodulation (IM) for the nonlinearity of a switch, and may generate a pseudo voice by the channel which adjoins by that cause. For example, when securing these adjoining channels for the information signal, the electric power of a pseudo voice must be maintained as small as possible. Switch compression or a "1-dB compression point" ("P1dB") shows the capability to process electric power. P1dB, it defines as input power when insertion loss increases only 1 dB from the low-electric-power value. Or when it has another way of

speaking, a 1-dB compression point is a degree of the electric energy which can be input into an RF switch in an input port, before output power of only 1 dB deviates from linear relation with input power.
[0011]
Switch compression is generated in any one of the two routes. In order to understand how switch compression occurs, it describes about operation of the MOSFET transistor shown in RF switch 10 of Fig.1 a - 1c. In order to carry out turn-on of the MOSFET as everyone knows in the transistor design field, the gate source bias exceeding threshold voltage Vt is required. Similarly, gate source bias must be smaller than Vt, in order for a switch to be come by off. Vt is positive in "N type" MOSFET, and negative in "P type" MOSFET. N-channel MOS FET is chosen as RF switch 10 of Fig.1 a - 1c. The source of N-channel MOS FET is a node of the lowest electric potential.
[0012]
If Fig.1 c is referred to again and the shunt transistor M2 (7) will carry out turn-on to the part period of an input signal cycle as a result of the transient voltage of the shunt transistor M2 (7), input power will be sent to a ground and will be lost to an output. The loss of this electric power will increase, if input power increases (namely, input signal of the electric power which increased), and thereby, it causes a first type of compression. The 1-dB compression point of RF switch 10 is determined by the signal vibration of the input in the point it stops in the shunt transistor M2 (7) which carried out the turn-off keeping [OFF / point] not been. After all, a negative vibration of an input is lower than a ground, and becomes lower than M2 gate potential in a similar manner (therefore, it source-izes). If this difference becomes equal to Vt, the transistor M2 (7) will begin to carry out turn-on, and compression will start. This first type of compression is caused by the turn-on phenomenon of the no MARIOFU type gate in the shunt leg of an RF switch. Once the shunt transistor M2 (7) carries out turn-on, the electric power of the output node 3 will not follow the electric power of a switch input part any longer at linearity. A second type of RF switch compression is generated when the source and drain of the shunt transistor M2 (7) carry out breakdown on excessive voltage. This voltage has only the possibility exceeding service voltage direct-current abbreviation+1V to a submicron silicon on insulator (SOI) device. In breakdown, a shunt device begins to conduct a lot of electric power, and the electric power which can be used with an output by that cause decreases.
[0013]
The simple figure of single pole double throw (SPDT) RF switch 20 by the advanced technology is shown in Fig.2. As shown in Fig.2, four MOSFET transistors 23, 24, 27, and 28 are contained in RF switch 20 of the advanced technology at worst. The transistors 23 and 25 work as a "path" or a "switching" transistor (to switching MOSFET transistor M1 (5) and the appearance of drawing 1 a-1c), It is constituted so that each of these related RF input node may be combined with RF node 25 common in alternative. For example, when operating, the switching transistor 23 combines the first input signal "RF1" that is an input to the first RF input node 21 to the RF common nodes 25 (namely, when switched to "ON"). Similarly, when operating, the switching transistor 24 combines the second RF input signal "RF2" which is an input to the second RF input node 22 to the RF common nodes 25. The shunt transistors 27 and 28 by the case where it is operating those related RF input nodes, When not having combined with the RF common nodes 25, it works in order to shunt each related RF input node to a ground in alternative (namely, when the turn-off of the switching transistor (23 or 24) connected to those related input nodes is carried out).

[0014]
In order to control operation of the RF switch of the advanced technology to be shown in Fig.2, two control voltage is used. The control voltage with the name of "SW" and its reverse "SW_" controls operation of the transistors 23, 24, 27, and 28. control voltage is an alternative about the pair of the selected transistor ---like -- an operation (turn-on) -- or it is adjusted so that it may be made non-operative (turn-off). For example, as shown in Fig.2, SW turns on (according to some embodiments). When this is determined by setting control voltage to a voltage level logically "high", for example, "+Vdd", the switching transistor 23 is operating and the related shunt transistor 28 also operates. However, reverse SW_ of SW controls operation and its related shunt transistor 27 of the second switching transistor 24, and control signal SW_, during ON (according to some embodiments, this is determined by setting SW_ as -Vdd) of SW, since it is off, these two transistors are non-operative in this same period -- or the turn-off is carried out. RF1 input signal is combined with the RF (passing switching transistor 23 which is operating) common port 25 in this state (in SW, SW_ turns off by ON). Since the turn-off of the second switching transistor 24 is carried out, RF2 input signal is blocked from the RF common port 25. Moreover, since an RF2 input signal is shunted in a ground via the shunt transistor 28 which is operating, it is further separated from the RF common port 25. When [whose SW control signal is "OFF" (and SW_ "ON") like] it will be understood easily, the person skilled in the art of the transistor design field, RF2 signal is the same method and is combined with the RF common port 25 (and RF1 signal is shunted to a block ** leg round).
[0015]
RF switches, such as SPDF, RF switch 20, etc. of Fig.2, have so far been realized with the result on various performances in different element technology including a bulk complementary metal oxide semiconductor (CMOS) and gallium arsenide (GaAs) technology. In fact, GaAs technology is being used for almost all highly efficient high frequency switches. In realization of the RF switch by the advanced technology, although it has tried to improve the above-mentioned RF switch performance characteristic, those results are miscellaneous and are various. [of the complexity of an integrated circuit and the degree of the yield] For example, bulk CMOS and an RF switch show a high insertion loss performance characteristic, the low compression performance characteristic, and an insufficient linearity performance characteristic to a disadvantageous thing. By contrast, for semi insulating [of GaAs material], the parasitism board resistance can decrease remarkably and, thereby, can decrease switch insertion loss. Similarly, a half-insulation GaAs substrate improves switch separation.
[0016]
Although improvement in a performance characteristic is brought about by realization of a GaAsRF switch, this technology has some faults. For example, the yield of the integrated circuit which functions normally in GaAs technology is comparatively low. It tends to become expensive [a design and manufacture] comparatively [a GaAsRF switch]. In addition, although GaAs switches improve an insertion loss characteristic as mentioned above, frequency restrictions may become low for the slow surface state which exists in a GaAs substrate. Since this technology is not fit for integration of the high level, an "off-chip" needs to realize the digital control circuit relevant to an RF switch from a switch. It turns out that the low-electric-power circuit relevant to a switch is difficult to be accumulated. Since this makes overall system cost or manufacturing cost, size, and complexity increase and decreases the throughput speed of a system similarly, it is disadvantageous.
[Description of the Invention]

[Problem to be solved by the invention]
[0017]
Therefore, it is desirable to provide the method of switching the RF switch and RF signal which have an improved performance characteristic. It is desirable to provide the RF switch which insertion loss, separation, and compression have improved especially. Design manufacture of such an RF switch was completed easily, it was manufactured comparatively inexpensive, and is fit for accumulation of the high level, and it is desirable that it is applicable from a low frequency wave to high frequency. It should enable it to accumulate a power control circuit on chip simply with a switch function. Such accumulation was difficult to realize until now using a Si substrate and a GaAs substrate. The present invention provides such an RF switch and the switching method of an RF signal.
[Means for solving problem]
[0018]
The outline of invention
It describes about the switching method of a new RF switching circuit and an RF signal. An RF switch is usable for a wireless use, and can be manufactured with silicon on insulator technology. In one embodiment, an RF switch is manufactured on an ultra-thin silicon ("UTSi") substrate. The following thing is contained in an RF switch in one embodiment. Namely, the first switching transistor group who is connected to the input part for receiving an RF signal, the input part for receiving an RF signal, and RF common port, and is controlled by switching voltage (SW), It is connected to a first switching transistor group and RF common port, The second switching transistor group controlled by switching voltage (SW_) is contained, and SW_ is the reverse of SW, and when a first switching transistor group is ON, a second switching transistor group is come by off. A switching transistor group connects each RF input signal to RF common port in alternative, while operating. In this embodiment, it is combined with an RF switch by the switching transistor group again, and the shunt transistor group controlled by the switching voltage SW and SW_ is contained. While operating, a shunt transistor group works so that those related RF input nodes may be shunted to a ground in alternative, and improves RF switch separation by it.
[0019]
One or more MOSFET transistors connected by lamination or series constitution are contained in both switching and a shunt transistor group. Within each transistor group, the gate of a lamination transistor is usually controlled by switching voltage (SW or SW_), and this switching voltage is combined with each transistor gate via each gate resistance machine. The compression point of a switch increases with lamination and the gate resistance machine of a transistor group device. The RC time constant formed of the gate resistance machine and gate capacitance of MOSFET is designed to become much longer than the cycle of an RF signal, and RF voltage is equally shared with the whole series-connection device. By this composition, the 1-dB compression point of an RF switch increases.
[0020]
It describes about the RF switch integrated completely. A digital switch control logic circuit and the negative power-supply-voltage generator accumulated with the RF switch of the present invention are contained in this RF switch. According to one embodiment, the RF switch of the advanced technology is provided with some functions not existing by the RF switch integrated completely. For example, in one embodiment, to the RF switch integrated completely. The built-in type oscillator which supplies a clock input signal to a charge pump circuit, and the charge

pump circuit which generates the negative power supply voltage which other RF switching circuits need and which were accumulated, The CMOS logic circuit which generates the control signal which controls RF switch transistor, The level shift circuit and low current voltage divider circuit which increase the reliability of a switch device, and the RF buffer circuit which separates RF signal energy from a charge pump circuit and a digital control logic circuit are included. It describes about some embodiments of a charge pump circuit, a level shift circuit, a voltage divider, and an RF buffer circuit. By the RF switch of the present invention, insertion loss, switch separation, and switch compression are improved. Thanks to the accumulation of a higher level which becomes available with the RF switch of the present invention, by using the present invention, a design and manufacturing cost of RF system decrease, and reliability increases.

[0021]

In the following brief explanation of the drawings, the same reference mark of various Drawings shows the same component.

[Best Mode of Carrying Out the Invention]

[0022]

DETAILED DESCRIPTION

It should let this Description pass and the preferable embodiment and working example to clarify should be considered as an illustration thing rather than the limitation to the present invention.

[0023]

The RF switch of the present invention

The present invention is a method for switching a new RF switch design and RF circuit. The first illustration embodiment of RF switch 30 of the present invention is shown in Fig.3. As shown in Fig.3, in one embodiment, four clusters or a "group" of an MOSFET transistor is contained in RF switch 30 of the present invention. These are shown in Fig.3 as the transistor groups 33, 34, 37, and 38. A "path" or "switching" transistor groups 33 and 34 are contained in two transistor groups, and the shunt transistor groups 37 and 38 are contained in two transistor groups. One or more MOSFET transistors arranged at series constitution are contained in each transistor group. For example, in the embodiment shown in Fig.3, three switching transistor M33A, M33B, and M33C are contained in the switching group 33. Similarly, three switching transistor M34A, M34B, and M34C is contained in the switching group 34. Three transistor M37A, M37B, and M37C are contained in the shunt group 37. Similarly, three transistor M38A, M38B, and M38C are contained in the shunt group 38. Although the transistor groups 33, 34, 37, and 38 are shown in Fig.3 as a thing containing three MOSFET transistors, The person skilled in the art of the RF switch design field will be understood [that a substitute group configuration can be used and], without deviating from the range or the meaning of the present invention. For example, without deviating from the range of the present invention so that it may describe in detail by the following, any convenient number of transistors can be used and the group who shows Fig.3 can be realized.

[0024]

In one embodiment of the RF switch of the present invention, an MOSFET transistor (for example, transistor M37A, M37B, and M37C) is realized using the substrate silicon on insulator (SOI) technology insulated completely. So that it may describe in detail by the following especially the MOSFET transistor of the RF switch of the present invention, It realizes using "ultra-thin silicon (Ultra-Thin-Silicon) (UTSi)" (in this Description, it is called "ultra-thin silicon on sapphire (ultrathin silicon-on-sapphire)") technology. In accordance with a UTSi manufacturing method, the transistor used in order to realize the RF switch of the present

invention is formed in the ultra-thin layer of the silicon in an insulating sapphire wafer. Perfect insulating silicon on sapphire improves the performance characteristic of the RF switch by the present invention by decreasing the harmful joint effect of a substrate relevant to a non-insulating substrate and a semi insulating substrate. For example, an improvement of insertion loss lowers the on resistance of a transistor, and is realized by decreasing parasitism board resistance. Switch separation improves using the perfect insulating substrate provided by UTSi technology. Thanks to insulation with perfect silicon on sapphire technology, as compared with bulk CMOS and other conventional integrated circuit production technology, the parasitism capacitance between the nodes of RF switch 30 decreases remarkably. As a result, in the RF switch of the present invention, switch separation is improved as compared with the RF switch design of the advanced technology.

[0025]

A transistor group is controlled by the two control signals SW and reverse SW_ of those like the switch described above in relation to Fig.2 to be shown in Fig.3.A control signal is combined with the gate of each transistor via each related gate resistance machine. For example, three transistors [in / in the control signal SW / the switching transistor group 33] (M 33A) Operation of M33B and M33C is controlled via the gate resistance machine (R33A, R33B, and R33C) relevant to three each. The control signal SW is input into input node 33', and controls the switching transistor group 33. SW is input into input node 38', and controls the shunt transistor group 38 again. Similarly, reverse SW_ of SW controls the switching transistor group 34 via input node 34'. SW_ is input into input node 37', and controls the shunt transistor group 37 again.

[0026]

In one embodiment, although about 30K ohm of a resistor is contained in a transistor group's resistor, substitute resistance can be used, without deviating from the meaning or the range of the present invention. In some embodiments of the present invention, any resistance element which has comparatively high resistance is contained in a gate resistance machine. For example, in one embodiment, a gate resistance machine may be realized using a reverse bias diode. A gate resistance machine is useful to increase the effective breakdown voltage of the whole series-connection transistor so that it may describe in detail by the following.

[0027]

Function as controlling a control signal about the transistor groups' 33, 34, 37, and 38 operation, and un-operating, and RF switch 30, or [passing an RF signal in a way similar with controlling the analog transistor of the switch in Fig.2 generally] -- or it functions as blocking. Especially the switching transistor groups 33 and 34 function as a path transistor or a switching transistor, and in alternative, they are constituted so that each related RF input node may be combined with common RF node 35. For example, if the switching transistor group 33 operates, he will combine with the RF common nodes 35 the first RF input signal "RF1" that is an input to the first RF input node 31. Similarly, if the switching transistor group 34 operates, he will combine the second RF input signal "RF2" which is an input to the second RF input node 32 to the RF common nodes 35. The shunt transistor groups 37 and 38, If it operates, when those related RF input nodes will not have combined with the RF common nodes 35 () That is, when the turn-off of the switching transistor group (33 or 34) connected to the related input node is carried out, each related RF input node is committed so that it may shunt to a ground in alternative.

[0028]

In alternative, the group as which the transistor group chose control voltage is connected an operation or in order to make it non-operative. For example, as shown in Fig.3, when SW is ON

(according to some embodiments) This is determined when the control voltage SW is set as a voltage level logically "high", The switching transistor group 33 operates (that is, all the transistors of the group 33 carry out turn-on), and the related shunt transistor group 38 also operates (that is, all the transistors of the group 38 carry out turn-on). However, like operation of the switch in Fig.2, since the second switching transistor group 34 and its related shunt transistor group 37 are controlled, reverse SW_ of SW, These two transistor groups become non-operative in this period (that is, the turn-off of all of the groups' 34 and 37 transistor is carried out). Therefore, when SW is ON, RF1 input signal is combined with the RF common nodes 35. Since the switching transistor group 34 is off, RF2 input signal is blocked from the RF common nodes 35. Since RF2 input signal is shunted in a ground via the shunt transistor group 38 who operated, it is further separated from the RF common nodes 35. Like, RF2 signal is the same method when [whose SW control signal is OFF (SW_control signal. and ON)] the person skilled in the art of the RF switch design field will be understood, and it is combined with the RF common nodes 35 (and RF1 signal is shunted to a block ** leg round).

[0029]

As shown in RF switch 30 of the present invention in Fig.3, one to laminate an MOSFET transistor and use a gate resistance machine is making high breakdown voltage of the whole series-connection transistor. The RC time constant formed of the gate capacitance of a gate resistance machine and MOSFET is designed to become much longer than the cycle of an RF signal. So, RF energy does not almost have dissipating via a gate resistance machine. RF voltage is effectively shared equally with the whole series-connection transistor by this arrangement. As a net effect, the breakdown voltage of the whole series-connection device increases by n times the breakdown voltage of individual FET. In this case, n is the number of the transistors connected in series. By this composition, the 1-dB compression point of RF switch 30 of the present invention increases.

[0030]

In order to improve switch performance, the RC time constant must be made into big size to an RF signal cycle. This will impose restrictions on the minimum of R which can be used mainly for realizing gate transistors (gate resistance machine). As mentioned above, although the typical value for R is 30komega in one embodiment of the present invention, other resistance can also be used, without deviating from the range of the present invention. Since an MOSFET gate input part does not draw a direct current near, the bias in a device is not changed for the IR drop of this whole resistance.

[0031]

RF switch 30 of the present invention can respond to the input signal of the power level which increased at an advantageous thing. Thanks to the serial arrangement of an MOSFET transistor including a transistor group (33, 34, 37, and 38), the power signal which increased can be supplied to an RF input node (namely, input nodes 31 and 32), without having influence harmful to switching. The person skilled in the art of the transistor design field will be understood [that it can respond to a bigger input power level increasing the number of transistors for every transistor group, or by changing the physical configuration of a transistor, and]. For example, in one embodiment, the dimension of a transistor is about 0.5x2,100 micrometers. However, substitute composition can be used, without deviating from the range or the meaning of the present invention.

[0032]

a silicon on insulator (SOI) -- PRIOR ART

As reference was made above in the description of the RF switch in Fig.3, SOI technology is attractive in realization of an RF switch for insulation with a perfect insulating substrate. As everyone knows, a highly efficient microelectronics device is realized and SOI has mainly been used for the use which needs radiation resistance and high-speed operation. The junction wafer and silicon on sapphire which have the thin silicon layer joined to SIMOX and an insulating layer, for example are contained in SOI technology. In order to attain the above-mentioned desirable switch performance characteristic, in one embodiment, the RF switch of the present invention is manufactured on silicon on sapphire.

[0033]

In order to manufacture a device on an insulating substrate, it is necessary to use the effective method for forming a silicon CMOS device on an insulating substrate. It is well recognized by the advantage of using the composite board which contains single crystal semiconductor layers which carried out epitaxial deposition, such as silicon, in insulating supporting boards, such as sapphire, and these advantages, Using insulating materials, such as sapphire (aluminum2O3), a spinel, or a high insulating material of other well-known, as a substrate, when making it the electric conduction course of the leakage current between devices certainly pass a substrate, it is realizable.

[0034]

It can be defined as an "ideal" silicon on sapphire wafer containing a silicon layer without a defect in it with a perfect single crystal with sufficient thickness which can manufacture an active device. Probably this silicon layer adjoins an insulating substrate and the disorder of the crystalline lattice in a silicon insulator interface is the minimum. The early trial which is going to manufacture this "ideal" silicon on sapphire wafer suffered a setback for the problem for which many were conspicuous. these problems -- (1) -- the annealing of the silicon layer being carried out and the elevated temperature used for first epitaxial silicon deposition, and after that, The thing by which a contaminant, especially aluminum of a p type dopant enter into an epitaxial deposited silicon layer considerably as a high temperature result used in order to decrease the defect in it and to do, (2) -- it can summarize as a crystal property with an insufficient epitaxial silicon layer when various elevated temperatures which devote themselves and pose a problem through the method of an annealing and/or re-growth are avoided. [and]

[0035]

Although it turns out that a quality silicon thin film suitable for the severe device use of a demand can be manufactured on silicon on sapphire, The annealing of the composite at the low-temperature ion implantation for embedding at epitaxial deposition of the silicon layer on silicon on sapphire and a silicon layer, and forming an amorphous region and the temperature below about 950 degrees C is contained in the method at this time.

[0036]

The example and method of manufacturing such a silicon on sapphire device are described in the following Descriptions. They, US,5,416,043,B Description ("minimum electric charge FET manufactured on a super-thin film silicon on sapphire wafer" (Minimum chargeFET fabricated on an ultrathin silicon)) on sapphire wafer, US,5,492,857,B Description ("high frequency wireless communication system on a single ultra-thin film silicon on sapphire chip" (High-frequency wireless communication system)) on asingle ultrathin silicon on sapphire chip, US,5,572,040,B Description ("high frequency wireless communication system on a single ultra-thin film silicon on sapphire chip" (High-frequency wirelesscommunication system)) on a single ultrathinsilicon on sapphire chip, US,5,596,205,B Description ("high frequency wireless

communication system on a single ultra-thin film silicon on sapphire chip" (High-frequency wireless communicationsystem)) on a single ultrathin silicon on sapphire chip, US,5,600,169,B Description ("minimum electric charge FET manufactured on a super-thin film silicon on sapphire wafer" (Minimum charge FET fabricated on an ultrathin silicon)) on sapphire wafer, US,5,663,570,B Description ("high frequency wireless communication system on a single ultra-thin film silicon on sapphire chip" (High-frequency wireless communication system)) on a single ultrathin silicon on sapphire chip, US,5,861,336,B Description ("high frequency wireless communication system on a single ultra-thin film silicon on sapphire chip" (High-frequency wireless communication system)) on a single ultrathin silicon on sapphire chip, The US,5,863,823,B Description ("edge control in a silicon on insulator by which self align was carried out" (Self-aligned edge control in silicon on insulator)), US,5,883,396,B Description ("high frequency wireless communication system on a single ultra-thin film silicon on sapphire chip" (High-frequency wireless communication system)) on a single ultrathin silicon on sapphire chip, US,5,895,957,B Description ("minimum electric charge FET manufactured on a super-thin film silicon on sapphire wafer" (Minimum charge FET fabricated on an ultrathin silicon)) on sapphire wafer, US,5,920,233,B Description ("false side band) Phase-locked loop" Phase locked loop including a samplingcircuit for reducing spurious side band including the sampling circuit for decreasing, US,5,930,638,B Description ("how to manufacture low parasitic resistance on an ultra-thin silicon on insulator" (Method of making a low parastic resistor on ultrathin)) silicon on insulator, the US,5,973,363,B Description (on "ultra-thin silicon on insulator) The CMOS circuit which has the shortened P channel length" (CMOS circuitry with shortened P-channel length on ultrathin silicon on insulator), The US,5,973,382,B Description. ("The capacitor on the ultra-thin semiconductor on an insulator".) (Capacitor on ultrathin.) semiconductor on insulator and the US,6,057,555,B Description ("minimum electric charge FET manufactured on a super-thin film silicon on sapphire wafer" (High-frequency wireless)) It is communicationsystem on a single ultrathin silicon on sapphire chip. In the whole instruction about an ultra-thin silicon on sapphire integrated circuit design and manufacture, all of these reference patents are used for this Description.

[0037]

An electron device can be formed in the silicon ultra-thin layer on an insulating synthesis sapphire wafer using the method described in the patent referred to above. Typically, silicon layer thickness is less than 150 nm. The advantage of insulating silicon on sapphire is maximized by such "ultra-thin" silicon layer, and it becomes possible to accumulate a many function on a single integrated circuit. With thick silicon, it is [the conventional transistor separation well needed] less necessary, transistor processing is simplified, and circuit density increases. In order to distinguish the method and device which were referred to by these above from a former thick silicon embodiment, in this Description, these are collectively called "ultra-thin silicon on sapphire."

[0038]

In some preferable embodiments of the present invention, a MOS transistor, US,5,416,043,B, No. 5,492,857, No. 5,572,040, No. 5,596,205, No. 5,600,169, No. 5,663,570, No. 5,861,336, No. 5,863,823, No. 5,883,396, It forms in ultra-thin silicon on sapphire by the method disclosed in each Description of No. 5,895,957, No. 5,920,233, No. 5,930,638, No. 5,973,363, No. 5,973,382, and No. 6,057,555. However, the method of other well-known which manufactures an ultra-thin silicon on sapphire integrated circuit can be used, without deviating from the meaning or the range of the present invention.

[0039]
A quality silicon thin film suitable for the severe device use of a demand as claim for patent is described and carried out to these patents, It can manufacture on an insulating substrate by the method containing the annealing of the low-temperature ion implantation for embedding at epitaxial deposition of the silicon layer to an insulating-substrate top, and a silicon layer, and forming AMORUFASU, and the composite in the temperature below about 950 degrees C. Any processings which expose a silicon layer to the temperature over about 950 degrees C are carried out in oxidation ambient environment. There is area density of an active state to the region which was not intentional to the silicon thin film which forms a transistor, and was doped electrically [less than abbreviation 5x10 11cm-2].
[0040]
As reference was made above, a UTSi substrate is desirable for especially RF use. A perfect insulating substrate is because the harmful influence of the substrate combination relevant to the conventional substrate (that is, it is not completely insulation) is decreased. As a result, RF switch 30 of Fig.3 is manufactured on a UTSi substrate by one embodiment.
[0041]
RF switch design trade-off
When designing RF switch 30 of the present invention described above in relation to Fig.3 and realizing, some design parameters and a trade-off should be taken into consideration. The RF switch of the present invention can be prepared so that it may exceed whether a desired system design demand and RF switch performance objective are filled. It describes here about the design trade-off and the thing which should be taken into consideration which affect an RF switch design.
[0042]
As it described above in relation to Fig.3, RF switch 30 is realized using an MOSFET transistor, although "N type" or "P type" may be used. However, in order to realize an RF switch in a CMOS technology, N channel transistor is preferable. It is because one with preferable N channel transistor has "ON" resistance of N channel transistor much smaller than the case of P channel transistor to fixed transistor size. This is because the mobility in electronic silicon is high to an electron hole. Control voltage is chosen so that the on resistance of an "on-" transistor may decrease reliably. the time of an "off-" transistor being made non-operative again as for control voltage -- reliably -- OFF and ****** -- it chooses like.
[0043]
In the transistor design field, "ON" resistance is in inverse proportion to the difference between the voltage applied to a transistor gate, and the voltage applied to a transistor source in an N-channel metal oxide semiconductor transistor as everyone knows. This voltage is usually called "Vgs" (gate source voltage). Although it is noticing easily, In an input port (for example, first RF input node 31 in Fig.3), Therefore, as the size of an RF signal (Vs) increases in the RF common port 35, Vgs of an on-transistor decreases (for example, Vgs of transistor M33 A in the switching transistor group 33 decreases as the size of RF1 signal increases). For this reason, it becomes saying that gate control voltage (for example, SW of input node 33') should as just as possible be carried out. However, though regrettable, the degree which can just do gate control voltage is restricted due to concern of reliability.
[0044]
The same concern exists also to an "off-" transistor. It is important to note that an RF input signal (for example, RF1 input signal) generally vibrates involving zero reference voltage in application

of a typical RF switch. The off-transistor (for example, the shunt transistor group's 37 transistor) must remain in as at non-operative or a turn-off between the voltage deviation of an RF input signal positive and negative. From this, it will be said that gate control voltage (for example, SW_control voltage signal) of an off-transistor should be made negative as much as possible. Again, the degree as for which gate control voltage is made negative is restricted due to concern of reliability.

[0045]

The 1-dB compression point of a switch is restricted by the design of an off-transistor for a CMOS switch again. In the transistor design field, there is breakdown voltage fundamental between the source and drain by a MOS transistor as everyone knows. If the electric potential of device both ends exceeds this breakdown voltage, even when the gate potential which is going to maintain the transistor to the OFF state exists, high electric current flows between a source and a drain. an improvement of the compression in a switch increases the breakdown voltage of a transistor -- it can attain. One of the methods which manufactures the MOS transistor which has high breakdown voltage is increasing gate length. Regrettably, by the increase in gate length, the channel resistance of a device increases also inconvenient and, thereby, the insertion loss of a device increases. Although the channel resistance can decrease by making width of a device wide, this makes switch separation be deteriorated again. Therefore, a trade-off exists in a MOS switch.

[0046]

As it described above in relation to RF switch 30 of the present invention in Fig.3, a transistor is laminated to series constitution and the 1-dB compression point of a switch is improved. The effective breakdown voltage of the whole series-connection transistor is increased with the combination of the comparatively high gate resistance machine of a value, and the laminated constitution of the transistor in a transistor group. It is made for a RC time constant (the resistance of a gate resistance machine and the gate capacitance of MOSFET determine) to become much longer than the cycle of the RF signal which RF switch 30 processes in a design and manufacture of a switch element. As mentioned above, it increases by one n times the rate [laminated constitution and / in / as a net effect of the gate resistance machine of high resistance / comparatively / in the breakdown voltage of the whole series-connection transistor / an individual transistor] of breakdown voltage (here). n is equal to the number of the transistors connected to series in a transistor group.

[0047]

What should be further taken into consideration on a design is related with the "body tie" currently used in the conventional bulk CMOS transistor. In the transistor design field, a body tie combines a device with either a well or a substrate as everyone knows. The well substrate junction must always keep reverse bias applied. A source body and the drain body junction must always keep reverse bias applied. Generally, a well (N well technology) is combined with the greatest electropositive potential applied to a circuit in a bulk CMOS design. A substrate (P well technology) is combined with the greatest electronegative potential applied to a circuit. Since an RF input signal vibrates the upper and lower sides of a ground symmetrically, a CMOS switch design shows insufficient performance about insertion loss, separation, and a 1-dB compression point. It is preferable to realize RF switch 30 of the present invention on an insulating substrate for these and the above-mentioned Reason.

[0048]

By realizing the RF switch of the present invention on an insulating substrate, some advantages, such as an improvement of switch separation and reduction of insertion loss, are provided. The further advantage is acquired by realizing the RF switch of the present invention using UTSi technology. For example, as compared with realizing the RF switch of the advanced technology to GaAs, the improvement of the integrated circuit yield, reduction of a manufacturing cost, and the increase in an accumulation level are attained by using UTSi. In the integrated circuit design field, GaAs are not fit for integration of a high level as everyone knows. therefore, the digital control circuit relevant to operation and the function of the RF switch and other circuits (a negative voltage electric power supply generator circuit --) The level shift circuit, the low current voltage divider circuit, the RF buffer circuit, etc. must often realize with an off-chip (that is, these functions are easily [as an RF switch] umaccumulable). This is connected to the degradation of the RF switch realized with an increase in cost and the advanced technology.
[0049]
By contrast, according to invention of this RF switch, a circuit required for normal operation of an RF switch and a function is realizable for the same integrated circuit as the switch itself together using UTSi technology. For example, an RF switch is accumulable on the same integrated circuit by realizing an RF switch with UTSi technology with a CMOS control logic circuit required to control operation of a negative voltage generator and an RF switch so that it may describe in detail by the following. Thanks to reduction of the control line required to control operation of a switch, the complexity of an RF switch also decreases. An RF switch control logic circuit is realizable for an advantageous thing using a low-voltage CMOS transistor. Even if it is for high power RF switch realization, electric power can be comparatively supplied to the RF switch of the present invention using the external power of low electric power. These characteristics are advantageous as compared with realization of GaAs by the advanced technology. It is because it is required to use a power generation circuit required to realize an electric power supply the external power of high power, positive, and negative [both] comparatively in the case of GaAs. For example, in the illustration embodiment described below in relation to Fig.4 - 12, the RF switch of the present invention only needs one 3V single external power. In the switch by the advanced technology, the external voltage generation circuit for realizing at least one 6V external power and a positive and negative electric power supply is required typically.
[0050]
The RF switch integrated completely
To Fig.4, it manufactures according to the present invention, and it is illustration-like and the simple block diagram of RF switch 100 integrated completely is shown. As shown in Fig.4, to RF switch 100 integrated completely, The RF switch 30(simplified schematic representation shows Fig.4)CMOS control logic circuit 110 and the negative voltage generator circuit 120 (in one embodiment, it realizes using a "charge pump" circuit) of the present invention which were described by Fig.3 in the above are included.The control signal 130 is input CMOS logic circuit block 110. The control signal 130 will have it understood from 0 volt in one embodiment that other logic circuit levels can be used, without the person skilled in the art of the digital logic circuit design field deviating from the range or the meaning of the present invention in the range of +Vdd. For the Reason shown above, RF switch 100 integrated completely is manufactured on a UTSi substrate at one embodiment. However, other insulating-substrate technology can also be used.
[0051]

Some the functions and the characteristics which are not in the RF switch of the advanced technology in Fig.2 are included in RF switch 100 integrated completely so that it may describe in detail by the following. For example, RF switch 30 (as it described above in relation to Fig.3) of the present invention In addition, a negative voltage generator and an RF switch control facility are accumulated together on the same integrated circuit as the switch of the present invention with RF switch 100 integrated completely using new lamination and gate-transistors (gate resistance) composition of a transistor. To RF switch 100 integrated completely, so that it may describe in detail by the following, The built-in type oscillator which supplies a clock input signal to a charge pump circuit, the integration charge pump circuit which generates the negative power supply voltage which other RF switching circuits need, The gate drain of the CMOS logic circuit which generates the control signal which controls RF switch transistor, and a switch transistor, a gate source, and drain source voltage by decreasing, The RF buffer circuit which separates RF signal energy from the level shift circuit to which reliability is made to increase, a charge pump circuit, and a digital control logic circuit is included. Each of these circuits are described in detail by the following with reference to related figures.

[0052]

A 1st embodiment of a negative voltage generator-charge pump

As shown in Fig.4, the negative voltage generator 120, i.e., a charge pump, is contained in one embodiment of RF switch 100 integrated completely. The negative power supply voltage (it is hereafter described as "-Vdd") which other circuits of RF switch 100 integrated completely need with the negative voltage generator 120 is generated. The two input sets (Vdd) 122, i.e., a positive DC-power-supply-voltage signal, and the clocked into (shown in a figure as a single input signal "Clk") 124 are supplied to the negative voltage generator 120. Although Fig.4 has shown the clocked into 124 as a single input signal, by some embodiments of the RF switch in the present invention, the clocked into 124 can include the clock input signal exceeding two or it so that it may describe in relation to Fig.5 b below.

[0053]

In the embodiment shown in Fig.4, direct-current 3V power supply source is included in the positive service voltage which is an input to the negative voltage generator circuit 120. However, other electric power supply levels may be used, without deviating from the range or the meaning of the present invention. For example, if it is a request, a positive electric power supply with the sufficient direct current 3.5V, the direct current 5V, or other arbitrary convenience can be considered as the input to the negative voltage generator circuit 120 of Fig.4. Typically, a positive electric power supply signal is generated with an external low-electric-power supply source.

[0054]

In one embodiment of the present invention, the negative voltage generator 120 of Fig.4 is realized using a charge pump circuit. The simple block diagram of one illustration embodiment in the negative voltage generator 120 of Fig.4 is shown in Fig.5 a.As shown in the simple block diagram of Fig.5 a, the oscillator 202, the clock generation machine circuit 204, and the charge pump circuit 206 of the present invention are included in a negative voltage generator. The output of the oscillator 202 is input into the clock generation machine circuit 204. The output of the clock generation machine circuit 204 is input into the charge pump circuit 206. The negative power supply voltage which other circuits of RF switch 100 integrated completely use with the negative voltage generator 120 is supplied.

[0055]

The negative power supply voltage must be generated to an RF switching circuit in a disadvantageous thing in an external circuit in many of RF switches by the advanced technology. In realization of other RF switches, joint approach required in order to shift the direct-current value of an RF input signal to the halfway point of the applied bias voltage is used. In this approach, generally, since an FET gate drive becomes half effectively because of this level shift, it is necessary to apply comparatively high bias voltage. Negative influence is brought to switch insertion loss by this when not increasing bias voltage. It is because gate drives decrease in number by this and FET channel resistance increases by it.

[0056]

In order to cope with these problems, in one embodiment of RF switch 100 integrated completely, the charge pump circuit 206 of the present invention shown in detail is used for Fig.5 b. As shown in Fig.5 b, two P channel MOS FET transistors 208 and 210 are contained in the first embodiment of the charge pump circuit 206, and these are connected to two N-channel metal oxide semiconductor FET transistors 212 and 214 in series at it. The left leg (the first P channel transistor 208 connected to the first N channel transistor 212 in series is included) of the charge pump circuit 206, First capacitor Cp216 is used for the right leg (the second P channel transistor 210 connected to the second N channel transistor 214 in series is included) of a charge pump circuit, and it is combined with it. The source of the second N channel transistor 214 is combined with the illustrated second capacitor C218 which is an output capacitor like. Two non-overlapping clock control signals "Clk1" and "Clk2" are used in order to control operation of the transistors 208, 210, 212, and 214. For example, reverse "Clk1_" of "Clk1" controls the gate of the P channel transistors 208 and 210 to be shown in Fig.5 b. The non-overlapping clock control signal "Clk2" of another side controls the gate of the N channel transistors 212 and 214 like a graphic display.

[0057]

The charge pump 206 generates negative power supply voltage (-Vdd) by using the non-overlapping clock control signals Clk1 and Clk2 which drive a transistor gate, and charging and discharging alternately two capacitors (Cp216 and output capacitor C218). Negative power-supply-voltage-Vdd is generated from the electric charge which charged the capacitor C218. According to one embodiment, the train of impulses (that is, a train of impulses is input as the clock input signals Clk1 and Clk2) which drives a charge pump is generated using a pulse shift circuit (not shown). Since a train of impulses is applied to the charge pump 206, capacitor Cp216 is applied in the positive electric power supply Vdd, then, is discharged by the counter direction over the capacitor C218, and generates negative power-supply-voltage-Vdd. No transistor of a charge pump needs to avoid the thing exceeding Vdd also between which source / drain node, therefore the reliability of the charge pump 206 increases dramatically.

[0058]

In one embodiment of the charge pump circuit 206 of the present invention, the capacitance of the output C218 is about 200 pF, and the capacitance of Cp216 is about 50 pF. The person skilled in the art of the charge pump design field will be understood [that other capacitance values can be used and], without deviating from the range or the meaning of the present invention.

[0059]

As shown in the simple block diagram of Fig.5 a, in one embodiment, two non-overlapping clock signals are derived from the oscillation signal which the internal oscillator 202 generates. As shown in Fig.5 a, the oscillator 202 inputs an oscillation signal into the clock generation machine

circuit 204, and generates shortly two non-overlapping clock signals with which this circuit controls a charge pump transistor gate (by the arbitrary and useful well-known method). According to one embodiment of RF switch 100 with which the present invention was integrated completely, the oscillator of a low frequency wave is contained comparatively (several MHz order) in the oscillator 202. According to this embodiment, an easy relaxation oscillator is contained in an oscillator. however, the person skilled in the art of the integrated circuit field is understood [that the present invention can be carried out using the oscillator of other types, and], without deviating from the meaning or the range of the present invention -- I will come out.
[0060]
The voltage swing of the two non-overlapping clock signals Clk1 and Clk2 which changes to Fig.5 c temporally is shown. As shown in Fig.5 c, two non-overlapping clock signals change by the voltage swing from -Vdd to Vdd. In one embodiment, a clock signal changes from direct-current-3V to direct-current+3V. The efficiency of the charge pump 206 is improved by adjusting in this way.
[0061]
The N channel (212 and 214) and P channel (208 and 210) device of a single threshold value are contained in being advantageous to the charge pump transistors 208, 210, 212, and 214. The conventional charge pump circuit needs use of two or more threshold level device. Therefore, in order to have realized the thing of these former, rather than the charge pump circuit 206 of the present invention in Fig.5 b, the design was complicated and cost started. In one embodiment of the charge pump 206 of the present invention, the width of the P channel transistors 208 and 210 is about 20 micrometers, and length is about 0.8 micrometer. The width of the N channel transistors 212 and 214 is about 8 micrometers, and length is about 0.8 micrometer. The person skilled in the art of the integrated circuit design field will be understood [that the transistor of other dimensions can be used, and], without deviating from the range or the meaning of the present invention. The charge pump circuit 206 of the present invention is dramatically efficient, and operates perfect in spite of change of temperature and a process.
[0062]
Level shift circuit
Since a charge pump circuit doubles efficiently the power supply voltage applied to this circuit, it must pay attention to the integrity problems of electric potential relevant to such high voltage. In order to realize a charge pump by a method which improves the reliability of a transistor, a level shift circuit is used and the gate source voltage, gate drain voltage, and drain source voltage of a transistor are restricted to a permissible level.
[0063]
The invention level shift circuit 300 created according to the present invention is shown in Fig.6 a. Using the level shift circuit 300, an "ordinary" digital input signal [typical or] (a digital signal ranges from a ground (GND) to the range of +Vdd typically) is converted or shifted so that the range of -Vdd to +Vdd may be attained to. Thereby, the reliability of the RF switch integrated completely increases. Although a control signal is shifted to the range of direct-current-3V to direct-current+3V, the person skilled in the art of the RF switch control field will have it understood in one embodiment of the present invention, without deviating from the meaning or the range of the present invention that other level-shifted-voltages ranges can be used.
[0064]
As shown in Fig.6 a, two or more inverters combined with feedback structure are contained in the level shift circuit 300 (henceforth, it is called the level shifter 300) of the present invention.

Especially in the embodiment shown in Fig.6 a, to the level shifter 300, Two groups' inverter is contained and "out of the 1st and the shifted second output signal 314, i.e., a first output node," and its reverse "out_" of the second output node 316 are generated using these inverters. The inverters 302, 304, and 304 are contained in a first inverter group. The inverters 308, 310, and 312 are contained in a second inverter group. An "ordinary" digital input signal [typical or] (namely, digital input signal covering the range of GND to +Vdd) is the input node 318 of the first inverter 320, and is input into the level shifter 300. The first inverter 320 generates the first input signal "in" (with output node 324), and this signal is input into the second inverter 322. The second inverter 322 generates the second input signal "in_" which is the reverse of a first input signal "in" in the output node 326. Therefore, the 1st and the second inverters 320 and 322 generate the signal input into the two above-mentioned inverter groups. For example, the first input signal "in" is combined with the input part 328 of the inverter 302. Similarly, the second input signal "in_" is combined with the input part 330 of the inverter 308.

[0065]

It is generated by the first output inverters 306 and a first inverter group's output "out" is supplied to the first output node 314. It is generated by the second output inverters 312 and a second inverter group's output "out_" is supplied to the second output node 316. Two level-shifter outputs "out" and out_" are input into other circuits of RF switch 100 with which Fig.4 was integrated completely. For example, in one embodiment a first output "out", It is combined with the gate of the device in the switching transistor group 33 and the shunt transistor group 38 (). Namely, the "out" signal in the first output node 314 of Fig.6 a, It is combined with the "SW" control input signal of Fig.3, and this controls operation of the switching transistor group 33 and the shunt transistor group 38 by input node 33' and 38', as it described above in relation to Fig.3. Similarly, it is combined with "SW_" control input signal of Fig.3 (with input node 34' and 38'), and, thereby, a second level-shifter output "out_" controls the switching transistor group 34 and the shunt transistor group 37 by this embodiment as mentioned above.

[0066]

The level shifter 300 of Fig.6 a shifts the direct current level of an input signal (namely, input signal supplied by the input node 318), and, on the other hand, makes the frequency response of an input signal eternal. The level shifter 300 uses sufficiently the floating technology provided by realization by the silicon on insulator substrate of RF switch 100 integrated completely. The inverter of the level shifter 300 operates based on differential bias. That is, a level shifter shifts a digital input signal based on the difference between two voltage signals. As long as the difference between the electric power supply signals especially supplied to inverters (for example, output inverters 306 and 312 etc.) is the order of Vdd, the level shifter 300 functions reliably and shifts an input signal in the range between -Vdd and +Vdd. In one embodiment, Vdd is equal to the direct current 3V. In this embodiment, the voltage applied between those sources / drain nodes does not become larger than the direct current 3V with the transistor which constitutes the inverter (for example, output inverters 306 and 312) of the level shifter 300. The reliability of a transistor device increases by this.

[0067]

If Fig.6 a is referred to again, a level shifter will shift a digital input signal from -Vdd to the voltage level of the range of +Vdd using a feedback method. In particular, a second inverter group's (308, 310, and 312) output (namely, "out_" signal) in the second output node 316 is supplied as feedback to a first inverter group's input part by the input part of the inverter 304. Similarly, a first inverter group's (302, 304, and 306) output (namely, "out" output signal) in the

first output node 314 is supplied as an input to a second inverter group, especially the inverter 310.
[0068]
When the digital input signal in the input node 318 will be in a state logically "high" (that is, in some embodiments) When an input signal changes from GND to +Vdd, it swerves and the "in" signal (it can set to the node 324) and "in_" signal (it can set to the node 326) are set to a ** leg round (for example, direct current 0V) and Vdd (for example, direct current 3V). The "out" signal of the first output node 314 is set to +Vdd. Simultaneously, the "out_" signal of the second output node 316 is set to -Vdd. ("out" which acts as feedforward to the input part of "out_" fed back to the input part of the inverter 304, and the inverter 310) By feedback composition, quick change of the state in the level shifter 300 is carried out reliably. The level shifter 300 works similarly, when an input signal changes in the low state logically from a high state (from +Vdd to namely, GND transition). If the digital input signal of the input node 318 will be in a state logically "low", the "in" signal (it can set to the node 324) and "in_" signal (it can set to the node 326) will become Vdd (for example, direct current 3V) and a ground, respectively. The "out" signal in the first output node 314 is set to -Vdd. Simultaneously, the "out_" signal in the second output node 316 is set to +Vdd. By feedback, quick change of the state in the level shifter 300 is carried out reliably again. According to grounding, the descent more than perfect Vdd voltage between the source / drain node in the MOSFET transistor of an inverter is reliably lost in a level-shifter inverter.
[0069]
One embodiment of the inverter (for example, inverters 302, 304, and 306) used for Fig.6 b in order to realize the level shifter 300 of Fig.6 a is shown. As shown in Fig.6 b, two MOSFET devices 342, i.e., P channel transistor, and the N channel transistor 344 are contained in the inverter 340. These devices are controlled by the illustrated input signal which is connected in series, combines the gate both, and is supplied to the input node 346 like. The source of the P channel transistor 342 is the node 350, and it is combined to first power supply voltage, and on the other hand, N channel transistor 344 source is the node 352, and is combined to second power supply voltage. It is combined, and both the illustrated drains that are devices like are the output nodes 348, and generate the output of an inverter. In one embodiment of the inverter 340 of the present invention, the P channel transistor 342 is 5 micrometers in width, and is 0 or 8 micrometers in length. In this embodiment, N channel transistor is 2 micrometers in width, and is 0.8 micrometer in length. The person skilled in the art of the transistor design field will be understood [that the thing of other physical sizes can be used as a transistor of the inverter 340, and], without deviating from the range or the meaning of the present invention. The logical expression of the inverter 340 is shown as the sign 360 in Fig.6 b again.
[0070]
Thus, by using the level shifter 300 of the present invention, the digital input signal which attains to the range of GND to +Vdd at the beginning is shifted so that the range of -Vdd to +Vdd may be attained to. The corresponding output signal which the level shifter 300 of the plot of a digital input signal of a voltage swing versus time and the present invention of Fig.6 a generates in Fig.7 a is shown. As shown in Fig.7 a, a digital input signal ranges from a ground or the direct current 0V to the range of Vdd. The output of the level shifter 300 of the present invention attains to the range of -Vdd to +Vdd. As for an input signal, according to one embodiment of the RF switch in the present invention, the output of the level shifter 300 ranges from the direct current 0V to the range of direct-current-3V to direct-current+3V in the range of direct-current+3V. The power

supply voltage of other values can be used without deviating from the range or the meaning of the present invention. For example, in one embodiment, an input signal can be made into the range of the direct current 4V from 0 to direct-current+3.5V, or 0. According to this embodiment, a level shifter shifts a signal to direct-current+3.5(or +4)V from direct-current-3.5(or -4)V.

[0071]

The simple logical symbols of the level shifter 300 of the present invention in Fig.6 a are shown in Fig.7 b. These logical symbols are used with next Drawings. As shown in Fig.7 b, a digital input signal is supplied by the input node 318 (the same input node 318 as having described above in relation to Fig.6 a). The level shifter 300 supplies reverse "two shifted outputs, i.e., "out", and out_" of those. These outputs are supplied by the output nodes 314 and 316 (the same output nodes 314 and 316 as having described above in relation to Fig.6 a), respectively.

[0072]

RF buffer circuit

Fig.8 a is an electric figure of the two-step level-shifter buffer circuit 400. Fig.8 b is a simple block diagram of an interface to a digital control input and the buffer circuit 400. The 1st step level shifter 300 and the 2nd step RF buffer circuit 402 are included in the two-step level shifter and the RF buffer circuit 400 of Fig.8 a. The 1st step level shifter 300 is the same as that of what was described above in relation to Fig.6 a, and 6b, 7a and 7b, therefore it does not carry out describing in details more here. The level-shifter stage 300 shifts the logical level of a digital control signal, and it is made to attain to the range of -Vdd to +Vdd, as described above. The RF buffer circuit 402 is included in the 2nd step of the circuit 400. The RF buffer circuit 402 performs only the role of a driver (an RF buffer circuit does not perform a level shift).

[0073]

An RF buffer separates electrically digital control signals (what the CMOS logical block 110 of Fig.4 generates) from RF switch 30 described above in relation to Fig.3.RF buffer 402 functions as inhibiting the sag of the control voltage (although it is SW and SW_, this Description and Fig.8 a shows as a control signal "out" and "out_" again, respectively) which controls the operation of a transistor and un-operating in RF switch 30. RF buffer 402 functions as a big-electric-power RF signal preventing combining with a negative electric power supply (namely, -Vdd) again so that it may describe in detail by the following. As it described above in relation to Fig.5 a - 5c, the charge pump circuit 206 generates this negative electric power supply. The extent of the big-electric-power RF signal in RF switch 30 carries out RF combination at the negative electric power supply which the charge pump 206 (Fig.5) generates, and, thereby, especially RF buffer 402 protects that current carries out drainage from a negative electric power supply.

[0074]

When the RF input signal of big electric power is extremely input into RF switch 30 of the present invention, in order to separate a digital logic signal from an RF switch, when the buffer circuit is not used, combination of an RF signal and a digital logic signal takes place. RF combination may have harmful influence on an RF transistor control signal (SW and SW_), and usually has harmful influence. For example, when the RF input signal of order of about 30 dB is input into 1-W RF switch 30, there is a possibility that the voltage oscillation of a zero mark bolt will happen by a digital control line, by RF combination. This is because an RF signal is fed back to a digital control circuit from an RF switch. This RF joint effect may have bad influence on an

RF transistor group's operation and non-operativeness, therefore normal operation of RF switch 30. The buffer circuit 402 of Fig.8 a protects the joint effect.
[0075]
As shown in Fig.8 a, in composition, the buffer circuit 402 of the present invention resembles dramatically the level shifter 300 which was described above as the 1st step of the two stage circuits 400, and was illustrated. Two inverter groups (404, 406, and 408), i.e., a first inverter group, and a second inverter group (410, 412, and 414) are contained in RF buffer 402 like the level shifter 300. It is generated by the first output inverters 408, and, by a diagram, the first inverter group's (404, 406, and 408) output has attached the code of "out", and is supplied by the first output node 416. It is generated by the second output inverters 414, and the second inverter group's (410, 412, and 414) output has attached the code of "out_", and is supplied by the second output node 418. The output signal "out_" is the reverse of an output signal "out."
[0076]
feedback is used for the level shifter 300 of the 1st step although it is important -- a level shift function -- performing (it described in relation to Fig.6 a -- as) -- the RF buffer circuit 402 does not feed back the output signal to an input. As a result, the digital input signal (namely, control input signal input into the level shifter 300 by the nodes 328 and 330) input into the 1st step, It separates from the output signal (that is, it is a control-output signal "out" of the output nodes 416 and 418, and its reverse "out_", and combined with SW and SW_controlling signal line, respectively) used in order to control RF switch transistor.
[0077]
If Fig.8 a is referred to again, especially the level shifter 300 will input a digital control signal "in" and its reverse signal "in_" by the nodes 328 and 330, respectively (in relation to Fig.6 a, it described in detail by the above like). The first output "out1" of the level shifter 300 in the output node 314 is fed back to the input part of the inverter 310 like a graphic display. Similarly, the second output "out1_" of the level shifter 300 in the output node 316 is fed back to the input part of the inverter 304. That as mentioned above, RF combination (that is, a level-shifter output signal piles up an RF signal on it) takes place because of this feedback topology, It is a case where the output signal of a level shifter is used in order to control RF switch transistor directly (namely, when there is no buffer circuit 402). Therefore, the RF buffer circuit 402 of the present invention is used without feedback of an output signal, and separates an input signal (namely, a digital input signal "in" and "in_") from the RF signal which exists in an RF switch. As shown in Fig.8 a, the first output signal "out1" of the level shifter 300 is input into the inverters 404 and 406 of an RF buffer circuit. Similarly, the second output signal "out1_" of the level shifter 300 is input into the inverters 410 and 412 of a buffer circuit. Two control outputs ("out" and "out_") of the RF buffer circuit 402 are not supplied as feedback to a level shifter, although it controls the operation of a transistor and un-operating in an RF switch. Therefore, an improvement of separation between an RF switch and a digital logic circuit is attained.
[0078]
In one embodiment, the inverter 340 described above in relation to Fig.6 b is contained in the inverter which realizes a two-step level shifter and the RF buffer circuit 400. However, the person skilled in the art of the inverter design field will have it understood that the two stage circuits 400 are realizable, without deviating from the range or the meaning of the present invention using a substitute inverter design. In one embodiment, the transistor used in order to realize the 1st step level shifter 300 is more nearly physically [than the transistor used in order to realize the 2nd step RF buffer circuit 402] small. The transistor of a bigger dimension is used in

the RF buffer circuit 402, in order to attain efficient amplification of a control signal. For example, in one embodiment, the amplification whose width is those with 3 times, as a result about 3 times the current is brought about rather than the transistor used in order that the transistor used in order to realize an RF buffer may realize the level shifter 300. The person skilled in the art of the transistor design field will be understood [that the transistor of other convenient dimensions can be used, and] in order to attain any desirable amplification in a digital control signal.

[0079]

The voltage divider used in the alternative level shift circuit of the present invention

Fig.9 a is an electric figure of one embodiment in the low current voltage divider ("LCVD") circuit 500. This circuit is used by the feedback path of one embodiment in the level shifter 300 described above in relation to Fig.6 a. The simple logical symbols used since the voltage divider 500 of Fig.9 a is expressed to Fig.9 b are shown. The voltage divider 500 is used by one embodiment, and the potential gate oxide integrity problems relevant to the excessive voltage oscillation of the whole gate oxide of a feedback inverter transistor are tackled. Various source drain voltage of MOSFET used in order to realize a level shifter, as it described above in relation to the level shifter 300, Although bigger voltage than Vdd never is not applied, the output (namely, an output signal "out" and "out_") of a level shifter, since 2xVdd may also vibrate from -Vdd to +Vdd namely,, the gate oxide of the feedback inverters 304 and 310 may be applied in the voltage of 2xVdd. These feedback voltage levels are applied to the whole gate oxide of the feedback inverters 304 and 310, and gate oxide integrity problems may produce them as a result.

[0080]

In order to be able to avoid gate oxide integrity problems, the maximum voltage applied to the whole gate oxide of the feedback inverters 304 and 310 is reliably reduced substantially to Vdd (not being the gate oxide voltage of 2xVdd). Therefore, in one embodiment in the RF switch with which the present invention was integrated completely, the voltage divider of Fig.9 a restricts the voltage applied to the gate of the level-shifter feedback inverters 304 and 310. In this embodiment, the output (namely, each output "out" and "out_" in the output nodes 314 and 316) of a level shifter, Instead of feeding back to the feedback inverter shown in the level shifter of each Fig.6 a directly, first, a level-shifter output signal is adjusted with the voltage divider 500 of Fig.9 a, and is fed back to a feedback inverter after that. The voltage applied to the gate oxide of the feedback inverters 304 and 310 reliably with the voltage divider 500 so that it may describe in detail by the following, It is made not to exceed the sum total (a voltage drop is the number of transistors and the function of transistor threshold voltage which are used in order to realize the voltage divider 500) of Vdd and a small voltage drop. In one embodiment, Vdd is the direct current 3V and a voltage drop is the direct current 0.9V. According to this embodiment, it becomes reliably that a gate oxide is never applied in the voltage exceeding the direct-current abbreviation 3.9V (that is, a feedback inverter is applied in the voltage covering the range of the direct current 0.9V from direct-current-3V), thanks to the voltage divider 500.

[0081]

two or more MOSFET devices (502, 504, 506, and 508) combined with both the voltage dividers 500 by series constitution (namely, -- being illustrated -- it puts on a mutual top by source drain arrangement like) when Fig.9 a was referred to here -- it is contained. According to both one embodiments, the gate and drain of MOSFETs 502, 504, 506, and 508 joined together, and have realized the lamination diode. Although MOSFET which realizes a diode is henceforth called a "diode device", these are laminated in series like a graphic display. MOSFETM3 (510) and

output MOSFETM2 (512) are contained in the voltage divider 500 again. The function of these two transistors is described more in details below.
[0082]
A diode device is used and the partial pressure of the voltage of the input signal supplied to the voltage divider 500 by the input node 514 is carried out. As shown in Fig.9 a, the signal by which a partial pressure is carried out to the voltage divider 500 is supplied to the drain (and gate connected) of the first device 502 as an input. when an input signal exceeds a positive voltage level once (nxVthn), "n" is the number of the diode devices used in order to realize the voltage divider 500 here -- Vthn -- the threshold voltage (namely, "diode descent" to a source from the drain of a device) of a device -- but, A diode device (502, 504, 506, and 508) begins to conduct a lot of current. the embodiment shown in Fig.9 a -- n= 4 and Vthn= -- 0.7 volt of alternative values can be but used to "n" and Vthn, without deviating from the range or the meaning of the present invention. For example, in other embodiments, by changing the number of the diode devices used in order to realize the voltage divider 500, the input signal supplied to a voltage divider is arbitrary, and can be restricted to a desired voltage level (namely, thing for which the value of "n" is changed). According to the embodiment shown in Fig.9 a, once input voltage exceeds the voltage level of (4x0.7), i.e., 2.8 volts, a lamination diode device will begin to conduct briskly.
[0083]
The ballast-resistances machine R516 is connected to the source of the output diode device 508 like a graphic display. Once a diode device carries out turn-on completely, any additional input voltage which exceeds the value of nxVthn for the ballast-resistances machine R516 will descend. According to the embodiment shown in Fig.9 a, any additional input voltage which exceeds the value of (the input voltage - (4xVthn)) for the ballast-resistances machine R516 descends. The output of the voltage divider 500 is pulled out from the gate drain to which the output diode device 508 was connected. The output signal by which the partial pressure was carried out is supplied by the output node 520. It is guaranteed for the voltage which descends by the diode drop of the diode devices 502, 504, and 506, and the ballast-resistances machine R516 whole that the output of the output node 520 substantially (input voltage - (3xVthn)) never exceeds. about [Vthn=] -- about [0.7V and] -- the output node 520 never exceeds (direct-current 3V- (3x direct current 0.7V)) 0.9V, i.e., a direct current, to the maximum input voltage of 3V. Thus, in the embodiment shown in Fig.9 a, the voltage divider 500 restricts the output of the output node 520 to the range of direct-current-3V to direct-current+0.9V to the input voltage which attains to the range between direct-current-3V and direct-current+3V.
[0084]
Output MOSFETM2 (512) is constituted as a capacitor, and it is used in order to support acceleration of the switching time of the voltage divider 500. When an input reaches negative potential, MOSFETM3 (510) carries out reliably that the output node 520 vibrates to the electric potential of the input signal in the input node 514. This is attained when an input signal reaches negative potential, and the device M3 (510) carries out turn-on. Therefore, when an input signal becomes -Vdd electric potential (for example, direct-current-3V), the output signal of the output node 520 is also set to -Vdd. The output device 508 can apply reverse bias during negative voltage vibration of an input signal, and, thereby, becomes trustworthy [that a direct current does not carry out drainage from a negative power supply source] during negative voltage vibration of an input signal. When the output of a voltage divider is direct-current abbreviation-3V, the voltage divider 500 does not draw current near at all. This is important. Current is direct-

current-3V and it is because the charge pump circuit described above in relation to Fig.5 b is made to discharge. When the output of a voltage divider is about 0.9v and the ballast-resistances machine R516 is chosen comparatively largely, there is comparatively little current which can be drawn near. However, since the current in this case is produced between positive voltage (0.9V) and a ground, charge pump current additional for operation of the voltage divider 500 of Fig.9 a is not sent.

[0085]

In one embodiment, the value of the ballast-resistances machine R516 is 100komega. In one embodiment, all the devices of the voltage divider 500 are the same length. For example, in one embodiment, all the devices are 0.8 micrometer in length. In one embodiment, the physical size of all the diode devices (502, 504, 506, and 508) is the same. In one embodiment, each diode device is 2 micrometers in width, and the device M3 (510) is the 2 micrometers with same width, and output MOSFETM2 (512) is 14 micrometers in width. the person skilled in the art of the integrated circuit design field is understood [that other values and alternative composition can be used and] to the device shown in Fig.9 a, without deviating from the range or the meaning of the present invention -- I will come out. for example, the person skilled in the art of the electric circuit design field in lamination of changing the number of diode elements "n", changing the value of Vthn, or a diode device, The output node 520 is pulled out on a different point (for example, like a graphic display). Instead of pulling out from the drain of the device 508, other voltage divider output levels will have it understood by what an output is pulled out for from the drain of the diode device 506 or 504 that it can adjust easily.

[0086]

The correction level shifter using a voltage divider

By decreasing the voltage applied to the gate oxide of RF switch transistor, the voltage divider 500 of Fig.9 a and 9b can be used advantageously, and the reliability of the transistor in both the above-mentioned level shifter 300 and a charge pump circuit can be improved. For example, the correction level shifter 600 which uses the voltage divider 500 of Fig.9 a for Fig.10 in combination with the level shifter 300 of Fig.6 a is shown. As shown in Fig.10, the output (it can set to the output node 314) of the inverter 306 in the level shifter 300 is applied to the input part of the first voltage divider 500'. Similarly, the output (it can set to the output node 316) of the inverter 312 of the level shifter 300 is applied to the input part of second voltage divider 500". The output of a voltage divider is fed back to the input part of the feedback inverters 304 and 310, as shown in Fig.10. If Fig.10 is referred to especially, the output "out" of a first voltage divider in output node 520' will be fed back to the input part of the feedback inverter 310. Similarly, the output "out_" of a second voltage divider in output node 520" is fed back to the input part of the feedback inverter 304. As it described above in relation to Fig.9 a, feedback voltage is decreased in the range of -Vdd to direct-current abbreviation+0.9V by the level shifter 500' and 500". The function of the level shifter 600 does not change for the voltage oscillation in which this feedback path decreased.

[0087]

Please pull out an RF switch control signal "SW" and "SW_" from a level-shifter output, and note being able to supply RF switch 30 of the present invention of Fig.3 as an input, before inputting them into the voltage divider 500' and 500". For example, as shown in Fig.10, since the switch control signal "SW" is generated, the output of the inverter 306 in the output node 314 can be pulled out and used. Similarly, since the switch control signal "SW_" is generated, the output of the inverter 312 in the output node 316 can be pulled out and used. According to one

embodiment, as it described above in relation to the two-step level shifter and the RF buffer circuit 400 of Fig.8 a, the control signal pulled out from the nodes 314 and 316 is stored in a buffer first, and is combined with RF switch transistor after that. Although the voltage oscillation covering the whole region is possible for the switch control signal SW and SW_, this does not cause the integrity problems of a gate oxide in an RF switch. Especially a switch control signal is crossed to the range from -Vdd to +Vdd (that is, the voltage level of a switch control signal is not restricted by the voltage divider). The all-out voltage oscillation of a switch control signal does not cause the integrity problems of a gate oxide about RF switch MOSFET. The source of RF switch MOSFET is because it is grounded. Therefore, a switch input signal relates to the ground in RF switch MOSFET. As a result, MOSFET is applied to the whole gate oxide in positive Vdd voltage to a ground, or negative Vdd voltage is applied to the whole gate oxide to a ground.

[0088]

The simple graphic table expression 601 of the part in the correction level shifter 600 is shown in Fig.10 again. The sign 601 expresses the portion which the dashed line region 601' of Fig.10 shows. As shown in Fig.10, first ininput "_" 630 corresponding to the input node 326 ("in_") are contained in the correction level shifter 601 with a sign. The second input "out" 632 corresponding to the input to the feedback inverter 310 is included in the correction level shifter 601 with a sign again. This signal should be careful of having come out of the outputting part 520' of the first voltage divider 500' again. Positive power supply voltage is input by the +Vdd input part 634. Negative power supply voltage is input by the -Vdd input part 636. There are three output signals, i.e., "out_pos" (it can set to the outputting part 638), "out_neg" (it can set to the outputting part 640), and "out_" (it can set to the outputting part 642) in the correction level shifter 601. These outputting parts correspond to the above-mentioned output nodes 606 and 608 and 520". In order to understand easily, in the Drawings described below, graphic table expression of the level shifter 601 is used.

[0089]

The potential gate oxide integrity problems relevant to the level shifter 300 described above in relation to Fig.6 a are avoided in the feedback path of the correction level shifter 600 using the voltage divider 500' and 500". The voltage divider 500' and 500" can also function in order to decrease the potential gate oxide integrity problems relevant to a charge pump circuit. As shown in Fig.10, the output of the inverters 308 and 310 is supplied to two output intervals as an input, in order to be pulled out from the level shifter 300 and to generate two output signals "out_pos" and "out_neg." Especially the output of the inverter 308 is supplied as an input to the first output inverters 602. Similarly, the output of the feedback inverter 310 is supplied as an input to the second output inverters 604.

[0090]

By combining the output inverters 602 and 604 by such a method, never exceeding Vdd (or -Vdd) of the output signal of the correction level shifter 600 is lost. Especially the first output inverters 602 generate the output signal "out_pos" covering the range of GND (namely, direct current 0V) to +Vdd in the first output node 606. The second output inverters 604 generate the second output signal "out_neg" covering the range of -Vdd to GND in the second output node 608. If the input signal "in_" is set to GND, the output signal "out_pos" will be set to GND. The output signal "out_neg" moves from GND to -Vdd. If the input signal "in_" is set to positive +Vdd, "out_pos" will be set to Vdd and "out_neg" will move from -Vdd to GND. Thus, if the correction level shifter 600 of the present invention is used, the "out_pos" output signal will be crossed to the range of GND to +Vdd, and, on the other hand, the "out_neg" output signal will be

crossed to the range of GND from -Vdd. The potential gate oxide integrity problems in a correction charge pump circuit are tackled using two output signals "out_pos" and "out_neg" so that it may describe in detail by the following. The potential gate oxide integrity problems in an RF buffer circuit can also be tackled using these output signals so that it may describe in relation to Fig.11 a and 11b here.

[0091]

A correction level shifter and an RF buffer circuit

In two steps of the level shifter and RF buffers 400 described above in relation to Fig.8 a, the voltage oscillation of abbreviation 2xVdd may be experienced in an RF buffer inverter input. As already described, in the voltage oscillation of this level, gate oxide integrity problems arise and it may have harmful influence on the function of RF buffer transistor.

[0092]

The alternative embodiment of the two-step level shifter and the RF buffer circuit 400 described above in relation to Fig.8 a to Fig.11 a and 11b is shown. The voltage concerning the gate oxide of an RF buffer is kept from exceeding Vdd from 0.9 volt reliably in the alternative embodiment of an RF buffer shown in Fig.11 b using the voltage divider circuit described above. As shown in Fig.11 b, the 2nd step RF buffer circuit 402' combined with the 1st step level shifter circuit 600 and it is included in substitute two-step level shifter and RF buffer circuit 400'. In this embodiment of a level shifter and the RF buffer circuit 400', An RF buffer output signal "out" and "out_" are generated using the output "out_pos" and "out_neg" of a correction level shifter which were described above in relation to Fig.11 as an input to an RF buffer inverter. For example, as shown in Fig.11 b, "out_pos" and the "out_neg" output signal which the first correction level shifter 700 generates are input into the two RF buffer inverters 702 and 704, respectively. Similarly, "out_pos" and the "out_neg" output signal which the second correction level shifter 706 generates are input into the two RF buffer inverters 708 and 710, respectively. According to Embodiment 400' of the substitution shown in Fig.11 a and 11b, as for the "out_pos" output, the input signal "in" is logically set to Vdd at the time of a high signal, and, on the other hand, "out_neg" is set to GND. Thus, logically, at the time of a high value, the output of the inverter 702 is set to GND and, as for the output of the inverter 704, the input signal "in" is set to -Vdd. Therefore, as for the output of the inverter 712, the input signal "in" is set to ("out")-Vdd when high. When low, an opposite output is generated for an input signal "in."

[0093]

The power supply voltage of the first RF output inverter 712 is controlled using the RF buffer inverters 702 and 704. Similarly, the power supply voltage of the second RF output inverter 714 is controlled using the RF buffer inverters 708 and 710. An RF switch is controlled by this embodiment using an RF buffer output signal "out" and "out_" (that is, the output signal "out" works as control voltage "SW", and, on the other hand, commits "out_" as control voltage "SW_").

[0094]

Correction charge pump alternative embodiment

As mentioned above, two output signals "out_pos" and "out_neg" which the correction level shifter 600 of Fig.10 generates, It can use by one embodiment of the substitution in a charge pump circuit, and the potential gate oxide integrity problems relevant to the excessive voltage applied to a charge pump can be decreased or eliminated. As it described above in relation to Fig.5 b and 5c, it is a charge pump transistor (). That is, the voltage oscillation of 2xVdd is among the clock signals used in order to control the gate of the P channel transistors 208 and 210

and the N channel transistors 212 and 214. For example, as shown in Fig.5 c, a charge pump clock signal "Clk1" and "Clk2" are crossed to the range of positive power-supply-voltage +Vdd from negative power-supply-voltage-Vdd. The voltage oscillation covering this whole region may cause oxide integrity problems in a charge pump circuit like the gate oxide integrity problems described above in relation to the RF buffer circuit and the level shifter circuit. Therefore, by restricting the voltage applied to a gate oxide from -Vdd to the range of 0.9V shows to Fig.12 the correction charge pump circuit which decreases in number or eliminates potential gate oxide integrity problems.

[0095]

The correction charge pump 800 is shown in Fig.12. This uses the correction level shifter 600 described above in relation to Fig.10. As shown in Fig.12, the charge pump circuit 206' and the charge pump clock generation circuit 802 of the present invention are included in the correction charge pump 800. By the charge pump clock generation circuit 802, the clock control signal which the charge pump circuit 206' uses is generated. The design resembles dramatically the charge pump 206 which the charge pump circuit 206' described above in relation to Fig.5 b. For example, it adds to path capacitor Cp216 and the output capacitor C218, and the pair of P channel transistors 208 and 210 and the pair of N channel transistors 212 and 214 are contained in the charge pump circuit 206'. According to one embodiment of the charge pump circuit 206', there is a capacitance of hundreds of pF order in the output capacitor C218, and there is a capacitance of about 50 pF in capacitor Cp216. The person skilled in the art of the charge pump design field will be understood [that other capacitance values can be used and], without deviating from the range or the meaning of the present invention.

[0096]

The function of charge pump 206' resembles dramatically the charge pump 206 described above in relation to Fig.5 a. Therefore, it does not carry out describing the operation in detail again here. That charge pump 206' shown in Fig.12 differs from the charge pump 206, The control signal used in order to control the transistor gate (namely, gate of the transistors 208, 210, 212, and 214) of charge pump 206', It is the point restricted to the region of the half of a voltage oscillation (that is, restricted to the range of Vdd from the ground or the ground from -Vdd). the potential gate oxide integrity problems produced when gate control voltage vibrates the whole region from -Vdd to Vdd namely, -- -- or [therefore, / decreasing] -- or it eliminates.

[0097]

As shown in Fig.12, the four correction level shifters 804, 806, 808, and 810 combined with feedback composition are contained in both the charge pump clock generation circuits 802. According to one embodiment of a correction charge pump, four correction level shifters are realized by the correction level shifter 600 described above in relation to Fig.10. The level shifter using the graphic table expression 601 of the level shifter 600 in Fig.10 is shown in Fig.12.According to this embodiment, the level shifters 804, 806, 808, and 810 carry out the same operation as the level shifter 600 of Fig.10. Two non-overlapping clock signals "Clk1" and "Clk2" (and each reverse signal "Clk1_" and "Clk2_") are input into "in_" input part of a level shifter as shown in Fig.12. Two input clock signals "Clk1" and "Clk2" are the same as that of the non-overlapping clock signal described above in relation to Fig.5 a - 5c. As shown above in relation to Fig.5 c, two non-overlapping clock signals change by the voltage swing of -Vdd to +Vdd. According to one embodiment, a clock signal changes from direct-current-3V to direct-current+3V.

[0098]

The clock control signal of the half region used by four correction level shifters in order to control charge pump 206' is generated. As especially shown in Fig.12, "CLK1POS_", "CLK1NEG_", "CLK2POS", and a "CLK2NEG" control signal are generated by four level shifters. These are input into the charge pump transistor gate control nodes 250, 252, 254, and 256, respectively. According to the embodiment shown in Fig.12, four transistor gate control signals "CLK1POS_", "CLK1NEG_", "CLK2POS", and "CLK2NEG" are generated by the level shifters 805 and 808. By the level shifter 806, "CLK1POS_" and a "CLK1NEG_" gate control signal are generated, and, on the other hand, "CLK2POS" and a "CLK2NEG" gate control signal are generated by the level shifter 808. As especially shown in Fig.12, the "out_pos" output ("CLK1POS_") of the level shifter 806 is combined in order to control the transistor gate input part 250 of the transistor 208. The "out_neg" output ("CLK1NEG_") of the level shifter 806 is combined in order to control the transistor gate input part 252 of the transistor 210. Similarly, the "out_pos" output ("CLK2POS") of the level shifter 808 is combined in order to control the transistor gate input part 254 of the transistor 214. Finally, the "out_neg" output ("CLK2NEG") of the level shifter 808 is combined in order to control the transistor gate input part 256 of the transistor 214. It functions as the clock generation circuit 802 preventing the excessive voltage of the whole gate oxide in a charge pump transistor.

[0099]

The person skilled in the art of the transistor design field will be understood [that other control constitution can be used and], without deviating from the meaning or the range of the present invention. For example, in the alternative embodiment of a correction charge pump, a control signal can be generated using other two level shifters (804 and 810). As it described above in relation to the charge pump circuit 206, correction charge pump 206' of the present invention is realizable using substitute transistor composition (an N channel and a P channel).

[0100]

As shown in Fig.12, the four level shifters 804, 806, 808, and 810, It is combined with both the groups (804, 806, and 808 and 810) of a level shifter in the feedback composition which resembles dramatically the feedback topology of the level shifter described above in relation to Fig.6 a. For example, the "out_" output node (signal) of the level shifter 804 is supplied to the "out" node of the level shifter 806 of the related group as feedback. Similarly, the "out_" output node of the level shifter 806 is supplied to the "out" node of the level shifter 804 of the related group as feedback. Similarly, the "out_" output node of the level shifter 808 is supplied as feedback to the "out" node of the level shifter 810 of the related group. The "out_" output node of the level shifter 810 is supplied to the "out" node of the level shifter 808 of the related group as feedback. In generating of four transistor gate control signals "CLK1POS_", "CLK1NEG_", "CLK2POS", and "CLK2NEG", the clock generation circuit 802 uses feedback composition.

[0101]

Outline

The new RF switch manufactured using SOI and a CMOS process is provided. If a switch is manufactured on a SOI substrate, as a result, board bias will be lost and it will become possible to accumulate the main CMOS-circuit configuration blocks with an RF switch element. By accumulating a CMOS structure block with an RF switch element, the solution [need / only a single external power (that is, negative power supply voltage is generated inner in the charge pump circuit accumulated with the RF switch) / to be used] of the RF switch integrated completely is provided. As this result, RF switch separation, insertion loss, and compression are improved. In one embodiment, the 1-dB compression point of an RF switch exceeds about 1 W,

insertion loss is less than about 0.5 dB, and switch separation is about about 40 dB in height. Switching time improves with a present invention switch again.
[0102]
It has described about some embodiments of the present invention. However, it will be understood that various corrections are possible, without deviating from the meaning and the range of the present invention.
[0103]
Therefore, the present invention should understand the specific thing which it is not limited by the illustrated embodiment but is limited by only attached Claims.
[Brief Description of the Drawings]
[0104]
[Fig.1 a] It is a simple electrical-and-electric-equipment figure of the single-pole single-throw (SPST) RF switch by the advanced technology used in order to describe the performance characteristic of an RF switch.
[Fig.1 b] It is a simple electrical-and-electric-equipment figure of SPST and the RF switch in Fig.1 a, and this switch turns "ON" and the characteristics with a main switch when passage of an RF signal is attained from an input node to an output node are shown.
[Fig.1 c] An RF switch turns "OFF" and the equivalent small signal electrical property of the RF switch in Fig.1 a when an RF signal is blocked with it from an output node, and 1b is shown.
[Drawing 2]It is a simple electrical-and-electric-equipment figure of the single pole double throw (SPDT) RF switch by the advanced technology.
[Drawing 3]It is an electric figure of the RF switch by one embodiment of the present invention.
[Drawing 4]It is a simple block diagram of the RF switch which was manufactured according to the present invention and which is illustration-like and was integrated completely.
[Fig.5 a] It is a simple block diagram of one illustration embodiment in the negative voltage generator shown in the simple block diagram of Fig.4.
[Fig.5 b] It is an electric figure of the first embodiment in the charge pump circuit used since negative service voltage is generated to the RF switch of Fig.4.
[Fig.5 c] It is the plot of a voltage swing versus [which shows two voltage swings of a clock signal which do not overlap but change temporally] time used in order to control the charge pump circuit of Fig.5 b.
[Fig.6 a] It is an electric figure of the first embodiment in the level shift circuit of the present invention.
[Fig.6 b] It is an electric figure of one embodiment in the inverter used in order to realize the level shifter of Fig.6 a.
[Fig.7 a] It is the plot of a voltage swing versus time of the output signal which the level shifter of the present invention of Fig.6 a corresponding to a digital input signal and it generates.
[Fig.7 b] They are simple logical symbols of the level shifter of the present invention in Fig.6 a.
[Fig.8 a] It is an electric figure of one embodiment in a two-step level shifter and RF buffer circuit including the level shifter of the 1st step, and the RF buffer circuit of the 2nd step.
[Fig.8 b] It is a simple block diagram of an interface to the RF buffer circuit of a digital control input and Fig.8 a.
[Fig.9 a] It is an electric figure of one embodiment in the low current voltage divider (LCVD) circuit which manufactured according to invention of this RF switch.
[Fig.9 b] They are simple logical symbols used in order to express the voltage divider of Fig.9 a.

[Drawing 10]It is an electric figure of the second embodiment in the level shift circuit which uses the low current voltage divider circuit of Fig.9 a in combination with the level shift circuit of Fig.6 a.
[Fig.11 a] It is an electric figure showing the alternative embodiment of the two-step level shifter and RF buffer circuit of Fig.8 a.
[Fig.11 b] It is an electric figure showing the alternative embodiment of the two-step level shifter and RF buffer circuit of Fig.8 a.
[Drawing 12]It is an electric figure of the correction charge pump which uses the level shift circuit of Fig.10.

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(54) Title: SWITCHING SYSTEM AND METHOD

(57) Abstract: The invention relates to a Radio Frequency System and method. A Radio Frequency (RF) system comprising a RF switch comprising a plurality of transistor switching elements implemented on Silicon on Insulator (SOI) for switching at least one or more RF signals and said SOI comprises a bulk substrate region and a buried oxide region. At least one filter is adapted to isolate the RF signal from the substrate and/or other high frequency signals or control signals present in the RF system. There is also provided a coupling capacitor adapted to cooperate with the filter to improve linearity of the transistor switch elements.

Title

Switching System and Method

Field of the Invention

The present invention generally relates to the field of semiconductors and RF systems. In particular, the invention relates to RF switches and to switching radio frequency (RF) signals within an integrated circuit.

Background to the Invention

RF switches are a key building block in wireless systems and find many uses in applications such as mobile phones and wireless LANS. The act of switching radio frequency signals in an integrated circuit is carried out by an RF switch circuit. Many technologies exist for the design of integrated RF switch circuits.

Generally an RF switch system does not consist of the RF switching circuit alone and typically must be controlled using digital logic circuitry. In addition both negative and positive voltage levels are required to optimise the performance of the switch. Therefore, a negative voltage generator may also be required as part of the switch system. A switch can have a number of switching elements, although it can be comprised of any number of switching elements, which control the flow of RF power between different points in the particular application. Often MOSFET switches are used as the switching element in the art of RF design.

Performance metrics such as low insertion loss, high linearity, high isolation and power handling are critical in RF switch design. However, the RF switch performance is limited by substrate interactions with the circuits which degrade all the key performance metrics as well as non-linearities in the circuits themselves. Switching to an SOI substrate has been shown to improve the loss in the substrate although additional treatment of the silicon substrate is necessary to improve linearity. This has been achieved using an implant step in the process which prevents charge build-up at the silicon surface beneath the oxide. However, these steps are still not sufficient to meet the stringent demands of wireless technologies and further techniques are required to serve the broader wireless market segment.

A publication by Botula A et al entitled 'A Thin Film SOI 190nm CMOS RF Switch Technology, IEEE, Piscataway, NJ, USA, 19 January 2009, XP031415569 discloses a thin film SOI technology developed for RF switch applications and provides a buffer to protect the circuits from the RF signals. Other publications include WO2008/057524 assigned to Skyworks Solutions Inc., US2003/090313, Burgener et al, and US 2005/176184, Okihara Masao. However, none of the RF designs disclosed in these publications deal with the problem of unintended interactions of the RF and/or DC (or control) signals which are present, by injection of RF signals into the DC and low frequency analog blocks or by direct coupling of the wires on an IC chip. If a portion of the RF signal becomes inadvertently superimposed on the DC bias signals it degrades the linearity of the circuits making them unsuitable for wireless applications that demand low harmonic distortion.

One solution to the substrate interaction problem involves using an alternative substrate material such as sapphire. However, this significantly increases manufacturing costs and may not completely solve the interaction of RF and DC signals. Another solution involves the use of III-V technologies such as GaAs but this also increases costs and decreases integration levels.

There is therefore a need to provide a RF switch system, method and architecture to overcome the above mentioned problems.

Summary of the Invention

According to the present invention there is provided, as set out in the appended claims, a Radio Frequency (RF) system and method comprising:

a RF switch comprising a plurality of transistor switching elements implemented on Silicon on Insulator (SOI) for switching at least one or more RF signals;

said SOI comprises a bulk substrate region and a buried oxide region;

characterised by:

at least one filter adapted to isolate the RF signal from the substrate and/or other high frequency signals or control signals present in the RF system.

The advantage of the invention is that the filter eliminates any possibility of coupling to neighbouring bias lines or the substrate which will result in superior linearity in the RF switch and reduce any RF swing that is associated with prior art RF switches. The system provides flexibility in how bias lines are routed on an IC chip and can save die area on larger switches since isolation between the bias lines can still be achieved without taking precautions to space them far apart or shield them from one another.

In one embodiment there is provided a coupling capacitor adapted to cooperate with said at least one filter to improve linearity of the transistor switch elements.

In one embodiment the at least one filter is coupled to a gate bias line of at least one of said transistor switching elements.

In one embodiment there is provided a trench implant layer adapted with means for capturing free carriers at the interface between the bulk substrate region and buried oxide region.

In one embodiment the at least one filter is coupled to a gate bias line and body bias line of at least one of said transistor switching elements.

In one embodiment both the gate and body bias signals are connected to a filter which is connected to a bias resistor and connected to the source or drain of the switch transistor through a capacitor. This has the effect of filtering the rf signal from the control line outside the bias resistor preventing coupling to the substrate and neighbouring signals while allowing the rf signal to couple locally to the gate and body of the switch transistor to improve it's linearity.

In one embodiment the filters are located in close proximity to the negative voltage generator and digital control block to prevent injection of the RF signal from the transistor bias signals into these circuits causing non-linearities.

In one embodiment the filters are distributed across the RF system along with the switches to the DC supplies so that filtering occurs directly at the switch arm which

eliminates the need to bus control signals with RF power superimposed across the RF system preventing injection of the RF power into the substrate as well as preventing coupling between control lines which will improve linearity.

In another embodiment partial filtering occurs locally at the at least one transistor and further filtering occurs at the digital block and negative voltage generator circuit blocks.

In another embodiment the width of the first and last transistor in the switch arm is reduced to fit the coupling capacitors into the same switch area without the coupling capacitors.

In a further embodiment the invention utilizes a trench implant layer in the semiconductor substrate that alleviates the problem of substrate charge build-up. In one embodiment the trench layer comprises means for capturing free carriers at the bulk substrate/buried oxide interface. The trench layer is typically implanted during the manufacturing process. This implanted trench layer captures the free carriers at the bulk substrate/buried oxide interface and so stops the charge build-up that creates the weak inversion layer. This improves the insertion loss performance of the RF switch and also reduces the generation of harmonic products.

In one embodiment the trench implant layer substantially surrounds at least one of the transistor switching elements.

In one embodiment at least one transistor comprises a connected drain-source resistor, Rds, to improve the linearity performance of the RF system. The use of the trench implant in RF switches yields improved switch performance in terms of insertion loss and linearity. The RF switch section consists of transistors that utilise drain-source resistors. The drain-source resistors improve the performance of the RF switch by increasing the linearity of the circuit.

In one embodiment the plurality of transistors are arranged in a stacked configuration.

In one embodiment at least one transistor element comprises a metal contact layer between source and drain regions using vias.

In one embodiment the metal interconnects to connect the drain of a first transistor to the source of the next transistor arranged in series.

In one embodiment a trench layer is positioned underneath the metal contact layers and/or metal interconnects tracks in the RF system.

In one embodiment said system comprises a digital control block and a negative voltage generator.

In one embodiment a filter comprises means to protect a digital control block and the negative voltage generator from high power high frequency signals present in the RF system.

In one embodiment the negative voltage generator comprises an oscillator circuit, a clock generator circuit and a charge pump.

In one embodiment the digital logic block comprises means to control the on-off state of the transistor elements of the RF system.

In a further embodiment of the present invention there is provided a Radio Frequency (RF) system comprising:

a RF switch comprising a plurality of transistor switching elements implemented on a layer of Silicon on Insulator (SOI);
a digital control block; and
a negative voltage generator,
wherein the layer of SOI comprises a trench implant layer to prevent unwanted substrate charge build-up.

In a further embodiment of the invention there is provided a method of manufacturing an RF system comprising the steps of:

arranging a plurality of transistor switching elements implemented on Silicon on Insulator (SOI), said SOI comprises a bulk substrate region and a buried oxide region;

positioning at least one filter adapted to isolate a RF signal from the substrate and/or other high frequency signals or control signals present in the RF system.

In a further embodiment there is provided a system comprising:

a switch comprising a plurality of transistor switching elements implemented on a layer of Silicon on Insulator (SOI);

said SOI layer comprises a bulk substrate region and a buried oxide region;

wherein a trench implant layer is provided with means for capturing free carriers at the interface between the bulk substrate region and buried oxide region.

In another embodiment there is provided a system comprising:

a switch comprising a plurality of transistor switching elements implemented on a layer of Silicon on Insulator (SOI);

a digital control block; and

a negative voltage generator,

wherein at least one transistor comprises a connected drain-source resistor, Rds, to improve the linearity performance of the system.

In another embodiment there is provided a Radio Frequency (RF) system comprising:

a RF switch comprising a plurality of transistor switching elements implemented on Silicon on Insulator (SOI) for switching at least one or more RF signals;

said SOI comprises a bulk substrate region and a buried oxide region;

a digital control block;

a negative voltage generator characterised by:

a trench implant layer adapted with means for capturing free carriers at the interface between the bulk substrate region and buried oxide region,

at least one filter adapted to isolate the RF signal from the substrate, the digital control block and/or negative voltage generator.

In another embodiment there is provided a RF switch comprising a plurality of transistor switching elements implemented on a semiconductor substrate for switching at least one or more RF signals; characterised by at least one filter adapted to isolate the RF signal from the substrate and/or other high frequency signals or control signals present in the RF system. The semiconductor substrate can be any type of material, but preferably comprises SOI material.

Brief Description of the Drawings

The present invention will be more clearly understood from the following description of an embodiment thereof, given by way of example only, with reference to the accompanying drawings, in which:

Figure 1 illustrates a cross-sectional diagram of a typical SOI process;

Figure 2 illustrates in block diagram of the main elements of an RF switch system;

Figure 3 illustrates an implementation of an RF switch containing two series and two shunt arms;

Figure 4 illustrates a cross-sectional diagram of a single NMOS transistor implemented in a standard SOI process;

Figure 5 illustrates the combination of a filter, a rf bias resistor and switch or shunt transistor, according to a preferred embodiment of the invention;

Figure 6 illustrates a filter and bias resistor on both the gate and body of the switch or shunt transistor, according to another embodiment of the invention;

Figure 7 illustrates a filter with a bias resistor and a coupling capacitor on the gate to drain, gate to source, body to drain and body to source terminals;

Figure 8 shows a filter blocking RF signals from reaching the digital logic blocks and the positive and negative power supplies;

Figure 9 illustrates an embodiment of a centralized filter bank according to another aspect of the invention;

Figure 10 illustrates the concept of a local filter per switch according to one embodiment of the invention;

Figure 11 illustrates a cross-sectional diagram of the charge build up in the substrate, occurring at the interface between the bulk substrate and the buried oxide;

Figure 12 illustrates a cross-sectional diagram of the trench implants that are used to remove the charge build-up in the substrate of an RF system according to one aspect of the invention;

Figure 13 shows a circuit level implementation of a switch arm where a number of transistors are connected together in series and parallel;

Figure 14 shows the same transistor level implementation of a switch arm as in Figure 13 except in this case the location of the trench layer implants is shown;

Figure 15 shows a layout view of a typical switch arm;

Figure 16 illustrates a cross-sectional diagram of the switch implementation of Figure 15;

Figure 17 illustrates a block diagram of the principle elements of the negative voltage generator block; and

Figure 18 illustrates a block diagram of the principle elements of the digital control block.

Detailed Description of the Drawings

Figure 1 illustrates a cross section of the principle elements of a typical SOI process. The SOI process consists of a thin silicon active area above an insulating layer. This insulating layer sits on top of a silicon substrate. A typical material for the insulating layer is silicon dioxide. In general SOI technologies consist of a bulk substrate 1, a buried oxide layer 2 and another thin active silicon layer 3. The bulk substrate 1 is generally a high resistivity substrate. The bulk substrate 1 can be either P-type or N-Type. A typical thickness for the bulk substrate is 250μm. The buried oxide layer 2 is an insulator layer, typically silicon dioxide. A typical thickness of the buried oxide layer 2 is 1um. The silicon layer 3 above the buried oxide is a thin layer of the order of 0.2μm.

Figure 2 shows a block diagram of the principle elements of an RF switch system. A switch system consists of an RF switch section 10, a digital logic section 11 and a negative voltage generator section 12. The RF switch 10 shown is a single pole two throw (SP2T) switch. The switch has four switching elements. Each switching element can be turned on or off. Ideally, when the switch 10 is on it behaves as a short circuit and when it is off it behaves as an open circuit. The on/off state of each switching element is controlled by DC voltages from the digital logic control block. The logic inputs are used to control what control voltage is applied to each switching element. To

meet required performance levels in RF switch design a negative voltage is needed to control the off state of the switching element. This negative voltage is supplied by the negative voltage generator 12. The negative voltage generator 12 supplies the digital control block with a constant negative DC voltage. This negative DC voltage, along with the positive supply voltage, is then used by the digital control block 11 to control the switching elements.

A typical example of an RF switch section is illustrated in Figure 3. This figure shows a single pole two throw switch. It contains two series arms 20, 21 and two shunt arms 22 23. The series arms 20, 21 are used to control the flow of RF signals between different points of the RF system. The shunt devices 22, 23 are used to improve the RF performance of the circuit by increasing the isolation. The single pole two throw switch functions as follows: when series arm 20 is on, series arm 21 is off, shunt arm 22 is off and shunt arm 23 is on. The on/off state of each arm is controlled by positive and negative voltages from the digital control block. The positive and negative control voltages are applied to the gates of the transistors of each arm through large resistors (Rg). One important aspect of the present invention is the provision of drain-source resistors, Rds, 24 that are used on each transistor in the switch circuit. These Rds resistors 24 are used to improve the linearity performance of the switch circuit.

As shown in Figure 3 each switching element of the switch circuit consists of five transistors connected is series. This series connection of transistors is known as "stacking". Multiple transistors are stacked in this manner to design a switch that can operate under high voltage conditions. This idea behind using stacked transistors is to replace the single transistors in the switch by a series of two or more transistors. As a result, if *m* transistors are used in the stack, then the voltage seen across the source and drain of each of the transistors will be distributed evenly and will be reduced by a factor *m*.

However, the system can contain any number of transistors without deviating from the scope of this invention. An arm is turned on by the application of a positive voltage to the gate resistors, Rg, of the transistors of the particular arm. In the case of series arm 20 application of a positive voltage creates a low resistance path between node 1 and node

2. The lower the resistance of this path the less RF power is lost when a signal travels from node 1 to node 2. The amount of signal power lost between node 1 and node 2 is known as the insertion loss of the switch.

As shown in Figure 4 transistors are made in the thin active layer of the process. The transistor consists of drain, source and gate regions, gate dielectric and a channel region. The source and drain regions are created in this thin silicon layer using a suitable heavy dopant. The channel region is the area of active silicon between the source and drain. The gate dielectric is formed over the channel region. Isolation implants can also be implanted in areas of unused active silicon. Contact to the source and drain regions can be made using vias that connect to the processes' metal layers.

Figure 5 shows the placement of a filter 60 before a number of bias resistors 61 on the gate of a number of transistors 62 of one of the arms shown in Figure 3, according to a preferred embodiment of the invention. The bias resistor 61 is typically a large value of ~50-100k Ohms but is limited in how large it can be by the switching time requirements of the switch. As a result of this limitation some RF power will leak through the resistors to the gate bias line. This RF power can couple to the substrate from the gate bias line or couple to another bias line on the chip resulting in non-linearities in the switch behaviour. The filter 60 attenuates this RF power/voltage to isolate the RF signal from the substrate and/or other high frequency signals or control signals present in the RF system. Figure 6 is similar to Figure 5 except there is a filter placed on the body contact as well as the gate. The additional body contact improves the transistor linearity but this benefit can be lost if a filter is not present.

Figure 7 shows the addition of a coupling capacitor 64 to the transistors 62 at each end of a switch arm. Figure 7 illustrates the filter with the bias resistor and the coupling capacitor on the gate to drain, gate to source, body to drain and body to source terminals. The capacitor 64 will feed more of the RF voltage to the transistor gate and body. This is advantageous for the transistor since the change in bias with incoming RF power will reduce the voltage differentials on the transistor and help it's response to be more linear. However, without the presence of the filter 60 more RF power would also

be coupled to the bias line adding non-linearities elsewhere in the DC and analog circuits or through coupling to the substrate through the bias lines.

Figure 8 is similar to Figure 7 but shows how the filters isolate the digital and low frequency analog circuits 65 and 66 from the RF power which will improve linearity. Figure 8 shows the filter 60 blocking RF signals from reaching the digital logic blocks 65 and the positive and negative power supplies 66.

Figure 9 shows one possible implementation of the filters 60 which are located together and in close proximity to the digital and low frequency analog circuits 65. Figure 9 illustrates how bias lines 70 run around the chip and can create coupling according to one embodiment. The bias lines 70 are designed to be relatively long can run for approximately a millimetre in length around the chip. Without the presence of an RF filter 70 significant rf voltage would be present on the bias lines and would couple to other bias lines or to the substrate which would cause non linearities in the switch characteristics. The design of the filter 60 significantly reduces the voltage swings on the bias lines 70.

Figure 10 shows another implementation where filters 60a, 60b, 60c and 60d (and associated circuits) are placed local to each switch. Figure 10 illustrates how the local filter architecture removes the long bias lines, according to one embodiment. Figure 10 shows how local filters are used to reduce any rf voltage on the bias lines but more importantly dramatically reduce the length of the bias lines themselves thus eliminating any possibility of coupling to neighbouring bias lines or the substrate which will result in superior linearity in the switch. The local filter architecture eliminates the long bias lines on the IC chip eliminating any possibility of rf coupling to each other or to the substrate.

Figure 11 shows the region where charge build-up can occur in an SOI process indicated generally by the reference numeral 30. Free carriers in the bulk substrate form a weak inversion layer 30 at the interface between the bulk substrate 1 and the buried oxide layer 2. This weak inversion layer 30 has adverse affects on the RF performance of a switch circuit. It results in a varying parasitic capacitance over the RF cycle that

creates unwanted harmonic products and increases insertion loss of the switch circuit. This seriously impacts the usefulness of SOI as a process for the design of RF switches. However, an important aspect of the invention is that the effects of this inversion layer can be reduced by using a trench implant layer 31. This is illustrated in Figure 12. The trench layer 31 is typically implanted during the manufacturing process has means for capturing the free carriers at the bulk substrate/buried oxide interface and so stops the charge build-up that creates the weak inversion layer 30. This improves the insertion loss performance of the RF switch and also reduces the generation of harmonic products. The trench implant layer process was developed to reduce harmonic distortion caused by substrate-circuit interactions. The trench is built after the transistors have been formed. This is achieved by etching down to the substrate where active devices are not present and implanting the substrate to create damage which will inhibit the formation of mobile electrons at the substrate interface.

As shown in Figure 3 typical RF switch applications utilise a number of transistors connected in series. This is done so that the switch circuit can operate under high voltage conditions. Typical switch designs also utilise a number of transistors connected in parallel. Figure 13 shows a typical implementation of a single arm of a switch circuit. As illustrated there are M transistors connected, or stacked, in series. M can be any number depending on the particular design requirements. Each series transistor in the stack of M transistors can themselves be made up of N transistors connected in parallel. N can be any number depending on the particular design requirements. However the weak inversion layer 30 has adverse affects on the RF performance of a transistors, resulting in a varying parasitic capacitance over the RF cycle that creates unwanted harmonic products and increases insertion loss of the switch circuit as outlined above.

Figure 14 shows the same implementation as Figure 15 except in this case the trench implant layer 31 is utilized. As can be seen the trench layer 31 surrounds each of the parallel transistors from 1 to N and each of the stacked cells from 1 to M. The trench layer improves the insertion loss performance of the RF switch and also reduces the generation of harmonic products.

Figure 15 shows a layout view of three of the M series transistors and two of the N parallel transistors of Figure 4. As can be seen each transistor is completely surrounded by the trench implant layer 31. Figure 16 shows a cross-section of Figure 15. Metal interconnects are used to connect the drain of each transistor to the source of the next series transistor. A trench implant is used underneath each of these metal interconnects and between each transistor in the stack. Those skilled in the basic art of RF switch layout will see that many similar layout implementations are possible while not deviating significantly from the invention described here.

As shown in Figure 2 as well as the RF switch itself is a complete switch system comprised of a digital block and negative voltage generator block 12. Figure 17 shows a block diagram of the principle elements of a negative voltage generator. The negative voltage generator 12 contains an oscillator circuit 40, a clock generator circuit 41 and a charge pump 42. As stated already the arms of the RF switch need to be turned on and off at various times. For many applications a negative voltage is required to turn the transistor arm off. This is due to high power nature of certain applications and also to the stringent linearity requirements that must be met.

Figure 18 shows a block diagram of the principle elements of the digital control block 11. The digital logic block in its simplest form is comprised of a decoder circuit 50, level shifter 51 and a filter 52, which functions in the same way as the filter 60 described above. The level shifter 51 takes the negative voltage generated in the negative voltage generator as one of its inputs. The filter 52 prevents unwanted high power RF signals from the RF switch from damaging the digital logic blocks and the negative voltage generator block. The function of the digital logic block is to control the on-off state of the transistor arms of the RF switch. The RF transistors operate under high power conditions. Under certain operating conditions the level shifter can be exposed to these high power RF signals. The filter 52 is positioned between the level shifter outputs and the gate resistors of the RF transistors. The filter 52 functions by blocking any RF signals from reaching the level shifter and so protect the circuitry from damage.

It will be appreciated that in the context of the present invention SOI is a preferred substrate to bring the invention into effect, however it is envisaged any type of semiconductor substrate can be used that is suitable for making a RF switching system as hereinbefore described with respect to the description and/or figures.

In the specification the terms "comprise, comprises, comprised and comprising" or any variation thereof and the terms include, includes, included and including" or any variation thereof are considered to be totally interchangeable and they should all be afforded the widest possible interpretation and vice versa.

The invention is not limited to the embodiments hereinbefore described but may be varied in both construction and detail.

Claims

1. A Radio Frequency (RF) system comprising:
   a RF switch comprising a plurality of transistor switching elements implemented on Silicon on Insulator (SOI) substrate for switching at least one or more RF signals; said SOI comprises a bulk substrate region and a buried oxide region; characterised by:
   at least one filter adapted to isolate the RF signal from the substrate and/or other high frequency signals or control signals present in the RF system.

2. The RF system of claim 1 wherein a coupling capacitor is adapted to cooperate with said at least one filter to improve linearity of the transistor switch elements.

3. The RF system as claimed in claims 1 or 2 comprising a trench implant layer adapted with means for capturing free carriers at the interface between the bulk substrate region and buried oxide region.

4. The RF system as claimed in any preceding claim wherein the at least one filter is coupled to a gate bias line of at least one of said transistor switching elements.

5. The RF system as claimed in any preceding claim wherein the at least one filter is coupled to a gate bias line and body bias line of at least one of said transistor switching elements.

6. The RF system as claimed in any preceding claim wherein gate and body bias signals are connected to the at least one filter which is connected to a bias resistor and connected to the source or drain of the switch transistor through a capacitor.

7. The RF system as claimed in any preceding claim wherein partial filtering occurs locally at the at least one transistor and further filtering occurs at the digital block and negative voltage generator circuit blocks.

8. The RF system as claimed in any preceding claim wherein the width of the first and last transistor in the switch is reduced to fit the coupling capacitors into the same switch area without the coupling capacitors.

9. The RF system as claimed in any preceding claim wherein the trench implant layer substantially surrounds at least one of the transistor switching elements.

10. The RF system of claims as claimed in any preceding claim wherein at least one transistor comprises a connected drain-source resistor, Rds, to improve the linearity performance of the RF system.

11. The RF system of any preceding claim wherein the plurality of transistors are arranged in a stacked configuration.

12. The RF system of any preceding claim comprising metal interconnects to connect the drain of a first transistor to the source of the next transistor arranged in series.

13. The RF system of claim 12 wherein a trench layer is positioned underneath the metal contact layers and/or metal interconnects tracks in the RF system.

14. The RF system of any preceding claim wherein said system comprises a digital control block and a negative voltage generator.

15. The RF system as claimed in claim 14 wherein the at least one filter comprises means to isolate the digital control block and the negative voltage generator from high power high frequency signals present in the RF system.

16. The RF system as claimed in claims 14 or 15 wherein the negative voltage generator comprises an oscillator circuit, a clock generator circuit and a charge pump.

17. The RF system as claimed in any of claims 14 to 16 wherein the digital logic block comprises means to control the on-off state of the transistor elements of the RF system.

18. A method of manufacturing an RF system comprising the steps of:

arranging a plurality of transistor switching elements implemented on Silicon on Insulator (SOI), said SOI comprises a bulk substrate region and a buried oxide region;

positioning at least one filter adapted to isolate a RF signal from the substrate and/or other high frequency signals or control signals present in the RF system.

19. The method of claim 18 comprising the step of implanting a trench implant layer between said substrate and buried oxide region for capturing free carriers at the interface between the bulk substrate region and buried oxide region.

20. The method of claim 19 wherein the trench implant layer substantially surrounds at least one of the transistor switching elements.

Drawings

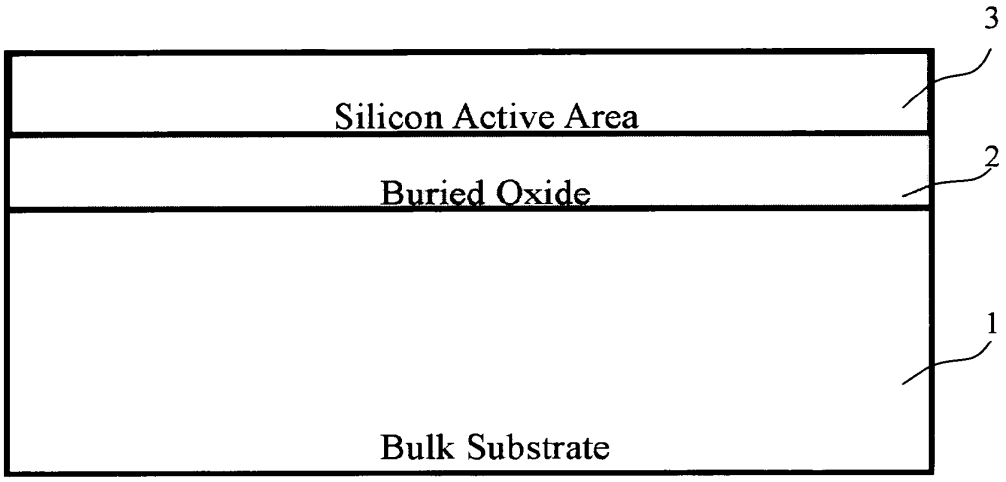

Figure 1

EX-1037
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0268

10
Switching element
+/- Vctrl
+/- Vctrl
+/- Vctrl
+/- Vctrl
RF Switch
Digital Logic Control
- Vctrl
Negative Voltage Generator
12
Logic Inputs
11
Vsupply

Figure 2

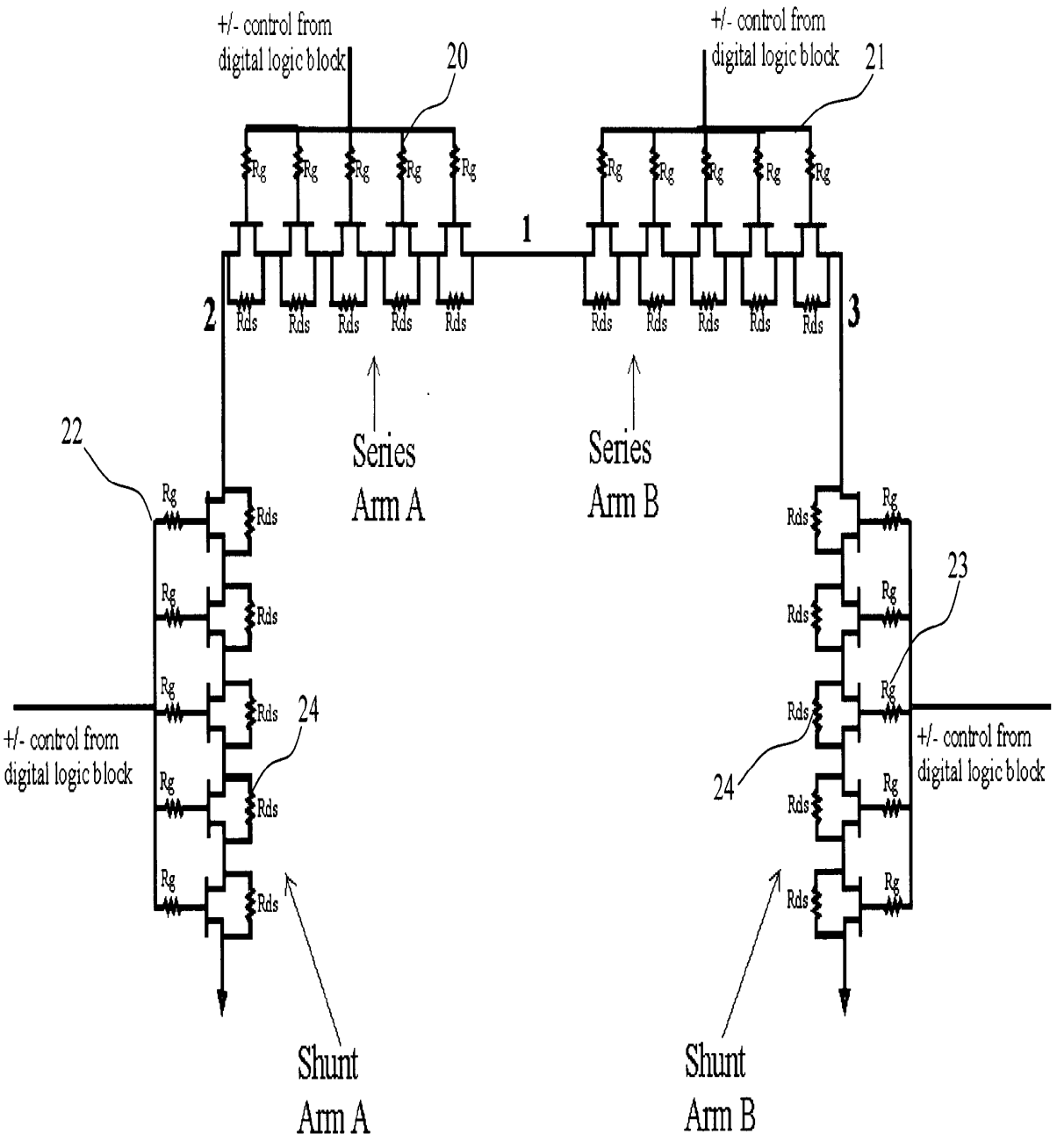

Figure 3

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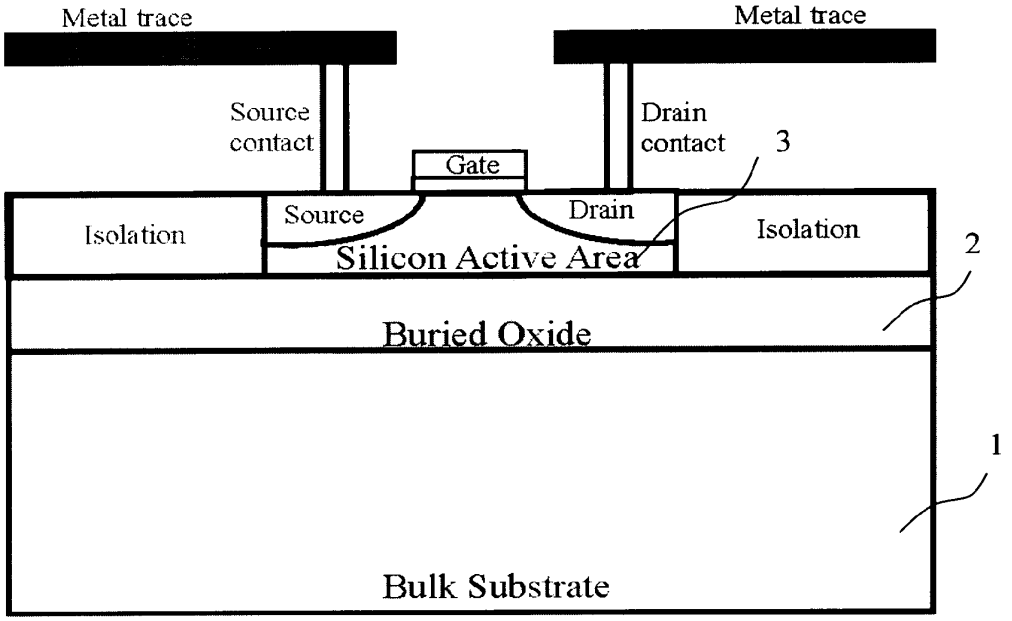

Figure 2

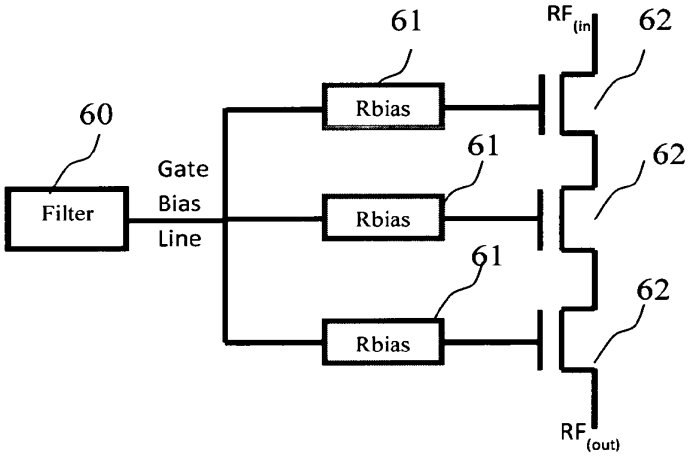

Figure 5

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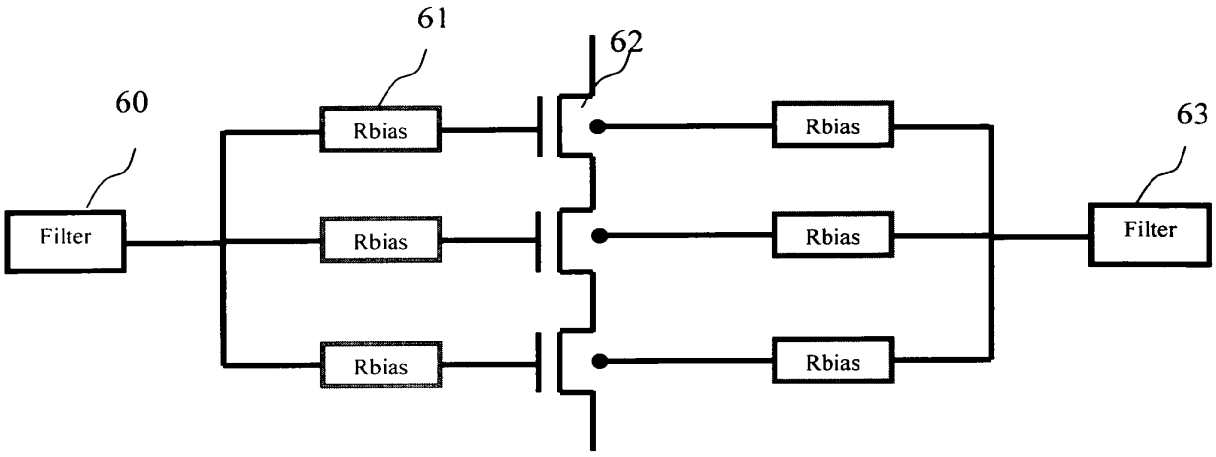

Figure 6

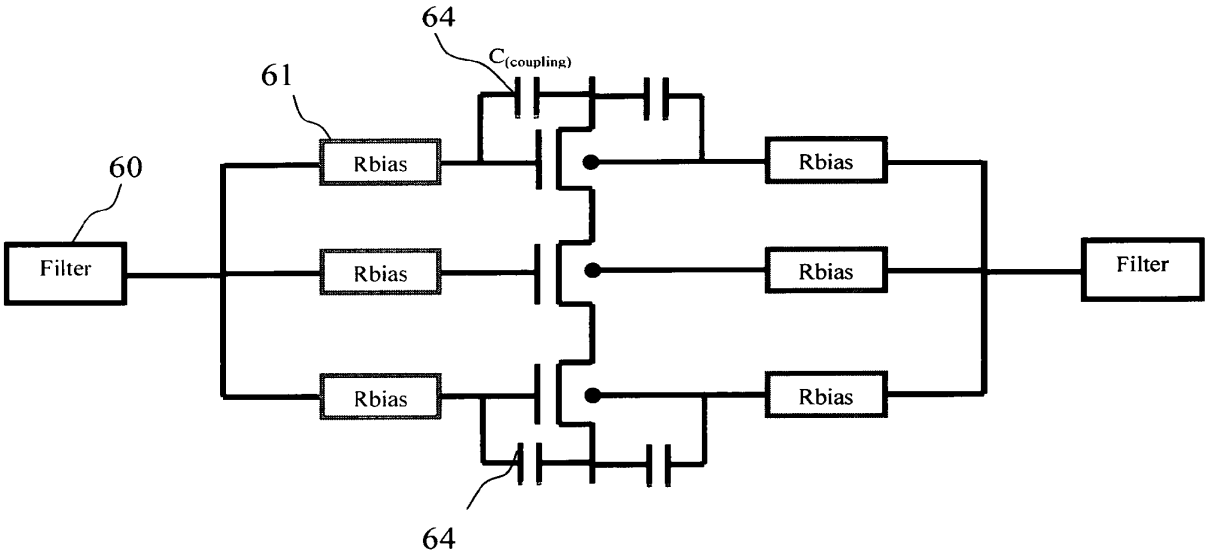

Figure 7

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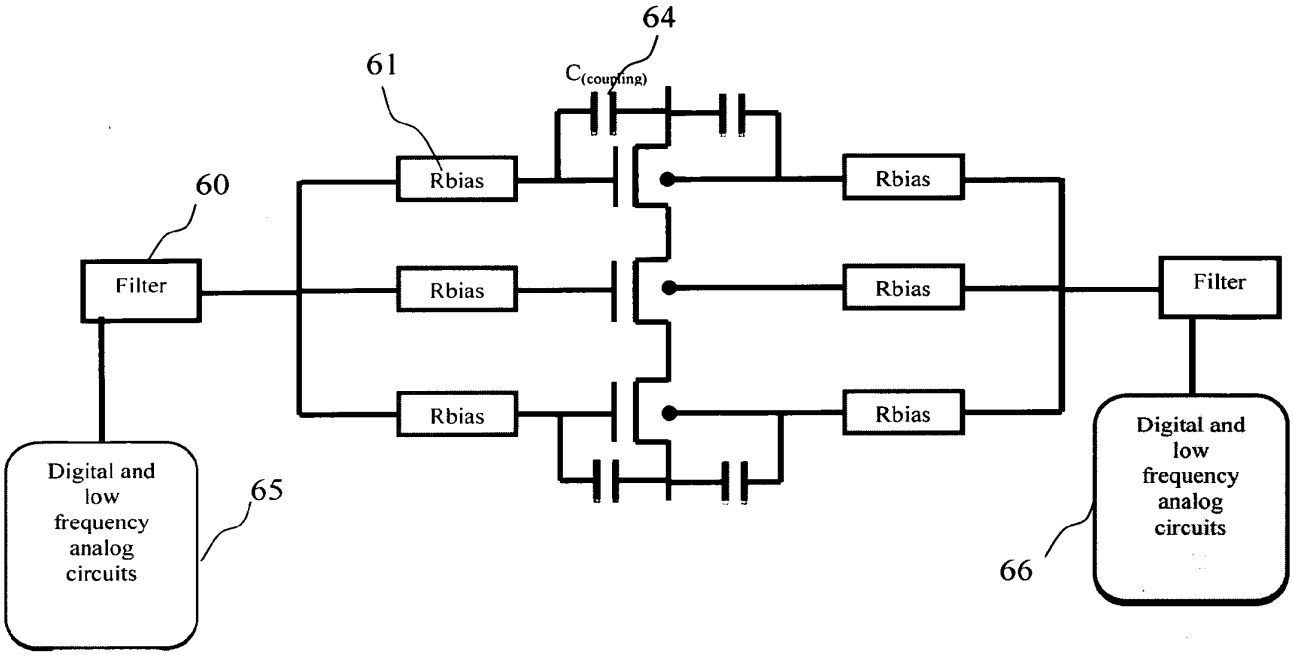

Figure 8

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0273

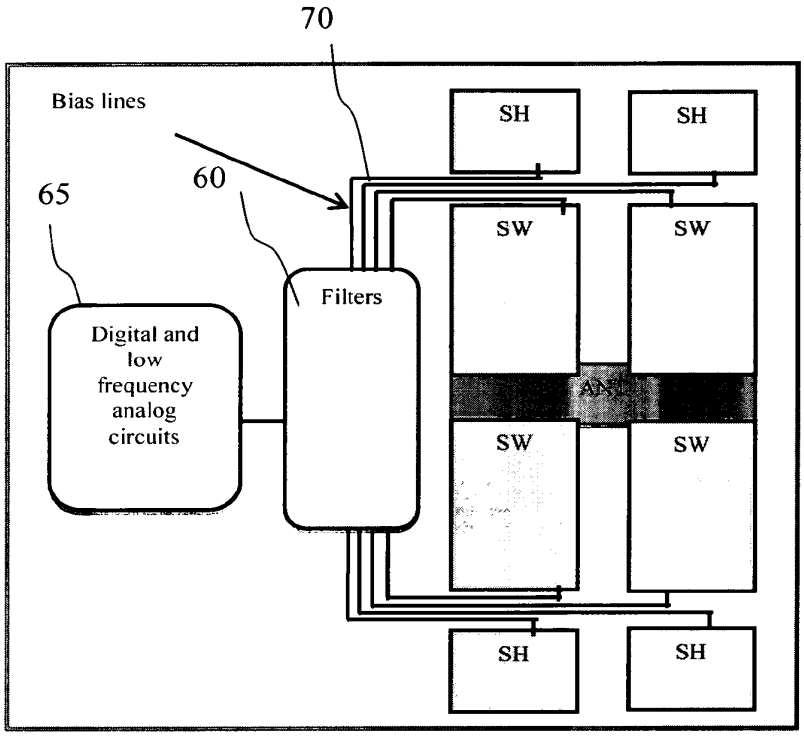

Figure 9

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Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.
0274

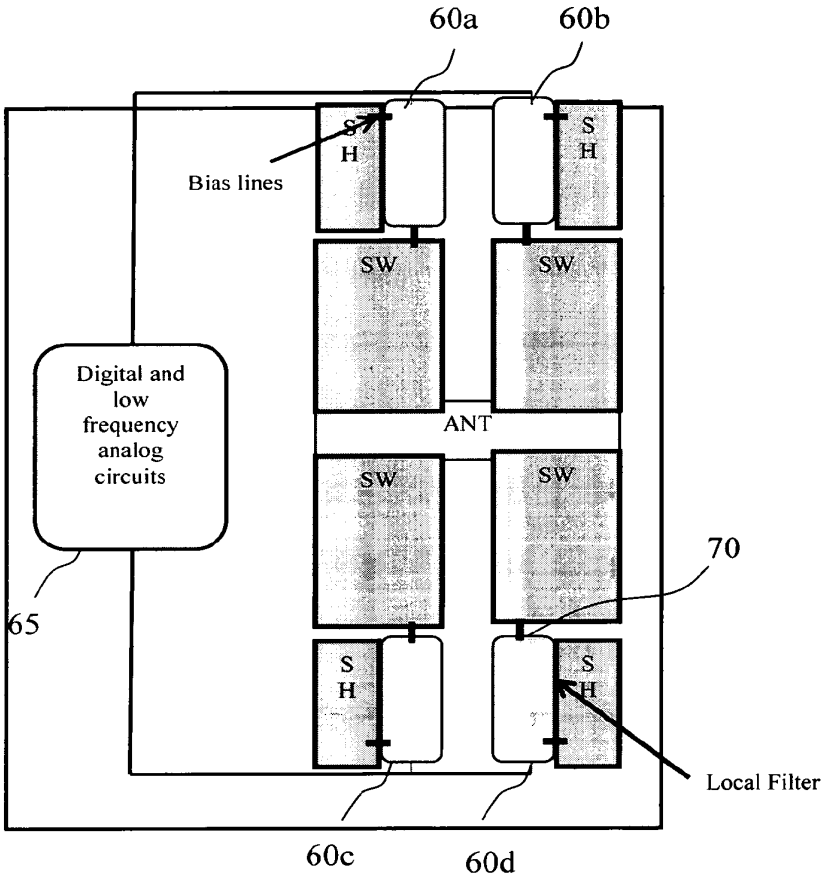

Figure 10

EX-1037
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.
0275

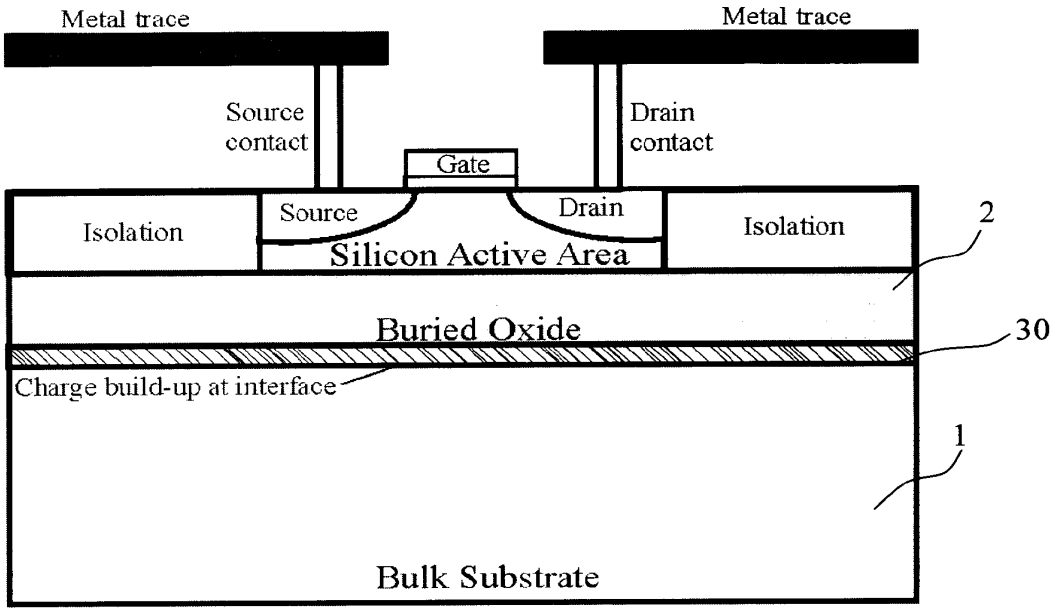

Figure 11

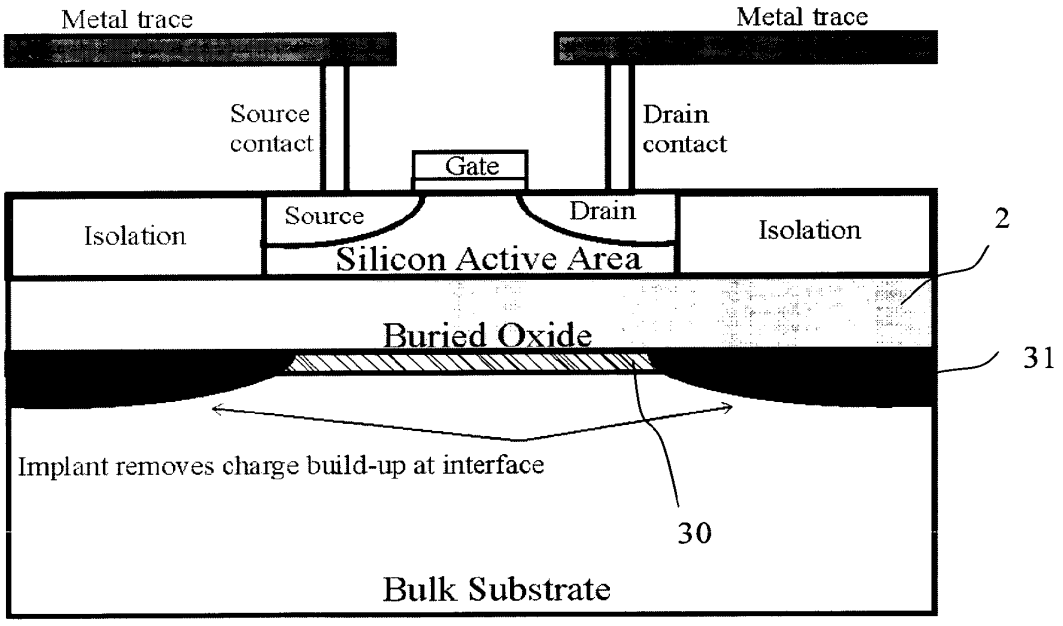

Figure 12

EX-1037
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.
0276

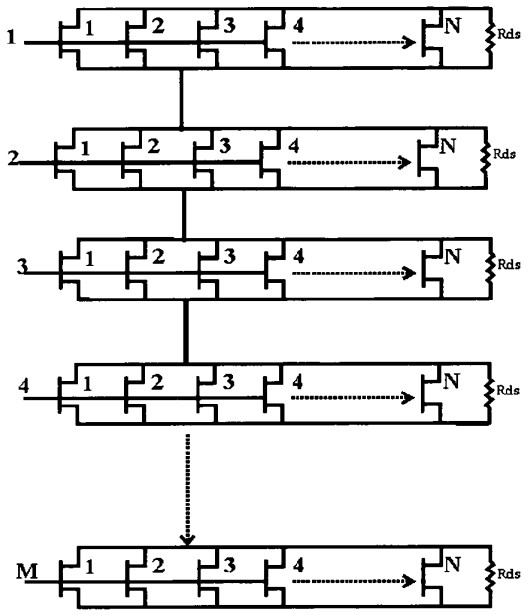

Figure 13

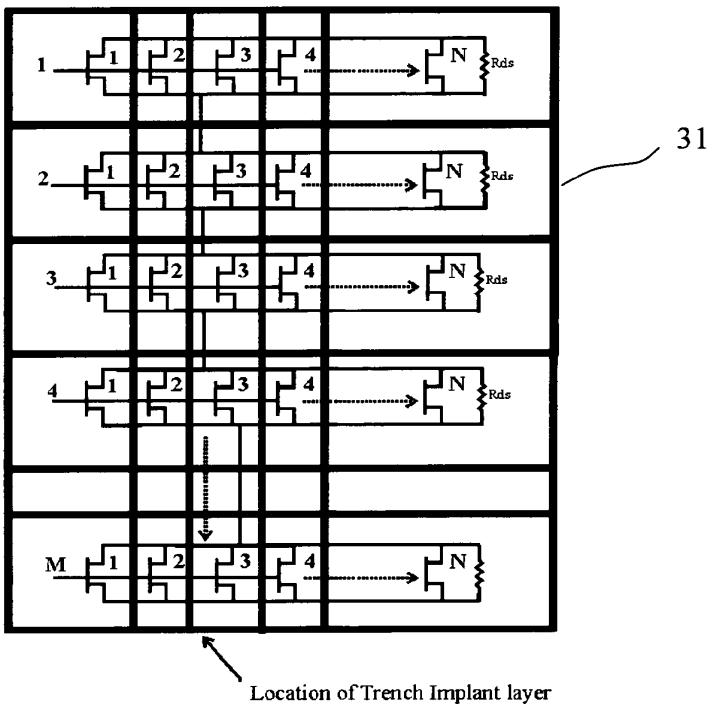

Figure 14

EX-1037
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.
0277

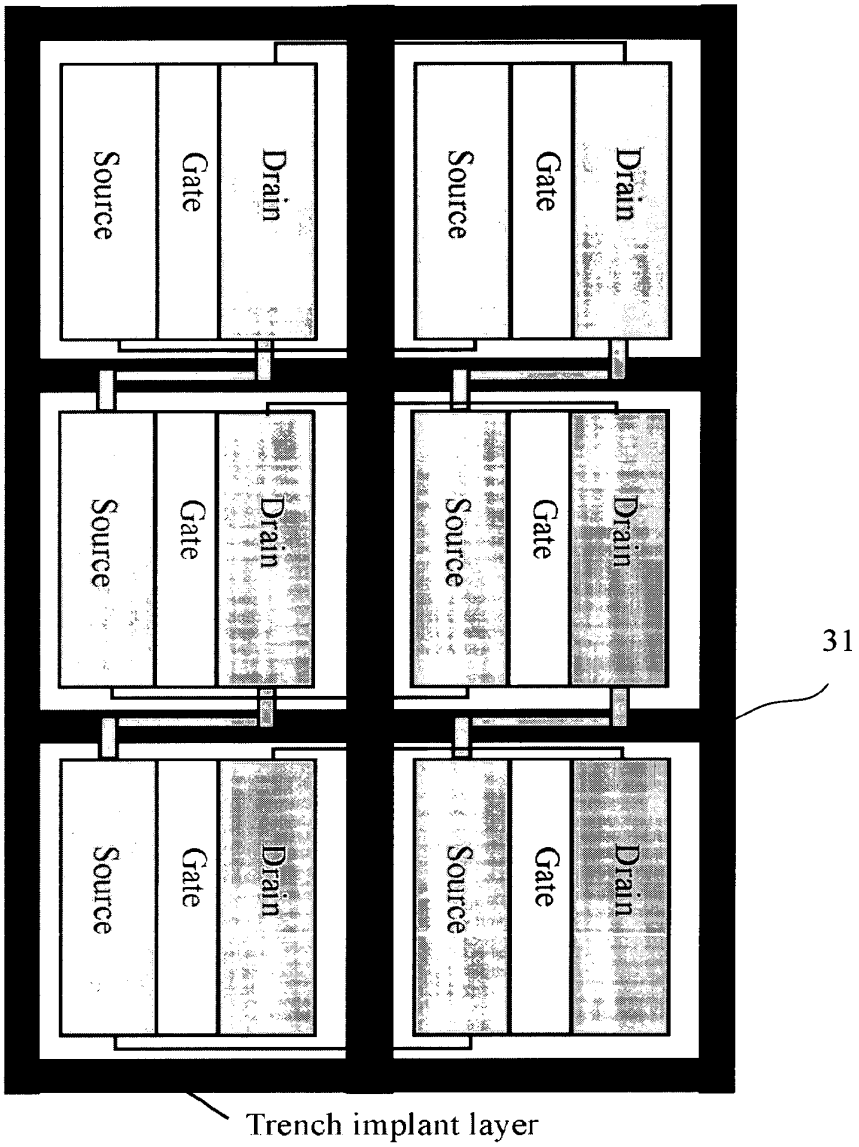

Figure 15

EX-1037
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.
0278

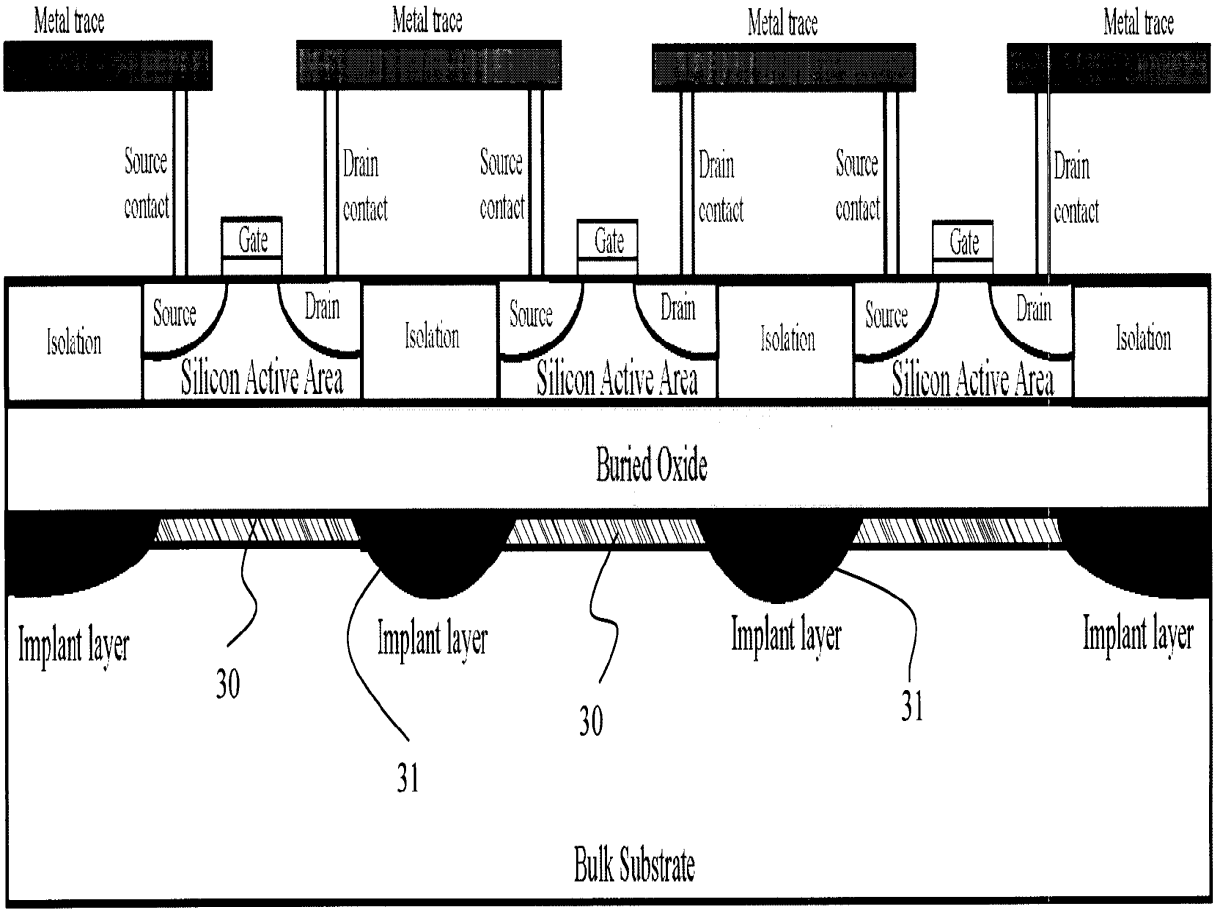
Metal trace
Metal trace
Metal trace
Metal trace
Source contact
Drain contact
Source contact
Drain contact
Source contact
Drain contact
Gate
Gate
Gate
Isolation
Source
Drain
Isolation
Source
Drain
Isolation
Source
Drain
Isolation
Silicon Active Area
Silicon Active Area
Silicon Active Area
Buried Oxide
Implant layer
Implant layer
Implant layer
Implant layer
30
31
30
31
Bulk Substrate

Figure 16

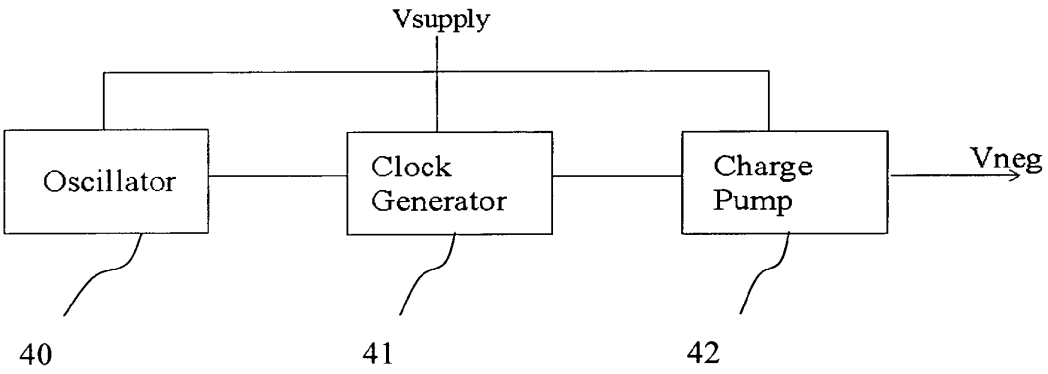

Figure 17

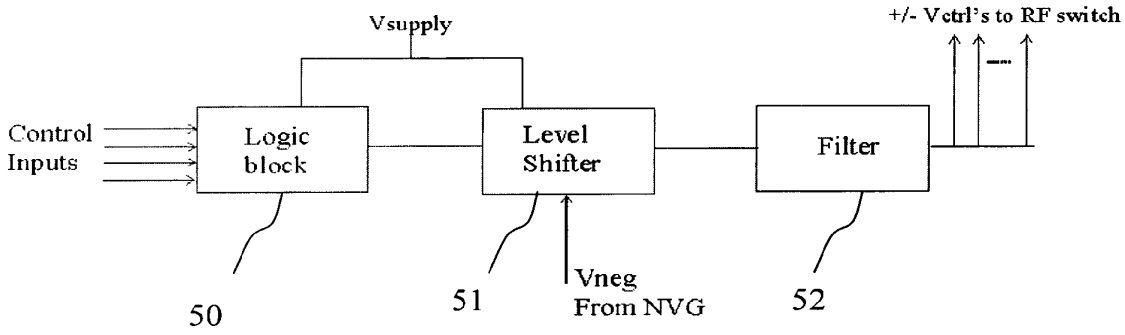

Figure 18

EX-1037
Kangxi Communication Technologies (Shanghai) Co., Ltd. v. Skyworks Solutions, Inc.
0280

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
HALE ALAN

FERNANDO HALE & CHANG LLP 4199 CAMPUS DRIVE, SUITE 550, #115 IRVINE CA 92612 USA

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Applicant's or agent's file reference 7591550035WO	Date of mailing *(day/month/year)* 23 December 2013 (23.12.2013) **FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. **PCT/US2013/049500**	International filing date *(day/month/year)* **06 July 2013 (06.07.2013)**

Applicant
SKYWORKS SOLUTIONS, INC.

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:

The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 - 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90bis.1 and 90bis.3).

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices. In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the PCT Applicant's Guide, National Chapters.

Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer COMMISSIONER Telephone No. 82-42-481-8754

Form PCT/ISA/220 (July 2010)

* Attention

Copies of the documents cited in the international search report can be searched in the following Korean Intellectual Property Office English website for three months from the date of mailing of the international search report.

http://www.kipo.go.kr/en/ => PCT Services => PCT Services

ID : PCT international application number
PW : **B788CL39**

Inquiries related to PCT International Search Report or Written Opinion prepared by KIPO as an International Searching Authority can be answered not only by KIPO but also through IPKC (Intellectual Property Korea Center), located in Vienna, VA, which functions as a PCT Help Desk for PCT applicants.

Homepage: http://www.ipkcenter.com

Email: ipkc@ipkcenter.com

Notes to Form PCT/ISA/220 (July 2010)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 759155003SWO	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. **PCT/US2013/049500**	International filing date *(day/month/year)* **06 July 2013 (06.07.2013)**	(Earliest) Priority Date *(day/month/year)* 07 July 2012 (07.07.2012)

Applicant

SKYWORKS SOLUTIONS, INC.

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 6 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed
      ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (See Box No. II)
3. ☒ **Unity of invention is lacking** (See Box No. III)
4. With regard to the **title,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:
5. With regard to the **abstract,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. With regard to the drawings,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 44A
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/049500

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Group 1, claims 1-21, directed to a radio-frequency (RF) switch comprising a coupling circuit that couples a respective body and gate of at least one first FET, the coupling circuit configured to be switchable between a resistive-coupling mode and a boy-floating mode.

Group 2, claims 22-56, 209-236, 307-326 directed to a radio-frequency (RF) switch comprising a compensation circuit connected to a respective source of at least one FET, the compensation circuit configured to compensate a non-linearity effect generated by the at lest one FET.

(See supplemental box)

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.: 1-21

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/049500

A. CLASSIFICATION OF SUBJECT MATTER

H03K 17/687(2006.01)i, H04B 1/44(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K 17/687; H04B 1/44; H03K 17/16; H04B 1/28; H01L 29/78; H03B 1/00; H03K 17/693; H01L 21/822

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords:float, body, gate, resistor, capacitor, switch, transistor, coupling circuit, semiconductor, antenna

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011-0169550 A1 (BRINDLE et al.) 14 July 2011 See paragraphs [0069]-[0081],[0130]-[0139],[0147]-[0163], and figures 2A-5D.	1-21
A	JP 2005-515657 A (PEREGRINE SEMICONDUCTOR CORPORATION) 26 May 2005 See abstract, pages 9-13, and figures 1A-5B.	1-21
A	US 2008-0272824 A1 (FU et al.) 06 November 2008 See abstract, paragraphs [0014]-[0017], and figures 2-3.	1-21
A	US 2006-0012407 A1 (BECHMAN et al.) 19 January 2006 See paragraphs [0015]-[0030], and figures 1-2.	1-21
A	US 2006-0199568 A1 (KELLY et al.) 07 September 2006 See paragraphs [0036]-[0055], and figures 1-6.	1-21

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 December 2013 (23.12.2013)	**23 December 2013 (23.12.2013)**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. +82-42-472-7140	KIM, Sung Gon Telephone No. +82-42-481-8746

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/049500

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011-0169550 A1	14/07/2011	CN 101218683 A0	09/07/2008
		CN 101218683 B	14/11/2012
		EP 1902474 A1	26/03/2008
		EP 1925030 A2	28/05/2008
		EP 2348532 A2	27/07/2011
		EP 2348532 A3	30/05/2012
		EP 2348533 A2	27/07/2011
		EP 2348533 A3	06/06/2012
		EP 2348534 A2	27/07/2011
		EP 2348534 A3	06/06/2012
		EP 2348535 A2	27/07/2011
		EP 2348535 A3	06/06/2012
		EP 2348536 A2	27/07/2011
		EP 2348536 A3	06/06/2012
		JP 05215850 B2	19/06/2013
		JP 2009-500868 A	08/01/2009
		JP 2013-138211 A	11/07/2013
		US 2007-0016247 A1	25/01/2007
		US 2007-0060291 A1	29/03/2007
		US 2008-0076371 A1	27/03/2008
		US 2012-169398 A1	05/07/2012
		US 7890891 B2	15/02/2011
		US 7910993 B2	22/03/2011
		US 8129787 B2	06/03/2012
		US 8140035 B2	27/03/2012
		US 8405147 B2	26/03/2013
		WO 2007-006934 A1	18/01/2007
		WO 2007-035610 A2	29/03/2007
		WO 2007-035610 A3	16/10/2008
JP 2005-515657 A	26/05/2005	AT 497642 T	15/02/2011
		DE 60239105 D1	17/03/2011
		EP 1451890 A2	01/09/2004
		EP 1451890 A4	17/11/2004
		EP 1451890 B1	02/02/2011
		EP 2387094 A1	16/11/2011
		US 2003-0090313 A1	15/05/2003
		US 2006-0017789 A1	27/01/2006
		US 2006-0194567 A1	31/08/2006
		US 2007-0120103 A1	31/05/2007
		US 2009-0117871 A1	07/05/2009
		US 2011-0092179 A1	21/04/2011
		US 6804502 B2	12/10/2004
		US 7123898 B2	17/10/2006
		US 7460852 B2	02/12/2008
		US 7529532 B1	05/05/2009
		US 7613442 B1	03/11/2009
		US 7796369 B2	14/09/2010
		US 7860499 B2	28/12/2010

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/049500

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		US 8583111 B2	12/11/2013
		WO 03-032431 A2	17/04/2003
US 2008-0272824 A1	06/11/2008	US 7848712 B2	07/12/2010
US 2006-0012407 A1	19/01/2006	US 7040863 B2	23/05/2006
		WO 2006-016954 A2	16/02/2006
		WO 2006-016954 A3	22/06/2006
US 2006-0199563 A1	07/09/2006	US 7619462 B2	17/11/2009

Form PCT/ISA/210 (patent family annex) (July 2009)

(Continued on Box No. III)

Group 3, claims 57-76, directed to a radio-frequency (RF) switch comprising a switchable resistive coupling circuit connected to each of respective gates and a switchable resistive grounding circuit connected to each of respective bodies.

Group 4, claims 77-101, directed to a radio-frequency (RF) switch comprising a resonance circuit that connects a body of each of at least one FET to a reference node.

Group 5, claims 102-166, directed to a radio-frequency (RF) switch comprising a coupling circuit configured to allow discharge of interface charge from a respective body.

Group 6, claims 167-183, directed to a radio-frequency (RF) switch system comprising a capacitor connected in series with a switch and configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

Group 7, claims 184-208, directed to a radio-frequency (RF) switch comprising an adjustable-resistance circuit connected to either or both of respective gate and bod of at lest one FET.

Group 8, claims 237-282, directed to a radio-frequency (RF) switch comprising a coupling circuit including a diode in series with a resistor and configured to facilitate removal of excess charge form a respective body.

Group 9, claims 283-306, directed to a switch circuit comprising a voltage distribution circuit configured to reduce voltage distribution variation across a switch.

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
HALE ALAN

FERNANDO HALE & CHANG LLP 4199 CAMPUS DRIVE, SUITE 550, #115 IRVINE CA 92612 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**23 December 2013 (23.12.2013)**
Applicant's or agent's file reference 7591550035WO	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2013/049500	**06 July 2013 (06.07.2013)**	07 July 2012 (07.07.2012)

International Patent Classification (IPC) or both national classification and IPC
H03K 17/687(2006.01)i, H04B 1/44(2006.01)i

Applicant
SKYWORKS SOLUTIONS, INC.

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [x] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. +82-42-472-7140	23 December 2013 (23.12.2013)	KIM, Sung Geon Telephone No. +82-42-481-8746

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2013/049500

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of :

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)

   ☐ on paper

   ☐ in electronic form

   b. (time)

   ☐ in the international application as filed.

   ☐ together with the international application in electronic form.

   ☐ subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2013/049500

Box No. IV Lack of unity of invention

1. ☒ In response to the invitation (Form PCT/ISA/206) to pay additional fees the applicant has, within the applicable time limit:
   - ☐ paid additional fees
   - ☐ paid additional fees under protest and, where applicable, the protest fee
   - ☐ paid additional fees under protest but the applicable protest fee was not paid
   - ☒ not paid additional fees
2. ☐ This Authority found that the requirement of unity of invention is not complied with and chose not to invite the applicant to pay additional fees.
3. This Authority considers that the requirement of unity of invention in accordance with Rule 13.1, 13.2 and 13.3 is
   - ☐ complied with
   - ☒ not complied with for the following reasons:

This ISA found multiple inventions as follows:

Group 1, claims 1-21, directed to a radio-frequency (RF) switch comprising a coupling circuit that couples a respective body and gate of at least one first FET, the coupling circuit configured to be switchable between a resistive-coupling mode and a boy-floating mode.

Group 2, claims 22-56, 209-236, 307-326 directed to a radio-frequency (RF) switch comprising a compensation circuit connected to a respective source of at least one FET, the compensation circuit configured to compensate a non-linearity effect generated by the at lest one FET.

Group 3, claims 57-76, directed to a radio-frequency (RF) switch comprising a switchable resistive coupling circuit connected to each of respective gates and a switchable resistive grounding circuit connected to each of respective bodies.

Group 4, claims 77-101, directed to a radio-frequency (RF) switch comprising a resonance circuit that connects a body of each of at least one FET to a reference node.

Group 5, claims 102-166, directed to a radio-frequency (RF) switch comprising a coupling circuit configured to allow discharge of interface charge from a respective body.

Group 6, claims 167-183, directed to a radio-frequency (RF) switch system comprising a capacitor connected in series with a switch and configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

Group 7, claims 184-208, directed to a radio-frequency (RF) switch comprising an adjustable-resistance circuit connected to either or both of respective gate and bod of at lest one FET.

Group 8, claims 237-282, directed to a radio-frequency (RF) switch comprising a coupling circuit including a diode in series with a resistor and configured to facilitate removal of excess charge form a respective body.

Group 9, claims 283-306, directed to a switch circuit comprising a voltage distribution circuit configured to reduce voltage distribution variation across a switch.

The inventions listed as Groups 1-9 do not ralate to a single general inventive concept under PCT Rule 13.1, because the above mention groups of claims do not share any of the technical features

Continued on Supplemental Box

4. Consequently, this opinion has been established in respect of the following parts of the international application :
   - ☐ all parts.
   - ☒ the parts relating to claims Nos. 1-21

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2013/049500

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-21	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	NONE	YES
	Claims	1-21	NO
Industrial applicability (IA)	Claims	1-21	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:
D1: US 2011-0169550 A1 (BRINDLE et al.) 14 July 2011

1. Novelty and Inventive Step

1.1 Claims [1-9]

D1, which is considered to be the closest prior art to the subject matter of independent claim [1], discloses a radio-frequency (RF) switch comprising: at least one first metal-oxide-field-effect transistor (MOSFET) (528) disposed between an input terminal (504) and an output terminal (505), each of the at least one first MOSFET having a respective body and gate; and a coupling circuit that couples an accumulated charge sink (ACS) terminal (508') and a gate terminal (502') (See paragraphs [0130]-[0139], [0147]-[0163], and figures 4A-5D in D1). The present invention slightly differs from D1 in that claim [1] comprises a coupling circuit configured to be switchable between a resistive-coupling mode and a body floating-mode, whereas D1 discloses the coupling circuit configured to remove an accumulated charge and implement a floating body condition. However, such a slight design change comes within the scope of customary practice followed by a person skilled in the art. Accordingly, claim [1] would have been obvious over D1.

The additional feature of claim [2] is known from D1 in the feature of the first MOSFET (528) which is a silicon-on-insulator MOSFET (See paragraphs [0148]-[0160], and figures 5A-5D in D1).

The additional features of claims [3-4] are virtually suggested by the features of D1 considering that the coupling circuit includes a diode (509); and the first MOSFET (528) is connected to a second MOSFET (526) (See paragraphs [0152]-[0162], and figures 5A-5D in D1).

Continued on Supplemental Box

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of : Box No. IV

identified.

In this case, the first named invention that will be searched without additional fees is Group I that is directed to a coupling circuit that couples a respective body and gate of at least one first FET, the coupling circuit configured to be switchable between a resistive-coupling mode and a boy-floating mode.

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of : Box No. V

The additional features of claims [5-6] are virtually suggested by the features of D1 considering that the first MOSFET (528) is configured to effectively remove accumulated charge when a device operates in an OFF-state, yet assume the characteristics of a floating body device when the device operates in an ON-state (See paragraphs [0130]-[0133], and figures 5A-5D in D1).

The additional feature of claim [7] is known from D1 in the feature of a gate resistor (514) connected to the gate terminal (502') (See paragraphs [0148]-[0150], and figures 5A-5D in D1).

The additional feature of claim [8] is known from D1 in the feature of the input terminal (504) configured to receive an RF signal having a power value and the output terminal (505) configured to output the RF signal when the second MOSFET (526) is in the ON-state (See paragraphs [0155]-[0159], and figures 5A-5D in D1).

The additional feature of claim [9] relates to the feature of at least one first FET including N FETs connected in series, the quantity N selected to allow a switch circuit to handle the power of an RF signal, which is merely a matter of design option when the general knowledge in the relevant field of the art is used.

Therefore, claims [1-9] lack an inventive step under PCT Article 33(3).

1.2 Claim [10]

Independent claim [10] relates to a method for operating a radio-frequency (RF) switch. However, its technical feature is the same as that of claim 1. The only difference is a matter of category. Accordingly, claim [10] would also have been obvious over D1. Therefore, claim [10] lacks an inventive step under PCT Article 33(3).

1.3 Claims [11-13]

Independent claim [11] is substantially the same as claim 1 except for a semiconductor die comprising a semiconductor substrate. However, such a slight design change comes within the scope of customary practice followed by a person skilled in the art. Accordingly, claim [11] would also have been obvious over D1.

The additional features of claims [12-13] are virtually suggested by the features of D1

Continued on The Next Page

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of : Previous Page

considering MOSFETs disposed on a Semiconductor-On-Insulator (SOI) substrate (See paragraphs [0077]-[0081], and figures 2A-3D in D1).

Therefore, claims [11-13] lack an inventive step under PCT Article 33(3).

1.4 Claims [14-15]

Independent claim [14] relates to a method for fabricating a semiconductor die. However, its technical feature is the same as that of claim 11. The only difference is a matter of category. Accordingly, claim [14] would also have been obvious over D1.

The additional feature of claim [15] is virtually suggested by the feature of D1 considering forming MOSFETs on a Semiconductor-On-Insulator (SOI) substrate (See paragraphs [0077]-[0081], and figures 2A-3D in D1).

Therefore, claims [14-15] lack an inventive step under PCT Article 33(3).

1.5 Claim [16-20]

Independent claim [16] is substantially the same as claim 1 except for a semiconductor die and a packaging substrate. However, such a slight design change comes within the scope of customary practice followed by a person skilled in the art. Accordingly, claim [16] would also have been obvious over D1.

The additional feature of claim [17] is virtually suggested by the feature of D1 considering that a Semiconductor-On-Insulator (SOI) substrate is a silicon-on-insulator substrate (See paragraphs [0077]-[0081], and figures 2A-3D in D1)

The additional features of claims [18-20] are virtually suggested by the features of D1 considering that a coupling circuit including a diode (509) is a part of the SOI substrate as at least one MOSFET (See paragraphs [0147]-[0163], and figures 4A-5D in D1).

Therefore, claims [16-20] lack an inventive step under PCT Article 33(3).

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Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of : Previous Page

1.6 Claim [21]

D1, which is considered to be the closest prior art to the subject matter of independent claim [21], discloses a wireless device comprising: a transmission path (256) configured to process RF signals; an RF antenna (258) in communication with the transmission path (256) configured to facilitate transmission of the RF signal; a switch connected to the transmission path (256) and configured to selectively route the RF signal to the RF antenna (258), the switch including at least one first metal-oxide-field-effect transistor (MOSFET) (528) disposed between an input terminal (504) and an output terminal (505), each of the at least one first MOSFET having a respective body and gate, and the switch further including a coupling circuit that couples an accumulated charge sink (ACS) terminal (508') and a gate terminal (502') (See paragraphs [0069]-[0080], [0130]-[0139], [0147]-[0163], and figures 2A-2B,4A-5D in D1). The present invention slightly differs from D1 in that claim [21] comprises a power amplifier connected to a transceiver, and a coupling circuit configured to be switchable between a resistive-coupling mode and a body floating-mode, whereas D1 discloses the coupling circuit configured to remove an accumulated charge and implement a floating body condition. However, such a slight design change comes within the scope of customary practice followed by a person skilled in the art. Accordingly, claim [21] would have been obvious over D1. Therefore, claim [21] lacks an inventive step under PCT Article 33(3).

2. Industrial Applicability

Claims [1-21] are industrially applicable under PCT Article 33(4).

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION
First Named Inventor/Applicant Name:	Anuj Madan
Filer:	Alan Troy Hale
Attorney Docket Number:	75900-50031D1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1600**

Electronic Acknowledgement Receipt

EFS ID:	23284319
Application Number:	14833076
International Application Number:	
Confirmation Number:	3042
Title of Invention:	RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION
First Named Inventor/Applicant Name:	Anuj Madan
Customer Number:	115870
Filer:	Alan Troy Hale
Filer Authorized By:	
Attorney Docket Number:	75900-50031D1
Receipt Date:	22-AUG-2015
Filing Date:	
Time Stamp:	18:04:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1600
RAM confirmation Number	7284
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	ADS.pdf	1505770 6919e66426d952097f20b1b2514fb0f1a7161ad1	no	7
Warnings:					
Information:					
2	Drawings-only black and white line drawings	2015-08-22_DrawingsAsFiled.pdf	95462 94b9b517a18bf96bdf9485de91b3438e9d4f4783	no	9
Warnings:					
Information:					
3		2015-08-22_SpecAsFiled.pdf	117536 08763bc90d42934ce0b3e152339b496eac3fe1f8	yes	25

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	21
Claims	22	24
Abstract	25	25

Warnings:					
Information:					
4	Transmittal Letter	2015-08-22_Transmittal.pdf	13794 93e122cb9cf2bd8669f88d59aa5f6cf4ba294962	no	1
Warnings:					
Information:					
5	Oath or Declaration filed	2015-08-22_Declaration.pdf	2850612 1279549067aeca9d9fd88a7324764d515b62009c	no	3
Warnings:					
Information:					
6	Information Disclosure Statement (IDS) Form (SB08)	IDS.pdf	613473 ef0c732c4c9c818c4e561768e65074ab12bfc9c4	no	7

Warnings:					
Information:					
7	Foreign Reference	JP2005515657A.pdf	11034587 f7030420c5135bb56c280860be5543bebbbd19d3	no	169
Warnings:					
Information:					
8	Foreign Reference	WO2011045442A2.pdf	1101212 9fec4fe67f3043019fdc567a5fbcb1374e66a491	no	31
Warnings:					
Information:					
9	Non Patent Literature	PCTUS2013049500-ISR-WO-2013-12-23.pdf	1058354 86067a0968498d8021c889b9dc4c1ba8339fa0bd	no	16
Warnings:					
Information:					
10	Fee Worksheet (SB06)	fee-info.pdf	35207 8fa416e03f14f0870b83514d715e240042676b6e0	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	18426007		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	75900-50031D1
	Application Number	
Title of Invention	RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Anuj		Madan	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Cambridge	State/Province	MA	Country of Residence i	US

Mailing Address of Inventor:

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Address 2	Apt. 1

City	Cambridge	State/Province	MA
Postal Code	02140	Country i	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Fikret		Altunkilic	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	North Andover	State/Province	MA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	86 Turnpike Street
Address 2	

City	North Andover	State/Province	MA
Postal Code	01854	Country i	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Guillaume	Alexandre	Blin	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	75900-50031D1
	Application Number	
Title of Invention	RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION	

City	Carlisle	State/Province	MA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	82 Lowell Street		
Address 2			
City	Carlisle	State/Province	MA
Postal Code	01741	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	115870		
Email Address	mail@fhcip.com	Add Email	Remove Email

Application Information:

Title of the Invention	RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION		
Attorney Docket Number	75900-50031D1	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	9	Suggested Figure for Publication (if any)	9

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	75900-50031D1
	Application Number	
Title of Invention	RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION	

Customer Number	115870

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Division of	13936175	2013-07-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
13936175	non provisional of	61669045	2012-07-07

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) [i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country [i]	Filing Date (YYYY-MM-DD)	Access Code [i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	75900-50031D1
	Application Number	
Title of Invention	RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	75900-50031D1
	Application Number	
Title of Invention	RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION	

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

○ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
◉ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	SKYWORKS SOLUTIONS, INC.		
Mailing Address Information:			
Address 1	20 Sylvan Road		
Address 2			
City	Woburn	**State/Province**	MA
Country [i]	US	Postal Code	01801
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section only if non-applicant assignee information is desired to be included on the patent application publication in accordance with 37 CFR 1.215(b). Do not include in this section an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest), as the patent application publication will include the name of the applicant(s).

Remove

If the Assignee is an Organization check here. ☐

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	75900-50031D1
	Application Number	
Title of Invention	RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION	

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information:

Address 1	
Address 2	

City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/Alan T. Hale/			Date (YYYY-MM-DD)	2015-08-22
First Name	Alan	Last Name	Hale	Registration Number	68226

Additional Signature may be generated within this form by selecting the Add button. Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

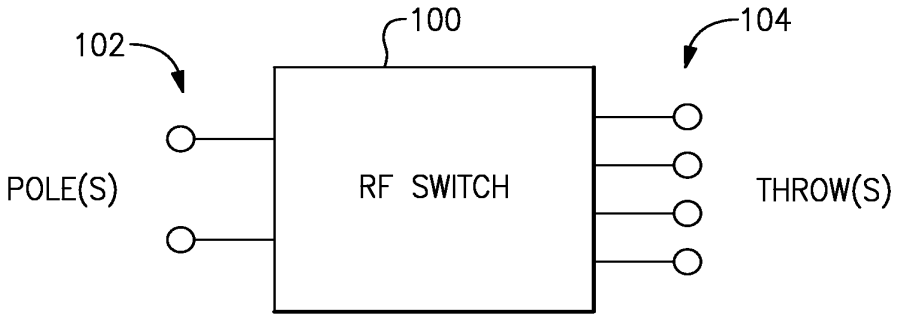
102
100
104
POLE(S)
RF SWITCH
THROW(S)

FIG.1

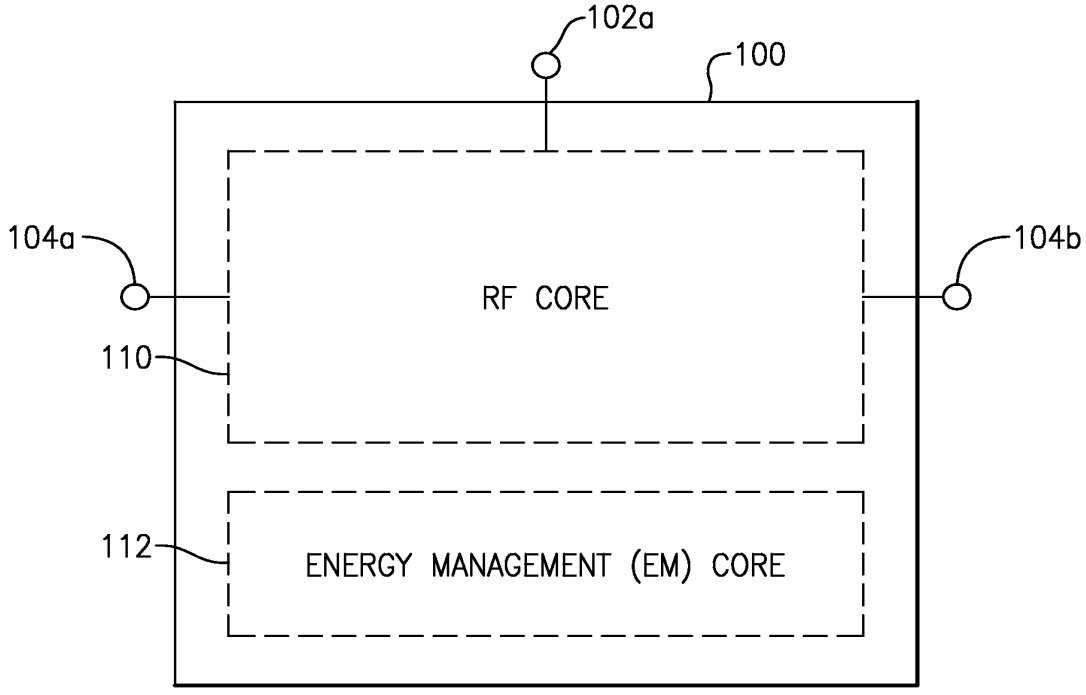
102a
100
104a
104b
RF CORE
110
112
ENERGY MANAGEMENT (EM) CORE

FIG.2

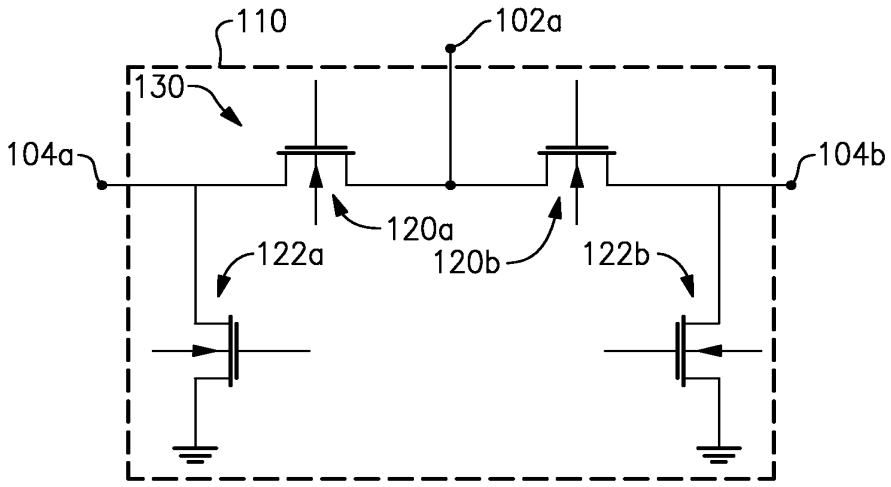
110
102a
130
104a
104b
120a
120b
122a
122b

FIG.3

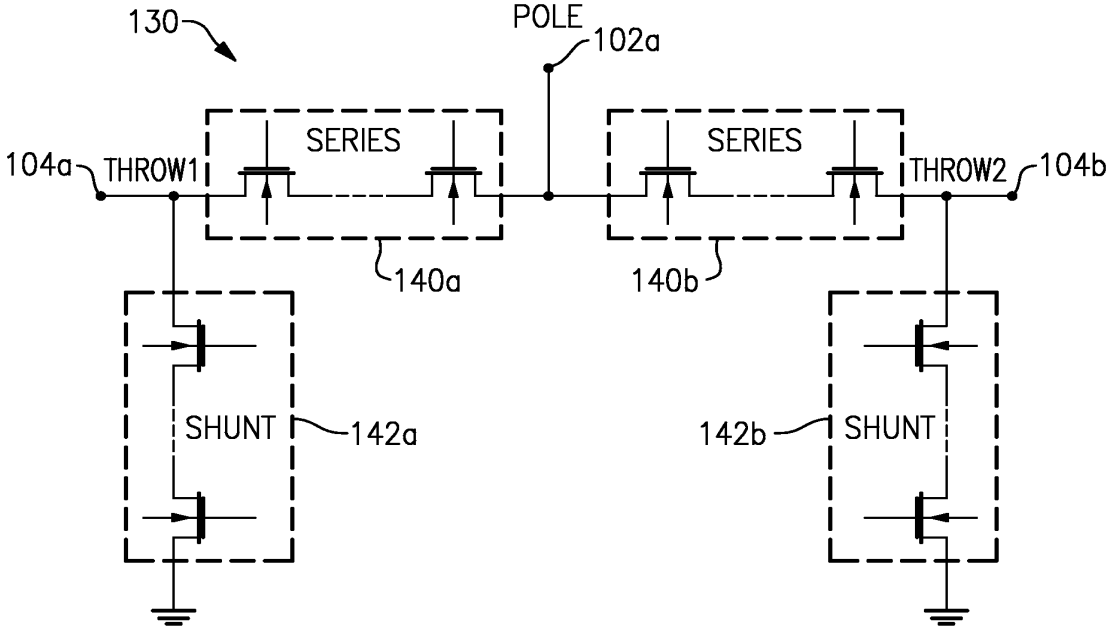
130
POLE
102a
SERIES
SERIES
104a
THROW1
THROW2
104b
140a
140b
SHUNT
142a
142b
SHUNT

FIG.4

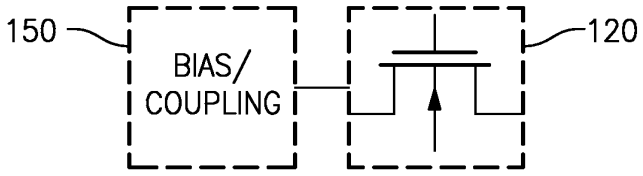
150
BIAS/
COUPLING
120

FIG.5

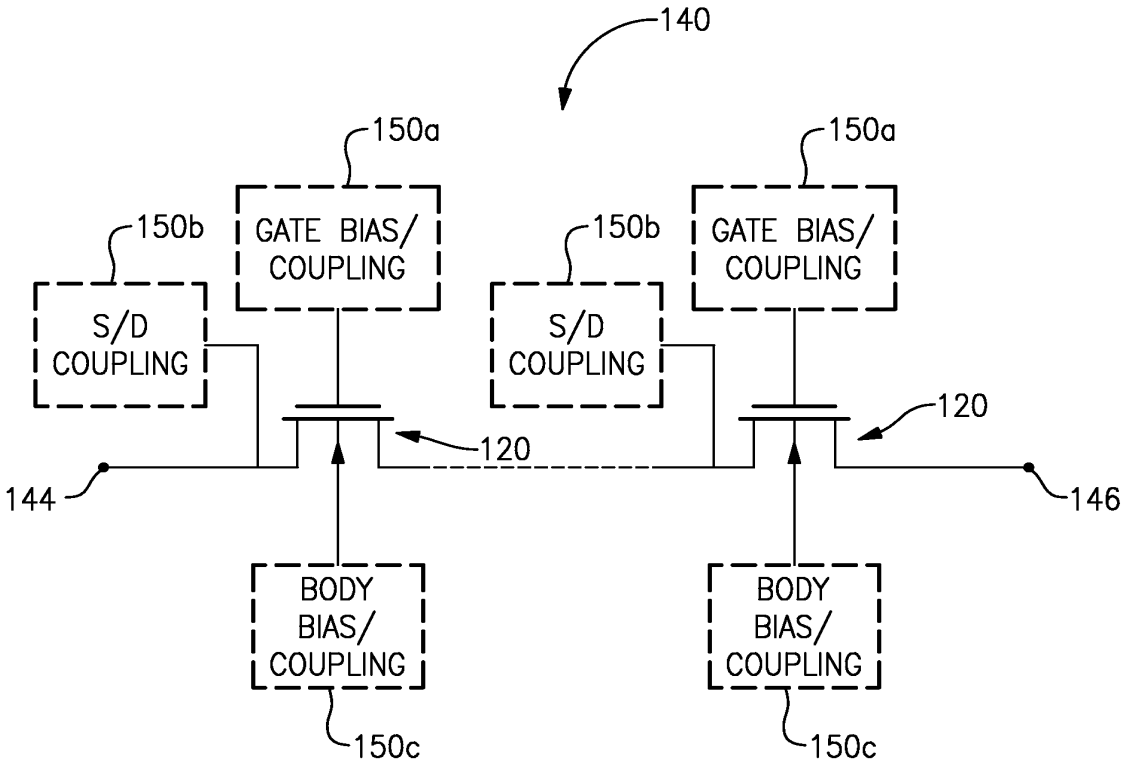
140
150a
150a
150b
GATE BIAS/
COUPLING
150b
GATE BIAS/
COUPLING
S/D
COUPLING
S/D
COUPLING
120
120
144
146
BODY
BIAS/
COUPLING
BODY
BIAS/
COUPLING
150c
150c

FIG.6

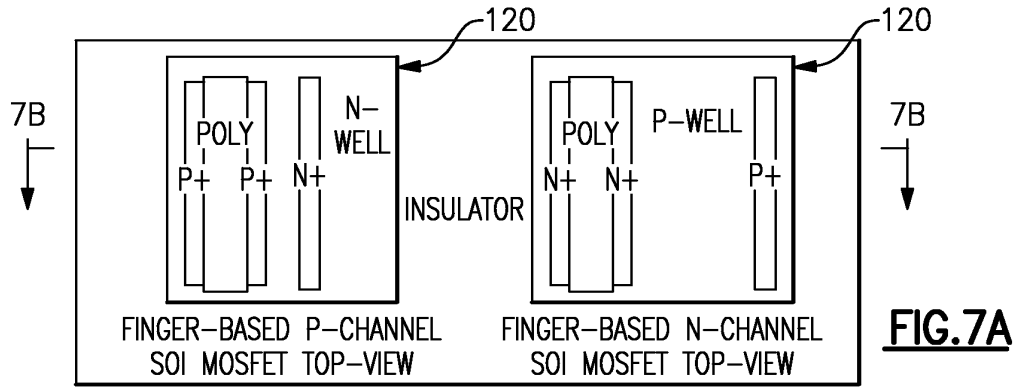

FIG.7A

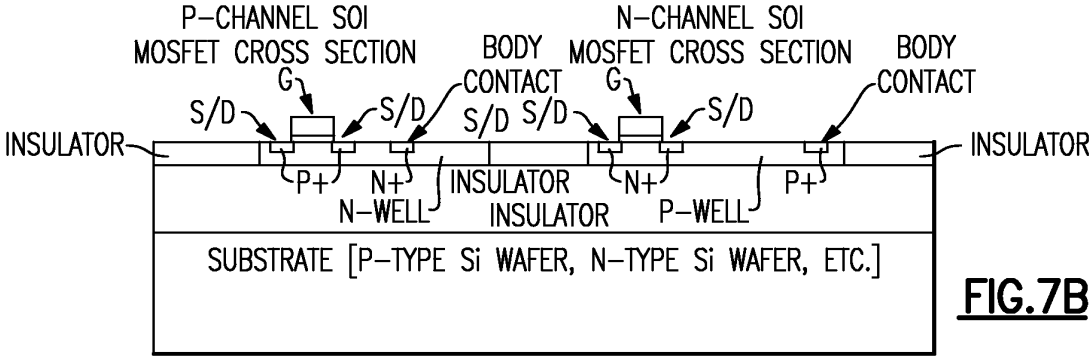

FIG.7B

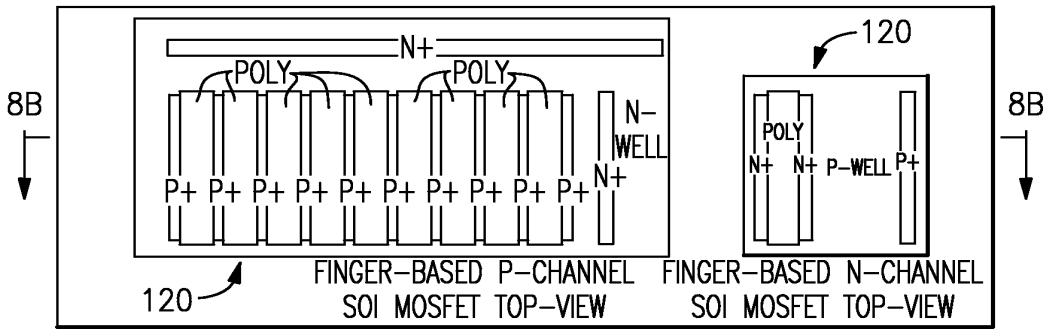

FIG.8A

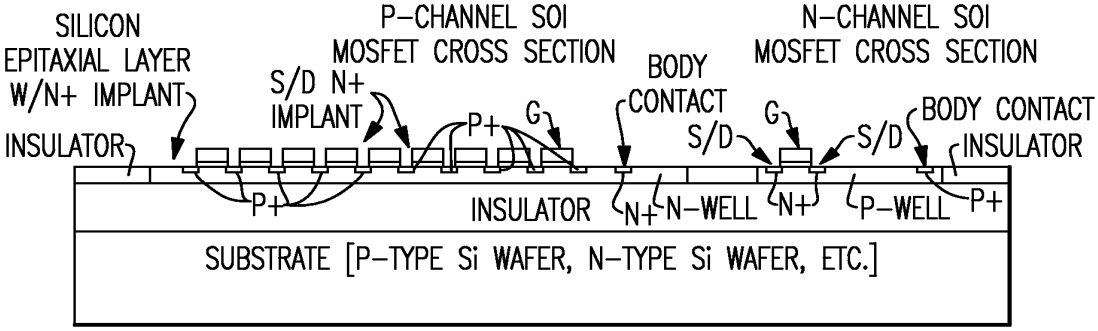

FIG.8B

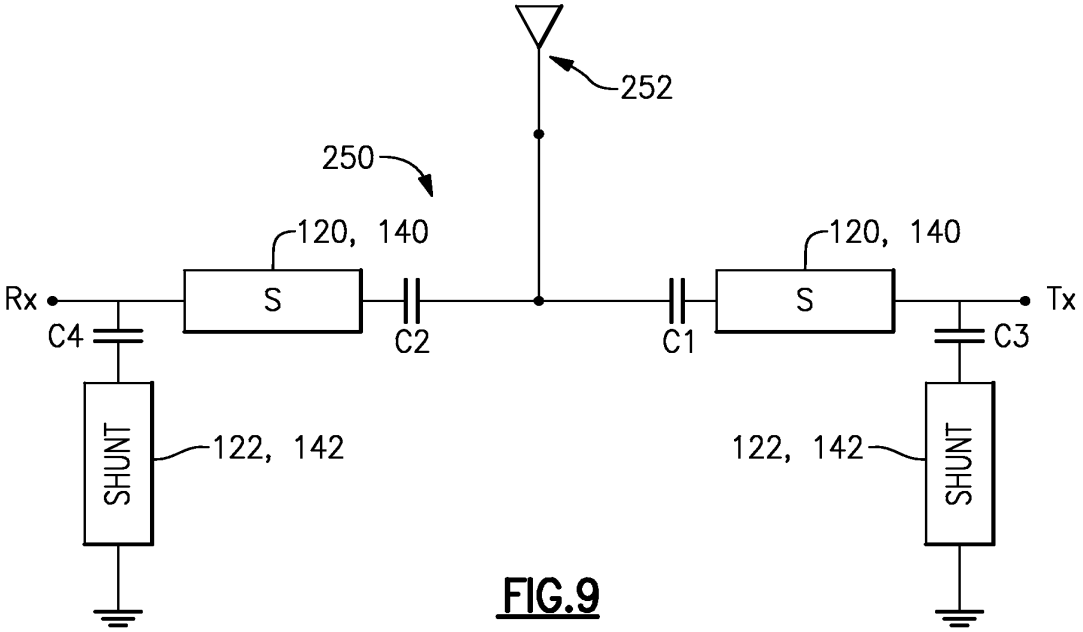
252
250
120, 140
120, 140
Rx
S
S
Tx
C4
C2
C1
C3
SHUNT
122, 142
122, 142
SHUNT

FIG.9

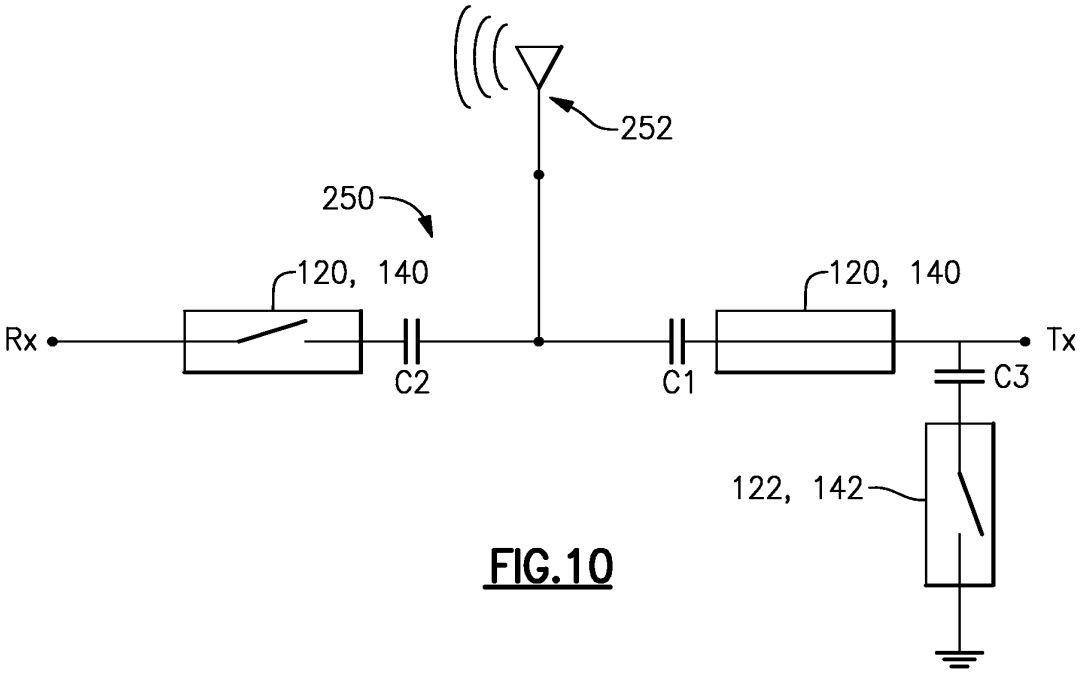
252
250
120, 140
120, 140
Rx
Tx
C2
C1
C3
122, 142

FIG.10

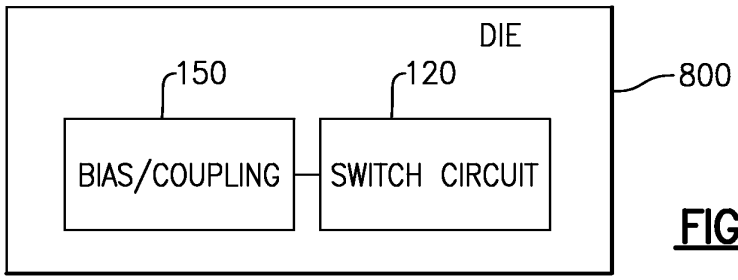

FIG.11A

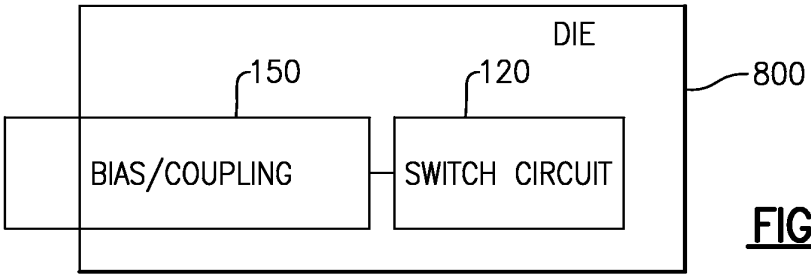

FIG.11B

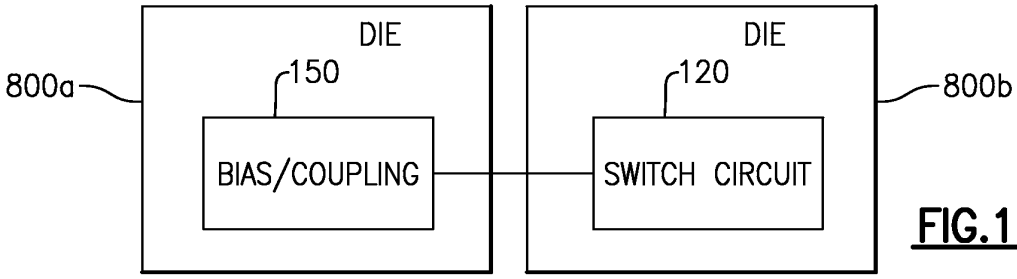

FIG.11C

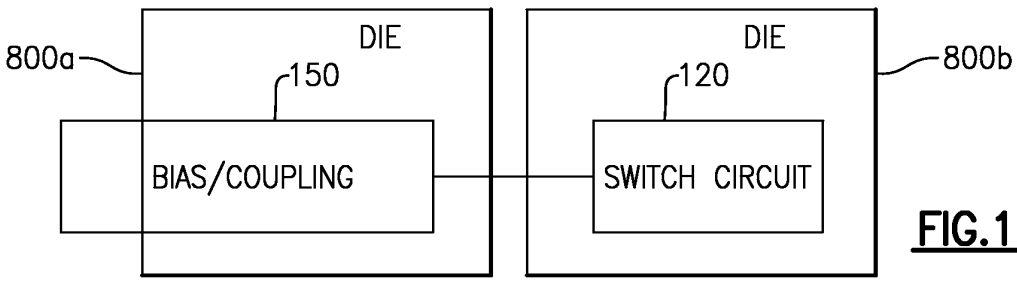

FIG.11D

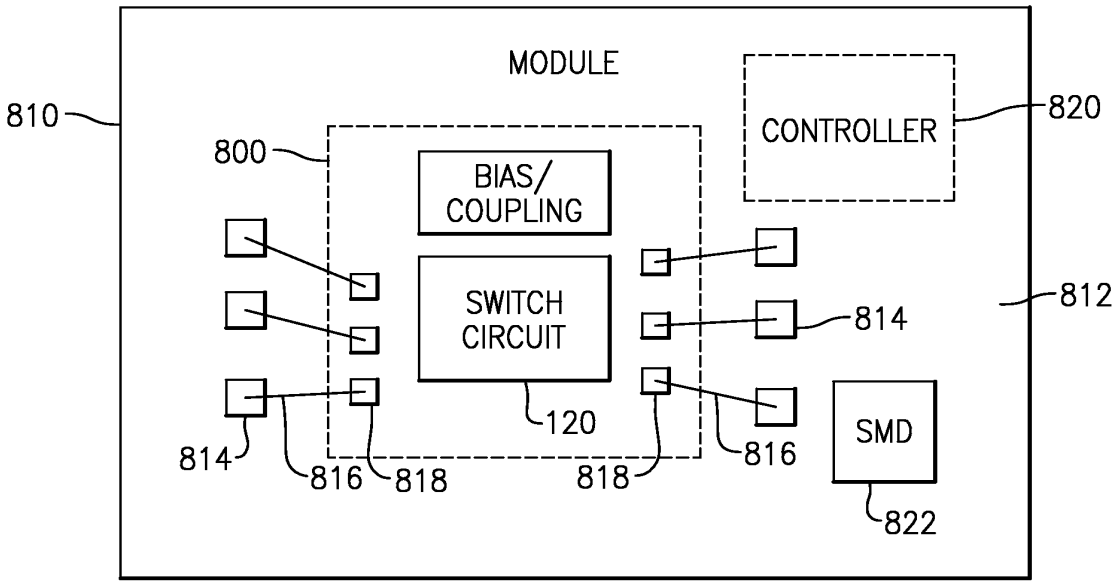

FIG.12A

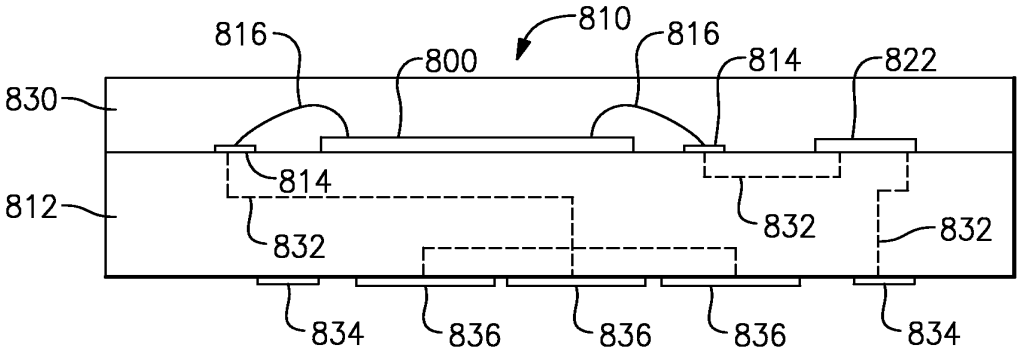

FIG.12B

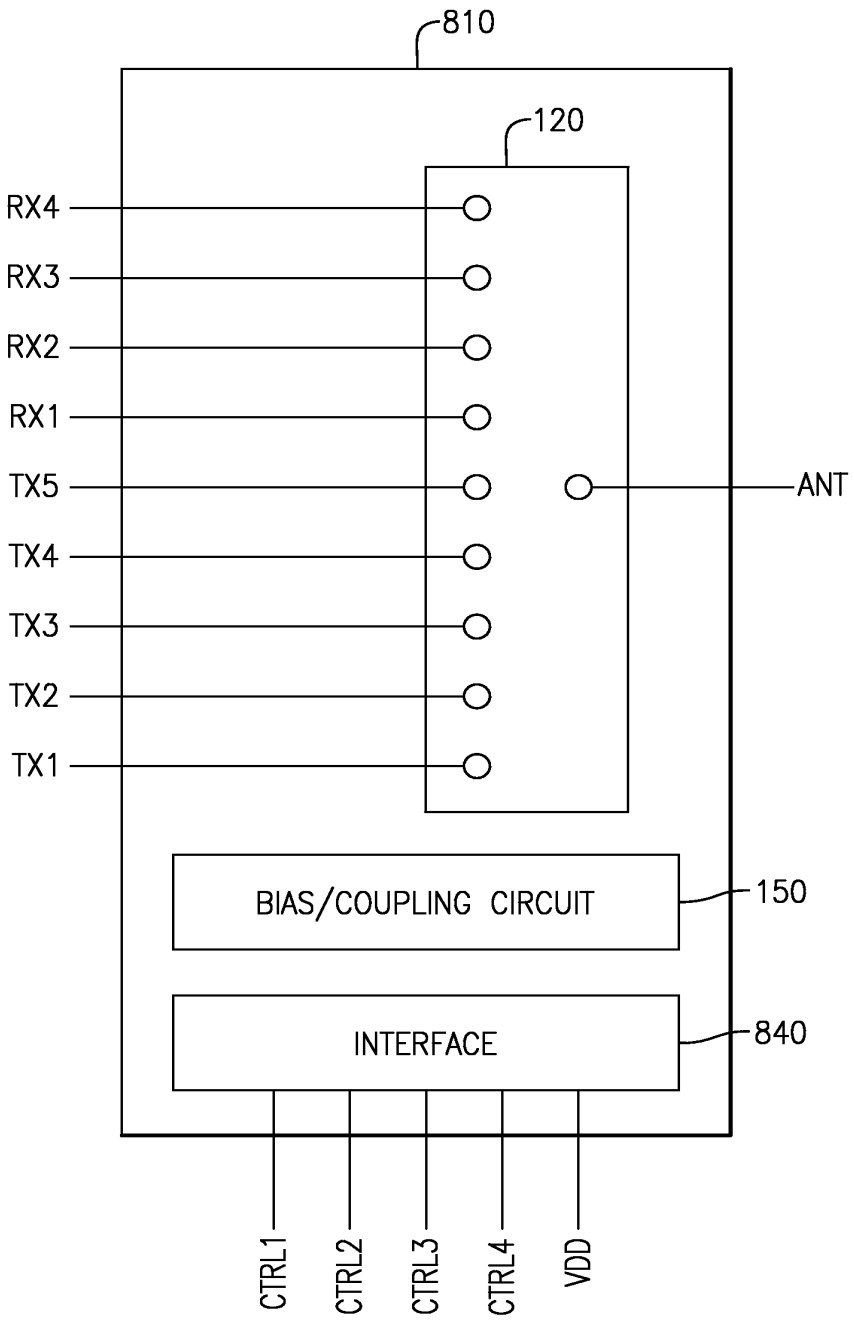
810
120
RX4
RX3
RX2
RX1
TX5
TX4
TX3
TX2
TX1
ANT
BIAS/COUPLING CIRCUIT
150
INTERFACE
840
CTRL1
CTRL2
CTRL3
CTRL4
VDD

FIG.13

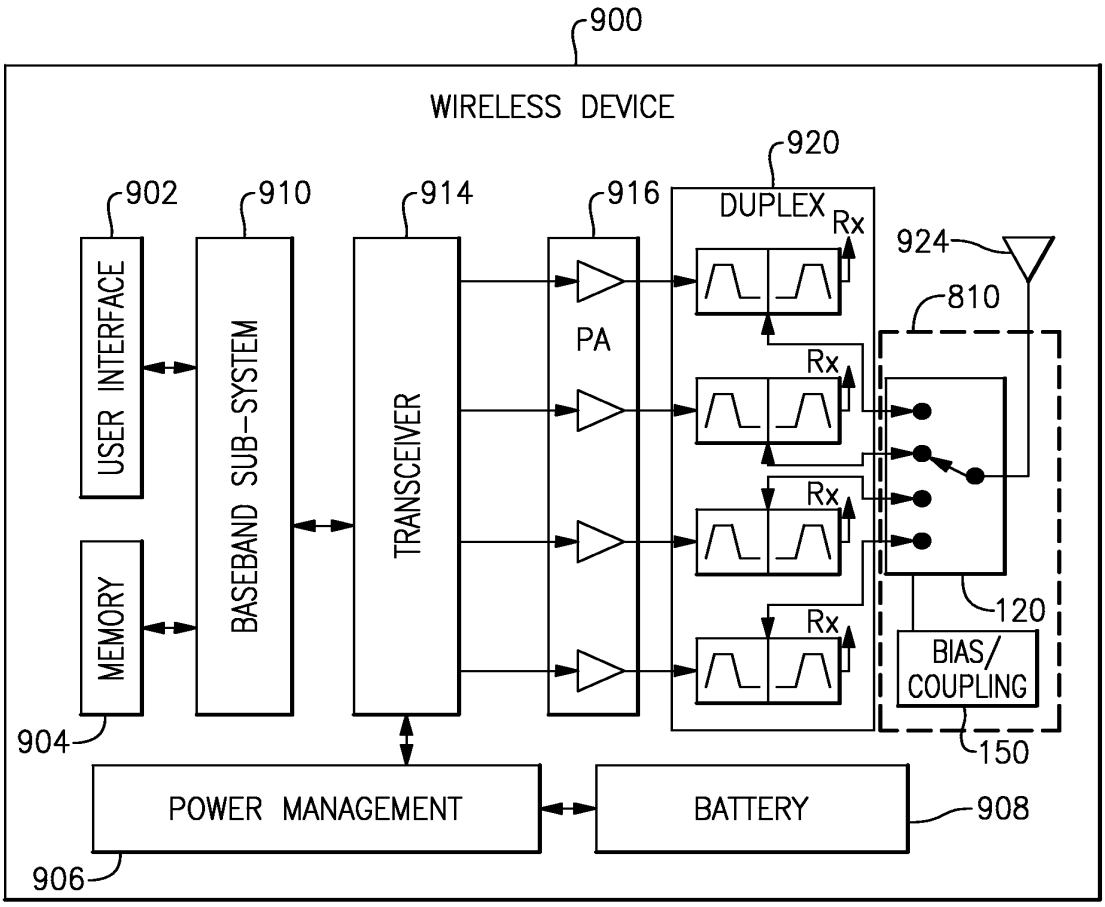
900
WIRELESS DEVICE
920
902
910
914
916
DUPLEX
Rx
924
USER INTERFACE
BASEBAND SUB-SYSTEM
TRANSCEIVER
PA
810
Rx
Rx
Rx
MEMORY
120
BIAS/
COUPLING
904
150
POWER MANAGEMENT
BATTERY
908
906

FIG.14

RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION

RELATED APPLICATION

[0001] This application is a divisional of U.S. Patent Application No. 13/936,175, filed on July 6, 2013, titled "Radio-Frequency Switch System Having Improved Intermodulation Distortion Performance," which claims priority to U.S. Provisional Application No. 61/669,045, filed on July 7, 2012, and entitled "Radio-Frequency Switch System Having Improved Intermodulation Distortion Performance," the disclosures of which are hereby incorporated by reference in its entirety.

BACKGROUND

Field

[0002] The present disclosure generally relates to the field of electronics, and more particularly, to radio-frequency switches.

Description of Related Art

[0003] Radio-frequency (RF) switches, such as transistor switches, can be used to switch signals between one or more poles and one or more throws. Transistor switches, or portions thereof, can be controlled through transistor biasing and/or coupling. Design and use of bias and/or coupling circuits in connection with RF switches can affect switching performance.

SUMMARY

[0004] In some implementations, the present disclosure relates to a radio-frequency (RF) switch system that includes a switch having a stack of field-effect transistors (FETs) connected in series between first and second nodes. The system further includes a capacitor connected in series with the switch and configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

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[0005] In some embodiments, the FETs can be silicon-on-insulator (SOI) FETs. In some embodiments, the first node can be an antenna node. The capacitor can be disposed between the switch and the antenna node. The switch can be part of a transmit path such that the second node of the switch is an input node for an amplified RF signal. The switch can be part of a receive path such that the second node of the switch is an output node for an RF signal received from the antenna.

[0006] According to some implementations, the present disclosure relates to a semiconductor die having a semiconductor substrate and a switch formed on the semiconductor substrate and having a stack of field-effect transistors (FETs) connected in series. The die further includes a capacitor formed on the semiconductor substrate and connected in series with the switch. The capacitor is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

[0007] In some embodiments, the die can further include an insulator layer disposed between the FETs and the semiconductor substrate. The die can be a silicon-on-insulator (SOI) die.

[0008] In a number of implementations, the present disclosure relates to a method for fabricating a semiconductor die. The method includes providing a semiconductor substrate and forming a stack of field-effect transistors (FETs) on the semiconductor substrate so as to be connected in series. The method further includes forming a capacitor on the semiconductor substrate so as to be connected in series with an end of the stack. The capacitor is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the stack.

[0009] In some embodiments, the method can further include forming an insulator layer between the FETs and the semiconductor substrate.

[0010] In accordance with some implementations, the present disclosure relates to a radio-frequency (RF) switch module that includes a packaging substrate configured to receive a plurality of components. The module further includes a semiconductor die mounted on the packaging

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substrate. The die includes a switch having a stack of field-effect transistors (FETs) connected in series. The module further includes a capacitor connected in series with the switch. The capacitor is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

[0011] In some embodiments, the semiconductor die can be a silicon-on-insulator (SOI) die. In some embodiments, the capacitor can be part of the same semiconductor die as the FETs. In some embodiments, the capacitor can be part of a second die mounted on the packaging substrate. In some embodiments, the capacitor circuit can be disposed at a location outside of the semiconductor die.

[0012] In an number of implementations, the present disclosure relates to a wireless device that includes a transceiver configured to process RF signals. The wireless device further includes an antenna in communication with the transceiver. The wireless device further includes a switch module interconnected to the antenna and the transceiver and configured to selectively route RF signals to and from the antenna. The switch module includes a switch having a stack of field-effect transistors (FETs) connected in series. The switch module further includes a capacitor connected in series with the switch. The capacitor is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Various embodiments are depicted in the accompanying drawings for illustrative purposes, and should in no way be interpreted as limiting the scope of the inventions. In addition, various features of different disclosed embodiments can be combined to form additional embodiments, which are part of this disclosure. Throughout the drawings, reference numbers may be reused to indicate correspondence between reference elements.

[0014] Figure 1 schematically shows a radio-frequency (RF) switch configured to switch one or more signals between one or more poles and one or more throws.

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[0015] Figure 2 shows that the RF switch 100 of Figure 1 can include an RF core and an energy management (EM) core.

[0016] Figure 3 shows an example of the RF core implemented in an single-pole-double-throw (SPDT) configuration.

[0017] Figure 4 shows an example of the RF core implemented in an SPDT configuration where each switch arm can include a plurality of field-effect transistors (FETs) connected in series.

[0018] Figure 5 schematically shows that controlling of one or more FETs in an RF switch can be facilitated by a circuit configured to bias and/or couple one or more portions of the FETs.

[0019] Figure 6 shows examples of the bias/coupling circuit implemented on different parts of a plurality of FETs in a switch arm.

[0020] Figures 7A and 7B show plan and side sectional views of an example finger-based FET device implemented in a silicon-on-insulator (SOI) configuration.

[0021] Figures 8A and 8B show plan and side sectional views of an example of a multiple-finger FET device implemented in an SOI configuration.

[0022] Figure 9 shows an example where an RF switching configuration can include one or more capacitors to, for example, inhibit a low-frequency blocker from mixing with a fundamental frequency.

[0023] Figure 10 shows an example where the switching configuration of Figure 9 is in a transmit mode.

[0024] Figures 11A-11D show examples of how various components for biasing, coupling, and/or facilitating the example configurations of Figures 9-10 can be implemented.

[0025] Figures 12A and 12B show an example of a packaged module that can include one or more features described herein.

[0026] Figure 13 shows that in some embodiments, one or more features of the present disclosure can be implemented in a switch device such as a single-pole-multi-throw (SPMT) switch configured to facilitate multi-band multi-mode wireless operation.

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[0027] Figure 14 shows an example of a wireless device that can include one or more features described herein.

DETAILED DESCRIPTION

[0028] The headings provided herein, if any, are for convenience only and do not necessarily affect the scope or meaning of the claimed invention.

Example Components of a Switching Device:

[0029] Figure 1 schematically shows a radio-frequency (RF) switch 100 configured to switch one or more signals between one or more poles 102 and one or more throws 104. In some embodiments, such a switch can be based on one or more field-effect transistors (FETs) such as silicon-on-insulator (SOI) FETs. When a particular pole is connected to a particular throw, such a path is commonly referred to as being closed or in an ON state. When a given path between a pole and a throw is not connected, such a path is commonly referred to as being open or in an OFF state.

[0030] Figure 2 shows that in some implementations, the RF switch 100 of Figure 1 can include an RF core 110 and an energy management (EM) core 112. The RF core 110 can be configured to route RF signals between the first and second ports. In the example single-pole-double-throw (SPDT) configuration shown in Figure 2, such first and second ports can include a pole 102a and a first throw 104a, or the pole 102a and a second throw 104b.

[0031] In some embodiments, EM core 112 can be configured to supply, for example, voltage control signals to the RF core. The EM core 112 can be further configured to provide the RF switch 100 with logic decoding and/or power supply conditioning capabilities.

[0032] In some embodiments, the RF core 110 can include one or more poles and one or more throws to enable passage of RF signals between one or more inputs and one or more outputs of the switch 100. For example, the RF core 110 can include a single-pole double-throw (SPDT or SP2T) configuration as shown in Figure 2.

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[0033] In the example SPDT context, Figure 3 shows a more detailed example configuration of an RF core 110. The RF core 110 is shown to include a single pole 102a coupled to first and second throw nodes 104a, 104b via first and second transistors (e.g., FETs) 120a, 120b. The first throw node 104a is shown to be coupled to an RF ground via an FET 122a to provide shunting capability for the node 104a. Similarly, the second throw node 104b is shown to be coupled to the RF ground via an FET 122b to provide shunting capability for the node 104b.

[0034] In an example operation, when the RF core 110 is in a state where an RF signal is being passed between the pole 102a and the first throw 104a, the FET 120a between the pole 102a and the first throw node 104a can be in an ON state, and the FET 120b between the pole 102a and the second throw node 104b can be in an OFF state. For the shunt FETs 122a, 122b, the shunt FET 122a can be in an OFF state so that the RF signal is not shunted to ground as it travels from the pole 102a to the first throw node 104a. The shunt FET 122b associated with the second throw node 104b can be in an ON state so that any RF signals or noise arriving at the RF core 110 through the second throw node 104b is shunted to the ground so as to reduce undesirable interference effects to the pole-to-first-throw operation.

[0035] Although the foregoing example is described in the context of a single-pole-double-throw configuration, it will be understood that the RF core can be configured with other numbers of poles and throws. For example, there may be more than one poles, and the number of throws can be less than or greater than the example number of two.

[0036] In the example of Figure 3, the transistors between the pole 102a and the two throw nodes 104a, 104b are depicted as single transistors. In some implementations, such switching functionalities between the pole(s) and the throw(s) can be provided by switch arm segments, where each switch arm segment includes a plurality of transistors such as FETs.

[0037] An example RF core configuration 130 of an RF core having such switch arm segments is shown in Figure 4. In the example, the pole 102a and the first throw node 104a are shown to be coupled via a first switch arm

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segment 140a. Similarly, the pole 102a and the second throw node 104b are shown to be coupled via a second switch arm segment 140b. The first throw node 104a is shown to be capable of being shunted to an RF ground via a first shunt arm segment 142a. Similarly, the second throw node 104b is shown to be capable of being shunted to the RF ground via a second shunt arm segment 142b.

[0038] In an example operation, when the RF core 130 is in a state where an RF signal is being passed between the pole 102a and the first throw node 104a, all of the FETs in the first switch arm segment 140a can be in an ON state, and all of the FETs in the second switch arm segment 104b can be in an OFF state. The first shunt arm 142a for the first throw node 104a can have all of its FETs in an OFF state so that the RF signal is not shunted to ground as it travels from the pole 102a to the first throw node 104a. All of the FETs in the second shunt arm 142b associated with the second throw node 104b can be in an ON state so that any RF signals or noise arriving at the RF core 130 through the second throw node 104b is shunted to the ground so as to reduce undesirable interference effects to the pole-to-first-throw operation.

[0039] Again, although described in the context of an SP2T configuration, it will be understood that RF cores having other numbers of poles and throws can also be implemented.

[0040] In some implementations, a switch arm segment (e.g., 140a, 140b, 142a, 142b) can include one or more semiconductor transistors such as FETs. In some embodiments, an FET may be capable of being in a first state or a second state and can include a gate, a drain, a source, and a body (sometimes also referred to as a substrate. In some embodiments, an FET can include a metal-oxide-semiconductor field effect transistor (MOSFET). In some embodiments, one or more FETs can be connected in series forming a first end and a second end such that an RF signal can be routed between the first end and the second end when the FETs are in a first state (e.g., ON state).

[0041] At least some of the present disclosure relates to how an FET or a group of FETs can be controlled to provide switching functionalities in desirable

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manners. Figure 5 schematically shows that in some implementations, such controlling of an FET 120 can be facilitated by a circuit 150 configured to bias and/or couple one or more portions of the FET 120. In some embodiments, such a circuit 150 can include one or more circuits configured to bias and/or couple a gate of the FET 120, bias and/or couple a body of the FET 120, and/or couple a source/drain of the FET 120.

[0042] Schematic examples of how such biasing and/or coupling of different parts of one or more FETs are described in reference to Figure 6. In Figure 6, a switch arm segment 140 (that can be, for example, one of the example switch arm segments 140a, 140b, 142a, 142b of the example of Figure 4) between nodes 144, 146 is shown to include a plurality of FETs 120. Operations of such FETs can be controlled and/or facilitated by a gate bias/coupling circuit 150a, and a body bias/coupling circuit 150c, and/or a source/drain coupling circuit 150b.

Gate Bias/Coupling Circuit

[0043] In the example shown in Figure 6, the gate of each of the FETs 120 can be connected to the gate bias/coupling circuit 150a to receive a gate bias signal and/or couple the gate to another part of the FET 120 or the switch arm 140. In some implementations, designs or features of the gate bias/coupling circuit 150a can improve performance of the switch arm 140. Such improvements in performance can include, but are not limited to, device insertion loss, isolation performance, power handling capability and/or switching device linearity.

Body Bias/Coupling Circuit

[0044] As shown in Figure 6, the body of each FET 120 can be connected to the body bias/coupling circuit 150c to receive a body bias signal and/or couple the body to another part of the FET 120 or the switch arm 140. In some implementations, designs or features of the body bias/coupling circuit 150c can improve performance of the switch arm 140. Such improvements in performance can include, but are not limited to, device insertion loss, isolation performance, power handling capability and/or switching device linearity.

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Source/Drain Coupling Circuit

[0045] As shown in Figure 6, the source/drain of each FET 120 can be connected to the coupling circuit 150b to couple the source/drain to another part of the FET 120 or the switch arm 140. In some implementations, designs or features of the coupling circuit 150b can improve performance of the switch arm 140. Such improvements in performance can include, but are not limited to, device insertion loss, isolation performance, power handling capability and/or switching device linearity.

Examples of Switching Performance Parameters:

Insertion Loss

[0046] A switching device performance parameter can include a measure of insertion loss. A switching device insertion loss can be a measure of the attenuation of an RF signal that is routed through the RF switching device. For example, the magnitude of an RF signal at an output port of a switching device can be less than the magnitude of the RF signal at an input port of the switching device. In some embodiments, a switching device can include device components that introduce parasitic capacitance, inductance, resistance, or conductance into the device, contributing to increased switching device insertion loss. In some embodiments, a switching device insertion loss can be measured as a ratio of the power or voltage of an RF signal at an input port to the power or voltage of the RF signal at an output port of the switching device. Decreased switching device insertion loss can be desirable to enable improved RF signal transmission.

Isolation

[0047] A switching device performance parameter can also include a measure of isolation. Switching device isolation can be a measure of the RF isolation between an input port and an output port an RF switching device. In some embodiments, it can be a measure of the RF isolation of a switching device while the switching device is in a state where an input port and an output port are electrically isolated, for example while the switching device is in an OFF state.

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Increased switching device isolation can improve RF signal integrity. In certain embodiments, an increase in isolation can improve wireless communication device performance.

Intermodulation Distortion

[0048] A switching device performance parameter can further include a measure of intermodulation distortion (IMD) performance. Intermodulation distortion (IMD) can be a measure of non-linearity in an RF switching device.

[0049] IMD can result from two or more signals mixing together and yielding frequencies that are not harmonic frequencies. For example, suppose that two signals have fundamental frequencies f_1 and f_2 ($f_2 > f_1$) that are relatively close to each other in frequency space. Mixing of such signals can result in peaks in frequency spectrum at frequencies corresponding to different products of fundamental and harmonic frequencies of the two signals. For example, a second-order intermodulation distortion (also referred to as IMD2) is typically considered to include frequencies f_1+f_2 f_2-f_1, $2f_1$, and $2f_2$. A third-order IMD (also referred to as IMD3) is typically considered to include $2f_1+f_2$, $2f_1-f_2$, f_1+2f_2, f_1-2f_2. Higher order products can be formed in similar manners.

[0050] In general, as the IMD order number increases, power levels decrease. Accordingly, second and third orders can be undesirable effects that are of particular interest. Higher orders such as fourth and fifth orders can also be of interest in some situations.

[0051] In some RF applications, it can be desirable to reduce susceptibility to interference within an RF system. Non linearity in RF systems can result in introduction of spurious signals into the system. Spurious signals in the RF system can result in interference within the system and degrade the information transmitted by RF signals. An RF system having increased non-linearity can demonstrate increased susceptibility to interference. Non-linearity in system components, for example switching devices, can contribute to the introduction of spurious signals into the RF system, thereby contributing to degradation of overall RF system linearity and IMD performance.

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[0052] In some embodiments, RF switching devices can be implemented as part of an RF system including a wireless communication system. IMD performance of the system can be improved by increasing linearity of system components, such as linearity of an RF switching device. In some embodiments, a wireless communication system can operate in a multi-band and/or multi-mode environment. Improvement in intermodulation distortion (IMD) performance can be desirable in wireless communication systems operating in a multi-band and/or multi-mode environment. In some embodiments, improvement of a switching device IMD performance can improve the IMD performance of a wireless communication system operating in a multi-mode and/or multi-band environment.

[0053] Improved switching device IMD performance can be desirable for wireless communication devices operating in various wireless communication standards, for example for wireless communication devices operating in the LTE communication standard. In some RF applications, it can be desirable to improve linearity of switching devices operating in wireless communication devices that enable simultaneous transmission of data and voice communication. For example, improved IMD performance in switching devices can be desirable for wireless communication devices operating in the LTE communication standard and performing simultaneous transmission of voice and data communication (e.g., SVLTE).

High Power Handling Capability

[0054] In some RF applications, it can be desirable for RF switching devices to operate under high power while reducing degradation of other device performance parameters. In some embodiments, it can be desirable for RF switching devices to operate under high power with improved intermodulation distortion, insertion loss, and/or isolation performance.

[0055] In some embodiments, an increased number of transistors can be implemented in a switch arm segment of a switching device to enable improved power handling capability of the switching device. For example, a switch arm segment can include an increased number of FETs connected in

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series, an increased FET stack height, to enable improved device performance under high power. However, in some embodiments, increased FET stack height can degrade the switching device insertion loss performance.

Examples of FET Structures and Fabrication Process Technologies:

[0056] A switching device can be implemented on-die, off-die, or some combination thereon. A switching device can also be fabricated using various technologies. In some embodiments, RF switching devices can be fabricated with silicon or silicon-on-insulator (SOI) technology.

[0057] As described herein, an RF switching device can be implemented using silicon-on-insulator (SOI) technology. In some embodiments, SOI technology can include a semiconductor substrate having an embedded layer of electrically insulating material, such as a buried oxide layer beneath a silicon device layer. For example, an SOI substrate can include an oxide layer embedded below a silicon layer. Other insulating materials known in the art can also be used.

[0058] Implementation of RF applications, such as an RF switching device, using SOI technology can improve switching device performance. In some embodiments, SOI technology can enable reduced power consumption. Reduced power consumption can be desirable in RF applications, including those associated with wireless communication devices. SOI technology can enable reduced power consumption of device circuitry due to decreased parasitic capacitance of transistors and interconnect metallization to a silicon substrate. Presence of a buried oxide layer can also reduce junction capacitance or use of high resistivity substrate, enabling reduced substrate related RF losses. Electrically isolated SOI transistors can facilitate stacking, contributing to decreased chip size.

[0059] In some SOI FET configurations, each transistor can be configured as a finger-based device where the source and drain are rectangular shaped (in a plan view) and a gate structure extends between the source and drain like a rectangular shaped finger. Figures 7A and 7B show plan and side sectional views of an example finger-based FET device implemented on SOI. As

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shown, FET devices described herein can include a p-type FET or an n-type FET. Thus, although some FET devices are described herein as p-type devices, it will be understood that various concepts associated with such p-type devices can also apply to n-type devices.

[0060] As shown in Figures 7A and 7B, a pMOSFET can include an insulator layer formed on a semiconductor substrate. The insulator layer can be formed from materials such as silicon dioxide or sapphire. An n-well is shown to be formed in the insulator such that the exposed surface generally defines a rectangular region. Source (S) and drain (D) are shown to be p-doped regions whose exposed surfaces generally define rectangles. As shown, S/D regions can be configured so that source and drain functionalities are reversed.

[0061] Figures 7A and 7B further show that a gate (G) can be formed on the n-well so as to be positioned between the source and the drain. The example gate is depicted as having a rectangular shape that extends along with the source and the drain. Also shown is an n-type body contact. Formations of the rectangular shaped well, source and drain regions, and the body contact can be achieved by a number of known techniques. In some embodiments, the source and drain regions can be formed adjacent to the ends of their respective upper insulator layers, and the junctions between the body and the source/drain regions on the opposing sides of the body can extend substantially all the way down to the top of the buried insulator layer. Such a configuration can provide, for example, reduced source/drain junction capacitance. To form a body contact for such a configuration, an additional gate region can be provided on the side so as to allow, for example, an isolated P+ region to contact the Pwell.

[0062] Figures 8A and 8B show plan and side sectional views of an example of a multiple-finger FET device implemented on SOI. Formations of rectangular shaped n-well, rectangular shaped p-doped regions, rectangular shaped gates, and n-type body contact can be achieved in manners similar to those described in reference to Figures 7A and 7B.

[0063] The example multiple-finger FET device of Figures 8A and 8B can be made to operate such that a drain of one FET acts as a source of its

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neighboring FET. Thus, the multiple-finger FET device as a whole can provide a voltage-dividing functionality. For example, an RF signal can be provided at one of the outermost p-doped regions (e.g., the leftmost p-doped region); and as the signal passes through the series of FETs, the signal's voltage can be divided among the FETs. In such an example, the rightmost p-doped region can act as an overall drain of the multi-finger FET device.

[0064] In some implementations, a plurality of the foregoing multi-finger FET devices can be connected in series as a switch to, for example, further facilitate the voltage-dividing functionality. A number of such multi-finger FET devices can be selected based on, for example, power handling requirement of the switch.

Examples of Bias and/or Coupling Configurations for Improved Performance:

[0065] Described herein are various examples of how FET-based switch circuits can be biased and/or coupled to yield one or more performance improvements. In some embodiments, such biasing/coupling configurations can be implemented in SOI FET-based switch circuits. It will be understood that some of the example biasing/coupling configurations can be combined to yield a combination of desirable features that may not be available to the individual configurations. It will also be understood that, although described in the context of RF switching applications, one or more features described herein can also be applied to other circuits and devices that utilize FETs such as SOI FETs.

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Example Configurations

[0066] Intermodulation distortion (IMD) measures an unwanted signal added to a desired signal due to mixing products from other RF signals. Such an effect can be particularly dominant in a multi-mode, multi-band environment. IMD can the result from two or more signals mixing together to yield frequencies that are not harmonic frequencies.

[0067] System designers typically strive to reduce interference susceptibility through, for example, improved linearity. A given system's linearity can govern how much IMD will occur within it, which in turn can create interferences. Through improved linearity of the system building blocks, such as an RF switch, the overall susceptibility of a system to interference can be decreased.

[0068] Performance features such as a lower IMD in RF switches can be an important factor in wireless-device designs. For example Long Term Evolution (LTE) systems can benefit significantly from RF switches having reduced IMDs. As a more specific example, system designs for simultaneous voice and data on LTE (SVLTE) can benefit significantly from RF switches having ultra-low levels of IMDs.

[0069] Figure 9 shows a switching configuration 250 in an example context of a single-pole-dual-throw (SPDT) application. The single pole is shown to be connected to an antenna 252. One of the two throws is shown to be coupled to a receive (Rx) port via a switch circuit S. The Rx port can be coupled to a ground via a shunt switch circuit.

[0070] Similarly, the other throw is shown to be coupled to a transmit (Tx) port via a switch circuit S. The Tx port can be coupled to the ground via a shunt switch circuit.

[0071] In some embodiments, each of the switch circuits ("S" and "Shunt") can include one or more FETs such as SOI FETs. A single FET is sometimes referred to herein with a reference numeral 120 or 122, and a stack of such FETs is sometimes referred to herein with a reference numeral 140 or 142.

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In some embodiments, the "S" and "Shunt" switches can include one or more features described herein to provide various advantageous functionalities.

[0072] The switching configuration of Figure 9 is shown to include capacitors to inhibit a low-frequency blocker from mixing with a fundamental frequency. For example, a capacitor C1 is provided between the antenna node and the switch arm S of the Tx throw. Similarly, a capacitor C2 is provided between the antenna node and the switch arm S of the Rx throw. For the shunt arms, a capacitor C3 is provided between the Tx node and its shunt switch arm. Similarly, a capacitor C4 is provided between the Rx node and its shunt switch arm. In some embodiments, a shunt arm may or may not be provided for the Rx node. With the foregoing capacitors, a low-frequency jammer signal can be blocked or reduced from mixing with any ON or OFF paths. This can lead to improvement in IMD performance, especially for low-frequency blocker signals.

[0073] Figure 10 shows an example operating configuration where some of the foregoing capacitors can provide desirable switching functionalities. In the example, the switching configuration is in a transmit mode. Accordingly, the transmit switch arm is ON (closed), and the receive switch arm is OFF (open). The shunt arm for the Tx node is OFF (open).

[0074] In some embodiments, capacitors C1-C4 described in reference to Figures 9 and 10 can be implemented on the same die as their respective switch circuits, off of the die, or any combination thereof.

[0075] In some implementations, and as described herein, the foregoing example configurations described in reference to Figures 9 and 10 can be relatively simpler and easier to implement, and can yield a number of improvements. For example, this technique can provide improved IMD performance by preventing a low-frequency blocker signal from mixing with a fundamental frequency signal.

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Examples of Implementations in Products:

[0076] Various examples of FET-based switch circuits and bias/coupling configurations described herein can be implemented in a number of different ways and at different product levels. Some of such product implementations are described by way of examples.

Semiconductor Die Implementation

[0077] Figures 11A-11D schematically show non-limiting examples of such implementations on one or more semiconductor die. Figure 11A shows that in some embodiments, a switch circuit 120 and a bias/coupling circuit 150 having one or more features as described herein can be implemented on a die 800. Figure 11B shows that in some embodiments, at least some of the bias/coupling circuit 150 can be implemented outside of the die 800 of Figure 11A.

[0078] Figure 11C shows that in some embodiments, a switch circuit 120 having one or more features as described herein can be implemented on a first die 800a, and a bias/coupling circuit 150 having one or more features as described herein can be implemented on a second die 800b. Figure 11D shows that in some embodiments, at least some of the bias/coupling circuit 150 can be implemented outside of the first die 800a of Figure 11C.

Packaged Module Implementation

[0079] In some embodiments, one or more die having one or more features described herein can be implemented in a packaged module. An example of such a module is shown in Figures 12A (plan view) and 12B (side view). Although described in the context of both of the switch circuit and the bias/coupling circuit being on the same die (e.g., example configuration of Figure 11A), it will be understood that packaged modules can be based on other configurations.

[0080] A module 810 is shown to include a packaging substrate 812. Such a packaging substrate can be configured to receive a plurality of components, and can include, for example, a laminate substrate. The

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components mounted on the packaging substrate 812 can include one or more dies. In the example shown, a die 800 having a switching circuit 120 and a bias/coupling circuit 150 is shown to be mounted on the packaging substrate 812. The die 800 can be electrically connected to other parts of the module (and with each other where more than one die is utilized) through connections such as connection-wirebonds 816. Such connection-wirebonds can be formed between contact pads 818 formed on the die 800 and contact pads 814 formed on the packaging substrate 812. In some embodiments, one or more surface mounted devices (SMDs) 822 can be mounted on the packaging substrate 812 to facilitate various functionalities of the module 810.

[0081] In some embodiments, the packaging substrate 812 can include electrical connection paths for interconnecting the various components with each other and/or with contact pads for external connections. For example, a connection path 832 is depicted as interconnecting the example SMD 822 and the die 800. In another example, a connection path 832 is depicted as interconnecting the SMD 822 with an external-connection contact pad 834. In yet another example a connection path 832 is depicted as interconnecting the die 800 with ground-connection contact pads 836.

[0082] In some embodiments, a space above the packaging substrate 812 and the various components mounted thereon can be filled with an overmold structure 830. Such an overmold structure can provide a number of desirable functionalities, including protection for the components and wirebonds from external elements, and easier handling of the packaged module 810.

[0083] Figure 13 shows a schematic diagram of an example switching configuration that can be implemented in the module 810 described in reference to Figures 12A and 12B. In the example, the switch circuit 120 is depicted as being an SP9T switch, with the pole being connectable to an antenna and the throws being connectable to various Rx and Tx paths. Such a configuration can facilitate, for example, multi-mode multi-band operations in wireless devices.

[0084] The module 810 can further include an interface for receiving power (e.g., supply voltage VDD) and control signals to facilitate operation of the

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switch circuit 120 and/or the bias/coupling circuit 150. In some implementations, supply voltage and control signals can be applied to the switch circuit 120 via the bias/coupling circuit 150.

Wireless Device Implementation

[0085] In some implementations, a device and/or a circuit having one or more features described herein can be included in an RF device such as a wireless device. Such a device and/or a circuit can be implemented directly in the wireless device, in a modular form as described herein, or in some combination thereof. In some embodiments, such a wireless device can include, for example, a cellular phone, a smart-phone, a hand-held wireless device with or without phone functionality, a wireless tablet, etc.

[0086] Figure 14 schematically depicts an example wireless device 900 having one or more advantageous features described herein. In the context of various switches and various biasing/coupling configurations as described herein, a switch 120 and a bias/coupling circuit 150 can be part of a module 810. In some embodiments, such a switch module can facilitate, for example, multi-band multip-mode operation of the wireless device 900.

[0087] In the example wireless device 900, a power amplifier (PA) module 916 having a plurality of PAs can provide an amplified RF signal to the switch 120 (via a duplexer 920), and the switch 120 can route the amplified RF signal to an antenna. The PA module 916 can receive an unamplified RF signal from a transceiver 914 that can be configured and operated in known manners. The transceiver can also be configured to process received signals. The transceiver 914 is shown to interact with a baseband sub-system 910 that is configured to provide conversion between data and/or voice signals suitable for a user and RF signals suitable for the transceiver 914. The transceiver 914 is also shown to be connected to a power management component 906 that is configured to manage power for the operation of the wireless device 900. Such a power management component can also control operations of the baseband sub-system 910 and the module 810.

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[0088] The baseband sub-system 910 is shown to be connected to a user interface 902 to facilitate various input and output of voice and/or data provided to and received from the user. The baseband sub-system 910 can also be connected to a memory 904 that is configured to store data and/or instructions to facilitate the operation of the wireless device, and/or to provide storage of information for the user.

[0089] In some embodiments, the duplexer 920 can allow transmit and receive operations to be performed simultaneously using a common antenna (e.g., 924). In Figure 14, received signals are shown to be routed to "Rx" paths (not shown) that can include, for example, a low-noise amplifier (LNA).

[0090] A number of other wireless device configurations can utilize one or more features described herein. For example, a wireless device does not need to be a multi-band device. In another example, a wireless device can include additional antennas such as diversity antenna, and additional connectivity features such as Wi-Fi, Bluetooth, and GPS.

General Comments:

[0091] Unless the context clearly requires otherwise, throughout the description and the claims, the words “comprise,” “comprising,” and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of “including, but not limited to.” The word “coupled”, as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words “herein,” “above,” “below,” and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word “or” in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

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[0092] The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative embodiments may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

[0093] The teachings of the invention provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

[0094] While certain embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

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WHAT IS CLAIMED IS:

1. A semiconductor die comprising:

a semiconductor substrate;

a switch formed on the semiconductor substrate and including a stack of field-effect transistors (FETs) connected in series; and

a capacitor formed on the semiconductor substrate and connected in series with the switch, the capacitor configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

2. The semiconductor die of claim 1 further comprising an insulator layer disposed between the stack of FETs and the semiconductor substrate.

3. The semiconductor die of claim 2 wherein the die is a silicon-on-insulator (SOI) die.

4. The semiconductor die of claim 1 wherein the stack of FETs includes silicon-on-insulator (SOI) FETs.

5. The semiconductor die of claim 1 wherein the capacitor is connected to an antenna node.

6. The semiconductor die of claim 5 wherein the capacitor is disposed between the switch and the antenna node.

7. The semiconductor die of claim 5 wherein the switch is part of a receive path, the switch being connected to an output node for an RF signal received from the antenna.

8. The semiconductor die of claim 1 wherein the switch is part of a transmit path, the switch being connected to an input node for an amplified RF signal.

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9. A method for operating a radio-frequency (RF) device, the method comprising:

controlling an RF switch including a plurality of field-effect transistors (FETs) connected in series between first and second nodes so that the FETs are collectively in an ON state or an OFF state; and

inhibiting a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch using a capacitor connected in series with the switch between the switch and the first node.

10. The method of claim 9 wherein the plurality of FETs is formed on an insulator layer disposed between the FETs and a semiconductor substrate.

11. The method of claim 9 wherein the switch is a silicon-on-insulator (SOI) switch.

12. The method of claim 9 wherein the first node is an antenna node.

13. The method of claim 9 wherein the switch is part of a receive path such that the second node of the switch is an output node for an RF signal received from the antenna.

14. The method of claim 9 wherein the switch is part of a transmit path such that the second node of the switch is an input node for an amplified RF signal.

15. A wireless device comprising:

a transceiver configured to process RF signals;

an antenna in communication with the transceiver; and

a switch module interconnected to the antenna and the transceiver and configured to selectively route RF signals to and from the antenna, the switch module including a switch including a stack of field-effect transistors (FETs) connected in series, the switch module further including a capacitor connected in series with the switch, the capacitor configured to

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inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

16. The wireless device of claim 15 wherein the switch is formed on a silicon-on-insulator (SOI) die of the wireless device.

17. The wireless device of claim 15 wherein the capacitor is part of the same semiconductor die as the stack of FETs.

18. The wireless device of claim 15 wherein the capacitor is disposed between the switch and the antenna.

19. The wireless device of claim 15 wherein the switch is part of a receive path, the switch being connected to an output node for an RF signal received from the antenna.

20. The wireless device of claim 15 wherein the switch is part of a transmit path, the switch being connected to an input node for an amplified RF signal.

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ABSTRACT

Radio-frequency (RF) devices are disclosed providing reduced intermodulation distortion. Disclosed RF and semiconductor devices can include a semiconductor substrate, a switch formed on the semiconductor substrate having a stack of field-effect transistors (FETs) connected in series, and a capacitor formed on the semiconductor substrate and connected in series with the switch, the capacitor configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Anuj Madan, et al.
App. No.	:	Not Assigned
Filed	:	On Even Date Herewith
Title	:	*RADIO FREQUENCY DEVICES HAVING REDUCED INTERMODULATION DISTORTION*
Examiner	:	Not Assigned
Art Unit	:	Not Assigned
Conf No.	:	Not Assigned

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The claims of the present application are different and possibly broader in scope than the claims pursued in the parent application(s). To the extent any prior amendments or characterizations of the scope of any claim or referenced art could be construed as a disclaimer of any subject matter supported by the present disclosure, the Applicant hereby rescinds and retracts such disclaimer. Accordingly, the references previously considered in the parent application(s) may need to be re-visited.

Respectfully submitted,
FERNANDO HALE & CHANG LLP

Dated: August 22, 2015

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	RADIO-FREQUENCY SWITCH SYSTEM HAVING IMPROVED INTERMODULATION DISTORTION PERFORMANCE

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☒ United States application or PCT international application number 13/936,175 filed on July 6, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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LEGAL NAME OF INVENTOR

Inventor: Anuj MADAN Date: 01/11/2014

Signature: [signature]

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	RADIO-FREQUENCY SWITCH SYSTEM HAVING IMPROVED INTERMODULATION DISTORTION PERFORMANCE

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 13/936,175 filed on July 6, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Fikret ALTUNKILIC Date: 01/02/2014

Signature: F. Altunkilic

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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LEGAL NAME OF INVENTOR

Inventor: Guillaume Alexandre BLIN Date: 3/14/14

Signature: G. Blin

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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