

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KANGXI COMMUNICATION TECHNOLOGIES (SHANGHAI) CO., LTD.
Petitioner,

v.

SKYWORKS SOLUTIONS, INC.
Patent Owner.

Case No. IPR2024-01457
U.S. Patent No. 9,148,194

PATENT OWNER'S RESPONSE

TABLE OF CONTENTS

	Page
I. INTRODUCTION	1
II. THE '194 PATENT (EX-1001)	3
A. Overview of the Patent	3
B. Challenged Claims	8
III. CLAIM CONSTRUCTION	9
IV. LEVEL OF ORDINARY SKILL IN THE ART	9
V. SCOPE AND CONTENT OF THE ASSERTED PRIOR ART	10
A. U.S. Pub No. 2011/0254614 to Huang (Ex-1005)	10
B. JP 2006-121217 to Seshimo (Ex-1006; Ex-1007 for translation).....	12
VI. PETITIONER FAILS TO SHOW THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE.....	14
A. The Challenged Claims Would Not Have Been Obvious Over Huang (Ground 1)	14
B. The Challenged Claims Would Not Have Been Obvious Over Seshimo (Ground 2)	44
VII. CONCLUSION.....	54

TABLE OF AUTHORITIES

	Page(s)
CASES	
<i>ActiveVideo Networks, Inc. v. Verizon Commc'ns., Inc.</i> , 694 F.3d 1312 (Fed. Cir. 2012)	42, 49, 52
<i>Comcast Cable Commc'ns, LLC v. Promptu Sys. Corp.</i> , 838 F. App'x 555 (Fed. Cir. 2021)	33
<i>Game & Tech. Co v. Activision Blizzard Inc.</i> , 926 F.3d 1370 (Fed. Cir. 2019)	33
<i>Graham v. John Deere Co.</i> , 383 U.S. 1 (1966).....	33
<i>In re Kotzab</i> , 217 F.3d 1365 (Fed. Cir. 2000)	15
<i>In re Magnum Oil Tools Int'l, Ltd.</i> , 829 F.3d 1364 (Fed. Cir. 2016)	14
<i>Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.</i> , 821 F.3d 1359 (Fed. Cir. 2016)	33
<i>Medtronic, Inc. v. Barry</i> , 891 F.3d 1368 (Fed. Cir. 2018)	16
<i>Qualcomm Inc. v. Apple Inc.</i> , 24 F.4th 1367 (Fed. Cir. 2022)	32, 41, 50, 51
<i>Securus Techs., Inc. v. Glob. Tel*Link Corp.</i> , 701 F. App'x 971 (Fed. Cir. 2017)	37, 38
<i>Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.</i> , 853 F.3d 1272 (Fed. Cir. 2017)	15
<i>WBIP, LLC v. Kohler Co.</i> , 829 F.3d 1317 (Fed. Cir. 2016)	37, 41, 49, 52

<i>Xerox Corp. v. Bytemark, Inc.</i> , IPR2022-00624, Paper 9, 15 (PTAB Aug. 24, 2022).....	18, 37, 38, 43, 53
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STATUTES, RULES, AND REGULATIONS

37 C.F.R. § 42.24(d)	58
37 C.F.R. §42.65(a).....	37
37 C.F.R. § 42.104(B)(4)	32, 41, 50, 51
37 C.F.R. § 42.107	57
35 U.S.C. § 103	8, 49
35 U.S.C. § 311(b)	<i>passim</i>
35 U.S.C. § 316(e)	14, 15, 45

Patent Owner Skyworks Solutions, Inc. ("Skyworks") submits the following Patent Owner Response ("POR") to the Petition filed by Kangxi Communication Technologies ("Petitioner") requesting *inter partes* review of claims 1-11 of U.S. Patent No. 9,148,194 ("the '194 patent").

I. INTRODUCTION

The '194 patent discloses a novel method for reducing unwanted interference in a radio-frequency (RF) device for transmitting and receiving information via a wireless signal. Some RF devices operate in multi-band and multi-mode environments such that they are exposed to signals at different frequencies. These signals can mix with each other causing intermodulation distortion (IMD), which can degrade how well the RF device communicates a desired signal. As the '194 patent explains, its novel method was a significant improvement over prior art RF devices because it inhibited a low-frequency blocker signal from mixing with a fundamental-frequency signal in an RF switch.

Petitioner's two primary references, Huang (Ex-1005) and Seshimo (Ex-1007), do not teach the claimed method and system. As shown herein, Huang and Seshimo fail to teach key aspects of the claims, including using first and second capacitors to inhibit a low-frequency blocker signal from mixing with a

fundamental-frequency signal, and forming first and second capacitors on the same semiconductor substrate as the switches.

Huang and Seshimo purport to address problems relating to DC biasing of transistors, and using capacitors to improve isolation of that biasing. Unlike the '194 patent, however, neither Huang nor Seshimo recognizes the problem of intermodulation distortion or the mixing of signals at different frequencies, let alone a low-frequency blocker signal with a fundamental-frequency signal. In fact, neither ever uses the term "low frequency" anywhere in its disclosure. Rather, Huang and Seshimo use capacitors solely for blocking DC signals, to ensure that the transistors are accurately, and individually, DC biased. For this reason, they cannot meet a key limitation of the '194 patent: "inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch." And as Petitioner's own expert admits, a DC signal is not the same as a low-frequency signal.

Lacking any express disclosure of various claimed limitations, Petitioner instead relies upon its expert's conclusory assertions that the missing claim elements are somehow present, or that the gaps of Huang and Seshimo would have somehow been filled by a POSITA's supposed "general knowledge." Such reliance on general knowledge, rather than printed publications or patents, is contrary to 35 U.S.C. § 311(b). Even setting that aside, Petitioner fails, however, to provide any support

for its allegations, and fails to even suggest why a person of ordinary skill in the art would have been motivated to modify Huang and Seshimo using the general knowledge of a POSITA. Instead, Petitioner and its expert offer only unexplained, conclusory string citations that are devoid of any analysis. They neither explain *how* any of the cited references would have rendered the missing '194 patent claim elements obvious to a skilled artisan, nor *how* exactly a skilled artisan would have modified Huang and Seshimo as a result. Nor do they provide any reason *why* a skilled artisan would have been motivated to modify Huang or Seshimo, much less any reason *why* they would have had a reasonable expectation of success in doing so. In the end, it is clear that Petitioner and its expert have used the '194 patent as a hindsight roadmap guiding their whole exercise—which is, of course, entirely improper. Accordingly, the conclusory assertions of Petitioner and its expert should receive no weight.

In short, Petitioner has not shown by a preponderance of the evidence that the challenged claims are invalid. Accordingly, the Board should confirm the patentability of the challenged claims.

II. THE '194 PATENT (EX-1001)

A. Overview of the Patent

The '194 patent discloses a novel architecture for reducing intermodulation distortion (IMD) in radio-frequency (RF) devices. Ex-1001, Title, Abstract.

“Intermodulation distortion (IMD) measures an unwanted signal added to a desired signal due to mixing products from other RF signals.” *Id.*, 8:55-57. The '194 patent explains that intermodulation distortion can be particularly problematic in “a multi-mode, multi-band environment” where intermodulation distortion “can result from two or more signals mixing together to yield frequencies that are not harmonic frequencies.” *Id.*, 8:57-60; *see also id.*, 6:51-54. Ex-2001, ¶ 20.

RF signals fluctuate over time. In other words, RF signals are AC signals which oscillate, not DC signals, which are constant. RF signals generally use a carrier wave having a relatively constant frequency, modulating the carrier wave to carry information. The frequency of the carrier wave is referred to as a fundamental frequency. By using a variety of different fundamental frequencies, wireless devices can operate in different frequency bands and therefore reduce interference. Ex-2001, ¶ 21.

Intermodulation distortion can create interferences in an RF device. Ex-1001, 8:62-67. In these types of multi-band environments, the RF devices are exposed to signals at different frequencies. “[T]wo or more signals mixing together and yielding frequencies that are not harmonic frequencies” results in intermodulation distortion. *Id.*, 6:15-16. The '194 patent provides the example of mixing two signals that “have fundamental frequencies ... that are relatively close to each other in

frequency space” that “can result in peaks in frequency spectrum at frequencies corresponding to different products of fundamental and harmonic frequencies of the two signals.” *Id.*, 6:17-27. When these two signals at different frequencies mix, it can generate undesired harmonics and intermodulation distortion, which can degrade the overall RF device performance. *See id.*, 8:55-67. Ex-2001, ¶ 22.

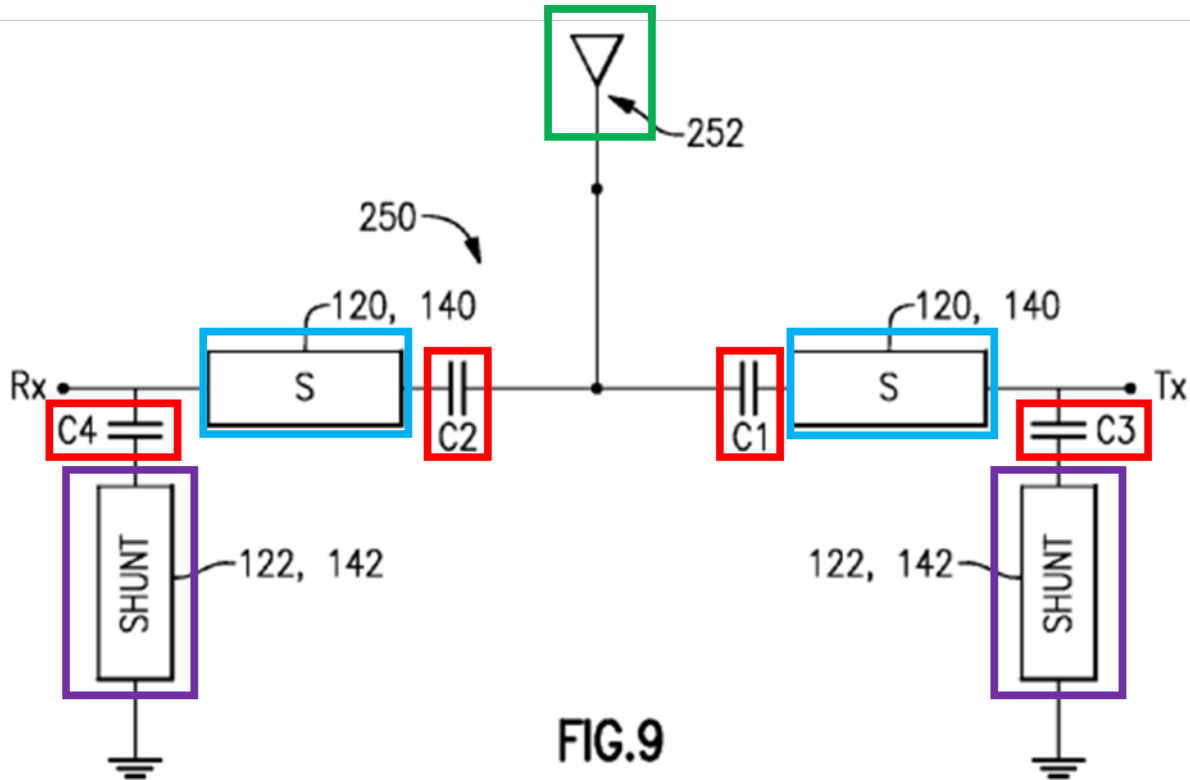
The '194 patent explains that intermodulation distortion can be reduced by improving linearity of the RF device. Ex-1001, 8:61-62, 6:13-14. The '194 patent recognizes the problem with non-linearity in RF systems: non-linearity “can result in introduction of spurious signals into the system” which “can result in interference within the system and degrade the information being transmitted by RF signals.” *Id.*, 6:36-38; *see also id.* 8:61-64 (“A given system’s linearity can govern how much IMD will occur within it, which in turn can create interferences.”). In other words, “[a]n RF system having increased non-linearity can demonstrate increased susceptibility to interference.” *Id.*, 6:38-40. By improving the linearity of the switch in the RF device, the “overall susceptibility of a system to interference can be decreased.” *Id.*, 8:65-67. Ex-2001, ¶ 23.

The claimed invention of the '194 patent reduces intermodulation distortion and non-linearity in an RF device by providing an RF device including, *inter alia*, “a first switch circuit connected between an antenna node and a transmit node,” “a

second switch circuit connected between the antenna node and a receive node,” “a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node,” “a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node,” wherein “at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” Ex-1001, cls. 1, 2. The capacitor is “connected in series with the switch and configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” *Id.*, 1:31-37; *see also id.*, Abstract (“[T]he capacitor configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.”), 1:52-54 (same), 1:65-67 (same), 2:12-14 (same), 2:30-34 (same). Ex-2001, ¶ 24.

Figure 9 of the '194 patent shows an exemplary “RF switching configuration” that can include one or more capacitors to, for example, “inhibit a low-frequency blocker from mixing with a fundamental frequency.” Ex-1001, 3:1-4. In particular, Figure 9 shows “a single-pole-dual-throw (SPDT)” RF switch, where the single pole is connected to **antenna 252**. *Id.*, 9:8-10. One of the two poles is connected to a receive (Rx) port via a **switch circuit S**. *Id.*, 9:10-12. The other of the two poles is

connected to a transmit (Tx) port via a **switch circuit S**. *Id.*, 9:14-15. Each pole is also connected to ground via a **shunt switch circuit SHUNT**. *Id.*, 9:12-13, 9:15-16.



Ex-1001, Fig. 9 (highlighted). Ex-2001, ¶ 25.

This exemplary switching configuration also includes **several capacitors** “to inhibit a low-frequency blocker from mixing with a fundamental frequency.” Ex-1001, 9:25-27. Capacitor C1 is provided between the antenna node and the switch arm of the Tx throw. *Id.*, 9:27-29. Capacitor C2 is provided between the antenna node and the switch arm of the Rx throw. *Id.*, 9:29-30. Capacitor C3 is provided between the Tx node and its shunt switch arm. *Id.*, 9:30-32. Finally, Capacitor C4

is provided between the Rx node and its shunt switch arm. *Id.*, 9:32-33. According to the patent, these capacitors help block or reduce low-frequency jammer signals from mixing with any ON or OFF signal paths. *Id.*, 9:35-37. The inclusion of these capacitors “can lead to improvement in IMD performance, especially for low-frequency blocker signals.” *Id.*, 9:37-39. Ex-2001, ¶ 26.

B. Challenged Claims

Petitioner challenges claims 1-11. The Petition is based on the following grounds:

Ground	Claims Challenged	Statutory Basis	Cited Document(s)
Ground I	1-11	35 U.S.C. § 103	Huang in view of the general knowledge of a POSITA
Ground II	1-11	35 U.S.C. § 103	Seshimo in view of the general knowledge of a POSITA

Claim 2 is representative and is reproduced below:

1. A radio-frequency (RF) Switch system comprising:
 - a first switch circuit connected between an antenna node and a transmit node;
 - a second switch circuit connected between the antenna node and a receive node;
 - a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node;

a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node;

a first shunt arm connected to the first switch circuit and the transmit node, the first shunt arm including a third switch circuit connected to ground; and

a second shunt arm connected to the second switch circuit and the receive node, the second shunt arm including a fourth switch circuit connected to ground.

2. The switch system of claim 1 wherein at least one of the first and second capacitors is configured to inhibit a low frequency blocker signal from mixing with a fundamental frequency signal in the switch.

III. CLAIM CONSTRUCTION

For the purposes of this IPR, Patent Owner applies the plain and ordinary meaning of the claim terms to show that Petitioner fails to demonstrate that the challenged claims are unpatentable. Patent Owner understands that Petitioner also applies the plain and ordinary meaning. Petition, 13; Ex-1003, ¶¶ 44-46. If Petitioner later proposes different constructions for any of the claim term, Patent Owner reserves the opportunity to respond. Ex-2001, ¶¶ 28-30.

IV. LEVEL OF ORDINARY SKILL IN THE ART

The Petition asserts “[a] POSITA in July 2012 would have been someone knowledgeable and familiar with RF electronics, including RF switches and electrical components of such switches, and semiconductor manufacturing processes. POSITAs would have gained knowledge of these concepts through a mixture of

training and work experience, such as by having a Bachelor's degree in electrical engineering, or related field, and approximately two to three years of related experience; or by obtaining a Master's degree in electrical engineering, or related field, but having only a year of related experience; or by having no formal education but experience in RF electronics and semiconductor packaging of at least six to eight years." Petition, 14. Ex-1003, ¶¶ 47-50. Skyworks agrees with Petitioner's definition except that a POSITA could have "no formal education but experience in RF electronics and semiconductor packaging of at least six to eight years," because one could have worked in RF electronics and semiconductor packaging but not have the adequate level of skill for issues of this case. Ex-2001, ¶¶ 31-32.

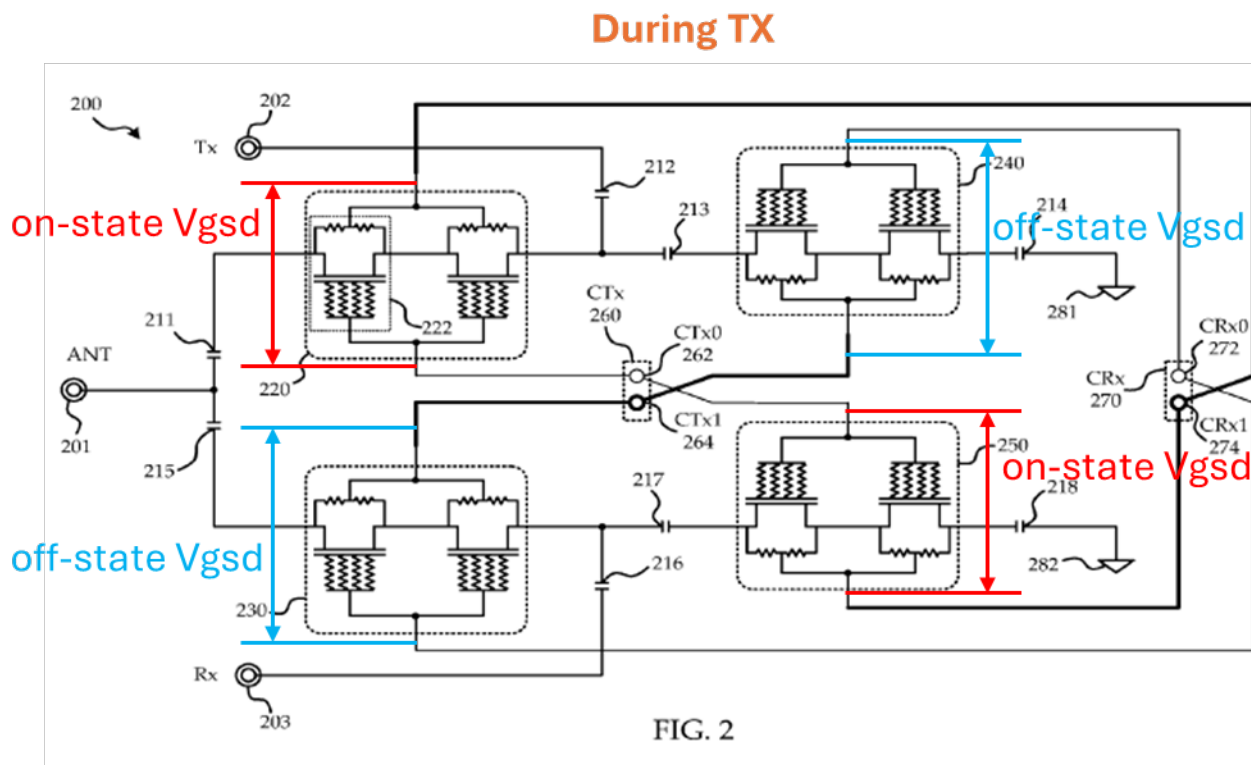
V. SCOPE AND CONTENT OF THE ASSERTED PRIOR ART

The Petition relies on Huang for the first ground and Seshimo for the second ground. Both Huang and Seshimo are directed to systems and methods for improving the DC biasing of transistors, which is the application of DC signals to terminals of the transistors to control their operating points in a RF switch circuit. Ex-2001, ¶ 33.

A. U.S. Pub No. 2011/0254614 to Huang (Ex-1005)

Huang is titled "System and Method of Transistor Switch Biasing in a High Power Semiconductor Switch." Ex-1005, Title. Accordingly, Huang is directed to "biasing transistor switches in a semiconductor based high power switch" by biasing

“off-state V_{gsd} ” (a voltage applied to place a transistor in an off state, which Huang refers to as an “off polarity”) less than “on-state V_{gsd} ” (a voltage applied to place a transistor in an on state, which Huang refers to as an “on polarity”). *Id.*, Abstract, ¶¶ 15-18. The “off-state V_{gsd} ” and “on-state V_{gsd} ” are shown below:



Id., Fig. 2 (annotated). Ex-2001, ¶ 35.

Huang states that it achieves improved performance, namely “low insertion loss and high isolation,” of a RF switch, without needing to fully bias the FETs in the switch with an on or off polarity. *Id.*, ¶ 8. Instead, Huang found that selecting “particular voltages,” less than the full bias voltage, for the off-state V_{gsd} and on-state V_{gsd} of the transistors in the switch still achieved low insertion loss and high

isolation. *Id.*, ¶ 39. For example, Huang suggests using 1.1-1.5V for the off-state V_{gsd} and 2.0-2.5V for the on-state V_{gsd} , even though those voltages are less than “the largest possible bias.” *Id.*, ¶¶ 40, 42. According to Huang, linearity in a switch device can still be achieved with such on/off-state V_{gsd} , even though the transistors are not fully biased on/off as in the prior art. *Id.*, ¶¶ 40-43. Ex-2001, ¶¶ 35-36.

Huang further discloses that “[g]roups of FETs are arranged in the switch along with judiciously chosen resistors and capacitors to ensure low insertion loss along the signal path and high isolation along from the off paths.” Ex-1005, ¶ 3. In particular, Figure 2 depicts “blocking capacitors” 211-218 placed in series with switches 220, 230, 240, and 250. *Id.*, ¶¶ 44-45. These DC blocking capacitors ensure that the on and off-state biasing voltages for each group of transistors in a switch circuit can be set independently from each other, which improves linearity. Ex-2001, ¶ 37.

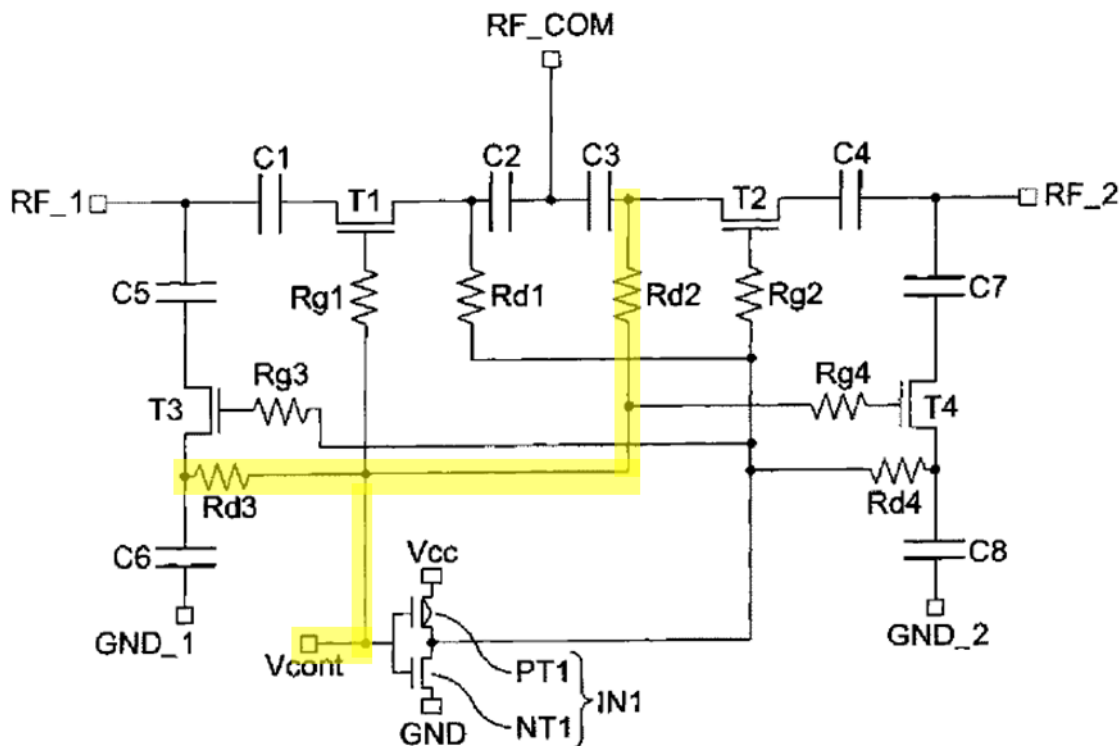
Huang never uses the term low frequency, let alone teach or disclose any low-frequency blocker signals or fundamental-frequency signals. Ex-2001, ¶ 38.

B. JP 2006-121217 to Seshimo (Ex-1006; Ex-1007 for translation)

Seshimo is also directed to DC biasing of transistors in a RF switch circuit to “enhance maximum permissible input power and suppress an increase in on-

resistance.” Ex-1007, Abstract. As highlighted below, the disclosed switching circuit in Seshimo biases either the source or the drain of each transistor.

FIG. 3



Id., Fig. 3 (highlighted). Ex-2001, ¶ 39.

Seshimo recognizes that when designing a high-frequency switch circuit using a MOSFET formed on a silicon substrate, the substrate's resistance and the ON-resistance of a transistor (its resistance when it is on) cause insertion loss (which is a loss of signal power). *Id.*, ¶ 4. Through its biasing technique, Seshimo claims that

it can keep ON-resistance low, thereby reducing insertion loss, and allowing higher input power. Ex-1007, ¶ 7. Ex-2001, ¶ 40.

VI. PETITIONER FAILS TO SHOW THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE

The Petitioner has the burden of proving unpatentability by a preponderance of the evidence. 35 U.S.C. § 316(e); *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1375 (Fed. Cir. 2016). The Petitioner cannot employ mere conclusory statements and must instead articulate specific reasoning based on evidence of record. *Id.*, 1380. This Petition fails to meet its burden. Ex-2001, ¶ 41.

Accordingly, the Petition does not establish unpatentability of the challenged claims by a preponderance of the evidence. 35 U.S.C. § 316(e).

A. The Challenged Claims Would Not Have Been Obvious Over Huang (Ground 1)

The Petition fails to meet its burden with respect to Ground 1. Huang does not disclose first and second capacitors that are configured to “inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” At most, Huang discloses capacitors for DC blocking. In addition, Huang does not disclose that the capacitors identified by the Petition are on the same substrate as the switch circuits as required by certain claims. While the Petition seems to recognize these shortcomings in Huang, and asserts that the claims would have been obvious over Huang in view of the knowledge of a POSITA, it fails to

provide any support for its allegations, and fails even to suggest why a person of ordinary skill in the art would have (1) been motivated to modify Huang and (2) had a reasonable expectation of success doing so. *Cf. In re Kotzab*, 217 F.3d 1365, 1370 (Fed. Cir. 2000) (“Even when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference.”); *Wasica Fin. GmbH v. Cont’l Auto. Sys., Inc.*, 853 F.3d 1272, 1286 (Fed. Cir. 2017) (affirming Board’s rejection of single-reference obviousness argument where petition “lack[ed] the factual substantiation necessary for an obviousness evaluation” and instead merely relied on “conclusory allegation that any differences between [the prior art reference] and claim [] would have been obvious.”). Accordingly, the Petition does not establish unpatentability of the challenged claims by a preponderance of the evidence. 35 U.S.C. § 316(e). Ex-2001, ¶ 42.

1. The Petition fails to show claim 2’s “at least one of the first and second capacitors configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch” is obvious over Huang in view of a POSITA’s knowledge

Claim 2 of the ’194 patent requires “at least one of the first and second capacitors configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” Ex-1001, cl. 2. As explained above,

the '194 patent explains that this claimed feature improves intermodulation distortion of a RF switch. *E.g., Id.*, 9:35-38. Ex-2001, ¶ 43.

To show this claim element, the Petition alleges that “blocking capacitor 211” and “blocking capacitor 215” from Huang’s Figure 2 “disclose” the claimed capacitors. Petition, 37 (citing Ex-1005, ¶ 45). But the Petition provides no evidence that either “blocking capacitor” in Huang is “configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch” as required by this claim element. *See* Petition, 37-38. Indeed, the Petition fails to identify *any disclosure* in Huang of a “low-frequency blocker signal” and a “fundamental-frequency signal,” let alone any “mixing” of any such signals. *Id.* Nor could it. Huang *never* uses the term “low frequency” anywhere in its disclosure because Huang does not address the intermodulation distortion problem solved by the '194 patent. As such, the evidence in the record undisputedly shows that Huang does not disclose this claimed feature. *Medtronic, Inc. v. Barry*, 891 F.3d 1368, 1377 (Fed. Cir. 2018) (The Board rejected Petitioner’s “characterization and pointed out that [Petitioner] and its expert failed to cite to any particular passage or figures from [the prior art] that ‘explicitly disclose’” the claimed feature). Ex-2001, ¶ 44.

Lacking this disclosure, Petitioner instead attempts to cobble together several disjointed paragraphs from Huang to suggest that the size of capacitors 211 and 215

could be selected to configure the capacitors in a way that Huang itself nowhere address—to inhibit a low-frequency blocker signal. Petition, 37-38. For example, the Petition states that “Huang also discloses the importance of selecting the ‘arrange[ment]’ of ‘groups of FETs’ and ‘judiciously chosen ... capacitors’, and of selecting the biasing voltages of the FETs when in ‘on’ and ‘off’ states, in ‘a high power transmit-receive switch using ... SOI’ to achieve, for example, ‘low insertion loss along the signal path’, ‘high isolation from the off paths’, ‘reduce[d] spurious harmonic emissions’, and ‘improve[d] linearity’ for the switch.” *Id.* (citing Ex-1005, ¶¶ 2-3, 39-40, 43-45, 55-59). But nowhere does Huang teach or suggest that the size of blocking capacitor 211 can be used to inhibit any low-frequency blocker signal from mixing with a fundamental-frequency signal. Rather, this argument by Petition is based on no more than application of hindsight bias from the ’194 patent itself. And even then, the Petition fails to offer any evidence or explanation that Huang’s disclosure of “judiciously chosen resistors and capacitors to ensure low insertion loss along the signal path and high isolation from the off paths” is the same as a capacitor configured to “inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” *See id.* Ex-2001, ¶ 45.

Petitioner’s expert’s declaration on this issue adds nothing because it essentially parrots the Petition verbatim. *Compare* Petition, 38-41, *with* Ex-1003,

¶¶ 95-101. As such, Petitioner's conclusory allegations should be given little weight. *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9, 15 (PTAB Aug. 24, 2022) (expert declaration that "merely repeats, verbatim, the conclusory assertion for which it is offered to support" without citing "any additional supporting evidence or provide any technical reasoning to support" is entitled to little weight).

Moreover, nowhere does the Petition allege that Huang's capacitor 211 is inherently "configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal." This is not surprising. Although the Petition alleges that Huang refers to capacitor 211 as a "blocking capacitor" and that a characteristic of capacitors is that they "allow high frequencies to pass through" "while blocking low frequencies" (Petition, 37-38 (citing Ex-1005, ¶ 51)), Huang is directed to a fundamentally different problem (DC biasing of switches) than the '194 patent (inhibiting low-frequency blocker signals from mixing with a fundamental frequency signal), and therefore, its capacitors do not perform the same function as recited in claim 7. Huang includes blocking capacitor 211 to block DC signals, not to block low-frequency signals. Accordingly, blocking capacitor 211 is not inherently configured to perform this function, nor does the Petition allege that it does. Ex-2001, ¶ 46.

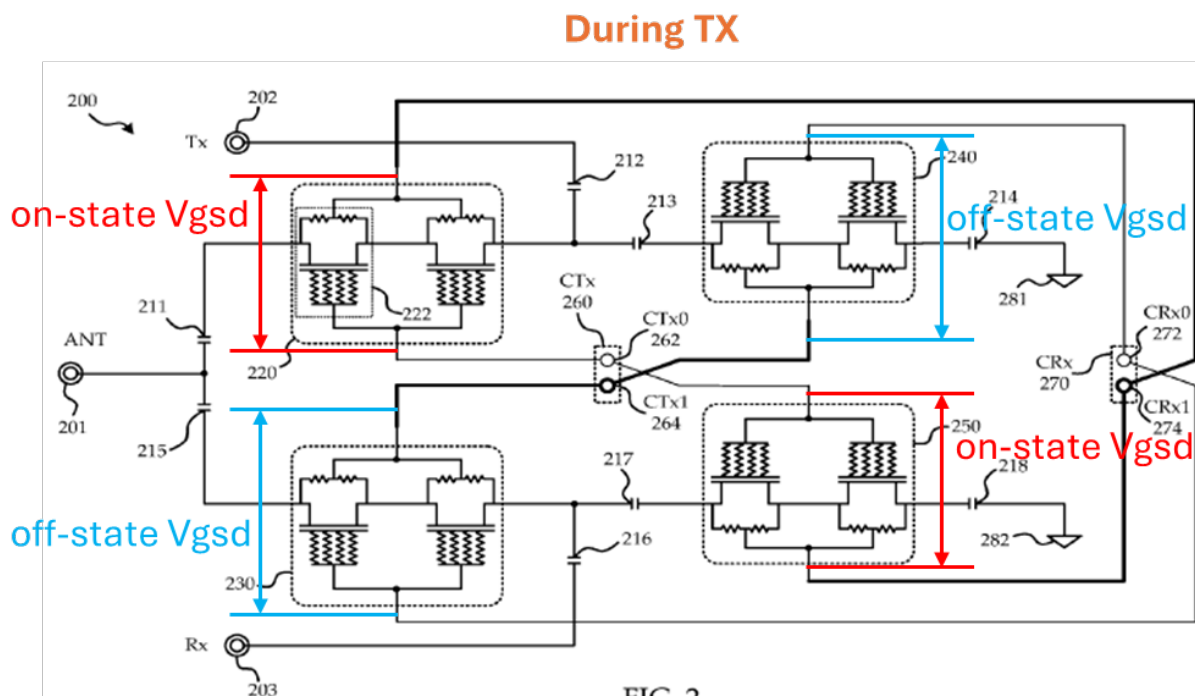
The Petition asserts that “Huang discloses this limitation to POSITAs.” Petition, 37. But as explained above, Huang never uses the term “low frequency” and does not mention anything about a “low-frequency blocker signal,” let alone a capacitor “configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” Huang also never mentions intermodulation distortion. Huang simply labels capacitor 211 as a “blocking capacitor,” and the Petition relies on that label to conclude that a POSITA would understand Huang to disclose that capacitor 211 can be used to inhibit a low-frequency blocker signal. But a POSITA would understand that blocking capacitor 211 in Huang is a DC blocking capacitor, not a capacitor used to inhibit a low-frequency blocker signal. Ex-2001, ¶ 47.

As Dr. Wentzloff explains, “a low-frequency blocker signal” is different from a DC signal. A DC signal is a signal that does not change with time. It has no frequency. Petitioner’s expert agrees, stating: “DC doesn’t change with time. Sometimes people might say DC is equivalent to 0 hertz and sometimes you’ll see that in the literature, but it’s essentially unchanging with time.” Ex-2003, 59:4-10. In contrast to DC signals, AC signals, including low frequency signals, *do* change over time. Petitioner’s expert also agrees with this fundamental principle, conceding “alternating current changes over time ... [but] DC does not change ever.” *Id.*,

57:14-22. As such, it is undisputed that inhibiting an AC, low-frequency blocker signal, from mixing with a fundamental frequency is not the same as Huang's DC blocking. DC blocking is blocking signals at 0 Hz (without frequency), whereas low frequency blocker signals are not a 0 Hz (*i.e.*, they have a frequency). *See* Ex-1001, 6:15-32 (explaining that interference occurs from two or more signals mixing together to yield frequencies that are not harmonic frequencies). Huang's DC blocking is therefore directed to a ***very different*** problem with a ***very different*** solution than the '194 patent claims' capacitor configured to inhibit a low-frequency blocker signal. Ex-2001, ¶ 48.

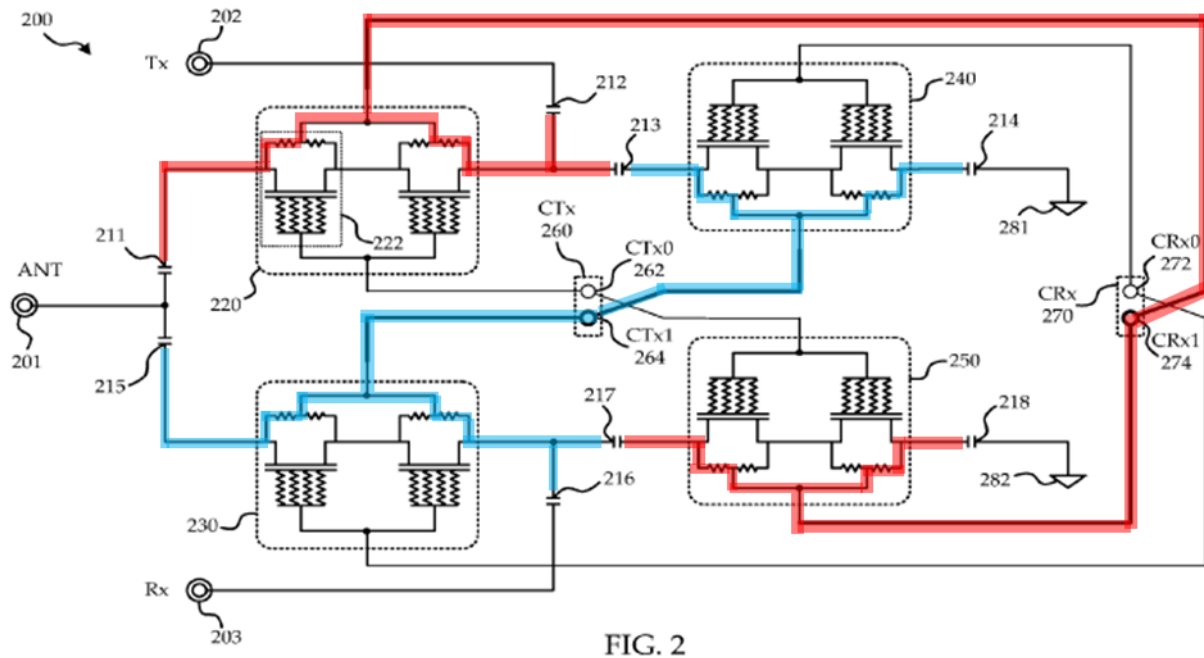
Petitioner's expert also conceded that transistors are biased with a DC bias voltage. Ex-2003, 59:11-14 ("Q. And so then you said when you're biasing these MOSFET transistors, you want to bias them with a DC bias signal, right? A. You ***have to*** bias them with DC, yes.") (emphasis added). Huang's disclosure makes clear that blocking capacitor 211 is only a DC blocking capacitor to isolate the DC bias voltages of the transistors. As explained above, Huang is directed to "biasing transistor switches in a semiconductor based high power switch" by biasing "off-state V_{gsd} " less than "on-state V_{gsd} ." Ex-1005, Abstract, ¶¶ 15-18. Huang clearly states that its invention achieves "low insertion loss and high isolation" by selecting "particular voltages" for the off-state V_{gsd} and on-state V_{gsd} bias voltages for the

transistors in a switch circuit. *Id.*, ¶ 39. Huang teaches that, in a switch circuit with multiple transistors (*e.g.*, MOSFETs or MultiGate FETs (MUGFETs)) in series, signal quality can be improved by biasing each transistor at a voltage level other than its maximum possible bias voltage. *Id.*, ¶ 40. This biasing gives lower harmonic emissions while staying within the reliability limits of the transistors. For example, Huang suggests using 1.1-1.5V for the off-state V_{gsd} and 2.0-2.5V for the on-state V_{gsd} (*i.e.*, biasing off-state V_{gsd} with a lower voltage in magnitude than on-state V_{gsd}). *Id.*, ¶¶ 42-43. The term V_{gsd} refers to the voltages between the nodes highlighted in the figure below, during transmission. *Id.*, ¶ 57. During reception, the on-state and off-state V_{gsd} are switched. *Id.*, ¶ 58.



Id., Fig. 2 (annotated). Dr. Larson, Petitioner's expert, agrees that Huang is about a specific biasing of transistors in a switch circuit. Ex-2003, 72:4-13. Ex-2001, ¶ 49.

Figure 2 depicts blocking capacitors 211-218 placed in series with switches 220, 230, 240, and 250. Ex-1005, ¶¶ 44-45. As Huang explains, blocking capacitors 211-218 “isolate” the bias voltages for the drain and source terminals of each of the MUGFETs to independently bias each transistor. For example, blocking capacitors 211, 212, and 213 block DC signals that could otherwise raise or lower the bias voltages of the transistors in switch 220. Huang refers to this phenomena as insertion loss and discloses that the values of the blocking capacitors should be “judiciously chosen” to minimize insertion loss. *Id.*, ¶ 3. As explained above, Huang uses carefully selected DC bias voltage levels—*e.g.*, 1.0-1.5 V for off-state and 2.0-2.5 V for on-state—to individually bias the groups of transistors, which differed from conventional biasing. In this context, capacitors 211 to 218 only protect the DC bias voltages of the transistors in switches 220 to 250, isolating the red and blue DC paths as shown below, so that transistors 220-250 can be individually biased.



Ex-1005, Fig. 2 (highlighted). Ex-2001, ¶ 50.

The function of the DC blocking capacitors in Huang becomes even clearer when viewed in light of the prior art upon which Huang aims to improve. In the background section, Huang describes a general method of using a series of transistors in an RF signal path, where the gate and source/drain terminals are biased to fully turn the transistors on or off. Ex-1005, ¶ 3. As an example, Huang discusses Nakatsuka (Ex-1013). *Id.*, ¶ 4. Figure 1A of Huang, which is from Nakatsuka, shows **biasing terminal 111** connected to the gates of transistors 122 in switch 120, and to the source/drain terminals of transistors (not labeled) in switch 130. *Id.*, Fig. 1A, Ex-1013, Fig. 1. Another **biasing terminal 112** connects to the source/drain

terminals of transistors 122 in switch 120, and to the gates of transistors (not labeled) in switch 130, as shown below:

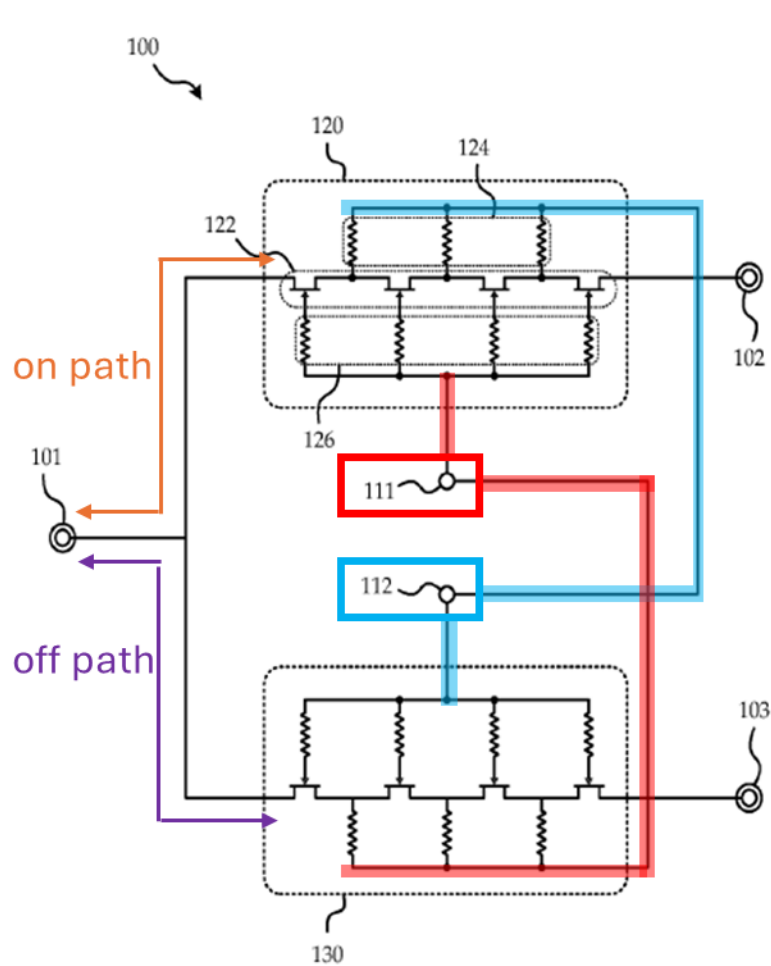


FIG. 1A (PRIOR ART)

Ex-1005, Fig. 1A (annotated), ¶¶ 4, 6; *see* Ex-1013, Fig. 1, ¶ 82. This configuration allows a high or low voltage to be applied simultaneously to the gates of the transistors in switch 120 and the drains/sources of the transistors in switch 130 **via biasing terminal 111**, and likewise to the drains/sources of the transistors in switch

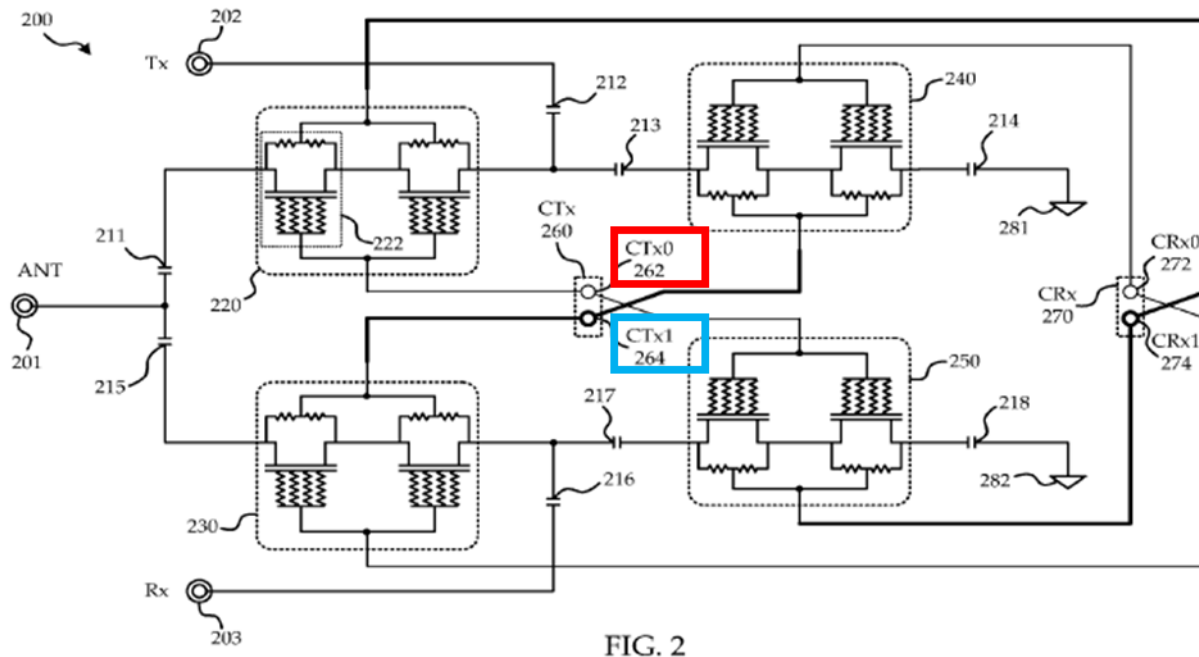
120 and the gates of the transistors in switch 130 **via biasing terminal 112**. As a result, when biasing terminal 111 is set to high and biasing terminal 112 is set to low, the transistors in switch 120 are turned fully on, establishing the **on path**, while the transistors in switch 130 are turned fully off, establishing the off path, as illustrated in the figure above. Ex-1005, ¶ 7. According to Huang, this configuration “fully” biases each transistor by applying the same bias voltage in magnitude but in reverse polarity and ensures “low insertion loss and high isolation which are very important when dealing with high-power signal transmission.” Ex-1005, ¶ 8. Ex-2001, ¶ 51.

Figure 1B of Huang (shown below), which is Figure 2 of Nakatsuka, adds **shunt switches 180 and 190** and **blocking capacitors 182 and 192** to Figure 1A of Huang (or Nakatsuka's Figure 1). Ex-1005, Fig. 1B; Ex-1013, Fig. 2. The Figure 1B circuit is configured so that switches 160 and 190 turn on and off together and switches 170 and 180 turn on and off together.

Nakatsuka explains the motivation behind its proposed configurations. Nakatsuka states, “[w]ith this configuration, the device can handle power larger than that of the prior art” and “[f]urthermore, the current consumption can be reduced.” Ex-1013, ¶ 21; Ex-2003, 76:13-77:7 (agreeing that Nakatsuka is directed to making a switch perform at a higher power level). Nakatsuka attributes these improvements to the configuration’s ability to prevent voltage levels at the intermediate connection points of the transistors from dropping. As a result, the circuit increases the power handling capability of the transistors and reduces current consumption compared to the prior art. Ex-1013, ¶ 24; Ex-2003, 77:8-80:16. Petitioner’s expert, Dr. Larson, agreed that the voltage levels in this context means DC voltage. Ex-2003, 81:3-10 (“Q. ... Nakatsuka is preventing the DC voltage from lowering, right? A. Yeah, I believe one effect of these resistors would be to affect the lowering of the DC voltage in this configuration with these FETs.”). Nakatsuka’s focus was about DC biasing, not about improving intermodulation distortion. Ex-2001, ¶¶ 53-54.

Returning to Figure 2 of Huang, Huang builds upon the circuit from Figure 2 of Nakatsuka. A key distinction in Huang is that the voltage level applied to the gates of the transistors in switch 220 via **primary bias output 262 (CTx0)** is different from the voltage applied to the drains/sources of the transistors in switch 230, which comes from **secondary bias output 264 (CTx1)**. Ex-1005, ¶ 54.

Another difference is that Huang adds additional blocking capacitors 211-213 and 214-217 to Nakatsuka. *Compare* Ex-1005, Fig. 2 *with* Fig. 1B; Ex-2003, 95:11-96:12.



Ex-1005, Fig. 2 (highlighted). While Nakatsuka applies the same voltage level (but in reverse polarity) to corresponding nodes, Huang applies two different voltage levels, simply biasing the off-state V_{gsd} lower than the on-state V_{gsd} , to improve signal quality. Ex-2003, 105:6-22 (explaining that “Huang talks about ... optimizing the VGSD of the devices in the ON and OFF states to get the best performance possible” and “optimizing the VGSD is about ... the DC bias of the gate and source/drain regions in order to ... optimize switch performance.”); Ex-2001, ¶ 55.

The two voltage levels (primary bias output 262 and secondary bias output 264) are explained further with Huang's Figure 4A:

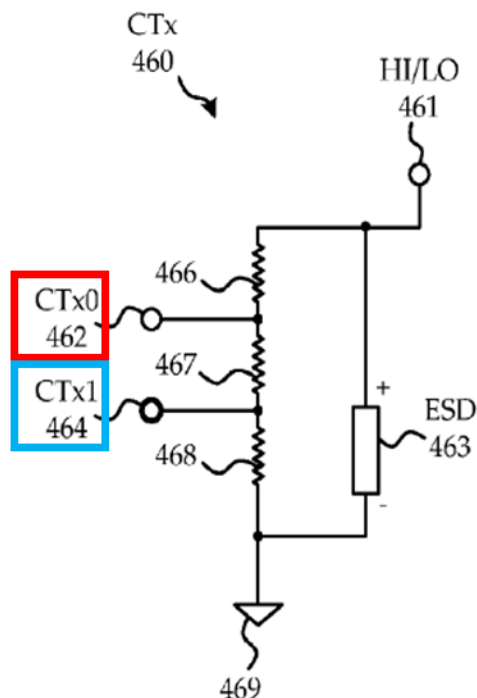


FIG. 4A

Ex-1005, Fig. 4A. Huang uses a voltage divider between a HI/LO voltage input terminal and ground to generate two distinct voltage levels: **CTx0** (primary bias output) and **CTx1** (secondary bias output). *Id.*, ¶ 48. The resistor ratio among resistors 466, 467, and 468 determines the specific voltage levels at CTx0 and CTx1, which determines the on-state and off-state Vgsd voltages. In other words, Huang enables more precise control of the DC bias voltages applied to the transistors than Nakatsuka. When read in this context, it becomes clear that Huang's reference to

“blocking capacitors” refers specifically to DC blocking capacitors, as they are essential for applying these carefully controlled DC bias levels. Ex-2001, ¶ 56.

Moreover, Huang's use of the term “blocking capacitor” is consistent with how that term was used in the RF field at the time of the invention of the '194 patent, to refer to a capacitor to block DC. The McGraw-Hill Dictionary of Electrical and Computer Engineering (6th Ed. 2003) provides the same definition for “blocking capacitor” and “coupling capacitor,” which is “[a] capacitor used to block the flow of direct current while allowing alternating or signal current to pass.” Ex-2005, 124. Even the references that the Petition cites in the State of the Art section confirm that blocking capacitor means a capacitor for blocking DC. *See, e.g.*, Ex-1011, 2617 (“on-chip dc blocking and decoupling MIM capacitors”); Ex-1024, Fig. 9 (“DC block”); Ex-1009, ¶ 83 (“prevents the DC-component”); Ex-1035, 5 (“each transistor is DC-isolated by a DC blocking capacitor”). Thus, contrary to the Petition's conclusory assertions, a POSITA would understand blocking capacitor 211 in Huang to be a “DC blocking capacitor” that blocks DC signals, which are constant signals, unlike the AC signals of the '194 patent, which oscillate and have a frequency. A POSITA would not understand blocking capacitor 211 in Huang to be configured to “inhibit a low frequency blocker signal from mixing with a fundamental-frequency signal” as required by claim 2. Ex-2001, ¶ 57.

As such, Huang fails to disclose, expressly or inherently, a capacitor “configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” Seemingly conceding that Huang does not disclose this claim element, the Petition sets forth an alternative position that a capacitor “configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch” would have been obvious over Huang in view of the general knowledge, skill, and creativity of a POSITA. Petition, 39 (“Furthermore, to the extent PO asserts that Huang does not expressly disclose blocking capacitor 211 performing this step in SPDT switch 200, with the SPDT switch 200 components arranged as shown in Annotated FIG. 2, and opposing series and shunt switches placed in ON and OFF states depending on the transmit or receive mode of SPDT switch 200 as disclosed by Huang, POSITAs understood this capacitor’s inhibition of low-frequency blocker signals from mixing with fundamental frequency signals in SPDT switch 200 to merely be a matter of design choice.”). However, the Petition fails to meet the standard required for such a shift. Rather than providing a proper analysis under the obviousness framework accepted by the Board, the Petition merely presents a collection of references without analyzing them under the proper legal framework. Ex-2001, ¶ 58.

Petitioner does not allege that a combination of Huang and another prior art reference renders the claims obvious. Instead, Petitioner relies on the supposed general knowledge, skill and creativity of a POSITA to supply the missing claim limitation—a capacitor “configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” Petition, 38-40 (relying on what “POSITAs understood” based on the Petition’s “discuss[ion] in the State of the Art section”). But a petitioner may request to cancel claims “only on the basis of prior art consisting of patents or printed publications.” 35 U.S.C. § 311(b). The “knowledge, skill, and creativity” of a POSITA” (Petition, 30) is not a patent or printed publication. *Id.*; see also *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1376-77 (Fed. Cir. 2022) (holding that the basis of a ground in an IPR must rely on prior art patents or printed publications); Director Memorandum, “Enforcement and Non-Waiver of 37 C.F.R. § 42.104(B)(4) and Permissible Uses of General Knowledge in Inter Partes Reviews (July 21, 2025) (“[P]ast efforts by the Office to permit limited use of general knowledge to satisfy a missing claim limitation are no longer consistent with Federal Circuit precedent.”). Accordingly, Petitioner’s reliance on the general knowledge of a POSITA to supply a missing claim limitation is improper.

In addition, the Petition does not identify the specific differences between the prior art and the claims at issue that it purports to rely upon such “general knowledge” to fill. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966) (“[D]ifferences between the prior art and the claims at issue are to be ascertained.”). It also does not identify any motivation that a POSITA would have had to modify Huang to arrive at the patented invention. The Petition identifies no modifications, nor explains how any such modifications would have worked. Nor does it provide any reason to expect success. The Petition therefore fails to meet its burden to show that the claims are obvious. *Cf. Game & Tech. Co v. Activision Blizzard Inc.*, 926 F.3d 1370, 1381 (Fed. Cir. 2019) (“A patent can be obvious in light of a single prior art reference if it would have been obvious to modify that reference to arrive at the patented invention”); *see also Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016) (“[O]ne must have a motivation to combine accompanied by a reasonable expectation of achieving what is claimed in the patent-at-issue”). The Board has previously rejected—and the Federal Circuit has upheld—petitions that provided far more support for obviousness than the Petition does here. *See, e.g., Comcast Cable Commc’ns, LLC v. Promptu Sys. Corp.*, 838 F. App’x 555, 557 (Fed. Cir. 2021) (“[T]he Board simply found that [Petitioner]’s conclusory, threadbare arguments were not enough to establish motivation to combine”).

In its deficient obviousness analysis, the Petition cites “low insertion loss along the signal path,” “high isolation from the off paths,” “reduce[d] spurious harmonic emissions,” and “improve[d] linearity” from Huang as the alleged motivation to turn to the general knowledge of a POSITA to fill the gap for a capacitor “configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” Petition, 37-38. But all of those cited benefits stem from Huang’s improved DC biasing technique. As explained above, Huang is directed to improved systems and methods for DC biasing the transistors in an RF switch. The Petition cites paragraphs 2-3, 39-40, 43-45, and 55-59 from Huang. Ex-2001, ¶ 59.

Paragraphs 2 and 3 discuss problems in the prior art related to the general approach of biasing transistors fully on and fully off—similar to Nakatsuka’s method—and emphasize the DC bias voltage of the transistors. Ex-1005, ¶¶ 2, 3 (“Many of the main advances in semiconductor-based transmit-receive switches have been with respect to isolation and insertion loss. Groups of FETs are arranged in the switch along with judiciously chosen resistors and capacitors to ensure low insertion loss along the signal path and high isolation from the off paths”); Ex-2003, 104:9-105:22. Ex-2001, ¶ 60.

Paragraphs 39 and 40 describe Huang's preferred embodiments, which again involve setting DC bias voltages. Ex-1005, ¶¶ 39 (“While maximizing the on-state V_{gsd} for the on-state FET group switches and fully maximizing the off-state V_{gsd} of the off-state FET group switches achieves respectively low insertion loss and high isolation where and as needed, a quality of the signals passing through the transmit-receive switch depends upon, amongst other things, the particular voltages chosen for off-state V_{gsd} and on-state V_{gsd} of the FETs within the switch.”), 40; Ex-2003, 105:23-108:2). Ex-2001, ¶ 61.

Likewise, paragraphs 43-45 discuss achieving low insertion loss and good linearity by configuring the DC bias voltages in specific ways. Ex-1005, ¶¶ 43 (“For the on-state FET group switches, lower harmonic emissions were found above a voltage level close to the gate to source breakdown voltage. With the 2.5V SOI technology, 2.0-2.5 V of on-state V_{gsd} was found to exhibit a very low insertion loss, and good linearity. Considering the reliability constraint of 2.5 V, the operating on-state V_{gsd} level for the turned on FET group switches is chosen to be 2.0 V-2.5 V.”), 44-45; Ex-2003, 108:3-109:18. Ex-2001, ¶ 62.

So do paragraphs 55-59. Ex-1005, ¶¶ 55, 56 (“As with the prior art, in order to ensure low insertion loss and adequate isolation, when the antenna 201 is utilized for transmission, the first series FET group switch 220 and the second shunt FET

group switch 250 are provided with on-state V_{gsd} such that a strong inversion layer creates a low resistance path between source and drain diffusions while the second series FET group switch 230 and the first shunt FET group switch 240 are provided off-state V_{gsd} wherein no channel is established. In order to reduce spurious harmonic emissions and to improve linearity, on-state V_{gsd} is chosen to be at a level between 2.0V and 2.5V while off-state V_{gsd} is chosen to be at a level between 1.1V and 1.5V.”), 57-59; Ex-2003, 109:19-111:12. As such, none of the cited paragraphs relate to improving intermodulation distortion or to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the RF switch. Ex-2001, ¶¶ 63-64.

The Petition mischaracterizes Huang and the '194 patent by asserting that Huang leaves “particular capacitor value implementation details to design choices of POSITAs.” Petition, 38-39. But Huang is fundamentally about DC biasing and does not even mention “low frequency” or “intermodulation distortion.” Even if Huang did leave capacitor value implementation details to design choice, as alleged, such choices—within the context of Huang—would only vary to the extent they improve DC biasing and insertion loss. To configure a capacitor to “inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal” and thereby improve intermodulation distortion, there must be a motivation to make such

a design choice. Huang does not teach or suggest any such motivation. That a capacitor is inherently a “frequency-dependent impedance” device cannot short-circuit the obviousness analysis—here, the relevant question is whether the reference provides any motivation for a POSITA to implement a capacitor in a specific way in a specific circuit, as claimed. Otherwise, every analog circuit patent would be rendered obvious merely for using known components—resistors, capacitors, inductors. *Xerox Corp.*, IPR2022-00624, Paper (finding insufficient Petitioner’s rationale where Petitioner’s expert’s “opinion on the alleged obviousness and simplicity of the combination appears to be based on nothing more than his ipse dixit; he provides no explanation why an ordinarily skilled artisan would have made the combination.”) (internal citation omitted); *Securus Techs., Inc. v. Glob. Tel*Link Corp.*, 701 F. App’x 971, 974-76 (Fed. Cir. 2017); *see also* 37 C.F.R. §42.65(a); *cf. WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1337 (Fed. Cir. 2016) (“The real question is whether that skilled artisan would have plucked one reference out of the sea of prior art ... and combined it with [other] ... elements to address some need present in the field. ... Whether a skilled artisan would be motivated to make a combination includes whether he would select particular references in order to combine their elements.”). Ex-2001, ¶ 65.

The Petition also asserts that “Huang’s disclosure is identical to the ’194 Patent’s disclosed positioning in its FIG. 9 SPDT switch 250,” citing the Prosecution History section. Petition 37. As explained above, Huang’s disclosure is not identical to the ’194 patent. The role of the capacitors in Huang and the ’194 patent are different. Moreover, the Petition’s citation to the prosecution history without any explanation is misleading. The Examiner found the claims patentable over the cited prior art. Ex-1002, 12. Ex-2001, ¶ 66.

Lastly, the Petition relies on the “State of the Art.” Petition, 40. The Petition fails to properly explain why a POSITA would be motivated to use any of these references to select a capacitor to “configured to inhibit a low frequency blocker from mixing with a fundamental-frequency signal.” Petitioner’s conclusory allegations should be given little weight. *Xerox Corp.*, IPR2022-00624, Paper (finding insufficient Petitioner’s rationale where Petitioner’s expert’s “opinion on the alleged obviousness and simplicity of the combination appears to be based on nothing more than his *ipse dixit*; he provides no explanation why an ordinarily skilled artisan would have made the combination.”) (internal citation omitted); *Securus Techs.*, 701 F. App’x at 975-76 (finding that Petitioner’s proposed obviousness ground was “simply too conclusory to satisfy its burden of proving by

a preponderance of the evidence that the skilled artisan would have combined these references in the way of the claimed invention.”). For example:

- Ex-1011 states “on-chip *dc biasing* MIM capacitors are required” (Ex-1011, 2616 (emphasis added)) and “on-chip *dc blocking* and decoupling MIM capacitors” (Ex-1011, 2617 (emphasis added));
- Ex-1024 states “DC block” (Ex-1024, Fig. 9);
- Ex-1029 states “ C_{B1} and C_{B2} [] allow *dc biasing* of the TX and RX nodes of the switch” (Ex-1029, 36 (emphasis added));
- Ex-1009 states “prevents the *DC-component* on the transmission-side from being generated on the reception-side, or vice versa” (Ex-1009, ¶ 83 (emphasis added)); and
- Ex-1035 states “each transistor is DC-isolated by a DC blocking capacitor” (Ex-1035, 5).

Ex-2003, 123:18-125:14, 126:6-127:9, 127:15-129:20. These references, like Huang, focus on DC biasing and blocking—not on inhibiting low-frequency blocker signals from mixing with fundamental-frequency signals to improve intermodulation distortion. The Petition offers no rationale regarding why a POSITA would be motivated to use any of these references to perform this function. Ex-2001, ¶ 67.

As such, the Petition fails to meet its burden of proving that a capacitor “configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch” would have been obvious over Huang in view of a POSITA’s knowledge.

2. The Petition fails to show claim 5’s “forming a [first/second] capacitor on the semiconductor substrate so as to be connected in series with the [first/second] switch circuit between the [first/second] switch circuit and the antenna node” is obvious over Huang in view of a POSITA’s knowledge

Claim 5 of the ’194 patent requires “a semiconductor substrate” with a “first switch circuit” “second switch circuit,” “first capacitor,” and “second capacitor” formed on “*the* semiconductor substrate.” Ex-1001, cl. 5 (emphasis added). As the ’194 patent specification explains, the claimed inhibiting capacitors can be “part of the same semiconductor die” as the transistors, as recited in claim 5, rather than, in alternative unclaimed embodiments, “part of a second die mounted on the packaging substrate” or “at a location outside the semiconductor die.” Ex-1001, 2:15-21; Ex-2003, 131:21-133:14 (agreeing that the capacitors can be at any of these locations); Ex-2001, ¶ 68.

The Petition treats Huang as disclosing all these elements on the same semiconductor substrate. *See* Petition, 44 (“Huang discloses ...”). However, Huang is silent as to whether its capacitors in the Figure 2 circuit are on the same die as the

other components. The Petition again generally relies on the State of the Art to the extent that Huang does not explicitly disclose this element by citing to a string of references. Petition, 44-45 (“To the extent PO asserts that Huang does not explicitly disclose ...”). But a petitioner may request to cancel claims “only on the basis of prior art consisting of patents or printed publications.” 35 U.S.C. § 311(b). The general “knowledge, skill, and creativity” of a POSITA (Petition, 35) is not a patent or printed publication. *Id.*; *see also Qualcomm*, 24 F.4th at 1376-77 (holding that the basis of a ground in an IPR must rely on prior art patents or printed publications); Director Memorandum, “Enforcement and Non-Waiver of 37 C.F.R. § 42.104(B)(4) and Permissible Uses of General Knowledge in Inter Partes Reviews (July 21, 2025) (“[P]ast efforts by the Office to permit limited use of general knowledge to satisfy a missing claim limitation are no longer consistent with Federal Circuit precedent.”). Accordingly, Petitioner’s reliance on the general knowledge of a POSITA to supply a missing claim limitation is improper. Ex-2001, ¶ 69.

Moreover, whether the claim elements were known in prior art references cannot be the end of the obviousness analysis. *WBIP*, 829 F.3d at 1337 (“The real question is whether that skilled artisan would have plucked one reference out of the sea of prior art ... and combined it with [other] ... elements to address some need present in the field. ... Whether a skilled artisan would be motivated to make a

combination includes whether he would select particular references in order to combine their elements.”); *ActiveVideo Networks, Inc. v. Verizon Commc’ns., Inc.*, 694 F.3d 1312, 1327 (Fed. Cir. 2012) (finding expert’s testimony “conclusory and factually unsupported” where “[t]he expert failed to explain how specific references could be combined, which combination(s) of elements in specific references would yield a predictable result, or how any specific combination would operate or read on the asserted claims.”).

A POSITA could choose off-die capacitors over on-die capacitors. Indeed, for Huang’s capacitors, a POSITA would have been motivated to implement them off-die, and thus not on the same semiconductor substrate as the transistors. Huang teaches that the goal of its capacitors is to reduce insertion loss. Ex-1005, ¶ 3. A POSITA implementing Huang would have therefore been motivated to select capacitors to achieve better insertion loss. A POSITA would have known that larger capacitors have better insertion loss. And a POSITA also would have known that capacitors could be larger if they were implemented off-die where there are not the same space constraints as for on-die capacitors. As such, a POSITA would have been motivated to implement the capacitors in Huang off-die where they could be larger and achieve better insertion loss. In contrast, the Petition does not consider insertion loss, one of Huang’s objectives, but simply assert “design choice” and

“cost.” Petition, 42. And again, Petitioner’s expert’s declaration on this issue nearly matches the Petition verbatim and should be entitled little weight. *Compare* Petition, 44-45, *with* Ex-1003, ¶¶ 118-120. *Xerox Corp.*, IPR2022-00624, Paper 9, 15 (PTAB Aug. 24, 2022) (expert declaration that “merely repeats, verbatim, the conclusory assertion for which it is offered to support” without citing “any additional supporting evidence or provide any technical reasoning to support” is entitled to little weight). Ex-2001, ¶ 69.

3. Dependent Claims

Because claim 6 depends from independent claim 5, claim 6 would not have been obvious over Huang in view of a POSITA’s knowledge for the same reason as claim 5 as explained above. The Petition fails for the same reason. Ex-2001, ¶ 70.

Dependent claim 8 would not have been obvious over Huang in view of a POSITA’s knowledge for the same reason as dependent claim 2 because claim 8 also requires “at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental frequency signal in the switch,” as explained above. The Petition fails for the same reason. Ex-2001, ¶ 71.

Dependent claim 9 would not have been obvious over Huang in view of a POSITA’s knowledge for the same reason as independent claim 5 for requiring the

“first capacitor” to be “part of the same semiconductor die as the first switch,” as explained above. The Petition fails for the same reason. Ex-2001, ¶ 72.

Dependent claim 10 would not have been obvious over Huang in view of a POSITA's knowledge for the same reason as independent claim 5 for requiring the “first capacitor” be “part of a second die,” which is not the same die as the semiconductor die where the first switch is formed. The Petition fails for the same reason. Ex-2001, ¶ 72.

B. The Challenged Claims Would Not Have Been Obvious Over Seshimo (Ground 2)

Ground 2 fails for similar reasons as Ground 1. As further explained below, Ground 2 is duplicative of Ground 1. Seshimo, like Huang, only discloses DC blocking capacitors and not capacitors “configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” Seshimo also does not disclose that the capacitors identified by the Petition are on the same substrate as the switch circuits as required by certain claims. While the Petition seems to recognize these shortcomings in Seshimo, and asserts that the claims would have been obvious over Seshimo in view of the knowledge of a POSITA, it only repeats the same argument made in Ground 1 based on Huang. The Petition therefore again fails to provide any support for its allegations, and fails to even suggest why a POSITA would have been motivated to modify Seshimo, much

less have had a reasonable expectation of success in doing so. Accordingly, the Petition does not establish unpatentability of the challenged claims by a preponderance of the evidence. 35 U.S.C. § 316(e). Ex-2001, ¶ 73.

1. The Petition fails to show claim 2's "at least one of the first and second capacitors configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch" is obvious over Seshimo in view of a POSITA's knowledge

As presented in the Petition, the Seshimo ground is duplicative of the Huang ground and should be rejected for the same reasons. Except for the opening paragraph of each ground and citations to each reference, the two grounds are identical. *Compare* Petition, 59-63 (Seshimo) *with* 37-41 (Huang). The Petition does not present any other evidence or analysis beyond substituting Huang's disclosures with those of Seshimo. The Seshimo ground, however, is just as deficient as the Huang ground, as explained below. Ex-2001, ¶ 74.

The Petition alleges that Seshimo's capacitor C3 in Figure 3 "discloses" the claimed "first capacitor" (Petition, 68) and renders obvious that the capacitor is "configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch." Petition, 70 ("POSITAs would understand Seshimo's disclosed implementation of capacitor C3 as being a high-pass filter that would 'inhibit[] a low-frequency blocker signal from mixing with a

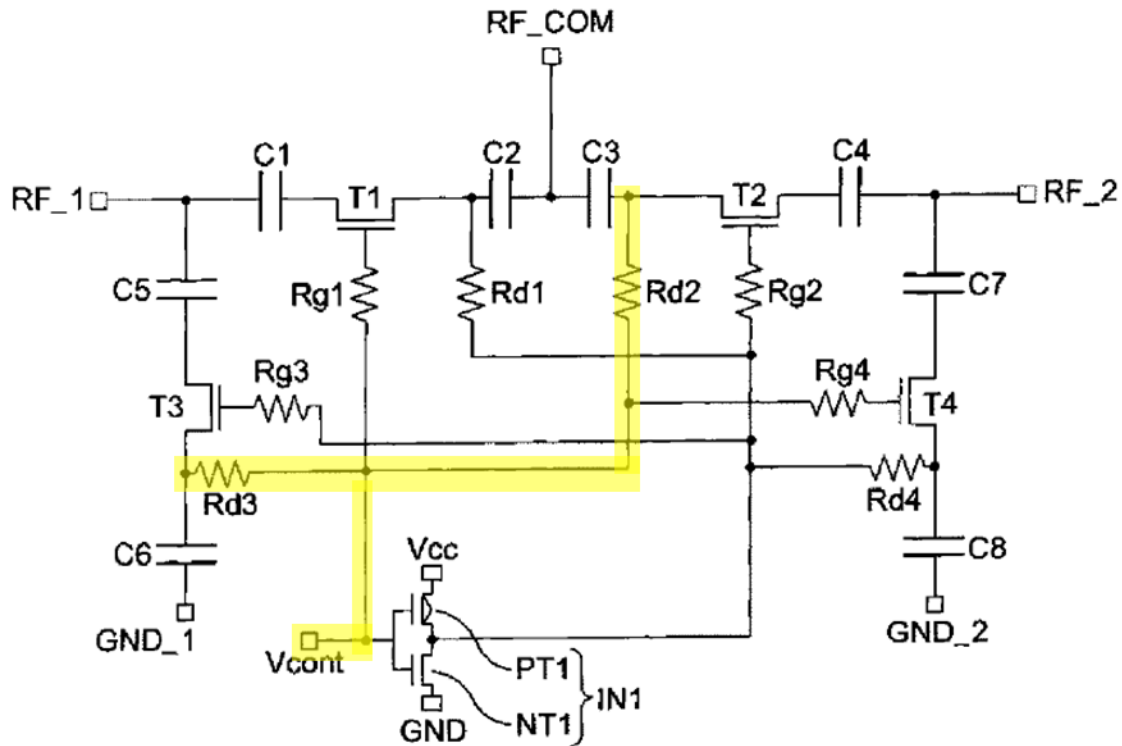
fundamental frequency signal in the RF switch.”). But just like Huang, Seshimo never mentions anything about a “low-frequency blocker signal” or a capacitor “configured to inhibit a low frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” Seshimo also never discusses intermodulation distortion. Ex-2001, ¶ 75.

Seshimo is clear that its capacitors C1-C8 are all DC blocking capacitors. Ex-1007, ¶ 90 (“C1 to C8: [DC] Component removal capacitor”); Ex-1006, ¶ 90 (“C1~C8 DC”); Ex-2004, ¶ 90 (“C1-C8: DC component removing capacitance”).¹

¹ In the English translation submitted by Petitioner (Ex-1007), “DC” is missing from paragraph 90 after the capacitor labels C1 through C8, despite “DC” being present, in English, in the original Japanese application (Ex-1006) at that exact location of paragraph 90. *Compare* Ex-1007, ¶ 90 *with* Ex-1006, ¶ 90. Seshimo consistently refers to capacitors C1-C4 as “DC component removal capacitors” in other embodiments. Ex-1007, ¶¶ 13-14, 33-35; Ex-2003, 117:10-16, 117:25-118:19. Therefore, it is clear that Seshimo intended all its capacitors C1 through C8 to likewise be DC component removal capacitors. Nevertheless, Patent Owner submits another certified English translation (Ex-2004), which provides a more accurate translation.

Petitioner's expert Dr. Larson agrees. Ex-2003, 121:5-15 ("Q. So fair to say that a more accurate translation for capacitors C1 to C8 is DC component removal capacitor? A. ... But certainly that hints that DC should have been included in the -
- perhaps it should have been included in the English translation."), 121:25-122:7 ("Q. As a person of ordinary skill in the art, would you agree that the phrase 'DC component removal capacitor' is the same as DC blocking capacitor? A. I don't see any substantial difference between those two and I think a person of ordinary skill in the art would view those as essentially the same."). Figure 3 of Seshimo shows the disclosed biasing configuration:

FIG. 3



Ex-1007, Fig. 3 (highlighted). As can be seen in highlighted Figure 3, Seshimo's transistor biasing is similar to Huang's. In Seshimo, instead of biasing both the source and drain of each transistor like Huang, only one of the source or drain of each transistor is biased. Seshimo does not use two different bias voltage levels (on-state and off-state) as in Huang. In essence, Seshimo is a similar, but alternative approach to the biasing circuit disclosed in Huang. Ex-2001, ¶ 76.

Like Huang, Seshimo is directed to “enhanc[ing] maximum permissible input power suppress[ing] an increase in ON-resistance” through a particular DC biasing

of transistors in a switch circuit. Ex-1007, Abstract, ¶ 7; Ex-2003, 122:8-123:6. Seshimo recognizes that the substrate's resistance and the ON-resistance of the MOSFET (*i.e.*, the resistance of a transistor when it is on) causes insertion loss (loss of signal power). Ex-1007, ¶ 4. By biasing transistors similarly to Huang, Seshimo proposes that ON-resistance can be reduced, and therefore, loss of signal power can also be reduced. However, like Huang, Seshimo does not address improving intermodulation distortion. Ex-2001, ¶ 77.

As for the obviousness analysis, this ground suffers the same deficiencies as the Huang ground. Because the Petition makes the same argument in Seshimo as it does in the Huang ground, and relies on the same "State of the Art," the response explained in detail above in Section VI.A.1 applies equally to those arguments. In particular, the Petition improperly relies on the supposed general knowledge of a POSITA to try to fill in the gaps of Seshimo, contrary to 35 U.S.C. § 311(b), and fails to perform a proper analysis under § 103. *See WBIP*, 829 F.3d at 1337 ("The real question is whether that skilled artisan would have plucked one reference out of the sea of prior art ... and combined it with [other] ... elements to address some need present in the field. ... Whether a skilled artisan would be motivated to make a combination includes whether he would select particular references in order to combine their elements."); *ActiveVideo Networks*, 694 F.3d at 1327 (finding expert's

testimony “conclusory and factually unsupported” where “[t]he expert failed to explain how specific references could be combined, which combination(s) of elements in specific references would yield a predictable result, or how any specific combination would operate or read on the asserted claims.”); *Qualcomm*, 24 F.4th at 1376-77 (holding that the basis of a ground in an IPR must rely on prior art patents or printed publications); Director Memorandum, “Enforcement and Non-Waiver of 37 C.F.R. § 42.104(B)(4) and Permissible Uses of General Knowledge in Inter Partes Reviews (July 21, 2025) (“[P]ast efforts by the Office to permit limited use of general knowledge to satisfy a missing claim limitation are no longer consistent with Federal Circuit precedent.”). Accordingly, Petitioner’s reliance on the general knowledge of a POSITA to supply a missing claim limitation is improper. Ex-2001, ¶ 77.

2. The Petition fails to show claim 5’s “forming a [first/second] capacitor on the semiconductor substrate so as to be connected in series with the [first/second] switch circuit between the [first/second] switch circuit and the antenna node” is obvious over Seshimo in view of a POSITA’s knowledge

As explained in the Huang ground, claim 5 requires “a semiconductor substrate” with a “first switch circuit,” “second switch circuit,” “first capacitor,” and “second capacitor” formed on “*the* semiconductor substrate.” Ex-1001, cl. 5 (emphasis added). As the ’194 patent specification explains, the claimed inhibiting

capacitors can be “part of the same semiconductor die” as the transistors, as recited in claim 5, rather than, in alternative unclaimed embodiments, “part of a second die mounted on the packaging substrate” or “at a location outside the semiconductor die.” Ex-1001, 2:15-21; Ex-2003, 131:21-133:14. Ex-2001, ¶ 79.

The Petition treats Seshimo also as disclosing all these elements on the same semiconductor substrate. *See* Petition, 66 (“Seshimo discloses ...”). However, Seshimo is silent as to whether its capacitors in the Figure 3 circuit are on the same die as the other components. The Petition again generally relies on the State of the Art, citing to a string of references. Petition, 66-67 (“To the extent PO asserts that Seshimo does not explicitly disclose ...”). But a petitioner may request to cancel claims “only on the basis of prior art consisting of patents or printed publications.” 35 U.S.C. § 311(b). The “general knowledge, skill, and creativity of a POSITA” is not a patent or printed publication. *Id.*; *see also Qualcomm*, 24 F.4th at 1376-77 (holding that the basis of a ground in an IPR must rely on prior art patents or printed publications); Director Memorandum, “Enforcement and Non-Waiver of 37 C.F.R. § 42.104(B)(4) and Permissible Uses of General Knowledge in Inter Partes Reviews (July 21, 2025) (“[P]ast efforts by the Office to permit limited use of general knowledge to satisfy a missing claim limitation are no longer consistent with Federal

Circuit precedent.”). Accordingly, Petitioner’s reliance on the general knowledge of a POSITA to supply a missing claim limitation is improper. Ex-2001, ¶ 80.

Moreover, as explained in the Huang ground, whether the claim elements were known in prior art references cannot be the end of the obviousness analysis. *WBIP*, 829 F.3d at 1337 (“The real question is whether that skilled artisan would have plucked one reference out of the sea of prior art ... and combined it with [other] ... elements to address some need present in the field. ... Whether a skilled artisan would be motivated to make a combination includes whether he would select particular references in order to combine their elements.”); *ActiveVideo Networks*, 694 F.3d at 1327 (finding expert’s testimony “conclusory and factually unsupported” where “[t]he expert failed to explain how specific references could be combined, which combination(s) of elements in specific references would yield a predictable result, or how any specific combination would operate or read on the asserted claims.”).

A POSITA could choose off-die capacitors over on-die capacitors. Like Huang, the stated goal of the capacitors in Seshimo is to reduce insertion loss. Ex-1007, ¶¶ 4, 7. A POSITA implementing Seshimo would also have been motivated to select capacitors to achieve better insertion loss. As explained above, a POSITA would have been motivated to implement the capacitors in Seshimo off-die where

they could be larger and achieve better insertion loss. Again, the Petition does not consider insertion loss, one of Huang's objectives, but simply asserts "design choice" and "cost." Petition, 66-67. And again, Petitioner's expert's declaration on this issue nearly matches the Petition verbatim and should be given little weight. *Compare* Petition, 61-62, with Ex-1003, ¶¶ 146-147. *Xerox Corp.*, IPR2022-00624, Paper 9, 15 (PTAB Aug. 24, 2022) (expert declaration that "merely repeats, verbatim, the conclusory assertion for which it is offered to support" without citing "any additional supporting evidence or provide any technical reasoning to support" is entitled to little weight). Ex-2001, ¶ 80.

3. Dependent Claims

Because dependent claim 6 depends from independent claim 5, claim 6 would not have been obvious over Seshimo in view of a POSITA's knowledge for the same reason as claim 5 as explained above. The Petition fails for the same reason. Ex-2001, ¶ 81.

Dependent claim 8 would not have been obvious over Seshimo in view of a POSITA's knowledge for the same reason as dependent claim 2 because claim 8 also requires "at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental frequency signal in the switch," as explained above. The Petition fails for the same reason. Ex-2001, ¶ 82.

Dependent claim 9 would not have been obvious over Seshimo in view of a POSITA's knowledge for the same reason as independent claim 5 for requiring the "first capacitor" to be "part of the same semiconductor die as the first switch," as explained above. The Petition fails for the same reason. Ex-2001, ¶ 83.

Dependent claim 10 would not have been obvious over Seshimo in view of a POSITA's knowledge for the same reason as independent claim 5 for requiring the "first capacitor" be "part of a second die," which is not the same die as the semiconductor die where the first switch is formed. The Petition fails for the same reason. Ex-2001, ¶ 82.

VII. CONCLUSION

Petitioner has failed to meet its burden to demonstrate that the challenged claims are unpatentable in view of the asserted references. As such, Patent Owner respectfully requests that the Board confirm the patentability of the challenged claims.

Dated: September 23, 2025

Respectfully submitted,

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PATENT OWNER'S TABLE OF EXHIBITS

Exhibit	Description
2001	Declaration of Dr. David Wentzloff
2002	CV of Dr. David Wentzloff
2003	Deposition Transcript of Dr. Larson
2004	Certified English Translation of Japanese Patent Publication No. JP 2006-121217 (Ex-1006)
2005	McGraw-Hill Dictionary of Electrical and Computer Engineering (6 th Ed. 2003)

CERTIFICATE OF SERVICE

I hereby certify that, on September 23, 2025, I caused a true and correct copy of:

- Patent Owner's Response Pursuant to 37 C.F.R. § 42.107
- Certificate of Word Count
- Patent Owner's Table of Exhibits
- Exhibits 2001-2005

to be served via electronic mail on the following attorneys of record:

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CERTIFICATE OF WORD COUNT UNDER 37 C.F.R. § 42.24(d)

I hereby certify that the foregoing Patent Owner's Response contains 10,705 words, including text-based images, as measured by the word-processing software used to prepare the document, in compliance with 37 C.F.R. § 42.24(d).

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Date: September 23, 2025