

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KANGXI COMMUNICATION TECHNOLOGIES (SHANGHAI) CO., LTD.
Petitioner,

v.

SKYWORKS SOLUTIONS, INC.
Patent Owner.

Case No. IPR2024-01457
U.S. Patent No. 9,148,194

**DECLARATION OF DR. DAVID WENTZLOFF REGARDING
CLAIMS 1-11 OF U.S. PATENT NO. 9,148,194**

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I, David Wentzloff, Ph.D., declare as follows:

I. INTRODUCTION

1. My name is David Wentzloff.

2. I am making this declaration at the request of Skyworks Solutions (“Skyworks” or “Patent Owner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office and to provide testimony pertinent to the Patent Owner’s Response for *Inter Partes* Review of U.S. Patent No. 9,148,194 (“’194 patent”). I understand that Kangxi Communication Technologies (“KCT” or “Petitioner”) challenged the patentability of claims 1-11 of the ’194 patent.

II. QUALIFICATION AND EXPERIENCE

3. My qualifications and publications are stated more fully in my curriculum vitae, which is Ex-2002. Below is a summary of my education, work experience, and other qualifications.

4. I received a Bachelor of Science in Electrical Engineering from the University of Michigan in 1999, and a Master of Science and Ph.D. in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology, in 2002 and 2007, respectively.

5. Throughout the course of my education and professional career, including in my work leading to my B.S., M.S., and Ph.D. degrees, I have been

involved in the design and fabrication of RF, analog, and mixed-signal integrated circuits (IC) and the applications they enable in communications, sensing, and power management, as well as other applications. For example, as a part of my work leading to my B.S. degree, I focused on analog integrated circuits as my area of concentration, which included courses in discrete circuits, electromagnetics, CMOS and Bipolar transistors, and integrated circuits. This included a capstone design course that was titled Monolithic Amplifier Circuits, which covered analog IC design with a design project. Similarly, as a part of my work leading to my Ph.D., I took every graduate-level analog and digital circuits course that MIT offered at that time. This included courses in both analog IC design and RF IC design, which covered amplifiers, biasing, and power amplifiers among other subjects. My Ph.D. thesis at MIT was titled Pulsed-Based Ultra-Wideband Transmitters for Digital Communication. In this thesis, I examined novel RF IC designs for wideband transmitters, and fabricated a number of chips in Bipolar and CMOS processes to demonstrate these techniques.

6. Since August 2007, I have been with the University of Michigan, Ann Arbor, where I am currently a Professor of Electrical Engineering and Computer Science. My research continues to focus on RF integrated circuits for wireless communication applications. This includes the study of novel circuit designs for RF

ICs that achieve better performance, energy efficiency, or higher levels of integration. My group has fabricated dozens of RF chips to prototype these designs and characterize their performance with measured results. These results have been published in over 100 peer-reviewed conferences and journals. I have advised and graduated twenty-five Ph.D. students since 2007, and currently advise ten Ph.D. candidates in my research group, all of whom are focused on RF IC design. I teach circuits classes ranging from introductory-level circuits to graduate level analog and RF IC courses.

7. I received numerous honors and awards for my work in this field. These have included the 2009 DARPA Young Faculty Award, 2009-2010 Eta Kappa Nu Professor of the Year Award, 2011 DAC/ISSCC Student Design Contest Award, 2012 IEEE Subthreshold Microelectronics Conference Best Paper Award, the 2012 NSF CAREER Award, the 2014 ISSCC Outstanding Forum Presenter Award, the 2014-2015 Eta Kappa Nu ECE Professor of the Year Award, the 2014-2015 EECS Outstanding Achievement Award, the 2015 Joel and Ruth Spira Excellence in Teaching Award, the ECE Innovator Award for the startup company SkyGig in 2018, the 2020 IEEE Custom Integrated Circuits Conference (“CICC”) Outstanding Invited Paper Award, the 2023 IEEE International Conference on Synthesis, Modeling, Analysis and Simulation Methods, and Applications to Circuit Design

(“SMACD”), Best Paper Award, and the University of Michigan Faculty Recognition Award in 2024. I have served on the technical program committee for the IEEE’s International Conference on Ultrawideband (“ICUWB”) from 2008-2010, the IEEE/ACM International Symposium on Low Power Electronics and Design (“ISLPED”) from 2011-2015, The IEEE’s S3S Conference from 2013-2014, the IEEE’s Radio Frequency Integrated Circuits (“RFIC”) Symposium from 2013-2022, and the IEEE’s International Solid-State Circuits Conference (“ISSCC”) from 2020-2022. I have also served as a guest editor for the IEEE’s peer reviewed journal Transactions on Microwave Theory and Techniques (“T-MTT”), the IEEE Communications Magazine, and the Elsevier Journal of Signal Processing: Image Communication. I am a senior member of IEEE, IEEE Circuits and Systems Society, IEEE Microwave Theory and Techniques Society, IEEE Solid-State Circuits Society, and the Tau Beta Pi engineering honors society.

8. In 2012, I co-founded Everactive, Inc. to commercialize self-powered Internet of Things (IoT) sensors based on ultra-low power wireless system-on-chip (“SoC”) solutions. *See* <https://everactive.com/>. Throughout my teaching, research, and entrepreneurship experiences, I have had extensive experience in the design and fabrication of RF and analog integrated circuits. For example, I have evaluated hundreds of student design projects in analog IC courses and assessed their

functionality and performance. Together with my research group, I have designed dozens of RF IC prototypes including the world's lowest power Bluetooth transmitter, the smallest fully-integrated transceiver, receivers for cellular commutation in GSM, 3G, 4G, and recently 5G satellite communication, and WiFi wakeup receivers. These have used CMOS or Bipolar processes, and have been fully characterized in my lab at the University of Michigan. Moreover, through my work at Everactive, I have commercialized certain of these technologies into production-level designs that are now being shipped in industrial IoT products.

III. PRIOR TESTIMONY AND COMPENSATION

9. I have provided expert reports and testimony for Skyworks to the United States International Trade Commission in Investigation No. 337-TA-1413. That case involved the same parties as this proceedings, Skyworks and KCT. The opinions I offered in that Investigation were not for the '194 patent.

10. I am being compensated for my time at my standard consulting rate of \$650 an hour plus expenses. My compensation is not dependent upon the conclusions expressed in this report or on the outcome of this proceeding.

IV. LEGAL PRINCIPLES

11. I am not an attorney. For the purposes of this declaration, I have been informed about certain aspects of the law that may be relevant to my opinions

concerning the validity of the '194 patent. My understanding of the law is set forth below.

A. Patent Claim

12. I have been informed and understand that a patent's claims define the invention made by the inventors and describe what the patent owner owns. I understand that claims may describe products, such as chips or circuits inside a chip, or processes and methods for making or using a product. I understand that claims are usually have several elements or steps called limitations. I understand that every claim term has to have a meaning.

13. I have been informed and understand that a patent may include independent and dependent claims. An independent claim is a standalone claim that includes only the limitations it recites. A dependent claim includes all the limitations that it recites plus all the limitations recited in the claim(s) from which it depends.

14. I have been informed and understand that an issued patent is presumed valid. I have been informed and understand the petitioner of an *inter partes* review bears the burden of proving whether the challenged claims are invalid through facts supported by a preponderance of the evidence and that "preponderance of evidence" means evidence sufficient to prove that a fact is more likely true than not.

B. Prior Art

15. I have been informed and understand that a claimed invention is not patentable if the claimed invention was disclosed in “prior art.” I have been informed and understand that in IPR, only printed publications qualify as prior art.

C. Anticipation

16. I have been informed and understand that, to prove that a patent claim is invalid for anticipation, the petitioner must demonstrate by a preponderance of evidence that each and every element of the claim is disclosed, either expressly or inherently, in a single prior-art reference. I also understand that, for a disclosure to be inherent, the petitioner must prove by a preponderance of evidence that the limitation is necessarily present in the alleged prior art reference. Inherency cannot be established by mere probabilities or possibilities. I understand that it is petitioner’s burden to prove that every element in a claimed invention is found in the prior art, either expressly or inherently.

D. Obviousness

17. I have been informed and understand that a patent claim is invalid as obvious only if, at the time of the invention, the subject matter as a whole would have been obvious to a person of ordinary skill in the art before the effective filing date of the claimed invention. I have been informed that obviousness is based on a factual inquiry, and includes analyzing (i) the scope and content of the prior art, (ii) the differences between the prior art and the claim, (iii) the level of ordinary skill in

the art at the effective filing date of the claimed invention, and (iv) the existence of objective indicia of non-obviousness.

18. I have been informed and understand that a claimed invention can be found obvious over a single prior art reference or multiple prior art references.

I have been informed and understand that the petitioner cannot prove that a claim comprising multiple elements is obvious simply by showing that each element, independently, was known in the prior art. I also understand that the petitioner must articulate some reason or motivation that would have led a person of ordinary skill in the art to combine or modify the relevant teachings in the prior art to arrive at the claimed invention. I understand that the motivation to combine prior art references can come from the knowledge of those skilled in the art, from the prior art reference itself, or from the nature of the problem to be solved. I further understand that the mere fact that a person of ordinary skill in the art could combine the references is not sufficient. The petitioner must show that some reason or motivation existed that would have led a person of ordinary skill in the art to combine or modify the relevant teachings in the prior art to obtain the claimed invention. In addition, I understand that the petitioner must show that a person of ordinary skill in the art would have had a reasonable expectation of success in achieving the claimed combination based on the teachings of the prior art.

V. MATERIALS CONSIDERED

19. In forming my opinions, in addition to my knowledge and experience, I have considered the materials cited herein and listed in List of Materials Considered.

VI. THE '194 PATENT (EX-1001)

A. Overview of the Patent

20. The '194 patent describes an RF switch for reducing intermodulation distortion (IMD) in radio-frequency (RF) devices. Ex-1001, Title, Abstract. Intermodulation distortion (IMD) is a measure of how much an unwanted signal is added to a desired signal due to mixing products from other RF signals. Ex-1001, 8:55-57. Unwanted RF signals could come from various sources, including nearby RF transmitters operating at a similar frequency, which can introduce interference. External noise and RF signals can infiltrate the RF circuit and interact with transmitted signals, mixing with each other to produce unwanted signals. These unwanted RF signals collectively affect intermodulation distortion. The '194 patent explains that intermodulation distortion can be particularly problematic in “a multi-mode, multi-band environment” where intermodulation distortion “can result from two or more signals mixing together to yield frequencies that are not harmonic frequencies.” Ex-1001, 8:57-60, 6:49-51.

21. As background, radio-frequency (RF) signals are alternating current (AC) signals that fluctuate over time, whereas direct current (DC) signals remain

constant. In communication systems, a carrier wave—typically with a stable frequency—is used to modulate an underlying signal to transmit information. This carrier wave frequency is often referred to as the fundamental frequency. By modulating signals onto different fundamental frequencies, wireless devices can operate across multiple bands, which helps minimize interference.

22. In practice, signals at different frequencies can interfere with one another, degrading the quality of modulation. This is called intermodulation distortion. Ex-1001, 8:62-67. In multi-band environments, RF devices are exposed to signals across various frequencies. When two or more of these signals mix, they can generate frequencies that are not harmonically related, resulting in intermodulation distortion. Ex-1001, 6:15-16. The '194 patent illustrates this with an example where two signals with fundamental frequencies “that are relatively close to each other in frequency space” that can produce “peaks in frequency spectrum at frequencies corresponding to different products of fundamental and harmonic frequencies of the two signals.” Ex-1001, 6:17-27. When these two signals at different frequencies mix, it can generate undesired harmonics and intermodulation distortion, ultimately degrading the performance of the RF device. Ex-1001, 8:55-67.

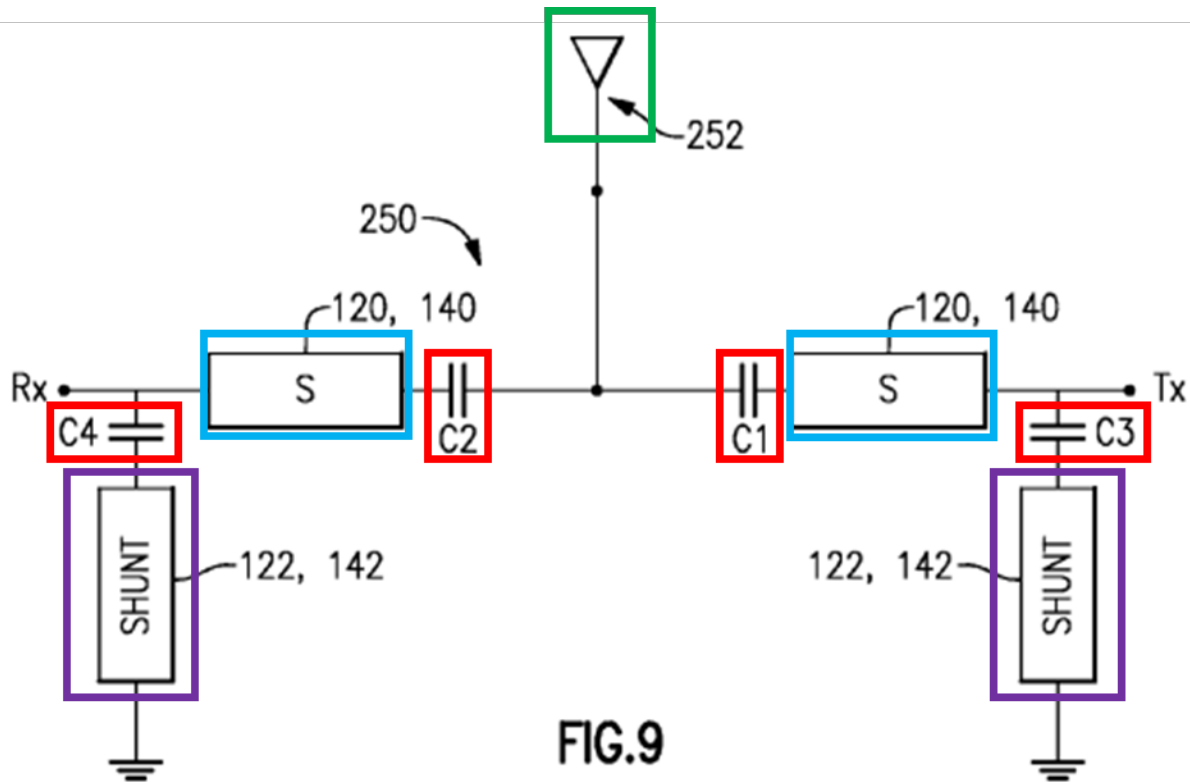
23. The '194 patent explains that intermodulation distortion can be reduced by improving linearity of the RF device. Ex-1001, 8:61-62, 6:12-13. Linearity in this context refers to an RF device that generates an output signal that is directly proportional to the input signal. On the other hand, non-linearity refers to an RF device in which a change in the input signal results in a non-proportional change in the output signal. The '194 patent identifies non-linearity in RF systems as a source of performance degradation. Specifically, it explains that non-linearity can introduce spurious signals into the system, leading to interference and compromising the integrity of the transmitted RF signals. Ex-1001, 6:33-38, 8:62-64 (“A given system’s linearity can govern how much IMD will occur within it, which in turn can create interferences.”). In other words, “[a]n RF system having increased non-linearity can demonstrate increased susceptibility to interference.” Ex-1001, 6:38-40. The patent explains that non-linearity in switching devices can degrade overall RF system linearity and IMD performance. Ex-1001, 6:40-44. Thus, by improving the linearity of the switch in the RF device, the “overall susceptibility of a system to interference can be decreased.” Ex-1001, 8:65-67.

24. The '194 patent addresses intermodulation distortion and non-linearity in RF devices by introducing a method of operation that includes, among other elements, “a first switch circuit connected between an antenna node and a transmit

node,” “a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node,” “a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node,” and “at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental frequency signal the RF switch.” Ex-1001, cls. 1-2. The capacitor, as described in the patent, is “connected in series with the switch and configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch” Ex-1001, 1:31-37, Abstract (“A capacitor connected in series with the switch is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.”). This feature is emphasized throughout the patent in 1:52-54, 1:65-67, 2:12-14, 2:32-34, and more.

25. Figure 9 of the '194 patent illustrates an example of an “RF switching configuration” that may include one or more capacitors designed to “inhibit a low-frequency blocker from mixing with a fundamental frequency.” Ex-1001, 3:1-4. Figure 9 shows “a single-pole-dual-throw (SPDT)” RF switch, where the single pole is connected to **antenna 252**. Ex-1001, 9:8-10. One of the two poles is connected to a receive (Rx) port via a switch circuit S. Ex-1001, 9:10-12. The other of the two poles is connected to a transmit (Tx) port via a **switch circuit S**. Ex-1001, 9:14-15.

Each pole is also connected to ground via a **shunt switch circuit SHUNT**. Ex-1001, 9:10-13, 9:15-16.



Ex-1001, Figure 9 (highlighted).

26. The exemplary switching configuration shown in the '194 patent incorporates **several capacitors** specifically chosen to “inhibit a low-frequency blocker from mixing with a fundamental frequency.” Ex-1001, 9:25-27. Capacitor C1 is placed between the antenna node and the switch arm of the Tx throw. Ex-1001, 9:27-29. Capacitor C2 is placed between the antenna node and the switch arm of the Rx throw. Ex-1001, 9:29-31. Capacitor C3 is placed between the Tx node

and its shunt switch arm. Ex-1001, 9:31-32. Capacitor C4 is placed between the Rx node and its shunt switch arm. Ex-1001, 9:32-34. The '194 patent includes these capacitors in this switching configuration because “[w]ith the foregoing capacitors, a low-frequency jammer signal can be blocked or reduced from mixing with any ON or OFF paths.” Ex-1001, 9:35-37. These capacitors “can lead to improvement in IMD performance, especially for low-frequency blocker signals.” Ex-1001, 9:37-39.

B. Challenged Claims

27. I understand that Petitioner challenges claims 1-11. Based on my reading of the '194 patent, claim 2 is representative and is reproduced below:

1. A radio-frequency (RF) Switch system comprising:

a first switch circuit connected between an antenna node and a transmit node;

a second switch circuit connected between the antenna node and a receive node;

a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node;

a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node;

a first shunt arm connected to the first switch circuit and the transmit node, the first shunt arm including a third switch circuit connected to ground; and

a second shunt arm connected to the second switch circuit and the receive node, the second shunt arm including a fourth switch circuit connected to ground.

2. The switch system of claim 1 wherein at least one of the first and second capacitors is configured to inhibit a low frequency blocker signal from mixing with a fundamental frequency signal in the switch.

VII. CLAIM CONSTRUCTION

28. I have been informed and understand that the words used in the patent's claims and the context in which the words are used in the claims are highly relevant in determining the meaning of the words. I also understand that the words of a claim are to be interpreted in the context of the entire patent, including the patent's claims, specification, and figures. I have been further instructed that, in general, a patent's prosecution history (also called the file history) may provide helpful evidence about how the U.S. Patent and Trademark Office and the applicant understood the patent and its claims. Therefore, I have been instructed that claims should also be interpreted with the patent's prosecution history in mind. I have also been instructed that "extrinsic evidence" (such as dictionaries, pertinent scientific or technical references, and expert opinion) may also help inform how a person of ordinary skill in the art would have understood a claim term. I have been instructed that extrinsic evidence must always be considered with intrinsic evidence and that intrinsic evidence has priority over extrinsic evidence.

29. I have been informed and understand that Petitioner and the Petitioner's expert Dr. Larson applied plain and ordinary meaning to interpret the challenged claims.

30. For the purposes of this IPR, I have also applied plain and ordinary meaning in view of the patent specification, file history, how I understand the claim terms are used in the field, including my own experience and knowledge. However, if Petitioner later proposes construction for any claim term, I reserve the right to respond to that construction. I also reserve the right to propose an express construction consistent with the term's plain and ordinary meaning, if needed.

VIII. LEVEL OF ORDINARY SKILL IN THE ART

31. I have been informed and understand that when considering validity of the claims of the '194 patent and Petitioner's asserted prior art, I must do so from the perspective of one of ordinary skill in the art as of the '194 patent's effective priority date.

32. I have been informed and understand that Petitioner and Dr. Larson proposes the following definition: "[a] POSITA in July 2012 would have been someone knowledgeable and familiar with RF electronics, including RF switches and electrical components of such switches, and semiconductor manufacturing processes. POSITAs would have gained knowledge of these concepts through a

mixture of training and work experience, such as by having a Bachelor's degree in electrical engineering, or related field, and approximately two to three years of related experience; or by obtaining a Master's degree in electrical engineering, or related field, but having only a year of related experience; or by having no formal education but experience in RF electronics and semiconductor packaging of at least six to eight years.” Ex-1003, ¶¶ 47-50. I agree with this definition except for the last qualification “by having no formal education but experience in RF electronics and semiconductor packaging of at least six to eight years.” The RF electronics and semiconductor field is broad with people working in many different roles, and without circuit background (either from academics or self-taught), one may not have the adequate level of skill to analyze circuits related to this case.

IX. SCOPE AND CONTENT OF THE ASSERTED PRIOR ART

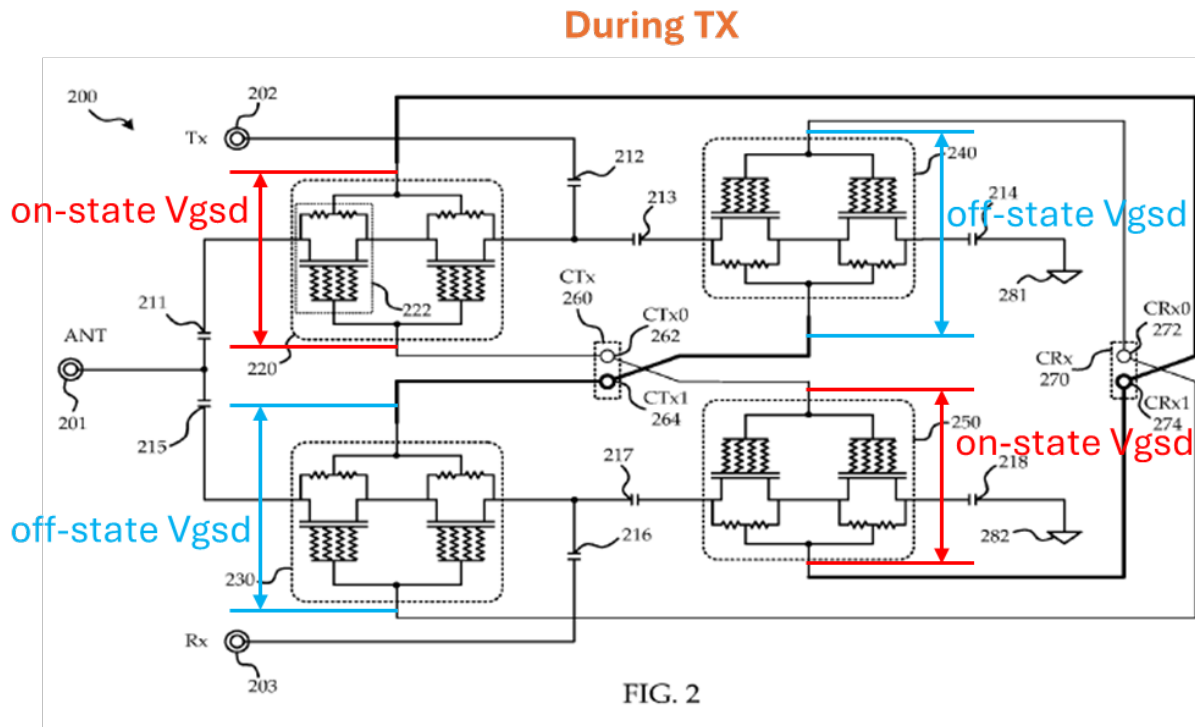
33. I understand that the Petition relies on Huang for the first ground and Seshimo for the second ground. I read both references. Huang and Seshimo both describe improvements to DC biasing of transistors in an RF switch circuit.

A. U.S. Pub No. 2011/0254614 to Huang (Ex-1005)

34. I understand that the Petition asserts Huang as a primary prior art reference in Ground 1.

35. Huang is about “biasing transistor switches in a semiconductor based high power switch” by biasing “off-state V_{gs} ” (or “off polarity” or “reverse

polarity”) less than “on-state V_{gsd} ” (or “on polarity” or “forward polarity”) Ex-1005, Abstract, ¶¶ 15-18. Below, using Figure 2 of Huang, I highlight what Huang refers to as “off-state V_{gsd} ” and “on-state V_{gsd} ”:



Ex-1005, Fig. 2 (annotated). Huang states that it achieves “low insertion loss and high isolation” of a RF switch by selecting “particular voltages” for the off-state V_{gsd} and on-state V_{gsd} of the transistors in the switch, less than conventional full bias voltage. Ex-1005, ¶ 39. For example, Huang suggests using 1.1-1.5V for the off-state V_{gsd} and 2.0-2.5V for the on-state V_{gsd} . Ex-1005, ¶¶ 42-43:

[0042] The spurious third harmonic emissions has a more steep slope versus power drive than that of the spurious second harmonic emissions, but both kinds of spurious harmonic emissions increase with increasing off-state

V_{gsd} beyond a certain bias voltage. Nonlinear effects in the high power switch were also found to increase with increasing off-state V_{gsd} of the off-state FET group switches. For a 2.5 V SOI, low levels of harmonic emissions and sufficient linearity, were found at off-state V_{gsd} of 1.5 V and less where the channel linking the source and drain is not in strong inversion. Considering the need for isolation, the operating off-state V_{gsd} level for the turned off FET group switches is chosen to be 1.1 V-1.5 V. In general, the off-state V_{gsd} level should be determined after an acceptable upper limit to the spurious harmonic emissions and an acceptable lower limit of linearity have been identified. Such identification will of course depend upon the application in which the switch is to be used. The identification of these limits allows reduction of the magnitude of the off-state V_{gsd} by only the amount required to meet the spurious harmonic and linearity requirements, and hence keeping as much of the benefits of higher isolation that large off-state V_{gsd} provides in comparison with off-states achieved by zero biasing or very small biasing of an on polarity. Higher isolation is achieved by using a significant off-state V_{gsd} level, since the off-state switch is then able to isolate larger amplitude signals to a greater degree than switches applied with a small or insignificant off-state V_{gsd}.

[0043] For the on-state FET group switches, lower harmonic emissions were found above a voltage level close to the gate to source breakdown voltage. With the 2.5V SOI technology, 2.0-2.5 V of on-state V_{gsd} was found to exhibit a very low insertion loss, and good linearity. Considering the reliability constraint of 2.5 V, the operating on-state V_{gsd} level for the turned on FET group switches is chosen to be 2.0 V-2.5 V.

Ex-1005, ¶¶ 42-43.

36. These two paragraphs explain the core of Huang's teaching. Huang teaches that linearity in a switch device can still be achieved by choosing 1.0-1.5V for the off-state V_{gsd} and 2.0-2.5V for the on-state V_{gsd} instead of fully biasing transistors on/off. Ex-1005, ¶ 42 ("The identification of these limits allows reduction of the magnitude of the off-state V_{gsd} *by only the amount required* to meet the spurious harmonic and linearity requirements, and hence keeping as much of the benefits of higher isolation that large off-state V_{gsd} *provides in comparison with off-states achieved by zero biasing* or very small biasing of an on polarity") (emphasis added). Referring to the figure above, during transmit, Huang suggests to use 2.0 V-2.5 V for the node CTx0 (262) and 1.0-1.5V for the node CTx1 (264), even though that is less than "the largest possible bias." Ex-1005, ¶¶ 40-43.

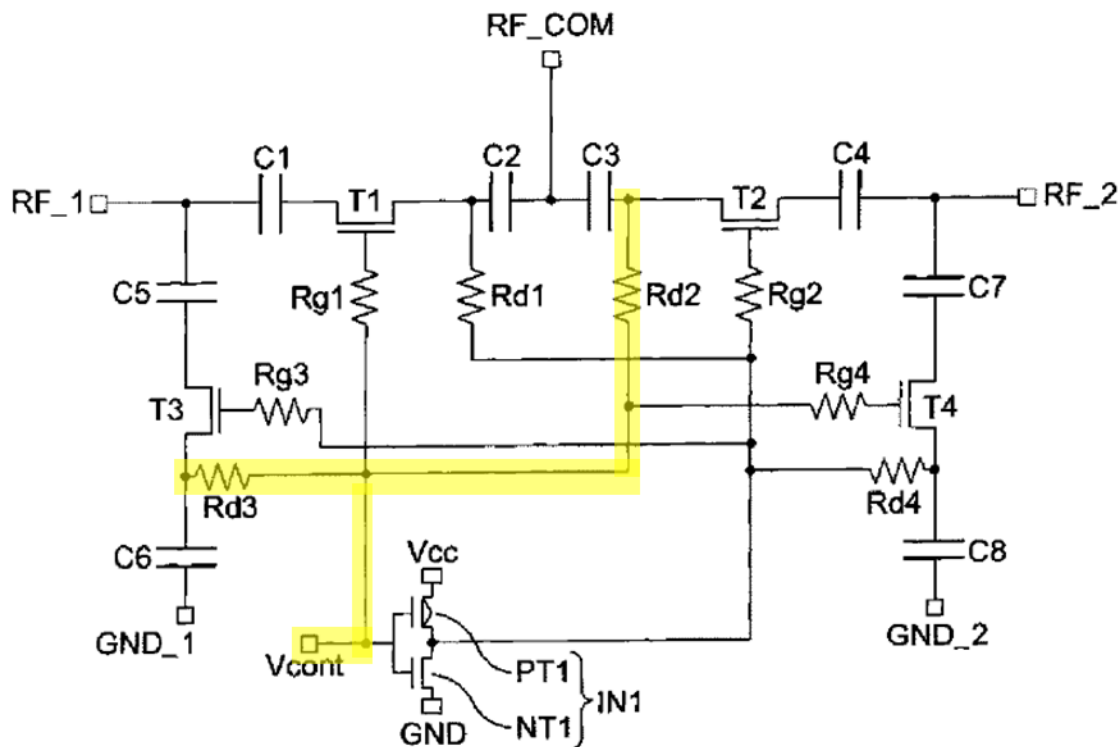
37. Huang further discloses that "[g]roups of FETs are arranged in the switch along with judiciously chosen resistors and capacitors to ensure low insertion loss along the signal path and high isolation along from the off paths." Ex-1005, ¶ 3. Figure 2 depicts those "blocking capacitors" 211-218 placed in series with switches 220, 230, 240, and 250. Ex-1005, ¶¶ 44-45. These blocking capacitors are DC blocking capacitors that enables using independent on-state and off-state biasing voltages (e.g., 2.0 V-2.5 V and 1.0-1.5V, respectively) for each of the transistors, and improves linearity, which Huang purports to achieve.

38. Huang does not use the term low frequency, low frequency blocker signal, fundamental frequency, or intermodulation distortion.

B. JP 2006-121217 to Seshimo (Ex-1006; Ex-1007 for translation)

39. Seshimo is also about DC biasing of transistors in a RF switch circuit to “enhance maximum permissible input power and suppress an increase in On-resistance.” Ex-1007, Abstract. Seshimo’s transistor biasing is similar to Huang, but simpler. Seshimo biases one of the source or the drain of each transistor as shown below:

FIG. 3



Ex-1007, Fig. 3 (highlighted).

40. Seshimo states that its objective is “to provide a semiconductor switching circuit capable of improving the maximum permissible input power while suppressing an increase in ON-resistance.” Ex-1007, ¶ 7. In a high-frequency switch circuit with MOSFETs (one type of transistors) formed on a silicon substrate, the substrate’s resistance and transistor’s ON-resistance (the resistance of the transistor itself when it is on and passing the RF signals) causes insertion loss, which degrades signal quality. Ex-1007, ¶ 4. Seshimo claims that its biasing scheme can keep the ON-resistance low and still allow higher input power. Ex-1007, ¶ 7

X. PETITIONER FAILS TO SHOW THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE.

41. I disagree with Dr. Larson’s opinion that the grounds asserted in the Petition demonstrate that the challenged claims are unpatentable. In my view, the evidence presented does not sufficiently support a finding of unpatentability for the challenged claims.

A. The Challenged Claims Would Not Have Been Obvious Over Huang (Ground 1)

42. Dr. Larson opines that Huang in view of a POSITA’s knowledge renders obvious the challenged claims. I disagree. Huang only discloses DC blocking capacitors, which are not “configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” Huang does not mention anything about the intermodulation distortion problem and not how ’194

patent solves such problem. Huang also does not disclose that the capacitors Dr. Larson identifies are necessarily on the same substrate as the rest of the switch circuit. Dr. Larson recognizes this weakness in Huang and asserts that the claims would have been obvious over Huang in view of the knowledge of a person of ordinary skill in the art but does not articulate why a person of ordinary skill in the art would have been motivated to modify Huang.

1. The Petition fails to show claim 2’s “at least one of the first and second capacitors configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch” is obvious over Huang in view of a POSITA’s knowledge

43. Claim 2 requires “at least one of the first and second capacitors configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” As explained in Section VI.A, the ’194 patent explains that this claimed feature improves intermodulation distortion of a RF switch. *E.g.*, Ex-1001, 9:35-38.

44. Dr. Larson asserts that “blocking capacitor 211” from Huang’s Figure 2 “discloses” the claimed capacitors. Ex-1003, ¶ 92 (citing Ex-1005 ¶ 45). However, he fails to provide any evidence that “blocking capacitor 211” in Huang is “configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch” as required by this claim element. *See*

Ex-1003, ¶¶ 92-101. Dr. Larson does not identify any disclosure in Huang of a “low-frequency blocker signal” or a “fundamental frequency signal,” nor does he show any “mixing” of such signals. *See* Ex-1003, ¶¶ 92-101. In fact, Huang never uses the term “low frequency” in its disclosure because, as it does not address the intermodulation distortion problem that the ’194 patent solves.

45. Dr. Larson puts together pieces from several paragraphs of Huang to suggest that the size of capacitor 211 could be selected to perform inhibiting a low-frequency blocker signal from mixing with a fundamental-frequency. Ex-1003, ¶ 94. For example, Dr. Larson states that “Huang also discloses the importance of selecting the ‘arrange[ment]’ of ‘groups of FETs’ and ‘judiciously chosen ... capacitors’, and of selecting the biasing voltages of the FETs when in ‘on’ and ‘off’ states, in ‘a high power transmit-receive switch using ... SOI’ to achieve, for example, ‘low insertion loss along the signal path’, ‘high isolation from the off paths’, ‘reduce[d] spurious harmonic emissions’, and ‘improve[d] linearity’ for the switch.” Ex-1003, ¶ 94 (citing Ex-1005, ¶¶ 2-3, 39-40, 43-45, 55-59). But none of those paragraphs says that the size of blocking capacitor 211 can be used to inhibit any low frequency blocker signal from mixing with a fundamental-frequency signal. And Dr. Larson does not explain that Huang’s disclosure of “judiciously chosen resistors and capacitors to ensure low insertion loss along the signal path and high

isolation from the off paths” is the same as “configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” *See* Ex-1003, ¶ 94.

46. Dr. Larson does not contend that capacitor 211 is inherently configured to “inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal.” As I understand it, establishing “inherency” in patent analysis requires a high standard—the feature must necessarily be present in the reference. Dr. Larson’s silence is therefore unsurprising. Dr. Larson alleges that Huang’s “blocking capacitor 211” “allow high frequencies to pass through” “while blocking low frequencies” because that is what a capacitor does. Ex-1003, ¶ 95 (citing Ex-1005, ¶ 51). However, Huang focuses on DC biasing of switches to enhance linearity, which is a fundamentally different approach from that of the ’194 patent. Consequently, the capacitors in Huang are not configured the same as recited in claim 2. Specifically, Huang’s blocking capacitor 211 is used to block DC signals, not low-frequency signals, as explained further below. Thus, it does not inherently perform the claimed function.

47. Despite the deficiencies in Huang’s disclosure, Dr. Larson opines that “Huang discloses this limitation to POSITAs.” Ex-1003, ¶ 92. However, as previously discussed, Huang never uses the term “low frequency” and makes no

reference to a “low-frequency blocker signal,” let alone to “configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” Huang also does not mention intermodulation distortion. Instead, Huang merely labels capacitor 211 as a “blocking capacitor,” and Dr. Larson relies on that label to conclude that a POSITA would interpret it is configured to inhibit a low-frequency blocker signal. But a POSITA would understand that capacitor 211 in Huang is a DC blocking capacitor—not one intended to inhibit low-frequency blocker signals. The core of Huang’s invention relies on independently setting the DC bias voltages for the transistors, therefore a DC blocking capacitor is used to separate those DC signals to achieve this goal.

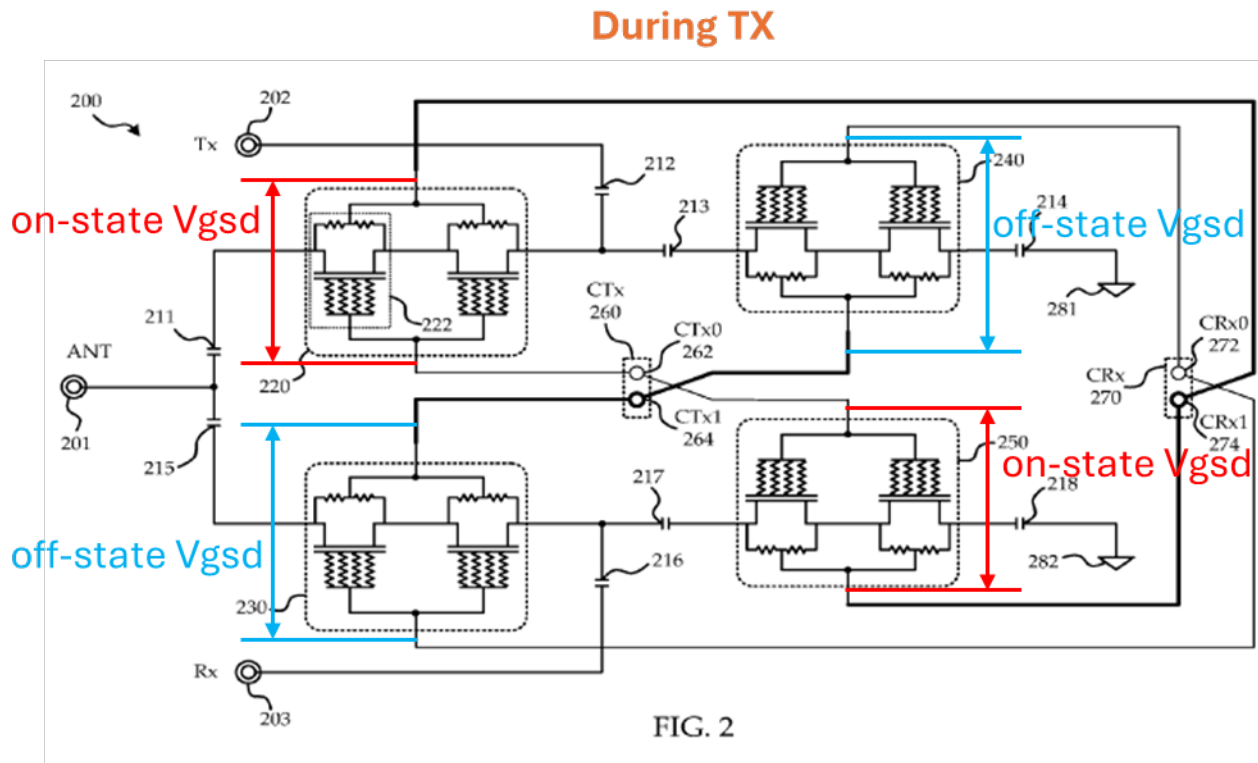
48. A “low-frequency blocker signal” is different from a DC signal. Low frequency signal refers to AC signals including RF signals at unwanted frequencies. In most cases, “low-frequency” is actually a frequency much higher than DC signals. In contrast, DC is at a frequency of zero Hz. Ex-2003, 59:4-10 (“Q. And a DC signal has no frequency because it's flat, it doesn't change with time as you said, right? A. DC doesn't change with time. Sometimes people might say DC is equivalent to 0 hertz and sometimes you'll see that in the literature, but it's essentially unchanging with time.”). Low frequency signals are AC signals with its amplitude changing over time. Ex-2003, 57:14-22 (“Q. Got it. So AC stands for -- I think it’s

short for alternating current and so it changes over time. Did I get that right? A. Yes, alternating current changes over time. Q. And then DC doesn't change over time and that's what distinguishes it from AC? A. Yes, yes. The assumption is that DC does not change ever.”). Thus, inhibiting a low-frequency blocker signal from mixing with a fundamental frequency is also not the same as DC blocking. Blocking DC is blocking signals at 0 Hz frequency. Low frequency blocker signals are AC signals, often RF signals at another fundamental frequency for a different switch, for example. Ex-2003, 59:11-60:23 (“A. ... Especially in the RF context, it can be a little bit of a gray area, DC. And in an RF context, it would just refer to something that's, like, at such a low frequency it's way below the signal of interest.”). The '194 patent explains intermodulation distortion results from mixing signals with different fundamental frequencies—that is, when mixing two AC signals. Ex-1001, 6:15-32.

49. Dr. Larson also agrees that transistors are biased with a DC bias voltage. Ex-2003, 59:11-14 (“Q. And so then you said when you’re biasing these MOSFET transistors, you want to bias them with a DC bias signal, right? A. You have to bias them with DC, yes.”). I reviewed Huang’s full disclosure, and it is apparent that blocking capacitor 211 serves solely as a DC blocking capacitor in Huang to isolate the DC bias voltages. That is because Huang is directed to “biasing transistor switches in a semiconductor based high power switch” by biasing “off-

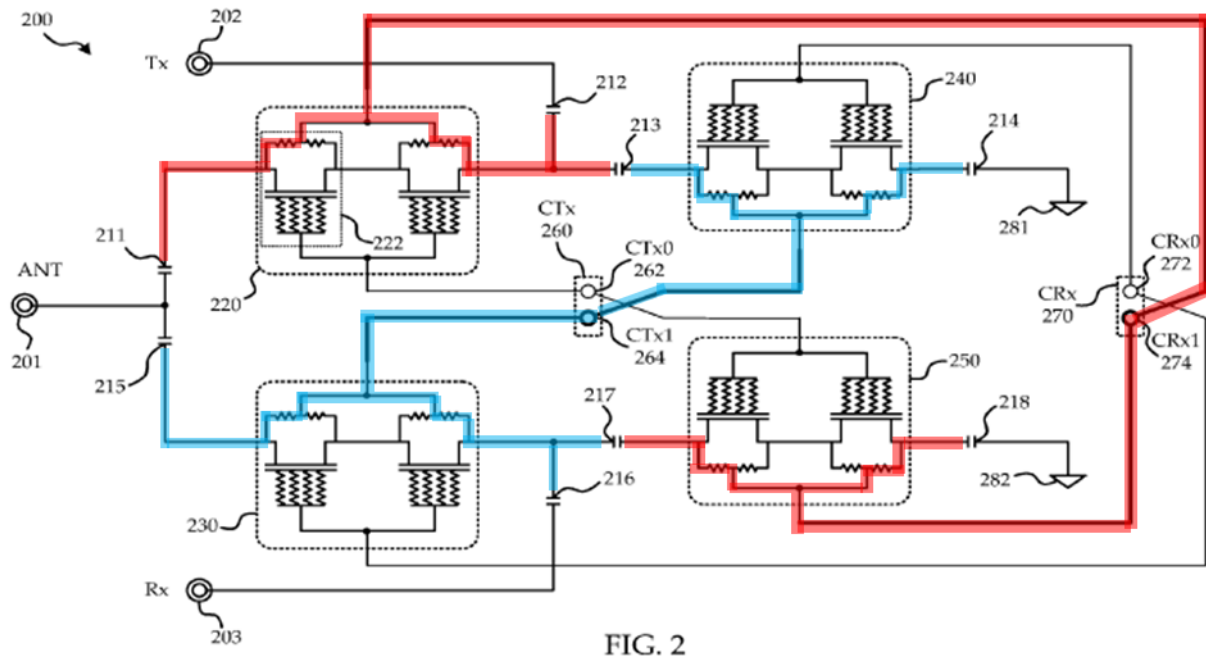
state V_{gsd} ” less than “on-state V_{gsd} .” Ex-1005, Abstract, ¶¶ 15-18. Huang explicitly states that its invention achieves “low insertion loss and high isolation” by selecting specific voltages for the off-state and on-state bias voltages, V_{gsd} , of transistors within a switch circuit. Ex-1005, ¶ 39. In circuits with multiple transistors (such as MOSFETs or MultiGate FETs (MUGFETs)) in series, Huang teaches that signal quality can be improved by biasing each transistor at a voltage level below its maximum possible bias voltage. Ex-1005, ¶ 40 (“improved signal quality is obtained from biasing the FETs at a level other than at the largest possible bias within the reliability/breakdown limits of operation”). Huang teaches that for the on-state, the V_{gsd} should be biased at a voltage slightly less than the maximum breakdown voltage to provide lower harmonic emissions while staying within the reliability limits of the transistors. For example, Huang recommends using 1.1–1.5V for the off-state V_{gsd} and 2.0–2.5V for the on-state V_{gsd} (the off-state is biased at a lower voltage than the on-state) instead of fully biasing on and off (e.g., off-state close to 0V and on-state close to 2.5V). Ex-1005, ¶¶ 42-43. As explained above, the term V_{gsd} refers to the voltages between the nodes highlighted in the figure below during transmission when switches 220 and 250 are on and switches 230 and 240 are off. Ex-1005, ¶ 57. Conversely, during reception when switches 220 and

250 are off and 230 and 240 are on, on-state and off-state annotated in the figure are switched. Ex-1005, ¶ 58.



Ex-1005, Fig. 2 (annotated). Dr. Larson seems to agree that the teachings of Huang is how to better bias each of transistors (MUGFETs). Ex-2003, 72:4-13 (“Q. And the focus of Huang is how to individually bias each of these MuGFET groups to improve the performance of the SPDT switch, right? A. Well, I mean, Huang certainly talks an awful lot about that. I think generally, you know, the purpose of Huang is to, you know, basically build a better switch. But certainly a lot of -- a lot of design goes into the bias of these switches in this patent.”).

50. Figure 2 depicts blocking capacitors 211-218 placed in series with switches 220, 230, 240, and 250. Ex-1005, ¶¶ 44-45. Blocking capacitors 211-218 “isolate” the V_{gsd} bias voltages, specifically for the drain and source terminals of each of the MUGFETs to allow each transistor to be biased independently. For example, blocking capacitors 211, 212, and 213 block DC signals that could otherwise raise or lower the bias voltages of the transistors in switch 220, enabling the drain and source of 220 to be set independent of other DC bias voltages. Because these capacitors are also in series with the desired RF signal, they can impact its amplitude. Huang refers to this phenomena as insertion loss and discloses that the values of the blocking capacitors should be “judiciously chosen” to minimize insertion loss. Ex-1005, ¶ 3. As explained above, Huang uses carefully selected DC bias voltage levels—e.g., 1.0-1.5 V for off-state and 2.0-2.5 V for on-state—to individually bias the groups of transistors, which differed from conventional biasing. The DC blocking capacitors are important here to individually bias the groups of transistors. As illustration, in Figure 2 below, I highlighted DC signal path in red and blue to show how blocking capacitors 211-218 isolate the red DC path from the blue DC path and to individually bias transistors in switches 220-250. Each of the capacitors 211-218 in Huang were included only to protect and isolate the bias voltages of the transistors in switches 220-250.



Ex-1005, Fig. 2 (highlighted).

51. The role of DC blocking capacitors in Huang becomes even more evident when considered in the context of the prior art it seeks to improve. In the background section, Huang outlines a conventional method involving a series of transistors in an RF signal path, where the gate and source/drain terminals are biased to fully switch the transistors on or off. Ex-1005, ¶ 3. As an example, Huang references Nakatsuka (Ex-1013). Ex-1005, ¶ 4. Figure 1A of Huang, which is from Nakatsuka, illustrates **biasing terminal 111** connected to the gates of transistors 122 in switch 120, as well as to the source/drain terminals of unlabeled transistors in switch 130. A second **biasing terminal, 112**, connects to the source/drain terminals

of transistors 122 in switch 120 and to the gates of the unlabeled transistors in switch 130, as shown below.:

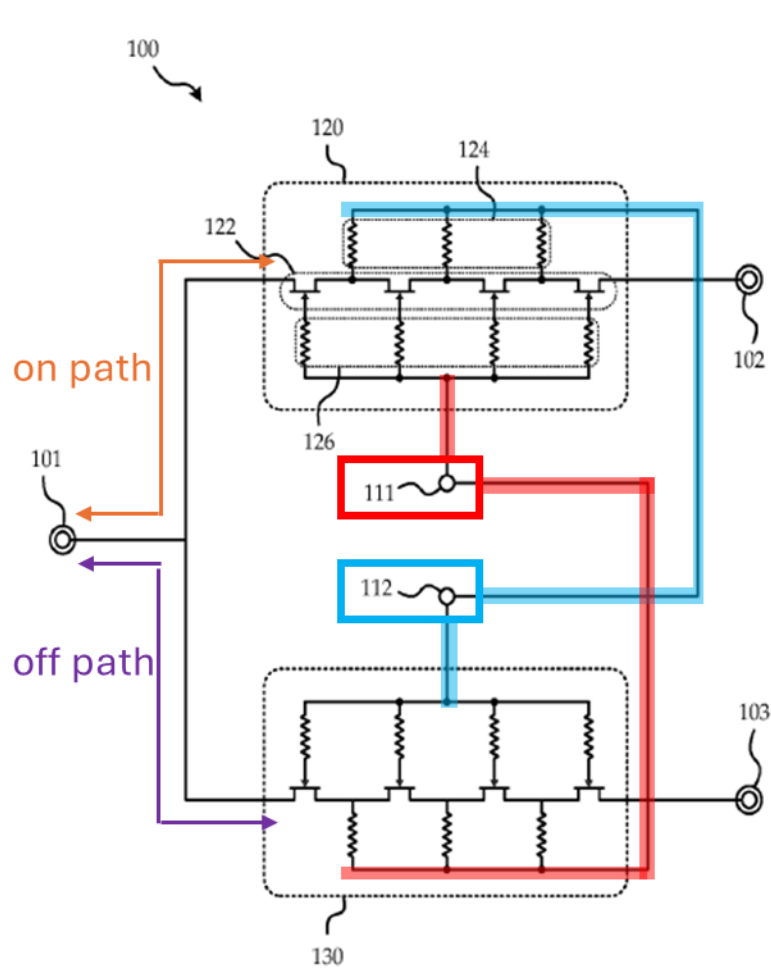


FIG. 1A (PRIOR ART)

Ex-1005, Fig. 1A (annotated), ¶¶ 4, 6; *see* Ex-1013, Fig. 1, ¶ 82. This configuration allows either a high or low voltage to be simultaneously applied to the gates of the transistors in switch 120 and the drains/sources of the transistors in switch 130 **via biasing terminal 111**, and likewise to the drains/sources of the transistors in switch

120 and the gates of the transistors in switch 130 **via biasing terminal 112**. As a result, when biasing terminal 111 is set to high and biasing terminal 112 to low, the transistors in switch 120 are turned fully on, forming the **on path**, while the transistors in switch 130 are turned fully off, forming the **off path**. Ex-1005, ¶ 7. According to Huang, this configuration “fully” biases each transistor and achieves “low insertion loss and high isolation which are very important when dealing with high-power signal transmission.” Ex-1005, ¶ 8. Of course, the annotation in the figure above only shows the case when switch 120 is on and switch 130 is off. Switching high/low of biasing terminals 111 and 112 will switch the on/off paths. The high isolation is a result of a reverse voltage applied to the Vgsd bias voltages to the off transistors. This has the effect of lowering coupling through the transistor, improving isolation, but as Huang states at the expense of worse linearity.

52. Figure 1B of Huang (shown below), which corresponds to Figure 2 of Nakatsuka, builds upon the circuit in Figure 1A (or Nakatsuka’s Figure 1) by adding shunt switches 180 and 190, along with blocking capacitors 182 and 192. In this configuration, switches 160 and 190 operate in tandem—turning on and off together—as do switches 170 and 180.

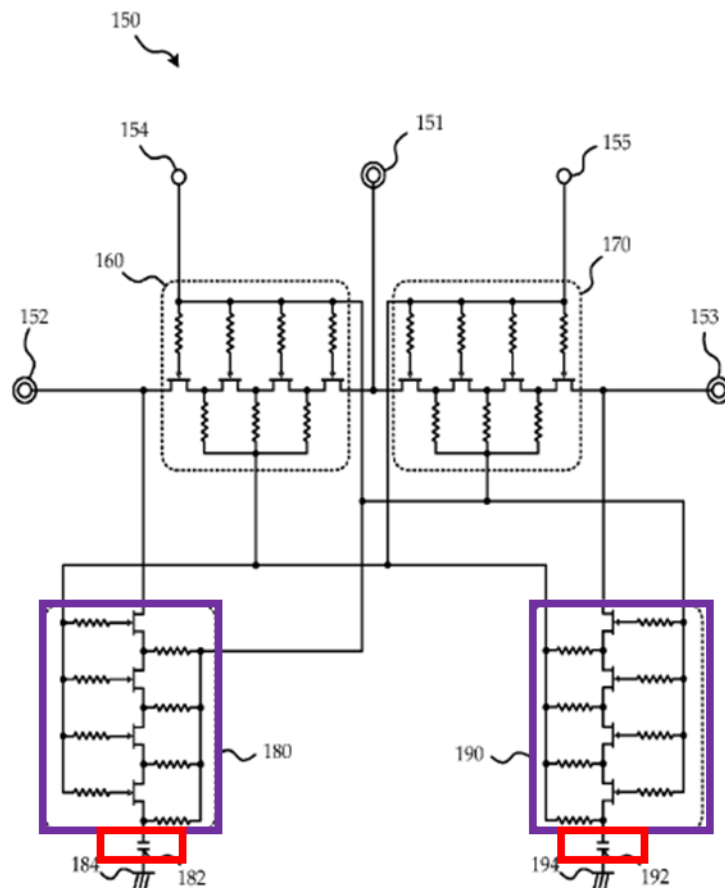


FIG. 1B (PRIOR ART)

Ex-1005, Fig. 1B (highlighted), ¶ 9; *see* Ex-1013, Fig. 2, ¶ 93; Ex-2003, 85:16-86:6 (“Q. And so you would agree that the circuits are the same? A. Oh, I see it. I’m sorry. I missed it. Q. But the labels and callouts differ? A. Yes, I would agree. Yes, the circuit elements, resistors, capacitors, yes, are the same”). In Figure 1B, similar to Huang’s Figure 1A, when biasing terminal 154 is set to a high voltage and terminal 155 to a low voltage, the transistors in switches 160 and 190 are biased to be fully on. At the same time, the transistors in switches 170 and 180 are biased

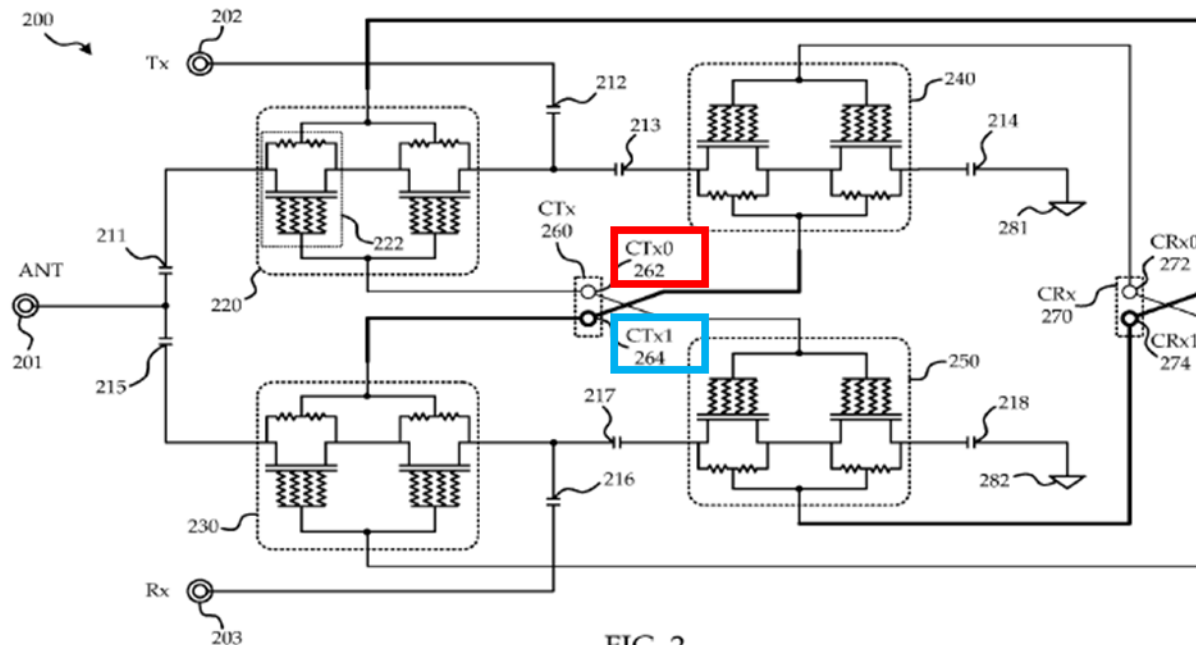
with the opposite polarity—though at the same voltage magnitude—resulting in those transistors being fully off. Ex-1005, ¶¶ 10-12.

53. An understanding of Nakatsuka provides helpful context for understanding Huang. Nakatsuka explains that its configuration allows the device to handle greater power than prior art and also reduces current consumption. Ex-1013, ¶ 21; Ex-2003, 76:13-77:7 (“Q. And Nakatsuka goes on to say that with this configuration, the device can handle power larger than that of the prior art. Furthermore, the current consumption can be reduced. Right? A. Yes, I see that.”). These improvements are attributed to the configuration’s ability to maintain voltage levels at the intermediate connection points of the transistors, preventing them from dropping. As a result, the circuit enhances the transistors’ power handling capability and lowers current consumption compared to earlier designs. Ex-1013, ¶ 24; Ex-2003, 77:8-80:16 (“A. ... Nakatsuka’s about increasing the power handling capacity of a FET switch ... But you know, I might point out, you know, like if you go to paragraph 19, it says that the object of the present invention is to provide a high-frequency switching device and a semiconductor device capable of handling power larger than that of the prior art. So I kind of see that as the point of the invention, purpose of the invention.”).

54. Dr. Larson also agreed that the voltage levels in this context means DC voltage. Ex-2003, 81:3-10 (“Q. ... Nakatsuka is preventing the DC voltage from lowering, right? A. Yeah, I believe one effect of these resistors would be to affect the lowering of the DC voltage in this configuration with these FETs.”). Dr. Larson’s additional comment that “the RF signal affects the DC bias and vice-versa [and] the DC bias can affect the RF” (Ex-2003, 81:17-19) does not change my opinion, and it also does not alter the fact that Nakatsuka’s focus is on DC biasing—not on addressing intermodulation distortion.

55. Returning to Figure 2 of Huang, Huang builds upon the circuit from Figure 2 of Nakatsuka. A key distinction in Huang is that the voltage level applied to the gates of the transistors in switch 220 via **primary bias output 262 (CTx0)** is different from the voltage applied to the drains/sources of the transistors in switch 230, which comes from **secondary bias output 264 (CTx1)**. Ex-1005, ¶ 54. Another difference is that Huang adds additional blocking capacitors 211-213 and 214-217 in addition to the blocking capacitors 214 and 218 that were already in Nakatsuka. *Compare* Ex-1005, Fig. 2 *with* Fig. 1B; Ex-2003, 95:11-96:12 (“Q. And then is it also fair to say, looking at Figure 2, that Huang added capacitors -- and I’ll walk through these ... A. Capacitor 211 does not appear in -- or its equivalent does not appear in Figure 1B in that location. ... Capacitor 215 does not appear in

Nakatsuka in that location ... Well, capacitors, or the equivalent of capacitors 212 and 213, does not appear in Nakatsuka. ... Capacitors 216 and 217 don't appear in Nakatsuka in those locations.”).



Ex-1005, Fig. 2 (highlighted). While Nakatsuka applies the same voltage level (but in reverse polarity) to corresponding nodes, Huang applies two different voltage levels, biasing the off-state V_{gsd} lower than the on-state V_{gsd} to improve signal quality. Ex-2003, 105:6-22 (“A. Well, I wouldn't put it that way. I mean, what Huang -- one of the things Huang talks about is optimizing the VGSD of the devices in the ON and OFF states to get the best performance possible. So it's -- and I think this was stated in the abstract as well.”).

56. The two voltage levels (primary bias output 262 and secondary bias output 264) are explained with Huang's Figure 4A:

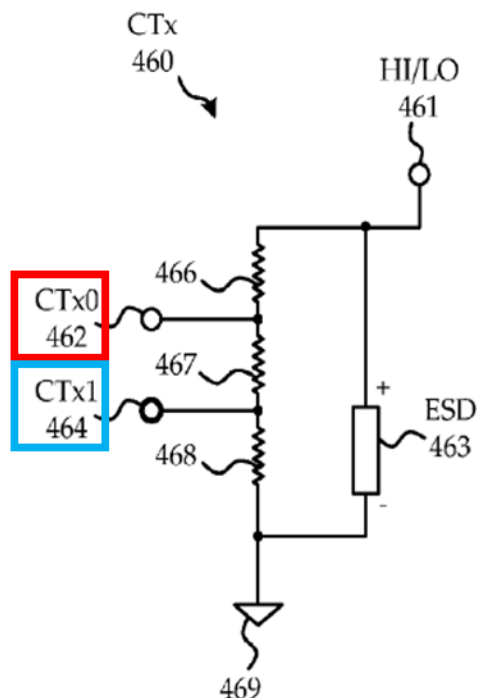


FIG. 4A

Ex-1005, Fig. 4A. A voltage divider between a HI/LO voltage input terminal and ground produces two different voltage levels: **CTx0** (primary bias output) and **CTx1** (secondary bias output). Ex-1005, ¶ 48. The specific voltage levels at CTx0 and CTx1 are determined by the resistor ratio among resistors 466, 467, and 468 and determine the on/off-state V_{gsd} voltages. This configuration allows Huang to achieve more precise control over the DC bias voltages applied to the transistors than Nakatsuka. In this context, Huang's mention of "blocking capacitors" clearly

refers to DC blocking capacitors, which are critical for preserving the integrity of these carefully selected DC bias levels.

57. Moreover, in the RF field at the time of the '194 patent (and even now), the term “blocking capacitor” was understood to mean a DC blocking capacitor. The McGraw-Hill Dictionary of Electrical and Computer Engineering (6th Ed. 2003) provides the same definition for “blocking capacitor” and “coupling capacitor,” which is “[a] capacitor used to block the flow of direct current while allowing alternating or signal current to pass.” Ex-2005, 124. Even the references Dr. Larson cites in the State of the Art section confirms that blocking capacitor means DC blocking. *E.g.*, Ex-1011, 2617 (“on-chip dc blocking and decoupling MIM capacitors”); Ex-1024, Fig. 9 (“DC block”); Ex-1009, ¶ 83 (“prevents the DC-component”); Ex-1035, 5 (“each transistor is DC-isolated by a DC blocking capacitor”). Thus, a POSITA would understand blocking capacitor 211 in Huang to be a “DC blocking capacitor” that blocks only DC signals, while allowing any frequency AC signal to pass. A POSITA would not understand that the intention of blocking capacitor 211 is to “configured to inhibit a low frequency blocker for mixing with a fundamental-frequency signal” as required by claim 2.

58. Seemingly conceding that Huang does not disclose capacitors “configured to inhibit a low-frequency blocker signal from mixing with a

fundamental-frequency signal in the switch,” contradicting his testimony that Huang discloses every limitation (Ex-2003, 31:14-24 (“Q So then you relied on -- and I'm quoting here – “the knowledge, skill, and creativity of a POSITA” to fill in the gaps of Huang, right? A. Well, I'm not sure what you mean by “fill in the gaps.” I don't think there are any gaps ...”), Dr. Larson also presents an alternative position that “configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch” would have been obvious over Huang in view of the general knowledge, skill, and creativity of a POSITA. Ex-1003, ¶ 98 (“Furthermore, to the extent PO asserts that Huang does not expressly disclose blocking capacitor 211 performing this step in SPDT switch 200, with the SPDT switch 200 components arranged as shown in Annotated FIG. 2, and opposing series and shunt switches placed in ON and OFF states depending on the transmit or receive mode of SPDT switch 200 as disclosed by Huang, POSITAs understood this capacitor's inhibition of low-frequency blocker signals from mixing with fundamental frequency signals in SPDT switch 200 to merely be a matter of design choice.”). However, Dr. Larson does not provide an analysis under the obviousness framework but merely presents a collection of references.

59. Dr. Larson cites “low insertion loss along the signal path,” “high isolation from the off paths,” “reduce[d] spurious harmonic emissions,” and

“improve[d] linearity” from Huang as the alleged motivation to turn to the general knowledge of a POSITA to fill the gap for “configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” Ex-1003, ¶ 94. However, as explained above, Huang is directed to improved systems and methods for DC biasing the transistors in an RF switch. According to Huang, all of the cited benefits stem from its improved DC biasing technique. Dr. Larson cites paragraphs 2-3, 39-40, 43-45, and 55-59 from Huang. Below, I go over each of those paragraphs.

60. Paragraphs 2 and 3 of Huang discuss problems in the prior art related to the general approach of biasing transistors fully on and fully off with the same voltage level in opposite polarity—similar to Nakatsuka’s method—and emphasize the DC bias voltage of the transistors. Ex-1005, ¶¶ 2, 3 (“Many of the main advances in semiconductor-based transmit-receive switches have been with respect to isolation and insertion loss. Groups of FETs are arranged in the switch along with judiciously chosen resistors and capacitors to ensure low insertion loss along the signal path and high isolation from the off paths”); Ex-2003, 104:9-105:22 (“Q: And so Huang is focused on biasing the gate and the source/drain to fully turn on and fully turn off the FETs, right? A. Well, I wouldn't put it that way. I mean what Huang -- one of the things Huang talks about is optimizing the VGSD of the devices

in the ON and OFF states to get the best performance possible. So it's -- and I think this was stated in the abstract as well”).

61. Paragraphs 39 and 40 describe Huang’s preferred embodiments, which again involve setting DC bias voltages. Ex-1005, ¶¶ 39 (“While maximizing the on-state V_{gsd} for the on-state FET group switches and fully maximizing the off-state V_{gsd} of the off-state FET group switches achieves respectively low insertion loss and high isolation where and as needed, a quality of the signals passing through the transmit-receive switch depends upon, amongst other things, the particular voltages chosen for off-state V_{gsd} and on-state V_{gsd} of the FETs within the switch.”), 40; Ex-2003, 105:23-108:2 (“Q. Yeah. And so according to Huang, biasing the FETs at a level other than the largest possible bias can lead to improved signal quality, right? A. Yeah, that's their -- their assertion is that a bias other than the highest level can in some cases lead to improved signal quality.”).

62. Paragraphs 43-45 discuss achieving low insertion loss and good linearity by configuring the DC bias voltages in specific ways. Ex-1005, ¶ 43 (“For the on-state FET group switches, lower harmonic emissions were found above a voltage level close to the gate to source breakdown voltage. With the 2.5V SOI technology, 2.0-2.5 V of on-state V_{gsd} was found to exhibit a very low insertion loss, and good linearity. Considering the reliability constraint of 2.5 V, the operating

on-state V_{gsd} level for the turned on FET group switches is chosen to be 2.0 V-2.5 V.”), 44-45; Ex-2003, 108:3-109:18 (“Q. And so it's the selection of the right DC bias that leads to the good linearity here, right? A. Well, the selection of the right DC bias is one of the things that you do to achieve good linearity, not the only thing. But it's -- it's a -- it's an effect that they've noted and are optimizing. Q. The DC bias though is the only thing that Huang describes here though, right? A. Sorry. Paragraph 43 is focused on the DC biasing.”).

63. Paragraphs 55-59 also describe achieving low insertion loss and good linearity by configuring the DC bias voltages in specific ways. Ex-1005, ¶¶ 55, 56 (“As with the prior art, in order to ensure low insertion loss and adequate isolation, when the antenna 201 is utilized for transmission, the first series FET group switch 220 and the second shunt FET group switch 250 are provided with on-state V_{gsd} such that a strong inversion layer creates a low resistance path between source and drain diffusions while the second series FET group switch 230 and the first shunt FET group switch 240 are provided off-state V_{gsd} wherein no channel is established. In order to reduce spurious harmonic emissions and to improve linearity, on-state V_{gsd} is chosen to be at a level between 2.0V and 2.5V while off-state V_{gsd} is chosen to be at a level between 1.1V and 1.5V.”), 57-59; Ex-2003, 109:19-111:12 (“Q. So this sentence is describing the VGSD voltage in both the ON and the OFF states,

right? A. Yeah, the sentence in paragraph 56 is talking about the DC bias gate to source/drain voltage in the ON and OFF states.”).

64. None of these cited paragraphs relate to improving intermodulation distortion or configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

65. Dr. Larson misrepresents both Huang and the '194 patent by claiming that Huang leaves “particular capacitor value implementation details to design choices of POSITAs.” Ex-1003, ¶ 96. Huang is fundamentally focused on DC biasing and makes no mention of “low frequency” or “intermodulation distortion.” Even if capacitor value selection were left to design discretion, such choices—within the context of Huang—would only be aimed at optimizing DC biasing and insertion loss. Huang provides no teaching or suggestion of motivation to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal and thereby improve intermodulation distortion. That a capacitor is inherently a “frequency-dependent impedance” device cannot be a motivation, if so, every analog circuit patent would be rendered obvious merely for using known components—resistors, capacitors, inductors. In analog circuits, countless of different circuits can be built, all with known components.

66. Dr. Larson also asserts that “Huang’s disclosure is identical to the ’194 Patent’s disclosed positioning in its FIG. 9 SPDT switch 250” citing the Prosecution History section. Ex-1003, ¶ 93. As explained above, Huang’s disclosure is not identical to the ’194 patent, particularly regarding the role of the capacitors in Huang and the ’194 patent. The Examiner found the claims patentable over the cited prior art. Ex-1002, 12.

67. Lastly, Dr. Larson relies on the “State of the Art.” Ex-1003, ¶¶ 99-100. But he does not explain why a person of ordinary skill in the art would be motivated to use any of these references to select a capacitor to “configured to inhibit a low frequency blocker from mixing with a fundamental-frequency signal” in Huang. Moreover, the references cited suffer from the same deficiencies as Huang. For example:

- Ex-1011 states “on-chip *dc biasing* MIM capacitors are required” (Ex-1011, 2616 (emphasis added)) and “on-chip *dc blocking* and decoupling MIM capacitors” (Ex-1011, 2617 (emphasis added));
- Ex-1024 states “DC block” (Ex-1024, Fig. 9);
- Ex-1029 states “ C_{B1} and C_{B2} [] allow *dc biasing* of the TX and RX nodes of the switch” (Ex-1029, 36 (emphasis added));

- Ex-1009 states “prevents the ***DC-component*** on the transmission-side from being generated on the reception-side, or vice versa” (Ex-1009, ¶ 83 (emphasis added)); and
- Ex-1035 states “each transistor is DC-isolated by a DC blocking capacitor” (Ex-1035, 5).

Ex-2003, 123:18-125:14, 126:6-127:9, 127:15-129:20. These references, like Huang, focus on DC biasing and blocking—not on inhibiting low-frequency blocker signals from mixing with fundamental-frequency signals to improve intermodulation distortion.

2. The Petition fails to show claim 5’s “forming a [first/second] capacitor on the semiconductor substrate so as to be connected in series with the [first/second] switch circuit between the [first/second] switch circuit and the antenna node” is obvious over Huang in view of a POSITA’s knowledge

68. Claim 5 requires the claimed “a semiconductor substrate” with a “first switch circuit” “second switch circuit,” “first capacitor,” and “second capacitor” formed on “*the* semiconductor substrate.” The ’194 patent specification explains that the inhibiting capacitors can be “part of the same semiconductor die” as the transistors, “part of a second die mounted on the packaging substrate” or “at a location outside the semiconductor die.” Ex-1001, 2:15-21; Ex-2003, 131:21-133:14 (“Q. So the ’194 patent discloses that the capacitor could be on the same die

as the FETs or not on the same die as the FETs, right? A. Yes, and as I said, that's a well-understood -- very well-understood at the time choice that an engineer would make.”).

69. Dr. Larson states that Huang discloses all of these elements. *See* Ex-1003, ¶¶ 118, 120 (“Huang discloses ...”). However, Huang is silent on whether its capacitors of the Figure 2 circuit are on the same die as the other components. Acknowledging this weakness, Dr. Larson again relies on the State of the Art, as if the State of the Art dictates using on-die capacitors with Huang. Ex-1003, ¶ 119 (“To the extent PO asserts that Huang does not explicitly disclose ...”). A POSITA could choose off-die capacitors over on-die capacitors. Off-die capacitors can be built with a larger capacitance value, and they have higher quality factor. Particularly in the context of Huang, off-die capacitors are known to perform better for DC blocking. Huang teaches that its capacitors is to reduce insertion loss. Ex-1005, ¶ 3 (“judiciously chosen resistors and capacitors to ensure low insertion loss along the signal path.”) Larger capacitors have been known to have less insertion loss. And in general, off-die capacitors are larger in size compared to on-die capacitors. As such, a person of ordinary skill in the art would have been motivated to implement a relatively large sized capacitors off-die in Huang to achieve better

insertion loss. Dr. Larson does not consider Huang's objectives, including insertion loss, and merely assert "design choice" and "cost." Ex-1003, ¶ 119.

3. Dependent Claims

70. Because claim 6 depends from independent claim 5, claim 6 would not have been obvious over Huang in view of a POSITA's knowledge for the same reason as claim 5 as explained above. My analysis for claim 5 equally applies.

71. Dependent claim 8 would not have been obvious over Huang in view of a POSITA's knowledge for the same reason as claim 2 for requiring "at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental frequency signal in the switch," as explained above. My analysis for claim 2 equally applies.

72. Dependent claim 9 would not have been obvious over Huang in view of a POSITA's knowledge for the same reason as independent claim 5 for requiring the "first capacitor" to be "part of the same semiconductor die as the first switch," as explained above. My analysis for claim 5 equally applies. Dependent claim 10 would not have been obvious over Huang in view of a POSITA's knowledge for the reasons I explained above regarding claim 5 for requiring the "first capacitor" be "part of a second die," which is not the same die as the semiconductor die where the first switch is formed. My analysis for claim 5 equally applies.

B. The Challenged Claims Would Not Have Been Obvious Over Seshimo (Ground 2)

73. Ground 2 fails for similar reasons as Ground 1. In my opinion, Ground 2 is duplicative of Ground 1. Seshimo, like Huang, only discloses DC blocking capacitors and not “configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.” Seshimo also does not disclose that the capacitors Petition identifies are on the same substrate as the switch circuits as required by certain claims. Dr. Larson recognizes this weakness in Seshimo and asserts that the claims would have been obvious over Seshimo in view of the knowledge of a POSITA but does not articulate why a person of ordinary skill in the art would have been motivated to modify Seshimo.

1. The Petition fails to show claim 2’s “at least one of the first and second capacitors configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch” is obvious over Seshimo in view of a POSITA’s knowledge

74. Dr. Larson’s opinion regarding Seshimo appears duplicative of his opinion regarding Huang. Except for the opening paragraph of each ground and citations to each reference, the two grounds seem identical. *Compare* Ex-1003, ¶¶ 163-171 (Seshimo) *with* 92-101 (Huang). Dr. Larson does not present any other evidence or analysis beyond substituting Huang’s disclosures with those of Seshimo.

75. Dr. Larson alleges that Seshimo's capacitor C3 in Figure 3 "discloses" the claimed "first capacitor" (Ex-1003, ¶ 163) and renders obvious that the capacitor is "configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch." Ex-1003, ¶ 167 ("POSITAs would understand Seshimo's disclosed implementation of capacitor C3 as being a high-pass filter that would 'inhibit[] a low-frequency blocker signal from mixing with a fundamental frequency signal in the RF switch.'"). Like Huang, Seshimo never mentions anything about a "low-frequency blocker signal" or "configured to inhibit a low frequency blocker signal from mixing with a fundamental-frequency signal in the switch." Seshimo also never discusses intermodulation distortion.

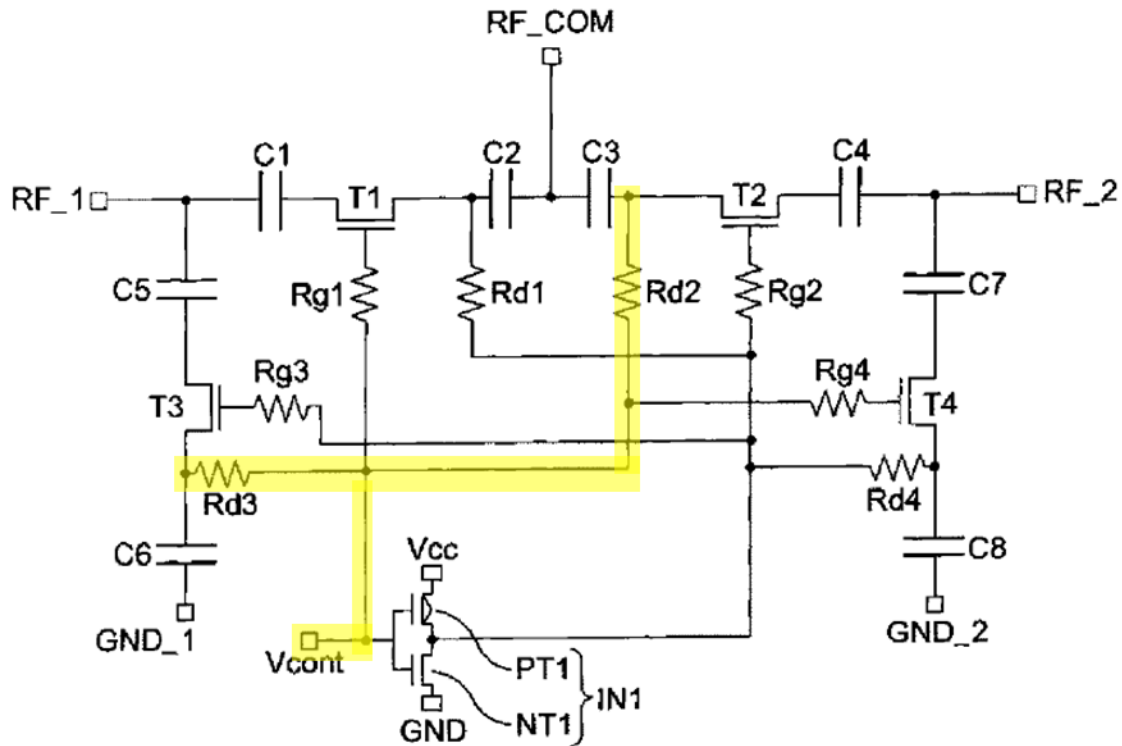
76. In my opinion, Seshimo is even clearer that its capacitors C1-C8 shown below in the figure are all DC blocking capacitors. Ex-1007, ¶ 90 ("C1 to C8: [DC] Component removal capacitor"); Ex-1006, ¶ 90 ("C1~C8 DC"); Ex-2004, ¶ 90 ("C1-C8: DC component removing capacitance").¹ Dr. Larson seems to agree. Ex-2003,

¹ In the English translation submitted by Petitioner (Ex-1007), "DC" is missing from paragraph 90. However, in the original Japanese application (Ex-1006), "DC" is included in the same location. *Compare* Ex-1007, ¶ 90 *with* Ex-1006, ¶ 90. Seshimo consistently refers to capacitors C1-C4 as "DC component removal

121:5-15 (“Q. So fair to say that a more accurate translation for capacitors C1 to C8 is DC component removal capacitor? A. ... But certainly that hints that DC should have been included in the -- perhaps it should have been included in the English translation.”), 121:25-122:7 (“Q. As a person of ordinary skill in the art, would you agree that the phrase ‘DC component removal capacitor’ is the same as DC blocking capacitor? A. I don't see any substantial difference between those two and I think a person of ordinary skill in the art would view those as essentially the same.”).

capacitors” in other embodiments. Ex-1007, ¶¶ 13-14, 33-35; Ex-2003, 117:10-16, 117:25-118:19. Therefore, it is clear that Seshimo intended the capacitors in its Figure 3 embodiments to also be DC component removal capacitors. Nevertheless, I reviewed another certified English translation obtained by Patent Owner (Ex-2004).

FIG. 3



Ex-1007, Fig. 3 (highlighted). As can be seen, Seshimo's transistor biasing is similar to Huang's: in Seshimo, either the source or the drain of each transistor is biased, whereas in Huang, both the source and drain of each transistor are biased. Seshimo does not use two different bias voltage levels (on-state and off-state) as in Huang. In essence, Seshimo is a similar but another approach to Huang's DC biasing.

77. Seshimo is also about “enhance[ing] maximum permissible input power suppress[ing] an increase in ON-resistance” through a particular DC biasing of transistors in a switch circuit like Huang. Ex-1007, Abstract, ¶ 7; EX-2003,

122:8-123:6. Seshimo recognizes that when designing a high-frequency switch circuit using a MOSFET formed on a silicon substrate, the substrate's resistance and the ON-resistance of the MOSFET (i.e., the resistance of a transistor when it is on) causes insertion loss. Ex-1007, ¶ 4. By biasing transistors similarly to Huang, Seshimo also proposes that ON-resistance can be reduced. Also like Huang, Seshimo does not address improving intermodulation distortion.

78. Since Dr. Larson makes the same argument with Seshimo as he does in the Huang ground, and relies on the same "State of the Art," the reasons I provide in detail above applies equally to those arguments.

2. The Petition fails to show claim 5's "forming a [first/second] capacitor formed on the same semiconductor substrate so as to be connected in series with the [first/second] switch circuit between the [first/second] switch circuit and the antenna node" is obvious over Seshimo in view of a POSITA's knowledge

79. As explained in the Huang ground, claim 5 requires "a semiconductor substrate" with a "first switch circuit," "second switch circuit," "first capacitor" and "second capacitor" formed on "*the* semiconductor substrate." The '194 patent specification explains that the inhibiting capacitors can be "part of the same semiconductor die" as the transistors, "part of a second die mounted on the packaging substrate" or "at a location outside the semiconductor die." Ex-1001, 2:15-21; Ex-2003, 131:21-133:14 ("Q. So the '194 patent discloses that the

capacitor could be on the same die as the FETs or not on the same die as the FETs, right? A. Yes, and as I said, that's a well-understood -- very well-understood at the time choice that an engineer would make.”).

80. Dr. Larson states that Huang discloses all of these elements. *See* Ex-1003, ¶¶ 188-191 (“Seshimo discloses ...”). However, Seshimo is silent on whether its capacitors in the Figure 3 circuit are on the same die as the other components. Acknowledging this weakness, Dr. Larson again relies on the State of the Art, as if the State of the Art dictates using on-die capacitors with Seshimo. Ex-1003, ¶ 190 (“To the extent PO asserts that Seshimo does not explicitly disclose ...”). As explained in the Huang ground, a POSITA could choose off-die capacitors over on-die capacitors. Off-die capacitors can be built with a larger capacitance value, and they have higher quality factor. Particularly in the context of Seshimo, as off-die capacitors are known to perform better for DC blocking. Similar to Huang, Seshimo also teaches that its capacitors reduce insertion loss. Ex-1007, ¶¶ 4 (“the substrate is conductive, which causes insertion loss due to the resistance of the substrate in addition to insertion loss due to the ON-resistance of the MOSFET”), 7 (“an object of the present invention is to provide a semiconductor switching circuit capable of improving the maximum permissible input power while suppressing an increase in ON-resistance.”). As explained above, larger capacitors have been known to have

less insertion loss, and off-die capacitors are larger in size compared to on-die capacitors. As such, a person of ordinary skill in the art would have been motivated to implement a relatively large sized capacitors off-die in Seshimo to achieve better insertion loss. Dr. Larson does not consider Seshimo's objectives, including insertion loss, and merely assert "design choice" and "cost." Ex-1003, ¶ 190.

3. Dependent Claims

81. Because claim 6 depends from independent claim 5, claim 6 would not have been obvious over Seshimo in view of a POSITA's knowledge for the same reason as claim 5 as explained above. My analysis for claim 5 equally applies.

82. Dependent claim 8 would not have been obvious over Seshimo in view of a POSITA's knowledge for the same reason as claim 2 for requiring "at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental frequency signal in the switch," as explained above. My analysis for claim 2 equally applies.

83. Dependent claim 9 would not have been obvious over Seshimo in view of a POSITA's knowledge for the same reason as independent claim 5 for requiring the "first capacitor" to be "part of the same semiconductor die as the first switch," as explained above. My analysis for claim 5 equally applies. Dependent claim 10 not have been obvious over Seshimo in view of a POSITA's knowledge for the

reasons I explained above regarding claim 5 for requiring the “first capacitor” be “part of a second die,” which is not the same die as the semiconductor die where the first switch is formed. My analysis for claim 5 equally applies.

XI. SUMMARY OF OPINIONS

84. It is my opinion that the Petitioner did not prove Huang in view of a POSITA’s knowledge renders obvious the challenged claims.

85. It is my opinion that the Petitioner did not prove Seshimo in view of a POSITA’s knowledge renders obvious the challenged claims.

XII. AVAILABILITY FOR CROSS-EXAMINATION

86. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

XIII. RIGHT TO SUPPLEMENT

87. I reserve the right to supplement my opinions in the future to respond to any arguments that the Petitioner raises and to take into account new information as it becomes available to me.

XIV. JURAT

88. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. I declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: September 23, 2025

By: 
David Wentzloff, Ph.D.

LIST OF MATERIALS CONSIDERED

Exhibit	Description
2001	Declaration of Dr. David Wentzloff
2002	CV of Dr. David Wentzloff
2003	Deposition Transcript of Dr. Larson
2004	Certified English Translation of Japanese Patent Publication No. JP 2006-121217 (Ex-1006)
2005	McGraw-Hill Dictionary of Electrical and Computer Engineering (6 th Ed. 2003)
N/A	IPR2024-01457 Petition
EX-1001	U.S. Patent No. 9,148,194 to Madan et al. (“’194 Patent”)
EX-1002	Prosecution History of U.S. Patent No. 9,148,194
EX-1005	U.S. Patent Publication No. 2011/0254614 A1 to C-W Huang, et al.
EX-1006	Japanese Patent Publication No. JP 2006-121217 to Seshimo, Toshiko et al.
EX-1007	Certified English Translation of Japanese Patent Publication No. JP 2006-121217 (EX-1006)
EX-1008	“General Purpose RF Switches”, Skyworks Solutions., Inc.
EX-1009	U.S. Patent Pub. No. 2012/0081262 to Tanaka, et al.
EX-1010	U.S. Patent Pub. No. 2010/0327948 to Nisbet, et al.
EX-1011	Madan, et al., “Fully Integrated Switch-LNA Front-End IC Design in CMOS: A Systematic Approach for WLAN”, IEEE Journal of Solid State Circuits, Vol. 46, No. 11
EX-1012	Excerpts from V. Veley, “The Benchtop Electronics Reference Manual,” Tab Books Inc., 1987
EX-1013	U.S. Patent Pub. No. 2004/0251952 to Nakatsuka et al.
EX-1014	Excerpts from Paul Horowitz, et al., “The Art of Electronics” (2d ed. 1989)
EX-1015	Japanese Patent Publication No. JP2011-166663A to Takashi et al.
EX-1016	English Machine Translation of Japanese Patent Publication No. JP2011-166663A (EX-1015)
EX-1017	U.S. Patent Publication No. 2013/0154761 to Ilkov
EX-1018	U.S. Patent No. 6,698,082 to Crenshaw, et al.
EX-1019	EP Pat. No. 2348532 to Brindle, et al.
EX-1020	International Patent Publication WO 2011/045442 to Heaney, et al.
EX-1021	C-W Huang, et al., “Highly Linear SOI Single-Pole, 4-Throw Switch with an Integrated Dual-band LNA and Bypass

	Attenuators”, SiGe Semiconductor, 2010 IEEE Radio Frequency Integrated Circuits Symposium
EX-1022	U.S. Patent Pub. No. 2011/0294443 to Nohra, et al.
EX-1023	U.S. Patent No. 7,359,677 to C-W Huang, et al.
EX-1024	Rick Cory, et al., “Solid State RF/Microwave Switch Technology: Part 2”, June 2009, Skyworks Solutions, Inc.
EX-1025	U.S. Patent No. 7,088,971 to Burgener, et al.
EX-1026	U.S. Patent Pub. No. 2011/0260773 to Granger-Jones et al.
EX-1027	Excerpts from R. Boylestead, et al., “Electricity, Electronics and Electromagnetics Principles and Applications,” Prentice-Hall, Inc., 1977
EX-1028	C-W Huang, et al., “Highly Linear 4.9-5.9 GHz WLAN Front-End Module Based on SiGe BiCMOS and SOI”, 2011 IEEE MTT-S International Microwave Symposium, Baltimore, MD, USA, August 4, 2011, pp. 1-4
EX-1029	F-J Huang, et al., “Single-Pole Double-Throw CMOS Switches for 900-MHz and 2.4-GHz Applications on p Silicon Substrates”, IEEE Journal of Solid-State Circuits, Vol. 39, No. 1, January 2004
EX-1030	U.S. Patent No. 7,265,604 to Yasuda et al.
EX-1031	Skyworks Solutions, Inc., “SKY14151-350LF High-Power Single Pole Four Throw (SP4T) Switch with Decoder”, Data Sheet, October 6, 2010
EX-1032	Skyworks Solutions, Inc., “SC Series: MIS Chip Capacitors”, Data Sheet, November 1, 2005
EX-1033	Skyworks Solutions, Inc., “AS191-73, AS191-73LF: PHEMT GaAs IC High-Linearity 3 V Control SPDT Switch 0.1–4 GHz”, Data Sheet, August 2, 2006
EX-1034	Korean Patent Publication No. KR100967847B1
EX-1035	English Machine Translation of Korean Patent Publication No. KR100967847B1 (EX-1034)
EX-1036	J. Oerth, et al., “Evaluating pHEMT Process Improvements Using Wafer Level RF Tests”, Skyworks Solutions, Inc.
EX-1037	Prosecution History of U.S. Patent No. 9,450,579
EX-1038	U.S. Patent Pub. No. 2010/0123215 to Pan et al.
EX-1039	“Choosing the Right RF Switches for Smart Mobile Device Applications” White Paper, Skyworks Solutions, Inc., May 9, 2011

EX-1040	T. Ranta et al., “Antenna Switch Linearity Requirements for GSM/WCDMA Mobile Phone Front-Ends,” presented at “The European Conference on Wireless Technology” in Paris, France, October 3-4, 2005, published in 2005 Wireless Technology Conference Proceedings, Horizon House Publications Ltd., pp. 23-36
EX-1041	S. Bellette, “Top Considerations When Buying or Specifying an RF Switch”, Skyworks Solutions, Inc.
EX-1042	Excerpts of “Linear Products 2008”, Skyworks Solutions, Inc.
EX-1043	Excerpts of M. Horowitz, “Elementary Electricity and Electronics”, TAB BOOKS Inc., 1986
EX-1044	G. Breed, “There’s Nothing Magic About 50 Ohms”, High Frequency Electronics magazine, Summit Technical Media, LLC, June 2007
EX-1045	“United States Frequency Allocations – The Radio Spectrum”, National Telecommunications and Information Administration Office of Spectrum Management, October 2003
EX-1046	P. J. Mole, “Integration of RF Systems on a Chip”, Chapter 3 of “Circuits and Systems for Wireless Communications”, Helfenstein, M., Moschytz, G.S. (eds), Springer, Boston, MA, 2002
EX-1047	“Personal Handy-phone System”, Wikipedia
EX-1048	“Extension of Frequency Band Allocations for Personal Handy-phone systems (PHS),” PHS MoU Document A-GN3.00-01-TS, Version 1, (April 20, 1999)
EX-1049	Skyworks Solutions, Inc., “SKY13399-468LF: 0.7 – 2.7 GHz DPx3T Switch”, Data Sheet