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(71) Applicant 000003078
Toshiba Corporation
1-1-1, Shibaura, Minato-ku, Tokyo

(74) Agent 100075812
Kenji YOSHITAKE, Attorney

(74) Agent 100088889
Hidetoshi TACHIBANA, Attorney

(74) Agent 100082991
Yasunori SATO, Attorney

(74) Agent 100096921
Hiroshi YOSHIMOTO, Attorney

(74) Agent 100103263
Yasushi KAWASAKI, Attorney

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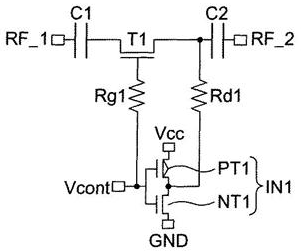
(54) [Title of the Invention] Semiconductor Switching Circuit

(57) [Abstract]

[Problem] To increase the maximum allowable input power while also suppressing a rise in ON-resistance.

[Solution] Provided is a semiconductor switching circuit comprising: an enhancement-type n-channel MOSFET T1; first and second terminals RF_1, RF_2; a control terminal Vcont receiving a control signal that controls MOSFET T1 switching; a first capacitive element C1 connected between the drain or source of the MOSFET T1 and the first terminal RF_1; a second capacitive element C2 connected between the source or drain of the MOSFET T1 and the second terminal RF_2; a first resistance Rg1 connected between the gate of the MOSFET T1 and the control terminal Vcont; a logic circuit IN1 that controls MOSFET T1 switching with the input side connected to the control terminal Vcont; and a second resistance Rd1 connected between one of the source or drain of the MOSFET T1 and the output side of the logic circuit IN1.

[Selected Drawing] FIG. 1



Skyworks Ex 2004
Kangxi v. Skyworks
IPR2024-01457

[Claims]

[Claim 1]

A semiconductor switching circuit comprising:
an enhancement-type n-channel MOSFET;
first and second terminals;
a control terminal receiving a control signal that controls MOSFET switching;
a first capacitive element connected between the drain or source of the MOSFET and the first terminal;
a second capacitive element connected between the source or drain of the MOSFET and the second terminal;
a first resistance connected between the gate of the MOSFET and the control terminal;
a logic circuit that controls MOSFET switching with the input side connected to the control terminal;
and a second resistance connected between one of the source or drain of the MOSFET and the output side of the logic circuit.

[Claim 2]

A semiconductor switching circuit comprising:
first and second enhancement-type n-channel MOSFETs;
first, second, and third terminals;
a control terminal receiving a control signal that controls switching of the first and second MOSFETs;
a first capacitive element connected between the drain or source of the first MOSFET and the first terminal;
a second capacitive element connected between the source or drain of the first MOSFET and the second terminal;
a third capacitive element connected between the drain or source of the second MOSFET and the second terminal;
a fourth capacitive element connected between the source or drain of the second MOSFET and the third terminal;
a first resistance connected between the gate of the first MOSFET and the control terminal;
a logic circuit that controls MOSFET switching with the input side connected to the control terminal;
a second resistance connected between one of the source or drain of the first MOSFET and the output side of the logic circuit;
a third resistance connected between one of the source or drain of the second MOSFET and the control terminal; and
a fourth resistance connected between the gate of the second MOSFET and the output side of the logic circuit.

[Claim 3]

The semiconductor switching circuit according to claim 2, further comprising inductor elements connected in parallel to the source and drain of at least one of the first and second MOSFETs.

[Claim 4]

A semiconductor switching circuit comprising:
first, second, third, and fourth enhancement-type n-channel MOSFETs;
first, second, third, fourth, and fifth terminals;
a control terminal receiving a control signal that controls switching of each of the first to fourth MOSFETs;
a first capacitive element connected between the drain or source of the first MOSFET and the first terminal;
a second capacitive element connected between the source or drain of the first MOSFET and the second terminal;
a third capacitive element connected between the drain or source of the second MOSFET and the second terminal;
a fourth capacitive element connected between the source or drain of the second MOSFET and the third terminal;

a fifth capacitive element connected between the drain or source of the third MOSFET and the first terminal;
a sixth capacitive element connected between the source or drain of the third MOSFET and the fourth terminal;
a seventh capacitive element connected between the drain or source of the fourth MOSFET and the third terminal;
an eighth capacitive element connected between the source or drain of the fourth MOSFET and the fifth terminal;
a first resistance connected between the gate of the first MOSFET and the control terminal;
a logic circuit that controls switching of the first to fourth MOSFETs with the input side connected to the control terminal;
a second resistance connected between one of the source or drain of the first MOSFET and the output side of the logic circuit;
a third resistance connected between one of the source or drain of the second MOSFET and the control terminal;
a fourth resistance connected between the gate of the second MOSFET and the output side of the logic circuit;
a fifth resistance connected between the gate of the third MOSFET and the output side of the logic circuit;
a sixth resistance connected between one of the source or drain of the third MOSFET and the control terminal;
a seventh resistance connected between the gate of the fourth MOSFET and the control terminal; and
an eighth resistance connected between one of the source or drain of the fourth MOSFET and the output side of the logic circuit.

[Claim 5]

The semiconductor switching circuit according to any of claims 1 to 4, wherein the logic circuit is an inverter circuit based on a CMOS configuration.

[Detailed Description of the Invention]

[Technical Field]

[0001]

The present invention relates to a semiconductor switching circuit, specifically a high-frequency semiconductor switching circuit that includes a MOSFET formed on a silicon substrate.

[Background Art]

[0002]

Compound semiconductors with a semi-insulating substrate and high electron mobility are widely used as high-frequency semiconductor switching circuits that realize excellent switching characteristics in the 1 GHz or higher frequency range.

[0003]

However, in recent years, development of high-frequency semiconductor switching circuits using CMOS processes has been significant. The main reason for this is that CMOS switches allow for CMOS, RF and IC integration.

[0004]

However, in attempts to realize high-frequency semiconductor switching circuits using MOSFETs formed on silicon substrates, a problem has occurred. Because a conductive substrate is used, insertion loss due to the substrate resistance occurs in addition to insertion loss due to ON-resistance of the MOSFET.

[0005]

In addition, when using a high-frequency semiconductor switching circuit as a send/receive changeover switch, very high maximum allowable input power is required. In order to realize this, it is necessary to stack MOSFETs vertically or to use a multi-gate structure. However, this means an increase in ON-resistance, which in turn leads to an increase in insertion loss. One method of reducing the increase in ON-resistance due to MOSFETs stacked vertically or a multi-structure is to increase the gate width. However, this leads to an increase in chip area and a deterioration in isolation. This trade-off relationship has been optimized, but the characteristics of the resulting CMOS switch are much inferior to those of a switching circuit using a compound semiconductor.

[0006]

The following is a list of patent documents that disclose high-frequency semiconductor switching circuits of the prior art.

[Patent Document 1] JP H10-242836 A

[Patent Document 2] JP H11-46101 A

[Patent Document 3] JP H09-289443 A

[Patent Document 4] JP H08-70245 A

[Patent Document 5] JP H09-214201 A

[Patent Document 6] JP H10-284901 A

[Patent Document 7] JP 2003-37521 A

[Patent Document 8] JP 2000-261302 A

[Disclosure of the Invention]

[Problem to Be Solved by the Invention]

[0007]

In view of these circumstances, it is an object of the present invention to provide a semiconductor switching circuit that can increase the maximum allowable input power while also suppressing a rise in ON-resistance.

[Means for Solving the Problem]

[0008]

One aspect of the present invention is a semiconductor switching circuit comprising:
an enhancement-type n-channel MOSFET;
first and second terminals;
a control terminal receiving a control signal that controls MOSFET switching;
a first capacitive element connected between the drain or source of the MOSFET and the first terminal;
a second capacitive element connected between the source or drain of the MOSFET and the second terminal;
a first resistance connected between the gate of the MOSFET and the control terminal;
a logic circuit that controls MOSFET switching with the input side connected to the control terminal;
and a second resistance connected between one of the source or drain of the MOSFET and the output side of the logic circuit.

[0009]

Another aspect of the present invention is a semiconductor switching circuit comprising:
first and second enhancement-type n-channel MOSFETs;
first, second, and third terminals;
a control terminal receiving a control signal that controls switching of the first and second MOSFETs;
a first capacitive element connected between the drain or source of the first MOSFET and the first terminal;
a second capacitive element connected between the source or drain of the first MOSFET and the second terminal;
a third capacitive element connected between the drain or source of the second MOSFET and the second terminal;
a fourth capacitive element connected between the source or drain of the second MOSFET and the third terminal;
a first resistance connected between the gate of the first MOSFET and the control terminal;
a logic circuit that controls MOSFET switching with the input side connected to the control terminal;
a second resistance connected between one of the source or drain of the first MOSFET and the output side of the logic circuit;
a third resistance connected between one of the source or drain of the second MOSFET and the control terminal; and
a fourth resistance connected between the gate of the second MOSFET and the output side of the logic circuit.

[0010]

Yet another aspect of the present invention is a semiconductor switching circuit comprising:
first, second, third, and fourth enhancement-type n-channel MOSFETs;
first, second, third, fourth, and fifth terminals;
a control terminal receiving a control signal that controls switching of each of the first to fourth MOSFETs;
a first capacitive element connected between the drain or source of the first MOSFET and the first terminal;
a second capacitive element connected between the source or drain of the first MOSFET and the second terminal;
a third capacitive element connected between the drain or source of the second MOSFET and the second terminal;
a fourth capacitive element connected between the source or drain of the second MOSFET and the third terminal;
a fifth capacitive element connected between the drain or source of the third MOSFET and the first terminal;
a sixth capacitive element connected between the source or drain of the third MOSFET and the fourth terminal;
a seventh capacitive element connected between the drain or source of the fourth MOSFET and the third terminal;
an eighth capacitive element connected between the source or drain of the fourth MOSFET and the fifth terminal;
a first resistance connected between the gate of the first MOSFET and the control terminal;
a logic circuit that controls switching of the first to fourth MOSFETs with the input side connected to the control terminal;
a second resistance connected between one of the source or drain of the first MOSFET and the output side of the logic circuit;
a third resistance connected between one of the source or drain of the second MOSFET and the control terminal;
a fourth resistance connected between the gate of the second MOSFET and the output side of the logic circuit;
a fifth resistance connected between the gate of the third MOSFET and the output side of the logic circuit;
a sixth resistance connected between one of the source or drain of the third MOSFET and the control terminal;

a seventh resistance connected between the gate of the fourth MOSFET and the control terminal; and an eighth resistance connected between one of the source or drain of the fourth MOSFET and the output side of the logic circuit.

[Effect of the Invention]

[0011]

The present invention is able to provide a semiconductor switching circuit that can increase the maximum allowable input power while also suppressing a rise in ON-resistance.

[Best Mode for Carrying Out the Invention]

[0012]

Embodiments of the present invention will now be described with reference to the drawings.

[0013]

(1) First Embodiment

The configuration of the high-frequency semiconductor switching circuit in first embodiment of the present invention is shown in FIG. 1.

[0014]

The first embodiment includes an enhancement-type n-channel MOSFET T1, DC component-removing capacitance C1, C2 with one end connected, respectively, to the source and drain of the MOSFET T1, high resistance Rg1 connected on one end to the gate of the MOSFET T1, high resistance Rd1 connected on one end to either the source or drain of the MOSFET T1, and a CMOS inverter circuit IN1 composed of a p-channel MOSFET PT1 and an n-channel MOSFET NT1, with input/output terminals connected between the other end of resistance Rg1 and the other end of resistance Rd1.

[0015]

Terminals RF_1 and RF_2 that are to be connected to high-frequency signal lines are connected to the other end of each of capacitance C1 and C2

[0016]

Terminal GND connected to the CMOS inverter circuit IN1 is a ground terminal, and terminal Vcc is a power supply voltage Vcc terminal.

[0017]

Control terminal Vcont, which supplies control voltage Vcont to control switching, is connected to the input terminal of the CMOS inverter circuit IN1.

[0018]

Resistance Rg1 and Rd1 are both resistance with a value of around 10 kΩ, for example, which is high enough to keep high-frequency signals from leaking.

[0019]

Operation of the first embodiment, which has the configuration described above, will now be explained.

[0020]

A1) When control voltage Vcont is 0 V

Control voltage Vcont of 0 V is inputted to the input terminal of the CMOS inverter circuit IN1, and power supply voltage Vcc is outputted from the output terminal.

[0021]

When 0 V is applied to the gate of the n-channel MOSFET T1, power supply voltage Vcc is applied to the drain or source (here, the source) connected to the output terminal of the CMOS inverter circuit IN1.

[0022]

If the power supply voltage Vcc is 3 V, the gate-source voltage Vgs of the MOSFET T1 is -3 V.

[0023]

Also, if the threshold voltage Vth of the MOSFET T1 is 0.7 V, then the MOSFET T1 will be OFF at this time.

[0024]

As a result, there is no conduction between terminals RF_1 and RF_2.

[0025]

B1) When control voltage Vcont is 3 V

Here, 3 V is applied to the gate of MOSFET T1, and 0 V is applied to the source. This causes the gate-source voltage Vgs of MOSFET T1 to become 3 V, turning ON MOSFET T1.

[0026]

When MOSFET T1 is turned ON, voltage Vgs – Vth = 2.3 V, and sufficiently low ON-resistance is realized.

[0027]

However, when MOSFET T1 is turned OFF, voltage Vgs-Vth = -3.7 V, enabling the OFF state to be maintained even with respect to a sufficiently large input amplitude.

[0028]

When terminal RF_2 is grounded and a sine wave voltage is applied to terminal RF_1, MOSFET T1 remains in the OFF state until the voltage amplitude reaches 7.4 V (14.8 Vpp peak to peak).

[0029]

When a voltage amplitude of 7.4V in a 50 Ω system is converted to power, it becomes 27.38 dBm. As a result, a maximum allowable input power that is sufficiently utilizable by, for example, the send/receive switch in a personal handyphone system (PHS) can be realized.

[0030]

In the first embodiment, by making the gate voltage swing between 0 V and 3 V and the source-drain voltage swing between 0 V and 3 V as explained above, the gate-source voltage Vgs is able to swing with an amplitude twice that of the power supply voltage Vcc (6 V).

[0031]

This enables the maximum allowable input amplitude to be increased, the OFF state to be maintained, and the ON-resistance of the MOSFET to be brought closer to the ON-resistance of a GaAs-based FET.

[0032]

Note that in the circuit configuration shown in FIG. 1, the input terminal of the CMOS inverter circuit IN1 is connected to resistance Rg1, and the output terminal is connected to resistance Rd1. However, conversely, the input terminal may be connected to resistance Rd1 and the output terminal may be connected to resistance Rg1. In this case, the only difference would be that the operating polarity with respect to control voltage Vcont would be reversed, but the same effects as the circuit configuration shown in FIG. 1 would be obtained.

[0033]

(2) Second Embodiment

The configuration of the high-frequency semiconductor switching circuit in the second embodiment of the present invention is shown in FIG. 2.

[0034]

When the circuit in the first embodiment is a single unit, the second embodiment uses two of these units, and corresponds to a so-called single-pole double-throw (SPDT) switch, in which two spiral inductors L1, L2 are connected between the source and drain of MOSFET T1 and between the source and drain of MOSFET T2.

[0035]

The second embodiment includes enhancement-type n-channel MOSFET T1 and MOSFET T2, DC component-removing capacitances C1 and C2 with one end connected to the source and drain of MOSFET T1, DC component-removing capacitances C3 and C4 with one end connected to the source and drain of MOSFET T2, high resistance Rg1 connected at one end to the gate of MOSFET T1, high resistance Rd1 connected at one end to either the source or drain of MOSFET T1, high resistance Rg2 connected at one end to the gate of MOSFET T2, high resistance Rd2 connected at one end to either the source or drain of MOSFET T1, a CMOS inverter circuit IN1 consisting of p-channel MOSFET PT1 and n-channel MOSFET NT1 in which the input terminals are connected to the other ends of resistance Rg1 and resistance Rg2, and the output terminals are connected between the other ends of resistance Rd1 and resistance Rg2, and as mentioned above, spiral inductors L1 and L2 connected, respectively, between the source and drain of MOSFET T1 and between the source and drain of MOSFET T2.

[0036]

The other end of capacitance C1 is connected to terminal RF_1, which is to be connected to a high-frequency signal line, and the other end of capacitance C4 is connected to terminal RF_2, which is to be connected to a high-frequency signal line.

[0037]

The connection point between the other end of capacitance C2 and the other end of capacitance C3 is connected to common terminal RF_COM.

[0038]

Terminal GND connected to the CMOS inverter circuit IN1 is a ground terminal, and terminal Vcc is a power supply voltage Vcc terminal.

[0039]

Control terminal Vcont, which supplies voltage Vcont for control of switching, is connected to the input terminal of the CMOS inverter circuit IN1.

[0040]

Resistance Rg1, Rg2, Rd1, and Rd2 is resistance with a value of around 10kΩ, for example, which is large enough to keep high-frequency signals from leaking.

[0041]

Operation of the second embodiment, which has the configuration described above, will now be explained.

[0042]

In the second embodiment, the signal path is switched based on control voltage Vcont between common terminal RF_COM and high-frequency signal terminal RF_1 or between common terminal RF_COM and high-frequency signal terminal RF_2.

[0043]

Spiral inductor L1 is designed to resonate in parallel with the OFF-capacitance of MOSFET T1 and the frequency of the high-frequency signal RF, and similarly, spiral inductor L2 is designed to resonate in parallel with the OFF-capacitance of MOSFET T2 and the frequency of the high-frequency signal RF.

[0044]

Here, the power supply voltage Vcc is 3 V and the threshold voltage Vth of both MOSFET T1 and MOSFET T2 is 0.7 V.

[0045]

A2) When control voltage Vcont is 0 V

The voltage of 0 V at the input terminal side of the CMOSFET inverter circuit IN1 is applied to the gate of transistor T1 and the source of transistor T2, and the voltage Vcc of 3 V at the output terminal is applied to the gate of transistor T2 and the source of transistor T1. MOSFET T1 is in the OFF state, and T2 is in the ON state.

[0046]

The conductivity between terminal RF_1 and terminal RF_COM is cut off, and conductivity between terminal RF_2 and terminal RF_COM is established.

[0047]

Here, because the OFF capacitance of MOSFET T1 and the spiral inductor L1 are designed to resonate in parallel at the frequency of high-frequency signals RF, sufficiently high isolation is realized in the OFF state.

[0048]

B2) When control voltage Vcont is 3 V

MOSFET T1 is in the ON state, and MOSFET T2 is in the OFF state. Thus, conductivity between terminal RF_1 and terminal RF_COM is established, and conductivity between terminal RF_2 and terminal RF_COM is cut off.

[0049]

The OFF-capacitance of MOSFET T2 and spiral inductor L2 are designed to resonate in parallel at the frequency of high-frequency signals RF, realizing sufficiently high isolation.

[0050]

In the second embodiment, as in the first embodiment, when either MOSFET T1 or MOSFET T2 is turned ON, low ON-resistance is realized because Vgs - Vth is sufficiently high at 2.3 V.

[0051]

Meanwhile, Vgs - Vth in the MOSFETs in the OFF state is sufficiently low at -3.7 V, and the maximum allowable input power is sufficiently high (27.38 dBm).

[0052]

If higher maximum allowable input power is required, MOSFETs T1 and T2 may be stacked vertically or a multi-gate structure may be used.

[0053]

Note that the spiral inductors L1, L2 may be configured as external components.

[0054]

(3) Third Embodiment

The configuration of the high-frequency semiconductor switching circuit in third embodiment of the present invention is shown in FIG. 3.

[0055]

The third embodiment is a so-called shunt-type SPDT switch, in which the MOSFET T1, capacitances C1, C2, resistances Rg1, Rd1, and inverter circuit IN1 in the first embodiment form a single unit, and four such units share an inverter circuit IN1.

[0056]

In other words, the first unit has MOSFET T1, capacitances C1 and C2, and resistances Rg1 and Rd1, and shares inverter circuit IN1, the second unit has MOSFET T2, capacitances C3 and C4, and resistances Rg2 and Rd2, and shares inverter circuit IN1, the second [sic] unit has MOSFET T3, capacitances C5 and C6, and resistances Rg3 and Rd3, and shares inverter circuit IN1, and the second [sic] unit has MOSFET T4, capacitances C7 and C8, and resistances Rg4 and Rd4, and shares inverter circuit IN1.

[0057]

In addition, terminals RF_1 and RF_2 which are to receive input from high-frequency signal lines, are connected, respectively, to the connection points at one end of each of capacitances C1 and C5, and the connection points at one end of each of capacitances C4 and C7.

[0058]

The GND_1 and GND_2 grounding terminals are connected to one end of each of capacitances C6 and C8.

[0059]

The GND terminal connected to the CMOS inverter circuit IN1 is a ground terminal, and terminal Vcc is a power supply voltage Vcc terminal.

[0060]

Control terminal Vcont, which supplies voltage Vcont to control switching, is connected to the input terminal of the CMOS inverter circuit IN1.

[0061]

In addition, resistances Rg1 to Rg4 and Rd1 to Rd4 are each resistances with a value of around 10 kΩ, for example, which is large enough to keep high-frequency signals from leaking.

[0062]

Operation of the fourth embodiment, which has the configuration described above, will now be explained.

[0063]

The signal path is switched between the two high-frequency signal input terminals RF_1 and RF_2, relative to the single common high-frequency signal input terminal RF_COM.

[0064]

As in the first and second embodiments, the power supply voltage Vcc is 3 V, and the threshold voltage Vth of each of MOSFETs T1 to T4 is 0.7 V.

[0065]

A3) When control voltage Vcont is 0 V

When a control voltage Vcont of 0 V is inputted to the input terminal of inverter circuit IN1, MOSFETs T1 and T4 turn OFF. Power supply voltage Vcc of 3 V is outputted from the output terminal of the inverter circuit IN1, and MOSFETs T2 and T3 are turned ON.

[0066]

This causes conductivity between terminal RF_1 and terminal RF_COM to be cut off, and conductivity between terminal RF_2 and terminal RF_COM to be established.

[0067]

B3) When control voltage Vcont is 3 V

MOSFET T1 and MOSFET T4 are turned ON, and MOSFET T2 and MOSFET T3 are turned OFF.

[0068]

As a result, there is conductivity between terminal RF_1 and terminal RF_COM, and conductivity between terminal RF_2 and terminal RF_COM is cut off.

[0069]

In the third embodiment, as in the first embodiment, Vgs - Vth of the MOSFETs in the ON state is sufficiently high at 2.3V, and low ON-resistance is realized.

[0070]

Also, Vgs - Vth in the MOSFETs in the OFF state is sufficiently low at -3.7 V, and the maximum allowable input power is sufficiently high (27.38 dBm).

[0071]

If higher maximum allowable input power is required, MOSFETs T1 to T4 may be stacked vertically or a multi-gate structure may be used.

[0072]

The following is a comparison of the high-frequency semiconductor switching circuit in the third embodiment with a comparative example.

[0073]

FIG. 4 shows the configuration of the shunt-type SPDT switch in the comparative example.

[0074]

The source and drain of MOSFET T1 for switching are connected between a common high-frequency input terminal RF_COM and one of the high-frequency input terminals RF_1, and the source and drain of MOSFET T1 [sic] for switching are connected between high-frequency input terminal RF_COM and one of the high-frequency input terminals RF_1.

[0075]

The source and drain of MOSFET T3 for shunting are connected between terminal RF_1 and ground terminal GND_1, and the source and drain of MOSFET T4 for shunting are connected between terminal RF_2 and ground terminal GND_2.

[0076]

The input terminal of the inverter circuit IN1, receives input of control voltage Vcont, is connected via resistance Rg1 and resistance Rg4 to the gates of MOSFETs T1 and T4, and the output terminal of the inverter circuit IN1 is connected via resistance Rg2 and resistance Rg3 to the gates of MOSFETs T2 and T3.

[0077]

Capacitance C1 to C5 are connected between terminals RF_1, RF_2, RF_COM, GND_1, and GND_2 and one end of each MOSFET.

[0078]

In this comparative example, an intermediate potential Vbias is applied as a bias potential to one end of each of transistors T1 to T4 via resistance Rdd1 to Rdd3.

[0079]

When the power supply voltage Vcc is 3 V and the threshold voltage Vth is 0.7 V, as in the first to third embodiments, and the intermediate potential Vbias is 1.5 V, the value of Vgs - Vth is calculated as follows.

[0080]

A0) When turned ON

Vgs – Vth = 3 - 1.5 - 0.7 = 0.8 V

This value is lower than the 2.3V in the first to third embodiments, and so the ON-resistance is higher than the first to third embodiments.

[0081]

B0) When turned OFF

Vgs – Vth = 0 - 1.5 - 0.7 = -2.2 V

The values for the first to third examples are -3.7 V, and the maximum allowable input power is lower in the comparative example.

[0082]

As described above, in the first to third embodiments, the maximum allowable input power is increased while the ON-resistance is decreased.

[0083]

Three embodiments of the present invention, namely, the first to third embodiments, were described above, but the same effects can be realized by any switch configured using multiple units of the circuit shown in the first embodiment.

[0084]

In addition, CMOS switches formed using silicon-on-insulator (SOI) substrates generally have excellent high-frequency characteristics, and the use of SOI is also effective in the present invention.

[0085]

In the explanation of the first to third embodiments, the power supply voltage Vcc was 3 V, but the maximum allowable input power will increase when a higher power supply voltage is used.

[0086]

It is also effective to increase the maximum allowable input power by boosting the externally supplied power supply voltage Vcc using a separately provided charge pump circuit and supplying the boosted power to the power supply terminal Vcc.

[0087]

The present invention is not limited to the capacitance used in the first to third embodiments in terms of configuration, and use of a metal-insulator-metal (MIM) configuration with excellent high-frequency characteristics can further improve high-frequency characteristics. It is also desirable to take into consideration the values of parasitic inductance in bonding wires, etc., and to set the value so that it resonates in series with them.

[0088]

Also, when configuring an SPnT switch (where n is an integer equal to or greater than 3), in order to reduce the number of control terminals, the logic circuits such as the inverter circuit in the first to third embodiments may be configured with a CMOS circuit and integrated on the same semiconductor substrate.

[Brief Description of the Drawings]

[0089]

[FIG. 1]

FIG. 1 is a circuit diagram showing the configuration of the high-frequency semiconductor switching circuit in the first embodiment of the present invention.

[FIG. 2]

FIG. 2 is a circuit diagram showing the configuration of the high-frequency semiconductor switching circuit in the second embodiment of the present invention.

[FIG. 3]

FIG. 3 is a circuit diagram showing the configuration of the high-frequency semiconductor switching circuit in the third embodiment of the present invention.

[FIG. 4]

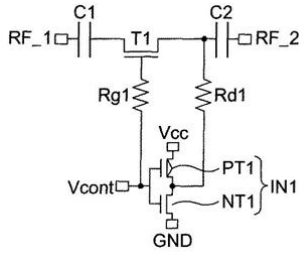
FIG. 4 is a circuit diagram showing the configuration of a high-frequency semiconductor switching circuit of the prior art.

[Reference Numbers]

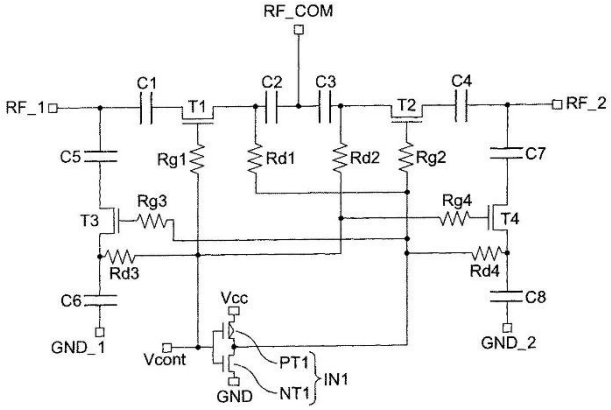
[0090]

Rg1-Rg4, Rd1-Rd4: High-frequency signal blocking resistance
C1-C8: DC component removing capacitance
T1-T4: Enhancement-type n-channel MOSFETs
RF_COM: High-frequency signal input terminal
RF_1, RF_2: Shared high-frequency signal input terminals
GND_1, GND_2: High-frequency ground terminals
GND: Ground terminal
Vcc: Power supply voltage terminal
Vcont: Control terminal
PT1: p-channel MOSFET
NT1: n-channel MOSFET
IN1: CMOS inverter circuit

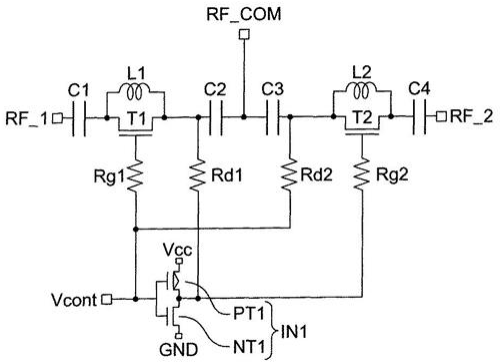
[FIG. 1]



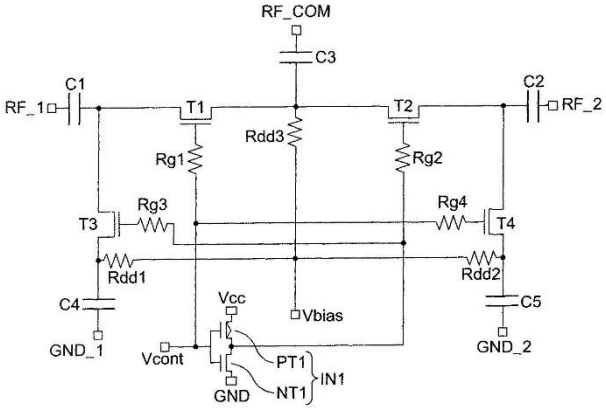
[FIG. 3]



[FIG. 2]



[FIG. 4]



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(72) Inventor Toshiki SESHIMO
Microelectronics Center, Toshiba Corporation, 1, Komukai, Toshiba-cho, Saiwai-ku, Kawasaki-shi, Kanagawa-ken

(72) Inventor Yoshitomo SAKAE
Microelectronics Center, Toshiba Corporation, 1, Komukai, Toshiba-cho, Saiwai-ku, Kawasaki-shi, Kanagawa-ken

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Certification of Accuracy of Translation

Sun IP Project # 25-291

I, Frank McGee, hereby declare:

That I possess advanced knowledge of the Japanese and English languages. The attached Japanese into English translation of JP2006121217A has been translated by me and to the best of my knowledge, is a true and accurate translation.

Declarant hereby acknowledges that any willful false statements made in this Declaration are punishable by fine or imprisonment, or both. Furthermore, all statements made of Declarant's own knowledge are true, and all statements made on information and belief are believed to be true.

January 24, 2025