

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KANGXI COMMUNICATION TECHNOLOGIES (SHANGHAI) CO., LTD.
Petitioner,

v.

SKYWORKS SOLUTIONS, INC.
Patent Owner.

Case No. IPR2024-01457
U.S. Patent No. 9,148,194

PATENT OWNER'S DEMONSTRATIVES FOR ORAL ARGUMENT

Kangxi Communication Technologies (Shanghai) Co., Ltd. v.
Skyworks Solutions, Inc.

Patent Owner's Demonstratives

March 6, 2026

IPR2024-01456, -01457

U.S. Patent Nos. 9,450,579, 9,148,194

A graphic on the right side of the slide consisting of a series of white, stylized, interconnected diamond or hexagonal shapes that form a larger, abstract geometric pattern, resembling a molecular structure or a network diagram.

SKYWORKS®

Grounds

	IPR2024-01456 ('579 Patent)	IPR2024-01457 ('194 Patent)
Ground 1	Claims 1-3, 7-9, 13-15 are obvious over Huang in view of the Knowledge of POSITAs	Claims 1-11 are obvious over Huang in view of the Knowledge of POSITAs
Ground 2	Claims 1-3, 7-9, 13-15 are obvious over Seshimo in view of the Knowledge of POSITAs	Claims 1-11 are obvious over Seshimo in view of the Knowledge of POSITAs

Summary

- **Neither Huang nor Seshimo disclose or render obvious “inhibiting a low-frequency blocker signal from mixing with a fundamental-frequency signal in the RF switch”**
 - '579 patent, claims 7-9
 - '194 patent, claims 2, 8
- **Neither Huang nor Seshimo disclose or render obvious the claimed capacitors formed on the same semiconductor substrate as the RF switches**
 - '579 patent, claims 1-3, 15
 - '194 patent, claims 5-6, 9-10

The '579 and '194 Patents

'579 and '194 Patents

The patents improve IMD performance

Intermodulation Distortion

A switching device performance parameter can further include a measure of intermodulation distortion (IMD) performance. Intermodulation distortion (IMD) can be a measure of non-linearity in an RF switching device.

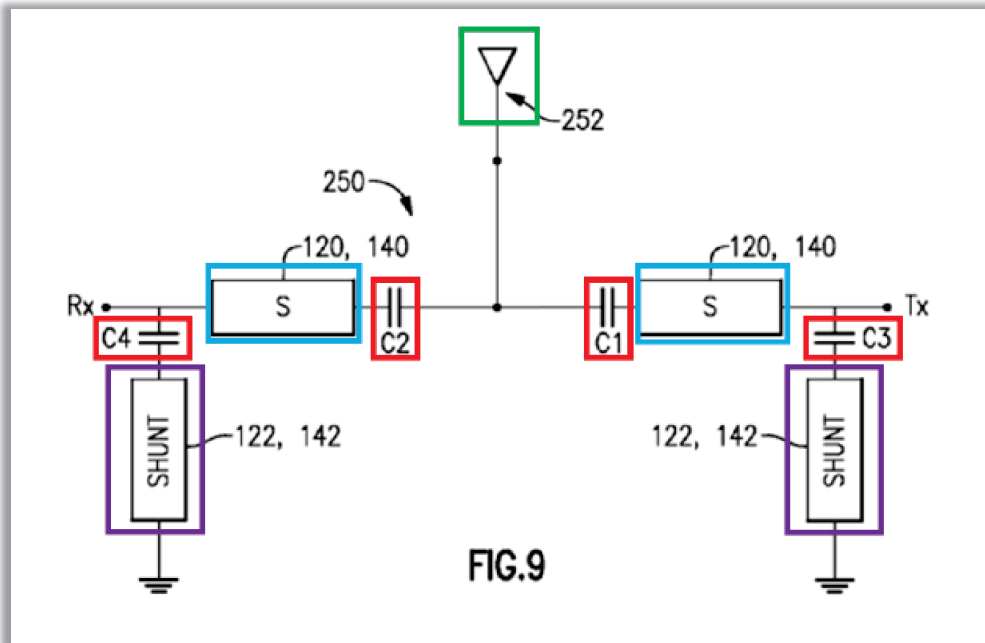
IMD can result from two or more signals mixing together and yielding frequencies that are not harmonic frequencies. For example, suppose that two signals have fundamental frequencies f_1 and f_2 ($f_2 > f_1$) that are relatively close to each other in frequency space. Mixing of such signals can result in peaks in frequency spectrum at frequencies corresponding to different products of fundamental and harmonic frequencies of the two signals. For example, a second-order intermodulation distortion (also referred to as IMD2) is typically considered to include frequencies $f_1 + f_2$, $f_2 - f_1$, $2f_1$, and $2f_2$. A third-order IMD (also referred to as IMD3) is typically considered to include $2f_1 + f_2$, $2f_1 - f_2$, $f_1 + 2f_2$, $f_1 - 2f_2$. Higher order products can be formed in similar manners.

a multi-band and/or multi-mode environment. In some embodiments, improvement of a switching device IMD performance can improve the IMD performance of a wireless communication system operating in a multi-mode and/or multi-band environment.

POR, 4-5; Sur-Reply, 7-8; Ex-1001, 6:20-7:13

'579 and '194 Patents

The claimed capacitors inhibit low-frequency blocker signals to improve IMD performance



The switching configuration of FIG. 9 is shown to include capacitors to inhibit a low-frequency blocker from mixing with a fundamental frequency. For example, a capacitor C1 is provided between the antenna node and the switch arm S of the Tx throw. Similarly, a capacitor C2 is provided between the antenna node and the switch arm S of the Rx throw. For the shunt arms, a capacitor C3 is provided between the Tx node and its shunt switch arm. Similarly, a capacitor C4 is provided between the Rx node and its shunt switch arm. In some embodiments, a shunt arm may or may not be provided for the Rx node. With the foregoing capacitors, a low-frequency jammer signal can be blocked or reduced from mixing with any ON or OFF paths. This can lead to improvement in IMD performance, especially for low-frequency blocker signals.

POR, 6-8; Ex-1001, 9:39-53, Fig. 9

'579 and '194 Patents

'579 Patent, claim 7

7. A method for operating a radio-frequency (RF) device, the method comprising:
providing an RF device including a first switch circuit connected between an antenna node and a transmit node, a second switch circuit connected between the antenna node and a receiver node, a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node, a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node, and a first shunt arm connected to the first switch circuit and the transmit node, the first shunt arm including a third switch circuit connected to ground;
controlling an RF switch of the RF device by placing the first switch circuit in an ON state and placing the third switch circuit in an OFF state; and
inhibiting a low-frequency blocker signal from mixing with a fundamental-frequency signal in the RF switch using the first capacitor.

'194 Patent, claim 2

1. A radio-frequency (RF) switch system comprising:
a first switch circuit connected between an antenna node and a transmit node;
a second switch circuit connected between the antenna node and a receive node;
a first capacitor connected in series with the first switch circuit between the first switch circuit and the antenna node;
a second capacitor connected in series with the second switch circuit between the second switch circuit and the antenna node;
a first shunt arm connected to the first switch circuit and the transmit node, the first shunt arm including a third switch circuit connected to ground; and
a second shunt arm connected to the second switch circuit and the receive node, the second shunt arm including a fourth switch circuit connected to ground.
2. The switch system of claim 1 wherein at least one of the first and second capacitors is configured to inhibit a low-frequency blocker signal from mixing with a fundamental-frequency signal in the switch.

Ex-1001 ('579), cl. 7; Ex-1001 ('194), cls. 1-2

'579 and '194 Patents

'579 Patent, claim 1

1. A semiconductor die comprising:
 - a semiconductor substrate;
 - a first switch circuit formed on the semiconductor substrate connected between an antenna node and a transmit node;
 - a second switch circuit formed on the semiconductor substrate and connected between the antenna node and a receive node;
 - a first capacitor formed on the semiconductor substrate and connected in series with the first switch circuit between the first switch circuit and the antenna node;
 - a second capacitor formed on the semiconductor substrate and connected in series with the second switch circuit between the second switch circuit and the antenna node; and
 - a first shunt arm formed on the semiconductor substrate and connected to the first switch circuit and the transmit node, the first shunt arm including a third switch circuit connected to ground.

'194 Patent, claim 5

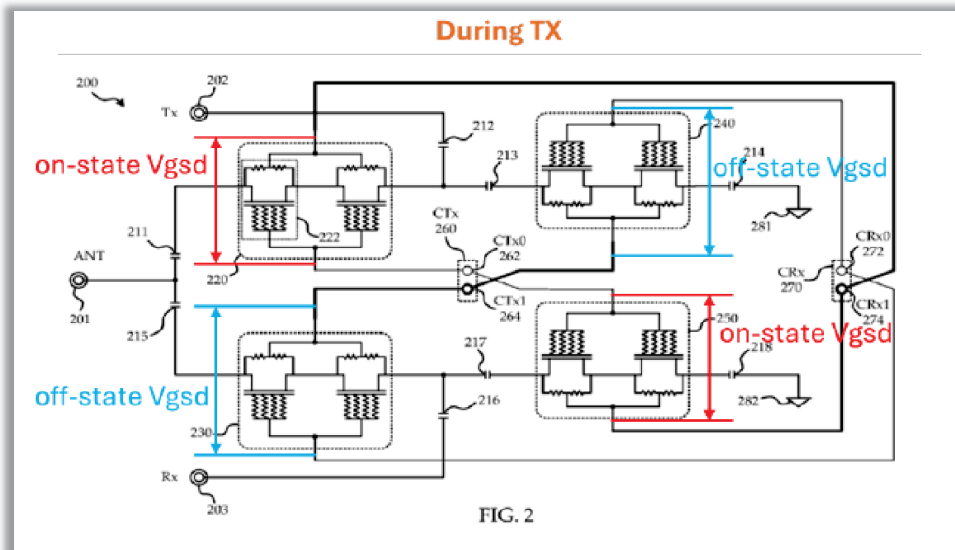
5. A method for fabricating a semiconductor die, the method comprising:
 - providing a semiconductor substrate;
 - forming a first switch circuit on the semiconductor substrate so as to be connected between an antenna node and a transmit node;
 - forming a second switch circuit on the semiconductor substrate so as to be connected between the antenna node and a receive node;
 - forming a first capacitor on the semiconductor substrate so as to be connected in series with the first switch circuit between the first switch circuit and the antenna node;
 - forming a second capacitor on the semiconductor substrate so as to be connected in series with the second switch circuit between the second switch circuit and the antenna node;
 - forming a first shunt arm connected to the first switch circuit and the transmit node, the first shunt arm including a third switch circuit connected to ground; and
 - forming a second shunt arm connected to the second switch circuit and the receive node, the second shunt arm including a fourth switch circuit connected to ground.

Ex-1001 ('579), cl. 1; Ex-1001 ('194), cl. 5

Ground 1: Huang

Huang's Teachings

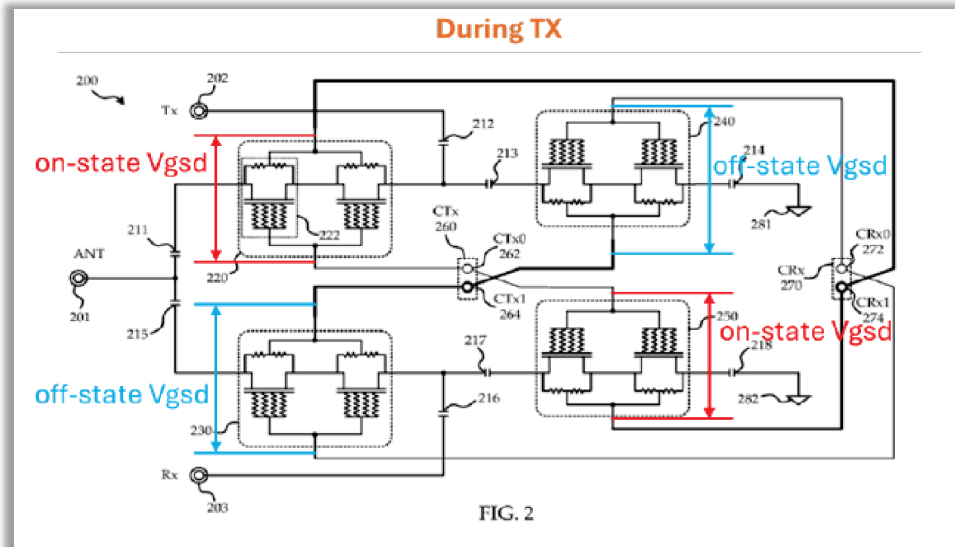
Huang teaches reducing insertion loss and improving switch linearity by choosing particular on-state and off-state bias voltages (V_{gsd})



[0039] While maximizing the on-state V_{gsd} for the on-state FET group switches and fully maximizing the off-state V_{gsd} of the off-state FET group switches achieves respectively low insertion loss and high isolation where and as needed, a quality of the signals passing through the transmit-receive switch depends upon, amongst other things, the particular voltages chosen for off-state V_{gsd} and on-state V_{gsd} of the FETs within the switch.

Huang's Teachings

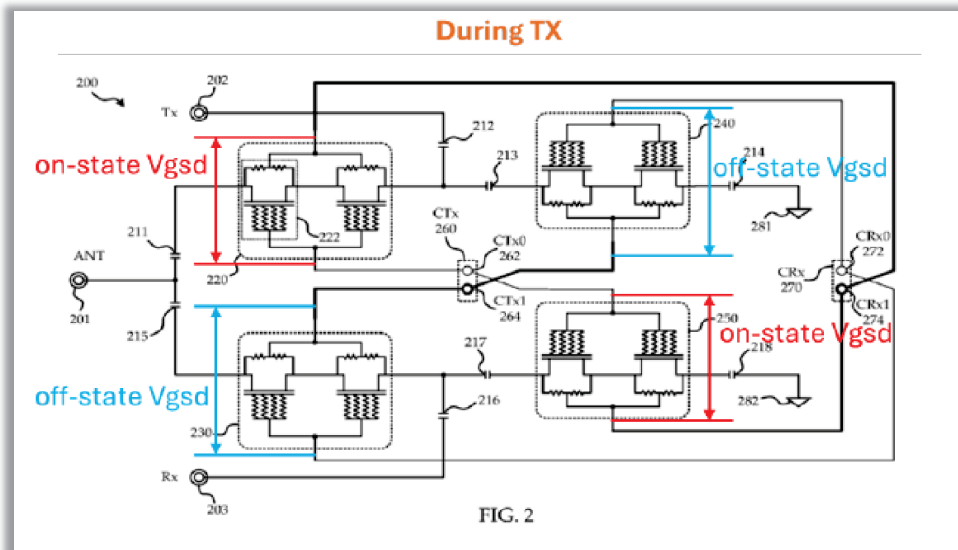
Huang teaches off-state V_{gsd} between 1.1-1.5V achieves low harmonic emissions and sufficient linearity



[0042] The spurious third harmonic emissions has a more steep slope versus power drive than that of the spurious second harmonic emissions, but both kinds of spurious harmonic emissions increase with increasing off-state V_{gsd} beyond a certain bias voltage. Nonlinear effects in the high power switch were also found to increase with increasing off-state V_{gsd} of the off-state FET group switches. For a 2.5 V SOI, low levels of harmonic emissions and sufficient linearity, were found at off-state V_{gsd} of 1.5 V and less where the channel linking the source and drain is not in strong inversion. Considering the need for isolation, the operating off-state V_{gsd} level for the turned off FET group switches is chosen to be 1.1 V-1.5 V. In general, the off-state V_{gsd} level should be

Huang's Teachings

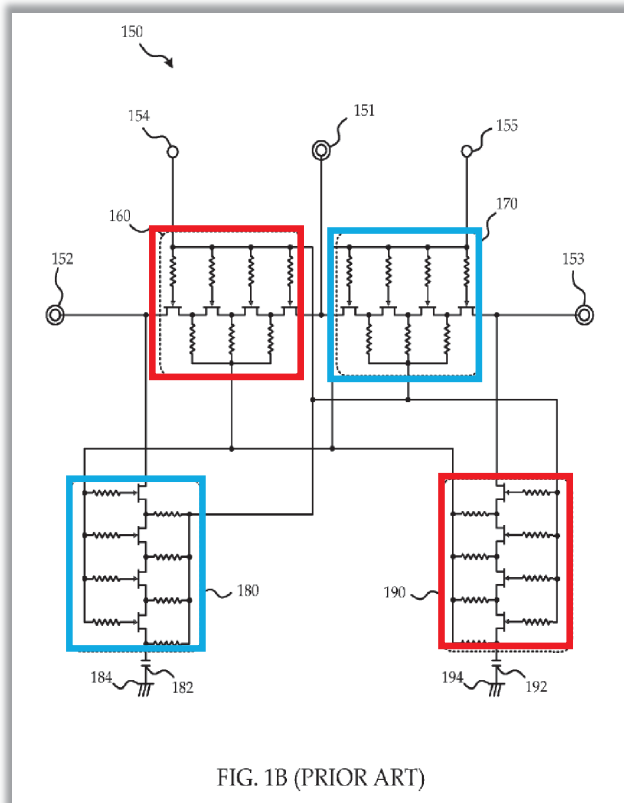
Huang teaches on-state V_{gsd} between 2.0-2.5V achieves low insertion loss and good linearity



[0043] For the on-state FET group switches, lower harmonic emissions were found above a voltage level close to the gate to source breakdown voltage. With the 2.5V SOI technology, 2.0-2.5 V of on-state V_{gsd} was found to exhibit a very low insertion loss, and good linearity. Considering the reliability constraint of 2.5 V, the operating on-state V_{gsd} level for the turned on FET group switches is chosen to be 2.0V-2.5 V.

Huang's Teachings

Huang improves prior art that taught full-on, full-off biasing



[0011] When the first biasing terminal 154 is V_{HI} and the second biasing terminal 155 is V_{LO} , the first and fourth FET group switches 160, 190 are biased to full on while the second and third group switches 170, 180 are biased with reverse polarity to full off. Consequently, the pole 151 is strongly coupled with the first input/output terminal 152 while being strongly isolated from the second input/output terminal 153, the first input/output terminal 152 is strongly isolated from ground 184 while the second input/output terminal 153 is strongly coupled, or shunted, to ground 194.

POR, 23-27; Ex-1005 ¶ 11, Fig. 1B

Huang's Teachings

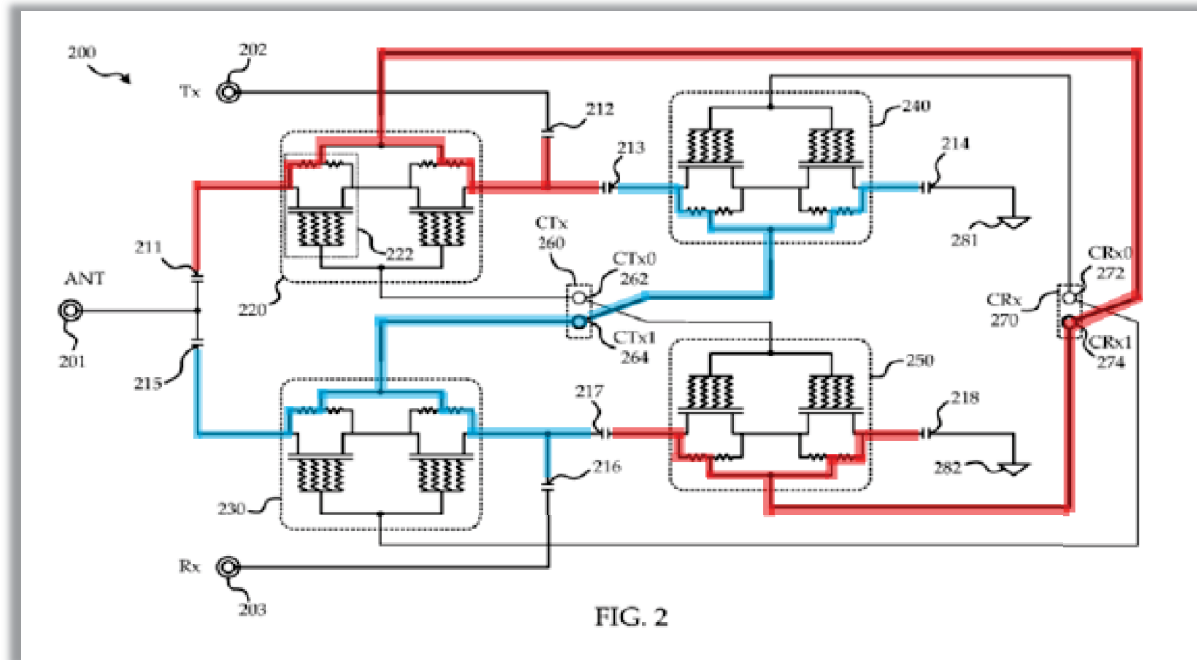
Huang selects particular on-state and off-state V_{gsd} voltages because “little advantage is gained from” prior art’s full-on, full-off biasing

[0040] The inventors have found in the implementation of a high power transmit-receive switch using silicon on insulator (SOI) which has a breakdown voltage lower than the switch control voltage level and utilizing a single or a series of connected MOSFETs and/or MultiGate FETs (MUGFETs), that improved signal quality is obtained from biasing the FETs at a level other than at the largest possible bias within the reliability/breakdown limits of operation.

[0041] The inventors have observed that applying off-state V_{gsd} to the off-state FET group switches beyond a certain voltage level has very little effect on the isolation obtained therefrom and hence little advantage is gained from maximizing the off-state V_{gsd} of the off-state FET group switches to the same level that the on-state FET group switches are biased, except perhaps for simplicity of design. The inventors have also observed that at relatively high signal strengths, spurious harmonic emissions were emanating from the off-state FET group switches and nonlinear effects in the switching circuit resulted.

POR, 11-12; Ex-1005 ¶¶ 40-41

Huang's capacitors isolate signal path to individually bias transistors with the selected voltages (1.0-1.5 V off-state and 2.0-2.5 V on-state)



POR, 21-22; Ex-1005 ¶¶ 44-45, Fig. 2

Huang's Teachings

Huang's capacitors ensure the selected DC bias voltages (V_{gsd}) are applied



Dr. Wentzloff

A. Huang teaches improving the linearity of the switch as well as improving insertion loss and includes DC blocking capacitors in order to apply different DC voltages to the switches to improve their linearity.



Dr. Larson

A Yeah, optimizing the VGSD is about -- what Huang talks about is, yeah, the DC bias of the gate and source/drain regions in order to, you know, optimize switch performance.

POR, 12, 28; Ex-1050, 195:22-196:4; Ex-2003, 105:19-22

Huang Does Not Disclose Claimed “inhibiting”

- **Huang does not teach or suggest that its capacitors inhibit low-frequency blocker signals to improve intermodulation distortion**
- **Huang’s capacitors are DC blocking capacitors for isolating DC bias voltages**
- **Petitioner’s obviousness analysis fails to present any reason a POSITA would have been motivated to modify Huang’s capacitors to inhibit a low frequency blocker signal**

Huang Does Not Disclose Claimed “inhibiting”

Petitioner concedes Huang discloses only “positioning” of capacitors

Petitioner’s Reply

Huang discloses positioning, in SPDT switch 200 (the RF switch), (i) blocking capacitor 211 (the first capacitor) between antenna 201 (the antenna node) and Tx series FET group switch 220 (the first switch circuit), and (ii) blocking capacitor 215 between antenna 201 and Rx series FET group switch 230. Pet. 48-49.



Dr. Larson

A Yeah, I have no opinion on anticipation in my declaration. My declaration only covers issues of obviousness.

POR, 31; Sur-reply, 9-10; Reply, 6; Ex-2003, 31:11-13

Petitioner Relies on Hindsight, Not Huang's Teachings

In the context of Huang, the “judiciously chosen resistors and capacitors” are “to ensure” low insertion loss and high isolation by optimizing bias voltages of transistors

Petition

Huang also discloses the importance of selecting the “arrange[ment]” of “groups of FETs” and “judiciously chosen... capacitors”, and of selecting the biasing voltages of the FETs when in “on” and “off” states, in “a high power transmit-receive switch using... SOI” to achieve, for example, “low insertion loss along the signal path”, “high isolation from the off paths”, “reduce[d] spurious harmonic emissions”, and “improve[d] linearity” for the switch. EX-1005, [0002]-[0003], [0039]-[0040], [0043]-[0045], [0055]-[0059]; EX-1003, ¶111. Moreover, Huang expressly refers to capacitor

Huang

[0003] Many of the main advances in semiconductor-based transmit-receive switches have been with respect to isolation and insertion loss. Groups of FETs are arranged in the switch along with judiciously chosen resistors and capacitors to ensure low insertion loss along the signal path and high isolation from the off paths. One general approach utilizes, instead of a single FET switch along each alternative path, a group of FET switches in series. This general approach moreover does not simply turn the FETs on and off by utilizing only a voltage at the gate, but instead biases both the gate and the source/drain in a forward and reverse manner to turn the FETs full-on and full-off respectively.

POR, 16-17, 22-31; Petition, 49; Ex-1005 ¶ 3

Petitioner Relies on Hindsight, Not Huang's Teachings

Dr. Larson repeats the Petition

Petition

Huang also discloses the importance of selecting the “arrange[ment]” of “groups of FETs” and “judiciously chosen... capacitors”, and of selecting the biasing voltages of the FETs when in “on” and “off” states, in “a high power transmit-receive switch using... SOI” to achieve, for example, “low insertion loss along the signal path”, “high isolation from the off paths”, “reduce[d] spurious harmonic emissions”, and “improve[d] linearity” for the switch. EX-1005, [0002]-[0003], [0039]-[0040], [0043]-[0045], [0055]-[0059]; EX-1003, ¶111. Moreover, Huang expressly refers to capacitor

Dr. Larson

111. Huang also discloses the importance of selecting the “arrange[ment]” of “groups of FETs” and “judiciously chosen... capacitors”, and of selecting the biasing voltages of the FETs when in “on” and “off” states, in “a high power transmit-receive switch using... SOI” to achieve, for example, “low insertion loss along the signal path”, “high isolation from the off paths”, “reduce[d] spurious harmonic emissions”, and “improve[d] linearity” for the switch. EX-1005, [0002]-[0003], [0039]-[0040], [0043]-[0045], [0055]-[0059].

POR, 17-18; Petition, 49; Ex-1003 ¶ 111

Petitioner Relies on Hindsight, Not Huang's Teachings

Dr. Larson agreed that Huang is focused on optimizing bias voltages

Q And so then if you can look at the next paragraph, please. And in particular, I'd like to focus on the last sentence of paragraph 3. That sentence states that a general approach moreover does not simply turn the FETs on and off by utilizing only a voltage at the gate, but instead biases both the gate and the source/drain in a forward and reverse manner to turn the FETs full on and full off respectively. Correct?

A That's what it says, yes.

A Well, I wouldn't put it that way. I mean, what Huang -- one of the things Huang talks about is optimizing the VGSD of the devices in the ON and OFF states to get the best performance possible. So it's -- and I think this was stated in the abstract as well.

Q And so to clarify that, optimizing VGSD, does that refer to setting the bias voltage of the FETs?

A Yeah, optimizing the VGSD is about -- what Huang talks about is, yeah, the DC bias of the gate and source/drain regions in order to, you know, optimize switch performance.

POR, 17-18, 28, 34; Ex-2003, 104:21-105:22

Petitioner's Obviousness Analysis is Deficient

Petition incorrectly relies on “general knowledge” for the claimed “inhibiting”

Moreover, given this fundamental, frequency-dependent impedance characteristic of capacitors, the typical (picofarad) capacitor values selected for RF switches in Huang's disclosed use cases, and the known solution—having “the switch see[] an open circuit at the blocker frequencies”—to the well-known low-frequency, “out-of-band blocker” signal problem in non-linear RF switches, POSITAs understood Huang's disclosed implementation of blocking capacitor 211 in SPDT switch 200 as being a high-pass filter that would “inhibit[] a low-frequency blocker signal from mixing with a fundamental frequency signal in the RF switch.” *Id.*, §V.F.1 (EX-1012, 231-234, 175-176; EX-1027, 82-83, 50; EX-1014, 20, 30, 29-32, 36-37, 39-40, 42, FIGS. 1.52-1.55, 1.56(A); EX-1043, 128-129, 137-139, 236-238, FIGS. 5-17(A), 8-17(B), 8-17(D), 8-18(B), 8-18(D); EX-1011, 2615-2618, FIG. 9A; EX-1024, 3-4; EX-1026, [0049]; EX-1031, 8-9, FIG. 13; EX-1010, [0040]; EX-1044, 1-2; EX-1029, 36-39; EX-1032, 1-2; EX-1033, 1; EX-1042, 96, 172, 180, 227, 275, 286; EX-1017, [0025]); §V.F.2 (EX-1039, FIG. 5, 2-6, 8-12 (*citing* EX-1040, 3-6, FIGS. 3-4); EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1045, 1, EX-1049, p.3); EX-1003, ¶114.

(b) SCOPE.—

35 U.S.C. § 311(b)

A petitioner in an inter partes review may request to cancel as unpatentable 1 or more claims of a patent only on a ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or printed publications.

Director Memorandum (July 21, 2025)

The United States Patent and Trademark Office (USPTO) will enforce and no longer waive the requirement of 37 C.F.R. § 42.104(b)(4) (Rule 104(b)(4)) that a petition for inter partes review (IPR) “must specify where each element of the claim is found in the prior art patents or printed publications relied upon.”¹ As a practical matter, enforcement of Rule 104(b)(4) means that applicant admitted prior art (AAPA), expert testimony, common sense, and other evidence that is not “prior art consisting of patents or printed publications” (collectively, “general knowledge”) may not be used to supply a missing claim limitation. Per 35 U.S.C. § 312(a)(4), the Board shall deny an IPR petition that fails to comply with Rule 104(b)(4). General knowledge may still be

POR, 32; Sur-reply, 2-3; Petition, 50

Petitioner's Obviousness Analysis Is Deficient

Petitioner's "simple design choice" argument ignores different solutions taught by Huang and the '579 and '194 patents

'579 and '194 patents

a multi-band and/or multi-mode environment. In some embodiments, improvement of a switching device IMD performance can improve the IMD performance of a wireless communication system operating in a multi-mode and/or multi-band environment.

Improved switching device IMD performance can be desirable for wireless communication devices operating in various wireless communication standards, for example for wireless communication devices operating in the LTE communication standard. In some RF applications, it can be desirable to improve linearity of switching devices operating in wireless communication devices that enable simultaneous transmission of data and voice communication. For example, improved IMD performance in switching devices

Huang

[0041] The inventors have observed that applying off-state V_{gsd} to the off-state FET group switches beyond a certain voltage level has very little effect on the isolation obtained therefrom and hence little advantage is gained from maximizing the off-state V_{gsd} of the off-state FET group switches to the same level that the on-state FET group switches are biased, except perhaps for simplicity of design. The inventors have also observed that at relatively high signal strengths, spurious harmonic emissions were emanating from the off-state FET group switches and nonlinear effects in the switching circuit resulted.

POR, 36-37; Sur-reply, 7-8; Ex-1001, 6:20-7:13; Ex-1005 ¶ 41

Petitioner's Obviousness Analysis Is Deficient

A different motivation and a different solution cannot be substituted by simply labeling the claimed approach a “simple design choice.”



Polaris Indus., Inc. v. Arctic Cat, Inc., 882 F.3d 1056, 1067-70, 1069 n.4 (Fed. Cir. 2018)

“[m]erely stating that a particular placement of an element is a design choice does not make it obvious.”



Hesai Tech. Co., Ltd. v. Ouster, Inc., IPR2023-01422, Paper 33, 53-54 (PTAB Mar. 13, 2025)

Putting a transformer coil **outside** would not have been an obvious design choice when the relied-on references disclose putting a transformer coil **inside** and “suggest[] that there were good reasons for doing this in their configurations.”



Xerox Corp. v. Bytemark, Inc., IPR2022-00624, Paper 9, 14-15 (PTAB Aug. 24, 2022)

“[B]locking a purchaser” would not render obvious “blocking the account of the purchaser” where the only supporting evidence is Petitioner’s expert declarant that merely repeats the Petitioner’s assertion

Sur-reply, 4-5; POR, 36-37

Petitioner's Obviousness Analysis Is Deficient

Huang's biasing allows its switches tolerate higher amplitude blocker signals



Dr. Wentzloff

Q. And so if Huang has a more linear switch, what does that mean for the mixing of signals in Huang?

A. If the switch is more linear, then that means for the, for a given amount of blocker signal and fundamental signal, the IMD would be lower. So a more linear switch implies that your switch circuit could tolerate higher amplitude blocker signals going through it because higher amplitude blocker signals and fundamentals through a more linear switch would produce smaller IMD terms.

Sur-reply, 10-11; POR, 36-37; Ex-1050, 195:8-18

Petitioner's Obviousness Analysis Is Deficient

A larger-sized capacitor works better for Huang



Dr. Wentzloff

Q. And so then if you could tolerate higher amplitude blocker signals how would a POSITA be motivated to size the capacitors in Huang?

A. Huang teaches improving the linearity of the switch as well as improving insertion loss and includes DC blocking capacitors in order to apply different DC voltages to the switches to improve their linearity.

So a POSITA implementing Huang based on those teachings would be motivated to use the largest possible value for that DC blocking capacitor with ideally the highest quality factor as well.

Sur-reply, 10-11; POR, 36-37; Ex-1050, 195:19-196:9

Petitioner's obviousness analysis is deficient



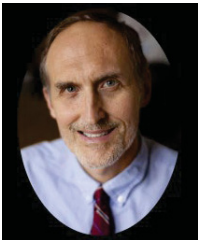
Dr. Wentzloff

Q. And would a POSITA be motivated to size the capacitors in Huang to inhibit a low frequency blocker signal from mixing with a fundamental frequency signal?

A. No. There is no mention of low frequency blockers or interact modulation distortion that I saw in Huang.

Petitioner's Obviousness Analysis Is Deficient

Petitioner fails to explain why a POSITA would (not could) depart from Huang's DC blocking, larger capacitors



Dr. Larson

element (with decreasing impedance with increasing frequency), POSITAs understood that tuning the resulting high-pass filter, *i.e.*, setting the frequency range above which **blocking capacitor 211** permits frequencies (*e.g.* the desired RF frequency) to pass essentially unimpeded, and below which (*e.g.*, the “-3dB breakpoint”) it impedes lower frequencies (*e.g.*, low-frequency “out-of-band blocker” signals), is simply a matter of picking the size capacitor that yields the desired pass/inhibit thresholds within the practical size constraints for the RF device (*e.g.*, “traditional WLAN radio”) with a reasonable expectation of success. *Id.*; see

No reply declaration was provided in response to Patent Owner's arguments

Sur-reply, 10-11; POR, 34-40; Ex-1003 ¶ 116

Petitioner's Obviousness Analysis Is Deficient

Reply mischaracterizes Dr. Wentzloff's testimony



Dr. Wentzloff

Q. And what value -- what capacitance value would be needed for first capacitor, second capacitor, and third capacitor to block DC signals?

A. Well, any value other than zero or infinity. All capacitors block DC.

Q. The patents -- would you agree that the patents assume that non-linearities will exist in the switching devices at the RF switch?

A. Oh yes, very much so. Actually, I think they rely on that.

Sur-reply, 14-15; Ex-1050, 83:9-13, 132:22-133:4

Petitioner's Obviousness Analysis Is Deficient

Reply mischaracterizes Dr. Wentzloff's testimony



Dr. Wentzloff

Q. So then is mixing of signals more or less of a problem in RF switches that are more linear?

A. For a switch that is more linear?

Q. Correct.

A. The intermodulation distortion would be less of a problem.

Petitioner's Obviousness Analysis Is Deficient

Petitioner improperly argues that any capacitor discloses the claimed inhibiting



Dr. Wentzloff

The second part is on a blocker. A POSITA would understand a blocker to mean a signal at a specific frequency that causes spurious emissions that would then degrade the performance of your radio. So not all signals are necessarily blockers. Not all low frequency signals are necessarily blockers.

Petitioner's Obviousness Analysis Is Deficient

Petitioner is not allowed to now argue a combination of Huang and Ex-1011

Petitioner's Reply

to operate.” EX-1050 169:3-170:9. And, he conceded that, in the RF field, “DC blocking capacitor” was used—in *his relied-on EX-1011*—to refer to capacitors with 10pF values that blocked DC signals, attenuated low-frequency AC signals, passed higher-frequency AC signals (2.4GHz and higher), and were formed on-chip EX-1050 168:7-169:15, 171:10-173:7 (discussing EX-1011, EX-1052, 3);

Sur-reply, 16-17; Reply, 18-19

Huang Does Not Disclose Capacitors Formed on the Same Semiconductor Substrate

- **Huang does not teach or suggest that its capacitors are formed on the same semiconductor substrate as the other claimed elements**
- **Petitioner's obviousness analysis fails to present any reason a POSITA would have been motivated to form the capacitors on the same semiconductor substrate as the other claimed elements**

Huang Does Not Disclose Capacitors Formed on the Same Semiconductor Substrate

Nowhere does Huang disclose capacitors placed on the same substrate

As the Petition explains, POSITAs understood that *Huang* discloses all of the FIG. 3 SPDT switch components are formed on a semiconductor substrate of a semiconductor die because *Huang* states “[t]he invention relates to high power semiconductor switches”, and discloses the “transistor switches” in such high power, “semiconductor-based transmit-receive switches”, including SPDT switch 200, can be “silicon-on-insulator FET switches.” Pet. 39. The Petition also

¶82. Huang states “[t]he invention relates to high power semiconductor switches”, and discloses the “transistor switches” in such high power, “semiconductor-based transmit-receive switches”, including SPDT switch 200, can be “silicon-on-insulator FET switches.” EX-1005, [0001]-[0003], Abstract, [0040], [0042]-[0043], [0122], claims 5, 19, FIG. 2; EX-1003, ¶83. Accordingly, POSITAs reading Huang would understand

Huang, claim 5

5. A method according to claim 1 wherein said transistor switches are silicon-on-insulator FET switches, and wherein said on-state V_{gsd} level is between 2.0 V and 2.5 V, and wherein the off-state V_{gsd} level is between 1.1 V and 1.5 V.

Petitioner's Reply

Petition

POR, 40-41; Sur-reply, 19-20; Reply, 24; Petition, 39

Petitioner's Obviousness Analysis Is Deficient



Dr. Wentzloff

Q. If a POSITA is motivated to make a capacitor as large as possible with the highest Q factor as possible, where would it be motivated to place the capacitor?

A. A POSITA especially at the time in 2012 would be motivated to put that capacitor off-chip because those provide the highest capacitor density and the highest quality factor of capacitance.

POR, 42-43; Sur-reply, 19-20; Ex-1050, 197:17-198:2

Ground 2: Seshimo

Seshimo Is Also Directed to Reducing Insertion Loss

Like Huang, Seshimo teaches reducing insertion loss by suppressing on-resistance

[0004]

However, when attempting to achieve a high-frequency semiconductor switching circuit using a MOSFET formed on a silicon substrate, the substrate is conductive, which causes insertion loss due to the resistance of the substrate in addition to insertion loss due to the ON-resistance of the MOSFET.

PROBLEM TO BE SOLVED BY THE INVENTION [0007]

[0007]

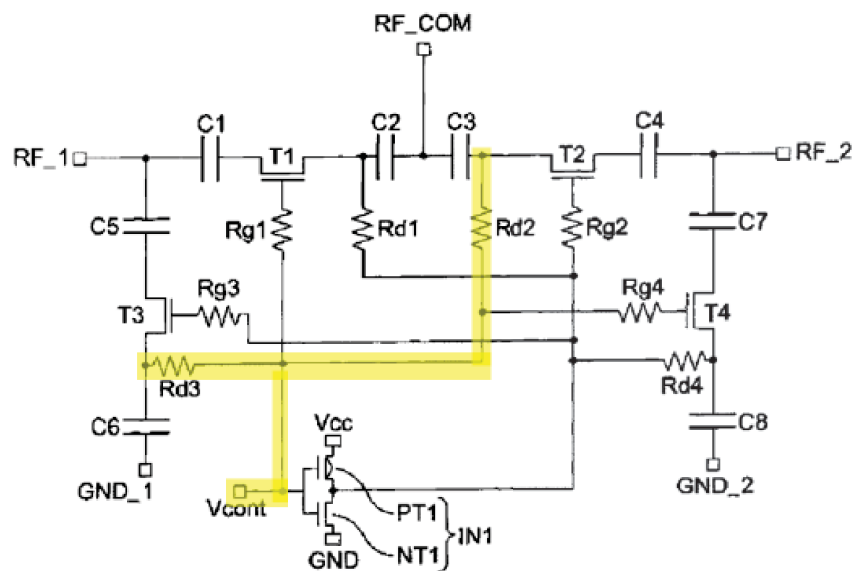
In view of the foregoing, an object of the present invention is to provide a semiconductor switching circuit capable of improving the maximum permissible input power while suppressing an increase in ON-resistance.

POR, 12-13, 47-48; EX-1007 ¶¶ 4, 7

Like Huang, Seshimo Teaches DC Biasing

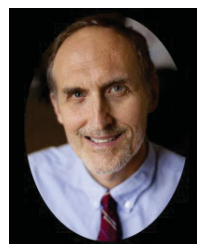
Seshimo expressly states its capacitors are for DC blocking.

FIG. 3



[0090]

Rg1-Rg4, Rd1-Rd4: High-frequency signal blocking resistance
C1-C8: DC component removing capacitance
T1-T4: Enhancement-type n-channel MOSFETs
RF_COM: High-frequency signal input terminal



Dr. Larson

Q As a person of ordinary skill in the art, would you agree that the phrase "DC component removal capacitor" is the same as DC blocking capacitor?

A I don't see any substantial difference between those two and I think a person of ordinary skill in the art would view those as essentially the same.

POR, 12-13, 47-48; Ex-2004 ¶ 90; Ex-1007 ¶ 90

Petitioner's Obviousness Analysis Is Deficient

Seshimo ground is duplicative of Huang ground

Moreover, given this fundamental, frequency-dependent impedance characteristic of capacitors, the typical (picofarad) capacitor values selected for RF switches in Huang's disclosed use cases, and the known solution—having “the switch see[] an open circuit at the blocker frequencies”—to the well-known low-frequency, “out-of-band blocker” signal problem in non-linear RF switches, POSITAs understood Huang's disclosed implementation of blocking capacitor 211 in SPDT switch 200 as being a high-pass filter that would “inhibit[] a low-frequency blocker signal from mixing with a fundamental frequency signal in the RF switch.” *Id.*, §V.F.1 (EX-1012, 231-234, 175-176; EX-1027, 82-83, 50; EX-1014, 20, 30, 29-32, 36-37, 39-40, 42, FIGS. 1.52-1.55, 1.56(A); EX-1043, 128-129, 137-139, 236-238, FIGS. 5-17(A), 8-17(B), 8-17(D), 8-18(B), 8-18(D); EX-1011, 2615-2618, FIG. 9A; EX-1024, 3-4; EX-1026, [0049]; EX-1031, 8-9, FIG. 13; EX-1010, [0040]; EX-1044, 1-2; EX-1029, 36-39; EX-1032, 1-2; EX-1033, 1; EX-1042, 96, 172, 180, 227, 275, 286; EX-1017, [0025]); §V.F.2 (EX-1039, FIG. 5, 2-6, 8-12 (*citing* EX-1040, 3-6, FIGS. 3-4); EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1045, 1, EX-1049, p.3); EX-1003, ¶114.

Huang ground

Moreover, given this fundamental, frequency-dependent impedance characteristic of capacitors, the typical (picofarad) capacitor values selected for RF switches in Seshimo's disclosed use cases, and the known solution—having “the switch see[] an open circuit at the blocker frequencies”—to the well-known low-frequency, “out-of-band blocker” signal problem in non-linear RF switches, POSITAs would understand Seshimo's disclosed implementation of capacitor C3 as being a high-pass filter that would “inhibit[] a low-frequency blocker signal from mixing with a fundamental frequency signal in the RF switch.” *Id.*, §V.F.1 (EX-1012, 231-234, 175-176; EX-1027, 82-83, 50; EX-1014, 20, 30, 29-32, 36-37, 39-40, 42, FIGS. 1.52-1.55, 1.56(A); EX-1043, 128-129, 137-139, 236-238, FIGS. 5-17(A), 8-17(B), 8-17(D), 8-18(B), 8-18(D); EX-1011, 2615-2618, FIG. 9A; EX-1024, 3-4; EX-1026, [0049]; EX-1031, 8-9, FIG. 13; EX-1010, [0040], EX-1044, 1-2; EX-1029, 36-39; EX-1032, 1-2; EX-1033, 1; EX-1042, 96, 172, 180, 227, 275, 286; EX-1017, [0025]); §V.F.2 (EX-1039, FIG. 5, 2-6, 8-12 (*citing* EX-1040, 3-6, FIGS. 3-4); EX-1036, 1-2; EX-1019, FIG. 19, [0191], [0199]; EX-1046, 23-24; EX-1045, 1; EX-1049, p.3); EX-1003, ¶¶172-173.

Seshimo ground

POR, 44-49; Sur-reply, 17-19; Petition, 50, 70

Petitioner's Obviousness Analysis Is Deficient

Seshimo ground is duplicative of Huang ground

To the extent PO asserts that Huang does not explicitly disclose forming “blocking capacitor 211” (and, *e.g.*, “blocking capacitor 213”) on the same semiconductor (*e.g.*, SOI) substrate of the same semiconductor die as the other components (*e.g.*, SOI FETs) of SPDT switch 200, as discussed in the State of the Art sections, POSITAs would have been motivated to do so as a mere design choice to achieve known and predictable benefits, including making manufacturing, testing, and production of SPDT switch 200 (and ICs incorporating the same) easier and less costly, with a reasonable expectation of success, including because low capacitance value (picofarad) capacitors are small in size and typically used in RF switches since, as was well-known to POSITAs, they would pass (with very low impedance) the high frequencies-of-interest (*e.g.*, 2.4GHz associated with “traditional WLAN radio[s]”) while impeding low, out-of-band-blocker frequencies. *Id.*; §V.F.3 (EX-1034, FIG. 2;

Huang ground

To the extent PO asserts that Seshimo does not explicitly disclose forming “capacitor C3” (and, *e.g.*, “capacitor C2”) on the same semiconductor substrate of the same semiconductor die as the other components (*e.g.*, SOI FETs) of FIG. 3 SPDT switch, as discussed in the State of the Art sections, POSITAs would have been motivated to do so as a mere design choice to achieve known and predictable benefits, including making manufacturing, testing, and production of FIG. 3 SPDT switch (and ICs incorporating the same) easier and less costly, with a reasonable expectation of success, including because low capacitance value (*e.g.*, picofarad) capacitors are small in size and typically used in RF switches since, as was well-known to POSITAs, they would pass (with very low impedance) the high RF frequencies-of-interest (*e.g.*, 1.88-1.93GHz associated with “PHS”) while impeding low, out-of-band blocker frequencies.

Seshimo ground

POR, 50-52; Sur-reply, 23-24; Petition, 42-43, 61-62

'579 Patent File History: No Disclaimer that Inhibiting Was Known

1. (Currently amended) A semiconductor die comprising:
 - a semiconductor substrate;
 - a first switch circuit formed on the semiconductor substrate ~~and including a stack of field-effect transistors (FETs) connected in series~~ connected between an antenna node and a transmit node; [[and]]
 - a second switch circuit formed on the semiconductor substrate and connected between the antenna node and a receive node;
 - a first capacitor formed on the semiconductor substrate and connected in series with the first switch circuit between the first switch circuit and the antenna node;
 - a second, the capacitor formed on the semiconductor substrate and connected in series with the second switch circuit between the second switch circuit and the antenna node; and configured to inhibit a low-frequency blocker signal from mixing with a fundamental frequency signal in the switch
 - a first shunt arm formed on the semiconductor substrate and connected to the first switch circuit and the transmit node, the first shunt arm including a third switch circuit connected to ground.

No Disclaimers or Disavowals

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, the Applicant is not conceding in this application that previously pending claims are not patentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application. The Applicant reserves the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that the Applicant has made any disclaimers or disavowals of any subject matter supported by the present application.

Ex-1031 Shows Off Chip DC-Blocking Capacitors

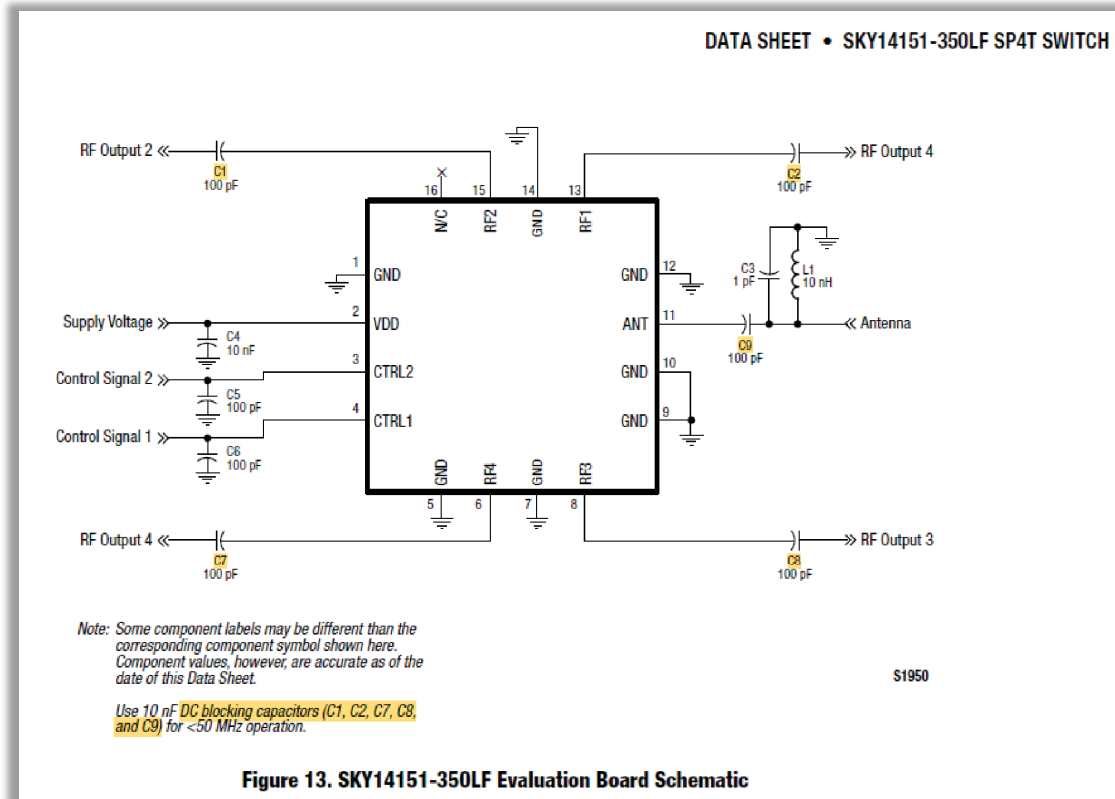


Figure 13. SKY14151-350LF Evaluation Board Schematic

POR, 32; Sur-reply, 2-3; Petition, 50; Ex-1031, 9

Ex-1033 Shows Off Chip DC Blocking Capacitors

SKYWORKS®

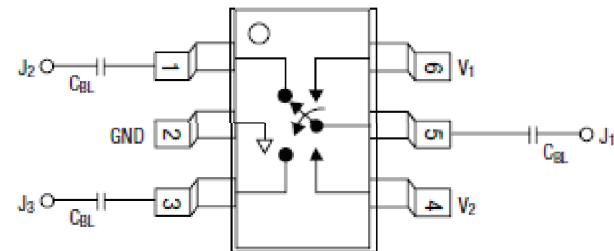
DATA SHEET

AS191-73, AS191-73LF: PHEMT GaAs IC High-Linearity 3 V Control SPDT Switch 0.1–4 GHz

Features

- 2.5 to 5 V linear operation
- Harmonics $H_2, H_3 > 65$ dBc @ $P_{IN} = 34.5$ dBm
- Low insertion loss (0.5 dB @ 0.9 GHz)
- High isolation (27 dB @ 0.9 GHz)
- Ultraminiature SOT-6 package
- PHEMT process
- Available lead (Pb)-free and RoHS-compliant MSL-1 @ 260 °C per JEDEC J-STD-020

Pin Out



DC blocking capacitors (C_{BL}) must be supplied externally.
 $C_{BL} = 47$ pF for operating frequency >500 MHz.

POR, 32; Sur-reply, 2-3; Petition, 50; Ex-1033, 1

CERTIFICATE OF SERVICE

I hereby certify that, on March 3, 2026, I caused a true and correct copy of:

- Patent Owner's Demonstratives for Oral Argument

to be served via electronic mail on the following attorneys of record:

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