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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

AXION BIOSYSTEMS, INC.,

Petitioner,

v.

AGILENT TECHNOLOGIES, INC.,

Patent Owner.

Case No. IPR2024-01467

Patent 11,906,508

**PATENT OWNER AGILENT TECHNOLOGIES, INC.'S
PRELIMINARY RESPONSE**

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PATENT OWNER'S EXHIBIT LIST

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Ex. 2002	File History of U.S. Patent No. 11,906,508
Ex. 2003-1	File History of U.S. Patent No. 9,709,548 (pp. 1-263)
Ex. 2003-2	File History of U.S. Patent No. 9,709,548 (pp. 264-551)
Ex. 2003-3	File History of U.S. Patent No. 9,709,548 (pp. 552-862)
Ex. 2003-4	File History of U.S. Patent No. 9,709,548 (pp. 863-1115)
Ex. 2003-5	File History of U.S. Patent No. 9,709,548 (pp. 1116-1316)
Ex. 2004	Declaration of Brian T. Cunningham, Ph.D.
Ex. 2005	<i>Curriculum Vitae</i> of Brian T. Cunningham, Ph.D.
Ex. 2006	Graf, Modern Dictionary of Electronics (1999) (excerpts)
Ex. 2007	File History of U.S. Patent No. 7,459,918 (Jones)

I. Introduction

The '508 Patent describes a novel impedance-based cellular analysis system incorporating multiple analog-to-digital ("A2D") signal converters and accompanying circuit architecture for continuous, real-time, non-labelled, highly sensitive, and non-invasive electrical impedance¹ measurements at millisecond time resolution across multiple wells on a well plate at the same time.

The advancements of the '508 Patent opened up a whole new field of applications previously unavailable in impedance-based cellular analysis. In particular, with the improved apparatus and system described and claimed in the '508 Patent, researchers and scientists were for the first time able to conduct studies of fast cellular activities requiring measurements with millisecond time resolution, such as the mechanism of excitation and contraction coupling of cardiomyocytes, cardio safety profiling/analysis for drugs or drug candidates,

¹ **"Impedance"** is "[t]he total opposition (i.e., resistance and reactance) a circuit offers to the flow of alternating current at a given frequency . . . It is measured in ohms Symbol: Z." Ex. 2006 at 10; Ex. 1001, Col. 13:21-23 ("[I]mpedance has two components, resistance and reactance (reactance can be divided into two categories, capacitive reactance and inductive reactance)." Ex. 2004 ¶ 22.

functional studies of cardiomyocytes derived from stem cells, cardio disease modelling by gene modification of cardiomyocyte, and physiological and disease processes of muscle cells in a high throughput manner. Ex. 2004 ¶ 21.

Axion's Petition is fundamentally flawed for two independent reasons. First, Axion fails to establish that its relied-upon references disclose the "millisecond time resolution" limitation of Claims 1-15, as would have been understood by a POSA in the 2008 time frame.² That claim term is not simply directed to the time required to take one measurement of the electrical impedance of one well, as Axion incorrectly argues throughout its Petition. Rather, as the '508 Patent expressly defines and explains, that claim term is directed to the time between two impedance measurements of each and every well being evaluated in the claimed apparatus or system. Thus, the system or apparatus must be capable of performing at least two consecutive impedance measurements for all of the wells being evaluated on a well plate in the claimed apparatus or system within

² Claim 1 of the '508 Patent recites, *inter alia*, "wherein the impedance analyzer monitors the electrode arrays at millisecond time resolution between first measurements of the cell-substrate impedance and second measurements of the cell-substrate impedance for each well." Ex. 1001, Col. 47:13-18 (Cl. 1).

milliseconds of each other. Axion's Petition incorrectly asserts that the term is simply directed to the time required to take one measurement of the electrical impedance of one well.

Second, Axion's Petition is also fundamentally flawed because Axion fails to establish that the relied-upon references disclose the claimed "impedance analyzer [which measures multiple wells' impedances] at [a] time" claim limitation.³ That claim phrase is not directed to an impedance analyzer which sequentially measures the impedances of multiple wells one at a time, as Axion incorrectly argues throughout its Petition and which the '508 Patent expressly distinguishes.⁴ Rather, as the '508 Patent repeatedly explains, that claim phrase is

³ Claim 16 of the '508 Patent recites, *inter alia*, "wherein the impedance analyzer measures, via digitally converted signals from the A2D signal converters, a first plurality of cell-substrate impedances at a first time and a second plurality of cell-substrate impedances at a second time." Ex. 1001, Col. 48:10-14 (Cl. 16).

⁴ "In 'one-well at a time' mode, when the software issues a command for measuring one well's impedance, the measurement circuitry would perform the measurement for one well The system will not perform any measurement for

directed to an impedance analyzer which measures impedances of two or more wells at the same time, or nearly the same time.⁵ That is, in the claimed apparatus or system, the impedance analyzer measures multiple wells on a well plate *in parallel*. Because the references relied upon by Axion in the Petition, neither alone nor in combination with one another, disclose or suggest the “millisecond time resolution” limitation or the “an impedance analyzer which measures multiple wells’ impedances at a time” limitation, the Petition should be denied.

In addition, Xu-752 was presented to, and evaluated by, the Office during prosecution of the ’508 Patent. Axion relies on Jones for the same purposes as

another well until completing the measurement of this well and until receiving another command for the measurement of another well.” Ex. 1001, Col. 25:5-17.

⁵ “In ‘multiple wells at a time’ mode, the software would issue a command for measuring multiple wells’ impedances. The measurement circuitry would simultaneously or nearly simultaneously perform signal conversion, signal processing and impedance calculation for multiple wells.” Ex. 1001, Col. 25:17-22; *see also id.*, Col. 47:29-33 (Cl. 4) (“monitoring multiple cell-substrate impedances in different wells of the plurality of wells at approximately the same time”).

other references that the Office evaluated during prosecution (namely, Oka and Yu), and therefore Jones is a cumulative reference. Because Axion fails to recognize and address the Section 325(d) issue, Axion also fails to demonstrate that the Office erred in any manner material to the patentability of the '508 Patent during prosecution. Thus, under the two-prong framework set forth in the Board's precedential *Advanced Bionics* decision, the Petition should be denied under Section 325(d).

II. Legal Standard for an *Inter Partes* Review

An *inter partes* review may not be instituted “unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). “In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); see 37 C.F.R. § 42.108(c). The petitioner’s burden never shifts to the patent owner. See *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v.*

Videotek, Inc., 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes* review).

III. Ground 1, Claims 23-30: Agilent’s Statutory Disclaimer of Claims 23-30 Moots Ground 1

Agilent has statutorily disclaimed Claims 9, 10, and 23-30 of the ’508 Patent. Ex. 2001. This statutory disclaimer moots Ground 1 of the Petition. 37 C.F.R. § 42.107 (“The patent owner may file a statutory disclaimer under 35 U.S.C. 253(a) in compliance with § 1.321(a) of this chapter, disclaiming one or more claims in the patent. No *inter partes* review will be instituted based on disclaimed claims.”).

IV. Ground 2, Claims 1-15: Axion Fails to Establish that Jones Discloses the “Millisecond Time Resolution” Claim Limitation as Expressly Defined in the ’508 Patent

Axion fails to show that Jones discloses the “millisecond time resolution” claim limitation of Claims 1-15. As discussed below, Axion relies on an incorrect understanding of the claim phrase “wherein the impedance analyzer monitors the electrode arrays at millisecond time resolution between first measurements of the cell-substrate impedance and second measurements of the cell-substrate impedance for each well” (collectively the “millisecond time resolution” limitation) to support its Ground 2 challenge with respect to Claims 1-15. Under the correct construction of that term, however, Axion does not (and could not) show that Jones teaches the “millisecond time resolution” limitation, which requires that the system or

apparatus must be capable of performing at least two consecutive impedance measurements across all of the wells being evaluated on a well plate in the claimed apparatus or system within milliseconds of each other. Therefore, Axion fails to meet its burden of establishing a reasonable likelihood that it would prevail with respect to any of Claims 1-15 challenged in the Petition.

A. “Millisecond Time Resolution” Means that the System Performs “at Least Two Consecutive Impedance Measurements” for “Each and Every Well of the System” in “Less than 300 Milliseconds from One Another”

In an IPR proceeding, the Board applies the same *Phillips* claim construction standard as federal courts. *See* 37 C.F.R. § 42.100(b). Under the *Phillips* standard, “the words of a claim are generally given their ordinary and customary meaning.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*) (internal quotation marks and citation omitted). However, “the specification acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication.” *Id.* at 1321 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996) (citing *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (*en banc*), *aff’d*, U.S. 116 S. Ct. 1384, 1393 (1996))); *Irdeto Access, Inc. v. Echostar Satellite Corp.*, 383 F.3d 1295, 1300 (Fed. Cir. 2004) (“Even when guidance is not provided in explicit definitional format, the specification may define claim terms by implication such

that the meaning may be found in or ascertained by a reading of the patent documents.”).

Axion recognizes that the ’508 Patent “contains a ‘Definitions’ section.” Pet. at 13. But without any explanation whatsoever, Axion then simply concludes that “Petitioner does not believe there is any need to adopt any definitions from [the Definitions] section to address the grounds below.” *Id.* Instead, Axion argues that “[i]n this Petition, all of the claim terms are given their plain meaning, as understood by the POSA, unless indicated otherwise.” *Id.* Thus, Axion does not propose any construction for any claim term.

As discussed below, however, Axion relies on an incorrect understanding of the claim term “millisecond time resolution” to support its Ground 2. Under the correct claim construction—as *expressly defined by the ’508 Patent*—Axion does not (and could not) show that Jones teaches the “millisecond time resolution” claim limitation. Therefore, Axion fails to meet its burden of establishing a reasonable likelihood that it would prevail with respect to any of Claims 1-15 of the ’508 Patent challenged in the Petition.

Here, the specification of the ’508 Patent includes a “Definitions” section, which expressly defines numerous terms. Ex. 1001, Cols. 9:35 – 16:14. The ’508 Patent also explicitly states that “the definition set forth in this section prevails over the definition that is incorporated herein by reference.” *Id.*, Col. 9:45-47.

Accordingly, the definitions provided in the '508 Patent provide the POSA with essential understandings of the meanings of the claim terms.

Importantly here, the “Definitions” section of the '508 Patent sets forth the meaning for “millisecond time resolution”:

As used herein, “**impedance measurement at millisecond time resolution**” refers to the ability to perform a series of at least two consecutive impedance measurements within milliseconds of one another **for each and every well of the system** where each well is associated with an electrode array for impedance measurement. In each instance **the time between two consecutive impedance measurements are less than 300 milliseconds from one another.**

Preferably, consecutive impedance measurements are less than 200 milliseconds from one another. More preferably impedance measurements are less than 100 milliseconds from one another. For example, the time between two consecutive impedance measurements are 40 milliseconds from one another **for each and every well of the system.** **To be clear, that is to say,** in a time period of 40 milliseconds, **the system has the ability to measure two impedance data points for each and every well of the system.**

Ex. 1001, Col. 10:8-24 (emphasis added). Thus, the '508 Patent defines the term “millisecond time resolution” to mean that at least two consecutive impedance measurements for each and every well being evaluated in the claimed apparatus or system can be performed in less than 300 milliseconds from one another. *Id.*; Ex. 2004 ¶ 31.

The '508 Patent's specification has numerous disclosures that are entirely consistent with this understanding of the "millisecond time resolution" claim term:

In embodiments where the device includes multiple wells, the impedance analyzer has the capability to allow impedance measurements for each and every well at millisecond time resolution. That is to say, for a selected time period, the impedance data for each and every well of the system is measured at millisecond time resolution. Further, when groups of wells are monitored, the groups are monitored at millisecond time resolution.

Ex. 1001, Col. 3:24-32.

Throughout the present application where the device includes multiple wells each of which is associated with an electrode array, millisecond time resolution refers to that for any selected time period, the impedance measurement for each and every well can be performed with two consecutive measurements separated with millisecond resolution. Further, when groups of wells, such as subsets of all wells of a device, are monitored a group of wells may be monitored using millisecond time resolution.

Id., Cols. 3:65 – 4:6.

For example, if the system comprises a device having 96 wells, the system hardware and software should be capable of, for a given time period, measuring the impedances of all 96 wells with millisecond time resolution between two adjacent or consecutive impedance measurement points for each and every well. Thus, comparing two impedance analyzers, one for impedance measurement of 96 wells

with millisecond resolution and another for impedance measurement of a single well with millisecond time resolution, the one for 96 well measurement is effectively 96-times faster than one for a single well measurement since it is required to have a capability for performing impedance measurement for all 96 wells with millisecond time resolution.

Id., Col. 24:22-35; Ex. 2004 ¶ 32.

Therefore, in accordance with the patentees’ express definition in the ’508 Patent, the term “millisecond time resolution” does not mean measuring the impedance of one well in under 300 milliseconds, as Axion repeatedly asserts. *See infra* Section IV.B. Instead, the term “millisecond time resolution” means the time between two consecutive impedance measurements for each and every well being evaluated in the claimed apparatus or system is under 300 milliseconds from one another. Ex. 2004 ¶ 31.

Under the correct claim construction—as expressly defined by the ’508 Patent—Axion does not (and could not) establish that Jones teaches the “millisecond time resolution” claim limitation. Therefore, Axion fails to meet its burden of establishing a reasonable likelihood that it would prevail with respect to any of Claims 1-15 of the ’508 Patent challenged in the Petition.

B. In Ground 2, Axion Incorrectly Interprets the Term “Millisecond Time Resolution” in Contradiction to Its Express Definition

Axion relies on two references to formulate its Ground 2:

1. **Xu-752**, which Axion argues describes every limitation of the '508 Patent's claims "except for ADCs" and "for sampling at 'millisecond time resolution;" and
2. **Jones**, which Axion argues "describes an improved impedance measurement system that includes the limitations that Xu-752 does not explicitly describe."

Pet. at 31-32. Although Axion relies on Jones for the "millisecond time resolution" limitation, Axion inexplicably asserts that "the Board does not need to construe 'millisecond time resolution' to find the claims unpatentable on the stated grounds." *Id.* at 14. Indeed, the only articulated disclosure of Jones' that Axion relies upon to support the "millisecond time resolution" limitation is Paragraph [0030], which states in its entirety:

Each well is subject to a stepped sweep (a series of single frequency bursts-one burst for each selected frequency). The bursts consist of an integral number of cycles. In one embodiment, the number of cycles is typically 15. The number of cycles for additional embodiments are chosen to be sufficient for well and gain multiplexer switching transients to settle and to obtain the necessary number of sample points. From preliminary modeling and testing, **no more than 68.2 ms per well** for all frequencies is required to obtain sufficient samples. For an embodiment in which a 96 well plate with 12 wells per row plus four reference network channels, calculations to

determine sufficient samples suggest a 1091 mS measurement period, leaving 409 mS for multiplexer switching and signal settling within the target 1.5 second update period.

Ex. 1006 ¶ [0030]; Ex. 2004 ¶ 33.

Axion argues that “Jones’ impedance analyzer is capable of monitoring *each well* at a millisecond time resolution between two measurements of the cell-substrate impedance of the well.” Pet. at 34 (emphasis added). This argument is theorized from Jones’ single disclosure of “an exemplary 1.5-second update period for an entire 96-well plate, where the 1.5-second period includes 1091 milliseconds

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of measurement time, leaving 409 milliseconds for multiplexer⁶ switching⁷ and signal settling.”⁸ *Id.* (footnotes added). Axion further asserts, incorrectly, that

⁶ A “**multiplexer**” is “[a]n analog or linear device for selecting one of a number of inputs and switching its information to the output[.]” Ex. 2006 at 12. Ex. 2004 ¶ 34. An “**analog multiplexer**” is a “[c]ircuit used for time-sharing of analog-to-digital converters between a number of different analog information channels. . . . Multiplexing is performed by sequentially turning on each switch one at a time, switching each individual input to a common output.” Ex. 2006 at 9; Ex. 2004 ¶ 34.

⁷ “**Switching time**” is “[t]he time for a multiplexer to change from one channel to the next with the new output signal remaining within a specified percentage of its final value.” Ex. 2006 at 14; Ex. 2004 ¶ 34.

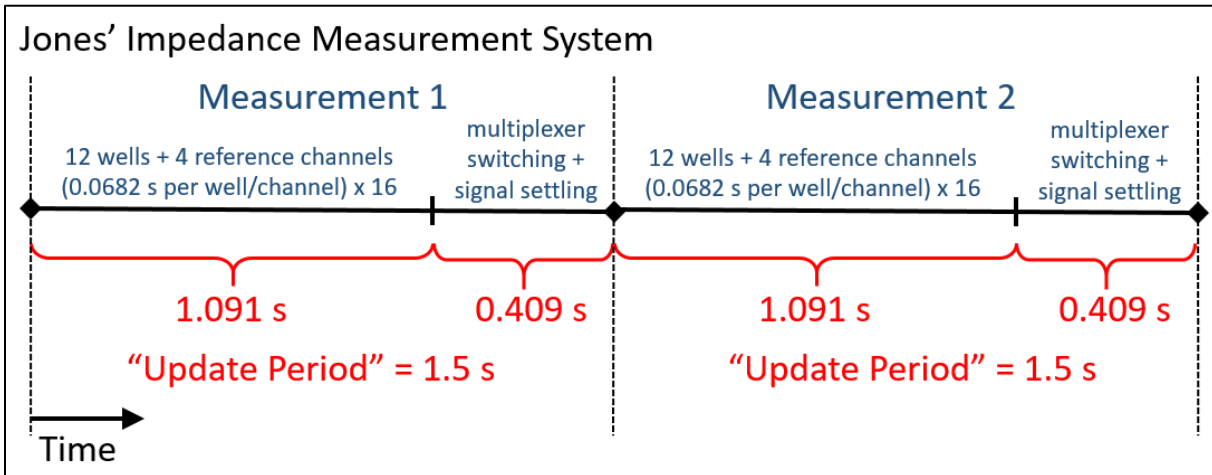
⁸ In an exercise of pure hindsight reconstruction, Axion contorts the single-paragraph disclosure in Jones into multiple pages of complex calculations and results-oriented interpretations. *E.g.*, Pet. at 34-35. A POSA would understand that Jones provides a single disclosure of a 68.2 ms time to scan a single well, plus a 1091 ms time to scan 12 wells and 4 references in series, plus a 409 ms time for

“[t]he disclosure in Jones also describes taking first and second measurements of impedance of *a single well* of a 96-well plate milliseconds apart as part of the stepped frequency sweep that is completed for each well in ‘no more than 68.2 ms per well.’ EX1006, ¶[0030].” *Id.* at 35 (emphasis added). Finally, Axion asserts, again incorrectly, that “for a multiwell plate having even fewer wells, or where the user only wanted to monitor a more limited number of wells in a 96-well plate, Jones discloses providing a higher measurement rate with less time between two measurements in *each well*.” *Id.* at 36 (emphasis added).

Contrary to Axion’s arguments, Jones’ Paragraph [0030] explains that its 8-row, 96-well system requires a measurement time for a single well to be “no more than 68.2 ms *per well*,” with a “target 1.5 second update period”. Ex. 1006 ¶ [0030] (emphasis added); Ex. 2004 ¶ 35. Thus, Jones teaches that 1.5 seconds are required between two consecutive measurements of each well (the “update period”): 12 wells plus the 4 reference channels on a daughter board measured sequentially (in series), with an additional 0.409 seconds for “multiplexer switching and signal settling”: $(0.0682 \text{ seconds} \times (12 + 4)) + 0.409 \text{ seconds} = 1.5$

“multiplexer switching and signal settling,” resulting in a combined “update period” of 1.5 seconds between scans. Ex. 1006 ¶ [0030]; Ex. 2004 ¶ 35.

seconds). Ex. 1006 ¶ [0030]; Ex. 2004 ¶ 35. Jones' Paragraph [0030] discussion can be illustrated as follows:



Ex. 2004 ¶ 36.

Axion therefore misinterprets the “millisecond time resolution” limitation to simply mean the time required to measure the impedance of a single well—not the time required between two impedance measurements of each and every well of the claimed apparatus or system being evaluated, as expressly defined by the ’508 Patent.

C. Axion Fails to Establish that Jones Discloses the “Millisecond Time Resolution” Claim Limitation Under the Proper Construction of that Limitation

In relying on Jones for the “millisecond time resolution” limitation, Axion completely ignores the patentees’ express definition and applies a much broader definition, which is untethered to the ’508 Patent’s disclosure. Under the correct

claim construction, as defined by the '508 Patent, Jones does not disclose the “millisecond time resolution” limitation.

As discussed above, Jones teaches “[f]or an embodiment in which a 96 well plate with 12 wells per row plus four reference network channels, calculations to determine sufficient samples suggest a 1091 mS measurement period, leaving 409 mS for multiplexer switching and signal settling within the target 1.5 second update period.” Ex. 1006 ¶ [0030]. This disclosure teaches that the 12 wells in a row (with 4 additional channels) are measured one at a time, *i.e.*, in series, such that a measurement time of 68.2 ms per well provides a total measurement time of $(12 + 4) \times 68.2 \text{ ms} = 1.091 \text{ seconds}$. *Id.*; Ex. 2004 ¶ 35. Because the wells are measured one at a time (*i.e.*, in series), Jones includes an additional 0.409 seconds for “multiplexer switching and signal settling.” *Id.*; *see supra* notes 6 & 7 (definitions of “multiplexer” and “switching time,” respectively). Thus, the total “update period” between two consecutive measurements of the wells is $1.091 \text{ seconds} + 0.409 \text{ seconds} = 1.5 \text{ seconds}$. Ex. 2004 ¶ 35.

Jones, therefore, discloses an impedance measurement system that can perform two consecutive impedance measurements for 12 wells that are 1.5 seconds apart. Thus, Jones operates on a time resolution on the scale of *seconds* versus the claimed *millisecond* time resolution. Ex. 2004 ¶ 35. The '508 Patent

provides an illustrative example to explain why millisecond time resolution is an order-of-magnitude type increase in measurement speed:

Thus, comparing two impedance analyzers, one for impedance measurement of 96 wells with millisecond resolution and another for impedance measurement of a single well with millisecond time resolution, the one for 96 well measurement is effectively 96-times faster than one for a single well measurement since it is required to have a capability for performing impedance measurement for all 96 wells with millisecond time resolution.

Ex. 1001, Col. 24:27-35; Ex. 2004 ¶ 37.

It is not surprising that Jones does not operate at the claimed millisecond time resolution because Jones does not contemplate measurements in the context of cardiomyocyte beating or other situations where fast measurements are necessary. *See infra* Section IV.D. Because Jones operates on a scale of seconds, not milliseconds as claimed in the '508 Patent, Jones does not disclose the “millisecond time resolution” limitation under the correct claim construction.

D. The '508 Patent Explains the Importance of “Millisecond Time Resolution” for Applications Such as Cardiomyocytes, While Jones' 1.5 Second “Update Period” Would Be Inadequate for Such Applications

The '508 Patent is directed to “impedance-based monitoring of cells and more particularly to systems and methods for monitoring excitation-contraction coupling and excitable cells using impedance based systems with millisecond time

resolution.” Ex. 1001, Col. 1:28-32; Ex. 2004 ¶ 38. The claimed invention “fill[s] a major technological gap in monitoring of excitation-contraction coupling and excitable cells, such as cardiomyocytes, *in vitro*. This is accomplished, in part, from the development of an impedance-based system and monitoring method that employs **millisecond time resolution**.” Ex. 1001, Col. 16:19-24; *see also id.*, Col. 3:48-54 (“[M]illisecond time resolution enhances measurement such that excitation-contraction coupling of excitable cells may be effectively monitored. In some embodiments the excitation cycle is a beating cycle, such as a beating cycle of a cardiomyocyte.”), Col. 30:38-41 (“[T]he development of millisecond time resolution permits impedance monitoring of the cardiomyocyte beating cycle as well as fluctuations, even minor alterations, in response to external stimuli.”); Ex. 2004 ¶ 38.

With respect to cardiomyocytes in particular, “[a] beating cycle may be as short as **between 100 and 200 milliseconds**, translating to a beating rate of 600 to 300 beats per minute.” Ex. 1001, Col. 10:44-46. Because of the important applications repeatedly discussed, the ’508 Patent focuses on time resolutions between two impedance measurements of “less than 300 milliseconds”:

The method has particular utility with cells that are known or suspected to be capable of or undergo excitation-contraction coupling, such as cardiomyocytes. The method may also be useful for monitoring neurological cells or neurological systems. Impedance

measurements may be performed in millisecond time resolution. In some embodiments, two consecutive impedance measurements for each and every well of the system are performed less than 300 milliseconds apart.

Id., Col. 4:51-59; *see id.*, Col. 47:15 (“millisecond time resolution”) (Cl. 1), Col. 47:54 (“less than 100 milliseconds”) (Cl. 11), Col. 47:57 (“less than 40 milliseconds”) (Cl. 12), Col. 47:59 (“less than 20 milliseconds”) (Cl. 13), Col. 47:62 (“less than 5 milliseconds”) (Cl. 14); Ex. 2004 ¶ 39.

The '508 Patent further explains why, in some embodiments, time resolutions may be significantly less than 300 milliseconds for these kinds of applications:

With millisecond time resolution for impedance measurement, it becomes possible to resolve individual beating cycles of cardiomyocytes cultured on electrodes. Whilst theoretically one needs at least two data points for each beating cycle, in practice more than 2 data points are needed for each beating cycle. For example, if cells have a beating rate of 60 beats per minute, i.e[.], one beat per second. It would be preferred to have a time resolution of at least 200 milliseconds so that each beating cycle consists of 5 data points. More preferably, the measurement time resolution is 100 milliseconds. Still more preferably, the time resolution is 50 milliseconds or less.

Ex. 1001, Col. 25:33-44; Ex. 2004 ¶ 40. Consistent with this discussion, the '508 Patent discloses multiple experiments using a 40-millisecond resolution for

impedance measurements of cardiomyocytes. *See, e.g.*, Ex. 1001, Figs. 9C, 9D, 11A-T, Col. 45:32-34 (“Similar to the cell index plot shown in FIGS. 9C and 9D, the time resolution between two adjacent points in all the figures in FIGS. 11A-11T is 40 milliseconds.”); Ex. 2004 ¶ 41.

Particularly relevant here, the ’508 Patent explains why then-existing systems that used “seconds” time resolution between consecutive impedance measurements (like Jones’ 1.5 seconds “update period”) would be incapable of accomplishing the objectives of the invention:

Millisecond time resolution of impedance-based devices provides a significant technical step over traditional impedance measuring devices, which are typically limited to **second** or minute **resolution**.

* * *

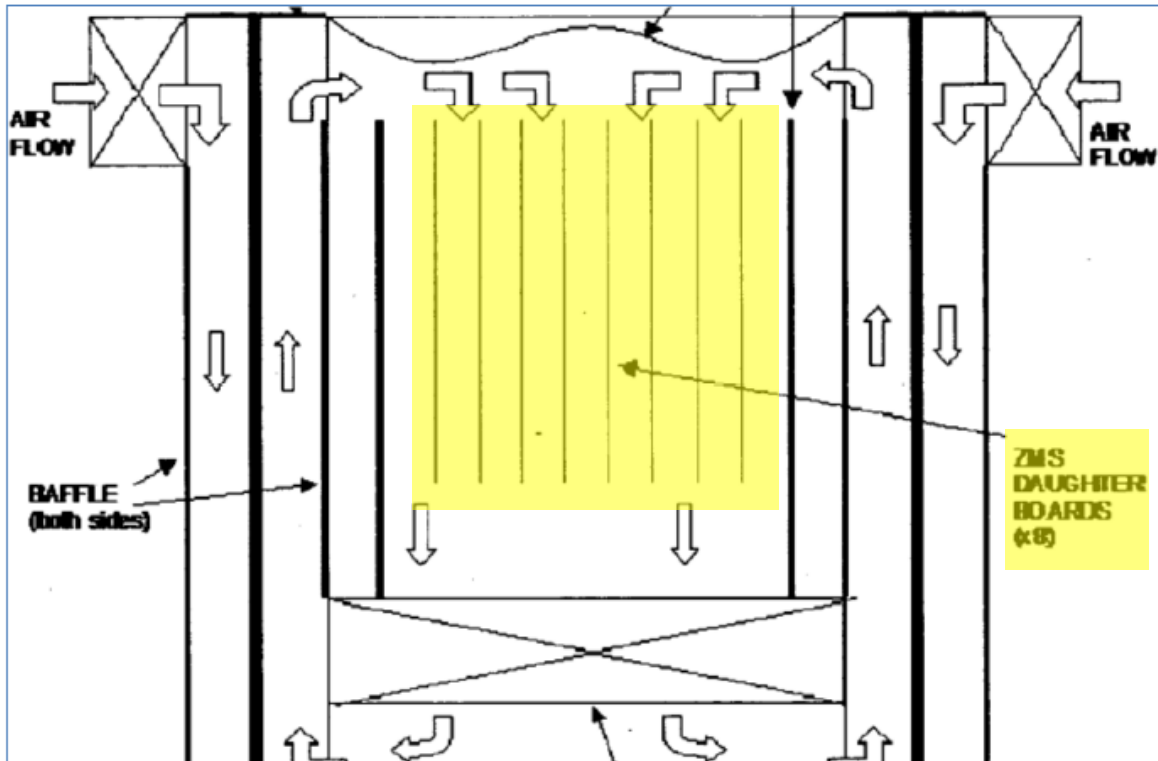
Without millisecond time resolution, it would not be possible to perform detailed analysis of the beating cycle of the excitable cells. For example, for cardiomyocytes, if the impedance is measured at **seconds time-resolution** such as a ten-second or **even one-second resolution**, it would not be possible to observe beating of the cardiomyocytes or resolve a beating cycle of the cardiomyocytes with an impedance measurement. The cardiomyocytes-beating-resulted impedance change would be shown as “noise” on the impedance curves measured at **seconds** or minutes **time-resolution**.

Ex. 1001, Cols. 24:11-14, 16:40-58. Thus, the 1.5 second update period disclosed in Jones would be unable to effectively perform the analysis of the excitable cells repeatedly discussed and emphasized in the '508 Patent. Ex. 2004 ¶ 42.

Indeed, Jones does not mention any particular applications for its system, including the types of cells to be monitored or their particular nature (such as excitable cells or cardiomyocytes). Ex. 2004 ¶ 43. And Jones does not disclose millisecond time resolution or include any discussion about improving measurement time resolution. *Id.* Instead, Jones is directed to the physical arrangement of its system, with the goal of improving “internal correction of impedance measurement drift, maximized measurement accuracy, and minimized system size.” Ex. 1006, Abstract.

[T]he ZMS employs [hardware] parallelism to obtain the required throughput at the repeatability required and incorporates novel calibration, self-check, and in-run compensation schemes as well as internal temperature control to ensure increased measurement accuracy and stabilization against thermal drift. *Id.* ¶ [0003]; Ex. 2004 ¶ 44. Indeed, Jones is titled “Impedance Measurement System With Incorporated Internal Measurement Drift Compensation Networks.” Ex. 1006 at 1.

The hardware “parallelism” mentioned in Jones, and acknowledged by Axion, is illustrated in the figures of the published patent application, such as the eight daughter boards physically arranged in parallel in Figure 4:



Pet. at 33 (“Jones Figure 4 . . . shows eight daughter boards, arranged in parallel.”);
Ex. 1006, Fig. 4 (excerpt); Ex. 2004 ¶ 45.

Accordingly, the ’508 Patent’s “millisecond time resolution,” as described and claimed, provides a substantial improvement in the field of impedance measuring systems, particularly with respect to important applications such as excitable cells like cardiomyocytes. Ex. 2004 ¶ 46.

V. Ground 2, Claims 16-22: Axion Fails to Establish that Jones Discloses the “An Impedance Analyzer Measur[ing] . . . a First Plurality of Cell-Substrate Impedances at a First Time and a Second Plurality of Cell-Substrate Impedances at a Second Time” (“An Impedance Analyzer Which Measures Multiple Wells’ Impedances at a Time”) Claim Limitation as Explained in the ’508 Patent

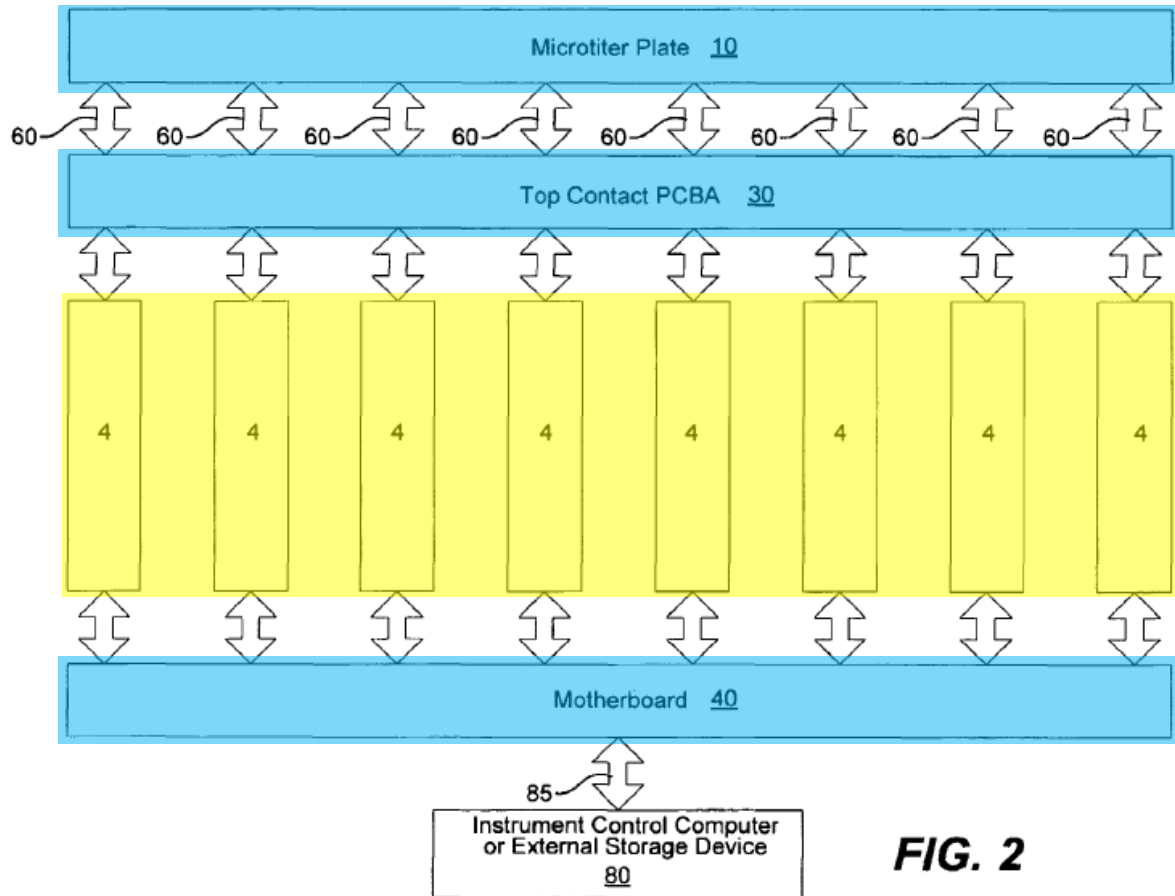
Axion fails to establish that Jones discloses the “an impedance analyzer which measures multiple wells’ impedances at a time” claim limitation of Claims 16-22. Axion also conflates the physical configuration of the daughter boards (and other hardware components) in Jones, which are arranged in parallel with one another, with the claimed system performing a plurality of impedance measurements at a given time, *i.e.*, in parallel. Axion does not demonstrate that Jones discloses an impedance analyzer which measures the impedances of multiple wells at the same (or nearly the same) time, *i.e.*, in parallel.

As discussed below, Axion relies on an incorrect understanding of the claim phrase “wherein the impedance analyzer measures, via digitally converted signals from [a plurality of analog-to-digital (A2D) signal converters electrically arranged in parallel to one another], a first plurality of cell-substrate impedances at a first time and a second plurality of cell-substrate impedances at a second time” (the “an impedance analyzer which measures multiple wells’ impedances at a time” limitation) to support its Ground 2 challenge with respect to Claims 16-22. Under the correct construction of that phrase, however, Axion does not (and could not) show that Jones teaches the “an impedance analyzer which measures multiple

wells' impedances at a time" claim limitation, which requires an impedance analyzer to measure multiple impedances on a well plate in parallel at the same (or nearly the same) time (*i.e.*, simultaneously or nearly simultaneously (*see supra* notes 4 & 5)).

Axion points to Jones' few mentions of the words "parallel" and "parallelism" to argue that Jones satisfies the "electrically arranged in parallel" limitation of Claims 16-22. *E.g.*, Pet. at 66-67. But as discussed above, the '508 Patent's claims are directed to the impedance analyzer of the claimed system measuring multiple wells' impedances in parallel, not to the physical arrangement of the system's hardware components. Indeed, Axion recognizes that the "parallelism" mentioned in Jones is directed to the physical configuration of the components in Jones' impedance measurement system:

U.S. Patent No. 7,459,918, the patent that issued on December 2, 2018 from Jones, includes a Figure 2 that shows the **spatial relationship** of the plate 10 to the top contact PCBA 30 to the daughter boards 4 to the motherboard 40, as described in Jones.



Ex. 1003 ¶ 67 (citing Ex. 1007 at Fig. 2, 2:1-48; Ex. 1006, ¶¶ [0012]-[0016]).⁹

⁹ Figures 2 and 3 of Exhibit 1007, the Jones *patent*, are not included in the figures of Exhibit 1006, the Jones *publication*. Compare Ex. 1006 with Ex. 1007. During prosecution, in a July 12, 2007 amendment, Jones asserted that newly added Figures 2 and 3 did not include any new matter. Ex. 2007 at 87-90 (“Paragraphs [005]-[018] have been amended to add drawing descriptions and element numbers for newly added drawings Figures 2 and 3. Applicant

Within the Impedance Measurement System the top contact PCBA lies in a plane **parallel** to and immediately below the microtiter plate, while the daughter boards are **perpendicular** to the plane of the microtiter plate. A **horizontal** mother board is located below the daughter boards.

Ex. 1006 ¶ [0014]; Ex. 2004 ¶ 57. Indeed, all of the claims in the relied-upon Jones publication—Jones’ purported invention—are directed to the parallel orientation of the impedance measurement system’s hardware. Ex. 1006, Cls. 1, 15 (claiming parallel structural components, but requiring only “at least one daughter board comprising measurement and multiplexing circuitry”). The same is equally true of Jones’ issued patent. Ex. 1007, Cls. 1, 15 (same).

Therefore, Axion fails to meet its burden of establishing a reasonable likelihood that it would prevail with respect to any of Claims 16-22 challenged in the Petition.

respectfully asserts that no new matter has been added with these amendments.”).

For purposes of this Patent Owner Preliminary Response, Agilent does not dispute Jones’ assertion in that regard.

A. “An Impedance Analyzer which Measures Multiple Wells’ Impedances at a Time” Means an Impedance Analyzer Measures the Impedance of Multiple Wells at the Same Time by Measuring the Wells in Parallel

Claim 16 of the ’508 Patent is directed to a system for impedance analysis, comprising, *inter alia*:

- a) a plurality of analog-to-digital (A2D) signal converters electrically arranged in parallel to one another;
- b) a well plate comprising a plurality of wells on a nonconductive substrate, wherein each well of the plurality of wells comprises one electrode array of a plurality of electrode arrays disposed on the nonconductive substrate that is connected to the plurality of A2D signal converters;
- c) an impedance analyzer connected to or including the plurality of A2D signal converters, wherein the impedance analyzer measures, via digitally converted signals from the A2D signal converters, a first plurality of cell-substrate impedances at a first time and a second plurality of cell-substrate impedances at a second time, the first plurality of cell-substrate impedances and the second plurality of cell-substrate impedances being measured between a first electrode structure and a second electrode structure in each electrode array and across a cell sample attached within each well of the plurality of wells;

Ex. 1001, Col. 48:1-20 (Cl. 16). Element a) of Claim 16 recites “a plurality of analog-to-digital (A2D) signal converters electrically arranged in parallel to one another.” *Id.*; Ex. 2004 ¶ 48. Element b) of Claim 16 recites “a well plate

comprising a plurality of wells” wherein the plurality of wells are connected to the plurality of A2D signal converters of Element a) through electrode arrays. *Id.*

Element c) of Claim 16 recites “an impedance analyzer” that is “connect[ed] to or include[es] the plurality of A2D signal converters [of Element a)],” which are

“electrically arranged in parallel to one other.” *Id.* The impedance analyzer of

Element c) “measures, via digitally converted signals from the A2D signal converters [of Element a)], a first plurality of cell-substrate impedances at a first

time and a second plurality of cell-substrate impedances at a second time[.]” *Id.*

Accordingly, the claimed “impedance analyzer” measures more than one

impedance at a time via the plurality of A2D signal converters that are “electrically arranged in parallel.” Ex. 2004 ¶ 49. This further means that the claimed

“impedance analyzer” measures the impedances of multiple wells in parallel, *i.e.*,

at the same time (or nearly the same time), via the plurality of A2D signal

converters that are “electrically arranged in parallel to one another.” *Id.* This

measuring of a plurality of wells’ impedances at the same time (or nearly the same time) by an impedance analyzer is emphasized by the claim recital that “the

impedance analyzer measures . . . a first plurality of cell-substrate impedances at a

first time and a second plurality of cell-substrate impedances at a second time . . .

.” *Id.*

The '508 Patent's specification repeatedly explains the differences between (a) its inventive "measurement of multiple-wells' impedances at a time" using A2D converters electrically arranged in parallel to one another, and (b) the conventional "measurement of one-well's impedance at a time," which is described in Jones (*see infra* Section V.C), as follows:

[A] very important improvement is to replace previous working mode of "measurement of one-well's impedance at a time" with a mode of "measurement of multiple-wells' impedances at a time". In "one-well at a time" mode, when the software issues a command for measuring one well's impedance, the measurement circuitry would perform the measurement for one well including signal generation to the well, converting the voltage signal and the electric current signal for the well to digital signal, digitally processing the signals to do impedance calculation and sending the well's impedance data to the computer over the communication line between the impedance measurement circuitry and the computer. The system will not perform any measurement for another well until completing the measurement of this well and until receiving another command for the measurement of another well. In "multiple wells at a time" mode, the software would issue a command for measuring multiple wells' impedances. The measurement circuitry would simultaneously or nearly simultaneously perform signal conversion, signal processing and impedance calculation for multiple wells.

Ex. 1001, Col. 25:2-22; Ex. 2004 ¶ 50. Thus, as emphasized in the '508 Patent's disclosure of the improved technology, the impedance analyzer recited in Claim 16 performs its measurements in a "multiple wells at a time" mode, *i.e.*, measuring multiple wells' impedance at a time in reliance on the measurement circuitry, including the A2D converters electrically arranged in parallel to one another. Ex. 2004 ¶ 51.

Accordingly, the "an impedance analyzer which measures multiple wells' impedances at a time" limitation means an impedance analyzer measures multiple wells' impedances on a well plate at the same (or nearly the same) time, *i.e.*, in parallel. Ex. 2004 ¶ 51.

B. In Ground 2, Axion Interprets the "An Impedance Analyzer which Measures Multiple Wells' Impedances at a Time" Claimed Limitation in a Manner Inconsistent with the Specification of the '508 Patent

With respect to the "an impedance analyzer which measures multiple wells' impedances at a time" limitation, Axion argues that "Xu-752 describes the impedance analyzer monitoring electrode arrays in **each well** 'continuously' over various time periods, and thus taking multiple measurements of **each well** over such periods." Pet. at 70 (emphasis added). Axion asserts that although "Xu-752 does not explicitly describe measuring pluralities of impedances via digitally converted signals from the plural ADCs[,] Jones describes an impedance analyzer that uses digitally converted signals from the plural ADCs to measure pluralities of

impedances, as claimed.” *Id.* Thus, in its Petition, Axion completely overlooks the “an impedance analyzer which measures multiple wells’ impedances at a time” claim limitation, failing to explain how that limitation is disclosed in Xu-752 or Jones. Axion has not shown that Jones discloses an impedance analyzer which measures the impedances of multiple wells at the same time, versus describing a system having a physical configuration with parallel structural components. Ex. 2004 ¶ 52.

Jones teaches that each row of wells on a well plate (or “microtiter plate”) is addressed by a “daughter board” that includes an impedance analyzer for measuring the plate’s wells *in series*:

In one embodiment, each row of sensors on a microtiter plate is addressed by **measurement circuitry** (in the form of analog signal conditioning circuits, **multiplexing circuits**, analog-digital converters, and **digital signal processors**) **on a single daughter board**.

Ex. 1006 ¶ [0012]; Ex. 2004 ¶ 52. Thus, the impedance measurement is accomplished by the “measurement circuitry” on each daughter board in conjunction with the “multiplexing circuitry.” *Id.*

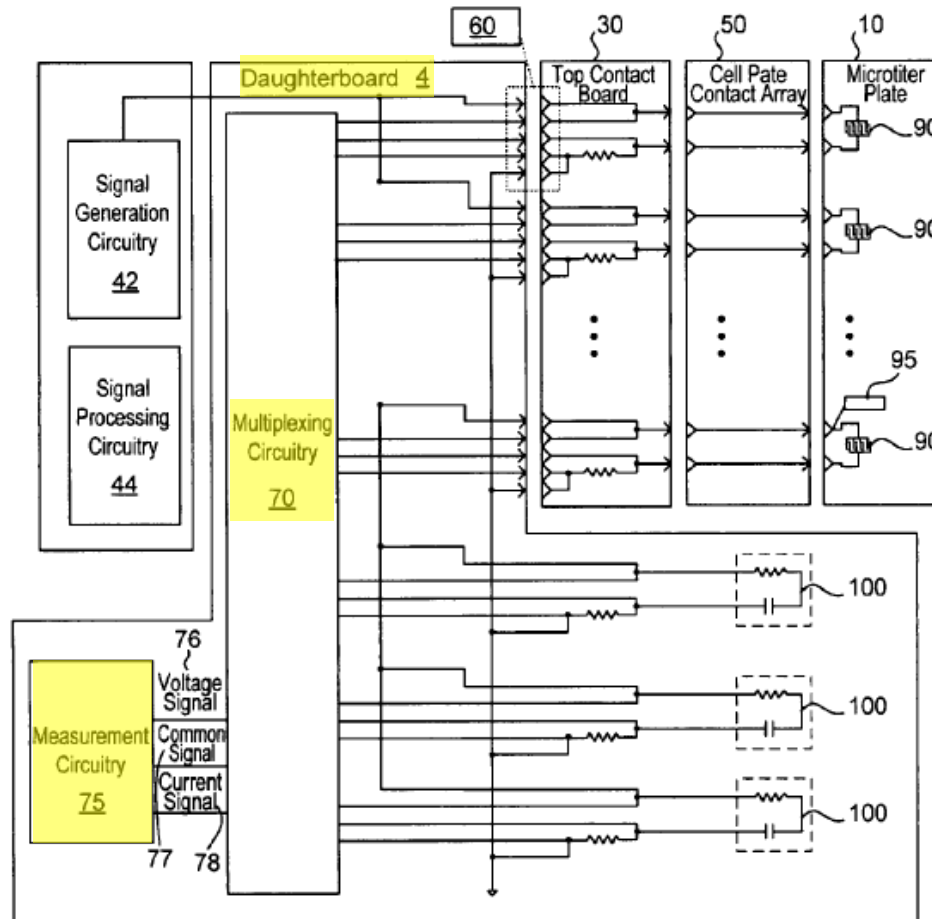


FIG. 3

Ex. 1007, Fig. 3; *see supra* note 9 (newly added Figure 3); Ex. 2004 ¶ 52.

The impedance data for a microtiter plate row is processed by a digital signal processor dedicated to each row and located on the daughter boards.

Ex. 1006 ¶ [0018]. Thus, the “measurement circuitry” on each “daughter board” measures the “impedance data for a microtiter plate row,” which is “processed by a digital signal processor dedicated to each row and located on the daughter boards”

in series, not in parallel. The Jones' specification is replete with descriptions that confirm this understanding:

In an additional embodiment, each column of sensors, rather than each row of sensors, on a microtiter plate is addressed by measurement circuitry on a single daughter board with the system arrangement of the boards remaining the same.

Ex. 1006 ¶ [0025].

(1) at least one daughter board comprising measurement and multiplexing circuitry . . .

Id., Cl. 1(1), Cl. 15(1); Ex. 2004 ¶ 52.

Indeed, Jones emphasizes that its “mother board” receives the “impedance measurement data” from each of the daughter boards:

The ZMS [Impedance Measurement System] daughter boards mate at their lowest edge with the mother board. . . . The mother board processes the impedance measurement data, at a specific time and frequency, of all wells of the microtiter plate and communicates the results to the system controller.

Id. ¶ [0020]; Ex. 2004 ¶ 53.

Moreover, Jones repeatedly (and exclusively) relies on multiplexing circuitry on each daughter board, confirming that each well on the microtiter plate is measured sequentially (*i.e.*, in series). *See, e.g.*, Ex. 1006, Abstract (“multiplexing”), ¶ [0003] (“multiplexing of impedance measurement channels”), ¶ [0012] (“[E]ach row of sensors on a microtiter plate is addressed by measurement

circuitry (in the form of analog signal conditioning circuits, multiplexing circuits, analog digital converters, and digital signal processors) on a single daughter board.”), ¶ [0012] (“Each daughter board has multiplexing circuitry allowing one or more measurement channels to address the sensors for each well in the row.”), ¶ [0030] (“The number of cycles for additional embodiments are chosen to be sufficient for well and gain multiplexer switching transients to settle and to obtain the necessary number of sample points.”), ¶ [0030] (“leaving 409 mS for multiplexer switching and signal settling within the target 1.5 second update period.”); Ex. 2004 ¶ 54. Indeed, all of the claims of Jones recite multiplexing circuitry on each daughter board. *See* Ex. 1006, Cl. 1(1) (“at least one daughter board comprising measurement and multiplexing circuitry . . .”), Cl. 15(1) (same); *see also* Ex. 1007, Cl. 1(1) & Cl. 15(1) (same).

Axion therefore misinterprets the “an impedance analyzer which measures multiple wells’ impedances at a time” limitation to simply mean taking multiple measurements of each well over various time periods—not that an impedance analyzer measures multiple impedances on a well plate at the same time (or nearly the same time), *i.e.*, in parallel, as taught by the ’508 Patent.

C. Axion Fails to Establish that Jones Discloses the “An Impedance Analyzer which Measures Multiple Wells’ Impedances at a Time” Claim Limitation Under the Proper Understanding of that Limitation

Jones discloses a device having multiple daughter boards, each daughter board having a dedicated impedance analyzer or “measurement circuitry”. Ex. 1006 ¶ [0012]. Each daughter board sequentially takes impedance measurements of one well at a time for each of the wells in a row. *Id.* ¶ [0030]; Ex. 2004 ¶ 55. Thus, each impedance analyzer of Jones takes a single impedance measurement at a time. Ex. 2004 ¶ 55. Critically, Axion does not show that Jones describes an impedance analyzer that measures impedance of multiple wells at the same time, as described and claimed in the ’508 Patent. *Id.*

Jones only teaches “one-well at a time” for the measurement of impedance by way of a daughter board (*i.e.*, the wells measured in series):

The daughter boards carry the electronic components to drive and process a row of wells. One daughter board is assigned to each row of the microtiter plate. In one embodiment, the top edge of the daughter boards is equipped with a row of well drivers and an interlaced set of multiplexing field effect transistors (or FETs, a type of transistor commonly used for signal switching or amplification) for well selection within a row. . . . A digital-to-analog converter may be used to provide DC offset correction to the current channel to ensure the analog-to-digital converter input is centered on the common mode range. Additionally, the daughter boards may be equipped with

multiple analog-to-digital converters (including one for the voltage channel and one for the current channel), digital control circuitry (e.g., digital signal processors, memory devices, field programmable gate arrays, and/or electrically programmable logic devices), and voltage regulation circuitry. In one embodiment, these additional components are arranged below and to the side of the analog sections. The impedance data for a microtiter plate row is processed by a digital signal processor dedicated to each row and located on the daughter boards.

Ex. 1006 ¶ [0018]; Ex. 2004 ¶ 56.

As quoted above, in Jones' impedance measurement system, one daughter board is assigned to a row of wells and "equipped with a row of well drivers and an interlaced set of multiplexing field effect transistors (or FETs, a type of transistor commonly used for signal switching or amplification) for well selection in a row."

Id. Jones discloses that "each row of sensors on a microtiter plate is addressed by measurement circuitry (in the form of analog signal conditioning circuits, multiplexing circuits, analog-digital converters, and digital signal processors) on a single daughter board." Ex. 1006 ¶ [0012]. Thus, the daughter board in Jones measures the impedance of each of the wells in series, using multiplexers and switching circuitry to measure each well in sequence (*i.e.*, one well at a time). *See supra* notes 6 & 7 (definitions of "multiplexer" and "switching time", respectively); Ex. 2004 ¶ 34.

Jones further discloses that 12 wells in a row (with 4 additional channels), which is controlled by one daughter board having an impedance analyzer, are measured in series, such that a measurement time of 68.2 ms per well provides a total measurement time of $(12 + 4) \times 68.2 \text{ seconds} = 1.091 \text{ seconds}$. Ex. 1006 ¶ [0030]; Ex. 2004 ¶ 35. An additional 0.409 seconds are provided “for multiplexer switching and signal settling,” providing a total time of 1.5 seconds for the “update period.” *Id.* Thus, a daughter board disclosed in Jones has an impedance analyzer operates in what the ’508 Patent calls a “one-well at a time” mode, not “multiple wells at a time” mode. Ex. 2004 ¶¶ 52, 55, 56.

Axion argues that “Jones describes an impedance analyzer that uses digitally converted signals from the plural ADCs to measure pluralities of impedances, as claimed.” Pet. at 70. Citing ¶¶ [0003], [0012], [0018], [0026], [0035], Axion then contends that “Jones describes using ‘parallel impedance measurement channels.’” *Id.* However, only Paragraph [0003] uses the term “parallel impedance measurement *channels*,” referring to the *physical arrangement* of multiple daughter boards (each board having “measurement channels”) placed in parallel with one another within Jones’ impedance measurement system. Ex. 1006 ¶ [0003]; *see id.* ¶ [0012] (“Each daughter board has multiplexing circuitry allowing one or more *measurement channels* to address the sensors for each well in the row.”) (emphasis added); Ex. 2004 ¶ 59. As discussed above, Jones describes

this parallel physical arrangement of daughter boards in which each daughter board has “measurement circuitry” that measures cell impedances of the wells in a row on the plate in series. Ex. 1006 ¶¶ [0012] & [0018] (“[E]ach row of sensors on a microtiter plate is addressed by measurement circuitry. . . . The impedance data for a microtiter plate row is processed by a digital signal processor dedicated to each row and located on the daughter boards.”); Ex. 2004 ¶ 52. Indeed, Jones emphasizes the importance of this physical parallel configuration: “Electrical performance dictates that the daughter board assembly be closely coupled to the top contact board and that the circuitry be kept as tightly arranged as possible.” *Id.* ¶ [0021]; Ex. 2004 ¶ 58.

Jones’ disclosure, including its claims, are primarily directed to the *form factor* of the Impedance Measurement System (or “ZMS”):

This physical arrangement and electrical configuration maximizes the accuracy of the impedance measurements by minimizing the electrical path length and stray impedances associated with connecting the microtiter plate sensor to the measurement circuit. The minimized path length also optimizes phase and gain tracking, and maximizes the immunity to noise.

The physical configuration minimizes the number of needed mechanical supports and eliminates key thermal expansion problems associated with other designs. The configuration minimizes the size of the Impedance Measurement System thereby allowing more

efficient internal packaging and thermal stabilization of the electronic components (due to reduced convection). The minimized path length also optimizes phase and gain tracking, and maximizes the immunity to noise.

Id. ¶¶ [0023]-[0024]; Ex. 2004 ¶¶ 43-45, 57-60.

As quoted above, it is Jones’ compact form factor, with the parallel arrangement of the hardware components, multiple fans, baffles, air deflectors, etc., that Jones asserts allows the system to “increase measurement accuracy and stabilization against thermal drift.” *E.g., id.* ¶ [0003]; *id.*, Abstract (“allowing internal correction of impedance measurement drift, maximized measurement accuracy, and minimized system size.”); Ex. 2004 ¶¶ 43-45. Nowhere does Jones disclose—or even suggest—any desire to increase the speed of performing the impedance measurements, let alone to dramatically increase that speed from seconds to millisecond time resolution. Ex. 2004 ¶ 43.

And while Jones teaches that a “mother board” is connected to each of the daughter boards that are physically arranged in parallel (*id.* ¶ [0020] (“The ZMS daughter boards mate at their lowest edge with the mother board.”)), and the mother board receives the impedance measurements from the daughter boards, Jones does not teach or suggest that the mother board performs any impedance measurements, and does not disclose that *any* processing of the received

measurements from the “measurement circuitry” on the daughter boards is performed in parallel:

The mother board accommodates various electrical components and functions, including the digital signal source, excitation low pass filtering, supervisory processing, ROM/RAM, host data communications, and may control enclosure temperature. The mother board processes the impedance measurement data, at a specific time and frequency, of all wells of the microtiter plate and communicates the results to the system controller.

Id. ¶ [0020]; Ex. 2004 ¶ 61.

Thus, the “parallelism” referred to by Jones is the physical arrangement of the system’s hardware, such as the parallel daughter boards and the parallel mother board/top contact board/microtiter plate. *See* Ex. 1006, Figs. 1, 2, & 4 (parallel hardware configuration); Ex. 1007, Figs. 1, 2, & 4 (same); Ex. 2004 ¶¶ 43-45, 57-62. Axion has not shown that Jones describes an impedance analyzer that measures more than one impedance at a time, as claimed in Claims 16-22, that is, in a mode of “measurement of multiple-wells’ impedances at a time.” Ex. 1001, Col. 25:2-5; Ex. 2004 ¶¶ 52-56. In particular, Axion does not identify any disclosure in Jones that teaches an impedance analyzer that measures more than one well’s impedance at a time. *Id.*

In stark contrast from Jones, the ’508 Patent expressly distinguishes the “one-well at a time” system of the prior art, such as the system taught by Jones:

For example, if the system comprises a device having 96 wells, the system hardware and software should be capable of, for a given time period, measuring the impedances of all 96 wells with millisecond time resolution between two adjacent or consecutive impedance measurement points for each and every well. Thus, comparing two impedance analyzers, one for impedance measurement of 96 wells with millisecond resolution and another for impedance measurement of a single well with millisecond time resolution, the one for 96 well measurement is effectively 96-times faster than one for a single well measurement since it is required to have a capability for performing with millisecond time resolution.

Ex. 1001, Col. 24:22-35; Ex. 2004 ¶ 62. Thus, Axion fails to establish that Jones discloses the claimed “an impedance analyzer which measures multiple wells’ impedances at a time” limitation.

D. The ’508 Patent Explains the “Important Improvement” of “Measurement of Multiple-Wells’ Impedances at a Time”, Distinguishing the Conventional “Measurement of One-Well’s Impedance at a Time,” like that Disclosed In Jones

As discussed above, the “an impedance analyzer which measures multiple wells’ impedances at a time” claim limitation is emphasized and explained in the ’508 Patent’s disclosure as a “very important improvement”:

Another example of improvements includes the use of multiple analogue-to-digital (AD) conversion channels so that analog electronic signals from multiple channels can be converted to digital signals simultaneously. Such parallel AD conversion is important,

particular for the system having multiple wells, each of which's measurement time resolution is required to be in the millisecond resolution. And, a **very important improvement** is to replace previous working mode of **"measurement of one-well's impedance at a time"** with a mode of **"measurement of multiple-wells' impedances at a time"**. In "one-well at a time" mode, when the software issues a command for measuring one well's impedance, the measurement circuitry would perform the measurement for one well including signal generation to the well, converting the voltage signal and the electric current signal for the well to digital signal, digitally processing the signals to do impedance calculation and sending the well's impedance data to the computer over the communication line between the impedance measurement circuitry and the computer. The system will not perform any measurement for another well until completing the measurement of this well and until receiving another command for the measurement of another well. In **"multiple wells at a time"** mode, the software would issue a command for measuring multiple wells' impedances. The measurement circuitry would simultaneously or nearly simultaneously perform signal conversion, signal processing and impedance calculation for multiple wells.

Ex. 1001, Col. 24:62 – 25:32; Ex. 2004 ¶ 64.

The '508 Patent further provides a practical example of how its new and improved system using an impedance analyzer which measures "multiple wells at a time" is a dramatic improvement over a conventional "one well at a time" system:

[C]omparing two impedance analyzers, one for impedance measurement of 96 wells with millisecond resolution and another for impedance measurement of a single well with millisecond time resolution, the one for 96 well measurement is **effectively 96-times faster** than one for a single well measurement since it is required to have a capability for performing impedance measurement for all 96 wells with millisecond time resolution.

Ex. 1001, Col. 24:27-35; Ex. 2004 ¶ 65.

The '508 Patent also relates the impedance analyzer which measures “multiple wells at a time” to the “millisecond time resolution” claim limitation:

[W]here the device includes **multiple wells**, the impedance analyzer has the capability to allow impedance measurements for **each and every well at millisecond time resolution**. That is to say, for a selected time period, the impedance data for **each and every well of the system is measured at millisecond time resolution**. Further, when groups of wells are monitored, the **groups are monitored at millisecond time resolution**.

Ex. 1001, Col. 3:24-32; Ex. 2004 ¶ 66.

In contrast to the improvements described and claimed in the '508 Patent, Jones simply discloses the conventional “measurement of one well’s impedance at a time”. Ex. 1006 ¶ [0030]; Ex. 2004 ¶¶ 52-56. That is, Jones simply discloses a conventional system that measures the impedance of each well in series, using known multiplexing techniques, to achieve a total “update period” of 1.5 seconds.

Id. Jones nowhere discusses an impedance analyzer which measures “multiple wells at a time,” or even improving the speed of measuring multiple wells. Ex. 2004 ¶¶ 43, 52-56.

Accordingly, the claimed “an impedance analyzer which measures multiple wells’ impedances at a time” of the ’508 Patent, as described and claimed, provides a substantial improvement in the field of impedance measuring systems, particularly with respect to measuring multiple wells at a time using A2D converters arranged in parallel with one another.

VI. The Petition Should be Denied Under 35 U.S.C. § 325(d)

Section 325(d) provides that the Director may deny institution of an IPR “if the challenges to the patent is based on matters previously presented to the Office.” 35 U.S.C. § 325(d). Axion relies on only two references for its challenge to the patentability of the ’508 Patent: (1) Xu-752; and (2) Jones. Pet. at 1. Axion asserts, incorrectly, that “[n]either reference was cited by the PTO or applied during prosecution of the ’508 patent.” *Id.* at 2. Consequently, Axion wholly ignores the Section 325(d) basis for denial of institution.

As discussed below, Xu-752 was presented to, and evaluated by, the Office during prosecution of the ’508 Patent. In addition, Axion relies on Jones for the same purposes as other references that were evaluated by the Office during prosecution, and therefore Jones is cumulative prior art. Because Axion fails to

recognize and address the Section 325(d) issue, Axion also fails to demonstrate that the Office erred in any manner material to the patentability of the '508 Patent during prosecution. Thus, under the two-prong framework set forth in the Board's precedential *Advanced Bionics* decision, the Petition should be denied under Section 325(d).

A. The Legal Standard

“Section 325(d) provides that the Director may elect not to institute a proceeding if the challenge to the patent is based on matters previously presented to the Office.” *Advanced Bionics, LLC v. Med-El Electromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 7 (PTAB Feb. 13, 2020) (precedential) (“*Advanced Bionics*”). The Board applies a two-part framework to determine matters under Section 325(d):

(1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.

Id. at 8. To apply that framework, the Board may consider six non-exclusive factors set forth in *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (“*Becton, Dickinson*”):

(a) the similarities and material differences between the asserted art and the prior art involved during examination; (b) the cumulative nature of the asserted art and the prior art evaluated during examination; (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection; (d) the extent of the overlap between the arguments made during examination and the manner in which petitioner relies on the prior art; (e) whether petitioner has pointed out sufficiently how the examiner erred in its evaluation of the asserted prior art; and (f) the extent to which additional evidence and facts presented in the petition warrant reconsideration of the prior art or arguments.

Advanced Bionics, Paper 6 at 9 (citing *Becton, Dickinson*, Paper 8 at 17-18 (precedential as to § III.C.5, first paragraph)). Specifically, factors (a), (b), and (d) pertain to part one of the framework, *i.e.*, whether the same or substantially the same art or arguments previously were presented to the Office; and factors (c), (e), and (f) pertain to part two of the framework, *i.e.*, whether the petitioner has demonstrated a material error by the Office. *Advanced Bionics*, Paper 6 at 10.

B. Substantially the Same Art and Arguments Previously Were Presented to the Office

As explained below, Xu-752 was presented to the Office in an IDS and considered by the examiner during the prosecution of the '508 Patent. Jones discloses substantially the same information already considered by the Office in the context of the Oka (Ex. 1026) and Yu (Ex. 1008) references, both of which

were considered by the examiner during the prosecution of the '508 Patent. Thus, the Office found the claims allowable over the same information now asserted by Axion. Accordingly, the first prong of the *Advanced Bionics* framework is met.

1. Xu-752 Was Presented to, and Evaluated by, the Office During Prosecution of the '508 Patent

Axion asserts that Xu-752 was not “cited by the PTO or applied during prosecution of the '508 patent.” Petition at 2, 11. This assertion is simply incorrect. It cannot be disputed that Xu-752 was disclosed to the Office in an IDS during the prosecution of the '508 Patent. Pet. at 2; Ex. 1002 at 133; Ex. 2002 at 159 (IDS submitted by the applicant, listing “7192752 B2 2007-03-20 Xu, et al.”). The IDS was initialed by the examiner, indicating that references listed on the IDS, including Xu-752, were considered by the examiner. Ex. 2002 at 234 (“/A.H/ . . . 7192752 B2 2007-03-20 Xu, et al.”). Indeed, Xu-752 is listed on the face of the '508 Patent under “References Cited.” Ex. 1001 at 2, Col. 2:9 (“7,192,752 B2 3/2007 Xu et al.”).

When evaluating the *Becton, Dickinson* factors for the Section 325(d) analysis, there is no authority that requires interpreting “involved” or “evaluated” during examination as “cited by the PTO or applied during prosecution.” Indeed, the Board’s precedent considers art provided to the Office by an applicant on an IDS as previously presented art for Section 325(d) analysis. *Advanced Bionics*, Paper 6 at 7-8. And the Board has consistently reached the same conclusion. *See*,

e.g., Microsoft Corp. v. IPA Techs, Inc., IPR2019-00840, Paper 9 at 15–17 (PTAB Nov. 12, 2019) (finding that the “FIPA97” reference, which appears on the face of the challenged patent but not relied on in a rejection, was both “involved” and “evaluated” during examination); *Google LLC v. Valtrus Innovations LTD*, IPR2022-01197, Paper 18 at 15-17 (PTAB June 13, 2023) (finding that a reference provided to the Office in an IDS was “involved” and “evaluated” during examination pursuant to *Becton, Dickinson* factors (a) and (b)).

Axion grudgingly acknowledges that Xu-752 was disclosed “in an IDS that listed over 330 documents.” Pet. at 2. Axion appears to suggest that the examiner somehow failed to consider Xu-752 because there were purportedly too many references in the IDS. *Id.* But the number of references disclosed in an IDS is not relevant for evaluating the *Becton, Dickinson* factors. In fact, the Board has found that a reference, which was cited in an IDS with over 1,200 other prior art references but not cited in a rejection or discussed by the examiner, was “involved during examination.” *AgaMatrix, Inc. v. Dexcom, Inc.*, IPR2018-01715, Paper 10, 10, 13–14 (PTAB Feb. 19, 2019).

Accordingly, Xu-752 was “involved” and “evaluated during examination” of the ’508 Patent and therefore is prior art previously presented to the Office for purposes of prong one of the *Advanced Bionics* Section 325(d) analysis.

2. Jones Is Substantially the Same as Previously Considered References With Respect to the “ADC” Limitations and the “Millisecond Time Resolution” Limitation

Axion argues that “Xu-752 describes the combination of every structural component in claims 1-22, except for ADCs, and also describes the claimed functionality, except for sampling at ‘millisecond time resolution.’” Pet. at 31. Axion further asserts that Jones “describes an improved impedance measurement system that includes the limitations that Xu-752 does not explicitly describe.” *Id.* at 31-32. Axion then contends that “[t]he combination of Xu-752 and Jones discloses” several elements of claims 1, 2-4, and 16 of the ’508 Patent that are directed to ADCs and/or millisecond time resolution. *Id.* at 52-55 (elements 5 and 6 of claim 1), 58-60 (claims 2-4), 66-68 (element 1 of claim 16), 68-73 (elements 3-6 of claim 16). Axion further contends that claims 9-14, which are directed to various millisecond time resolution, “would have been obvious over Xu-752 and Jones.” *Id.* at 63. Thus, Axion relies on Jones’ disclosures for the ADC limitations and millisecond time resolution limitation of the ’508 Patent. *Id.* at 33-36.

As discussed in Section IV.C, *supra*, although Jones contains disclosures relating to a 1.5 second update period for impedance measurements, it does not disclose the millisecond time resolution limitation as claimed in the ’508 Patent. Indeed, several other references were considered during prosecution that have

disclosures similar to, and cumulative of, Jones' disclosures relating to Axion's arguments regarding the ADCs and millisecond time resolution claim limitations.

a. Jones' Disclosure of ADCs is Cumulative of the Examiner's Reliance on the Disclosure of Oka

Axion asserts that, with respect to the ADC limitations of the '508 Patent, "Jones describes that (i) each row of sensors/wells of a microtiter plate has an associated daughter board, and (ii) each daughter board has an ADC, and multiplexing circuitry enables each well within a given row to be addressed." Pet. at 33. Jones further discloses that "the daughter boards may be equipped with multiple analog-to-digital converters (including one for the voltage channel and one for the current channel)" Ex. 1006 ¶ [0018]. Axion also asserts that "Jones Figure 4 . . . shows eight daughter boards, arranged in parallel." Pet. at 33. Accordingly, Axion relies on Jones for its disclosures of at least two ADCs on each daughter board and that Jones' daughter boards are arranged in parallel.

During prosecution of the '508 Patent, the examiner found that Oka discloses "multiple analogue-to-digital conversion channels to perform signal conversion in parallel across multiple wells" Ex. 2002 at 219, 221.¹⁰ Thus,

¹⁰ Oka is a planar multielectrode array that measures via extracellular recording instead of impedance.

Axion's arguments provided in support of the combination of Jones with Xu-752 are substantially the same as those arguments overcome with respect to Oka for a showing of the requisite parallel processing limitations. Therefore, with respect to arguments provided for the parallel processing/ADC limitations, Jones is substantially the same as, and cumulative of, Oka.

b. Jones' Disclosure of a Millisecond Scan Time for a Single Well Is Cumulative of the Examiner's Reliance on the Disclosures of Oka and Yu

With respect to the millisecond time resolution limitation, Axion relies exclusively on Paragraph 30 of Jones. Pet. at 34. Specifically, "Jones describes an exemplary 1.5-second update period for an entire 96-well plate, where the 1.5-second period includes 1091 milliseconds of measurement time, leaving 409 milliseconds for multiplexer switching and signal settling." *Id.* In addition, "Jones describes that 'no more than 68.2 ms per well for all frequencies is required to obtain sufficient samples'[".]” *Id.*

During prosecution of the '508 Patent, the examiner found that Oka discloses "a time difference between two adjacent measurement is less than 500 ms." Ex. 2002 at 221 (3/28/23 Office Action at 6) (citing Oka, Fig. 5B); *see* Ex. 1026 at Fig. 5B "200 msec intervals."). This 0.2 seconds interval cited by the examiner is even shorter than Jones' disclosure of a "1.5 second update period" for

the time difference between two consecutive measurements. *See* Ex. 1006

¶ [0030].

In addition, the '508 Patent is a continuation of a series of applications that first issued as the '548 Patent. During the prosecution of the '548 Patent, the examiner initially rejected the application as being unpatentable over Xu-752 (the primary reference in Axion's Ground 2), Yu, and several other secondary references. Ex. 1014 at 241; Ex. 2003-5 at 1193; Ex. 1005 (Xu-752); Ex. 1008 (Yu). The examiner relied on Yu for teaching "an impedance device . . . capable of millisecond time resolution and collecting measurements at 50ms/well" Ex. 1014 at 242; Ex. 2003-5 at 1194; Ex. 1008 at 37. Thus, Yu's disclosure of 50ms/well measurement collecting time for a single well is faster than the 68.2ms/well time for a single well disclosed in Jones.

Thus, with respect to the arguments provided in support the millisecond time resolution limitation, Jones discloses (at the most) substantially the same information as the examiner relied upon in Oka and Yu. Accordingly, with respect to arguments provided for millisecond time resolution limitation, Jones is substantially the same as, and cumulative of, Oka and Yu.

c. Jones Is Cumulative of Oka and Yu, Both of Which Are of Record

It is undisputed that Xu-752 was evaluated during the prosecution of the '508 Patent. Although the Jones reference itself was not before the Office, as

discussed above, Jones is cumulative of Oka and Yu with respect to the ADC limitations and/or the millisecond time resolution limitation. Axion relies on Jones in the same manner as the examiners relied on Oka and Yu for those claim limitations. Thus, Ground 2 in the Petition only includes “the same or substantially the same prior art that was previously presented to the office.” *Advanced Bionics*, Paper 6 at 14-19 (finding that a reference not of record during prosecution of the challenged patent was substantially the same art as a considered reference because the petitioner relied on the reference not of record in the same manner as the examiner relied on the considered reference during prosecution). Accordingly, the first prong of the *Advanced Bionics* Section 325(d) analysis is met here.

C. Axion Fails to Demonstrate any Material Error by the Office

With respect to the second prong of the Section 325(d) analysis, the Board evaluates whether a petitioner has “demonstrate[d] that the Examiner erred in the evaluation of the prior art, for example, by showing that the Examiner misapprehended or overlooked specific teachings in the relevant prior art such that the error by the Office was material to the patentability of the challenged claims.” *Advanced Bionics*, Paper 6 at 21.

Here, Axion fails to identify any errors by the examiner during prosecution. Axion makes the generalized assertion that the PTO should never have issued the ’508 Patent. Pet. at 1, 11. However, Axion does not point to any specific

teachings in Xu-752, Oka, or Yu that the Office misapprehended or overlooked. In fact, Axion argues, incorrectly, that “[n]either [Xu-752 or Jones] was cited by the PTO or applied during prosecution of the ’508 Patent.” *Id.* at 2. Axion also argues that the examiner “did not apply the best available prior art of which the PTO was already aware (Xu-752, Yu) and was missing other relevant art (Jones).” *Id.* at 11. These generalized arguments are, at best, directed to the first prong of the *Advanced Bionics* framework, *i.e.*, whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office. As discussed above, Axion ignores the relevant Section 325(d) analysis and overlooks the relevant evidence.

Axion laments that there are too many disclosed references (“[t]he patentee [sic] disclosed Xu-752 in an IDS that listed over 330 documents”) (Pet. at 2, 11), the examiners are different (“the PTO Examiner for Wang-548 and the ’508 patent was not the same”) (*id.*), and “the ’508 prosecution was not rigorous—one rejection, one interview, one response with claim amendments, and allowance.”). *Id.* at 11. But other than criticizing Agilent’s and the Office’s conduct during prosecution, Axion does not assert that that the examiner erred in evaluating any prior art or argument, let alone in a manner material to patentability. Accordingly, the second prong of the *Advanced Bionics* framework is also met.

VII. Axion Has Not Shown a Reasonable Likelihood of Success of Prevailing on at Least One Challenged Claim Based on Xu-752 and Jones (Ground 2)

The '508 Patent “relates generally to impedance-based monitoring of cells and more particularly to systems and methods for monitoring excitation-contraction coupling and excitable cells using impedance based systems with millisecond time resolution.” Ex. 1001, Col. 1:28-32. The millisecond time resolution is necessary to effectively monitor impedances of excitation-contraction coupling and excitable cells because those cells have activities in the milliseconds. *E.g., id.*, Col. 16:40-58. Indeed, the '508 Patent describes devices and systems which “fill a major technological gap in monitoring of excitation-contraction coupling and excitable cells, such as cardiomyocytes, in vitro” by “the development of an impedance-based system and monitoring method that employs millisecond time resolution.” *Id.*, Col. 16:19-24. Thus, prior art like Xu-752 and Jones that does not disclose the “millisecond time resolution” limitation completely miss a key inventive aspect of the '508 Patent.

The '508 Patent further explains that “[a] number of improvements in the impedance measurement circuitry, electronic switching circuitry, communication between impedance measurement circuitry and software can be used to achieve such millisecond time resolution.” *Id.*, Col. 24:53-56. One of the “very important improvement[s] is to replace previous working mode of ‘measurement of one-

well's impedance at a time' with a mode of 'measurement of multiple-wells' impedances at a time.'" *Id.*, Col. 25:2-5. This is because "[i]n 'multiple wells at a time' mode, the software would issue a command for measuring multiple wells' impedances. The measurement circuitry would simultaneously or nearly simultaneously perform signal conversion, signal processing and impedance calculation for multiple wells." *Id.*, Col. 25:17-19. Thus, the "an impedance analyzer which measures multiple wells' impedances at a time" limitation is directed to the "multiple wells at a time" mode, and not disclosing this limitation in the relied-upon references misses another key inventive aspect of the '508 Patent.

Xu-752 and Jones, as discussed above, do not disclose the "millisecond time resolution" or the "an impedance analyzer which measures multiple wells' impedances at a time" claim limitations. Thus, Xu-752 and Jones describe nothing more than what was already known in the field at the time of invention, which the examiner considered during prosecution of the '508 Patent. Thus, combining these two references would not get any closer to the invention described and claimed in the '508 Patent.

In addition, Jones is directed to utilizing "a novel combination of parallel impedance measurement channels, multiplexing, and reference impedance networks" to "allow[] internal correction of impedance measurement drift, maximized measurement accuracy, and minimized system size." Ex. 1006,

Abstract, ¶ [0003]. Therefore, the objective of Jones was *not* to reduce the impedance measurement time, but to improve measurement accuracy and reduce thermal drift and system size. *Id.*, Abstract, ¶¶ [0003], [0023], [0044]. Jones nowhere discusses any objective of measuring impedance in millisecond time resolution. Ex. 2004 ¶ 43. Thus, even if there were a desire to develop an impedance system that would be capable of millisecond time resolution based on the teachings of Xu-752 (which in fact there is not), a POSA would not look to Jones to satisfy that desire because Jones does not teach an impedance system capable of millisecond time resolution, or even suggest any solution or reason to increase the *seconds* time resolution of Jones' disclosed system.

Accordingly, Xu-752 in combination with Jones does not render obvious the claims of the '508 Patent because they both fail to disclose the "millisecond time resolution" and "an impedance analyzer which measures multiple wells' impedances at a time" limitations. *See e.g., Securus Tech., Inc. v. Global Tel*Link Corp.*, IPR2016-00267, Paper 8 at 8-13 (PTAB June 3, 2016) (the petitioner failed to show that the prior art disclosed two limitations of the claims of the challenged patent; accordingly, the PTAB found that the petitioner failed to meet its burden and declined to institute the requested *inter partes* review.); *VMR Prod. LLC v. Fontem Holdings I B.V.*, IPR2015-00859, Paper 9 at 14-17 (PTAB Sept. 16, 2015) (similar); *Lenroc Co. v. Enviro Tech Chem. Servs., Inc.*, IPR2014-00382, Paper 12

at 15-16 (PTAB July 24, 2014) (similar). Neither of these claim limitations was well-known or common knowledge in the 2008 time frame, and Axion does not assert as much. And Axion nowhere suggests (nor could it reasonably do so) that a POSA would have somehow modified the Xu-752 and/or Jones references to satisfy the “millisecond time resolution” and the “an impedance analyzer which measures multiple wells’ impedances at a time” claim limitations.¹¹ Thus, Xu-752 in combination with Jones does not render obvious any of Claims 1-22 of the ’508 Patent (Ground 2).

¹¹ Axion argues that the Impedance Measurement System disclosed in Jones could be modified in some unspecified manner and operated somehow differently to shorten the expressly disclosed times of 68.2 ms/well with a 1.5 second “update period.” *E.g.*, Pet. at 53-54. However, Axion’s arguments are nothing more than hindsight-induced attempts to overhaul and reengineer the system described in Jones after viewing the ’508 Patent, purposely disregarding Jones’ express and straightforward disclosure. There is no teaching or suggestion in Jones to make any such modifications. Ex. 2004 ¶ 43. And there is no teaching or suggestion in Jones why any such modifications would be particularly desirable. *Id.*

VIII. Conclusion

For the foregoing reasons, Axion has failed to meet its burden to show that an *inter partes* review should be initiated. Accordingly, Agilent respectfully requests that the Board deny the Petition for *Inter Partes* Review.

Respectfully submitted,

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Dated: December 26, 2024

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CERTIFICATE OF WORD COUNT UNDER 37 C.F.R. § 42.24(d)

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that foregoing Patent Owner Preliminary Response, exclusive of the parts exempted as provided in 37 C.F.R. § 42.24(b), contains 12,612 words and therefore complies with the type-volume limitations of 37 C.F.R. § 42.24(b)(1).

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of the **PATENT OWNER**
PRELIMINARY RESPONSE is being served on December 26, 2024,
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