

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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AXION BIOSYSTEMS, INC.,  
Petitioner,

v.

AGILENT TECHNOLOGIES, INC.,  
Patent Owner.

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IPR2024-01467  
Patent 11,906,508 B2

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Before GEORGIANNA W. BRADEN, DAVID COTTA, and  
MICHAEL A. VALEK, *Administrative Patent Judges*.

VALEK, *Administrative Patent Judge*.

DECISION  
Granting Institution of *Inter Partes* Review  
35 U.S.C. § 314

## I. INTRODUCTION

Axion BioSystems, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”), seeking *inter partes* review of claims 1–30 of U.S. Patent No. 11,906,508 B2 (Ex. 1001, “the ’508 patent”). Agilent Technologies, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

In its Preliminary Response, Patent Owner states it “has statutorily disclaimed claims 9, 10, and 23–30” of the ’508 patent. Prelim. Resp. 6 (citing Ex. 2001 (disclaimer dated Dec. 20, 2024)). Accordingly, Petitioner’s challenges to the patentability of those claims are moot, but the challenges to claims 1–8 and 11–22 remain.

With our authorization, Petitioner filed a Reply to Patent Owner’s Preliminary Response (Paper 7, “Prelim. Reply”) to address Patent Owner’s discretionary denial arguments under 35 U.S.C. § 325(d), and Patent Owner filed a Sur-reply (Paper 8, “Prelim. Sur-reply”).

Considering the arguments and evidence currently of record, we determine the Petition demonstrates “a reasonable likelihood that [P]etitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). We also decline to exercise discretion to deny institution under § 325(d). Accordingly, we institute *inter partes* review of claims 1–8 and 11–22 of the ’508 patent.

## II. BACKGROUND

### A. Real Parties-in-Interest

The parties identify themselves as the real parties-in-interest. Pet. 83; Paper 4, 1.

*B. Related Matters*

The parties identify *Agilent Technologies, Inc. v. Axion BioSystems, Inc.*, 1:24-cv-00300 (D. Del.) as a related matter involving the '508 patent. Pet. 84; Paper 4, 21.

*C. The '508 Patent*

The '508 patent issued on February 20, 2024, and claims priority to a series of applications, the earliest of which was filed on May 5, 2008. Ex. 1001, codes (45), (60).

The '508 patent generally describes “[a] system for monitoring cells, which includes a device for monitoring cell-substrate impedance, the device having a plurality of wells on a nonconductive substrate” where each well has an electrode array for measuring the cell-substrate impedance. Ex. 1001, Abstr. “[E]lectronic circuitry with multiple analogue-to-digital conversion channels” connects the electrode arrays to an “impedance analyzer” that measures the impedance over time. *Id.* The system further includes “a software program that controls the electronic circuitry and records and analyzes data obtained from the impedance analyzer.” *Id.* at 3:11–13.

At least some embodiments of this system provide impedance monitoring at “millisecond time resolution.” Ex. 1001, 3:44–45. In a subsection titled “Definitions,” the Specification explains that:

As used herein, “impedance measurement at millisecond time resolution” refers to the ability to perform a series of at least two consecutive impedance measurements within milliseconds of one another for each and every well of the system where each well is associated with an electrode array for impedance measurement. In each instance the time between two consecutive impedance measurements are less than 300 milliseconds from one another.

*Id.* at 9:34, 10:8–15. Elsewhere the Specification notes that “required or desired time resolution may vary” and “[i]n some embodiments 500 millisecond time resolution is sufficient, such that at least two consecutive impedance measurements are between about 300 milliseconds and about 500 milliseconds apart.” *Id.* at 23:47–55: *see also id.* at 24:35–39 (similar).

#### *D. Challenged Claims*

After Patent Owner’s statutory disclaimer, the remaining challenged claims are claims 1–8 and 11–22. Independent claim 1 is reproduced below, reformatted with the designations Petitioner uses to identify limitations shown in brackets.

1. [Preamble] An apparatus for continuous, label free, real-time monitoring of cells using impedance-based analysis, the apparatus comprising:
  - [Element 1] a) a multiwell plate comprising a plurality of wells on a nonconductive substrate,
  - [Element 2] wherein each of the plurality of wells comprises an electrode array of a plurality of electrode arrays that is disposed on the nonconductive substrate;
  - [Element 3] b) an impedance analyzer that independently measures a cell-substrate impedance at each well,
  - [Element 4] the cell-substrate impedance being measured between a first electrode structure and a second electrode structure of the electrode array and across a cellular sample comprising a plurality of cells disposed within each well,
  - [Element 5] the impedance analyzer including at least two analogue-to-digital conversion channels coupled to the plurality of electrode arrays,
  - [Element 6] wherein the impedance analyzer monitors the electrode arrays at millisecond time resolution between first measurements of the cell-substrate impedance and second measurements of the cell-substrate impedance for each well;
- and

[Element 7] c) a software program that analyzes the first measurements and the second measurements to produce a time period analysis of the cellular sample.

Ex. 1001, 46:65–47:21. Claims 2–8 and 11–15 depend from and thus incorporate the limitations of claim 1, including element 6.

Independent claim 16 is reproduced below, reformatted with the designations Petitioner uses to identify different limitations in brackets.

16. [Preamble] A system for continuously monitoring cells in real-time, label free, with impedance-based analysis, the system comprising:

[Element 1] a) a plurality of analog-to-digital (A2D) signal converters electrically arranged in parallel to one another;

[Element 2] b) a well plate comprising a plurality of wells on a nonconductive substrate,

[Element 3] wherein each well of the plurality of wells comprises one electrode array of a plurality of electrode arrays disposed on the nonconductive substrate that is connected to the plurality of A2D signal converters;

[Element 4] c) an impedance analyzer connected to or including the plurality of A2D signal converters,

[Element 5] wherein the impedance analyzer measures, via digitally converted signals from the A2D signal converters, a first plurality of cell-substrate impedances at a first time and a second plurality of cell-substrate impedances at a second time,

[Element 6] the first plurality of cell-substrate impedances and the second plurality of cell-substrate impedances being measured between a first electrode structure and a second electrode structure in each electrode array and across a cell sample attached within each well of the plurality of wells; and

[Element 7] d) a software program that analyzes the first plurality of cell-substrate impedances from the first time and the second plurality of cell-substrate impedances from the second time to produce a plurality of time period analyses of the plurality of cell samples,

[Element 8] wherein individual time period analyses of the plurality of time period analyses are associated with individual wells of the plurality of wells.

Claims 17–22 depend from claim 16. Claims 16–22 differ from claim 1 and its dependent claims in that they do not recite that the impedance analyzer “monitors the electrode arrays at millisecond time resolution” between measurements (hereinafter “the ‘millisecond time resolution’ limitation”).

*E. Asserted Grounds of Unpatentability*

Petitioner’s Ground 1 alleging that claims 23–30 are anticipated by Xu-752<sup>1</sup> is moot in light of Patent Owner’s disclaimer of those claims. *See* Pet. 1; Ex. 2001 (disclaimer). Claims 9 and 10 have also been disclaimed. *Id.* Therefore, the only remaining ground is the following.

| <b>Claim(s) Challenged</b> | <b>35 U.S.C. §<sup>2</sup></b> | <b>Reference(s)/Basis</b>  |
|----------------------------|--------------------------------|----------------------------|
| 1–8, 11–22                 | 103(a)                         | Xu-752, Jones <sup>3</sup> |

In addition to other record evidence, Petitioner offers the declaration of Bruce C. Kim, Ph.D. (Ex. 1003) in support of this ground. Patent Owner offers the declaration of Brian T. Cunningham, Ph.D. (Ex. 2004) with its Preliminary Response.

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<sup>1</sup> US 7,192,752 B2, issued Mar. 20, 2007 (Ex. 1005) (“Xu-752”).

<sup>2</sup> The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), included revisions to 35 U.S.C. § 103 that became effective after the filing of the applications to which the ’508 patent claims priority. Therefore, we apply the pre-AIA version of § 103.

<sup>3</sup> US 2007/0057680 A1, published Mar. 15, 2007 (Ex. 1006) (“Jones”).

### III. ANALYSIS OF PETITIONER’S GROUND

#### *A. Legal Standard*

Under the pre-AIA version of § 103(a), a claim is unpatentable for obviousness if, to one of ordinary skill in the pertinent art, “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made.” 35 U.S.C. § 103(a) (2006); *see also KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

#### *B. Level of Ordinary Skill in the Art*

Petitioner contends a person of ordinary skill in the art (“POSA”) as of May 2009 “would have had a B.S. in electrical/mechanical/biomedical engineering or biological science, or a related field, and approximately 2 years of relevant experience or equivalent study in systems and methods for bioanalysis of cells.” Pet. 14 (citing Ex. 1003 ¶¶ 23–25). Patent Owner does not dispute or otherwise respond to Petitioner’s description of a POSA in its Preliminary Response.

At this stage, we find Petitioner’s description of the level of ordinary skill in the art to be sufficiently supported by the record and apply it for purposes of this decision.

### *C. Claim Construction*

In an *inter partes* review, claim terms “shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b).

The Petition purports to give “all of the claim terms . . . their plain meaning, as understood by the POSA.” Pet. 13. Petitioner observes that the Specification contains a “Definitions” section, but “does not believe there is any need to adopt any definitions from this section to address the grounds” in the Petition. *Id.* (citing Ex. 1001, 9:34–16:14). Regarding the “millisecond time resolution” limitation in claim 1, Petitioner acknowledges that the “Definitions” section “suggests that measurements must occur at less than 300 milliseconds.” *Id.* at 14. But Petitioner urges that “other portions of the specification discuss measurements at 500 milliseconds (and also claims 9-10)” and “[t]he prior art shows measurements taken at 500 or fewer milliseconds.” *Id.* (citing Ex. 1001, 23:52–55, 24:37–39, 39:47–52, 43:27–33, 47:46–41; Ex. 1003 ¶ 28). Thus, Petitioner contends we do “not need to construe ‘millisecond time resolution’ to find the claims unpatentable on the stated grounds.” *Id.*

Patent Owner disagrees. According to Patent Owner, the Specification “defines . . . ‘millisecond time resolution’ to mean that at least two consecutive impedance measurements for each and every well being evaluated in the claimed apparatus or system can be performed in less than 300 milliseconds from one another.” Prelim. Resp. 9 (citing Ex. 1001, 10:8–

24; Ex. 2004 ¶ 31). Patent Owner urges that “[u]nder the correct claim construction—as expressly defined by the ’508 Patent, [Petitioner] does not (and could not) establish that Jones teaches the ‘millisecond time resolution’ claim limitation.” *Id.* at 11.

We need not resolve this dispute at this stage because claims 16–22 do not recite a “millisecond time resolution” limitation, and, as explained below, Petitioner has demonstrated a reasonable likelihood that it will prevail in demonstrating those claims are unpatentable.<sup>4</sup> However, to provide guidance for developing this claim construction issue at trial, we offer some initial thoughts regarding the parties’ arguments.

The pertinent portion of the Specification’s “Definitions” section states:

As used herein, “impedance measurement at millisecond time resolution” refers to the ability to perform a series of at least two consecutive impedance measurements within milliseconds of one another for each and every well of the system where each well is associated with an electrode array for impedance measurement. In each instance the time between two consecutive impedance measurements are less than 300 milliseconds from one another.

Ex. 1001, 10:8–15. There does not appear to be any dispute as to the definitional nature of the first sentence in the passage above. That is, Petitioner appears to agree that the recitation of “millisecond time resolution” in claim 1 requires that consecutive impedance measurements

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<sup>4</sup> We also determine that no other claim construction is necessary to resolve the issues presented at this stage of the proceeding. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.”).

occur within milliseconds of one another for each and every well in the system. *See* Pet. 14 (urging no specific construction is necessary because, consistent with the broader description in the Specification, the prior art discloses taking consecutive measurements less than 500 milliseconds apart); 53 (offering an example of a 16-well system where consecutive measurements are “repeated every 470 milliseconds” for each well).

The parties’ dispute centers on the second sentence, which states that “[i]n *each instance*” the time between consecutive measurements is “less than 300 milliseconds from one another.” Ex. 1001, 10:13–15 (emphasis added). Taken on its own, this sentence supports Patent Owner’s position that regardless of its ordinary meaning, “millisecond time resolution” as used in the ’508 patent requires that consecutive measurements for a given well occur less than 300 milliseconds apart. *See Thorner v. Sony Computer Entertainment America LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012) (An exception to the “general rule” that claim terms have their ordinary meaning as understood by a POSA is “when a patentee sets out a definition and acts as his own lexicographer.”).

As Petitioner points out, however, other portions of the intrinsic record seemingly contradict the second sentence from the “Definitions” section and support a broader interpretation of the term “millisecond time resolution,” i.e., one encompassing measurements occurring as long as 500 milliseconds apart. *See* Pet. 14. For example, the Specification elsewhere explains that “[i]n some embodiments 500 millisecond time resolution is sufficient.” Ex. 1001, 23:49–55; *see also id.* at 24:37–39 (similar). Moreover, dependent claims 9 and 10, which were originally at issue but have since been disclaimed, state that “*the* millisecond time resolution”

(referring to the term as initially recited in claim 1 for antecedent) between consecutive measurements is “less than 500 milliseconds” (claim 9) and “between 500 and 100 milliseconds” (claim 10). *Id.* at 47:46–51 (emphasis added).

At this stage, neither party has sufficiently addressed this seeming contradiction in the intrinsic record. Therefore, this issue would benefit from further development. In particular, the parties are encouraged to address the following in their subsequent papers at trial: (1) the extent to which the second sentence from the “Definitions” section should be considered definitional of the maximum time between measurements allowed by the term “millisecond time resolution” in view of the other instances noted above where the intrinsic record appears to use the term more broadly; (2) whether Patent Owner’s statutory disclaimer (Ex. 2001) affects the probative weight of claims 9 and 10 in the claim construction analysis; and (3) any claim construction precedent involving a lexicographer definition that the parties consider similar to the facts here.

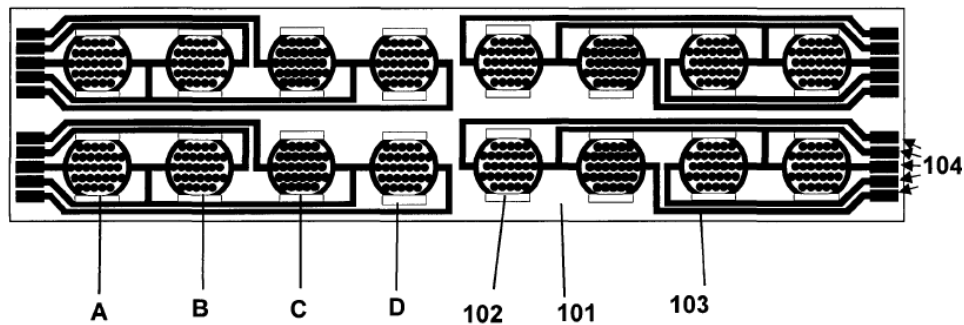
#### *D. Asserted References*

##### *i. Xu-752*

Xu-752 is a patent issued on March 20, 2007. Ex. 1005, code (45). Petitioner asserts, and Patent Owner does not dispute, that Xu-752 qualifies as prior art under 35 U.S.C. § 102(b). Pet. 2.

Xu-752 discloses systems and devices “for assaying cells using cell-substrate impedance monitoring.” Ex. 1005, code (57). Xu-752’s system comprises “one or more cell-substrate monitoring devices comprising multiple wells each having an electrode array, an impedance analyzer, a

device station that connects arrays of individual wells to the impedance analyzer, and software for controlling the device station and impedance analyzer.” *Id.* Figure 1A of Xu-752, reproduced below, is a schematic drawing of the cell-substrate impedance measurement device.



The embodiment shown in Figure 1A above has 16 electrode arrays 102 arranged in a 2-row by 8-column configuration on glass substrate 101. *Id.* at 7:20–24; 19:35–40. “The substrate of the device has a surface suitable for cell attachment or growth,” which “can result in a detectable change in impedance between or among the electrode structures within each electrode array.” *Id.* at 4:8–12.

“The device is assembled such that a single array of the substrate is at the bottom of a receptacle or well” and “associated with a well of a multi-well plate.” Ex. 1005, 21:29–33. Figure 4 of Xu-752, reproduced below, depicts multiple cell-substrate impedance measurement devices in a device station.

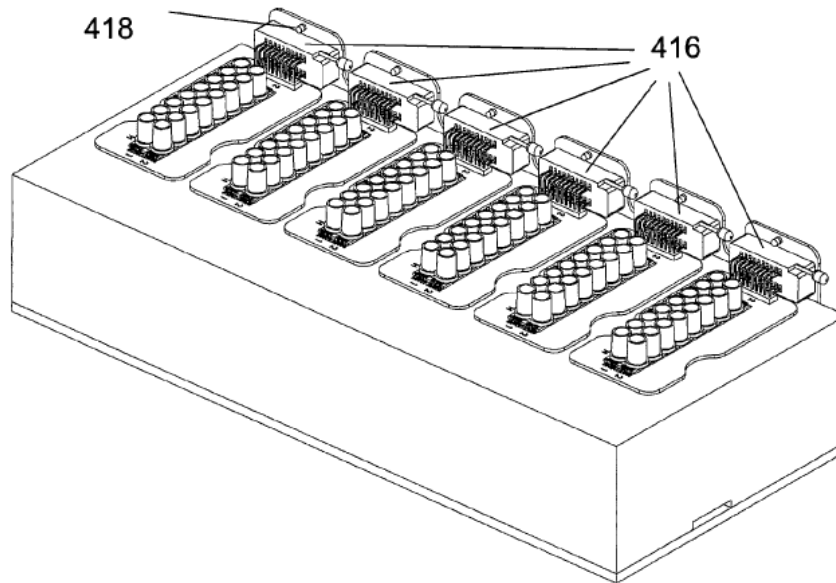


Figure 4 above is an illustration showing six devices each having 16 wells connected to the station through sockets 416. *See id.* at 24:13–24. The station comprises electronic circuitry that connects the electrode arrays in each individual well to an impedance analyzer. *Id.* at 23:44–48, 24:13–24.

Software directs switches in the device station to connect arrays to the impedance analyzer and monitor impedance over time in a given well. *See* Ex. 1005, 23:48–62 (“Preferably, impedance monitoring is performed at more than one time point for a given assay.”). According to Xu-752, “[t]he device station can connect individual arrays of a device to an impedance analyzer to monitor one, some, or all of the arrays of a device for a measurement time point” and selected arrays can “be monitored in rapid succession for each desired monitoring time point.” *Id.* at 23:57–62. Xu-752 further teaches that “the device station software is programmable to direct impedance monitoring of any of the wells of the device that comprise arrays at chosen time intervals.” *Id.* at 23:66–24:2; *see also* Fig. 6, 7:38–55

(showing and describing “pages from real-time cell electronic sensing software”).

*ii. Jones*

Jones is a patent application publication published on March 15, 2007. Ex. 1006, code (43). Petitioner asserts, and Patent Owner does not dispute, that Jones qualifies as prior art under 35 U.S.C. § 102(b). Pet. 2.

Jones discloses an “Impedance Measurement System (ZMS) for measuring the complex impedance of each well of a single well or multiwell microtiter plate utilizing a novel combination of parallel impedance measurement channels, multiplexing, and reference impedance networks.” Ex. 1006, code (57), ¶ 3. According to Jones, its “system can be used for impedance measurements of varying time periods, single or multiple frequencies, and various measurements rates” and “employs parallelism to obtain the required throughput at the repeatability required.” Ex. 1006 ¶ 3.

In Jones’s system, “each row of sensors on a microtiter plate is addressed by measurement circuitry (in the form of analog signal conditioning circuits, multiplexing circuits, analog-digital converter, and digital signal processors) on a single daughter board.” Ex. 1006 ¶¶ 12, 18 (teaching that “daughter boards carry the electronic components to drive and process a row of wells” and “may be equipped with multiple analog-to-digital converters”). The “ZMS daughter boards mate” with a “mother board [that] processes the impedance measurement data, at a specific time and frequency, of all wells of the microtiter plate and communicates the results to the system controller.” *Id.* ¶ 20.

Jones teaches that “[e]ach well is subject to a stepped sweep (a series of single frequency bursts-one burst for each selected frequency.” Ex. 1006

¶ 30. Jones explains that:

From preliminary modeling and testing, no more than 68.2 ms per well for all frequencies is required to obtain sufficient samples. For an embodiment in which [sic] a 96 well plate with 12 wells per row plus four reference network channels, calculations to determine sufficient samples suggest a 1091 mS measurement period, leaving 409 mS for multiplexer switching and signal setting within the target 1.5 second update period.

*Id.*

#### *E. Alleged Obviousness over Xu-752 and Jones*

Petitioner contends that claims 1–8 and 11–22 would have been obvious over Xu-752 and Jones. *See* Pet. 31–88. In particular, Petitioner argues that “Xu-752 describes the combination of every structural component in [these claims] except for ADCs [i.e., analog-to-digital converters<sup>5</sup>], and also the claimed functionality, except for sampling at ‘millisecond time resolution.’” *Id.* at 31. Petitioner asserts that Jones “describes an improved impedance measurement system that includes the limitations that Xu-752 does not explicitly describe” and that “a POSA would have been motivated to combine Xu-752 with Jones for several reasons.” *Id.* at 31–32. At this stage, Patent Owner disputes Petitioner’s

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<sup>5</sup> The Petition defines the term “ADC” to mean “analog-to-digital conversion.” Pet. 10. Both parties, however, use the term “ADCs” to refer to the plurality of “A2D signal converters” recited in claim 16. *See, e.g.*, Pet 66–67; Prelim. Resp. 51–52. We do the same herein. If there is a material distinction between these terms, the parties should clarify that point at trial.

allegations concerning certain teachings in Jones, including those relating to the “millisecond time resolution” limitation. *See* Prelim. Resp. 6–45.

As noted above, claims 16–22 do not recite the “millisecond time resolution” limitation. We begin our analysis with those claims before separately addressing claims 1–8 and claims 11–15 and the parties’ arguments concerning the “millisecond time resolution” limitation.

*i. Claims 16–22*

Petitioner contends that Xu-752 generally discloses the system recited in claim 16, “but does not explicitly describe that its impedance-based cell analysis system has a plurality of ADCs electrically arranged in parallel to one another” and “does not explicitly describe measuring pluralities of impedances via digitally converted signals from the plural ADCs.” *See* Pet. 66–77. Petitioner relies on Jones for these aspects of claim 16, urging that Jones discloses a system with “a plurality of ADCs electrically arranged in parallel to one another,” i.e., on “daughter boards” each of which “has multiple ADCs and a digital signal processor to process impedance data.” *Id.* at 67 (citing Ex. 1006 ¶¶ 2, 3, 12, 14, 18, 20, 35, Figs. 2–4). Petitioner further asserts that Jones teaches using these “parallel impedance measurement channels” to “measure pluralities of impedances, as claimed.” *Id.* at 70 (citing Ex. 1003 ¶ 195; Ex. 1006 ¶¶ 3, 12, 18, 26, 36).

Petitioner argues that “[i]t would have been obvious to a POSA . . . to modify Xu-752’s system for monitoring cells using impedance-based analysis with an impedance analyzer, such as Jones’s device, having the claimed ADC . . . features.” Pet. 36. (citing Ex. 1003 ¶¶ 107–108). According to Petitioner, “a POSA would have readily understood that the use of parallel ADCs for simultaneously measuring multiple impedances

would have advantageously enabled increased throughput,” particularly given Jones’s explicit teachings regarding “parallelism.” *Id.* at 41–42 (citing Ex. 1003 ¶ 117; Ex. 1006 ¶¶ 2–3). Petitioner further contends that “[b]eyond the advantages of parallelism, speed, and efficiency,” Jones describes other advantages, e.g., “internal correction of impedance measurement drift, maximized measurement accuracy, and minimized system size,” that “would have motivated a POSA to modify Xu-752’s system to use Jones’s impedance analyzer.” *Id.* at 43 (citing Ex. 1003 ¶ 121; Ex. 1006 ¶ 3).

Having reviewed Petitioner’s showing, we find that it demonstrates a reasonable likelihood that Petitioner will prevail in demonstrating that claim 16 is unpatenable over Xu-752 and Jones. Patent Owner’s arguments in the Preliminary Response are unavailing on the current record. We address those arguments below.

At this stage, Patent Owner’s arguments against the merits of Petitioner’s showing for this set of claims are premised on the disclosure in Jones as applied to claim 16’s recitation of a plurality of ADCs “electrically arranged in parallel to one other” in element 1 and the phrase “the impedance analyzer measures . . . a first plurality of cell-substrate impedances at a first time and a second plurality of cell-substrate impedances at a second time” in element 5. *See* Prelim. Resp. 24–31. According to Patent Owner, this claim language, particularly when read in light of the supporting description in the Specification, means that the impedance analyzer of claim 16 “measures multiple wells’ impedances on a well plate at the same (or nearly the same) time, *i.e.*, in parallel.” *Id.* at 30–31 (citing Ex. 1001, 25:2–22; Ex. 2004 ¶ 50–51). Patent Owner refers to this as the

“‘an impedance analyzer which measures multiple wells impedances at a time’ limitation.” *Id.* at 31.

Patent Owner argues that the Petition “completely overlooks” this limitation, urging that Petitioner “has not shown that Jones discloses an impedance analyzer which measures the impedances of multiple wells at the same time, versus describing a system having a physical configuration with parallel structural components.” Prelim. Resp. 32. According to Patent Owner, “[e]ach daughter board [in Jones’s system] sequentially takes impedance measurements of one well at a time for each of the wells in a row.” *Id.* at 36. Patent Owner faults Petitioner’s reliance on Jones’s teaching that its system uses “parallel impedance measurement channels,” contending that this and Jones’s other mentions of “parallelism” refer only “to the *physical arrangement* of multiple daughter boards (each board having ‘measurement channels’) placed in parallel with one another within Jones’[s] impedance measurement system.” *Id.* at 25–27, 38, 41 (“[T]he ‘parallelism’ referred to by Jones is the physical arrangement of the system’s hardware, such as the parallel daughter boards and the parallel mother board/top contact board/microtiter plate.”). Thus, Patent Owner contends, Petitioner has not identified “any disclosure in Jones that teaches an impedance analyzer that measures more than one well’s impedance at a time.” *Id.* at 41.

As an initial matter, we agree with Patent Owner that claim 16 requires an impedance analyzer that measures the impedances of multiple wells at a time. Element 5 of claim 16 recites that the “impedance analyzer measures . . . a first plurality of cell-substrate impedances at a first time and a second plurality of cell-substrate impedances at a second time.” Ex. 1001, 48:10–14. Moreover, element 5 states that these measurements occur “via

digitally converted signals from the A2D signal converters,” which element 1 recites as being “arranged in parallel.” *Id.* at 48:1–2, 10–14. Based on the current record, we understand claim 16 to require an impedance analyzer “connected to or including” multiple ADCs that are electrically arranged in parallel and that operate in parallel to make multiple (i.e., a “first plurality” and a “second plurality”) impedance measurements at time.<sup>6</sup> *Id.* at 48:9–14.

We disagree, however, with Patent Owner’s assertion that the Petition overlooks these requirements. Regarding element 1 of claim 16, Petitioner relies on Jones’s disclosure of a system with eight daughter boards electrically arranged in parallel, each of which has “multiple ADCs and a digital signal processor to process impedance data.” Pet. 67 (citing Ex. 1006 ¶¶ 2–3, 12, 14, 18, 20, 35 Figs. 2–4). Regarding element 5, Petitioner explains that Jones’s impedance analyzer “uses digitally converted signals from the plural ADCs to measure plurality of impedances, as claimed,” i.e., by using “parallel impedance measurement channels” to “simultaneously measur[e] multiple impedances.” *Id.* at 41–42, 70–71 (citing Ex. 1003 ¶ 117; Ex. 1006 ¶¶ 3, 12, 18, 26, 35). Petitioner further supports these allegations by citing Jones’s disclosure that each daughter board has “circuitry allowing one or more measurements channels” and that the circuitry in each daughter board is connected to a “mother board” that processes the impedance measurement data for all of the wells in the system. *Id.* at 70–71 (quoting Ex. 1006 ¶¶ 12, 20).

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<sup>6</sup> Element 5 states that the A2D signal converts are “connected to or includ[ed]” in the impedance analyzer.

Patent Owner’s argument in its Preliminary Response that Jones’s teachings regarding “parallelism” are limited only to the physical arrangement of its components is unavailing. Jones teaches that its system utilizes “parallel impedance measurement channels” and “employs parallelism *to obtain the required throughput* at the repeatability required.” Ex. 1006 ¶ 3 (emphasis added). At least on the current record, these teachings reasonably suggest that not only are Jones’s plurality of ADCs physically arranged on parallel daughter boards, but also that such hardware is operated in parallel to measure multiple wells’ impedances at a time, thereby increasing system throughput. Ex. 1003 ¶ 117.

Indeed, on the preliminary record, it is unclear what other purpose Jones’s parallel architecture might serve. The Preliminary Response does not directly address Jones’s teaching that parallelism is employed “to obtain the required throughput.” Ex. 1006 ¶ 3. Instead, Patent Owner suggests that Jones’s physical arrangement of parallel daughter boards is intended to provide a “compact form factor.” *See* Prelim. Resp. 39–40. But even if the physical arrangement of daughter boards does provide for a compact form factor for Jones’s system, this does not explain why Jones employs eight daughter boards each with its own measurement circuitry if that circuitry only operates serially on one daughter board at time, as Patent Owner suggests.

Patent Owner also appears to dismiss Jones’s teaching that its “mother board” is connected to the daughter boards and processes impedance data for all of the wells (Ex. 1006 ¶ 20) because, according to Patent Owner, “Jones does not teach or suggest that the mother board performs any impedance measurements, and does not disclose that *any* processing of the received

measurements from the ‘measurement circuitry’ on the daughter boards is performed in parallel.” *See* Prelim. Resp. 40–41. This distinction is not explained sufficiently in the Preliminary Response and would benefit from further development at trial. In doing so, Patent Owner should address the fact that claim 16 recites “an impedance analyzer *connected to* or including the plurality A2D signal converters,” which seems to suggest that the impedance analyzer need not be co-located with the A2D signal converters or other measurement circuitry. Ex. 1001, 48:9–10 (emphasis added).

For these reasons, Petitioner has established a reasonable likelihood that it will prevail in demonstrating that claim 16 is unpatentable as obvious over Xu-752 and Jones.

Petitioner’s showing for dependent claims 17–22 is also sufficient for institution. The Petition presents evidence and argument sufficient to support Petitioner’s assertion that the cited references teach or suggest the additional limitations recited in each of these claims. Pet. 77–83 (addressing additional limitations in claims 17–22). At this stage, Patent Owner does not make any additional arguments against Petitioner’s showing for these claims and its arguments contesting Petitioner’s showing for claim 16 are unavailing as explained above.

*ii. Claims 1–8 and 11–15*

Petitioner contends that claims 1–8 and 11–15 would also have been obvious over Xu-752 and Jones. *See* Pet. 31–66. As noted above, claims 1–8 and 11–15 differ from claims 16–22 in that they additionally recite the “millisecond time resolution” limitation.

Petitioner argues that “Jones describes an impedance analyzer that can monitor electrode arrays in wells at millisecond-time resolution between two

measurements of cell-substrate impedance for each well.” Pet. 53. More specifically, Petitioner relies on a “simple example” offered by its declarant, Dr. Kim, based on “a 16-well plate with an 8 x 2 configuration (such as in one of Xu-752 preferred plates) with Jones’s exemplary impedance analyzer that uses three reference network channels and eight daughter boards.” *Id.* (citing Ex. 1003 ¶¶ 69–75, 137–140). Dr. Kim uses information from the 96-well embodiment described in paragraph 30 of Jones to calculate the time between measurements for his 16-well example, concluding that in his example “measurements of any given well” would be “repeated every 470 milliseconds.” *Id.* at 54 (citing Ex. 1003 ¶ 137).

In addition, Petitioner relies on a second example from Dr. Kim wherein measurements are taken at a single frequency to “provide for even faster measurements than in the above example. Pet. 54 (citing Ex. 1003 ¶¶ 138–140). In this single frequency example, Dr. Kim assumes the same “16-well plate with an 8 x 2 configuration” with measurements “at a single frequency of 10 kHz,” resulting in measurements being “repeated every 136 milliseconds.” *Id.* According to Petitioner, Dr. Kim’s examples demonstrate “how a POSA would use Jones’s impedance analyzer for impedance measurements with millisecond-time resolution between measurements to monitor multiple wells.” *Id.* at 54–55 (citing Ex. 1003 ¶¶ 69–75, 141, 169–177).

Patent Owner disputes Petitioner’s showing for the “millisecond time resolution” limitation in claims 1–8 and 11–15, urging that Jones discloses a 96-well embodiment with 12 wells per row and four reference network channels that “can perform two consecutive impedance measurements for 12 wells that are 1.5 seconds apart.” Prelim. Resp. 17 (citing Ex. 1006 ¶ 30).

Thus, Patent Owner argues, “Jones operates on a time resolution on the scale of *seconds* versus the claimed *millisecond* time resolution.” *Id.* (citing Ex. 2004 ¶ 35).

Because the burden for institution has been met for claims 16–22, we need not resolve the parties’ disputes regarding the “millisecond time resolution” limitation at this stage, nor do we need to determine whether Petitioner has demonstrated a reasonable likelihood of prevailing on its challenge to claims 1–8 and 11–15. However, to provide guidance for developing these issues at trial, we describe some initial concerns we have regarding Petitioner’s showing for the “millisecond time resolution” limitation.

Petitioner’s showing is premised on the disclosure in paragraph 30 of Jones, which describes a 96-well embodiment. But Jones teaches that embodiment has a “1.5 second update period” between impedance measurements for each of the 12 wells in a given row. Ex. 1006 ¶ 30. The current record supports Patent Owner’s position that Jones’s 96-well embodiment, which “operates on a time resolution on the scale of *seconds*,” does not teach or suggest monitoring at “millisecond time resolution” as recited in claim 1. *See* Prelim. Resp. 17.

Indeed, Petitioner does not argue otherwise. Instead of relying on the 96-well embodiment in paragraph 30, or any other embodiment expressly described in Jones, Petitioner relies on “examples” evidenced by Dr. Kim’s testimony and based on modifications of the 96-well embodiment taught in Jones. *See* Pet. 53–55 (citing Ex. 1003 ¶¶ 69–75, 137–141; Ex. 1006 ¶ 30). Dr. Kim’s examples modify multiple aspects of Jones’s 96-well embodiment, i.e., reducing both the total number of wells and wells per row

to an “8 x 2 configuration,” reducing the number of reference channels from four to three, and further for the single frequency example changing from a “stepped sweep” of multiple frequencies to a single measurement at 10 kHz. *Id.*

Petitioner and Dr. Kim’s reasoning for those changes is not explained sufficiently in the Petition. While Petitioner offers some evidence of applications where faster sampling times are desirable (*see* Pet. 36–41), the relationship, if any, between those applications and the modifications to Jones’s 96-well embodiment that Dr. Kim uses for his examples is unclear. Nor does the Petition account for any negative effects these modifications (i.e., fewer wells, reference channels, frequencies, etc.) would have on Jones’s 96-well embodiment. *See Arctic Cat Inc. v. Polaris Indus., Inc.*, 795 Fed. Appx. 827, \*833 (Fed. Cir. Dec. 23, 2019) (“The Board must weigh[] the benefits and drawbacks of the modification against each other, to determine whether there would be a motivation to combine.”).

In sum, this leads us to question whether the parameters for Dr. Kim’s examples were chosen not because they were obvious, but because they would result in a time between measurements of 500 milliseconds or less, and thereby accord with Petitioner’s apparent interpretation of the term “millisecond time resolution” (*see supra* § III.C).<sup>7</sup> If so, such cherry-picking

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<sup>7</sup> For instance, Dr. Kim’s first example relies on the measurement and “switching/settling” times disclosed in paragraph 30 of Jones, but for only the five measurements, i.e., two wells per row and three reference channels, required in his “8 x 2 configuration,” concluding that the total time between measurements for a given well in his example would be “~470 ms.” Ex. 1003 ¶ 137. Based on these calculations, it would seem that the addition of either another well or another reference channel to the configuration in

suggests that Petitioner’s showing for claims 1–8 and 11–15 is improperly premised on hindsight knowledge of the ’508 patent as opposed to what Jones teaches or reasonably suggests to a POSA regarding the “millisecond time resolution” limitation. This concern exists whether the term “millisecond time resolution” is construed to mean that the time between consecutive measurements for each well is under 300 milliseconds (as Patent Owner contends) or more broadly to encompass consecutive measurements made in 500 milliseconds or less. In any event, these issues are complex and would benefit from further development at trial.<sup>8</sup>

#### IV. DISCRETION UNDER 35 U.S.C. § 325(d)

Patent Owner argues that we should exercise discretion to deny institution under 35 U.S.C. § 325(d) because “Xu-752 was presented to, and evaluated by, the Office during prosecution” and “Jones is cumulative” of other art evaluated during prosecution. *See* Prelim. Resp. 45–55. Patent Owner further asserts that Petitioner has not shown any material error in the Examiner’s consideration of these references. *Id.* at 46. Petitioner disagrees. *See* Prelim. Reply 1–5.

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Dr. Kim’s example would result in a total time between measurements for each well that exceeds 500 milliseconds.

<sup>8</sup> While Petitioner may “address issues discussed in the institution decision” in its reply at trial, Petitioner is cautioned against seeking to introduce new evidence that “it could have presented earlier, e.g. to make out a prima facie case of unpatentability” in the Petition. *See* Consolidated Trial Practice Guide (Nov. 2019) 73–75, *available at* <https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf> (“CTPG”).

*A. Legal Standard*

Section 325(d) provides that the Director may elect not to institute a proceeding if the challenge to the patent is based on matters previously presented to the Office. The statute states, in pertinent part, “[i]n determining whether to institute . . . the Director may take into account whether, and reject the petition . . . because, the same or substantially the same prior art or arguments previously were presented to the Office.” 35 U.S.C. § 325(d).

The question of whether a petition presents art or arguments that are “the same or substantially the same” as art or arguments previously presented to the Office is a factual inquiry, which may be resolved by reference to the factors set forth in *Becton, Dickinson*.<sup>9</sup> The precedential section of that decision sets forth the following non-exclusive factors for consideration:

- (a) the similarities and material differences between the asserted art and the prior art involved during examination;
- (b) the cumulative nature of the asserted art and the prior art evaluated during examination;
- (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;
- (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art;
- (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and

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<sup>9</sup> *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential as to § III.C.5, first paragraph) (“*Becton, Dickinson*”).

(f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

*Becton, Dickinson*, 17–18.

*Advanced Bionics*<sup>10</sup> sets out a two-part framework for analyzing these factors. In the first part, we consider factors (a), (b), and (d) to determine whether the art and arguments presented in the petition are the same or substantially the same as those previously presented to the Office. *Advanced Bionics*, 8–10. “If, after review of factors (a), (b), and (d), it is determined that the same or substantially the same art or arguments previously were presented to the Office,” then we move on to the second part of the analysis to determine “whether the petitioner has demonstrated a material error by the Office” in view of factors (c), (e), and (f). *Id.*

#### *B. Advanced Bionics Part One*

There is no dispute that Xu-752 was cited in an IDS and therefore was previously presented to the Office. Ex. 2002, 159; *see also* Prelim. Reply 1 (Petitioner acknowledging this fact). There is also no dispute that Jones was *not* previously presented to the Office. *See* Prelim. Resp. 53 (Patent Owner acknowledging Jones “was not before the Office”). Instead, the parties dispute whether Jones is cumulative of other art previously presented to the Office and thus whether the Examiner previously considered substantially the same art and arguments as those in the Petition.

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<sup>10</sup> *Advanced Bionics, LLC v. MED-EL Electromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 10 (Feb. 13, 2020) (precedential) (“*Advanced Bionics*”).

As it relates to the parallel processing and ADC limitations in claims 16–22, Patent Owner contends that Jones is cumulative of Oka.<sup>11</sup> According to Patent Owner, “[d]uring prosecution of the ’508 Patent, the examiner found that Oka discloses ‘multiple analogue-to-digital conversion channels to perform signal conversion in parallel across multiple wells ....’” Prelim. Resp. 51 (citing Ex. 2001, 219, 221). Therefore, Patent Owner contends, Petitioner’s arguments in the Petition “are substantially the same as those arguments overcome with respect to Oka for a showing of the requisite parallel processing limitations.” *Id.* at 52.

In reply, Petitioner argues that, unlike Jones, Oka “does not disclose parallel ADCs, nor simultaneous measurements. Oka instead uses a *single ADC* and a switch for sequentially connecting different electrodes to the ADC for *non-simultaneous measurements*.” Prelim. Reply 2. Petitioner also points out that the applicants overcame the Examiner’s rejections based on Oka by “arguing that Oka does not describe measuring cell-substrate impedance, or even taking measurements from multiple wells of a multiwell plate.” *Id.* at 4 (citing Ex. 1002, 187–197).

We agree with Petitioner that Oka is not cumulative of Jones. Jones discloses an impedance measuring system for measuring the impedance of each well of a multiwell plate. Ex. 1006, code (57). Moreover, Jones clearly teaches that the daughter boards in its system “may be equipped with multiple analog-to-digital converters.” *Id.* ¶ 18. Oka, in contrast, does not. As Patent Owner acknowledges, “Oka is a *planar* multielectrode array that

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<sup>11</sup> *Oka et al.*, “A new planar multielectrode array for extracellular recording: application to hippocampal acute slice,” 93 J. of Neuroscience Methods 61–67 (1999) (Ex. 1026) (“Oka”).

measures via extracellular recording *instead of impedance*.” Prelim. Resp. 51 n. 10 (emphases added). This is consistent with the applicants’ arguments during prosecution that Oka does not disclose a multiwell plate, plurality of wells, or even measuring cell-substrate impedance. *See, e.g.*, Ex. 1002, 191–193. Moreover, as Petitioner points out, Oka appears to disclose only a single ADC connected to a switch. *See* Ex. 1026, 63 (Fig. 2); *see also* Ex. 1002, 188 (applicant urging that “*Oka* uses a switch to connect the AD-C to different electrodes at different times” and therefore is not performing measurements for individual electrode arrays). Thus, unlike Jones, Oka does not disclose a plurality of ADCs, much less multiple ADCs arranged and operated in parallel such that impedances for multiple wells are measured at a time.<sup>12</sup>

Nor does it appear that the same or substantially the same arguments advanced for claims 16–22 in the Petition were presented during prosecution of the ’508 patent. There, in response to a non-statutory double patenting rejection based on a related patent and Oka, and an anticipation rejection based on Oka, the claim which became claim 16 in the ’508 patent was substantially rewritten to recite the ADC limitations in elements 1 and 5. Ex. 1002, 182–183 (amendment to claim 18). Along with this amendment, the applicants submitted the arguments discussed above, urging that Oka

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<sup>12</sup> Patent Owner does not dispute the assertion on page 2 of the Preliminary Reply that Oka “uses a *single ADC* and switch.” *See generally* Prelim. Sur-reply 2–3. Instead, Patent Owner reiterates its argument that “neither the Petition nor the [Kim] declaration assert that Jones’[s] ADCs, which are arranged *physically* in parallel, result in an impedance analyzer which measures *electrical* impedance in parallel.” *Id.* We have already addressed this argument above and, on the current record, disagree with Patent Owner. *See supra* § III.E.i.

does not describe the elements “related to the electronic circuitry” in claim 16. *Id.* at 191. The Examiner’s subsequent notice of allowance suggests those arguments were accepted. *See id.* at 204–205 (reasons for allowing claim 18). Accordingly, we see no evidence that arguments similar to Petitioner’s present obviousness ground, which is premised on the combination of two references each of which discloses measuring impedance in a multiwell system and with Jones further describing a system that employs parallel impedance measurement channels and daughter boards having multiple ADCs, were previously presented to the Office.

In sum, we find that neither the same or substantially the same art or arguments were previously presented to the Office in its consideration of claims 16–22.<sup>13</sup>

### *C. Advanced Bionics Part Two*

Because the first step in the *Advanced Bionics* framework has not been shown, we need not reach step two. We therefore decline to exercise discretion to deny institution under 35 U.S.C. § 325(d).

## V. CONCLUSION

Based on the current record, we determine Petitioner has shown a reasonable likelihood that it will prevail in establishing that at least one

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<sup>13</sup> We need not reach Patent Owner’s additional argument that Yu (Ex. 1008) is cumulative of Jones because that argument is limited to the “millisecond time resolution” limitation in claims 1–8 and 11–15. *See* Prelim. Resp. 53. Thus, even if we agreed that Yu’s disclosure was cumulative of Jones in this respect, our determination that substantially the same art/arguments had not been previously presented for claims 16–22 remains the same.

claim of the '508 patent is unpatentable. Accordingly, we institute review of all claims challenged on all of the grounds in the Petition. *See* CTPG 64.

At this stage of the proceeding, the Board has not made a final determination as to the patentability of any challenged claim. Our view with regard to any finding or conclusion reached in the foregoing analysis could change upon completion of the record.

## VI. ORDER

Accordingly, it is:

ORDERED that pursuant to 35 U.S.C. § 314, an *inter partes* review is hereby instituted as to claims 1–8 and 11–22 of the '508 patent based on the unpatentability challenges presented in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial commencing on the entry date of this decision.

IPR2024-01467  
Patent 11,906,508 B2

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