505486615 05/21/2019

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5533419

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
JEFFERIES FINANCE LLC	05/17/2019

RECEIVING PARTY DATA

Name:	LATTICE SEMICONDUCTOR CORPORATION
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	SILICON IMAGE, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	SIBEAM, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	DVDO, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124

PROPERTY NUMBERS Total: 1143

Property Type	Number
Patent Number:	5574678
Patent Number:	5510738
Patent Number:	5493205
Patent Number:	5617064
Patent Number:	5670907

Property Type	Number
Patent Number:	5490074
Patent Number:	5596524
Patent Number:	5491433
Patent Number:	5756367
Patent Number:	5594687
Patent Number:	5570046
Patent Number:	5583451
Patent Number:	5621650
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Patent Number:	5754471
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Property Type	Number
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Patent Number:	5672521
Patent Number:	5809522
Patent Number:	5739713
Patent Number:	5736888
Patent Number:	5719516
Patent Number:	5598346
Patent Number:	5623217
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Patent Number:	5646901
Patent Number:	5751163
Patent Number:	5666087
Patent Number:	5748525
Patent Number:	5864486
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Patent Number:	5723984
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Patent Number:	5991907
Patent Number:	5805607
Patent Number:	5811987
Patent Number:	5892962
Patent Number:	5717342
Patent Number:	6028993

Property Type	Number
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Patent Number:	5885904
Patent Number:	6190966
Patent Number:	5905385
Patent Number:	5844912
Patent Number:	5835405
Patent Number:	6087275
Patent Number:	6034541
Patent Number:	5949279
Patent Number:	5989957
Patent Number:	5978272
Patent Number:	6028447
Patent Number:	6072351
Patent Number:	6359466
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Patent Number:	6093946
Patent Number:	6128770
Patent Number:	6064225
Patent Number:	5982683
Patent Number:	6556154
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Patent Number:	6154050
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Patent Number:	6524911
Patent Number:	6287916
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Patent Number:	6414521
Patent Number:	6496969
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Patent Number:	7339952
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Application Number:	10392751
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Patent Number:	6873187
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Patent Number:	7064973
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Patent Number:	7382293
Patent Number:	7589648
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Property Type	Number
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Patent Number:	7295035
Patent Number:	7411419
Patent Number:	7606851
Patent Number:	7187586
Application Number:	11206282
Patent Number:	7301182
Patent Number:	7167405
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Patent Number:	7538574
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Patent Number:	7466190
Patent Number:	7521969
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Property Type	Number
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Patent Number:	7535258
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Property Type	Number
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Patent Number:	8069329
Patent Number:	7652500
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Property Type	Number
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Patent Number:	7768300
Patent Number:	8255733
Patent Number:	7969248
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Property Type	Number
Application Number:	14021513
Application Number:	14043920
Application Number:	14053026
Application Number:	14070975
Application Number:	14095310
Application Number:	14136482
Application Number:	14137443
Application Number:	14147796
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Patent Number:	6786564
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Application Number:	61989417
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Property Type	Number
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Application Number:	61989411
Application Number:	14463146
Application Number:	14578266
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Application Number:	62089767
Patent Number:	8482462
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Application Number:	14196993
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Application Number:	62100841
Patent Number:	8571126
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Application Number:	14234623
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Patent Number:	6374361
Patent Number:	6738417

Property Type	Number
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Patent Number:	7408992
Patent Number:	7123307

Property Type	Number
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Patent Number:	7062004
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Patent Number:	8885435
Application Number:	13770984
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Application Number:	14563797

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Application Number:	62075554
Application Number:	14570817
Application Number:	14589889
Application Number:	14589925
Application Number:	14591845
Application Number:	14449095
Application Number:	12842190

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NAME OF SUBMITTER:	URMILA KARANDIKAR
SIGNATURE:	/Urmila Karandikar/
DATE SIGNED:	05/21/2019
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 97

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RELEASE OF A SECURITY INTEREST -- PATENTS

May 17, 2019

WHEREAS, pursuant to that certain (i) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035222, Frame 0866, (ii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035308, Frame 0428, (iii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035223, Frame 0001, (iv) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035226, Frame 0289, (v) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035223, Frame 0387, (vi) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035226, Frame 0147, (vii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035220, Frame 0048, (viii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035220, Frame 0226, (ix) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035309, Frame 0142, (x) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035308, Frame 0345, (xi) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035225, Frame 0839 and (xii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035225, Frame 0352, LATTICE SEMICONDUCTOR CORPORATION, SILICON IMAGE, INC., SIBEAM, INC. and DVDO, INC., each a Delaware corporation (each, a "Releasee"), granted to JEFFERIES FINANCE LLC, as collateral agent for the ratable benefit of the Secured Creditors (the "Releasor"), a continuing security interest in all right, title and interest of the Releasees in, to and under United States Patents listed on the attached Schedule A (the "Patents"), and all Proceeds in respect thereof (with all of the Releasee's rights listed above being collectively referred to as the "Collateral") to secure the payment, performance and observance of the Obligations;

WHEREAS, the Releasees have satisfied their Obligations; and

WHEREAS, the Releasee has requested and the Releasor has agreed to provide a document suitable for recording in the United States Patent and Trademark Office evidencing and effecting the release, relinquishment and discharge of its security interest in the Collateral.

NOW, THEREFORE, in consideration of and in exchange for good and valuable consideration, the Releasor hereby agrees as follows:

1. Defined Terms. All capitalized terms used but not otherwise defined herein have the meanings given to them in the Grants of Security Interests in United States Patents.

2. Release of Security Interest. The Releasor hereby, without any representation and warranty and without any recourse to the Releasor, releases, relinquishes and discharges all of its security interest in the Collateral.

[Signature Page Follows]

IN WITNESS WHEREOF, the undersigned has executed and delivered this Release as of the date first written above.

JEFFERIES FINANCE LLC,
as Collateral Agent and Releasor

By: _____
Name: Paul Chisholm
Title: Managing Director

[Signature Page to Release of Patent Security Interest]

SCHEDULE A

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/396,994	5574678	United States	Continuous Time Programmable Analog Block Architecture	Issued	Lattice Semiconductor Corporation
08/403,359	5510738	United States	CMOS Programmable Resistor-Based Transconductor	Issued	Lattice Semiconductor Corporation
08/403,354	5493205	United States	Low Distortion Differential Transconductor Output Current Mirror	Issued	Lattice Semiconductor Corporation
08/403,352	5617064	United States	Active Resistor For Stability Compensation [of Transconductor & Op-Amp Based Gain & Filter Stages]	Issued	Lattice Semiconductor Corporation
08/403,595	5670907	United States	VBB Reference for Pumped Substrates	Issued	Lattice Semiconductor Corporation
08/423,303	5490074	United States	Constant delay interconnect for coupling configurable logic blocks	Issued	Lattice Semiconductor Corporation
08/427,117	5596524	United States	CMOS memory cell with gate oxide of both NMOS and PMOS transistors as tunneling window for program and erase	Issued	Lattice Semiconductor Corporation
08/444,306	5491433	United States	Cascode array cell partitioning for a sense amplifier of a programmable logic device	Issued	Lattice Semiconductor Corporation
08/449,384	5756367	United States	Method of making a spacer based antifuse structure for low capacitance and high reliability	Issued	Lattice Semiconductor Corporation
08/447,991	5594687	United States	Completely complementary MOS memory cell with tunneling through the NMOS and PMOS transistors during program and erase	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/453,184	5570046	United States	Lead frame with noisy and quiet Vss and Vdd leads	Issued	Lattice Semiconductor Corporation
08/453,479	5583451	United States	Polarity control circuit which may be used with a ground bounce limiting buffer	Issued	Lattice Semiconductor Corporation
08/456,946	5621650	United States	Programmable gate array with improved interconnect structure, input/output structure and configurable logic block	Issued	Lattice Semiconductor Corporation
08/459,960	5521529	United States	Very high-density complex programmable logic device with a multi-tiered hierarchical switch matrix and optimized flexible logic allocation	Issued	Lattice Semiconductor Corporation
08/459,230	5818254	United States	Multi-tiered hierarchical high speed switch matrix structure for very high-density complex programmable logic devices	Issued	Lattice Semiconductor Corporation
08/459,234	5781030	United States	Programmable uniform symmetrical distribution logic allocator for a high-density complex PLD	Issued	Lattice Semiconductor Corporation
08/459,786	5638018	United States	P-type flip flop	Issued	Lattice Semiconductor Corporation
08/458,865	5589782	United States	Macrocell and clock signal allocation circuit for a programmable logic device (PLD) enabling PLD resources to provide multiple functions	Issued	Lattice Semiconductor Corporation
08/459,570	6531890	United States	Programmable optimized-distribution logic allocator for a high-density complex PLD	Issued	Lattice Semiconductor Corporation
08/461,196	5586044	United States	Array of configurable logic blocks including cascadable lookup tables	Issued	Lattice Semiconductor Corporation
08/462,934	5469368	United States	Array of configurable logic blocks each including a first	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			lookup table coupled to selectively replace an output of second lookup with an alternate function output		Corporation
08/486,178	5764078	United States	Family of multiple segmented programmable logic blocks interconnected by a high speed centralized switch matrix	Issued	Lattice Semiconductor Corporation
08/474,629	5612631	United States	An I/O macrocell for a programmable logic device	Issued	Lattice Semiconductor Corporation
08/479,872	5869981	United States	A High density programmable logic device	Issued	Lattice Semiconductor Corporation
08/486,174	5594365	United States	Architecture of a multiple array high density programmable logic device with a plurality of programmable switch matrices	Issued	Lattice Semiconductor Corporation
08/474,635	5811986	United States	Flexible synchronous/asynchronous cell structure for a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/466,438	5754471	United States	Reference for CMOS memory cell having PMOS and NMOS transistors with a common floating gate	Issued	Lattice Semiconductor Corporation
08/466,438	5754471	United States	Low power CMOS array for a PLD with program and erase using controlled avalanche injection	Issued	Lattice Semiconductor Corporation
08/473,620	5594657	United States	Field Programmable Gate Array Using Look-Up Tables, Multiplexers and Decoders	Issued	Lattice Semiconductor Corporation
08/483,623	5617042	United States	Multiple array programmable logic device with a plurality of programmable switch matrices	Issued	Lattice Semiconductor Corporation
08/492,604	5526278	United States	System for Synthesizing Field Programmable Gate Array	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 39

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Implementations From High Level Circuit Descriptions		Corporation
08/493,640	5679599	United States	Isolation using self-aligned trench formation and conventional LOCOS	Issued	Lattice Semiconductor Corporation
08/494,271	5565794	United States	Voltage range tolerant CMOS output buffer with reduced input capacitance	Issued	Lattice Semiconductor Corporation
08/497,992	5742542	United States	Nonvolatile memory cells using only positive charge to store data	Issued	Lattice Semiconductor Corporation
08/500,295	5700698	United States	Method for screening non-volatile memory and programmable logic devices	Issued	Lattice Semiconductor Corporation
08/501,230	5604370	United States	Field Implant For Semiconductor Device	Issued	Lattice Semiconductor Corporation
08/505,837	5635855	United States	Method for Simultaneous Programming of In-System Programmable Integrated Circuits	Issued	Lattice Semiconductor Corporation
08/507,893	5570039	United States	Method and Apparatus for Converting Field-Programmable Gate Array Implementations Into Mask-Programmable Logic Cell Implementations	Issued	Lattice Semiconductor Corporation
08/507,957	5559450	United States	Programmable Function Unit As Parallel Multiplier Cell	Issued	Lattice Semiconductor Corporation
08/528,030	5581126	United States	Interlaced layout configuration for differential pairs of interconnect lines	Issued	Lattice Semiconductor Corporation
08/535,362	5528170	United States	Low-Skew Signal Routing In A Programmable Array	Issued	Lattice Semiconductor Corporation
08/551,974	5615150	United States	control gate-addressed cmos non-volatile cell that programs through gates of CMOS transistors	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 40

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/554,092	5587945	United States	CMOS EEPROM cell with tunneling window in the read path	Issued	Lattice Semiconductor Corporation
08/560,038	5666309	United States	Memory cell for a programmable logic device (PLD) avoiding pumping programming voltage above an NMOS threshold	Issued	Lattice Semiconductor Corporation
08/560,933	5587921	United States	Array of configurable logic blocks each including a lookup table having inputs coupled to a first multiplexer and having outputs to a second multiplexer	Issued	Lattice Semiconductor Corporation
08/561,306	5672521	United States	Method of forming multiple gate oxide thicknesses on a wafer substrate	Issued	Lattice Semiconductor Corporation
08/573,622	5809522	United States	Microprocessor system with process identification tag entries to reduce cache flushing after a context switch	Issued	Lattice Semiconductor Corporation
08/574,776	5739713	United States	Deconvolution input buffer compensating for capacitance of a switch matrix of a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/575,898	5736888	United States	Capacitance elimination circuit	Issued	Lattice Semiconductor Corporation
08/575,852	5719516	United States	Clock generator circuit for use with a dual edge register that provides a separate enable for each edge over an input clock signal	Issued	Lattice Semiconductor Corporation
08/596,679	5598346	United States	Array of configurable logic blocks including network means for broadcasting clock signals to different pluralities of logic blocks	Issued	Lattice Semiconductor Corporation
08/606,702	5623217	United States	Field Programmable Gate Array With Write-Port Enabled Memory	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 41

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/614,728	5926841	United States	Segment descriptor cache for a processor	Issued	Lattice Semiconductor Corporation
08/625,403	5646901	United States	CMOS memory cell with tunneling during program and erase through the NMOS and PMOS transistors and a pass gate separating the NMOS and PMOS transistors	Issued	Lattice Semiconductor Corporation
08/632,811	5751163	United States	Parallel Programming of ISP Devices Using An Automatic Tester	Issued	Lattice Semiconductor Corporation
08/635,184	5666087	United States	Active Resistor For Stability Compensation [of Transconductor & Op-Amp Based Gain & Filter Stages]	Issued	Lattice Semiconductor Corporation
08/643,807	5748525	United States	Array cell circuit with split read/write line	Issued	Lattice Semiconductor Corporation
08/643,291	5864486	United States	Method And Apparatus For In-System Programming of A Programmable Logic Device Using a Two-Wire Interface	Issued	Lattice Semiconductor Corporation
08/653,186	5789939	United States	Very high-density complex programmable logic device with a multi-tiered hierarchical switch matrix and optimized flexible logic allocation	Issued	Lattice Semiconductor Corporation
08/659,279	5723984	United States	Field programmable gate array (FPGA) with interconnect encoding	Issued	Lattice Semiconductor Corporation
08/659,941	5808942	United States	Field programmable gate array (FPGA) having an improved configuration memory and look up table	Issued	Lattice Semiconductor Corporation
08/664,190	5830795	United States	Simplified masking process for programmable logic device manufacture	Issued	Lattice Semiconductor Corporation
08/666,193	5760609	United States	Clock signal providing circuit with enable and a pulse generator with enable for use	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 42

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			in a block clock circuit of a programmable logic device		
08/668,141	5796295	United States	Reference for CMOS memory cell having PMOS and NMOS transistors with a common floating gate	Issued	Lattice Semiconductor Corporation
08/668,896	5751164	United States	Programmable logic device with multi-level power control	Issued	Lattice Semiconductor Corporation
08/683,685	5734275	United States	Programmable logic device having a sense amplifier with virtual ground	Issued	Lattice Semiconductor Corporation
08/683,373	5818294	United States	Temperature insensitive current source	Issued	Lattice Semiconductor Corporation
08/690,768	5801551	United States	Depletion mode pass gates with controlling decoder and negative power supply for a programmable logic device	Issued	Lattice Semiconductor Corporation
08/689,523	5942780	United States	An integrated circuit having, and process providing, different oxide layer thicknesses on a substrate	Issued	Lattice Semiconductor Corporation
08/696,444	5796750	United States	Method for Programming a PLD In An Automatic Tester	Issued	Lattice Semiconductor Corporation
08/700,616	5740069	United States	Logic device (PLD) having direct connections between configurable logic blocks (CLBs) and configurable input/output blocks (IOBs)	Issued	Lattice Semiconductor Corporation
08/699,401	5960274	United States	Oxide formation process for manufacturing programmable logic device	Issued	Lattice Semiconductor Corporation
08/702,846	5959336	United States	Decoder circuit with short channel depletion transistors	Issued	Lattice Semiconductor Corporation
08/710,445	5862365	United States	Configuration Pin Emulation Circuit For a Field Programmable Array	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 43

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/723,082	5760605	United States	Programmable high speed routing switch	Issued	Lattice Semiconductor Corporation
08/726,512	5761116	United States	Vpp only scalable EEPROM memory cell having transistors with thin tunnel gate oxide	Issued	Lattice Semiconductor Corporation
08/729,117	5991907	United States	Method for Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/734,888	5805607	United States	Method for user-controlled I/O switching during in-circuit programming of CPLDs through the IEEE 1149.1 test access port	Issued	Lattice Semiconductor Corporation
08/740,948	5811987	United States	Block clock and initialization circuit for a complex high density PLD	Issued	Lattice Semiconductor Corporation
08/748,041	5892962	United States	FPGA-based Processor	Issued	Lattice Semiconductor Corporation
08/745,410	5717342	United States	Output buffer incorporating shared intermediate nodes	Issued	Lattice Semiconductor Corporation
08/781,882	6028993	United States	Timed Circuit Simulation In Hardware Using FPGAs	Issued	Lattice Semiconductor Corporation
08/785,096	5841701	United States	Method of charging and discharging floating gage transistors to reduce leakage current	Issued	Lattice Semiconductor Corporation
08/799,153	5904575	United States	Method and apparatus incorporating nitrogen selectively for differential oxide growth	Issued	Lattice Semiconductor Corporation
08/799,235	5885904	United States	Method to incorporate, and a device having, oxide enhancement dopants using gas immersion laser doping (GILD) for selectively growing an oxide layer	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/823,953	6190966	United States	Process for fabricating semiconductor memory device with high data retention including silicon nitride etch stop layer formed at high temperature with low hydrogen ion	Issued	Lattice Semiconductor Corporation
08/828,520	5905385	United States	Memory bits used to couple look up table inputs to facilitate increased availability to routing resources particularly for variable sized look up tables for a field programmable gate array (FPGA)	Issued	Lattice Semiconductor Corporation
08/831,372	5844912	United States	Fast verify for CMOS memory cell	Issued	Lattice Semiconductor Corporation
08/827,671	5835405	United States	Application Specific Modules in a Programmable Logic Device	Issued	Lattice Semiconductor Corporation
08/843,150	6087275	United States	Reduction of n-channel parasitic transistor leakage by using low power/low pressure phosphosilicate glass	Issued	Lattice Semiconductor Corporation
08/838,487	6034541	United States	In-System Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
08/856,926	5949279	United States	Devices for sourcing constant supply current from power supply in system with integrated circuit having variable supply current requirement	Issued	Lattice Semiconductor Corporation
08/859,761	5989957	United States	Process for fabricating semiconductor memory device with high data retention including silicon nitride etch stop layer formed at high temperature with low hydrogen ion concentration	Issued	Lattice Semiconductor Corporation
08/871,589	5978272	United States	Nonvolatile memory structure for programmable logic devices	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 45

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/899,428	6028447	United States	FPGA Having Predictable Open-Drain Drive Mode	Issued	Lattice Semiconductor Corporation
08/912,763	6072351	United States	Output buffer for making a high voltage (5.0 volt) compatible input/output in a low voltage (2.5 volt) semiconductor process	Issued	Lattice Semiconductor Corporation
08/931,798	6359466	United States	Circuitry to provide fast carry	Issued	Lattice Semiconductor Corporation
08/938,550	6020755	United States	Hybrid Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/948,306	6097212	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/947,888	5854114	United States	Data retention of EEPROM cell with shallow trench isolation using thicker liner oxide	Issued	Lattice Semiconductor Corporation
08/949,992	6028463	United States	Programmable Clock Manager For A Programmable Logic Device that Can Generate At Least Two Different Output Clocks	Issued	Lattice Semiconductor Corporation
08/950,444	6216191	United States	Field Programmable Gate Array Having A Dedicated Processor Interface	Issued	Lattice Semiconductor Corporation
08/950,446	5986471	United States	Bi-directional Buffers and Supplemental Logic and Interconnect Cells for Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
08/950,448	6060902	United States	A Programmable Clock Manager For A Programmable Logic Device that Can Be Programmed Without Reconfiguring the Device	Issued	Lattice Semiconductor Corporation
08/950,624	6049224	United States	Programmable Logic Device With Logic Cells Having A Flexible Input Structure	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 46

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/951,128	6043677	United States	Programmable Clock Manager For A Programmable Logic Device that Can Implement Delay-Locked Loop Functions	Issued	Lattice Semiconductor Corporation
08/964,421	6389321	United States	Simultaneous Wired and Wireless Remote In-System Programming of Multiple Remote Systems	Issued	Lattice Semiconductor Corporation
08/974,799	6003150	United States	Method for Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/996,361	6275064	United States	Symmetrical, extended and fast direct connections between variable grain blocks in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/996,049	6127843	United States	Dual port SRAM memory for run time use in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,615	6034544	United States	Programmable input/output block (IOB) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,614	5982193	United States	Input/output block (IOB) connections to MAXL lines, NOR lines and dendrites in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,612	5990702	United States	Flexible direct connections between input/output blocks (IOBs) and variable grain blocks (VBGs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/997,221	6107823	United States	Programmable control multiplexing for input/output blocks (IOBs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/996,119	5986480	United States	Multiple input zero power and/nor gate for use in a field programmable gate array (FPGA)	Issued	Lattice Semiconductor Corporation
08/996,530	6134703	United States	A Process for Programming PLDs and Embedded Non-Volatile Memories	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 47

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/998,978	6102963	United States	Electrically erasable and reprogrammable, nonvolatile integrated storage device with in-system programming and verification (ISPAV) capabilities for supporting in-system reconfiguring of PLD's	Issued	Lattice Semiconductor Corporation
09/008,762	6130551	United States	Synthesis-friendly FPGA architecture with variable length and variable timing interconnect	Issued	Lattice Semiconductor Corporation
09/010,000	6034538	United States	Virtual Logic System For Reconfigurable Hardware	Issued	Lattice Semiconductor Corporation
09/023,669	6025637	United States	Spacer based antifuse structure for low capacitance and high reliability and method of fabrication thereof	Issued	Lattice Semiconductor Corporation
09/023,506	6023570	United States	Sequential and Simultaneous Manufacturing Programming of Multiple In-System Programmable Systems Through a Data Network	Issued	Lattice Semiconductor Corporation
09/026,814	6093946	United States	EEPROM cell with field-edgeless tunnel window using shallow trench isolation process	Issued	Lattice Semiconductor Corporation
09/037,095	6128770	United States	Configurable logic array including IOB to longlines interconnect means for providing selectable access to plural longlines from each IOB (input/output block)	Issued	Lattice Semiconductor Corporation
09/045,128	6064225	United States	Global Signal Distribution With Reduced Routing Tracks In An FPGA	Issued	Lattice Semiconductor Corporation
09/046,404	5982683	United States	Enhanced method of testing semiconductor devices having nonvolatile elements	Issued	Lattice Semiconductor Corporation
09/053,251	6556154	United States	Offset Voltage Calibration DAC With Reduced Sensitivity To Mismatch	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 48

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Errors		
09/059,552	6108806	United States	Method of Testing and Diagnosing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/067,320	6154050	United States	Internal tristate bus with arbitration logic	Issued	Lattice Semiconductor Corporation
09/067,318	6104207	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/069,035	6133750	United States	Combination of global clock and localized clocks	Issued	Lattice Semiconductor Corporation
09/069,768	6002610	United States	Non-Volatile Memory Element For Programmable Logic Applications and Operational Methods Therefor	Issued	Lattice Semiconductor Corporation
09/080,906	6225821	United States	Package migration for related programmable logic devices	Issued	Lattice Semiconductor Corporation
09/083,335	6304099	United States	Method and structure for dynamic in-system programming	Issued	Lattice Semiconductor Corporation
09/083,336	6066977	United States	Programmable Output Voltage Levels	Issued	Lattice Semiconductor Corporation
09/083,205	6255847	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/086,437	6087696	United States	Stacked tunneling dielectric technology for improving data retention of EEPROM cell	Issued	Lattice Semiconductor Corporation
09/109,123	6202182	United States	Method and Apparatus For Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/114,385	6028758	United States	Electrostatic discharge (ESD) protection for a 5.0 volt compatible input/output (I/O) in a 2.5 volt semiconductor process	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 49

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/114,717	6091595	United States	Electrostatic discharge (ESD) protection for NMOS pull up transistors of a 5.0 volt compatible output buffer using 2.5 volt process transistors	Issued	Lattice Semiconductor Corporation
09/114,718	6043969	United States	Ballast resistors with parallel stacked NMOS transistors used to prevent secondary breakdown during ESD with 2.5 volt process transistors	Issued	Lattice Semiconductor Corporation
09/115,683	6124732	United States	Signaling Voltage Range Discriminator	Issued	Lattice Semiconductor Corporation
09/118,200	6028446	United States	Flexible Synchronous and Asynchronus Circuits for A Very High Density Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/134,174	6064105	United States	Data retention of EEPROM cell with shallow trench isolation using thicker liner oxide	Issued	Lattice Semiconductor Corporation
09/145,793	6087854	United States	High Speed Line Driver With Direct and Complementary Outputs	Issued	Lattice Semiconductor Corporation
09/169,848	6347387	United States	Test Circuits For Multiple FPGA Systems	Issued	Lattice Semiconductor Corporation
09/169,492	6424003	United States	EEPROM cell with self-aligned tunneling window	Issued	Lattice Semiconductor Corporation
09/187,691	6228696	United States	Semiconductor-oxide-semiconductor capacitor formed in integrated circuit	Issued	Lattice Semiconductor Corporation
09/187,689	6154051	United States	Tileable and compact layout for super variable grain blocks within FPGA device	Issued	Lattice Semiconductor Corporation
09/186,917	6229336	United States	Programmable integrated circuit device with slew control and skew control	Issued	Lattice Semiconductor Corporation
09/188,778	6169432	United States	High voltage switch for	Issued	Lattice

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			providing voltages higher than 2.5 volts with transistors made using a 2.5 volt process		Semiconductor Corporation
09/192,094	6291327	United States	Optimization of S/D annealing to minimize random S/D shorts in memory array	Issued	Lattice Semiconductor Corporation
09/192,096	6221733	United States	Reduction of mechanical stress in shallow trench isolation process	Issued	Lattice Semiconductor Corporation
09/196,449	6191612	United States	Enhanced I/O control flexibility for generating control signals	Issued	Lattice Semiconductor Corporation
09/196,080	5912550	United States	Power converter with 2.5 semiconductor process components	Issued	Lattice Semiconductor Corporation
09/198,796	6218857	United States	Variable sized line driving amplifiers for input/output blocks (IOBs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/200,395	6261944	United States	Semiconductor device having high reliability passivation and fabrication method	Issued	Lattice Semiconductor Corporation
09/198,653	6009033	United States	Method of programming and erasing an EEPROM device under an elevated temperature and apparatus thereof	Issued	Lattice Semiconductor Corporation
09/199,664	6353352	United States	Clock tree topology	Issued	Lattice Semiconductor Corporation
09/201,081	6133769	United States	Phase locked loop with a lock detector	Issued	Lattice Semiconductor Corporation
09/203,149	6404006	United States	EEPROM cell with tunneling across entire separated channels	Issued	Lattice Semiconductor Corporation
09/217,647	5969992	United States	EEPROM cell using p-well for	Issued	Lattice Semiconductor Corporation
09/207,558	6175266	United States	Operational amplifier with CMOS transistors made using	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 51

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			2.5 volt process transistors		Corporation
09/208,203	6163168	United States	Efficient interconnect network for use in FPGA device having variable grain architecture	Issued	Lattice Semiconductor Corporation
09/212,022	6124730	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/212,330	6100715	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/212,331	6081473	United States	FPGA integrated circuit having embedded SRAM memory blocks each with statically and dynamically controllable read mode	Issued	Lattice Semiconductor Corporation
09/216,662	6204686	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	Issued	Lattice Semiconductor Corporation
09/216,051	6214666	United States	Method of forming a non-volatile memory device	Issued	Lattice Semiconductor Corporation
09/217,648	6232631	United States	Floating gate memory cell structure with programming mechanism outside the read path	Issued	Lattice Semiconductor Corporation
09/217,646	6282123	United States	Method of fabricating, programming, and erasing a dual pocket two sided program/erase non-volatile memory cell	Issued	Lattice Semiconductor Corporation
09/218,987	6294810	United States	EEPROM cell with tunneling at separate edge and channel regions	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/220,469	6157568	United States	Avalanche programmed floating gate memory cell structure with program element in first polysilicon layer	Issued	Lattice Semiconductor Corporation
09/221,360	6294809	United States	Avalanche programmed floating gate memory cell structure with program element in polysilicon	Issued	Lattice Semiconductor Corporation
09/226,702	6215700	United States	PMOS avalanche programmed floating gate memory cell structure	Issued	Lattice Semiconductor Corporation
09/227,981	6197638	United States	Oxide formation process for manufacturing programmable logic device	Issued	Lattice Semiconductor Corporation
09/235,356	6097664	United States	Multi-port SRAM cell array having plural write paths including for writing through addressable port and through serial boundary scan	Issued	Lattice Semiconductor Corporation
09/235,351	6181163	United States	FPGA integrated circuit having embedded SRAM memory blocks and interconnect channel for broadcasting address and control	Issued	Lattice Semiconductor Corporation
09/235,615	6211695	United States	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	Issued	Lattice Semiconductor Corporation
09/239,072	5999449	United States	Two transistor EEPROM cell using P-well for tunneling across a channel	Issued	Lattice Semiconductor Corporation
09/240,560	6297128	United States	Process for manufacturing shallow trenches filled with dielectric material having low mechanical stress	Issued	Lattice Semiconductor Corporation
09/245,813	6294811	United States	Two transistor EEPROM cell	Issued	Lattice Semiconductor Corporation
09/255,410	6075724	United States	Method for sorting	Issued	Lattice

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			semiconductor devices having a plurality of non-volatile memory cells		Semiconductor Corporation
09/255,053	6255169	United States	Process for fabricating a high-endurance non-volatile memory device	Issued	Lattice Semiconductor Corporation
09/256,245	6133164	United States	Fabrication of oxide regions having multiple thicknesses using minimized number of thermal cycles	Issued	Lattice Semiconductor Corporation
09/261,776	6256758	United States	Fault Tolerance Operation of Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/263412	6075293	United States	Semiconductor device having a multi-layer metal interconnect structure	Issued	Lattice Semiconductor Corporation
09/268,897	6207989	United States	Non-volatile memory device having a high-reliability composite insulation layer	Issued	Lattice Semiconductor Corporation
09/276,991	6031365	United States	Band gap reference using a low voltage power supply	Issued	Lattice Semiconductor Corporation
09/276,990	6163175	United States	High voltage detector to control a power supply voltage pump for a 2.5 volt semiconductor process device	Issued	Lattice Semiconductor Corporation
09/277,441	6326663	United States	Avalanche injection EEPROM memory cell with p-type control gate	Issued	Lattice Semiconductor Corporation
09/280,887	6172392	United States	Boron doped silicon capacitor plate	Issued	Lattice Semiconductor Corporation
09/286,830	6284626	United States	Angled nitrogen ion implantation for minimizing mechanical stress on side walls of an isolation trench	Issued	Lattice Semiconductor Corporation
09/288,062	6265900	United States	High Speed Logical OR Circuit	Issued	Lattice Semiconductor Corporation
09/287,976	6413826	United States	Gate insulator process for	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 54

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			nanometer MOSFETs		Corporation
09/310,071	6424000	United States	Floating gate memory apparatus and method for selected programming thereof	Issued	Lattice Semiconductor Corporation
09/316,241	6274898	United States	Triple-well EEPROM cell using p-well for tunneling across a channel	Issued	Lattice Semiconductor Corporation
09/318,570	6552595	United States	High Voltage Discharge Scheme	Issued	Lattice Semiconductor Corporation
09/320389	6118693	United States	Electrically erasable non-volatile memory cell with integrated SRAM to reduce testing time	Issued	Lattice Semiconductor Corporation
09/320,392	6067252	United States	Electrically erasable non-volatile memory cell with no static power dissipation	Issued	Lattice Semiconductor Corporation
09/326,940	6184713	United States	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	Issued	Lattice Semiconductor Corporation
09/326,140	6150841	United States	Enhanced storage macrocell module for high density CPLD architectures	Issued	Lattice Semiconductor Corporation
09/330,753	6628660	United States	Finite State Machine with Associated Memory	Issued	Lattice Semiconductor Corporation
09/334,051	6028789	United States	Zero-power CMOS non-volatile memory cell having an avalanche injection element	Issued	Lattice Semiconductor Corporation
09/334,052	6034893	United States	Non-volatile memory cell having dual avalanche injection elements	Issued	Lattice Semiconductor Corporation
09/400,029	6404226	United States	Integrated Circuit With Standard Cell Logic and Spare Gates	Issued	Lattice Semiconductor Corporation
09/405,958	6550030	United States	On-Line Testing of the Programmable Logic Blocks In Field Programmable Gate	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Arrays		
09/406,219	6574761	United States	On-Line Testing of the Programmable Interconnect Network In Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/433,642	6191609	United States	Combination of global clock and localized clocks	Issued	Lattice Semiconductor Corporation
09/440,460	6294925	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/440,207	6278311	United States	Method for minimizing instantaneous currents when driving bus signals	Issued	Lattice Semiconductor Corporation
09/441,220	6208559	United States	Method of operating EEPROM memory cells having transistors with thin gate oxide and reduced disturb	Issued	Lattice Semiconductor Corporation
09/452,017	6137738	United States	Method For In-System Programming of Serially Configured EEPROMS Using a JTAG Interface of an FPGA	Issued	Lattice Semiconductor Corporation
09/454,322	6326808	United States	Inversion of Product Term Line Before or Logic in a Programmable Logic Device (PLD)	Issued	Lattice Semiconductor Corporation
09/472,645	6150842	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/506,180	6362684	United States	Amplifier Having an Adjustable Resistor Network	Issued	Lattice Semiconductor Corporation
09/507,580	6424209	United States	Integrated Programmable Continuous Time Filter with Programmable Capacitor Arrays	Issued	Lattice Semiconductor Corporation
09/548,171	6351157	United States	Output buffer for making a high voltage (5.0 volt) compatible input/output in a low voltage (2.5 volt)	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 56

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			semiconductor process		
09/567,898	6288937	United States	Decoded Generic Routing Pool	Issued	Lattice Semiconductor Corporation
09/578,086	6570212	United States	Complementary avalanche injection EEPROM cell	Issued	Lattice Semiconductor Corporation
09/603,119	6292930	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/603,807	6216257	United States	FPGA device and method that includes a variable grain function architecture for implementing configuration logic blocks and a complimentary variable length interconnect architecture for providing configurable routing between configuration logic blocks	Issued	Lattice Semiconductor Corporation
09/611,449	6530049	United States	On-line Fault Tolerant Operation Via Incremental Reconfiguration of Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/626,094	6380759	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/632,319	6567969	United States	Configurable Logic Array Including Lookup Table Means For Generating Functions of Different Numbers Of Input Terms	Issued	Lattice Semiconductor Corporation
09/643,279	6627947	United States	Compact single-poly two-transistor EEPROM cell	Issued	Lattice Semiconductor Corporation
09/651,689	6433602	United States	High speed schmitt trigger with low supply voltage	Issued	Lattice Semiconductor Corporation
09/660,707	6370071	United States	High Voltage CMOS switch	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 57

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
09/661,585	6462576	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/668,896	6701340	United States	Double Differential Comparator and Programmable Analog Block Architecture Using Same	Issued	Lattice Semiconductor Corporation
09/669,186	6249144	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/671,853	6631487	United States	On-Line Testing of Field Programmable Gate Array Resources	Issued	Lattice Semiconductor Corporation
09/692,694	6470485	United States	Scalable and parallel processing methods and structures for testing configurable interconnect network in FPGA device	Issued	Lattice Semiconductor Corporation
09/704,487	6507212	United States	Wide input programmable logic system and method	Issued	Lattice Semiconductor Corporation
09/651,805	6455912	United States	Process for manufacturing shallow trenches filled with dielectric material having low mechanical stress	Issued	Lattice Semiconductor Corporation
09/712,000	6356107	United States	Method and structure for dynamic in-system programming	Issued	Lattice Semiconductor Corporation
09/721,153	6348813	United States	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	Issued	Lattice Semiconductor Corporation
09/732,216	6735706	United States	Programmable power management system and method	Issued	Lattice Semiconductor Corporation
09/731,184	6524911	United States	Combination of BPTEOS oxide film with CMP and RTA to achieve good data	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 58

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			retention		
09/731,185	6287916	United States	Method for forming a semiconductor device using LPCVD nitride to protect floating gate from charge loss	Issued	Lattice Semiconductor Corporation
09/733,878	6526558	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	Issued	Lattice Semiconductor Corporation
09/775,488	6462602	United States	Voltage Level Translator Systems And Methods	Issued	Lattice Semiconductor Corporation
09/775,489	6414521	United States	Improved sense amplifier systems and methods	Issued	Lattice Semiconductor Corporation
09/818,257	6496969	United States	Programming Programmable Logic Devices Using Hidden Switches	Issued	Lattice Semiconductor Corporation
09/841,209	6590415	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/863,656	6535043	United States	Clock Signal Selection System, Method of Generating A Clock Signal And Programmable Clock Manager Including Same	Issued	Lattice Semiconductor Corporation
09/864,276	6486705	United States	Signal Distribution Scheme In Field Programmable Gate Array (FPGA) or Field Programmable Systems Chip (FPSC) Including Cycle Stealing Units	Issued	Lattice Semiconductor Corporation
09/864,284	6472904	United States	Double Data Rate Input And Output In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/864,289	6480026	United States	Multi-functional I/O Buffers In a Field Programmable Gate	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 59

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Array (FPGA)		Corporation
09/864,277	6483342	United States	Multi-Master Multi-Slave Bus In Field Programmable Gate Array (FPGA)	Issued	Lattice Semiconductor Corporation
09/864,290	6772230	United States	Field Programmable Gate Array (FPGA) Bit Stream Format	Issued	Lattice Semiconductor Corporation
09/870,877	6498538	United States	Low Jitter Integrated Phase Locked Loop With Broad Tuning Range	Issued	Lattice Semiconductor Corporation
09/870,541	6455375	United States	EEPROM tunnel window for program injection via P+ contacted inversion	Issued	Lattice Semiconductor Corporation
09/881,950	6614291	United States	Low Voltage, High Speed CMOS CML Latch and MUX Devices	Issued	Lattice Semiconductor Corporation
09/885,243	6429692	United States	High Speed Data Sampling With Reduced Metastability	Issued	Lattice Semiconductor Corporation
09/927,289	6492877	United States	Improved Coupling For LC-Based VCO	Issued	Lattice Semiconductor Corporation
09/927,612	6525617	United States	Buffering For LC-Based Stage	Issued	Lattice Semiconductor Corporation
09/927,793	6653860	United States	Enhanced logic macrocell with expanded PT (product term) sharing capability for Use in High Density CPLD Architectures	Issued	Lattice Semiconductor Corporation
09/941,454	6489835	United States	Low Voltage Bandgap Reference Circuit	Issued	Lattice Semiconductor Corporation
09/949,112	6593222	United States	Method to improve the reliability of thermosonic gold to aluminum wire bonds	Issued	Lattice Semiconductor Corporation
09/966,967	6832231	United States	Multiple Width Random Number Generation	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 60

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/011,549	6693830	United States	Single Poly Two-Transistor EEPROM Cell With Differentially Doped Floating Gate	Issued	Lattice Semiconductor Corporation
10/053,004	6989551	United States	Test structure for determining the minimum tunnel opening size in a non-volatile memory cell	Issued	Lattice Semiconductor Corporation
10/010,011	6515899	United States	Non-Volatile Memory Cell With Enhanced Cell Drive Current	Issued	Lattice Semiconductor Corporation
09/991,245	6611463	United States	Zero Power Programmable Memory Cell	Issued	Lattice Semiconductor Corporation
09/992,493	6489806	United States	Zero power logic cell for use in programmable logic devices	Issued	Lattice Semiconductor Corporation
10/006,559	7003066	United States	Digital Phase locked Loop with Phase Selector having Minimized Number of Phase Interpolators	Issued	Lattice Semiconductor Corporation
10/006,610	6999543	United States	Clock Data Recovery Deserializer With Programmable Sync Detect Logic	Issued	Lattice Semiconductor Corporation
10/006,516	6993108	United States	Digital Phase Locked Loop With Programmable Digital Filter	Issued	Lattice Semiconductor Corporation
10/021,873	6661254	United States	Programmable Interconnect Circuit With A Phase-Locked Loop	Issued	Lattice Semiconductor Corporation
10/017,725	6674303	United States	Programmable I/O cell with bidirectional and shift register capabilities	Issued	Lattice Semiconductor Corporation
10/017,859	6605959	United States	Structure and Method for Implementing Wide Multiplexers	Issued	Lattice Semiconductor Corporation
10/022,464	7154298	United States	Block oriented architecture for programmable interconnect circuit	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 61

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/021,844	6703860	United States	I/O Block for Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/023,053	6653861	United States	Multi-level Routing Structure for a Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/023,226	6650141	United States	High Speed Interface For a Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/059,624	6636442	United States	Non-volatile memory element having a cascoded transistor scheme to reduce oxide field stress	Issued	Lattice Semiconductor Corporation
10/061,057	6845044	United States	Method of preventing high Icc at start-up in zero-power EEPROM cells for PLD applications	Issued	Lattice Semiconductor Corporation
10/066,031	6680625	United States	Symmetrical CML Logic Gate System	Issued	Lattice Semiconductor Corporation
10/082,050	6781170	United States	Integrated Circuit Base Transistor Structure And Associated Programmable Cell Library	Issued	Lattice Semiconductor Corporation
10/083,728	6600188	United States	An EEPROM with neutralized doping at tunnel window edge	Issued	Lattice Semiconductor Corporation
10/090,209	6621298	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
10/103,100	6795959	United States	Integrated Delay Discriminator For Use With a Field- Programmable Gate Array and A Method of Determining a Time Delay Thereof	Issued	Lattice Semiconductor Corporation
10/106,509	6907439	United States	FFT address generation method and apparatus	Issued	Lattice Semiconductor Corporation
10/108,401	6976047	United States	Skipped carry incrementer for FFT address generation	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 62

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/112,370	6639431	United States	Differential Input Comparator	Issued	Lattice Semiconductor Corporation
10/128,943	6660579	United States	Zero Power Memory Cell With Improved Data Retention	Issued	Lattice Semiconductor Corporation
10/131,883	7032162	United States	Polynomial Expander for Generating Coefficients of a Polynomial from Roots of the Polynomial	Issued	Lattice Semiconductor Corporation
10/133,016	6765408	United States	Device and Method with Generic Logic Blocks	Issued	Lattice Semiconductor Corporation
10/135,308	6814296	United States	Integrated Circuit and Associated Design Method With Antenna Error Control Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/135,325	6600341	United States	Integrated Circuit and Associated Design Method Using Spare Gate Islands	Issued	Lattice Semiconductor Corporation
10/146,739	6714048	United States	Input Buffer With Selectable PCL, GTL, or PECL Compatibility	Issued	Lattice Semiconductor Corporation
10/146,826	6657458	United States	Output Buffer With Feedback From An Input Buffer To Provide Selectable PCL, GTL, or PECL Compatability	Issued	Lattice Semiconductor Corporation
10/146,769	6870391	United States	Input Buffer With CMOS Driver Gate Current Control Enabling Selectable PCL, GTL, or PECL Compatibility	Issued	Lattice Semiconductor Corporation
10/147,199	6714043	United States	Output Buffer Having Programmable Drive Current And Output Voltage Limits	Issued	Lattice Semiconductor Corporation
10/146,734	6720755	United States	Band Gap Reference Circuit	Issued	Lattice Semiconductor Corporation
10/147,011	6760209	United States	Electrostatic Discharge Protection Circuit	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 63

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/151,753	6798244	United States	Output Buffer With Overvoltage Protection	Issued	Lattice Semiconductor Corporation
10/150,410	6848095	United States	Method of Assigning Logic Functions To Macrocells In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/159,009	6583652	United States	Highly linear programmable transconductor with large input-signal range	Issued	Lattice Semiconductor Corporation
10/159,089	6717451	United States	Precision analog level shifter with programmable options	Issued	Lattice Semiconductor Corporation
10/159,681	6806771	United States	Multimode output stage converting differential to single-ended signals using current-mode input signals	Issued	Lattice Semiconductor Corporation
10/162,337	6596587	United States	Shallow junction EEPROM Device and Process for Fabricating the Device	Issued	Lattice Semiconductor Corporation
10/160,855	6794236	United States	EEPROM Device with Improved Capacitive Coupling and Fabrication Process	Issued	Lattice Semiconductor Corporation
10/161,283	6716705	United States	EEPROM Device having a Retrograde Program Junction Region And Process for Fabrication the Device	Issued	Lattice Semiconductor Corporation
10/164,484	6703305	United States	Semiconductor Device Having Metallized Interconnect Structure And Method Of Fabricaton	Issued	Lattice Semiconductor Corporation
10/187,236	6844757	United States	Converting Bits to Vectors In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/191,888	6650143	United States	FPGA Based Upon Transistor gate Oxide Breakdown	Issued	Lattice Semiconductor Corporation
10/194,771	7028281	United States	FPGA With Register-Intensive Architecture	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 64

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/200,645	6714066	United States	Integrated Programmable Continuous Time Filter with Programmable Capacitor Arrays	Issued	Lattice Semiconductor Corporation
10/207,292	6683477	United States	Wide input programmable logic system and method	Issued	Lattice Semiconductor Corporation
10/210,367	6938197	United States	CRC Calculation System And Method For A Packet Arriving On An N-Byte Wide Bus	Issued	Lattice Semiconductor Corporation
10/211,125	6545313	United States	EEPROM tunnel window for program injection via P+ contacted inversion	Issued	Lattice Semiconductor Corporation
10/219,046	6650142	United States	Enhanced CPLD Macrocell Module Having Selectable Bypass of Steering-based Resource Allocation and Methods of Use	Issued	Lattice Semiconductor Corporation
10/233,021	7043511	United States	Performing Conditional Operations In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/232,912	6841447	United States	EEPROM Device Having An Isolation -Bounded Tunnel Capacitor And Fabrication Process	Issued	Lattice Semiconductor Corporation
10/235,380	6725442	United States	Scalable and parallel processing methods and structures for testing configurable interconnect network in FPGA device	Issued	Lattice Semiconductor Corporation
10/236,829	6842372	United States	EEPROM Cell Having Floating Gate Transistor Within a Cell Well And a Process For Fabricating the Memory Cell	Issued	Lattice Semiconductor Corporation
10/236,114	6833602	United States	Device Having Electrically Isolated Low Voltage And High Voltage Regions And Process For Fabricating the Device	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 65

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/236,718	6649514	United States	EEPROM Device Having Improved Data Retention And Process for Fabricating The Device	Issued	Lattice Semiconductor Corporation
10/242,809	6738306	United States	Multiport SRAM Cell	Issued	Lattice Semiconductor Corporation
10/243,014	6917536	United States	Memory access Circuit and Method for reading and writing data with the same clock signal	Issued	Lattice Semiconductor Corporation
10/251,608	6700154	United States	EEPROM cell with trench coupling capacitor	Issued	Lattice Semiconductor Corporation
10/255,474	6907592	United States	Method of Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,875	6809551	United States	Method of Optimizing Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,499	6803787	United States	State Machine In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,656	6812738	United States	Vector Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/263,251	6748575	United States	Programming Programmable Logic Devices Using Hidden Switches	Issued	Lattice Semiconductor Corporation
10/263,507	6846714	United States	Voltage Limted EEPROM Device And Process For Fabricating the Device	Issued	Lattice Semiconductor Corporation
10/266,361	6639434	United States	Low voltage differential signaling systems and methods	Issued	Lattice Semiconductor Corporation
10/269,804	7111183	United States	Expansion method for complex power-sequencing applications	Issued	Lattice Semiconductor Corporation
10/269,450	6791394	United States	Power Supply Control Circuits	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 66

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/269,439	6762618	United States	Innovative verify scheme for two level GRP fuse in programmable bus switching family	Issued	Lattice Semiconductor Corporation
10/272,582	6901572	United States	Power Sequence Controller Programming Technique	Issued	Lattice Semiconductor Corporation
10/278,415	6639449	United States	Asynchronous glitch-free clock multiplexer	Issued	Lattice Semiconductor Corporation
10/282,524	7051261	United States	Turbo Encoder With Reduced Processing Delay	Issued	Lattice Semiconductor Corporation
10/283,765	6700823	United States	Programmable common mode termination for differential input/output circuits	Issued	Lattice Semiconductor Corporation
10/288,667	7000210	United States	Adaptive Adjustment Of Constraints During PLD Placement Processing	Issued	Lattice Semiconductor Corporation
10/288,668	6813754	United States	Placement Processing For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/300,190	6825733	United States	Low Jitter Integrated Phase Locked Loop With Broad Tuning Range	Issued	Lattice Semiconductor Corporation
10/302,439	6797568	United States	Flash Technology Transistors and Method For Forming Same	Issued	Lattice Semiconductor Corporation
10/308,420	6710641	United States	Low Voltage Bandgap Reference Circuit	Issued	Lattice Semiconductor Corporation
10/309,302	6650188	United States	Improved Coupling For LC-Based VCO	Issued	Lattice Semiconductor Corporation
10/334,642	6777979	United States	FIFO memory architecture	Issued	Lattice Semiconductor Corporation
10/338,619	6753696	United States	Programmable optimized-distribution logic allocator for	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			a high-density complex PLD		Corporation
10/365,083	7034596	United States	Adaptive input logic for phase adjustments	Issued	Lattice Semiconductor Corporation
10/368,023	6915323	United States	Macrocells Supporting A Carry Cascade	Issued	Lattice Semiconductor Corporation
10/366,956	6788101	United States	Programmable input buffer for differential and single-ended signals	Issued	Lattice Semiconductor Corporation
10/367,323	6812869	United States	Noise Reduction Techniques For Programmable I/O Circuits	Issued	Lattice Semiconductor Corporation
10/370,232	6861870	United States	Dynamic Cross point Switch With Shadow Memory Architecture	Issued	Lattice Semiconductor Corporation
10/377,320	6859066	United States	Bank based input/output buffers in field programmable gate arrays with multiple reference voltages	Issued	Lattice Semiconductor Corporation
10/387,814	7305047	United States	Automatic lane assignment for Receiver	Issued	Lattice Semiconductor Corporation
10/387,243	7339952	United States	Pointer Processing For Optical Communication Systems	Issued	Lattice Semiconductor Corporation
10/391,094	6870395	United States	PLDs With Integrated Standard Cell Logic Blocks	Issued	Lattice Semiconductor Corporation
10/392,751	RE39510	United States	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	Issued	Lattice Semiconductor Corporation
10/397,669	6967500	United States	Electronic Circuit With OnChip Programmable Terminations	Issued	Lattice Semiconductor Corporation
10/400,705	6873187	United States	Method and Apparatus for Controlling Signal Distribution In An Electronic	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 68

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Circuit		
10/406,050	7000212	United States	Hierarchical General Interconnect Architecture For High Density FPGA's	Issued	Lattice Semiconductor Corporation
10/409,543	6986004	United States	FIFO memory with programmable data port widths	Issued	Lattice Semiconductor Corporation
10/417,290	6879184	United States	Programmable logic device architecture based on arrays of LUT-based Boolean terms	Issued	Lattice Semiconductor Corporation
10/425,863	6903575	United States	Scalable device architecture for high-speed interfaces	Issued	Lattice Semiconductor Corporation
10/425,862	6894530	United States	Programmable And Fixed Logic Circuitry For High-Speed Interfaces	Issued	Lattice Semiconductor Corporation
10/428,889	6879182	United States	CPLD with multi-function blocks and distributed memory	Issued	Lattice Semiconductor Corporation
10/428,885	6861871	United States	Cascaded logic block architecture for complex programmable logic devices	Issued	Lattice Semiconductor Corporation
10/428,888	6864713	United States	Multi-Stage Interconnect Architecture For Complex Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/428,982	6922078	United States	Enhanced wide and deep logic capability for high density, high performance CPLDs	Issued	Lattice Semiconductor Corporation
10/439,602	6828823	United States	Non-volatilie and reconfigurable PLDs	Issued	Lattice Semiconductor Corporation
10/441,814	7039842	United States	Measuring Propagation Delays of Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/447,120	7301996	United States	skew cancellation for source synchronous clock and data signals	Issued	Lattice Semiconductor Corporation
10/447,451	7009433	United States	Digitally Controlled Delay Cells	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 69

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/457,630	7304863	United States	Integrated Circuit Including External Electronic Components With Low Insertion Loss	Issued	Lattice Semiconductor Corporation
10/459,091	6879598	United States	Flexible Media Access Control Architecture	Issued	Lattice Semiconductor Corporation
10/460,385	6856171	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
10/463,781	6861868	United States	High Speed Interface For A Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/464,083	6882555	United States	Bi-directional buffering for memory data lines	Issued	Lattice Semiconductor Corporation
10/600,042	6822477	United States	Integrated Circuit And Associated Design Method Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/610,253	6977408	United States	High-Performance Non-volatile Memory Device and Fabrication Process	Issued	Lattice Semiconductor Corporation
10/613,460	7132903	United States	Noise-shielding, switch-controlled load circuitry for oscillators and the like	Issued	Lattice Semiconductor Corporation
10/613,462	6952115	United States	Programmable I/O Interfaces For FPGAs And Other PLDs	Issued	Lattice Semiconductor Corporation
10/617,980	6958625	United States	PLD With Hardwired Microsequencer	Issued	Lattice Semiconductor Corporation
10/619,711	6903573	United States	Programmable Logic Device With Enhanced Wide Input Product Term Cascading	Issued	Lattice Semiconductor Corporation
10/620,286	6919736	United States	FPGA having partitionable embedded memory with configurable depth and width	Issued	Lattice Semiconductor Corporation
10/619,645	7098685	United States	Scalable Serializer-Deserializer Architecture and	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 70

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Programmable Interface		Corporation
10/620,147	7032203	United States	Algorithm to increase logic input width by cascading product terms	Issued	Lattice Semiconductor Corporation
10/624,965	6940309	United States	Programmable Logic Device With A Memory-Based Finite State Machine	Issued	Lattice Semiconductor Corporation
10/626,089	6737702	United States	Zero Power Memory Cell with Reduced Threshold Voltage	Issued	Lattice Semiconductor Corporation
10/628,656	6970047	United States	Programmable lock detector and corrector	Issued	Lattice Semiconductor Corporation
10/628,657	6924659	United States	Programmable Signal Termination for FPGAs and the Like	Issued	Lattice Semiconductor Corporation
10/629,223	7019577	United States	Clock Generator	Issued	Lattice Semiconductor Corporation
10/629,512	6903574	United States	Memory Access Via Serial Memory Interface	Issued	Lattice Semiconductor Corporation
10/629,221	6885227	United States	Clock Generator With Skew Control	Issued	Lattice Semiconductor Corporation
10/640,804	6877667	United States	Integrated Circuit And Associated Design Method With Antenna Error Control Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/640,828	6838904	United States	Enhanced CPLD Macrocell Module Having Selectable Bypass of Steering-Based Resource Allocation	Issued	Lattice Semiconductor Corporation
10/641,260	6940779	United States	Programmable broadcasting initialization of embedded memory blocks on FPGA	Issued	Lattice Semiconductor Corporation
10/642,370	6924664	United States	FPGA	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 71

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/655,686	6842037	United States	Shared Transmission Line Communication System and Method	Issued	Lattice Semiconductor Corporation
10/660,814	7038490	United States	Delay matched ASIC conversion of a PLD	Issued	Lattice Semiconductor Corporation
10/665,920	6970022	United States	Controlled hysteresis comparator with rail-to-rail input	Issued	Lattice Semiconductor Corporation
10/671,378	6943583	United States	Programmable I/O structure for FPGAs and the like having reduced pad capacitance	Issued	Lattice Semiconductor Corporation
10/671,363	6943582	United States	Programmable I/O structure for FPGAs and the Like Having Shared Circuitry	Issued	Lattice Semiconductor Corporation
10/671,756	6909663	United States	Multiport Memory With Twisted Bitlines	Issued	Lattice Semiconductor Corporation
10/676,536	7269771	United States	Semiconductor Device Adapted For Forming Multiple Scan Chains	Issued	Lattice Semiconductor Corporation
10/687,468	6809674	United States	Analog-to-digital converters	Issued	Lattice Semiconductor Corporation
10/699,321	7067883	United States	Lateral High-Voltage Junction Device	Issued	Lattice Semiconductor Corporation
10/701,005	7091763	United States	Clock generation	Issued	Lattice Semiconductor Corporation
10/704,025	7088134	United States	PLD With Flexible Memory Allocation And Routing	Issued	Lattice Semiconductor Corporation
10/726,972	7100058	United States	Programmable Power Management System And Method	Issued	Lattice Semiconductor Corporation
10/728,685	7187157	United States	Power supply remote voltage sensing	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 72

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/737,514	6981381	United States	Linear Thermoelectric Device Driver	Issued	Lattice Semiconductor Corporation
10/744,353	7132864	United States	Method for configuring multiple-output phase-locked loop frequency synthesizer	Issued	Lattice Semiconductor Corporation
10/769,174	7024646	United States	Electrostatic Discharge Simulation	Issued	Lattice Semiconductor Corporation
10/768,643	7019584	United States	Output Stages For High Current Low Noise Bandgap Reference Circuit Implementations	Issued	Lattice Semiconductor Corporation
10/782,564	6972986	United States	Combination FPGA	Issued	Lattice Semiconductor Corporation
10/783,886	7081771	United States	Upgradeable And Reconfigurable Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/791,073	7191388	United States	Fast diagonal interleaved parity (DIP) calculator	Issued	Lattice Semiconductor Corporation
10/794,079	7257727	United States	Timer Systems and Methods	Issued	Lattice Semiconductor Corporation
10/794,524	7017063	United States	systems and methods for controlling voltage regulator module power supplies	Issued	Lattice Semiconductor Corporation
10/794,498	7028201	United States	Powering up a device having digital and analog circuitry	Issued	Lattice Semiconductor Corporation
10/797,759	7068556	United States	Sense Amplifier Systems and Methods	Issued	Lattice Semiconductor Corporation
10/809,180	7234030	United States	Table based scheduler for FIFOs and the like	Issued	Lattice Semiconductor Corporation
10/809,658	7095247	United States	Configuring FPGAs and the like using one or more serial memory devices	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 73

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/815,403	7167032	United States	Self-adjusting schmitt trigger	Issued	Lattice Semiconductor Corporation
10/817,215	7081781	United States	Charge pump for a low-voltage wide-tuning range phase-locked loop	Issued	Lattice Semiconductor Corporation
10/829,865	6998896	United States	Dynamic gain adjustment systems and method for metastability resistance	Issued	Lattice Semiconductor Corporation
10/834,528	6998906	United States	Low pass filter systems and methods	Issued	Lattice Semiconductor Corporation
10/837,086	7307319	United States	High Voltage Protection Device And Process	Issued	Lattice Semiconductor Corporation
10/842,345	7002418	United States	Control Signal Generation ...	Issued	Lattice Semiconductor Corporation
10/841,987	7224213	United States	switched-capacitor ripple-smoothing filter	Issued	Lattice Semiconductor Corporation
10/843,708	7061269	United States	IO buffer architecture for programmable devices	Issued	Lattice Semiconductor Corporation
10/856,100	7196551	United States	Current Mode Logic Buffer	Issued	Lattice Semiconductor Corporation
10/857,667	7064973	United States	Combination FPGA	Issued	Lattice Semiconductor Corporation
10/885,419	7116585	United States	Memory Systems And Methods	Issued	Lattice Semiconductor Corporation
10/910,091	7215591	United States	Byte enable logic for memory	Issued	Lattice Semiconductor Corporation
10/912,943	7471752	United States	Data Transmission Synchronization	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 74

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/928,563	7078286	United States	Process for fabricating a semiconductor device having electrically isolated low voltage and high voltage regions	Issued	Lattice Semiconductor Corporation
10/929,199	7484144	United States	Testing embedded memory in an integrated circuit	Issued	Lattice Semiconductor Corporation
10/944,978	7135886	United States	FPGA Using Both Volatile and NonVolatile Memory Cell Properties	Issued	Lattice Semiconductor Corporation
10/974,453	7307912	United States	Variable data width memory systems and methods	Issued	Lattice Semiconductor Corporation
10/973,750	7149129	United States	memory output data systems and methods with feedback	Issued	Lattice Semiconductor Corporation
10/974,107	7164290	United States	FPGA Logic Unit	Issued	Lattice Semiconductor Corporation
10/974,305	7129749	United States	PLD Having A Configurable DRAM With Transparent Refresh	Issued	Lattice Semiconductor Corporation
10/978,899	7376872	United States	Testing embedded memory in integrated circuits such as progammable logic circuits	Issued	Lattice Semiconductor Corporation
10/996,283	7161862	United States	Low power asynchronous sense amp	Issued	Lattice Semiconductor Corporation
11/007,954	7230810	United States	Dynamic over-voltage protection scheme for integrated circuit devices	Issued	Lattice Semiconductor Corporation
11/012,550	7215149	United States	Interface circuitry for electrical systems	Issued	Lattice Semiconductor Corporation
11/012,548	7215148	United States	Programmable current LVDS output buffer	Issued	Lattice Semiconductor Corporation
11/015,265	7177221	United States	Method of initializing configurable multi-port	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 75

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			embedded memory blocks in an FPGA		Corporation
11/016,665	7187203	United States	Cascadable memory	Issued	Lattice Semiconductor Corporation
11/015,369	7177207	United States	Sense amplifier timing	Issued	Lattice Semiconductor Corporation
11/036,630	7257750	United States	Self-verification of configuration memory in PLDs	Issued	Lattice Semiconductor Corporation
11/036,738	7242053	United States	EEPROM Device with voltage-limiting charge pump circuit	Issued	Lattice Semiconductor Corporation
11/040,772	7208975	United States	Serdes with programmable I/O architecture	Issued	Lattice Semiconductor Corporation
11/041,319	7183798	United States	Synchronous memory	Issued	Lattice Semiconductor Corporation
11/044,089	7109754	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
11/044,149	7109756	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
11/044,508	7034599	United States	Clock Generator With Skew Control	Issued	Lattice Semiconductor Corporation
11/054,011	7221607	United States	Mult-port memory systems and methods for bit line coupling	Issued	Lattice Semiconductor Corporation
11/055,280	6975137	United States	PLDs With Integrated Standard Cell Logic Blocks	Issued	Lattice Semiconductor Corporation
11/054,750	7382293	United States	Data Decompression	Issued	Lattice Semiconductor Corporation
11/054,855	7589648	United States	Data Decompression	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/064,477	7532646	United States	Distributed multiple channel alignment scheme	Issued	Lattice Semiconductor Corporation
11/071,356	7245154	United States	Differential Input Receiver with Programmable Failsafe	Issued	Lattice Semiconductor Corporation
11/070,926	7057397	United States	Output Impedance Measurement Techniques	Issued	Lattice Semiconductor Corporation
11/083,625	7376204	United States	Detection of Unknown symbol rate in a digitally modulated signal	Issued	Lattice Semiconductor Corporation
11/098,713	7265578	United States	In-System Programming Of a Non-Compliant Device Using Multiple Interfaces Of A PLD	Issued	Lattice Semiconductor Corporation
11/100,718	7397274	United States	In-System Programming Of a Non-Compliant Device Using Multiple Interfaces Of A PLD	Issued	Lattice Semiconductor Corporation
11/108,927	7193436	United States	Fast Processing Path Using FPGA Logic Units	Issued	Lattice Semiconductor Corporation
11/109,301	7630464	United States	Analog-to-digital systems and methods	Issued	Lattice Semiconductor Corporation
11/109,966	6977521	United States	FPGA	Issued	Lattice Semiconductor Corporation
11/121,326	7400171	United States	Electronic Switch Having Extended Voltage Range	Issued	Lattice Semiconductor Corporation
11/134,152	7009423	United States	Programmable I/O Interfaces For FPGAs And Other PLDs	Issued	Lattice Semiconductor Corporation
11/157,345	7685483	United States	Design-For-Test features for a memory in an FPGA	Issued	Lattice Semiconductor Corporation
11/157,349	7378879	United States	Decoding systems and methods	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 77

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/165,709	7256613	United States	Programmable Interconnect Architecture for PLDs	Issued	Lattice Semiconductor Corporation
11/165,853	7342838	United States	PLD With A Double Data Rate SDRAM Interface	Issued	Lattice Semiconductor Corporation
11/185,242	7519139	United States	Signal monitoring systems and methods	Issued	Lattice Semiconductor Corporation
11/187,179	7342846	United States	address decoding systems and methods	Issued	Lattice Semiconductor Corporation
11/187,114	7253674	United States	Fine output clock phase alignment circuitry	Issued	Lattice Semiconductor Corporation
11/189,067	7505752	United States	Receiver used for differential signaling and reference voltage signaling with programmable common mode	Issued	Lattice Semiconductor Corporation
11/194,871	7414913	United States	Bitline twisting scheme for a multiport memory	Issued	Lattice Semiconductor Corporation
11/194,356	7262630	United States	Dynamic programmable termination for parallel and differential schemes	Issued	Lattice Semiconductor Corporation
11/199,287	7599457	United States	clock-and-data-recovery system having a multi-phase clock generator for one or more channel circuits	Issued	Lattice Semiconductor Corporation
11/200,983	7295035	United States	Programmable Logic Device With Enhanced Logic Block Architecture	Issued	Lattice Semiconductor Corporation
11/200,941	7411419	United States	I/O Systems and Methods	Issued	Lattice Semiconductor Corporation
11/202,149	7606851	United States	Correlator having user-defined processing	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 78

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/201,620	7187586	United States	Flash memory erase verification systems and methods	Issued	Lattice Semiconductor Corporation
11/206,282	RE40311	United States	Zero Power Programmable Memory Cell	Issued	Lattice Semiconductor Corporation
11/226,695	7301182	United States	Circuit layout for improved performance while preserving or improving density	Issued	Lattice Semiconductor Corporation
11/230,087	7167405	United States	Data transfer verification systems and methods	Issued	Lattice Semiconductor Corporation
11/235,616	7376037	United States	PLD with power-saving architecture	Issued	Lattice Semiconductor Corporation
11/236,967	7405446	United States	Electrostatic Protection Systems and Methods	Issued	Lattice Semiconductor Corporation
11/243,255	7088132	United States	Configuring FPGAs and the like using one or more serial memory devices	Issued	Lattice Semiconductor Corporation
11/251,682	7196963	United States	Address isolation for user-defined configuration memory in programmable devices	Issued	Lattice Semiconductor Corporation
11/252,094	7263024	United States	Clock reset address decoder for block memory	Issued	Lattice Semiconductor Corporation
11/252,126	7061275	United States	FPGA	Issued	Lattice Semiconductor Corporation
11/257,137	7685215	United States	Fast-carry arithmetic circuit using a multi-input LUT	Issued	Lattice Semiconductor Corporation
11/257,641	7317343	United States	PULSE-GENERATION CIRCUIT HAVING PULSE GENERATORS AND SET-RESET LATCHES	Issued	Lattice Semiconductor Corporation
11/260,097	7212051	United States	Control signal generation for a low jitter switched-capacitor frequency synthesizer	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/281,651	7495495	United States	Digital I/O Timing Control	Issued	Lattice Semiconductor Corporation
11/287,720	7327159	United States	Interface Block Architectures	Issued	Lattice Semiconductor Corporation
11/290,205	7242634	United States	Pseudo-dynamic word-line driver	Issued	Lattice Semiconductor Corporation
11/293,941	7538574	United States	Transparent Field Reconfiguration for PLDs	Issued	Lattice Semiconductor Corporation
11/302,097	7620839	United States	Jitter Tolerant Delay-Locked Loop Circuit	Issued	Lattice Semiconductor Corporation
11/300,886	7495467	United States	Temperature independent, linear on-chip termination resistance	Issued	Lattice Semiconductor Corporation
11/332,986	7382169	United States	Systems and Methods for Reducing Static Phase Error	Issued	Lattice Semiconductor Corporation
11/335,890	7439783	United States	Phase-Locked Loop Systems And Methods	Issued	Lattice Semiconductor Corporation
11/345,713	7547995	United States	dynamic over voltage protection scheme for interface circuitry	Issued	Lattice Semiconductor Corporation
11/346,817	7554357	United States	Efficient Configuration of Daisy-Chained Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
11/350,436	7375549	United States	Reconfiguration of PLDs	Issued	Lattice Semiconductor Corporation
11/356,805	7277348	United States	Memory Cell Comprising And OTP NV Memory Unit And SRAM Unit	Issued	Lattice Semiconductor Corporation
11/360,337	7355441	United States	PLD with distributed memory and non-volatile memory	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 80

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/361,584	7596744	United States	Auto recovery from volatile soft error upsets (SEUs)	Issued	Lattice Semiconductor Corporation
11/362,289	7759926	United States	dynamic phase offset measurement	Issued	Lattice Semiconductor Corporation
11/361,643	7446573	United States	Comparator Systems And Methods	Issued	Lattice Semiconductor Corporation
11/398,437	7459931	United States	PLDs with transparent field reconfiguration	Issued	Lattice Semiconductor Corporation
11/397,985	7554358	United States	PLDs with user non-volatile memory	Issued	Lattice Semiconductor Corporation
11/416,881	7623378	United States	Selective programming of non-volatile memory facilitated by security fuses	Issued	Lattice Semiconductor Corporation
11/435,956	7102934	United States	Sense Amplifier Systems and Methods	Issued	Lattice Semiconductor Corporation
11/442,186	7411417	United States	Selective loading of configuration data into configuration memory cells	Issued	Lattice Semiconductor Corporation
11/446,548	7378873	United States	PLD providing a serial peripheral interface	Issued	Lattice Semiconductor Corporation
11/445,620	7378872	United States	PLD architecture with multiple slice types	Issued	Lattice Semiconductor Corporation
11/446,542	7385417	United States	Dual slice architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/446,351	7397276	United States	Logic block control architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/446,308	7546498	United States	PLDs with custom identification systems and methods	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 81

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/446,309	7495970	United States	Flexible memory architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/447,591	7631223	United States	PLD methods and systems for providing multi-boot configuration data support	Issued	Lattice Semiconductor Corporation
11/452,714	7463060	United States	PLD and method of testing	Issued	Lattice Semiconductor Corporation
11/455,315	7215139	United States	Upgradeable And Reconfigurable Programmable Logic Device	Issued	Lattice Semiconductor Corporation
11/425,273	7702100	United States	Key generation for advanced encryption standard (AES) decryption and the like	Issued	Lattice Semiconductor Corporation
11/425,881	7657773	United States	Clock distribution chip for generating both zero-delay and non-zero-delay clock signals	Issued	Lattice Semiconductor Corporation
11/477,759	7348914	United States	Methods and systems to align output signals of an analog-to-digital converter	Issued	Lattice Semiconductor Corporation
11/487,647	7636259	United States	Flash memory array with independently erasable sectors	Issued	Lattice Semiconductor Corporation
11/487,751	7512015	United States	Negative voltage blocking for embedded memories	Issued	Lattice Semiconductor Corporation
11/492,687	7466190	United States	Charge pump with four-well transistors	Issued	Lattice Semiconductor Corporation
11/494,862	7521969	United States	Switch sequencing circuit systems and methods	Issued	Lattice Semiconductor Corporation
11/461,222	7411432	United States	Integrated circuits and complementary CMOS circuits for frequency dividers	Issued	Lattice Semiconductor Corporation
11/498,645	7675313	United States	Methods and systems for storing a security key using programmable fuses	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 82

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/498,646	7605606	United States	Area efficient routing architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/530,620	7456672	United States	Clock systems and methods	Issued	Lattice Semiconductor Corporation
11/533,188	7511641	United States	Efficient bitstream compression	Issued	Lattice Semiconductor Corporation
11/551,459	7831754	United States	Multiple Communication Channel Configuration Systems And Methods	Issued	Lattice Semiconductor Corporation
11/556,528	7663401	United States	Multiplexer initialization systems and methods	Issued	Lattice Semiconductor Corporation
11/593,274	7535258	United States	Programmable Voltage LVDS Output Buffer	Issued	Lattice Semiconductor Corporation
11/557,808	7725803	United States	PLD programming verification systems and methods	Issued	Lattice Semiconductor Corporation
11/638,156	7429875	United States	Low Static Current Drain Logic Circuit	Issued	Lattice Semiconductor Corporation
11/643,288	7443192	United States	Output buffer with digital slew control	Issued	Lattice Semiconductor Corporation
11/624,021	7623391	United States	Data transfer verification systems and methods	Issued	Lattice Semiconductor Corporation
11/671,948	7576563	United States	Flexible High Fan-out Signal Routing Systems and Methods	Issued	Lattice Semiconductor Corporation
11/675,246	7313025	United States	Flash memory erase verification systems and methods	Issued	Lattice Semiconductor Corporation
11/676,071	7430706	United States	Fast diagonal interleaved parity (DIP) calculator	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 83

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/680,526	7598765	United States	Redundancy for Configuration RAM	Issued	Lattice Semiconductor Corporation
11/691,003	7536615	United States	Logic analyzer systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/691,040	7743296	United States	Logic analyzer systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/737,702	7509598	United States	Clock Boosting Systems and Methods	Issued	Lattice Semiconductor Corporation
11/750,790	7401280	United States	Self-verification of configuration memory in PLDs	Issued	Lattice Semiconductor Corporation
11/750,616	7632011	United States	Integrated Circuit Temperature Sensors Systems and Methods	Issued	Lattice Semiconductor Corporation
11/760,411	8065574	United States	Real Soft Error Detect Scheme for Testing	Issued	Lattice Semiconductor Corporation
11/761,221	7570078	United States	PLD Providing A Serial Peripheral Interfaces	Issued	Lattice Semiconductor Corporation
11/778,457	7573770	United States	Distributed front-end FIFO for source-synchronized interfaces with non-continuous clocks	Issued	Lattice Semiconductor Corporation
11/779,246	7446679	United States	FPGA data compression using combined RLE BE, LZ, Row LZ and BE ROW encoding	Issued	Lattice Semiconductor Corporation
11/863,016	7681160	United States	Weight based look up table collapsing for programmable logic devices	Issued	Lattice Semiconductor Corporation
11/865,556	7539076	United States	Variable data width memory systems and methods	Issued	Lattice Semiconductor Corporation
11/869,019	7616029	United States	Hysteresis-based processing for applications such as signal bias monitors	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 84

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/872,950	7586344	United States	Dynamic delay or advance adjustment of oscillating signal phase	Issued	Lattice Semiconductor Corporation
11/875,748	7757198	United States	Scan chain systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/877,434	7411414	United States	Single-Ended Output Driver Buffer	Issued	Lattice Semiconductor Corporation
11/924,088	8132040	United States	Channel-to-channel deskew systems and methods	Issued	Lattice Semiconductor Corporation
11/934,711	7573291	United States	Programmable Logic Device With Enhanced Logic Block Architecture	Issued	Lattice Semiconductor Corporation
11/937,328	7788620	United States	An IO placement systems and methods to reduce SSO noise	Issued	Lattice Semiconductor Corporation
11/937,300	7895555	United States	Simultaneous Switching Output Noise Estimation and Reduction Systems and Methods	Issued	Lattice Semiconductor Corporation
11/939,787	7863931	United States	Flexible Delay Cell Architecture	Issued	Lattice Semiconductor Corporation
11/941,031	7902865	United States	Compression and decompression of configuration data using repeated data frames	Issued	Lattice Semiconductor Corporation
11/941,006	7535253	United States	Method of Retaining Register Data during Field Update of PLD	Issued	Lattice Semiconductor Corporation
11/947,662	7788623	United States	Composite wire indexing for PLDs	Issued	Lattice Semiconductor Corporation
11/949,130	7586325	United States	IC having independent voltage and process/temperature control	Issued	Lattice Semiconductor Corporation
12/001,600	7728625	United States	Serial interface for PLDs	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 85

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/957,598	7605609	United States	A programmable level shifter optimized for high performance and low power.	Issued	Lattice Semiconductor Corporation
11/959,329	7630259	United States	PLD with built in self test	Issued	Lattice Semiconductor Corporation
11/970,212	7646643	United States	Process charging monitor for nonvolatile memory	Issued	Lattice Semiconductor Corporation
12/019,526	7787326	United States	PLD With Mult-Rate SDRAM Interface	Issued	Lattice Semiconductor Corporation
12/021,202	8069329	United States	Dynamic Multiple Pattern Configuration Scheme For Volatile FPGAs	Issued	Lattice Semiconductor Corporation
12/044,842	7652500	United States	Reconfiguration of PLDs	Issued	Lattice Semiconductor Corporation
12/055,170	7890913	United States	Wire Mapping For PLDs	Issued	Lattice Semiconductor Corporation
12/060,776	7459935	United States	PLD With Distributed Memory	Issued	Lattice Semiconductor Corporation
12/061,885	7831856	United States	Detection of Timing Errors in Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/099,933	7661878	United States	On-Chip Temperature Sensor For An Integrated Circuit	Issued	Lattice Semiconductor Corporation
12/100,859	7558143	United States	Programmable Logic Device With Power-Saving Architecture	Issued	Lattice Semiconductor Corporation
12/105,146	7557606	United States	Synchronization Of Data Signals And Clock Signals For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/105,959	7696784	United States	PLD With Multiple Slice	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 86

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Types		Corporation
12/107,883	7560953	United States	Power Management Systems And Methods for PLDs	Issued	Lattice Semiconductor Corporation
12/122,489	7897448	United States	Formation Of High Voltage Transistor With High Breakdown Voltage	Issued	Lattice Semiconductor Corporation
12/146,042	8463832	United States	Digital Signal Processing Block Architecture For PLD	Issued	Lattice Semiconductor Corporation
12/164,265	7592834	United States	Logic Block Control Architectures For PLDs	Issued	Lattice Semiconductor Corporation
12/182,940	8261160	United States	Serial data recovery out of 8 samples with FPGAs	Issued	Lattice Semiconductor Corporation
12/186,027	7579865	United States	Selective Loading Of Configuration Data Into Configuration Memory Cells	Issued	Lattice Semiconductor Corporation
12/188,120	7605602	United States	Low-Power Output Driver Buffer Circuit	Issued	Lattice Semiconductor Corporation
12/238,959	7911229	United States	Programmable Signal Routing Systems	Issued	Lattice Semiconductor Corporation
12/273,868	7663419	United States	Clock Systems And Methods	Issued	Lattice Semiconductor Corporation
12/277,217	8112731	United States	Congestion-driven placement based on region interconnection for FPGA	Issued	Lattice Semiconductor Corporation
12/323,974	7992120	United States	congestion estimation based on pass probability net estimation process	Issued	Lattice Semiconductor Corporation
12/327,128	7656193	United States	Programmable Logic Device And Method Of Testing	Issued	Lattice Semiconductor Corporation
12/337,502	8856718	United States	Precise Congestion Estimation for FPGA Router	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
12/341,929	8181139	United States	Multi-Priority Placement	Issued	Lattice Semiconductor Corporation
12/370,039	7714608	United States	Temperature-Independent, Linear On-Chip Termination Resistance	Issued	Lattice Semiconductor Corporation
12/389,149	7957208	United States	Flexible memory architectures for PLDs	Issued	Lattice Semiconductor Corporation
12/402,751	7844243	United States	Receiver used for differential signaling and reference voltage signaling with programmable common mode	Issued	Lattice Semiconductor Corporation
12/406,772	8069431	United States	An alternative method for pin swapping in FPGA routing	Issued	Lattice Semiconductor Corporation
12/408,047	8086986	United States	Clock Boosting Systems And Methods	Issued	Lattice Semiconductor Corporation
12/409,757	7675321	United States	Dual-Slice Architectures For PLDs	Issued	Lattice Semiconductor Corporation
12/413,787	7808405	United States	Efficient Bitstream Compression	Issued	Lattice Semiconductor Corporation
12/430,848	7741865	United States	Soft Error Upset Hardened Integrated Circuit Systems And Methods	Issued	Lattice Semiconductor Corporation
12/464,822	7876125	United States	Method of Retaining Register Data during Field Update of PLD	Issued	Lattice Semiconductor Corporation
12/465,444	7868654	United States	Economical way to improve volatile FPGA boot up data throughput by utilizing one or more SPI boot PROMs w/o sacrificing additional FPGA pins	Issued	Lattice Semiconductor Corporation
12/467,800	7737723	United States	Transparent Field Reconfiguration for PLDs	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 88

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
12/476,155	8044682	United States	FPGA Having Low Power, Fast Carry Chain	Issued	Lattice Semiconductor Corporation
12/480,565	7702977	United States	PLDs with custom identification systems and methods	Issued	Lattice Semiconductor Corporation
12/494,822	8165164	United States	Circuit For In-System Reconfigurable Mapping Of IQ Data Into A CPRI Basic Frame	Issued	Lattice Semiconductor Corporation
12/502,141	7724029	United States	Power Management For Integrated Circuits Such As Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/511,388	7768300	United States	PLD Providing A Serial Peripheral Interfaces	Issued	Lattice Semiconductor Corporation
12/512,944	8255733	United States	Method of selecting precise delay or skew shifts	Issued	Lattice Semiconductor Corporation
12/512,961	7969248	United States	VCO digital center frequency coarse tune algorithm	Issued	Lattice Semiconductor Corporation
12/538,810	7808855	United States	Distributed front-end FIFO for source-synchronized interfaces with non-continuous clocks	Issued	Lattice Semiconductor Corporation
12/561,140	8010871	United States	Auto recovery from volatile soft error upsets (SEUs)	Issued	Lattice Semiconductor Corporation
12/564,781	7746107	United States	Redundancy for Configuration RAM	Issued	Lattice Semiconductor Corporation
12/578,470	8122277	United States	Clock distribution chip	Issued	Lattice Semiconductor Corporation
12/578,492	8112656	United States	Clock distribution chip	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 89

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/607,868	7989911	United States	STI with trench liner of increased thickness	Issued	Lattice Semiconductor Corporation
12/607,333	7985656	United States	STI with trench liner of increased thickness	Issued	Lattice Semiconductor Corporation
12/611,262	8059470	United States	Flash memory array with independently erasable sectors	Issued	Lattice Semiconductor Corporation
12/626,289	7944765	United States	PLD with built in self test	Issued	Lattice Semiconductor Corporation
12/630,163	8060784	United States	PLD And Methods For Providing Multi-Boot Configuration Data Support	Issued	Lattice Semiconductor Corporation
12/637,884	8200179	United States	Combined Variable Gain Amplifier And Linear Equalizer With Independent Gain And Frequency Control	Issued	Lattice Semiconductor Corporation
12/698,283	8040152	United States	IO Ring Configuration Scheme with sharing of BC7 register	Issued	Lattice Semiconductor Corporation
12/706,227	7924054	United States	Latency measurement circuit for wireless communications applications	Issued	Lattice Semiconductor Corporation
12/709,685	7834652	United States	Methods and systems for storing a security key using programmable fuses	Issued	Lattice Semiconductor Corporation
12/729,952	8040159	United States	High Speed Comparator with Data Dependent Jitter Mitigation	Issued	Lattice Semiconductor Corporation
12/752,455	8384427	United States	Serial Peripheral Interface Daisy Chaining using a Flow-Through Option	Issued	Lattice Semiconductor Corporation
12/757,087	8664774	United States	A Method for Arranging IC Bondwires for the Reduction of Crosstalk	Issued	Lattice Semiconductor Corporation
12/786,359	8108754	United States	PLD programming verification systems and methods	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 90

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/813,540	8164499	United States	Shared-Array Multiple-Output Digital to Analog Converter	Issued	Lattice Semiconductor Corporation
12/813,573	8441292	United States	Method of delaying data from clock in 1UI steps	Issued	Lattice Semiconductor Corporation
12/818,544	7868646	United States	Soft Error Upset Hardened Integrated Circuit Systems And Methods	Issued	Lattice Semiconductor Corporation
12/871,764	8286116	United States	Composite Wire Indexing For PLDs	Issued	Lattice Semiconductor Corporation
12/977,011	8522126	United States	Method Of Blocking PLC Distributed SRAM Readback In User Mode	Issued	Lattice Semiconductor Corporation
12/976,412	8351287	United States	Bitline Floating Circuit For Power Reduction On SRAM Array	Issued	Lattice Semiconductor Corporation
12/976,520	8477549	United States	Strobed And Latched Readback Of SRAM Bits In A FPGA	Issued	Lattice Semiconductor Corporation
12/987,393	8274412	United States	Low Power SerDes With Built- In Word Alignment For Odd And Even Gearing Ratios	Issued	Lattice Semiconductor Corporation
13/006,622	8384428	United States	Programmable IO Pad - embedded function block	Issued	Lattice Semiconductor Corporation
13/007,804	8248136	United States	Low Power And Glitch-less Delay Element For High Speed Receiver Interface	Issued	Lattice Semiconductor Corporation
13/007,688	8324934	United States	Programmable Ratio Input Buffer	Issued	Lattice Semiconductor Corporation
13/026,555	8104009	United States	Wire Mapping For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
13/034,174	8058898	United States	Compression and Decompression Of Configuration Data Using	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 91

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Repeated Data Frames		
13/038,259	8368424	United States	Wakeup from sleep mode using slave I2C port or slave SPI port with powered down core logic	Issued	Lattice Semiconductor Corporation
13/038,270	8816718	United States	Slow Respond Mode Protocol For Synchronous Read	Issued	Lattice Semiconductor Corporation
13/037,703	8654600	United States	Current Sense Amplifier With Low Voltage Operation	Issued	Lattice Semiconductor Corporation
13/052,142	8553463	United States	Positive-To-Negative Voltage Discharge Circuit	Issued	Lattice Semiconductor Corporation
13/076,300	8319521	United States	Safe programming of key information into NV memory	Issued	Lattice Semiconductor Corporation
13/079,578	8314634	United States	Power Saving Standby Mode With Glitch-Less Output Controls	Issued	Lattice Semiconductor Corporation
13/079,595	8531222	United States	PLL Switchable Feedback Loops Among Internal And External Feedback Paths	Issued	Lattice Semiconductor Corporation
13/083,889	8138790	United States	Latency measurement circuit for wireless communications applications	Issued	Lattice Semiconductor Corporation
13/154,885	8441284	United States	Flexible Way To Incrementally Update Multi-Bit Data Registers	Issued	Lattice Semiconductor Corporation
13/155,547	8547075	United States	Filter And Stability Capacitor Reuse For On-Chip Dual Output Voltage Regulators	Issued	Lattice Semiconductor Corporation
13/164,108	8555217	United States	Cross-Probing Technology Between Software Plug-In Modules	Issued	Lattice Semiconductor Corporation
13/178,599	8539409	United States	Multiple silicon products from a common base set of masks	Issued	Lattice Semiconductor Corporation
13/178,536	8495264	United States	Packet And Control Symbol	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Alignment Circuit For SRIO		Corporation
13/193,984	8314632	United States	Placing ICs Into Ultra-Low Voltage Mode For Standby Purposes	Issued	Lattice Semiconductor Corporation
13/212,121	8451679	United States	Bit-Line Clamping Circuit To Improve Write Performance Of Dual-Port SRAM	Issued	Lattice Semiconductor Corporation
13/275,102	8169237	United States	High Speed Comparator with Data Dependent Jitter Mitigation	Issued	Lattice Semiconductor Corporation
13/299,507	8370691	United States	Testing of Soft Error Detection Logic For PLDs	Issued	Lattice Semiconductor Corporation
13/452,060	8823561	United States	In-System Reconfigurable Circuit For Mapping Data Words Of Different Lengths	Issued	Lattice Semiconductor Corporation
13/585,142	8461894	United States	Low Power And Glitch-less Delay Element For High Speed Receiver Interface	Issued	Lattice Semiconductor Corporation
13/616,173	8912933	United States	Low Power SerDes With Built- In Word Alignment For Odd And Even Gearing Ratios	Issued	Lattice Semiconductor Corporation
13/653,827	8710898	United States	Bandgap Reference Circuit Design With Triple-Trim Methodology For Mass Production	Issued	Lattice Semiconductor Corporation
13/680,947	8643398	United States	Placing ICs Into Low Voltage Mode For Standby Purposes	Issued	Lattice Semiconductor Corporation
13/685,385	8643168	United States	Input Capacitance Compensation In Package	Issued	Lattice Semiconductor Corporation
13/721,867	8686773	United States	In-System Margin Measurement Circuit	Issued	Lattice Semiconductor Corporation
13/738,265	8797064	United States	Low power, optimized H-bridge and CML driver	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
13/764,221	RE45200	United States	Programmable Signal Routing Systems Having Low Static Leakage	Issued	Lattice Semiconductor Corporation
13/857,919	8786482	United States	Analog-To-Digital-Converter	Issued	Lattice Semiconductor Corporation
13/892,948	8648636	United States	Method of Delaying Data from Clock in 1UI steps	Issued	Lattice Semiconductor Corporation
14/040,955	8829944	United States	Dynamic Power Supply Switching For Clock Signals	Issued	Lattice Semiconductor Corporation
13/155,261		United States	JTAG Based Parallel Measuring And Trimming for Time Based Parameters	Pending	Lattice Semiconductor Corporation
13/412,408		United States	Double Rate Throughput Processing Booster For DSP Slices	Pending	Lattice Semiconductor Corporation
13/466,463		United States	Early Match FIFO	Pending	Lattice Semiconductor Corporation
13/681,782		United States	Multi-channel transmitter synchronization circuitry	Pending	Lattice Semiconductor Corporation
13/777,243		United States	RAM Data Path Sense Leakage Abatement Circuit	Pending	Lattice Semiconductor Corporation
13/858,422		United States	Method To Enable And Disable Scan Test Mode Reliably Through JTAG Port With Maximum Scan Coverage	Pending	Lattice Semiconductor Corporation
13/868,738		United States	Loss of signal detection in high-speed serial link	Pending	Lattice Semiconductor Corporation
13/901,853		United States	Dual-Port SRAM With Bit Line Clamping	Pending	Lattice Semiconductor Corporation
13/904,861		United States	Bring up sequence for configurable PCIe IP in an	Pending	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 94

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			FPGA		Corporation
13/947,553		United States	Method For Hot Swapping Or Hot Plugging With Stable Supply-Side Reference Over Wide Voltage Range	Pending	Lattice Semiconductor Corporation
14/021,513		United States	Phase Locked Loop Circuit With Selectable Feedback Paths	Pending	Lattice Semiconductor Corporation
14/043,920		United States	Robust Serialized State-machine Interface Architecture Optimized for Implementation in Programmable Devices	Pending	Lattice Semiconductor Corporation
14/053,026		United States	ASB SW modeling methodology	Pending	Lattice Semiconductor Corporation
14/070,975		United States	Method to enable system board pin escape for tight ball pitch packages	Pending	Lattice Semiconductor Corporation
14/095,310		United States	A Novel ESD Implementation for 40nm FPGA	Pending	Lattice Semiconductor Corporation
14/136,482		United States	Automatic Quadrant Clock Assignment For Programmable Logic Devices	Pending	Lattice Semiconductor Corporation
14/137,443		United States	Using Critical Groups in FPGA Routing	Pending	Lattice Semiconductor Corporation
14/147,796		United States	A Hot Socket Implementation for General Purpose IO for 40nm FPGA	Pending	Lattice Semiconductor Corporation
14/172,678		United States	All Mosfet Circuit for Generating Accurate Collector Currents	Pending	Lattice Semiconductor Corporation
14/179,651		United States	LOW-VOLTAGE CURRENT SENSE AMPLIFIER	Pending	Lattice Semiconductor Corporation
14/194,484		United States	Logic Element Placement with Repacking Optimization	Pending	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 95

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/220,377		United States	DPHY using FPGA differential & single ended I/Os	Pending	Lattice Semiconductor Corporation
14/223,096		United States	DPHY using FPGA differential & single ended I/Os	Pending	Lattice Semiconductor Corporation
14/245,920		United States	Deterministic Dynamic Element Matching for Generating Precise Current Ratios	Pending	Lattice Semiconductor Corporation
14/271,331		United States	Inline Defect To Sort Test Correlation In Semiconductor Manufacturing	Pending	Lattice Semiconductor Corporation
14/271,955		United States	Performance-focused Adaptive Automatic Incremental Flow	Pending	Lattice Semiconductor Corporation
14/283,329		United States	Configuration logic controlled memory BIST (built-in self-test) for back-to-back initialization and readback of embedded block RAMs in FPGAs	Pending	Lattice Semiconductor Corporation
14/308,747		United States	A novel Output Driver drive strength and termination resistor continuously calibrating PVT compensation scheme	Pending	Lattice Semiconductor Corporation
14/313,443		United States	FPGA Hardware debug during post-config power-up and before logic analyzer connect	Pending	Lattice Semiconductor Corporation
14/313,778		United States	IOLOGIC Delay Cell Stealing for Holdtime Correction	Pending	Lattice Semiconductor Corporation
14/316,049		United States	Mapping Constant Multipliers To ICE Devices	Pending	Lattice Semiconductor Corporation
14/319,481		United States	Incrementer Absorption into Multiplier Logic	Pending	Lattice Semiconductor Corporation
14/320,169		United States	Method to Implement Mixed-	Pending	Lattice

DELL/HP/LENOVO EXHIBIT 1002
Page 96

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Width Mode Memory in Fixed-Mode Memory Architecture with Masking		Semiconductor Corporation
14/320,074		United States	Two Level Voltage Regulator scheme for SRAM Operation	Pending	Lattice Semiconductor Corporation
14/327,811		United States	Implementing Dual Boot For XO2 and Multiple ASCs	Pending	Lattice Semiconductor Corporation
14/339,164		United States	A unique method to optimize clock to out path	Pending	Lattice Semiconductor Corporation
14/339,229		United States	New method on bus-based clock_to_out timing optimization	Pending	Lattice Semiconductor Corporation
14/482,001		United States	Physically-aware Programmable Multiport Memory BIST with on-the-fly ATE-configurable memory tests	Pending	Lattice Semiconductor Corporation
14/509,564		United States	Dont-care based mux absorption into ice40 carry chain	Pending	Lattice Semiconductor Corporation
14/525,240		United States	Level shifter that eliminates static power dissipation	Pending	Lattice Semiconductor Corporation
14/535,454		United States	Low power and high performance class AB amplifier control common mode in SerDes Transmitter	Pending	Lattice Semiconductor Corporation
14/535,351		United States	ICO metastability prevention during start-up	Pending	Lattice Semiconductor Corporation
14/558,851		United States	Low Power and Flexible TX FFE With Programmable Tap Positions And Coefficients Driver Architecture	Pending	Lattice Semiconductor Corporation
14/576,348		United States	Reconfigurable and Scalable Hardware Management Architecture	Pending	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 97

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/576,245		United States	Methodology that allows multiple hardware or hardware-software controllers with different bus interfaces to share a common resource	Pending	Lattice Semiconductor Corporation
14/604,515		United States	Enhancement of FPGA hardware debugger to be used as a design controller/exerciser with user registers	Pending	Lattice Semiconductor Corporation
14/609,181		United States	Algorithm to Optimize Hot Swapping	Pending	Lattice Semiconductor Corporation
14/610,074		United States	Ripple Mode using 3-LUT for Generate	Pending	Lattice Semiconductor Corporation
14/610,127		United States	Combine OFX with LUT output and SUM into a single output to reduce number of signals to routing block	Pending	Lattice Semiconductor Corporation
14/611,069		United States	High speed complementary NMOS LUT logic	Pending	Lattice Semiconductor Corporation
14/611,095		United States	Shared Logic for Multiple Registers with asynchronous initialization with preload	Pending	Lattice Semiconductor Corporation
11/949,454	7,427,874	United States	Interface block architectures	Issued	Lattice Semiconductor Corporation
11/676,196	7,327,160	United States	SERDES with programmable I/O architecture	Issued	Lattice Semiconductor Corporation
6,786,564	6,786,564	United States	Inkjet printer, drive method and drive device for same	Issued	Lattice Semiconductor Corporation
11/839,107	7,856,050	United States	Receiver and transmitter calibration to compensate for frequency dependent I/Q imbalance	Issued	Lattice Semiconductor Corporation
07/679,370	5,255,221	United States	Fully configurable versatile field programmable function	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 98

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			element		Corporation
06/551,735	4,642,797	United States	High speed first-in-first-out memory	Issued	Lattice Semiconductor Corporation
08/042,533	5,394,037	United States	Sense amplifiers and sensing methods	Issued	Lattice Semiconductor Corporation
08/115,533	5,404,055	United States	Input routing pool	Issued	Lattice Semiconductor Corporation
08/115,723	5,394,033	United States	Structure and method for implementing hierarchical routing pools in a programmable logic circuit	Issued	Lattice Semiconductor Corporation
08/342,675	5,506,517	United States	Output enable structure and method for a programmable logic device	Issued	Lattice Semiconductor Corporation
07/911,841	5,357,156	United States	Active clamp circuit scheme for CMOS devices	Issued	Lattice Semiconductor Corporation
08/179,887	5,886,378	United States	Single polysilicon layer flash E.sup.2 PROM cell	Issued	Lattice Semiconductor Corporation
07/853,453	5,231,316	United States	Temperature compensated CMOS voltage to current converter	Issued	Lattice Semiconductor Corporation
08/108,363	5,353,246	United States	Programmable semiconductor antifuse structure and method of fabricating	Issued	Lattice Semiconductor Corporation
07/785,442	5,281,906	United States	Tunable voltage reference circuit to provide an output voltage with a predetermined temperature coefficient independent of variation in supply voltage	Issued	Lattice Semiconductor Corporation
07/696,453	5,251,169	United States	Non-volatile erasable and programmable interconnect cell	Issued	Lattice Semiconductor Corporation
07/538,211	5,255,203	United States	Interconnect structure for programmable logic device	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 99

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
08/106,263	5,412,260	United States	Multiplexed control pins for in-system programming and boundary scan state machines in a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/033,934	5,418,390	United States	Single polysilicon layer E.sup.2 PROM cell	Issued	Lattice Semiconductor Corporation
07/993,711	5,452,229	United States	Programmable integrated-circuit switch	Issued	Lattice Semiconductor Corporation
07/957,311	5,329,179	United States	Arrangement for parallel programming of in-system programmable IC logical devices	Issued	Lattice Semiconductor Corporation
07/288,945	4,896,296	United States	Programmable logic device configurable input/output cell	Issued	Lattice Semiconductor Corporation
06/882,602	4,887,239	United States	One-time programmable data security system for programmable logic device	Issued	Lattice Semiconductor Corporation
06/871,063	4,766,569	United States	Programmable logic array	Issued	Lattice Semiconductor Corporation
06/862,815	4,879,688	United States	In-system programmable logic device	Issued	Lattice Semiconductor Corporation
06/707,670	4,833,646	United States	Programmable logic device with limited sense currents and noise reduction	Issued	Lattice Semiconductor Corporation
07/236,348	4,852,044	United States	Programmable data security circuit for programmable logic device	Issued	Lattice Semiconductor Corporation
11/400,924	7411424	United States	Programmable logic function generator using non-volatile programmable memory switches	Issued	Lattice Semiconductor Corporation
13/403,146		United States	Surface Mountable Integrated Circuit Packaging Scheme	Pending	SiBEAM, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/242,665		United States	High Speed Integrated Circuit Interface	Pending	SiBEAM, Inc.
14/196,978		United States	Calibration of Single-Ended High-Speed Interfaces	Pending	Silicon Image, Inc.
14/474,005		United States	Inter-Device Conflict Resolution on a Multimedia Link	Pending	Silicon Image, Inc.
61/989,417		United States	Control Target Selection	Pending	Silicon Image, Inc.
61/988,812		United States	Lip Sync Delay Compensation	Pending	Silicon Image, Inc.
61/989,415		United States	Streaming Data and Metadata Synchronization	Pending	Silicon Image, Inc.
61/991,126		United States	Stream Creation with Limited Topology Information	Pending	Silicon Image, Inc.
61/989,411		United States	Topology Discovery	Pending	Silicon Image, Inc.
14/463,146		United States	Radio Frequency Interference Reduction In Multimedia Interfaces	Pending	Silicon Image, Inc.
14/578,266		United States	Control Target Selection	Pending	Silicon Image, Inc.
14/578,257		United States	System for Dynamic Audio Visual Capabilities Exchange	Pending	Silicon Image, Inc.
62/089,767		United States	High-Bandwidth Digital Content Protection over Audio Return Channel	Pending	Silicon Image, Inc.
12/573,492	8482462	United States	MULTI-ANTENNA BEAM-FORMING SYSTEM FOR TRANSMITTING CONSTANT ENVELOPE SIGNALS DECOMPOSED FROM A VARIABLE ENVELOPE SIGNAL	Issued	Silicon Image, Inc.
12/678,463	8207892	United States	TECHNIQUE FOR DETERMINING AN ANGLE OF ARRIVAL IN A COMMUNICATION SYSTEM	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/675,269	8374558	United States	ANTENNA ARRAY WITH FLEXIBLE INTERCONNECT FOR A MOBILE WIRELESS DEVICE	Issued	Silicon Image, Inc.
12/333,134	8213872	United States	TECHNIQUE FOR LOW-POWER OPERATION OF A WIRELESS DEVICE	Issued	Silicon Image, Inc.
12/933,876	8256123	United States	DISPLACEMENT SENSING USING A FLEXIBLE SUBSTRATE	Issued	Silicon Image, Inc.
14/196,993		United States	Calibration of Single-Ended High-Speed Interfaces	Pending	Silicon Image, Inc.
13/988,047		United States	INTEGRATED PHASE-SHIFTING-AND-COMBINING CIRCUITRY TO SUPPORT MULTIPLE ANTENNAS	Pending	Silicon Image, Inc.
14/002,353		United States	TRACKING SYSTEM WITH ORTHOGONAL POLARIZATIONS AND A RETRO-DIRECTIVE ARRAY	Pending	Silicon Image, Inc.
13/726,822		United States	HIGH-ACCURACY DETECTION IN COLLABORATIVE TRACKING SYSTEMS	Pending	Silicon Image, Inc.
13/859,764		United States	ANTENNA SELECTION AND PILOT COMPRESSION IN MIMO SYSTEMS	Pending	Silicon Image, Inc.
62/100,841		United States	I/Q Imbalance Correction for the Combination of Multiple Radio Frequency Frontends	Pending	Silicon Image, Inc.
12/532,107	8571126	United States	MULTI-ANTENNA TRANSMITTER FOR MULTI-TONE SIGNALING	Issued	Silicon Image, Inc.
14/065,420		United States	MULTI-ANTENNA TRANSMITTER FOR MULTI-TONE SIGNALING	Pending	Silicon Image, Inc.
12/679,764	8605823	United States	COMMUNICATION USING	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			CONTINUOUS-PHASE MODULATED SIGNALS		Inc.
14/101,274		United States	COMMUNICATION USING CONTINUOUS-PHASE MODULATED SIGNALS	Pending	Silicon Image, Inc.
12/746,526	8484277	United States	TRANSFORMING SIGNALS USING PASSIVE CIRCUITS	Issued	Silicon Image, Inc.
13/498,884	8610474	United States	SIGNAL DISTRIBUTION NETWORKS AND RELATED MET	Issued	Silicon Image, Inc.
14/089,094		United States	SIGNAL DISTRIBUTION NETWORKS AND RELATED METHODS	Pending	Silicon Image, Inc.
13/519,302		United States	Phase Detection Circuits and Methods	Pending	Silicon Image, Inc.
13/574,586	8795082	United States	DIRECTIONAL BEAM STEERING SYSTEM AND METHOD TO DETECT LOCATION AND MOTION	Issued	Silicon Image, Inc.
14/331,144		United States	DIRECTIONAL BEAM STEERING SYSTEM AND METHOD TO DETECT LOCATION AND MOTION	Pending	Silicon Image, Inc.
13/704,564		United States	Methods and Systems for Near-Field MIMO Communications	Pending	Silicon Image, Inc.
14/235,783		United States	HIGH-ACCURACY AND LOW-POWER TRACKING SYSTEM FOR MOBILE DEVICES	Pending	Silicon Image, Inc.
14/234,623		United States	LOW-COST TRACKING SYSTEM	Pending	Silicon Image, Inc.
14/240,405		United States	CALIBRATING A RETRO-DIRECTIVE ARRAY FOR AN ASYMMETRIC WIRELESS LINK	Pending	Silicon Image, Inc.
14/364,002		United States	COLLABORATIVE CHANNEL SOUNDING IN MULTI-ANTENNA	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			SYSTEMS		
08/815,486	6,157,360	United States	System And Method For Driving Columns Of An Active Matrix Display	Issued	Silicon Image, Inc.
08/920,336	5,955,929	United States	Voltage-Controlled Oscillator Resistant To Supply Voltage Noise	Issued	Silicon Image, Inc.
09/007,707	5,969,552	United States	Dual Loop Delay-Locked Loop	Issued	Silicon Image, Inc.
09/298,647	6,259,427	United States	Scaling Multi-Dimensional Signals Using Variable Weighting Factors	Issued	Silicon Image, Inc.
09/298,369	6,374,361	United States	Skew-Insensitive Low Voltage Differential Receiver	Issued	Silicon Image, Inc.
09/393,849	6,738,417	United States	Method And Apparatus For Bidirectional Data Transfer Between A Digital Display And A Computer	Issued	Silicon Image, Inc.
09/326,503	6,940,496	United States	Display Module Driving System And Digital To Analog Converter For Driving Display	Issued	Silicon Image, Inc.
09/392,229	6,564,269	United States	Bi-Directional Data Transfer Using The Video Blanking Period In A Digital Data Stream	Issued	Silicon Image, Inc.
09/393,234	6,307,543	United States	Bi-Directional Data Transfer Using Two Pair Of Differential Lines As A Single Additional Differential Pair	Issued	Silicon Image, Inc.
09/947,008	6,492,984	United States	Bi-Directional Data Transfer Using Two Pair Of Differential Lines As A Single Additional Differential Pair	Issued	Silicon Image, Inc.
09/759,624	6,891,910	United States	Baud-Rate Timing Recovery	Issued	Silicon Image, Inc.
09/574,571	6,326,826	United States	Wide Frequency-Range Delay- Locked Loop Circuit	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/881,271	6,954,491	United States	Methods And Systems For Sending Side-Channel Data During Data Inactive Period	Issued	Silicon Image, Inc.
09/922,990	6,961,095	United States	Digital Display Jitter Correction Apparatus And Method	Issued	Silicon Image, Inc.
11/219,323	7,557,863	United States	Digital Display Jitter Correction Apparatus And Method	Issued	Silicon Image, Inc.
09/989,587	6,717,478	United States	Multi-Phase Voltage Controlled Oscillator (VCO) With Common Mode Control	Issued	Silicon Image, Inc.
10/371,220	7,231,009	United States	Data Synchronization Across An Asynchronous Boundary Using, For Example, Multi-Phase Clocks	Issued	Silicon Image, Inc.
09/989,580	7,103,013	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
11/441,669	7,599,316	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
12/573,847	8,116,240	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
10/045,297	7,257,129	United States	Memory Architecture With Multiple Serial Communications Ports	Issued	Silicon Image, Inc.
11/828,286	7,903,684	United States	Communications Architecture For Transmission Of Data Between Memory Bank Caches And Ports	Issued	Silicon Image, Inc.
09/167,527	6,380,978	United States	Digital Video System And Methods For Providing Same	Issued	DVDO, INC. and Silicon Image, Inc.
10/032,136	7,215,376	United States	Digital Video System And Methods For Providing Same	Issued	DVDO, INC. and Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/942,740	7,359,624	United States	Portable DVD Player	Issued	Silicon Image, Inc.
09/372,713	6,489,998	United States	Method And Apparatus For Deinterlacing Digital Video	Issued	Silicon Image, Inc.
09/941,949	6,909,469	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
10/251,642	7,027,099	United States	Method And Apparatus For Deinterlacing Digital Video Images	Issued	Silicon Image, Inc.
11/054,748	7,391,481	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
11/357,364	7,499,103	United States	Method And Apparatus For Detecting Frequency In Digital Video Images	Issued	Silicon Image, Inc.
11/932,808	7,633,559	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
09/410,543	6,700,622	United States	Method And Apparatus For Detecting The Source Format Of Video Images	Issued	Silicon Image, Inc.
09/396,993	6,515,706	United States	Method And Apparatus For Detecting And Smoothing Diagonal Features In Video Images	Issued	Silicon Image, Inc.
10/191,764	6,829,013	United States	Method And Apparatus For Detecting And Smoothing Diagonal Features In Video Images	Issued	Silicon Image, Inc.
09/363,312	6,681,059	United States	Method And Apparatus For Efficient Video Scaling	Issued	Silicon Image, Inc.
09/359,530	6,587,158	United States	Method And Apparatus For Reducing On-Chip Memory In Vertical Video Processing	Issued	Silicon Image, Inc.
09/226,776	6,219,747	United States	Methods And Apparatus For Variable Length SDRAM	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Transfers		
09/805,588	6,385,692	United States	Methods and Apparatus for Variable Length SDRAM Transfers	Issued	Silicon Image, Inc.
09/227,502	6,393,505	United States	Methods And Apparatus For Data Bus Arbitration	Issued	Silicon Image, Inc.
09/226,381	6,473,476	United States	Method And Apparatus For Providing Deterministic Resets For Clock Divider Systems	Issued	Silicon Image, Inc.
09/837,894	6,867,814	United States	Method, System And Article Of Manufacture For Identifying The Source Type And Quality Level Of A Video Sequence	Issued	Silicon Image, Inc.
09/478,122	7,203,557	United States	Audio Signal Delay Apparatus And Method	Issued	Silicon Image, Inc.
10/663,413	7,408,992	United States	Detection And Repair Of MPEG-2 Chroma Upconversion Artifacts	Issued	Silicon Image, Inc.
09/905,318	7,123,307	United States	Clock Jitter Limiting Scheme In Video Transmission Through Multiple Stages	Issued	Silicon Image, Inc.
09/905,615	6,944,804	United States	System And Method For Measuring Pseudo Pixel Error Rate	Issued	Silicon Image, Inc.
09/904,783	6,625,560	United States	Method Of Testing Serial Interface	Issued	Silicon Image, Inc.
09/989,590	6,845,461	United States	High-Speed Bus With Embedded Clock Signals	Issued	Silicon Image, Inc.
09/989,645	6,809,567	United States	System And Method For Multiple-Phase Clock Generation	Issued	Silicon Image, Inc.
09/905,511	7,062,004	United States	Method And Apparatus For Adaptive Control Of PLL Loop Bandwidth	Issued	Silicon Image, Inc.
10/057,823	7,023,487	United States	Deinterlacing Of Video Sources Via Image Feature Edge Detection	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/954,663	7,558,326	United States	Method And Apparatus For Sending Auxiliary Data On A TMDS-Like Link	Issued	Silicon Image, Inc.
10/036,234	7,359,437	United States	Encoding Method And System For Reducing Inter-Symbol Interference Effects In Transmission Over A Serial Link	Issued	Silicon Image, Inc.
10/095,422	7,257,163	United States	Method And System For Reducing Inter-Symbol Interference Effects In Transmission Over A Serial Link With Mapping Of Each Word In A Cluster Of Received Words To A Single Transmitted Word	Issued	Silicon Image, Inc.
10/171,860	7,088,398	United States	Method And Apparatus For Regenerating A Clock For Auxiliary Data Transmitted Over A Serial Link With Video Data	Issued	Silicon Image, Inc.
10/192,296	6,914,637	United States	Method And System For Video And Auxiliary Data Transmission Over A Serial Link	Issued	Silicon Image, Inc.
10/357,750	7,283,566	United States	Method And Circuit For Generating Time Stamp Data From An Embedded-Clock Audio Data Stream And A Video Clock	Issued	Silicon Image, Inc.
10/016,247	6,714,206	United States	Method And System For Spatial-Temporal Dithering For Displays With Overlapping Pixels	Issued	Silicon Image, Inc.
10/133,813	7,136,484	United States	Cryptosystems Using Commuting Pairs In A Monoid	Issued	Silicon Image, Inc.
10/047,772	7,109,958	United States	Supporting Circuitry And Method For Controlling Pixels	Issued	Silicon Image, Inc.
10/045,393	7,039,121	United States	Method And System For Transition-Controlled Selective Block Inversion	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Communications		
08/656,032	6,018,456	United States	Enclosure For Removable Computer Peripheral Equipment	Issued	CMD Technology Inc. and Silicon Image, Inc.
08/906,775	5,991,546	United States	System And Method For Interfacing Manually Controllable Input Devices To A Universal Computer Bus System	Issued	CMD Technology Inc. and Silicon Image, Inc.
10/171,820	7,225,282	United States	Method And Apparatus For A Two-Wire Serial Command Bus Interface	Issued	Silicon Image, Inc.
11/713,241	7,441,065	United States	Adaptive Beam-Steering Methods To Maximize Wireless Link Budget And Reduce Delay-Spread Using Multiple Transmit And Receive Antennas	Issued	Silicon Image, Inc.
10/210,839	7,171,525	United States	Method And System For Arbitrating Priority Bids Sent Over Serial Links To A Multi-Port Storage Device	Issued	Silicon Image, Inc.
09/688,536	6,380,783	United States	Cyclic Phase Signal Generation From A Single Clock Source Using Current Phase Interpolation	Issued	Silicon Image, Inc.
09/847,837	6,535,029	United States	Fully Differential Continuous-Time Current-Mode High Speed CMOS Comparator	Issued	Silicon Image, Inc.
10/270,882	7,009,827	United States	Voltage Swing Detection Circuit For Hot Plug Event Or Device Detection Via A Differential Link	Issued	Silicon Image, Inc.
10/162,046	6,843,674	United States	Method And Apparatus For Connecting Serial ATA Storage Components	Issued	Silicon Image, Inc.
09/945,278	7,131,004	United States	Method And Apparatus For Encrypting Data Transmitted Over A Serial Link	Issued	Silicon Image, Inc.
11/499,124	7,900,047	United States	Method And Apparatus For Encrypting Data Transmitted	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Over A Serial Link		Inc.
11/543,501	7,757,085	United States	Method And Apparatus For Encrypting Data Transmitted Over A Serial Link	Issued	Silicon Image, Inc.
10/224,995	7,218,737	United States	System And Method For An Adaptive State Machine To Control Signal Filtering In A Serial Link	Issued	Silicon Image, Inc.
09/991,057	7,242,766	United States	Method And System For Encrypting And Decrypting Data Using An External Agent	Issued	Silicon Image, Inc.
10/085,177	7,035,290	United States	Method And System For Temporary Interruption Of Video Data Transmission	Issued	Silicon Image, Inc.
10/036,794	6,976,201	United States	Method And System For Host Handling Of Communications Errors	Issued	Silicon Image, Inc.
10/053,461	7,113,507	United States	Method And System For Communicating Control Information Via Out-Of-Band Symbols	Issued	Silicon Image, Inc.
10/045,625	7,746,798	United States	Method And System For Integrating Packet Type Information With Synchronization Symbols	Issued	Silicon Image, Inc.
10/035,911	7,154,905	United States	Method And System For Nesting Of Communications Packets	Issued	Silicon Image, Inc.
10/045,600	6,771,192	United States	Method And System For DC-Balancing At The Physical Layer	Issued	Silicon Image, Inc.
10/045,601	7,340,558	United States	Multisection Memory Bank System	Issued	Silicon Image, Inc.
09/989,647	7,058,121	United States	Logic Gates Including Diode-Connected Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) To Control Input Threshold Voltage Levels And Switching Transients Of	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Output Logic Signals		
09/989,487	6,985,005	United States	Differential Amplifiers Using Asymmetric Transfer Characteristics To Suppress Input Noise In Output Logic Signals	Issued	Silicon Image, Inc.
11/330,047	7,456,648	United States	Differential Amplifiers Using Asymmetric Transfer Characteristics To Suppress Input Noise In Output Logic Signals	Issued	Silicon Image, Inc.
12/275,686	7,847,583	United States	Transmitter And Receiver Using Asymmetric Transfer Characteristics In Differential Amplifiers To Suppress Noise	Issued	Silicon Image, Inc.
10/403,477	6,819,166	United States	Continuous-Time, Low-Frequency-Gain/High-Frequency-Boosting	Issued	Silicon Image, Inc.
10/417,712	7,348,991	United States	Video Graphics Text Mode Enhancement Method For Digitally Processed Data	Issued	Silicon Image, Inc.
10/287,976	6,873,341	United States	Detection Of Video Windows And Graphics Windows	Issued	Silicon Image, Inc.
10/298,722	7,539,304	United States	Integrated Circuit Having Self Test Capability Using Message Digest And Method For Testing Integrated Circuit Having Message Digest Generation Circuitry	Issued	Silicon Image, Inc.
10/215,936	6,717,468	United States	Dynamically Biased Full-Swing Operation Amplifier For An Active Matrix Liquid Crystal Display Driver	Issued	Silicon Image, Inc.
10/268,832	7,412,053	United States	Cryptographic Device With Stored Key Data And Method For Using Stored Key Data To Perform An Authentication Exchange Of Self Test	Issued	Silicon Image, Inc.
11/950,088	7,797,536	United States	Cryptographic Device With Stored Key Data And Method	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			For Using Stored Key Data To Perform An Authentication Exchange Of Self Test		
10/244,152	6,814,583	United States	Through-Broad PCB Edge Connector, System And Method	Issued	Silicon Image, Inc.
10/247,675	8,064,508	United States	Equalizer With Controllably Weighted Parallel High Pass And Low Pass Filters And Receiver Including Such An Equalizer	Issued	Silicon Image, Inc.
11/796,175	8,275,026	United States	Equalizer With Controllably Weighted Parallel High Pass And Low Pass Filters And Receiver Including Such An Equalizer	Issued	Silicon Image, Inc.
10/651,500	7,551,909	United States	CMOS Transceiver With Dual Current Path VCO	Issued	Silicon Image, Inc.
10/099,533	7,158,593	United States	Combining A Clock Signal And A Data Signal	Issued	Silicon Image, Inc.
10/642,259	7,409,031	United States	Data Sampling Method And Apparatus With Alternating Edge Sampling Phase Detection For Loop Characteristic Stabilization	Issued	Silicon Image, Inc.
10/459,989	7,187,307	United States	Method And System For Encapsulation Of Multiple Levels Of Communication Protocol Functionality Within Line Codes	Issued	Silicon Image, Inc.
10/794,015	7,502,411	United States	Method And Circuit For Adaptive Equalization Of Multiple Signals In Response To A Control Signal Generated From One Of The Equalized Signals	Issued	Silicon Image, Inc.
10/459,992	6,747,580	United States	Method And Apparatus For Encoding Or Decoding Data In Accordance With An Nb/(N+1)B Block Code, And Method For Determining Such A Block Code	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/781,405	7,269,673	United States	Cable With Circuitry For Asserting Stored Cable Data Or Other Information To An External Device Or User	Issued	Silicon Image, Inc.
11/848,758	7,500,032	United States	Cable With Circuitry For Asserting Stored Cable Data Or Other Information To An External Device Or User	Issued	Silicon Image, Inc.
11/123,353	7,375,960	United States	Apparatus For Removably Securing Storage Components In An Enclosure	Issued	Silicon Image, Inc.
10/763,905	7,236,553	United States	Reduced Dead-Cycle, Adaptive Phase Tracking Method And Apparatus	Issued	Silicon Image, Inc.
10/835,301	6,897,793	United States	Method And Apparatus For Run Length Limited TMDS-Like Encoding Of Data	Issued	Silicon Image, Inc.
10/842,231	7,991,096	United States	Data Sampling Method And Apparatus Using Through-Transition Counts To Reject Worst Sampling Position	Issued	Silicon Image, Inc.
10/439,446	7,031,858	United States	Method And Circuit For DC Measurement Of Phase Uniformity Of Multi-Phase Clocks	Issued	Silicon Image, Inc.
10/302,436	7,274,690	United States	An Age Selection Switching Scheme For Data Traffic In A Crossbar Switch	Issued	Silicon Image, Inc.
10/645,786	7,505,422	United States	Preference Programmable First-One Detector And Quadrature Based Random Grant Generator	Issued	Silicon Image, Inc.
10/645,787	7,461,167	United States	A Method For Multicast Service In A Crossbar Switch	Issued	Silicon Image, Inc.
10/762,950	7,352,764	United States	Content Addressable Merged Queue Architecture For Switching Data	Issued	Silicon Image, Inc.
10/434,785	7,519,066	United States	A Method For Switching Data In A Crossbar Switch	Issued	Silicon Image, Inc.
11/372,866	7,694,204	United States	Error Detection In Physical	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Interfaces For Point-To-Point Communications Between Integrated Circuits		Inc.
12/712,124	7,937,644	United States	Error Detection In Physical Interfaces For Point-To-Point Communications Between Integrated Circuits	Issued	Silicon Image, Inc.
13/099,254	8,099,648	United States	Error Detection In Physical Interfaces For Point-To-Point Communications Between Integrated Circuits	Issued	Silicon Image, Inc.
11/669,416	7,844,762	United States	Parallel Interface Bus To Communicate Video Data Encoded For Serial Data Links	Issued	Silicon Image, Inc.
11/056,995	7,102,446	United States	Phase Lock Loop With Coarse Control Loop Having Frequency Lock Detector And Device Including Same	Issued	Silicon Image, Inc.
11/643,388	7,589,559	United States	Current Mode Circuitry To Modulate A Common Mode Voltage	Issued	Silicon Image, Inc.
12/555,300	7,872,498	United States	Current Mode Circuitry to Modulate a Common Mode Voltage	Issued	Silicon Image, Inc.
11/477,049	7,793,179	United States	Test Clock Control Structures To Generate Configurable Test Clocks For Scan-Based Testing Of Electronic Circuits Using Programmable Test Clock Controllers	Issued	Silicon Image, Inc.
11/856,640	7,782,934	United States	Parameter Scanning For Signal Over-Sampling	Issued	Silicon Image, Inc.
11/592,792	7,450,038	United States	Determining Oversampled Data To Be Included In Unit Intervals	Issued	Silicon Image, Inc.
11/510,254	8,595,434	United States	Smart Scalable Storage Switch Architecture	Issued	Silicon Image, Inc.
14/067,363		United States	Smart Scalable Storage Switch Architecture	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/314,162	7,571,269	United States	A Covert Channel For Conveying Supplemental Messages In A Protocol-Defined Link For A System Of Storage Devices	Issued	Silicon Image, Inc.
11/637,254	7,602,253	United States	Adaptive Bandwidth Phase Locked Loop With Feedforward Divider	Issued	Silicon Image, Inc.
11/656,331	7,984,369	United States	Concurrent Code Checker And Hardware Efficient High-Speed I/O Having Built-In Self-Test And Debug Features	Issued	Silicon Image, Inc.
11/694,819	7,949,863	United States	Multi-Port Memory Device Having Variable Port Speeds	Issued	Silicon Image, Inc.
11/694,813	7,639,561	United States	Power-Saving Clocking Technique	Issued	Silicon Image, Inc.
11/690,629	7,831,778	United States	Mechanism For Streaming Media Data Over Wideband Wireless Networks	Issued	Silicon Image, Inc.
11/476,457	7,840,861	United States	Scan-Based Testing Of Devices Implementing A Test Clock Control Structure (â€œTCCSâ€)	Issued	Silicon Image, Inc.
11/861,175	8,160,192	United States	Signal Interleaving for Serial Clock and Data Recovery	Issued	Silicon Image, Inc.
11/690,642	7,908,501	United States	Shared Nonvolatile Memory Architecture	Issued	Silicon Image, Inc.
11/742,358	7,698,088	United States	Interface Test Circuitry And Methods	Issued	Silicon Image, Inc.
11/848,641	8,233,432	United States	Ensuring Physical Locality Of Entities Sharing Data	Issued	Silicon Image, Inc.
11/683,608	7,831,877	United States	Method And Apparatus For A Two-Wire Serial Command Bus Interface	Issued	Silicon Image, Inc.
11/690,659	7,849,339	United States	Progressive Power Control Of A Multi-Port Memory Device	Issued	Silicon Image, Inc.
11/567,514	7,365,659	United States	Method Of Context Adaptive Binary Arithmetic Coding	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			And Coding Apparatus Using The Same		
12/778,882		United States	Multi-Level Port Expansion For Port Multipliers	Pending	Silicon Image, Inc.
12/147,248	7,836,223	United States	Operation Of Media Interface To Provide Bidirectional Communications	Issued	Silicon Image, Inc.
11/849,163	8,695,034	United States	Delivering On Screen Display Data To Existing Display Devices	Issued	Silicon Image, Inc.
11/828,219	8,599,315	United States	On Screen Displays Associated With Remote Video Source Devices	Issued	Silicon Image, Inc.
14/070,373		United States	On Screen Displays Associated With Remote Video Source Devices	Pending	Silicon Image, Inc.
11/829,800	7,903,550	United States	Bandwidth Reservation For Data Flows In Interconnection Networks	Issued	Silicon Image, Inc.
11/828,223	8,149,711	United States	Data Stream Control For Network Devices	Issued	Silicon Image, Inc.
13/541,390	8,924,509	United States	Automated Service Discovery And Dynamic Connection Management	Issued	Silicon Image, Inc.
11/836,082	8,468,212	United States	Network Repository For Metadata	Issued	Silicon Image, Inc.
13/919,773		United States	Network Repository For Metadata	Pending	Silicon Image, Inc.
11/829,790	7,911,956	United States	Packet Level Prioritization In Interconnection Networks	Issued	Silicon Image, Inc.
11/828,226		United States	Streaming Data Content In A Network	Pending	Silicon Image, Inc.
11/848,153	7,936,790	United States	Synchronizing Related Data Streams In Interconnection Networks	Issued	Silicon Image, Inc.
11/952,052	8,001,334	United States	Bank Sharing And Refresh In A Shared Multi-Port Memory Device	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/075,954	7,979,589	United States	Method, Apparatus, And System For Port Multiplier Enhancement	Issued	Silicon Image, Inc.
13/298,001		United States	Iddq Testing Of CMOS Devices	Pending	Silicon Image, Inc.
10/788,704	6,944,086	United States	Semiconductor Memory Device	Issued	Silicon Image, Inc.
10/876,231	7,016,255	United States	Multi-Port Memory Device	Issued	Silicon Image, Inc.
10/877,318	7,089,465	United States	Multi-Port Memory Device Having Serial I/O Interface	Issued	Silicon Image, Inc.
12/075,906	7,904,566	United States	Method, Apparatus, And System For Employing An Enhanced Port Multiplier	Issued	Silicon Image, Inc.
12/497,391	8,386,867	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
13/776,508	8,667,354	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
14/145,751	8,924,805	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
12/197,020	8,086,886	United States	Group Power Management Of Network Devices	Issued	Silicon Image, Inc.
12/683,365	8,543,873	United States	Multi-Site Testing Of Computer Memory Devices And Serial I/O Ports	Issued	Silicon Image, Inc.
14/035,795	8,839,058	United States	Multi-Site Testing Of Computer Memory Devices And Serial I/O Ports	Issued	Silicon Image, Inc.
11/969,847	8,090,030	United States	Method, Apparatus And System For Generating And Facilitating Mobile High-Definition Multimedia Interface	Issued	Silicon Image, Inc.
11/969,852	7,856,520	United States	Control Bus For Connection Of Electronic Devices	Issued	Silicon Image, Inc.
11/969,865	7,921,231	United States	Discovery Of Electronic Devices Utilizing A Control	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Bus		
12/172,187	8,238,653	United States	Methods And Mechanisms For Probabilistic Color Correction	Issued	Silicon Image, Inc.
12/392,000		United States	Method, Apparatus, And System For Pre-Authentication And Processing Of Data Streams	Pending	Silicon Image, Inc.
12/391,987	8,644,504	United States	Method, Apparatus, And System For Deciphering Media Content Stream	Issued	Silicon Image, Inc.
12/605,134	8,407,427	United States	Method And System For Improving Serial Port Memory Communication Latency And Reliability	Issued	Silicon Image, Inc.
13/850,147	8,892,825	United States	Method and System for Improving Serial Port Memory Communication Latency and Reliability	Issued	Silicon Image, Inc.
12/260,970	8,036,248	United States	Method, Apparatus, And System For Automatic Data Aligner For Multiple Serial Receivers	Issued	Silicon Image, Inc.
12/359,025	8,026,726	United States	Fault Testing For Interconnections	Issued	Silicon Image, Inc.
12/486,969	8,793,723	United States	Detection Of Encryption Utilizing Error Detection For Received Data	Issued	Silicon Image, Inc.
12/570,874	8,644,334	United States	Messaging To Provide Data Link Integrity	Issued	Silicon Image, Inc.
12/260,972	7,777,652	United States	Coding System For Memory Systems Employing High-Speed Serial Links	Issued	Silicon Image, Inc.
12/847,416	7,978,099	United States	17b/20b Coding System	Issued	Silicon Image, Inc.
12/351,698	8,374,346	United States	Method, Apparatus, And System For Pre-Authentication And Keep-Authentication Of Content Protected Ports	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/316,305	8,347,081	United States	Method, Apparatus And System For Employing A Content Protection System	Issued	Silicon Image, Inc.
12/577,707	8,275,914	United States	Method And System For Transmitting Or Receiving N-Bit Video Data Over A Serial Link	Issued	Silicon Image, Inc.
12/606,096	8,176,214	United States	Transmission Of Alternative Content Over Standard Device Connectors	Issued	Silicon Image, Inc.
12/351,712	8,185,739	United States	Method And System For Detecting Successful Authentication Of Multiple Ports In A Time Based Roving Architecture	Issued	Silicon Image, Inc.
12/512,877	8,458,343	United States	Signaling For Transitions Between Modes Of Data Transmission	Issued	Silicon Image, Inc.
12/983,233	8,489,784	United States	Adaptive Interconnection Scheme For Multimedia Devices	Issued	Silicon Image, Inc.
13/004,359	8,755,431	United States	Transmission And Detection Of Multi-Channel Signals In Reduced Channel Format	Issued	Silicon Image, Inc.
12/650,357		United States	Method, Apparatus, And System For Simultaneously Previewing Contents From Multiple Protected Sources	Pending	Silicon Image, Inc.
12/712,933	8,692,937	United States	Video Frame Synchronization	Issued	Silicon Image, Inc.
12/966,194		United States	Transmission And Handling Of Three-Dimensional Video Content	Pending	Silicon Image, Inc.
12/873,124	8,325,757	United States	De-Encapsulation Of Data Streams Into Multiple Links	Issued	Silicon Image, Inc.
12/704,417	8,510,487	United States	Hybrid Interface For Serial And Parallel Communication	Issued	Silicon Image, Inc.
13/934,147	8,751,709	United States	Hybrid Interface For Serial And Parallel Communication	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/842,165	8,930,692	United States	Mechanism For Internal Processing Of Content Through Partial Authentication On Secondary Channel	Issued	Silicon Image, Inc.
12/842,190		United States	Mechanism For Partial Encryption Of Data Streams	Pending	Silicon Image, Inc.
13/021,958		United States	Determination Of Physical Connectivity Status Of Devices Based On Electrical Measurement	Allowed	Silicon Image, Inc.
12/898,528	8,598,898	United States	Testing Of High-Speed Input-Output Devices	Issued	Silicon Image, Inc.
13/434,273		United States	Method, Apparatus And System For Transitioning An Audio/Video Device Between A Source Mode And A Sink Mode	Pending	Silicon Image, Inc.
12/848,037	8,624,960	United States	Multi-View Display System	Issued	Silicon Image, Inc.
14/094,668		United States	Multi-View Display System	Pending	Silicon Image, Inc.
12/816,437	8,698,958	United States	Mechanism For Memory Reduction In Picture-In-Picture Video Generation	Issued	Silicon Image, Inc.
13/753,408		United States	Communication Bridging Between Devices Via Multiple Bridge Elements	Pending	Silicon Image, Inc.
13/198,584		United States	Conversion Of Multimedia Data Streams For Use By Connected Devices	Pending	Silicon Image, Inc.
12/906,939	8,537,201	United States	Combining Video Data Streams Of Differing Dimensionality For Concurrent Display	Issued	Silicon Image, Inc.
13/172,745	8,484,387	United States	Detection Of Cable Connections For Electronic Devices	Issued	Silicon Image, Inc.
13/172,742	8,601,173	United States	Detection Of Cable Connections For Electronic	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Devices		
13/362,930		United States	Mechanism For Low Power Standby Mode Control Circuit	Allowed	Silicon Image, Inc.
13/217,138	8,379,145	United States	Conversion And Processing Of Deep Color Video In A Single Clock Domain	Issued	Silicon Image, Inc.
12/979,995	8,874,820	United States	Mechanism For Facilitating A Configurable Port-Type Peripheral Component Interconnect Express/Serial Advanced Technology Attachment Host Controller Architecture	Issued	Silicon Image, Inc.
12/950,850	8,504,672	United States	Discovery Of Electronic Devices In A Combined Network	Issued	Silicon Image, Inc.
13/959,592	8,799,443	United States	Discovery of Electronic Devices in a Combined Network	Issued	Silicon Image, Inc.
13/348,378		United States	Proxy Device Operation In Command And Control Network	Pending	Silicon Image, Inc.
12/950,867		United States	Transfer Of Control Bus Signaling On Packet-Switched Network	Pending	Silicon Image, Inc.
13/339,339		United States	Mechanism For Recovering Clock For Streaming Content Over A Packetized Network	Pending	Silicon Image, Inc.
13/302,452		United States	Multimedia I/O System Architecture for Advanced Digital Television	Pending	Silicon Image, Inc.
13/107,031		United States	Audio And Video Data Multiplexing For Multimedia Stream Switch	Pending	Silicon Image, Inc.
13/174,630		United States	Single-Ended Configurable Multi-Mode Driver	Pending	Silicon Image, Inc.
13/173,302		United States	Fine-Grained Self Refresh Control For DRAM Devices	Pending	Silicon Image, Inc.
13/174,616	8,760,188	United States	Configurable Multi-Dimensional Driver And	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Receiver		Inc.
13/083,399	8,611,486	United States	Adjustment Of Clock Signals Regenerated From A Data Stream	Issued	Silicon Image, Inc.
11/437,357	7,982,798	United States	Edge Detection	Issued	Silicon Image, Inc.
13/153,230	8,446,525	United States	Edge Detection	Issued	Silicon Image, Inc.
10/753,909	7,400,359	United States	Video Stream Routing And Format Conversion Unit With Audio Delay	Issued	Silicon Image, Inc.
10/889,855	7,710,501	United States	Time Base Correction And Frame Rate Conversion	Issued	Silicon Image, Inc.
11/487,144	8,004,606	United States	Original Scan Line Detection	Issued	Silicon Image, Inc.
11/941,050	8,086,067	United States	Noise Cancellation	Issued	Silicon Image, Inc.
11/512,754	8,120,703	United States	Source-Adaptive Video Deinterlacer	Issued	Silicon Image, Inc.
12/204,760	8,559,746	United States	System, Method And Apparatus For Smoothing Of Edges In Images To Remove Irregularities	Issued	Silicon Image, Inc.
14/054,575		United States	System, Method and Apparatus for Smoothing of Edges in Images to Remove Irregularities	Pending	Silicon Image, Inc.
12/703,623	8,452,117	United States	Block Noise Detection And Filtering	Issued	Silicon Image, Inc.
13/899,222	8,891,897	United States	Block Noise Detection And Filtering	Issued	Silicon Image, Inc.
13/335,398		United States	Ringing Suppression In Video Scalers	Pending	Silicon Image, Inc.
13/546,904		United States	Transmission Of Multiple Protocol Data Elements Via An Interface Utilizing A Data Tunnel	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/202,995	7,904,117	United States	Wireless Communication Device Using Adaptive Beamforming	Issued	SiBEAM, Inc.
11/706,711	7,710,319	United States	HD Physical Layer Of A Wireless Communication Device	Issued	SiBEAM, Inc.
12/748,276	7,982,669	United States	Adaptive Beam-Steering Methods To Maximize Wireless Link Budget And Reduce Delay-Spread Using Multiple Transmit And Receive Antennas	Issued	SiBEAM, Inc.
11/706,470	8,014,416	United States	Inter-Port Communication In A Multi-Port Memory Device	Issued	Silicon Image, Inc.
11/689,386	7,881,258	United States	Circuitry To Prevent Peak Power Problems During Scan Shift	Issued	SiBEAM, Inc.
11/726,874	8,155,712	United States	Low Power Very High-Data Rate Device	Issued	SiBEAM, Inc.
11/588,472	8,022,887	United States	Planar Antenna	Issued	SiBEAM, Inc.
11/752,073		United States	A Compact Millimeter Wave Vertical Interconnection Scheme By Combining Flip-Chip, Layer Transition	Pending	SiBEAM, Inc.
11/752,083	7,675,465	United States	Surface Mountable Integrated Circuit Packaging Scheme	Issued	SiBEAM, Inc.
12/215,959		United States	Mechanism For Communication With Multiple Wireless Video Area Networks	Pending	SiBEAM, Inc.
11/981,935		United States	Wireless HD Mac Frame Format	Pending	SiBEAM, Inc.
11/938,126	8,170,522	United States	Multi-Transformer Architecture For An RF Active Circuit	Issued	SiBEAM, Inc.
11/999,810	8,750,241	United States	Concurrent Association With Multiple WVAN Network	Issued	SiBEAM, Inc.
12/079,133	8,831,225	United States	Data Security	Issued	SiBEAM, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/011,404	7,948,961	United States	Wireless Proximity Estimation	Issued	SiBEAM, Inc.
11/982,209	8,279,784	United States	Wireless HD AV Packet Format	Issued	SiBEAM, Inc.
12/055,160	8,170,617	United States	Extensions To Adaptive BeamSteering Method	Issued	SiBEAM, Inc.
12/164,757		United States	Exchanging Information Between Components Coupled With An I2C Bus Via Separate Banks	Pending	SiBEAM, Inc.
12/167,195	8,229,352	United States	Wireless Architecture For 60 GHz	Issued	SiBEAM, Inc.
11/901,069	7,986,753	United States	Modified Branch Metric For Decoders And Equalizers	Issued	SiBEAM, Inc.
12/059,757	7,915,909	United States	RF Integrated Circuit Test Methodology And System	Issued	SiBEAM, Inc.
12/164,907		United States	Dispatch Capability Using A Single Physical Interface	Pending	SiBEAM, Inc.
12/165,468		United States	Bitmap Device Identification In A Wireless Communication System	Pending	SiBEAM, Inc.
12/165,472	8,897,719	United States	Initializing A Transceiver In A Wireless Communication System	Issued	SiBEAM, Inc.
12/164,849	8,341,271	United States	Device Discovery In A Wireless Communication System	Issued	SiBEAM, Inc.
12/164,810	8,116,333	United States	Connection Control In A Wireless Communication System	Issued	SiBEAM, Inc.
12/699,758	8,588,193	United States	Enhanced Wireless Data Rates Using Multiple Beams	Issued	SiBEAM, Inc.
12/699,781	8,457,026	United States	Enhanced Wireless Data Rates Using Multiple Beams	Issued	SiBEAM, Inc.
13/113,318		United States	Apparatus, System, And Method For A Compact Symmetrical Transition Structure For Radio	Allowed	SiBEAM, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Frequency Applications		
14/128,551		United States	Method To Drive HDMI Or MHL Or USB Data Through One Set Of Pins	Pending	Silicon Image, Inc.
13/984,018		United States	Concept And Method Of Reducing Data Dependent Jitter	Pending	Silicon Image, Inc.
13/269,450		United States	Identification And Handling Of Data Streams Using Coded Preambles	Allowed	Silicon Image, Inc.
13/611,786		United States	Combining Video And Audio Streams Utilizing Pixel Repetition Bandwidth	Pending	Silicon Image, Inc.
14/118,832		United States	Compensation Scheme For MHL Common Mode Clock Swing	Pending	Silicon Image, Inc.
13/773,534		United States	Transmitting Multiple Differential Signals Over a Reduced Number of Physical Channels	Pending	Silicon Image, Inc.
13/460,393		United States	Cost-Efficient And Low-Latency Motion Picture Encoding For Limited Channel Bandwidth	Pending	Silicon Image, Inc.
13/791,494	8,925,003	United States	Mechanism For Facilitating Syncronization Of Audio And Video Between Multiple Media Devices	Issued	Silicon Image, Inc.
13/622,286	8,885,435	United States	Interfacing Between Integrated Circuits With Asymmetric Voltage Swing	Issued	Silicon Image, Inc.
13/770,984		United States	Configurable Single Ended Driver	Pending	Silicon Image, Inc.
13/779,372	8,920,188	United States	Integrated Connector/Flex Cable	Issued	Silicon Image, Inc.
13/834,927		United States	Simultaneous Transmission Of Clock And Bidirectional Data Over A Communication Channel	Allowed	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
13/605,708	8,841,974	United States	Test Solution For Ring Oscillators	Issued	Silicon Image, Inc.
14/193,932		United States	Test Solution for a Random Number Generator	Pending	Silicon Image, Inc.
13/787,664		United States	Auxiliary Data Encoding In Video Data	Pending	Silicon Image, Inc.
13/738,768		United States	Method And Apparatus For Reducing Digital Video Image Data	Pending	Silicon Image, Inc.
13/736,765	8,832,338	United States	Mechanism For Facilitating Dynamic Timestamp-Less Clock Regeneration For Transmitting Media Streams Over Shared Channels	Issued	Silicon Image, Inc.
14/123,037		United States	Timing Controlled Cascade Feed-Through High Speed Line Driver	Pending	Silicon Image, Inc.
13/776,577		United States	Apparatus, System And Method For Providing Clock And Data Signaling	Pending	Silicon Image, Inc.
13/940,038		United States	Integrated Mobile Desktop	Pending	Silicon Image, Inc.
13/915,586		United States	Multiple Protocol Tunneling Using Time Division Operations	Pending	Silicon Image, Inc.
13/891,842	8,786,776	United States	Method, Apparatus And System For Communicating Sideband Data With Non-Compressed Video	Issued	Silicon Image, Inc.
13/671,527		United States	Methods And Apparatuses To Provide And Electro-Optical Alignment	Pending	Silicon Image, Inc.
14/371,973		United States	Charge Pump Calibration for Dual-Path Phase-Locked Loop	Pending	Silicon Image, Inc.
14/115,324		United States	Mechanism for Facilitating Dynamic Phase Detection with High Jitter Tolerance for Images of Media Streams	Allowed	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/135,470		United States	Apparatus, System and Method for Formatting Audio-Video Information	Pending	Silicon Image, Inc.
13/839,671		United States	Full Frame Buffer To Improve Video Performance In Low- Latency Video Communication Systems	Pending	Silicon Image, Inc.
12/057,051		United States	Bi-Directional Digital Interface For Video And Audio (DIVA)	Pending	Silicon Image, Inc.
11/760,164	7,940,809	United States	Digital Video Interface With Bi-Directional Half-Duplex Clock Channel Used As Auxiliary Data Channel	Issued	Silicon Image, Inc.
11/865,621	7,916,780	United States	Adaptive Equalizer For Use With Clock And Data Recovery Circuit Of Serial Communication Link	Issued	Silicon Image, Inc.
12/222,745	7,737,802	United States	Passive Equalizer With Negative Impedance To Increase A Gain	Issued	Silicon Image, Inc.
12/636,063	8,680,712	United States	Power Delivery Over Digital Interactive Interface For Video And Audio (DIIVA)	Issued	Silicon Image, Inc.
13/521,739		United States	Multi-Media USB Data Transfer Over Digital Interaction Interface for Video and Audio (DIIVA)	Pending	Silicon Image, Inc.
13/521,762		United States	Video Management And Control In Home Multimedia Network	Pending	Silicon Image, Inc.
14/381,186		United States	Linear Regulator with Improved Power Supply Ripple Rejection	Pending	Silicon Image, Inc.
13/844,152		United States	Electronic Alignment Of Optical Signals	Pending	Silicon Image, Inc.
14/391,382		United States	Frequency Response Compensation in a Digital to Analog Converter	Pending	Silicon Image, Inc.
14/165,340		United States	Apparatus, System and	Pending	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Method for Providing Switching with a T-Coil Circuit		Inc.
13/836,895	8,928,411	United States	Integration Of Signal Sampling Within Transistor Amplifier Stage	Issued	Silicon Image, Inc.
14/165,345		United States	Apparatus, Method and System for Asymmetric Full-Duplex Communication	Pending	Silicon Image, Inc.
14/209,785		United States	Method And Apparatus For Implementing Wide Data Range And Wide Common-Mode Receivers	Pending	Silicon Image, Inc.
14/296,377		United States	Transmitting Apparatus with Source Termination	Pending	Silicon Image, Inc.
14/368,781		United States	Caching of Capabilities Information of Counterpart Device for Efficient Handshaking Operation	Pending	Silicon Image, Inc.
14/163,981		United States	Mechanism for Facilitating Dynamic Counter Synchronization and Packetization in High-Definition Multimedia Interface and Mobile High-Definition Link	Pending	Silicon Image, Inc.
14/253,808		United States	Communication of Multimedia Data Streams Over Multiple Communication Lanes	Pending	Silicon Image, Inc.
14/279,316		United States	HDCP2.2 Authentication Engine and Stream Cipher Engine Sharing in Digital Content Protection Architectures	Pending	Silicon Image, Inc.
14/383,865		United States	Techniques for Fractional-N Phase Locked Loops	Pending	Silicon Image, Inc.
61/949,901		United States	Compressed Video Transfer Over HDMI and MHL	Pending	Silicon Image, Inc.
14/563,797		United States	Electrical Duplex to Optical Conversion	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/470,750		United States	Arbitration Signaling within a Multimedia High Definition Link (MHL 3) Device	Pending	Silicon Image, Inc.
14/275,692		United States	Error Detection and Mitigation in Video Channels	Pending	Silicon Image, Inc.
14/339,393		United States	Phase-Modulated On-Off Keying for Millimeter Wave Spectrum Control	Pending	Silicon Image, Inc.
14/145,715		United States	Messaging to Provide Data Link Integrity	Pending	Silicon Image, Inc.
14/145,736	8,854,548	United States	Mechanism for Memory Reduction in Picture-In-Picture Video Generation	Issued	Silicon Image, Inc.
14/470,613		United States	Compressed Video Transfer Over a Multimedia Link	Pending	Silicon Image, Inc.
14/184,647		United States	Video Frame Synchronization	Pending	Silicon Image, Inc.
14/181,446		United States	Power Delivery Over Digital Interaction Interface for Video and Audio (DiiVA)	Pending	Silicon Image, Inc.
14/470,804		United States	Phase Relationship Control for Control Channel of a Multimedia Communication Link	Pending	Silicon Image, Inc.
14/470,809		United States	Retry Disparity for Control Channel of a Multimedia Communication Link	Pending	Silicon Image, Inc.
61/943,267		United States	Pre-Processor and Post-Processor for Compression of 4:2:0 Encoded Video Streams with Video Compression Codecs Embedded within an Audio/Video Standard	Pending	Silicon Image, Inc.
14/278,255		United States	Encoding Guard Band Data for Transmission Via a Communications Interface Utilizing Transition-Minimized Differential Signaling (Tmds) Coding	Pending	Silicon Image, Inc.
14/322,753		United States	Calibration Of Single-Ended	Pending	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			High-Speed Interfaces		Inc.
61/947,704		United States	Reversible Connector	Pending	Silicon Image, Inc.
14/460,737		United States	System and Method for Transcoding Data	Pending	Silicon Image, Inc.
14/502,928		United States	Electrical Connector with Optical Channel	Pending	Silicon Image, Inc.
14/322,753		United States	Cable with Circuitry for Communicating Performance Information	Pending	Silicon Image, Inc.
61/973,837		United States	Error Correction for Transmission of Compressed Video Data Over Standards-Defined Coded Audio/Video Links	Pending	Silicon Image, Inc.
61/975,517		United States	(MHL) Connector Cable Detect, Cable Orientation Detect and/or Lane Re-Mapping	Pending	Silicon Image, Inc.
61/979,477		United States	MHL3 Router without HDCP2.2 Decryption and Encryption Operation	Pending	Silicon Image, Inc.
61/979,483		United States	TDD over 5-Pin Interface	Pending	Silicon Image, Inc.
14/470,620		United States	Compressed Blanking Period Transfer Over a Multimedia Link	Pending	Silicon Image, Inc.
14/273,400		United States	Transmission and Detection of Multi-Channel Signals in Reduced Channel Format	Pending	Silicon Image, Inc.
61/989,409		United States	System for Dynamic Capabilities, Status, and Metadata Exchange	Pending	Silicon Image, Inc.
14/300,166		United States	Configurable Multi-Dimensional Driver and Receiver	Pending	Silicon Image, Inc.
14/483,013		United States	Enhanced Communication Link Using Synchronization Signal as Link Command	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
62/043,218		United States	Run Length Programmable Unified Built-In Self-Test (BIST) Scheme for Various High-Speed Serial IO Standards	Pending	Silicon Image, Inc.
14/559,523		United States	Determination of Physical Connectivity Status of Devices Based on Electrical Measurement	Pending	Silicon Image, Inc.
14/516,136		United States	Method and System for Improving Serial Port Memory Communication Latency and Reliability	Pending	Silicon Image, Inc.
62/061,630		United States	Secure Control Communication Between an Application Processor and a Transmitter	Pending	Silicon Image, Inc.
62/075,554		United States	Metadata Transfer for HDMI/MHL	Pending	Silicon Image, Inc.
14/570,817		United States	Mechanism for Facilitating Dynamic Phase Detection with High Jitter Tolerance for Images of Media Streams	Pending	Silicon Image, Inc.
14/589,889		United States	Displaying Multiple Videos on Sink Device Using Display Information of Source Device	Pending	Silicon Image, Inc.
14/589,925		United States	Lower Power Operations in a Wireless Tunneling Transceiver	Pending	Silicon Image, Inc.
14/591,845		United States	Simultaneous Transmission of Clock and Bidirectional Data Over a Communication Channel	Pending	Silicon Image, Inc.
14/449095	20150036756	United States	Radio Frequency Interference Reduction In Multimedia Interfaces	Pending	Silicon Image, Inc.

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5533419

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
JEFFERIES FINANCE LLC	05/17/2019

RECEIVING PARTY DATA

Name:	LATTICE SEMICONDUCTOR CORPORATION
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	SILICON IMAGE, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	SIBEAM, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	DVDO, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124

PROPERTY NUMBERS Total: 1143

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Application Number:	12842190

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SIGNATURE:	/Urmila Karandikar/
DATE SIGNED:	05/21/2019
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 97

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RELEASE OF A SECURITY INTEREST -- PATENTS

May 17, 2019

WHEREAS, pursuant to that certain (i) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035222, Frame 0866, (ii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035308, Frame 0428, (iii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035223, Frame 0001, (iv) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035226, Frame 0289, (v) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035223, Frame 0387, (vi) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035226, Frame 0147, (vii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035220, Frame 0048, (viii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035220, Frame 0226, (ix) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035309, Frame 0142, (x) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035308, Frame 0345, (xi) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035225, Frame 0839 and (xii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035225, Frame 0352, LATTICE SEMICONDUCTOR CORPORATION, SILICON IMAGE, INC., SIBEAM, INC. and DVDO, INC., each a Delaware corporation (each, a "Releasee"), granted to JEFFERIES FINANCE LLC, as collateral agent for the ratable benefit of the Secured Creditors (the "Releasor"), a continuing security interest in all right, title and interest of the Releasees in, to and under United States Patents listed on the attached Schedule A (the "Patents"), and all Proceeds in respect thereof (with all of the Releasee's rights listed above being collectively referred to as the "Collateral") to secure the payment, performance and observance of the Obligations;

WHEREAS, the Releasees have satisfied their Obligations; and

WHEREAS, the Releasee has requested and the Releasor has agreed to provide a document suitable for recording in the United States Patent and Trademark Office evidencing and effecting the release, relinquishment and discharge of its security interest in the Collateral.

NOW, THEREFORE, in consideration of and in exchange for good and valuable consideration, the Releasor hereby agrees as follows:

1. Defined Terms. All capitalized terms used but not otherwise defined herein have the meanings given to them in the Grants of Security Interests in United States Patents.

2. Release of Security Interest. The Releasor hereby, without any representation and warranty and without any recourse to the Releasor, releases, relinquishes and discharges all of its security interest in the Collateral.

[Signature Page Follows]

IN WITNESS WHEREOF, the undersigned has executed and delivered this Release as of the date first written above.

JEFFERIES FINANCE LLC,
as Collateral Agent and Releasor

By: _____
Name: Paul Chisholm
Title: Managing Director

[Signature Page to Release of Patent Security Interest]

SCHEDULE A

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/396,994	5574678	United States	Continuous Time Programmable Analog Block Architecture	Issued	Lattice Semiconductor Corporation
08/403,359	5510738	United States	CMOS Programmable Resistor-Based Transconductor	Issued	Lattice Semiconductor Corporation
08/403,354	5493205	United States	Low Distortion Differential Transconductor Output Current Mirror	Issued	Lattice Semiconductor Corporation
08/403,352	5617064	United States	Active Resistor For Stability Compensation [of Transconductor & Op-Amp Based Gain & Filter Stages]	Issued	Lattice Semiconductor Corporation
08/403,595	5670907	United States	VBB Reference for Pumped Substrates	Issued	Lattice Semiconductor Corporation
08/423,303	5490074	United States	Constant delay interconnect for coupling configurable logic blocks	Issued	Lattice Semiconductor Corporation
08/427,117	5596524	United States	CMOS memory cell with gate oxide of both NMOS and PMOS transistors as tunneling window for program and erase	Issued	Lattice Semiconductor Corporation
08/444,306	5491433	United States	Cascode array cell partitioning for a sense amplifier of a programmable logic device	Issued	Lattice Semiconductor Corporation
08/449,384	5756367	United States	Method of making a spacer based antifuse structure for low capacitance and high reliability	Issued	Lattice Semiconductor Corporation
08/447,991	5594687	United States	Completely complementary MOS memory cell with tunneling through the NMOS and PMOS transistors during program and erase	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/453,184	5570046	United States	Lead frame with noisy and quiet Vss and Vdd leads	Issued	Lattice Semiconductor Corporation
08/453,479	5583451	United States	Polarity control circuit which may be used with a ground bounce limiting buffer	Issued	Lattice Semiconductor Corporation
08/456,946	5621650	United States	Programmable gate array with improved interconnect structure, input/output structure and configurable logic block	Issued	Lattice Semiconductor Corporation
08/459,960	5521529	United States	Very high-density complex programmable logic device with a multi-tiered hierarchical switch matrix and optimized flexible logic allocation	Issued	Lattice Semiconductor Corporation
08/459,230	5818254	United States	Multi-tiered hierarchical high speed switch matrix structure for very high-density complex programmable logic devices	Issued	Lattice Semiconductor Corporation
08/459,234	5781030	United States	Programmable uniform symmetrical distribution logic allocator for a high-density complex PLD	Issued	Lattice Semiconductor Corporation
08/459,786	5638018	United States	P-type flip flop	Issued	Lattice Semiconductor Corporation
08/458,865	5589782	United States	Macrocell and clock signal allocation circuit for a programmable logic device (PLD) enabling PLD resources to provide multiple functions	Issued	Lattice Semiconductor Corporation
08/459,570	6531890	United States	Programmable optimized-distribution logic allocator for a high-density complex PLD	Issued	Lattice Semiconductor Corporation
08/461,196	5586044	United States	Array of configurable logic blocks including cascadable lookup tables	Issued	Lattice Semiconductor Corporation
08/462,934	5469368	United States	Array of configurable logic blocks each including a first	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			lookup table coupled to selectively replace an output of second lookup with an alternate function output		Corporation
08/486,178	5764078	United States	Family of multiple segmented programmable logic blocks interconnected by a high speed centralized switch matrix	Issued	Lattice Semiconductor Corporation
08/474,629	5612631	United States	An I/O macrocell for a programmable logic device	Issued	Lattice Semiconductor Corporation
08/479,872	5869981	United States	A High density programmable logic device	Issued	Lattice Semiconductor Corporation
08/486,174	5594365	United States	Architecture of a multiple array high density programmable logic device with a plurality of programmable switch matrices	Issued	Lattice Semiconductor Corporation
08/474,635	5811986	United States	Flexible synchronous/asynchronous cell structure for a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/466,438	5754471	United States	Reference for CMOS memory cell having PMOS and NMOS transistors with a common floating gate	Issued	Lattice Semiconductor Corporation
08/466,438	5754471	United States	Low power CMOS array for a PLD with program and erase using controlled avalanche injection	Issued	Lattice Semiconductor Corporation
08/473,620	5594657	United States	Field Programmable Gate Array Using Look-Up Tables, Multiplexers and Decoders	Issued	Lattice Semiconductor Corporation
08/483,623	5617042	United States	Multiple array programmable logic device with a plurality of programmable switch matrices	Issued	Lattice Semiconductor Corporation
08/492,604	5526278	United States	System for Synthesizing Field Programmable Gate Array	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Implementations From High Level Circuit Descriptions		Corporation
08/493,640	5679599	United States	Isolation using self-aligned trench formation and conventional LOCOS	Issued	Lattice Semiconductor Corporation
08/494,271	5565794	United States	Voltage range tolerant CMOS output buffer with reduced input capacitance	Issued	Lattice Semiconductor Corporation
08/497,992	5742542	United States	Nonvolatile memory cells using only positive charge to store data	Issued	Lattice Semiconductor Corporation
08/500,295	5700698	United States	Method for screening non-volatile memory and programmable logic devices	Issued	Lattice Semiconductor Corporation
08/501,230	5604370	United States	Field Implant For Semiconductor Device	Issued	Lattice Semiconductor Corporation
08/505,837	5635855	United States	Method for Simultaneous Programming of In-System Programmable Integrated Circuits	Issued	Lattice Semiconductor Corporation
08/507,893	5570039	United States	Method and Apparatus for Converting Field-Programmable Gate Array Implementations Into Mask-Programmable Logic Cell Implementations	Issued	Lattice Semiconductor Corporation
08/507,957	5559450	United States	Programmable Function Unit As Parallel Multiplier Cell	Issued	Lattice Semiconductor Corporation
08/528,030	5581126	United States	Interlaced layout configuration for differential pairs of interconnect lines	Issued	Lattice Semiconductor Corporation
08/535,362	5528170	United States	Low-Skew Signal Routing In A Programmable Array	Issued	Lattice Semiconductor Corporation
08/551,974	5615150	United States	control gate-addressed cmos non-volatile cell that programs through gates of CMOS transistors	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/554,092	5587945	United States	CMOS EEPROM cell with tunneling window in the read path	Issued	Lattice Semiconductor Corporation
08/560,038	5666309	United States	Memory cell for a programmable logic device (PLD) avoiding pumping programming voltage above an NMOS threshold	Issued	Lattice Semiconductor Corporation
08/560,933	5587921	United States	Array of configurable logic blocks each including a lookup table having inputs coupled to a first multiplexer and having outputs to a second multiplexer	Issued	Lattice Semiconductor Corporation
08/561,306	5672521	United States	Method of forming multiple gate oxide thicknesses on a wafer substrate	Issued	Lattice Semiconductor Corporation
08/573,622	5809522	United States	Microprocessor system with process identification tag entries to reduce cache flushing after a context switch	Issued	Lattice Semiconductor Corporation
08/574,776	5739713	United States	Deconvolution input buffer compensating for capacitance of a switch matrix of a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/575,898	5736888	United States	Capacitance elimination circuit	Issued	Lattice Semiconductor Corporation
08/575,852	5719516	United States	Clock generator circuit for use with a dual edge register that provides a separate enable for each edge over an input clock signal	Issued	Lattice Semiconductor Corporation
08/596,679	5598346	United States	Array of configurable logic blocks including network means for broadcasting clock signals to different pluralities of logic blocks	Issued	Lattice Semiconductor Corporation
08/606,702	5623217	United States	Field Programmable Gate Array With Write-Port Enabled Memory	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/614,728	5926841	United States	Segment descriptor cache for a processor	Issued	Lattice Semiconductor Corporation
08/625,403	5646901	United States	CMOS memory cell with tunneling during program and erase through the NMOS and PMOS transistors and a pass gate separating the NMOS and PMOS transistors	Issued	Lattice Semiconductor Corporation
08/632,811	5751163	United States	Parallel Programming of ISP Devices Using An Automatic Tester	Issued	Lattice Semiconductor Corporation
08/635,184	5666087	United States	Active Resistor For Stability Compensation [of Transconductor & Op-Amp Based Gain & Filter Stages]	Issued	Lattice Semiconductor Corporation
08/643,807	5748525	United States	Array cell circuit with split read/write line	Issued	Lattice Semiconductor Corporation
08/643,291	5864486	United States	Method And Apparatus For In-System Programming of A Programmable Logic Device Using a Two-Wire Interface	Issued	Lattice Semiconductor Corporation
08/653,186	5789939	United States	Very high-density complex programmable logic device with a multi-tiered hierarchical switch matrix and optimized flexible logic allocation	Issued	Lattice Semiconductor Corporation
08/659,279	5723984	United States	Field programmable gate array (FPGA) with interconnect encoding	Issued	Lattice Semiconductor Corporation
08/659,941	5808942	United States	Field programmable gate array (FPGA) having an improved configuration memory and look up table	Issued	Lattice Semiconductor Corporation
08/664,190	5830795	United States	Simplified masking process for programmable logic device manufacture	Issued	Lattice Semiconductor Corporation
08/666,193	5760609	United States	Clock signal providing circuit with enable and a pulse generator with enable for use	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			in a block clock circuit of a programmable logic device		
08/668,141	5796295	United States	Reference for CMOS memory cell having PMOS and NMOS transistors with a common floating gate	Issued	Lattice Semiconductor Corporation
08/668,896	5751164	United States	Programmable logic device with multi-level power control	Issued	Lattice Semiconductor Corporation
08/683,685	5734275	United States	Programmable logic device having a sense amplifier with virtual ground	Issued	Lattice Semiconductor Corporation
08/683,373	5818294	United States	Temperature insensitive current source	Issued	Lattice Semiconductor Corporation
08/690,768	5801551	United States	Depletion mode pass gates with controlling decoder and negative power supply for a programmable logic device	Issued	Lattice Semiconductor Corporation
08/689,523	5942780	United States	An integrated circuit having, and process providing, different oxide layer thicknesses on a substrate	Issued	Lattice Semiconductor Corporation
08/696,444	5796750	United States	Method for Programming a PLD In An Automatic Tester	Issued	Lattice Semiconductor Corporation
08/700,616	5740069	United States	Logic device (PLD) having direct connections between configurable logic blocks (CLBs) and configurable input/output blocks (IOBs)	Issued	Lattice Semiconductor Corporation
08/699,401	5960274	United States	Oxide formation process for manufacturing programmable logic device	Issued	Lattice Semiconductor Corporation
08/702,846	5959336	United States	Decoder circuit with short channel depletion transistors	Issued	Lattice Semiconductor Corporation
08/710,445	5862365	United States	Configuration Pin Emulation Circuit For a Field Programmable Array	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 174

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/723,082	5760605	United States	Programmable high speed routing switch	Issued	Lattice Semiconductor Corporation
08/726,512	5761116	United States	Vpp only scalable EEPROM memory cell having transistors with thin tunnel gate oxide	Issued	Lattice Semiconductor Corporation
08/729,117	5991907	United States	Method for Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/734,888	5805607	United States	Method for user-controlled I/O switching during in-circuit programming of CPLDs through the IEEE 1149.1 test access port	Issued	Lattice Semiconductor Corporation
08/740,948	5811987	United States	Block clock and initialization circuit for a complex high density PLD	Issued	Lattice Semiconductor Corporation
08/748,041	5892962	United States	FPGA-based Processor	Issued	Lattice Semiconductor Corporation
08/745,410	5717342	United States	Output buffer incorporating shared intermediate nodes	Issued	Lattice Semiconductor Corporation
08/781,882	6028993	United States	Timed Circuit Simulation In Hardware Using FPGAs	Issued	Lattice Semiconductor Corporation
08/785,096	5841701	United States	Method of charging and discharging floating gage transistors to reduce leakage current	Issued	Lattice Semiconductor Corporation
08/799,153	5904575	United States	Method and apparatus incorporating nitrogen selectively for differential oxide growth	Issued	Lattice Semiconductor Corporation
08/799,235	5885904	United States	Method to incorporate, and a device having, oxide enhancement dopants using gas immersion laser doping (GILD) for selectively growing an oxide layer	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/823,953	6190966	United States	Process for fabricating semiconductor memory device with high data retention including silicon nitride etch stop layer formed at high temperature with low hydrogen ion	Issued	Lattice Semiconductor Corporation
08/828,520	5905385	United States	Memory bits used to couple look up table inputs to facilitate increased availability to routing resources particularly for variable sized look up tables for a field programmable gate array (FPGA)	Issued	Lattice Semiconductor Corporation
08/831,372	5844912	United States	Fast verify for CMOS memory cell	Issued	Lattice Semiconductor Corporation
08/827,671	5835405	United States	Application Specific Modules in a Programmable Logic Device	Issued	Lattice Semiconductor Corporation
08/843,150	6087275	United States	Reduction of n-channel parasitic transistor leakage by using low power/low pressure phosphosilicate glass	Issued	Lattice Semiconductor Corporation
08/838,487	6034541	United States	In-System Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
08/856,926	5949279	United States	Devices for sourcing constant supply current from power supply in system with integrated circuit having variable supply current requirement	Issued	Lattice Semiconductor Corporation
08/859,761	5989957	United States	Process for fabricating semiconductor memory device with high data retention including silicon nitride etch stop layer formed at high temperature with low hydrogen ion concentration	Issued	Lattice Semiconductor Corporation
08/871,589	5978272	United States	Nonvolatile memory structure for programmable logic devices	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 176

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/899,428	6028447	United States	FPGA Having Predictable Open-Drain Drive Mode	Issued	Lattice Semiconductor Corporation
08/912,763	6072351	United States	Output buffer for making a high voltage (5.0 volt) compatible input/output in a low voltage (2.5 volt) semiconductor process	Issued	Lattice Semiconductor Corporation
08/931,798	6359466	United States	Circuitry to provide fast carry	Issued	Lattice Semiconductor Corporation
08/938,550	6020755	United States	Hybrid Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/948,306	6097212	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/947,888	5854114	United States	Data retention of EEPROM cell with shallow trench isolation using thicker liner oxide	Issued	Lattice Semiconductor Corporation
08/949,992	6028463	United States	Programmable Clock Manager For A Programmable Logic Device that Can Generate At Least Two Different Output Clocks	Issued	Lattice Semiconductor Corporation
08/950,444	6216191	United States	Field Programmable Gate Array Having A Dedicated Processor Interface	Issued	Lattice Semiconductor Corporation
08/950,446	5986471	United States	Bi-directional Buffers and Supplemental Logic and Interconnect Cells for Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
08/950,448	6060902	United States	A Programmable Clock Manager For A Programmable Logic Device that Can Be Programmed Without Reconfiguring the Device	Issued	Lattice Semiconductor Corporation
08/950,624	6049224	United States	Programmable Logic Device With Logic Cells Having A Flexible Input Structure	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 177

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/951,128	6043677	United States	Programmable Clock Manager For A Programmable Logic Device that Can Implement Delay-Locked Loop Functions	Issued	Lattice Semiconductor Corporation
08/964,421	6389321	United States	Simultaneous Wired and Wireless Remote In-System Programming of Multiple Remote Systems	Issued	Lattice Semiconductor Corporation
08/974,799	6003150	United States	Method for Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/996,361	6275064	United States	Symmetrical, extended and fast direct connections between variable grain blocks in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/996,049	6127843	United States	Dual port SRAM memory for run time use in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,615	6034544	United States	Programmable input/output block (IOB) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,614	5982193	United States	Input/output block (IOB) connections to MAXL lines, NOR lines and dendrites in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,612	5990702	United States	Flexible direct connections between input/output blocks (IOBs) and variable grain blocks (VBGs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/997,221	6107823	United States	Programmable control multiplexing for input/output blocks (IOBs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/996,119	5986480	United States	Multiple input zero power and/nor gate for use in a field programmable gate array (FPGA)	Issued	Lattice Semiconductor Corporation
08/996,530	6134703	United States	A Process for Programming PLDs and Embedded Non-Volatile Memories	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 178

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/998,978	6102963	United States	Electrically erasable and reprogrammable, nonvolatile integrated storage device with in-system programming and verification (ISPAV) capabilities for supporting in-system reconfiguring of PLD's	Issued	Lattice Semiconductor Corporation
09/008,762	6130551	United States	Synthesis-friendly FPGA architecture with variable length and variable timing interconnect	Issued	Lattice Semiconductor Corporation
09/010,000	6034538	United States	Virtual Logic System For Reconfigurable Hardware	Issued	Lattice Semiconductor Corporation
09/023,669	6025637	United States	Spacer based antifuse structure for low capacitance and high reliability and method of fabrication thereof	Issued	Lattice Semiconductor Corporation
09/023,506	6023570	United States	Sequential and Simultaneous Manufacturing Programming of Multiple In-System Programmable Systems Through a Data Network	Issued	Lattice Semiconductor Corporation
09/026,814	6093946	United States	EEPROM cell with field-edgeless tunnel window using shallow trench isolation process	Issued	Lattice Semiconductor Corporation
09/037,095	6128770	United States	Configurable logic array including IOB to longlines interconnect means for providing selectable access to plural longlines from each IOB (input/output block)	Issued	Lattice Semiconductor Corporation
09/045,128	6064225	United States	Global Signal Distribution With Reduced Routing Tracks In An FPGA	Issued	Lattice Semiconductor Corporation
09/046,404	5982683	United States	Enhanced method of testing semiconductor devices having nonvolatile elements	Issued	Lattice Semiconductor Corporation
09/053,251	6556154	United States	Offset Voltage Calibration DAC With Reduced Sensitivity To Mismatch	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 179

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Errors		
09/059,552	6108806	United States	Method of Testing and Diagnosing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/067,320	6154050	United States	Internal tristate bus with arbitration logic	Issued	Lattice Semiconductor Corporation
09/067,318	6104207	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/069,035	6133750	United States	Combination of global clock and localized clocks	Issued	Lattice Semiconductor Corporation
09/069,768	6002610	United States	Non-Volatile Memory Element For Programmable Logic Applications and Operational Methods Therefor	Issued	Lattice Semiconductor Corporation
09/080,906	6225821	United States	Package migration for related programmable logic devices	Issued	Lattice Semiconductor Corporation
09/083,335	6304099	United States	Method and structure for dynamic in-system programming	Issued	Lattice Semiconductor Corporation
09/083,336	6066977	United States	Programmable Output Voltage Levels	Issued	Lattice Semiconductor Corporation
09/083,205	6255847	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/086,437	6087696	United States	Stacked tunneling dielectric technology for improving data retention of EEPROM cell	Issued	Lattice Semiconductor Corporation
09/109,123	6202182	United States	Method and Apparatus For Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/114,385	6028758	United States	Electrostatic discharge (ESD) protection for a 5.0 volt compatible input/output (I/O) in a 2.5 volt semiconductor process	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/114,717	6091595	United States	Electrostatic discharge (ESD) protection for NMOS pull up transistors of a 5.0 volt compatible output buffer using 2.5 volt process transistors	Issued	Lattice Semiconductor Corporation
09/114,718	6043969	United States	Ballast resistors with parallel stacked NMOS transistors used to prevent secondary breakdown during ESD with 2.5 volt process transistors	Issued	Lattice Semiconductor Corporation
09/115,683	6124732	United States	Signaling Voltage Range Discriminator	Issued	Lattice Semiconductor Corporation
09/118,200	6028446	United States	Flexible Synchronous and Asynchronus Circuits for A Very High Density Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/134,174	6064105	United States	Data retention of EEPROM cell with shallow trench isolation using thicker liner oxide	Issued	Lattice Semiconductor Corporation
09/145,793	6087854	United States	High Speed Line Driver With Direct and Complementary Outputs	Issued	Lattice Semiconductor Corporation
09/169,848	6347387	United States	Test Circuits For Multiple FPGA Systems	Issued	Lattice Semiconductor Corporation
09/169,492	6424003	United States	EEPROM cell with self-aligned tunneling window	Issued	Lattice Semiconductor Corporation
09/187,691	6228696	United States	Semiconductor-oxide-semiconductor capacitor formed in integrated circuit	Issued	Lattice Semiconductor Corporation
09/187,689	6154051	United States	Tileable and compact layout for super variable grain blocks within FPGA device	Issued	Lattice Semiconductor Corporation
09/186,917	6229336	United States	Programmable integrated circuit device with slew control and skew control	Issued	Lattice Semiconductor Corporation
09/188,778	6169432	United States	High voltage switch for	Issued	Lattice

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			providing voltages higher than 2.5 volts with transistors made using a 2.5 volt process		Semiconductor Corporation
09/192,094	6291327	United States	Optimization of S/D annealing to minimize random S/D shorts in memory array	Issued	Lattice Semiconductor Corporation
09/192,096	6221733	United States	Reduction of mechanical stress in shallow trench isolation process	Issued	Lattice Semiconductor Corporation
09/196,449	6191612	United States	Enhanced I/O control flexibility for generating control signals	Issued	Lattice Semiconductor Corporation
09/196,080	5912550	United States	Power converter with 2.5 semiconductor process components	Issued	Lattice Semiconductor Corporation
09/198,796	6218857	United States	Variable sized line driving amplifiers for input/output blocks (IOBs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/200,395	6261944	United States	Semiconductor device having high reliability passivation and fabrication method	Issued	Lattice Semiconductor Corporation
09/198,653	6009033	United States	Method of programming and erasing an EEPROM device under an elevated temperature and apparatus thereof	Issued	Lattice Semiconductor Corporation
09/199,664	6353352	United States	Clock tree topology	Issued	Lattice Semiconductor Corporation
09/201,081	6133769	United States	Phase locked loop with a lock detector	Issued	Lattice Semiconductor Corporation
09/203,149	6404006	United States	EEPROM cell with tunneling across entire separated channels	Issued	Lattice Semiconductor Corporation
09/217,647	5969992	United States	EEPROM cell using p-well for	Issued	Lattice Semiconductor Corporation
09/207,558	6175266	United States	Operational amplifier with CMOS transistors made using	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 182

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			2.5 volt process transistors		Corporation
09/208,203	6163168	United States	Efficient interconnect network for use in FPGA device having variable grain architecture	Issued	Lattice Semiconductor Corporation
09/212,022	6124730	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/212,330	6100715	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/212,331	6081473	United States	FPGA integrated circuit having embedded SRAM memory blocks each with statically and dynamically controllable read mode	Issued	Lattice Semiconductor Corporation
09/216,662	6204686	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	Issued	Lattice Semiconductor Corporation
09/216,051	6214666	United States	Method of forming a non-volatile memory device	Issued	Lattice Semiconductor Corporation
09/217,648	6232631	United States	Floating gate memory cell structure with programming mechanism outside the read path	Issued	Lattice Semiconductor Corporation
09/217,646	6282123	United States	Method of fabricating, programming, and erasing a dual pocket two sided program/erase non-volatile memory cell	Issued	Lattice Semiconductor Corporation
09/218,987	6294810	United States	EEPROM cell with tunneling at separate edge and channel regions	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/220,469	6157568	United States	Avalanche programmed floating gate memory cell structure with program element in first polysilicon layer	Issued	Lattice Semiconductor Corporation
09/221,360	6294809	United States	Avalanche programmed floating gate memory cell structure with program element in polysilicon	Issued	Lattice Semiconductor Corporation
09/226,702	6215700	United States	PMOS avalanche programmed floating gate memory cell structure	Issued	Lattice Semiconductor Corporation
09/227,981	6197638	United States	Oxide formation process for manufacturing programmable logic device	Issued	Lattice Semiconductor Corporation
09/235,356	6097664	United States	Multi-port SRAM cell array having plural write paths including for writing through addressable port and through serial boundary scan	Issued	Lattice Semiconductor Corporation
09/235,351	6181163	United States	FPGA integrated circuit having embedded SRAM memory blocks and interconnect channel for broadcasting address and control	Issued	Lattice Semiconductor Corporation
09/235,615	6211695	United States	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	Issued	Lattice Semiconductor Corporation
09/239,072	5999449	United States	Two transistor EEPROM cell using P-well for tunneling across a channel	Issued	Lattice Semiconductor Corporation
09/240,560	6297128	United States	Process for manufacturing shallow trenches filled with dielectric material having low mechanical stress	Issued	Lattice Semiconductor Corporation
09/245,813	6294811	United States	Two transistor EEPROM cell	Issued	Lattice Semiconductor Corporation
09/255,410	6075724	United States	Method for sorting	Issued	Lattice

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			semiconductor devices having a plurality of non-volatile memory cells		Semiconductor Corporation
09/255,053	6255169	United States	Process for fabricating a high-endurance non-volatile memory device	Issued	Lattice Semiconductor Corporation
09/256,245	6133164	United States	Fabrication of oxide regions having multiple thicknesses using minimized number of thermal cycles	Issued	Lattice Semiconductor Corporation
09/261,776	6256758	United States	Fault Tolerance Operation of Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/263412	6075293	United States	Semiconductor device having a multi-layer metal interconnect structure	Issued	Lattice Semiconductor Corporation
09/268,897	6207989	United States	Non-volatile memory device having a high-reliability composite insulation layer	Issued	Lattice Semiconductor Corporation
09/276,991	6031365	United States	Band gap reference using a low voltage power supply	Issued	Lattice Semiconductor Corporation
09/276,990	6163175	United States	High voltage detector to control a power supply voltage pump for a 2.5 volt semiconductor process device	Issued	Lattice Semiconductor Corporation
09/277,441	6326663	United States	Avalanche injection EEPROM memory cell with p-type control gate	Issued	Lattice Semiconductor Corporation
09/280,887	6172392	United States	Boron doped silicon capacitor plate	Issued	Lattice Semiconductor Corporation
09/286,830	6284626	United States	Angled nitrogen ion implantation for minimizing mechanical stress on side walls of an isolation trench	Issued	Lattice Semiconductor Corporation
09/288,062	6265900	United States	High Speed Logical OR Circuit	Issued	Lattice Semiconductor Corporation
09/287,976	6413826	United States	Gate insulator process for	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 185

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			nanometer MOSFETs		Corporation
09/310,071	6424000	United States	Floating gate memory apparatus and method for selected programming thereof	Issued	Lattice Semiconductor Corporation
09/316,241	6274898	United States	Triple-well EEPROM cell using p-well for tunneling across a channel	Issued	Lattice Semiconductor Corporation
09/318,570	6552595	United States	High Voltage Discharge Scheme	Issued	Lattice Semiconductor Corporation
09/320389	6118693	United States	Electrically erasable non-volatile memory cell with integrated SRAM to reduce testing time	Issued	Lattice Semiconductor Corporation
09/320,392	6067252	United States	Electrically erasable non-volatile memory cell with no static power dissipation	Issued	Lattice Semiconductor Corporation
09/326,940	6184713	United States	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	Issued	Lattice Semiconductor Corporation
09/326,140	6150841	United States	Enhanced storage macrocell module for high density CPLD architectures	Issued	Lattice Semiconductor Corporation
09/330,753	6628660	United States	Finite State Machine with Associated Memory	Issued	Lattice Semiconductor Corporation
09/334,051	6028789	United States	Zero-power CMOS non-volatile memory cell having an avalanche injection element	Issued	Lattice Semiconductor Corporation
09/334,052	6034893	United States	Non-volatile memory cell having dual avalanche injection elements	Issued	Lattice Semiconductor Corporation
09/400,029	6404226	United States	Integrated Circuit With Standard Cell Logic and Spare Gates	Issued	Lattice Semiconductor Corporation
09/405,958	6550030	United States	On-Line Testing of the Programmable Logic Blocks In Field Programmable Gate	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 186

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Arrays		
09/406,219	6574761	United States	On-Line Testing of the Programmable Interconnect Network In Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/433,642	6191609	United States	Combination of global clock and localized clocks	Issued	Lattice Semiconductor Corporation
09/440,460	6294925	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/440,207	6278311	United States	Method for minimizing instantaneous currents when driving bus signals	Issued	Lattice Semiconductor Corporation
09/441,220	6208559	United States	Method of operating EEPROM memory cells having transistors with thin gate oxide and reduced disturb	Issued	Lattice Semiconductor Corporation
09/452,017	6137738	United States	Method For In-System Programming of Serially Configured EEPROMS Using a JTAG Interface of an FPGA	Issued	Lattice Semiconductor Corporation
09/454,322	6326808	United States	Inversion of Product Term Line Before or Logic in a Programmable Logic Device (PLD)	Issued	Lattice Semiconductor Corporation
09/472,645	6150842	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/506,180	6362684	United States	Amplifier Having an Adjustable Resistor Network	Issued	Lattice Semiconductor Corporation
09/507,580	6424209	United States	Integrated Programmable Continuous Time Filter with Programmable Capacitor Arrays	Issued	Lattice Semiconductor Corporation
09/548,171	6351157	United States	Output buffer for making a high voltage (5.0 volt) compatible input/output in a low voltage (2.5 volt)	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 187

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			semiconductor process		
09/567,898	6288937	United States	Decoded Generic Routing Pool	Issued	Lattice Semiconductor Corporation
09/578,086	6570212	United States	Complementary avalanche injection EEPROM cell	Issued	Lattice Semiconductor Corporation
09/603,119	6292930	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/603,807	6216257	United States	FPGA device and method that includes a variable grain function architecture for implementing configuration logic blocks and a complimentary variable length interconnect architecture for providing configurable routing between configuration logic blocks	Issued	Lattice Semiconductor Corporation
09/611,449	6530049	United States	On-line Fault Tolerant Operation Via Incremental Reconfiguration of Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/626,094	6380759	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/632,319	6567969	United States	Configurable Logic Array Including Lookup Table Means For Generating Functions of Different Numbers Of Input Terms	Issued	Lattice Semiconductor Corporation
09/643,279	6627947	United States	Compact single-poly two-transistor EEPROM cell	Issued	Lattice Semiconductor Corporation
09/651,689	6433602	United States	High speed schmitt trigger with low supply voltage	Issued	Lattice Semiconductor Corporation
09/660,707	6370071	United States	High Voltage CMOS switch	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 188

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
09/661,585	6462576	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/668,896	6701340	United States	Double Differential Comparator and Programmable Analog Block Architecture Using Same	Issued	Lattice Semiconductor Corporation
09/669,186	6249144	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/671,853	6631487	United States	On-Line Testing of Field Programmable Gate Array Resources	Issued	Lattice Semiconductor Corporation
09/692,694	6470485	United States	Scalable and parallel processing methods and structures for testing configurable interconnect network in FPGA device	Issued	Lattice Semiconductor Corporation
09/704,487	6507212	United States	Wide input programmable logic system and method	Issued	Lattice Semiconductor Corporation
09/651,805	6455912	United States	Process for manufacturing shallow trenches filled with dielectric material having low mechanical stress	Issued	Lattice Semiconductor Corporation
09/712,000	6356107	United States	Method and structure for dynamic in-system programming	Issued	Lattice Semiconductor Corporation
09/721,153	6348813	United States	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	Issued	Lattice Semiconductor Corporation
09/732,216	6735706	United States	Programmable power management system and method	Issued	Lattice Semiconductor Corporation
09/731,184	6524911	United States	Combination of BPTEOS oxide film with CMP and RTA to achieve good data	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 189

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			retention		
09/731,185	6287916	United States	Method for forming a semiconductor device using LPCVD nitride to protect floating gate from charge loss	Issued	Lattice Semiconductor Corporation
09/733,878	6526558	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	Issued	Lattice Semiconductor Corporation
09/775,488	6462602	United States	Voltage Level Translator Systems And Methods	Issued	Lattice Semiconductor Corporation
09/775,489	6414521	United States	Improved sense amplifier systems and methods	Issued	Lattice Semiconductor Corporation
09/818,257	6496969	United States	Programming Programmable Logic Devices Using Hidden Switches	Issued	Lattice Semiconductor Corporation
09/841,209	6590415	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/863,656	6535043	United States	Clock Signal Selection System, Method of Generating A Clock Signal And Programmable Clock Manager Including Same	Issued	Lattice Semiconductor Corporation
09/864,276	6486705	United States	Signal Distribution Scheme In Field Programmable Gate Array (FPGA) or Field Programmable Systems Chip (FPSC) Including Cycle Stealing Units	Issued	Lattice Semiconductor Corporation
09/864,284	6472904	United States	Double Data Rate Input And Output In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/864,289	6480026	United States	Multi-functional I/O Buffers In a Field Programmable Gate	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 190

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Array (FPGA)		Corporation
09/864,277	6483342	United States	Multi-Master Multi-Slave Bus In Field Programmable Gate Array (FPGA)	Issued	Lattice Semiconductor Corporation
09/864,290	6772230	United States	Field Programmable Gate Array (FPGA) Bit Stream Format	Issued	Lattice Semiconductor Corporation
09/870,877	6498538	United States	Low Jitter Integrated Phase Locked Loop With Broad Tuning Range	Issued	Lattice Semiconductor Corporation
09/870,541	6455375	United States	EEPROM tunnel window for program injection via P+ contacted inversion	Issued	Lattice Semiconductor Corporation
09/881,950	6614291	United States	Low Voltage, High Speed CMOS CML Latch and MUX Devices	Issued	Lattice Semiconductor Corporation
09/885,243	6429692	United States	High Speed Data Sampling With Reduced Metastability	Issued	Lattice Semiconductor Corporation
09/927,289	6492877	United States	Improved Coupling For LC-Based VCO	Issued	Lattice Semiconductor Corporation
09/927,612	6525617	United States	Buffering For LC-Based Stage	Issued	Lattice Semiconductor Corporation
09/927,793	6653860	United States	Enhanced logic macrocell with expanded PT (product term) sharing capability for Use in High Density CPLD Architectures	Issued	Lattice Semiconductor Corporation
09/941,454	6489835	United States	Low Voltage Bandgap Reference Circuit	Issued	Lattice Semiconductor Corporation
09/949,112	6593222	United States	Method to improve the reliability of thermosonic gold to aluminum wire bonds	Issued	Lattice Semiconductor Corporation
09/966,967	6832231	United States	Multiple Width Random Number Generation	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 191

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/011,549	6693830	United States	Single Poly Two-Transistor EEPROM Cell With Differentially Doped Floating Gate	Issued	Lattice Semiconductor Corporation
10/053,004	6989551	United States	Test structure for determining the minimum tunnel opening size in a non-volatile memory cell	Issued	Lattice Semiconductor Corporation
10/010,011	6515899	United States	Non-Volatile Memory Cell With Enhanced Cell Drive Current	Issued	Lattice Semiconductor Corporation
09/991,245	6611463	United States	Zero Power Programmable Memory Cell	Issued	Lattice Semiconductor Corporation
09/992,493	6489806	United States	Zero power logic cell for use in programmable logic devices	Issued	Lattice Semiconductor Corporation
10/006,559	7003066	United States	Digital Phase locked Loop with Phase Selector having Minimized Number of Phase Interpolators	Issued	Lattice Semiconductor Corporation
10/006,610	6999543	United States	Clock Data Recovery Deserializer With Programmable Sync Detect Logic	Issued	Lattice Semiconductor Corporation
10/006,516	6993108	United States	Digital Phase Locked Loop With Programmable Digital Filter	Issued	Lattice Semiconductor Corporation
10/021,873	6661254	United States	Programmable Interconnect Circuit With A Phase-Locked Loop	Issued	Lattice Semiconductor Corporation
10/017,725	6674303	United States	Programmable I/O cell with bidirectional and shift register capabilities	Issued	Lattice Semiconductor Corporation
10/017,859	6605959	United States	Structure and Method for Implementing Wide Multiplexers	Issued	Lattice Semiconductor Corporation
10/022,464	7154298	United States	Block oriented architecture for programmable interconnect circuit	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 192

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/021,844	6703860	United States	I/O Block for Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/023,053	6653861	United States	Multi-level Routing Structure for a Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/023,226	6650141	United States	High Speed Interface For a Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/059,624	6636442	United States	Non-volatile memory element having a cascoded transistor scheme to reduce oxide field stress	Issued	Lattice Semiconductor Corporation
10/061,057	6845044	United States	Method of preventing high Icc at start-up in zero-power EEPROM cells for PLD applications	Issued	Lattice Semiconductor Corporation
10/066,031	6680625	United States	Symmetrical CML Logic Gate System	Issued	Lattice Semiconductor Corporation
10/082,050	6781170	United States	Integrated Circuit Base Transistor Structure And Associated Programmable Cell Library	Issued	Lattice Semiconductor Corporation
10/083,728	6600188	United States	An EEPROM with neutralized doping at tunnel window edge	Issued	Lattice Semiconductor Corporation
10/090,209	6621298	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
10/103,100	6795959	United States	Integrated Delay Discriminator For Use With a Field- Programmable Gate Array and A Method of Determining a Time Delay Thereof	Issued	Lattice Semiconductor Corporation
10/106,509	6907439	United States	FFT address generation method and apparatus	Issued	Lattice Semiconductor Corporation
10/108,401	6976047	United States	Skipped carry incrementer for FFT address generation	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/112,370	6639431	United States	Differential Input Comparator	Issued	Lattice Semiconductor Corporation
10/128,943	6660579	United States	Zero Power Memory Cell With Improved Data Retention	Issued	Lattice Semiconductor Corporation
10/131,883	7032162	United States	Polynomial Expander for Generating Coefficients of a Polynomial from Roots of the Polynomial	Issued	Lattice Semiconductor Corporation
10/133,016	6765408	United States	Device and Method with Generic Logic Blocks	Issued	Lattice Semiconductor Corporation
10/135,308	6814296	United States	Integrated Circuit and Associated Design Method With Antenna Error Control Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/135,325	6600341	United States	Integrated Circuit and Associated Design Method Using Spare Gate Islands	Issued	Lattice Semiconductor Corporation
10/146,739	6714048	United States	Input Buffer With Selectable PCL, GTL, or PECL Compatibility	Issued	Lattice Semiconductor Corporation
10/146,826	6657458	United States	Output Buffer With Feedback From An Input Buffer To Provide Selectable PCL, GTL, or PECL Compatability	Issued	Lattice Semiconductor Corporation
10/146,769	6870391	United States	Input Buffer With CMOS Driver Gate Current Control Enabling Selectable PCL, GTL, or PECL Compatibility	Issued	Lattice Semiconductor Corporation
10/147,199	6714043	United States	Output Buffer Having Programmable Drive Current And Output Voltage Limits	Issued	Lattice Semiconductor Corporation
10/146,734	6720755	United States	Band Gap Reference Circuit	Issued	Lattice Semiconductor Corporation
10/147,011	6760209	United States	Electrostatic Discharge Protection Circuit	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 194

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/151,753	6798244	United States	Output Buffer With Overvoltage Protection	Issued	Lattice Semiconductor Corporation
10/150,410	6848095	United States	Method of Assigning Logic Functions To Macrocells In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/159,009	6583652	United States	Highly linear programmable transconductor with large input-signal range	Issued	Lattice Semiconductor Corporation
10/159,089	6717451	United States	Precision analog level shifter with programmable options	Issued	Lattice Semiconductor Corporation
10/159,681	6806771	United States	Multimode output stage converting differential to single-ended signals using current-mode input signals	Issued	Lattice Semiconductor Corporation
10/162,337	6596587	United States	Shallow junction EEPROM Device and Process for Fabricating the Device	Issued	Lattice Semiconductor Corporation
10/160,855	6794236	United States	EEPROM Device with Improved Capacitive Coupling and Fabrication Process	Issued	Lattice Semiconductor Corporation
10/161,283	6716705	United States	EEPROM Device having a Retrograde Program Junction Region And Process for Fabrication the Device	Issued	Lattice Semiconductor Corporation
10/164,484	6703305	United States	Semiconductor Device Having Metallized Interconnect Structure And Method Of Fabricaton	Issued	Lattice Semiconductor Corporation
10/187,236	6844757	United States	Converting Bits to Vectors In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/191,888	6650143	United States	FPGA Based Upon Transistor gate Oxide Breakdown	Issued	Lattice Semiconductor Corporation
10/194,771	7028281	United States	FPGA With Register-Intensive Architecture	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 195

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/200,645	6714066	United States	Integrated Programmable Continuous Time Filter with Programmable Capacitor Arrays	Issued	Lattice Semiconductor Corporation
10/207,292	6683477	United States	Wide input programmable logic system and method	Issued	Lattice Semiconductor Corporation
10/210,367	6938197	United States	CRC Calculation System And Method For A Packet Arriving On An N-Byte Wide Bus	Issued	Lattice Semiconductor Corporation
10/211,125	6545313	United States	EEPROM tunnel window for program injection via P+ contacted inversion	Issued	Lattice Semiconductor Corporation
10/219,046	6650142	United States	Enhanced CPLD Macrocell Module Having Selectable Bypass of Steering-based Resource Allocation and Methods of Use	Issued	Lattice Semiconductor Corporation
10/233,021	7043511	United States	Performing Conditional Operations In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/232,912	6841447	United States	EEPROM Device Having An Isolation -Bounded Tunnel Capacitor And Fabrication Process	Issued	Lattice Semiconductor Corporation
10/235,380	6725442	United States	Scalable and parallel processing methods and structures for testing configurable interconnect network in FPGA device	Issued	Lattice Semiconductor Corporation
10/236,829	6842372	United States	EEPROM Cell Having Floating Gate Transistor Within a Cell Well And a Process For Fabricating the Memory Cell	Issued	Lattice Semiconductor Corporation
10/236,114	6833602	United States	Device Having Electrically Isolated Low Voltage And High Voltage Regions And Process For Fabricating the Device	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 196

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/236,718	6649514	United States	EEPROM Device Having Improved Data Retention And Process for Fabricating The Device	Issued	Lattice Semiconductor Corporation
10/242,809	6738306	United States	Multiport SRAM Cell	Issued	Lattice Semiconductor Corporation
10/243,014	6917536	United States	Memory access Circuit and Method for reading and writing data with the same clock signal	Issued	Lattice Semiconductor Corporation
10/251,608	6700154	United States	EEPROM cell with trench coupling capacitor	Issued	Lattice Semiconductor Corporation
10/255,474	6907592	United States	Method of Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,875	6809551	United States	Method of Optimizing Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,499	6803787	United States	State Machine In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,656	6812738	United States	Vector Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/263,251	6748575	United States	Programming Programmable Logic Devices Using Hidden Switches	Issued	Lattice Semiconductor Corporation
10/263,507	6846714	United States	Voltage Limted EEPROM Device And Process For Fabricating the Device	Issued	Lattice Semiconductor Corporation
10/266,361	6639434	United States	Low voltage differential signaling systems and methods	Issued	Lattice Semiconductor Corporation
10/269,804	7111183	United States	Expansion method for complex power-sequencing applications	Issued	Lattice Semiconductor Corporation
10/269,450	6791394	United States	Power Supply Control Circuits	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 197

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/269,439	6762618	United States	Innovative verify scheme for two level GRP fuse in programmable bus switching family	Issued	Lattice Semiconductor Corporation
10/272,582	6901572	United States	Power Sequence Controller Programming Technique	Issued	Lattice Semiconductor Corporation
10/278,415	6639449	United States	Asynchronous glitch-free clock multiplexer	Issued	Lattice Semiconductor Corporation
10/282,524	7051261	United States	Turbo Encoder With Reduced Processing Delay	Issued	Lattice Semiconductor Corporation
10/283,765	6700823	United States	Programmable common mode termination for differential input/output circuits	Issued	Lattice Semiconductor Corporation
10/288,667	7000210	United States	Adaptive Adjustment Of Constraints During PLD Placement Processing	Issued	Lattice Semiconductor Corporation
10/288,668	6813754	United States	Placement Processing For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/300,190	6825733	United States	Low Jitter Integrated Phase Locked Loop With Broad Tuning Range	Issued	Lattice Semiconductor Corporation
10/302,439	6797568	United States	Flash Technology Transistors and Method For Forming Same	Issued	Lattice Semiconductor Corporation
10/308,420	6710641	United States	Low Voltage Bandgap Reference Circuit	Issued	Lattice Semiconductor Corporation
10/309,302	6650188	United States	Improved Coupling For LC-Based VCO	Issued	Lattice Semiconductor Corporation
10/334,642	6777979	United States	FIFO memory architecture	Issued	Lattice Semiconductor Corporation
10/338,619	6753696	United States	Programmable optimized-distribution logic allocator for	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 198

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			a high-density complex PLD		Corporation
10/365,083	7034596	United States	Adaptive input logic for phase adjustments	Issued	Lattice Semiconductor Corporation
10/368,023	6915323	United States	Macrocells Supporting A Carry Cascade	Issued	Lattice Semiconductor Corporation
10/366,956	6788101	United States	Programmable input buffer for differential and single-ended signals	Issued	Lattice Semiconductor Corporation
10/367,323	6812869	United States	Noise Reduction Techniques For Programmable I/O Circuits	Issued	Lattice Semiconductor Corporation
10/370,232	6861870	United States	Dynamic Cross point Switch With Shadow Memory Architecture	Issued	Lattice Semiconductor Corporation
10/377,320	6859066	United States	Bank based input/output buffers in field programmable gate arrays with multiple reference voltages	Issued	Lattice Semiconductor Corporation
10/387,814	7305047	United States	Automatic lane assignment for Receiver	Issued	Lattice Semiconductor Corporation
10/387,243	7339952	United States	Pointer Processing For Optical Communication Systems	Issued	Lattice Semiconductor Corporation
10/391,094	6870395	United States	PLDs With Integrated Standard Cell Logic Blocks	Issued	Lattice Semiconductor Corporation
10/392,751	RE39510	United States	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	Issued	Lattice Semiconductor Corporation
10/397,669	6967500	United States	Electronic Circuit With OnChip Programmable Terminations	Issued	Lattice Semiconductor Corporation
10/400,705	6873187	United States	Method and Apparatus for Controlling Signal Distribution In An Electronic	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 199

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Circuit		
10/406,050	7000212	United States	Hierarchical General Interconnect Architecture For High Density FPGA's	Issued	Lattice Semiconductor Corporation
10/409,543	6986004	United States	FIFO memory with programmable data port widths	Issued	Lattice Semiconductor Corporation
10/417,290	6879184	United States	Programmable logic device architecture based on arrays of LUT-based Boolean terms	Issued	Lattice Semiconductor Corporation
10/425,863	6903575	United States	Scalable device architecture for high-speed interfaces	Issued	Lattice Semiconductor Corporation
10/425,862	6894530	United States	Programmable And Fixed Logic Circuitry For High-Speed Interfaces	Issued	Lattice Semiconductor Corporation
10/428,889	6879182	United States	CPLD with multi-function blocks and distributed memory	Issued	Lattice Semiconductor Corporation
10/428,885	6861871	United States	Cascaded logic block architecture for complex programmable logic devices	Issued	Lattice Semiconductor Corporation
10/428,888	6864713	United States	Multi-Stage Interconnect Architecture For Complex Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/428,982	6922078	United States	Enhanced wide and deep logic capability for high density, high performance CPLDs	Issued	Lattice Semiconductor Corporation
10/439,602	6828823	United States	Non-volatilie and reconfigurable PLDs	Issued	Lattice Semiconductor Corporation
10/441,814	7039842	United States	Measuring Propagation Delays of Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/447,120	7301996	United States	skew cancellation for source synchronous clock and data signals	Issued	Lattice Semiconductor Corporation
10/447,451	7009433	United States	Digitally Controlled Delay Cells	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/457,630	7304863	United States	Integrated Circuit Including External Electronic Components With Low Insertion Loss	Issued	Lattice Semiconductor Corporation
10/459,091	6879598	United States	Flexible Media Access Control Architecture	Issued	Lattice Semiconductor Corporation
10/460,385	6856171	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
10/463,781	6861868	United States	High Speed Interface For A Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/464,083	6882555	United States	Bi-directional buffering for memory data lines	Issued	Lattice Semiconductor Corporation
10/600,042	6822477	United States	Integrated Circuit And Associated Design Method Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/610,253	6977408	United States	High-Performance Non-volatile Memory Device and Fabrication Process	Issued	Lattice Semiconductor Corporation
10/613,460	7132903	United States	Noise-shielding, switch-controlled load circuitry for oscillators and the like	Issued	Lattice Semiconductor Corporation
10/613,462	6952115	United States	Programmable I/O Interfaces For FPGAs And Other PLDs	Issued	Lattice Semiconductor Corporation
10/617,980	6958625	United States	PLD With Hardwired Microsequencer	Issued	Lattice Semiconductor Corporation
10/619,711	6903573	United States	Programmable Logic Device With Enhanced Wide Input Product Term Cascading	Issued	Lattice Semiconductor Corporation
10/620,286	6919736	United States	FPGA having partitionable embedded memory with configurable depth and width	Issued	Lattice Semiconductor Corporation
10/619,645	7098685	United States	Scalable Serializer-Deserializer Architecture and	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 201

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Programmable Interface		Corporation
10/620,147	7032203	United States	Algorithm to increase logic input width by cascading product terms	Issued	Lattice Semiconductor Corporation
10/624,965	6940309	United States	Programmable Logic Device With A Memory-Based Finite State Machine	Issued	Lattice Semiconductor Corporation
10/626,089	6737702	United States	Zero Power Memory Cell with Reduced Threshold Voltage	Issued	Lattice Semiconductor Corporation
10/628,656	6970047	United States	Programmable lock detector and corrector	Issued	Lattice Semiconductor Corporation
10/628,657	6924659	United States	Programmable Signal Termination for FPGAs and the Like	Issued	Lattice Semiconductor Corporation
10/629,223	7019577	United States	Clock Generator	Issued	Lattice Semiconductor Corporation
10/629,512	6903574	United States	Memory Access Via Serial Memory Interface	Issued	Lattice Semiconductor Corporation
10/629,221	6885227	United States	Clock Generator With Skew Control	Issued	Lattice Semiconductor Corporation
10/640,804	6877667	United States	Integrated Circuit And Associated Design Method With Antenna Error Control Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/640,828	6838904	United States	Enhanced CPLD Macrocell Module Having Selectable Bypass of Steering-Based Resource Allocation	Issued	Lattice Semiconductor Corporation
10/641,260	6940779	United States	Programmable broadcasting initialization of embedded memory blocks on FPGA	Issued	Lattice Semiconductor Corporation
10/642,370	6924664	United States	FPGA	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/655,686	6842037	United States	Shared Transmission Line Communication System and Method	Issued	Lattice Semiconductor Corporation
10/660,814	7038490	United States	Delay matched ASIC conversion of a PLD	Issued	Lattice Semiconductor Corporation
10/665,920	6970022	United States	Controlled hysteresis comparator with rail-to-rail input	Issued	Lattice Semiconductor Corporation
10/671,378	6943583	United States	Programmable I/O structure for FPGAs and the like having reduced pad capacitance	Issued	Lattice Semiconductor Corporation
10/671,363	6943582	United States	Programmable I/O structure for FPGAs and the Like Having Shared Circuitry	Issued	Lattice Semiconductor Corporation
10/671,756	6909663	United States	Multiport Memory With Twisted Bitlines	Issued	Lattice Semiconductor Corporation
10/676,536	7269771	United States	Semiconductor Device Adapted For Forming Multiple Scan Chains	Issued	Lattice Semiconductor Corporation
10/687,468	6809674	United States	Analog-to-digital converters	Issued	Lattice Semiconductor Corporation
10/699,321	7067883	United States	Lateral High-Voltage Junction Device	Issued	Lattice Semiconductor Corporation
10/701,005	7091763	United States	Clock generation	Issued	Lattice Semiconductor Corporation
10/704,025	7088134	United States	PLD With Flexible Memory Allocation And Routing	Issued	Lattice Semiconductor Corporation
10/726,972	7100058	United States	Programmable Power Management System And Method	Issued	Lattice Semiconductor Corporation
10/728,685	7187157	United States	Power supply remote voltage sensing	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 203

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/737,514	6981381	United States	Linear Thermoelectric Device Driver	Issued	Lattice Semiconductor Corporation
10/744,353	7132864	United States	Method for configuring multiple-output phase-locked loop frequency synthesizer	Issued	Lattice Semiconductor Corporation
10/769,174	7024646	United States	Electrostatic Discharge Simulation	Issued	Lattice Semiconductor Corporation
10/768,643	7019584	United States	Output Stages For High Current Low Noise Bandgap Reference Circuit Implementations	Issued	Lattice Semiconductor Corporation
10/782,564	6972986	United States	Combination FPGA	Issued	Lattice Semiconductor Corporation
10/783,886	7081771	United States	Upgradeable And Reconfigurable Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/791,073	7191388	United States	Fast diagonal interleaved parity (DIP) calculator	Issued	Lattice Semiconductor Corporation
10/794,079	7257727	United States	Timer Systems and Methods	Issued	Lattice Semiconductor Corporation
10/794,524	7017063	United States	systems and methods for controlling voltage regulator module power supplies	Issued	Lattice Semiconductor Corporation
10/794,498	7028201	United States	Powering up a device having digital and analog circuitry	Issued	Lattice Semiconductor Corporation
10/797,759	7068556	United States	Sense Amplifier Systems and Methods	Issued	Lattice Semiconductor Corporation
10/809,180	7234030	United States	Table based scheduler for FIFOs and the like	Issued	Lattice Semiconductor Corporation
10/809,658	7095247	United States	Configuring FPGAs and the like using one or more serial memory devices	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 204

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/815,403	7167032	United States	Self-adjusting schmitt trigger	Issued	Lattice Semiconductor Corporation
10/817,215	7081781	United States	Charge pump for a low-voltage wide-tuning range phase-locked loop	Issued	Lattice Semiconductor Corporation
10/829,865	6998896	United States	Dynamic gain adjustment systems and method for metastability resistance	Issued	Lattice Semiconductor Corporation
10/834,528	6998906	United States	Low pass filter systems and methods	Issued	Lattice Semiconductor Corporation
10/837,086	7307319	United States	High Voltage Protection Device And Process	Issued	Lattice Semiconductor Corporation
10/842,345	7002418	United States	Control Signal Generation ...	Issued	Lattice Semiconductor Corporation
10/841,987	7224213	United States	switched-capacitor ripple-smoothing filter	Issued	Lattice Semiconductor Corporation
10/843,708	7061269	United States	IO buffer architecture for programmable devices	Issued	Lattice Semiconductor Corporation
10/856,100	7196551	United States	Current Mode Logic Buffer	Issued	Lattice Semiconductor Corporation
10/857,667	7064973	United States	Combination FPGA	Issued	Lattice Semiconductor Corporation
10/885,419	7116585	United States	Memory Systems And Methods	Issued	Lattice Semiconductor Corporation
10/910,091	7215591	United States	Byte enable logic for memory	Issued	Lattice Semiconductor Corporation
10/912,943	7471752	United States	Data Transmission Synchronization	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 205

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/928,563	7078286	United States	Process for fabricating a semiconductor device having electrically isolated low voltage and high voltage regions	Issued	Lattice Semiconductor Corporation
10/929,199	7484144	United States	Testing embedded memory in an integrated circuit	Issued	Lattice Semiconductor Corporation
10/944,978	7135886	United States	FPGA Using Both Volatile and NonVolatile Memory Cell Properties	Issued	Lattice Semiconductor Corporation
10/974,453	7307912	United States	Variable data width memory systems and methods	Issued	Lattice Semiconductor Corporation
10/973,750	7149129	United States	memory output data systems and methods with feedback	Issued	Lattice Semiconductor Corporation
10/974,107	7164290	United States	FPGA Logic Unit	Issued	Lattice Semiconductor Corporation
10/974,305	7129749	United States	PLD Having A Configurable DRAM With Transparent Refresh	Issued	Lattice Semiconductor Corporation
10/978,899	7376872	United States	Testing embedded memory in integrated circuits such as progammable logic circuits	Issued	Lattice Semiconductor Corporation
10/996,283	7161862	United States	Low power asynchronous sense amp	Issued	Lattice Semiconductor Corporation
11/007,954	7230810	United States	Dynamic over-voltage protection scheme for integrated circuit devices	Issued	Lattice Semiconductor Corporation
11/012,550	7215149	United States	Interface circuitry for electrical systems	Issued	Lattice Semiconductor Corporation
11/012,548	7215148	United States	Programmable current LVDS output buffer	Issued	Lattice Semiconductor Corporation
11/015,265	7177221	United States	Method of initializing configurable multi-port	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 206

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			embedded memory blocks in an FPGA		Corporation
11/016,665	7187203	United States	Cascadable memory	Issued	Lattice Semiconductor Corporation
11/015,369	7177207	United States	Sense amplifier timing	Issued	Lattice Semiconductor Corporation
11/036,630	7257750	United States	Self-verification of configuration memory in PLDs	Issued	Lattice Semiconductor Corporation
11/036,738	7242053	United States	EEPROM Device with voltage-limiting charge pump circuit	Issued	Lattice Semiconductor Corporation
11/040,772	7208975	United States	Serdes with programmable I/O architecture	Issued	Lattice Semiconductor Corporation
11/041,319	7183798	United States	Synchronous memory	Issued	Lattice Semiconductor Corporation
11/044,089	7109754	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
11/044,149	7109756	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
11/044,508	7034599	United States	Clock Generator With Skew Control	Issued	Lattice Semiconductor Corporation
11/054,011	7221607	United States	Mult-port memory systems and methods for bit line coupling	Issued	Lattice Semiconductor Corporation
11/055,280	6975137	United States	PLDs With Integrated Standard Cell Logic Blocks	Issued	Lattice Semiconductor Corporation
11/054,750	7382293	United States	Data Decompression	Issued	Lattice Semiconductor Corporation
11/054,855	7589648	United States	Data Decompression	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/064,477	7532646	United States	Distributed multiple channel alignment scheme	Issued	Lattice Semiconductor Corporation
11/071,356	7245154	United States	Differential Input Receiver with Programmable Failsafe	Issued	Lattice Semiconductor Corporation
11/070,926	7057397	United States	Output Impedance Measurement Techniques	Issued	Lattice Semiconductor Corporation
11/083,625	7376204	United States	Detection of Unknown symbol rate in a digitally modulated signal	Issued	Lattice Semiconductor Corporation
11/098,713	7265578	United States	In-System Programming Of a Non-Compliant Device Using Multiple Interfaces Of A PLD	Issued	Lattice Semiconductor Corporation
11/100,718	7397274	United States	In-System Programming Of a Non-Compliant Device Using Multiple Interfaces Of A PLD	Issued	Lattice Semiconductor Corporation
11/108,927	7193436	United States	Fast Processing Path Using FPGA Logic Units	Issued	Lattice Semiconductor Corporation
11/109,301	7630464	United States	Analog-to-digital systems and methods	Issued	Lattice Semiconductor Corporation
11/109,966	6977521	United States	FPGA	Issued	Lattice Semiconductor Corporation
11/121,326	7400171	United States	Electronic Switch Having Extended Voltage Range	Issued	Lattice Semiconductor Corporation
11/134,152	7009423	United States	Programmable I/O Interfaces For FPGAs And Other PLDs	Issued	Lattice Semiconductor Corporation
11/157,345	7685483	United States	Design-For-Test features for a memory in an FPGA	Issued	Lattice Semiconductor Corporation
11/157,349	7378879	United States	Decoding systems and methods	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 208

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/165,709	7256613	United States	Programmable Interconnect Architecture for PLDs	Issued	Lattice Semiconductor Corporation
11/165,853	7342838	United States	PLD With A Double Data Rate SDRAM Interface	Issued	Lattice Semiconductor Corporation
11/185,242	7519139	United States	Signal monitoring systems and methods	Issued	Lattice Semiconductor Corporation
11/187,179	7342846	United States	address decoding systems and methods	Issued	Lattice Semiconductor Corporation
11/187,114	7253674	United States	Fine output clock phase alignment circuitry	Issued	Lattice Semiconductor Corporation
11/189,067	7505752	United States	Receiver used for differential signaling and reference voltage signaling with programmable common mode	Issued	Lattice Semiconductor Corporation
11/194,871	7414913	United States	Bitline twisting scheme for a multiport memory	Issued	Lattice Semiconductor Corporation
11/194,356	7262630	United States	Dynamic programmable termination for parallel and differential schemes	Issued	Lattice Semiconductor Corporation
11/199,287	7599457	United States	clock-and-data-recovery system having a multi-phase clock generator for one or more channel circuits	Issued	Lattice Semiconductor Corporation
11/200,983	7295035	United States	Programmable Logic Device With Enhanced Logic Block Architecture	Issued	Lattice Semiconductor Corporation
11/200,941	7411419	United States	I/O Systems and Methods	Issued	Lattice Semiconductor Corporation
11/202,149	7606851	United States	Correlator having user-defined processing	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/201,620	7187586	United States	Flash memory erase verification systems and methods	Issued	Lattice Semiconductor Corporation
11/206,282	RE40311	United States	Zero Power Programmable Memory Cell	Issued	Lattice Semiconductor Corporation
11/226,695	7301182	United States	Circuit layout for improved performance while preserving or improving density	Issued	Lattice Semiconductor Corporation
11/230,087	7167405	United States	Data transfer verification systems and methods	Issued	Lattice Semiconductor Corporation
11/235,616	7376037	United States	PLD with power-saving architecture	Issued	Lattice Semiconductor Corporation
11/236,967	7405446	United States	Electrostatic Protection Systems and Methods	Issued	Lattice Semiconductor Corporation
11/243,255	7088132	United States	Configuring FPGAs and the like using one or more serial memory devices	Issued	Lattice Semiconductor Corporation
11/251,682	7196963	United States	Address isolation for user-defined configuration memory in programmable devices	Issued	Lattice Semiconductor Corporation
11/252,094	7263024	United States	Clock reset address decoder for block memory	Issued	Lattice Semiconductor Corporation
11/252,126	7061275	United States	FPGA	Issued	Lattice Semiconductor Corporation
11/257,137	7685215	United States	Fast-carry arithmetic circuit using a multi-input LUT	Issued	Lattice Semiconductor Corporation
11/257,641	7317343	United States	PULSE-GENERATION CIRCUIT HAVING PULSE GENERATORS AND SET-RESET LATCHES	Issued	Lattice Semiconductor Corporation
11/260,097	7212051	United States	Control signal generation for a low jitter switched-capacitor frequency synthesizer	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/281,651	7495495	United States	Digital I/O Timing Control	Issued	Lattice Semiconductor Corporation
11/287,720	7327159	United States	Interface Block Architectures	Issued	Lattice Semiconductor Corporation
11/290,205	7242634	United States	Pseudo-dynamic word-line driver	Issued	Lattice Semiconductor Corporation
11/293,941	7538574	United States	Transparent Field Reconfiguration for PLDs	Issued	Lattice Semiconductor Corporation
11/302,097	7620839	United States	Jitter Tolerant Delay-Locked Loop Circuit	Issued	Lattice Semiconductor Corporation
11/300,886	7495467	United States	Temperature independent, linear on-chip termination resistance	Issued	Lattice Semiconductor Corporation
11/332,986	7382169	United States	Systems and Methods for Reducing Static Phase Error	Issued	Lattice Semiconductor Corporation
11/335,890	7439783	United States	Phase-Locked Loop Systems And Methods	Issued	Lattice Semiconductor Corporation
11/345,713	7547995	United States	dynamic over voltage protection scheme for interface circuitry	Issued	Lattice Semiconductor Corporation
11/346,817	7554357	United States	Efficient Configuration of Daisy-Chained Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
11/350,436	7375549	United States	Reconfiguration of PLDs	Issued	Lattice Semiconductor Corporation
11/356,805	7277348	United States	Memory Cell Comprising And OTP NV Memory Unit And SRAM Unit	Issued	Lattice Semiconductor Corporation
11/360,337	7355441	United States	PLD with distributed memory and non-volatile memory	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/361,584	7596744	United States	Auto recovery from volatile soft error upsets (SEUs)	Issued	Lattice Semiconductor Corporation
11/362,289	7759926	United States	dynamic phase offset measurement	Issued	Lattice Semiconductor Corporation
11/361,643	7446573	United States	Comparator Systems And Methods	Issued	Lattice Semiconductor Corporation
11/398,437	7459931	United States	PLDs with transparent field reconfiguration	Issued	Lattice Semiconductor Corporation
11/397,985	7554358	United States	PLDs with user non-volatile memory	Issued	Lattice Semiconductor Corporation
11/416,881	7623378	United States	Selective programming of non-volatile memory facilitated by security fuses	Issued	Lattice Semiconductor Corporation
11/435,956	7102934	United States	Sense Amplifier Systems and Methods	Issued	Lattice Semiconductor Corporation
11/442,186	7411417	United States	Selective loading of configuration data into configuration memory cells	Issued	Lattice Semiconductor Corporation
11/446,548	7378873	United States	PLD providing a serial peripheral interface	Issued	Lattice Semiconductor Corporation
11/445,620	7378872	United States	PLD architecture with multiple slice types	Issued	Lattice Semiconductor Corporation
11/446,542	7385417	United States	Dual slice architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/446,351	7397276	United States	Logic block control architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/446,308	7546498	United States	PLDs with custom identification systems and methods	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 212

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/446,309	7495970	United States	Flexible memory architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/447,591	7631223	United States	PLD methods and systems for providing multi-boot configuration data support	Issued	Lattice Semiconductor Corporation
11/452,714	7463060	United States	PLD and method of testing	Issued	Lattice Semiconductor Corporation
11/455,315	7215139	United States	Upgradeable And Reconfigurable Programmable Logic Device	Issued	Lattice Semiconductor Corporation
11/425,273	7702100	United States	Key generation for advanced encryption standard (AES) decryption and the like	Issued	Lattice Semiconductor Corporation
11/425,881	7657773	United States	Clock distribution chip for generating both zero-delay and non-zero-delay clock signals	Issued	Lattice Semiconductor Corporation
11/477,759	7348914	United States	Methods and systems to align output signals of an analog-to-digital converter	Issued	Lattice Semiconductor Corporation
11/487,647	7636259	United States	Flash memory array with independently erasable sectors	Issued	Lattice Semiconductor Corporation
11/487,751	7512015	United States	Negative voltage blocking for embedded memories	Issued	Lattice Semiconductor Corporation
11/492,687	7466190	United States	Charge pump with four-well transistors	Issued	Lattice Semiconductor Corporation
11/494,862	7521969	United States	Switch sequencing circuit systems and methods	Issued	Lattice Semiconductor Corporation
11/461,222	7411432	United States	Integrated circuits and complementary CMOS circuits for frequency dividers	Issued	Lattice Semiconductor Corporation
11/498,645	7675313	United States	Methods and systems for storing a security key using programmable fuses	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/498,646	7605606	United States	Area efficient routing architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/530,620	7456672	United States	Clock systems and methods	Issued	Lattice Semiconductor Corporation
11/533,188	7511641	United States	Efficient bitstream compression	Issued	Lattice Semiconductor Corporation
11/551,459	7831754	United States	Multiple Communication Channel Configuration Systems And Methods	Issued	Lattice Semiconductor Corporation
11/556,528	7663401	United States	Multiplexer initialization systems and methods	Issued	Lattice Semiconductor Corporation
11/593,274	7535258	United States	Programmable Voltage LVDS Output Buffer	Issued	Lattice Semiconductor Corporation
11/557,808	7725803	United States	PLD programming verification systems and methods	Issued	Lattice Semiconductor Corporation
11/638,156	7429875	United States	Low Static Current Drain Logic Circuit	Issued	Lattice Semiconductor Corporation
11/643,288	7443192	United States	Output buffer with digital slew control	Issued	Lattice Semiconductor Corporation
11/624,021	7623391	United States	Data transfer verification systems and methods	Issued	Lattice Semiconductor Corporation
11/671,948	7576563	United States	Flexible High Fan-out Signal Routing Systems and Methods	Issued	Lattice Semiconductor Corporation
11/675,246	7313025	United States	Flash memory erase verification systems and methods	Issued	Lattice Semiconductor Corporation
11/676,071	7430706	United States	Fast diagonal interleaved parity (DIP) calculator	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 214

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/680,526	7598765	United States	Redundancy for Configuration RAM	Issued	Lattice Semiconductor Corporation
11/691,003	7536615	United States	Logic analyzer systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/691,040	7743296	United States	Logic analyzer systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/737,702	7509598	United States	Clock Boosting Systems and Methods	Issued	Lattice Semiconductor Corporation
11/750,790	7401280	United States	Self-verification of configuration memory in PLDs	Issued	Lattice Semiconductor Corporation
11/750,616	7632011	United States	Integrated Circuit Temperature Sensors Systems and Methods	Issued	Lattice Semiconductor Corporation
11/760,411	8065574	United States	Real Soft Error Detect Scheme for Testing	Issued	Lattice Semiconductor Corporation
11/761,221	7570078	United States	PLD Providing A Serial Peripheral Interfaces	Issued	Lattice Semiconductor Corporation
11/778,457	7573770	United States	Distributed front-end FIFO for source-synchronized interfaces with non-continuous clocks	Issued	Lattice Semiconductor Corporation
11/779,246	7446679	United States	FPGA data compression using combined RLE BE, LZ, Row LZ and BE ROW encoding	Issued	Lattice Semiconductor Corporation
11/863,016	7681160	United States	Weight based look up table collapsing for programmable logic devices	Issued	Lattice Semiconductor Corporation
11/865,556	7539076	United States	Variable data width memory systems and methods	Issued	Lattice Semiconductor Corporation
11/869,019	7616029	United States	Hysteresis-based processing for applications such as signal bias monitors	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 215

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/872,950	7586344	United States	Dynamic delay or advance adjustment of oscillating signal phase	Issued	Lattice Semiconductor Corporation
11/875,748	7757198	United States	Scan chain systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/877,434	7411414	United States	Single-Ended Output Driver Buffer	Issued	Lattice Semiconductor Corporation
11/924,088	8132040	United States	Channel-to-channel deskew systems and methods	Issued	Lattice Semiconductor Corporation
11/934,711	7573291	United States	Programmable Logic Device With Enhanced Logic Block Architecture	Issued	Lattice Semiconductor Corporation
11/937,328	7788620	United States	An IO placement systems and methods to reduce SSO noise	Issued	Lattice Semiconductor Corporation
11/937,300	7895555	United States	Simultaneous Switching Output Noise Estimation and Reduction Systems and Methods	Issued	Lattice Semiconductor Corporation
11/939,787	7863931	United States	Flexible Delay Cell Architecture	Issued	Lattice Semiconductor Corporation
11/941,031	7902865	United States	Compression and decompression of configuration data using repeated data frames	Issued	Lattice Semiconductor Corporation
11/941,006	7535253	United States	Method of Retaining Register Data during Field Update of PLD	Issued	Lattice Semiconductor Corporation
11/947,662	7788623	United States	Composite wire indexing for PLDs	Issued	Lattice Semiconductor Corporation
11/949,130	7586325	United States	IC having independent voltage and process/temperature control	Issued	Lattice Semiconductor Corporation
12/001,600	7728625	United States	Serial interface for PLDs	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/957,598	7605609	United States	A programmable level shifter optimized for high performance and low power.	Issued	Lattice Semiconductor Corporation
11/959,329	7630259	United States	PLD with built in self test	Issued	Lattice Semiconductor Corporation
11/970,212	7646643	United States	Process charging monitor for nonvolatile memory	Issued	Lattice Semiconductor Corporation
12/019,526	7787326	United States	PLD With Mult-Rate SDRAM Interface	Issued	Lattice Semiconductor Corporation
12/021,202	8069329	United States	Dynamic Multiple Pattern Configuration Scheme For Volatile FPGAs	Issued	Lattice Semiconductor Corporation
12/044,842	7652500	United States	Reconfiguration of PLDs	Issued	Lattice Semiconductor Corporation
12/055,170	7890913	United States	Wire Mapping For PLDs	Issued	Lattice Semiconductor Corporation
12/060,776	7459935	United States	PLD With Distributed Memory	Issued	Lattice Semiconductor Corporation
12/061,885	7831856	United States	Detection of Timing Errors in Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/099,933	7661878	United States	On-Chip Temperature Sensor For An Integrated Circuit	Issued	Lattice Semiconductor Corporation
12/100,859	7558143	United States	Programmable Logic Device With Power-Saving Architecture	Issued	Lattice Semiconductor Corporation
12/105,146	7557606	United States	Synchronization Of Data Signals And Clock Signals For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/105,959	7696784	United States	PLD With Multiple Slice	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 217

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Types		Corporation
12/107,883	7560953	United States	Power Management Systems And Methods for PLDs	Issued	Lattice Semiconductor Corporation
12/122,489	7897448	United States	Formation Of High Voltage Transistor With High Breakdown Voltage	Issued	Lattice Semiconductor Corporation
12/146,042	8463832	United States	Digital Signal Processing Block Architecture For PLD	Issued	Lattice Semiconductor Corporation
12/164,265	7592834	United States	Logic Block Control Architectures For PLDs	Issued	Lattice Semiconductor Corporation
12/182,940	8261160	United States	Serial data recovery out of 8 samples with FPGAs	Issued	Lattice Semiconductor Corporation
12/186,027	7579865	United States	Selective Loading Of Configuration Data Into Configuration Memory Cells	Issued	Lattice Semiconductor Corporation
12/188,120	7605602	United States	Low-Power Output Driver Buffer Circuit	Issued	Lattice Semiconductor Corporation
12/238,959	7911229	United States	Programmable Signal Routing Systems	Issued	Lattice Semiconductor Corporation
12/273,868	7663419	United States	Clock Systems And Methods	Issued	Lattice Semiconductor Corporation
12/277,217	8112731	United States	Congestion-driven placement based on region interconnection for FPGA	Issued	Lattice Semiconductor Corporation
12/323,974	7992120	United States	congestion estimation based on pass probability net estimation process	Issued	Lattice Semiconductor Corporation
12/327,128	7656193	United States	Programmable Logic Device And Method Of Testing	Issued	Lattice Semiconductor Corporation
12/337,502	8856718	United States	Precise Congestion Estimation for FPGA Router	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 218

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
12/341,929	8181139	United States	Multi-Priority Placement	Issued	Lattice Semiconductor Corporation
12/370,039	7714608	United States	Temperature-Independent, Linear On-Chip Termination Resistance	Issued	Lattice Semiconductor Corporation
12/389,149	7957208	United States	Flexible memory architectures for PLDs	Issued	Lattice Semiconductor Corporation
12/402,751	7844243	United States	Receiver used for differential signaling and reference voltage signaling with programmable common mode	Issued	Lattice Semiconductor Corporation
12/406,772	8069431	United States	An alternative method for pin swapping in FPGA routing	Issued	Lattice Semiconductor Corporation
12/408,047	8086986	United States	Clock Boosting Systems And Methods	Issued	Lattice Semiconductor Corporation
12/409,757	7675321	United States	Dual-Slice Architectures For PLDs	Issued	Lattice Semiconductor Corporation
12/413,787	7808405	United States	Efficient Bitstream Compression	Issued	Lattice Semiconductor Corporation
12/430,848	7741865	United States	Soft Error Upset Hardened Integrated Circuit Systems And Methods	Issued	Lattice Semiconductor Corporation
12/464,822	7876125	United States	Method of Retaining Register Data during Field Update of PLD	Issued	Lattice Semiconductor Corporation
12/465,444	7868654	United States	Economical way to improve volatile FPGA boot up data throughput by utilizing one or more SPI boot PROMs w/o sacrificing additional FPGA pins	Issued	Lattice Semiconductor Corporation
12/467,800	7737723	United States	Transparent Field Reconfiguration for PLDs	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
12/476,155	8044682	United States	FPGA Having Low Power, Fast Carry Chain	Issued	Lattice Semiconductor Corporation
12/480,565	7702977	United States	PLDs with custom identification systems and methods	Issued	Lattice Semiconductor Corporation
12/494,822	8165164	United States	Circuit For In-System Reconfigurable Mapping Of IQ Data Into A CPRI Basic Frame	Issued	Lattice Semiconductor Corporation
12/502,141	7724029	United States	Power Management For Integrated Circuits Such As Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/511,388	7768300	United States	PLD Providing A Serial Peripheral Interfaces	Issued	Lattice Semiconductor Corporation
12/512,944	8255733	United States	Method of selecting precise delay or skew shifts	Issued	Lattice Semiconductor Corporation
12/512,961	7969248	United States	VCO digital center frequency coarse tune algorithm	Issued	Lattice Semiconductor Corporation
12/538,810	7808855	United States	Distributed front-end FIFO for source-synchronized interfaces with non-continuous clocks	Issued	Lattice Semiconductor Corporation
12/561,140	8010871	United States	Auto recovery from volatile soft error upsets (SEUs)	Issued	Lattice Semiconductor Corporation
12/564,781	7746107	United States	Redundancy for Configuration RAM	Issued	Lattice Semiconductor Corporation
12/578,470	8122277	United States	Clock distribution chip	Issued	Lattice Semiconductor Corporation
12/578,492	8112656	United States	Clock distribution chip	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 220

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/607,868	7989911	United States	STI with trench liner of increased thickness	Issued	Lattice Semiconductor Corporation
12/607,333	7985656	United States	STI with trench liner of increased thickness	Issued	Lattice Semiconductor Corporation
12/611,262	8059470	United States	Flash memory array with independently erasable sectors	Issued	Lattice Semiconductor Corporation
12/626,289	7944765	United States	PLD with built in self test	Issued	Lattice Semiconductor Corporation
12/630,163	8060784	United States	PLD And Methods For Providing Multi-Boot Configuration Data Support	Issued	Lattice Semiconductor Corporation
12/637,884	8200179	United States	Combined Variable Gain Amplifier And Linear Equalizer With Independent Gain And Frequency Control	Issued	Lattice Semiconductor Corporation
12/698,283	8040152	United States	IO Ring Configuration Scheme with sharing of BC7 register	Issued	Lattice Semiconductor Corporation
12/706,227	7924054	United States	Latency measurement circuit for wireless communications applications	Issued	Lattice Semiconductor Corporation
12/709,685	7834652	United States	Methods and systems for storing a security key using programmable fuses	Issued	Lattice Semiconductor Corporation
12/729,952	8040159	United States	High Speed Comparator with Data Dependent Jitter Mitigation	Issued	Lattice Semiconductor Corporation
12/752,455	8384427	United States	Serial Peripheral Interface Daisy Chaining using a Flow-Through Option	Issued	Lattice Semiconductor Corporation
12/757,087	8664774	United States	A Method for Arranging IC Bondwires for the Reduction of Crosstalk	Issued	Lattice Semiconductor Corporation
12/786,359	8108754	United States	PLD programming verification systems and methods	Issued	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 221

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/813,540	8164499	United States	Shared-Array Multiple-Output Digital to Analog Converter	Issued	Lattice Semiconductor Corporation
12/813,573	8441292	United States	Method of delaying data from clock in 1UI steps	Issued	Lattice Semiconductor Corporation
12/818,544	7868646	United States	Soft Error Upset Hardened Integrated Circuit Systems And Methods	Issued	Lattice Semiconductor Corporation
12/871,764	8286116	United States	Composite Wire Indexing For PLDs	Issued	Lattice Semiconductor Corporation
12/977,011	8522126	United States	Method Of Blocking PLC Distributed SRAM Readback In User Mode	Issued	Lattice Semiconductor Corporation
12/976,412	8351287	United States	Bitline Floating Circuit For Power Reduction On SRAM Array	Issued	Lattice Semiconductor Corporation
12/976,520	8477549	United States	Strobed And Latched Readback Of SRAM Bits In A FPGA	Issued	Lattice Semiconductor Corporation
12/987,393	8274412	United States	Low Power SerDes With Built- In Word Alignment For Odd And Even Gearing Ratios	Issued	Lattice Semiconductor Corporation
13/006,622	8384428	United States	Programmable IO Pad - embedded function block	Issued	Lattice Semiconductor Corporation
13/007,804	8248136	United States	Low Power And Glitch-less Delay Element For High Speed Receiver Interface	Issued	Lattice Semiconductor Corporation
13/007,688	8324934	United States	Programmable Ratio Input Buffer	Issued	Lattice Semiconductor Corporation
13/026,555	8104009	United States	Wire Mapping For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
13/034,174	8058898	United States	Compression and Decompression Of Configuration Data Using	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Repeated Data Frames		
13/038,259	8368424	United States	Wakeup from sleep mode using slave I2C port or slave SPI port with powered down core logic	Issued	Lattice Semiconductor Corporation
13/038,270	8816718	United States	Slow Respond Mode Protocol For Synchronous Read	Issued	Lattice Semiconductor Corporation
13/037,703	8654600	United States	Current Sense Amplifier With Low Voltage Operation	Issued	Lattice Semiconductor Corporation
13/052,142	8553463	United States	Positive-To-Negative Voltage Discharge Circuit	Issued	Lattice Semiconductor Corporation
13/076,300	8319521	United States	Safe programming of key information into NV memory	Issued	Lattice Semiconductor Corporation
13/079,578	8314634	United States	Power Saving Standby Mode With Glitch-Less Output Controls	Issued	Lattice Semiconductor Corporation
13/079,595	8531222	United States	PLL Switchable Feedback Loops Among Internal And External Feedback Paths	Issued	Lattice Semiconductor Corporation
13/083,889	8138790	United States	Latency measurement circuit for wireless communications applications	Issued	Lattice Semiconductor Corporation
13/154,885	8441284	United States	Flexible Way To Incrementally Update Multi-Bit Data Registers	Issued	Lattice Semiconductor Corporation
13/155,547	8547075	United States	Filter And Stability Capacitor Reuse For On-Chip Dual Output Voltage Regulators	Issued	Lattice Semiconductor Corporation
13/164,108	8555217	United States	Cross-Probing Technology Between Software Plug-In Modules	Issued	Lattice Semiconductor Corporation
13/178,599	8539409	United States	Multiple silicon products from a common base set of masks	Issued	Lattice Semiconductor Corporation
13/178,536	8495264	United States	Packet And Control Symbol	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Alignment Circuit For SRIO		Corporation
13/193,984	8314632	United States	Placing ICs Into Ultra-Low Voltage Mode For Standby Purposes	Issued	Lattice Semiconductor Corporation
13/212,121	8451679	United States	Bit-Line Clamping Circuit To Improve Write Performance Of Dual-Port SRAM	Issued	Lattice Semiconductor Corporation
13/275,102	8169237	United States	High Speed Comparator with Data Dependent Jitter Mitigation	Issued	Lattice Semiconductor Corporation
13/299,507	8370691	United States	Testing of Soft Error Detection Logic For PLDs	Issued	Lattice Semiconductor Corporation
13/452,060	8823561	United States	In-System Reconfigurable Circuit For Mapping Data Words Of Different Lengths	Issued	Lattice Semiconductor Corporation
13/585,142	8461894	United States	Low Power And Glitch-less Delay Element For High Speed Receiver Interface	Issued	Lattice Semiconductor Corporation
13/616,173	8912933	United States	Low Power SerDes With Built- In Word Alignment For Odd And Even Gearing Ratios	Issued	Lattice Semiconductor Corporation
13/653,827	8710898	United States	Bandgap Reference Circuit Design With Triple-Trim Methodology For Mass Production	Issued	Lattice Semiconductor Corporation
13/680,947	8643398	United States	Placing ICs Into Low Voltage Mode For Standby Purposes	Issued	Lattice Semiconductor Corporation
13/685,385	8643168	United States	Input Capacitance Compensation In Package	Issued	Lattice Semiconductor Corporation
13/721,867	8686773	United States	In-System Margin Measurement Circuit	Issued	Lattice Semiconductor Corporation
13/738,265	8797064	United States	Low power, optimized H-bridge and CML driver	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
13/764,221	RE45200	United States	Programmable Signal Routing Systems Having Low Static Leakage	Issued	Lattice Semiconductor Corporation
13/857,919	8786482	United States	Analog-To-Digital-Converter	Issued	Lattice Semiconductor Corporation
13/892,948	8648636	United States	Method of Delaying Data from Clock in 1UI steps	Issued	Lattice Semiconductor Corporation
14/040,955	8829944	United States	Dynamic Power Supply Switching For Clock Signals	Issued	Lattice Semiconductor Corporation
13/155,261		United States	JTAG Based Parallel Measuring And Trimming for Time Based Parameters	Pending	Lattice Semiconductor Corporation
13/412,408		United States	Double Rate Throughput Processing Booster For DSP Slices	Pending	Lattice Semiconductor Corporation
13/466,463		United States	Early Match FIFO	Pending	Lattice Semiconductor Corporation
13/681,782		United States	Multi-channel transmitter synchronization circuitry	Pending	Lattice Semiconductor Corporation
13/777,243		United States	RAM Data Path Sense Leakage Abatement Circuit	Pending	Lattice Semiconductor Corporation
13/858,422		United States	Method To Enable And Disable Scan Test Mode Reliably Through JTAG Port With Maximum Scan Coverage	Pending	Lattice Semiconductor Corporation
13/868,738		United States	Loss of signal detection in high-speed serial link	Pending	Lattice Semiconductor Corporation
13/901,853		United States	Dual-Port SRAM With Bit Line Clamping	Pending	Lattice Semiconductor Corporation
13/904,861		United States	Bring up sequence for configurable PCIe IP in an	Pending	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 225

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			FPGA		Corporation
13/947,553		United States	Method For Hot Swapping Or Hot Plugging With Stable Supply-Side Reference Over Wide Voltage Range	Pending	Lattice Semiconductor Corporation
14/021,513		United States	Phase Locked Loop Circuit With Selectable Feedback Paths	Pending	Lattice Semiconductor Corporation
14/043,920		United States	Robust Serialized State-machine Interface Architecture Optimized for Implementation in Programmable Devices	Pending	Lattice Semiconductor Corporation
14/053,026		United States	ASB SW modeling methodology	Pending	Lattice Semiconductor Corporation
14/070,975		United States	Method to enable system board pin escape for tight ball pitch packages	Pending	Lattice Semiconductor Corporation
14/095,310		United States	A Novel ESD Implementation for 40nm FPGA	Pending	Lattice Semiconductor Corporation
14/136,482		United States	Automatic Quadrant Clock Assignment For Programmable Logic Devices	Pending	Lattice Semiconductor Corporation
14/137,443		United States	Using Critical Groups in FPGA Routing	Pending	Lattice Semiconductor Corporation
14/147,796		United States	A Hot Socket Implementation for General Purpose IO for 40nm FPGA	Pending	Lattice Semiconductor Corporation
14/172,678		United States	All Mosfet Circuit for Generating Accurate Collector Currents	Pending	Lattice Semiconductor Corporation
14/179,651		United States	LOW-VOLTAGE CURRENT SENSE AMPLIFIER	Pending	Lattice Semiconductor Corporation
14/194,484		United States	Logic Element Placement with Repacking Optimization	Pending	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 226

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/220,377		United States	DPHY using FPGA differential & single ended I/Os	Pending	Lattice Semiconductor Corporation
14/223,096		United States	DPHY using FPGA differential & single ended I/Os	Pending	Lattice Semiconductor Corporation
14/245,920		United States	Deterministic Dynamic Element Matching for Generating Precise Current Ratios	Pending	Lattice Semiconductor Corporation
14/271,331		United States	Inline Defect To Sort Test Correlation In Semiconductor Manufacturing	Pending	Lattice Semiconductor Corporation
14/271,955		United States	Performance-focused Adaptive Automatic Incremental Flow	Pending	Lattice Semiconductor Corporation
14/283,329		United States	Configuration logic controlled memory BIST (built-in self-test) for back-to-back initialization and readback of embedded block RAMs in FPGAs	Pending	Lattice Semiconductor Corporation
14/308,747		United States	A novel Output Driver drive strength and termination resistor continuously calibrating PVT compensation scheme	Pending	Lattice Semiconductor Corporation
14/313,443		United States	FPGA Hardware debug during post-config power-up and before logic analyzer connect	Pending	Lattice Semiconductor Corporation
14/313,778		United States	IOLOGIC Delay Cell Stealing for Holdtime Correction	Pending	Lattice Semiconductor Corporation
14/316,049		United States	Mapping Constant Multipliers To ICE Devices	Pending	Lattice Semiconductor Corporation
14/319,481		United States	Incrementer Absorption into Multiplier Logic	Pending	Lattice Semiconductor Corporation
14/320,169		United States	Method to Implement Mixed-	Pending	Lattice

DELL/HP/LENOVO EXHIBIT 1002
Page 227

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Width Mode Memory in Fixed-Mode Memory Architecture with Masking		Semiconductor Corporation
14/320,074		United States	Two Level Voltage Regulator scheme for SRAM Operation	Pending	Lattice Semiconductor Corporation
14/327,811		United States	Implementing Dual Boot For XO2 and Multiple ASCs	Pending	Lattice Semiconductor Corporation
14/339,164		United States	A unique method to optimize clock to out path	Pending	Lattice Semiconductor Corporation
14/339,229		United States	New method on bus-based clock_to_out timing optimization	Pending	Lattice Semiconductor Corporation
14/482,001		United States	Physically-aware Programmable Multiport Memory BIST with on-the-fly ATE-configurable memory tests	Pending	Lattice Semiconductor Corporation
14/509,564		United States	Dont-care based mux absorption into ice40 carry chain	Pending	Lattice Semiconductor Corporation
14/525,240		United States	Level shifter that eliminates static power dissipation	Pending	Lattice Semiconductor Corporation
14/535,454		United States	Low power and high performance class AB amplifier control common mode in SerDes Transmitter	Pending	Lattice Semiconductor Corporation
14/535,351		United States	ICO metastability prevention during start-up	Pending	Lattice Semiconductor Corporation
14/558,851		United States	Low Power and Flexible TX FFE With Programmable Tap Positions And Coefficients Driver Architecture	Pending	Lattice Semiconductor Corporation
14/576,348		United States	Reconfigurable and Scalable Hardware Management Architecture	Pending	Lattice Semiconductor Corporation

DELL/HP/LENOVO EXHIBIT 1002
Page 228

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/576,245		United States	Methodology that allows multiple hardware or hardware-software controllers with different bus interfaces to share a common resource	Pending	Lattice Semiconductor Corporation
14/604,515		United States	Enhancement of FPGA hardware debugger to be used as a design controller/exerciser with user registers	Pending	Lattice Semiconductor Corporation
14/609,181		United States	Algorithm to Optimize Hot Swapping	Pending	Lattice Semiconductor Corporation
14/610,074		United States	Ripple Mode using 3-LUT for Generate	Pending	Lattice Semiconductor Corporation
14/610,127		United States	Combine OFX with LUT output and SUM into a single output to reduce number of signals to routing block	Pending	Lattice Semiconductor Corporation
14/611,069		United States	High speed complementary NMOS LUT logic	Pending	Lattice Semiconductor Corporation
14/611,095		United States	Shared Logic for Multiple Registers with asynchronous initialization with preload	Pending	Lattice Semiconductor Corporation
11/949,454	7,427,874	United States	Interface block architectures	Issued	Lattice Semiconductor Corporation
11/676,196	7,327,160	United States	SERDES with programmable I/O architecture	Issued	Lattice Semiconductor Corporation
6,786,564	6,786,564	United States	Inkjet printer, drive method and drive device for same	Issued	Lattice Semiconductor Corporation
11/839,107	7,856,050	United States	Receiver and transmitter calibration to compensate for frequency dependent I/Q imbalance	Issued	Lattice Semiconductor Corporation
07/679,370	5,255,221	United States	Fully configurable versatile field programmable function	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 229

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			element		Corporation
06/551,735	4,642,797	United States	High speed first-in-first-out memory	Issued	Lattice Semiconductor Corporation
08/042,533	5,394,037	United States	Sense amplifiers and sensing methods	Issued	Lattice Semiconductor Corporation
08/115,533	5,404,055	United States	Input routing pool	Issued	Lattice Semiconductor Corporation
08/115,723	5,394,033	United States	Structure and method for implementing hierarchical routing pools in a programmable logic circuit	Issued	Lattice Semiconductor Corporation
08/342,675	5,506,517	United States	Output enable structure and method for a programmable logic device	Issued	Lattice Semiconductor Corporation
07/911,841	5,357,156	United States	Active clamp circuit scheme for CMOS devices	Issued	Lattice Semiconductor Corporation
08/179,887	5,886,378	United States	Single polysilicon layer flash E.sup.2 PROM cell	Issued	Lattice Semiconductor Corporation
07/853,453	5,231,316	United States	Temperature compensated CMOS voltage to current converter	Issued	Lattice Semiconductor Corporation
08/108,363	5,353,246	United States	Programmable semiconductor antifuse structure and method of fabricating	Issued	Lattice Semiconductor Corporation
07/785,442	5,281,906	United States	Tunable voltage reference circuit to provide an output voltage with a predetermined temperature coefficient independent of variation in supply voltage	Issued	Lattice Semiconductor Corporation
07/696,453	5,251,169	United States	Non-volatile erasable and programmable interconnect cell	Issued	Lattice Semiconductor Corporation
07/538,211	5,255,203	United States	Interconnect structure for programmable logic device	Issued	Lattice Semiconductor

DELL/HP/LENOVO EXHIBIT 1002
Page 230

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
08/106,263	5,412,260	United States	Multiplexed control pins for in-system programming and boundary scan state machines in a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/033,934	5,418,390	United States	Single polysilicon layer E.sup.2 PROM cell	Issued	Lattice Semiconductor Corporation
07/993,711	5,452,229	United States	Programmable integrated-circuit switch	Issued	Lattice Semiconductor Corporation
07/957,311	5,329,179	United States	Arrangement for parallel programming of in-system programmable IC logical devices	Issued	Lattice Semiconductor Corporation
07/288,945	4,896,296	United States	Programmable logic device configurable input/output cell	Issued	Lattice Semiconductor Corporation
06/882,602	4,887,239	United States	One-time programmable data security system for programmable logic device	Issued	Lattice Semiconductor Corporation
06/871,063	4,766,569	United States	Programmable logic array	Issued	Lattice Semiconductor Corporation
06/862,815	4,879,688	United States	In-system programmable logic device	Issued	Lattice Semiconductor Corporation
06/707,670	4,833,646	United States	Programmable logic device with limited sense currents and noise reduction	Issued	Lattice Semiconductor Corporation
07/236,348	4,852,044	United States	Programmable data security circuit for programmable logic device	Issued	Lattice Semiconductor Corporation
11/400,924	7411424	United States	Programmable logic function generator using non-volatile programmable memory switches	Issued	Lattice Semiconductor Corporation
13/403,146		United States	Surface Mountable Integrated Circuit Packaging Scheme	Pending	SiBEAM, Inc.

DELL/HP/LENOVO EXHIBIT 1002
Page 231

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/242,665		United States	High Speed Integrated Circuit Interface	Pending	SiBEAM, Inc.
14/196,978		United States	Calibration of Single-Ended High-Speed Interfaces	Pending	Silicon Image, Inc.
14/474,005		United States	Inter-Device Conflict Resolution on a Multimedia Link	Pending	Silicon Image, Inc.
61/989,417		United States	Control Target Selection	Pending	Silicon Image, Inc.
61/988,812		United States	Lip Sync Delay Compensation	Pending	Silicon Image, Inc.
61/989,415		United States	Streaming Data and Metadata Synchronization	Pending	Silicon Image, Inc.
61/991,126		United States	Stream Creation with Limited Topology Information	Pending	Silicon Image, Inc.
61/989,411		United States	Topology Discovery	Pending	Silicon Image, Inc.
14/463,146		United States	Radio Frequency Interference Reduction In Multimedia Interfaces	Pending	Silicon Image, Inc.
14/578,266		United States	Control Target Selection	Pending	Silicon Image, Inc.
14/578,257		United States	System for Dynamic Audio Visual Capabilities Exchange	Pending	Silicon Image, Inc.
62/089,767		United States	High-Bandwidth Digital Content Protection over Audio Return Channel	Pending	Silicon Image, Inc.
12/573,492	8482462	United States	MULTI-ANTENNA BEAM-FORMING SYSTEM FOR TRANSMITTING CONSTANT ENVELOPE SIGNALS DECOMPOSED FROM A VARIABLE ENVELOPE SIGNAL	Issued	Silicon Image, Inc.
12/678,463	8207892	United States	TECHNIQUE FOR DETERMINING AN ANGLE OF ARRIVAL IN A COMMUNICATION SYSTEM	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/675,269	8374558	United States	ANTENNA ARRAY WITH FLEXIBLE INTERCONNECT FOR A MOBILE WIRELESS DEVICE	Issued	Silicon Image, Inc.
12/333,134	8213872	United States	TECHNIQUE FOR LOW-POWER OPERATION OF A WIRELESS DEVICE	Issued	Silicon Image, Inc.
12/933,876	8256123	United States	DISPLACEMENT SENSING USING A FLEXIBLE SUBSTRATE	Issued	Silicon Image, Inc.
14/196,993		United States	Calibration of Single-Ended High-Speed Interfaces	Pending	Silicon Image, Inc.
13/988,047		United States	INTEGRATED PHASE-SHIFTING-AND-COMBINING CIRCUITRY TO SUPPORT MULTIPLE ANTENNAS	Pending	Silicon Image, Inc.
14/002,353		United States	TRACKING SYSTEM WITH ORTHOGONAL POLARIZATIONS AND A RETRO-DIRECTIVE ARRAY	Pending	Silicon Image, Inc.
13/726,822		United States	HIGH-ACCURACY DETECTION IN COLLABORATIVE TRACKING SYSTEMS	Pending	Silicon Image, Inc.
13/859,764		United States	ANTENNA SELECTION AND PILOT COMPRESSION IN MIMO SYSTEMS	Pending	Silicon Image, Inc.
62/100,841		United States	I/Q Imbalance Correction for the Combination of Multiple Radio Frequency Frontends	Pending	Silicon Image, Inc.
12/532,107	8571126	United States	MULTI-ANTENNA TRANSMITTER FOR MULTI-TONE SIGNALING	Issued	Silicon Image, Inc.
14/065,420		United States	MULTI-ANTENNA TRANSMITTER FOR MULTI-TONE SIGNALING	Pending	Silicon Image, Inc.
12/679,764	8605823	United States	COMMUNICATION USING	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			CONTINUOUS-PHASE MODULATED SIGNALS		Inc.
14/101,274		United States	COMMUNICATION USING CONTINUOUS-PHASE MODULATED SIGNALS	Pending	Silicon Image, Inc.
12/746,526	8484277	United States	TRANSFORMING SIGNALS USING PASSIVE CIRCUITS	Issued	Silicon Image, Inc.
13/498,884	8610474	United States	SIGNAL DISTRIBUTION NETWORKS AND RELATED MET	Issued	Silicon Image, Inc.
14/089,094		United States	SIGNAL DISTRIBUTION NETWORKS AND RELATED METHODS	Pending	Silicon Image, Inc.
13/519,302		United States	Phase Detection Circuits and Methods	Pending	Silicon Image, Inc.
13/574,586	8795082	United States	DIRECTIONAL BEAM STEERING SYSTEM AND METHOD TO DETECT LOCATION AND MOTION	Issued	Silicon Image, Inc.
14/331,144		United States	DIRECTIONAL BEAM STEERING SYSTEM AND METHOD TO DETECT LOCATION AND MOTION	Pending	Silicon Image, Inc.
13/704,564		United States	Methods and Systems for Near-Field MIMO Communications	Pending	Silicon Image, Inc.
14/235,783		United States	HIGH-ACCURACY AND LOW-POWER TRACKING SYSTEM FOR MOBILE DEVICES	Pending	Silicon Image, Inc.
14/234,623		United States	LOW-COST TRACKING SYSTEM	Pending	Silicon Image, Inc.
14/240,405		United States	CALIBRATING A RETRO-DIRECTIVE ARRAY FOR AN ASYMMETRIC WIRELESS LINK	Pending	Silicon Image, Inc.
14/364,002		United States	COLLABORATIVE CHANNEL SOUNDING IN MULTI-ANTENNA	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			SYSTEMS		
08/815,486	6,157,360	United States	System And Method For Driving Columns Of An Active Matrix Display	Issued	Silicon Image, Inc.
08/920,336	5,955,929	United States	Voltage-Controlled Oscillator Resistant To Supply Voltage Noise	Issued	Silicon Image, Inc.
09/007,707	5,969,552	United States	Dual Loop Delay-Locked Loop	Issued	Silicon Image, Inc.
09/298,647	6,259,427	United States	Scaling Multi-Dimensional Signals Using Variable Weighting Factors	Issued	Silicon Image, Inc.
09/298,369	6,374,361	United States	Skew-Insensitive Low Voltage Differential Receiver	Issued	Silicon Image, Inc.
09/393,849	6,738,417	United States	Method And Apparatus For Bidirectional Data Transfer Between A Digital Display And A Computer	Issued	Silicon Image, Inc.
09/326,503	6,940,496	United States	Display Module Driving System And Digital To Analog Converter For Driving Display	Issued	Silicon Image, Inc.
09/392,229	6,564,269	United States	Bi-Directional Data Transfer Using The Video Blanking Period In A Digital Data Stream	Issued	Silicon Image, Inc.
09/393,234	6,307,543	United States	Bi-Directional Data Transfer Using Two Pair Of Differential Lines As A Single Additional Differential Pair	Issued	Silicon Image, Inc.
09/947,008	6,492,984	United States	Bi-Directional Data Transfer Using Two Pair Of Differential Lines As A Single Additional Differential Pair	Issued	Silicon Image, Inc.
09/759,624	6,891,910	United States	Baud-Rate Timing Recovery	Issued	Silicon Image, Inc.
09/574,571	6,326,826	United States	Wide Frequency-Range Delay- Locked Loop Circuit	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/881,271	6,954,491	United States	Methods And Systems For Sending Side-Channel Data During Data Inactive Period	Issued	Silicon Image, Inc.
09/922,990	6,961,095	United States	Digital Display Jitter Correction Apparatus And Method	Issued	Silicon Image, Inc.
11/219,323	7,557,863	United States	Digital Display Jitter Correction Apparatus And Method	Issued	Silicon Image, Inc.
09/989,587	6,717,478	United States	Multi-Phase Voltage Controlled Oscillator (VCO) With Common Mode Control	Issued	Silicon Image, Inc.
10/371,220	7,231,009	United States	Data Synchronization Across An Asynchronous Boundary Using, For Example, Multi-Phase Clocks	Issued	Silicon Image, Inc.
09/989,580	7,103,013	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
11/441,669	7,599,316	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
12/573,847	8,116,240	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
10/045,297	7,257,129	United States	Memory Architecture With Multiple Serial Communications Ports	Issued	Silicon Image, Inc.
11/828,286	7,903,684	United States	Communications Architecture For Transmission Of Data Between Memory Bank Caches And Ports	Issued	Silicon Image, Inc.
09/167,527	6,380,978	United States	Digital Video System And Methods For Providing Same	Issued	DVDO, INC. and Silicon Image, Inc.
10/032,136	7,215,376	United States	Digital Video System And Methods For Providing Same	Issued	DVDO, INC. and Silicon Image, Inc.

DELL/HP/LENOVO EXHIBIT 1002
Page 236

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/942,740	7,359,624	United States	Portable DVD Player	Issued	Silicon Image, Inc.
09/372,713	6,489,998	United States	Method And Apparatus For Deinterlacing Digital Video	Issued	Silicon Image, Inc.
09/941,949	6,909,469	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
10/251,642	7,027,099	United States	Method And Apparatus For Deinterlacing Digital Video Images	Issued	Silicon Image, Inc.
11/054,748	7,391,481	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
11/357,364	7,499,103	United States	Method And Apparatus For Detecting Frequency In Digital Video Images	Issued	Silicon Image, Inc.
11/932,808	7,633,559	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
09/410,543	6,700,622	United States	Method And Apparatus For Detecting The Source Format Of Video Images	Issued	Silicon Image, Inc.
09/396,993	6,515,706	United States	Method And Apparatus For Detecting And Smoothing Diagonal Features In Video Images	Issued	Silicon Image, Inc.
10/191,764	6,829,013	United States	Method And Apparatus For Detecting And Smoothing Diagonal Features In Video Images	Issued	Silicon Image, Inc.
09/363,312	6,681,059	United States	Method And Apparatus For Efficient Video Scaling	Issued	Silicon Image, Inc.
09/359,530	6,587,158	United States	Method And Apparatus For Reducing On-Chip Memory In Vertical Video Processing	Issued	Silicon Image, Inc.
09/226,776	6,219,747	United States	Methods And Apparatus For Variable Length SDRAM	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Transfers		
09/805,588	6,385,692	United States	Methods and Apparatus for Variable Length SDRAM Transfers	Issued	Silicon Image, Inc.
09/227,502	6,393,505	United States	Methods And Apparatus For Data Bus Arbitration	Issued	Silicon Image, Inc.
09/226,381	6,473,476	United States	Method And Apparatus For Providing Deterministic Resets For Clock Divider Systems	Issued	Silicon Image, Inc.
09/837,894	6,867,814	United States	Method, System And Article Of Manufacture For Identifying The Source Type And Quality Level Of A Video Sequence	Issued	Silicon Image, Inc.
09/478,122	7,203,557	United States	Audio Signal Delay Apparatus And Method	Issued	Silicon Image, Inc.
10/663,413	7,408,992	United States	Detection And Repair Of MPEG-2 Chroma Upconversion Artifacts	Issued	Silicon Image, Inc.
09/905,318	7,123,307	United States	Clock Jitter Limiting Scheme In Video Transmission Through Multiple Stages	Issued	Silicon Image, Inc.
09/905,615	6,944,804	United States	System And Method For Measuring Pseudo Pixel Error Rate	Issued	Silicon Image, Inc.
09/904,783	6,625,560	United States	Method Of Testing Serial Interface	Issued	Silicon Image, Inc.
09/989,590	6,845,461	United States	High-Speed Bus With Embedded Clock Signals	Issued	Silicon Image, Inc.
09/989,645	6,809,567	United States	System And Method For Multiple-Phase Clock Generation	Issued	Silicon Image, Inc.
09/905,511	7,062,004	United States	Method And Apparatus For Adaptive Control Of PLL Loop Bandwidth	Issued	Silicon Image, Inc.
10/057,823	7,023,487	United States	Deinterlacing Of Video Sources Via Image Feature Edge Detection	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/954,663	7,558,326	United States	Method And Apparatus For Sending Auxiliary Data On A TMDS-Like Link	Issued	Silicon Image, Inc.
10/036,234	7,359,437	United States	Encoding Method And System For Reducing Inter-Symbol Interference Effects In Transmission Over A Serial Link	Issued	Silicon Image, Inc.
10/095,422	7,257,163	United States	Method And System For Reducing Inter-Symbol Interference Effects In Transmission Over A Serial Link With Mapping Of Each Word In A Cluster Of Received Words To A Single Transmitted Word	Issued	Silicon Image, Inc.
10/171,860	7,088,398	United States	Method And Apparatus For Regenerating A Clock For Auxiliary Data Transmitted Over A Serial Link With Video Data	Issued	Silicon Image, Inc.
10/192,296	6,914,637	United States	Method And System For Video And Auxiliary Data Transmission Over A Serial Link	Issued	Silicon Image, Inc.
10/357,750	7,283,566	United States	Method And Circuit For Generating Time Stamp Data From An Embedded-Clock Audio Data Stream And A Video Clock	Issued	Silicon Image, Inc.
10/016,247	6,714,206	United States	Method And System For Spatial-Temporal Dithering For Displays With Overlapping Pixels	Issued	Silicon Image, Inc.
10/133,813	7,136,484	United States	Cryptosystems Using Commuting Pairs In A Monoid	Issued	Silicon Image, Inc.
10/047,772	7,109,958	United States	Supporting Circuitry And Method For Controlling Pixels	Issued	Silicon Image, Inc.
10/045,393	7,039,121	United States	Method And System For Transition-Controlled Selective Block Inversion	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Communications		
08/656,032	6,018,456	United States	Enclosure For Removable Computer Peripheral Equipment	Issued	CMD Technology Inc. and Silicon Image, Inc.
08/906,775	5,991,546	United States	System And Method For Interfacing Manually Controllable Input Devices To A Universal Computer Bus System	Issued	CMD Technology Inc. and Silicon Image, Inc.
10/171,820	7,225,282	United States	Method And Apparatus For A Two-Wire Serial Command Bus Interface	Issued	Silicon Image, Inc.
11/713,241	7,441,065	United States	Adaptive Beam-Steering Methods To Maximize Wireless Link Budget And Reduce Delay-Spread Using Multiple Transmit And Receive Antennas	Issued	Silicon Image, Inc.
10/210,839	7,171,525	United States	Method And System For Arbitrating Priority Bids Sent Over Serial Links To A Multi-Port Storage Device	Issued	Silicon Image, Inc.
09/688,536	6,380,783	United States	Cyclic Phase Signal Generation From A Single Clock Source Using Current Phase Interpolation	Issued	Silicon Image, Inc.
09/847,837	6,535,029	United States	Fully Differential Continuous-Time Current-Mode High Speed CMOS Comparator	Issued	Silicon Image, Inc.
10/270,882	7,009,827	United States	Voltage Swing Detection Circuit For Hot Plug Event Or Device Detection Via A Differential Link	Issued	Silicon Image, Inc.
10/162,046	6,843,674	United States	Method And Apparatus For Connecting Serial ATA Storage Components	Issued	Silicon Image, Inc.
09/945,278	7,131,004	United States	Method And Apparatus For Encrypting Data Transmitted Over A Serial Link	Issued	Silicon Image, Inc.
11/499,124	7,900,047	United States	Method And Apparatus For Encrypting Data Transmitted	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Over A Serial Link		Inc.
11/543,501	7,757,085	United States	Method And Apparatus For Encrypting Data Transmitted Over A Serial Link	Issued	Silicon Image, Inc.
10/224,995	7,218,737	United States	System And Method For An Adaptive State Machine To Control Signal Filtering In A Serial Link	Issued	Silicon Image, Inc.
09/991,057	7,242,766	United States	Method And System For Encrypting And Decrypting Data Using An External Agent	Issued	Silicon Image, Inc.
10/085,177	7,035,290	United States	Method And System For Temporary Interruption Of Video Data Transmission	Issued	Silicon Image, Inc.
10/036,794	6,976,201	United States	Method And System For Host Handling Of Communications Errors	Issued	Silicon Image, Inc.
10/053,461	7,113,507	United States	Method And System For Communicating Control Information Via Out-Of-Band Symbols	Issued	Silicon Image, Inc.
10/045,625	7,746,798	United States	Method And System For Integrating Packet Type Information With Synchronization Symbols	Issued	Silicon Image, Inc.
10/035,911	7,154,905	United States	Method And System For Nesting Of Communications Packets	Issued	Silicon Image, Inc.
10/045,600	6,771,192	United States	Method And System For DC-Balancing At The Physical Layer	Issued	Silicon Image, Inc.
10/045,601	7,340,558	United States	Multisection Memory Bank System	Issued	Silicon Image, Inc.
09/989,647	7,058,121	United States	Logic Gates Including Diode-Connected Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) To Control Input Threshold Voltage Levels And Switching Transients Of	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Output Logic Signals		
09/989,487	6,985,005	United States	Differential Amplifiers Using Asymmetric Transfer Characteristics To Suppress Input Noise In Output Logic Signals	Issued	Silicon Image, Inc.
11/330,047	7,456,648	United States	Differential Amplifiers Using Asymmetric Transfer Characteristics To Suppress Input Noise In Output Logic Signals	Issued	Silicon Image, Inc.
12/275,686	7,847,583	United States	Transmitter And Receiver Using Asymmetric Transfer Characteristics In Differential Amplifiers To Suppress Noise	Issued	Silicon Image, Inc.
10/403,477	6,819,166	United States	Continuous-Time, Low-Frequency-Gain/High-Frequency-Boosting	Issued	Silicon Image, Inc.
10/417,712	7,348,991	United States	Video Graphics Text Mode Enhancement Method For Digitally Processed Data	Issued	Silicon Image, Inc.
10/287,976	6,873,341	United States	Detection Of Video Windows And Graphics Windows	Issued	Silicon Image, Inc.
10/298,722	7,539,304	United States	Integrated Circuit Having Self Test Capability Using Message Digest And Method For Testing Integrated Circuit Having Message Digest Generation Circuitry	Issued	Silicon Image, Inc.
10/215,936	6,717,468	United States	Dynamically Biased Full-Swing Operation Amplifier For An Active Matrix Liquid Crystal Display Driver	Issued	Silicon Image, Inc.
10/268,832	7,412,053	United States	Cryptographic Device With Stored Key Data And Method For Using Stored Key Data To Perform An Authentication Exchange Of Self Test	Issued	Silicon Image, Inc.
11/950,088	7,797,536	United States	Cryptographic Device With Stored Key Data And Method	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			For Using Stored Key Data To Perform An Authentication Exchange Of Self Test		
10/244,152	6,814,583	United States	Through-Broad PCB Edge Connector, System And Method	Issued	Silicon Image, Inc.
10/247,675	8,064,508	United States	Equalizer With Controllably Weighted Parallel High Pass And Low Pass Filters And Receiver Including Such An Equalizer	Issued	Silicon Image, Inc.
11/796,175	8,275,026	United States	Equalizer With Controllably Weighted Parallel High Pass And Low Pass Filters And Receiver Including Such An Equalizer	Issued	Silicon Image, Inc.
10/651,500	7,551,909	United States	CMOS Transceiver With Dual Current Path VCO	Issued	Silicon Image, Inc.
10/099,533	7,158,593	United States	Combining A Clock Signal And A Data Signal	Issued	Silicon Image, Inc.
10/642,259	7,409,031	United States	Data Sampling Method And Apparatus With Alternating Edge Sampling Phase Detection For Loop Characteristic Stabilization	Issued	Silicon Image, Inc.
10/459,989	7,187,307	United States	Method And System For Encapsulation Of Multiple Levels Of Communication Protocol Functionality Within Line Codes	Issued	Silicon Image, Inc.
10/794,015	7,502,411	United States	Method And Circuit For Adaptive Equalization Of Multiple Signals In Response To A Control Signal Generated From One Of The Equalized Signals	Issued	Silicon Image, Inc.
10/459,992	6,747,580	United States	Method And Apparatus For Encoding Or Decoding Data In Accordance With An Nb/(N+1)B Block Code, And Method For Determining Such A Block Code	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/781,405	7,269,673	United States	Cable With Circuitry For Asserting Stored Cable Data Or Other Information To An External Device Or User	Issued	Silicon Image, Inc.
11/848,758	7,500,032	United States	Cable With Circuitry For Asserting Stored Cable Data Or Other Information To An External Device Or User	Issued	Silicon Image, Inc.
11/123,353	7,375,960	United States	Apparatus For Removably Securing Storage Components In An Enclosure	Issued	Silicon Image, Inc.
10/763,905	7,236,553	United States	Reduced Dead-Cycle, Adaptive Phase Tracking Method And Apparatus	Issued	Silicon Image, Inc.
10/835,301	6,897,793	United States	Method And Apparatus For Run Length Limited TMDS-Like Encoding Of Data	Issued	Silicon Image, Inc.
10/842,231	7,991,096	United States	Data Sampling Method And Apparatus Using Through-Transition Counts To Reject Worst Sampling Position	Issued	Silicon Image, Inc.
10/439,446	7,031,858	United States	Method And Circuit For DC Measurement Of Phase Uniformity Of Multi-Phase Clocks	Issued	Silicon Image, Inc.
10/302,436	7,274,690	United States	An Age Selection Switching Scheme For Data Traffic In A Crossbar Switch	Issued	Silicon Image, Inc.
10/645,786	7,505,422	United States	Preference Programmable First-One Detector And Quadrature Based Random Grant Generator	Issued	Silicon Image, Inc.
10/645,787	7,461,167	United States	A Method For Multicast Service In A Crossbar Switch	Issued	Silicon Image, Inc.
10/762,950	7,352,764	United States	Content Addressable Merged Queue Architecture For Switching Data	Issued	Silicon Image, Inc.
10/434,785	7,519,066	United States	A Method For Switching Data In A Crossbar Switch	Issued	Silicon Image, Inc.
11/372,866	7,694,204	United States	Error Detection In Physical	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Interfaces For Point-To-Point Communications Between Integrated Circuits		Inc.
12/712,124	7,937,644	United States	Error Detection In Physical Interfaces For Point-To-Point Communications Between Integrated Circuits	Issued	Silicon Image, Inc.
13/099,254	8,099,648	United States	Error Detection In Physical Interfaces For Point-To-Point Communications Between Integrated Circuits	Issued	Silicon Image, Inc.
11/669,416	7,844,762	United States	Parallel Interface Bus To Communicate Video Data Encoded For Serial Data Links	Issued	Silicon Image, Inc.
11/056,995	7,102,446	United States	Phase Lock Loop With Coarse Control Loop Having Frequency Lock Detector And Device Including Same	Issued	Silicon Image, Inc.
11/643,388	7,589,559	United States	Current Mode Circuitry To Modulate A Common Mode Voltage	Issued	Silicon Image, Inc.
12/555,300	7,872,498	United States	Current Mode Circuitry to Modulate a Common Mode Voltage	Issued	Silicon Image, Inc.
11/477,049	7,793,179	United States	Test Clock Control Structures To Generate Configurable Test Clocks For Scan-Based Testing Of Electronic Circuits Using Programmable Test Clock Controllers	Issued	Silicon Image, Inc.
11/856,640	7,782,934	United States	Parameter Scanning For Signal Over-Sampling	Issued	Silicon Image, Inc.
11/592,792	7,450,038	United States	Determining Oversampled Data To Be Included In Unit Intervals	Issued	Silicon Image, Inc.
11/510,254	8,595,434	United States	Smart Scalable Storage Switch Architecture	Issued	Silicon Image, Inc.
14/067,363		United States	Smart Scalable Storage Switch Architecture	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/314,162	7,571,269	United States	A Covert Channel For Conveying Supplemental Messages In A Protocol-Defined Link For A System Of Storage Devices	Issued	Silicon Image, Inc.
11/637,254	7,602,253	United States	Adaptive Bandwidth Phase Locked Loop With Feedforward Divider	Issued	Silicon Image, Inc.
11/656,331	7,984,369	United States	Concurrent Code Checker And Hardware Efficient High-Speed I/O Having Built-In Self-Test And Debug Features	Issued	Silicon Image, Inc.
11/694,819	7,949,863	United States	Multi-Port Memory Device Having Variable Port Speeds	Issued	Silicon Image, Inc.
11/694,813	7,639,561	United States	Power-Saving Clocking Technique	Issued	Silicon Image, Inc.
11/690,629	7,831,778	United States	Mechanism For Streaming Media Data Over Wideband Wireless Networks	Issued	Silicon Image, Inc.
11/476,457	7,840,861	United States	Scan-Based Testing Of Devices Implementing A Test Clock Control Structure (â€œTCCSâ€)	Issued	Silicon Image, Inc.
11/861,175	8,160,192	United States	Signal Interleaving for Serial Clock and Data Recovery	Issued	Silicon Image, Inc.
11/690,642	7,908,501	United States	Shared Nonvolatile Memory Architecture	Issued	Silicon Image, Inc.
11/742,358	7,698,088	United States	Interface Test Circuitry And Methods	Issued	Silicon Image, Inc.
11/848,641	8,233,432	United States	Ensuring Physical Locality Of Entities Sharing Data	Issued	Silicon Image, Inc.
11/683,608	7,831,877	United States	Method And Apparatus For A Two-Wire Serial Command Bus Interface	Issued	Silicon Image, Inc.
11/690,659	7,849,339	United States	Progressive Power Control Of A Multi-Port Memory Device	Issued	Silicon Image, Inc.
11/567,514	7,365,659	United States	Method Of Context Adaptive Binary Arithmetic Coding	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			And Coding Apparatus Using The Same		
12/778,882		United States	Multi-Level Port Expansion For Port Multipliers	Pending	Silicon Image, Inc.
12/147,248	7,836,223	United States	Operation Of Media Interface To Provide Bidirectional Communications	Issued	Silicon Image, Inc.
11/849,163	8,695,034	United States	Delivering On Screen Display Data To Existing Display Devices	Issued	Silicon Image, Inc.
11/828,219	8,599,315	United States	On Screen Displays Associated With Remote Video Source Devices	Issued	Silicon Image, Inc.
14/070,373		United States	On Screen Displays Associated With Remote Video Source Devices	Pending	Silicon Image, Inc.
11/829,800	7,903,550	United States	Bandwidth Reservation For Data Flows In Interconnection Networks	Issued	Silicon Image, Inc.
11/828,223	8,149,711	United States	Data Stream Control For Network Devices	Issued	Silicon Image, Inc.
13/541,390	8,924,509	United States	Automated Service Discovery And Dynamic Connection Management	Issued	Silicon Image, Inc.
11/836,082	8,468,212	United States	Network Repository For Metadata	Issued	Silicon Image, Inc.
13/919,773		United States	Network Repository For Metadata	Pending	Silicon Image, Inc.
11/829,790	7,911,956	United States	Packet Level Prioritization In Interconnection Networks	Issued	Silicon Image, Inc.
11/828,226		United States	Streaming Data Content In A Network	Pending	Silicon Image, Inc.
11/848,153	7,936,790	United States	Synchronizing Related Data Streams In Interconnection Networks	Issued	Silicon Image, Inc.
11/952,052	8,001,334	United States	Bank Sharing And Refresh In A Shared Multi-Port Memory Device	Issued	Silicon Image, Inc.

DELL/HP/LENOVO EXHIBIT 1002
Page 247

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/075,954	7,979,589	United States	Method, Apparatus, And System For Port Multiplier Enhancement	Issued	Silicon Image, Inc.
13/298,001		United States	Iddq Testing Of CMOS Devices	Pending	Silicon Image, Inc.
10/788,704	6,944,086	United States	Semiconductor Memory Device	Issued	Silicon Image, Inc.
10/876,231	7,016,255	United States	Multi-Port Memory Device	Issued	Silicon Image, Inc.
10/877,318	7,089,465	United States	Multi-Port Memory Device Having Serial I/O Interface	Issued	Silicon Image, Inc.
12/075,906	7,904,566	United States	Method, Apparatus, And System For Employing An Enhanced Port Multiplier	Issued	Silicon Image, Inc.
12/497,391	8,386,867	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
13/776,508	8,667,354	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
14/145,751	8,924,805	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
12/197,020	8,086,886	United States	Group Power Management Of Network Devices	Issued	Silicon Image, Inc.
12/683,365	8,543,873	United States	Multi-Site Testing Of Computer Memory Devices And Serial I/O Ports	Issued	Silicon Image, Inc.
14/035,795	8,839,058	United States	Multi-Site Testing Of Computer Memory Devices And Serial I/O Ports	Issued	Silicon Image, Inc.
11/969,847	8,090,030	United States	Method, Apparatus And System For Generating And Facilitating Mobile High-Definition Multimedia Interface	Issued	Silicon Image, Inc.
11/969,852	7,856,520	United States	Control Bus For Connection Of Electronic Devices	Issued	Silicon Image, Inc.
11/969,865	7,921,231	United States	Discovery Of Electronic Devices Utilizing A Control	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Bus		
12/172,187	8,238,653	United States	Methods And Mechanisms For Probabilistic Color Correction	Issued	Silicon Image, Inc.
12/392,000		United States	Method, Apparatus, And System For Pre-Authentication And Processing Of Data Streams	Pending	Silicon Image, Inc.
12/391,987	8,644,504	United States	Method, Apparatus, And System For Deciphering Media Content Stream	Issued	Silicon Image, Inc.
12/605,134	8,407,427	United States	Method And System For Improving Serial Port Memory Communication Latency And Reliability	Issued	Silicon Image, Inc.
13/850,147	8,892,825	United States	Method and System for Improving Serial Port Memory Communication Latency and Reliability	Issued	Silicon Image, Inc.
12/260,970	8,036,248	United States	Method, Apparatus, And System For Automatic Data Aligner For Multiple Serial Receivers	Issued	Silicon Image, Inc.
12/359,025	8,026,726	United States	Fault Testing For Interconnections	Issued	Silicon Image, Inc.
12/486,969	8,793,723	United States	Detection Of Encryption Utilizing Error Detection For Received Data	Issued	Silicon Image, Inc.
12/570,874	8,644,334	United States	Messaging To Provide Data Link Integrity	Issued	Silicon Image, Inc.
12/260,972	7,777,652	United States	Coding System For Memory Systems Employing High-Speed Serial Links	Issued	Silicon Image, Inc.
12/847,416	7,978,099	United States	17b/20b Coding System	Issued	Silicon Image, Inc.
12/351,698	8,374,346	United States	Method, Apparatus, And System For Pre-Authentication And Keep-Authentication Of Content Protected Ports	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/316,305	8,347,081	United States	Method, Apparatus And System For Employing A Content Protection System	Issued	Silicon Image, Inc.
12/577,707	8,275,914	United States	Method And System For Transmitting Or Receiving N-Bit Video Data Over A Serial Link	Issued	Silicon Image, Inc.
12/606,096	8,176,214	United States	Transmission Of Alternative Content Over Standard Device Connectors	Issued	Silicon Image, Inc.
12/351,712	8,185,739	United States	Method And System For Detecting Successful Authentication Of Multiple Ports In A Time Based Roving Architecture	Issued	Silicon Image, Inc.
12/512,877	8,458,343	United States	Signaling For Transitions Between Modes Of Data Transmission	Issued	Silicon Image, Inc.
12/983,233	8,489,784	United States	Adaptive Interconnection Scheme For Multimedia Devices	Issued	Silicon Image, Inc.
13/004,359	8,755,431	United States	Transmission And Detection Of Multi-Channel Signals In Reduced Channel Format	Issued	Silicon Image, Inc.
12/650,357		United States	Method, Apparatus, And System For Simultaneously Previewing Contents From Multiple Protected Sources	Pending	Silicon Image, Inc.
12/712,933	8,692,937	United States	Video Frame Synchronization	Issued	Silicon Image, Inc.
12/966,194		United States	Transmission And Handling Of Three-Dimensional Video Content	Pending	Silicon Image, Inc.
12/873,124	8,325,757	United States	De-Encapsulation Of Data Streams Into Multiple Links	Issued	Silicon Image, Inc.
12/704,417	8,510,487	United States	Hybrid Interface For Serial And Parallel Communication	Issued	Silicon Image, Inc.
13/934,147	8,751,709	United States	Hybrid Interface For Serial And Parallel Communication	Issued	Silicon Image, Inc.

DELL/HP/LENOVO EXHIBIT 1002
Page 250

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/842,165	8,930,692	United States	Mechanism For Internal Processing Of Content Through Partial Authentication On Secondary Channel	Issued	Silicon Image, Inc.
12/842,190		United States	Mechanism For Partial Encryption Of Data Streams	Pending	Silicon Image, Inc.
13/021,958		United States	Determination Of Physical Connectivity Status Of Devices Based On Electrical Measurement	Allowed	Silicon Image, Inc.
12/898,528	8,598,898	United States	Testing Of High-Speed Input-Output Devices	Issued	Silicon Image, Inc.
13/434,273		United States	Method, Apparatus And System For Transitioning An Audio/Video Device Between A Source Mode And A Sink Mode	Pending	Silicon Image, Inc.
12/848,037	8,624,960	United States	Multi-View Display System	Issued	Silicon Image, Inc.
14/094,668		United States	Multi-View Display System	Pending	Silicon Image, Inc.
12/816,437	8,698,958	United States	Mechanism For Memory Reduction In Picture-In-Picture Video Generation	Issued	Silicon Image, Inc.
13/753,408		United States	Communication Bridging Between Devices Via Multiple Bridge Elements	Pending	Silicon Image, Inc.
13/198,584		United States	Conversion Of Multimedia Data Streams For Use By Connected Devices	Pending	Silicon Image, Inc.
12/906,939	8,537,201	United States	Combining Video Data Streams Of Differing Dimensionality For Concurrent Display	Issued	Silicon Image, Inc.
13/172,745	8,484,387	United States	Detection Of Cable Connections For Electronic Devices	Issued	Silicon Image, Inc.
13/172,742	8,601,173	United States	Detection Of Cable Connections For Electronic	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Devices		
13/362,930		United States	Mechanism For Low Power Standby Mode Control Circuit	Allowed	Silicon Image, Inc.
13/217,138	8,379,145	United States	Conversion And Processing Of Deep Color Video In A Single Clock Domain	Issued	Silicon Image, Inc.
12/979,995	8,874,820	United States	Mechanism For Facilitating A Configurable Port-Type Peripheral Component Interconnect Express/Serial Advanced Technology Attachment Host Controller Architecture	Issued	Silicon Image, Inc.
12/950,850	8,504,672	United States	Discovery Of Electronic Devices In A Combined Network	Issued	Silicon Image, Inc.
13/959,592	8,799,443	United States	Discovery of Electronic Devices in a Combined Network	Issued	Silicon Image, Inc.
13/348,378		United States	Proxy Device Operation In Command And Control Network	Pending	Silicon Image, Inc.
12/950,867		United States	Transfer Of Control Bus Signaling On Packet-Switched Network	Pending	Silicon Image, Inc.
13/339,339		United States	Mechanism For Recovering Clock For Streaming Content Over A Packetized Network	Pending	Silicon Image, Inc.
13/302,452		United States	Multimedia I/O System Architecture for Advanced Digital Television	Pending	Silicon Image, Inc.
13/107,031		United States	Audio And Video Data Multiplexing For Multimedia Stream Switch	Pending	Silicon Image, Inc.
13/174,630		United States	Single-Ended Configurable Multi-Mode Driver	Pending	Silicon Image, Inc.
13/173,302		United States	Fine-Grained Self Refresh Control For DRAM Devices	Pending	Silicon Image, Inc.
13/174,616	8,760,188	United States	Configurable Multi-Dimensional Driver And	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Receiver		Inc.
13/083,399	8,611,486	United States	Adjustment Of Clock Signals Regenerated From A Data Stream	Issued	Silicon Image, Inc.
11/437,357	7,982,798	United States	Edge Detection	Issued	Silicon Image, Inc.
13/153,230	8,446,525	United States	Edge Detection	Issued	Silicon Image, Inc.
10/753,909	7,400,359	United States	Video Stream Routing And Format Conversion Unit With Audio Delay	Issued	Silicon Image, Inc.
10/889,855	7,710,501	United States	Time Base Correction And Frame Rate Conversion	Issued	Silicon Image, Inc.
11/487,144	8,004,606	United States	Original Scan Line Detection	Issued	Silicon Image, Inc.
11/941,050	8,086,067	United States	Noise Cancellation	Issued	Silicon Image, Inc.
11/512,754	8,120,703	United States	Source-Adaptive Video Deinterlacer	Issued	Silicon Image, Inc.
12/204,760	8,559,746	United States	System, Method And Apparatus For Smoothing Of Edges In Images To Remove Irregularities	Issued	Silicon Image, Inc.
14/054,575		United States	System, Method and Apparatus for Smoothing of Edges in Images to Remove Irregularities	Pending	Silicon Image, Inc.
12/703,623	8,452,117	United States	Block Noise Detection And Filtering	Issued	Silicon Image, Inc.
13/899,222	8,891,897	United States	Block Noise Detection And Filtering	Issued	Silicon Image, Inc.
13/335,398		United States	Ringing Suppression In Video Scalers	Pending	Silicon Image, Inc.
13/546,904		United States	Transmission Of Multiple Protocol Data Elements Via An Interface Utilizing A Data Tunnel	Pending	Silicon Image, Inc.

DELL/HP/LENOVO EXHIBIT 1002
Page 253

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/202,995	7,904,117	United States	Wireless Communication Device Using Adaptive Beamforming	Issued	SiBEAM, Inc.
11/706,711	7,710,319	United States	HD Physical Layer Of A Wireless Communication Device	Issued	SiBEAM, Inc.
12/748,276	7,982,669	United States	Adaptive Beam-Steering Methods To Maximize Wireless Link Budget And Reduce Delay-Spread Using Multiple Transmit And Receive Antennas	Issued	SiBEAM, Inc.
11/706,470	8,014,416	United States	Inter-Port Communication In A Multi-Port Memory Device	Issued	Silicon Image, Inc.
11/689,386	7,881,258	United States	Circuitry To Prevent Peak Power Problems During Scan Shift	Issued	SiBEAM, Inc.
11/726,874	8,155,712	United States	Low Power Very High-Data Rate Device	Issued	SiBEAM, Inc.
11/588,472	8,022,887	United States	Planar Antenna	Issued	SiBEAM, Inc.
11/752,073		United States	A Compact Millimeter Wave Vertical Interconnection Scheme By Combining Flip-Chip, Layer Transition	Pending	SiBEAM, Inc.
11/752,083	7,675,465	United States	Surface Mountable Integrated Circuit Packaging Scheme	Issued	SiBEAM, Inc.
12/215,959		United States	Mechanism For Communication With Multiple Wireless Video Area Networks	Pending	SiBEAM, Inc.
11/981,935		United States	Wireless HD Mac Frame Format	Pending	SiBEAM, Inc.
11/938,126	8,170,522	United States	Multi-Transformer Architecture For An RF Active Circuit	Issued	SiBEAM, Inc.
11/999,810	8,750,241	United States	Concurrent Association With Multiple WVAN Network	Issued	SiBEAM, Inc.
12/079,133	8,831,225	United States	Data Security	Issued	SiBEAM, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/011,404	7,948,961	United States	Wireless Proximity Estimation	Issued	SiBEAM, Inc.
11/982,209	8,279,784	United States	Wireless HD AV Packet Format	Issued	SiBEAM, Inc.
12/055,160	8,170,617	United States	Extensions To Adaptive BeamSteering Method	Issued	SiBEAM, Inc.
12/164,757		United States	Exchanging Information Between Components Coupled With An I2C Bus Via Separate Banks	Pending	SiBEAM, Inc.
12/167,195	8,229,352	United States	Wireless Architecture For 60 GHz	Issued	SiBEAM, Inc.
11/901,069	7,986,753	United States	Modified Branch Metric For Decoders And Equalizers	Issued	SiBEAM, Inc.
12/059,757	7,915,909	United States	RF Integrated Circuit Test Methodology And System	Issued	SiBEAM, Inc.
12/164,907		United States	Dispatch Capability Using A Single Physical Interface	Pending	SiBEAM, Inc.
12/165,468		United States	Bitmap Device Identification In A Wireless Communication System	Pending	SiBEAM, Inc.
12/165,472	8,897,719	United States	Initializing A Transceiver In A Wireless Communication System	Issued	SiBEAM, Inc.
12/164,849	8,341,271	United States	Device Discovery In A Wireless Communication System	Issued	SiBEAM, Inc.
12/164,810	8,116,333	United States	Connection Control In A Wireless Communication System	Issued	SiBEAM, Inc.
12/699,758	8,588,193	United States	Enhanced Wireless Data Rates Using Multiple Beams	Issued	SiBEAM, Inc.
12/699,781	8,457,026	United States	Enhanced Wireless Data Rates Using Multiple Beams	Issued	SiBEAM, Inc.
13/113,318		United States	Apparatus, System, And Method For A Compact Symmetrical Transition Structure For Radio	Allowed	SiBEAM, Inc.

DELL/HP/LENOVO EXHIBIT 1002
Page 255

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Frequency Applications		
14/128,551		United States	Method To Drive HDMI Or MHL Or USB Data Through One Set Of Pins	Pending	Silicon Image, Inc.
13/984,018		United States	Concept And Method Of Reducing Data Dependent Jitter	Pending	Silicon Image, Inc.
13/269,450		United States	Identification And Handling Of Data Streams Using Coded Preambles	Allowed	Silicon Image, Inc.
13/611,786		United States	Combining Video And Audio Streams Utilizing Pixel Repetition Bandwidth	Pending	Silicon Image, Inc.
14/118,832		United States	Compensation Scheme For MHL Common Mode Clock Swing	Pending	Silicon Image, Inc.
13/773,534		United States	Transmitting Multiple Differential Signals Over a Reduced Number of Physical Channels	Pending	Silicon Image, Inc.
13/460,393		United States	Cost-Efficient And Low-Latency Motion Picture Encoding For Limited Channel Bandwidth	Pending	Silicon Image, Inc.
13/791,494	8,925,003	United States	Mechanism For Facilitating Syncronization Of Audio And Video Between Multiple Media Devices	Issued	Silicon Image, Inc.
13/622,286	8,885,435	United States	Interfacing Between Integrated Circuits With Asymmetric Voltage Swing	Issued	Silicon Image, Inc.
13/770,984		United States	Configurable Single Ended Driver	Pending	Silicon Image, Inc.
13/779,372	8,920,188	United States	Integrated Connector/Flex Cable	Issued	Silicon Image, Inc.
13/834,927		United States	Simultaneous Transmission Of Clock And Bidirectional Data Over A Communication Channel	Allowed	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
13/605,708	8,841,974	United States	Test Solution For Ring Oscillators	Issued	Silicon Image, Inc.
14/193,932		United States	Test Solution for a Random Number Generator	Pending	Silicon Image, Inc.
13/787,664		United States	Auxiliary Data Encoding In Video Data	Pending	Silicon Image, Inc.
13/738,768		United States	Method And Apparatus For Reducing Digital Video Image Data	Pending	Silicon Image, Inc.
13/736,765	8,832,338	United States	Mechanism For Facilitating Dynamic Timestamp-Less Clock Regeneration For Transmitting Media Streams Over Shared Channels	Issued	Silicon Image, Inc.
14/123,037		United States	Timing Controlled Cascade Feed-Through High Speed Line Driver	Pending	Silicon Image, Inc.
13/776,577		United States	Apparatus, System And Method For Providing Clock And Data Signaling	Pending	Silicon Image, Inc.
13/940,038		United States	Integrated Mobile Desktop	Pending	Silicon Image, Inc.
13/915,586		United States	Multiple Protocol Tunneling Using Time Division Operations	Pending	Silicon Image, Inc.
13/891,842	8,786,776	United States	Method, Apparatus And System For Communicating Sideband Data With Non-Compressed Video	Issued	Silicon Image, Inc.
13/671,527		United States	Methods And Apparatuses To Provide And Electro-Optical Alignment	Pending	Silicon Image, Inc.
14/371,973		United States	Charge Pump Calibration for Dual-Path Phase-Locked Loop	Pending	Silicon Image, Inc.
14/115,324		United States	Mechanism for Facilitating Dynamic Phase Detection with High Jitter Tolerance for Images of Media Streams	Allowed	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/135,470		United States	Apparatus, System and Method for Formatting Audio-Video Information	Pending	Silicon Image, Inc.
13/839,671		United States	Full Frame Buffer To Improve Video Performance In Low- Latency Video Communication Systems	Pending	Silicon Image, Inc.
12/057,051		United States	Bi-Directional Digital Interface For Video And Audio (DIVA)	Pending	Silicon Image, Inc.
11/760,164	7,940,809	United States	Digital Video Interface With Bi-Directional Half-Duplex Clock Channel Used As Auxiliary Data Channel	Issued	Silicon Image, Inc.
11/865,621	7,916,780	United States	Adaptive Equalizer For Use With Clock And Data Recovery Circuit Of Serial Communication Link	Issued	Silicon Image, Inc.
12/222,745	7,737,802	United States	Passive Equalizer With Negative Impedance To Increase A Gain	Issued	Silicon Image, Inc.
12/636,063	8,680,712	United States	Power Delivery Over Digital Interactive Interface For Video And Audio (DIIVA)	Issued	Silicon Image, Inc.
13/521,739		United States	Multi-Media USB Data Transfer Over Digital Interaction Interface for Video and Audio (DIIVA)	Pending	Silicon Image, Inc.
13/521,762		United States	Video Management And Control In Home Multimedia Network	Pending	Silicon Image, Inc.
14/381,186		United States	Linear Regulator with Improved Power Supply Ripple Rejection	Pending	Silicon Image, Inc.
13/844,152		United States	Electronic Alignment Of Optical Signals	Pending	Silicon Image, Inc.
14/391,382		United States	Frequency Response Compensation in a Digital to Analog Converter	Pending	Silicon Image, Inc.
14/165,340		United States	Apparatus, System and	Pending	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Method for Providing Switching with a T-Coil Circuit		Inc.
13/836,895	8,928,411	United States	Integration Of Signal Sampling Within Transistor Amplifier Stage	Issued	Silicon Image, Inc.
14/165,345		United States	Apparatus, Method and System for Asymmetric Full-Duplex Communication	Pending	Silicon Image, Inc.
14/209,785		United States	Method And Apparatus For Implementing Wide Data Range And Wide Common-Mode Receivers	Pending	Silicon Image, Inc.
14/296,377		United States	Transmitting Apparatus with Source Termination	Pending	Silicon Image, Inc.
14/368,781		United States	Caching of Capabilities Information of Counterpart Device for Efficient Handshaking Operation	Pending	Silicon Image, Inc.
14/163,981		United States	Mechanism for Facilitating Dynamic Counter Synchronization and Packetization in High-Definition Multimedia Interface and Mobile High-Definition Link	Pending	Silicon Image, Inc.
14/253,808		United States	Communication of Multimedia Data Streams Over Multiple Communication Lanes	Pending	Silicon Image, Inc.
14/279,316		United States	HDCP2.2 Authentication Engine and Stream Cipher Engine Sharing in Digital Content Protection Architectures	Pending	Silicon Image, Inc.
14/383,865		United States	Techniques for Fractional-N Phase Locked Loops	Pending	Silicon Image, Inc.
61/949,901		United States	Compressed Video Transfer Over HDMI and MHL	Pending	Silicon Image, Inc.
14/563,797		United States	Electrical Duplex to Optical Conversion	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/470,750		United States	Arbitration Signaling within a Multimedia High Definition Link (MHL 3) Device	Pending	Silicon Image, Inc.
14/275,692		United States	Error Detection and Mitigation in Video Channels	Pending	Silicon Image, Inc.
14/339,393		United States	Phase-Modulated On-Off Keying for Millimeter Wave Spectrum Control	Pending	Silicon Image, Inc.
14/145,715		United States	Messaging to Provide Data Link Integrity	Pending	Silicon Image, Inc.
14/145,736	8,854,548	United States	Mechanism for Memory Reduction in Picture-In-Picture Video Generation	Issued	Silicon Image, Inc.
14/470,613		United States	Compressed Video Transfer Over a Multimedia Link	Pending	Silicon Image, Inc.
14/184,647		United States	Video Frame Synchronization	Pending	Silicon Image, Inc.
14/181,446		United States	Power Delivery Over Digital Interaction Interface for Video and Audio (DiiVA)	Pending	Silicon Image, Inc.
14/470,804		United States	Phase Relationship Control for Control Channel of a Multimedia Communication Link	Pending	Silicon Image, Inc.
14/470,809		United States	Retry Disparity for Control Channel of a Multimedia Communication Link	Pending	Silicon Image, Inc.
61/943,267		United States	Pre-Processor and Post-Processor for Compression of 4:2:0 Encoded Video Streams with Video Compression Codecs Embedded within an Audio/Video Standard	Pending	Silicon Image, Inc.
14/278,255		United States	Encoding Guard Band Data for Transmission Via a Communications Interface Utilizing Transition-Minimized Differential Signaling (Tmds) Coding	Pending	Silicon Image, Inc.
14/322,753		United States	Calibration Of Single-Ended	Pending	Silicon Image,

DELL/HP/LENOVO EXHIBIT 1002
Page 260

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			High-Speed Interfaces		Inc.
61/947,704		United States	Reversible Connector	Pending	Silicon Image, Inc.
14/460,737		United States	System and Method for Transcoding Data	Pending	Silicon Image, Inc.
14/502,928		United States	Electrical Connector with Optical Channel	Pending	Silicon Image, Inc.
14/322,753		United States	Cable with Circuitry for Communicating Performance Information	Pending	Silicon Image, Inc.
61/973,837		United States	Error Correction for Transmission of Compressed Video Data Over Standards-Defined Coded Audio/Video Links	Pending	Silicon Image, Inc.
61/975,517		United States	(MHL) Connector Cable Detect, Cable Orientation Detect and/or Lane Re-Mapping	Pending	Silicon Image, Inc.
61/979,477		United States	MHL3 Router without HDCP2.2 Decryption and Encryption Operation	Pending	Silicon Image, Inc.
61/979,483		United States	TDD over 5-Pin Interface	Pending	Silicon Image, Inc.
14/470,620		United States	Compressed Blanking Period Transfer Over a Multimedia Link	Pending	Silicon Image, Inc.
14/273,400		United States	Transmission and Detection of Multi-Channel Signals in Reduced Channel Format	Pending	Silicon Image, Inc.
61/989,409		United States	System for Dynamic Capabilities, Status, and Metadata Exchange	Pending	Silicon Image, Inc.
14/300,166		United States	Configurable Multi-Dimensional Driver and Receiver	Pending	Silicon Image, Inc.
14/483,013		United States	Enhanced Communication Link Using Synchronization Signal as Link Command	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
62/043,218		United States	Run Length Programmable Unified Built-In Self-Test (BIST) Scheme for Various High-Speed Serial IO Standards	Pending	Silicon Image, Inc.
14/559,523		United States	Determination of Physical Connectivity Status of Devices Based on Electrical Measurement	Pending	Silicon Image, Inc.
14/516,136		United States	Method and System for Improving Serial Port Memory Communication Latency and Reliability	Pending	Silicon Image, Inc.
62/061,630		United States	Secure Control Communication Between an Application Processor and a Transmitter	Pending	Silicon Image, Inc.
62/075,554		United States	Metadata Transfer for HDMI/MHL	Pending	Silicon Image, Inc.
14/570,817		United States	Mechanism for Facilitating Dynamic Phase Detection with High Jitter Tolerance for Images of Media Streams	Pending	Silicon Image, Inc.
14/589,889		United States	Displaying Multiple Videos on Sink Device Using Display Information of Source Device	Pending	Silicon Image, Inc.
14/589,925		United States	Lower Power Operations in a Wireless Tunneling Transceiver	Pending	Silicon Image, Inc.
14/591,845		United States	Simultaneous Transmission of Clock and Bidirectional Data Over a Communication Channel	Pending	Silicon Image, Inc.
14/449095	20150036756	United States	Radio Frequency Interference Reduction In Multimedia Interfaces	Pending	Silicon Image, Inc.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/434,273	01/05/2016	9232265	30850-25622	7248

120363 7590 12/16/2015

Lattice Semiconductor/FENWICK
801 California Street
Mountain View, CA 94041

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 709 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Invensense, Inc, San Jose, CA;
Conrad Arlo Maxwell, Herriman, UT;
Lance Davies, Loveland, CO;
Graeme P. Jones, Tampa, FL;
Glenn L. Marks, Corona, CA;
Jonathan Regalado-Hawkey, Woolston, UNITED KINGDOM;
Christian Rudel, Wunstork, GERMANY;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

120363 7590 09/25/2015
Lattice Semiconductor/FENWICK
801 California Street
Mountain View, CA 94041

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/434,273	03/29/2012	Conrad Arlo Maxwell	30850-25622	7248

TITLE OF INVENTION: METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	12/28/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
BARTELS, CHRISTOPHER A.	2184	710-014000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Fenwick & West LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Lattice Semiconductor Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Portland, Oregon

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 192555 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☐ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Goutham Kondapalli/ Date November 30, 2015

Typed or printed name Goutham Kondapalli Registration No. 71,166

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DELL/HP/LENOVO EXHIBIT 1002
Page 264

Electronic Patent Application Fee Transmittal

Application Number:	13434273
Filing Date:	29-Mar-2012
Title of Invention:	METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE
First Named Inventor/Applicant Name:	Conrad Arlo Maxwell
Filer:	Goutham Kondapalli
Attorney Docket Number:	30850-25622

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**960**

Electronic Acknowledgement Receipt

EFS ID:	24218522
Application Number:	13434273
International Application Number:	
Confirmation Number:	7248
Title of Invention:	METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE
First Named Inventor/Applicant Name:	Conrad Arlo Maxwell
Customer Number:	120363
Filer:	Goutham Kondapalli
Filer Authorized By:	
Attorney Docket Number:	30850-25622
Receipt Date:	30-NOV-2015
Filing Date:	29-MAR-2012
Time Stamp:	18:21:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$960
RAM confirmation Number	6828
Deposit Account	192555
Authorized User	KONDAPALLI, GOUTHAM
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	25622_Issue_Fee_Transmittal.pdf	165620 d8325c69afbf4fbc5321717163174020195141 77	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31096 09d513cd6fcb8ae8f080812e3d239f4752dc0098	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	196716		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

120363 7590 09/25/2015

Lattice Semiconductor/FENWICK
801 California Street
Mountain View, CA 94041

EXAMINER
BARTELS, CHRISTOPHER A.

ART UNIT	PAPER NUMBER
2184	

DATE MAILED: 09/25/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/434,273	03/29/2012	Conrad Arlo Maxwell	30850-25622	7248

TITLE OF INVENTION: METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	12/28/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

DELL/HP/LENOVO EXHIBIT 1002
Page 269

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

120363 7590 09/25/2015
Lattice Semiconductor/FENWICK
801 California Street
Mountain View, CA 94041

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/434,273	03/29/2012	Conrad Arlo Maxwell	30850-25622	7248

TITLE OF INVENTION: METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	12/28/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
BARTELS, CHRISTOPHER A.	2184	710-014000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DELL/HP/LENOVO EXHIBIT 1002
Page 270

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/434,273	03/29/2012	Conrad Arlo Maxwell	30850-25622	7248

120363 7590 09/25/2015

Lattice Semiconductor/FENWICK
801 California Street
Mountain View, CA 94041

EXAMINER	
BARTELS, CHRISTOPHER A.	
ART UNIT	PAPER NUMBER
2184	

DATE MAILED: 09/25/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/434,273	Applicant(s) MAXWELL ET AL.	
	Examiner CHRISTOPHER BARTELS	Art Unit 2184	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *08/07/2015*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1,3-5,7,9,11-13,15,17,19 and 21-26*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☒ Other *PTO-2323 paper no. 20150907*.

/C. B./ Examiner, Art Unit 2184	/HENRY TSAI/ Supervisory Patent Examiner, Art Unit 2184

DETAILED ACTION

This office action is in response to communication response received on 08/07/2015. Claims 1, 3-5, 7, 9, 11-13, 15, 17, 19, and 21-26 are subject to allowance.

Response to Arguments

1. Applicant's arguments, filed 08/07/2015, have been fully considered and are persuasive. The outstanding ground of rejection(s) has been withdrawn.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Goutham Kondapalli (Agent No. 71166) on September 1st, 2015. In addition to considering and entering the amended claim listing filed (08/07/2015), the following amendment has been made:

22. (Amended) The method of claim 21, wherein the range of values includes 1.5 kilo ohms and [[2.5]] 2.0 kilo ohms.

24. (Amended) The device of claim 23, wherein the range of values includes 1.5 kilo ohms and [[2.5]] 2.0 kilo ohms.

26. (Amended) The method of claim 25, wherein the range of values includes 1.5 kilo ohms and [[2.5]] 2.0 kilo ohms.

Reasons for Allowance

2. The following is an examiner's statement of reasons for allowance: As to newly amended independent claim 1, now recites the limitation(s) "***initializing a first audio/video (AV) device to operate in a default AV sink operation mode in response to a power-on-reset or powering up of the first AV device;" in combination with the other claimed elements and features is not taught nor suggested by the prior art of record. Similar recitations also incorporated into independent claims 9 and 15.***

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references indicate the current state of the art:

US 8745251 B2, US 20070263669 A1, US 20090141180 A1,
US 7945708 B2, US 8019906 B2, US 8095714 B2,
US 8275914 B2, US 8484387 B2, US 8683087 B2.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER BARTELS whose telephone number is (571)270-3182. The examiner can normally be reached on Monday To Friday ; 9:00am to 5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DR. HENRY TSAI can be reached on (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. B./
Examiner, Art Unit 2184

/HENRY TSAI/
Supervisory Patent Examiner, Art Unit 2184

Notice of References Cited	Application/Control No. 13/434,273	Applicant(s)/Patent Under Reexamination MAXWELL ET AL.	
	Examiner CHRISTOPHER BARTELS	Art Unit 2184	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2007/0263669 A1	11-2007	Maginity et al.	370/503
*	B	US-2009/0141180 A1	06-2009	Kondo et al.	348/723
*	C	US-7,945,708 B2	05-2011	Ohkita, Hideki	710/14
*	D	US-8,019,906 B2	09-2011	Lee et al.	710/14
*	E	US-8,095,714 B2	01-2012	Huo et al.	710/110
*	F	US-8,275,914 B2	09-2012	Kim et al.	710/15
*	G	US-8,484,387 B2	07-2013	Kim et al.	710/11
*	H	US-8,683,087 B2	03-2014	Connolly, Graham L S	710/11
*	I	US-8,745,251 B2	06-2014	Zou et al.	709/230
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

AFCP 2.0 Decision	Application No.	Applicant(s)
	13/434,273	MAXWELL ET AL.
	Examiner	Art Unit
	CHRISTOPHER BARTELS	2184

This is in response to the After Final Consideration Pilot request filed 08/07/2015.

1. **Improper Request** – The AFCP 2.0 request is improper for the following reason(s) and the after final amendment submitted with the request will be treated under pre-pilot procedure.

   ☐ An AFCP 2.0 request form PTO/SB/434 (or equivalent document) was not submitted.

   ☐ A non-broadening amendment to at least one independent claim was not submitted.

   ☐ A proper AFCP 2.0 request was submitted in response to the most recent final rejection.

   ☐ Other:

2. **Proper Request**

   A. After final amendment submitted with the request will not be treated under AFCP 2.0.
   The after final amendment cannot be reviewed and a search conducted within the guidelines of the pilot program.

   ☐ The after final amendment will be treated under pre-pilot procedure.

   B. Updated search and/or completed additional consideration.
   The examiner performed an updated search and/or completed additional consideration of the after final amendment within the time authorized for the pilot program. The result(s) of the updated search and/or completed additional consideration are:

   ☒ 1. All of the rejections in the most recent final Office action are overcome and a Notice of Allowance is issued herewith.

   ☐ 2. The after final amendment would not overcome all of the rejections in the most recent final Office action. See attached interview summary for further details.

   ☐ 3. The after final amendment was reviewed, and it raises a new issue(s). See attached interview summary for further details.

   ☐ 4. The after final amendment raises new issues, but would overcome all of the rejections in the most recent final Office action. A decision on determining allowability could not be made within the guidelines of the pilot. See attached interview summary for further details, including any newly discovered prior art.

   ☐ 5. Other:

   Examiner Note: Please attach an interview summary when necessary as described above.

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13434273	MAXWELL ET AL.
	Examiner	**Art Unit**
	CHRISTOPHER BARTELS	2184

CPC							
Symbol						**Type**	**Version**
H04N		21	/	43635		F	2013-01-01
H04L		12	/	12		I	2013-01-01
H04L		12	/	2829		I	2013-01-01
H04L		2012	/	2849		A	2013-01-01
H04N		5	/	775		I	2013-01-01
H04N		21	/	44227		I	2013-01-01
Y02B		60	/	34		A	2013-01-01
G06F		3	/	14		I	2013-01-01
G09G		5	/	006		I	2013-01-01
G09G		2330	/	02		A	2013-01-01
G09G		2370	/	12		A	2013-01-01
G09G		2370	/	22		A	2013-01-01
			/				
			/				
			/				

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

/C.B./ Examiner.Art Unit 2184 (Assistant Examiner)	09/07/2015 (Date)	**Total Claims Allowed:** 18	
/HENRY TSAI/ Supervisory Patent Examiner.Art Unit 2184 (Primary Examiner)	09/08/2015 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 4A

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13434273	MAXWELL ET AL.
	Examiner	**Art Unit**
	CHRISTOPHER BARTELS	2184

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
710	14	G	0	6	F	3 / 00 (2006.01.01)						

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				

/C.B./ Examiner.Art Unit 2184	09/07/2015	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	18	
/HENRY TSAI/ Supervisory Patent Examiner.Art Unit 2184	09/08/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4A

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13434273	MAXWELL ET AL.
	Examiner	**Art Unit**
	CHRISTOPHER BARTELS	2184

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	15	17												
-	2	-	18												
2	3	16	19												
3	4	-	20												
4	5	6	21												
-	6	7	22												
5	7	12	23												
-	8	13	24												
8	9	17	25												
-	10	18	26												
9	11														
10	12														
11	13														
-	14														
14	15														
-	16														

/C.B./ Examiner.Art Unit 2184	09/07/2015	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	18	
/HENRY TSAI/ Supervisory Patent Examiner.Art Unit 2184	09/08/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4A

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13434273	MAXWELL ET AL.
	Examiner	Art Unit
	CHRISTOPHER BARTELS	2184

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/05/2014	05/19/2015	09/07/2015						
	1	✓	✓	=						
	2	✓	-	-						
	3	✓	✓	=						
	4	✓	✓	=						
	5	✓	✓	=						
	6	✓	-	-						
	7	✓	✓	=						
	8	✓	-	-						
	9	✓	✓	=						
	10	✓	✓	-						
	11	✓	✓	=						
	12	✓	✓	=						
	13	✓	✓	=						
	14	✓	-	-						
	15	✓	✓	=						
	16	✓	✓	-						
	17	✓	✓	=						
	18	✓	-	-						
	19	✓	✓	=						
	20	✓	-	-						
	21			=						
	22			=						
	23			=						
	24			=						
	25			=						
	26			=						

AMENDMENTS TO THE CLAIMS

Claims 1, 9, 15, and 19 are hereby amended, and new claims 21-26 are added. All pending claims are produced below.

1. (Currently Amended): A method comprising:

initializing a first audio/video (AV) device to operate in a default AV sink operation mode in response to a power-on-reset or powering up of the first AV device;

detecting with control circuitry of [[a]]the first ~~audio/video (~~AV[[)]] device, a coupling between the first AV device and a second AV device;

determining whether a first supply voltage is provided at a channel of a connector, the connector coupling the first AV device and the second AV device;

in response to determining that the first supply voltage is provided at the channel of the connector, configuring communication logic of the first AV device to ~~operate~~ continue operating the first AV device in [[an]] the AV sink operation mode; ~~, wherein~~

when operating the first AV device in the AV sink operation mode, ~~receives~~ receiving AV data provided to the first AV device via the connector and ~~receives~~ receiving power from the first supply voltage provided to the first AV device at the channel of the connector ~~in the AV sink operation mode, the AV sink operation mode being a default mode of operation~~; [[and]]

in response to determining that the first supply voltage is not provided at the channel of the connector, configuring the communication logic of the first AV device to transition the first AV device from the AV sink operation mode to an AV source operation mode~~, wherein~~; and

when operating the first AV device in the AV source operation mode, ~~sends~~ sending AV data via the connector and ~~provides~~ providing a second supply voltage at the channel of the connector ~~in the AV source operation mode~~.

2. (Canceled)

3. (Original) The method of claim 1, wherein the default operation mode is for communication according to a high-definition multimedia interface standard.

4. (Previously Presented) The method of claim 1, wherein a first impedance is provided for a data channel of the connector in the AV source operation mode, and the first impedance is not provided for the data channel in the AV sink operation mode.

5. (Previously Presented) The method of claim 1, further comprising:

performing an AV data exchange between the first device and the second device.

6. (Canceled)

7. (Previously Presented) The method of claim 5, further comprising:

detecting a change to the connectivity of the first AV device after the AV data exchange; and

in response to the detected change to the connectivity, placing the communication logic into the AV sink operation mode.

8. (Canceled)

9. (Currently Amended) An audio/video (AV) device comprising:

communication logic to couple to a connector, the communication logic including circuitry configured to implement:

an AV sink operation mode for the communication logic to receive AV data provided to the AV device at the connector and to receive power from a first supply voltage provided to the AV device via a channel of the connector, the AV sink operation mode being a default mode of operation for the AV device, and

an AV source operation mode for the communication logic to send AV data from the AV device via the connector and to provide a second supply voltage at the channel of the connector; and

control logic including circuitry to configure the communication logic to initialize the AV device to operate in the default AV sink operation mode in response to a power-on-reset or powering up of the AV device, to continue operating ~~operate~~ the AV device in the AV sink operation mode in response to determining that the first supply voltage is provided at the channel of the connector, and to configure the communication logic to transition the AV device from the AV sink operation mode to the AV source operation mode in response to determining that the first supply voltage is not provided at the channel of the connector.

10. (Canceled)

11. (Original) The device of claim 9, wherein the default operation mode is for communication according to a high-definition multimedia interface standard.

12. (Previously Presented) The device of claim 9, wherein the communication logic is further configured to provide a first impedance for a data channel of the connector in the AV source operation mode and is configured to not provide the first impedance for the data channel in the AV sink operation mode.

13. (Previously Presented) The device of claim 9, further comprising:

detector logic to detect, while the communication logic is in the default operation mode, a coupling of the AV device to another AV device via the connector; and

wherein the communication logic is further configured to perform an AV data exchange with the other device in response to the detection.

14. (Canceled)

15. (Currently Amended) A system comprising:

a connector;

communication logic of an audio/video (AV) device coupled to the connector, the communication logic including circuitry configured to implement:

an ~~audio/video (~~AV[[)]] sink operation mode for the communication logic to receive AV data provided to the system at the connector and to receive power from a first supply voltage provided to the system at a channel of the connector, the AV sink operation mode being a default mode of operation for the system, and

an AV source operation mode for the communication logic to send AV data from the system via the connector and to provide a second supply voltage at the channel of the connector; and

control logic including circuitry to configure the communication logic to initialize the AV device to operate in the default AV sink operation mode in response to a power-on-reset or powering up of the AV device, to continue operating ~~operate~~ the AV device in the AV sink operation mode in response to determining that the first supply voltage is provided at the channel of the connector, and to configure the communication logic to transition the AV device from the AV sink operation mode to the AV source operation mode in response to determining that the first supply voltage is not provided at the channel of the connector.

16. (Canceled)

17. (Previously Presented) The system of claim 15, further comprising:

detector logic to detect, while the communication logic is in the default operation mode, a coupling of the system to an AV device via the connector; and

wherein the communication logic is further configured to perform an AV data exchange with the AV device in response to the detection.

18. (Canceled)

19. (Currently Amended) The system of claim 17, wherein the detector logic is further configured to detect a change to the connectivity after the AV data exchange, wherein, in response to the detected change to the connectivity, the control logic further configured to place the communication logic into the AV sink operation mode.

20. (Canceled)

21. (New) The method of claim 1, wherein the communication logic is further configured to transition the first AV device from the AV sink operation mode to the AV source operation mode in response to determining that an impedance at a second channel of the connector is outside a range of values.

22. (New) The method of claim 21, wherein the range of values includes 1.5 kilo ohms and 2.5 kilo ohms.

23. (New) The device of claim 9, wherein the communication logic is further configured to transition the first AV device from the AV sink operation mode to the AV source operation mode in response to determining that an impedance at a second channel of the connector is outside a range of values.

24. (New) The device of claim 23, wherein the range of values includes 1.5 kilo ohms and 2.5 kilo ohms.

25. (New) The system of claim 15, wherein the communication logic is further configured to transition the first AV device from the AV sink operation mode to the AV source operation mode in response to determining that an impedance at a second channel of the connector is outside a range of values.

26. (New) The system of claim 25, wherein the range of values includes 1.5 kilo ohms and 2.5 kilo ohms.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	43596	(stimpot trimpot digipot (slid$3 thumb thumbwheel) near2 pot rheostat)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 17:36
S2	231052	(stimpot trimpot digipot (slid$3 thumb thumbwheel) near2 pot rheostat potentiometer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 17:36
S3	405	S2 and (range ohm slid$3 resistance) with ("1.5" and "2.5")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 17:37
S4	231052	(stimpot trimpot digipot (slid$3 thumb thumbwheel) near2 pot rheostat potentiometer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 20:04
S5	405	S4 and (range ohm slid$3 resistance) with ("1.5" and "2.5")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 20:04
S6	81	S5 and (dvr dvd digital near2 (video recorder device) hdmi high adj definition mhl mobile near2 high adj (definition link))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 20:04
S7	534	S4 and (range ohm slid$3 resistance resistor resistive load) with ("1.5" and "2.5")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 20:58
S8	98	S7 and (dvr dvd digital near2 (video	US-PGPUB;	OR	ON	2015/08/31

		recorder device) hdmi high adj definition mhl mobile near2 high adj (definition link))	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			20:58
S9	17	S8 not S6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 20:59
S10	46518	(range ohm slid$3 resistance) with ("1.5" and "2.5")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 21:00
S11	48940	(range ohm slid$3 resistance resistor resistive load) with ("1.5" and "2.5")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 21:00
S12	2062	S11 and (dvr dvd digital near2 (video recorder device) hdmi high adj definition mhl mobile near2 high adj (definition link))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 21:01
S13	1700	S11 and (dvr dvd digital near2 (video recorder device) hdmi high adj definition mhl mobile near2 high adj (definition link)) and (cable standard "1.3a" "1.3" version)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 21:01
S14	49	S11 and (dvr dvd digital near2 (video recorder device) hdmi high adj definition mhl mobile near2 high adj (definition link)) and (cable standard) with ("1.3a" "1.3" version)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 21:01
S15	138277	(range ohm slid$3 resistance) with ("1.5" and "2")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/01 10:35
S16	151588	(range ohm slid$3 resistance resistor resistive load) with ("1.5" and "2")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2015/09/01 10:35

			IBM_TDB			
S17	467	S16 and (dvr dvd digital near2 (video recorder device) hdmi high adj definition mhl mobile near2 high adj (definition link)) and (cable standard) with ("1.3a" "1.3" version)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/01 10:35
S18	9	S17 and (stimpot trimpot digipot (slid$3 thumb thumbwheel) near2 pot rheostat potentiometer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/01 10:36
S19	288	S17 and (default intial) with (mode sink source)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/01 10:37
S20	20	S17 and (default intial) with (mode and sink source)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/01 11:01
S21	288	S17 and (default intial) with mode and (sink source)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/01 11:02
S22	21	S17 and (default initial) with (mode and sink source)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/01 11:02
S23	268	S21 not (S20 S22)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/01 11:08
S24	1	S23 not silverbrook	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/01 11:08
S25	22	S17 and (default initial$7) with (mode and sink source)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2015/09/01 11:09

			EPO; JPO; DERWENT; IBM_TDB			
S26	1	S25 not S22	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/01 11:10
S27	179	S17 not S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/01 11:10
S28	35	(scl and sda) with ("1.5" and "2")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/01 12:14
S29	0	(scl and sda) with ("1.5" and "2.5")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/01 12:14
S30	41	("7827319" | "6618773" | "7761709" | "7889201" | "20080205306" | "7979910" | "8453008" | "20100131782" | "20080270635" | "20090046690" | "20080270635" | "7995043" | "8510483" | "20090174817" | "7995043" | "20100131782" | "20080205306" | "20090083825" | "8266335" | "8447158" | "20090083825").Pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/01 12:21
S31	0	S30 and "2009046690"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/01 12:23
S32	3	S30 and "20090046690"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/01 12:24
S33	10	("20080205306" "20090083825" "20080270635" "20100131782").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2015/09/01 14:36

			IBM_TDB			

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S34	370644	(710/14.ccls.) (G06F$).CPC.	USPAT; UPAD	OR	ON	2015/09/06 13:06
S35	10785	S34 AND ((stimpot trimpot digipot (slid$3 thumb thumbwheel) near2 pot rheostat potentiometer) impedance resist$4).clm.	USPAT; UPAD	OR	ON	2015/09/06 13:08
S36	76	S35 and (hdmi high near4 (definition multi multimedia interface multi adj media) (av audio adj video) near2 (source sink mode target request$3)).clm.	USPAT; UPAD	OR	ON	2015/09/06 13:16

9/7/2015 11:25:18 PM
C:\Users\cbartels\Documents\EAST\Workspaces\13434273afcpSearch.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13434273	MAXWELL ET AL.
	Examiner	Art Unit
	CHRISTOPHER BARTELS	2184

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner
(G09G5, H04N, G06F, H04L, G08C and relevant sub-groups) text search in EAST	07/02/2014-07/03/2014	C.A.B.
(G03B, G09G, H05B, G06F and relevant sub-groups) text search in East	05/15/2015	C.A.B.

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Text search in EAST (ALL DATABASES)	12/09/13, 12/20/13, 7/2/14, 5/15/2015, 08/31/2015	C.A.B.
710/15, 1 AND (713 714) text search in East	12/09/2013	C.A.B.
Inventor Search performed (USPAT, UPAD)	12/09/2013	C.A.B.

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	(710/14 and G06F relevant subgroups) interference search in EAST	09/06/2015	C.A.B.

/C.B./ Examiner.Art Unit 2184	

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

APPLICANT:	Conrad Arlo Maxwell, et al.
APPLICATION NO.:	13/434,273
FILING DATE:	March 29, 2012
TITLE:	Method, Apparatus And System For Transitioning An Audio/Video Device Between A Source Mode And A Sink Mode
EXAMINER:	Christopher A. Bartels
GROUP ART UNIT:	2184
CONFIRMATION NO.	7248
ATTY. DKT. NO.:	30850-25622/US

CERTIFICATE OF ELECTRONIC (EFS-WEB) TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with 37 C.F.R. § 1.8(a)(i)(C) from the **Pacific Time Zone** of the United States on the local date shown below.

Dated: August 7, 2015 By: /Goutham Kondapalli/
Goutham Kondapalli, Reg. No. 71,166

AMENDMENT B AFTER FINAL UNDER 37 CFR § 1.116

This Amendment and Response is in reply to the final Office action dated May 28, 2015.

Please amend the application as follows:

Amendments to the Claims begin on page 2 of this paper.

Remarks follow the Amendments to the Claims section.

AMENDMENTS TO THE CLAIMS

Claims 1, 9, 15, and 19 are hereby amended, and new claims 21-26 are added. All pending claims are produced below.

1. (Currently Amended): A method comprising:

initializing a first audio/video (AV) device to operate in a default AV sink operation mode in response to a power-on-reset or powering up of the first AV device;

detecting with control circuitry of [[a]]the first ~~audio/video (~~AV[[)]] device, a coupling between the first AV device and a second AV device;

determining whether a first supply voltage is provided at a channel of a connector, the connector coupling the first AV device and the second AV device;

in response to determining that the first supply voltage is provided at the channel of the connector, configuring communication logic of the first AV device to ~~operate~~ continue operating the first AV device in [[an]] the AV sink operation mode; ~~, wherein~~

when operating the first AV device in the AV sink operation mode, ~~receives~~ receiving AV data provided to the first AV device via the connector and ~~receives~~ receiving power from the first supply voltage provided to the first AV device at the channel of the connector ~~in the AV sink operation mode, the AV sink operation mode being a default mode of operation~~; [[and]]

in response to determining that the first supply voltage is not provided at the channel of the connector, configuring the communication logic of the first AV device to transition the first AV device from the AV sink operation mode to an AV source operation mode~~, wherein~~; and

when operating the first AV device in the AV source operation mode, ~~sends~~ sending AV data via the connector and ~~provides~~ providing a second supply voltage at the channel of the connector ~~in the AV source operation mode~~.

DELL/HP/LENOVO EXHIBIT 1002
Page 297

2. (Canceled)

3. (Original) The method of claim 1, wherein the default operation mode is for communication according to a high-definition multimedia interface standard.

4. (Previously Presented) The method of claim 1, wherein a first impedance is provided for a data channel of the connector in the AV source operation mode, and the first impedance is not provided for the data channel in the AV sink operation mode.

5. (Previously Presented) The method of claim 1, further comprising:

performing an AV data exchange between the first device and the second device.

6. (Canceled)

7. (Previously Presented) The method of claim 5, further comprising:

detecting a change to the connectivity of the first AV device after the AV data exchange; and

in response to the detected change to the connectivity, placing the communication logic into the AV sink operation mode.

8. (Canceled)

9. (Currently Amended) An audio/video (AV) device comprising:

communication logic to couple to a connector, the communication logic including circuitry configured to implement:

DELL/HP/LENOVO EXHIBIT 1002
Page 298

an AV sink operation mode for the communication logic to receive AV data provided to the AV device at the connector and to receive power from a first supply voltage provided to the AV device via a channel of the connector, the AV sink operation mode being a default mode of operation for the AV device, and

an AV source operation mode for the communication logic to send AV data from the AV device via the connector and to provide a second supply voltage at the channel of the connector; and

control logic including circuitry to configure the communication logic to initialize the AV device to operate in the default AV sink operation mode in response to a power-on-reset or powering up of the AV device, to continue operating ~~operate~~ the AV device in the AV sink operation mode in response to determining that the first supply voltage is provided at the channel of the connector, and to configure the communication logic to transition the AV device from the AV sink operation mode to the AV source operation mode in response to determining that the first supply voltage is not provided at the channel of the connector.

10. (Canceled)

11. (Original) The device of claim 9, wherein the default operation mode is for communication according to a high-definition multimedia interface standard.

12. (Previously Presented) The device of claim 9, wherein the communication logic is further configured to provide a first impedance for a data channel of the connector in the AV source operation mode and is configured to not provide the first impedance for the data channel in the AV sink operation mode.

13. (Previously Presented) The device of claim 9, further comprising:

detector logic to detect, while the communication logic is in the default operation mode, a coupling of the AV device to another AV device via the connector; and

wherein the communication logic is further configured to perform an AV data exchange with the other device in response to the detection.

14. (Canceled)

15. (Currently Amended) A system comprising:

a connector;

communication logic of an audio/video (AV) device coupled to the connector, the communication logic including circuitry configured to implement:

an ~~audio/video (~~AV[[)]] sink operation mode for the communication logic to receive AV data provided to the system at the connector and to receive power from a first supply voltage provided to the system at a channel of the connector, the AV sink operation mode being a default mode of operation for the system, and

an AV source operation mode for the communication logic to send AV data from the system via the connector and to provide a second supply voltage at the channel of the connector; and

DELL/HP/LENOVO EXHIBIT 1002
Page 300

control logic including circuitry to configure the communication logic to initialize the AV device to operate in the default AV sink operation mode in response to a power-on-reset or powering up of the AV device, to continue operating ~~operate~~ the AV device in the AV sink operation mode in response to determining that the first supply voltage is provided at the channel of the connector, and to configure the communication logic to transition the AV device from the AV sink operation mode to the AV source operation mode in response to determining that the first supply voltage is not provided at the channel of the connector.

16. (Canceled)

17. (Previously Presented) The system of claim 15, further comprising:

detector logic to detect, while the communication logic is in the default operation mode, a coupling of the system to an AV device via the connector; and

wherein the communication logic is further configured to perform an AV data exchange with the AV device in response to the detection.

18. (Canceled)

19. (Currently Amended) The system of claim 17, wherein the detector logic is further configured to detect a change to the connectivity after the AV data exchange, wherein, in response to the detected change to the connectivity, the control logic further configured to place the communication logic into the AV sink operation mode.

20. (Canceled)

21. (New) The method of claim 1, wherein the communication logic is further configured to transition the first AV device from the AV sink operation mode to the AV source operation mode in response to determining that an impedance at a second channel of the connector is outside a range of values.

22. (New) The method of claim 21, wherein the range of values includes 1.5 kilo ohms and 2.5 kilo ohms.

23. (New) The device of claim 9, wherein the communication logic is further configured to transition the first AV device from the AV sink operation mode to the AV source operation mode in response to determining that an impedance at a second channel of the connector is outside a range of values.

24. (New) The device of claim 23, wherein the range of values includes 1.5 kilo ohms and 2.5 kilo ohms.

25. (New) The system of claim 15, wherein the communication logic is further configured to transition the first AV device from the AV sink operation mode to the AV source operation mode in response to determining that an impedance at a second channel of the connector is outside a range of values.

26. (New) The system of claim 25, wherein the range of values includes 1.5 kilo ohms and 2.5 kilo ohms.

DELL/HP/LENOVO EXHIBIT 1002
Page 302

REMARKS

Claims 1, 3-5, 7, 9, 11-13, 15, 17, and 19 were pending in the application. Claims 1, 3-5, 7, 9, 11-13, 15, 17, and 19 were rejected in a final Office action dated May 28, 2015 ("the Final Office Action").

Claims 1, 9, 15, and 19 are hereby amended, and new claims 21-26 are added. Support for the amended claims and the newly added claims can be found, for example, at paragraphs [0046]-[0054] of the specification.

Based on the above Amendment and the following Remarks, reconsideration and withdrawal of all rejections is respectfully requested.

Summary of Substance of Interview

Applicant's representatives Jason E. Amsel (Reg. No. 60,650) and Goutham Kondapalli (Reg. No. 71,166), conducted a telephonic interview with Examiner Christopher A. Bartels and SPE Henry Tsai on Tuesday, August 4, 2015. During the interview, pending claim 1 and its rejection was discussed. An agreement was reached during the interview that claims as amended overcome the prior art of record.

Claim Rejections under 35 U.S.C §§ 102 and 103

Claims 1, 3-5, 7, 9, 11-13, 15, 17, and 19:

In the Final Office Action, claims 1, 3, 5, 7, 9, 11-13, 15, 17, and 19 were rejected pre-AIA under 35 U.S.C. § 102(b) as being anticipated by Sato et al (US Pat. App. Pub. No. 2009/0174817 A1) and claim 4 was rejected as obvious over Sato in view of Noorbakhsh et al. (US Pat No. 7995043 B2). These rejections are addressed together for clarity and are now overcome in view of the preceding amendments and following remarks.

DELL/HP/LENOVO EXHIBIT 1002
Page 303

Claim 1 as amended, *inter alia*, recites:

> initializing a first audio/video (AV) device to operate in a default AV sink operation mode in response to a power-on-reset or powering up of the first AV device;
>
> …
>
> in response to determining that the first supply voltage is not provided at the channel of the connector, configuring the communication logic of the first AV device to transition the first AV device from the AV sink operation mode to an AV source operation mode.

As agreed in the interview of August 4, 2015, Sato fails to disclose the above-recited claim elements as amended. *See* Sato, Figures 15, 16, 23, and 27; ¶¶ [0010], [0203]-[0209], [0255], [0260], [0326], [0330]-[0334], [0384], and [0385].

Noorbakhsh fails to cure the deficiencies of Sato. Noorbakhsh is directed to "a method that provides arbitration between conflicting memory access requests for the single on-board memory that stores both EDID and processor related executable instructions and data." (Noorbakhsh, col. 2:57-60). While Noorbakhsh discloses an ON mode and an OFF mode, Noorbakhsh's ON mode is not the claimed "AV source operation mode" at least because Noorbakhsh's display controller does not "provide a second supply voltage," as recited in amended claim 1.

Moreover, Noorbakhsh also fails to disclose "transition[ing] . . . from the AV sink operation mode to an AV source operation mode," "in response to determining that the first supply voltage is not provided at the channel of the connector," because Noorbakhsh discloses that its display controller transitions from an OFF mode to the ON mode when its internal power regulator is turned on rather than checking for a supply voltage provided to the display controller externally. (See Noorbakhsh, col. 6:14-42).

DELL/HP/LENOVO EXHIBIT 1002
Page 304

Consequently, amended independent claim 1 is patentably distinguishable over the cited art. Independent claims 9 and 15 also recited features similar to the features discussed above with reference to claim 1, and therefore are patentably distinguishable over the cited art.

Each of the dependent claims 3-5, 7, 11, 12, 13, 17, and 19 incorporates the limitations of one of independent claims 1, 9, or 15. Therefore, these dependent claims are also patentably distinguishable over the cited art for at least the same reasons as set forth above.

New claims 21-26:

Each of the new dependent claims 21-26 incorporates the limitations of one of independent claims 1, 9, or 15. Therefore, these dependent claims are also patentably distinguishable over the cited art for at least the same reasons as set forth above with reference to their independent claims.

Moreover, Sato in view of Noorbakhsh fails to disclose or suggest at least "the communication logic is further configured to transition the first AV device from the AV sink operation mode to the AV source operation mode in response to determining that an impedance at a second channel of the connector is outside a range of values," as recited in each of the dependent claims 21, 23, and 25. For at least these reasons, new dependent claims 21-26 are patentably distinguishable over the cited art.

Accordingly, withdrawal of these rejections is respectfully requested.

DELL/HP/LENOVO EXHIBIT 1002
Page 305

CONCLUSION

Therefore, reconsideration of the basis for the rejections to these claims and allowance of these claims is respectfully requested.

In addition, the Examiner is invited to contact the undersigned at the number provided below if the Examiner believes such contact will help expedite furtherance of this application.

Respectfully submitted,

Dated: August 7, 2015

/Goutham Kondapalli/

Goutham Kondapalli, Reg. No. 71,166
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Doc Code: A.NE.AFCP
Document Description: After Final Consideration Pilot Program Request

PTO/SB/434 (05-13)

CERTIFICATION AND REQUEST FOR CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0

Practitioner Docket No.:	Application No.:	Filing Date:
30850-25622/US	13/434,273	March 29, 2012
First Named Inventor:	**Title:**	
Conrad A. Maxwell	Method, Apparatus And System For Transitioning An Audio/Video Device Between A Source Mode And A Sink Mode	

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0 (AFCP 2.0) OF THE ACCOMPANYING RESPONSE UNDER 37 CFR 1.116.

1. The above-identified application is (i) an original utility, plant, or design nonprovisional application filed under 35 U.S.C. 111(a) [a continuing application (*e.g.*, a continuation or divisional application) is filed under 35 U.S.C. 111(a) and is eligible under (i)], or (ii) an international application that has entered the national stage in compliance with 35 U.S.C. 371(c).
2. The above-identified application contains an outstanding final rejection.
3. Submitted herewith is a response under 37 CFR 1.116 to the outstanding final rejection. The response includes an amendment to at least one independent claim, and the amendment does not broaden the scope of the independent claim in any aspect.
4. This certification and request for consideration under AFCP 2.0 is the only AFCP 2.0 certification and request filed in response to the outstanding final rejection.
5. Applicant is willing and available to participate in any interview requested by the examiner concerning the present response.
6. This certification and request is being filed electronically using the Office's electronic filing system (EFS-Web).
7. Any fees that would be necessary consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, extension of time fees, are being concurrently filed herewith. [There is no additional fee required to request consideration under AFCP 2.0.]
8. By filing this certification and request, applicant acknowledges the following:

- Reissue applications and reexamination proceedings are not eligible to participate in AFCP 2.0.
- The examiner will verify that the AFCP 2.0 submission is compliant, *i.e.*, that the requirements of the program have been met (see items 1 to 7 above). For compliant submissions:
  - The examiner will review the response under 37 CFR 1.116 to determine if additional search and/or consideration (i) is necessitated by the amendment and (ii) could be completed within the time allotted under AFCP 2.0. If additional search and/or consideration is required but cannot be completed within the allotted time, the examiner will process the submission consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, by mailing an advisory action.
  - If the examiner determines that the amendment does not necessitate additional search and/or consideration, or if the examiner determines that additional search and/or consideration is required and could be completed within the allotted time, then the examiner will consider whether the amendment places the application in condition for allowance (after completing the additional search and/or consideration, if required). If the examiner determines that the amendment does not place the application in condition for allowance, then the examiner will contact the applicant and request an interview.
    - The interview will be conducted by the examiner, and if the examiner does not have negotiation authority, a primary examiner and/or supervisory patent examiner will also participate.
    - If the applicant declines the interview, or if the interview cannot be scheduled within ten (10) calendar days from the date that the examiner first contacts the applicant, then the examiner will proceed consistent with current practice concerning responses after final rejection under 37 CFR 1.116.

Signature	Date
/Goutham Kondapalli/	August 7, 2015
Name (Print/Typed) Goutham Kondapalli	**Practitioner Registration No.** 71,166

Note: *This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.*

[✓] * Total of 1 forms are submitted.

Electronic Acknowledgement Receipt

EFS ID:	23154892
Application Number:	13434273
International Application Number:	
Confirmation Number:	7248
Title of Invention:	METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE
First Named Inventor/Applicant Name:	Conrad Arlo Maxwell
Customer Number:	120363
Filer:	Goutham Kondapalli
Filer Authorized By:	
Attorney Docket Number:	30850-25622
Receipt Date:	07-AUG-2015
Filing Date:	29-MAR-2012
Time Stamp:	21:00:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		25622_Amendment_B_After_Final.pdf	113291 5d7cd23b7e68e8bd3cdd3be3dff79e268ff18169	yes	11

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Response After Final Action	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	11

Warnings:					
Information:					
2	After Final Consideration Program Request	25622_Certification_and_Request_for_Consideration_after_Final.pdf	134060 6e2246d788751b3b87f6086cb13fa60a99a847fa	no	1
Warnings:					
Information:					
		Total Files Size (in bytes):	247351		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/434,273	Filing Date 03/29/2012	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	08/07/2015	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SLIE
/INEZ MCMILLIAN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/434,273	03/29/2012	Conrad Arlo Maxwell	30850-25622	7248

120363 7590 05/28/2015

Silicon Image/FENWICK
801 California Street
Mountain View, CA 94041

EXAMINER
BARTELS, CHRISTOPHER A.

ART UNIT	PAPER NUMBER
2184	

NOTIFICATION DATE	DELIVERY MODE
05/28/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ptoc@fenwick.com

Office Action Summary	Application No. 13/434,273	Applicant(s) MAXWELL ET AL.	
	Examiner CHRISTOPHER BARTELS	Art Unit 2184	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/20/2015*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) *2,6,8,14,18 and 20* is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1,3-5,7,9-13,15-17 and 19* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *09/12/2014*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Response to Amendment

2. This Action is responsive to the Applicant's Amendment/Remarks filed on 3/04/2015.

Note claims 1-20 are currently pending.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 09/12/2014. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3, 5, 7, 9, 11-13, 15 and 17 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Sato et al. (USPGPUB No. ***2009/0174817 A1***, *hereinafter referred to as Sato*).

Referring to claim 1, Sato discloses a method {see Figs. 24-25 and 27} ***comprising:***

detecting with control circuitry {although not shown in Figure 27, there's a control circuitry receiving "PlugDetect SG613" for detecting a coupling "HPD" between first device "source device 213" and second AV device "sink device 253" ([0380]).} ***of a first audio/video (AV) device, a coupling between the first AV device and a second AV device;***

determining whether a first supply voltage {first supply voltage "5.0V" coupled to inverter "620" ([0376]).} ***is provided at a channel of a connector*** {said voltage provided at channel "SCL 803" of a connector "HDMI CABLE 351" (see Fig. 27, [0376]).} ***, the connector*** {connector "HDMI CABLE 351", see Fig. 27} ***coupling the first AV device and the second AV device;***

in response to determining {the first supply voltage provided as claimed in the form of "HDMI sink process" step s194 "transmit E-EDID" as it relies on enabling "DdcAct line" through "inverter 620" ([330], [0286-0289]).} ***that the first supply voltage is provided at the channel of the connector, configuring communication logic*** {communication logic "DDC terminals 651 and 652" (see Fig. 27, [0368], [0373]) as "DDC" standards for "transmission channel called a display data channel and a CEC line" ([0115, [0144]) control data is communicated on the same

line.} ***of the first AV device to operate the first AV device in an AV sink operation mode*** {see the first bubble, and step s151 of Fig. 24, [0330].}***, wherein the first AV device receives AV data provided*** {receives AV data "RX data is selected", see Fig. 24, [0332].} ***to the first AV device via the connector and receives power from the first supply voltage provided*** {see above in claim 1.} ***to the first AV device at the channel of the connector in the AV sink operation mode, the AV sink operation mode being a default mode*** {this AV sink operation mode "S151-S152" is the default "first" mode of operation selected before duplex or half-duplex communication is selected (steps 155-157, respectively in Figure 24).} ***of operation; and***

in response to determining that the first supply voltage is not provided {on the other hand, step s194 (see Fig. 25) opposite of step s154 (Fig. 24) means the first supply voltage is not provided ([0345]).} ***at the channel of the connector, to transition the first AV device from the AV sink operation mode to an AV source operation mode*** {the first bubble of Figure 25, [0345].}***, wherein the first AV device sends AV data via the connector and provides a second supply voltage*** {based on the same DDC logic as the first supply voltage, second supply voltage "5.0V" provided and coupled through resistor 653 and DDC terminals ([0368], [0373]).} ***at the channel of the connector in***

the AV source operation mode.

As per claim 3, the rejection of claim 1 is incorporated and Sato discloses wherein the default operation mode is for communication according to a high-definition multimedia interface standard {see claim 1, Figure 27, and "HDMI cable 351"}.

As per claim 5, the rejection of claim 1 is incorporated and Sato discloses further comprising:

performing an AV data exchange {see claim 1 and either steps s155-s157 (see Fig. 24) or steps s196-s198 (see Fig. 25) for the AV data exchange as claimed.} ***between the first device and the second device;***

As per claim 7, the rejection of claim 5 is incorporated and Sato discloses further comprising:

detecting a change {subsequent to AV data exchange steps (see claim 5, Figs. 24-25 respectively), the process loops back to step S151 (Fig. 24) or step s191 (Fig. 25) checking if second AV device (and conversely, the first) realizes "new electronic device connected" ([0330]) via the HPD detect signal (see claim

1, Fig. 27, "PlugDetect SG613").} ***to the connectivity of the first AV device after the AV data exchange;***

and in response to the detected change to the connectivity, placing the communication logic into the AV sink operation mode {see claim 1 with respect to communication logic "DDC terminals" and Fig. 25, s192-195.}.

Referring to claims 9 and 11-13, 15, 17 are device claims corresponding to the method claims of claims 1-3 and 6-8, respectively, thereby rejected under the same reasoning recited in claims 1-3, and 6-8 above.

Claim Rejections - 35 USC § 103

6. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 4 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Sato in view of Noorbakhsh et al. (US Pat No. ***7995043 B2,*** *hereinafter referred to as Noor*).

As per claim 4, the rejection of claim 1 is incorporated and Noor discloses wherein a first impedance {first impedance "resistor R2" (see Fig. 4, Col 9, lines 1-19) for an "auto activity detection circuit 400”/“detection circuit 128" when recognizing the data channel "virtual EDID operation" of the connector “cable 112” (Col 7, lines 22-48).} ***for a data channel of the connector in the AV source operation mode, and the first impedance*** {see claim 1 and note the “logic combination of this bit register bits] and Tclk is used to do the power switching [of Figure 5E]” and thus affecting the data channel provided by the communication logic (Col 7, lines 45-49).} ***is not provided for the data channel in the AV sink operation mode.***

Sato and Noor are analogous art because they are from the same problem-solving area, methods and systems for communicating with display devices.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Sato and Noor before him or her, to modify Noor’s “DDC terminals” to incorporate Noor’s “auto activity detection circuit” (see Fig. 4).

The suggestion/motivation for doing so would have been to provide a dual interface (Noor Col 2, lines 36-48) thus permitting support the EDID through DDC ports without having two

separate EDID ROM devices that further provides arbitration between conflicting memory access requests for both EDID and processor related executable instructions and data (Noor Col 2, lines 49-60).

Therefore, it would have been obvious to combine Noor with Sato to obtain the invention as specified in the instant claim(s).

Response to Arguments

Applicant's arguments filed (01/20/2015) have been fully considered but are deemed moot in view of the new ground of rejection(s).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references applicable as a 103 rejection teaches limitations recited in claim 1:

US 20080205306 A1, US 20080270635 A1, US 20090046690 A1, US 20090083825 A1, US 20100131782 A1, US 6618773 B1, US 7827319 B2, US 7979910 B2, US 7995043 B2.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER A. BARTELS whose telephone number is (571)270-3182. The examiner can normally be reached on Monday To Thursday; 7:30am to 5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Dr. Henry Tsai can be reached on (571) 272-4176. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. B./
Examiner, Art Unit 2184

/HENRY TSAI/
Supervisory Patent Examiner, Art Unit 2184

Notice of References Cited	Application/Control No. 13/434,273	Applicant(s)/Patent Under Reexamination MAXWELL ET AL.	
	Examiner CHRISTOPHER BARTELS	Art Unit 2184	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,618,773 B1	09-2003	Chang et al.	710/16
*	B	US-2008/0205306 A1	08-2008	Saito, Tetsuji	370/294
*	C	US-2008/0270635 A1	10-2008	Nakahama, Masahiko	710/8
*	D	US-2009/0046690 A1	02-2009	Hsieh, Kun-Li	370/342
*	E	US-2009/0083825 A1	03-2009	Miller et al.	725/151
*	F	US-2010/0131782 A1	05-2010	Higuchi, Satoshi	713/310
*	G	US-7,827,319 B2	11-2010	Kimura et al.	710/5
*	H	US-7,979,910 B2	07-2011	Mantani, Nobunori	726/26
*	I	US-7,995,043 B2	08-2011	Noorbakhsh et al.	345/204
*	J	US-2009/0174817	07-2009	Sato et al.	348/554
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)				*Complete if Known*	
				Application Number	13/434,273
				Filing Date	March 29, 2012
				First Named Inventor	Conrad Arlo Maxwell
				Art Unit	2184
				Confirmation Number	7248
				Examiner Name	Christopher A. Bartels
Sheet	1	of	2	Attorney Docket Number	30850-25622/US

U.S. PATENT DOCUMENTS				
		Document No.		
Examiner Initials*	Cite No.[1]	Number – Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
/C.B./	A1	US-2009/0046690 A1	02-19-2009	Hsieh

FOREIGN PATENT DOCUMENTS					
		Foreign Patent Document			
Examiner Initials*	Cite No.[1]	Country Code[3] – Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6]

OTHER REFERENCES – NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[6]
/C.B./	C1	Extended European Search Report, European Application No. 12762781.8, August 13, 2014, 7 pages.	

EXAMINER SIGNATURE	
Examiner Signature	/Christopher Bartels/
Date Considered	05/19/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (option). [2] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [3] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

[5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.B./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)				Complete if Known	
				Application Number	13/434,273
				Filing Date	March 29, 2012
				First Named Inventor	Conrad Arlo Maxwell
				Art Unit	2184
				Confirmation Number	7248
				Examiner Name	Christopher A. Bartels
Sheet	2	of	2	Attorney Docket Number	30850-25622/US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Goutham Kondapalli/	Date (YYYY-MM-DD)	2014-09-12
Name/Print	Goutham Kondapalli	Registration Number	71,166

30850/25622/DOCS/3488724.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.B./

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13434273	MAXWELL ET AL.
	Examiner	Art Unit
	CHRISTOPHER BARTELS	2184

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/05/2014	05/19/2015							
	1	✓	✓							
	2	✓	-							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	-							
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	11	✓	✓							
	12	✓	✓							
	13	✓	✓							
	14	✓	-							
	15	✓	✓							
	16	✓	✓							
	17	✓	✓							
	18	✓	-							
	19	✓	✓							
	20	✓	-							

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	75	("5276458" | "20070055876" | "20080152023" | "7729874" | "7860398" | "20040143847" | "20070222779" | "7979590" | "20060092152" | "20070036158" | "20070165997" | "20050141851" | "20050182876" | "20070186015" | "20070283071" | "7176980" | "7873980" | "7539808" | "20060206734" | "20070070402" | "20040125886" | "20020060676" | "20080134237" | "20070280646" | "20090177818" | "20090178086" | "20100283894" | "7856520" | "20050225547" | "20070047638" | "20070220150" | "20070242062" | "5943029" | "20050116884" | "20050228995" | "20060280055" | "20070236605" | "7079129").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/12/09 18:48
S2	298987	"I9" not S1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/12/09 18:48
S20	40	(US-6618773-$ or US-7761709-$ or US-7899941-$ or US-8462843-$ or US-8375147-$ or US-8510483-$ or US-8453008-$ or US-7827319-$ or US-8266335-$ or US-7523241-$ or US-7979910-$ or US-7962663-$ or US-6738856-$ or US-7124326-$ or US-8244925-$ or US-8356121-$ or US-8199258-$ or US-8447158-$ or US-7889201-$ or US-7995043-$).did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/12/20 21:16
S21	5	S20 and (usb universal near2 bus upnp pnp plug near2 play)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/12/20 21:16
S24	15	hpd adj (switch$3 mux toggl$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/03 17:42
S25	348	hpd with ddc	US-PGPUB; USPAT;	OR	ON	2014/07/03 17:50

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S26	477	hpd with (cec ddc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/03 17:50
S27	311	hpd with (cec ddc) and edid	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/03 17:50
S28	245	S27 and (switch$3 bus adj interfac$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/03 17:51
S29	254	S27 and (switch$3 bus adj interfac$3 master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/03 17:51
S30	290	S27 and (switch$3 bus adj interfac$3 master slave source sink)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/03 17:51
S31	8	"7761709"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/10 15:40
S32	341	lamp adj ballast and lcd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/10 15:42
S33	82	lamp adj ballast and lcd and (pcie bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/10 15:42

S34	82	lamp adj ballast and lcd and (pcie bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/10 17:08
S35	12	S34 and projector	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/10 17:08
S36	2	(US-20040027515-$ or US-20080074622-$).did.	US-PGPUB	OR	OFF	2014/07/10 18:13
S37	7781	((G03B21/20 OR G03B21/2046 OR G03B21/2053 OR G09G2370/047 OR G09G5/00 OR G09G5/006 OR H05B41/2921 G06F3/00 G06F3/042 G06F3/14).CPC.)	US-PGPUB	OR	OFF	2014/07/10 18:37
S38	80	S37 and hpd with (cec ddc) and edid	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/10 18:37
S39	61	hpd and switch$3 and (diode delimiter) and (ddcv5 ddc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/11/12 14:52
S40	68	hpd and switch$3 and (diode delimiter) and (ddcv5 ddc scl sda)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/11/12 15:25
S41	102	hpd and (diode delimiter) and (ddcv5 ddc scl sda)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/11/13 13:37
S42	86	("5276458" | "20070055876" | "20080152023" | "7729874" | "7860398" | "20040143847" | "20070222779" | "7979590" | "20060092152" | "20070036158" | "20070165997" | "20050141851" | "20050182876" | "20070186015" | "20070283071" | "7176980" | "7873980" | "7539808" | "20060206734" | "20070070402" | "20040125886" | "20020060676" | "20080134237" | "20070280646" | "20090177818" | "20090178086" |	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:08

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S43	332385	"I9" not S42	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:08
S44	40	(US-6618773-$ or US-7761709-$ or US-7899941-$ or US-8462843-$ or US-8375147-$ or US-8510483-$ or US-8453008-$ or US-7827319-$ or US-8266335-$ or US-7523241-$ or US-7979910-$ or US-7962663-$ or US-6738856-$ or US-7124326-$ or US-8244925-$ or US-8356121-$ or US-8199258-$ or US-8447158-$ or US-7889201-$ or US-7995043-$).did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/05/15 23:08
S45	5	S44 and (usb universal near2 bus upnp pnp plug near2 play)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/05/15 23:08
S46	19	hpd adj (switch$3 mux toggl$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:08
S47	409	hpd with ddc	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:08
S48	569	hpd with (cec ddc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:08
S49	371	hpd with (cec ddc) and edid	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:08
S50	298	S49 and (switch$3 bus adj interfac$3)	US-PGPUB; USPAT; USOCR;	OR	ON	2015/05/15 23:08

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S51	307	S49 and (switch$3 bus adj interfac$3 master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:08
S52	350	S49 and (switch$3 bus adj interfac$3 master slave source sink)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:08
S53	9	"7761709"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:08
S54	364	lamp adj ballast and lcd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:08
S55	90	lamp adj ballast and lcd and (pcie bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:08
S56	90	lamp adj ballast and lcd and (pcie bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:08
S57	14	S56 and projector	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:08
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S59	8083	((G03B21/20 OR G03B21/2046 OR G03B21/2053 OR G09G2370/047 OR G09G5/00 OR G09G5/006 OR H05B41/2921 G06F3/00 G06F3/042 G06F3/14).CPC.)	US-PGPUB	OR	OFF	2015/05/15 23:08

S60	104	S59 and hpd with (cec ddc) and edid	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:08
S61	72	hpd and switch$3 and (diode delimiter) and (ddcv5 ddc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:08
S62	79	hpd and switch$3 and (diode delimiter) and (ddcv5 ddc scl sda)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:08
S63	114	hpd and (diode delimiter) and (ddcv5 ddc scl sda)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:08
S64	18	S63 and (supply near2 voltage vss vdd) with (connect$3 port cable)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:11
S65	2	"12530300"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:12
S66	18	S63 and (supply near2 voltage vss vdd ddc5v) with (connect$3 port cable)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:23
S67	18	S63 and (supply near2 voltage vss vdd ddc5v ddc near2 (5v volt)) with (connect$3 port cable)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:24
S68	56	S63 and (supply near2 voltage vss vdd ddc5v ddc near2 (5v volt) source and sink) with (connect$3 port cable)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2015/05/15 23:24

			DERWENT; IBM_TDB			
S69	38	S68 not S67	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/15 23:38

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S3	104117	(710/15,1).ccls. ("713" "714").clas.	USPAT; UPAD	OR	ON	2013/12/09 17:27
S4	4364	S3 and (extend$3 near4 (display$3 identif$7 data) edid)	USPAT; UPAD	OR	ON	2013/12/09 17:54
S5	2751	S4 and (voltage vss vcc power power near2 supply)	USPAT; UPAD	OR	ON	2013/12/09 17:54
S6	2646	S5 and (error threshold bias limit$3)	USPAT; UPAD	OR	ON	2013/12/09 17:55
S7	499	S6 and (ddc display$3 near2 (data channel))	USPAT; UPAD	OR	ON	2013/12/09 17:55
S8	536	S6 and (ddc display$3 near2 (data channel) vesa svga hdmi displayport)	USPAT; UPAD	OR	ON	2013/12/09 17:56
S9	536	S6 and (ddc display$3 near2 (data channel) vesa svga hdmi displayport display adj port)	USPAT; UPAD	OR	ON	2013/12/09 17:56
S10	147	S9 and (hpd hot near2 (plug$4 detect$3 swap$4) (chang$3 configu$5 repair$3) near5 (interrupt$3 servic$3 disrupt$3))	USPAT; UPAD	OR	ON	2013/12/09 17:58
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S14	12467	((extend$3 near4 (display$3 identif$7 data) edid)).clm.	USPAT; UPAD	OR	ON	2013/12/09 20:37
S15	1973	S14 and (voltage vss vcc power power near2 supply).clm.	USPAT; UPAD	OR	ON	2013/12/09 20:38
S16	317	S15 and (error threshold bias limit$3).clm.	USPAT;	OR	ON	2013/12/09

			UPAD			20:38
S17	27	S16 and (ddc display$3 near2 (data channel)).clm.	USPAT; UPAD	OR	ON	2013/12/09 20:38
S18	27	S16 and (ddc display$3 near2 (data channel) vesa svga hdmi displayport display adj port).clm.	USPAT; UPAD	OR	ON	2013/12/09 20:39
S19	1	S18 and (hpd hot near2 (plug$4 detect$3 swap$4) (chang$3 configu$5 repair$3) near5 (interrupt$3 servic$3 disrupt$3)).clm.	USPAT; UPAD	OR	ON	2013/12/09 20:39
S22	20	"Term Removed"	USPAT	OR	OFF	2013/12/20 21:15
S23	20	"Term Removed"	USPAT	OR	OFF	2013/12/20 21:15
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S71	4903	S70 and (extend$3 near4 (display$3 identif$7 data) edid)	USPAT; UPAD	OR	ON	2015/05/15 23:08
S72	3106	S71 and (voltage vss vcc power power near2 supply)	USPAT; UPAD	OR	ON	2015/05/15 23:08
S73	3000	S72 and (error threshold bias limit$3)	USPAT; UPAD	OR	ON	2015/05/15 23:08
S74	592	S73 and (ddc display$3 near2 (data channel))	USPAT; UPAD	OR	ON	2015/05/15 23:08
S75	644	S73 and (ddc display$3 near2 (data channel) vesa svga hdmi displayport)	USPAT; UPAD	OR	ON	2015/05/15 23:08
S76	644	S73 and (ddc display$3 near2 (data channel) vesa svga hdmi displayport display adj port)	USPAT; UPAD	OR	ON	2015/05/15 23:08
S77	187	S76 and (hpd hot near2 (plug$4 detect$3 swap$4) (chang$3 configu$5 repair$3) near5 (interrupt$3 servic$3 disrupt$3))	USPAT; UPAD	OR	ON	2015/05/15 23:08
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S81	14033	((extend$3 near4 (display$3 identif$7 data) edid)).clm.	USPAT; UPAD	OR	ON	2015/05/15 23:08
S82	2268	S81 and (voltage vss vcc power power near2 supply).clm.	USPAT; UPAD	OR	ON	2015/05/15 23:08

S83	351	S82 and (error threshold bias limit$3).clm.	USPAT; UPAD	OR	ON	2015/05/15 23:08
S84	30	S83 and (ddc display$3 near2 (data channel)).clm.	USPAT; UPAD	OR	ON	2015/05/15 23:08
S85	30	S83 and (ddc display$3 near2 (data channel) vesa svga hdmi displayport display adj port).clm.	USPAT; UPAD	OR	ON	2015/05/15 23:08
S86	3	S85 and (hpd hot near2 (plug$4 detect$3 swap$4) (chang$3 configu$5 repair$3) near5 (interrupt$3 servic$3 disrupt$3)).clm.	USPAT; UPAD	OR	ON	2015/05/15 23:08
S87	20	"Term Removed"	USPAT	OR	OFF	2015/05/15 23:08
S88	20	"Term Removed"	USPAT	OR	OFF	2015/05/15 23:08

5/ 16/ 2015 11:53:40 PM
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13434273	MAXWELL ET AL.
	Examiner	Art Unit
	CHRISTOPHER BARTELS	2184

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner
(G09G5, H04N, G06F, H04L, G08C and relevant sub-groups) text search in EAST	07/02/2014-07/03/2014	C.A.B.
(G03B, G09G, H05B, G06F and relevant sub-groups) text search in East	05/15/2015	C.A.B.

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Text search in EAST (ALL DATABASES)	12/09/13, 12/20/13, 7/2/14, 5/15/2015	C.A.B.
710/15, 1 AND (713 714) text search in East	12/09/2013	C.A.B.
Inventor Search performed (USPAT, UPAD)	12/09/2013	C.A.B.

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/C.B./ Examiner.Art Unit 2184	

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

APPLICANT:	Conrad Arlo Maxwell, et al.
APPLICATION NO.:	13/434,273
FILING DATE:	March 29, 2012
TITLE:	Method, Apparatus And System For Transitioning An Audio/Video Device Between A Source Mode And A Sink Mode
EXAMINER:	Christopher A. Bartels
GROUP ART UNIT:	2184
CONFIRMATION NO.	7248
ATTY. DKT. NO.:	30850-25622/US

CERTIFICATE OF ELECTRONIC (EFS-WEB) TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with 37 C.F.R. § 1.8(a)(i)(C) from the **Pacific Time Zone** of the United States on the local date shown below.

Dated: January 20, 2015 By: /Goutham Kondapalli/
Goutham Kondapalli, Reg. No. 71,166

AMENDMENT A AND RESPONSE UNDER 37 CFR § 1.111

This Amendment and Response is in reply to the Office action dated September 10, 2014. A fee for a two-month extension of time is submitted herewith to extend a statutory period for response the Office action to February 10, 2015. Please amend the application as follows:

Amendments to the Claims begin on page 2 of this paper.

Remarks follow the Amendments to the Claims section.

DELL/HP/LENOVO EXHIBIT 1002
Page 337

AMENDMENTS TO THE CLAIMS

Claims 1, 4, 5, 7, 9, 12, 13, 15, 17, and 19 are hereby amended, and claims 2, 6, 8, 10, 14, 16, 18, and 20 are canceled. All pending claims are produced below.

1. (Currently Amended): A method ~~at an audio/video (AV) device, the method~~ comprising:

detecting with control circuitry ~~an indication of one of a power up event at the AV device, a power down event at the AV device, or a reset event at~~ of a first audio/video (AV) device, a coupling between the first AV device and a second AV device; [[and]]

determining whether a first supply voltage is provided at a channel of a connector, the connector coupling the first AV device and the second AV device;

in response to determining that the first supply voltage is provided at the channel of the connector, configuring communication logic of the first AV device to operate the first AV device in an AV sink operation mode, wherein the first AV device receives AV data provided to the first AV device via the connector and receives power from the first supply voltage provided to the first AV device at the channel of the connector in the AV sink operation mode, the AV sink operation mode being a default mode of operation; and

in response to determining that the first supply voltage is not provided at the channel of the connector, ~~the indication, automatically initializing~~ configuring the communication logic of the first AV device ~~with the control circuitry~~ to transition the first AV device from the AV sink operation mode to an AV source operation mode, ~~wherein an AV sink operation mode of the communication logic is for the communication logic to receive AV data provided to the device via a connector, the AV sink operation mode further for the communication logic to receive power from a first supply voltage provided to the~~

~~device at a channel of the connector, wherein an AV source operation mode of the communication logic is for the communication logic to send~~ wherein the first AV device sends AV data ~~from the device~~ via the connector~~, the AV source operation mode further for the communication logic to provide~~ and provides a second supply voltage at the channel of the connector in the AV source operation mode~~, and wherein automatically initializing the communication logic includes placing the communication logic into a default operation mode which prevents the second supply voltage from being provided by the communication logic at the channel of the connector~~.

2. (Canceled)

3. (Original) The method of claim 1, wherein the default operation mode is for communication according to a high-definition multimedia interface standard.

4. (Currently Amended) The method of claim 1, wherein ~~the AV Source operation mode is further for the communication logic to provide~~ a first ~~total amount of~~ impedance is provided for a data channel of the connector in the AV source operation mode, and ~~wherein the default operation mode further prevents~~ the first ~~total amount of~~ impedance is not provided for the data channel ~~from being provided by the communication logic~~ in the AV sink operation mode.

5. (Currently Amended) The method of claim 1, further comprising:

~~detecting a connectivity of the device to another device via the connector, the detecting the connectivity while the communication logic is in the default operation mode;~~

~~in response to the detected connectivity, performing a determination of whether to transition the communication logic from the default operation mode to another operation mode; and~~

performing an AV data exchange ~~with the other~~ between the first device and the second device ~~based on the determination~~.

6. (Canceled)

7. (Currently Amended) The method of claim 5, further comprising:

detecting a change to the connectivity of the first AV device after the AV data exchange; and

in response to the detected change to the connectivity, placing the communication logic into the AV sink operation mode ~~a first operation mode which prevents the second supply voltage from being provided by the communication logic at the channel of the connector~~.

8. (Canceled)

9. (Currently Amended) [[A]] An audio/video (AV) device comprising:

communication logic to couple to a connector, the communication logic including circuitry configured to implement:

an ~~audio/video (AV) Sink~~ AV sink operation mode for the communication logic to receive AV data provided to the AV device at the connector~~, the AV Sink operation mode further for the communication logic~~ and to receive power from a first supply voltage provided to the AV device via a channel of the connector[[;]], the AV sink operation mode being a default mode of operation for the AV device, and

an AV ~~Source~~ source operation mode for the communication logic to send AV data from the AV device via the connector~~, the AV Source operation mode further for the communication logic~~ and to provide a second supply voltage at the channel of the connector; and

control logic including circuitry to ~~automatically initialize~~ configure the communication logic ~~in response to one of a power up event at the AV device, a power down event at the AV device, or a reset event at the AV device, wherein the control logic to place the communication logic into a default operation mode which prevents the second supply voltage from being provided by the communication logic at the channel of the connector~~ to operate the AV device in the AV sink operation mode in response to determining that the first supply voltage is provided at the channel of the connector and to configure the communication logic to transition the AV device from the AV sink operation mode to the AV source operation mode in response to determining that the first supply voltage is not provided at the channel of the connector.

10. (Canceled)

11. (Original) The device of claim 9, wherein the default operation mode is for communication according to a high-definition multimedia interface standard.

12. (Currently Amended) The device of claim 9, wherein the ~~AV source operation mode is further for the~~ communication logic is further configured to provide a first ~~total amount of~~ impedance for a data channel of the connector in the AV source operation mode and ~~wherein the default operation mode further prevents~~ is configured to not provide the first ~~total amount of~~ impedance for the data channel ~~from being provided by the communication logic~~ in the AV sink operation mode.

13. (Currently Amended) The device of claim 9, further comprising:

detector logic to detect, while the communication logic is in the default operation mode, a ~~connectivity~~ coupling of the AV device to another AV device via the connector;

DELL/HP/LENOVO EXHIBIT 1002
Page 341

~~wherein, in response to the detected connectivity, the control logic further to perform a determination of whether to transition the communication logic from the default operation mode to another operation mode;~~ and

wherein the communication logic is further configured to perform an AV data exchange with the other device ~~based on the determination~~ in response to the detection.

14. (Canceled)

15. (Currently Amended) A system comprising:

a connector;

communication logic coupled to the connector, the communication logic including circuitry configured to implement:

an audio/video (AV) sink operation mode for the communication logic to receive AV data provided to the system at the connector~~, the AV sink operation mode further for the communication logic~~ and to receive power from a first supply voltage provided to the system at a channel of the connector, the AV sink operation mode being a default mode of operation for the system,[[;]] and

an AV source operation mode for the communication logic to send AV data from the system via the connector~~, the AV source operation mode further for the communication logic~~ and to provide a second supply voltage at the channel of the connector; and

DELL/HP/LENOVO EXHIBIT 1002
Page 342

control logic including circuitry to ~~automatically initialize~~ configure the communication logic ~~in response to one of a power up event at the AV device, a power down event at the AV device, or a reset event at the AV device, wherein the control logic to place the communication logic into a default operation mode which prevents the second supply voltage from being provided by the communication logic at the channel of the connector~~ to operate the AV device in the AV sink operation mode in response to determining that the first supply voltage is provided at the channel of the connector and to configure the communication logic to transition the AV device from the AV sink operation mode to the AV source operation mode in response to determining that the first supply voltage is not provided at the channel of the connector.

16. (Canceled)

17. (Currently Amended) The system of claim 15, further comprising:

detector logic to detect, while the communication logic is in the default operation mode, a ~~connectivity~~ coupling of the system to [[a]] an AV device via the connector;

~~wherein, in response to the detected connectivity, the control logic further to perform a determination of whether to transition the communication logic from the default operation mode to another operation mode;~~ and

wherein the communication logic is further configured to perform an AV data exchange with the AV device ~~based on the determination~~ in response to the detection.

18. (Canceled)

19. (Currently Amended) The system of claim 17, the ~~detect~~ detector logic further configured to detect a change to the connectivity after the AV data exchange, wherein, in response to the detected change to the connectivity, the control logic further configured to place the communication logic into the AV sink operation mode ~~a first operation mode which prevents the second supply voltage from being provided by the communication logic at the channel of the connector~~.

20. (Canceled)

DELL/HP/LENOVO EXHIBIT 1002
Page 344

REMARKS

Claims 1-20 were pending in the application. Claims 1-20 were rejected in an Office action dated September 10, 2014 ("Office Action").

Claims 1, 4, 5, 7, 9, 12, 13, 15, 17, and 19 are hereby amended, and claims 2, 6, 8, 10, 14, 16, 18, and 20 are canceled Support for these amendments can be found, for example, at paragraphs [0049]-[0054] of the specification.

Based on the above Amendment and the following Remarks, reconsideration and withdrawal of all rejections is respectfully requested.

Summary of Substance of Interview

Applicant's representatives Jason E. Amsel (Reg. No. 60,650) and Goutham Kondapalli (Reg. No. 71,166), conducted a telephonic interview with Examiner Christopher A. Bartels and SPE Henry Tsai on Friday, January 16, 2015. During the interview, pending claim 1 and its rejection was discussed. An agreement was reached during the interview that claims as amended overcome the prior art of record.

Claim Rejections under 35 U.S.C §§ 102 and 103

Claims 1-2, 4-10, and 12-20 are rejected pre-AIA under 35 U.S.C. § 102(e) as being anticipated by over Noorbakhsh et al. (US Pat No. 7995043 B2). Claims 3 and 11 are rejected under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over Noorbakhsh in view of Yato (US Pat No. 7889201 B2). These rejections are addressed together for clarity and are now overcome.

Claim 1 as amended, *inter alia*, recites:

> in response to determining that the first supply voltage is not provided at the channel of the connector, configuring the communication logic of the first AV device to transition the first AV device from the AV sink operation mode to an AV

source operation mode, the first AV device sends AV data via the connector and provides a second supply voltage at the channel of the connector in the AV source operation mode.

As agreed in the interview of January 16, 2015, Noorbakhsh fails to disclose the above-recited claim element as amended. *See* Noorbakhsh, col. 2:57-60 and col. 6:14-42.

Consequently, independent claim 1 is patentably distinguishable over the cited art. Independent claims 9 and 15 also recited features similar to the features discussed above with reference to claim 1, and therefore are patentably distinguishable over the cited art.

Each of the dependent claims 3, 4, 5, 7, 11, 12, 13, 17, and 19 incorporates the limitations of one of independent claims 1, 9, or 15. Therefore, these dependent claims are also patentably distinguishable over the cited art for at least the same reasons as set forth above.

Accordingly, withdrawal of these rejections is respectfully requested.

CONCLUSION

Therefore, reconsideration of the basis for the rejections to these claims and allowance of these claims is respectfully requested.

In addition, the Examiner is invited to contact the undersigned at the number provided below if the Examiner believes such contact will help expedite furtherance of this application.

Respectfully submitted,

Dated: January 20, 2015

/Goutham Kondapalli/

Goutham Kondapalli, Reg. No. 71,166
FENWICK & WEST LLP
801 California Street
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Electronic Patent Application Fee Transmittal

Application Number:	13434273
Filing Date:	29-Mar-2012
Title of Invention:	METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE
First Named Inventor/Applicant Name:	Conrad Arlo Maxwell
Filer:	Goutham Kondapalli/Lynn Hoffman-Luce
Attorney Docket Number:	30850-25622

Filed as Large Entity

Filing Fees for **Utility under 35 USC 111(a)**

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 2 months with $0 paid	1252	1	600	600
Miscellaneous:				
			Total in USD ($)	**600**

Electronic Acknowledgement Receipt

EFS ID:	21249470
Application Number:	13434273
International Application Number:	
Confirmation Number:	7248
Title of Invention:	METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE
First Named Inventor/Applicant Name:	Conrad Arlo Maxwell
Customer Number:	120363
Filer:	Goutham Kondapalli
Filer Authorized By:	
Attorney Docket Number:	30850-25622
Receipt Date:	20-JAN-2015
Filing Date:	29-MAR-2012
Time Stamp:	15:07:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$600
RAM confirmation Number	1657
Deposit Account	192555
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		25622_US_Amendment_A.pdf	109563 d96e4a30f0a19b8265bb9ab264f477f23c62b8ce	yes	11

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	8
	Applicant Arguments/Remarks Made in an Amendment	9	11

Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31330 05c463b774598447c0ed2ee2917a176c263fe8ac	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	140893		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/434,273	Filing Date 03/29/2012	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	01/20/2015	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 12	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/STEFANIE BRYCE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)				*Complete if Known*	
				Application Number	13/434,273
				Filing Date	March 29, 2012
				First Named Inventor	Conrad Arlo Maxwell
				Art Unit	2184
				Confirmation Number	7248
				Examiner Name	Christopher A. Bartels
Sheet	1	of	2	Attorney Docket Number	30850-25622/US

U.S. PATENT DOCUMENTS				
		Document No.		
Examiner Initials*	Cite No.[1]	Number – Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
	A1	US-2009/0046690 A1	02-19-2009	Hsieh

FOREIGN PATENT DOCUMENTS					
		Foreign Patent Document			
Examiner Initials*	Cite No.[1]	Country Code[3] – Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6]

OTHER REFERENCES – NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[6]
	C1	Extended European Search Report, European Application No. 12762781.8, August 13, 2014, 7 pages.	

EXAMINER SIGNATURE	
Examiner Signature	
Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (option). [2] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [3] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

[5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)				Complete if Known	
				Application Number	13/434,273
				Filing Date	March 29, 2012
				First Named Inventor	Conrad Arlo Maxwell
				Art Unit	2184
				Confirmation Number	7248
				Examiner Name	Christopher A. Bartels
Sheet	2	of	2	Attorney Docket Number	30850-25622/US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Goutham Kondapalli/	Date (YYYY-MM-DD)	2014-09-12
Name/Print	Goutham Kondapalli	Registration Number	71,166

30850/25622/DOCS/3488724.1

DELL/HP/LENOVO EXHIBIT 1002
Page 354

Electronic Patent Application Fee Transmittal

Application Number:	13434273
Filing Date:	29-Mar-2012
Title of Invention:	METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE
First Named Inventor/Applicant Name:	Conrad Arlo Maxwell
Filer:	Goutham Kondapalli/Sarah Glenn
Attorney Docket Number:	30850-25622

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	20128978
Application Number:	13434273
International Application Number:	
Confirmation Number:	7248
Title of Invention:	METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE
First Named Inventor/Applicant Name:	Conrad Arlo Maxwell
Customer Number:	120363
Filer:	Goutham Kondapalli
Filer Authorized By:	
Attorney Docket Number:	30850-25622
Receipt Date:	12-SEP-2014
Filing Date:	29-MAR-2012
Time Stamp:	17:39:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	4214
Deposit Account	192555
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Information Disclosure Statement (IDS) Form (SB08)	25622IDS.pdf	183448 ffa953586900c8882e20527a1a37a39004aeb8ad	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
2	Non Patent Literature	EP_Ext_Search_Report_EP12762781_8_Aug_13_2014.pdf	3141607 0b36e5e736ccab7a85660b6cd75043794211ef4e	no	7
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	31020 3a5ebb798f1a4c78d98bf33fcf60f0ba529e5a8b	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	3356075		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/434,273	03/29/2012	Conrad Arlo Maxwell	30850-25622	7248

120363 7590 09/10/2014

Silicon Image/FENWICK
801 California Street
Mountain View, CA 94041

EXAMINER	
BARTELS, CHRISTOPHER A.	

ART UNIT	PAPER NUMBER
2184	

NOTIFICATION DATE	DELIVERY MODE
09/10/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ptoc@fenwick.com

Office Action Summary	Application No. 13/434,273	Applicant(s) MAXWELL ET AL.	
	Examiner CHRISTOPHER BARTELS	Art Unit 2184	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/29/2012*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☒ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *3/29/2012* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *12/09/2013*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

2. Claims 1-20 are pending as of listing filed on 3/29/2012.

Drawings

3. The drawings were received on 3/29/2012. These drawings are accepted.

Specification

4. The disclosure is objected to because of the following informalities: In the last two lines of [0004], the term DVD is used once in the entire specification. Thus, “DVD” must be spelt out. Appropriate correction is required.

Priority

5. Receipt is acknowledged of certified copies of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

6. The information disclosure statement (IDS) submitted on 12/09/2013. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-2, 4-10, and 12-20 are rejected pre-AIA under 35 U.S.C. 102(e) as being anticipated by over Noorbakhsh et al. (US Pat No. ***7995043 B2***, *hereinafter referred to as Noor*).

Referring to claim 1, Noor discloses a method at an audio/video (AV) device {AV device "system 100", see Fig. 1, Col 5, lines 23-48.}, ***the method comprising:***

detecting with control circuitry {control circuitry "controller 102" (see Fig. 1, Col 6, lines 14-42) detects an indication through "on-board power regulator 124" in one of a power up event "ON_MODE" or a power down event "OFF_MODE".} ***an indication of one of a power up event at the AV device, a power down event at the AV device, or a reset event at the AV device;***

and in response to the indication, automatically initializing communication logic {initializes communication logic "bridge section 120" (Col 6, lines 35-42).} ***of the AV device with the control circuitry, wherein an AV sink operation mode*** {AV sink mode "controller 102 conforms to the I2C protocol… [since] it has its own bus that can act as a [sink] receiver and/or [source] transmitter" (see Fig. 1, Col 6, lines 4-13).} ***of the communication logic is for the communication logic to receive AV data provided*** {receiving AV data "DDC-DVI"/"DDC-VGA channel" ports 108a/b via a connector "cable 112" (see Figs. 1 and 3, Col 6, lines 20-27).} ***to the device via a connector, the AV sink operation mode further for the communication logic to receive power from a first supply voltage*** {in the off mode, first supply voltage "power is supplied by either of [channels] DDC ports cable (VGA/DVI)" in the connector "cable 112" (see Figs. 1 and 2, Col 8, lines 21-42).} ***provided to the device at a channel of the connector, wherein an AV source operation mode of the communication logic is for the communication logic to send AV data*** {reiterating Col 6, lines 4-13, this time as AV source operation mode "transmitter" on the basis of duplex operation "it is mean that [AV] data can be transferred in both directions at the same time" (Col 4, lines 60-65).} ***from the device via the connector, the AV source operation mode further for the***

communication logic to provide a second supply voltage {see Fig. 5E, allowing two paths toward different power supply voltages (either step 582 or 578, Col 10, lines 23-37); in this case second supply voltage "by the on-board power supply only step 582" during ON_MODE.} ***at the channel of the connector, and wherein automatically initializing the communication logic includes placing the communication logic into a default operation mode*** {by default, thanks to "DDC standard" the device "system 100" and communication logic works in a default operation mode recognizing the external device "uses this channel to convey its identity and capabilities [as a source device] to the display adapter[/system 100]" thus causing it into AV sink mode (Col 5, lines 43-48) which is the "no branch of step 576" thereby preventing the second supply voltage "step 582" (see Fig. 5E).} ***which prevents the second supply voltage from being provided by the communication logic at the channel of the connector.***

As per claim 2, the rejection of claim 1 is incorporated and Noor discloses wherein the default operation mode is the AV sink operation mode {see claim 1, Col 5, lines 40-48.}.

As per claim 4, the rejection of claim 1 is incorporated and Noor discloses wherein the AV Source operation mode is further for the communication logic to provide a first total amount of impedance {total amount of impedance "resistor R2" (see Fig. 4, Col 9, lines 1-19) for an "auto activity detection circuit 400"/"detection circuit 128" when recognizing the data channel "virtual EDID operation" of the connector "cable 112" (Col 7, lines 22-48).} ***for a data channel of the connector, and wherein the default operation mode further prevents the first total amount of impedance*** {see claim 1 and note the "logic combination of this bit register bits] and Tclk is used to do the power switching [of Figure 5E]" and thus affecting the data channel provided by the communication logic (Col 7, lines 45-49).} ***for the data channel from being provided by the communication logic.***

As per claim 5, the rejection of claim 1 is incorporated and Noor discloses further comprising:

detecting a connectivity {see claim 1, as connectivity to another device "video source 10" (see Fig. 1) as claimed.} ***of the device to another device via the connector, the detecting***

the connectivity while the communication logic is in the default operation mode;

in response to the detected connectivity, performing a determination of whether to transition {transition to another operation "ON_MODE" (steps 582-586) when the device "system 100" operating in the AV source mode "every device connected to the I2C bus… act as a transmitter, depending on the functionality" (Col 6, lines 10-13).} ***the communication logic from the default operation mode to another operation mode; and performing an AV data exchange with the other device*** {see claim 1.} ***based on the determination.***

As per claim 6, the rejection of claim 5 is incorporated and Noor discloses wherein detecting the connectivity includes detecting that the other device {see either claims 1 or 5 and Figure 1 and Figure 5.} ***is providing the first supply voltage to the channel of the connector.***

As per claim 7, the rejection of claim 5 is incorporated and Noor discloses further comprising:

detecting a change to the connectivity after the AV data exchange; and in response to the detected change to the connectivity, placing the communication logic into a first

operation mode which prevents {see either claims 1 or 5 and Figure 1 and Figure 5.} ***the second supply voltage from being provided by the communication logic at the channel of the connector.***

As per claim 8, the rejection of claim 7 is incorporated and Noor discloses wherein the first operation mode is the default operation mode {see claim 2.}.

Referring to claims 9-10, 12-20 are device claims corresponding to the method claims of claims 1-2 and 4-8, respectively, thereby rejected under the same reasoning recited in claims 1-2, 4-8 above.

Claim Rejections - 35 USC § 103

9. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3 and 11 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Noor in view of Yato (US Pat No. ***7889201 B2***).

As per claim 3, the rejection of claim 1 is incorporated however Noor does not appear to explicitly disclose any limitation in this dependent claim.

Furthermore, Yato discloses ***wherein the default operation mode is for communication according to a high-definition multimedia interface standard.***

Noor and Yato are analogous art because they are from the same problem-solving area, methods and systems for communicating with display devices.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Noor and Yato before him or her, to modify Noor's "system 100" to incorporate Yato's "HDMI connector 18" (see Fig. 8).

The suggestion/motivation for doing so would have been to provide a HDMI cable can transmit various commands for operation control of the connection destination (Yato Col 3, lines 24-30) thereby addressing the problems arising in power switching states of large-screen high-definition receivers which manages transmit of data to acquire information necessary for performing operation control (Yato Col 1 line 65 through Col 2, line 7).

Therefore, it would have been obvious to combine Yato with Noor to obtain the invention as specified in the instant claim(s).

As per claim 11 is a device claim corresponding in claim functionality of the method claim of claim 3, thereby rejected under the same rationale as claim 3 above.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure (as noted on Form 892).

The following reference(s) employs a system teaching limitations cited in claim 1 applicable as a 103 rejection:

US 6618773 B1, US 7761709 B2, US 8510483 B2, US 8453008 B2, US 7827319 B2, US 8266335 B2, US 7979910 B2, US 8447158 B2.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER A. BARTELS whose telephone number is (571)270-3182. The examiner can normally be reached on Monday To Thursday ; 7:30am to 5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. A. B./

/HENRY TSAI/
Supervisory Patent Examiner, Art Unit 2184

Notice of References Cited	Application/Control No. 13/434,273	Applicant(s)/Patent Under Reexamination MAXWELL ET AL.	
	Examiner CHRISTOPHER BARTELS	Art Unit 2184	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,618,773 B1	09-2003	Chang et al.	710/16
*	B	US-7,761,709 B2	07-2010	Choi, Young-hun	713/168
*	C	US-7,827,319 B2	11-2010	Kimura et al.	710/5
*	D	US-7,979,910 B2	07-2011	Mantani, Nobunori	726/26
*	E	US-8,266,335 B2	09-2012	Kitano et al.	710/15
*	F	US-8,453,008 B2	05-2013	Kimoto, Tatsuya	714/4.1
*	G	US-8,447,158 B2	05-2013	Yamamoto, Yuji	386/200
*	H	US-8,510,483 B2	08-2013	Kawai, Shigehiro	710/33
*	I	US-7,995,043	08-2011	Noorbakhsh et al.	345/204
*	J	US-7,889,201	02-2011	Yato, Shinsuke	345/501
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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CONFIRMATION NO. 7248

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/434,273	03/29/2012	710	2184	30850-25622

APPLICANTS

Invensense, Inc, San Jose, CA, Assignee (with 37 CFR 1.172 Interest);

INVENTORS

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Glenn L. Marks, Corona, CA;
Jonathan Regalado-Hawkey, Woolston, UNITED KINGDOM;
Christian Rudel, Wunstork, GERMANY;

**** CONTINUING DATA ***************************

This appln claims benefit of 61/470,431 03/31/2011

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

04/09/2012

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /CHRISTOPHER A. BARTELS/ Examiner's Signature	☐ Met after Allowance C.A.B. Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		UT	7	20	3

ADDRESS

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Mountain View, CA 94041
UNITED STATES

TITLE

METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE

FILING FEE RECEIVED		
1380	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known

Application Number	13/434,273
Filing Date	March 29, 2012
First Named Inventor	Maxwell, Conrad
Group Art Unit	2184
Examiner Name	Bartels, Christopher A.

Sheet 1 of 1

Attorney Docket No: 8029P107

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/C.B./		US-20080205306	08/28/2008	Saito, T.	
/C.B./		US-20080270635	10/30/2008	Nakahama, M.	
/C.B./		US-20090083825	03/26/2009	Miller, R. D., et al.	
/C.B./		US-20100131782	05/27/2010	Higuchi, S.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
/C.B./		"International Search Report and Written Opinion of the International Searching Authority, for International Patent Application No. PCT/US2012/031463 (Attorney Docket No. 8029P107PCT)", (October 31, 2012), Whole Document	
/C.B./		"Preliminary Report on Patentability (Chapter I of the Patent Cooperation Treaty), for International Patent Application No. PCT/US2012/031463 (Attorney Docket No. 8029P107PCT)", (October 10, 2013), Whole Document	

EXAMINER /Christopher Bartels/ **DATE CONSIDERED** 09/05/2014

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.B./

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	75	("5276458" | "20070055876" | "20080152023" | "7729874" | "7860398" | "20040143847" | "20070222779" | "7979590" | "20060092152" | "20070036158" | "20070165997" | "20050141851" | "20050182876" | "20070186015" | "20070283071" | "7176980" | "7873980" | "7539808" | "20060206734" | "20070070402" | "20040125886" | "20020060676" | "20080134237" | "20070280646" | "20090177818" | "20090178086" | "20100283894" | "7856520" | "20050225547" | "20070047638" | "20070220150" | "20070242062" | "5943029" | "20050116884" | "20050228995" | "20060280055" | "20070236605" | "7079129").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/12/09 18:48
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S20	40	(US-6618773-$ or US-7761709-$ or US-7899941-$ or US-8462843-$ or US-8375147-$ or US-8510483-$ or US-8453008-$ or US-7827319-$ or US-8266335-$ or US-7523241-$ or US-7979910-$ or US-7962663-$ or US-6738856-$ or US-7124326-$ or US-8244925-$ or US-8356121-$ or US-8199258-$ or US-8447158-$ or US-7889201-$ or US-7995043-$).did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/12/20 21:16
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EAST Search History (Interference)

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S3	104117	(710/15,1).ccls. ("713" "714").clas.	USPAT; UPAD	OR	ON	2013/12/09 17:27
S4	4364	S3 and (extend$3 near4 (display$3 identif$7 data) edid)	USPAT; UPAD	OR	ON	2013/12/09 17:54
S5	2751	S4 and (voltage vss vcc power power near2 supply)	USPAT; UPAD	OR	ON	2013/12/09 17:54
S6	2646	S5 and (error threshold bias limit$3)	USPAT; UPAD	OR	ON	2013/12/09 17:55
S7	499	S6 and (ddc display$3 near2 (data channel))	USPAT; UPAD	OR	ON	2013/12/09 17:55
S8	536	S6 and (ddc display$3 near2 (data channel) vesa svga hdmi displayport)	USPAT; UPAD	OR	ON	2013/12/09 17:56
S9	536	S6 and (ddc display$3 near2 (data channel) vesa svga hdmi displayport display adj port)	USPAT; UPAD	OR	ON	2013/12/09 17:56
S10	147	S9 and (hpd hot near2 (plug$4 detect$3 swap$4) (chang$3 configu$5 repair$3) near5 (interrupt$3 servic$3 disrupt$3))	USPAT; UPAD	OR	ON	2013/12/09 17:58
S11	19	"Term Removed"	USPAT	OR	OFF	2013/12/09 18:47
S12	10	("5276458" | "20070055876" | "20080152023" | "7729874" | "7860398" | "20040143847" | "20070222779" | "7979590" | "20060092152" | "20070036158" | "20070165997" | "20050141851" | "20050182876" | "20070186015" | "20070283071" | "7176980" | "7873980" | "7539808" | "20060206734" | "20070070402" | "20040125886" | "20020060676" | "20080134237" | "20070280646" | "20090177818" | "20090178086" | "20100283894" | "7856520" | "20050225547" | "20070047638" | "20070220150" | "20070242062" | "5943029" | "20050116884" | "20050228995" | "20060280055" | "20070236605" | "7079129").PN.	USPAT; UPAD	OR	ON	2013/12/09 18:48
S13	10	S12 not S11	USPAT; UPAD	OR	ON	2013/12/09 18:49
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S15	1973	S14 and (voltage vss vcc power power near2 supply).clm.	USPAT; UPAD	OR	ON	2013/12/09 20:38
S16	317	S15 and (error threshold bias limit$3).clm.	USPAT; UPAD	OR	ON	2013/12/09 20:38
S17	27	S16 and (ddc display$3 near2 (data channel)).clm.	USPAT; UPAD	OR	ON	2013/12/09 20:38
S18	27	S16 and (ddc display$3 near2 (data channel) vesa svga hdmi displayport display adj port).clm.	USPAT; UPAD	OR	ON	2013/12/09 20:39
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S23	20	"Term Removed"	USPAT	OR	OFF	2013/12/20 21:15

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DELL/HP/LENOVO EXHIBIT 1002

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13434273	MAXWELL ET AL.
	Examiner	Art Unit
	CHRISTOPHER BARTELS	2184

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner
(G09G5, H04N, G06F, H04L, G08C and relevant sub-groups) text search in EAST	07/02/2014-07/03/2014	C.A.B.

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Text search in EAST (ALL DATABASES)	12/09/13, 12/20/13, 7/2/14	C.A.B.
710/15, 1 AND (713 714) text search in East	12/09/2013	C.A.B.
Inventor Search performed (USPAT, UPAD)	12/09/2013	C.A.B.

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/C.B./ Examiner.Art Unit 2184	

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13434273	MAXWELL ET AL.
	Examiner	Art Unit
	CHRISTOPHER BARTELS	2184

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/05/2014								
	1	✓								
	2	✓								
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	19	✓								
	20	✓								

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	75	("5276458" | "20070055876" | "20080152023" | "7729874" | "7860398" | "20040143847" | "20070222779" | "7979590" | "20060092152" | "20070036158" | "20070165997" | "20050141851" | "20050182876" | "20070186015" | "20070283071" | "7176980" | "7873980" | "7539808" | "20060206734" | "20070070402" | "20040125886" | "20020060676" | "20080134237" | "20070280646" | "20090177818" | "20090178086" | "20100283894" | "7856520" | "20050225547" | "20070047638" | "20070220150" | "20070242062" | "5943029" | "20050116884" | "20050228995" | "20060280055" | "20070236605" | "7079129").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/12/09 18:48
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S20	40	(US-6618773-$ or US-7761709-$ or US-7899941-$ or US-8462843-$ or US-8375147-$ or US-8510483-$ or US-8453008-$ or US-7827319-$ or US-8266335-$ or US-7523241-$ or US-7979910-$ or US-7962663-$ or US-6738856-$ or US-7124326-$ or US-8244925-$ or US-8356121-$ or US-8199258-$ or US-8447158-$ or US-7889201-$ or US-7995043-$).did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/12/20 21:16
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S25	10	(US-8375147-$ or US-7827319-$ or US-8266335-$ or US-6738856-$ or US-7124326-$).did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2014/07/02 17:49

			IBM_TDB			
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S27	40	(US-6618773-$ or US-7761709-$ or US-7899941-$ or US-8462843-$ or US-8375147-$ or US-8510483-$ or US-8453008-$ or US-7827319-$ or US-8266335-$ or US-7523241-$ or US-7979910-$ or US-7962663-$ or US-6738856-$ or US-7124326-$ or US-8244925-$ or US-8356121-$ or US-8199258-$ or US-8447158-$ or US-7889201-$ or US-7995043-$).did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/07/02 17:49
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S30	1365	S29 and (mobile near4 (hd high adj definition link))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2014/07/02 17:51

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S32	131	S29 and (mobile near4 (hd high adj definition link)) with (mode select$3 switch$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/07/02 17:52
S33	49	S31 not S32	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/07/02 17:52
S36	317149	((G09G5/006 OR G09G2370/047 OR G09G2370/12 OR G09G2330/022 OR G09G2370/042 OR G09G5/001 OR G09G2330/021 OR G09G2370/045 OR G09G5/363 OR G09G2310/0267 OR G09G2310/0275 OR G09G2330/02 OR G09G2350/00 OR G09G2360/125 OR G09G2370/04 OR G09G2370/06 OR G09G3/2096 OR G09G5/12 OR H04N5/775 OR H04N21/43632 OR H04N5/765 OR H04N21/43635 OR H04N21/4367 OR H04N5/85 OR H04N21/2541 OR H04N21/4122 OR H04N21/43622 OR H04N21/43637 OR H04N21/4627 OR H04N21/835 OR H04N5/232 OR H04N5/38 OR H04N5/77 OR H04N5/913 OR H04N7/183 OR H04N7/50 OR H04N17/002 OR H04N2005/4433 OR H04N21/25816 OR H04N21/4113 OR H04N21/4143 OR H04N21/42206 OR H04N21/436 OR H04N21/43615 OR H04N21/44227 OR H04N21/4436 OR H04N5/268 OR H04N5/4403 OR H04N5/44513 OR H04N5/44582 OR H04N5/44591 OR H04N5/63 OR H04N5/76 OR H04N5/781 OR G06F13/4081 OR G06F13/1605 OR G06F13/387 OR G06F13/4291 OR G06F1/3203 OR G06F1/3265 OR G06F3/033 OR G06F3/03543 OR G06F3/038 OR G06F3/14 OR H04L63/08 OR H04L2463/101 OR H04L2209/08 OR H04L2209/60 OR H04L9/3271 OR G08C17/02 OR G08C2201/30 OR G08C2201/41 OR G08C2201/50).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/07/03 15:41
S37	180	S36 and (mobile near4 (hd high adj definition link)) with (mode select$3 switch$3 hdmi sda sclk)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2014/07/03 15:41

DELL/HP/LENOVO EXHIBIT 1002
Page 381

			DERWENT; IBM_TDB			
S38	131	S36 and (mobile near4 (hd high adj definition link)) with (mode select$3 switch$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/07/03 15:41
S39	49	S37 not S38	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/07/03 15:41
S40	1	S39 and rsen	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/03 15:41
S41	1	S39 and (rsen receiver near4 (sense adj input))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/03 15:41
S42	10	S39 and (rsen receiver near4 (sense input))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/03 15:42

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S3	104117	(710/15,1).ccls. ("713" "714").clas.	USPAT; UPAD	OR	ON	2013/12/09 17:27
S4	4364	S3 and (extend$3 near4 (display$3 identif$7 data) edid)	USPAT; UPAD	OR	ON	2013/12/09 17:54
S5	2751	S4 and (voltage vss vcc power power near2 supply)	USPAT; UPAD	OR	ON	2013/12/09 17:54
S6	2646	S5 and (error threshold bias limit$3)	USPAT; UPAD	OR	ON	2013/12/09 17:55
S7	499	S6 and (ddc display$3 near2 (data channel))	USPAT; UPAD	OR	ON	2013/12/09 17:55
S8	536	S6 and (ddc display$3 near2 (data channel) vesa svga hdmi displayport)	USPAT; UPAD	OR	ON	2013/12/09 17:56
S9	536	S6 and (ddc display$3 near2 (data channel) vesa svga hdmi displayport display adj port)	USPAT; UPAD	OR	ON	2013/12/09 17:56
S10	147	S9 and (hpd hot near2 (plug$4 detect$3 swap$4) (chang$3 configu$5 repair$3) near5 (interrupt$3 servic$3 disrupt$3))	USPAT; UPAD	OR	ON	2013/12/09 17:58

S11	19	"Term Removed"	USPAT	OR	OFF	2013/12/09 18:47
S12	10	("5276458" | "20070055876" | "20080152023" | "7729874" | "7860398" | "20040143847" | "20070222779" | "7979590" | "20060092152" | "20070036158" | "20070165997" | "20050141851" | "20050182876" | "20070186015" | "20070283071" | "7176980" | "7873980" | "7539808" | "20060206734" | "20070070402" | "20040125886" | "20020060676" | "20080134237" | "20070280646" | "20090177818" | "20090178086" | "20100283894" | "7856520" | "20050225547" | "20070047638" | "20070220150" | "20070242062" | "5943029" | "20050116884" | "20050228995" | "20060280055" | "20070236605" | "7079129").PN.	USPAT; UPAD	OR	ON	2013/12/09 18:48
S13	10	S12 not S11	USPAT; UPAD	OR	ON	2013/12/09 18:49
S14	12467	((extend$3 near4 (display$3 identif$7 data) edid)).clm.	USPAT; UPAD	OR	ON	2013/12/09 20:37
S15	1973	S14 and (voltage vss vcc power power near2 supply).clm.	USPAT; UPAD	OR	ON	2013/12/09 20:38
S16	317	S15 and (error threshold bias limit$3).clm.	USPAT; UPAD	OR	ON	2013/12/09 20:38
S17	27	S16 and (ddc display$3 near2 (data channel)).clm.	USPAT; UPAD	OR	ON	2013/12/09 20:38
S18	27	S16 and (ddc display$3 near2 (data channel) vesa svga hdmi displayport display adj port).clm.	USPAT; UPAD	OR	ON	2013/12/09 20:39
S19	1	S18 and (hpd hot near2 (plug$4 detect$3 swap$4) (chang$3 configu$5 repair$3) near5 (interrupt$3 servic$3 disrupt$3)).clm.	USPAT; UPAD	OR	ON	2013/12/09 20:39
S22	20	"Term Removed"	USPAT	OR	OFF	2013/12/20 21:15
S23	20	"Term Removed"	USPAT	OR	OFF	2013/12/20 21:15
S34	15	"Term Removed"	USPAT	OR	OFF	2014/07/02 17:49
S35	15	"Term Removed"	USPAT	OR	OFF	2014/07/02 17:49

9/5/2014 3:19:04 PM
C:\Users\cbartels\Documents\EAST\Workspaces\13434273InventClassIDS.wsp

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/434,273	03/29/2012	Conrad Arlo Maxwell	8029P107

CONFIRMATION NO. 7248

120363
Silicon Image/FENWICK
801 California Street
Mountain View, CA 94041

POA ACCEPTANCE LETTER

OC0000000066281102

Date Mailed: 02/10/2014

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/22/2014.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/hchristian/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/434,273	03/29/2012	Conrad Arlo Maxwell	8029P107

CONFIRMATION NO. 7248

POWER OF ATTORNEY NOTICE

65702
SILICON IMAGE/BSTZ
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

OC000000066281070

Date Mailed: 02/10/2014

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/22/2014.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/hchristian/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PTO/AIA/80 (07-12)
Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☒ Practitioners associated with Customer Number: 120363

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☒ The address associated with Customer Number: 120363

OR

☐	Firm or Individual Name		
	Address		
	City	State	Zip
	Country		
	Telephone	Email	

Assignee Name and Address: Silicon Image, Inc.
1140 East Arques Avenue
Sunnyvale, CA 94085

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record
The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	January 13, 2014
Name	Edward Lopez	Telephone	408-616-4173
Title	Chief Legal Officer		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
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U.S. Patent and Trademark Office;U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Conrad Arlo Maxwell, Lance Davies, Graeme P. Jones, Glenn L. Marks et al

Application No./Patent No.: 13/434,273 Filed/Issue Date: 03/29/2012

Titled: METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE

Silicon Image, Inc., a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 028547, Frame 0958, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

   2. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by37 CFR3.73(b). The information is required toobtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentialityis governed by35 U.S.C. 122and 37 CFR1.11 and1.14. Thiscollection is estimated to take 12 minutes to complete, including gathering, preparing, and submittingthe completed application form to the USPTO.Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent tothe Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.**SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

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6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

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☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Dohyun Ahn/	Jan. 22, 2014
Signature	Date
Dohyun Ahn	63,237
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that yoube given certain informationin connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, pleasebe advised that: (1) the general authority forthe collection of thisinformation is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and(3) the principal purpose forwhich the information isused by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent applicationor patent. If you do not furnish the requested information,the U.S. Patent and Trademark Office may not be able to process and/or examineyour submission,which may result in termination of proceedings or abandonment of the applicationor expiration of the patent.

The informationprovided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the informationin order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an InternationalApplication filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, arecord may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from thissystem of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	17997490
Application Number:	13434273
International Application Number:	
Confirmation Number:	7248
Title of Invention:	METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE
First Named Inventor/Applicant Name:	Conrad Arlo Maxwell
Customer Number:	65702
Filer:	Dohyun Ahn/Sarah Glenn
Filer Authorized By:	Dohyun Ahn
Attorney Docket Number:	8029P107
Receipt Date:	22-JAN-2014
Filing Date:	29-MAR-2012
Time Stamp:	20:21:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	SIMG_Executed_POA_80.pdf	244840 f27f330bae48eee8fdcb4211f95b335b3b230cdc	no	1

Warnings:	
Information:	

2	Assignee showing of ownership per 37 CFR 3.73.	25622_Stmt_3_73.pdf	120668 8909045ace38cfc3acaeb2b4dbc37d18c6f77bb7	no	3

Warnings:	
Information:	
Total Files Size (in bytes):	365508

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	13/434,273
	Filing Date	March 29, 2012
	First Named Inventor	Maxwell, Conrad
	Group Art Unit	2184
	Examiner Name	Bartels, Christopher A.
Sheet 1 of 1	Attorney Docket No: 8029P107	

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**
		US-20080205306	08/28/2008	Saito, T.	
		US-20080270635	10/30/2008	Nakahama, M.	
		US-20090083825	03/26/2009	Miller, R. D., et al.	
		US-20100131782	05/27/2010	Higuchi, S.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	**Cite No [1]**	**Foreign Patent Document** Country Code/Number/Kind Code (if known)	**Publication Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	**T [2]**

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T [2]**
		"International Search Report and Written Opinion of the International Searching Authority, for International Patent Application No. PCT/US2012/031463 (Attorney Docket No. 8029P107PCT)", (October 31, 2012), Whole Document	
		"Preliminary Report on Patentability (Chapter I of the Patent Cooperation Treaty), for International Patent Application No. PCT/US2012/031463 (Attorney Docket No. 8029P107PCT)", (October 10, 2013), Whole Document	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
8029P107PCT		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2012/031463	**30 MARCH 2012 (30.03.2012)**	31 MARCH 2011 (31.03.2011)

Applicant

SILICON IMAGE, INC. et al

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed
      ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (See Box No. II)
3. ☐ **Unity of invention is lacking** (See Box No. III)
4. With regard to the **title,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:
5. With regard to the **abstract,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. With regard to the drawings,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 1
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figure is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/031463

A. CLASSIFICATION OF SUBJECT MATTER

H04L 29/10(2006.01)i, H04L 29/12(2006.01)i, H04L 12/10(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04L 29/10; G06F 1/28; H04N 7/16; G06F 3/00; H04L 5/16

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: Audio/video, AV, source, sink, transition, mode, and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008-0205306 A1 (T. SAITO) 28 August 2008 See abstract; figures 1, 3; paragraphs [0032]-[0034], [0042], [0046].	1-20
A	US 2009-0083825 A1 (R. D. MILLER et al.) 26 March 2009 See abstract; figure 1; paragraphs [0023], [0024]; claim 1.	1-20
A	US 2008-0270635 A1 (M. NAKAHAMA) 30 October 2008 See abstract; figure 1; paragraphs [0040], [0042]; claim 1.	1-20
A	US 2010-0131782 A1 (S. HIGUCHI) 27 May 2010 See abstract; figure 1; paragraphs [0053], [0054].	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 OCTOBER 2012 (31.10.2012)	**31 OCTOBER 2012 (31.10.2012)**

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

Kim Sun Jong

Telephone No. 82-42-481-8260

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2012/031463

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008-0205306 A1	28.08.2008	JP 04-343967 B2	17.07.2009
		JP 2008-219157 A	18.09.2008
		JP 4343967 B2	14.10.2009
		US 7626954 B2	01.12.2009
US 2009-0083825 A1	26.03.2009	US 8203325 B2	19.06.2012
		WO 2009-032333 A1	12.03.2009
US 2008-0270635 A1	30.10.2008	BR PI0801191A2	09.12.2008
		CN 101296073 A	29.10.2008
		CN 101296073 B	04.01.2012
		CN 101296073 C0	29.10.2008
		EP 1988541 A2	05.11.2008
		EP 1988541 A3	14.04.2010
		JP 05-029121 B2	06.07.2012
		JP 2008-271460 A	06.11.2008
		KR 10-2008-0095771 A	29.10.2008
		RU 2008116377 A	27.10.2009
		RU 2384961 C2	20.03.2010
		TW 200904174 A	16.01.2009
		US 8190786 B2	29.05.2012
US 2010-0131782 A1	27.05.2010	CN 101742203 A	16.06.2010
		EP 2190193 A2	26.05.2010
		EP 2190193 A3	12.09.2012
		JP 04-735709 B2	13.05.2011
		JP 2010-130068 A	10.06.2010
		JP 4735709 B2	27.07.2011

DELL/HP/LENOVO EXHIBIT 1002
Page 395

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
VINCENT LESTER J.

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP 1279
OAKMEAD PARKWAY SNNYVALE CA 94085-4040 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**31 OCTOBER 2012 (31.10.2012)**
Applicant's or agent's file reference 8029P107PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2012/031463	**30 MARCH 2012 (30.03.2012)**	31 MARCH 2011 (31.03.2011)

International Patent Classification (IPC) or both national classification and IPC

H04L 29/10(2006.01)i, H04L 29/12(2006.01)i, H04L 12/10(2006.01)i

Applicant

SILICON IMAGE, INC. et al

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. 82-42-472-7140	31 OCTOBER 2012 (31.10.2012)	Kim Sun Jong Telephone No.82-42-481-8260

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2012/031463

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of :

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____ , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. a sequence listing filed or furnished
      ☐ on paper
      ☐ in electronic form

   b. time of filing or furnishing
      ☐ contained in the international application as filed.
      ☐ filed together with the international application in electronic form.
      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additioanl copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

DELL/HP/LENOVO EXHIBIT 1002
Page 397

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2012/031463

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-20	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-20	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 2008-0205306 A1 (T. SAITO) 28 August 2008
D2: US 2009-0083825 A1 (R. D. MILLER et al.) 26 March 2009
D3: US 2008-0270635 A1 (M. NAKAHAMA) 30 October 2008
D4: US 2010-0131782 A1 (S. HIGUCHI) 27 May 2010

1. Novelty and Inventive step

1.1 Regarding independent claim 1, document D1 which is considered to represent the most relevant state of the art discloses (the references in parentheses applying to this document):

A method at an audio/video (AV) device, the method comprising:
- detecting with control circuitry an indication of one of a power up event at the AV device, a power down event at the AV device, or a reset event at the AV device(paragraph [0042]; *receiving a switch request for switching the transmission direction*)
- in response to the indication, automatically initializing communication logic of the AV device with the control circuitry, wherein an AV sink operation mode of the communication logic is for the communication logic to receive AV data provided to the device via a connector, the AV sink operation mode further for the communication logic to receive power of a first supply voltage provided to the device at a channel of the connector, wherein an AV source operation mode of the communication logic is for the communication logic to send AV data from the device via the connector, the AV source operation mode further for the communication logic to provide a second supply voltage at the channel of the connector(paragraph [0046]; *switches the transmission direction of the data communication unit from the sending side to the receiving side*), and
- wherein automatically initializing the communication logic includes placing the communication logic into a default operation mode which prevents the second supply voltage from being provided by the communication logic at the channel of the connector.

The subject matter of claim 1 differs from that of D1 in that D1 does not explicitly disclose a feature of placing the communication logic into a default operation mode which prevents the second supply volage from being provided by the communication logic at the channel of the connector. However, this difference would not have been obvious to a person skilled in the art at the time the application of the invention was filed. Therefore, the subject matter of claim 1 meets the requirements of PCT Article 33(2) and 33(3) with respect to novelty and inventive step.

Continued on Supplemental Box

DELL/HP/LENOVO EXHIBIT 1002
Page 398

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:

Box V

1.2 The features of device claim 9 and system claim 15 essentially correspond to method claim 1 except for the different claimed categories. Therefore, the subject matter of claims 9 and 15 meets the requirements of PCT Article 33(2) and 33(3) with respect to novelty and inventive step for the same reasoning as given for claim 1.

1.3 Claims 2-8 are dependent on claim 1 and therefore meet the requirements of PCT Article 33(2) and 33(3).

1.4 Claims 10-14 are dependent on claim 9 and therefore meet the requirements of PCT Article 33(2) and 33(3).

1.5 Claims 16-20 are dependent on claim 15 and therefore meet the requirements of PCT Article 33(2) and 33(3).

2. Industrial Applicability

Claims 1-20 have industrial applicability and meet the requirement of PCT Article 33(4).

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY
(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44*bis*)

Applicant's or agent's file reference 8029P107PCT	FOR FURTHER ACTION	See item 4 below
International application No. PCT/US2012/031463	International filing date *(day/month/year)* 30 March 2012 (30.03.2012)	Priority date *(day/month/year)* 31 March 2011 (31.03.2011)
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant SILICON IMAGE, INC.		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 *bis*.1(a).

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44*bis*.3(c) and 93*bis*.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44*bis* .2).

	Date of issuance of this report 01 October 2013 (01.10.2013)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland	Authorized officer Simin Baharlou
Facsimile No. +41 22 338 82 70	e-mail: pt09.pct@wipo.int

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
VINCENT LESTER J.

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP 1279
OAKMEAD PARKWAY SNNYVALE CA 94085-4040 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	31 OCTOBER 2012 (31.10.2012)
Applicant's or agent's file reference 8029P107PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2012/031463	**30 MARCH 2012 (30.03.2012)**	31 MARCH 2011 (31.03.2011)

International Patent Classification (IPC) or both national classification and IPC

H04L 29/10(2006.01)i, H04L 29/12(2006.01)i, H04L 12/10(2006.01)i

Applicant

SILICON IMAGE, INC. et al

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. 82-42-472-7140	31 OCTOBER 2012 (31.10.2012)	Kim Sun Jong Telephone No.82-42-481-8260

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2012/031463

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. a sequence listing filed or furnished
      ☐ on paper
      ☐ in electronic form

   b. time of filing or furnishing
      ☐ contained in the international application as filed.
      ☐ filed together with the international application in electronic form.
      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2012/031463

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-20	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-20	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 2008-0205306 A1 (T. SAITO) 28 August 2008
D2: US 2009-0083825 A1 (R. D. MILLER et al.) 26 March 2009
D3: US 2008-0270635 A1 (M. NAKAHAMA) 30 October 2008
D4: US 2010-0131782 A1 (S. HIGUCHI) 27 May 2010

1. Novelty and Inventive step

1.1 Regarding independent claim 1, document D1 which is considered to represent the most relevant state of the art discloses (the references in parentheses applying to this document):

A method at an audio/video (AV) device, the method comprising:
- detecting with control circuitry an indication of one of a power up event at the AV device, a power down event at the AV device, or a reset event at the AV device(paragraph [0012]: *receiving a switch request for switching the transmission direction*)
- in response to the indication, automatically initializing communication logic of the AV device with the control circuitry, wherein an AV sink operation mode of the communication logic is for the communication logic to receive AV data provided to the device via a connector, the AV sink operation mode further for the communication logic to receive power of a first supply voltage provided to the device at a channel of the connector, wherein an AV source operation mode of the communication logic is for the communication logic to send AV data from the device via the connector, the AV source operation mode further for the communication logic to provide a second supply voltage at the channel of the connector(paragraph [0046]: *switches the transmission direction of the data communication unit from the sending side to the receiving side*), and
- wherein automatically initializing the communication logic includes placing the communication logic into a default operation mode which prevents the second supply voltage from being provided by the communication logic at the channel of the connector.

The subject matter of claim 1 differs from that of D1 in that D1 does not explicitly disclose a feature of placing the communication logic into a default operation mode which prevents the second supply voltage from being provided by the communication logic at the channel of the connector. However, this difference would not have been obvious to a person skilled in the art at the time the application of the invention was filed. Therefore, the subject matter of claim 1 meets the requirements of PCT Article 33(2) and 33(3) with respect to novelty and inventive step.

Continued on Supplemental Box

DELL/HP/LENOVO EXHIBIT 1002
Page 403

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:

Box V

1.2 The features of device claim 9 and system claim 15 essentially correspond to method claim 1 except for the different claimed categories. Therefore, the subject matter of claims 9 and 15 meets the requirements of PCT Article 33(2) and 33(3) with respect to novelty and inventive step for the same reasoning as given for claim 1.

1.3 Claims 2-8 are dependent on claim 1 and therefore meet the requirements of PCT Article 33(2) and 33(3).

1.4 Claims 10-14 are dependent on claim 9 and therefore meet the requirements of PCT Article 33(2) and 33(3).

1.5 Claims 16-20 are dependent on claim 15 and therefore meet the requirements of PCT Article 33(2) and 33(3).

2. Industrial Applicability

Claims 1-20 have industrial applicability and meet the requirement of PCT Article 33(4).

DELL/HP/LENOVO EXHIBIT 1002
Page 404

Electronic Acknowledgement Receipt

EFS ID:	17606396
Application Number:	13434273
International Application Number:	
Confirmation Number:	7248
Title of Invention:	METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE
First Named Inventor/Applicant Name:	Conrad Arlo Maxwell
Customer Number:	65702
Filer:	Dermot G. Miller/Julie Dussault
Filer Authorized By:	Dermot G. Miller
Attorney Docket Number:	8029P107
Receipt Date:	09-DEC-2013
Filing Date:	29-MAR-2012
Time Stamp:	19:12:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		8029P107_IDS_12-9-13.pdf	221950 e8e893bfa7339b80138b94836e7c47c2fe34e071	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	1
	Information Disclosure Statement (IDS) Form (SB08)	2	2

Warnings:					
Information:					
2	Foreign Reference	8029P107PCT_ISRWO_103112.pdf	1215709 ea0cff16195ed3149376e905c88bbd210b6ebbc6	no	7
Warnings:					
Information:					
3	Foreign Reference	8029P107PCT_IPRP_101013.pdf	1452441 736d7ba409611f2e4502dbcc11de4f58d408fa64	no	5
Warnings:					
Information:					
		Total Files Size (in bytes):	2890100		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	13/434,273
Filing Date	March 29, 2012
First Inventor	Conrad Arlo Maxwell, et al.
Art Unit	2184
Examiner Name	Bartels, Christopher A.
Attorney Docket No.	8029P107 Conf. No. 7248

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of a first Office Action on the merits. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The references listed were cited in a Search Report dated October 31, 2012 (copy enclosed herewith and, if not in the English language, a cover sheet with English language translation is attached).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☐ The IDS Filing Fee in the amount of $180.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 02-2666.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Dermot G. Miller/	Date (MM-DD-YYYY)	12-09-2013
Name/Print	Dermot G. Miller	Registration Number	58309

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Julie Dussault /Julie Dussault/ *Date* *12-09-13*

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/434,273	03/29/2012	Conrad Arlo Maxwell	8029P107

CONFIRMATION NO. 7248

65702
SILICON IMAGE/BSTZ
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

PUBLICATION NOTICE

OC000000057383414

Title:METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE

Publication No.US-2012-0274857-A1
Publication Date:11/01/2012

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/434,273	03/29/2012	2852	1380	8029P107	20	3

CONFIRMATION NO. 7248

UPDATED FILING RECEIPT

65702
SILICON IMAGE/BSTZ
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

OC000000055494547

Date Mailed: 07/20/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Conrad Arlo Maxwell, Herriman, UT;
Lance Davies, Loveland, CO;
Graeme P. Jones, Tampa, FL;
Glenn L. Marks, Corona, CA;
Jonathan Regalado-Hawkey, Woolston, UNITED KINGDOM;
Christian Rudel, Wunstork, GERMANY;

Power of Attorney: The patent practitioners associated with Customer Number 65702

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/470,431 03/31/2011

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 04/09/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/434,273**

Projected Publication Date: 11/01/2012

Non-Publication Request: No

Early Publication Request: No

Title

METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE

Preliminary Class

396

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

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No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/434,273

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 60 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 250 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1250

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

Electronic Acknowledgement Receipt

EFS ID:	13251820
Application Number:	13434273
International Application Number:	
Confirmation Number:	7248
Title of Invention:	METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE
First Named Inventor/Applicant Name:	Conrad Arlo Maxwell
Correspondence Address:	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP - 1279 OAKMEAD PARKWAY - SUNNYVALE CA 94085-4040 US 4087208300 -
Filer:	Dermot G. Miller/Julie Dussault
Filer Authorized By:	Dermot G. Miller
Attorney Docket Number:	8029P107
Receipt Date:	13-JUL-2012
Filing Date:	29-MAR-2012
Time Stamp:	18:40:15
Application Type:	Utility under 35 USC 111(a)

07/19/2012 VVAN11 00000019 022666 13434273
01 FC:1051 130.00 DA

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$560

RAM confirmation Number	5654
Deposit Account	022666
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	8029P107_SIMG0383_DecPoa_signed.pdf	1325034 f76f0dba4edfd59d20eba3e9317c4161e913583a	no	5
Warnings:					
Information:					
2	Applicant Response to Pre-Exam Formalities Notice	8029P107_Resp_MP_071312.pdf	30407 f1ef6659262225 40cb021fe8960fea0d5b816af3	no	1
Warnings:					
Information:					
3	Extension of Time	8029P107_EOT_071312.pdf	32226 74bcae4c555e6ca5073d933787184921f243e304	no	1
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30944 39ef02ef2266997487c63694e2b0ae535fcdc807	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1418611		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

ATTORNEY DOCKET NO.: 8029P107

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

CONRAD ARLO MAXWELL, ET AL.

Application No.: 13/434,273

Filed: March 29, 2012

For: **METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE**

Art Group: 2852

Examiner: TBD

Confirmation No.: 7248

Mail Stop Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

Sir:

In response to the Notice to File Missing Parts of Nonprovisional Application mailed April 12, 2012, please find enclosed:

- a duly executed Declaration and Power of Attorney with payment in the amount of $130.00 for the surcharge of 37 CFR § 1.16(f);
- a Petition for Extension of Time and payment in the amount of $560.00;

If any additional fee is required, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: July 13, 2012

/Dermot G. Miller/

Dermot G. Miller, Reg. No. 58309

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
Telephone: (503) 439-8778

/Julie Dussault/ 07/13/12

Julie Dussault ***Date***

Docket No.: 8029P107

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

CONRAD ARLO MAXWELL, ET AL.

Art Group: 2852

Application No.: 13/434,273

Examiner: TBD

Filed: March 29, 2012

For: **METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE**

PETITION FOR EXTENSION OF TIME PURSUANT TO 37 C.F.R. § 1.136(a)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F. R. §1.136(a), Applicants for the above-identified application respectfully Petition the Commissioner for a two (2) month extension of time, extending the period for response to August 12, 2012, from the Notice to File Missing Parts of NonProvisional Application dated April 12, 2012. The petition filing fee of $560.00 and a Response to Notice to File Missing Parts of Nonprovisional Application are attached. (If a check is not attached, you are hereby authorized to charge deposit account no. 02-2666.)

If it should be determined that a longer extension of time is required to prevent this application from being abandoned, please charge any additional fees to Deposit Account No. 02-2666.

Respectfully submitted,

Blakely, Sokoloff, Taylor & Zafman LLP

Date: July 13, 2012

/Dermot G. Miller/

Dermot G. Miller, Reg. No. 58309

CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

/Julie Dussault/ *07-13-12*

Julie Dussault ***Date***

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
Telephone: (503) 439-8778

Electronic Patent Application Fee Transmittal

Application Number:	13434273
Filing Date:	29-Mar-2012
Title of Invention:	METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE
First Named Inventor/Applicant Name:	Conrad Arlo Maxwell
Filer:	Dermot G. Miller/Julie Dussault
Attorney Docket Number:	8029P107

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 2 months with $0 paid	1252	1	560	560

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**560**

Electronic Acknowledgement Receipt	
EFS ID:	13251820
Application Number:	13434273
International Application Number:	
Confirmation Number:	7248
Title of Invention:	METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE
First Named Inventor/Applicant Name:	Conrad Arlo Maxwell
Correspondence Address:	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP - 1279 OAKMEAD PARKWAY - SUNNYVALE CA 94085-4040 US 4087208300 -
Filer:	Dermot G. Miller/Julie Dussault
Filer Authorized By:	Dermot G. Miller
Attorney Docket Number:	8029P107
Receipt Date:	13-JUL-2012
Filing Date:	29-MAR-2012
Time Stamp:	18:40:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$560

RAM confirmation Number	5654
Deposit Account	022666
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	8029P107_SIMG0383_DecPoa_signed.pdf	1325034 f76f0dba4edfd59d20eba3e9317c4161e913583a	no	5
Warnings:					
Information:					
2	Applicant Response to Pre-Exam Formalities Notice	8029P107_Resp_MP_071312.pdf	30407 f1ef665926222540cb021fe8960fea0d5b816af3	no	1
Warnings:					
Information:					
3	Extension of Time	8029P107_EOT_071312.pdf	32226 74bcae4c555e6ca5073d93378718492f1243e304	no	1
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30944 39ef02ef2266997487c63694e2b0ae535fcdc807	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1418611		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (37 CFR 1.63)		Attorney Docket Number	8029P107
☐ Declaration Submitted with Initial Filing OR ☒ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16(e)) required)		First Named Inventor	Conrad Arlo Maxwell
		COMPLETE IF KNOWN	
		Application Number	13/434,273
		Filing Date	March 29, 2012
		Art Unit	TBD
		Examiner Name	TBD

I hereby declare that: (1) Each inventor's residence, mailing address, and citizenship are as stated below next to their name; and (2) I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE

(Title of the Invention)

the specification of which

☐ is attached hereto.

OR

☒ was filed on (MM/DD/YYYY)

03/29/2012 as United States Application Number 13/434,273

or

_____ PCT International Application Number _____

and was amended on (MM/DD/YYYY) _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment specifically referred to above.

I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application. I do not know and do not believe that the claimed invention was in public use or on sale in the United States of America more than one year prior to this application, nor do I know or believe that the invention has been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

DELL/HP/LENOVO EXHIBIT 1002
Page 423

Authorization To Permit Access to Application by Participating Offices

☒ If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), and any other intellectual property offices in which a foreign application claiming priority to the above-identified application is filed access to the above-identified patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, or other intellectual property office in which a foreign application claiming priority to the above-identified application is filed to have access to the application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the application-as-filed with respect to: (1) the above-identified application, (2) any foreign application to which the above-identified application claims priority under 35 USC 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the above-identified US application, and (3) any U.S. application from which benefit is sought in the above-identified application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing the Authorization to Permit Access to Application by Participating Offices.

Claim of Foreign Priority Benefits

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s):

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?
			☐	☐ Yes ☐ No
			☐	☐ Yes ☐ No
			☐	☐ Yes ☐ No
			☐	☐ Yes ☐ No
			☐	☐ Yes ☐ No

Appointment of Practitioners:

I hereby appoint the practitioners associated with Customer Number: 65702 as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected herewith.

If this patent application is assigned, then the undersigned hereby authorizes the patent attorneys and patent agents named herein to accept and follow instructions from the assignee(s) as to any action to be taken in the United States Patent and Trademark Office regarding this application without direct communication between the patent attorneys and patent agents and the undersigned. In the event of a change in the persons from whom instructions may be taken, at least one patent attorney or patent agent named herein will be so notified by the undersigned.

Correspondence:

Direct all correspondence to Customer Number 65702.

DELL/HP/LENOVO EXHIBIT 1002
Page 424

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioner/applicant should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available. Petitioner/applicant is advised that documents which form the record of a patent application (such as the PTO/SB/01) are placed into the Privacy Act system of records DEPARTMENT OF COMMERCE, COMMERCE-PAT-7, System name: *Patent Application Files*. Documents not retained in an application file (such as the PTO-2038) are placed into the Privacy Act system of COMMERCE/PAT-TM-10, System name: *Deposit Accounts and Electronic Funds Transfer Profiles*.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

NAME OF SOLE OR FIRST INVENTOR: ☐ A petition has been filed for this unsigned inventor

Full Name: Conrad Arlo Maxwell
(First, Middle [if any], Family Name (or Surname), and Suffix [if any])

Inventor's Signature Conrad Arlo Maxwell Date 5/22/12

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DELL/HP/LENOVO EXHIBIT 1002
Page 425

NAME OF SECOND INVENTOR: ☐ A petition has been filed for this unsigned inventor

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NAME OF FOURTH INVENTOR: ☐ A petition has been filed for this unsigned inventor

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Inventor's Signature _____ Date 6/1/12

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Inventor's Signature _____ Date 6/25/2012

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DELL/HP/LENOVO EXHIBIT 1002
Page 426

NAME OF SIXTH INVENTOR: ☐ A petition has been filed for this unsigned inventor

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Inventor's Signature C. Rudel Date 6/19/12

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NAME OF SEVENTH INVENTOR: ☐ A petition has been filed for this unsigned inventor

Full Name:
(First, Middle [if any], Family Name (or Surname), and Suffix [if any])

Inventor's Signature Date

Residence Citizenship
(City, State, Country) *(Country)*

Mailing Address

NAME OF EIGHTH INVENTOR: ☐ A petition has been filed for this unsigned inventor

Full Name:
(First, Middle [if any], Family Name (or Surname), and Suffix [if any])

Inventor's Signature Date

Residence Citizenship
(City, State, Country) *(Country)*

Mailing Address

NAME OF NINTH INVENTOR: ☐ A petition has been filed for this unsigned inventor

Full Name:
(First, Middle [if any], Family Name (or Surname), and Suffix [if any])

Inventor's Signature Date

Residence Citizenship
(City, State, Country) *(Country)*

Mailing Address

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Page 427

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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/434,273	03/29/2012	Conrad Arlo Maxwell	8029P107

CONFIRMATION NO. 7248

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

FORMALITIES LETTER

OC000000053631506

Date Mailed: 04/12/2012

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- A surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of $**130** for a non-small entity, must be submitted.

SUMMARY OF FEES DUE:

Total fee(s) required within **TWO MONTHS** from the date of this Notice is $**130** for a non-small entity
- $**130** Surcharge.

Replies should be mailed to:

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/masfaw/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/434,273

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 60 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 250 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1250

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/434,273	03/29/2012	2852	1250	8029P107	20	3

CONFIRMATION NO. 7248

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

FILING RECEIPT

OC000000053631505

Date Mailed: 04/12/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Conrad Arlo Maxwell, Residence Not Provided;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/470,431 03/31/2011

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)

If Required, Foreign Filing License Granted: 04/09/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/434,273**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE

Preliminary Class

396

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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UNITED STATES PATENT APPLICATION

for

METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE

INVENTOR:
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Attorney Docket No.: 8029.P107

TITLE

METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE

RELATED APPLICATIONS

[0001] This application claims priority from Provisional Application Serial Number 61/470,431, filed March 31, 2011, entitled "METHOD, APPARATUS AND SYSTEM FOR PROVIDING A BIDIRECTIONAL OPERATING MODE TO EXCHANGE AUDIO/VIDEO CONTENT", the teaching of which is incorporated herein by reference.

BACKGROUND

1. Technical Field

[0002] Embodiments relate generally to techniques for exchanging audio/video information. More particularly, certain embodiments provide techniques for controlling an audio/video device to selectively receive or send audio/video information.

2. Background Art

[0003] The size of computers and other audio/video (AV) capable electronic devices continue to scale with successive improvements in integrated circuit (IC) fabrication techniques. Consequently, there is a general trend toward a wider variety of AV devices, notably smaller AV devices, implementing functionality to support higher throughput and/or higher quality of AV information.

DELL/HP/LENOVO EXHIBIT 1002
Page 435

[0004] Certain conventional AV devices include a High-Definition Multimedia Interface (HDMI) connector or other such hardware for coupling to some other device, where the AV device operates as a source to provide AV information to the other device via the connector. Typical examples of conventional AV sources include a camcorder, digital camera, personal computer (e.g. tablet, notebook, laptop, desktop and/or the like), smart phone, video game console, DVD player, digital video recorder (DVR), set-top box, plug-in storage peripheral or other such device which is capable of sending AV information to some other device.

[0005] Other conventional AV devices operate as a sink to receive AV information from another device via such coupling hardware. Typical examples of conventional AV sinks include a television, monitor, display, home theater receiver, personal computer, projector or other such device which is capable of receiving AV information from some AV source.

[0006] One consequence of the current trends in AV technology is smaller and/or higher-capacity AV devices placing an increasing premium on the area which is taken up by multiple AV connectors. Another consequence of current trends is the increasing variety of combinations of AV devices which may be coupled to one another to exchange AV information. Due to such consequences, systems which exchange AV information between electronic devices are increasingly prone to inefficiencies in how such devices are to couple to and communicate with one another.

DELL/HP/LENOVO EXHIBIT 1002
Page 436

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The various embodiments of the present invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which:

[0008] FIG. 1 is a block diagram showing elements of a system for exchanging audio/video data according to an embodiment.

[0009] FIG. 2A is a flow diagram showing elements of a method for controlling an audio/video device according to an embodiment.

[0010] FIG. 2B is a flow diagram showing elements of a method for controlling an audio/video device according to an embodiment.

[0011] FIG. 3 is a layout diagram showing elements of a connector for exchanging audio/video data according to an embodiment.

[0012] FIG. 4A is a flow diagram showing elements of a method for controlling an audio/video device according to an embodiment.

[0013] FIG. 4B is a flow diagram showing elements of a method for controlling an audio/video device according to an embodiment.

[0014] FIG. 5 is a block diagram showing elements of an audio/video device according to an embodiment.

DELL/HP/LENOVO EXHIBIT 1002
Page 437

DETAILED DESCRIPTION

[0015] Embodiments discussed herein variously make, use or otherwise provide circuit logic to selectively control an audio/video (or "AV") device for operation at different times in various ones of a plurality of operation modes. The plurality of operation modes may include what is referred to herein as an "AV Sink" operation mode, for the AV device (also referred to herein as simply "device") to be a sink for receiving AV information from another AV device via a connector, and what is referred to herein as an "AV Source" operation mode, for the AV device to be a source for providing AV information to another AV device via the same connector. In an embodiment, the AV device includes the connector. In an alternate embodiment, the AV device may operate in a system which includes the connector – e.g. where the connector is to couple the system with some external device for an exchange of AV information.

[0016] As used herein, "audio/video" or "AV" refers to the characteristic of relating to either audio content or video content, or relating to both audio content and video content. For example, AV information may include some or all of audio data and/or control information and video data and/or control information. In an embodiment, an AV device may, in addition to exchanging AV information with another device, be operable to render audio content and/or video content for a user, although certain embodiments are not limited in this regard.

[0017] An AV device according to an embodiment includes communication logic to exchange AV data according to some interface standard. By way of illustration and not limitation, such communication logic may exchange AV data via a connector which is compatible with one or more of an HDMI standard such as the HDMI 1.4 standard released May 28, 2009 by HDMI Licensing, LLC of Sunnyvale, CA, a Mobile High-Definition Link (MHL)

DELL/HP/LENOVO EXHIBIT 1002
Page 438

standard such as the MHL 1.0 specification released June 30, 2010 by the MHL Consortium of Sunnyvale, CA, a Digital Visual Interface (DVI) standard such as the DVI 1.0 standard released April 02, 1999 by the Digital Display Working Group of Vancouver, WA, a DisplayPort standard such as the DisplayPort 1.2 standard released December 22, 2009 by the Video Electronics Standards Association of Newark, CA and/or the like.

[0018] In an embodiment, such communication logic may implement communications which, at different times, are compatible with different interface standards, where all such communications are via the same connector. For example, communication logic may include first logic to detect the presence of, and communicate with, an HDMI device and second logic to detect the presence of, and communicate with, an HDMI device, where the respective detection and communication functionalities of the first logic and second logic do not conflict with or otherwise impede the other. Such communication logic may, for example, be referred to as "MHL-ready HDMI," "HDMI/MHL" and/or the like. Features of various embodiments are discussed herein in the context of exchanging AV information according to an HDMI interface standard. However, such discussion may be extended to apply to any of a variety of additional or alternative interface standards for exchanging AV data, according to different embodiments.

[0019] Certain embodiments variously provide that, from either or both of a device power up and a device reset, an AV device will, by default, return to or otherwise be in a Sink mode. While in this mode such an AV device may then determine by stimulus and response or measurement means described herein that it is connected to an AV Sink device, in which case it may safely transition to an AV Source operation mode. In an embodiment, the AV device may translate back to AV Sink operation mode in response to an indication of a change in connectivity to the AV Sink device.

DELL/HP/LENOVO EXHIBIT 1002
Page 439

[0020] FIG. 1 illustrates elements of a system 100 for exchanging AV information according to an embodiment. System 100 may include a first device 110 comprising AV logic 112 to variously implement AV communications between first device 110 and one or more other devices. One embodiment may, for example, be implemented entirely within AV logic 112. Another embodiment may be implemented by first device 110 as a whole. Still another embodiment may be implemented by system 100 as a whole. Any of a variety of other embodiments may be alternatively implemented according to techniques discussed herein.

[0021] In an embodiment, first device 110 includes functionality of one or more of conventional AV source devices and/or functionality of one or more conventional AV sink devices. By way of illustration and not limitation, first device 110 may include functionality of one or more devices including, but not limited to, a personal computer (e.g. tablet, notebook, laptop, desktop and/or the like), camcorder, smart phone, video game console, television, monitor, display, set-top box, home theater receiver and/or the like.

[0022] First device 110 may include a connector 114, coupled via one or more signal lines to AV logic 112, to variously connect first device 110 to some other device of system 100 for an exchange of AV information. Connector 114 may include a plurality of channels, such as pins and/or other interconnect hardware, which are compatible with a particular AV interface standard – e.g. an HDMI standard.

[0023] In an illustrative embodiment, connector 114 may, at some point in time, couple first device 110 via an interconnect 122 to a second device 120 of system 100 – e.g. for an exchange 124 of AV information from second device 120 to first device 110. The particular direction of exchange 124 is not limiting on certain embodiments, and may alternatively be in the opposite

DELL/HP/LENOVO EXHIBIT 1002
Page 440

direction, where first device 110 operates as the AV Source and second device 120 operates as the AV Sink. Accordingly, second device 120 may, for example, include both logic (not shown) to implement conventional AV Source functionality or conventional AV Sink functionality. In another embodiment, second device 120 may include logic to variously provide both AV Source functionality and AV Sink functionality according to techniques described herein.

[0024] Certain embodiments variously mitigate at least one problem which might otherwise arises if two conventional AV devices are coupled to one another when those two devices are concurrently configured each for respective operation as an AV Source. Such connecting of AV Source devices to one another can risk damage to transmission hardware in either or both devices. For example, the two devices may attempt to drive power in opposite directions in the same power supply voltage channel of a connector. Alternatively, or in addition, two such devices may attempt to drive data signals in opposite directions via the same data channel of the connector. Such AV Source devices may risk driving any of a variety of other signals – e.g. hot plug detect signals, clock signals and/or the like – against one another each on some common respective channel of a connector.

[0025] AV logic 112 may limit the risk of the resulting damage in system 100 by providing a control mechanism to selectively prevent one or more aspects of AV Source functionality from being provided during operation of first device 110. By way of illustration and not limitation, AV logic 112 may selectively transition itself between a plurality of operation modes which includes an AV Source operation mode and an AV Sink operation mode. The AV Source operation mode may be for AV logic 112 to provide a particular signal to connection 114 – e.g. a supply voltage, a digital data signal and/or the like. Additionally or alternatively, the AV Source operation mode may be for AV logic 112 to provide a particular amount of impedance – e.g.

pull-up impedance, pull-down impedance and/or the like – for a signal line coupled to a channel of connection 114.

[0026] In an embodiment, control logic (not shown) of AV logic 112 selects one of the plurality of operation modes in response to an indication of a particular type of event at first device 110. Whether and/or how AV logic 112 might transition between operation modes may be based, for example, on whether the indicated event is a power-up event, a power-down event a reset event, and/or the like.

[0027] Whether and/or how AV logic 112 might transition between operation modes may be additionally or alternatively based on an event which detects a particular characteristic (or absence of said characteristic) regarding connectivity between connector 114 and second device 120. By way of illustration and not limitation, such a characteristic may include whether (or not) some second device 120 is providing a supply voltage at a particular channel of connector 114. For example, connector 114 may be compatible with an interface standard which stipulates that an AV Source is to provide a supply voltage to its corresponding AV Sink – e.g. the +5V output to be provided from Source to Sink according to HDMI, as on pin 18 of a 19-pin HDMI connector.

[0028] Additionally or alternatively, such a characteristic may include whether (or not) second device 120 is providing to connector 114 a hot plug detect (HPD) signal. For example, connector 114 may be compatible with an interface standard which stipulates that an AV Sink is to indicate its presence with a HPD signal to its corresponding AV Source – e.g. the HPD signal to be provided from Sink to Source according to HDMI, as on pin 19 of a 19-pin HDMI connector.

DELL/HP/LENOVO EXHIBIT 1002
Page 442

[0029] Additionally or alternatively, such a characteristic may include whether (or not) second device 120 is providing a clock signal to connector 114. For example, connector 114 may be compatible with an interface standard which stipulates that an AV Source is to provide a clock signal to an AV Sink – e.g. the DDC_SCL signal to be provided from Source to Sink according to HDMI, as on pin 15 of a 19-pin HDMI connector.

[0030] Additionally or alternatively, such a characteristic may include whether (or not) a particular amount of impedance is being provided by second device 120 for a channel of connector 114. For example, connector 114 may be compatible with an interface standard which stipulates that a particular pull-up impedance is to be implemented at an AV Sink – e.g. a 47kΩ pull-up resistance which HDMI requires be provided at an AV Sink for a SDA line (e.g. pin 16 of a 19-pin HDMI connector).

[0031] In an embodiment, the functionality of AV logic 112 allows connector 114 to be variously coupled, decoupled and/or recoupled at different times to one or more devices, while limiting a risk of damage to hardware in system 100. By way of illustration and not limitation, connector 114 may at some point in time be decoupled from second device 120 and subsequently coupled via an interconnect 132 to some third device 130 – e.g. for an exchange 134 of AV information to third device 130 from first device 110. The particular direction of exchange 134 is not limiting on certain embodiments, any may alternatively be in the opposite direction, where first device 110 operates as the AV Sink and third device 130 operates as the AV Source. In an embodiment, third device 130 is simply second device 120 – e.g. where second device 120 is decoupled from and subsequently recoupled to first device 110 and/or where first device 110 and second device 120 switch AV Sink and AV Source roles for different AV information exchanges.

DELL/HP/LENOVO EXHIBIT 1002
Page 443

[0032] As shown in the discussion herein, AV logic 112 may protect various circuitry of system 100 for different successive couplings of first device 110 each to a respective device and/or for successive different AV information exchanges each between first device 110 and a respective device.

[0033] FIG. 2A illustrates elements of a method 200 for controlling operation of an AV device according to an embodiment. An AV device controlled by performing method 200 may, for example, be a device including some or all of the features of first device 110. In one embodiment, an AV device controlled by performing method 200 may merely include some or all of the features of AV logic 112 – e.g. without also including other features of first device 110 such as connector 114. Features of various embodiments are discussed herein in terms of performing method 200 to control AV logic 112 within first device 110. However, such discussion may be extended to apply to any of a variety of additional or alternative AV hardware, consistent with the techniques disclosed herein.

[0034] In an embodiment, the AV device includes communication logic comprising circuitry to operate at different times in different ones of a plurality of operation modes which include an AV Source operation mode and an AV Sink operation mode. The AV Sink operation mode may, for example, be for the communication logic to receive AV data provided to the AV device via a connector – e.g. via connector 114. The AV Sink operation mode may further be for the communication logic to receive power from a first supply voltage provided via a channel of the connector. By contrast, the AV Source operation mode may be for the communication logic to send AV data from the AV device, where the AV data is sent through the connector. The AV Source operation mode may further be for the communication logic to provide a second supply

DELL/HP/LENOVO EXHIBIT 1002
Page 444

voltage at the channel of the connector. In an embodiment, a level of the first supply voltage is equal to a level of the second supply voltage.

[0035] In an embodiment, method 200 includes, at 210, detecting an indication of one of a power up event at the AV device, a power down event at the device or a reset event at the AV device. The detecting at 210 may, for example, include control circuitry of AV logic 112 directly or indirectly detecting an indication sent from some agent included in or otherwise accessible to AV logic 112. By way of illustration and not limitation, first device 110 may include a power management unit, a host processor or other agent which sends to AV logic 112 a signal specifying, for example, that first device 110 is going through, has gone through, or is expected to go through a boot up or boot down operation, or otherwise to transition to or from an operative power state. In an embodiment, transitioning to or from such an operative power state may include transitioning between a first power state in which AV logic 112 is incapable of exchanging AV information via connector 114 and a second power state in which AV logic 112 is capable of exchanging AV information via connector 114. Alternatively or in addition, AV logic 112 may include detector logic to evaluate power state of AV logic 112 and/or of other components of first device 110.

[0036] The detecting at 210 may additionally or alternatively include control circuitry of AV logic 112 directly or indirectly detecting a signal from some agent, included in or otherwise accessible to AV logic 112, the signal specifying or otherwise indicating that AV logic 112 or some other component of first device 110 have been, are being, or are expected to be reset. Such a reset may flush some current state of circuit logic in favor of some predetermined baseline configuration. A reset may, for example, return some or all of first device 110 to a predetermined configuration without powering down first device 110.

[0037] In response to the indication detected at 210, method 200 may, at 220, automatically initialize communication logic of the AV device. By way of illustration and not limitation, control logic of AV logic 112 may automatically place the communication logic of AV logic 112 into a default operation mode which prevents the second supply voltage from being provided by the communication logic at the channel of the connector. In an embodiment, the default operation mode is the AV Sink operation mode. In an embodiment, the AV Source operation mode is further for the communication logic of the AV device to provide a first total amount of impedance for a data channel of the connector. In such an embodiment, the default operation mode may prevent the first total amount of impedance for the data channel from being provided by the communication logic.

[0038] FIG. 2B illustrates elements of a method 250 for controlling operation of an AV device according to an embodiment. An AV device controlled by performing method 250 may, for example, be a device having some or all of the features of a device controlled by method 200. Method 250 may, for example, be performed after method 200 – although certain embodiments are not limited in this regard. Features of various embodiments are discussed herein in terms of performing method 250 to control AV logic 112 within first device 110. However, such discussion may be extended to apply to any of a variety of additional or alternative AV hardware, consistent with the techniques disclosed herein.

[0039] Method 250 may include, at 260, detecting a characteristic regarding a connectivity of the AV device to another device via a connector – e.g. connector 114. For example, detector logic of AV logic 112 may detect connectivity to the other device via the connector – e.g. the detecting while the communication logic of the AV device is in the default operation mode of method 200. Additionally or alternatively, such detector logic of AV logic 112 may detect a

DELL/HP/LENOVO EXHIBIT 1002
Page 446

change in a state of connectivity to the other device via the connector. The detecting the characteristic at 260 may, for example, include detecting an indication that the other device is providing the first supply voltage discussed with regard to method 200. Alternatively or in addition, the detecting at 260 may include detecting that the other device is providing to the connector a hot plug detect (HPD) signal, a clock signal and/or any of a variety combinations of one or more other signals. Alternatively or in addition, the detecting at 260 may include evaluating an impedance of a signal line which couples the other device to the connector.

[0040] In response to detecting the characteristic at 260, method 200 may, at 270, automatically place the communication logic of the AV device into some first operation mode which prevents a providing of the second supply voltage referred to in the discussion of method 200. The first operation mode may, for example, be the default operation mode of method 200, although certain embodiments are not limited in this regard. In placing the AV device into the first operation mode, method 250 may limit the possibility of circuit damage due to conflicting output signals from two coupled AV devices, each device attempting to operate as an AV Source.

[0041] FIG. 3 illustrates select elements of a connector 300 for exchanging AV information according to an embodiment. Connector 300 may include some or all of the features of connector 114, for example. The illustrative connector 300 is a 19-channel (e.g. 19-pin) connector which is compatible with an HDMI interface standard, although certain embodiments are not limited in this regard. Connector 300 may support AV information exchanges by any of a variety of other types of interconnect hardware – e.g. a connector including more, fewer, or alternative channels to those shown in FIG. 3 – where communication via such a connector is consistent with techniques discussed herein.

DELL/HP/LENOVO EXHIBIT 1002
Page 447

[0042] The illustrative connector 300 includes interconnect hardware to support transition-minimized differential signaling (TMDS) in HDMI communication. More particularly, the respective functions of the channels in connector 300 may be assigned according to HDMI 1.4 or some other HDMI interface standard – e.g. as follows:

Channel 1	TMDS Data2+
Channel 2	TMDS Data2 Shield
Channel 3	TMDS Data2–
Channel 4	TMDS Data1+
Channel 5	TMDS Data1 Shield
Channel 6	TMDS Data1–
Channel 7	TMDS Data0+
Channel 8	TMDS Data0 Shield
Channel 9	TMDS Data0–
Channel 10	TMDS Clock+
Channel 11	TMDS Clock Shield
Channel 12	TMDS Clock–
Channel 13	Consumer Electronics Control (CEC)
Channel 14	HDMI Ethernet Channel (HEC) Data
Channel 15	System Clock Line (SCL) – I^2C Serial Clock for Display Data Channel (DDC)
Channel 16	System Data (SDA) – I^2C Serial Data Line for DDC
Channel 17	DDC/CEC/HEC Ground
Channel 18	+5 V Power
Channel 19	Hot Plug Detect (HPD) and/or HEC Data+

Potential conflict may result when two connected AV devices concurrently attempt to drive respective supply voltages and/or other signals according to the same function assignments for connector 300.

DELL/HP/LENOVO EXHIBIT 1002
Page 448

[0043] In an embodiment, an AV device including or coupled to connector 300 may implement techniques to reduce the likelihood of such conflict – e.g. techniques including some or all of the features discussed with respect to method 200 and/or method 250. By way of illustration and not limitation, control logic of such an AV device may provide that after some event – e.g. from one or more of a power up event, a power down event and a reset event – communication logic of the AV device will operate in an AV Source operation mode only after certain connectivity conditions are subsequently identified. For example, the control logic may configure the AV device after/during power up – or before/during a power down – for a default operation mode in which a functionality required for operation as an AV Source is disabled. For instance, the disabled functionality may be required for operation as an AV Source device according to the conditions of HDMI or some other interface standard.

[0044] Alternatively or in addition, the control logic may configure the AV device for an AV Sink operation mode in response to detecting a change of a characteristic regarding connectivity between the AV devices. For example, the AV device may be set to, or return to, some default AV Sink operation mode in response to an indication of a loss or absence at connector 300 of a supply voltage, an indication of a loss or absence of a HPD signal, an indication of a signal line pull-up impedance implemented by any other connected AV device, and/or an indication of a clock signal provided by any other connected AV device. Any of a variety of additional or alternative detected conditions may determine whether and/or how the AV device may be configured – or reconfigured – for operation in such a default mode. In one embodiment, the default operating mode is a SINK mode of HDMI in which the AV device is capable of operation as an AV Sink.

DELL/HP/LENOVO EXHIBIT 1002
Page 449

[0045] In an embodiment, control logic of an AV device may implement a state machine or other mechanism for transitioning the communication logic between operation modes including SINK mode and SOURCE mode. By way of illustration and not limitation, the AV device may default its communication logic to SINK mode in response to (or during) a power up of the AV device (or in response to, or during, a power down of the AV device), and/or in response to detecting that a connectivity characteristic with another AV device is absent or has changed. The AV device may variously transition between SINK mode and SOURCE mode, depending on one or more connectivity characteristics detected for connector 300. Such connectivity characteristics may include, but are not limited to, whether a +5V voltage is provided by another AV device through connector 300, and/or whether one or more signals or other connectivity characteristics (e.g. HPD, DDC pull ups, TDMS termination, etc.) indicate presence or absence of functionality of some other connected AV device as an operable Sink or operable Source.

[0046] FIG. 4A and 4B illustrate select elements of methods 400a, 400b, respectively, for controlling operation of an AV device according to an embodiment. An AV device controlled by performing either or both of methods 400a, 400b may, for example, be a device including some or all of the features of first device 110. In one embodiment, the AV device controlled by performing either or both of methods 400a, 400b may merely include some or all of the features of AV logic 112 – e.g. without also including other features of first device 110 such as connector 114. Methods 400a, 400b may include some or all of the features discussed herein with respect to methods 200, 250, although certain embodiments are not limited in this regard.

[0047] FIG. 4A and 4B are discussed herein with respect to features which are specific to HDMI interface requirements. However, such discussion may be extended to apply to requirements of any of a variety of additional or alternative interface standards for

DELL/HP/LENOVO EXHIBIT 1002
Page 450

communicating AV information. For example, various additional or alternative test conditions (e.g. different delays, resistance values, signal outputs, test conditions, etc.) may be used, according to different embodiments, for determining whether and/or how one or more operation mode transitions of an AV device are to take place.

[0048] Method 400a may, at 405, initialize the AV device to SINK mode by default in response to an indication of a reset event, a power-on event or a power-off event. The initializing at 405 may, for example, include disabling one or more of a +5V HDMI output (channel 18), HPD output (pin 19), some or all DDC outputs (pins 15 and/or 16), and respective 1.8K pull-up resistors for such DDC outputs. The initializing at 405 may further include initializing extended display identification data (EDID) functionality of the AV device in preparation for identifying capabilities to any other device coupled via the connector – e.g. connector 114. After the initializing at 405, method 400 may, at 410, provide some delay – e.g. 100ms – for a high-value pull-down resistor to discharge the +5V HDMI output. However, such delay may not be required, in certain embodiments.

[0049] After delay at 410, method 400 may test for some indication that another device is coupled to the AV device being controlled by method 400a. By way of illustration and not limitation, method 400a may test, at 415, test whether a +5V HDMI supply voltage is being provided at connector 114 – indicating that a device coupled via the connector is operating in some AV Source mode. If the +5V supply voltage is detected at 415, then method 400a may, at 420, assert a HPD signal at the connector (pin 19) and, at 425, commence operation of the communication logic of the AV device in a SINK mode. The AV device may test for a change in connectivity with the other device – e.g. by occasionally testing at 430 +5V supply voltage continues to be provided at the connector by the other device. In an embodiment, detecting that

the +5V supply voltage is not being so provided may result in method 400a disabling its HPD signal, its DDC output functionality and/or any other AV Sink functionality that is not currently being used. Method 400a may then return to providing the delay at 410 in preparation for again testing for presence of any connected device.

[0050] If the +5V supply voltage is not detected at 415, then method 400a may detect for the presence of any device which might be coupled via the connector and which is operating in some AV Sink mode. By way of illustration and not limitation, method 400a may test, at 440, to confirm that there is a 47kΩ pull-up resistor on the clock channel of the connector (SCL channel 15) as required by the HDMI specification, that an impedance on the data (SDA channel 16) is not in the HDMI specified Source range of 1.5kΩ to 2.0kΩ, and that a receiver sense input (RSEN) signal indicates that one or more differential pairs of the connector are provided with terminators at some coupled device. If no AV Sink device is detected at 415, method 400a may then return to providing the delay at 410, in preparation for again testing for presence of any connected device.

[0051] If an AV Sink device is detected at 415, then in one embodiment, operations of method 400b may follow. For example, method 400b may, at 450, initiate a transition to SOURCE mode – e.g. including enabling the communication logic of the AV device to provide the +5V supply voltage to the connector. In an embodiment, method 400b may, at 455, start a HPD timer – e.g. set for 0.5 seconds – for timing out if a HPD signal is not detected from some AV Sink device. Method 400b may test, at 460, whether an HPD signal is detected – e.g. where the test at 460 may be successively performed according to a test at 480 of whether the HPD timer has expired. If an HPD signal is detected at 460, method 400b may begin operation of the AV device in a SOURCE mode, at 465.

DELL/HP/LENOVO EXHIBIT 1002
Page 452

[0052] If the HPD timer is determined to have expired at 480, method 400b may perform evaluations of whether one or more indications of a coupled AV Sink device are still present at the connector. By way of illustration and not limitation, method 400b may test, at 485, to confirm whether there is a 47kΩ pull-up resistor on the clock channel of the connector (SCL channel 15) as required by the HDMI specification. If such a 47kΩ pull-up resistor is detected at 485, method 400b may return to setting another HPD timer at 455.

[0053] If no such 47kΩ pull-up resistor is detected at 485, method 400b may begin preparations, at 445, to transition the AV device back to a SINK mode – e.g. including disabling one or more of a +5V HDMI output (channel 18), some or all DDC outputs (pins 15 and/or 16), respective 1.8K pull-up resistors for such DDC outputs, and/or the like. After the preparation for SINK mode operation at 445, method 400b may be followed by an operation of method 400a – e.g. the providing of a delay at 410.

[0054] In an embodiment, operation of the AV device in SOURCE mode, at 465, includes enabling 1.8K pull-up resistors for DDC channels of the connector which are to serve as output channels. Additionally or alternatively, SOURCE mode operation at 465 may include performing an EDID read of the capabilities of the detected AV Sink device. Operation of the AV device in SOURCE mode may continue until a test at 470 indicates that the detected AV Sink device is no longer providing a HPD signal. If such an HPD signal is no longer detected, method 400b may begin to protect the AV device from possible harm – e.g. caused by the detected AV Sink device somehow transitioning to AV Source operation. By way of illustration and not limitation, method 400b may, at 475, disable respective 1.8 kΩ pull-up resistors for one or more DDC channels of the connector. After the disabling at 475, method 400b may perform the presence test at 485.

DELL/HP/LENOVO EXHIBIT 1002
Page 453

[0055] FIG. 5 illustrates select elements of a system 500 for exchanging AV information according to an embodiment. System 500 may include some or all of the features of first device 110, for example. For example, system 500 may include AV logic 570 having some or all of the features of AV logic 112.

[0056] System 500 may include an AV connector – represented by an illustrative HDMI connector 510 at the edge of system 500 – to couple system 500 to some external device (not shown) for an AV information exchange. AV logic 570 may include mechanisms to variously implement different operation modes in system 500 to accommodate different types of AV communications via HDMI connector 510. By way of illustration and not limitation, AV 570 may include control logic 505 to receive information indicating a presence or absence of one or more characteristics regarding connectivity of system 500 with some AV device via HDMI connector 510.

[0057] For example, control logic 505 may include or otherwise have access to detection logic 520 of system 500 which relays and/or analyzes signals exchanged via HDMI connector 510. In an embodiment, detection logic 520 may include one or more of logic to detect for a supply voltage output, logic to detect for a signal line termination, logic to detect for an EDID or other such identifier, logic to detect for a digital data functionality, logic to detect for a clock signal and/or the like. The particular mechanism for detection logic 520 to perform such detecting may be adapted from conventional techniques for detecting clock signals, data voltage inputs, impedances, etc., and are not limiting on certain embodiment. Although shown as being coupled along the data exchange path to intercept one or more signals exchanged via HDMI connector 510, detection logic 520 may, in an alternate embodiment, be configured to passively sense signals exchanged via HDMI connector 510.

DELL/HP/LENOVO EXHIBIT 1002
Page 454

[0058] Messages from detection logic 520 may indicate to control logic 505 whether and/or how system 500 is to transition logic of system 500 between operating modes. In an embodiment, control logic 505 may provide control functionality to variously place communication logic 580 of system 500 at different times in different ones of a plurality of operation modes – e.g. where the plurality of operation modes includes a SINK mode and a SOURCE mode. For example, control logic 505 may transition communication logic 580 between operation modes according to some or all of the techniques of method 500 and/or method 550.

[0059] By way of illustration and not limitation, control logic 505 may configure a switch of communication logic 580 – represented by an illustrative analog switch 530 – to switch between HDMI (or other AV interface standard) transmit logic 540 for SOURCE mode operation and HDMI (or other AV interface standard) receive logic 550 for SINK mode operation.

[0060] Control logic 505 may also provide functionality to further configure either or both of HDMI transmitter logic 540 and HDMI receive logic 550, although certain embodiments are not limited in this regard. For example, HDMI receive logic 550 may include HDMI/MHL functionality to switch between a sub-mode to receive HDMI information from another AV device and a sub-mode to receive MHL information. Control logic 505 may provide signaling (not shown) to selectively configure HDMI receive logic 550 to variously operate in such sub-modes at different times.

[0061] Techniques and architectures for configuring an AV device are described herein. In the above description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of certain embodiments. It will be apparent, however,

to one skilled in the art that certain embodiments can be practiced without these specific details. In other instances, structures and devices are shown in block diagram form in order to avoid obscuring the description.

[0062] Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment.

[0063] Some portions of the detailed description herein are presented in terms of algorithms and symbolic representations of operations on data bits within a computer memory. These algorithmic descriptions and representations are the means used by those skilled in the computing arts to most effectively convey the substance of their work to others skilled in the art. An algorithm is here, and generally, conceived to be a self-consistent sequence of steps leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like.

[0064] It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the discussion herein, it is appreciated that throughout the description, discussions utilizing terms such as "processing" or

DELL/HP/LENOVO EXHIBIT 1002
Page 456

"computing" or "calculating" or "determining" or "displaying" or the like, refer to the action and processes of a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

[0065] Certain embodiments also relate to apparatus for performing the operations herein. This apparatus may be specially constructed for the required purposes, or it may comprise a general purpose computer selectively activated or reconfigured by a computer program stored in the computer. Such a computer program may be stored in a computer readable storage medium, such as, but is not limited to, any type of disk including floppy disks, optical disks, CD-ROMs, and magnetic-optical disks, read-only memories (ROMs), random access memories (RAMs) such as dynamic RAM (DRAM), EPROMs, EEPROMs, magnetic or optical cards, or any type of media suitable for storing electronic instructions, and coupled to a computer system bus.

[0066] The algorithms and displays presented herein are not inherently related to any particular computer or other apparatus. Various general purpose systems may be used with programs in accordance with the teachings herein, or it may prove convenient to construct more specialized apparatus to perform the required method steps. The required structure for a variety of these systems will appear from the description herein. In addition, certain embodiments are not described with reference to any particular programming language. It will be appreciated that a variety of programming languages may be used to implement the teachings of such embodiments as described herein.

DELL/HP/LENOVO EXHIBIT 1002
Page 457

[0067] Besides what is described herein, various modifications may be made to the disclosed embodiments and implementations thereof without departing from their scope. Therefore, the illustrations and examples herein should be construed in an illustrative, and not a restrictive sense. The scope of the invention should be measured solely by reference to the claims that follow.

DELL/HP/LENOVO EXHIBIT 1002
Page 458

CLAIMS

What is claimed is:

1. A method at an audio/video (AV) device, the method comprising:

detecting with control circuitry an indication of one of a power up event at the AV device, a power down event at the AV device, or a reset event at the AV device; and

in response to the indication, automatically initializing communication logic of the AV device with the control circuitry, wherein an AV sink operation mode of the communication logic is for the communication logic to receive AV data provided to the device via a connector, the AV sink operation mode further for the communication logic to receive power from a first supply voltage provided to the device at a channel of the connector, wherein an AV source operation mode of the communication logic is for the communication logic to send AV data from the device via the connector, the AV source operation mode further for the communication logic to provide a second supply voltage at the channel of the connector, and wherein automatically initializing the communication logic includes placing the communication logic into a default operation mode which prevents the second supply voltage from being provided by the communication logic at the channel of the connector.

2. The method of claim 1, wherein the default operation mode is the AV sink operation mode.

3. The method of claim 1, wherein the default operation mode is for communication according to a high-definition multimedia interface standard.

DELL/HP/LENOVO EXHIBIT 1002
Page 459

4. The method of claim 1, wherein the AV Source operation mode is further for the communication logic to provide a first total amount of impedance for a data channel of the connector, and wherein the default operation mode further prevents the first total amount of impedance for the data channel from being provided by the communication logic.

5. The method of claim 1, further comprising:

detecting a connectivity of the device to another device via the connector, the detecting the connectivity while the communication logic is in the default operation mode;

in response to the detected connectivity, performing a determination of whether to transition the communication logic from the default operation mode to another operation mode; and

performing an AV data exchange with the other device based on the determination.

6. The method of claim 5, wherein detecting the connectivity includes detecting that the other device is providing the first supply voltage to the channel of the connector.

7. The method of claim 5, further comprising:

detecting a change to the connectivity after the AV data exchange; and

in response to the detected change to the connectivity, placing the communication logic into a first operation mode which prevents the second supply voltage from being provided by the communication logic at the channel of the connector.

8. The method of claim 7, wherein the first operation mode is the default operation mode.

DELL/HP/LENOVO EXHIBIT 1002
Page 460

9. A device comprising:

communication logic to couple to a connector, the communication logic including circuitry to implement:

an audio/video (AV) Sink operation mode for the communication logic to receive AV data provided to the device at the connector, the AV Sink operation mode further for the communication logic to receive power from a first supply voltage provided to the device via a channel of the connector; and

an AV Source operation mode for the communication logic to send AV data from the device via the connector, the AV Source operation mode further for the communication logic to provide a second supply voltage at the channel of the connector;

control logic including circuitry to automatically initialize the communication logic in response to one of a power up event at the AV device, a power down event at the AV device, or a reset event at the AV device, wherein the control logic to place the communication logic into a default operation mode which prevents the second supply voltage from being provided by the communication logic at the channel of the connector.

10. The device of claim 9, wherein the default operation mode is the AV Sink operation mode.

11. The device of claim 9, wherein the default operation mode is for communication according to a high-definition multimedia interface standard.

12. The device of claim 9, wherein the AV source operation mode is further for the communication logic to provide a first total amount of impedance for a data channel of the

DELL/HP/LENOVO EXHIBIT 1002
Page 461

connector, and wherein the default operation mode further prevents the first total amount of impedance for the data channel from being provided by the communication logic.

13. The device of claim 9, further comprising:

detector logic to detect, while the communication logic is in the default operation mode, a connectivity of the device to another device via the connector;

wherein, in response to the detected connectivity, the control logic further to perform a determination of whether to transition the communication logic from the default operation mode to another operation mode; and

wherein the communication logic further to perform an AV data exchange with the other device based on the determination.

14. The device of claim 13, wherein the detector logic to detect the connectivity includes the detector logic to detect that the other device is providing the first supply voltage to the channel of the connector.

15. A system comprising:

a connector;

communication logic coupled to the connector, the communication logic including circuitry to implement:

an audio/video (AV) sink operation mode for the communication logic to receive AV data provided to the system at the connector, the AV sink operation mode further for the

DELL/HP/LENOVO EXHIBIT 1002
Page 462

communication logic to receive power from a first supply voltage provided to the system at a channel of the connector; and

an AV source operation mode for the communication logic to send AV data from the system via the connector, the AV source operation mode further for the communication logic to provide a second supply voltage at the channel of the connector;

control logic including circuitry to automatically initialize the communication logic in response to one of a power up event at the AV device, a power down event at the AV device, or a reset event at the AV device, wherein the control logic to place the communication logic into a default operation mode which prevents the second supply voltage from being provided by the communication logic at the channel of the connector.

16. The system of claim 15, wherein the default operation mode is the AV sink operation mode.

17. The system of claim 15, further comprising:

detector logic to detect, while the communication logic is in the default operation mode, a connectivity of the system to a device via the connector;

wherein, in response to the detected connectivity, the control logic further to perform a determination of whether to transition the communication logic from the default operation mode to another operation mode; and

wherein the communication logic further to perform an AV data exchange with the device based on the determination.

DELL/HP/LENOVO EXHIBIT 1002
Page 463

18. The system of claim 17, wherein the detector logic to detect the connectivity includes the detector logic to detect that the device is providing the first supply voltage to the channel of the connector.

19. The system of claim 17, the detect logic further to detect a change to the connectivity after the AV data exchange, wherein, in response to the detected change to the connectivity, the control logic further to place the communication logic into a first operation mode which prevents the second supply voltage from being provided by the communication logic at the channel of the connector.

20. The system of claim 19, wherein the first operation mode is the default operation mode.

DELL/HP/LENOVO EXHIBIT 1002
Page 464

ABSTRACT OF THE DISCLOSURE

Techniques and mechanisms for determining an operation mode of an audio-video (AV) device. In an embodiment, communication logic of the AV device may be configured at different times for different ones of a plurality of operation modes including an AV source operation mode for providing AV information to another device and an AV sink operation mode for receiving AV information from another device. In response to a detected event, control logic initializes the communication logic of the AV device into a default mode which prevents operation of the communication logic as an AV source.

DELL/HP/LENOVO EXHIBIT 1002
Page 465

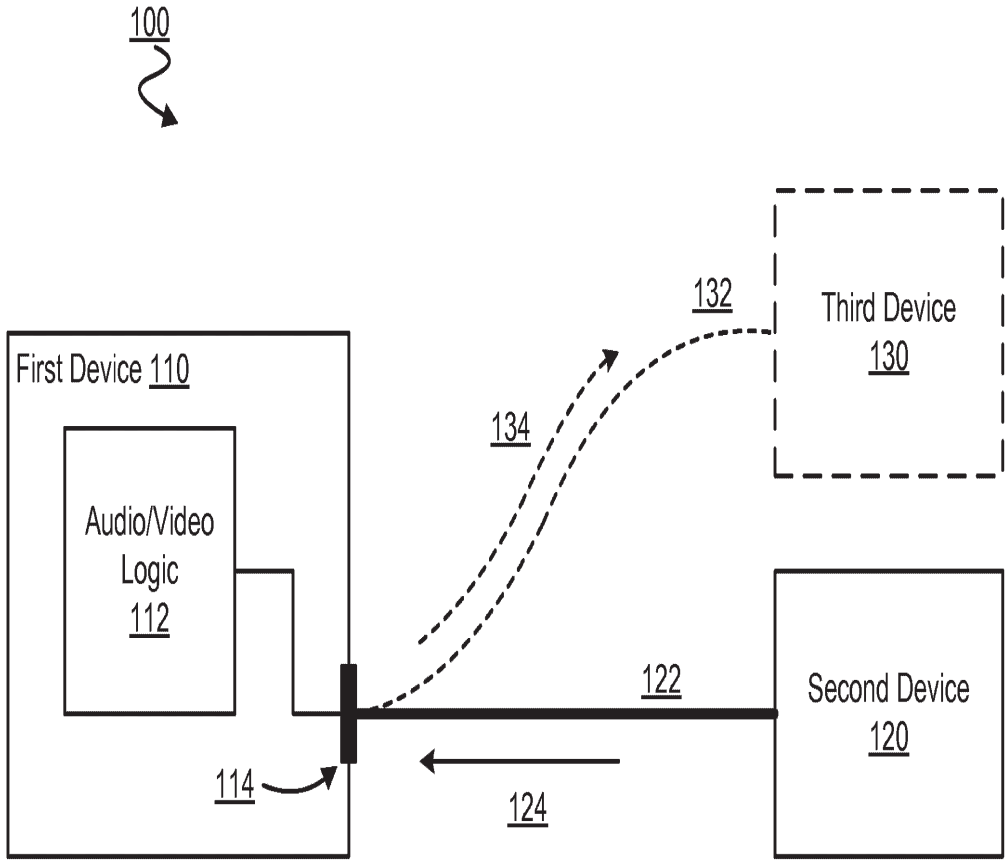

100
First Device 110
Audio/Video Logic 112
114
132
134
Third Device 130
122
Second Device 120
124

FIG. 1

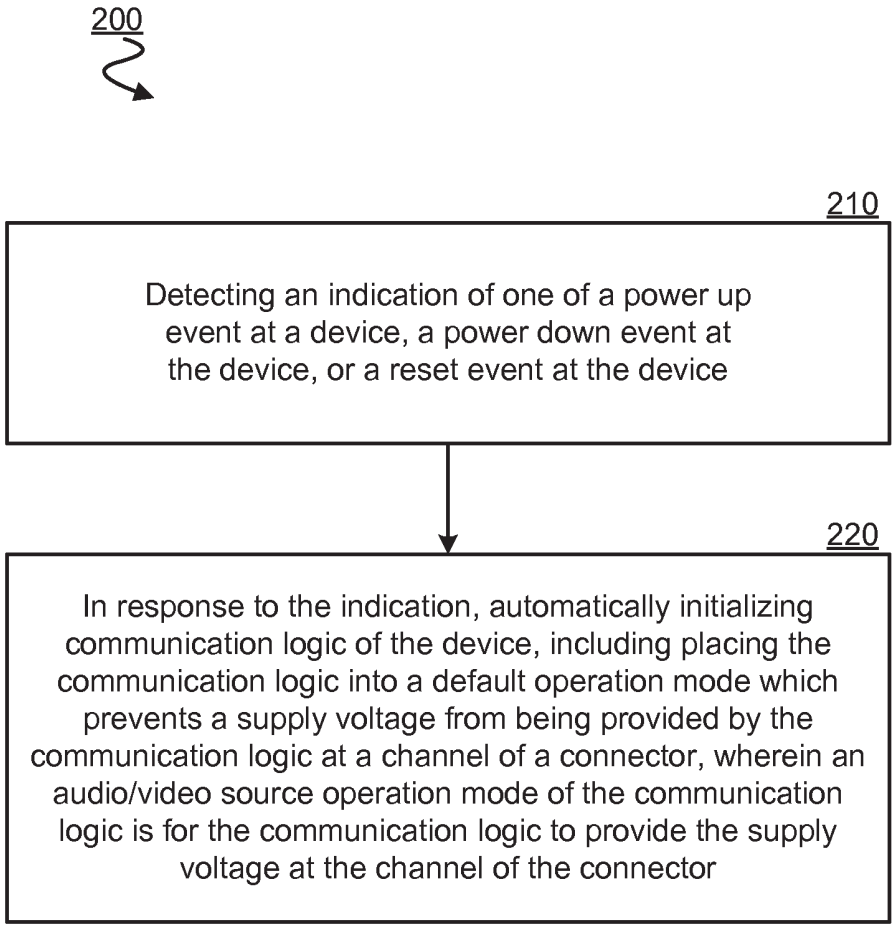

200
210
Detecting an indication of one of a power up event at a device, a power down event at the device, or a reset event at the device
220
In response to the indication, automatically initializing communication logic of the device, including placing the communication logic into a default operation mode which prevents a supply voltage from being provided by the communication logic at a channel of a connector, wherein an audio/video source operation mode of the communication logic is for the communication logic to provide the supply voltage at the channel of the connector

FIG. 2A

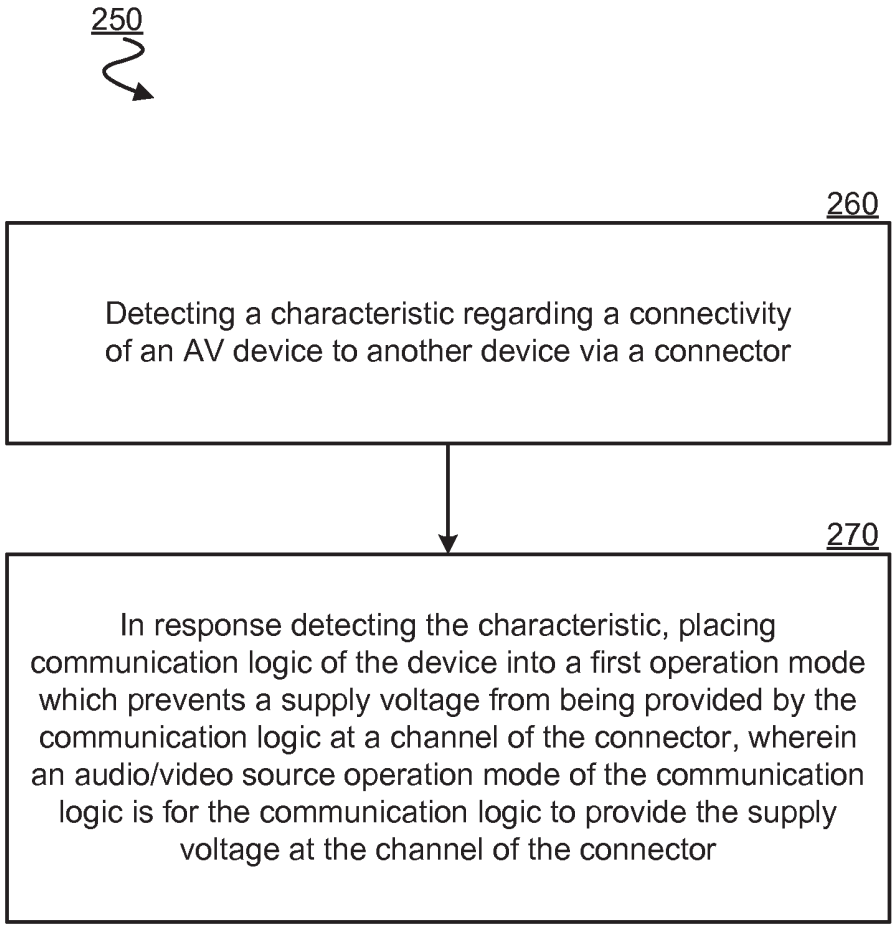

250
260
Detecting a characteristic regarding a connectivity of an AV device to another device via a connector
270
In response detecting the characteristic, placing communication logic of the device into a first operation mode which prevents a supply voltage from being provided by the communication logic at a channel of the connector, wherein an audio/video source operation mode of the communication logic is for the communication logic to provide the supply voltage at the channel of the connector

FIG. 2B

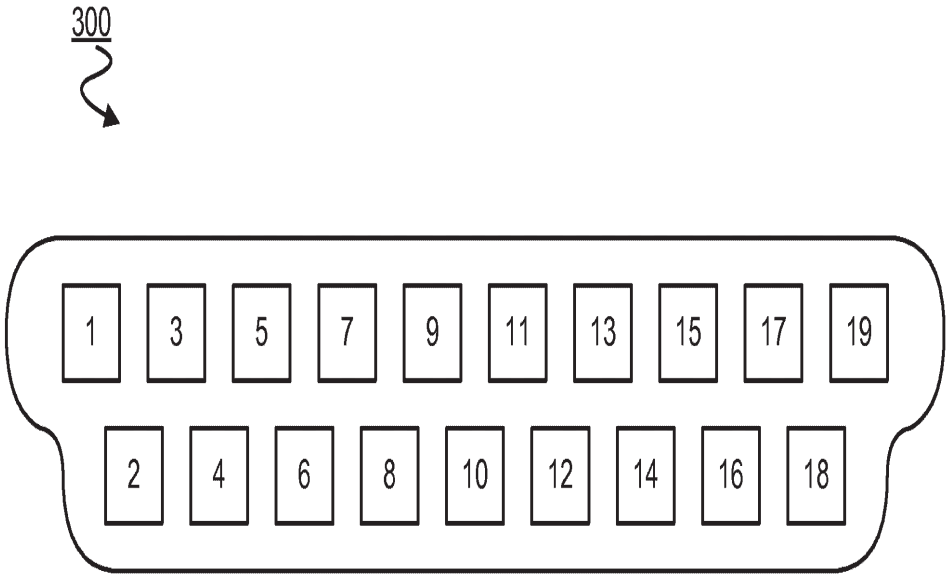


FIG. 3

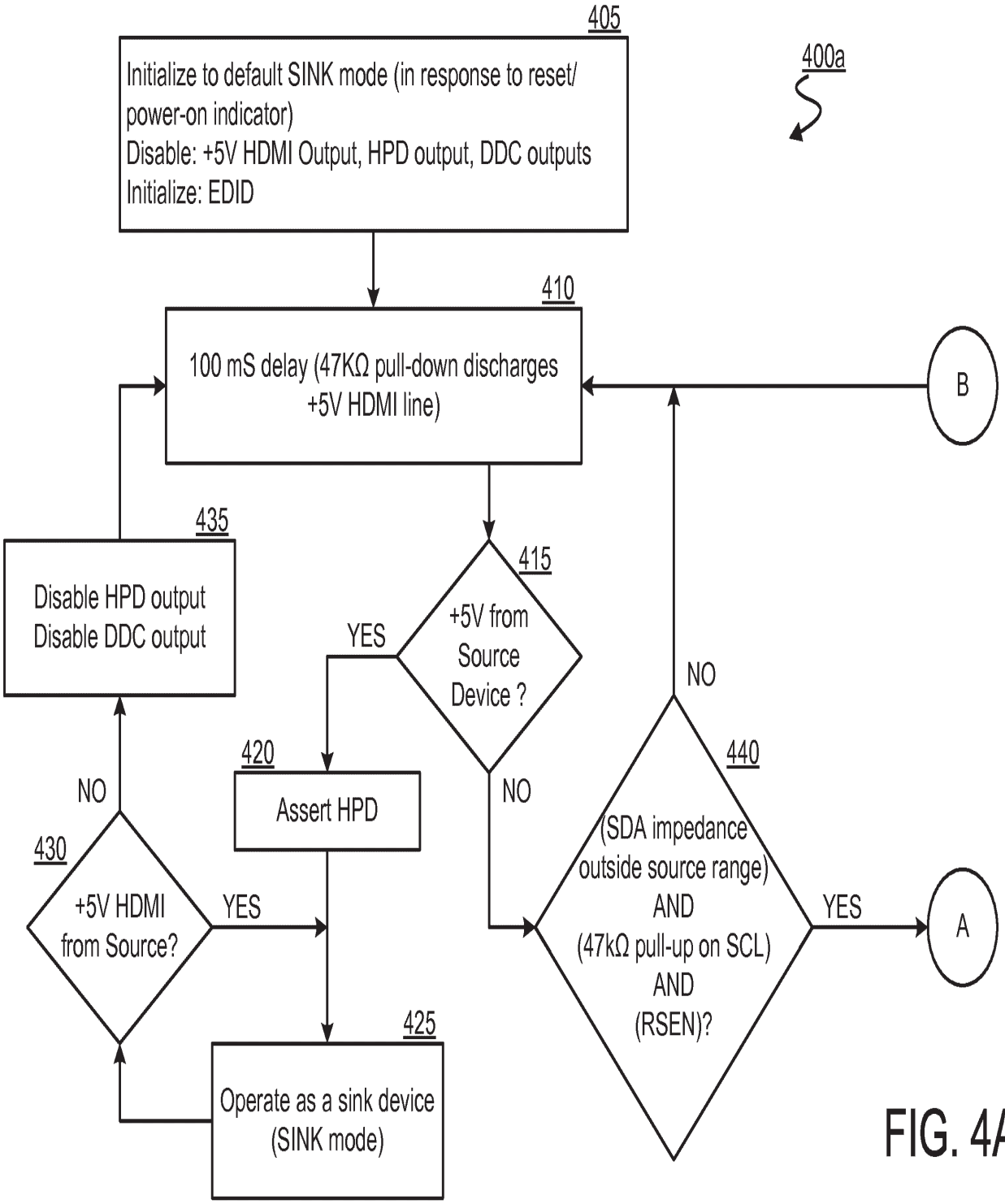

405
Initialize to default SINK mode (in response to reset/ power-on indicator)
Disable: +5V HDMI Output, HPD output, DDC outputs
Initialize: EDID
400a
410
100 mS delay (47KΩ pull-down discharges +5V HDMI line)
B
435
Disable HPD output
Disable DDC output
415
+5V from Source Device ?
YES
NO
420
Assert HPD
NO
430
+5V HDMI from Source?
YES
440
(SDA impedance outside source range) AND (47kΩ pull-up on SCL) AND (RSEN)?
YES
A
425
Operate as a sink device (SINK mode)

FIG. 4A

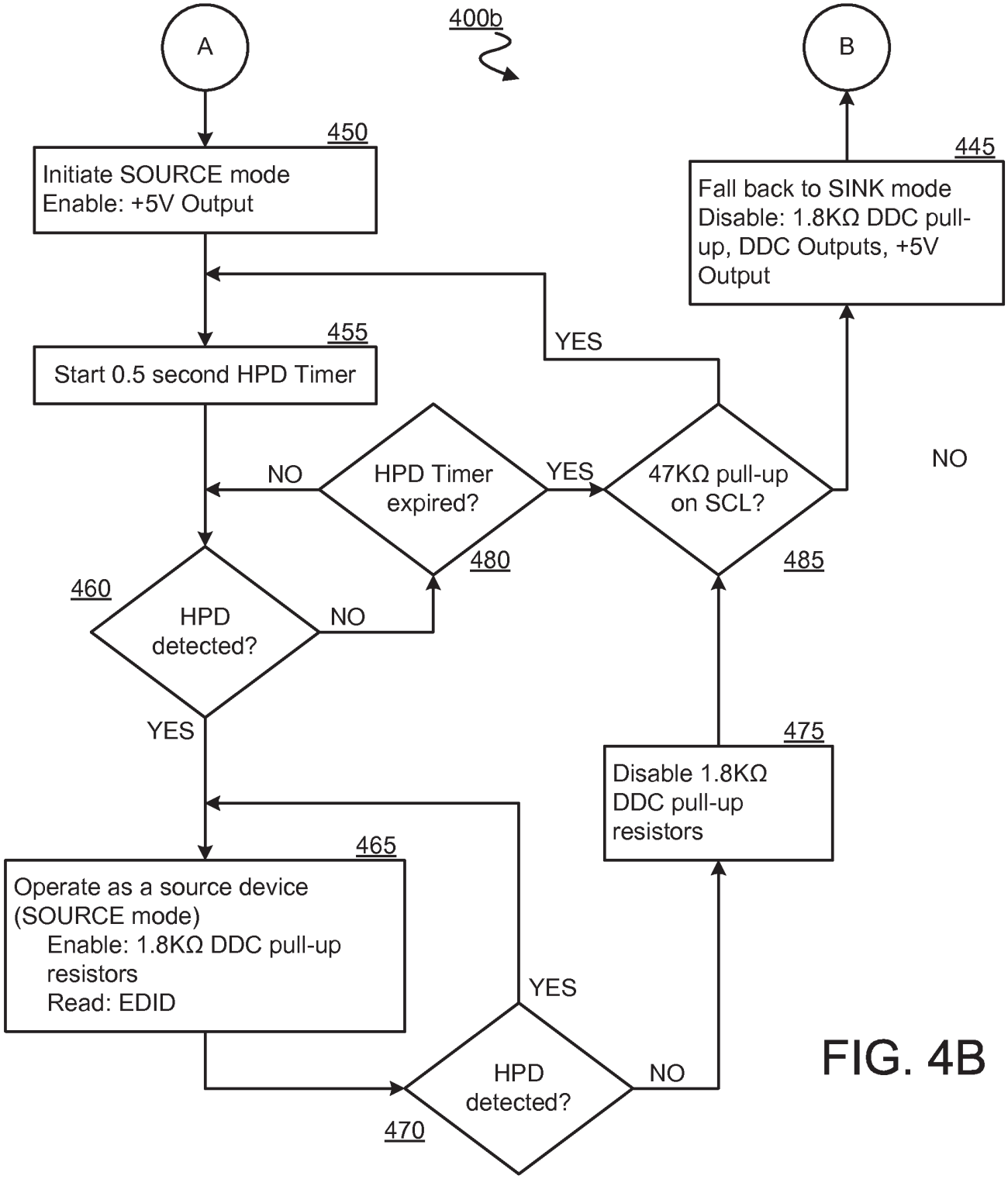

400b
A
B
450
Initiate SOURCE mode
Enable: +5V Output
445
Fall back to SINK mode
Disable: 1.8KΩ DDC pull-up, DDC Outputs, +5V Output
455
Start 0.5 second HPD Timer
YES
NO
HPD Timer expired?
YES
47KΩ pull-up on SCL?
NO
480
485
460
HPD detected?
NO
YES
475
Disable 1.8KΩ DDC pull-up resistors
465
Operate as a source device (SOURCE mode)
Enable: 1.8KΩ DDC pull-up resistors
Read: EDID
YES
HPD detected?
NO
470

FIG. 4B

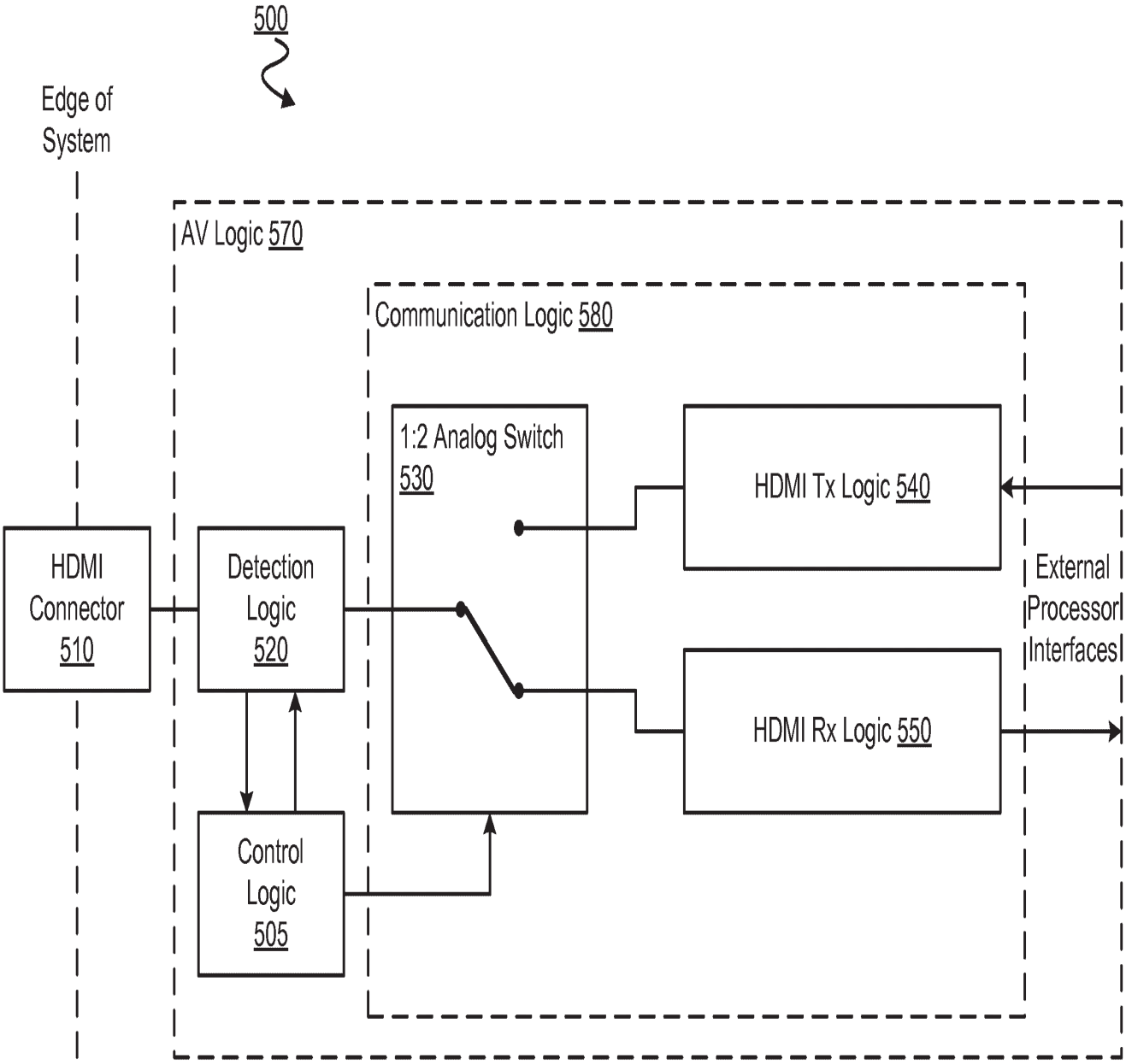

500
Edge of System
AV Logic 570
Communication Logic 580
1:2 Analog Switch 530
HDMI Tx Logic 540
HDMI Connector 510
Detection Logic 520
External Processor Interfaces
HDMI Rx Logic 550
Control Logic 505

FIG. 5

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE
First Named Inventor/Applicant Name:	Conrad Arlo Maxwell
Filer:	Dermot G. Miller/Julie Dussault
Attorney Docket Number:	8029P107

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	380	380
Utility Search Fee	1111	1	620	620
Utility Examination Fee	1311	1	250	250
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1250**

Electronic Acknowledgement Receipt

EFS ID:	12418162
Application Number:	13434273
International Application Number:	
Confirmation Number:	7248
Title of Invention:	METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE
First Named Inventor/Applicant Name:	Conrad Arlo Maxwell
Customer Number:	65702
Filer:	Dermot G. Miller/Julie Dussault
Filer Authorized By:	Dermot G. Miller
Attorney Docket Number:	8029P107
Receipt Date:	29-MAR-2012
Filing Date:	
Time Stamp:	16:43:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1250
RAM confirmation Number	3845
Deposit Account	022666
Authorized User	

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Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		SIMG0383_0395_8029P107_Application.pdf	160492 f18a43e32b09b1ae210ed7ca43c2a0623faa898c	yes	32

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	25
Claims	26	31
Abstract	32	32

Warnings:

Information:

2	Drawings-only black and white line drawings	SIMG0383_0395_8029P107_Figures.pdf	59797 1ed8ece3344d12029b2877fa6a3db41996daafa7	no	7

Warnings:

Information:

3	Fee Worksheet (SB06)	fee-info.pdf	33523 48cee780550cd11ea2ff2d1a531e1b6428b61752	no	2

Warnings:

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	12418162
Application Number:	13434273
International Application Number:	
Confirmation Number:	7248
Title of Invention:	METHOD, APPARATUS AND SYSTEM FOR TRANSITIONING AN AUDIO/VIDEO DEVICE BETWEEN A SOURCE MODE AND A SINK MODE
First Named Inventor/Applicant Name:	Conrad Arlo Maxwell
Customer Number:	65702
Filer:	Dermot G. Miller/Julie Dussault
Filer Authorized By:	Dermot G. Miller
Attorney Docket Number:	8029P107
Receipt Date:	29-MAR-2012
Filing Date:	
Time Stamp:	16:43:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1250
RAM confirmation Number	3845
Deposit Account	022666
Authorized User	

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Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		SIMG0383_0395_8029P107_Application.pdf	160492 f18a43e32b09b1ae210ed7ca43c2a0623faa898c	yes	32

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	25
Claims	26	31
Abstract	32	32

Warnings:

Information:

2	Drawings-only black and white line drawings	SIMG0383_0395_8029P107_Figures.pdf	59797 1ed8ece3344d12029b2877fa6a3db41996daafa7	no	7

Warnings:

Information:

3	Fee Worksheet (SB06)	fee-info.pdf	33523 48cee780550cd11ea2ff2d1a531e1b6428b61752	no	2

Warnings:

Information:

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New International Application Filed with the USPTO as a Receiving Office

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