Powering ICs On and Off

Modern integrated circuits employ sophisticated circuits to ensure that they turn on in a known state, preserve memory, boot quickly, and conserve power when they are powered down. This two-part article provides tips for using power-on reset and power-down functions.

Power-On Reset

By Miguel Usach Merino

Introduction

The power-on reset (POR) circuit included in many ICs guarantees that the analog and digital blocks initialize in a known state after the power supply is applied. The basic POR function generates an internal reset pulse to avoid race conditions and keep the device static until the supply voltage reaches a threshold that guarantees correct operation. Note that this threshold voltage is not the same as the minimum power-supply voltage shown in the data sheet. Once the supply reaches the threshold voltage, the POR circuit releases the internal reset signal and the state machine initializes the device. Until initialization is complete, the device should ignore external signals, including transmitted data. The only exception is the reset pin, which, if included, would be internally gated with the POR signal. A POR circuit can be represented as a window comparator, as shown in Figure 1. The comparator level, V_{T2}, is defined during the circuit design depending on the device's operational voltage and process geometry.

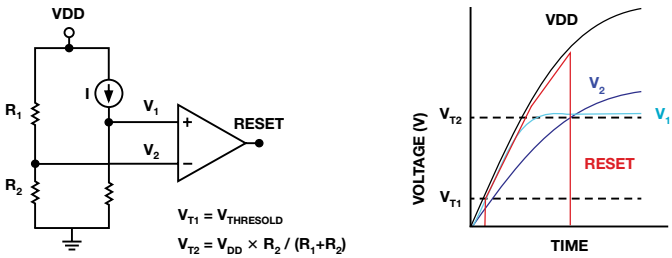

Figure 1. Simplified POR circuit.

POR Strategy

The comparator window is typically defined by the digital supply level. The digital block controls the analog block, and the voltage required for the digital block to be fully functional is similar to the minimum voltage required for the analog block to function, as shown in Figure 2.

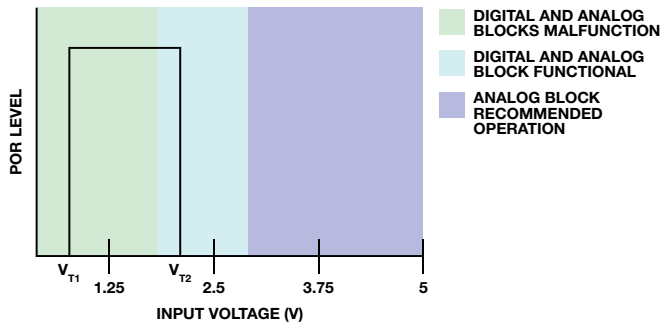

Figure 2. POR threshold voltages.

A higher threshold for V_{T2} is better for the analog block, but making it too close to the minimum recommended supply voltage could inadvertently trigger a reset if the voltage drops slightly. If the device includes separate analog and digital supplies, a strategy to avoid malfunctions is to add a second POR circuit that keeps both blocks reset until the supply voltage is high enough to ensure functionality. For example, in a 3-V IC process, $V_{T1} \approx 0.8$ V and $V_{T2} \approx 1.6$ V.

These voltages can change depending on the process and other design variations, but these are reasonable approximations. The threshold tolerance can be 20% or more; some old designs had up to 40% tolerance. The high tolerance is related to power consumption. The POR must be enabled all of the time, so the ever-present trade-off between accuracy and power consumption is important, as higher accuracy will make the circuit dissipate more power in standby mode without making a real difference in functionality.

Brownout Detector

The POR circuit sometimes integrates a brownout detector (BOD), which avoids malfunction by preventing a reset if the voltage drops unexpectedly for only a short time. From a practical perspective, the brownout circuit adds hysteresis, typically around 300 mV, to the threshold voltages defined in the POR block. The BOD guarantees that once the supply falls above V_{T2}, the POR will not generate a reset pulse unless the supply drops below a different threshold, V_{BOD}, as shown in Figure 3.

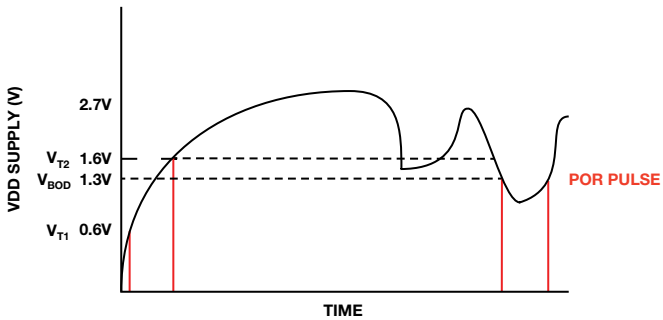

Figure 3. Brownout detector.

The brownout threshold level is high enough to guarantee that the digital circuit retains the information, but is not high enough to guarantee functionality. This allows the controller to halt activity if the supply drops below some level, without requiring the device to be reinitialized if the supply level drops for a limited amount of time.

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Correct Device Power Up

Practical POR circuits are more complex than the simple version shown in Figure 1; using MOS transistors in place of resistors, for example. Thus, parasitic models must be considered. Also, the POR circuit requires a start-up block to generate the start pulse, and this could fail under some conditions. Other important considerations are described in the following paragraphs.

It is important to use a monotonic power supply, as a nonmonotonic ramp could cause a problem if the deviation is close to any threshold level. The high threshold variation can cause the same nonmonotonic sequence to work in one unit, but fail in others, as shown in Figure 4.

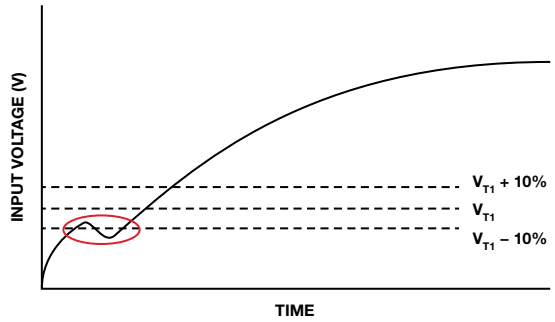

Figure 4. Nonmonotonic supply ramp.

Sometimes, even when the supply is disconnected (LDO disabled), storage capacitors retain some residual voltage, as shown in Figure 5. This voltage should be kept as small as possible to guarantee that the supply drops below V_{T1} or the POR will not reset correctly and the device will not initialize correctly.

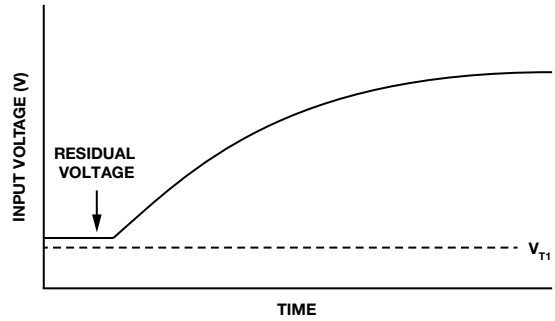

Figure 5. Residual voltage.

Some data sheets define the recommended supply sequence that should be applied to devices that have more than one supply pin. It is important that this sequence be followed. For example, consider a device with two independent supplies. The recommended supply sequence states that the digital supply must be powered before the analog supply (this is common, as the digital block controls the analog block so it must be powered first). The sequence states that the block must be initialized first. It does not matter which supply starts to ramp first, but the digital supply must cross the threshold before the analog supply, as shown in Figure 6. If the delay between supplies is on the order of 100 µs, the impact should be minor and the device should initialize correctly.

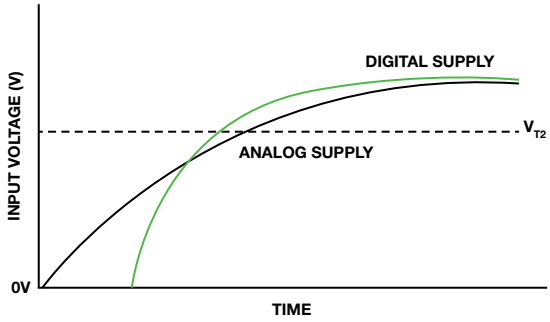

Figure 6. Recommended supply sequence.

Due to internal transistor parasitics, slow supply ramps, on the order of 100 ms, can cause problems. The POR circuit is evaluated at various slew rates to guarantee correct operation within normal power conditions. The data sheet will state whether a fast supply ramp (100 µs or less) is required.

A poor ground connection, for example, from a board connected to the supply with a thin cable, will have a high ground impedance, which could generate glitches during power up. In addition, in some electromagnetic environments (EME), the parasitic gate capacitance of the MOS transistor can charge, causing the transistor to malfunction until the capacitance is discharged. This could cause a failure in the POR initialization.

Drift and tolerance need to be considered as well. In some cases, discrete components such as capacitors have high tolerances—up to 40%—and high drift vs. temperature, voltage, and time. In addition, the threshold voltages have a negative temperature coefficient. For example, V_{T1} could vary from 0.8 V at room temperature to 0.9 V at –40°C and 0.7 V at +105°C.

Conclusion

This article describes some common problems when powering a board that could cause system problems, and provides basic rules to guarantee correct board initialization. The supply is often overlooked, but both its final voltage accuracy and its transitional behavior are important.

References

"*Insight into digiPOT Specifications and Architecture Enhances AC Performance*." *Analog Dialogue*, Volume 45, Number 3.

Power Off or Power Down?

By Dushyant Juneja

"Power down, of course!" those alarmed by the question would exclaim. Others might wonder about the difference between the two proposals. Power-down modes often promise memory retention, shorter boot up time, and ultralow leakage current, while turning off or gating the power does none of these things. But what if these features are not needed? Would the designer be wasting power by keeping the supplies stable and using the power-down mode? Can't we reduce the leakage current by simply shutting off the power? Are there any basic, underlying requirements for power-down modes? Intrigued? Read on.

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Temptation and Risk

Modern systems bloom with a rich set of features, achieved through multiple levels of design complexity that often encompass more than one chip. Power is a concern for many applications such as portable medical devices, so these chips often include one or more power-down modes. These modes provide features such as memory retention, peripheral usage, and fast turn-on, all while drawing minimal supply current. An alternative is to do a complete power shutdown. This tactic completely cuts the power supplied to the chip, not allowing any current flow to its supply pins. This reduces the power dissipation, but not without serious side effects.

Consider the example of a complex system comprising multiple chips connecting through a multiplexed bus. If the system is intended for a power-constrained application, it might seem lucrative to simply shut off power to a chip that is not currently being used, especially if the other features offered by power-down modes are not required. Shutting off the supplies reduces the leakage current, but without supplies, the pins can act as low-impedance nodes to incoming signals, resulting in unpredictable operation and potential system-level threats. Tempting as the power-cut option may be, power-down modes offer a fundamental advantage for complex systems: they keep the individual chips in known, desirable states and maintaining safe, reliable operation even as the chip cycles between low-power and high-performance modes. The details can be shown by looking at an I/O node.

A Simple Example

The pin in Figure 7 connects to a multiplexed node, with its operation set by a verified system architecture. As an I/O pin, it has both input and output functions.

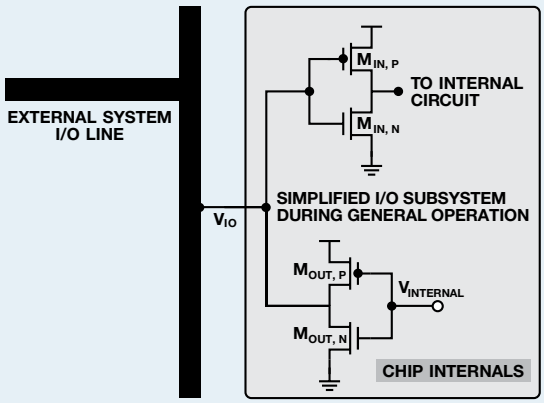

Figure 7. Simplified I/O circuit.

Disregarding issues with the device used for the power switch, turning off the supplies for this chip (assuming that none of the chip operations are required) would lead to the situation shown in Figure 8, with unknown states scattered throughout the chip core. In the worst case, the floating gate output devices (M_{OUT}, p and M_{OUT}, n) could be exposed to unexpected external voltages while they are electrically asleep. With a CMOS I/O, as shown in this example, this could lead to a low-impedance connection to ground via the drain connection of the NMOS (highlighted in red). A high current would ensue, possibly maxing out the drive capacity of the previous stage, causing damage to the MOS circuit in the chip, or both. If it did not damage the system, it could still decrease its performance.

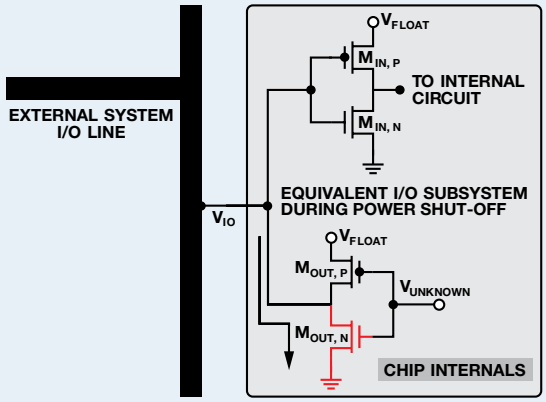

Figure 8. I/O circuit in power-cut mode. Note the unknown state of the internal gates.

Power-Down Mode

Power-down modes equip the chip with an extra layer of protection against these undesired operating conditions. The implementation differs for different modes, product families, and vendors, but the essential focus is providing a safe I/O boundary while the core of the chip sleeps, maintaining a known, dependable, low-power state. The advantage is that I/O operations between system components, with a system-wide multiplexed bus, for example, do not pose a threat to the sleeping device. One implementation could put the I/O pins in a high-impedance state during low-power mode, allowing the internal nodes connecting to the boundary pin to be in a well-defined state. A simplified implementation is shown in Figure 9. Signals will have no impact on the internal circuit, keeping them intrinsically safe. Other implementations, such as light-sleep modes might keep the I/O periphery powered up as well, while ensuring that the interaction between the chip's peripherals and core are verified during power-down mode. This enables the chip to handle active use situations, while keeping power consumption low. In addition, this system reduces the cost of the power switch, which would otherwise need to be a large, low-resistance device that would consume significant leakage and on-state power.

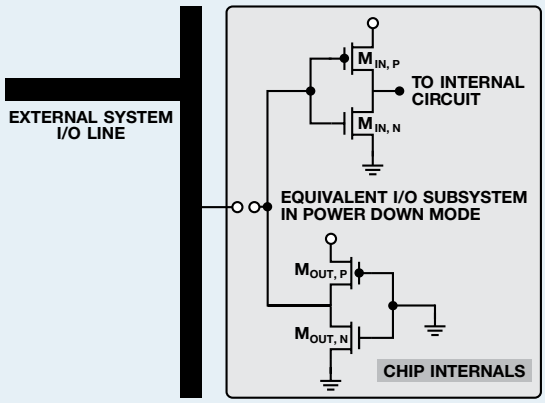

Figure 9. I/O circuit in power-down mode. Note that all internal nodes are well defined.

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Power-down modes vary from chip to chip and vendor to vendor, so names such as "light-sleep mode" might not always mean the same thing. Some of these enable memory retention, while others might permit an increased number of interrupts or other similar features. One prominent advantage of these modes is reduced system response time, as compared to full-power shutdown. Some circuits provide separate I/O and core supplies. One advantage of this decoupling is that the board designer can shut off the core supplies to reduce leakage, while keeping the I/O powered. It is always advisable to get the exact details from the data sheet to ensure that the required features and protection methods are supported.

Effect of Shrinking Geometries

Modern IC process technologies offer higher density packaging as a natural consequence of reduced device sizes, making optimal use of power-down modes increasingly important. This also reduces the stress handling capacity of the device, however. For instance, a 28-nm device has a thinner gate oxide than its 180-nm technology counterpart. Thus, the stress applied by the gate voltage in power-cut mode would be more likely to rupture the smaller device. In addition, layout dependent parameters could also cause catastrophic failures in smaller geometry devices.

All of these effects make power-down modes increasingly desirable for modern devices. Packed with features, the modern chip comprises of millions of devices, each of which can contribute to the leakage current when kept on. Optimizing feature usage and powering down unused parts of the chip can save a major portion of this leakage. Make sure that the vendor supports these modes explicitly though, rather than trying to develop your own power-down capability.

A Few More Situations

The power-down puzzle has more pieces. What if we cut the ground connection as well, since that opens another low-impedance path? This is similar to an ESD situation where I/O pins are forced directly without enabling supplies, and if the signal strength is sufficient, it might trigger the ESD protection structure, causing high currents to flow through other connected I/O pins and creating a false power-up situation. A more probable case is a signal that is somewhat weaker, but still powerful enough to reach the supplies through a path, such as the I/O clamp. The signal may not be able to trigger the supply clamp, but could create unexpected ghost voltages on the supplies, which could cause unknown states of operation depending on the topology of the chip. In either case, if the situation persists, the chip might be damaged, unless the previous stage has already stopped supplying high current. If the signal strength is not sufficient to trigger the I/O clamp, it still might stress the first transistor it encounters, possibly damaging it after prolonged operation.

How about disconnecting the supplies and pulling the supply inputs low? Now the chip has no floating supplies and no chance of triggering any ESD structure, but the PMOS drain can reach a higher voltage than the body, forward biasing the drain-to-body diode. The current from the preceding stage would then flow through the PMOS device to ground until the device burns out, the previous stage gives up, or the designer notices the alarm.

Conclusion

Power-down modes result in a faster, safer system-wide response, making them an indispensable feature, especially when looking at the full signal chain in complex systems. Complete power cutoff could be considered if interactions between components are limited, or the system as a whole is simple enough to ensure no complications occur.

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Volume 45, Number 3

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