

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

DELL INC., DELL TECHNOLOGIES INC., HP INC., and LENOVO (UNITED STATES) INC.

Petitioners

v.

UNIVERSAL CONNECTIVITY TECHNOLOGIES INC.,

Patent Owner.

DECLARATION OF JAMES WEBB

Case No. IPR2024-01480

Mail Stop Patent Board
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

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TABLE OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 9,852,103 (“the ’103 Patent”)
1002	Prosecution history of the ’103 Patent
1003	Declaration of James Webb
1004	Curriculum Vitae of James Webb
1005	U.S. Patent Publ. No. 2007/0201492 to Kobayashi
1006	U.S. Patent No. 8,799,537 (“Zhu”)
1007	Declaration of William Lempesis
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1009	U.S. Patent No. 5,974,464 (“Shin”)
1010	U.S. Publ. No. 2013/0266154 (“McCormack”)
1011	Excerpts from Newton’s Telecom Dictionary, 12 th Ed. (1997)
1012	U.S. Patent No. 4,486,739 (“Franaszek”)
1013	Exhibit K to UCT’s First Amended Infringement Contentions in <i>Universal Connectivity Technologies Inc. v. Dell Technologies Inc. and Dell Inc.</i> , No. 1:23-CV-01506-RP (W.D. Tex.)
1014	U.S. Patent Publ. No. 2014/0019653 (“Amchislavsky”)
1015	Declaration of Nathaniel E. Frank-White of the Internet Archive

Exhibit No.	Description
1016	Maxim Application Note 3524, “Efficient Bit-Banged SPI Port for 8051-Compatible Microcontrollers” (June 8, 2015)
1017	Muller and Niesler, “Development of a USB Telephony Interface Device for Speech Recognition Applications,” <i>Southern African Telecommunication Networks and Applications Conference (SATNAC) 2005 Proceedings</i> , Vol. 1 at 487-492 (2005).
1018	Halder et al., “Implementation of MCU Invariant I2C Slave Driver Using Bit Banging,” <i>ICONS 2011: The Sixth International Conference on Systems</i> (2011).
1019	Aly et al., “Scalable ZigBee-Based Smart Authentication and Access Control System Design Using XMOS Programmable Chips,” <i>International Journal of Scientific & Engineering Research</i> , Vol. 2, Issue 9 (September 2011).
1020	U.S. Patent App. Publ. No. 2012/0146989
1021	U.S. Patent App. Publ. No. 2013/0174208 (“Lee”)
1022	U.S. Patent App. Publ. No. 2005/0209808
1023	U.S. Patent No. 8,235,294
1024	U.S. Patent No. 7,652,752

Exhibit No.	Description
1025	U.S. Patent No. 7,973,566
1026	U.S. Patent No. 8,680,777
1027	U.S. Patent App. Publ. No. 2012/0142032
1028	U.S. Patent No. 7,356,789
1029	U.S. Patent No. 6,496,546
1030	U.S. Patent No. 9,210,010 (“Whitby-Strevens”)
1031	U.S. Patent Prov. App. No. 61/979,483 (“the ’103 Provisional Application”)
1032	DisplayPort Standard, Version 1, Revision 2 (“DisplayPort 1.2”) and October 8, 2010 Errata Version 1

LISTING OF CHALLENGED CLAIMS

Claim 1	
1[p]	1. A method of transmitting data over a multimedia link, comprising:
1[a]	over a first physical channel of the multimedia link: sending forward units of data from a source device to a sink device during one or more first time periods, the forward units of data comprising video data and forward data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data;
1[b]	receiving backward units of data at the source device from the sink device during one or more second time periods, the backward units of data comprising backward data compliant with the first standard; and

1[c]	over a second physical channel of the multimedia link distinct from the first physical channel: sending control data from the source device to the sink device.
Claim 2	
	2. The method of claim 1, further comprising sending a first synchronization signal of a first length after sending a first forward unit of data of the forward units of data, and before sending another forward unit of data from the source device.
Claim 3	
	3. The method of claim 2, further comprising sending a second synchronization signal of a second length longer than the first synchronization signal to initialize communication over the first physical channel before sending the first forward unit of data.

Claim 10	
	10. The method of claim 1, further comprising receiving control data from the sink device to the source device over the second physical channel of the multimedia link distinct from the first physical channel.
Claim 11	
11[p]	11. A method of transmitting data over a multimedia link, comprising:
11[a]	over a first physical channel of the multimedia link: receiving forward units of data from a source device by a sink device during one or more first time periods, the forward units of data comprising video data and forward communication data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data;

11[b]	sending backward units of data from the sink device to the source device during one or more second time periods, the backward units of data comprising backward communication data compliant with the first standard; and
11[c]	over a second physical channel of the multimedia link distinct from the first physical channel: receiving control data from the source device to the sink device.
Claim 12	
	12. The method of claim 11, further comprising receiving a first synchronization signal of a first length after receiving a first forward unit of data of the forward units of data, and before receiving a second forward unit of data from the source device.
Claim 13	
	13. The method of claim 12, further comprising detecting a second synchronization signal of a second length longer than the first synchronization signal to initialize communication over the first physical channel before receiving the first forward unit of data.

Claim 17	
	17. The method of claim 11, further comprising aligning a boundary of a symbol in a first forward unit of data of the forward units of data using the first synchronization signal.
Claim 20	
	20. The method of claim 11, further comprising sending control data from the sink device to the source device over the second physical channel of the multimedia link distinct from the first physical channel.
Claim 21	
21[p]	21. A source device for communicating data with a sink device over a multimedia link, comprising:

21[a]	a transmitter coupled to a first physical channel of the multimedia link and configured to send forward units of data from the source device to the sink device over the first physical channel during one or more first time periods, the forward units of data comprising video data and forward data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data;
21[b]	a receiver coupled to the first physical channel and configured to receive backward units of data at the source device from the sink device over the first physical channel during one or more second time periods, the backward units of data comprising backward data compliant with the first standard; and
21[c]	a control signal transceiver coupled to a second physical channel of the multimedia link distinct from the first physical channel and configured to at least send control data from the source device to the sink device over the second physical channel.

Claim 22

22[a]	22. A non-transitory computer readable storage medium storing instructions thereon, the instructions representing a digital design of a circuit comprising:
22[b]	a transmitter coupled to a first physical channel of the multimedia link and configured to send forward units of data from a source device to a sink device over the first physical channel during one or more first time periods, the forward units of data comprising video data and forward data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data;
22[c]	a receiver coupled to the first physical channel and configured to receive backward units of data at the source device from the sink device over the first physical channel during one or more second time periods, the backward units of data comprising backward data compliant with the first standard; and

22[d]	a control signal transceiver coupled to a second physical channel of the multimedia link distinct from the first physical channel and configured to at least send control data from the source device to the sink device over the second physical channel.
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I. INTRODUCTION

1. My name is James Webb. I have prepared this Declaration in connection with the Petition for *Inter Partes* Review of U.S. Patent No. 9,852,103 (“the ’103 Patent”) (EX1001) by Dell Inc. and Dell Technologies Inc. (collectively, “Dell”), HP Inc. (“HP”), and Lenovo (United States) Inc. (“Lenovo”) (collectively, “Petitioners”), which is to be filed concurrently with this Declaration.

2. In the course of preparing this Declaration, I reviewed the ’103 Patent, its prosecution file history, as well as the other documents discussed in this Declaration.

3. I have expertise in communications in general and, specifically, in high-speed video including connectivity standards such as, for example, DisplayPort.

4. I have been retained by Dell on behalf of the Petitioners as an expert in the fields of display technology, specifically video interfaces using analog and digital circuit design. I have been asked to provide my opinion regarding the state of the art of the technology described in the ’103 Patent and on the patentability of the claims of this patent. I am being compensated at my normal consulting rate for my time. My compensation is not dependent on and in no way affects the substance of my statements in this Declaration. I have no financial interest in Petitioners, the ’103 Patent, or the owner of the ’103 Patent.

II. BACKGROUND AND QUALIFICATIONS

5. My professional qualifications, experience, publications, and presentations, as well as a list of previous cases in which I have provided expert testimony, are outlined in my *Curriculum Vitae* (EX1004).

6. After graduating from the University of Colorado, Boulder, with a degree in Applied Math from the engineering school in Boulder, CO, I researched Ionospheric and Magnetospheric properties on radio communications at the National Bureau of Standards, wintering in 1970 at McMurdo Station, Antarctica [NBS 69-71]. Since then, I have focused my career on consumer product design. Products that can be made effectively in high volume, including the first hand-held pocket calculators [Commodore 1972-75], communication controllers-modems for remote industrial data collection [Data Pathing Inc. 75-76] and the Hubble Telescope [Ball 77-78], computer displays, and factory automation [Data Ray 78-86, Display Labs 86-00].

7. At Display Labs, my team and I licensed our IP in custom product designs and chips for international companies, including SONY, Samsung, Sampo, and LG Philips. I am a listed inventor on more than two dozen US and international patents, covering the now ubiquitous laptop keyboard switch, computer displays, and factory automation vision systems.

8. After down-sizing my company [2000], I consulted for and represented various companies at VESA [2002 – 2010]. While working with Genesis Microchip in their new product development and marketing department, I proposed “desktop-express,” a computer interface to unify and replace USB, SATA, HDMI, and DVI, connecting computer peripherals of all kinds. This effort was refocused on creating a “royalty-free” computer video interface that became the VESA DisplayPort Standard. I served as VESA Display Systems Standards Committee chair, responsible for and actively contributing to task groups: E-EDID, EDDC, Display-ID, MDDI, DisplayPort, Net2Display, MCCS, DDC/CI, and as vice chair of the board in 2008-2009.

III. DOCUMENTS AND MATERIALS CONSIDERED

9. In forming my opinions, I have considered the materials cited in this Declaration and the documents and things that I have obtained or that have been provided to me, as listed in the Table of Exhibits, in addition to my knowledge, education, training, and experience.

10. I reserve the right to supplement or amend this Declaration if additional information that affects my opinions becomes available.

IV. RELEVANT LEGAL PRINCIPLES

11. I am not an attorney and offer no opinions on the law. Counsel has informed me of legal standards that apply to the issue of patent validity. I have applied these standards in arriving at my conclusions.

A. Burden of Proof

12. I understand that in an *inter partes* review the petitioner has the burden of proving unpatentability by a preponderance of the evidence. I understand this standard is different from the standard that applies in a district court, where I understand a challenger bears the burden of proving invalidity by clear and convincing evidence.

B. Invalidity Based on Anticipation

13. I understand that a patent claim is invalid based on anticipation if a single prior art reference discloses all of the features of that claim in a way that enables one of ordinary skill in the art to make and use the invention. I further understand that anticipation applies if each of the claim features is present in the prior art reference, whether expressly or inherently. I understand that even if a prior art reference does not expressly disclose a feature, if the prior art necessarily functions in accordance with or necessarily includes a claim's feature, then that prior art inherently discloses that feature. I have relied on this understanding in expressing the opinions set forth below.

14. I understand that a prior art reference describes the claimed invention if it either expressly or inherently describes each and every feature set forth in the claim; *i.e.*, in determining whether a single item of prior art anticipates a patent claim, one should take into consideration not only what is expressly disclosed in that item, but also what is inherently present as a natural result of the practice of the system or method disclosed in that item.

15. I understand that to establish inherency, the evidence must make clear that the missing descriptive matter is necessarily present in the item of prior art and, that it would be so recognized by persons of ordinary skill in the art. I also understand that prior art use of the claimed patented invention that was accidental, unrecognized, or unappreciated at the time of filing can still be an invalidating anticipation.

16. I understand that although multiple prior art references may not be combined to show anticipation, additional references may be used to interpret the allegedly anticipating reference and shed light on what it would have meant to those skilled in the art at the time of the invention. These additional references must make it clear that the missing descriptive matter in the patent claim is necessarily present in the allegedly anticipating reference and that it would be so recognized by persons of ordinary skill in the art.

C. Invalidity Based on Obviousness

17. I understand that a patent may not be valid even though the invention is not identically disclosed or described in the prior art if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art in the relevant subject matter at the time the invention was made.

18. I understand that obviousness must be tested as of the time the invention was made. I understand that the test for obviousness is what the combined teachings of the prior art references would have suggested, disclosed, or taught to one of ordinary skill in the art.

19. To determine if a claim is obvious, the following factors shall be considered: (1) the level of ordinary skill in the art at the time the invention was made; (2) the scope and content of the prior art; (3) the differences between the claimed invention and the prior art; and (4) secondary considerations, including evidence of commercial success, long-felt but unsolved need, unsuccessful attempts by others, copying of the claimed invention, unexpected and superior results, acceptance and praise by others, independent invention by others, and the like.

20. For example, I understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an obviousness analysis need not seek out

precise teachings directed to the specific subject matter of the challenged claim because a court can take account of the inferences and/or creative steps that a person of ordinary skill in the art would employ.

21. I understand that the following rationales may be used to determine whether a piece of prior art can be combined with other prior art or with other information within the knowledge of one of ordinary skill in the art:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Predictable use or combination of prior art elements according to their established functions;
- Use of known techniques to improve similar devices (methods or products) in the same way;
- Applying a known technique to a known device (method or product) ready for improvement to yield predictable results;
- “Obvious to try” - choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;
- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; or
- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

22. I understand that when a work is available in one field of endeavor, design incentives and/or other market forces, for example, can prompt variations of it, either in the same field or a different one. Moreover, if a person of ordinary skill can implement a predictable variation, I understand this likely bars its patentability.

23. I understand that another factor to be considered is common sense. For example, I understand that common sense teaches that familiar items may have obvious uses beyond their primary purposes, and, in many cases, a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle.

24. I understand that the Supreme Court articulated additional guidance for obviousness in its *KSR* decision. My understanding is that the Supreme Court said that technical people of ordinary skill look for guidance in other solutions to problems of a similar nature, and that the obviousness inquiry must track reality, and not legal fictions. I have relied on these understandings in expressing the opinions set forth below.

25. I understand that a new use of an old product or material cannot be claimed as a new product; the apparatus or system itself is old and cannot be patented. I further understand that, in general, merely discovering and claiming a new benefit to an old process cannot render the process newly patentable.

D. Claim Interpretation

26. I understand that for purposes of my analysis in this *inter partes* review proceeding, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning.” In determining the ordinary and customary meaning, the words of a claim are given their plain meaning that those words would have had to a person of ordinary skill in the art (“POSITA”). I understand that the so-called “intrinsic record,” which includes the patent’s claims, specification, and file history, informs claim terms’ plain meaning. Moreover, “extrinsic evidence” such as treatises and dictionaries may be used, albeit under limited circumstances, to determine the meaning attributed by a POSITA to a claim term at the time of filing. I have followed this approach in my analysis, and for all of the claim terms considered in this declaration, I have applied the plain and ordinary meaning of those terms.

27. I also understand that the words of the claims should be interpreted as a POSITA would have interpreted them at the time the alleged invention was made (not today). I have been asked to use the priority date of April 14, 2014.

28. I further understand that claims may be drafted in independent or dependent form. I understand that an independent claim is a standalone claim that contains all the limitations necessary to define an invention. I understand that a dependent claim must refer to a claim previously set forth and must further limit that

claim. I further understand that a claim in dependent form incorporates by reference all the limitations of the claim to which it refers—that is, a dependent claim includes all limitations of the claim to which it references, plus any additional limitations recited in the dependent claim.

V. SUMMARY OF THE '103 PATENT

A. Brief Description

29. The '103 Patent relates to “half-duplex bidirectional transmission of data compliant with a first standard (e.g., Universal Serial Bus (USB) standard) over a physical channel of a multimedia link for transmitting audio/video (‘A/V’) data compliant with a second standard (e.g., Mobile High-Definition Link (MHL)) between a source device and a sink device using time division multiplexing (TDM).” EX1001 at Abstract; *see also id.* at 1:17-19. According to the '103 Patent, prior art USB links did not provide the speed required to transmit high-definition video data according to standards such as MHL or High-Definition Multimedia Interface (HDMI). In contrast, such prior art video standards purportedly did not provide for bidirectional USB transmission. *Id.* at 1:21-47. The '103 Patent purports to solve this problem by providing methods and apparatuses for transmitting, over an A/V physical channel of a multimedia link between a source device and a sink device, both video data and USB data in the forward direction and USB data in the backward direction. *See id.* at 3:20-37. In particular, the data may be transmitted over the A/V

physical channel in a half-duplex manner, in which forward and backward data are transmitted respectively during non-overlapping time periods. *Id.* The claimed embodiments also include a second bidirectional physical channel for sending and/or receiving control data between the source and sink. *See, e.g.,* '103 Patent at claims 1 and 10.

30. As shown in Fig. 1 of the '103 Patent, an embodiment includes a source device 110 and a sink device 120. *Id.* at 3:50-53.

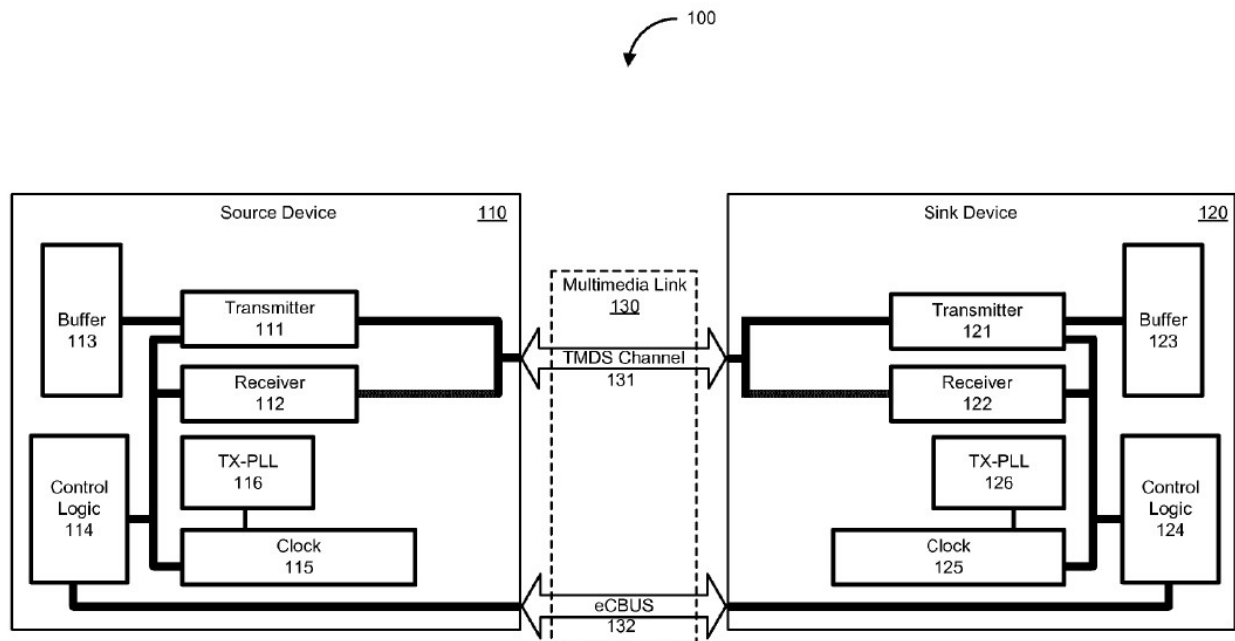


FIG. 1

31. The source and sink are connected by a multimedia link 130, including an A/V channel (e.g., Transition Minimized Differential Signaling (TMDS) Channel 131) and a bidirectional channel for control data (e.g., eCBUS 132). *Id.* at 3:60 – 4:14. Source device 110 includes a transmitter 111 for encoding and sending packets

of A/V and USB data from the source to the sink over TMDS channel 131 and a receiver 112 for receiving and decoding USB data received from the sink over TMDS channel 131. *Id.* at 4:21-43. Similarly, sink device 120 includes a transmitter 121 that sends USB data over TMDS channel 131 to the source device 110 and a receiver 122 that receives both USB data and A/V data over the TMDS channel. *Id.* at 5:3-17. Transmitters 111 and 121 may also encode and transmit, and receivers 112 and 122 may also receive and decode, control data over eCBUS 132. *Id.* at 4:21-43.

32. Although the disclosed embodiments are described with reference to a modified version of the MHL standard, the '103 Patent explains that the same principles can be applied to other standards including HDMI standards, Digital Visual Interface (DVI) standards, and DisplayPort standards. *Id.* at 3:53-59.

33. Figure 2 of the '103 Patent illustrates half-duplex TDM transmission of USB and A/V in the forward direction and USB data in the reverse direction over the A/V physical channel.

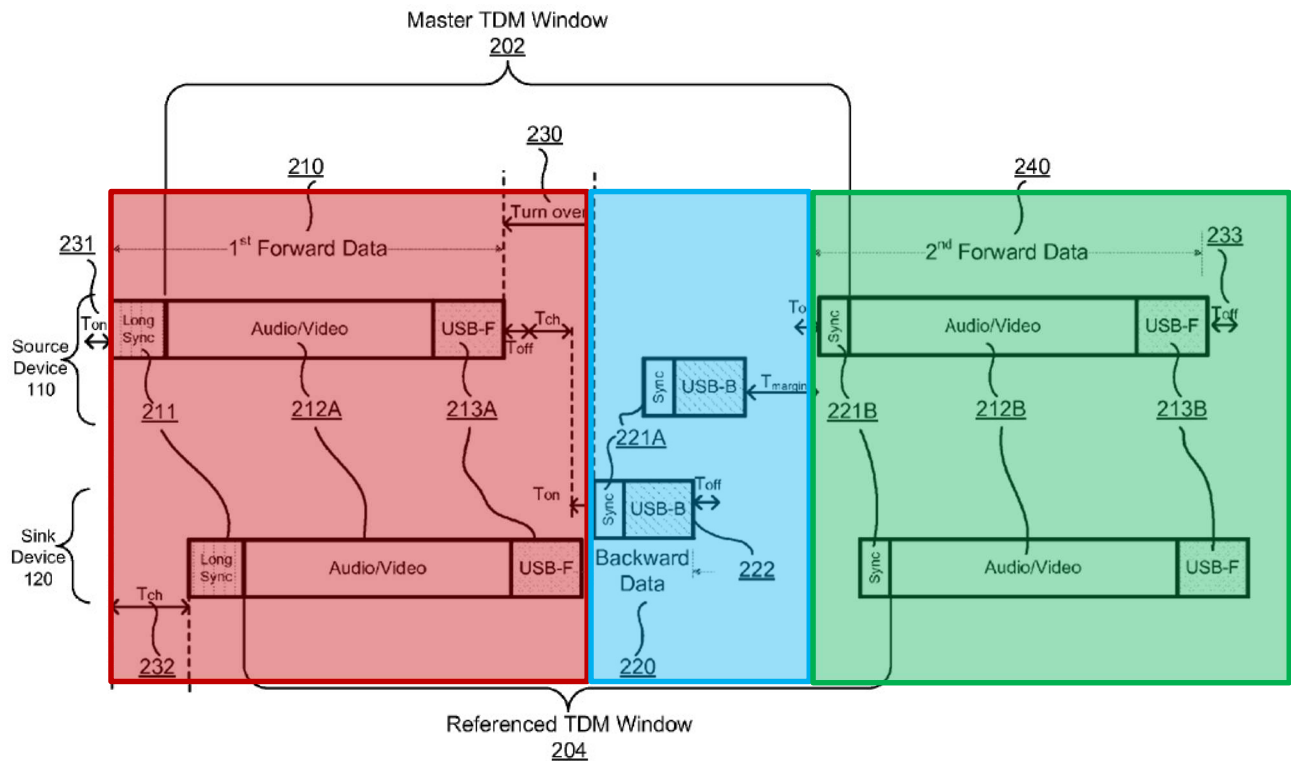


FIG. 2

34. In particular, during a first time period for forward transmission (red box in annotated Fig. 2, above), the first forward data packet 210, including long synchronization signal 211, A/V data 212A, and USB-forward data 213A, is transmitted by the source and received by the sink over the A/V physical channel. *Id.* at 5:19-6:4; Fig. 5; 7:64 – 8:8. Long synchronization signal 211 initializes communication between the source and sink. *Id.* at 5:52-54.

35. During a second time period for backward transmission (blue box in annotated Fig. 2, above), the sink device may transmit a backward data packet 220, including short synchronization signal 221A (including character symbols used to

synchronize clock and align symbol boundaries), and USB-backward data 222, to the source device over the A/V physical channel. *Id.* at 6:5-21, Fig. 5, 8:14-26.

36. Second forward data packet 240, which is sent during a subsequent time period for forward transmission (green box in annotated Fig. 2, above), is similar to first forward data packet 210, except that it starts with a short synchronization signal 221B. *Id.* at 6:22-27.

A. Summary of the Prosecution

37. I have reviewed the prosecution history of the '103 Patent.

38. On April 8, 2015, the '103 Patent was filed as Application No. 14/681,992 (“the '992 Application”) entitled “Bidirectional Transmission of USB Data Using Audio/Video Data Channel.” *See* EX1001. The '992 Application claims priority to Provisional Application No. 61/979,483, filed on April 14, 2014, and lists twenty-four claims. EX1002 at 25. The original applicant was Silicon Image, Inc. EX1002 at 1.

39. During prosecution of the '992 Application, the PTO issued one non-final office action on April 10, 2017. EX1002 at 81. In the office action, the Examiner rejected claims 1-24 as anticipated by U.S. Patent Publ. No. 2007/0201492 to Kobayashi. EX1002 at 84-88. In response, the Applicant amended the claims to specifically require that the recited “first standard” is a USB standard and argued only that Kobayashi teaches sending video data over a channel (“main link 222”)

that is distinct from an auxiliary channel over which USB data is communicated, whereas the claims required that USB data be sent and received over the same physical channel used to send video data. EX1002 at 99-106. Representative amended claim 1 is reproduced below.

1. **(Currently Amended)** A method of transmitting data over a multimedia link, comprising:
 - sending a first unit of data from a source device to a sink device over a first physical channel of the multimedia link during a first time, the first unit of data comprising video data and forward data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data;
 - receiving a second unit of data by the source device over the first physical channel of the multimedia link during a second time, the second unit of data comprising backward data compliant with the first standard; and
 - sending control data from the source device to the sink device over a second physical channel of the multimedia link distinct from the first physical channel.

EX1002 at 99. Applicant did not dispute the Examiner's mapping of Kobayashi to any other elements, including the Examiner's argument that signals sent during link training and/or link setup and management in Kobayashi satisfy the first and second synchronization signals recited in various claims. EX1002 at 85; EX1005 at [0071], [0079], and [0086].

40. The Examiner entered an amendment and allowed claims 1-6, 8-14, and 16-24 on August 25, 2017. EX1002 at 117-125. Exemplary claim 1 as amended by

the examiner is reproduced below. The amendments appear to clarify that unidirectional video data and bidirectional USB are communicated over the same “first physical channel.”

1. **(Currently Amended)** A method of transmitting data over a multimedia link, comprising:

over a first physical channel of the multimedia link:

sending ~~a first~~ forward units of data from a source device to a sink device

~~over a first physical channel of the multimedia link during [[a]]~~

one or more first time periods, the ~~first forward~~ units of data comprising video data and forward data compliant with a first

standard comprising a universal serial bus (USB) standard and different from a standard of the video data;

receiving ~~a second~~ backward units of data ~~by~~ at the source device from the

sink device ~~over the first physical channel of the multimedia link~~

during [[a]] one or more second time periods, the ~~second backward~~ units of data comprising backward data compliant with the first

standard; and

over a second physical channel of the multimedia link distinct from the first physical channel:

sending control data from the source device to the sink device ~~over a~~

~~second physical channel of the multimedia link distinct from the~~

~~first physical channel.~~

EX1002 at 118-119.

VI. LEVEL OF ORDINARY SKILL IN THE ART

41. In my opinion, a person of ordinary skill in the art (POSITA) working with this technology, would have had a bachelor’s degree in electrical engineering,

computer engineering, computer science, or equivalent training, and three years of experience with data communications systems or interfaces, including at least some experience with serial or display data communications systems or interfaces. Additional education can substitute for less work experience, and vice versa.

VII. OVERVIEW OF THE PRIOR ART

A. Zhu (EX1006)

42. U.S. Patent No. 8,799,537 (“Zhu”) was filed as U.S. Application No. 13/461,761 on May 1, 2012 and issued on August 5, 2014.

43. Zhu discloses the same idea as the ’103 Patent except that, instead of modifying the MHL standard, it modifies the DisplayPort Standard, Version 1, Revision 2 (“DisplayPort 1.2”) to allow bidirectional USB transmission over the A/V link. EX1001 at 3:53-59 (stating that the principles described in the ’103 Patent apply equally to DisplayPort).

44. Zhu discloses a system and method in which a “first device may be configured to transmit, on a DisplayPort link to the second device, a data flow comprising both USB protocol data and uncompressed high definition media data signals [and t]he devices may be configured such that the USB protocol data is transferred from the second device to the first device during a video blanking period associated with the uncompressed high definition media data signals.” EX1006 at Abstract. Figure 35c in particular illustrates a “mixed mode” in which source device

3405 is “configured to transmit a data flow including both USB protocol data and uncompressed high definition media data to the sink device” 3415 and the sink device is configured to send USB data to the source. *Id.* at 33:63 – 34:38. Figure 35c illustrates the combined forward USB / video data flow as 3530 and the backward USB data flow as 3550. EX1006 at 34:48-51.

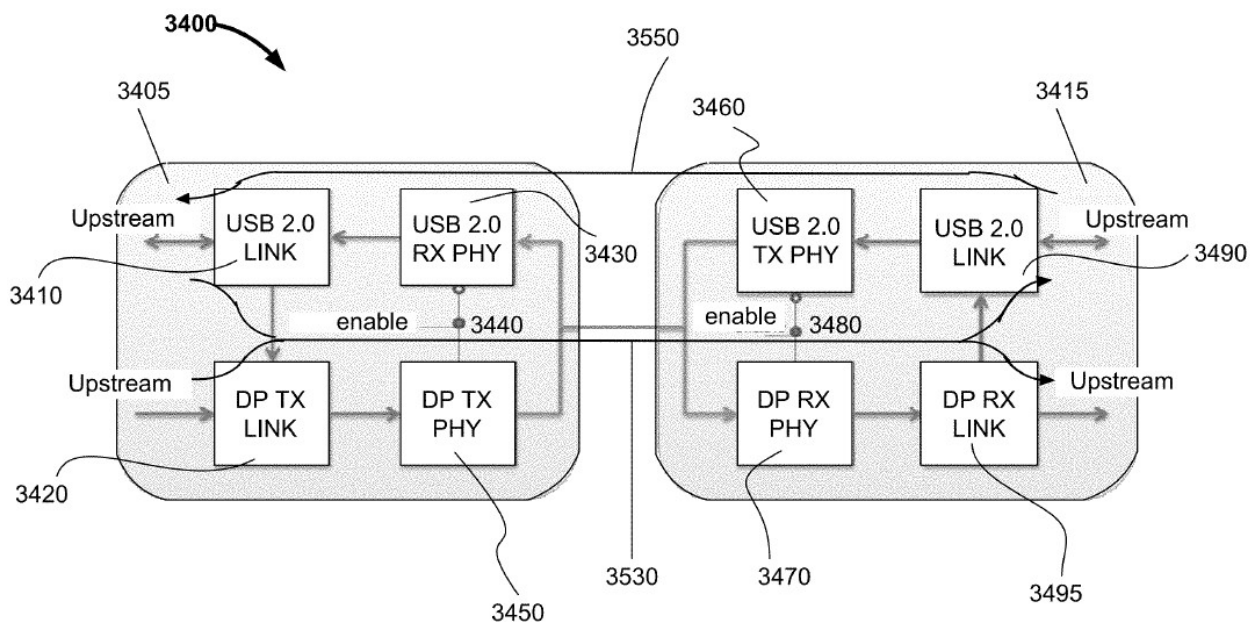


FIG. 35c

45. Like the '103 Patent, Zhu teaches that transmission on the link is half-duplex such that forward and backward data flows occur at different times. *Id.* at Fig. 41, 34:1-38, 35:58 – 36:17. USB and video data may be sent from source to sink when DP TX PHY 3450 of source device 3405 and DP RX PHY 3470 of sink device 3415 are enabled, *Id.* at 34:3-10; 34:47-51. As illustrated in Figure 37, a USB data packet is included in the forward data stream with the VC (virtual channel) video

data payload in a packet (MTP) of the DisplayPort 1.2 multi-stream transport (MST) protocol. *Id.* at 34:52-61; 35:35-44.

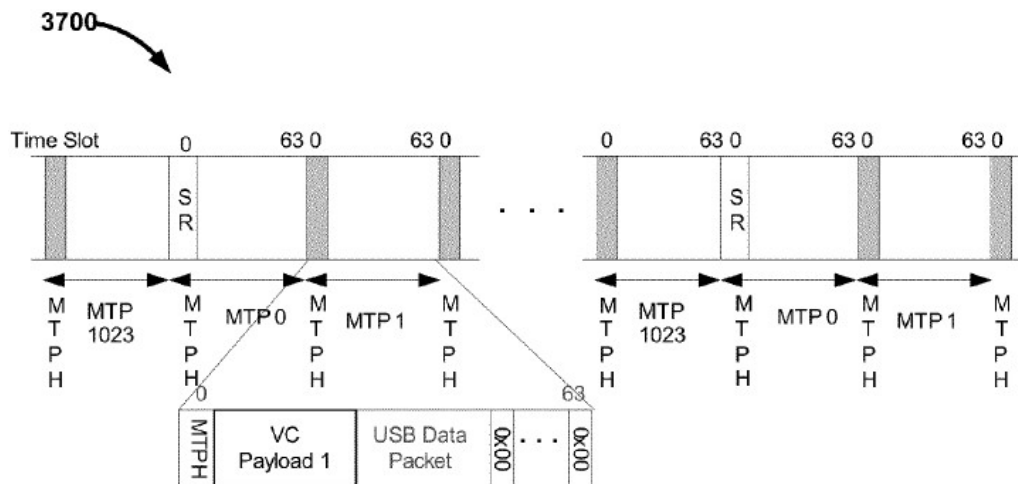


FIG. 37

46. At other times, such as a video blanking period, USB 2.0 TX PHY 3450 of sink device 3415 and USB 2.0 RX PHY 3430 of source device 3405 are enabled and USB data may be sent from the sink to the source. *Id.* at 34:25-31; 34:47-51.

47. Zhu also discloses a second physical channel for bidirectional communication of control data—in particular, a “two way serial communication side-band channel.” *See id.* at 1:52-57, 5:6-11. The side-band channel may be formed by conductors that carry the various control channels defined in DisplayPort (including, e.g. AUX). *Id.* at 34:39-41. Alternatively, the side-band channel may be a single control bus known as the C-wire that consolidates one or more of the DisplayPort control functions. *Id.* at 5:6-11, 7:28-35.

A. DisplayPort 1.2 (EX1032)

48. Display Port Version 1, Revision 2 (“DisplayPort 1.2”) is a version of the DisplayPort standard developed by the Video Electronics Standards Association (“VESA”). DisplayPort 1.2 was published on January 5, 2010, before the Priority Date. *See, e.g.*, EX1032 at 1; EX1007, ¶¶1-6.

49. DisplayPort 1.2 was well known to POSITAs before the Priority Date. The ’103 Patent itself refers to “a DisplayPort standard” (EX1001 at 3:53-59) and prior art patents refer explicitly to DisplayPort 1.2. *See* EX1006 at 1:42-47; EX1020 at [0008]. Before the Priority Date, interested members of the public would have been aware of DisplayPort 1.2, would have known where to locate a copy, and could have accessed a copy from VESA either through membership in VESA or via the VESA website for a fee. EX1007, ¶¶6-10. I was a contributor throughout the development of DisplayPort up to and including version 1.2, and I recall that the standard was made available in early 2010. EX1032 at 18 (listing “Jim Webb” of Luxtera as one of the “Main Contributors”). People working in the relevant industry knew about the standard and where to find it by at least that time. In the fall of 2009, while we were developing DisplayPort 1.2, I gave a seminar on its predecessor (DisplayPort 1.1) to a large group of Texas Instruments Euro engineers in Nice, France, in November of 2009.

50. Table 0-1 of DisplayPort 1.2 lists the “main contributors” to the standard. EX1032 at 17-19. In my recollection, that list includes many (if not most) of the major players in the display industry at that time. Additional players in the display industry who were not contributors to DisplayPort 1.2 were VESA members. For example, Silicon Image and Lattice Semiconductor were members at least as of March 29, 2014. EX1015 at pp. 7-8. It is my understanding that all VESA members at that time had access to the DisplayPort standards, including DisplayPort 1.2.

51. DisplayPort 1.2 “define[s] a flexible system and apparatus capable of transporting video, audio and other data between a Source Device and a Sink Device over a digital communications interface.” EX1032 at 1. In particular, DisplayPort 1.2 defines several transport channels, including a unidirectional main link for A/V data, a half-duplex bidirectional auxiliary channel (AUX) used for link management and device control, and a hot plug detect signal. *Id.* at 34.

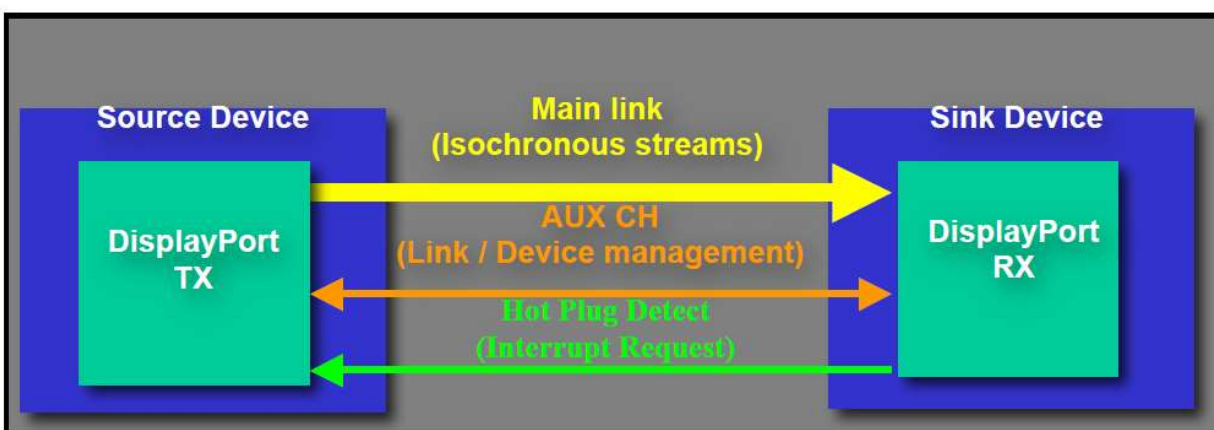


Figure 1-1: DisplayPort Data Transport Channels

52. A DisplayPort 1.2 source device includes a transmitter for transmitting A/V data over the main link, while a DisplayPort sink device includes a receiver for receiving A/V data. *Id.* at 28, 34. The source and sink devices also include a “transceiver circuit for AUX CH.” *Id.* at 28.

53. DisplayPort 1.2 teaches synchronization signals that are communicated between the source and sink devices. These include control functions defined in 8b/10b format, many of which are “comma characters.” *Id.* at 165, 353. The bit sequences of these symbols are unique and can be recognized within a contiguous bit stream of other data. This makes them useful for synchronization (as well as or necessary in channel initialization, clock recovery, and symbol boundary alignment). EX1012 at 8:39-9:36 and Table III. During DisplayPort 1.2 link training (i.e., link initialization), long strings of 8b/10b encoded control symbols (including comma characters such as K28.5) are sent as training symbols. EX1032 at 353-362.

Table 3-16: Symbol Patterns of Link Training

Pattern Number	Purpose	Name
TPS1	For locking clock recovery circuit of the DisplayPort receiver	Repetition of D10.2 characters without scrambling
TPS2	For optimizing equalization, determining symbol boundary, and achieving inter-lane alignment	K28.5-, D11.6, K28.5+, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2 without scrambling
TPS3	For optimizing equalization, determining symbol boundary, and achieving inter-lane alignment	K28.5-, K28.5+, K28.5-, K28.5+, D10.2-, D10.2-, D10.2-, D10.2-, D10.2-, D10.2-, D10.2-, D10.2-, K28.5-, K28.5+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+ without scrambling

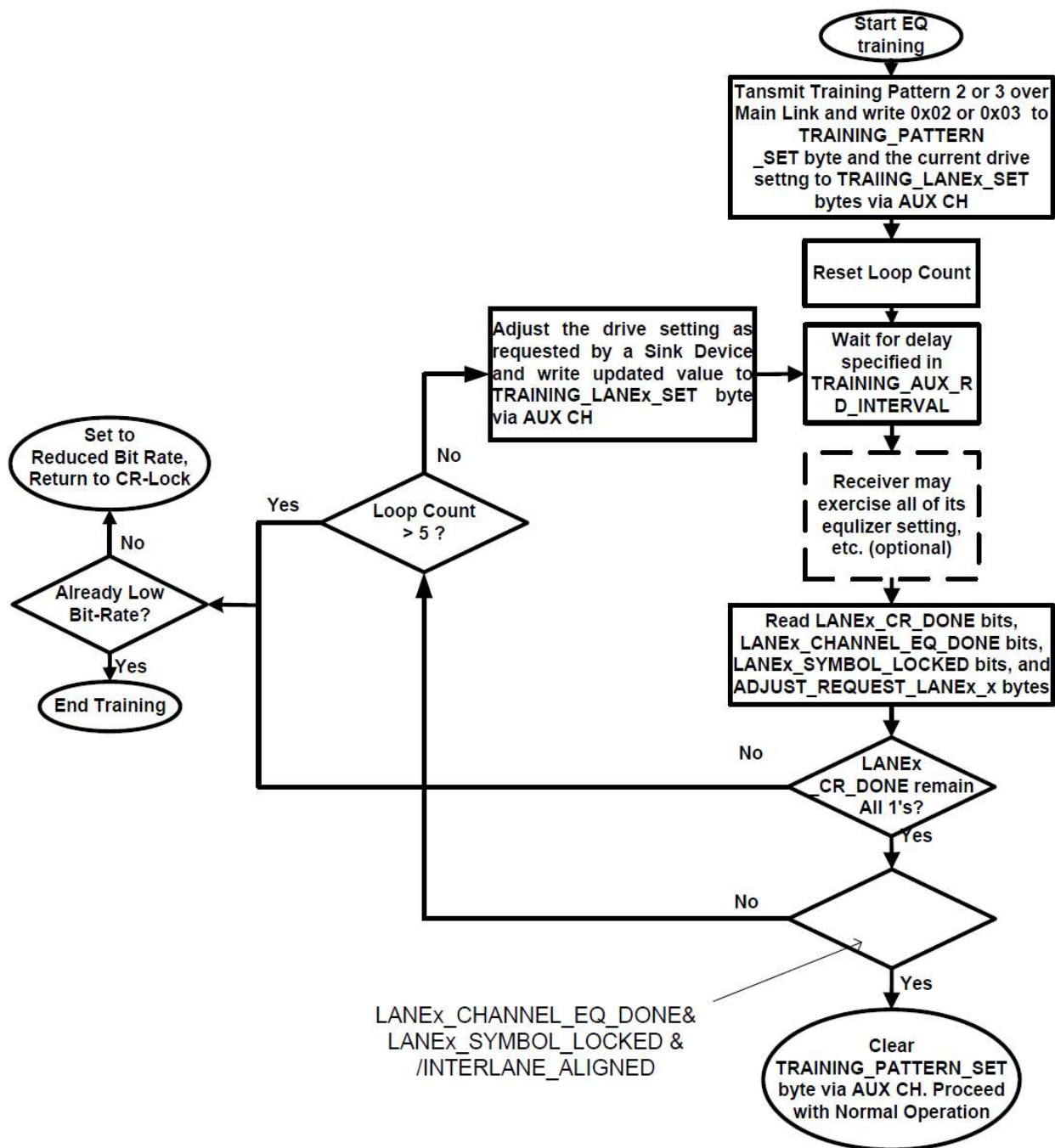


Figure 3-33: Channel Equalization Sequence of Link Training

54. Additionally, shorter groups of specific comma characters also serve as control symbols, such as blank start (BS) and scrambler reset (SR) may be sent along with data packets. EX1032 at 47-48, 165, 353.

Table 3-15: ANSI 8B/10B Special Characters for DisplayPort Control Symbols

Special Character	Control Symbol in Single Stream Enhanced Mode	Control Symbol in Multi-Stream Mode
K28.0	SR	Indexed 2
K28.1	CP	Direct RESERVED
K28.2	SS	Indexed 3
K28.3	BF	Indexed 4
K28.4	RESERVED	Direct RESERVED
K28.5	BS	Direct SR
K28.6	RESERVED	Indexed 5
K28.7	RESERVED	Direct RESERVED
K23.7	FE	Indexed 0
K27.7	BE	Indexed 1
K29.7	SE	Indexed 6
K30.7	FS	Indexed 7

Table 2-65: MTP Header Control Functions

Control Function	Code/Control Symbol Sequence³	Comment
SR (Scrambler Reset)	K28.5	Comma character; Link Frame Indicator
RESERVED	K28.1	Not used.
RESERVED	K28.7	Not used to avoid coding complication
RESERVED	K28.4	Not used for EMI reduction purpose
ACT (Allocation Change Trigger)	C0-C1-C1-C0	Trigger to downstream device indicating change in allocation on local link. ACT Control Function sequence is unique from others; its 4-code control symbol sequence spans four consecutive MTP Header time slots).

B. Lyle (EX1008)

55. U.S. Patent No. 7,558,326 (“Lyle”) was filed as U.S. Application No. 09/954,663 on September 12, 2001 and issued on July 7, 2009. Lyle was originally assigned to Silicon Image, Inc. (the original assignee of the ’103 Patent) and names at least two common inventors with the ’103 Patent.

56. Lyle discloses “a communication system including a transmitter, a receiver, and a TMDS-like link, in which video data and auxiliary data (often including timing data associated with other auxiliary data) are transmitted from the transmitter to the receiver, or in which video data are transmitted over the link from the transmitter to the receiver, and auxiliary data (often including timing data associated with other auxiliary data) are transmitted from the receiver to the transmitter (or from the transmitter to the receiver and also from receiver to the transmitter).” EX1008 at 6:25-34. The auxiliary data of Lyle may be USB data. *Id.* at 50:47-54. The TMDS link of Lyle may be half-duplex and bidirectional. For example, one or more video data transmission channels of the TMDS link may be reversed “during blanking periods (to send auxiliary data from the receiver of the video data to the transmitter of the video data).” *Id.* at 45:43-48. Lyle also discloses a separate control channel “for bidirectional communication between the transmitter and a monitor associated with the receiver in accordance with the conventional Display Data Channel standard.” *Id.* at 28:28-34.

57. Lyle specifically describes the embodiments by reference to the Digital Video Interface (DVI) standard (*id.* at 1:63-65), and the '103 Patent teaches that the principles described therein could be applied equally to DVI. '103 Patent at 3:53-59.

C. Shin (EX1009)

58. U.S. Patent No. 5,974,464 (“Shin”) was filed September 30, 1996 and issued October 26, 1999. Shin discloses a data coding system for transition-minimized signaling. In particular, as used in TMDS, Shin describes the use of multiple consecutive out-of-band synchronization characters for synchronization and symbol boundary alignment during link initialization and data transmission. *See* EX1009 at 14:36-15:28.

C. Amchislavsky (EX1014)

59. U.S. Patent Publ. No. 2014/0019653 to Amchislavsky et al. (“Amchislavsky”), filed July 1, 2012 and published January 16, 2014, is a Silicon Image patent filing relating to bidirectional communication of USB over an AV protocol link. EX1014. Like the '103 Patent, Amchislavsky describes bidirectional communication of USB over a Mobile High-definition Link (MHL) connection. As shown in Figure 13, Amchislavsky describes a link including a data channel for AV data and a separate bidirectional control channel.

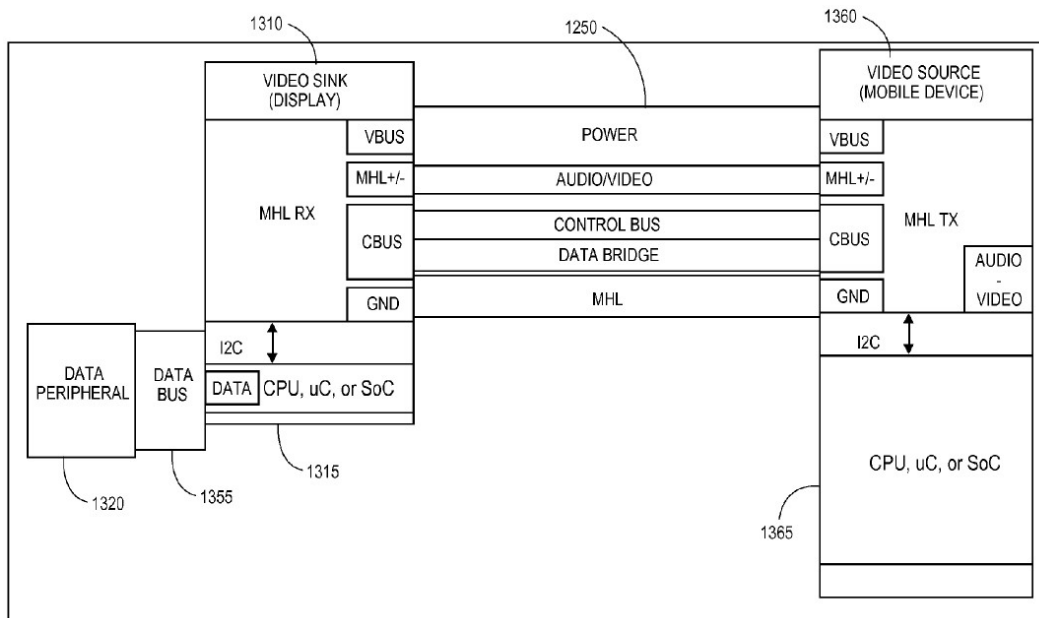


FIG. 13

60. According to Amchislavsky, the MHL “specification allows for a connector to be utilized for transmission of both MHL data and USB™ (Universal Serial Bus) data, where USB data may be transmitted when the connector is not being utilized for the transmission of MHL data” but that “such use may be limited to only one of such protocols at any time.” EX1014 at [0002]-[0003]. Amchislavsky thus describes methods and apparatus allowing, during separate time periods, bidirectional USB data transmission and unidirectional AV data transmission over an MHL link.

C. Kobayashi (EX1005)

61. Kobayashi was filed April 26, 2007 and published August 30, 2007. Kobayashi describes a system used to connect a video source to a video display unit, including a simplex (unidirectional) main link, for video data, and a bidirectional

auxiliary channel, that may be used to send and receive USB data. EX1005 at [0053],

Fig. 2A.

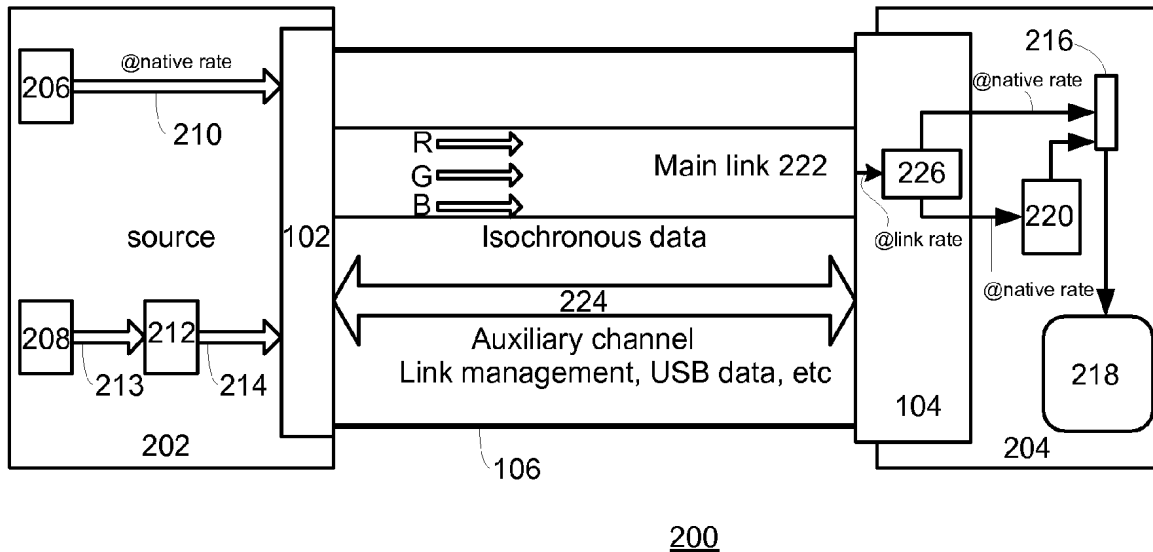


Fig. 2A

62. Kobayashi further teaches that a synchronization signal (8b/10b comma character K28.5) is “[i]nserted between packets” in the A/V data stream and included in test patterns sent as part of link training. EX1005 at [0071], [0075], Figs. 11, 13.

VIII. THERE IS A REASONABLE LIKELIHOOD THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE

63. For the reasons explained below, it is my opinion that the challenged claims are unpatentable, either as anticipated or obvious in view of the prior art.

A. Grounds 1 and 2. Claims 1, 10, 11, and 20-22 anticipated by Zhu and claims 1, 2, 10-12, and 20-22 obvious over Zhu and the knowledge of a POSITA

64. For the reasons explained below, it is my opinion that Zhu anticipates claims 1, 10, 11, and 20-22 of the '103 Patent and that Zhu, in view of the knowledge of a POSITA, renders obvious claims 1, 2, 10-12, and 20-22 of the '103 Patent.

1. Claims 1 and 11

a. “A method of transmitting data over a multimedia link, comprising:” [1.p] / [11.p]

65. In my opinion, to the extent the preamble is limiting, Zhu teaches the limitation. Specifically, Zhu discloses methods for “transmit[ting], on a DisplayPort link [from a first device] to [a] second device, a data flow comprising both USB protocol data and uncompressed high definition media data signals” and transmitting “USB protocol data . . . from the second device to the first device during a video blanking period.” EX1006 at Abstract; *see also id.* at Figs. 34, 35c, and 41; 33:20-34:51. This is shown, for example, in Figures 34 and 35c, which illustrate “system[s] that allow[] USB data transmission on a media port link.” *Id.* at 4:14-26.

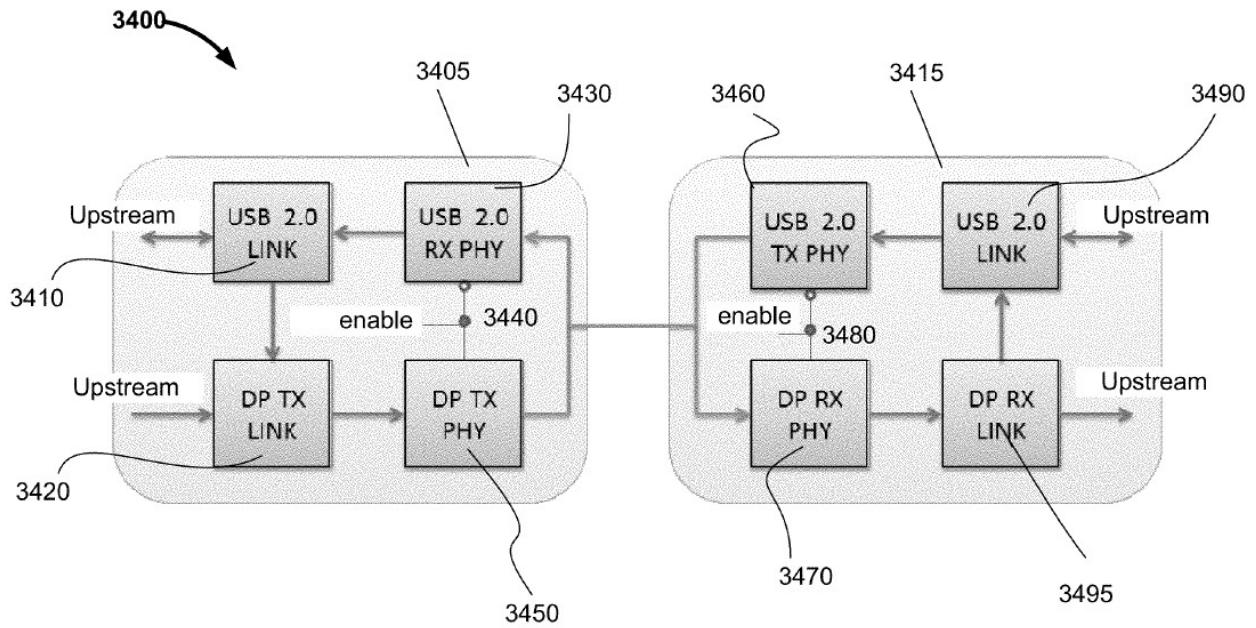


FIG. 34

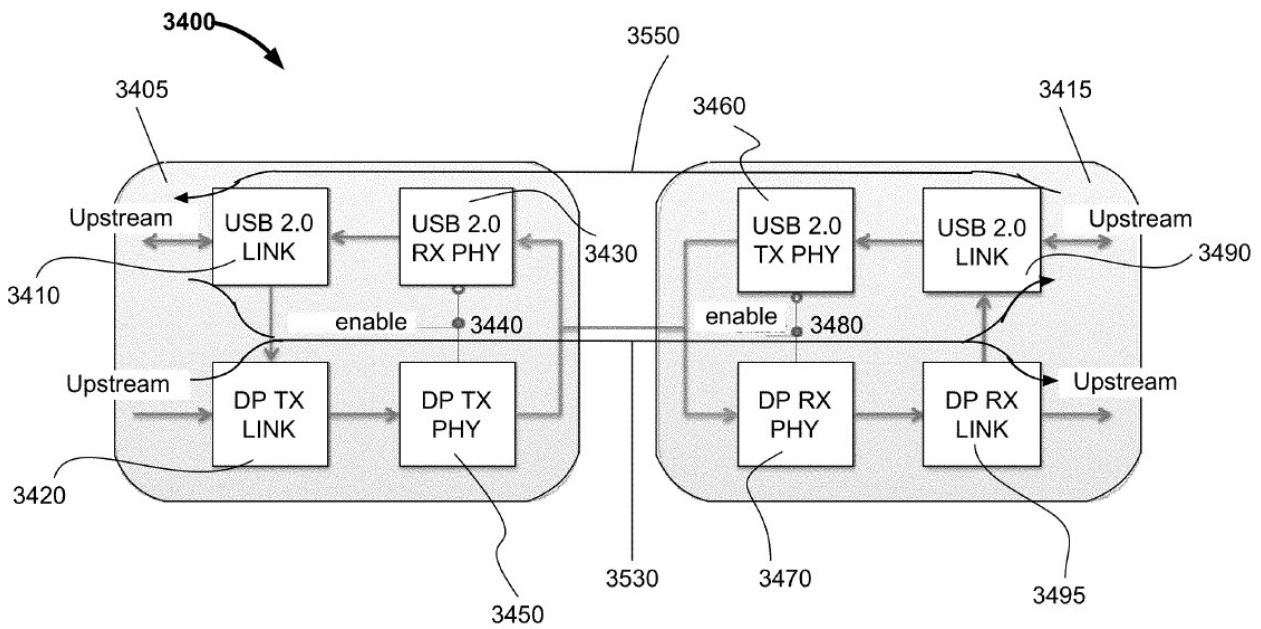


FIG. 35c

66. A DisplayPort link is a “multimedia link” as claimed. EX1006 at 5:4-6 (“The uncompressed high definition media data may comprise at least one lane of media or multimedia data in accordance with a DisplayPort standard.”), 31:38-39 (“DisplayPort defines a high-speed audio/video data transfer interface with 1 to 4 data lanes and one AUX channel”). Indeed, the ’103 Patent explicitly teaches that its “principle can be applied to . . . a DisplayPort standard.” *Id.* at 3:53-59.

b. “over a first physical channel of the multimedia link: [sending / receiving] forward units of data from a source device [to / by] a sink device during one or more first time periods, the forward units of data comprising video data and forward [communication] data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data;” [1.a] / [11.a]

67. In my opinion, Zhu teaches this limitation.

68. Of note, claims 1 and 11 are very similar and are complementary. Claim 1 recites several steps from the perspective of a source device, whereas claim 11 recites the complementary steps from the perspective of a sink device. Additionally, whereas claim 1 recites forward and backward “data compliant with” a USB standard, claim 11 recites forward and backward “communication data compliant with” a USB standard. The ’103 Patent uses the phrase “communication data” only in claim 11 (that phrase does not appear elsewhere in the patent). Moreover, the ’103 Patent does not distinguish between different types of USB data. Therefore, a POSITA would understand that “communication data compliant with” a USB

standard refers to USB data that is communicated (either sent or received) over the first physical channel.

69. Zhu discloses embodiments in which a source device sends, and a sink device receives, “a data flow comprising both USB protocol data and uncompressed high definition media data signals” over a DisplayPort Main Link data lane (*first physical channel*). EX1006 at Abstract, 31:25-27 (“A protocol to merge the USB data stream into the DisplayPort data lane(s) to more efficiently utilize the available bandwidth on the DisplayPort link is described herein.”). Zhu discloses (and in my opinion, a POSITA would understand) that a DisplayPort Main Link data lane is a single channel formed as a differential pair of wires. *See, e.g.*, EX1006 at 7:21-28 (“The signals may include at least one differential video data pair defining a lane in accordance with a DisplayPort standard.”); *see also id.* at 12:53-58. Figures 34 and 35a-c illustrate “exemplary embodiment[s] of [] systems that allows USB data transmission on a media port link.” *Id.* at 4:14-26. Figure 35c illustrates a “mixed mode” operation in which “the DisplayPort source side may be configured to transmit a data flow that includes both USB protocol data and uncompressed high definition media data to the sink device.” *Id.* at 33:63-66. “The exemplary [mixed-mode] data flow 3530 may include the DisplayPort data flow together with USB forward data flow.” *Id.* at 34:47-51.

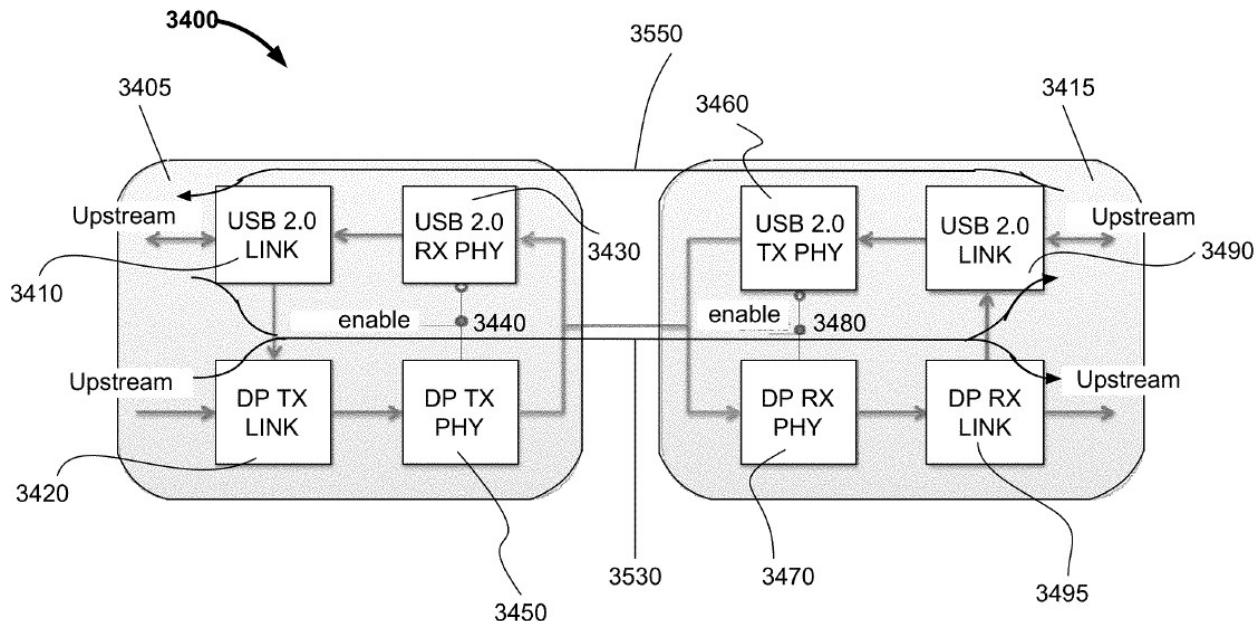


FIG. 35c

70. In this mixed mode, “the USB 2.0 transmitter data is sent to the DPTX LINK 3420 and multiplexed (muxed) together with the video data from upstream.” *Id.* at 34:11-13. Zhu explains that this can be achieved by modifying the MST protocol of DisplayPort 1.2 to insert USB data packets alongside the virtual channel (VC) payloads, which “represent[] active video pixels,” in an MTP. *Id.* at 34:13-15, Fig. 37, and 34:52-35:5. In my opinion, a POSITA would recognize that an MTP in this context is a DisplayPort 1.2 “Multi-stream Transport Packet.” *See, e.g.,* EX1032 at 120, 136. This data arrangement in which USB packet and video data payload are sent “in parallel” within an MTP (*forward units of data comprising video data and forward [communication] data compliant with a first standard comprising a*

universal serial bus (USB) standard and different from a standard of the video data) is shown in Figure 37. EX1006 at 35:38-40.

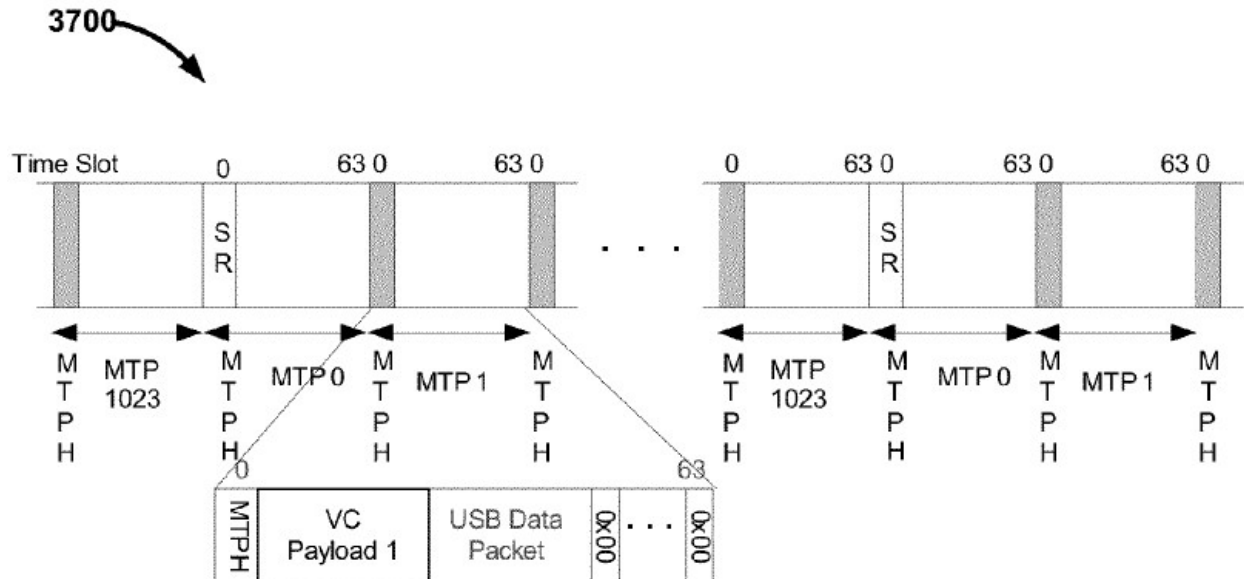


FIG. 37

71. Zhu teaches that the USB data is compliant with a USB standard, such as the USB 2.0 specification and the video data is compliant with a DisplayPort standard, such as DisplayPort 1.2. *See, e.g.*, EX1006 at 31:25-44; 33:20-29; 34:52-56; 34:62-65. USB 2.0 is different from DisplayPort 1.2.

72. In Zhu, MTPs containing DisplayPort and USB data (*forward units of data...*) are sent over the first physical channel during one or more first time periods. Zhu teaches that data is transmitted in both directions over the same link, but not at the same time. Rather, a process of “link turn-around” selectively activates (and

deactivates) the transmitters and receivers in the source and sink to ensure that data flows in only one direction at a time. EX1006 at 33:63-34:10. USB and DisplayPort data are sent in the forward direction from the source device and received by the sink device when DP TX PHY 3450 and DP RX PHY 3470 are enabled but USB 2.0 TX PHY 3460 and USB 2.0 RX PHY 3430 are disabled. *Id.* at 34:3-6. Conversely, USB data is sent in the backward direction when DP TX PHY 3450 and DP RX PHY 3470 are disabled, and USB 2.0 TX PHY 3460 and USB 2.0 RX PHY 3430 are enabled. *Id.* at 34:28-31. “The link turn-around from the forward direction to the backward direction may take place after the last active pixel of the current display line is sent and the necessary MSA/VBID/SDP is transferred, which is done in the forward direction. MSA refers to Main Stream Attribute data, VBID refers to the Vertical Blanking IDentification data packet and SDP refers to the Secondary Data Packet.” *Id.* at 34:31-38. After the backward transmission of USB data from sink to source is complete, “another link turn-around may occur. That is, the link may go from the backward direction back to the forward direction, and the link may prepare for the next video line active pixels transfer.” *Id.* at 34:41-46. Thus, Zhu teaches that the forward USB and video data are sent from the source and received by the sink during time periods when DP TX PHY 3450 and DP RX PHY 3470 are enabled but USB 2.0 TX PHY 3460 and USB 2.0 RX PHY 3430 are disabled (*first time periods*).

c. “over a first physical channel of the multimedia link: . . . [receiving / sending] backward units of data [at the source device from the sink device / from the sink device to the source device] during one or more second time periods, the backward units of data comprising backward [communication] data compliant with the first standard; and” [1.b] / [11.b]

73. In my opinion, Zhu teaches this limitation. As recited in limitations [1.a] and [11.a], the “first standard” is a USB standard. In the “mixed mode” embodiment of Figure 35c, “USB 2.0 transaction is bi-directional, so the data transfer on the link may be performed in either the forward direction or backward direction.” EX1006 at 34:1-3; *see also id.* at 34:25-26 (“In the backward direction, the USB data may be sent from DisplayPort sink side back to the DisplayPort source side.”). An example allocation of USB data packets transmitted as part of DisplayPort transfer units (“TU”) in the backward direction is illustrated in Figure 40 of Zhu:

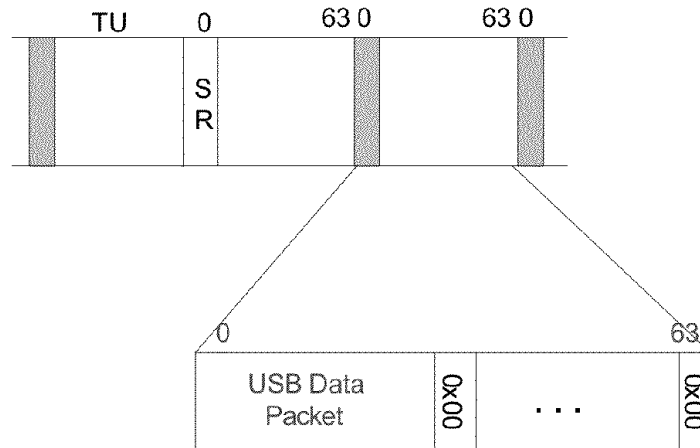


FIG. 40

See EX1006 at 35:35-44.

74. As explained in Sections VII.A and VIII.A.1.b (Grounds 1 and 2, limitations 1.a and 11.a) above, Zhu teaches that this backward transmission of USB data packets in TUs (*backward units of data comprising backward [communication] data compliant with the first standard*) occurs over the same channel (*first physical channel*) over which USB data and video data are sent in the forward direction, but during time periods when the DP TX PHY 3450 and DP RX PHY 3470 are disabled and the USB 2.0 TX PHY 3460 and USB 2.0 RX PHY 3430 are enabled (*second time periods*). *Id.* at 34:28-31. In a particular example, USB data may be communicated in the backward (i.e. sink-to-source) direction “during the video blanking period.” *Id.* at 34:27-29.

d. “over a second physical channel of the multimedia link distinct from the first physical channel: [sending / receiving] control data from the source device to the sink device.” [1.c] / [11.c]

75. In my opinion, this limitation is disclosed by or at least obvious in view of Zhu. Specifically, Zhu explains that the disclosed DisplayPort-based system includes *second physical channel* in the form of a “two-way serial communication side-band channel [] for setting up the lanes requirement and other communications on both sides[, which] may accommodate 3-wires (namely AUXP, AUXN and HPD) of communication into a single wire externally to both the devices on either side,”¹ which is distinct from the Main Link data lane used to send video and USB data (*first physical channel*). EX1006 at 5:6-17; *see also id.* at 1:67-2:3; 5:6-11; 7:21-35; 12:61-65; 20:7-57; 31:38-39. One wire of a USB connector may be assigned as the single wire for side-band information, known as the C-wire. *See, e.g.,* EX1006 at 23:10-29; 26:28-36. Figure 19 illustrates a USB connector 1910 that includes a C-wire (annotated in red, below).

¹ Notably, in the co-pending district court litigation against Dell, UCT alleges that this limitation is satisfied by a “sideband channel” in USB4. EX1013 at 40-41.

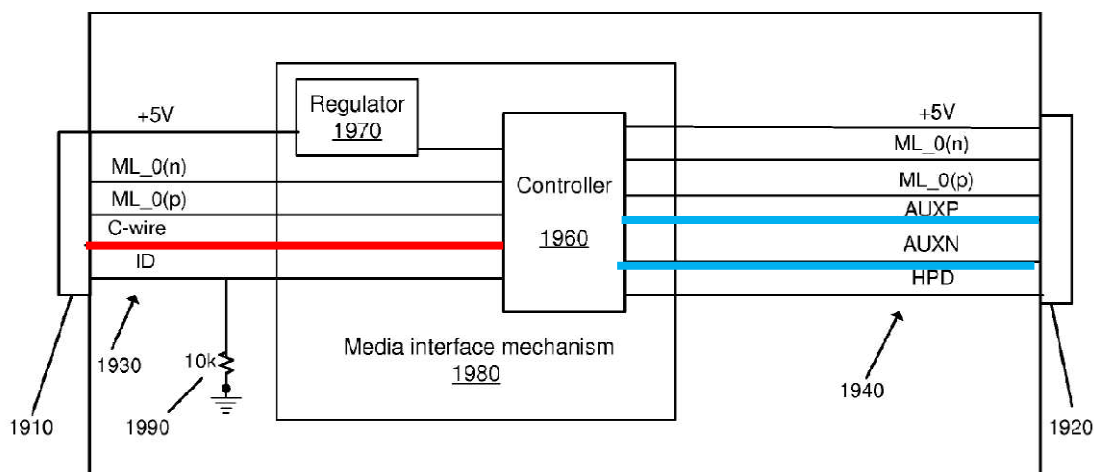


FIG. 19

76. Alternatively, the side-band information may be “communicated through the AUX channel of the DisplayPort link.” EX1006 at 34:39-41; *see also id.* at 31:36-39 and 35:60-63. Figure 19 also illustrates a media connector 1920 having a dedicated differential wire pair for the DisplayPort AUX channel (annotated in blue, above). EX1006 at 23:55-64. In my opinion, the AUX channel and C-wire are functionally equivalent.

77. Zhu explains that either or both connector types may be used at the sink and source devices of the described embodiments. EX1006 at 36:28-35 (“In various embodiments, various USB connectors and/or DisplayPort connectors, examples of which are described herein, may be used at sink and/or source device to couple to an external interface for data transfer between the devices.”). Thus, Zhu discloses that

the mixed mode embodiment of Figure 35c includes a distinct physical side-band channel in the form of either a C-wire (in the USB-type connector) or a differential AUX wire pair (in the DisplayPort-type connector).

78. Alternatively, given Zhu's explicit teaching that either connector type could be used with the disclosed embodiments, a POSITA would have at least found it obvious to implement Zhu's teaching of a distinct physical channel (C-wire or differential AUX wire pair) in connection with the mixed mode embodiment. *See* EX1006 at 36:28-32. In my opinion, this teaching and Zhu's description of DisplayPort AUX channel signals communicated as part of mixed mode operation would have at least led a POSITA to use either of the USB-type or DisplayPort-type connectors in the source and sink devices of the mixed mode embodiment of Figure 35c. *See, e.g.,* EX1006 at 34:39-41, 35:60-66. Such use would involve merely a simple substitution of one known element (either the USB-type or DisplayPort-type connector) for another (other possible connectors) to obtain predictable results and the predictable use or combination of prior art elements (one of the disclosed connectors with the source and sink devices of Figure 35c) according to their established function (providing a connection to these devices).

79. Zhu discloses that control data is sent over the side-band channel. Specifically, the two-way side-band channel is used "for device configurations on either side" and "to identify and set the correct transmission of the multimedia

content.” *Id.* at 1:52-57. The C-wire, for example, may be used to communicate data signals for various control functions, such as “plugged device type identification,” “link training,” and “downstream HDCP authentication . . . to transfer the hand shake information as defined in a DisplayPort standard specification.” *Id.* at 27:17-27; 27:34-37; 29:14-17; 29:26-29. Figures 32 and 33 illustrate request and reply transactions over the C-wire, which can include up to 16 bytes of “Data.”



FIG. 32

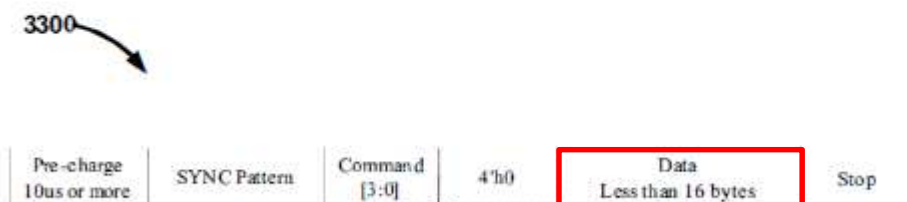


FIG. 33

EX1006 at Figs. 32-33 (annotated); *see also id.* at 26:38-27:13.

80. Zhu also teaches that “[t]he number of bytes [of USB data] to be sent in the backward direction may be precalculated and communicated through the AUX channel of the DisplayPort link.” EX1006 at 34:39-41. Moreover, the source and sink send messages to each other over the side-band channel to implement mixed-

mode link turn-around. EX1006 at 34:39-41; 35:58-66. In particular, the source may send the sink an inquiry over the AUX channel. *Id.* If the sink device sends a message to the source acknowledging its receipt of the inquiry, both devices prepare for link turn-around. *Id.* In my opinion, a POSITA would understand that the “AUX channel” described in that portion of Zhu may be implemented either as a distinct, dedicated DisplayPort AUX channel or as a C-wire that carries AUX channel signals (and potentially other control signals). EX1006 at 20:7-20 (describing C-wire), 31:36-39 and 34:39-41 (describing DisplayPort AUX channel); *see also id.* at Fig. 19.

81. A POSITA would understand that the previously discussed side-band channel signals in Zhu are “control data,” at least because they include data and are communicated for purposes of control.

2. Claims 2 and 12: “The method of claim [1 / 11], further comprising [sending / receiving] a first synchronization signal of a first length after [sending / receiving] a first forward unit of data of the forward units of data, and before [sending / receiving] [another / a second] forward unit of data from the source device.”

82. As discussed above, it is my opinion that claims 1 and 11 are anticipated by or obvious in view of Zhu and the knowledge of a POSITA. In my opinion, dependent claims 2 and 12 (which depend from claims 1 and 11, respectively) are also obvious in view of Zhu and the knowledge of a POSITA.

83. Specifically, Zhu teaches that the forward data is sent in an MTP according to the DisplayPort 1.2 MST protocol link timing scheme. EX1006 at Fig. 37, 34:52-61. As shown in Figure 37, a symbol “SR” (*first synchronization signal*) is sent periodically in the forward data stream.

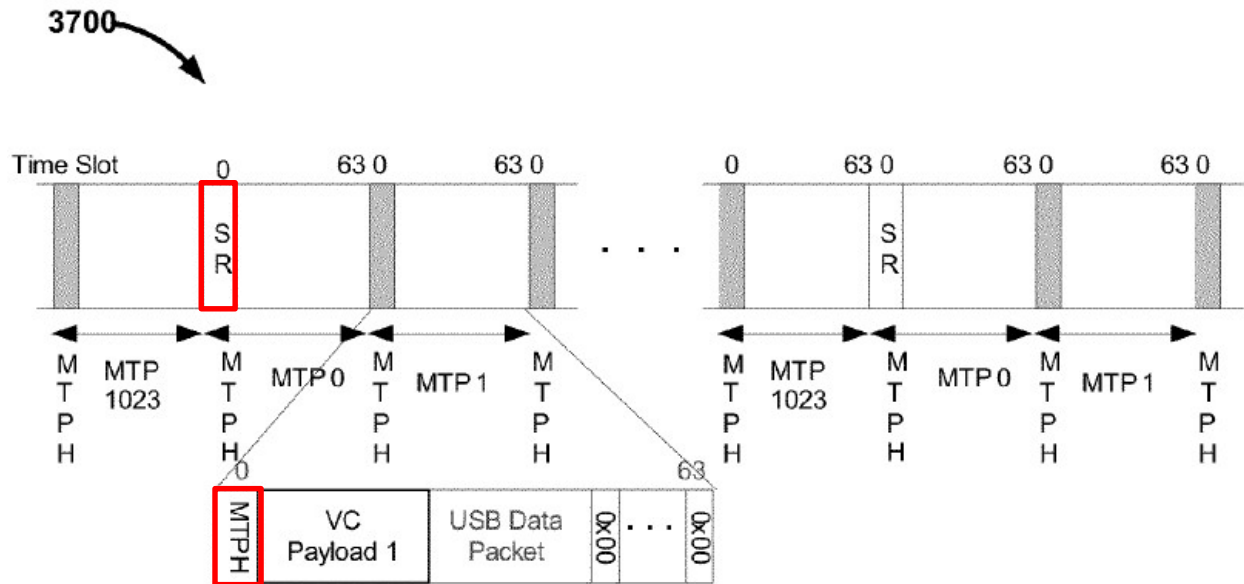


FIG. 37

EX1006 at Fig. 37 (annotated). As illustrated in Figure 37 of Zhu, SR is sent/received after one or more preceding MTPs, such as MTP 1023 (*first forward unit of data of the forward units of data*), and before one or more subsequent MTPs, such as MTP0 and MTP1 (*second / another forward unit of data*). SR has a “first length” (i.e. the length of the SR symbol).

84. In my opinion, a POSITA would understand that “SR” as used in Zhu is the DisplayPort 1.2 control function Scrambler Reset, and that SR is assigned to the comma symbol (also known as “comma character”) K28.5 in the DisplayPort 1.2 MST protocol. EX1032 at Table 2-65. It is further my opinion that a POSITA would have been familiar with 8b/10b K-codes and would have known that comma symbols (including K28.5) have special properties used for synchronization and control. This is described, for example, in the Franaszek patent. *See* EX1012 at 8:39-9:36 and Table III. Based on this knowledge, in my opinion a POSITA would have found it obvious that SR in Zhu also functions as a symbol boundary alignment synchronization signal due to its unique and particular sequence of bits within the data stream.

85. Moreover, SR is a “first synchronization signal” at least as interpreted by UCT. In the related litigation against Dell, UCT alleges that this limitation is satisfied by the “Blanking Start (BS) header” in the accused DisplayPort tunneling over USB4. EX1013 at 2 (“[E]ach accused product comprises sending a first synchronization signal of a first length as the Blanking Start (BS) header.”). Like SR, BS is a DisplayPort control symbol. EX1032 at 140. Moreover, according to the evidence cited in UCT’s infringement contentions, the BS packet is used “to indicate the beginning of a horizontal or vertical blanking period, *reset scrambler* and

transfer control information at the beginning of a blanking period,” and the following figure cited in UCT’s contentions shows that the BS header includes an SR symbol:

Figure 10-31. Blank Start Header Format



EX1013 at 3 (emphasis added).

3. Claims 10 and 20: “The method of claim [1 / 11], further comprising [receiving / sending] control data from the sink device to the source device over the second physical channel of the multimedia link distinct from the first physical channel.”

86. As discussed above, it is my opinion that Zhu discloses or renders obvious all elements of claims 1 and 11. In my opinion, Zhu also teaches the further limitations of dependent claims 10 and 20 (which depend from claims 1 and 11, respectively) and, thus, these claims are anticipated by or obvious in view of Zhu. As explained in Section VIII.A.1.d (Grounds 1 and 2, limitations 1.c and 11.c) above, Zhu discloses a distinct side-band channel (*second physical channel of the multimedia link distinct from the first physical channel*) that the source and sink use to bidirectionally communicate control data. Thus, Zhu describes receiving / sending control data from sink to source over the second physical channel.

87. As a particular example, Zhu explains that the source and sink send control data to each other over the side-band channel to implement link turn-around. EX1006 at 35:58-66; Fig. 41. After receiving an inquiry from the source regarding

whether “there is a need for a USB backward transfer,” the sink device may send, and the source device receive, an acknowledgment over the AUX channel that results in both sides preparing for link turn-around. *Id.* As explained in Section VIII.A.1.d (Grounds 1 and 2, limitations 1.c and 11.c), a POSITA would understand that the “AUX channel” described in that portion of Zhu may be implemented either as a distinct, dedicated DisplayPort AUX channel or as a C-wire that carries AUX channel signals (and potentially other control signals). It is also my opinion that a POSITA would understand that the acknowledgment sent by the sink device is link “control data.”

88. As another example, Zhu explains that the C-wire “may communicate handshake information for link training.” EX1006 at 20:48-52. A POSITA would recognize that a handshake necessarily involves bidirectional communication (and, thus, sending control data from the sink to the source).

4. Claim 21

89. As explained below, it is my opinion that claim 21 is anticipated by or obvious in view of Zhu.

a. “A source device for communicating data with a sink device over a multimedia link, comprising:” [21.p]

90. In my opinion, to the extent the preamble is limiting, Zhu teaches the limitation. Zhu discloses a source device 3405 (*source device for communicating*

data) that communicates data with a sink device 3415 (*sink device*) over the DisplayPort link (*multimedia link*).

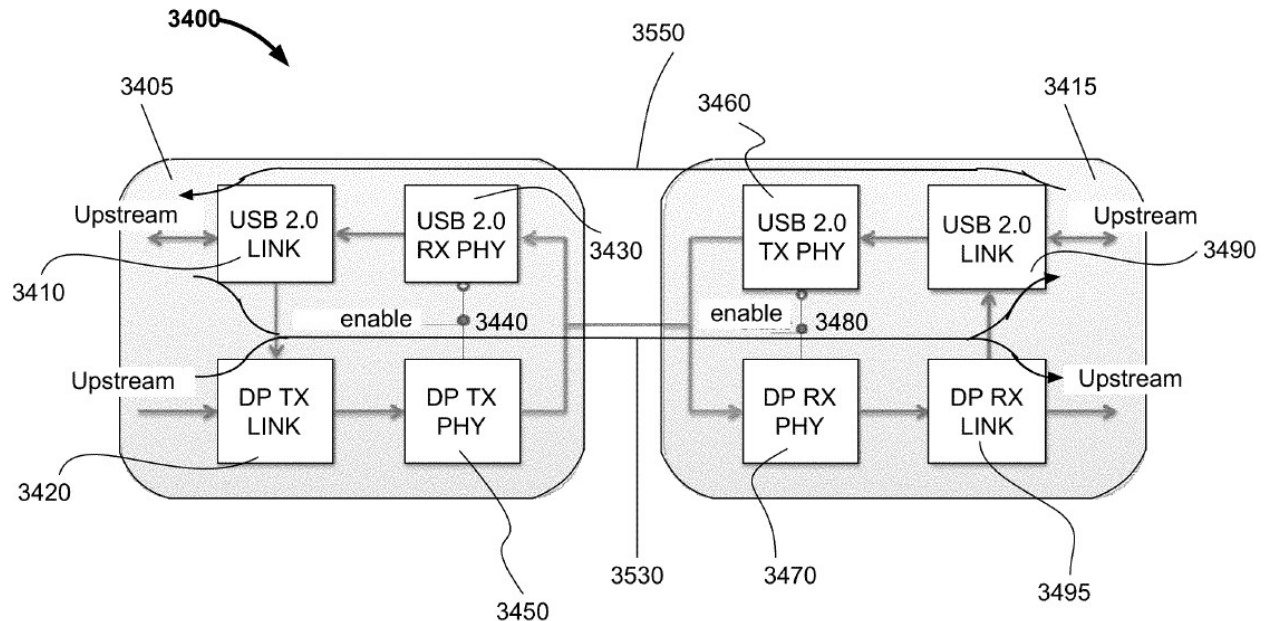


FIG. 35c

See also EX1006 at 33:63-34:24. *See also* Section VIII.A.1 (Grounds 1 and 2, claims 1 and 11), *supra*.

b. “a transmitter coupled to a first physical channel of the multimedia link and configured to send forward units of data from the source device to the sink device over the first physical channel during one or more first time periods, the forward units of data comprising video data and forward data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data;” [21.a]

91. As discussed in Section VIII.A.1.b (Grounds 1 and 2, limitations 1.a and 11.a), Zhu discloses limitation 1.a. In my opinion, Zhu also discloses limitation 21.a, which recites a “transmitter” coupled to the first physical channel and

configured to perform the function recited in limitation 1.a. Zhu discloses that the source device 3405 includes DP TX PHY 3450 and/or DP TX LINK 3420 (*transmitter*) coupled to a DisplayPort Main Link data lane (*first physical channel*), that transmits DisplayPort and USB data in the forward direction to the sink device 3415. EX1006 at 33:63-34:10; 34:47-51. *See also* Section VIII.A.1 (Grounds 1 and 2, claims 1 and 11), *supra*.

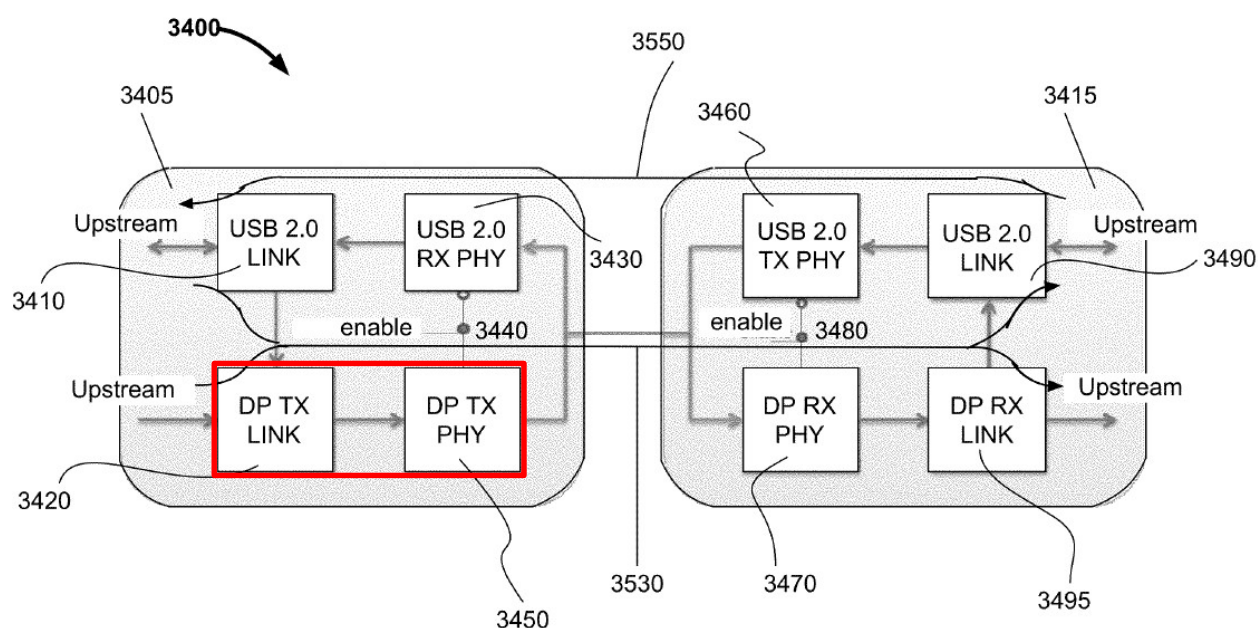


FIG. 35c

c. “a receiver coupled to the first physical channel and configured to receive backward units of data at the source device from the sink device over the first physical channel during one or more second time periods, the backward units of data comprising backward data compliant with the first standard; and” [21.b]

92. As discussed in Section VIII.A.1.c (Grounds 1 and 2, limitations 1.b and 11.b), Zhu discloses limitation 1.b. In my opinion, Zhu also discloses limitation

21.b, which recites a “receiver” coupled to the first physical channel and configured to perform the function recited in limitation 1.b. Zhu discloses that the source device includes a receiver, USB 2.0 RX PHY 3430 and/or USB 2.0 LINK 3410, coupled to the first physical channel that receives USB data in the backward direction from the sink device. EX1006 at 34:25-38. *See also* Section VIII.A.1 (Grounds 1 and 2, claims 1 and 11), *supra*.

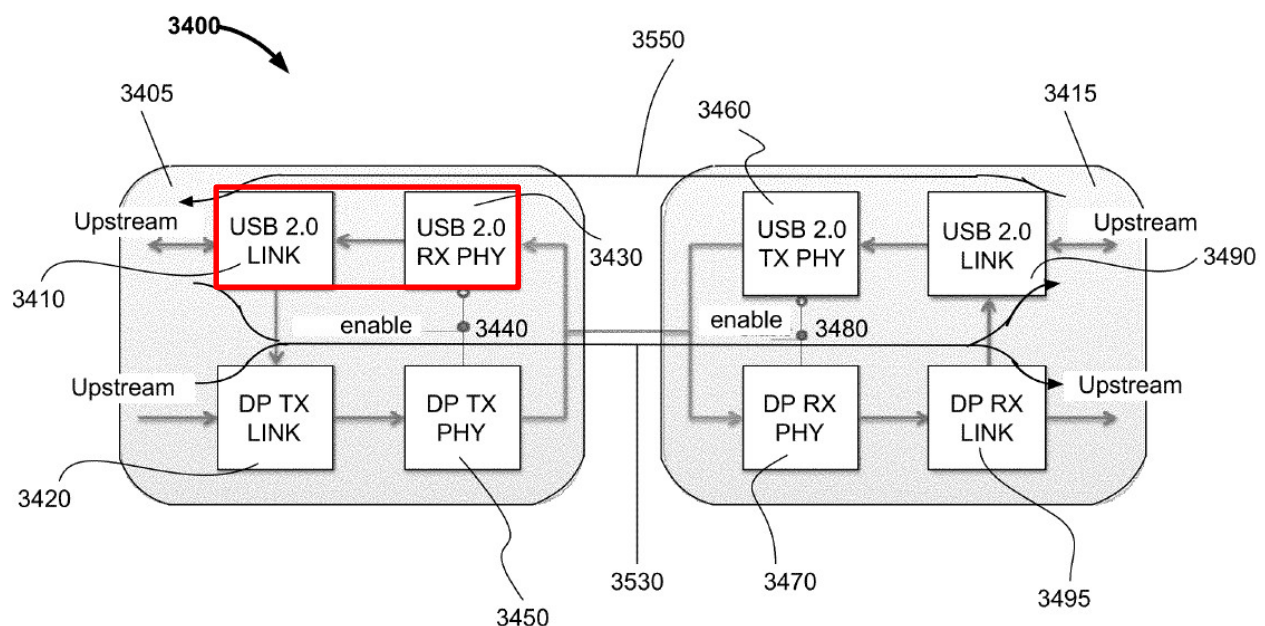


FIG. 35c

d. “a control signal transceiver coupled to a second physical channel of the multimedia link distinct from the first physical channel and configured to at least send control data from the source device to the sink device over the second physical channel.” [21.c]

93. As discussed in Section VIII.A.1.d (Grounds 1 and 2, limitations 1.c and 11.c), Zhu discloses or renders obvious limitation 1.c. In my opinion, Zhu also

discloses or renders obvious limitation 21.c, which recites a “control signal transceiver” coupled to the second physical channel and configured to perform the function recited in limitation 1.c. As discussed in Section VIII.A.1.d (Grounds 1 and 2, limitations 1.c and 11.c) above, Zhu discloses a side-band channel for transmitting control data bidirectionally between the source and sink. *See also* Section VIII.A.1 (Grounds 1 and 2, claims 1 and 11), *supra*.

94. Zhu also discloses a “control signal transceiver” to perform bidirectional side-band channel communication. For example, Zhu discloses a circuit 1810 within a source device that includes “a transmitter TX 1820 [and] a receiver RX 1840” (*control signal transceiver*) for sending and receiving, respectively, “side-band communication data” on a second physical channel (i.e. the C-wire). EX1006 at 22:43-60.

1800

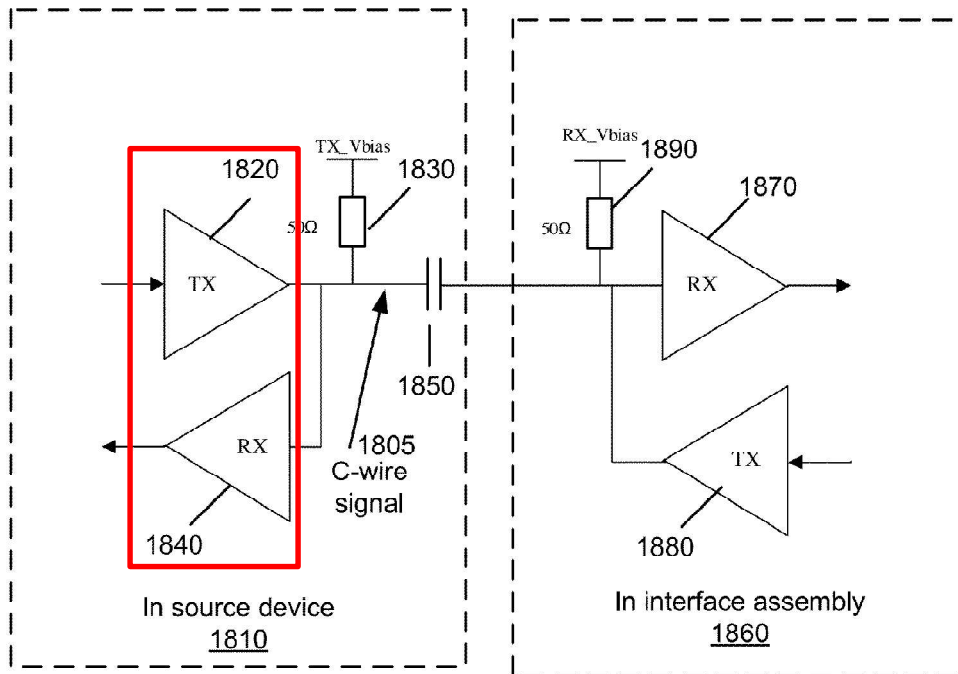


FIG. 18

EX1006 at Fig. 18. Although 1860 is identified as an “interface assembly,” a POSITA would recognize that it acts as a sink device in the sense that it receives DisplayPort signals from a source. This is consistent with the ’103 patent, which indicates that a sink device is an “other device” that receives A/V data from a source device. EX1001 at 4:15-16 (“The source device 110 herein refers to a device that sends A/V data to other devices (e.g., sink device 120).”).

95. In my opinion, a POSITA would have understood Zhu's teachings of bidirectional communication of control data over the side-band channel (either AUX channel differential wire pair or C-wire) between the source device and the sink device to disclose a control signal transceiver coupled to the side-band channel ("second physical channel"). To make this bidirectional communication possible, a POSITA would have understood that the source device includes something that transmits and receives the control data. A device that transmits and receives is, by definition, a "transceiver." A device (or combination of devices) that transmits and receives signals is, by definition, a "transceiver." EX1011 at 665 (defining "transceiver" as "[a]ny device that transmits and receives").

96. A POSITA would have at least found it obvious and been motivated to include a control signal transceiver in the source device of Zhu to perform the bidirectional communication of control data over the side-band channel that is taught in Zhu. Transceivers are a well-known technology for transmitting and receiving data and, in my opinion, a POSITA would have found it obvious that a transceiver could be used to transmit and receive the control data discussed in Zhu. EX1032 at Figure 1-1 and p. 28; EX1021 at Fig. 3; EX1014 at [0128], Fig. 17.

97. It is my opinion that a POSITA would have been motivated to include, within the source device, a control signal transceiver coupled to the second physical channel to send control signals because doing so would merely involve (a) the

predictable use of a prior art element (transceiver) according to its established functions (transmitting and receiving signals), (b) the use of known techniques (transmitting and receiving signals via a transceiver) to improve similar devices (the source device) in the same way, (c) applying a known technique (transmitting and receiving signals via a transceiver) to a known device (DisplayPort source device) ready for improvement to yield predictable results, and (d) choosing from a finite number of identified, predictable solutions (transceiver versus other options), with a reasonable expectation of success. A POSITA would have had a reasonable expectation of success in doing so at least because transceivers were well known and widely used before the Priority Date.

98. Even if a transceiver is narrowly defined to require a combined transmitter and receiver within a single package, in my opinion, a POSITA would have found it obvious to use such a transceiver to transmit and receive the control signals described in Zhu, as it is one of a finite number of identified, predictable solutions for transmitting and receiving signals (the other being the use of separately packaged transmitter and receiver), with a reasonable expectation of success based on the widespread use of such transceivers for this purpose.

99. For example, a POSITA would have at least found it obvious to employ the side-band channel transceiver of Figure 18 in the source device of Figure 35c “mixed mode” embodiment. Figure 18 specifically illustrates a transceiver for side-

band communication over a C-wire and, as discussed above, Zhu explains that the various embodiments (including, for example, Figure 35c) may include a C-wire.

5. Claim 22

100. As discussed in the previous section, it is my opinion that claim 21 is anticipated by or obvious in view of Zhu. Claim 22 recites substantially identical elements compared to claim 21; the only difference between the two claims is in the preamble. In its infringement contention claim chart for claim 22, UCT cites no evidence in connection with the preamble and, for every other element of claim 22, merely cross-references to the corresponding element of claim 21. EX1013 at 44-45. Thus, at least according to UCT's interpretation of this claim for purposes of infringement, it is my opinion that Zhu anticipates and/or renders obvious claim 22 for the same reasons stated in connection with claim 21. *See* Section VIII.A.4 (Grounds 1 and 2, claim 21).

101. It is my further opinion that Claim 22 is obvious in view of Zhu for the additional reasons below.

a. “A non-transitory computer readable storage medium storing instructions thereon, the instructions representing a digital design of a circuit comprising:” [22.p]

102. In my opinion, this limitation is obvious in view of Zhu and the knowledge of a POSITA. The phrase “digital design of a circuit” is not used anywhere else in the '103 Patent and it is not discussed in the prosecution history.

103. To the extent “digital design of a circuit” refers to a memory storing a digital schematic (or other design) of a circuit having the recited elements, the claim would have been obvious to a POSITA. Digital circuit design is a major branch of modern electronics and computer technology. Designs can be represented and stored in many forms, from schematics on paper, or in CAD programs. It would have been obvious to a POSITA that the circuit recited in claim 22 could be designed using a digital circuit design tool and such design stored in computer memory. Software-based digital circuit design is a known method that yields predictable results (a digital circuit design), would merely require applying a known technique (designing a circuit on a computer) to a known device (the circuit design described in claim 22) to yield predictable results (a digital circuit design), and would at the very least be obvious to try because digital circuit design is one of a finite number of identified, predictable solutions (others include designing a circuit by hand or building a physical circuit by trial-and-error) with a reasonable expectation of success. Moreover, digital circuit design is supported by market incentives such as the ability to design, simulate, debug, and manufacture products with complicated circuits inexpensively.

104. For example, U.S. Patent Publ. No. 2005/0209808, which was filed March 7, 2005 and published September 22, 2005 (both well before the Priority Date), describes “[v]arious software programs [that] have been developed to assist

the automated testing engineer with discreet [sic] portions of the test development process” including “the PSPICE® program from Cadence Design Systems, Inc., which provides a predictive simulated graphical analytical environment as an aid for designing circuits” and “allows an engineer to draw and graphically illustrate a circuit on a display, and the program will then create a suggested circuit board layout and predict the outcome of simulate tests run on the circuit.” EX1022 at [0027]-[0028]. PSPICE and other similar computer-based circuit design tools were well-known in the prior art. EX1023 at 20:61-67 (listing numerous exemplary “hardware description languages, circuit descriptions, netlist descriptions, mask descriptions, or layout descriptions” including PSPICE); EX1024 at 18:49-52 and 20:51-59 (recommending use of “PSPICE® circuit emulation, available as software from Cadence Design Systems . . . [as a] design support tool prior to board fabrication.”); EX1025 at 12:24-25, 13:62-66, 14:43-46 (describing use of PSPICE to simulate circuit designs); EX1026 at 9:57 – 10:7 (describing use of “[t]he PSPICE® circuit simulator tool”); EX1027 at [0035], [0085], [0089]-[0091], [0100] (describing use of PSPICE to simulate circuit designs). U.S. Patent No. 7,356,789, filed May 27, 2005 and issued April 8, 2008, describes “Electronic Design Automation (EDA) tools from companies such as Synopsys, Cadence Design Systems, and Mentor Graphics . . . [that] simulate and formally verify circuits described at the register transfer level (RTL) level using languages such as Verilog and VHDL.” EX1028 at

1:15-21. Such a circuit description takes the form of instructions in a “Hardware Description Language (HDL)” in a “programmed computer.” *Id.* at 2:11-23.

105. To the extent “digital design of a circuit” in claim 22 refers to a memory storing instructions capable of performing the functions of the recited circuit elements (transmitter, receiver, and control signal transceiver), this would also be obvious in view of Zhu and the knowledge of a POSITA. The ’103 Patent includes very thin description of such an embodiment. In describing the source device 110 of Figure 1, the ’103 Patent states merely that each of transmitter 111, receiver 112, buffer 113, and control logic 114 “is hardware, firmware, software, or a combination thereof.” EX1001 at 4:21-63. Figure 6 of the ’103 Patent discloses a system that includes transmitter 652, receiver 654, and control logic 656 (which transmits and receives control data) and one or more non-volatile memories “for storing information and instructions to be executed by the processor(s) 604.” EX1001 at 8:64-9:41.

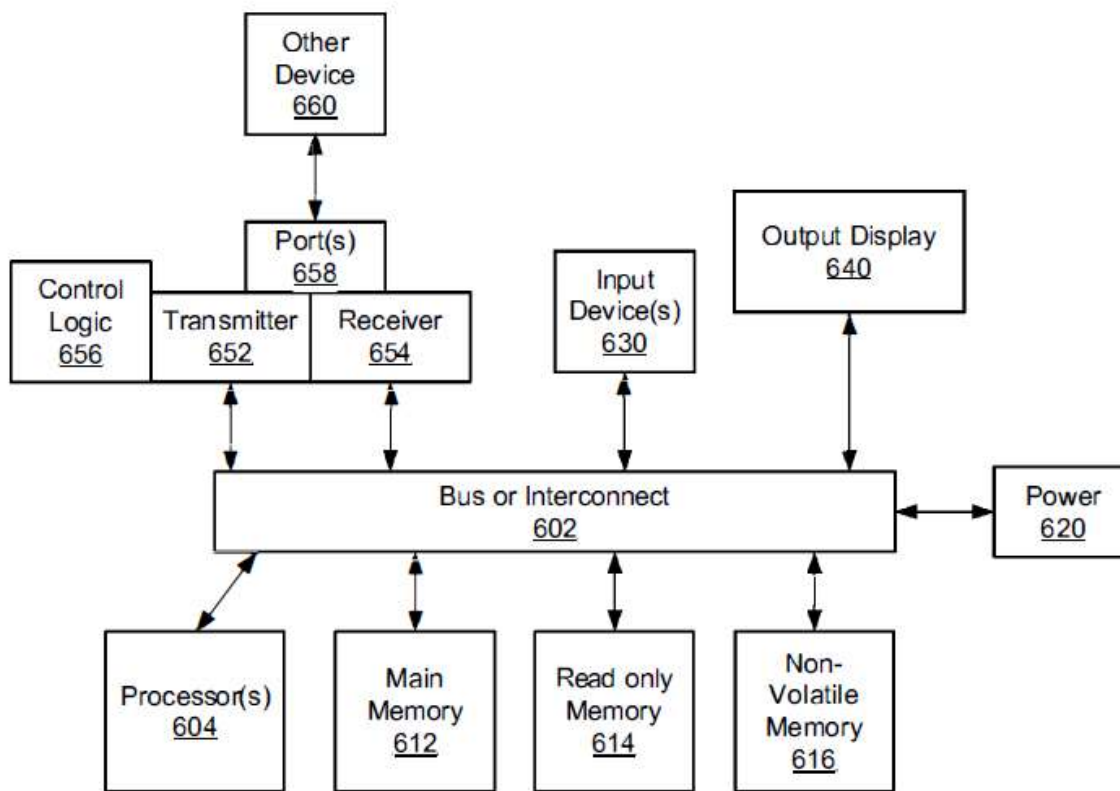


FIG. 6

600

EX1001 at Fig. 6. However, the '103 Patent does not state that the instructions stored on memory perform the functions of the transmitter, receiver, or control signal transceiver.

106. Zhu includes similar disclosure, explaining that certain embodiments may be implemented by a processor executing instructions stored in a memory. *See* EX1006 at 21:12-21 and 6:21-29. In particular, Figure 1B of Zhu illustrates a source device that “includes a processor 132, memory 134, input 135, display 138, and data communication mechanism 140.” EX1006 at 6:14-20. Data communication

mechanism 140 includes the circuitry used for transmission and reception of signals according to protocols such as DisplayPort and USB. *Id.* at 6:39-56. Like the '103 Patent, Zhu teaches that “[p]rocessor 132 may be used to execute instructions that are stored in memory 134.” *Id.* at 6:21-29.

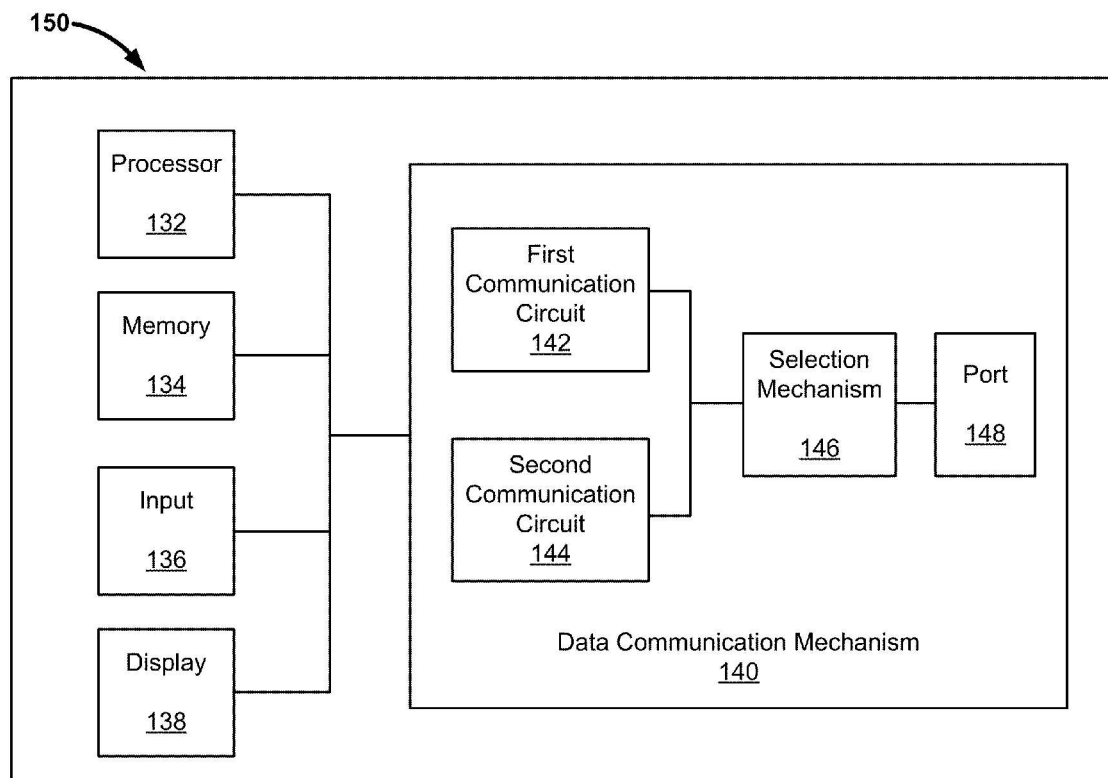


FIG. 1B

107. Moreover, software implementations of transceivers (and thus, of transmitters and receivers) were well-known in the art and a POSITA would have been familiar with them before the Priority Date. For example, U.S. Patent 6,496,546, issued December 17, 2002, explains that software-defined transmitters,

receivers, and transceivers were well known in the art even at that time. EX1029 at 2:5-34.

108. Amchislavsky, another Silicon Image patent, discloses that a transmitter and a receiver (and therefore, a transceiver) for communicating video, USB, and control data could be implemented by software instructions stored on memory to the same extent as, and in nearly identical terms used in, the '103 Patent. In particular, Amchislavsky discloses “an apparatus and system to provide data tunneling transmission of multiple protocol elements via a connector utilizing a data tunnel.” EX1014 at [0041], Fig. 1.

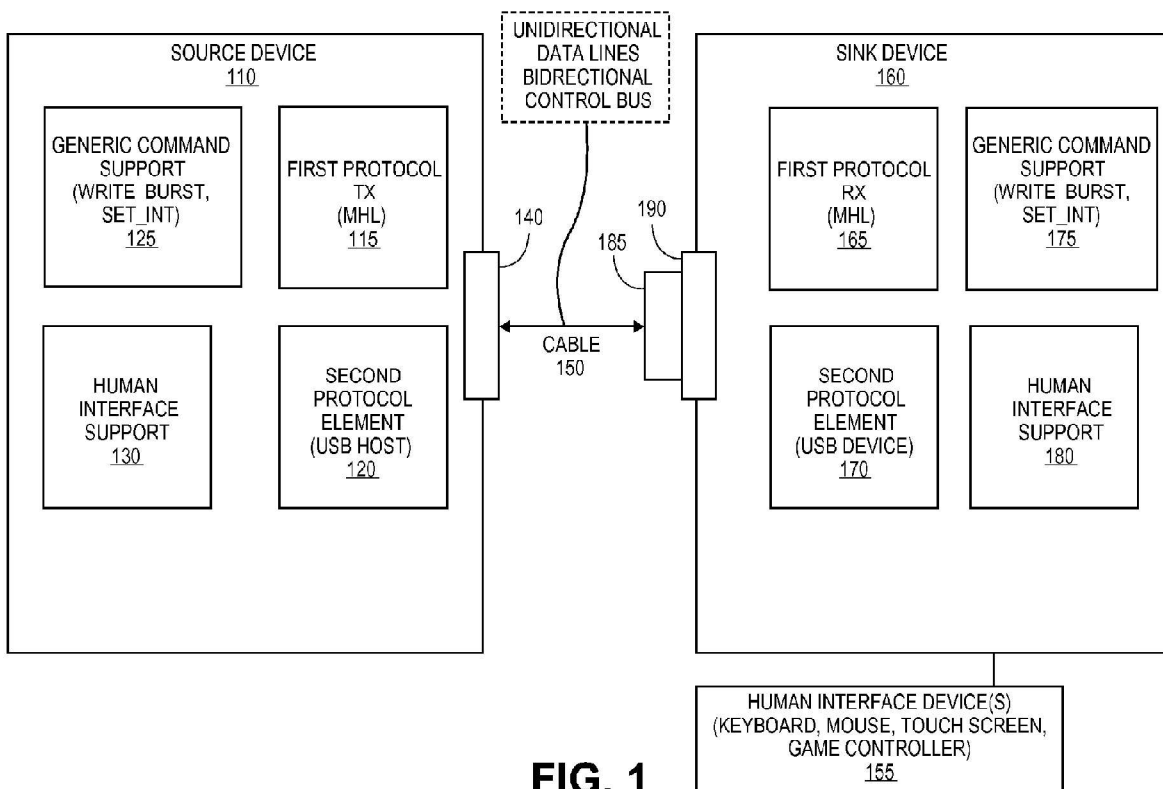


FIG. 1

109. The system of Figure 1 includes unidirectional data lines, a bidirectional control bus, and a source device that includes an MHL transmitter and a sink device that includes an MHL receiver. Amchislavsky discloses numerous embodiments along similar lines (*see, e.g.*, EX1014 at Figs. 12, 13, 15, and 16) and explains that “[t]he processes of the present invention may be performed by hardware components or may be embodied in computer-readable instructions, which may be used to cause a general purpose or special purpose processor or logic circuits programmed with the instructions to perform the processes.” EX1014 at [0132]. Moreover, Figure 17 of Amchislavsky illustrates a system that—just like Figure 6 of the ’103 Patent—includes a transmitter/receiver, processors, and memories “storing information and instructions to be executed by the processors.” EX1014 at [0125]-[0128].

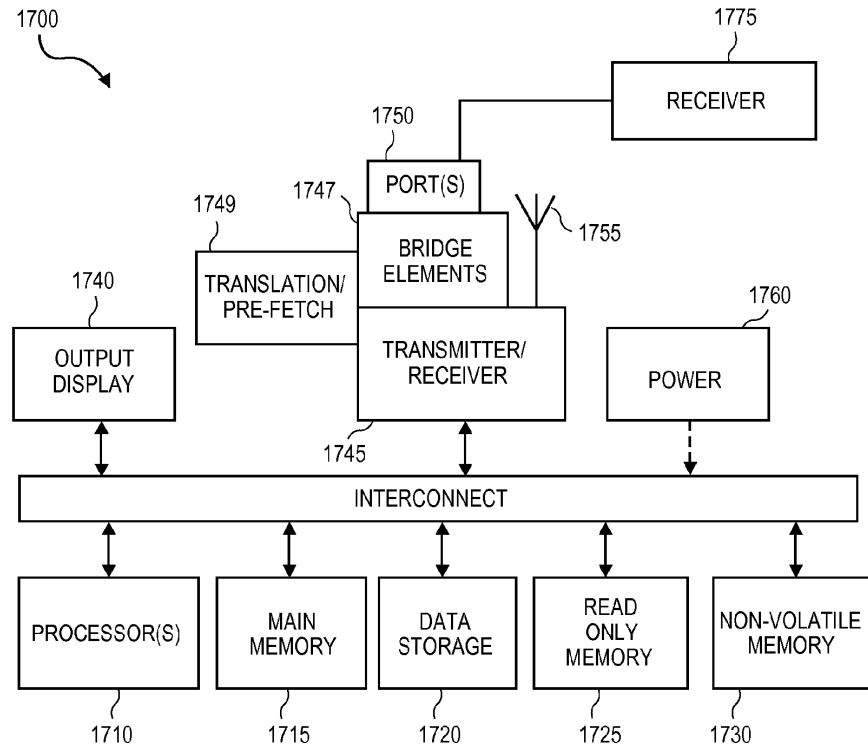


FIG. 17

110. Amchislavsky therefore teaches that a transmitter and a receiver (and therefore, a transceiver) could be implemented in software instructions stored on memory to the same extent as, and in nearly identical terms used in, the '103 Patent.

111. As another example, U.S. Patent Publ. No. 2013/0174208 to Lee and Hussain ("Lee") was filed Dec, 29, 2011 and published July 4, 2013, before the Priority Date. Lee relates "to the field of image display systems" and specifically refers to DVI, HDMI, and DisplayPort interfaces. EX1021 at [0002]. Figure 1 of Lee illustrates "an exemplary known display system" that includes display source 12 and

display sink 14 connected by an audio/video bus 32 and a bidirectional I²C bus for communicating control data such as Display Data Channel and/or Command Interface (DDC/CI) signals and extended display identification data (EDID) between the source and sink. EX1021 at [0003]-[0012], Fig. 1.

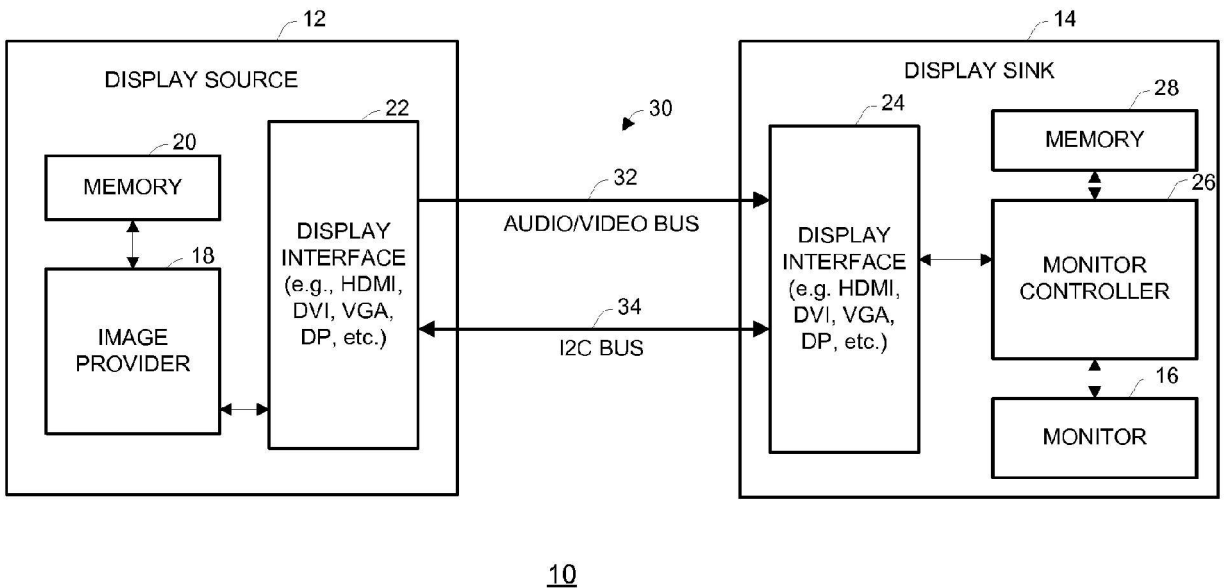


**FIG. 1
(PRIOR ART)**

112. Display source 12 and display sink 14, respectively, include display interfaces 22 and 24 for communicating video and control signals, and memories 20 and 28 that “may include software or firmware with program instructions” to be executed by a processor. EX EX1021 at [0004]-[0005].

113. Figure 2 of Lee illustrates versions of the source and sink of Figure 1 that have been modified to include wireless source device 142 and wireless sink device 144. EX1021 at [0038], Fig. 2.

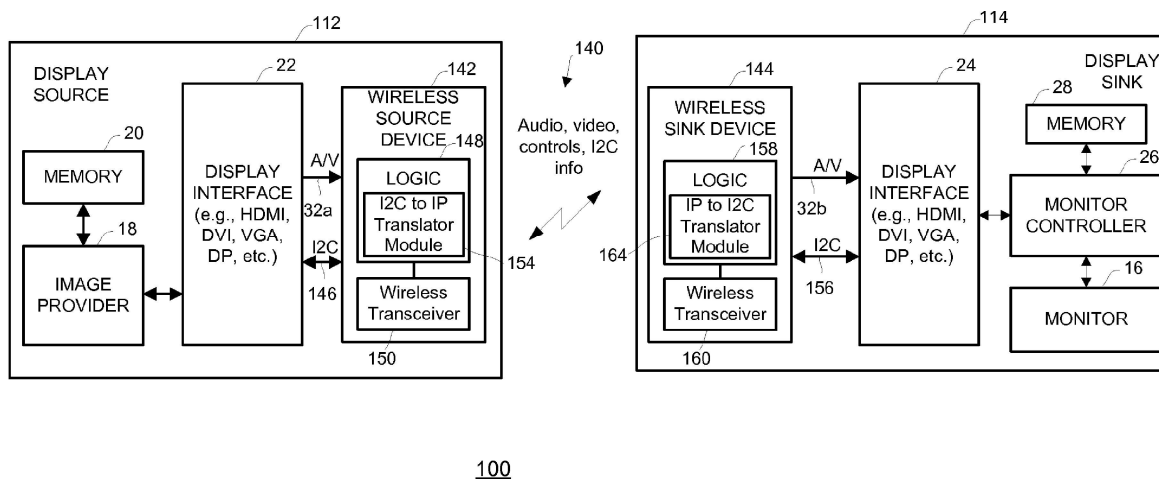


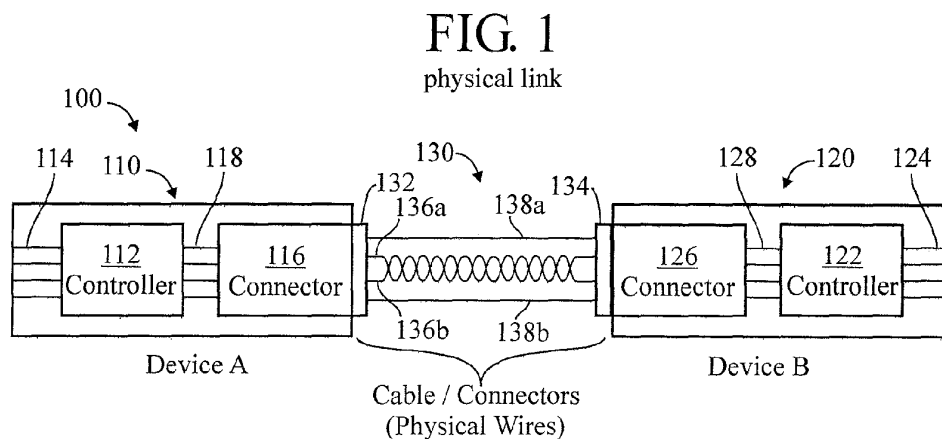
FIG. 2

114. Wireless source device 142 and wireless sink device 144 each include a transceiver. Lee further explains that the source and sink may each include a processor and “a memory that includes software and/or firmware code containing instructions that, when executed by the processor, cause the processor to perform the functions of” the source or sink, respectively. EX1021 at [0044]; *see also id.* at [0038], [0048].

115. Yet another example is U.S. Patent No. 9,210,010 to Whitby-Strevens (“Whitby-Strevens”), which was filed March 14, 2013 and issued December 8, 2015.

Whitby-Strevens describes a DisplayPort transmitter and receiver that “could readily be implemented in software.” EX1030 at Fig. 4A, 7:63-8:3.

116. Another particular example is U.S. Publ. No. 2013/0266154 (“McCormack”), which was filed February 26, 2013 and published October 10, 2013. McCormack discloses a well-known technique for implementing a software-based transceiver known as “bit banging,” specifically in the context of communicating data according to a standardized protocol (such as USB, DisplayPort, HDMI, etc.). EX1010 at [0084]. Figure 1 of McCormack “illustrates a physical communications link 100 between two electronic devices that communicate according to a standard-based protocol. EX1010 at [0072], Fig. 1.



117. Each device includes a controller 112, 122 that includes transceivers and may be “implemented as a system on chip.” EX1010 at [0075]-[0076]; *see also* [0148] (describing a “transceiver [that] may be implemented as a chip comprising a transmitter (Tx), a receiver (Rx), and related components”). McCormack further

explains that such chips may be “implemented, at least partially, by software running on a microcontroller. For example, ‘bit banging’ is a technique for serial communications using software instead of dedicated hardware.” EX1010 at [0069]. It is my opinion that, before the Priority Date, a POSITA would have been familiar with bit banging as an approach to designing a transceiver. Besides McCormack, numerous other authors discussed bit banging applications before the Priority Date. *See, e.g.*, EX1016 (describing an “Efficient Bit-Banged SPI Port for 8051-Compatible Microcontrollers”); EX1017 (“A method commonly referred to as ‘bit banging’ is used to create a software-based SPI port. This method uses general-purpose I/O lines to emulate a serial port”); EX1018 (discusses an “Implementation of MCU Invariant I²C Slave Driver Using Bit Banging”); EX1019 at 3 (explaining that “[b]it banging is a technique for serial communications using software instead of dedicated hardware” and “can be implemented at very low cost, and is widely used in embedded systems”).

118. In my opinion, as demonstrated by the prior art discussed above, a POSITA would have been well aware that transmitters, receivers, and transceivers for data communication could be implemented in software. It is my opinion that a POSITA would have been motivated to implement the transceiver, receiver, and control signal transceiver of Zhu in software at least because doing so would have involved (a) the simple substitution of one known element (a software-based

transmitter, receiver, or transceiver) for another (hardware implementation of same) to obtain predictable results, (b) the predictable use of prior art elements (software-based transmitter, receiver, and transceiver) according to their established functions, (c) the use of known techniques (software implementation) to improve similar devices (transmitter, receiver, transceiver) in the same way, (d) applying a known technique (software implementation) to a known device transmitter, receiver, transceiver) ready for improvement to yield predictable results (transmitter, receiver, and transceiver operation), choosing from a finite number of identified, predictable solutions (software or hardware), with a reasonable expectation of success, and (e) design incentives and market forces (e.g. the lower cost, greater design flexibility and simplicity of implementing a software-based circuit). *See, e.g.*, EX1019 at 3 (“Bit-banging can be implemented at very low cost, and is widely used in embedded systems.”); EX1016 (“Although 8051-compatible microcontrollers with SPI ports are available, a lower cost device with an SPI port bit-banged through GPIO pins often suffices for many applications.”). Moreover, as explained above, Zhu suggests the use of software for implementing portions of the disclosed circuit, and, in my opinion, this would have further inspired a POSITA to implement a transmitter, receiver, and control signal transceiver of Zhu in software. A POSITA would have had a reasonable expectation of success in doing so, because software-based

transmitters, receivers, and transceivers were well-known and widely used before the Priority Date.

119. Thus, in view of this knowledge and Figure 1B in Zhu, it is my opinion that a POSITA would have found it obvious to implement the transmitter, receiver, and control signal transceiver in Zhu through instructions stored on a non-transitory computer-readable storage medium.

b. Limitations 22.a, 22.b, and 22.c

120. Limitations 22.a, 22.b, and 22.c are substantially identical to limitations 21.a, 21.b, and 21.c which, as explained in Sections VIII.A.4.b-d (Grounds 1 and 2, limitations 21.a-c), Zhu discloses or renders obvious. For the reasons stated in the previous section, in my opinion it would have been obvious that a digital design of the transmitter, receiver, and control signal transceiver circuit of Zhu could be represented by instructions on a computer-readable storage medium.

B. Ground 3. Claims 1-3, 10-13, 17, and 20-22 obvious over Zhu and DisplayPort 1.2

121. For the reasons explained below, it is my opinion that claims 1-3, 10-13, 17, and 20-22 of the '103 Patent would have been obvious in view of Zhu in combination with DisplayPort 1.2.

1. Motivation to Combine Zhu and DisplayPort 1.2

122. In my opinion, a POSITA would have been motivated to combine Zhu with DisplayPort 1.2 and would have had a reasonable expectation of success in

doing so, because (a) DisplayPort 1.2 was and remains a well-known protocol for AV communication and (b) Zhu teaches that the disclosed embodiments employ DisplayPort 1.2 with specific modifications.

123. The motivation to combine Zhu and DisplayPort 1.2 can be found in the teachings of Zhu itself. Zhu explicitly cites several versions of the DisplayPort specification. EX1006 at 1:42-47 (“A DisplayPort (DP) communication standard is an interface and link protocol for transferring high definition video/audio and data across computer systems and electronics devices. The Video Electronics Standards Association (VESA) has defined various standards versions, which are incorporated by reference herein, including 1.1, 1.1a and 1.2.”). To enable the “mixed-mode” operation discussed above, Zhu instructs adding extra hardware blocks to “legacy DisplayPort 1.2 specification” source and sink devices. EX1006 at 33:20-29 (“Compared with legacy DisplayPort 1.2 specification, the USB 2.0TX/RX PHY 3430 and 3460 and LINK blocks 3410 and 3490 are extra hardware to support USB 2.0 data transfer on the DisplayPort link.”); *see also id.* at 33:63-34:38. Zhu further instructs to apply the “same link timing generation scheme” of the DisplayPort 1.2 MST protocol, with minor modifications to include USB data in the MTPs sent from source to sink over the DisplayPort 1.2 Main Link. EX1006 at 34:47-36:24 (e.g., “In various embodiments, the Main Stream Attribute (MSA) data format, originally defined in DisplayPort specification, is modified to support USB data transfer.”).

Zhu further instructs that USB data may be transmitted from sink to source using “the SST (single-stream transport) protocol defined in DP 1.2 standard.” EX1006 at 35:45-49.

124. Thus, in my opinion, a POSITA would have been motivated to apply the teachings of Zhu to a DisplayPort interface as specified in DisplayPort 1.2, because Zhu teaches embodiments that merely modify the underlying DisplayPort 1.2 protocols. To the extent that Zhu does not sufficiently describe, for example, synchronization signals (or how they are used), a distinct channel for control data (as discussed above, it is my opinion that Zhu does disclose a distinct channel for control data in the form of the AUX and/or C-Wire channels), or a control signal transceiver, a POSITA would have been motivated to implement the control symbols, link training, AUX channel, and AUX channel transceiver that are part of DisplayPort 1.2 in conjunction with the methods and apparatuses disclosed in Zhu. In addition to the express teachings of Zhu, such a combination would reflect the use of a known technique to improve similar devices (methods or products) in the same way and applying a known technique to a known device (method or product) ready for improvement to yield predictable results.

125. In my opinion, a POSITA would have had a reasonable expectation of success in combining Zhu and DisplayPort 1.2, at least because the embodiments disclosed in Zhu implement DisplayPort 1.2 with minor modifications to a standard

DisplayPort 1.2 interface. *See* EX1006 at 1:42-47, 33:20-29, 33:63-34:38, 34:47-36:24. Zhu provides detailed guidance that would enable a POSITA to make the disclosed modifications to DisplayPort 1.2. *See, e.g.*, EX1006 at 33:20-36:35. Thus, in my opinion, a POSITA would have been motivated to apply the modifications and hardware disclosed in Zhu to a system that is otherwise compliant with (and includes the features of) DisplayPort 1.2, and would have a reasonable expectation of success in doing so. Given Zhu's extensive discussion of DisplayPort 1.2, it is further my opinion that a POSITA would have been motivated to consult DisplayPort 1.2 to understand Zhu's disclosure (for example, the details of the MST and SST protocols).

2. Claims 1 and 11

126. As explained in Section VIII.A.1 (Grounds 1 and 2, claims 1 and 11), it is my opinion that Zhu anticipates or renders obvious claims 1 and 11. As explained below, it is further my opinion that claims 1 and 11 would have been obvious in view of Zhu and DisplayPort 1.2.

127. Moreover, to the extent it is argued that Zhu's reference to MTPs in the forward data flow according to the DisplayPort 1.2 MST protocol does not explicitly disclose "forward units of data" as recited in limitation 1.a, that is certainly disclosed in DisplayPort 1.2, which explains that an MTP is a "Multi-stream Transport Packet." EX1032 at 136 ("The vessel of uPackets is called MTP (Multi-Stream

Transport Packet). The MTP is 64 link-symbol cycles (that is, 64 time slots) long, starting with MTP Header in the first time slot (or Time Slot 0), and is constantly transported regardless of the presence/absence of streams.”).

128. And to the extent it is argued that Zhu does not disclose both a first physical channel (as recited in limitations 1.a/11.a and 1.b/11.b) and a second physical channel distinct from the first physical channel (as recited in limitation 1.c/11.c), it is my opinion that this limitation is at least obvious in view of Zhu and DisplayPort 1.2, which discloses bidirectional communication of control data between source and sink over a side-band AUX channel (*second physical channel of the multimedia link distinct from the first physical channel*) that is distinct from the Main Link lanes (each a *first physical channel*). EX1032 at 34 (“The auxiliary channel is a half-duplex bidirectional channel used for link management and device control”); 35 (“The correct number of lanes is enabled at the correct link rate with the correct drive current and equalization level through the handshake between DisplayPort transmitter and receiver via AUX CH.”); 170 (“This section describes the DisplayPort AUX transaction syntax suitable for a half-duplex, bidirectional AUX CH PHY”). Zhu explicitly describes the communication of bidirectional control data over the DisplayPort “AUX channel” in connection with the “mixed mode” embodiment. *See* EX1006 at 35:60-66 (describing the exchange of control data over the AUX channel to facilitate link turn-around). In my opinion, a POSITA

would thus find it obvious to implement the AUX channel as described in DisplayPort 1.2.

129. DisplayPort 1.2 teaches that the AUX channel is a “second physical channel . . . distinct from the first physical channel” (i.e. Main Link data lane). EX1032 at 35 (“AUX CH consists of an AC-coupled, doubly-terminated differential pair.”). This is shown, for example, in Figure 1-1 of DisplayPort 1.2:

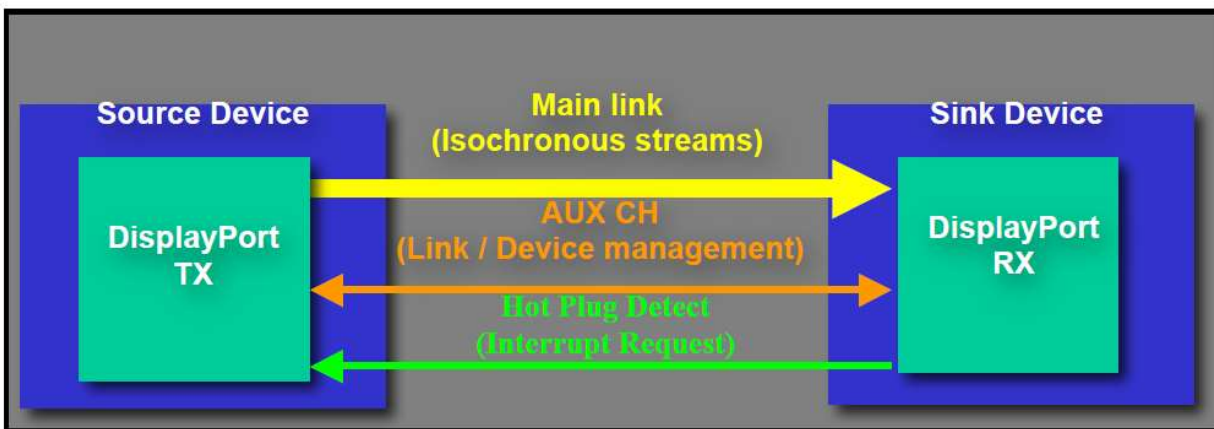


Figure 1-1: DisplayPort Data Transport Channels

EX1032 at 34.

130. Pins 15 and 17 (“AUX_CH(p)” and “AUX_CH(n)”) of a DisplayPort connector are assigned to the AUX channel, further demonstrating that the AUX channel is a physical channel (in the form of a differential wire pair) that is distinct from a first physical channel (one of the Main Link lanes, such as the one assigned to pins ML_Lane_1(n) and ML_Lane_1(p)).

Table 4-4 Downstream Port Connector Pin Assignment

Pin Number	Signal Type	Pin Name	Mating Row Contact Location	Vertically Opposed Connector's Front View
1	Out	ML Lane 0(p)	Top	
2	GND	GND	Bottom	
3	Out	ML Lane 0 (n)	Top	
4	Out	ML Lane 1 (p)	Bottom	
5	GND	GND	Top	
6	Out	ML Lane 1 (n)	Bottom	
7	Out	ML Lane 2 (p)	Top	
8	GND	GND	Bottom	
9	Out	ML Lane 2 (n)	Top	
10	Out	ML Lane 3 (p)	Bottom	
11	GND	GND	Top	
12	Out	ML Lane 3 (n)	Bottom	
13	CONFIG (see note 1)	CONFIG1	Top	
14	CONFIG (see note 1)	CONFIG2	Bottom	
15	I/O	AUX CH (p)	Top	
16	GND	GND	Bottom	
17	I/O	AUX CH (n)	Top	
18	In	Hot Plug Detect	Bottom	
19	RTN	Return	Top	
20	PWR Out (see note 2)	DP PWR	Bottom	

EX1032 at 401 (annotated).

131. Zhu explicitly describes “merg[ing] the USB data stream into the DisplayPort data lane(s)” and communicating bidirectional control data over the DisplayPort AUX channel in connection with the “mixed mode” embodiment. *See* EX1006 at 31:25-30, 35:60-66. In my opinion, a POSITA would thus understand, or at least find it obvious, that the side-band channel and Main Link data lanes of Zhu are distinct physical channels, as described in DisplayPort 1.2.

3. Claims 2 and 12: “The method of claim [1 / 11], further comprising [sending / receiving] a first synchronization signal of a first length after [sending / receiving] a first forward unit of data of

the forward units of data, and before [sending / receiving] [another / a second] forward unit of data from the source device.”

132. As explained in the previous section, it is my opinion that claims 1 and 11 would have been obvious in view of Zhu and DisplayPort 1.2. In my opinion, dependent claims 2 and 12 (which depend from claims 1 and 11, respectively) are also obvious in view of Zhu and DisplayPort 1.2.

133. As explained in Section VIII.A.2 (Grounds 1 and 2, claims 2 and 12) above, Zhu teaches that the forward data stream includes control function SR, which satisfies the additional limitations of these claims. Zhu employs the DisplayPort 1.2 MST protocol, modified to insert a USB Data Packet within the MST packet (MTP). EX1006 at 34:52-61; Fig. 37. DisplayPort 1.2 offers more detail about the MTP, the MTP header (MTPH), and the “control function codes” that may be used for synchronization, including SR. *See* EX1032 at 165 (annotated tables below).

Table 2-65: MTP Header Control Functions

Control Function	Code/Control Symbol Sequence ²	Comment
SR (Scrambler Reset)	K28.5	Comma character; Link Frame Indicator
RESERVED	K28.1	Not used.
RESERVED	K28.7	Not used to avoid coding complication
RESERVED	K28.4	Not used for EMI reduction purpose
ACT (Allocation Change Trigger)	C0-C1-C1-C0	Trigger to downstream device indicating change in allocation on local link. ACT Control Function sequence is unique from others; its 4-code control symbol sequence spans four consecutive MTP Header time slots).

Table 2-66: MTP Payload Control Functions

Control Function	Control Symbol Sequence (C_x, C_y, C_z, C_aa)
RG (Rate Governing)	C0-C1-C2-C3
BS (Blank Start)	C0-C0-C0-C0
BE (Blank End)	C1-C1-C1-C1
RESERVED	C2-C2-C2-C2
SS (Secondary Start)	C3-C3-C3-C3
SF (Stream Fill)	C4-C4-C4-C4
RESERVED	C5-C5-C5-C5
SE (Secondary End)	C6-C6-C6-C6
RESERVED	C7-C7-C7-C7

134. For example, DisplayPort 1.2 explains that SR is a “comma character,” which is an 8b/10b symbol with special properties that make it useful for synchronization. EX1012 at 8:39-9:36 and Table III. As shown in Figure 37 of Zhu, SR is only sent periodically.

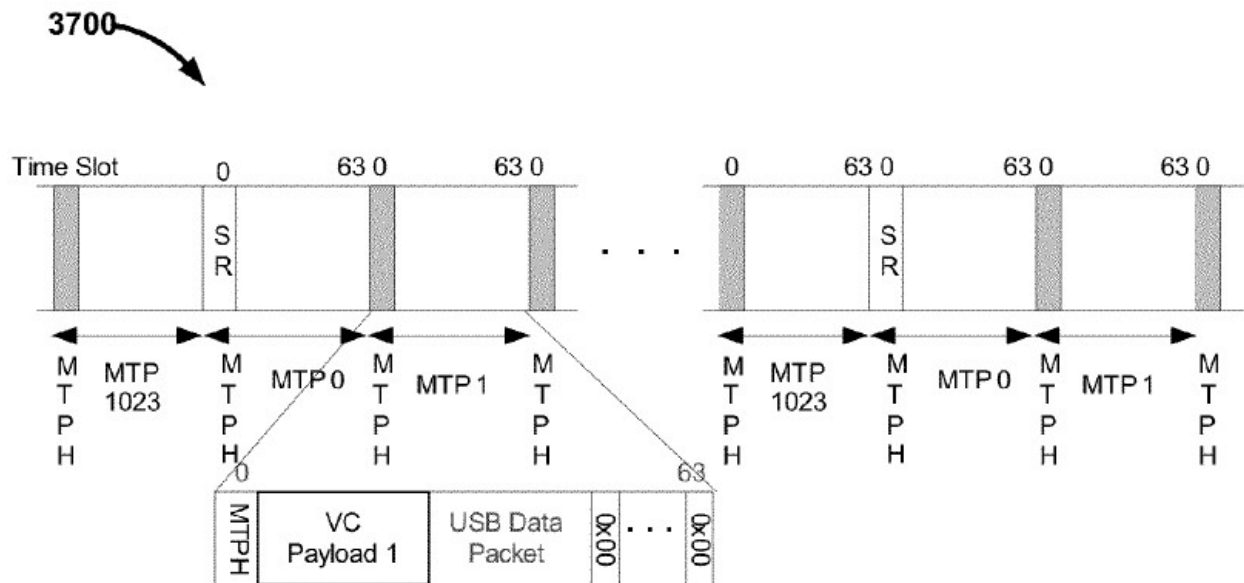


FIG. 37

135. Thus, Zhu and DisplayPort 1.2 together disclose that SR (*first synchronization signal*) is sent/received after one or more MTPs sent before SR, such as MTP 1023 (*first forward unit of data*), and before one or more MTPs sent after SR, such as MTP 0 and MTP 1 (*second / another forward unit of data*). Moreover, SR has a “first length” (40 bits, the length of four K28.5 codes). EX1032 at 46 (“In Enhanced Framing Mode, the Scrambler Reset consists of four symbol sequence on each lane.”).

136. The MTP payload includes additional synchronization signals. For example, it may include “Blank Start” (BS), represented by a sequence of four 8b/10b symbols. EX1032 at 165-166. In the related litigation against Dell, UCT

alleges that the BS header in the accused DisplayPort tunneling over USB4 satisfies this element EX1013 at 2 (“[E]ach accused product comprises sending a first synchronization signal of a first length as the Blanking Start (BS) header.”). Thus, at least under UCT’s own interpretation of this claim, BS is also a “first synchronization symbol.”

4. Claims 3 and 13: “The method of claim [2 / 12], further comprising [sending / detecting] a second synchronization signal of a second length longer than the first synchronization signal to initialize communication over the first physical channel before [sending / receiving] the first forward unit of data.”

137. As explained in the previous section, it is my opinion that claims 2 and 12 would have been obvious in view of Zhu and DisplayPort 1.2. In my opinion, dependent claims 3 and 13 (which depend from claims 2 and 12, respectively) are also obvious in view of Zhu and DisplayPort 1.2.

138. DisplayPort 1.2 describes sending/receiving a second synchronization signal that is longer than the first synchronization signal as part of link training, which “must be performed unless the Source Main Link transmitter and the Sink Main Link receiver are already in synchronization.”² EX1032 at 250. Link training, which initializes the DisplayPort Main Link and synchronizes the DisplayPort

² Zhu also references DisplayPort “link training” throughout its disclosure.

EX1006 at 20:48-51; 27:30-36; and 29:14-25.

receiver to Main Link data, involves two tasks: (1) Clock Recovery and (2) Channel Equalization / Symbol-Lock / Inter-lane Alignment. EX1032 at 250, 354. As part of the Channel Equalization Sequence, the source device (“Upstream device”) transmits training pattern TPS2 or TPS3 (either a *second synchronization signal*). EX1032 at 358 (“In the Channel Equalization (EQ) sequence, the Upstream device transmits the appropriate pattern (TPS2 or TPS3) with scrambling disabled.”). This is shown in Figure 3-33:

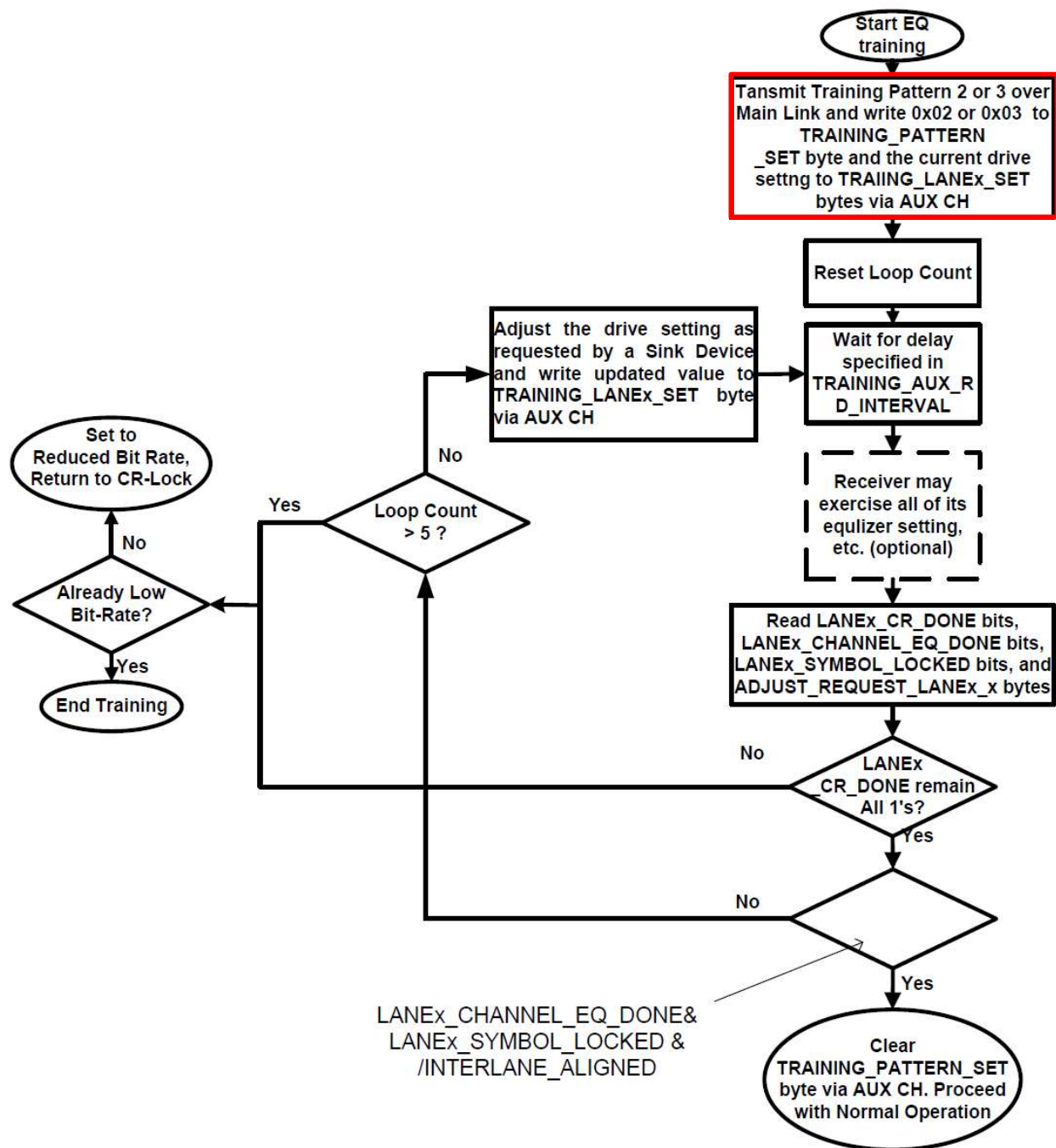


Figure 3-33: Channel Equalization Sequence of Link Training

EX1032 at 360 (annotated). TPS2 and TPS3 are each constructed as a sequence of 8b/10b symbols, as shown In Table 3-16 of DisplayPort 1.2:

Table 3-16: Symbol Patterns of Link Training

Pattern Number	Purpose	Name
TPS1	For locking clock recovery circuit of the DisplayPort receiver	Repetition of D10.2 characters without scrambling
TPS2	For optimizing equalization, determining symbol boundary, and achieving inter-lane alignment	K28.5-, D11.6, K28.5+, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2 without scrambling
TPS3	For optimizing equalization, determining symbol boundary, and achieving inter-lane alignment	K28.5-, K28.5+, K28.5-, K28.5+, D10.2-, D10.2-, D10.2-, D10.2-, D10.2-, D10.2-, D10.2-, K28.5-, K28.5+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-,D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-, D30.3+, D30.3-,D30.3+, D30.3-,D30.3+ without scrambling

EX1032 at 355-56.

139. TPS2 and TPS3 are “synchronization signals” because they are signals sent as part of link training, through which the “DisplayPort receiver is synchronized to incoming Main Link data.” EX1032 at 250. Moreover, TPS2 and TPS3 each include instances of K28.5- and K28.5+, which are 8b/10b comma characters with special properties that are useful for synchronization. EX1012 at 8:39-9:36 and Table III. Furthermore, Table 3-16 explains that one “purpose” of TPS2 and TPS3 is “determining symbol boundary,” which is a form of synchronization. EX1032 at 356.

140. DisplayPort 1.2 teaches that TPS2 and TPS3 are “detected” by the sink device, explaining that “[t]he receiver must use the recognition of this training pattern [i.e. either TPS2 or TPS3] to decide whether the channel equalization is successful or not” and “[t]he receiver sets the LANEx_SYMBOL_LOCKED bits in DPCD Link Status field only when it has properly detected and aligned the ANSI8B/10B symbol boundaries” in the training patterns. EX1032 at 358-59;

141. TPS2 is a sequence of ten 8b/10b symbols, and TPS3 is a sequence of 34 8b/10b symbols. Both TPS2 and TPS3 are, therefore, of a “second length longer than the first synchronization signal” (e.g., SR or BS, which are each a series of four 8b/10b symbols).

142. TPS2 and/or TPS3 are sent “before sending the first forward unit of data” because the DisplayPort link training must typically be performed before transporting a stream. EX1032 at 250.

143. Notably, during prosecution of the '103 Patent, the examiner mapped claim 3 to paragraphs in U.S. Patent Publ. No. 2007/0201492 (“Kobayashi”) that describes similar 8b/10b training patterns. EX1002 at 85; EX1005 at ¶¶ 0071, 0075-76 (teaching that the “main link transmitter 102 sends a pre-defined training pattern so that the receiver 104 can determine whether it can achieve a solid bit/character lock” and discussing 8b/10b encoding). The applicant did not dispute that mapping.

5. Claims 10 and 20: “The method of claim [1 / 11], further comprising [receiving / sending] control data from the sink device to the source device over the second physical channel of the multimedia link distinct from the first physical channel.”

144. As explained in Section VIII.B.2 (Ground 3, claims 1 and 11), it is my opinion that claims 1 and 11 would have been obvious in view of Zhu and DisplayPort 1.2. It is further my opinion that dependent claims 10 and 20 would have been obvious in view of Zhu and DisplayPort 1.2.

145. As explained in Section VIII.A.3 (Grounds 1 and 2, claims 10 and 20), Zhu teaches the additional limitation of dependent claims 10 and 20 expressly. To the extent it is argued Zhu does not disclose a second physical channel distinct from the first physical channel (as discussed above, it is my opinion that Zhu does disclose a distinct channel for control data in the form of the AUX and/or C-Wire channels), it is my further opinion that this claim would at least be obvious over Zhu in further view of DisplayPort 1.2, for the reasons explained in Section VIII.B.2 (Ground 3, claims 1 and 11) above.

6. Claim 17: “The method of claim 11, further comprising aligning a boundary of a symbol in a first forward unit of data of the forward units of data using the first synchronization signal.”

146. As explained in Sections VIII.A.1 (Ground 2, claims 1 and 11) and VIII.B.2 (Ground 3, claims 1 and 11), it is my opinion that claim 11 is anticipated by or obvious in view of Zhu and obvious in view of Zhu and DisplayPort 1.2. In my opinion, dependent claim 17, which depends from claim 11, is also obvious in view of Zhu and DisplayPort 1.2.

147. As explained in Sections VIII.A.2 (Grounds 1 and 2, claims 2 and 12) and VIII.B.3 (Ground 3, claims 2 and 12) above, the forward data stream of Zhu and DisplayPort 1.2 include SR (*first synchronization signal*), which is assigned to 8b/10b code K28.5. In my opinion, SR is a first synchronization signal that is used to align a boundary of a symbol in a first forward unit of data. DisplayPort 1.2

explains that SR is a “Link Frame Indicator” and that SR is inserted in the “MTP Header time slot every 1024th MTP as a Link Frame boundary marker.” EX1032 at 136, 165.

Table 2-65: MTP Header Control Functions

Control Function	Code/Control Symbol Sequence ²	Comment
SR (Scrambler Reset)	K28.5	Comma character; Link Frame Indicator
RESERVED	K28.1	Not used.
RESERVED	K28.7	Not used to avoid coding complication
RESERVED	K28.4	Not used for EMI reduction purpose
ACT (Allocation Change Trigger)	C0-C1-C1-C0	Trigger to downstream device indicating change in allocation on local link. ACT Control Function sequence is unique from others: its 4-code control symbol sequence spans four consecutive MTP Header time slots).

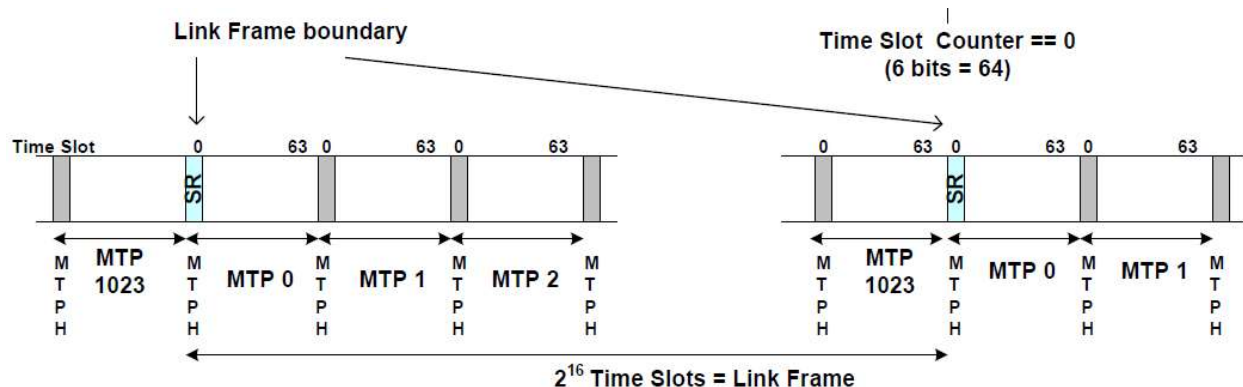


Figure 2-66: Link Timing Generation in MST Mode

148. SR is assigned a unique out-of-band symbol (comma character K28.5). In my opinion, a POSITA would understand that this sequence of bits, will only occur intentionally—that is, the K28.5 pattern is unique and particular, and a contiguous sequence of in-band symbol bits will never produce the K28.5 bit pattern.

A POSITA would further understand that, as a result, the SR symbol is a uniquely identifiable boundary marker and thus serves to align symbol boundaries in data, including “a first forward unit of data.” This is explained, for example, in the Franaszek patent, which states that a comma character such as K28.5 “indicates the proper byte boundaries and can be used for instantaneous acquisition or verification of byte synchronization.” EX1012 at 9:2-12

149. Indeed, DisplayPort 1.2 explicitly teaches that the special character K28.5 is used in Fast AUX (“FAUX”) mode “in the Preamble sequence for both bit sync and comma alignment.” EX1032 at 332; *see also id.* at 339 (describing use of K28.5 for “symbol alignment”). Moreover, Table 3-5 indicates that certain symbols are reserved in FAUX mode for USB.

Table 3-5: ANSI 8B/10B Special Characters for DisplayPort Control Symbols

Special Character	Symbol for FAUX Transactions	Comments
K28.0	XUSB_IDLE_START	RESERVED for USB, see Note 2
K28.1	RESERVED	
K28.2	XUSB_FRAME_START	See Note 2 RESERVED for USB, see Note 2
K28.3	XUSB_IDLE_END	RESERVED for USB, see Note 2
K28.4	RESERVED	See Note 1
K28.5	Preamble	K28.5 rd- is used in the Preamble sequence for both bit sync and comma alignment See Note 1
K28.6	XUSB_CRC_MARKER	RESERVED for USB, see Note 2
K28.7	Preamble/XUSB_FRAME_END	K28.7 rd- is used in the Preamble sequence for squelch detection, and it otherwise RESERVED for USB, see Note 2
K23.7	FAUX_END	
K27.7	Preamble	
K29.7	RESERVED	See Note 1
K30.7	FAUX_START	

150. In my opinion, a POSITA would understand from this teaching that the same technique could be applied to use SR (which, in MST protocol, is represented by special character K28.5) for symbol alignment on the main link, especially in combination with Zhu’s teaching of bidirectional USB communication on the main link.

151. Moreover, as explained in Section VIII.B.3 (Ground 3, claims 2 and 12), the MTP may also include control function BS. DisplayPort 1.2 explains that BS is “[i]nserted after the last active pixel during the vertical display period.” EX1032 at 45. Further, in MST mode, “[t]he BS symbol sequence is used as Stream Framing Control Symbol only.” EX1032 at 139-140.

Table 2-60: Summary of VC Payload Control Symbol Sequence		
VC Payload Control Symbol Sequence ¹	Symbol Name	Control Code Sequence
VC Payload Fill Control	VCPF	C0-C1-C2-C3 ²
Stream Control		
Stream Framing Control	BS	C0-C0-C0-C0
	BE	C1-C1-C1-C1
	SS	C3-C3-C3-C3
	SE	C6-C6-C6-C6
Stream Fill Control	SF	C4-C4-C4-C4

152. In the related litigation against Dell, UCT alleges that the BS header in the accused DisplayPort tunneling over USB4 satisfies this claim. EX1013 at 2 and

15. Thus, BS also satisfies the additional limitation of dependent claim 17 at least under UCT's interpretation of the claim in the litigation against Dell.

7. Claims 21 and 22

153. For the reasons stated below, it is my opinion that claims 21 and 22 would have been obvious in view of Zhu and DisplayPort 1.2.

a. Limitations 21.p, 21.a, 21.b, 22.p, 22.a, and 22.b

154. As explained in Sections VIII.A.4.a-c (Grounds 1 and 2, limitations 21.p, 21.a, and 21.b) and VIII.A.5.a-b (Grounds 1 and 2, limitations 22.p, 22.a, and 22.b), Zhu discloses or renders obvious these limitations.

b. “a control signal transceiver coupled to a second physical channel of the multimedia link distinct from the first physical channel and configured to at least send control data from the source device to the sink device over the second physical channel.” [21.c] / [22.c]

155. As explained in Sections VIII.A.4.d (Grounds 1 and 2, limitation 21.c) and VIII.A.5.b (Grounds 1 and 2, limitation 22.c), this limitation is disclosed in or obvious in view of Zhu. In my opinion, this claim is further obvious in view of Zhu and DisplayPort 1.2, which teaches that the DisplayPort transmitter in the source device includes “[c]ircuitry that transmits the DisplayPort Main Link data [and a]lso contains the transceiver circuit for AUX CH” (*control signal transceiver . . . configured to at least send control data from the source device to the sink device over the second physical channel*). EX1032 at Figure 1-1 and p. 28. “AUX CH”

refers to the auxiliary side-band channel of DisplayPort 1.2 referenced by Zhu (*second physical channel of the multimedia link distinct from the first physical channel*). See EX1032 at 34 (“The auxiliary channel is a half-duplex bidirectional channel used for link management and device control”). Thus, DisplayPort 1.2 discloses the control signal transceiver recited in this limitation.

C. Ground 4: Claims 1, 2, 10-12, 17, and 20-22 obvious over Lyle and the knowledge of a POSITA

156. For the reasons stated below, it is my opinion that claims 1, 2, 10-12, 17, and 20-22 of the '103 Patent would have been obvious in view of Lyle given the knowledge of a POSITA.

1. Claims 1 and 11

157. For the reasons stated below, it is my opinion that claims 1 and 11 would have been obvious in view of Lyle and the knowledge of a POSITA.

a. “A method of transmitting data over a multimedia link, comprising:” [1.p] / [11.p]

158. To the extent the preamble is limiting, it is my opinion that Lyle teaches the limitation. Specifically, Lyle discloses “[a] communication system including a transmitter, a receiver, and a TMDS-like link [*(multimedia link)*], in which video data and auxiliary data (typically including timing data associated with other auxiliary data) are transmitted from the transmitter to the receiver, or in which video data are transmitted over the link from the transmitter to the receiver, and auxiliary

data (typically including timing data associated with other auxiliary data) are transmitted from the receiver to the transmitter.” EX1008 at Abstract.

b. “over a first physical channel of the multimedia link: [sending / receiving] forward units of data from a source device [to / by] a sink device during one or more first time periods, the forward units of data comprising video data and forward [communication] data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data;” [1.a] / [11.a]

159. In my opinion, this limitation is obvious in view of Lyle and the knowledge of a POSITA. Lyle describes a TMDS link according to a Digital Video Interface (DVI) standard. EX1008 at 1:63-2:2, 27:10-20, 28:26-44. As shown in Figure 21, the TMDS link includes several channels.

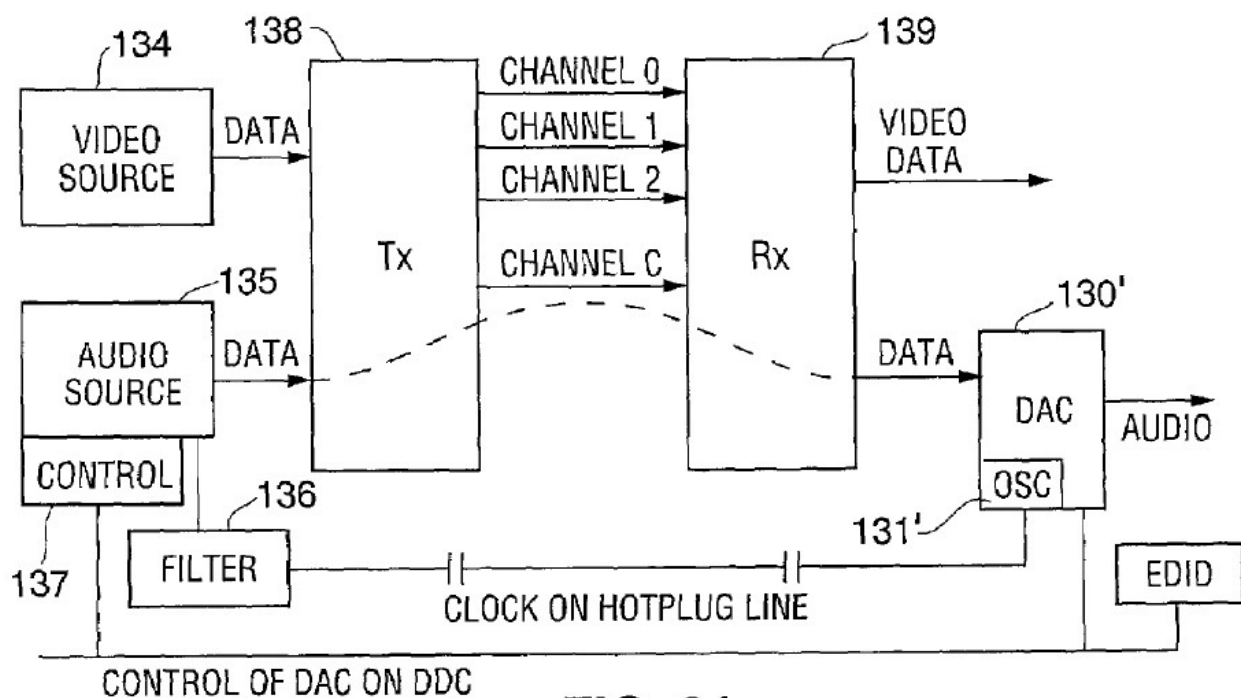


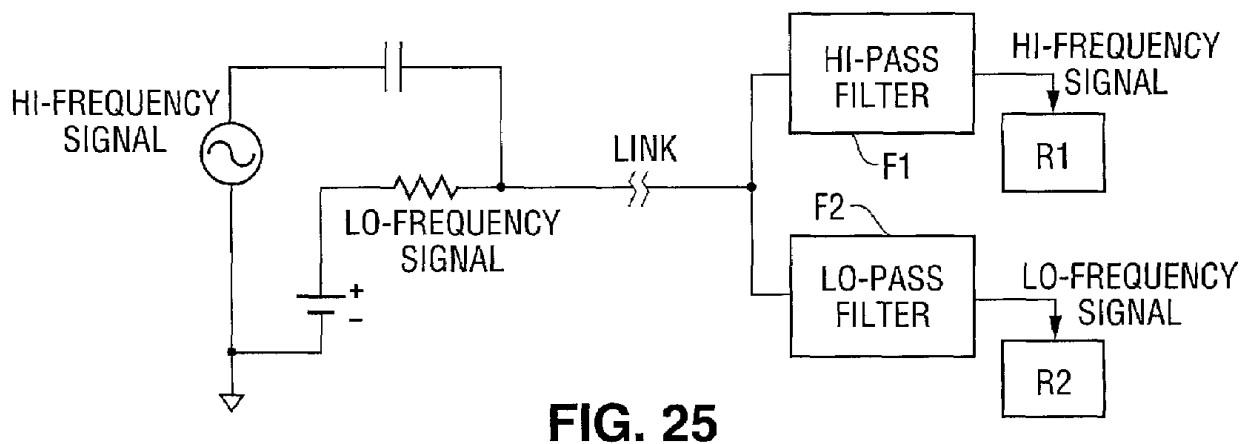
FIG. 21

EX1008 at Fig. 21; *see also id.* at Figs. 6, 19, and 29.

160. Typically, “video data are transmitted from transmitter 138 to receiver 139 over Channels 0, 1, [and] 2” (any one a *first physical channel*). EX1008 at 27:12-20. Lyle describes embodiments in which “[e]ach available conductor or channel can be employed to transmit auxiliary data (or a clock therefor) either in addition to or instead of each conventional function for which it is employed in a conventional TMDS-like link.” EX1008 at 27:49-63. Because “auxiliary data” is a broad term that encompasses “any other type of data other than video data and timing information for video data” (*id.* at 5:57-60), it is my opinion that a POSITA would understand that the auxiliary data could be USB data (*forward [communication] data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data*). Indeed, Lyle lists high-bandwidth USB data as an example of such auxiliary data. EX1008 at 50:47-54. USB is different from the standard of the video data, which, in Lyle, may be a DVI standard. EX1008 at 11:26-30. Thus, it would have been obvious that the Lyle source device could send (and the sink device receive) forward units of data comprising video data and USB data over a first physical channel (e.g., one of Channels 0-2).

161. Lyle explains that both video data and auxiliary data are transmitted in packets (*forward units of data*). EX1008 at 16:65-17:9 (describing transmitting TMDS data in packets), 19:22-60 (describing transmitting auxiliary data in packets).

162. Lyle describes several different strategies for sending video and auxiliary data on the same channel, and, in my opinion, a POSITA would find it obvious that any one of these strategies could be used to send both video and USB data over the same channel. First, Lyle describes a “frequency multiplication” technique, in which “one or more conventional signals” (e.g., video data for a Channel 0-2) are sent “as a ‘Hi-Frequency Signal’ in a first wavelength band . . . and one or more auxiliary signals” (e.g., USB data) are sent “as a ‘Lo-Frequency Signal’ in the second wavelength band.” EX1008 at 36:54-37:3; Fig. 25.



163. Second, Lyle describes a “threshold level multiplexing” technique, in which one type of data (e.g., video data) generated by a “low swing modulator” is superimposed via an adder with the other type of data (e.g., auxiliary USB data) generated by a “high swing modulator” and then the combined signal is transmitted over the TMDS channel. EX1008 at 38:13-43; Fig. 26.

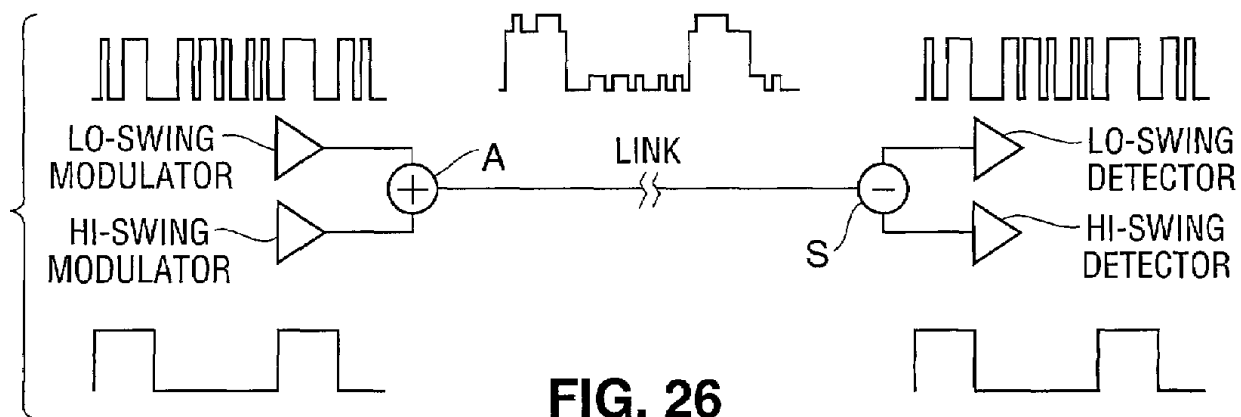


FIG. 26

164. Third, Lyle explains that “ “[i]n the specific case of a channel conventionally used for video data transmission, auxiliary data as well as video data can be sent over the channel in one or both directions using the same physical layer protocol of in-band and out-of-band characters, while at the same time using a macro layer to pack data in various protocols onto the same lines. For example, TMDS-encoded video data can be sent using in-band characters to indicate the pixel data. Using the same physical interconnect and either the same or a different in-band/out-of-band character scheme, auxiliary data can also be sent.” EX1008 at 44:54-64. In my opinion, a POSITA would understand that the in-band characters (for video pixel data) and out-of-band characters (for auxiliary data, such as USB) could be contained within a single packet for transmission on a TMDS channel.

165. Lyle also teaches a switching approach, illustrated in Figure 24, that allows “transmit[ing] auxiliary data or a clock therefor in one direction over the

channel, and some other signal in another direction over the same channel.” EX1008 at 35:25-59.

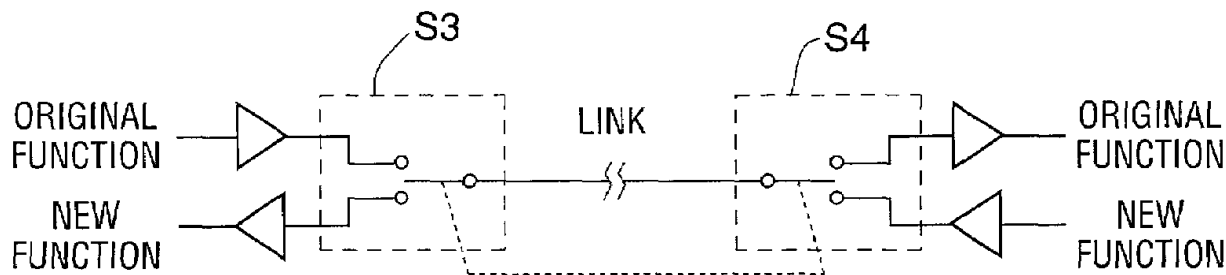


FIG. 24

166. Switches S3 and S4 can be implemented so that signals pass in opposite directions over the link during different time periods. See EX1008 at 36:9-14 and 36:49-53.

167. Lyle further teaches that “many combinations of the described auxiliary data (and clock) transmission strategies (and variations thereon) are possible” and “[f]or example, switching can be combined with frequency or level multiplexing schemes to change either the direction of auxiliary data transmission, or to eliminate conflicts or interference with conventional functions.” EX1008 at 40:5-15. Thus, Lyle teaches that the frequency multiplication, threshold level multiplexing, and/or in-band/out-of-band techniques can be combined with a switching approach such that video data and auxiliary data are transmitted from the source device to the sink device over one of Channels 0-2 (*first physical channel*) during times when the switches are set to allow forward data transmission (*first time periods*).

168. In my opinion, a POSITA would have found it obvious to make such a combination at least based on the explicit teaching / suggestion to do so found in Lyle. Moreover, such a combination would merely involve (a) combining prior art elements (the different strategies of Lyle) according to known methods to yield predictable results (ability to send video and USB data and receive USB data over the same channel) and (b) the predictable use or combination of prior art elements (the different strategies of Lyle) according to their established functions (allowing transmission of more than one data type over the same channel).

c. “over a first physical channel of the multimedia link: . . . [receiving / sending] backward units of data [at the source device from the sink device / from the sink device to the source device] during one or more second time periods, the backward units of data comprising backward [communication] data compliant with the first standard; and” [1.b] / [11.b]

169. In my opinion, this limitation is obvious in view of Lyle and the knowledge of a POSITA.

170. Lyle generally teaches that auxiliary data may be transmitted bidirectionally over the same channel of a TMDS link, including over a channel conventionally used to transmit video data. EX1008 at 44:54-59 (“[A]uxiliary data as well as video data can be sent over the channel in one or both directions[.]”). As explained in Section VIII.C.1.b (Ground 4, limitations 1.a and 11.a) above, Lyle teaches a combination of frequency multiplication, threshold level multiplexing,

and/or in-band/out-of-band techniques with a switching approach. EX1008 at 40:7-12. In such a combination, auxiliary data is sent by the sink device and received by the source device during “second time periods.” For example, auxiliary data may be sent as backward data over the channel at times when the channel is not being used to transmit forward data. EX1008 at 35:65-36:53 (describing various examples of the switching approach for bidirectional data transfer). Lyle explains that auxiliary data may be sent in the backward direction (from sink to source) by “reversing one video data transmission channel . . . during blanking periods (to send auxiliary data from the receiver of the video data to the transmitter of the video data).” EX1008 at 45:43-48; *see also id.* at 29:3-9, 46:61-67.

171. As recited in limitations 1.a and 11.a, the “first standard” is a USB standard. As explained in Section VIII.C.1.b (Ground 4, limitations 1.a and 11.a) above, Lyle teaches (and it would at least be obvious to a POSITA) that the auxiliary data of Lyle could be USB data (and that such USB data would be compliant with a USB standard).

d. “over a second physical channel of the multimedia link distinct from the first physical channel: [sending / receiving] control data from the source device to the sink device.” [1.c] / [11.c]

172. In my opinion, Lyle teaches this limitation. Specifically, Lyle discloses a DDC interface, which “provides a serial bus for bidirectional communication between the transmitter and a monitor associated with the receiver” and “employed

to initialize and authenticate an HDCP link.” EX1008 at 28:26-44; *see also id.* at 28:29-38 (“The DDC interface provides a serial bus for bidirectional communication between the transmitter and a monitor associated with the receiver in accordance with the conventional Display Data Channel standard . . . The DDC interface is also employed to initialize and authenticate an HDCP link.”), 39:50-62 (describing bidirectional transmission of . . . DDC signals” over the DDC bus), and Figs. 23-26. These DDC signals are used for control functions, such as initialization and authentication. *See id.* For example, Lyle explains that a monitor (sink device) transmits “an Extended Display Identification (‘EDID’) message that specifies various characteristics of the monitor” and a TMDS transmitter (source device) transmits “control signals for the monitor” over the DDC lines. EX1008 at 2:17-23. A POSITA would understand that the EDID message and control signals are “control data.”

173. The DDC bus (*second physical channel*) is distinct from a DVI data channel used to carry video (*first physical channel*). EX1008 at 2:2-23 (describing the DDC lines as “conductors” separate from the conductors that carry Channels 0-2). In particular, Lyle explains that “the invention typically cannot eliminate the need for all special conductors that are conventionally used for bidirectional communication between the transmitter and receiver” which would include, for example, the DDC lines. EX1008 at 47:17-23.

2. Claims 2 and 12: “The method of claim [1 / 11], further comprising [sending / receiving] a first synchronization signal of a first length after [sending / receiving] a first forward unit of data of the forward units of data, and before [sending / receiving] [another / a second] forward unit of data from the source device.”

174. As explained above, claims 1 and 11 would have been obvious in view of Lyle and the knowledge of a POSITA. In my opinion, Lyle discloses the additional limitations of dependent claims 2 and 12 (which depend from claims 1 and 11, respectively).

175. For example, Lyle teaches that “[t]he pre-reserved time slots allocated (by the specifications of the conventional DVI link) for transmission of out-of-band words indicative of control bits CTL0, CTL1, CTL2 and CTL3 allow data transmitted in these slots to be used to accomplish synchronization within a video frame.” EX1008 at 29:16-21; *see also id.* at 1:29-37 (“the encoder can generate . . . ‘out-of-band’ words in response to control or sync signals”). In particular, Lyle describes a TMDS link in which “a byte boundary is realigned only in response to the occurrence of three consecutive ones of the above-mentioned special characters” (that is, the out-of-band words indicative of control bits CTL0, CTL1, CTL2 and CTL3). *Id.* at 30:65-31:1. Thus, three consecutive instances of the special characters is a “first synchronization signal.” This first synchronization signal has a “first length” (i.e. the collective length of three out-of-band words).

176. Because this synchronization signal comprises out-of-band words transmitted as part of the data stream, it is communicated “after . . . a first forward unit of data” (i.e. video and/or USB data preceding the out-of-band words) and “before . . . another / a second forward unit of data” (i.e. video and/or USB data following the out-of-band words).

3. Claim 10 / 20: “The method of claim [1 / 11], further comprising [receiving / sending] control data from the sink device to the source device over the second physical channel of the multimedia link distinct from the first physical channel.”

177. As explained above, claims 1 and 11 would have been obvious in view of Lyle and the knowledge of a POSITA. In my opinion, Lyle discloses the additional limitations of dependent claims 10 and 20 (which depend from claims 1 and 11, respectively).

178. Lyle teaches that control data is communicated bidirectionally over the DDC bus (*second physical channel*) between a TMDS transmitter (*source device*) and a monitor (*sink device*). EX1008 at 28:26-44, 39:50-62; Section VIII.C.1.d (Ground 4, limitations 1.c and 11.c). For example, Lyle explains that the monitor transmits “an Extended Display Identification (‘EDID’) message that specifies various characteristics of the monitor” to the transmitter over the DDC lines. EX1008 at 2:17-23. Thus, Lyle teaches that control data is sent from a monitor (*sink device*) and received by a transmitter (*source device*) over the DDC bus (*second physical channel*).

4. Claim 17: “The method of claim 11, further comprising aligning a boundary of a symbol in a first forward unit of data of the forward units of data using the first synchronization signal.”

179. As explained above, claim 11 is obvious in view of Lyle and the knowledge of a POSITA. In my opinion, Lyle discloses the additional limitation of dependent claim 17, which depends from claim 11.

180. As explained in Section VIII.C.2 (Ground 4, claims 2 and 12) above, Lyle teaches a “first synchronization signal” in the form of three consecutive instances of the special characters and that this first synchronization signal is used to realign a byte boundary (*aligning a boundary of a symbol in a first forward unit of data of the forward units of data using the first synchronization signal*). Lyle further explains that “video data are encoded and then transmitted as encoded words (each 8-bit word of digital video data is converted to an encoded 10-bit word before transmission).” EX1008 at 1:26-28. A POSITA would thus understand that one byte (that is, 8 bits of data) corresponds to a “symbol” (that is, as a 10-bit encoded word) in Lyle.

5. Claim 21

181. For the reasons stated below, it is my opinion that claim 21 would have been obvious in view of Lyle and the knowledge of a POSITA.

a. “A source device for communicating data with a sink device over a multimedia link, comprising:” [21.p]

182. To the extent the preamble is limiting, it is my opinion that Lyle teaches the limitation. Lyle discloses that video source 134 and transmitter 138 (*source device*) communicates with a monitor associated with receiver 139 (*sink device*) over a DVI link (*multimedia link*). EX1008 at Fig. 21, 27:10-20, 28:26-44.

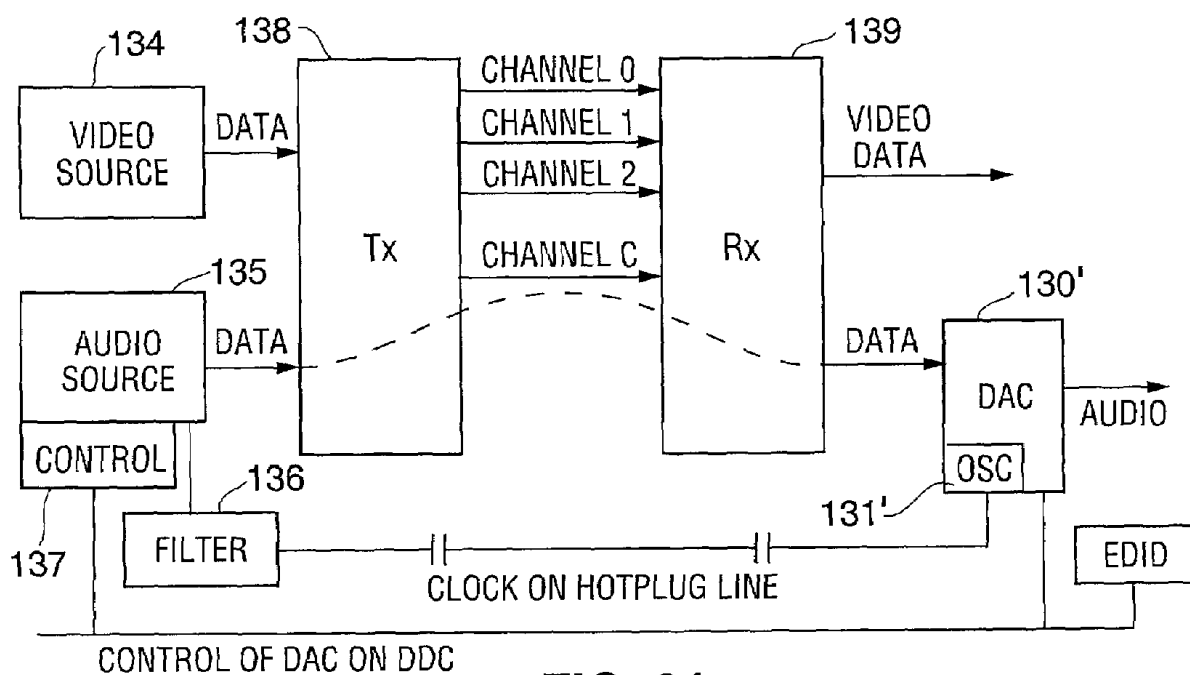


FIG. 21

b. “a transmitter coupled to a first physical channel of the multimedia link and configured to send forward units of data from the source device to the sink device over the first physical channel during one or more first time periods, the forward units of data comprising video data and forward data compliant with a first standard comprising a universal

serial bus (USB) standard and different from a standard of the video data;” [21.a]

183. As explained in Section VIII.C.1.b (Ground 4, limitations 1.a and 11.a) above, it is my opinion that limitation 1.a would have been obvious in view of Lyle and the knowledge of a POSITA. Limitation 21.a recites a “transmitter” coupled to the first physical channel and configured to perform the function recited in limitation 1.a. In my opinion, it would have been obvious to a POSITA that the transmitter disclosed in Lyle could be used to perform that function.

184. Lyle discloses a “transmitter” (e.g. transmitter 138) that is coupled to, and sends video data and auxiliary data, such as USB data, over a TMDS channel (*first physical channel of a multimedia link*). EX1008 at Fig. 21, 27:12-20, Fig. 24, 32:6-15. As discussed in Section VIII.C.1.b (Ground 4, limitations 1.a and 11.a) above, Lyle teaches the combination of, for example, either the frequency multiplier or threshold level multiplexing approach for sending video and auxiliary data in one direction over a TMDS channel with the switching approach that allows use of the same TMDS channel to send auxiliary data in the opposite direction over the same channel. As shown in the annotated Figures 24-26 below, Lyle discloses transmitters in connection with each of these approaches.

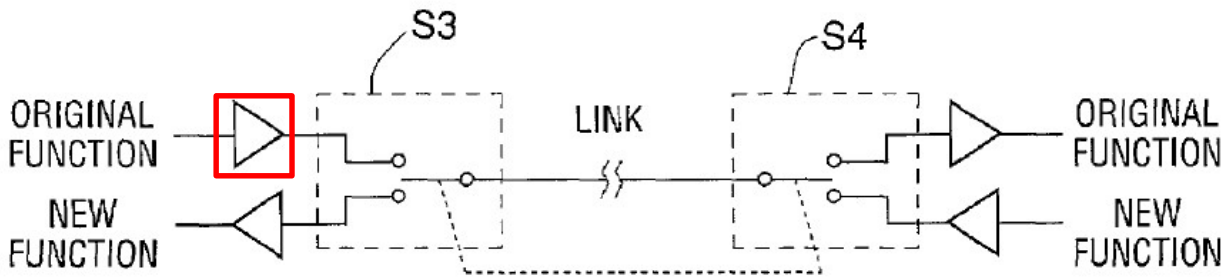


FIG. 24

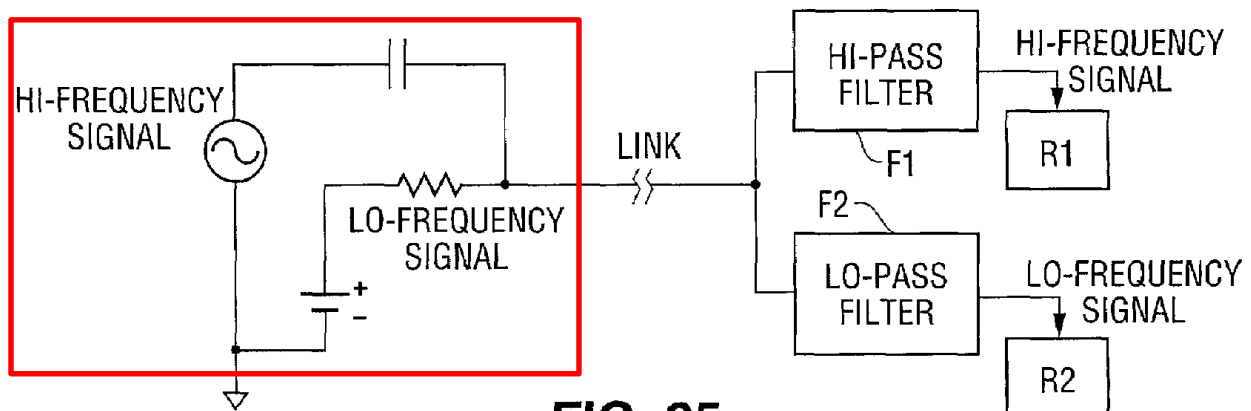


FIG. 25

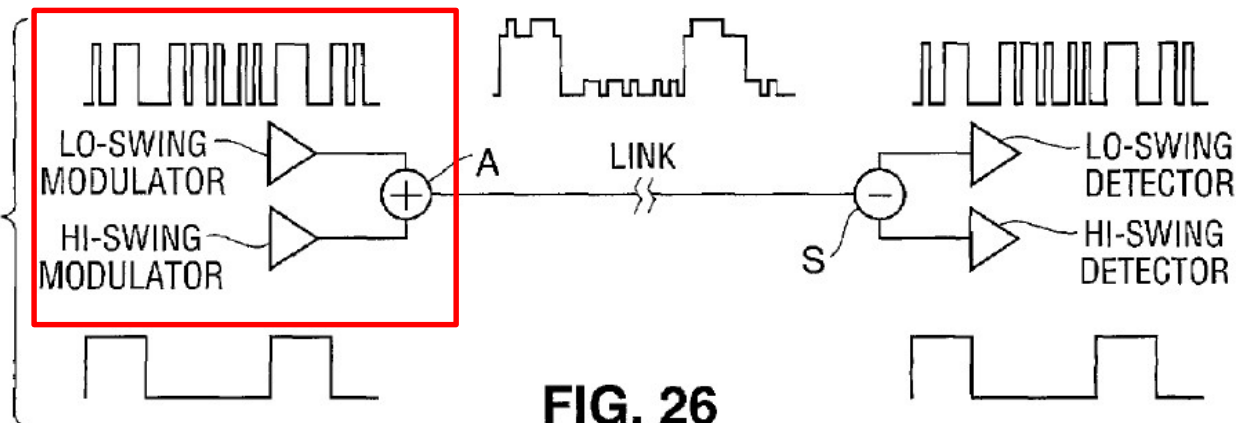


FIG. 26

c. “a receiver coupled to the first physical channel and configured to receive backward units of data at the source device from the sink device over the first physical channel during one or more second time periods, the backward units

of data comprising backward data compliant with the first standard; and” [21.b]

185. As explained in Section VIII.C.1.c above (Ground 4, limitations 1.b and 11.b), it is my opinion that limitation 1.b would have been obvious in view of Lyle and the knowledge of a POSITA. Limitation 21.b recites a “receiver” coupled to the first physical channel and configured to perform the function recited in limitation 1.b. In my opinion, it would have been obvious to a POSITA that the receiver disclosed in Lyle could be used to perform that function.

186. In connection with the switching approach, Figure 24 illustrates a receiver “configured to recover each auxiliary signal” in the source device. EX1008 at 35:25-64.

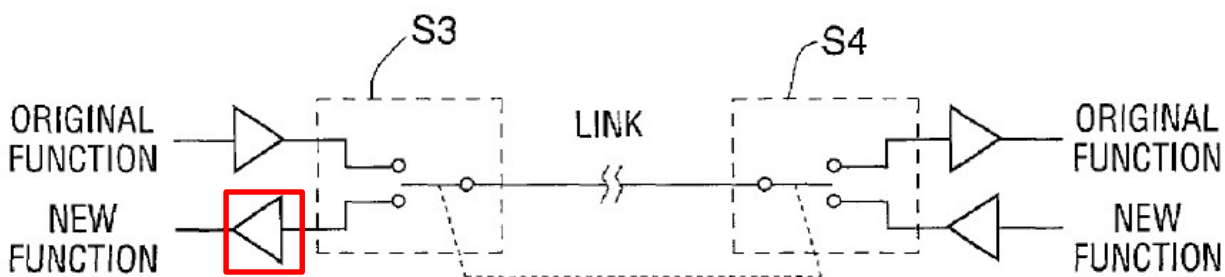


FIG. 24

EX1008 at Fig. 24 (annotated). As explained in Section VIII.C.1.c (Ground 4, limitations 1.b and 11.b) above, it would have been obvious to a POSITA that this auxiliary signal could include USB data.

d. “a control signal transceiver coupled to a second physical channel of the multimedia link distinct from the first

physical channel and configured to at least send control data from the source device to the sink device over the second physical channel.” [21.c]

187. As explained in Section VIII.C.1.d above (Ground 4, limitations 1.c and 11.c), it is my opinion that limitation 1.c is disclosed by or at least would have been obvious in view of Lyle and the knowledge of a POSITA. Limitation 21.c recites a “control signal transceiver” coupled to, and configured to perform the function recited in, limitation 1.c. In my opinion, limitation 21.c is disclosed by or obvious in view of Lyle.

188. As discussed in connection with limitations 1.c and 11.c above, Lyle discloses bidirectional communication of control data over the DDC bus (*second physical channel*). It is my opinion that a POSITA would understand this teaching in Lyle to disclose a “control signal transceiver” within the source device, coupled to the DDC bus. *See* Section VIII.A.4.d (Grounds 1 and 2, limitation 21.c).

189. As also discussed above, Lyle describes a switching approach that can be used for bidirectional communication over a TMDS channel, such as the DDC lines. A source device employing this switching approach includes a transceiver (see red box).

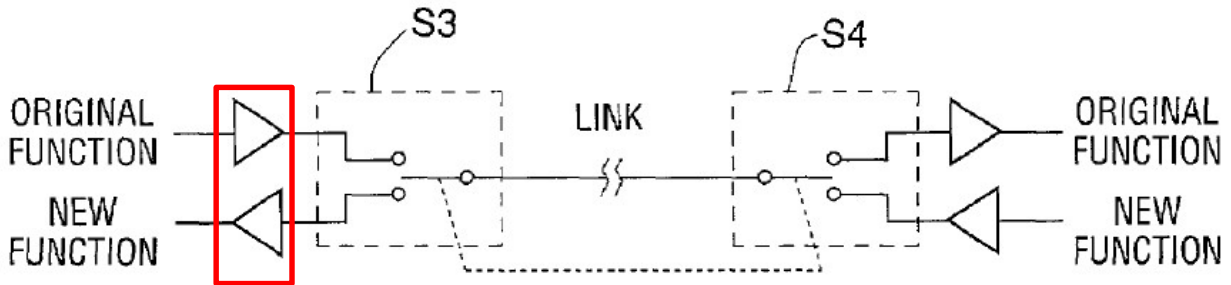


FIG. 24

EX1008 at Fig. 24 (annotated). Lyle specifically describes an example in which the switching approach is employed on the DDC channel (second physical channel).

EX1008 at 36:24-53.

190. Moreover, Figure 26 of Lyle illustrates transmitters and receivers for threshold level multiplexing.

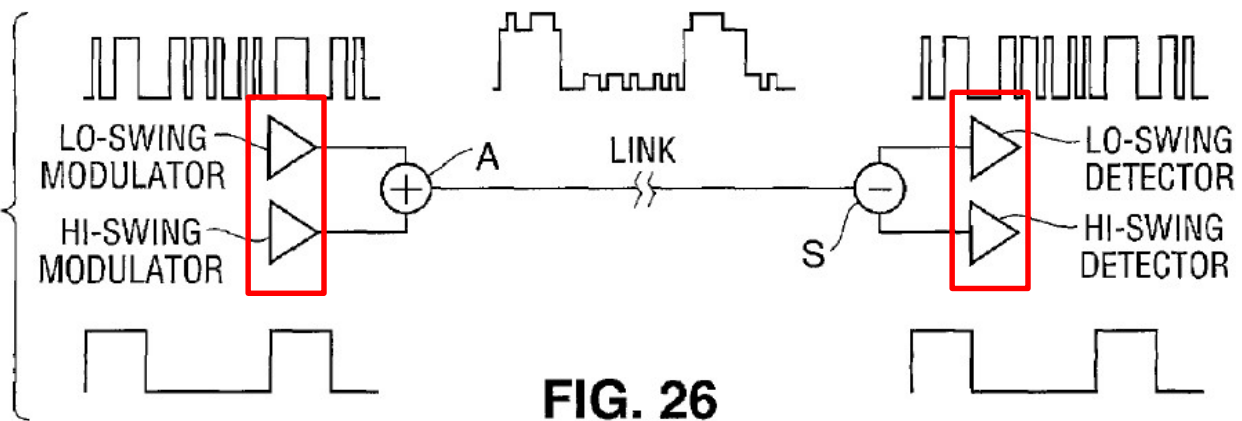


FIG. 26

EX1008 at Fig. 26 (annotated). Lyle further teaches that “since a conventional DDC bus is bidirectional, two of the FIG. 26 circuits can be included in an embodiment of the invention (one with the circuitry on the left side of FIG. 26 in the transmitter and the other with the circuitry on the right side of FIG. 26 in the transmitter) to allow

bidirectional transmission of the auxiliary data as well as the DDC signals” (*control data*). EX1008 at 39:50-62. In other words, Lyle teaches that the disclosed system could include two circuits like Figure 26, pointing in opposite directions, both attached to the DDC bus. Thus, Lyle teaches both a transmitter and receiver for control data (a *control signal transceiver*) in the source device.

191. Moreover, to the extent it is not expressly disclosed, a control signal transceiver coupled to the second physical channel would have been obvious from the teachings of Lyle. Lyle teaches bidirectional transmission between the source and sink of DDC signals (*control data*) over the DDC bus (*second physical channel*). EX1008 at 39:50-62. A POSITA would thus understand that the source device would include something that transmits and receives these signals. A device (or combination of devices) that transmits and receives signals is, by definition, a “transceiver.” EX1011 at 665 (defining “transceiver” as “[a]ny device that transmits and receives”). Even if a transceiver is narrowly defined to require a combined transmitter and receiver within a single package, in my opinion, a POSITA would have found it obvious to use such a transceiver to transmit and receive the control signals described in Lyle, as it is one of a finite number of identified, predictable solutions for transmitting and receiving signals (the other being the use of separately packaged transmitter and receiver), with a reasonable expectation of success based on the widespread use of such transceivers for this purpose.

6. Claim 22

192. Claim 22 recites substantially identical elements compared to claim 21; the only difference between the two claims is in the preamble. UCT does not distinguish between claim 21 and 22 in its infringement contentions. EX1013 at 44-45. Thus, at least according to UCT's interpretation of this claim for purposes of infringement, claim 22 is obvious over Lyle and the knowledge of a POSITA for at least the reasons explained in connection with claim 21 above.

193. Moreover, claim 22 is obvious in view of Lyle and the knowledge of a POSITA for the additional reasons explained below.

a. "A non-transitory computer readable storage medium storing instructions thereon, the instructions representing a digital design of a circuit comprising:" [22.p]

194. To the extent the preamble is limiting, the limitation is obvious in view of Lyle and the knowledge of a POSITA.

195. To the extent claim 22 recites a non-transitory memory storing a digital circuit design such as an electronic schematic file, it would have been obvious to a POSITA that instructions representing a digital design of a circuit comprising the transmitter, receiver, and control signal transceiver of Lyle could be stored on a non-transitory computer readable medium for the same reasons explained in Section VIII.A.5.a (Grounds 1 and 2, limitation 22.p), above. A POSITA would have been motivated to do so because software-based digital circuit design is a known method

that yields predictable results (a digital circuit design), would merely require applying a known technique (designing a circuit on a computer) to a known device (the circuit design described in claim 22) to yield predictable results (a digital circuit design), and would at the very least be obvious to try because digital circuit design is one of a finite number of identified, predictable solutions (others include designing a circuit by hand or building a physical circuit by trial-and-error) with a reasonable expectation of success. Moreover, digital circuit design is supported by market incentives such as the ability to design, simulate, and debug complicated circuits inexpensively.

196. However, to the extent claim 22 instead recites a memory storing instructions to perform the functions of the recited transmitter, receiver, and control signal transceiver, this would also be obvious in view of Lyle and the knowledge of a POSITA. Lyle explains that at least some aspects of a receiver may be implemented in software. EX1008 at 18:52-58, 19:29-34, and 19:45-50 (each describing receiver functions implemented in either hardware or software). Lyle further describes a software-based control signal transceiver. EX1008 at 41:7-24 (“Some implementations employ single-sided control, in which a smart agent (e.g., a software driver or firmware) on one side of the link has direct control over auxiliary data transmission and reception operating modes for both sides of the link.”). As explained in Section VIII.A.5.a (Grounds 1 and 2, limitation 22.p) above, software

implementation of transceivers (and thus, of transmitters and receivers) was well-known in the art. *See* Section VIII.A.5.a (Grounds 1 and 2, limitation 22.p). Thus, in view of this knowledge and Lyle's teaching to use software for at least some or all of the receiver and control signal transceiver functionality, and in further view of the reasons explained in Section VIII.A.5 (Grounds 1 and 2, claim 22), above, it would have been obvious to implement the transmitter, receiver, and control signal transceiver in Lyle in software.

197. It is my opinion that a POSITA would have been motivated to implement the transceiver, receiver, and control signal transceiver of Lyle in software at least because doing so would have involved (a) the simple substitution of one known element (a software-based transmitter, receiver, or transceiver) for another (hardware implementation of same) to obtain predictable results, (b) the predictable use of prior art elements (software-based transmitter, receiver, and transceiver) according to their established functions, (c) the use of known techniques (software implementation) to improve similar devices (transmitter, receiver, transceiver) in the same way, (d) applying a known technique (software implementation) to a known device transmitter, receiver, transceiver) ready for improvement to yield predictable results (transmitter, receiver, and transceiver operation), (e) choosing from a finite number of identified, predictable solutions (software or hardware), with a reasonable expectation of success, and (f) design

incentives and market forces (e.g. the lower cost, flexibility, and greater simplicity of implementing a software-based circuit). Moreover, as explained above, Lyle suggests the use of software for implementing portions of the disclosed circuit and, in my opinion, this would have further inspired a POSITA to implement the transmitter, receiver, and control signal transceiver of Lyle in software.

198. In my opinion, a POSITA would have had a reasonable expectation of success in doing so at least because, as discussed in Section VIII.A.5.a (Grounds 1 and 2, limitation 22.p), software-based transmitters, receivers, and transceivers were well known and widely used before the Priority Date.

b. Limitations 22.a, 22.b, and 22.c

199. Limitations 22.a, 22.b, and 22.c are substantially identical to limitations 21.a, 21.b, and 21.c, which, as explained in Sections VIII.A.4.b-d (Grounds 1 and 2, limitations 21.a, 21.b, 21.c), would have been obvious in view of Lyle and the knowledge of a POSITA. For the reasons stated in the previous section, it would have been obvious to a POSITA that the transmitter, receiver, and transceiver recited in these limitations could be represented by instructions stored on a computer readable storage medium.

D. Ground 5: Claims 2, 3, 12, 13, and 17 would have been obvious over Lyle and Shin

200. For the reasons stated below, it is my opinion that claims 2, 3, 12, 13, and 17 would have been obvious in view of Lyle in combination with Shin.

1. Motivation to Combine Lyle and Shin

201. The motivation to combine Lyle and Shin can be found in the teachings of the references themselves. First of all, Lyle and Shin were both assigned to Silicon Image. Lyle discusses a TMDS-based link. EX1008 at 6:25-34. Shin is cited on the face of Lyle and is noted with an asterisk, indicating that it was “cited by [the] examiner” during prosecution of Lyle. EX1008 at 2. The inventors of the Shin patent were at Silicon Image, which is where TMDS was developed, and in my opinion a POSITA would have been aware of that connection. EX1009. Although it did not coin the phrase “TMDS” or “transition-minimized differential signaling,” Shin discusses a “low transition mode” of operation and minimizing logical transitions. *See* EX1009 at Abstract. Shin also explains that the new interface “uses low-swing differential voltage which minimizes EMI” and explains that “in a high-transition mode of operation, the bits within data blocks includ[e] less than a minimum number of logical transitions.” *Id.* Moreover, Shin includes tables of TMDS symbols. EX1009 at 20:10-23:60. In my opinion, a POSITA would thus recognize Shin as a reference relating to TMDS. A POSITA would have been motivated to implement, to the extent possible, the TMDS signaling of Shin in the system disclosed in Lyle at least because it would have involved merely combining prior art elements (TMDS signaling of Shin with the TMDS-based communication system of Lyle) according to known methods to yield predictable results.

202. In my opinion, a POSITA would, therefore, be motivated to combine Lyle and Shin based on their respective teachings regarding TMDS signaling and, because Lyle applies the TMDS signaling described and defined in Shin, would have a reasonable expectation of success in making such a combination.

2. Claims 2 and 12: “The method of claim [1 / 11], further comprising [sending / receiving] a first synchronization signal of a first length after [sending / receiving] a first forward unit of data of the forward units of data, and before [sending / receiving] [another / a second] forward unit of data from the source device.”

203. As explained above, these claims (and claims 1 and 11, from which claims 2 and 12 depend) would have been obvious in view of Lyle and the knowledge of a POSITA. It is further my opinion that dependent claims 2 and 12 would have been obvious in view of Lyle and Shin.

204. As explained in Section VIII.C.2 (Ground 4, claims 2 and 12) above, Lyle discloses sending and receiving a “first synchronization signal” in the form of three consecutive out-of-band TMDS characters. Similarly, Shin teaches a “decoder synchronization module 114 [that] provides an indication to the decoder 44 of the frame boundary of each transmitted 10-bit character T[9:0].” EX1009 at 14:37-39. Shin explains that a “preamble sequence is produced by the encoder 18 at various times (e.g., at system power-up) in order to facilitate frame boundary detection by the synchronization module” and that “[d]uring each preamble period, three repetitions of the same synchronization character are produced by the encoder.” *Id.*

at 14:43-46; 15:20-28. Thus, Shin teaches sending and receiving a “first synchronization signal” (three repetitions of an out-of-band character) of a “first length” (30 bits, the length of three out-of-band characters). Because the out-of-band characters may be sent “within any preamble period” and “at various other times,” they are sent/received “after . . . a first forward unit of data” (i.e. video and/or USB data preceding the out-of-band characters) and “before . . . another / a second forward unit of data” (i.e. video and/or USB data following the out-of-band characters). *Id.* at 10:41-51.

3. Claims 3 and 13: “The method of claim [2 / 12], further comprising [sending / detecting] a second synchronization signal of a second length longer than the first synchronization signal to initialize communication over the first physical channel before [sending / receiving] the first forward unit of data.”

205. As explained in the previous section, it is my opinion that claims 2 and 12 would have been obvious in view of Lyle and Shin. In my opinion, dependent claims 3 and 13 (which depend from claims 2 and 12, respectively) would have been obvious in view of Lyle further combined with Shin.

206. As explained in the previous section, Shin teaches the transmission and reception of three consecutive out-of-band characters (*first synchronization signal*) for purposes of synchronization. Shin further teaches that an “out-of-band synchronization character[.]” (*second synchronization signal*) may be “transmitted three *or more* consecutive times within any preamble period” including “as part of

system initialization.” EX1009 at 10:41-51 (emphasis added). A POSITA would understand that system initialization initializes communication over the system, which, in the combination of Lyle and Shin, would include the first physical channel (e.g., one of TMDS Channels 0-2 of Lyle). Moreover, a POSITA would understand that initializing an idle channel may require precharging the channel to eliminate any DC imbalance. This may be achieved by sending a long string of DC-balanced symbols of the out-of-bound type. For example, in DisplayPort, idle channel initialization sequences can last up to 10ms. *See* EX1032 at 359 (explaining that the “duration of the link training period” is “10ms or less”).

207. Thus, Shin teaches sending and detecting a “second synchronization signal” (more than three consecutive out-of-band synchronization characters) of a “second length” (more than 30 bits) longer than the first synchronization signal to initialize communication over the first physical channel.

208. Also, a POSITA would understand that “system initialization” occurs to initialize the link before data is transmitted. *See, e.g.,* EX1009 at 10:45-47 (“In this regard a ‘preamble’ Sequence is sent during a preamble period preceding each transmission of encoded characters.”). Thus, a POSITA would understand that the second synchronization signal of Shin is sent “before sending/receiving the first forward unit of data.”

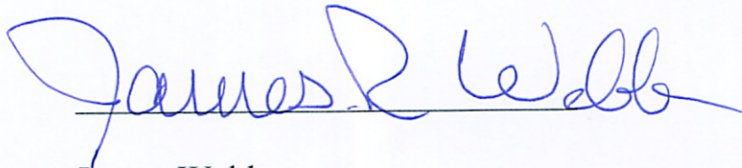
4. Claim 17: “The method of claim 11, further comprising aligning a boundary of a symbol in a first forward unit of data of the forward units of data using the first synchronization signal.”

209. As explained in Section VIII.C.4 (Ground 4, claim 17) above, in my opinion claim 17 is obvious in view of Lyle and the knowledge of a POSITA.

210. In my opinion, claim 17 is further obvious in view of Shin, which teaches using the preamble containing three or more consecutive out-of-bound characters “to facilitate frame boundary detection by the synchronization module.” EX1009 at 14:43-46. Shin further explains that “several repetitions of specially selected out-of-band characters are produced by the encoder 18 during the preamble period as a means of ensuring rapid frame boundary identification within the decoder synchronization module 114. At the conclusion of the preamble period, the module 114 will ‘know’ which of the bit lines RX[9:0] corresponds to the first bit T[0] of the 10-bit transmitted character.” *Id.* at 14:53-62. Thus, in my opinion, Shin discloses “aligning a boundary of a symbol in a first forward unit of data of the forward units of data” (the 10-bit transmitted character) using the “first synchronization signal” (three consecutive out-of-band characters).

I, James Webb, declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on 30 Sept. 2024


James Webb