

U.S. Patent No. 9,852,103 (“’103 Patent”)

Accused Products

Dell products (laptops¹, desktops², and workstations³) made, used, sold, offered for sale, or imported into the United States by Dell that support USB 4 Version 1.0 and later versions, such as the Dell Alienware m17 R5 AMD laptop (“Accused Products”), infringe at least Claims 1, 2, 3, 11, 12, 13, 17, 20, 21, and 22 of the ’103 Patent.

Claim 1

Claim 1	Exemplary Infringement Evidence
[1pre] A method of transmitting data over a multimedia link, comprising:	To the extent the preamble is limiting, each Accused Product comprises a method of transmitting data over a multimedia link.
[1a] over a first physical channel of the multimedia link: sending forward units of data from a source device to a sink device during one or more first time periods, the forward units of data comprising video data and forward data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data;	Each Accused Product comprises a method of transmitting data over a first physical channel of the multimedia link and sending forward units of data from a source device to a sink device during one or more first time periods, the forward units of data comprising video data and forward data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data. <i>See</i> [21a]
[1b] receiving backward units of data at the source device from the sink device during one or more second time periods, the backward units of data comprising backward data compliant with the first standard; and	Each Accused Product receives backward units of data at the source device from the sink device during one or more second time periods, the backward units of data comprising backward data compliant with the first standard. <i>See</i> [21b]

¹ Claims 1, 2, 3, 11, 12, 13, 17, 20, 21, and 22.

² Claims 1, 2, 3, 11, 12, 13, 17, 20, 21, and 22.

³ Claims 1, 2, 3, 11, 12, 13, 17, 20, 21, and 22.

Claim 1	Exemplary Infringement Evidence
[1c] over a second physical channel of the multimedia link distinct from the first physical channel: sending control data from the source device to the sink device.	Each Accused Product comprises a method of transmitting data over a second physical channel of the multimedia link distinct from the first physical channel and sending control data from the source device to the sink device. <i>See [21c]</i>

Claim 2

Claim 2	Exemplary Infringement Evidence
[2] The method of claim 1, further comprising sending a first synchronization signal of a first length after sending a first forward unit of data of the forward units of data, and before sending another forward unit of data from the source device.	Each Accused Product practices the method of claim 1, further comprising sending a first synchronization signal of a first length after sending a first forward unit of data of the forward units of data, and before sending another forward unit of data from the source device. For example, each accused product comprises sending a first synchronization signal of a first length as the Blanking Start (BS) header. This sync signal is sent after a first unit of data in the form of video data corresponding to a horizontal line. Another forward unit of data corresponding to the next horizontal line is only sent after the sync signal/BS header is sent. <i>See, e.g.:</i> 10.5.1 SST Tunneling The video and audio data carried over a DisplayPort SST Main-Link is organized into frames. Each frame contains several active scan lines followed by a vertical blanking period. Each scan line contains active pixel data followed by a horizontal blanking period. The active pixel data is organized into fixed-size chunks called Transfer Units. Each Transfer Unit (TU) contains active pixel data followed by Stuffing Symbols. Stuffing Symbols are also sent during the horizontal and vertical blanking periods. When a DisplayPort SST Main-Link is mapped onto USB4, the continuous Main-Link data stream is encapsulated into Tunneled Packets.

Exemplary Infringement Evidence

Figure 10-22 shows how a scan line is encapsulated into Tunneled Packets by a DP IN Adapter.

Figure 10-22. Main-Link SST Stream to Tunneled Packets

Note: DisplayPort Tunneling does not support Default Framing mode.

Universal Serial Bus 4 Specification, Version 1.0, pg. 384-385

10.5.1.3 Blank Start Packet

The Blank Start Packet has the *PDF* field in the Tunneled Packet header set to 2. It is used by a DP IN Adapter to indicate the beginning of a horizontal or vertical blanking period, reset scrambler and transfer control information at the beginning of a blanking period. A Blank Start Packet shall consist of a Blank Start header followed by packet payload. The packet payload shall contain the encoding of all 4 sets of <VB-ID, Mvid 7:0, Maud 7:0>. The Blank Start header format is shown in Figure 10-31.

Figure 10-31. Blank Start Header Format

31	24	0
S	C	
R	P	
Reserved		Fill Count
		ECC

10.5.1.3 Blank Start Packet

Claim 2	Exemplary Infringement Evidence
	The Blank Start Packet has the <i>PDF</i> field in the Tunneled Packet header set to 2. It used by a DP IN Adapter to indicate the beginning of a horizontal or vertical blanking period, reset scrambler and transfer control information at the beginning of a blanking period. A Blank Start Packet shall consist of a Blank Start header followed by packet payload. The packet payload shall contain the encoding of all 4 sets of <VB-ID, Mvid 7:0, Maud 7:0>. The Blank Start header format is shown in Figure 10-31. Figure 10-31. Blank Start Header Format 31 S R 24 C P Reserved Fill Count ECC 0

Figure 10-32. Blank Start Packet Format

4 Lanes – DP Main Link			
31	PDF = 2	*	0
	HOP ID	Length = 10h	HEC
Blank Start Header			
	VB-ID	VB-ID	VB-ID
	Mvid 7:0	Mvid 7:0	Mvid 7:0
	Maud 7:0	Maud 7:0	Maud 7:0

2 Lanes – DP Main Link			
31	PDF = 2	*	0
	HOP ID	Length = 10h	HEC
Blank Start Header			
	VB-ID	Mvid 7:0	Mvid 7:0
	Maud 7:0	VB-ID	VB-ID
	Mvid 7:0	Maud 7:0	Maud 7:0

1 Lane – DP Main Link			
31	PDF = 2	*	0
	HOP ID	Length = 10h	HEC
Blank Start Header			
	VB-ID	Mvid 7:0	VB-ID
	Mvid 7:0	Maud 7:0	Mvid 7:0
	Maud 7:0	VB-ID	Maud 7:0

* SupplD

Table 10-12. Blank Start Control Link Symbols Mapping

Claim 2	Exemplary Infringement Evidence
	Universal Serial Bus 4 Specification, Version 1.0, pg. 392-3

Claim 3

Claim 3	Exemplary Infringement Evidence
[3] The method of claim 2, further comprising sending a second synchronization signal of a second length longer than the first synchronization signal to initialize communication over the first physical channel before sending the first forward unit of data.	Each Accused Product practices the method of claim 2, further comprising sending a second synchronization signal of a second length longer than the first synchronization signal to initialize communication over the first physical channel before sending the first forward unit of data. For example, each accused product comprises sending a second synchronization signal of a second length (e.g. at least 3 DP Sync Clock Packets) longer than the first sync signal (e.g. BS header of 32 bits) to initialize communication over the first physical channel (e.g. Main lane) during/after DP Link Training that is before sending the first forward unit of data. <i>See, e.g.,</i>

Claim 3

Exemplary Infringement Evidence

10.3.4DisplayPort Over USB4 Fabric

10.3.4.1DisplayPort Data Packet Types

A DP Adapter encapsulates DisplayPort traffic into the Tunneled Packet types defined in this section. The Tunneled Packet types for DP Adapters are defined in Table 10-3 and Table 10-4. The Tunneled Packets types defined in Table 10-3 shall only be used for the AUX Path. The Tunneled Packet Types defined in Table 10-4 shall only be used for the Main-Link Path.

Table 10-3. AUX Path Tunneled Packet Types

PDF	Type	Reference
0h	AUX Packet	Section 10.3.4.2.1
1h	HPD Status Packet	Section 10.3.4.2.2
2h	SET_CONFIG Packet	Section 10.3.4.2.3
3h	ACK Packet	Section 10.3.4.2.4
4h-Fh	Reserved	

Table 10-4. Main-Link Path Tunneled Packet Types

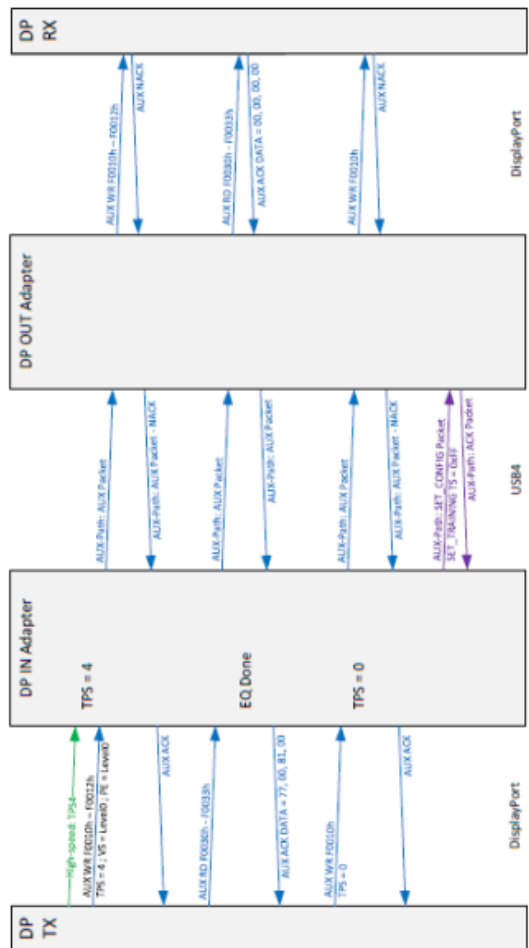
PDF	Type	Reference
0h	Reserved	
1h	SST Video Data Packet	Section 10.5.1.1
2h	SST Blank Start Packet	Section 10.5.1.3
3h	SST Main Stream Attribute Packet	Section 10.5.1.2
4h	SST Secondary Stream Packet	Section 10.5.1.4
5h	DP Clock Sync Packet	Section 10.6.1.3
6h	Multi Stream Packet	Section 10.5.2.3
7h	FEC Decode Packet	Section 10.5.3
8h-Fh	Reserved	

Universal Serial Bus 4 Specification, Version 1.0, pg. 353.

Claim 3	Exemplary Infringement Evidence
	10.4.10.1.3.2 LTTPR – EQ Phase Figure 10-19 shows a sequence of events that starts from DPTX Transmit TPS4 and ends as DPTX finishes LTTPR EQ phase: 1. TPS4 Initiate • DPTX starts transmitting TPS4. • DPTX writes TPS4 to TRAINING_PATTERN_SET_PHY_REPEATER1 and Level0 to Voltage Swing and Pre-emphasis at TRAINING_LANE0_SET_PHY_REPEATER1. 2. EQ Status • The DP IN Adapter achieves equalization, symbol lock and lanes alignment. • The DP IN starts its Lifetime Counter. • DPTX reads LTTPR's status from LANE0_1_STATUS, LANE_ALIGN_STATUS_UPDATED & ADJUST_REQUEST_LANE0_1. • The DP IN Adapter alters the AUX response according to: ◦ Its internal EQ_DONE, SYMBOL_LOCK & LANE_ALIGNMENT states. ◦ It sent three DP Clock Sync Packets. • In this example, it achieves EQ_DONE, SYMBOL_LOCK & LANE_ALIGNMENT on both Lanes and was able to send at least three DP Clock Sync Packets.

- DPTX writes 0x0 to TRAINING_PATTERN_SET_PHY_REPEATER1 signifying that DP Link training between the DPTX and the UFP of the LTPR is done.
- A DP IN Adapter sends a SET_CONFIG Packet of type SET_TRAINING with a TS field = 0xFF.

Figure 10-19. DP Link Training - LTTPR - EQ Phase



Universal Serial Bus 4 Specification, Version 1.0, pg. 377-378

Claim 3	10.6.1.3 DP Clock Sync Packet A DP Clock Sync Packet has the <i>PDF</i> field in the Tunneled Packet header set to 5. It is sent over the Main-Link Path from a DP IN Adapter to a DP OUT Adapter. A DP Clock Sync Packet shall have the format shown in Figure 10-54. Figure 10-54. DP Clock Sync Packet Format 31 0 <table><tr><td>DW0</td><td>PDF = 5</td><td>*</td><td>HOP ID</td><td>Length = 20h</td><td>HEC</td></tr><tr><td>DW1</td><td colspan="5">Reserved</td></tr><tr><td>DW2</td><td colspan="5">Reserved</td></tr><tr><td>DW3</td><td colspan="5">Window Count</td></tr><tr><td>DW4</td><td colspan="5">FLC [31:0]</td></tr><tr><td>DW5</td><td colspan="5">FLC [63:32]</td></tr><tr><td>DW6</td><td colspan="3">Reserved</td><td colspan="2">FLC [71:64]</td></tr><tr><td>DW7</td><td colspan="5">Reserved</td></tr><tr><td>DW8</td><td colspan="5">CRC32</td></tr></table> * SupplID	DW0	PDF = 5	*	HOP ID	Length = 20h	HEC	DW1	Reserved					DW2	Reserved					DW3	Window Count					DW4	FLC [31:0]					DW5	FLC [63:32]					DW6	Reserved			FLC [71:64]		DW7	Reserved					DW8	CRC32				
DW0	PDF = 5	*	HOP ID	Length = 20h	HEC																																																		
DW1	Reserved																																																						
DW2	Reserved																																																						
DW3	Window Count																																																						
DW4	FLC [31:0]																																																						
DW5	FLC [63:32]																																																						
DW6	Reserved			FLC [71:64]																																																			
DW7	Reserved																																																						
DW8	CRC32																																																						

Claim 3	Exemplary Infringement Evidence
	10.6.2.1 DP IN Adapter Requirements A DP IN Adapter shall: • Implement a Lifetime Counter as described in Section 10.6.1.1.2. • Implement the logic to perform the LC filtering. • Update FLC upon an Update Counter Event. • Upon the first Measure Window Event: ○ Capture the current FLC. ○ Store the current captured FLC to be used as previous captured FLC at the next Measure Window Even. • Upon each subsequent Measure Window Event: ○ Capture the current FLC. ○ Compute the Window Count by calculating the current captured FLC minus the FLC that was captured at the previous Measure Event. ○ Construct a DP Clock Sync Packet and send it over the Main-Link Path within <code>T_{CLOCK_SYNC}</code> after the Measure Window Event. ○ Store the current captured FLC to be used as previous captured FLC at the next Measure Window Event.

Claim 3	Exemplary Infringement Evidence
	<i>Note: A DP IN Adapter may send a DP Clock Sync Packet before DP Link Training is completed.</i> 10.6.2.2 DP OUT Adapter Requirements A DP OUT Adapter shall: • Implement a Lifetime Counter as described in Section 10.6.1.2. • Implement the logic to perform the LC filtering. • Update FLC upon an Update Counter Event. • Upon a Measure Window Event: ○ Capture the current FLC. ○ Compute the Window Count as described in Section 10.6.1.3. • Upon receiving a DP Clock Sync Packet after the Measure Window Event and before the PLL Adjust Event, compute the PLL frequency adjustment. The method for computing the PLL frequency adjustment is outside the scope of this specification. • Upon an Adjust PLL Event, adjust the PLL frequency based on the computation performed at the Measure Window Event. If a DP OUT Adapter receives a DP Clock Sync Packet after an Adjust PLL Event but before the next Measure Window Event, it shall not adjust the PLL and shall silently discard the packet. If a DP OUT Adapter receives a DP Clock Sync Packet before it computed the first Window Count, it shall not adjust the PLL and shall silently discard the packet. When a DP OUT Adapter changes the DisplayPort Main-Link transmitter frequency as a result of adjusting the PLL frequency, it shall adhere to the DisplayPort 1.4a Specification. The PLL frequency adjustment shall be completed within tDPPLLAdjust after the Adjust PLL Event. Universal Serial Bus 4 Specification, Version 1.0, pg. 416- 418.

Claim 10

Claim 10	Exemplary Infringement Evidence
[10] The method of claim 1, further comprising receiving control data from the sink device to the source device over the second physical channel of the multimedia link distinct from the first physical channel.	Each Accused Product practices the method of claim 1, further comprising receiving control data from the sink device to the source device over the second physical channel of the multimedia link distinct from the first physical channel. For example, each accused product comprises a control signal transceiver (e.g., USB4 DFP port controller) coupled to a second physical channel (e.g., Sideband Channel) of the multimedia link distinct from the first physical channel (e.g., Lane 0 or bonded Lane 0 and Lane 1) and configured to receive control data (e.g., USB4 Port Connect/Disconnect; Lane Initialization and Endable/Disable; entry or exit from Sleep state, etc.) from the sink device to the source device over the second physical channel (e.g., Sideband channel). See [21c]

Claim 11

Claim 11	Exemplary Infringement Evidence
[11pre] A method of transmitting data over a multimedia link, comprising:	To the extent the preamble is limiting, each Accused Product comprises a method of transmitting data over a multimedia link.
[11a] over a first physical channel of the multimedia link: receiving forward units of data from a source device by a sink device during one or more first time periods, the forward units of data comprising video data and forward communication data compliant with a first standard comprising a universal serial bus	Each Accused Product comprises a method of transmitting data over a first physical channel of the multimedia link and receiving forward units of data from a source device by a sink device during one or more first time periods, the forward units of data comprising video data and forward communication data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data. See [21a]

Claim 11	Exemplary Infringement Evidence
(USB) standard and different from a standard of the video data;	
[11b] sending backward units of data from the sink device to the source device during one or more second time periods, the backward units of data comprising data comprising backward communication data compliant with the first standard; and	Each Accused Product sends backward units of data from the sink device to the source device during one or more second time periods, the backward units of data comprising backward communication data compliant with the first standard. <i>See</i> [21b]
[11c] over a second physical channel of the multimedia link distinct from the first physical channel: receiving control data from the source device to the sink device.	Each Accused Product comprises a method of receives control data from the source device to the sink device over a second physical channel of the multimedia link distinct from the first physical channel. <i>See</i> [21c]

Claim 12

Claim 12	Exemplary Infringement Evidence
[12] The method of claim 11, further comprising receiving a first synchronization signal of a first length after receiving a first forward unit of data of the first length after receiving a first forward unit of data of the first forward unit of data of the forward units of data, and before receiving a second forward unit of data from the source device.	Each Accused Product practices the method of claim 11, further comprising receiving a first synchronization signal of a first length after receiving a first forward unit of data of the forward units of data, and before receiving a second forward unit of data from the source device. <i>See</i> [2]

Claim 13

Claim 13	Exemplary Infringement Evidence
[13] The method of claim 12, further comprising detecting a second synchronization signal of a second length longer than the first synchronization signal to initialize communication over the first physical channel before receiving the first forward unit of data.	Each Accused Product practices the method of claim 12, further comprising detecting a second synchronization signal of a second length longer than the first synchronization signal to initialize communication over the first physical channel before receiving the first forward unit of data. <i>See</i> [3]

Claim 17

Claim 17	Exemplary Infringement Evidence
[17] The method of claim 11, further comprising aligning a boundary of a symbol in a first forward unit of data of the forward units of data using the first synchronization signal.	Each Accused Product practices the method of claim 11, further comprising aligning a boundary of a symbol in a first forward unit of data of the forward units of data using the first synchronization signal. <i>See</i> [2]

Claim 20

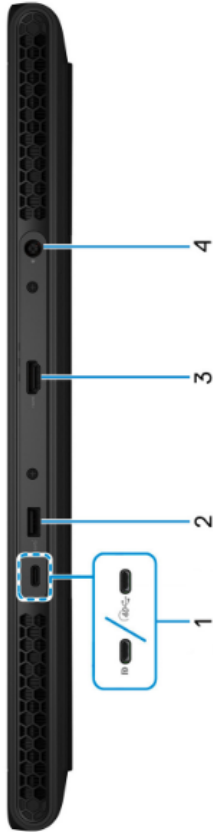
Claim 20	Exemplary Infringement Evidence
[20] The method of claim 11, further comprising sending control data from the sink device to the source device over the second physical channel of the multimedia link distinct from the first physical channel.	Each Accused Product practices the method of claim 11, further comprising sending control data from the sink device to the source device over the second physical channel of the multimedia link distinct from the first physical channel. <i>See</i> [10]

Claim 21

Claim 21	Exemplary Infringement Evidence
[21pre] A source device for communicating data with a sink device over a multimedia link, comprising:	To the extent the preamble is limiting, each Accused Product comprises a source device for communicating data with a sink device over a multimedia link. For example, an exemplary Dell Alienware m17 R5 AMD laptop comprises a source device (USB4 Host) for communicating data with a sink device (USB4 Device/Peripheral Device) over a multimedia link (USB 4 link for DisplayPort 1.4 video and USB data). The USB 4 standard supports display tunneling based on DisplayPort protocol. <i>See, e.g.:</i> Alienware m17 R5 AMD A photograph of a Dell Alienware m17 R5 AMD laptop. The laptop is black with a glowing blue Alienware logo on the lid. The screen is open, showing a dark background with the Alienware logo. The laptop is shown from a front-three-quarter view.

Claim 21

Exemplary Infringement Evidence



1. **USB 3.2 Gen 2 (Type-C) port with DisplayPort, for computers with a NVIDIA GeForce RTX 3050 Ti graphics card**
Connect devices such as external storage devices, printers, and external displays. Provides data transfer rate of up to 10 Gbps. Supports DisplayPort 1.4 and also enables you to connect an external display using a display adapter.
- ① **NOTE:** A USB Type-C to DisplayPort adapter (sold separately) is required to connect a DisplayPort device.
- USB 4.0 40 Gbps (Type-C) port with DisplayPort, for computers with a NVIDIA GeForce RTX 3060/3070 Ti/3080/3080 Ti and AMD Radeon RX 6700M/RX 6850M XT graphics card**
Supports USB4, DisplayPort 2.0, and also enables you to connect to an external display using a display adapter. Provides data transfer rates of up to 40 Gbps for USB4.

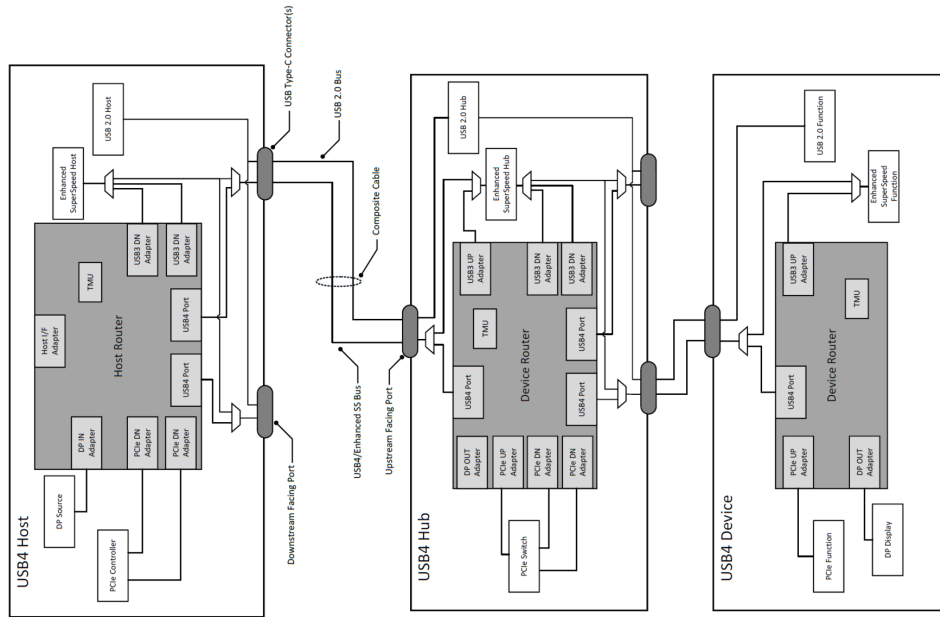
<https://dl.dell.com/content/manual/7958950-alienware-m17-r5-amd-setup-and-specifications.pdf?language=en-us>

Term/Abbreviation	Description
Receiver	The receiver in a Lane Adapter.
Transaction	The unit of communication across the Sideband Channel. A Transaction consists of a set of defined symbols. There are three types of Transactions: LT Transactions, AT Transactions, and RT Transactions.

Claim 21	Exemplary Infringement Evidence	
	Sideband (SB) Channel	The connection between the USB4 Ports of two interconnected Routers that provides initial communication and setup functionality.
	Transmitter	Refers to a USB4 Transmitter.
	Universal Serial Bus 4 Specification, Version 1.0, pg. 8-9. 2 Architectural Overview This chapter presents an overview of Universal Serial Bus 4 (USB4™) architecture and key concepts. USB4 is similar to earlier versions of USB in that it is a cable bus supporting data exchange between a host computer and a wide range of simultaneously accessible peripherals. However, USB4 also allows a host computer to setup data exchange between compatible peripherals. The attached peripherals share bandwidth as configured by the host computer. The bus allows peripherals to be attached, configured, used, and detached while the host and other peripherals are in operation. When configured over a USB Type-C® connector interface, USB4 functionally replaces USB 3.2 while retaining USB 2.0 bus operating in parallel. Enhanced SuperSpeed USB, as defined in USB 3.2, remains the fundamental architecture for USB data transfer on a USB4 Fabric. The difference with USB4 versus USB 3.2 is that USB4 is a connection-oriented, tunneling architecture designed to combine multiple protocols onto a single physical interface, so that the total speed and performance of the USB4 Fabric can be dynamically shared. USB4 allows for USB data transfers to operate in parallel with other independent protocols specific to display, load/store and host-to-host interfaces. Additionally, USB4 extends performance beyond the 20 Gbps (Gen 2 x 2) of USB 3.2 to 40 Gbps (Gen 3 x 2) over the same dual-lane, dual-simplex architecture. This specification introduces the concept of protocol tunneling to USB bus architecture. Besides tunneling Enhanced SuperSpeed USB (USB3), display tunneling based on DisplayPort (DP) protocol and load/store tunneling based on PCI Express (PCIe) are defined. These protocol tunnels operate independently over the USB4 transport and physical layers. Additionally, USB4 allocates packets for bus configuration and management, and packets can be allocated specifically for host-to-host data connections. Universal Serial Bus 4 Specification, Version 1.0, pg. 10.	

Claim 21	Exemplary Infringement Evidence
	2.1 USB4 System Description Figure 2-1 illustrates the dual bus architecture of USB 3.2 as augmented by USB4. As architected, backward compatibility is supported with minimum interoperability starting at USB 2.0, working up through USB 3.2, and finally up to USB4 based on the highest common bus level supported across the interconnected components. Protocol tunnels are interfaced via Protocol Adapters specific to each protocol. For USB and PCIe protocols, native USB hubs and PCIe switches are required to handle protocol-related packet routing and buffering. For display tunneling, no intermediate DP-specific logic is required with display tunnels being established as an end-to-end link. Time synchronization across a USB4 Fabric uses distributed time management units (TMUs) associated with each Router.

Figure 2-1. USB4/USB3.2 Dual Bus System Architecture



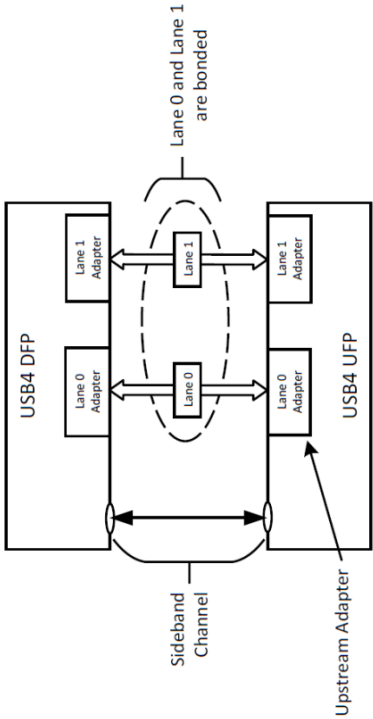
Universal Serial Bus 4 Specification, Version 1.0, pg. 10-11.

Claim 21	Exemplary Infringement Evidence
	2.1.1.4 USB4 Devices 2.1.1.4.1 USB4 Peripheral Device A USB4 peripheral device has a single Upstream Facing Port. It does not have any Downstream Facing Ports. A USB4 peripheral device contains a Device Router and can also optionally contain one or more of the following: • An Enhanced SuperSpeed hub or endpoint. • A PCIe switch or endpoint. • A DisplayPort Source or Sink. A USB4 peripheral device supports 20G USB4 operation (Gen2x2) and optionally 40G USB4 operation (Gen3x2). 2.1.1.4.2 USB4 Hub At a high level, a USB4 hub is functionally similar to a USB 3.2 hub – it consists of one Upstream Facing Port and one or more Downstream Facing Ports. USB4 hub functionally operates as a tree-like structure for enabling one or more Downstream Facing Ports to be served by one Upstream Facing Port, typically for the purpose of port expansion. In addition to the USB4-specific hub functionality, USB 3.2 and USB 2.0 hub functionality is supported such that Downstream Facing Ports of a USB4 hub can support backward - compatibility with USB 3.2 and USB 2.0 devices.

Claim 21	Exemplary Infringement Evidence
	A USB4 hub contains: • A Device Router. • An Enhanced SuperSpeed USB hub. • A PCIe switch. • A USB 2.0 hub. A USB4 hub supports 20G USB4 operation (Gen2x2) and 40G USB4 operation (Gen3x2). A USB4 hub is required to support DisplayPort Alt Mode on all of its DFP. See the USB Type-C Specification for a full definition of the requirements and details regarding DisplayPort Alt Mode support on a DFP. 2.1.1.5 USB4 Host A USB4 host contains: • A Host Router. • An internal host controller. • A DisplayPort Source. A USB4 host can also optionally contain a PCIe controller. A USB4 host supports 20G USB4 operation (Gen2x2) and optionally 40G USB4 operation (Gen3x2). A USB4 host is required to support DisplayPort Alt Mode on all of its DFP. See the USB Type-C Specification for a full definition of the requirements and details regarding DisplayPort Alt Mode support on a DFP. Universal Serial Bus 4 Specification, Version 1.0, pg. 14-15.

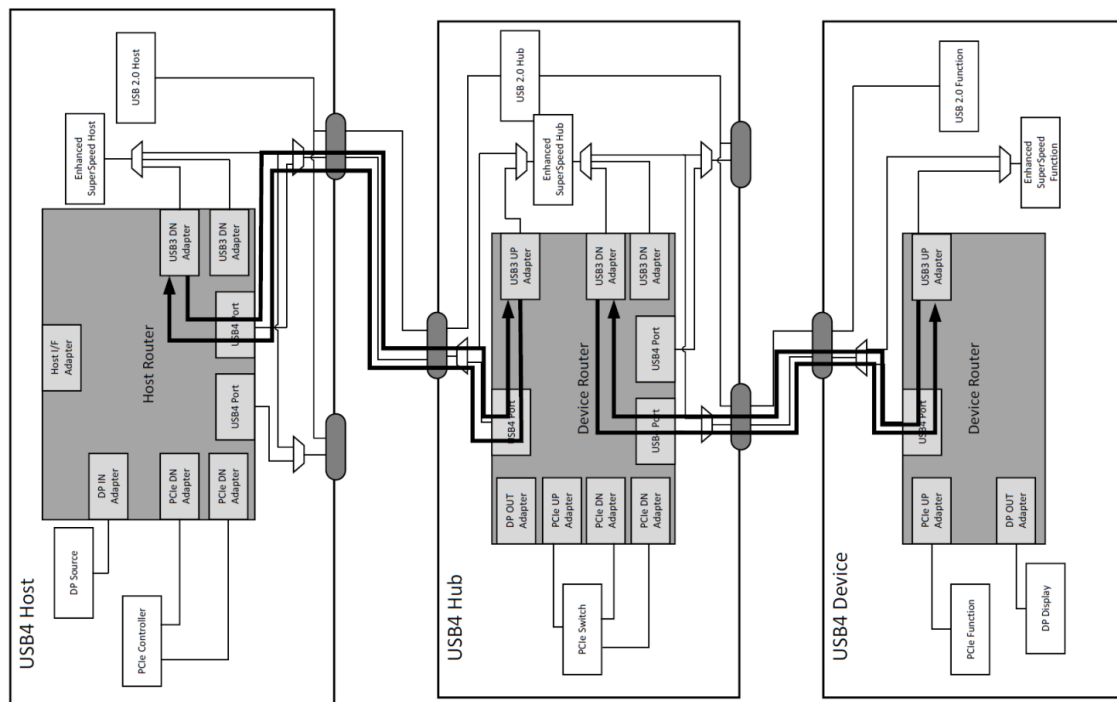
Claim 21	Exemplary Infringement Evidence
	A USB4 host shall support DP tunneling. A Host Router shall contain at least one DP IN Adapter and may optionally contain one or more DP OUT Adapters. A USB4 hub shall support DP Tunneling. A USB4 Hub shall contain at least one DP OUT Adapter and may optionally contain one or more DP IN Adapters. <i>Note: The DP OUT Adapter in a USB4 hub is to enable a DisplayPort Sink connected on a DFP (or non-USB display connector if USB4 hub is a USB4-Based Dock). See the USB Type-C Specification for more details.</i> Universal Serial Bus 4 Specification, Version 1.0, pg. 346.
[21a] a transmitter coupled to a first physical channel of the multimedia link and configured to send forward units of data from the source device to the sink device over the first physical channel during one or more first time periods, the forward units of data comprising video data and forward data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data;	Each Accused Product comprises a transmitter coupled to a first physical channel of the multimedia link and configured to send forward units of data from the source device to the sink device over the first physical channel during one or more first time periods, the forward units of data comprising video data and forward data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data. For example, each accused product comprises a transmitter (e.g., USB4 DFP which has a transceiver for transmitting data) coupled to a first physical channel (e.g., Lane 0 or bonded Lane 0 and Lane 1 of the USB4 port) of the multimedia link (e.g., USB4 link) and configured to send forward units of data from the source device to the sink device over the first physical channel during one or more first time periods (e.g., forward sending periods when single directional DP data are sent with USB data), the forward units of data comprising video data (e.g., DisplayPort 1.4 video via DisplayPort Adapter Layer Tunneled Packets) and forward data with a first standard (e.g., USB 2.0 Packets and/or USB3 Adapter Layer Tunneled Packets) comprising a universal serial bus (USB) standard and different from a standard of the video data (e.g., DisplayPort video data). <i>See, e.g.,</i>

Claim 21	Exemplary Infringement Evidence
	2.1.1.1.3 USB4 Ports and Links A USB4 Port is the entity that provides the USB4 functional interface that resides on each end of a USB4 Link. It consists of the transmit and receive Lanes of the USB4 data bus along with a two-wire Sideband (SB) Channel (SBTX/SBRX). USB4 Ports operate as either a Single-Lane Link or Dual-Lane Link. When operating as a Single-Lane Link, Lane 1 of the USB4 Port is disabled. When operating as a Dual-Lane Link, Lanes 0 and 1 are logically bonded together to provide a single data channel. Figure 2-2 shows a Single-Lane Link. Figure 2-3 shows a Dual-Lane Link. Figure 2-2. Single-Lane USB4 Link The diagram illustrates a Single-Lane USB4 Link between a USB4 DFP (Downstream Facing Port) on the left and a USB4 UFP (Upstream Facing Port) on the right. Each side contains a 'Lane 0 Adapter' and a 'Lane 1 Adapter'. A 'Sideband Channel' is shown as a curved line connecting the two ports. A 'Lane 1' box is shown between the adapters, with an arrow pointing to it from the text 'Lane 1 is disabled'. An arrow labeled 'Upstream Adapter' points to the 'Lane 0 Adapter' on the UFP side. Bidirectional arrows connect the 'Lane 0 Adapter' on the DFP to the 'Lane 0 Adapter' on the UFP, and the 'Lane 1 Adapter' on the DFP to the 'Lane 1 Adapter' on the UFP.

Claim 21	Exemplary Infringement Evidence
	Figure 2-3. Dual-Lane USB4 Link  The primary communication channel of the USB4 Fabric is over the USB4 Link that interconnects two USB4 Ports. The USB4 Link transports packets for both Tunneler Protocol traffic and bus management traffic between Routers. The Sideband Channel of a USB4 Port is used to initialize and manage the USB4 Link between the USB4 Ports. For a USB4-enabled USB Type-C port, the complete interface includes a USB4 Port, a USB 2.0 data bus, and the USB Type-C Configuration Channel (CC) along with power/ground (V_{BUS}, V_{CONN} and GND). Universal Serial Bus 4 Specification, Version 1.0, pg. 12-13.

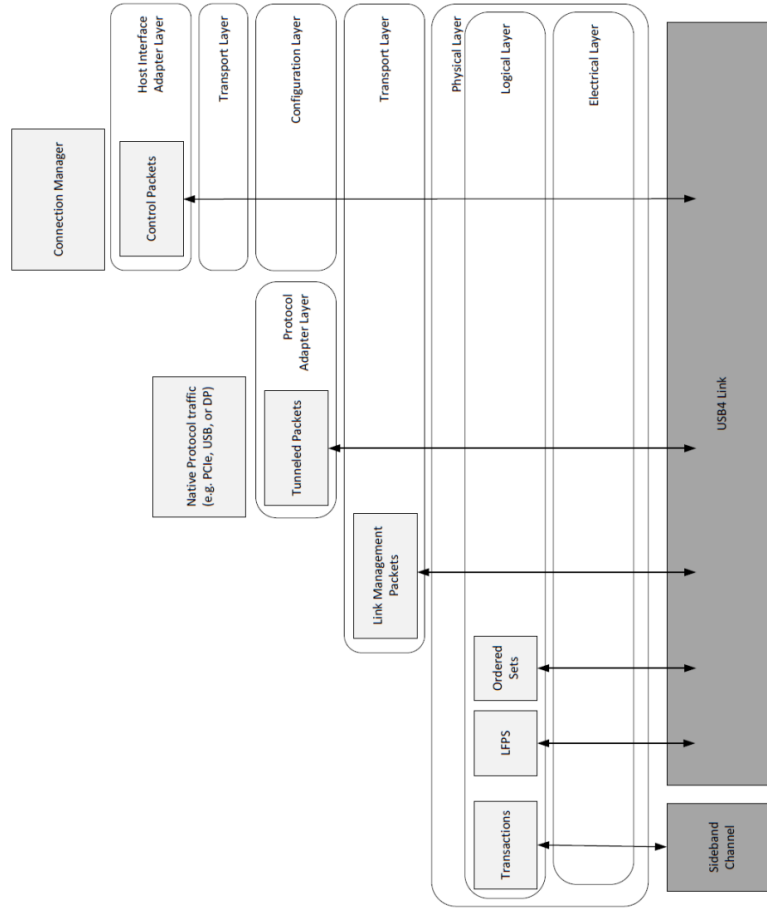
Claim 21	Exemplary Infringement Evidence
	2.1.1.5 USB4 Host A USB4 host contains: • A Host Router. • An internal host controller. • A DisplayPort Source. A USB4 host can also optionally contain a PCIe controller. A USB4 host supports 20G USB4 operation (Gen2x2) and optionally 40G USB4 operation (Gen3x2). A USB4 host is required to support DisplayPort Alt Mode on all of its DFP. See the USB Type-C Specification for a full definition of the requirements and details regarding DisplayPort Alt Mode support on a DFP. Universal Serial Bus 4 Specification , Version 1.0, pg. 14. 2.2.3 Paths A Path represents a directional logical connection over the USB4 Fabric. A Path is defined either between two Protocol Adapters or between the Connection Manager and a Control Adapter. A Path can be end-to-end (as is the case for Display and Host-to-Host Tunneling) or it can traverse a single USB4 Link (as is the case for USB3 tunneling and PCIe Tunneling). Figure 2-9 shows an example of a set of Paths that tunnel USB3 traffic between a USB4 host and a USB4 device.

Figure 2-9. Paths across a USB4 Fabric



Claim 21	Exemplary Infringement Evidence
	A Tunnel is configured end-to-end before data transfer can take place. Each packet carries an identifier (called a HopID) that identifies the Path in the context of a given Link. The HopID is configured by a Connection Manager and can vary across each Link in the Path. When a Router receives a packet, it uses the HopID to determine the packet's next HopID and which Egress Adapter to forward the packet to. 2.2.4 Communication Constructs Figure 2-10 shows the various constructs that are used for communication over the USB4 Fabric.

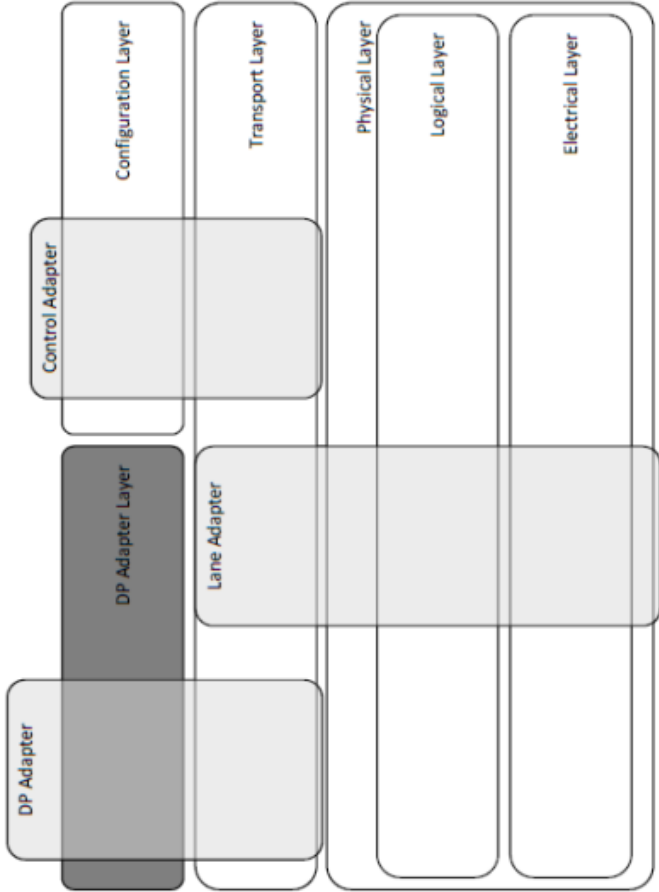
Figure 2-10. USB4 Communication by Functional Layer



Universal Serial Bus 4 Specification, Version 1.0, pg. 19-20.

Claim 21	Exemplary Infringement Evidence
	9 USB3 Tunneling The diagram illustrates the USB3 Tunneling architecture. It features a central 'USB3 Adapter Layer' (dark grey rectangle). To its left is a 'USB3 Adapter' (light grey rectangle) and to its right is a 'Control Adapter' (light grey rectangle). Below the 'USB3 Adapter Layer' is a 'Lane Adapter' (light grey rectangle). The entire structure is overlaid on a background of layers: 'Configuration Layer' at the top, 'Transport Layer' below it, and a 'Physical Layer' at the bottom. The 'Physical Layer' is further divided into 'Logical Layer' and 'Electrical Layer'. USB4™ Hosts: A USB4 host shall support USB3 tunneling. The Host Router in a USB4 host shall have one Downstream USB3 Adapter per Downstream Facing Port. Each Downstream USB3 Adapter shall interface to a downstream port on the host controller. USB4 Hubs: A USB4 hub shall support USB3 tunneling. A USB4 hub shall incorporate an internal USB SuperSpeed Plus hub per the USB 3.2 Specification with the modifications defined in this chapter.

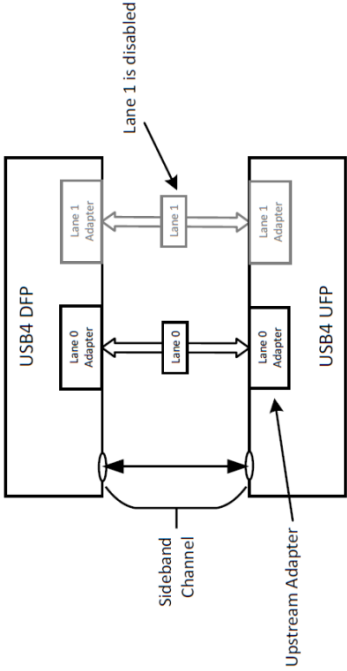
Claim 21	Exemplary Infringement Evidence
	9.1 USB3 Adapter Layer 9.1.1 Encapsulation When a USB3 Adapter Layer receives one of the USB3 constructs listed in this section from the internal USB3 device, it encapsulates the construct in a Tunneled Packet then passes it to the Transport layer for transmission over the USB4 fabric. The USB3 Adapter Layer encapsulates the following USB3 constructs: • Low Frequency Periodic Signaling (LFPS). • Ordered Sets. • Link Commands. • Link Management Packets (LMP). • Transaction Packets (TP). • Isochronous Timestamp Packets (ITP). • Data Packets (DP). Universal Serial Bus 4 Specification, Version 1.0, pg. 329-330.

Claim 21	Exemplary Infringement Evidence
	10 DisplayPort™ Tunneling  This chapter describes DP IN and DP OUT Adapters, which tunnel DP traffic over the USB4™ Fabric. This chapter only applies to USB4 products that implement DisplayPort Source or Sink. A USB4 host shall support DP tunneling. A Host Router shall contain at least one DP IN Adapter and may optionally contain one or more DP OUT Adapters. A USB4 hub shall support DP Tunneling. A USB4 Hub shall contain at least one DP OUT Adapter and may optionally contain one or more DP IN Adapters.

Claim 21	Exemplary Infringement Evidence
	10.1.2 Protocol Adapter Layer The Protocol Adapter Layer in a DP IN Adapter encapsulates Main-Link data and AUX channel transactions into Tunneled Packets for transmission over the USB4 Fabric. It also reconstructs AUX channel transactions from Tunneled Packets received over the USB4 Fabric. The Protocol Adapter Layer in a DP OUT Adapter reconstructs Main-Link data and AUX channel transactions from Tunneled Packets received over the USB4 Fabric. It also encapsulates AUX channel transactions into Tunneled Packets for transmission over the USB4 Fabric. 10.1.3 DP Physical Layer A DP Adapter shall either implement the DisplayPort Physical Layer as defined in the DisplayPort 1.4a Specification or shall implement its functional equivalent (e.g. DP Adapter is connected to a DPRX or a DPTX as part of an SoC). A DP IN Adapter which does not implement a Physical Layer shall generate a stream of DisplayPort Tunneled packets as if a Physical Layer exists. This is to ensure that a DP OUT Adapter can properly reconstruct the DisplayPort Physical stream. Universal Serial Bus 4 Specification, Version 1.0, pg. 347.

Claim 21	Exemplary Infringement Evidence USB4™ Host – DisplayPort™ Requirements • USB4 Host DisplayPort requirements are fairly straight forward • USB4 Host Must Support: • USB4 Fabric Configuration: Minimum of 2 lanes at 10 Gbps (Gen 2 x 2) • USB 3.2 Data Transport, USB 2.0 Native • DisplayPort • DisplayPort tunneling through USB4 • DisplayPort Alt Mode on all of it's DFPs The diagram illustrates the USB4 Host System architecture and network topology. The top part shows a 'USB4 Host System' block containing a 'CPU + GPU' section with 'USB2 Host', 'USB3 Host', 'DisplayPort Source', and 'PCIe Controller' components. These are connected to a 'USB4 Host Router' section which includes a 'USB3 Adapter', 'DP Input Adapter', and 'PCIe Adapter'. The system connects to 'USB-C® Connector(s)' for 'USB2' and 'USB4' output. A list of requirements is provided: 'USB4 with fallback to USB3' and 'Support for DP Alt Mode'. The bottom part shows a network topology where a central 'USB4 Router' is connected via 'USB4' links to two peripheral 'USB4 Router' nodes. Each peripheral router is connected to a 'USB Device', 'DisplayPort Sink', and 'PCIe Device'. A legend indicates the 'USB4 Interface with tunneled USB, DP and PCIe data' using colored segments: USB (green), DP (red), USB3 (blue), and PCIe (purple).
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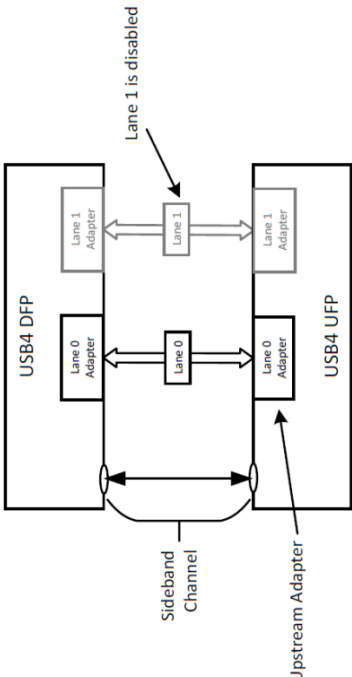
Claim 21	Exemplary Infringement Evidence
[21b] a receiver coupled to the first physical channel and configured to receive backward units of data at the source device from the sink device over the first physical channel during one or more second time periods, the backward units of data comprising backward data compliant with the first standard; and	https://www.usb.org/sites/default/files/D2T1-4%20-%20VESA%20DP%20Alt%20Mode%20over%20USB%20Type-C.pdf Each Accused Product comprises a receiver coupled to the first physical channel and configured to receive backward units of data at the source device from the sink device over the first physical channel during one or more second time periods, the backward units of data comprising backward data compliant with the first standard. For example, each accused product comprises a receiver (e.g., USB4 DFP with a transceiver for receiving data) coupled to the first physical channel (e.g., Lane 0 or bonded Lane 0 and Lane 1 of the USB4 port) and configured to receive backward units of data at the source device from the sink device over the first physical channel during one or more second time periods (e.g., periods when the sink send USB data to the source). The backward units of data comprises data with the first standard (e.g., USB data). <i>See, e.g.,</i>

Claim 21	Exemplary Infringement Evidence
	2.1.1.1.3 USB4 Ports and Links A USB4 Port is the entity that provides the USB4 functional interface that resides on each end of a USB4 Link. It consists of the transmit and receive Lanes of the USB4 data bus along with a two-wire Sideband (SB) Channel (SBTX/SBRX). USB4 Ports operate as either a Single-Lane Link or Dual-Lane Link. When operating as a Single-Lane Link, Lane 1 of the USB4 Port is disabled. When operating as a Dual-Lane Link, Lanes 0 and 1 are logically bonded together to provide a single data channel. Figure 2-2 shows a Single-Lane Link. Figure 2-3 shows a Dual-Lane Link. Figure 2-2. Single-Lane USB4 Link  The diagram illustrates a Single-Lane USB4 Link between a USB4 DFP (Downstream Facing Port) and a USB4 UFP (Upstream Facing Port). On the DFP side, there are two adapters: 'Lane 0 Adapter' and 'Lane 1 Adapter'. On the UFP side, there are also two adapters: 'Lane 0 Adapter' and 'Lane 1 Adapter'. A 'Sideband Channel' is shown as a curved line connecting the two ports. An arrow points from the 'Lane 1 Adapter' on the DFP side to the text 'Lane 1 is disabled'. Another arrow points from the 'Lane 1 Adapter' on the UFP side to the text 'Upstream Adapter'.

Claim 21	Exemplary Infringement Evidence Figure 2-3. Dual-Lane USB4 Link The diagram illustrates a Dual-Lane USB4 Link. On the left is a block labeled 'USB4 DFP' (Downstream Facing Port) containing 'Lane 0 Adapter' and 'Lane 1 Adapter'. On the right is a block labeled 'USB4 UFP' (Upstream Facing Port) containing 'Lane 0 Adapter' and 'Lane 1 Adapter'. A 'Sideband Channel' is shown as a dashed line with arrows connecting the two blocks. An 'Upstream Adapter' is indicated by an arrow pointing to the UFP side. A bracket on the right side of the diagram indicates that 'Lane 0 and Lane 1 are bonded'. The primary communication channel of the USB4 Fabric is over the USB4 Link that interconnects two USB4 Ports. The USB4 Link transports packets for both Tunneled Protocol traffic and bus management traffic between Routers. The Sideband Channel of a USB4 Port is used to initialize and manage the USB4 Link between the USB4 Ports. For a USB4-enabled USB Type-C port, the complete interface includes a USB4 Port, a USB 2.0 data bus, and the USB Type-C Configuration Channel (CC) along with power/ground (V_{BUS}, V_{CONN} and GND). Universal Serial Bus 4 Specification, Version 1.0, pg. 12-13. 2.2.3 Paths A Path represents a directional logical connection over the USB4 Fabric. A Path is defined either between two Protocol Adapters or between the Connection Manager and a Control Adapter. A Path can be end-to-end (as is the case for Display and Host-to-Host Tunneling) or it can traverse a single USB4 Link (as is the case for USB3 tunneling and PCIe Tunneling). Figure 2-9 shows an example of a set of Paths that tunnel USB3 traffic between a USB4 host and a USB4 device.
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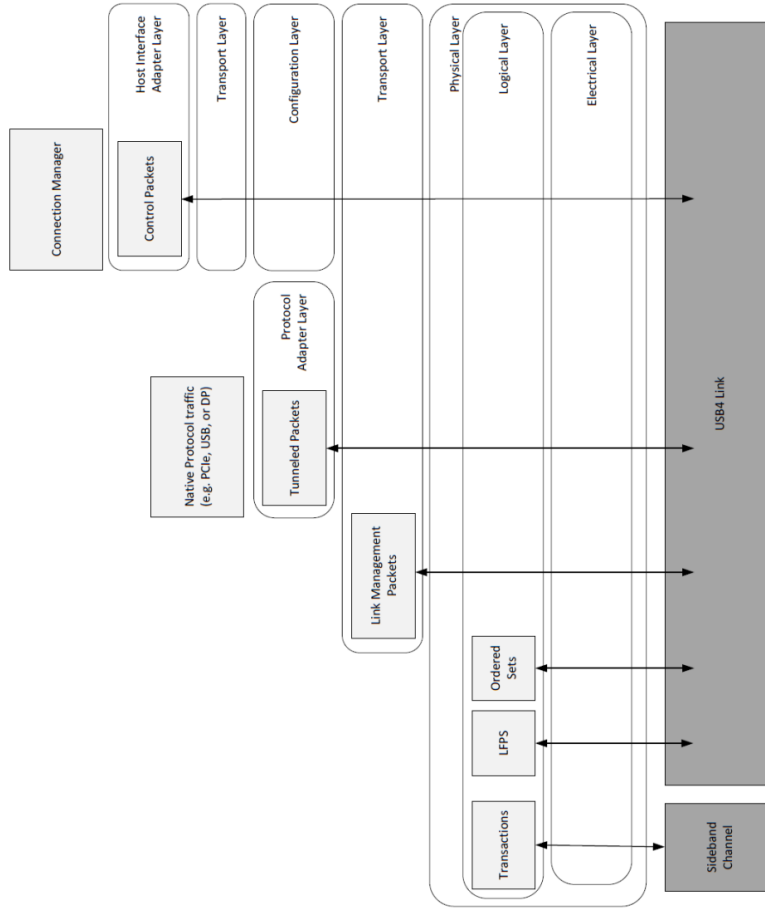
Claim 21	Exemplary Infringement Evidence A Tunnel is configured end-to-end before data transfer can take place. Each packet carries an identifier (called a HopID) that identifies the Path in the context of a given Link. The HopID is configured by a Connection Manager and can vary across each Link in the Path. When a Router receives a packet, it uses the HopID to determine the packet's next HopID and which Egress Adapter to forward the packet to. 2.2.4 Communication Constructs Figure 2-10 shows the various constructs that are used for communication over the USB4 Fabric. Figure 2-10. USB4 Communication by Functional Layer
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Claim 21	Exemplary Infringement Evidence
	Universal Serial Bus 4 Specification, Version 1.0, pg. 19-20
[21c] a control signal transceiver coupled to a second physical channel of the multimedia link distinct from the first physical channel and configured to at least send control data from the source device to the sink device over the second physical channel.	Each Accused Product comprises a control signal transceiver coupled to a second physical channel of the multimedia link distinct from the first physical channel and configured to at least send control data from the source device to the sink device over the second physical channel. For example, each accused product comprises a control signal transceiver (e.g., USB4 DFP port controller) coupled to a second physical channel (e.g., Sideband Channel) of the multimedia link distinct from the first physical channel (e.g., Lane 0 or bonded Lane 0 and Lane 1) and configured to send control data (e.g., USB4 Port Connect/Disconnect; Lane Initialization and Endable/Disable; entry or exit from Sleep state, etc.) from the source device to the sink device over the second physical channel (e.g., Sideband channel). <i>See, e.g.,</i>

Claim 21	Exemplary Infringement Evidence
	2.1.1.1.3 USB4 Ports and Links A USB4 Port is the entity that provides the USB4 functional interface that resides on each end of a USB4 Link. It consists of the transmit and receive Lanes of the USB4 data bus along with a two-wire Sideband (SB) Channel (SBTX/SBRX). USB4 Ports operate as either a Single-Lane Link or Dual-Lane Link. When operating as a Single-Lane Link, Lane 1 of the USB4 Port is disabled. When operating as a Dual-Lane Link, Lanes 0 and 1 are logically bonded together to provide a single data channel. Figure 2-2 shows a Single-Lane Link. Figure 2-3 shows a Dual-Lane Link. Figure 2-2. Single-Lane USB4 Link  The diagram illustrates a Single-Lane USB4 Link. On the left, a box labeled 'USB4 DFP' contains two 'Lane Adapter' blocks: 'Lane 0 Adapter' and 'Lane 1 Adapter'. On the right, a box labeled 'USB4 UFP' contains two 'Lane Adapter' blocks: 'Lane 0 Adapter' and 'Lane 1 Adapter'. A 'Sideband Channel' is shown as a curved line with arrows connecting the 'Lane 0 Adapter' blocks of both DFP and UFP. An 'Upstream Adapter' is shown as a box between the 'Lane 0 Adapter' blocks of DFP and UFP. A 'Lane 1' block is shown between the 'Lane 1 Adapter' blocks of DFP and UFP, with an arrow pointing to it from the text 'Lane 1 is disabled'.

Claim 21	Exemplary Infringement Evidence
	Figure 2-3. Dual-Lane USB4 Link The diagram illustrates a Dual-Lane USB4 Link. On the left, a box labeled 'USB4 DFP' contains two sub-boxes: 'Lane 0 Adapter' and 'Lane 1 Adapter'. On the right, a box labeled 'USB4 UFP' contains two sub-boxes: 'Lane 0 Adapter' and 'Lane 1 Adapter'. A dashed oval in the center, labeled 'Sideband Channel', connects the 'Lane 0 Adapter' of the DFP to the 'Lane 0 Adapter' of the UFP, and the 'Lane 1 Adapter' of the DFP to the 'Lane 1 Adapter' of the UFP. Arrows indicate bidirectional data flow between these adapters. A bracket on the right side of the diagram, labeled 'Upstream Adapter', points to the 'Lane 0 Adapter' and 'Lane 1 Adapter' of the UFP. A note on the right states 'Lane 0 and Lane 1 are bonded'. The primary communication channel of the USB4 Fabric is over the USB4 Link that interconnects two USB4 Ports. The USB4 Link transports packets for both Tunnelled Protocol traffic and bus management traffic between Routers. The Sideband Channel of a USB4 Port is used to initialize and manage the USB4 Link between the USB4 Ports. For a USB4-enabled USB Type-C port, the complete interface includes a USB4 Port, a USB 2.0 data bus, and the USB Type-C Configuration Channel (CC) along with power/ground (V_{BUS}, V_{CONN} and GND). Universal Serial Bus 4 Specification, Version 1.0, pg. 12-13.

Figure 2-10. USB4 Communication by Functional Layer



Claim 21	Exemplary Infringement Evidence
	2.2.4.2 Sideband Channel The Sideband Channel handles the following events: • Lane Initialization. • Connection or disconnect on a USB4 Port. • Lane disable or enable. • Entry or exit from Sleep state. Universal Serial Bus 4 Specification, Version 1.0, pg. 20-21 3.1 Sideband Channel Electrical Specifications The Sideband Channel shall operate at 1 Mbps rate. Universal Serial Bus 4 Specification, Version 1.0, pg. 39.

Claim 22

Claim 22	Exemplary Infringement Evidence
[22pre] A non-transitory computer readable storage medium storing instructions thereon, the instructions representing a digital design of a circuit comprising:	To the extent the preamble is limiting, each Accused Product comprises a non-transitory computer readable storage medium storing instructions thereon, the instructions representing a digital design of a circuit.

Claim 22	Exemplary Infringement Evidence
[22a] a transmitter coupled to a first physical channel of the multimedia link and configured to send forward units of data from a source device to a sink device over the first physical channel during one or more first time periods, the forward units of data comprising video data and forward data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data;	Each Accused Product comprised of a non-transitory computer readable storage medium storing instructions representing a digital design of a circuit containing a transmitter coupled to a first physical channel of the multimedia link and configured to send forward units of data from a source device to a sink device over the first physical channel during one or more first time periods, the forward units of data comprising video data and forward data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data <i>See</i> [21a]
[22b] a receiver coupled to the first physical channel and configured to receive backward units of data at the source device from the sink device over the first physical channel during one or more second time periods, the backward units of data comprising backward data compliant with the first standard; and	Each Accused Product comprised of a non-transitory computer readable storage medium storing instructions representing a digital design of a circuit containing a receiver coupled to the first physical channel and configured to receive backward units of data at the source device from the sink device over the first physical channel during one or more second time periods, the backward units of data comprising backward data compliant with the first standard. <i>See</i> [21b]
[22c] a control signal transceiver coupled to a second physical channel of the multimedia link distinct from the first physical channel and configured to at least send control data from the source device to the sink device over the second physical channel.	Each Accused Product comprised of a non-transitory computer readable storage medium storing instructions representing a digital design of a circuit containing a control signal transceiver coupled to a second physical channel of the multimedia link distinct from the first physical channel and configured to at least send control data from the source device to the sink device over the second physical channel. <i>See</i> [21c]