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Whitby-Strevens

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(54) **METHODS AND APPARATUS FOR SCRAMBLING SYMBOLS OVER MULTI-LANE SERIAL INTERFACES**

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G06F 3/14	(2006.01)
G09G 5/12	(2006.01)

(52) **U.S. Cl.**

CPC ***H04L 25/03866*** (2013.01); ***G09G 5/006*** (2013.01); *G06F 3/14* (2013.01); *G09G 5/12* (2013.01); *G09G 2330/06* (2013.01); *G09G 2370/12* (2013.01)

(58) **Field of Classification Search**

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USPC 375/220, 257, 285; 380/268

See application file for complete search history.

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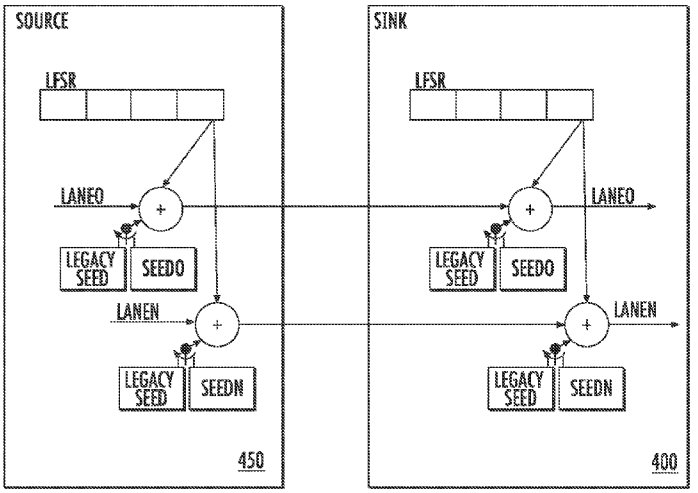
(74) *Attorney, Agent, or Firm* — Gazdzinski & Associates PC

(57) **ABSTRACT**

Methods and apparatus for scrambling symbols over multi-lane serial interfaces in order to improve undesired electromagnetic emissions. In one embodiment the scrambling is based on a seed value associated with each lane. In a second embodiment, the scrambling values are selected from various taps of a scrambling component, where the selection is based on the associated lane. In still a third embodiment, each lane is associated with a distinct scrambling component.

18 Claims, 8 Drawing Sheets



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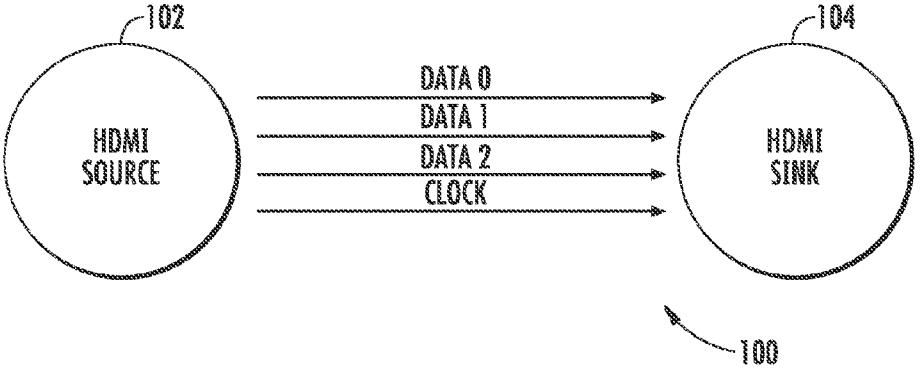


FIG. 1

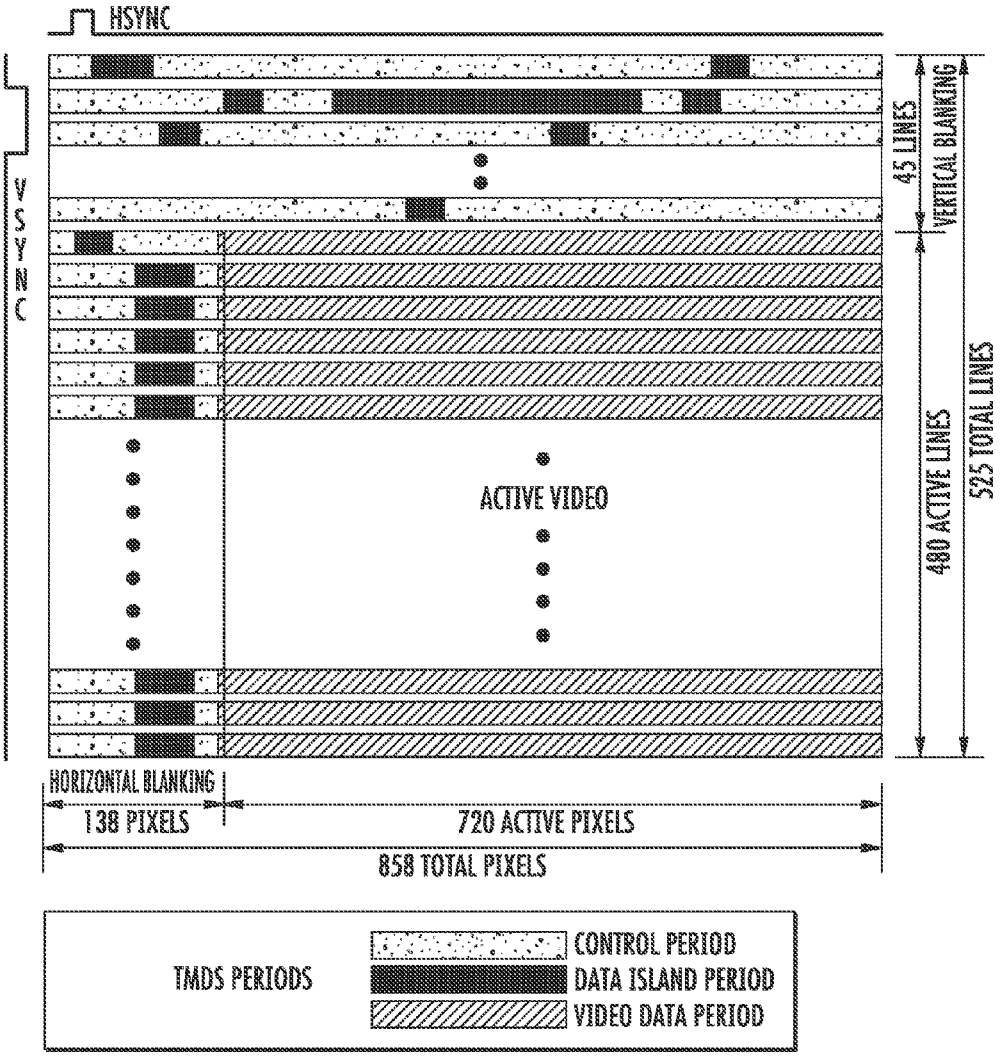

HSYNC
VSYNC
45 LINES
VERTICAL BLANKING
ACTIVE VIDEO
480 ACTIVE LINES
525 TOTAL LINES
HORIZONTAL BLANKING
138 PIXELS
720 ACTIVE PIXELS
858 TOTAL PIXELS
TMDS PERIODS
CONTROL PERIOD
DATA ISLAND PERIOD
VIDEO DATA PERIOD

FIG. 2

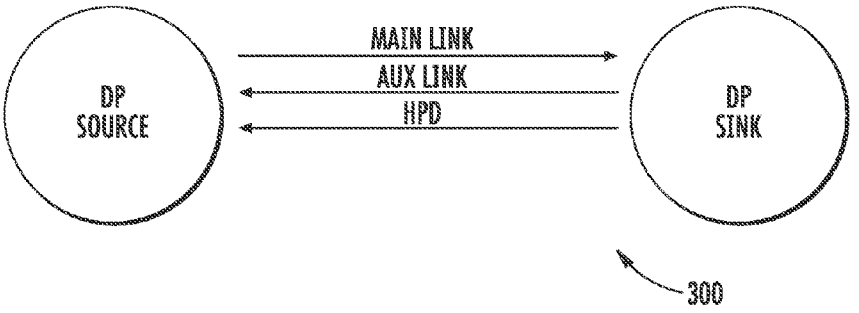
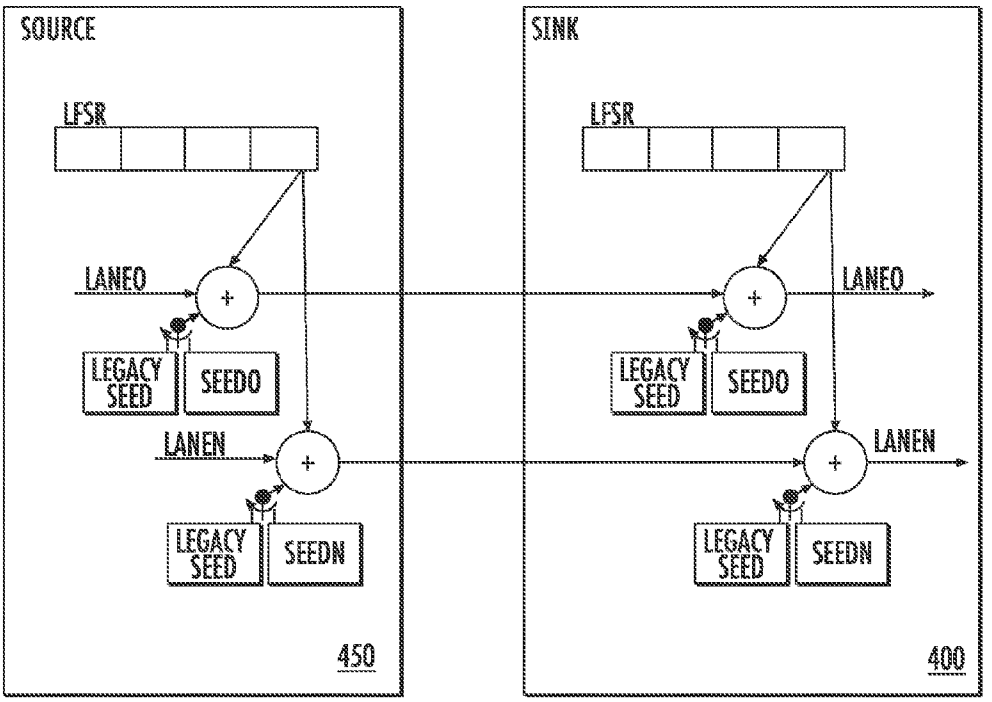


FIG. 3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LFSR
LANE0
LEGACY SEED
SEED0
LANEN
LEGACY SEED
SEEDN
450
SINK
LFSR
LANE0
LEGACY SEED
SEED0
LANEN
LEGACY SEED
SEEDN
400

FIG. 4A

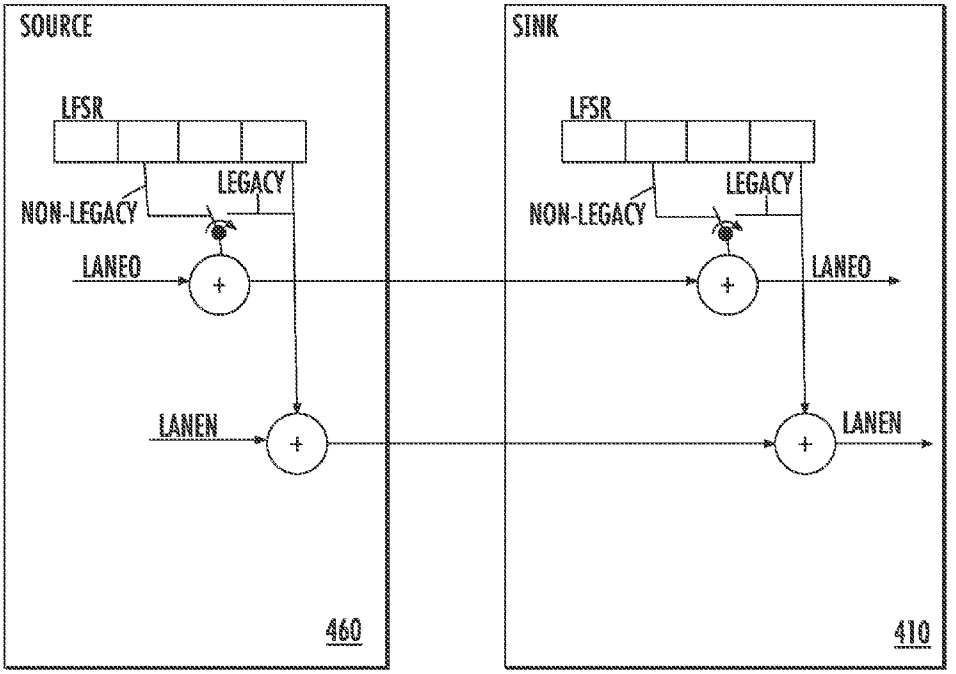
SOURCE
LFSR
LEGACY
NON-LEGACY
LANE0
LANEN
460
SINK
LFSR
LEGACY
NON-LEGACY
LANE0
LANEN
410

FIG. 4B

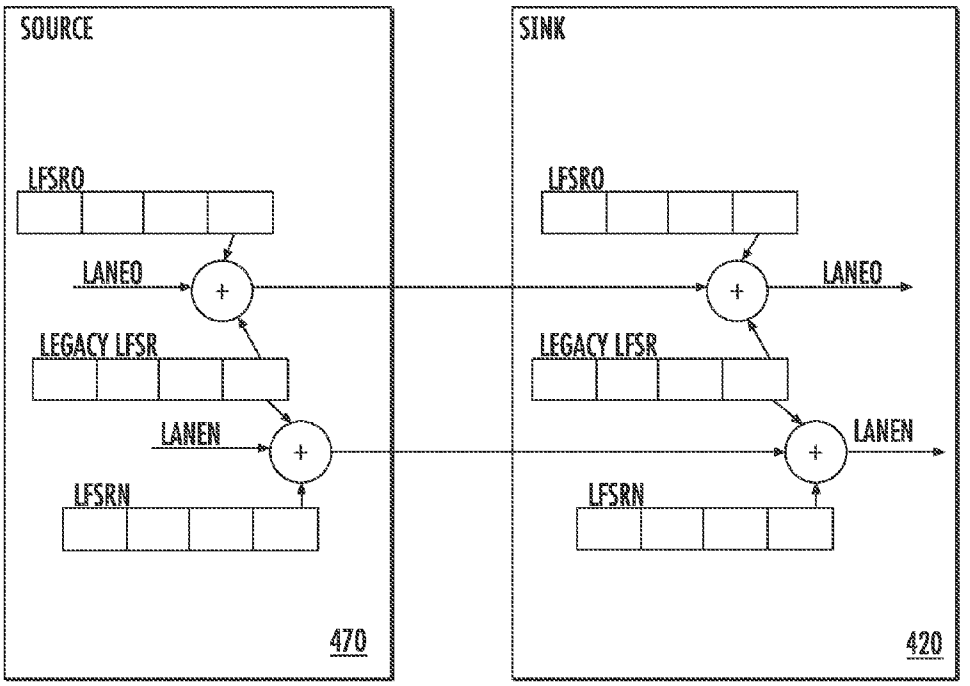
SOURCE
LFSR0
LANE0
LEGACY LFSR
LANEN
LFSRN
470
SINK
LFSR0
LANE0
LEGACY LFSR
LANEN
LFSRN
420

FIG. 4C

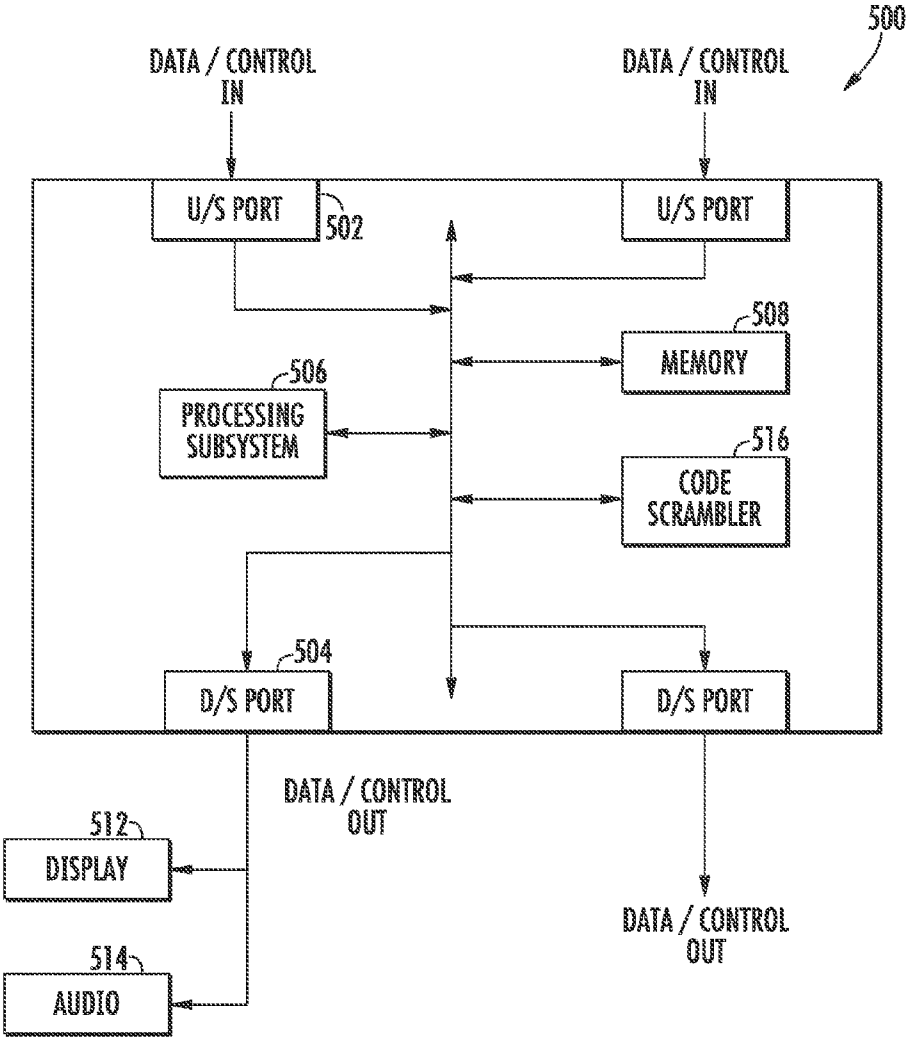
500
DATA / CONTROL IN
DATA / CONTROL IN
U/S PORT
502
U/S PORT
508
MEMORY
506
PROCESSING SUBSYSTEM
516
CODE SCRAMBLER
504
D/S PORT
D/S PORT
DATA / CONTROL OUT
512
DISPLAY
DATA / CONTROL OUT
514
AUDIO

FIG. 5

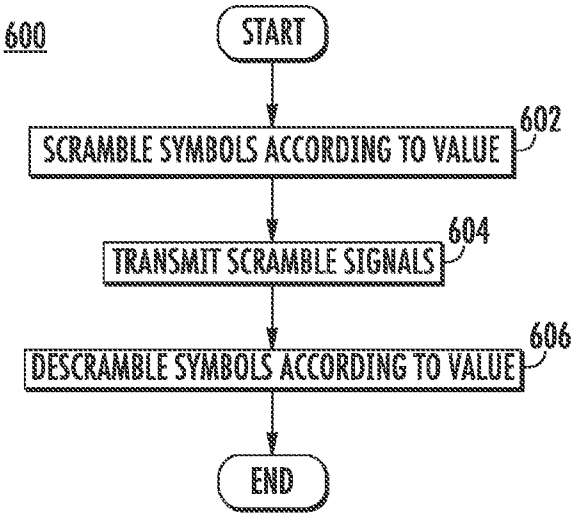
600
START
SCRAMBLE SYMBOLS ACCORDING TO VALUE
602
TRANSMIT SCRAMBLE SIGNALS
604
DESCRAMBLE SYMBOLS ACCORDING TO VALUE
606
END

FIG. 6

METHODS AND APPARATUS FOR SCRAMBLING SYMBOLS OVER MULTI-LANE SERIAL INTERFACES

RELATED APPLICATIONS

This application is related to co-owned, co-pending U.S. patent application Ser. No. 13/747,264 filed on Jan. 22, 2013 and entitled "METHODS AND APPARATUS FOR THE INTELLIGENT SCRAMBLING OF CONTROL SYMBOLS", Ser. No. 13/747,383 filed Jan. 22, 2013 and entitled "METHODS AND APPARATUS FOR ERROR RATE ESTIMATION", and Ser. No. 12/976,274 filed Dec. 22, 2010 and entitled "METHODS AND APPARATUS FOR THE INTELLIGENT ASSOCIATION OF CONTROL SYMBOLS", each of the foregoing being incorporated herein by reference in its entirety.

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BACKGROUND

1. Technological Field

The present disclosure relates generally to the field of data networking and telecommunications. More particularly, in one exemplary aspect, the present disclosure is directed to scrambling symbols over multi-lane serial interfaces in order to improve undesired electromagnetic emissions.

2. Description of Related Technology

Many serial communications systems send data over more than one lane or channel. Commercial examples include without limitation, DisplayPort, HDMI (High-Definition Multimedia Interface), etc.

As is well known within the electrical arts, rapid signaling changes in a transmission line will generate undesirable electromagnetic interference (EMI) in neighboring circuitry and/or devices. Consequently, in order to reduce EMI, certain technologies (such as for example and without limitation, DisplayPort, Firewire, etc.) utilize a transmitter "scrambler" that is configured to add/spread the signal with pseudorandom noise; the resulting "scrambled" signal has a reduction in peak spectral noise, and a wider spectral "footprint". The receiver has a corresponding "descrambler" which can remove the pseudorandom noise and reconstruct the original signal. Many types of pseudorandom number generators exist; however, scramblers are typically implemented with linear feedback shift registers (LFSRs) due to the simplicity and relatively inexpensive cost.

One problem with multi-channel scrambling technologies (such as DisplayPort, etc.) occurs when the same data is transmitted on each channel. For example, during video data transmissions so-called "blanking" intervals can include long periods of null data which are typically represented with the same value (e.g., all zeros (0) or all ones (1)). Under these circumstances, the scrambled result for each lane of the multi-lane transceiver is identical (each lane transmits the same value, which is identically scrambled). Since each lane is perfectly correlated with the other lanes, the overall EMI magnitude of the multi-lane transmission is a direct sum of

each of the contributing EMIs. The resulting spectral footprint of the multi-lane transmission line may be strong enough to interrupt nearby circuitry. Large EMI can be especially problematic for devices that have very aggressive form factors (i.e., where components are in very close proximity).

Accordingly, improved apparatus and methods are needed in order to address these EMI concerns with regards to multi-lane serial bus technologies such as e.g., DisplayPort, etc. More generally, such apparatus and methods would ideally provide for mechanisms that improve the EMI characteristics of multi-lane high speed serial bus operation, while also advantageously leveraging existing hardware in certain implementations so as to minimize circuitry costs in future implementations.

SUMMARY

The aforementioned needs are satisfied by providing, inter cilia, improved apparatus and methods for scrambling symbols over multi-lane serial interfaces in order to improve undesired electromagnetic emissions.

In a first aspect, an apparatus configured to scramble a plurality of symbols is disclosed. In one embodiment, the apparatus includes a first interface that includes a plurality of lanes. In a legacy mode, each lane is characterized by a common scrambling mechanism. Moreover, in a non-legacy mode each lane is characterized by a corresponding distinct scrambling mechanism. The apparatus further includes a processor that is in data communication with the first interface; and a non-transitory computer-readable medium comprising one or more instructions which when executed by the processor, causes the apparatus to: when in the non-legacy mode: transmit symbols via the plurality of lanes with the symbols being configured to be descrambled by a receiver and when in the legacy mode: transmit symbols compatible with legacy systems via the plurality of lanes. The symbols that are compatible with legacy systems is further configured to be descrambled by the receiver responsive to reception.

In a variant, in non-legacy mode each lane of the plurality of lanes is associated with a distinct linear feedback shift register (LFSR).

In another variant, in non-legacy mode each lane of the plurality of lanes is associated with unique bits of one or more linear feedback shift registers (LFSRs).

In yet another variant, in non-legacy mode each corresponding distinct scrambling mechanism is self-synchronizing.

In yet another variant, in non-legacy mode each corresponding distinct scrambling mechanism is selected to minimize electro-magnetic interference (EMI) with at least one other corresponding distinct scrambling mechanism.

In a second aspect, a method for scrambling symbols is disclosed. In one embodiment, the method includes determining when an apparatus is in a non-legacy mode or in a legacy mode and when the apparatus is in the non-legacy mode, transmitting symbols via a plurality of lanes, where the symbols are configured to be descrambled by a receiver responsive to reception of the symbols. Alternatively, when the apparatus is in the legacy mode, transmitting symbols compatible with legacy systems via the plurality of lanes, where the symbols compatible with legacy systems are configured to be received by the receiver responsive to reception of the symbols compatible with legacy systems. When in the legacy mode each of the plurality of lanes is unscrambled and when in the non-legacy mode each of the plurality of lanes is characterized by a corresponding distinct scrambling mechanism.

In a variant, the symbols are generated by one or more linear feedback shift registers (LFSRs).

In another variant, each one of the one or more LFSRs is characterized by a different characteristic polynomial.

In yet another variant, each one of the one or more LFSRs is seeded with a different value.

In yet another variant, a corresponding plurality of scrambling values are generated by different bits of the one or more LFSRs.

In yet another variant, the one or more LFSRs are self-synchronizing. In yet another variant, the one or more LFSRs are selected to maximize a run length.

In yet another variant, the method further includes negotiating a deterministic scheme for generating the plurality of symbols.

In a third aspect, an apparatus configured to descramble symbols is disclosed. In one embodiment, the apparatus includes a first interface having a plurality of lanes. In a legacy mode each lane is not distinctly scrambled and in a non-legacy mode each lane is characterized by a corresponding distinct scrambling mechanism. The apparatus further includes a processor in data communication with the first interface; and a non-transitory computer-readable medium comprising one or more instructions, which when executed by the processor, causes the apparatus to: determine when to operate in the non-legacy mode or in the legacy mode and when in the non-legacy mode, for each symbol received, descramble each symbol according to a corresponding lane; and when in the legacy mode, receive symbols compatible with legacy systems via the plurality of lanes.

In a variant, the computer-readable medium further includes one or more instructions, which when executed by the processor, causes the apparatus to negotiate the distinct scrambling mechanism.

In a fourth aspect, a method for descrambling symbols is disclosed. In one embodiment, the method includes: determining when to operate in a non-legacy mode or in a legacy mode and when in the non-legacy mode, receive the symbols via a multi-lane interface; and when in the legacy mode, receive other symbols via the multi-lane interface. For each symbol of the received symbols, descrambling each symbol according to a corresponding lane, where at least two lanes of the multi-lane interface are characterized by distinct scrambling mechanisms; and for each symbol of the received other symbols, descrambling the each symbol, where no lanes of the multi-lane interface are characterized by distinct scrambling mechanisms.

In a variant, the distinct scrambling mechanisms are uncorrelated. In another variant the distinct scrambling mechanisms are self-synchronizing.

Other features and advantages will immediately be recognized by persons of ordinary skill in the art with reference to the attached drawings and detailed description of exemplary embodiments as given below.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a graphical representation of one exemplary HDMI multimedia system that includes one or more multimedia sources and one or more multimedia sinks.

FIG. **2** is an exemplary prior art HDMI 720×480p video frame.

FIG. **3** is a graphical representation of one exemplary DisplayPort interface.

FIG. **4**A is a graphical representation of an exemplary embodiment of a receiver and transmitter configured to scramble symbols according to a seeded value in order to improve undesired electromagnetic emissions, in accordance with the present disclosure.

FIG. **4**B is a graphical representation of an exemplary embodiment of a receiver and transmitter configured to scramble each lane with different bits of an LFSR in order to improve undesired electromagnetic emissions, in accordance with the present disclosure.

FIG. **4**C is a graphical representation of an exemplary embodiment of a receiver and transmitter configured to scramble each lane with a different LFSR in order to improve undesired electromagnetic emissions, in accordance with the present disclosure.

FIG. **5** is a logical block diagram of an exemplary embodiment of a user device (apparatus) having multi-lane symbol encoding/decoding capability.

FIG. **6** is a logical flow diagram representing one embodiment of a generalized method for scrambling symbols over multi-lane serial interfaces.

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DETAILED DESCRIPTION

Reference is now made to the drawings, wherein like numerals refer to like parts throughout.

Detailed Description Of Exemplary Embodiments

Exemplary embodiments are now described in detail. While these embodiments are primarily discussed in the context of an HDMI and DisplayPort audio/visual (A/V) networks, it will be recognized by those of ordinary skill that the present disclosure is not in any way limited to such applications. In fact, the various aspects set forth herein are useful in any network that can benefit from the reduction of electromagnetic interference in multi-lane serial bus transactions.

Furthermore, while these embodiments are disclosed in a serial transmission of digital data represented as electrical levels, ones having ordinary skill in the related arts will recognize that the various techniques may also extend to other systems and applications including, inter alia, multi-level wired systems (e.g., three-level encoded Ethernet), and modulated transmission schemes (e.g., a high frequency carrier that is modulated in the amplitude or frequency domain {AM or FM} by the signals being transmitted).

Existing HDMI Operation—

Referring now to FIG. **1**, one exemplary HDMI multimedia system is illustrated. As shown the system **100** includes one or more multimedia sources **102**, and one or more multimedia sinks **104**. Common examples of multimedia sources include, without limitation, media players (e.g., Digital Video Disk (DVD) players, Blue-ray players, etc.), content delivery networks, audio/visual (A/V) equipment (e.g., camcorders, etc.), personal computers (PC), etc. Common examples of multimedia sinks include, without limitation, media displays, televisions, monitors, etc.

The exemplary HDMI interface comprises four (4) unidirectional differential signaling pairs that consist of three (3) data channels (data channel 0, data channel 1, data channel 2), and a clock (characterized by a 1/10 bit-rate frequency). In other configurations (such as e.g., future implementations of HDMI, and Mobile High Definition Link (MHL)), the clock differential pair may be replaced with another data channel.

FIG. **2** is a graphical representation of exemplary data traffic representing a frame of 720×480 pixels of video data. It should be noted that the foregoing resolution is merely illustrative of a common video frame size, those of ordinary skill in the related arts will appreciate that other video frame

sizes may be substituted. As a brief aside, the current incarnation of HDMI specifies five (5) different types of information: (i) control information, (ii) preamble, (iii) guard band, (iv) data island data and (v) video data. As shown in FIG. **2**, the first 45 scan lines constitute the vertical blanking interval. Thereafter, the first 138 pixels of each scan line is a horizontal blanking interval, the remaining 720 pixels is video data. During both the horizontal and vertical blanking intervals, the data channels may transmit either control data or data islands. The preamble and guard band information are provided to facilitate identification of data islands and/or video data. A preamble immediately precedes data island periods and video data periods. Both video data periods and data island periods start with a guard band. Data island periods may also conclude with a guard band.

Prior art HDMI TMDS observes a fixed set of rules that enables only a subset of possible symbols, based on the type of data. Moreover, for simplicity, only 10-bit patterns are used to represent the information to be transmitted (i.e., the symbols do not change in length). Specifically, the 10-bit encodings used for control and preamble transmissions share common symbols which are disjoint from (i.e., do not overlap) the 10-bit symbols used for the other types of data (guard band, data island and video data). Similarly, the 10-bit symbol encodings used for data island transmissions (also referred to as TERC4 (TMDS Error Reduction Coding 4-bit) encoding) are distinct. The 10-bit symbols used for the guard band are a subset of the symbol encodings used for video data.

Existing HDMI implementations do not implement any form of scrambling over the individual channels. Incipient research is directed to incorporating scrambling functionality to improve future implementations of HDMI.

Existing DisplayPort Operation—

From an application software standpoint, DisplayPort is very similar to HDMI, in fact in some applications DisplayPort can be used to encapsulate HDMI data. However, the physical interface of DisplayPort is markedly different.

Referring now to FIG. **3**, the exemplary DisplayPort interface comprises: a main link which may consist of one (1), two (2) or four (4) unidirectional differential signaling pairs (or "lanes"), an auxiliary link is a half-duplex bi-directional signaling link used for link management and device control, and a hot-plug detect (HPD). All signaling pairs carry data, there is no dedicated clock signaling (the receiver must recover the clock from the transmitted data). Each data lane uses 8B/10B encoding.

While TMDS could be considered a form of 8B/10B encoding, it is appreciated that as used within the relevant arts, the term "8B/10B" refers to a specific protocol developed by IBM (the IBM 8B/10B scheme was subject to patents which have since expired). DisplayPort utilizes the IBM 8B/10B encoding (as described within "*A DC Balanced, Partitioned-Block,* 8B/10B Transmission Code" to Widmer and Franaszek, incorporated herein by reference in its entirety). 8B/10B encoding maps an 8-bit data byte or one of a set of twelve control symbols to a 10-bit symbol in order to achieve the DC balance. The mapping is such that the mapped versions of the control symbols and data symbols are distinct. The 8-bit symbol can either be an 8-bit data byte or a control symbol. In both cases, they are mapped into 10-bit symbols. One particularly useful property of 8B/10B encoded symbols is that in any sequence of 10-bit symbols, there will never be more than a disparity of +1 or −1 when counting the number of ones and zeros (at symbol boundaries). For example, if after a number of 10-bit symbols the running disparity is −1, then the next symbol will either have exactly five (5) ones and five (5) zeros (i.e., the running disparity remains −1), or it will have six (6) ones and four (4) zeros (i.e., the running disparity changes to +1). Since the running disparity is only used at symbol boundaries, the bit-wise running disparity can range between +3 and −3.

As the scheme name suggests, eight (8) bits of data are encoded and transmitted as a 10-bit symbol. The low five (5) bits of data are encoded into a 6-bit group (i.e. the so-called 5b/6b portion) and the top three (3) bits are encoded into a 4-bit group (i.e. the so-called 3b/4b portion). These two sub-encoding groups are subsequently concatenated together to form the 10-bit symbol that is transmitted over the transmission medium. The data symbols are often referred to in the format "D.x.y" where x ranges in value from 0-31 (2^5=32) and y ranges in value from 0-7 (2^3=8), i.e. the five (5) and three (3) bit portions.

One useful property of such an encoding scheme is that since 10-bit symbols are utilized to encode 8-bit words, some of the possible one-thousand twenty-four (2^{10}=1024) codes can be excluded in order to comply with the previously mentioned run-length limit of five (5) consecutive equal bits and a differential limit such that the difference of the count of 0s and 1s is no more than two (2) for a given twenty bit string of bits. In addition, some of the two-hundred fifty-six (256) possible 8-bit words can be encoded in two alternative ways. Using these alternative encodings, the scheme is able to affect long-term DC-balance on the transmission line.

This DC-balance is accomplished in part via a mechanism known as "running disparity" that keeps the number of 1 s and 0s that are transmitted roughly equal. That is, for each 5b/6b and 3b/4b code with an unequal number of 1 s and 0s, there are two (2) bit patterns that can be used to transmit it. For example, a first ten-bit with two more 1s then 0s can be represented as follows: 001011 1110. This first ten-bit pattern can also be represented by its inverse, thereby encoding two or more 0s than 1 s as follows: 110100 0001. Accordingly, depending on the current running disparity of the signal, the encoding hardware selects which of the two possible 10-bit sequences to send for the given data.

In addition, 8B/10B encoding possesses what are known as a "special symbols". They are typically referred to in the form "K.x.y" and have different encodings from any of the possible "D.x.y" symbols; i.e., they are symbols which cannot result via the encoding of an 8-bit data symbol. Table 1 below illustrates the format for these special symbols, which include a first 10-bit code for a running disparity of negative one (−1), along with its inverse for a running disparity of positive one (+1):

TABLE 1

8B/10B Special Symbols

Input - Special Symbols		RD = −1	RD = +1
K-Codes	HGF EDCBA	abcdei fghj	abcdei fghj
K.28.0	000 11100	001111 0100	110000 1011
K.28.1	001 11100	001111 1001	110000 0110
K.28.2	010 11100	001111 0101	110000 1010
K.28.3	011 11100	001111 0011	110000 1100
K.28.4	100 11100	001111 0010	110000 1101
K.28.5	101 11100	001111 1010	110000 0101
K.28.6	110 11100	001111 0110	110000 1001
K.28.7	111 11100	001111 1000	110000 0111
K.23.7	111 10111	111010 1000	000101 0111
K.27.7	111 11011	110110 1000	001001 0111
K.29.7	111 11101	101110 1000	010001 0111
K.30.7	111 11110	011110 1000	100001 0111

These special symbols are inserted into the data stream and accordingly, can be used for executing low-level control functions separate and apart from encoded data symbols. For example, the DisplayPort specification sets forth a number of control functions that can be mapped onto these so-called "K-codes" of the IBM 8B/10B encoder specification. These control functions include: (1) Blanking Start (BS); (2) Blanking End (BE); (3) Fill Start (FS); (4) Fill End (FE); (5) Secondary-data Start (SS); (6) Secondary-data End (SE); (7) Scrambler Reset (SR); (8) Content Protection BS (CPBS); and (9) Content Protection SR (CPSR).

Referring back to FIG. **3**, each data lane is scrambled with the eight (8) most significant bits of a 16-bit LFSR in reverse bit order. The characteristic polynomial for this 16-bit internal LFSR is set forth below at Equation (1).

$$G(X)=X16+X5+X4+X3+1 \quad \text{(Equation 1)}$$

The resulting data can be represented by Equation (2).

$$D'[7:0]=D[7:0]XOR\ LFSR[8:15] \quad \text{(Equation 1)}$$

Additionally, DisplayPort specifies certain rules for scrambler operation. The scrambling/descrambling LFSR advances on all symbols (both D and K), however some usages of the K symbols are not scrambled (DisplayPort versions 1.2 introduced "multistream" operation which scrambles certain K symbols). Data symbols (including null or "fill" data) is scrambled). Furthermore, certain special symbols can be used to reset the scrambling/descrambling LFSR. DisplayPort implements inter-lane skew on the data (each successive lane is offset from its predecessor by two (2) symbols), thus the data is scrambled first and the lane-to-lane skew is applied.

Apparatus—

Various embodiments of the present disclosure are directed to distinctly scrambling each lane of a multi-lane transceiver. Ideally (but not mandatorily), each lane is scrambled so as to produce uncorrelated outputs (as compared to the other scrambled lanes). Unlike correlated scrambling which results in EMI that constructively interferes (i.e., a direct sum), uncorrelated scrambling will result in EMI that adds according to a root mean square (which significantly improves overall EMI emissions). For example, with two (2) lanes, the overall EMI will be approximately 1.414 times (square root of two (2)) a single lane EMI.

LFSRs are advantageously used in exemplary implementations of the disclosure because the operation of the LFSR is deterministic, while also providing a sequence of bits that appears random. Accordingly, and as discussed previously herein, synchronization between transmitter and receiver can be maintained if the cycles between the LFSR at the transmitter and the LFSR at the receiver remains synchronized. In an exemplary embodiment, each LFSR is a 16-bit LFSR, although it is appreciated that other LFSR's (including those of other lengths, and/or tap configurations) could readily be substituted such as those described previously herein. When using an exemplary 16-bit LFSR, a subset of bits is used for symbol encoding.

Several distinct constructions are provided to illustrate the foregoing; however, those of ordinary skill in the related arts will readily appreciate that virtually any such scheme that results in uncorrelated scrambling for each lane of a multi-lane transceiver will result in reduced EMI emissions.

Referring now to FIG. **4**A, an exemplary embodiment of a receiver **400** and transmitter **450** configured to scramble symbols according to a seeded value in order to improve undesired electromagnetic emissions is illustrated. The circuit illustrated in FIG. **4**A is shown implemented in hardware; although it is appreciated that the logic illustrated in FIG. **4**A could readily be implemented in software, or combinations of hardware and software, as well.

The receiver **400** and transmitter **450** include complementary LFSRs **402** which are used for each lane but each lane is further modified uniquely by a seed value. For example, in a first variant, the data is XOR'd (exclusively OR'd) with an LFSR and then is further XOR'd with the lane (or channel number) that it is associated with for transport. In a similar variant, a pre-agreed scrambler reset seed is associated with the lane, so that when scrambler reset occurs, the LFSRs on different lanes are set to different values. It should be further noted that these two (2) variants are not exclusive, in fact a different scrambler reset can be used for each lane as well as an XOR with the lane number. While both of the foregoing examples use seed values that are based on the lane, it is readily appreciated that virtually any seed value may be used.

Other examples of seed values may include e.g., randomly generated seed values, incrementing seed values, configurable seed values, etc. In systems where the seed is dynamically set (not an agreed upon value), the receiver and transmitter may be required to negotiate or coordinate operation based on e.g., out of band signaling, an initial exchange (e.g., via non-scrambled transactions, etc.).

Referring now to FIG. **4**B, an exemplary embodiment of a receiver **410** and transmitter **460** configured to scramble each lane with different bits of an LFSR in order to improve undesired electromagnetic emissions is illustrated.

In this example, the transmitter **460** and receiver **410** have matching LFSR bits XOR'd with the appropriate lanes. For example, as shown the first lane may use LFSR [8:15], the second lane may use LFSR[7:0], the third lane may use LFSR [0:3 . . . 8:11], and the fourth lane may use LFSR[15:12 . . . 7:4], etc. In other examples, a 32-bit LFSR can be used such that: the first lane uses [0:7], the second lane uses [8:15], the third lane uses 16:23], and the fourth lane uses [23:31]. Those of ordinary skill will recognize that the foregoing selection of bits is merely illustrative of the myriad of combinations that are possible.

Referring now to FIG. **4**C, an exemplary embodiment of a receiver **420** and transmitter **470** configured to scramble each lane with a different LFSR in order to improve undesired electromagnetic emissions is illustrated.

As shown each lane is associated with a distinct LFSR. Those of ordinary skill in the related arts will recognize that significant research has been devoted to discovering LFSRs with desirable properties e.g., maximal length, self-synchronization, maximal run length, etc. Accordingly variants may select LFSRs based on any of such desirable properties. For example certain applications may be more interested in self-synchronizing LFSRs than LFSRs which have guarantee shorter maximal run lengths or vice versa.

Moreover, it is further appreciated that in some circumstances, it may be desirable to combine one or more of the foregoing schemes of FIGS. **4**A-C. For example, in some embodiments, each lane may be seeded with a different initial value and additionally use unique bits of the LFSR.

Still further, it is appreciated that since both the transmitter and receiver must agree on the multi-lane scrambling scheme, various systems may be configured to negotiate the multi-lane scrambling configuration and/or default to a specific configuration. In some variants, the default configuration is compatible with legacy systems.

Referring now to FIG. **5**, an exemplary embodiment of a user device (apparatus) **500** having multi-lane symbol encoding/decoding capability is illustrated. As used herein, the term "user device" includes but is not limited to cellular tele-

phones, smartphones (such as for example an iPhone™ manufactured by the Assignee hereof), personal computers (PCs), such as for example an iMac™, Mac Pro™, Mac Mini™, MacBook™, MacBook Pro™, MacBook Air™, and minicomputers, whether desktop, laptop, or otherwise, as well as mobile devices such as handheld computers, PDAs, video cameras, set-top boxes, personal media devices (PMDs), such as for example an iPod™, tablets or phablets, such as e.g., the iPad™, display devices (e.g., those compliant with the aforementioned HDMI standard(s)), or any combinations of the foregoing.

While a specific device configuration and layout is shown and discussed, it is recognized that many other configurations may be readily implemented by one of ordinary skill given the present disclosure, the apparatus **500** of FIG. **5** being merely illustrative of the broader principles of the disclosure. For example, it is appreciated that the device illustrated in FIG. **5** could readily be implemented as either a source or alternatively as a sink, or in fact could be configured to operate as both. Appropriate modifications to the layout shown would be readily apparent to one of ordinary skill given the present disclosure.

The illustrated apparatus **500** of FIG. **5** includes an upstream plurality of ports and corresponding receiving elements (e.g., receiver or transceiver network interfaces) **502**, a downstream plurality of ports and corresponding transmitting elements (transmitting interfaces or transceivers) **504**. As used herein, the terms "network interface" or "interface" typically refer to any signal, data, or software interface with a component, network or process including for example and without limitation those of the HDMI, FireWire (e.g., FW400, FW800, etc.), USB (e.g., USB2, USB 2.0, USB 3.0, wireless USB), Ethernet (e.g., 10/100, 10/100/1000 (Gigabit Ethernet), 10-Gig-E, etc.), Thunderbolt, or wireless varieties.

The upstream plurality of ports and associated receiving elements **502** may comprise one or more upstream auxiliary channels, one or more upstream media ports, and receiver apparatus (e.g., multiplexing switches, reception logic, clock recovery circuitry, etc.). In one exemplary embodiment, the auxiliary channel is bi-directional and carries management and device control data, and the upstream media ports minimally comprise receivers for unidirectional data lanes, and use of an embedded clock. The receiver apparatus monitors and selectively enables and disables the auxiliary and media ports. In certain embodiments, the receiver apparatus may be adapted to utilize a packet-based unidirectional network protocol, such as the DisplayPort or HDMI protocol previously described herein.

Similarly, the downstream plurality of ports and associated receiving elements **504** comprise one or more downstream auxiliary channels, one or more downstream media ports, and transmitter apparatus (e.g. demultiplexing switches, transmission logic, clock embedding circuitry, etc.). In one exemplary embodiment, the auxiliary channel is bi-directional and carries management and device control data, and the downstream media ports minimally comprise transmitters for unidirectional data lanes, and inclusion of an embedded clock. The transmitter apparatus monitors and selectively enables and disables the auxiliary and media ports. As with the receiver, the transmitter apparatus may be adapted to utilize a packet-based unidirectional network protocol.

In an exemplary implementation, the downstream-facing ports may include a serializer adapted to receive an input word and output a bit stream. For example, in one configuration, the serializer may receive a 10-bit input word and output ten (10) serial bits. In addition, the serializer may also provide an optional corresponding clock.

Conversely, in another configuration, the upstream-facing ports may also include a de-serializer adapted to receive a serial bit stream and output a word. Furthermore, such de-serializing apparatus may additionally require clock recovery circuitry and boundary detection, as is well understood in the digital computing arts. For example, in one embodiment, the de-serializer may receive 10 (ten) serial bits, and convert it into one 10-bit word. When the de-serializer detects a misalignment of timing by one or more bits, the de-serializer accordingly skips or pads its rate accordingly. Furthermore, during initialization, the de-serializer may recognize an initiation sequence.

Also included are one or more storage devices (e.g., a memory subsystem) **510** used to store for example data for transmission or that has been received.

It will be appreciated that not all elements are required in a single device for operation within a "network". For instance, a device only capable of "source" operation would not require upstream ports, or certain audio or video elements. Conversely, a "sink" device may not require downstream ports. Moreover, the "receiver" **502** and "transmitter" **504** elements may comprise transceivers capable of both transmission and reception if desired.

Note that as used herein, such network may be comprised of (without limitation) as few as two devices in communication with one another via an interface, or even two components in communication with one another within the same host apparatus.

The processing subsystem **506** may comprise one or more of central processing units (CPU) or digital processors, such as a microprocessor, digital signal processor, field-programmable gate array, RISC core, or plurality of processing components mounted on one or more substrates.

The processing subsystem is coupled to memory subsystem **510**, which may include for example SRAM, FLASH and SDRAM components. As used herein, the term "memory" includes any type of integrated circuit or other storage device adapted for storing digital data including, without limitation, ROM. PROM, EEPROM, DRAM, SDRAM, DDR/2 SDRAM, EDO/FPMS, RLDRAM, SRAM, "flash" memory (e.g., NAND/NOR), and PSRAM.

The processing subsystem may also comprise additional co-processors, such as a dedicated graphics accelerator, network processor (NP), or audio/video processor. As shown processing subsystem **806** includes discrete components, however it is understood that in some embodiments they may be consolidated or fashioned in a SoC (system-on-chip) configuration.

The processing subsystem **506** is adapted to receive one or more media streams from an upstream apparatus **502** for processing for media displays such as a video display **512**, or audio speakers **514**. Processing subsystem **506** may preferentially comprise graphics processors, applications processors, and or audio processors. In "thin clients", the processing subsystem **506** may be significantly reduced in complexity and limited to simple logic, or in extreme cases altogether non-existent.

It will be readily appreciated by those of ordinary skill that different combinations and/or variations of the foregoing can be made depending on the desired application and performance attributes.

Methods—

Referring now to FIG. **6**, one generalized embodiment of a method **600** for scrambling symbols over multi-lane serial interfaces is disclosed.

At step **602** of the method **600**, a plurality of symbols are scrambled according to at least a corresponding plurality of scrambling values.

In one variant, the scrambling is based on a seed value. The seed value may be fixed or variable. For example, the seed value may be the lane number associated with the symbol. In other embodiments, the seed value may be set according to a pre-determined scheme (e.g., based on time, application, incrementing count, etc.). In certain scenarios, the seed value may be communicated, negotiated, or otherwise actively agreed upon between the transmitter and the receiver.

In another variant, the scrambling values are selected from various taps of a scrambling component. For example, the scrambling values may be any arrangement of bits, nibbles, bytes, word, etc. of an LFSR output. Moreover, the taps may be selected contiguously, non-contiguously, little endian, big endian, etc.

In still another variant, the scrambling values are selected from different scrambling components. For example, the receiver and transmitter may have an array of LFSRs which are assigned to individual lanes, etc.

In some embodiments, the scrambling component is a linear feedback shift register (LFSR). In other embodiments, the scrambling component is a memory with an appropriately randomized sequence of values. In still other embodiments, the scrambling component is an algorithm implemented within software.

Various LFSRs may be used according to design requirements. In some variants, the LFSR is a maximal length LFSR. Alternately, the LFSR may be a self-synchronizing LFSR. In still other scenarios, the LFSR may guarantee a maximum run length.

At step **604** of the method **600**, the plurality of scrambled symbols are transmitted via a corresponding plurality of lanes to a receiver.

At step **606** of the method **600**, the plurality of received scrambled symbols are descrambled. Descrambling is performed in the exemplary embodiment with an appropriately complementary descrambler.

It will be recognized that while certain aspects of the disclosure are described in terms of a specific sequence of steps of a method, these descriptions are only illustrative of the broader methods, and may be modified as required by the particular application. Certain steps may be rendered unnecessary or optional under certain circumstances. Additionally, certain steps or functionality may be added to the disclosed embodiments, or the order of performance of two or more steps permuted. All such variations are considered to be encompassed within the disclosure and claims herein.

While the above detailed description has shown, described, and pointed out novel features of the disclosure as applied to various embodiments, it will be understood that various omissions, substitutions, and changes in the form and details of the device or process illustrated may be made by those skilled in the art. The foregoing description is of the best mode presently contemplated. This description is in no way meant to be limiting, but rather should be taken as illustrative of the general principles, and the scope of the various aspects of the disclosure should be determined with reference to the claims.

What is claimed is:

1. An apparatus configured to scramble a plurality of symbols, comprising:

a first interface that comprises a plurality of lanes, where in a legacy mode each lane is characterized by a common scrambling mechanism and in a non-legacy mode each lane is characterized by a corresponding distinct scrambling mechanism;

a processor in data communication with the first interface; and

a non-transitory computer-readable medium comprising one or more instructions, which when executed by the processor, causes the apparatus to:

when in the non-legacy mode:

transmit a plurality of symbols via the plurality of lanes; and

wherein the plurality of symbols are configured to be descrambled by a receiver, responsive to reception of the plurality of symbols; and

when in the legacy mode:

transmit another plurality of symbols compatible with legacy systems via the plurality of lanes; and

wherein the another plurality of symbols compatible with legacy systems is configured to be descrambled by the receiver, responsive to reception of the another plurality of symbols compatible with legacy systems.

2. The apparatus of claim **1**, wherein in the non-legacy mode each lane of the plurality of lanes is associated with a distinct linear feedback shift register (LFSR).

3. The apparatus of claim **1**, wherein in the non-legacy mode each lane of the plurality of lanes is associated with a plurality of unique bits of one or more linear feedback shift registers (LFSRs).

4. The apparatus of claim **1**, wherein in the non-legacy mode each corresponding distinct scrambling mechanism is self-synchronizing.

5. The apparatus of claim **1**, wherein in the non-legacy mode each corresponding distinct scrambling mechanism is selected to minimize electro-magnetic interference (EMI) with at least one other corresponding distinct scrambling mechanism.

6. A method for scrambling a plurality of symbols, the method comprising:

determining when an apparatus is in a non-legacy mode or in a legacy mode;

when the apparatus is in the non-legacy mode, transmitting a plurality of symbols via a plurality of lanes, where the plurality of symbols are configured to be descrambled by a receiver responsive to reception of the plurality of symbols; and

when the apparatus is in the legacy mode, transmitting another plurality of symbols compatible with legacy systems via the plurality of lanes, where the another plurality of symbols compatible with legacy systems are configured to be received by the receiver responsive to reception of the another plurality of symbols compatible with legacy systems;

wherein when in the legacy mode, the another plurality of symbols transmitted via the plurality of lanes is unscrambled; and

wherein when in the non-legacy mode each of the plurality of lanes is characterized by a corresponding distinct scrambling mechanism.

7. The method of claim **6**, wherein the plurality of symbols are generated by one or more linear feedback shift registers (LFSRs).

8. The method of claim **7**, wherein each one of the one or more LFSRs is characterized by a different characteristic polynomial.

9. The method of claim **7**, wherein each one of the one or more LFSRs is seeded with a different value.

10. The method of claim **7**, wherein a corresponding plurality of scrambling values are generated by different bits of the one or more LFSRs.

11. The method of claim **7**, wherein the one or more LFSRs are self-synchronizing.

12. The method of claim **7**, wherein the one or more LFSRs are selected to maximize a run length.

13. The method of claim **6**, further comprising negotiating a deterministic scheme for generating the plurality of symbols.

14. An apparatus configured to descramble a plurality of symbols, the apparatus comprising:

a first interface that comprises a plurality of lanes, where in a legacy mode each lane is characterized by a not distinct scrambling mechanism and in a non-legacy mode each lane is characterized by a corresponding distinct scrambling mechanism;

a processor in data communication with the first interface; and

a non-transitory computer-readable medium comprising one or more instructions, which when executed by the processor, causes the apparatus to:

determine when to operate in the non-legacy mode or in the legacy mode;

when in the non-legacy mode, receive the plurality of symbols via the plurality of lanes;

for each symbol of the received plurality of symbols, descramble the each symbol according to a corresponding lane; and

otherwise when in the legacy mode, receive another plurality of symbols compatible with legacy systems via the plurality of lanes.

15. The apparatus of claim **14**, further comprising one or more instructions, which when executed by the processor, causes the apparatus to negotiate the distinct scrambling mechanism.

16. A method for descrambling a plurality of symbols, the method comprising:

determining when to operate in a non-legacy mode or in a legacy mode;

when in the non-legacy mode, receiving the plurality of symbols via a multi-lane interface;

when in the legacy mode, receiving another plurality of symbols via the multi-lane interface; and

for each symbol of the received plurality of symbols, descrambling the each symbol according to a corresponding lane, where at least two lanes of the multi-lane interface are characterized by distinct scrambling mechanisms; and

for each symbol of the received another plurality of symbols, descrambling the each symbol, where no lanes of the multi-lane interface are characterized by distinct scrambling mechanisms.

17. The method of claim **16**, wherein the distinct scrambling mechanisms are uncorrelated.

18. The method of claim **17**, wherein the distinct scrambling mechanisms are self-synchronizing.

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