PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5533419

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
JEFFERIES FINANCE LLC	05/17/2019

RECEIVING PARTY DATA

Name:	LATTICE SEMICONDUCTOR CORPORATION
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	SILICON IMAGE, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	SIBEAM, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	DVDO, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124

PROPERTY NUMBERS Total: 1143

Property Type	Number
Patent Number:	5574678
Patent Number:	5510738
Patent Number:	5493205
Patent Number:	5617064
Patent Number:	5670907

Property Type	Number
Patent Number:	5490074
Patent Number:	5596524
Patent Number:	5491433
Patent Number:	5756367
Patent Number:	5594687
Patent Number:	5570046
Patent Number:	5583451
Patent Number:	5621650
Patent Number:	5521529
Patent Number:	5818254
Patent Number:	5781030
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Patent Number:	5589782
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Patent Number:	5764078
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Patent Number:	5594365
Patent Number:	5811986
Patent Number:	5754471
Patent Number:	5594657
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Property Type	Number
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Patent Number:	5672521
Patent Number:	5809522
Patent Number:	5739713
Patent Number:	5736888
Patent Number:	5719516
Patent Number:	5598346
Patent Number:	5623217
Patent Number:	5926841
Patent Number:	5646901
Patent Number:	5751163
Patent Number:	5666087
Patent Number:	5748525
Patent Number:	5864486
Patent Number:	5789939
Patent Number:	5723984
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Patent Number:	5751164
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Patent Number:	5991907
Patent Number:	5805607
Patent Number:	5811987
Patent Number:	5892962
Patent Number:	5717342
Patent Number:	6028993

Property Type	Number
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Patent Number:	5885904
Patent Number:	6190966
Patent Number:	5905385
Patent Number:	5844912
Patent Number:	5835405
Patent Number:	6087275
Patent Number:	6034541
Patent Number:	5949279
Patent Number:	5989957
Patent Number:	5978272
Patent Number:	6028447
Patent Number:	6072351
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Property Type	Number
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Patent Number:	6093946
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Patent Number:	6064225
Patent Number:	5982683
Patent Number:	6556154
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Patent Number:	6133769
Patent Number:	6404006
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Patent Number:	6175266
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Patent Number:	6524911
Patent Number:	6287916
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Patent Number:	6414521
Patent Number:	6496969
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Patent Number:	6993108
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Patent Number:	6870395
Application Number:	10392751
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Patent Number:	6873187
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Patent Number:	6924664
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Patent Number:	6975137
Patent Number:	7382293
Patent Number:	7589648
Patent Number:	7532646
Patent Number:	7245154
Patent Number:	7057397

Property Type	Number
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Patent Number:	7414913
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Patent Number:	7599457
Patent Number:	7295035
Patent Number:	7411419
Patent Number:	7606851
Patent Number:	7187586
Application Number:	11206282
Patent Number:	7301182
Patent Number:	7167405
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Patent Number:	7263024
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Patent Number:	7317343
Patent Number:	7212051
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Property Type	Number
Patent Number:	7538574
Patent Number:	7620839
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Patent Number:	7382169
Patent Number:	7439783
Patent Number:	7547995
Patent Number:	7554357
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Patent Number:	7466190
Patent Number:	7521969
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Property Type	Number
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Patent Number:	7663401
Patent Number:	7535258
Patent Number:	7725803
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Property Type	Number
Patent Number:	7630259
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Patent Number:	8069329
Patent Number:	7652500
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Patent Number:	7459935
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Property Type	Number
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Patent Number:	7768300
Patent Number:	8255733
Patent Number:	7969248
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Property Type	Number
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Patent Number:	8654600
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Patent Number:	8797064
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Application Number:	13155261
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Application Number:	13466463
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Property Type	Number
Application Number:	14021513
Application Number:	14043920
Application Number:	14053026
Application Number:	14070975
Application Number:	14095310
Application Number:	14136482
Application Number:	14137443
Application Number:	14147796
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Application Number:	14482001
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Property Type	Number
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Application Number:	14611069
Application Number:	14611095
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Application Number:	12242665
Application Number:	14196978
Application Number:	14474005
Application Number:	61989417
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Application Number:	61989415

Property Type	Number
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Application Number:	61989411
Application Number:	14463146
Application Number:	14578266
Application Number:	14578257
Application Number:	62089767
Patent Number:	8482462
Patent Number:	8207892
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Application Number:	14196993
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Patent Number:	8571126
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Application Number:	14234623
Application Number:	14240405
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Patent Number:	6374361
Patent Number:	6738417

Property Type	Number
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Patent Number:	6473476
Patent Number:	6867814
Patent Number:	7203557
Patent Number:	7408992
Patent Number:	7123307

Property Type	Number
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Patent Number:	6809567
Patent Number:	7062004
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Application Number:	13770984
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Application Number:	14570817
Application Number:	14589889
Application Number:	14589925
Application Number:	14591845
Application Number:	14449095
Application Number:	12842190

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SIGNATURE:	/Urmila Karandikar/
DATE SIGNED:	05/21/2019
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 97

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RELEASE OF A SECURITY INTEREST -- PATENTS

May 17, 2019

WHEREAS, pursuant to that certain (i) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035222, Frame 0866, (ii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035308, Frame 0428, (iii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035223, Frame 0001, (iv) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035226, Frame 0289, (v) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035223, Frame 0387, (vi) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035226, Frame 0147, (vii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035220, Frame 0048, (viii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035220, Frame 0226, (ix) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035309, Frame 0142, (x) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035308, Frame 0345, (xi) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035225, Frame 0839 and (xii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035225, Frame 0352, LATTICE SEMICONDUCTOR CORPORATION, SILICON IMAGE, INC., SIBEAM, INC. and DVDO, INC., each a Delaware corporation (each, a "Releasee"), granted to JEFFERIES FINANCE LLC, as collateral agent for the ratable benefit of the Secured Creditors (the "Releasor"), a continuing security interest in all right, title and interest of the Releasees in, to and under United States Patents listed on the attached Schedule A (the "Patents"), and all Proceeds in respect thereof (with all of the Releasee's rights listed above being collectively referred to as the "Collateral") to secure the payment, performance and observance of the Obligations;

WHEREAS, the Releasees have satisfied their Obligations; and

WHEREAS, the Releasee has requested and the Releasor has agreed to provide a document suitable for recording in the United States Patent and Trademark Office evidencing and effecting the release, relinquishment and discharge of its security interest in the Collateral.

NOW, THEREFORE, in consideration of and in exchange for good and valuable consideration, the Releasor hereby agrees as follows:

1. Defined Terms. All capitalized terms used but not otherwise defined herein have the meanings given to them in the Grants of Security Interests in United States Patents.

2. Release of Security Interest. The Releasor hereby, without any representation and warranty and without any recourse to the Releasor, releases, relinquishes and discharges all of its security interest in the Collateral.

[Signature Page Follows]

IN WITNESS WHEREOF, the undersigned has executed and delivered this Release as of the date first written above.

JEFFERIES FINANCE LLC,
as Collateral Agent and Releasor

By: _____
Name: Paul Chisholm
Title: Managing Director

[Signature Page to Release of Patent Security Interest]

SCHEDULE A

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/396,994	5574678	United States	Continuous Time Programmable Analog Block Architecture	Issued	Lattice Semiconductor Corporation
08/403,359	5510738	United States	CMOS Programmable Resistor-Based Transconductor	Issued	Lattice Semiconductor Corporation
08/403,354	5493205	United States	Low Distortion Differential Transconductor Output Current Mirror	Issued	Lattice Semiconductor Corporation
08/403,352	5617064	United States	Active Resistor For Stability Compensation [of Transconductor & Op-Amp Based Gain & Filter Stages]	Issued	Lattice Semiconductor Corporation
08/403,595	5670907	United States	VBB Reference for Pumped Substrates	Issued	Lattice Semiconductor Corporation
08/423,303	5490074	United States	Constant delay interconnect for coupling configurable logic blocks	Issued	Lattice Semiconductor Corporation
08/427,117	5596524	United States	CMOS memory cell with gate oxide of both NMOS and PMOS transistors as tunneling window for program and erase	Issued	Lattice Semiconductor Corporation
08/444,306	5491433	United States	Cascode array cell partitioning for a sense amplifier of a programmable logic device	Issued	Lattice Semiconductor Corporation
08/449,384	5756367	United States	Method of making a spacer based antifuse structure for low capacitance and high reliability	Issued	Lattice Semiconductor Corporation
08/447,991	5594687	United States	Completely complementary MOS memory cell with tunneling through the NMOS and PMOS transistors during program and erase	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/453,184	5570046	United States	Lead frame with noisy and quiet Vss and Vdd leads	Issued	Lattice Semiconductor Corporation
08/453,479	5583451	United States	Polarity control circuit which may be used with a ground bounce limiting buffer	Issued	Lattice Semiconductor Corporation
08/456,946	5621650	United States	Programmable gate array with improved interconnect structure, input/output structure and configurable logic block	Issued	Lattice Semiconductor Corporation
08/459,960	5521529	United States	Very high-density complex programmable logic device with a multi-tiered hierarchical switch matrix and optimized flexible logic allocation	Issued	Lattice Semiconductor Corporation
08/459,230	5818254	United States	Multi-tiered hierarchical high speed switch matrix structure for very high-density complex programmable logic devices	Issued	Lattice Semiconductor Corporation
08/459,234	5781030	United States	Programmable uniform symmetrical distribution logic allocator for a high-density complex PLD	Issued	Lattice Semiconductor Corporation
08/459,786	5638018	United States	P-type flip flop	Issued	Lattice Semiconductor Corporation
08/458,865	5589782	United States	Macrocell and clock signal allocation circuit for a programmable logic device (PLD) enabling PLD resources to provide multiple functions	Issued	Lattice Semiconductor Corporation
08/459,570	6531890	United States	Programmable optimized-distribution logic allocator for a high-density complex PLD	Issued	Lattice Semiconductor Corporation
08/461,196	5586044	United States	Array of configurable logic blocks including cascadable lookup tables	Issued	Lattice Semiconductor Corporation
08/462,934	5469368	United States	Array of configurable logic blocks each including a first	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			lookup table coupled to selectively replace an output of second lookup with an alternate function output		Corporation
08/486,178	5764078	United States	Family of multiple segmented programmable logic blocks interconnected by a high speed centralized switch matrix	Issued	Lattice Semiconductor Corporation
08/474,629	5612631	United States	An I/O macrocell for a programmable logic device	Issued	Lattice Semiconductor Corporation
08/479,872	5869981	United States	A High density programmable logic device	Issued	Lattice Semiconductor Corporation
08/486,174	5594365	United States	Architecture of a multiple array high density programmable logic device with a plurality of programmable switch matrices	Issued	Lattice Semiconductor Corporation
08/474,635	5811986	United States	Flexible synchronous/asynchronous cell structure for a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/466,438	5754471	United States	Reference for CMOS memory cell having PMOS and NMOS transistors with a common floating gate	Issued	Lattice Semiconductor Corporation
08/466,438	5754471	United States	Low power CMOS array for a PLD with program and erase using controlled avalanche injection	Issued	Lattice Semiconductor Corporation
08/473,620	5594657	United States	Field Programmable Gate Array Using Look-Up Tables, Multiplexers and Decoders	Issued	Lattice Semiconductor Corporation
08/483,623	5617042	United States	Multiple array programmable logic device with a plurality of programmable switch matrices	Issued	Lattice Semiconductor Corporation
08/492,604	5526278	United States	System for Synthesizing Field Programmable Gate Array	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Implementations From High Level Circuit Descriptions		Corporation
08/493,640	5679599	United States	Isolation using self-aligned trench formation and conventional LOCOS	Issued	Lattice Semiconductor Corporation
08/494,271	5565794	United States	Voltage range tolerant CMOS output buffer with reduced input capacitance	Issued	Lattice Semiconductor Corporation
08/497,992	5742542	United States	Nonvolatile memory cells using only positive charge to store data	Issued	Lattice Semiconductor Corporation
08/500,295	5700698	United States	Method for screening non-volatile memory and programmable logic devices	Issued	Lattice Semiconductor Corporation
08/501,230	5604370	United States	Field Implant For Semiconductor Device	Issued	Lattice Semiconductor Corporation
08/505,837	5635855	United States	Method for Simultaneous Programming of In-System Programmable Integrated Circuits	Issued	Lattice Semiconductor Corporation
08/507,893	5570039	United States	Method and Apparatus for Converting Field-Programmable Gate Array Implementations Into Mask-Programmable Logic Cell Implementations	Issued	Lattice Semiconductor Corporation
08/507,957	5559450	United States	Programmable Function Unit As Parallel Multiplier Cell	Issued	Lattice Semiconductor Corporation
08/528,030	5581126	United States	Interlaced layout configuration for differential pairs of interconnect lines	Issued	Lattice Semiconductor Corporation
08/535,362	5528170	United States	Low-Skew Signal Routing In A Programmable Array	Issued	Lattice Semiconductor Corporation
08/551,974	5615150	United States	control gate-addressed cmos non-volatile cell that programs through gates of CMOS transistors	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/554,092	5587945	United States	CMOS EEPROM cell with tunneling window in the read path	Issued	Lattice Semiconductor Corporation
08/560,038	5666309	United States	Memory cell for a programmable logic device (PLD) avoiding pumping programming voltage above an NMOS threshold	Issued	Lattice Semiconductor Corporation
08/560,933	5587921	United States	Array of configurable logic blocks each including a lookup table having inputs coupled to a first multiplexer and having outputs to a second multiplexer	Issued	Lattice Semiconductor Corporation
08/561,306	5672521	United States	Method of forming multiple gate oxide thicknesses on a wafer substrate	Issued	Lattice Semiconductor Corporation
08/573,622	5809522	United States	Microprocessor system with process identification tag entries to reduce cache flushing after a context switch	Issued	Lattice Semiconductor Corporation
08/574,776	5739713	United States	Deconvolution input buffer compensating for capacitance of a switch matrix of a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/575,898	5736888	United States	Capacitance elimination circuit	Issued	Lattice Semiconductor Corporation
08/575,852	5719516	United States	Clock generator circuit for use with a dual edge register that provides a separate enable for each edge over an input clock signal	Issued	Lattice Semiconductor Corporation
08/596,679	5598346	United States	Array of configurable logic blocks including network means for broadcasting clock signals to different pluralities of logic blocks	Issued	Lattice Semiconductor Corporation
08/606,702	5623217	United States	Field Programmable Gate Array With Write-Port Enabled Memory	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/614,728	5926841	United States	Segment descriptor cache for a processor	Issued	Lattice Semiconductor Corporation
08/625,403	5646901	United States	CMOS memory cell with tunneling during program and erase through the NMOS and PMOS transistors and a pass gate separating the NMOS and PMOS transistors	Issued	Lattice Semiconductor Corporation
08/632,811	5751163	United States	Parallel Programming of ISP Devices Using An Automatic Tester	Issued	Lattice Semiconductor Corporation
08/635,184	5666087	United States	Active Resistor For Stability Compensation [of Transconductor & Op-Amp Based Gain & Filter Stages]	Issued	Lattice Semiconductor Corporation
08/643,807	5748525	United States	Array cell circuit with split read/write line	Issued	Lattice Semiconductor Corporation
08/643,291	5864486	United States	Method And Apparatus For In-System Programming of A Programmable Logic Device Using a Two-Wire Interface	Issued	Lattice Semiconductor Corporation
08/653,186	5789939	United States	Very high-density complex programmable logic device with a multi-tiered hierarchical switch matrix and optimized flexible logic allocation	Issued	Lattice Semiconductor Corporation
08/659,279	5723984	United States	Field programmable gate array (FPGA) with interconnect encoding	Issued	Lattice Semiconductor Corporation
08/659,941	5808942	United States	Field programmable gate array (FPGA) having an improved configuration memory and look up table	Issued	Lattice Semiconductor Corporation
08/664,190	5830795	United States	Simplified masking process for programmable logic device manufacture	Issued	Lattice Semiconductor Corporation
08/666,193	5760609	United States	Clock signal providing circuit with enable and a pulse generator with enable for use	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			in a block clock circuit of a programmable logic device		
08/668,141	5796295	United States	Reference for CMOS memory cell having PMOS and NMOS transistors with a common floating gate	Issued	Lattice Semiconductor Corporation
08/668,896	5751164	United States	Programmable logic device with multi-level power control	Issued	Lattice Semiconductor Corporation
08/683,685	5734275	United States	Programmable logic device having a sense amplifier with virtual ground	Issued	Lattice Semiconductor Corporation
08/683,373	5818294	United States	Temperature insensitive current source	Issued	Lattice Semiconductor Corporation
08/690,768	5801551	United States	Depletion mode pass gates with controlling decoder and negative power supply for a programmable logic device	Issued	Lattice Semiconductor Corporation
08/689,523	5942780	United States	An integrated circuit having, and process providing, different oxide layer thicknesses on a substrate	Issued	Lattice Semiconductor Corporation
08/696,444	5796750	United States	Method for Programming a PLD In An Automatic Tester	Issued	Lattice Semiconductor Corporation
08/700,616	5740069	United States	Logic device (PLD) having direct connections between configurable logic blocks (CLBs) and configurable input/output blocks (IOBs)	Issued	Lattice Semiconductor Corporation
08/699,401	5960274	United States	Oxide formation process for manufacturing programmable logic device	Issued	Lattice Semiconductor Corporation
08/702,846	5959336	United States	Decoder circuit with short channel depletion transistors	Issued	Lattice Semiconductor Corporation
08/710,445	5862365	United States	Configuration Pin Emulation Circuit For a Field Programmable Array	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/723,082	5760605	United States	Programmable high speed routing switch	Issued	Lattice Semiconductor Corporation
08/726,512	5761116	United States	Vpp only scalable EEPROM memory cell having transistors with thin tunnel gate oxide	Issued	Lattice Semiconductor Corporation
08/729,117	5991907	United States	Method for Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/734,888	5805607	United States	Method for user-controlled I/O switching during in-circuit programming of CPLDs through the IEEE 1149.1 test access port	Issued	Lattice Semiconductor Corporation
08/740,948	5811987	United States	Block clock and initialization circuit for a complex high density PLD	Issued	Lattice Semiconductor Corporation
08/748,041	5892962	United States	FPGA-based Processor	Issued	Lattice Semiconductor Corporation
08/745,410	5717342	United States	Output buffer incorporating shared intermediate nodes	Issued	Lattice Semiconductor Corporation
08/781,882	6028993	United States	Timed Circuit Simulation In Hardware Using FPGAs	Issued	Lattice Semiconductor Corporation
08/785,096	5841701	United States	Method of charging and discharging floating gage transistors to reduce leakage current	Issued	Lattice Semiconductor Corporation
08/799,153	5904575	United States	Method and apparatus incorporating nitrogen selectively for differential oxide growth	Issued	Lattice Semiconductor Corporation
08/799,235	5885904	United States	Method to incorporate, and a device having, oxide enhancement dopants using gas immersion laser doping (GILD) for selectively growing an oxide layer	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/823,953	6190966	United States	Process for fabricating semiconductor memory device with high data retention including silicon nitride etch stop layer formed at high temperature with low hydrogen ion	Issued	Lattice Semiconductor Corporation
08/828,520	5905385	United States	Memory bits used to couple look up table inputs to facilitate increased availability to routing resources particularly for variable sized look up tables for a field programmable gate array (FPGA)	Issued	Lattice Semiconductor Corporation
08/831,372	5844912	United States	Fast verify for CMOS memory cell	Issued	Lattice Semiconductor Corporation
08/827,671	5835405	United States	Application Specific Modules in a Programmable Logic Device	Issued	Lattice Semiconductor Corporation
08/843,150	6087275	United States	Reduction of n-channel parasitic transistor leakage by using low power/low pressure phosphosilicate glass	Issued	Lattice Semiconductor Corporation
08/838,487	6034541	United States	In-System Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
08/856,926	5949279	United States	Devices for sourcing constant supply current from power supply in system with integrated circuit having variable supply current requirement	Issued	Lattice Semiconductor Corporation
08/859,761	5989957	United States	Process for fabricating semiconductor memory device with high data retention including silicon nitride etch stop layer formed at high temperature with low hydrogen ion concentration	Issued	Lattice Semiconductor Corporation
08/871,589	5978272	United States	Nonvolatile memory structure for programmable logic devices	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/899,428	6028447	United States	FPGA Having Predictable Open-Drain Drive Mode	Issued	Lattice Semiconductor Corporation
08/912,763	6072351	United States	Output buffer for making a high voltage (5.0 volt) compatible input/output in a low voltage (2.5 volt) semiconductor process	Issued	Lattice Semiconductor Corporation
08/931,798	6359466	United States	Circuitry to provide fast carry	Issued	Lattice Semiconductor Corporation
08/938,550	6020755	United States	Hybrid Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/948,306	6097212	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/947,888	5854114	United States	Data retention of EEPROM cell with shallow trench isolation using thicker liner oxide	Issued	Lattice Semiconductor Corporation
08/949,992	6028463	United States	Programmable Clock Manager For A Programmable Logic Device that Can Generate At Least Two Different Output Clocks	Issued	Lattice Semiconductor Corporation
08/950,444	6216191	United States	Field Programmable Gate Array Having A Dedicated Processor Interface	Issued	Lattice Semiconductor Corporation
08/950,446	5986471	United States	Bi-directional Buffers and Supplemental Logic and Interconnect Cells for Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
08/950,448	6060902	United States	A Programmable Clock Manager For A Programmable Logic Device that Can Be Programmed Without Reconfiguring the Device	Issued	Lattice Semiconductor Corporation
08/950,624	6049224	United States	Programmable Logic Device With Logic Cells Having A Flexible Input Structure	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/951,128	6043677	United States	Programmable Clock Manager For A Programmable Logic Device that Can Implement Delay-Locked Loop Functions	Issued	Lattice Semiconductor Corporation
08/964,421	6389321	United States	Simultaneous Wired and Wireless Remote In-System Programming of Multiple Remote Systems	Issued	Lattice Semiconductor Corporation
08/974,799	6003150	United States	Method for Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/996,361	6275064	United States	Symmetrical, extended and fast direct connections between variable grain blocks in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/996,049	6127843	United States	Dual port SRAM memory for run time use in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,615	6034544	United States	Programmable input/output block (IOB) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,614	5982193	United States	Input/output block (IOB) connections to MAXL lines, NOR lines and dendrites in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,612	5990702	United States	Flexible direct connections between input/output blocks (IOBs) and variable grain blocks (VBGs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/997,221	6107823	United States	Programmable control multiplexing for input/output blocks (IOBs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/996,119	5986480	United States	Multiple input zero power and/nor gate for use in a field programmable gate array (FPGA)	Issued	Lattice Semiconductor Corporation
08/996,530	6134703	United States	A Process for Programming PLDs and Embedded Non-Volatile Memories	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/998,978	6102963	United States	Electrically erasable and reprogrammable, nonvolatile integrated storage device with in-system programming and verification (ISPAV) capabilities for supporting in-system reconfiguring of PLD's	Issued	Lattice Semiconductor Corporation
09/008,762	6130551	United States	Synthesis-friendly FPGA architecture with variable length and variable timing interconnect	Issued	Lattice Semiconductor Corporation
09/010,000	6034538	United States	Virtual Logic System For Reconfigurable Hardware	Issued	Lattice Semiconductor Corporation
09/023,669	6025637	United States	Spacer based antifuse structure for low capacitance and high reliability and method of fabrication thereof	Issued	Lattice Semiconductor Corporation
09/023,506	6023570	United States	Sequential and Simultaneous Manufacturing Programming of Multiple In-System Programmable Systems Through a Data Network	Issued	Lattice Semiconductor Corporation
09/026,814	6093946	United States	EEPROM cell with field-edgeless tunnel window using shallow trench isolation process	Issued	Lattice Semiconductor Corporation
09/037,095	6128770	United States	Configurable logic array including IOB to longlines interconnect means for providing selectable access to plural longlines from each IOB (input/output block)	Issued	Lattice Semiconductor Corporation
09/045,128	6064225	United States	Global Signal Distribution With Reduced Routing Tracks In An FPGA	Issued	Lattice Semiconductor Corporation
09/046,404	5982683	United States	Enhanced method of testing semiconductor devices having nonvolatile elements	Issued	Lattice Semiconductor Corporation
09/053,251	6556154	United States	Offset Voltage Calibration DAC With Reduced Sensitivity To Mismatch	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Errors		
09/059,552	6108806	United States	Method of Testing and Diagnosing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/067,320	6154050	United States	Internal tristate bus with arbitration logic	Issued	Lattice Semiconductor Corporation
09/067,318	6104207	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/069,035	6133750	United States	Combination of global clock and localized clocks	Issued	Lattice Semiconductor Corporation
09/069,768	6002610	United States	Non-Volatile Memory Element For Programmable Logic Applications and Operational Methods Therefor	Issued	Lattice Semiconductor Corporation
09/080,906	6225821	United States	Package migration for related programmable logic devices	Issued	Lattice Semiconductor Corporation
09/083,335	6304099	United States	Method and structure for dynamic in-system programming	Issued	Lattice Semiconductor Corporation
09/083,336	6066977	United States	Programmable Output Voltage Levels	Issued	Lattice Semiconductor Corporation
09/083,205	6255847	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/086,437	6087696	United States	Stacked tunneling dielectric technology for improving data retention of EEPROM cell	Issued	Lattice Semiconductor Corporation
09/109,123	6202182	United States	Method and Apparatus For Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/114,385	6028758	United States	Electrostatic discharge (ESD) protection for a 5.0 volt compatible input/output (I/O) in a 2.5 volt semiconductor process	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/114,717	6091595	United States	Electrostatic discharge (ESD) protection for NMOS pull up transistors of a 5.0 volt compatible output buffer using 2.5 volt process transistors	Issued	Lattice Semiconductor Corporation
09/114,718	6043969	United States	Ballast resistors with parallel stacked NMOS transistors used to prevent secondary breakdown during ESD with 2.5 volt process transistors	Issued	Lattice Semiconductor Corporation
09/115,683	6124732	United States	Signaling Voltage Range Discriminator	Issued	Lattice Semiconductor Corporation
09/118,200	6028446	United States	Flexible Synchronous and Asynchronus Circuits for A Very High Density Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/134,174	6064105	United States	Data retention of EEPROM cell with shallow trench isolation using thicker liner oxide	Issued	Lattice Semiconductor Corporation
09/145,793	6087854	United States	High Speed Line Driver With Direct and Complementary Outputs	Issued	Lattice Semiconductor Corporation
09/169,848	6347387	United States	Test Circuits For Multiple FPGA Systems	Issued	Lattice Semiconductor Corporation
09/169,492	6424003	United States	EEPROM cell with self-aligned tunneling window	Issued	Lattice Semiconductor Corporation
09/187,691	6228696	United States	Semiconductor-oxide-semiconductor capacitor formed in integrated circuit	Issued	Lattice Semiconductor Corporation
09/187,689	6154051	United States	Tileable and compact layout for super variable grain blocks within FPGA device	Issued	Lattice Semiconductor Corporation
09/186,917	6229336	United States	Programmable integrated circuit device with slew control and skew control	Issued	Lattice Semiconductor Corporation
09/188,778	6169432	United States	High voltage switch for	Issued	Lattice

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			providing voltages higher than 2.5 volts with transistors made using a 2.5 volt process		Semiconductor Corporation
09/192,094	6291327	United States	Optimization of S/D annealing to minimize random S/D shorts in memory array	Issued	Lattice Semiconductor Corporation
09/192,096	6221733	United States	Reduction of mechanical stress in shallow trench isolation process	Issued	Lattice Semiconductor Corporation
09/196,449	6191612	United States	Enhanced I/O control flexibility for generating control signals	Issued	Lattice Semiconductor Corporation
09/196,080	5912550	United States	Power converter with 2.5 semiconductor process components	Issued	Lattice Semiconductor Corporation
09/198,796	6218857	United States	Variable sized line driving amplifiers for input/output blocks (IOBs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/200,395	6261944	United States	Semiconductor device having high reliability passivation and fabrication method	Issued	Lattice Semiconductor Corporation
09/198,653	6009033	United States	Method of programming and erasing an EEPROM device under an elevated temperature and apparatus thereof	Issued	Lattice Semiconductor Corporation
09/199,664	6353352	United States	Clock tree topology	Issued	Lattice Semiconductor Corporation
09/201,081	6133769	United States	Phase locked loop with a lock detector	Issued	Lattice Semiconductor Corporation
09/203,149	6404006	United States	EEPROM cell with tunneling across entire separated channels	Issued	Lattice Semiconductor Corporation
09/217,647	5969992	United States	EEPROM cell using p-well for	Issued	Lattice Semiconductor Corporation
09/207,558	6175266	United States	Operational amplifier with CMOS transistors made using	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			2.5 volt process transistors		Corporation
09/208,203	6163168	United States	Efficient interconnect network for use in FPGA device having variable grain architecture	Issued	Lattice Semiconductor Corporation
09/212,022	6124730	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/212,330	6100715	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/212,331	6081473	United States	FPGA integrated circuit having embedded SRAM memory blocks each with statically and dynamically controllable read mode	Issued	Lattice Semiconductor Corporation
09/216,662	6204686	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	Issued	Lattice Semiconductor Corporation
09/216,051	6214666	United States	Method of forming a non-volatile memory device	Issued	Lattice Semiconductor Corporation
09/217,648	6232631	United States	Floating gate memory cell structure with programming mechanism outside the read path	Issued	Lattice Semiconductor Corporation
09/217,646	6282123	United States	Method of fabricating, programming, and erasing a dual pocket two sided program/erase non-volatile memory cell	Issued	Lattice Semiconductor Corporation
09/218,987	6294810	United States	EEPROM cell with tunneling at separate edge and channel regions	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/220,469	6157568	United States	Avalanche programmed floating gate memory cell structure with program element in first polysilicon layer	Issued	Lattice Semiconductor Corporation
09/221,360	6294809	United States	Avalanche programmed floating gate memory cell structure with program element in polysilicon	Issued	Lattice Semiconductor Corporation
09/226,702	6215700	United States	PMOS avalanche programmed floating gate memory cell structure	Issued	Lattice Semiconductor Corporation
09/227,981	6197638	United States	Oxide formation process for manufacturing programmable logic device	Issued	Lattice Semiconductor Corporation
09/235,356	6097664	United States	Multi-port SRAM cell array having plural write paths including for writing through addressable port and through serial boundary scan	Issued	Lattice Semiconductor Corporation
09/235,351	6181163	United States	FPGA integrated circuit having embedded SRAM memory blocks and interconnect channel for broadcasting address and control	Issued	Lattice Semiconductor Corporation
09/235,615	6211695	United States	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	Issued	Lattice Semiconductor Corporation
09/239,072	5999449	United States	Two transistor EEPROM cell using P-well for tunneling across a channel	Issued	Lattice Semiconductor Corporation
09/240,560	6297128	United States	Process for manufacturing shallow trenches filled with dielectric material having low mechanical stress	Issued	Lattice Semiconductor Corporation
09/245,813	6294811	United States	Two transistor EEPROM cell	Issued	Lattice Semiconductor Corporation
09/255,410	6075724	United States	Method for sorting	Issued	Lattice

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			semiconductor devices having a plurality of non-volatile memory cells		Semiconductor Corporation
09/255,053	6255169	United States	Process for fabricating a high-endurance non-volatile memory device	Issued	Lattice Semiconductor Corporation
09/256,245	6133164	United States	Fabrication of oxide regions having multiple thicknesses using minimized number of thermal cycles	Issued	Lattice Semiconductor Corporation
09/261,776	6256758	United States	Fault Tolerance Operation of Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/263412	6075293	United States	Semiconductor device having a multi-layer metal interconnect structure	Issued	Lattice Semiconductor Corporation
09/268,897	6207989	United States	Non-volatile memory device having a high-reliability composite insulation layer	Issued	Lattice Semiconductor Corporation
09/276,991	6031365	United States	Band gap reference using a low voltage power supply	Issued	Lattice Semiconductor Corporation
09/276,990	6163175	United States	High voltage detector to control a power supply voltage pump for a 2.5 volt semiconductor process device	Issued	Lattice Semiconductor Corporation
09/277,441	6326663	United States	Avalanche injection EEPROM memory cell with p-type control gate	Issued	Lattice Semiconductor Corporation
09/280,887	6172392	United States	Boron doped silicon capacitor plate	Issued	Lattice Semiconductor Corporation
09/286,830	6284626	United States	Angled nitrogen ion implantation for minimizing mechanical stress on side walls of an isolation trench	Issued	Lattice Semiconductor Corporation
09/288,062	6265900	United States	High Speed Logical OR Circuit	Issued	Lattice Semiconductor Corporation
09/287,976	6413826	United States	Gate insulator process for	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			nanometer MOSFETs		Corporation
09/310,071	6424000	United States	Floating gate memory apparatus and method for selected programming thereof	Issued	Lattice Semiconductor Corporation
09/316,241	6274898	United States	Triple-well EEPROM cell using p-well for tunneling across a channel	Issued	Lattice Semiconductor Corporation
09/318,570	6552595	United States	High Voltage Discharge Scheme	Issued	Lattice Semiconductor Corporation
09/320389	6118693	United States	Electrically erasable non-volatile memory cell with integrated SRAM to reduce testing time	Issued	Lattice Semiconductor Corporation
09/320,392	6067252	United States	Electrically erasable non-volatile memory cell with no static power dissipation	Issued	Lattice Semiconductor Corporation
09/326,940	6184713	United States	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	Issued	Lattice Semiconductor Corporation
09/326,140	6150841	United States	Enhanced storage macrocell module for high density CPLD architectures	Issued	Lattice Semiconductor Corporation
09/330,753	6628660	United States	Finite State Machine with Associated Memory	Issued	Lattice Semiconductor Corporation
09/334,051	6028789	United States	Zero-power CMOS non-volatile memory cell having an avalanche injection element	Issued	Lattice Semiconductor Corporation
09/334,052	6034893	United States	Non-volatile memory cell having dual avalanche injection elements	Issued	Lattice Semiconductor Corporation
09/400,029	6404226	United States	Integrated Circuit With Standard Cell Logic and Spare Gates	Issued	Lattice Semiconductor Corporation
09/405,958	6550030	United States	On-Line Testing of the Programmable Logic Blocks In Field Programmable Gate	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Arrays		
09/406,219	6574761	United States	On-Line Testing of the Programmable Interconnect Network In Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/433,642	6191609	United States	Combination of global clock and localized clocks	Issued	Lattice Semiconductor Corporation
09/440,460	6294925	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/440,207	6278311	United States	Method for minimizing instantaneous currents when driving bus signals	Issued	Lattice Semiconductor Corporation
09/441,220	6208559	United States	Method of operating EEPROM memory cells having transistors with thin gate oxide and reduced disturb	Issued	Lattice Semiconductor Corporation
09/452,017	6137738	United States	Method For In-System Programming of Serially Configured EEPROMS Using a JTAG Interface of an FPGA	Issued	Lattice Semiconductor Corporation
09/454,322	6326808	United States	Inversion of Product Term Line Before or Logic in a Programmable Logic Device (PLD)	Issued	Lattice Semiconductor Corporation
09/472,645	6150842	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/506,180	6362684	United States	Amplifier Having an Adjustable Resistor Network	Issued	Lattice Semiconductor Corporation
09/507,580	6424209	United States	Integrated Programmable Continuous Time Filter with Programmable Capacitor Arrays	Issued	Lattice Semiconductor Corporation
09/548,171	6351157	United States	Output buffer for making a high voltage (5.0 volt) compatible input/output in a low voltage (2.5 volt)	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			semiconductor process		
09/567,898	6288937	United States	Decoded Generic Routing Pool	Issued	Lattice Semiconductor Corporation
09/578,086	6570212	United States	Complementary avalanche injection EEPROM cell	Issued	Lattice Semiconductor Corporation
09/603,119	6292930	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/603,807	6216257	United States	FPGA device and method that includes a variable grain function architecture for implementing configuration logic blocks and a complimentary variable length interconnect architecture for providing configurable routing between configuration logic blocks	Issued	Lattice Semiconductor Corporation
09/611,449	6530049	United States	On-line Fault Tolerant Operation Via Incremental Reconfiguration of Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/626,094	6380759	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/632,319	6567969	United States	Configurable Logic Array Including Lookup Table Means For Generating Functions of Different Numbers Of Input Terms	Issued	Lattice Semiconductor Corporation
09/643,279	6627947	United States	Compact single-poly two-transistor EEPROM cell	Issued	Lattice Semiconductor Corporation
09/651,689	6433602	United States	High speed schmitt trigger with low supply voltage	Issued	Lattice Semiconductor Corporation
09/660,707	6370071	United States	High Voltage CMOS switch	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
09/661,585	6462576	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/668,896	6701340	United States	Double Differential Comparator and Programmable Analog Block Architecture Using Same	Issued	Lattice Semiconductor Corporation
09/669,186	6249144	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/671,853	6631487	United States	On-Line Testing of Field Programmable Gate Array Resources	Issued	Lattice Semiconductor Corporation
09/692,694	6470485	United States	Scalable and parallel processing methods and structures for testing configurable interconnect network in FPGA device	Issued	Lattice Semiconductor Corporation
09/704,487	6507212	United States	Wide input programmable logic system and method	Issued	Lattice Semiconductor Corporation
09/651,805	6455912	United States	Process for manufacturing shallow trenches filled with dielectric material having low mechanical stress	Issued	Lattice Semiconductor Corporation
09/712,000	6356107	United States	Method and structure for dynamic in-system programming	Issued	Lattice Semiconductor Corporation
09/721,153	6348813	United States	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	Issued	Lattice Semiconductor Corporation
09/732,216	6735706	United States	Programmable power management system and method	Issued	Lattice Semiconductor Corporation
09/731,184	6524911	United States	Combination of BPTEOS oxide film with CMP and RTA to achieve good data	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			retention		
09/731,185	6287916	United States	Method for forming a semiconductor device using LPCVD nitride to protect floating gate from charge loss	Issued	Lattice Semiconductor Corporation
09/733,878	6526558	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	Issued	Lattice Semiconductor Corporation
09/775,488	6462602	United States	Voltage Level Translator Systems And Methods	Issued	Lattice Semiconductor Corporation
09/775,489	6414521	United States	Improved sense amplifier systems and methods	Issued	Lattice Semiconductor Corporation
09/818,257	6496969	United States	Programming Programmable Logic Devices Using Hidden Switches	Issued	Lattice Semiconductor Corporation
09/841,209	6590415	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/863,656	6535043	United States	Clock Signal Selection System, Method of Generating A Clock Signal And Programmable Clock Manager Including Same	Issued	Lattice Semiconductor Corporation
09/864,276	6486705	United States	Signal Distribution Scheme In Field Programmable Gate Array (FPGA) or Field Programmable Systems Chip (FPSC) Including Cycle Stealing Units	Issued	Lattice Semiconductor Corporation
09/864,284	6472904	United States	Double Data Rate Input And Output In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/864,289	6480026	United States	Multi-functional I/O Buffers In a Field Programmable Gate	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Array (FPGA)		Corporation
09/864,277	6483342	United States	Multi-Master Multi-Slave Bus In Field Programmable Gate Array (FPGA)	Issued	Lattice Semiconductor Corporation
09/864,290	6772230	United States	Field Programmable Gate Array (FPGA) Bit Stream Format	Issued	Lattice Semiconductor Corporation
09/870,877	6498538	United States	Low Jitter Integrated Phase Locked Loop With Broad Tuning Range	Issued	Lattice Semiconductor Corporation
09/870,541	6455375	United States	EEPROM tunnel window for program injection via P+ contacted inversion	Issued	Lattice Semiconductor Corporation
09/881,950	6614291	United States	Low Voltage, High Speed CMOS CML Latch and MUX Devices	Issued	Lattice Semiconductor Corporation
09/885,243	6429692	United States	High Speed Data Sampling With Reduced Metastability	Issued	Lattice Semiconductor Corporation
09/927,289	6492877	United States	Improved Coupling For LC-Based VCO	Issued	Lattice Semiconductor Corporation
09/927,612	6525617	United States	Buffering For LC-Based Stage	Issued	Lattice Semiconductor Corporation
09/927,793	6653860	United States	Enhanced logic macrocell with expanded PT (product term) sharing capability for Use in High Density CPLD Architectures	Issued	Lattice Semiconductor Corporation
09/941,454	6489835	United States	Low Voltage Bandgap Reference Circuit	Issued	Lattice Semiconductor Corporation
09/949,112	6593222	United States	Method to improve the reliability of thermosonic gold to aluminum wire bonds	Issued	Lattice Semiconductor Corporation
09/966,967	6832231	United States	Multiple Width Random Number Generation	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/011,549	6693830	United States	Single Poly Two-Transistor EEPROM Cell With Differentially Doped Floating Gate	Issued	Lattice Semiconductor Corporation
10/053,004	6989551	United States	Test structure for determining the minimum tunnel opening size in a non-volatile memory cell	Issued	Lattice Semiconductor Corporation
10/010,011	6515899	United States	Non-Volatile Memory Cell With Enhanced Cell Drive Current	Issued	Lattice Semiconductor Corporation
09/991,245	6611463	United States	Zero Power Programmable Memory Cell	Issued	Lattice Semiconductor Corporation
09/992,493	6489806	United States	Zero power logic cell for use in programmable logic devices	Issued	Lattice Semiconductor Corporation
10/006,559	7003066	United States	Digital Phase locked Loop with Phase Selector having Minimized Number of Phase Interpolators	Issued	Lattice Semiconductor Corporation
10/006,610	6999543	United States	Clock Data Recovery Deserializer With Programmable Sync Detect Logic	Issued	Lattice Semiconductor Corporation
10/006,516	6993108	United States	Digital Phase Locked Loop With Programmable Digital Filter	Issued	Lattice Semiconductor Corporation
10/021,873	6661254	United States	Programmable Interconnect Circuit With A Phase-Locked Loop	Issued	Lattice Semiconductor Corporation
10/017,725	6674303	United States	Programmable I/O cell with bidirectional and shift register capabilities	Issued	Lattice Semiconductor Corporation
10/017,859	6605959	United States	Structure and Method for Implementing Wide Multiplexers	Issued	Lattice Semiconductor Corporation
10/022,464	7154298	United States	Block oriented architecture for programmable interconnect circuit	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/021,844	6703860	United States	I/O Block for Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/023,053	6653861	United States	Multi-level Routing Structure for a Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/023,226	6650141	United States	High Speed Interface For a Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/059,624	6636442	United States	Non-volatile memory element having a cascoded transistor scheme to reduce oxide field stress	Issued	Lattice Semiconductor Corporation
10/061,057	6845044	United States	Method of preventing high Icc at start-up in zero-power EEPROM cells for PLD applications	Issued	Lattice Semiconductor Corporation
10/066,031	6680625	United States	Symmetrical CML Logic Gate System	Issued	Lattice Semiconductor Corporation
10/082,050	6781170	United States	Integrated Circuit Base Transistor Structure And Associated Programmable Cell Library	Issued	Lattice Semiconductor Corporation
10/083,728	6600188	United States	An EEPROM with neutralized doping at tunnel window edge	Issued	Lattice Semiconductor Corporation
10/090,209	6621298	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
10/103,100	6795959	United States	Integrated Delay Discriminator For Use With a Field- Programmable Gate Array and A Method of Determining a Time Delay Thereof	Issued	Lattice Semiconductor Corporation
10/106,509	6907439	United States	FFT address generation method and apparatus	Issued	Lattice Semiconductor Corporation
10/108,401	6976047	United States	Skipped carry incrementer for FFT address generation	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/112,370	6639431	United States	Differential Input Comparator	Issued	Lattice Semiconductor Corporation
10/128,943	6660579	United States	Zero Power Memory Cell With Improved Data Retention	Issued	Lattice Semiconductor Corporation
10/131,883	7032162	United States	Polynomial Expander for Generating Coefficients of a Polynomial from Roots of the Polynomial	Issued	Lattice Semiconductor Corporation
10/133,016	6765408	United States	Device and Method with Generic Logic Blocks	Issued	Lattice Semiconductor Corporation
10/135,308	6814296	United States	Integrated Circuit and Associated Design Method With Antenna Error Control Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/135,325	6600341	United States	Integrated Circuit and Associated Design Method Using Spare Gate Islands	Issued	Lattice Semiconductor Corporation
10/146,739	6714048	United States	Input Buffer With Selectable PCL, GTL, or PECL Compatibility	Issued	Lattice Semiconductor Corporation
10/146,826	6657458	United States	Output Buffer With Feedback From An Input Buffer To Provide Selectable PCL, GTL, or PECL Compatability	Issued	Lattice Semiconductor Corporation
10/146,769	6870391	United States	Input Buffer With CMOS Driver Gate Current Control Enabling Selectable PCL, GTL, or PECL Compatibility	Issued	Lattice Semiconductor Corporation
10/147,199	6714043	United States	Output Buffer Having Programmable Drive Current And Output Voltage Limits	Issued	Lattice Semiconductor Corporation
10/146,734	6720755	United States	Band Gap Reference Circuit	Issued	Lattice Semiconductor Corporation
10/147,011	6760209	United States	Electrostatic Discharge Protection Circuit	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/151,753	6798244	United States	Output Buffer With Overvoltage Protection	Issued	Lattice Semiconductor Corporation
10/150,410	6848095	United States	Method of Assigning Logic Functions To Macrocells In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/159,009	6583652	United States	Highly linear programmable transconductor with large input-signal range	Issued	Lattice Semiconductor Corporation
10/159,089	6717451	United States	Precision analog level shifter with programmable options	Issued	Lattice Semiconductor Corporation
10/159,681	6806771	United States	Multimode output stage converting differential to single-ended signals using current-mode input signals	Issued	Lattice Semiconductor Corporation
10/162,337	6596587	United States	Shallow junction EEPROM Device and Process for Fabricating the Device	Issued	Lattice Semiconductor Corporation
10/160,855	6794236	United States	EEPROM Device with Improved Capacitive Coupling and Fabrication Process	Issued	Lattice Semiconductor Corporation
10/161,283	6716705	United States	EEPROM Device having a Retrograde Program Junction Region And Process for Fabrication the Device	Issued	Lattice Semiconductor Corporation
10/164,484	6703305	United States	Semiconductor Device Having Metallized Interconnect Structure And Method Of Fabricaton	Issued	Lattice Semiconductor Corporation
10/187,236	6844757	United States	Converting Bits to Vectors In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/191,888	6650143	United States	FPGA Based Upon Transistor gate Oxide Breakdown	Issued	Lattice Semiconductor Corporation
10/194,771	7028281	United States	FPGA With Register-Intensive Architecture	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/200,645	6714066	United States	Integrated Programmable Continuous Time Filter with Programmable Capacitor Arrays	Issued	Lattice Semiconductor Corporation
10/207,292	6683477	United States	Wide input programmable logic system and method	Issued	Lattice Semiconductor Corporation
10/210,367	6938197	United States	CRC Calculation System And Method For A Packet Arriving On An N-Byte Wide Bus	Issued	Lattice Semiconductor Corporation
10/211,125	6545313	United States	EEPROM tunnel window for program injection via P+ contacted inversion	Issued	Lattice Semiconductor Corporation
10/219,046	6650142	United States	Enhanced CPLD Macrocell Module Having Selectable Bypass of Steering-based Resource Allocation and Methods of Use	Issued	Lattice Semiconductor Corporation
10/233,021	7043511	United States	Performing Conditional Operations In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/232,912	6841447	United States	EEPROM Device Having An Isolation -Bounded Tunnel Capacitor And Fabrication Process	Issued	Lattice Semiconductor Corporation
10/235,380	6725442	United States	Scalable and parallel processing methods and structures for testing configurable interconnect network in FPGA device	Issued	Lattice Semiconductor Corporation
10/236,829	6842372	United States	EEPROM Cell Having Floating Gate Transistor Within a Cell Well And a Process For Fabricating the Memory Cell	Issued	Lattice Semiconductor Corporation
10/236,114	6833602	United States	Device Having Electrically Isolated Low Voltage And High Voltage Regions And Process For Fabricating the Device	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/236,718	6649514	United States	EEPROM Device Having Improved Data Retention And Process for Fabricating The Device	Issued	Lattice Semiconductor Corporation
10/242,809	6738306	United States	Multiport SRAM Cell	Issued	Lattice Semiconductor Corporation
10/243,014	6917536	United States	Memory access Circuit and Method for reading and writing data with the same clock signal	Issued	Lattice Semiconductor Corporation
10/251,608	6700154	United States	EEPROM cell with trench coupling capacitor	Issued	Lattice Semiconductor Corporation
10/255,474	6907592	United States	Method of Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,875	6809551	United States	Method of Optimizing Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,499	6803787	United States	State Machine In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,656	6812738	United States	Vector Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/263,251	6748575	United States	Programming Programmable Logic Devices Using Hidden Switches	Issued	Lattice Semiconductor Corporation
10/263,507	6846714	United States	Voltage Limted EEPROM Device And Process For Fabricating the Device	Issued	Lattice Semiconductor Corporation
10/266,361	6639434	United States	Low voltage differential signaling systems and methods	Issued	Lattice Semiconductor Corporation
10/269,804	7111183	United States	Expansion method for complex power-sequencing applications	Issued	Lattice Semiconductor Corporation
10/269,450	6791394	United States	Power Supply Control Circuits	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/269,439	6762618	United States	Innovative verify scheme for two level GRP fuse in programmable bus switching family	Issued	Lattice Semiconductor Corporation
10/272,582	6901572	United States	Power Sequence Controller Programming Technique	Issued	Lattice Semiconductor Corporation
10/278,415	6639449	United States	Asynchronous glitch-free clock multiplexer	Issued	Lattice Semiconductor Corporation
10/282,524	7051261	United States	Turbo Encoder With Reduced Processing Delay	Issued	Lattice Semiconductor Corporation
10/283,765	6700823	United States	Programmable common mode termination for differential input/output circuits	Issued	Lattice Semiconductor Corporation
10/288,667	7000210	United States	Adaptive Adjustment Of Constraints During PLD Placement Processing	Issued	Lattice Semiconductor Corporation
10/288,668	6813754	United States	Placement Processing For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/300,190	6825733	United States	Low Jitter Integrated Phase Locked Loop With Broad Tuning Range	Issued	Lattice Semiconductor Corporation
10/302,439	6797568	United States	Flash Technology Transistors and Method For Forming Same	Issued	Lattice Semiconductor Corporation
10/308,420	6710641	United States	Low Voltage Bandgap Reference Circuit	Issued	Lattice Semiconductor Corporation
10/309,302	6650188	United States	Improved Coupling For LC-Based VCO	Issued	Lattice Semiconductor Corporation
10/334,642	6777979	United States	FIFO memory architecture	Issued	Lattice Semiconductor Corporation
10/338,619	6753696	United States	Programmable optimized-distribution logic allocator for	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			a high-density complex PLD		Corporation
10/365,083	7034596	United States	Adaptive input logic for phase adjustments	Issued	Lattice Semiconductor Corporation
10/368,023	6915323	United States	Macrocells Supporting A Carry Cascade	Issued	Lattice Semiconductor Corporation
10/366,956	6788101	United States	Programmable input buffer for differential and single-ended signals	Issued	Lattice Semiconductor Corporation
10/367,323	6812869	United States	Noise Reduction Techniques For Programmable I/O Circuits	Issued	Lattice Semiconductor Corporation
10/370,232	6861870	United States	Dynamic Cross point Switch With Shadow Memory Architecture	Issued	Lattice Semiconductor Corporation
10/377,320	6859066	United States	Bank based input/output buffers in field programmable gate arrays with multiple reference voltages	Issued	Lattice Semiconductor Corporation
10/387,814	7305047	United States	Automatic lane assignment for Receiver	Issued	Lattice Semiconductor Corporation
10/387,243	7339952	United States	Pointer Processing For Optical Communication Systems	Issued	Lattice Semiconductor Corporation
10/391,094	6870395	United States	PLDs With Integrated Standard Cell Logic Blocks	Issued	Lattice Semiconductor Corporation
10/392,751	RE39510	United States	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	Issued	Lattice Semiconductor Corporation
10/397,669	6967500	United States	Electronic Circuit With OnChip Programmable Terminations	Issued	Lattice Semiconductor Corporation
10/400,705	6873187	United States	Method and Apparatus for Controlling Signal Distribution In An Electronic	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Circuit		
10/406,050	7000212	United States	Hierarchical General Interconnect Architecture For High Density FPGA's	Issued	Lattice Semiconductor Corporation
10/409,543	6986004	United States	FIFO memory with programmable data port widths	Issued	Lattice Semiconductor Corporation
10/417,290	6879184	United States	Programmable logic device architecture based on arrays of LUT-based Boolean terms	Issued	Lattice Semiconductor Corporation
10/425,863	6903575	United States	Scalable device architecture for high-speed interfaces	Issued	Lattice Semiconductor Corporation
10/425,862	6894530	United States	Programmable And Fixed Logic Circuitry For High-Speed Interfaces	Issued	Lattice Semiconductor Corporation
10/428,889	6879182	United States	CPLD with multi-function blocks and distributed memory	Issued	Lattice Semiconductor Corporation
10/428,885	6861871	United States	Cascaded logic block architecture for complex programmable logic devices	Issued	Lattice Semiconductor Corporation
10/428,888	6864713	United States	Multi-Stage Interconnect Architecture For Complex Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/428,982	6922078	United States	Enhanced wide and deep logic capability for high density, high performance CPLDs	Issued	Lattice Semiconductor Corporation
10/439,602	6828823	United States	Non-volatilie and reconfigurable PLDs	Issued	Lattice Semiconductor Corporation
10/441,814	7039842	United States	Measuring Propagation Delays of Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/447,120	7301996	United States	skew cancellation for source synchronous clock and data signals	Issued	Lattice Semiconductor Corporation
10/447,451	7009433	United States	Digitally Controlled Delay Cells	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/457,630	7304863	United States	Integrated Circuit Including External Electronic Components With Low Insertion Loss	Issued	Lattice Semiconductor Corporation
10/459,091	6879598	United States	Flexible Media Access Control Architecture	Issued	Lattice Semiconductor Corporation
10/460,385	6856171	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
10/463,781	6861868	United States	High Speed Interface For A Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/464,083	6882555	United States	Bi-directional buffering for memory data lines	Issued	Lattice Semiconductor Corporation
10/600,042	6822477	United States	Integrated Circuit And Associated Design Method Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/610,253	6977408	United States	High-Performance Non-volatile Memory Device and Fabrication Process	Issued	Lattice Semiconductor Corporation
10/613,460	7132903	United States	Noise-shielding, switch-controlled load circuitry for oscillators and the like	Issued	Lattice Semiconductor Corporation
10/613,462	6952115	United States	Programmable I/O Interfaces For FPGAs And Other PLDs	Issued	Lattice Semiconductor Corporation
10/617,980	6958625	United States	PLD With Hardwired Microsequencer	Issued	Lattice Semiconductor Corporation
10/619,711	6903573	United States	Programmable Logic Device With Enhanced Wide Input Product Term Cascading	Issued	Lattice Semiconductor Corporation
10/620,286	6919736	United States	FPGA having partitionable embedded memory with configurable depth and width	Issued	Lattice Semiconductor Corporation
10/619,645	7098685	United States	Scalable Serializer-Deserializer Architecture and	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Programmable Interface		Corporation
10/620,147	7032203	United States	Algorithm to increase logic input width by cascading product terms	Issued	Lattice Semiconductor Corporation
10/624,965	6940309	United States	Programmable Logic Device With A Memory-Based Finite State Machine	Issued	Lattice Semiconductor Corporation
10/626,089	6737702	United States	Zero Power Memory Cell with Reduced Threshold Voltage	Issued	Lattice Semiconductor Corporation
10/628,656	6970047	United States	Programmable lock detector and corrector	Issued	Lattice Semiconductor Corporation
10/628,657	6924659	United States	Programmable Signal Termination for FPGAs and the Like	Issued	Lattice Semiconductor Corporation
10/629,223	7019577	United States	Clock Generator	Issued	Lattice Semiconductor Corporation
10/629,512	6903574	United States	Memory Access Via Serial Memory Interface	Issued	Lattice Semiconductor Corporation
10/629,221	6885227	United States	Clock Generator With Skew Control	Issued	Lattice Semiconductor Corporation
10/640,804	6877667	United States	Integrated Circuit And Associated Design Method With Antenna Error Control Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/640,828	6838904	United States	Enhanced CPLD Macrocell Module Having Selectable Bypass of Steering-Based Resource Allocation	Issued	Lattice Semiconductor Corporation
10/641,260	6940779	United States	Programmable broadcasting initialization of embedded memory blocks on FPGA	Issued	Lattice Semiconductor Corporation
10/642,370	6924664	United States	FPGA	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/655,686	6842037	United States	Shared Transmission Line Communication System and Method	Issued	Lattice Semiconductor Corporation
10/660,814	7038490	United States	Delay matched ASIC conversion of a PLD	Issued	Lattice Semiconductor Corporation
10/665,920	6970022	United States	Controlled hysteresis comparator with rail-to-rail input	Issued	Lattice Semiconductor Corporation
10/671,378	6943583	United States	Programmable I/O structure for FPGAs and the like having reduced pad capacitance	Issued	Lattice Semiconductor Corporation
10/671,363	6943582	United States	Programmable I/O structure for FPGAs and the Like Having Shared Circuitry	Issued	Lattice Semiconductor Corporation
10/671,756	6909663	United States	Multiport Memory With Twisted Bitlines	Issued	Lattice Semiconductor Corporation
10/676,536	7269771	United States	Semiconductor Device Adapted For Forming Multiple Scan Chains	Issued	Lattice Semiconductor Corporation
10/687,468	6809674	United States	Analog-to-digital converters	Issued	Lattice Semiconductor Corporation
10/699,321	7067883	United States	Lateral High-Voltage Junction Device	Issued	Lattice Semiconductor Corporation
10/701,005	7091763	United States	Clock generation	Issued	Lattice Semiconductor Corporation
10/704,025	7088134	United States	PLD With Flexible Memory Allocation And Routing	Issued	Lattice Semiconductor Corporation
10/726,972	7100058	United States	Programmable Power Management System And Method	Issued	Lattice Semiconductor Corporation
10/728,685	7187157	United States	Power supply remote voltage sensing	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/737,514	6981381	United States	Linear Thermoelectric Device Driver	Issued	Lattice Semiconductor Corporation
10/744,353	7132864	United States	Method for configuring multiple-output phase-locked loop frequency synthesizer	Issued	Lattice Semiconductor Corporation
10/769,174	7024646	United States	Electrostatic Discharge Simulation	Issued	Lattice Semiconductor Corporation
10/768,643	7019584	United States	Output Stages For High Current Low Noise Bandgap Reference Circuit Implementations	Issued	Lattice Semiconductor Corporation
10/782,564	6972986	United States	Combination FPGA	Issued	Lattice Semiconductor Corporation
10/783,886	7081771	United States	Upgradeable And Reconfigurable Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/791,073	7191388	United States	Fast diagonal interleaved parity (DIP) calculator	Issued	Lattice Semiconductor Corporation
10/794,079	7257727	United States	Timer Systems and Methods	Issued	Lattice Semiconductor Corporation
10/794,524	7017063	United States	systems and methods for controlling voltage regulator module power supplies	Issued	Lattice Semiconductor Corporation
10/794,498	7028201	United States	Powering up a device having digital and analog circuitry	Issued	Lattice Semiconductor Corporation
10/797,759	7068556	United States	Sense Amplifier Systems and Methods	Issued	Lattice Semiconductor Corporation
10/809,180	7234030	United States	Table based scheduler for FIFOs and the like	Issued	Lattice Semiconductor Corporation
10/809,658	7095247	United States	Configuring FPGAs and the like using one or more serial memory devices	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/815,403	7167032	United States	Self-adjusting schmitt trigger	Issued	Lattice Semiconductor Corporation
10/817,215	7081781	United States	Charge pump for a low-voltage wide-tuning range phase-locked loop	Issued	Lattice Semiconductor Corporation
10/829,865	6998896	United States	Dynamic gain adjustment systems and method for metastability resistance	Issued	Lattice Semiconductor Corporation
10/834,528	6998906	United States	Low pass filter systems and methods	Issued	Lattice Semiconductor Corporation
10/837,086	7307319	United States	High Voltage Protection Device And Process	Issued	Lattice Semiconductor Corporation
10/842,345	7002418	United States	Control Signal Generation ...	Issued	Lattice Semiconductor Corporation
10/841,987	7224213	United States	switched-capacitor ripple-smoothing filter	Issued	Lattice Semiconductor Corporation
10/843,708	7061269	United States	IO buffer architecture for programmable devices	Issued	Lattice Semiconductor Corporation
10/856,100	7196551	United States	Current Mode Logic Buffer	Issued	Lattice Semiconductor Corporation
10/857,667	7064973	United States	Combination FPGA	Issued	Lattice Semiconductor Corporation
10/885,419	7116585	United States	Memory Systems And Methods	Issued	Lattice Semiconductor Corporation
10/910,091	7215591	United States	Byte enable logic for memory	Issued	Lattice Semiconductor Corporation
10/912,943	7471752	United States	Data Transmission Synchronization	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/928,563	7078286	United States	Process for fabricating a semiconductor device having electrically isolated low voltage and high voltage regions	Issued	Lattice Semiconductor Corporation
10/929,199	7484144	United States	Testing embedded memory in an integrated circuit	Issued	Lattice Semiconductor Corporation
10/944,978	7135886	United States	FPGA Using Both Volatile and NonVolatile Memory Cell Properties	Issued	Lattice Semiconductor Corporation
10/974,453	7307912	United States	Variable data width memory systems and methods	Issued	Lattice Semiconductor Corporation
10/973,750	7149129	United States	memory output data systems and methods with feedback	Issued	Lattice Semiconductor Corporation
10/974,107	7164290	United States	FPGA Logic Unit	Issued	Lattice Semiconductor Corporation
10/974,305	7129749	United States	PLD Having A Configurable DRAM With Transparent Refresh	Issued	Lattice Semiconductor Corporation
10/978,899	7376872	United States	Testing embedded memory in integrated circuits such as progammable logic circuits	Issued	Lattice Semiconductor Corporation
10/996,283	7161862	United States	Low power asynchronous sense amp	Issued	Lattice Semiconductor Corporation
11/007,954	7230810	United States	Dynamic over-voltage protection scheme for integrated circuit devices	Issued	Lattice Semiconductor Corporation
11/012,550	7215149	United States	Interface circuitry for electrical systems	Issued	Lattice Semiconductor Corporation
11/012,548	7215148	United States	Programmable current LVDS output buffer	Issued	Lattice Semiconductor Corporation
11/015,265	7177221	United States	Method of initializing configurable multi-port	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			embedded memory blocks in an FPGA		Corporation
11/016,665	7187203	United States	Cascadable memory	Issued	Lattice Semiconductor Corporation
11/015,369	7177207	United States	Sense amplifier timing	Issued	Lattice Semiconductor Corporation
11/036,630	7257750	United States	Self-verification of configuration memory in PLDs	Issued	Lattice Semiconductor Corporation
11/036,738	7242053	United States	EEPROM Device with voltage-limiting charge pump circuit	Issued	Lattice Semiconductor Corporation
11/040,772	7208975	United States	Serdes with programmable I/O architecture	Issued	Lattice Semiconductor Corporation
11/041,319	7183798	United States	Synchronous memory	Issued	Lattice Semiconductor Corporation
11/044,089	7109754	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
11/044,149	7109756	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
11/044,508	7034599	United States	Clock Generator With Skew Control	Issued	Lattice Semiconductor Corporation
11/054,011	7221607	United States	Mult-port memory systems and methods for bit line coupling	Issued	Lattice Semiconductor Corporation
11/055,280	6975137	United States	PLDs With Integrated Standard Cell Logic Blocks	Issued	Lattice Semiconductor Corporation
11/054,750	7382293	United States	Data Decompression	Issued	Lattice Semiconductor Corporation
11/054,855	7589648	United States	Data Decompression	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/064,477	7532646	United States	Distributed multiple channel alignment scheme	Issued	Lattice Semiconductor Corporation
11/071,356	7245154	United States	Differential Input Receiver with Programmable Failsafe	Issued	Lattice Semiconductor Corporation
11/070,926	7057397	United States	Output Impedance Measurement Techniques	Issued	Lattice Semiconductor Corporation
11/083,625	7376204	United States	Detection of Unknown symbol rate in a digitally modulated signal	Issued	Lattice Semiconductor Corporation
11/098,713	7265578	United States	In-System Programming Of a Non-Compliant Device Using Multiple Interfaces Of A PLD	Issued	Lattice Semiconductor Corporation
11/100,718	7397274	United States	In-System Programming Of a Non-Compliant Device Using Multiple Interfaces Of A PLD	Issued	Lattice Semiconductor Corporation
11/108,927	7193436	United States	Fast Processing Path Using FPGA Logic Units	Issued	Lattice Semiconductor Corporation
11/109,301	7630464	United States	Analog-to-digital systems and methods	Issued	Lattice Semiconductor Corporation
11/109,966	6977521	United States	FPGA	Issued	Lattice Semiconductor Corporation
11/121,326	7400171	United States	Electronic Switch Having Extended Voltage Range	Issued	Lattice Semiconductor Corporation
11/134,152	7009423	United States	Programmable I/O Interfaces For FPGAs And Other PLDs	Issued	Lattice Semiconductor Corporation
11/157,345	7685483	United States	Design-For-Test features for a memory in an FPGA	Issued	Lattice Semiconductor Corporation
11/157,349	7378879	United States	Decoding systems and methods	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/165,709	7256613	United States	Programmable Interconnect Architecture for PLDs	Issued	Lattice Semiconductor Corporation
11/165,853	7342838	United States	PLD With A Double Data Rate SDRAM Interface	Issued	Lattice Semiconductor Corporation
11/185,242	7519139	United States	Signal monitoring systems and methods	Issued	Lattice Semiconductor Corporation
11/187,179	7342846	United States	address decoding systems and methods	Issued	Lattice Semiconductor Corporation
11/187,114	7253674	United States	Fine output clock phase alignment circuitry	Issued	Lattice Semiconductor Corporation
11/189,067	7505752	United States	Receiver used for differential signaling and reference voltage signaling with programmable common mode	Issued	Lattice Semiconductor Corporation
11/194,871	7414913	United States	Bitline twisting scheme for a multiport memory	Issued	Lattice Semiconductor Corporation
11/194,356	7262630	United States	Dynamic programmable termination for parallel and differential schemes	Issued	Lattice Semiconductor Corporation
11/199,287	7599457	United States	clock-and-data-recovery system having a multi-phase clock generator for one or more channel circuits	Issued	Lattice Semiconductor Corporation
11/200,983	7295035	United States	Programmable Logic Device With Enhanced Logic Block Architecture	Issued	Lattice Semiconductor Corporation
11/200,941	7411419	United States	I/O Systems and Methods	Issued	Lattice Semiconductor Corporation
11/202,149	7606851	United States	Correlator having user-defined processing	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/201,620	7187586	United States	Flash memory erase verification systems and methods	Issued	Lattice Semiconductor Corporation
11/206,282	RE40311	United States	Zero Power Programmable Memory Cell	Issued	Lattice Semiconductor Corporation
11/226,695	7301182	United States	Circuit layout for improved performance while preserving or improving density	Issued	Lattice Semiconductor Corporation
11/230,087	7167405	United States	Data transfer verification systems and methods	Issued	Lattice Semiconductor Corporation
11/235,616	7376037	United States	PLD with power-saving architecture	Issued	Lattice Semiconductor Corporation
11/236,967	7405446	United States	Electrostatic Protection Systems and Methods	Issued	Lattice Semiconductor Corporation
11/243,255	7088132	United States	Configuring FPGAs and the like using one or more serial memory devices	Issued	Lattice Semiconductor Corporation
11/251,682	7196963	United States	Address isolation for user-defined configuration memory in programmable devices	Issued	Lattice Semiconductor Corporation
11/252,094	7263024	United States	Clock reset address decoder for block memory	Issued	Lattice Semiconductor Corporation
11/252,126	7061275	United States	FPGA	Issued	Lattice Semiconductor Corporation
11/257,137	7685215	United States	Fast-carry arithmetic circuit using a multi-input LUT	Issued	Lattice Semiconductor Corporation
11/257,641	7317343	United States	PULSE-GENERATION CIRCUIT HAVING PULSE GENERATORS AND SET-RESET LATCHES	Issued	Lattice Semiconductor Corporation
11/260,097	7212051	United States	Control signal generation for a low jitter switched-capacitor frequency synthesizer	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/281,651	7495495	United States	Digital I/O Timing Control	Issued	Lattice Semiconductor Corporation
11/287,720	7327159	United States	Interface Block Architectures	Issued	Lattice Semiconductor Corporation
11/290,205	7242634	United States	Pseudo-dynamic word-line driver	Issued	Lattice Semiconductor Corporation
11/293,941	7538574	United States	Transparent Field Reconfiguration for PLDs	Issued	Lattice Semiconductor Corporation
11/302,097	7620839	United States	Jitter Tolerant Delay-Locked Loop Circuit	Issued	Lattice Semiconductor Corporation
11/300,886	7495467	United States	Temperature independent, linear on-chip termination resistance	Issued	Lattice Semiconductor Corporation
11/332,986	7382169	United States	Systems and Methods for Reducing Static Phase Error	Issued	Lattice Semiconductor Corporation
11/335,890	7439783	United States	Phase-Locked Loop Systems And Methods	Issued	Lattice Semiconductor Corporation
11/345,713	7547995	United States	dynamic over voltage protection scheme for interface circuitry	Issued	Lattice Semiconductor Corporation
11/346,817	7554357	United States	Efficient Configuration of Daisy-Chained Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
11/350,436	7375549	United States	Reconfiguration of PLDs	Issued	Lattice Semiconductor Corporation
11/356,805	7277348	United States	Memory Cell Comprising And OTP NV Memory Unit And SRAM Unit	Issued	Lattice Semiconductor Corporation
11/360,337	7355441	United States	PLD with distributed memory and non-volatile memory	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/361,584	7596744	United States	Auto recovery from volatile soft error upsets (SEUs)	Issued	Lattice Semiconductor Corporation
11/362,289	7759926	United States	dynamic phase offset measurement	Issued	Lattice Semiconductor Corporation
11/361,643	7446573	United States	Comparator Systems And Methods	Issued	Lattice Semiconductor Corporation
11/398,437	7459931	United States	PLDs with transparent field reconfiguration	Issued	Lattice Semiconductor Corporation
11/397,985	7554358	United States	PLDs with user non-volatile memory	Issued	Lattice Semiconductor Corporation
11/416,881	7623378	United States	Selective programming of non-volatile memory facilitated by security fuses	Issued	Lattice Semiconductor Corporation
11/435,956	7102934	United States	Sense Amplifier Systems and Methods	Issued	Lattice Semiconductor Corporation
11/442,186	7411417	United States	Selective loading of configuration data into configuration memory cells	Issued	Lattice Semiconductor Corporation
11/446,548	7378873	United States	PLD providing a serial peripheral interface	Issued	Lattice Semiconductor Corporation
11/445,620	7378872	United States	PLD architecture with multiple slice types	Issued	Lattice Semiconductor Corporation
11/446,542	7385417	United States	Dual slice architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/446,351	7397276	United States	Logic block control architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/446,308	7546498	United States	PLDs with custom identification systems and methods	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/446,309	7495970	United States	Flexible memory architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/447,591	7631223	United States	PLD methods and systems for providing multi-boot configuration data support	Issued	Lattice Semiconductor Corporation
11/452,714	7463060	United States	PLD and method of testing	Issued	Lattice Semiconductor Corporation
11/455,315	7215139	United States	Upgradeable And Reconfigurable Programmable Logic Device	Issued	Lattice Semiconductor Corporation
11/425,273	7702100	United States	Key generation for advanced encryption standard (AES) decryption and the like	Issued	Lattice Semiconductor Corporation
11/425,881	7657773	United States	Clock distribution chip for generating both zero-delay and non-zero-delay clock signals	Issued	Lattice Semiconductor Corporation
11/477,759	7348914	United States	Methods and systems to align output signals of an analog-to-digital converter	Issued	Lattice Semiconductor Corporation
11/487,647	7636259	United States	Flash memory array with independently erasable sectors	Issued	Lattice Semiconductor Corporation
11/487,751	7512015	United States	Negative voltage blocking for embedded memories	Issued	Lattice Semiconductor Corporation
11/492,687	7466190	United States	Charge pump with four-well transistors	Issued	Lattice Semiconductor Corporation
11/494,862	7521969	United States	Switch sequencing circuit systems and methods	Issued	Lattice Semiconductor Corporation
11/461,222	7411432	United States	Integrated circuits and complementary CMOS circuits for frequency dividers	Issued	Lattice Semiconductor Corporation
11/498,645	7675313	United States	Methods and systems for storing a security key using programmable fuses	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/498,646	7605606	United States	Area efficient routing architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/530,620	7456672	United States	Clock systems and methods	Issued	Lattice Semiconductor Corporation
11/533,188	7511641	United States	Efficient bitstream compression	Issued	Lattice Semiconductor Corporation
11/551,459	7831754	United States	Multiple Communication Channel Configuration Systems And Methods	Issued	Lattice Semiconductor Corporation
11/556,528	7663401	United States	Multiplexer initialization systems and methods	Issued	Lattice Semiconductor Corporation
11/593,274	7535258	United States	Programmable Voltage LVDS Output Buffer	Issued	Lattice Semiconductor Corporation
11/557,808	7725803	United States	PLD programming verification systems and methods	Issued	Lattice Semiconductor Corporation
11/638,156	7429875	United States	Low Static Current Drain Logic Circuit	Issued	Lattice Semiconductor Corporation
11/643,288	7443192	United States	Output buffer with digital slew control	Issued	Lattice Semiconductor Corporation
11/624,021	7623391	United States	Data transfer verification systems and methods	Issued	Lattice Semiconductor Corporation
11/671,948	7576563	United States	Flexible High Fan-out Signal Routing Systems and Methods	Issued	Lattice Semiconductor Corporation
11/675,246	7313025	United States	Flash memory erase verification systems and methods	Issued	Lattice Semiconductor Corporation
11/676,071	7430706	United States	Fast diagonal interleaved parity (DIP) calculator	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/680,526	7598765	United States	Redundancy for Configuration RAM	Issued	Lattice Semiconductor Corporation
11/691,003	7536615	United States	Logic analyzer systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/691,040	7743296	United States	Logic analyzer systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/737,702	7509598	United States	Clock Boosting Systems and Methods	Issued	Lattice Semiconductor Corporation
11/750,790	7401280	United States	Self-verification of configuration memory in PLDs	Issued	Lattice Semiconductor Corporation
11/750,616	7632011	United States	Integrated Circuit Temperature Sensors Systems and Methods	Issued	Lattice Semiconductor Corporation
11/760,411	8065574	United States	Real Soft Error Detect Scheme for Testing	Issued	Lattice Semiconductor Corporation
11/761,221	7570078	United States	PLD Providing A Serial Peripheral Interfaces	Issued	Lattice Semiconductor Corporation
11/778,457	7573770	United States	Distributed front-end FIFO for source-synchronized interfaces with non-continuous clocks	Issued	Lattice Semiconductor Corporation
11/779,246	7446679	United States	FPGA data compression using combined RLE BE, LZ, Row LZ and BE ROW encoding	Issued	Lattice Semiconductor Corporation
11/863,016	7681160	United States	Weight based look up table collapsing for programmable logic devices	Issued	Lattice Semiconductor Corporation
11/865,556	7539076	United States	Variable data width memory systems and methods	Issued	Lattice Semiconductor Corporation
11/869,019	7616029	United States	Hysteresis-based processing for applications such as signal bias monitors	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/872,950	7586344	United States	Dynamic delay or advance adjustment of oscillating signal phase	Issued	Lattice Semiconductor Corporation
11/875,748	7757198	United States	Scan chain systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/877,434	7411414	United States	Single-Ended Output Driver Buffer	Issued	Lattice Semiconductor Corporation
11/924,088	8132040	United States	Channel-to-channel deskew systems and methods	Issued	Lattice Semiconductor Corporation
11/934,711	7573291	United States	Programmable Logic Device With Enhanced Logic Block Architecture	Issued	Lattice Semiconductor Corporation
11/937,328	7788620	United States	An IO placement systems and methods to reduce SSO noise	Issued	Lattice Semiconductor Corporation
11/937,300	7895555	United States	Simultaneous Switching Output Noise Estimation and Reduction Systems and Methods	Issued	Lattice Semiconductor Corporation
11/939,787	7863931	United States	Flexible Delay Cell Architecture	Issued	Lattice Semiconductor Corporation
11/941,031	7902865	United States	Compression and decompression of configuration data using repeated data frames	Issued	Lattice Semiconductor Corporation
11/941,006	7535253	United States	Method of Retaining Register Data during Field Update of PLD	Issued	Lattice Semiconductor Corporation
11/947,662	7788623	United States	Composite wire indexing for PLDs	Issued	Lattice Semiconductor Corporation
11/949,130	7586325	United States	IC having independent voltage and process/temperature control	Issued	Lattice Semiconductor Corporation
12/001,600	7728625	United States	Serial interface for PLDs	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/957,598	7605609	United States	A programmable level shifter optimized for high performance and low power.	Issued	Lattice Semiconductor Corporation
11/959,329	7630259	United States	PLD with built in self test	Issued	Lattice Semiconductor Corporation
11/970,212	7646643	United States	Process charging monitor for nonvolatile memory	Issued	Lattice Semiconductor Corporation
12/019,526	7787326	United States	PLD With Mult-Rate SDRAM Interface	Issued	Lattice Semiconductor Corporation
12/021,202	8069329	United States	Dynamic Multiple Pattern Configuration Scheme For Volatile FPGAs	Issued	Lattice Semiconductor Corporation
12/044,842	7652500	United States	Reconfiguration of PLDs	Issued	Lattice Semiconductor Corporation
12/055,170	7890913	United States	Wire Mapping For PLDs	Issued	Lattice Semiconductor Corporation
12/060,776	7459935	United States	PLD With Distributed Memory	Issued	Lattice Semiconductor Corporation
12/061,885	7831856	United States	Detection of Timing Errors in Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/099,933	7661878	United States	On-Chip Temperature Sensor For An Integrated Circuit	Issued	Lattice Semiconductor Corporation
12/100,859	7558143	United States	Programmable Logic Device With Power-Saving Architecture	Issued	Lattice Semiconductor Corporation
12/105,146	7557606	United States	Synchronization Of Data Signals And Clock Signals For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/105,959	7696784	United States	PLD With Multiple Slice	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Types		Corporation
12/107,883	7560953	United States	Power Management Systems And Methods for PLDs	Issued	Lattice Semiconductor Corporation
12/122,489	7897448	United States	Formation Of High Voltage Transistor With High Breakdown Voltage	Issued	Lattice Semiconductor Corporation
12/146,042	8463832	United States	Digital Signal Processing Block Architecture For PLD	Issued	Lattice Semiconductor Corporation
12/164,265	7592834	United States	Logic Block Control Architectures For PLDs	Issued	Lattice Semiconductor Corporation
12/182,940	8261160	United States	Serial data recovery out of 8 samples with FPGAs	Issued	Lattice Semiconductor Corporation
12/186,027	7579865	United States	Selective Loading Of Configuration Data Into Configuration Memory Cells	Issued	Lattice Semiconductor Corporation
12/188,120	7605602	United States	Low-Power Output Driver Buffer Circuit	Issued	Lattice Semiconductor Corporation
12/238,959	7911229	United States	Programmable Signal Routing Systems	Issued	Lattice Semiconductor Corporation
12/273,868	7663419	United States	Clock Systems And Methods	Issued	Lattice Semiconductor Corporation
12/277,217	8112731	United States	Congestion-driven placement based on region interconnection for FPGA	Issued	Lattice Semiconductor Corporation
12/323,974	7992120	United States	congestion estimation based on pass probability net estimation process	Issued	Lattice Semiconductor Corporation
12/327,128	7656193	United States	Programmable Logic Device And Method Of Testing	Issued	Lattice Semiconductor Corporation
12/337,502	8856718	United States	Precise Congestion Estimation for FPGA Router	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
12/341,929	8181139	United States	Multi-Priority Placement	Issued	Lattice Semiconductor Corporation
12/370,039	7714608	United States	Temperature-Independent, Linear On-Chip Termination Resistance	Issued	Lattice Semiconductor Corporation
12/389,149	7957208	United States	Flexible memory architectures for PLDs	Issued	Lattice Semiconductor Corporation
12/402,751	7844243	United States	Receiver used for differential signaling and reference voltage signaling with programmable common mode	Issued	Lattice Semiconductor Corporation
12/406,772	8069431	United States	An alternative method for pin swapping in FPGA routing	Issued	Lattice Semiconductor Corporation
12/408,047	8086986	United States	Clock Boosting Systems And Methods	Issued	Lattice Semiconductor Corporation
12/409,757	7675321	United States	Dual-Slice Architectures For PLDs	Issued	Lattice Semiconductor Corporation
12/413,787	7808405	United States	Efficient Bitstream Compression	Issued	Lattice Semiconductor Corporation
12/430,848	7741865	United States	Soft Error Upset Hardened Integrated Circuit Systems And Methods	Issued	Lattice Semiconductor Corporation
12/464,822	7876125	United States	Method of Retaining Register Data during Field Update of PLD	Issued	Lattice Semiconductor Corporation
12/465,444	7868654	United States	Economical way to improve volatile FPGA boot up data throughput by utilizing one or more SPI boot PROMs w/o sacrificing additional FPGA pins	Issued	Lattice Semiconductor Corporation
12/467,800	7737723	United States	Transparent Field Reconfiguration for PLDs	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
12/476,155	8044682	United States	FPGA Having Low Power, Fast Carry Chain	Issued	Lattice Semiconductor Corporation
12/480,565	7702977	United States	PLDs with custom identification systems and methods	Issued	Lattice Semiconductor Corporation
12/494,822	8165164	United States	Circuit For In-System Reconfigurable Mapping Of IQ Data Into A CPRI Basic Frame	Issued	Lattice Semiconductor Corporation
12/502,141	7724029	United States	Power Management For Integrated Circuits Such As Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/511,388	7768300	United States	PLD Providing A Serial Peripheral Interfaces	Issued	Lattice Semiconductor Corporation
12/512,944	8255733	United States	Method of selecting precise delay or skew shifts	Issued	Lattice Semiconductor Corporation
12/512,961	7969248	United States	VCO digital center frequency coarse tune algorithm	Issued	Lattice Semiconductor Corporation
12/538,810	7808855	United States	Distributed front-end FIFO for source-synchronized interfaces with non-continuous clocks	Issued	Lattice Semiconductor Corporation
12/561,140	8010871	United States	Auto recovery from volatile soft error upsets (SEUs)	Issued	Lattice Semiconductor Corporation
12/564,781	7746107	United States	Redundancy for Configuration RAM	Issued	Lattice Semiconductor Corporation
12/578,470	8122277	United States	Clock distribution chip	Issued	Lattice Semiconductor Corporation
12/578,492	8112656	United States	Clock distribution chip	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/607,868	7989911	United States	STI with trench liner of increased thickness	Issued	Lattice Semiconductor Corporation
12/607,333	7985656	United States	STI with trench liner of increased thickness	Issued	Lattice Semiconductor Corporation
12/611,262	8059470	United States	Flash memory array with independently erasable sectors	Issued	Lattice Semiconductor Corporation
12/626,289	7944765	United States	PLD with built in self test	Issued	Lattice Semiconductor Corporation
12/630,163	8060784	United States	PLD And Methods For Providing Multi-Boot Configuration Data Support	Issued	Lattice Semiconductor Corporation
12/637,884	8200179	United States	Combined Variable Gain Amplifier And Linear Equalizer With Independent Gain And Frequency Control	Issued	Lattice Semiconductor Corporation
12/698,283	8040152	United States	IO Ring Configuration Scheme with sharing of BC7 register	Issued	Lattice Semiconductor Corporation
12/706,227	7924054	United States	Latency measurement circuit for wireless communications applications	Issued	Lattice Semiconductor Corporation
12/709,685	7834652	United States	Methods and systems for storing a security key using programmable fuses	Issued	Lattice Semiconductor Corporation
12/729,952	8040159	United States	High Speed Comparator with Data Dependent Jitter Mitigation	Issued	Lattice Semiconductor Corporation
12/752,455	8384427	United States	Serial Peripheral Interface Daisy Chaining using a Flow-Through Option	Issued	Lattice Semiconductor Corporation
12/757,087	8664774	United States	A Method for Arranging IC Bondwires for the Reduction of Crosstalk	Issued	Lattice Semiconductor Corporation
12/786,359	8108754	United States	PLD programming verification systems and methods	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/813,540	8164499	United States	Shared-Array Multiple-Output Digital to Analog Converter	Issued	Lattice Semiconductor Corporation
12/813,573	8441292	United States	Method of delaying data from clock in 1UI steps	Issued	Lattice Semiconductor Corporation
12/818,544	7868646	United States	Soft Error Upset Hardened Integrated Circuit Systems And Methods	Issued	Lattice Semiconductor Corporation
12/871,764	8286116	United States	Composite Wire Indexing For PLDs	Issued	Lattice Semiconductor Corporation
12/977,011	8522126	United States	Method Of Blocking PLC Distributed SRAM Readback In User Mode	Issued	Lattice Semiconductor Corporation
12/976,412	8351287	United States	Bitline Floating Circuit For Power Reduction On SRAM Array	Issued	Lattice Semiconductor Corporation
12/976,520	8477549	United States	Strobed And Latched Readback Of SRAM Bits In A FPGA	Issued	Lattice Semiconductor Corporation
12/987,393	8274412	United States	Low Power SerDes With Built- In Word Alignment For Odd And Even Gearing Ratios	Issued	Lattice Semiconductor Corporation
13/006,622	8384428	United States	Programmable IO Pad - embedded function block	Issued	Lattice Semiconductor Corporation
13/007,804	8248136	United States	Low Power And Glitch-less Delay Element For High Speed Receiver Interface	Issued	Lattice Semiconductor Corporation
13/007,688	8324934	United States	Programmable Ratio Input Buffer	Issued	Lattice Semiconductor Corporation
13/026,555	8104009	United States	Wire Mapping For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
13/034,174	8058898	United States	Compression and Decompression Of Configuration Data Using	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Repeated Data Frames		
13/038,259	8368424	United States	Wakeup from sleep mode using slave I2C port or slave SPI port with powered down core logic	Issued	Lattice Semiconductor Corporation
13/038,270	8816718	United States	Slow Respond Mode Protocol For Synchronous Read	Issued	Lattice Semiconductor Corporation
13/037,703	8654600	United States	Current Sense Amplifier With Low Voltage Operation	Issued	Lattice Semiconductor Corporation
13/052,142	8553463	United States	Positive-To-Negative Voltage Discharge Circuit	Issued	Lattice Semiconductor Corporation
13/076,300	8319521	United States	Safe programming of key information into NV memory	Issued	Lattice Semiconductor Corporation
13/079,578	8314634	United States	Power Saving Standby Mode With Glitch-Less Output Controls	Issued	Lattice Semiconductor Corporation
13/079,595	8531222	United States	PLL Switchable Feedback Loops Among Internal And External Feedback Paths	Issued	Lattice Semiconductor Corporation
13/083,889	8138790	United States	Latency measurement circuit for wireless communications applications	Issued	Lattice Semiconductor Corporation
13/154,885	8441284	United States	Flexible Way To Incrementally Update Multi-Bit Data Registers	Issued	Lattice Semiconductor Corporation
13/155,547	8547075	United States	Filter And Stability Capacitor Reuse For On-Chip Dual Output Voltage Regulators	Issued	Lattice Semiconductor Corporation
13/164,108	8555217	United States	Cross-Probing Technology Between Software Plug-In Modules	Issued	Lattice Semiconductor Corporation
13/178,599	8539409	United States	Multiple silicon products from a common base set of masks	Issued	Lattice Semiconductor Corporation
13/178,536	8495264	United States	Packet And Control Symbol	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Alignment Circuit For SRIO		Corporation
13/193,984	8314632	United States	Placing ICs Into Ultra-Low Voltage Mode For Standby Purposes	Issued	Lattice Semiconductor Corporation
13/212,121	8451679	United States	Bit-Line Clamping Circuit To Improve Write Performance Of Dual-Port SRAM	Issued	Lattice Semiconductor Corporation
13/275,102	8169237	United States	High Speed Comparator with Data Dependent Jitter Mitigation	Issued	Lattice Semiconductor Corporation
13/299,507	8370691	United States	Testing of Soft Error Detection Logic For PLDs	Issued	Lattice Semiconductor Corporation
13/452,060	8823561	United States	In-System Reconfigurable Circuit For Mapping Data Words Of Different Lengths	Issued	Lattice Semiconductor Corporation
13/585,142	8461894	United States	Low Power And Glitch-less Delay Element For High Speed Receiver Interface	Issued	Lattice Semiconductor Corporation
13/616,173	8912933	United States	Low Power SerDes With Built- In Word Alignment For Odd And Even Gearing Ratios	Issued	Lattice Semiconductor Corporation
13/653,827	8710898	United States	Bandgap Reference Circuit Design With Triple-Trim Methodology For Mass Production	Issued	Lattice Semiconductor Corporation
13/680,947	8643398	United States	Placing ICs Into Low Voltage Mode For Standby Purposes	Issued	Lattice Semiconductor Corporation
13/685,385	8643168	United States	Input Capacitance Compensation In Package	Issued	Lattice Semiconductor Corporation
13/721,867	8686773	United States	In-System Margin Measurement Circuit	Issued	Lattice Semiconductor Corporation
13/738,265	8797064	United States	Low power, optimized H-bridge and CML driver	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
13/764,221	RE45200	United States	Programmable Signal Routing Systems Having Low Static Leakage	Issued	Lattice Semiconductor Corporation
13/857,919	8786482	United States	Analog-To-Digital-Converter	Issued	Lattice Semiconductor Corporation
13/892,948	8648636	United States	Method of Delaying Data from Clock in 1UI steps	Issued	Lattice Semiconductor Corporation
14/040,955	8829944	United States	Dynamic Power Supply Switching For Clock Signals	Issued	Lattice Semiconductor Corporation
13/155,261		United States	JTAG Based Parallel Measuring And Trimming for Time Based Parameters	Pending	Lattice Semiconductor Corporation
13/412,408		United States	Double Rate Throughput Processing Booster For DSP Slices	Pending	Lattice Semiconductor Corporation
13/466,463		United States	Early Match FIFO	Pending	Lattice Semiconductor Corporation
13/681,782		United States	Multi-channel transmitter synchronization circuitry	Pending	Lattice Semiconductor Corporation
13/777,243		United States	RAM Data Path Sense Leakage Abatement Circuit	Pending	Lattice Semiconductor Corporation
13/858,422		United States	Method To Enable And Disable Scan Test Mode Reliably Through JTAG Port With Maximum Scan Coverage	Pending	Lattice Semiconductor Corporation
13/868,738		United States	Loss of signal detection in high-speed serial link	Pending	Lattice Semiconductor Corporation
13/901,853		United States	Dual-Port SRAM With Bit Line Clamping	Pending	Lattice Semiconductor Corporation
13/904,861		United States	Bring up sequence for configurable PCIe IP in an	Pending	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			FPGA		Corporation
13/947,553		United States	Method For Hot Swapping Or Hot Plugging With Stable Supply-Side Reference Over Wide Voltage Range	Pending	Lattice Semiconductor Corporation
14/021,513		United States	Phase Locked Loop Circuit With Selectable Feedback Paths	Pending	Lattice Semiconductor Corporation
14/043,920		United States	Robust Serialized State-machine Interface Architecture Optimized for Implementation in Programmable Devices	Pending	Lattice Semiconductor Corporation
14/053,026		United States	ASB SW modeling methodology	Pending	Lattice Semiconductor Corporation
14/070,975		United States	Method to enable system board pin escape for tight ball pitch packages	Pending	Lattice Semiconductor Corporation
14/095,310		United States	A Novel ESD Implementation for 40nm FPGA	Pending	Lattice Semiconductor Corporation
14/136,482		United States	Automatic Quadrant Clock Assignment For Programmable Logic Devices	Pending	Lattice Semiconductor Corporation
14/137,443		United States	Using Critical Groups in FPGA Routing	Pending	Lattice Semiconductor Corporation
14/147,796		United States	A Hot Socket Implementation for General Purpose IO for 40nm FPGA	Pending	Lattice Semiconductor Corporation
14/172,678		United States	All Mosfet Circuit for Generating Accurate Collector Currents	Pending	Lattice Semiconductor Corporation
14/179,651		United States	LOW-VOLTAGE CURRENT SENSE AMPLIFIER	Pending	Lattice Semiconductor Corporation
14/194,484		United States	Logic Element Placement with Repacking Optimization	Pending	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/220,377		United States	DPHY using FPGA differential & single ended I/Os	Pending	Lattice Semiconductor Corporation
14/223,096		United States	DPHY using FPGA differential & single ended I/Os	Pending	Lattice Semiconductor Corporation
14/245,920		United States	Deterministic Dynamic Element Matching for Generating Precise Current Ratios	Pending	Lattice Semiconductor Corporation
14/271,331		United States	Inline Defect To Sort Test Correlation In Semiconductor Manufacturing	Pending	Lattice Semiconductor Corporation
14/271,955		United States	Performance-focused Adaptive Automatic Incremental Flow	Pending	Lattice Semiconductor Corporation
14/283,329		United States	Configuration logic controlled memory BIST (built-in self-test) for back-to-back initialization and readback of embedded block RAMs in FPGAs	Pending	Lattice Semiconductor Corporation
14/308,747		United States	A novel Output Driver drive strength and termination resistor continuously calibrating PVT compensation scheme	Pending	Lattice Semiconductor Corporation
14/313,443		United States	FPGA Hardware debug during post-config power-up and before logic analyzer connect	Pending	Lattice Semiconductor Corporation
14/313,778		United States	IOLOGIC Delay Cell Stealing for Holdtime Correction	Pending	Lattice Semiconductor Corporation
14/316,049		United States	Mapping Constant Multipliers To ICE Devices	Pending	Lattice Semiconductor Corporation
14/319,481		United States	Incrementer Absorption into Multiplier Logic	Pending	Lattice Semiconductor Corporation
14/320,169		United States	Method to Implement Mixed-	Pending	Lattice

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Width Mode Memory in Fixed-Mode Memory Architecture with Masking		Semiconductor Corporation
14/320,074		United States	Two Level Voltage Regulator scheme for SRAM Operation	Pending	Lattice Semiconductor Corporation
14/327,811		United States	Implementing Dual Boot For XO2 and Multiple ASCs	Pending	Lattice Semiconductor Corporation
14/339,164		United States	A unique method to optimize clock to out path	Pending	Lattice Semiconductor Corporation
14/339,229		United States	New method on bus-based clock_to_out timing optimization	Pending	Lattice Semiconductor Corporation
14/482,001		United States	Physically-aware Programmable Multiport Memory BIST with on-the-fly ATE-configurable memory tests	Pending	Lattice Semiconductor Corporation
14/509,564		United States	Dont-care based mux absorption into ice40 carry chain	Pending	Lattice Semiconductor Corporation
14/525,240		United States	Level shifter that eliminates static power dissipation	Pending	Lattice Semiconductor Corporation
14/535,454		United States	Low power and high performance class AB amplifier control common mode in SerDes Transmitter	Pending	Lattice Semiconductor Corporation
14/535,351		United States	ICO metastability prevention during start-up	Pending	Lattice Semiconductor Corporation
14/558,851		United States	Low Power and Flexible TX FFE With Programmable Tap Positions And Coefficients Driver Architecture	Pending	Lattice Semiconductor Corporation
14/576,348		United States	Reconfigurable and Scalable Hardware Management Architecture	Pending	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/576,245		United States	Methodology that allows multiple hardware or hardware-software controllers with different bus interfaces to share a common resource	Pending	Lattice Semiconductor Corporation
14/604,515		United States	Enhancement of FPGA hardware debugger to be used as a design controller/exerciser with user registers	Pending	Lattice Semiconductor Corporation
14/609,181		United States	Algorithm to Optimize Hot Swapping	Pending	Lattice Semiconductor Corporation
14/610,074		United States	Ripple Mode using 3-LUT for Generate	Pending	Lattice Semiconductor Corporation
14/610,127		United States	Combine OFX with LUT output and SUM into a single output to reduce number of signals to routing block	Pending	Lattice Semiconductor Corporation
14/611,069		United States	High speed complementary NMOS LUT logic	Pending	Lattice Semiconductor Corporation
14/611,095		United States	Shared Logic for Multiple Registers with asynchronous initialization with preload	Pending	Lattice Semiconductor Corporation
11/949,454	7,427,874	United States	Interface block architectures	Issued	Lattice Semiconductor Corporation
11/676,196	7,327,160	United States	SERDES with programmable I/O architecture	Issued	Lattice Semiconductor Corporation
6,786,564	6,786,564	United States	Inkjet printer, drive method and drive device for same	Issued	Lattice Semiconductor Corporation
11/839,107	7,856,050	United States	Receiver and transmitter calibration to compensate for frequency dependent I/Q imbalance	Issued	Lattice Semiconductor Corporation
07/679,370	5,255,221	United States	Fully configurable versatile field programmable function	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			element		Corporation
06/551,735	4,642,797	United States	High speed first-in-first-out memory	Issued	Lattice Semiconductor Corporation
08/042,533	5,394,037	United States	Sense amplifiers and sensing methods	Issued	Lattice Semiconductor Corporation
08/115,533	5,404,055	United States	Input routing pool	Issued	Lattice Semiconductor Corporation
08/115,723	5,394,033	United States	Structure and method for implementing hierarchical routing pools in a programmable logic circuit	Issued	Lattice Semiconductor Corporation
08/342,675	5,506,517	United States	Output enable structure and method for a programmable logic device	Issued	Lattice Semiconductor Corporation
07/911,841	5,357,156	United States	Active clamp circuit scheme for CMOS devices	Issued	Lattice Semiconductor Corporation
08/179,887	5,886,378	United States	Single polysilicon layer flash E.sup.2 PROM cell	Issued	Lattice Semiconductor Corporation
07/853,453	5,231,316	United States	Temperature compensated CMOS voltage to current converter	Issued	Lattice Semiconductor Corporation
08/108,363	5,353,246	United States	Programmable semiconductor antifuse structure and method of fabricating	Issued	Lattice Semiconductor Corporation
07/785,442	5,281,906	United States	Tunable voltage reference circuit to provide an output voltage with a predetermined temperature coefficient independent of variation in supply voltage	Issued	Lattice Semiconductor Corporation
07/696,453	5,251,169	United States	Non-volatile erasable and programmable interconnect cell	Issued	Lattice Semiconductor Corporation
07/538,211	5,255,203	United States	Interconnect structure for programmable logic device	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
08/106,263	5,412,260	United States	Multiplexed control pins for in-system programming and boundary scan state machines in a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/033,934	5,418,390	United States	Single polysilicon layer E.sup.2 PROM cell	Issued	Lattice Semiconductor Corporation
07/993,711	5,452,229	United States	Programmable integrated-circuit switch	Issued	Lattice Semiconductor Corporation
07/957,311	5,329,179	United States	Arrangement for parallel programming of in-system programmable IC logical devices	Issued	Lattice Semiconductor Corporation
07/288,945	4,896,296	United States	Programmable logic device configurable input/output cell	Issued	Lattice Semiconductor Corporation
06/882,602	4,887,239	United States	One-time programmable data security system for programmable logic device	Issued	Lattice Semiconductor Corporation
06/871,063	4,766,569	United States	Programmable logic array	Issued	Lattice Semiconductor Corporation
06/862,815	4,879,688	United States	In-system programmable logic device	Issued	Lattice Semiconductor Corporation
06/707,670	4,833,646	United States	Programmable logic device with limited sense currents and noise reduction	Issued	Lattice Semiconductor Corporation
07/236,348	4,852,044	United States	Programmable data security circuit for programmable logic device	Issued	Lattice Semiconductor Corporation
11/400,924	7411424	United States	Programmable logic function generator using non-volatile programmable memory switches	Issued	Lattice Semiconductor Corporation
13/403,146		United States	Surface Mountable Integrated Circuit Packaging Scheme	Pending	SiBEAM, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/242,665		United States	High Speed Integrated Circuit Interface	Pending	SiBEAM, Inc.
14/196,978		United States	Calibration of Single-Ended High-Speed Interfaces	Pending	Silicon Image, Inc.
14/474,005		United States	Inter-Device Conflict Resolution on a Multimedia Link	Pending	Silicon Image, Inc.
61/989,417		United States	Control Target Selection	Pending	Silicon Image, Inc.
61/988,812		United States	Lip Sync Delay Compensation	Pending	Silicon Image, Inc.
61/989,415		United States	Streaming Data and Metadata Synchronization	Pending	Silicon Image, Inc.
61/991,126		United States	Stream Creation with Limited Topology Information	Pending	Silicon Image, Inc.
61/989,411		United States	Topology Discovery	Pending	Silicon Image, Inc.
14/463,146		United States	Radio Frequency Interference Reduction In Multimedia Interfaces	Pending	Silicon Image, Inc.
14/578,266		United States	Control Target Selection	Pending	Silicon Image, Inc.
14/578,257		United States	System for Dynamic Audio Visual Capabilities Exchange	Pending	Silicon Image, Inc.
62/089,767		United States	High-Bandwidth Digital Content Protection over Audio Return Channel	Pending	Silicon Image, Inc.
12/573,492	8482462	United States	MULTI-ANTENNA BEAM-FORMING SYSTEM FOR TRANSMITTING CONSTANT ENVELOPE SIGNALS DECOMPOSED FROM A VARIABLE ENVELOPE SIGNAL	Issued	Silicon Image, Inc.
12/678,463	8207892	United States	TECHNIQUE FOR DETERMINING AN ANGLE OF ARRIVAL IN A COMMUNICATION SYSTEM	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/675,269	8374558	United States	ANTENNA ARRAY WITH FLEXIBLE INTERCONNECT FOR A MOBILE WIRELESS DEVICE	Issued	Silicon Image, Inc.
12/333,134	8213872	United States	TECHNIQUE FOR LOW-POWER OPERATION OF A WIRELESS DEVICE	Issued	Silicon Image, Inc.
12/933,876	8256123	United States	DISPLACEMENT SENSING USING A FLEXIBLE SUBSTRATE	Issued	Silicon Image, Inc.
14/196,993		United States	Calibration of Single-Ended High-Speed Interfaces	Pending	Silicon Image, Inc.
13/988,047		United States	INTEGRATED PHASE-SHIFTING-AND-COMBINING CIRCUITRY TO SUPPORT MULTIPLE ANTENNAS	Pending	Silicon Image, Inc.
14/002,353		United States	TRACKING SYSTEM WITH ORTHOGONAL POLARIZATIONS AND A RETRO-DIRECTIVE ARRAY	Pending	Silicon Image, Inc.
13/726,822		United States	HIGH-ACCURACY DETECTION IN COLLABORATIVE TRACKING SYSTEMS	Pending	Silicon Image, Inc.
13/859,764		United States	ANTENNA SELECTION AND PILOT COMPRESSION IN MIMO SYSTEMS	Pending	Silicon Image, Inc.
62/100,841		United States	I/Q Imbalance Correction for the Combination of Multiple Radio Frequency Frontends	Pending	Silicon Image, Inc.
12/532,107	8571126	United States	MULTI-ANTENNA TRANSMITTER FOR MULTI-TONE SIGNALING	Issued	Silicon Image, Inc.
14/065,420		United States	MULTI-ANTENNA TRANSMITTER FOR MULTI-TONE SIGNALING	Pending	Silicon Image, Inc.
12/679,764	8605823	United States	COMMUNICATION USING	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			CONTINUOUS-PHASE MODULATED SIGNALS		Inc.
14/101,274		United States	COMMUNICATION USING CONTINUOUS-PHASE MODULATED SIGNALS	Pending	Silicon Image, Inc.
12/746,526	8484277	United States	TRANSFORMING SIGNALS USING PASSIVE CIRCUITS	Issued	Silicon Image, Inc.
13/498,884	8610474	United States	SIGNAL DISTRIBUTION NETWORKS AND RELATED MET	Issued	Silicon Image, Inc.
14/089,094		United States	SIGNAL DISTRIBUTION NETWORKS AND RELATED METHODS	Pending	Silicon Image, Inc.
13/519,302		United States	Phase Detection Circuits and Methods	Pending	Silicon Image, Inc.
13/574,586	8795082	United States	DIRECTIONAL BEAM STEERING SYSTEM AND METHOD TO DETECT LOCATION AND MOTION	Issued	Silicon Image, Inc.
14/331,144		United States	DIRECTIONAL BEAM STEERING SYSTEM AND METHOD TO DETECT LOCATION AND MOTION	Pending	Silicon Image, Inc.
13/704,564		United States	Methods and Systems for Near-Field MIMO Communications	Pending	Silicon Image, Inc.
14/235,783		United States	HIGH-ACCURACY AND LOW-POWER TRACKING SYSTEM FOR MOBILE DEVICES	Pending	Silicon Image, Inc.
14/234,623		United States	LOW-COST TRACKING SYSTEM	Pending	Silicon Image, Inc.
14/240,405		United States	CALIBRATING A RETRO-DIRECTIVE ARRAY FOR AN ASYMMETRIC WIRELESS LINK	Pending	Silicon Image, Inc.
14/364,002		United States	COLLABORATIVE CHANNEL SOUNDING IN MULTI-ANTENNA	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			SYSTEMS		
08/815,486	6,157,360	United States	System And Method For Driving Columns Of An Active Matrix Display	Issued	Silicon Image, Inc.
08/920,336	5,955,929	United States	Voltage-Controlled Oscillator Resistant To Supply Voltage Noise	Issued	Silicon Image, Inc.
09/007,707	5,969,552	United States	Dual Loop Delay-Locked Loop	Issued	Silicon Image, Inc.
09/298,647	6,259,427	United States	Scaling Multi-Dimensional Signals Using Variable Weighting Factors	Issued	Silicon Image, Inc.
09/298,369	6,374,361	United States	Skew-Insensitive Low Voltage Differential Receiver	Issued	Silicon Image, Inc.
09/393,849	6,738,417	United States	Method And Apparatus For Bidirectional Data Transfer Between A Digital Display And A Computer	Issued	Silicon Image, Inc.
09/326,503	6,940,496	United States	Display Module Driving System And Digital To Analog Converter For Driving Display	Issued	Silicon Image, Inc.
09/392,229	6,564,269	United States	Bi-Directional Data Transfer Using The Video Blanking Period In A Digital Data Stream	Issued	Silicon Image, Inc.
09/393,234	6,307,543	United States	Bi-Directional Data Transfer Using Two Pair Of Differential Lines As A Single Additional Differential Pair	Issued	Silicon Image, Inc.
09/947,008	6,492,984	United States	Bi-Directional Data Transfer Using Two Pair Of Differential Lines As A Single Additional Differential Pair	Issued	Silicon Image, Inc.
09/759,624	6,891,910	United States	Baud-Rate Timing Recovery	Issued	Silicon Image, Inc.
09/574,571	6,326,826	United States	Wide Frequency-Range Delay- Locked Loop Circuit	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/881,271	6,954,491	United States	Methods And Systems For Sending Side-Channel Data During Data Inactive Period	Issued	Silicon Image, Inc.
09/922,990	6,961,095	United States	Digital Display Jitter Correction Apparatus And Method	Issued	Silicon Image, Inc.
11/219,323	7,557,863	United States	Digital Display Jitter Correction Apparatus And Method	Issued	Silicon Image, Inc.
09/989,587	6,717,478	United States	Multi-Phase Voltage Controlled Oscillator (VCO) With Common Mode Control	Issued	Silicon Image, Inc.
10/371,220	7,231,009	United States	Data Synchronization Across An Asynchronous Boundary Using, For Example, Multi-Phase Clocks	Issued	Silicon Image, Inc.
09/989,580	7,103,013	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
11/441,669	7,599,316	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
12/573,847	8,116,240	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
10/045,297	7,257,129	United States	Memory Architecture With Multiple Serial Communications Ports	Issued	Silicon Image, Inc.
11/828,286	7,903,684	United States	Communications Architecture For Transmission Of Data Between Memory Bank Caches And Ports	Issued	Silicon Image, Inc.
09/167,527	6,380,978	United States	Digital Video System And Methods For Providing Same	Issued	DVDO, INC. and Silicon Image, Inc.
10/032,136	7,215,376	United States	Digital Video System And Methods For Providing Same	Issued	DVDO, INC. and Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/942,740	7,359,624	United States	Portable DVD Player	Issued	Silicon Image, Inc.
09/372,713	6,489,998	United States	Method And Apparatus For Deinterlacing Digital Video	Issued	Silicon Image, Inc.
09/941,949	6,909,469	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
10/251,642	7,027,099	United States	Method And Apparatus For Deinterlacing Digital Video Images	Issued	Silicon Image, Inc.
11/054,748	7,391,481	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
11/357,364	7,499,103	United States	Method And Apparatus For Detecting Frequency In Digital Video Images	Issued	Silicon Image, Inc.
11/932,808	7,633,559	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
09/410,543	6,700,622	United States	Method And Apparatus For Detecting The Source Format Of Video Images	Issued	Silicon Image, Inc.
09/396,993	6,515,706	United States	Method And Apparatus For Detecting And Smoothing Diagonal Features In Video Images	Issued	Silicon Image, Inc.
10/191,764	6,829,013	United States	Method And Apparatus For Detecting And Smoothing Diagonal Features In Video Images	Issued	Silicon Image, Inc.
09/363,312	6,681,059	United States	Method And Apparatus For Efficient Video Scaling	Issued	Silicon Image, Inc.
09/359,530	6,587,158	United States	Method And Apparatus For Reducing On-Chip Memory In Vertical Video Processing	Issued	Silicon Image, Inc.
09/226,776	6,219,747	United States	Methods And Apparatus For Variable Length SDRAM	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Transfers		
09/805,588	6,385,692	United States	Methods and Apparatus for Variable Length SDRAM Transfers	Issued	Silicon Image, Inc.
09/227,502	6,393,505	United States	Methods And Apparatus For Data Bus Arbitration	Issued	Silicon Image, Inc.
09/226,381	6,473,476	United States	Method And Apparatus For Providing Deterministic Resets For Clock Divider Systems	Issued	Silicon Image, Inc.
09/837,894	6,867,814	United States	Method, System And Article Of Manufacture For Identifying The Source Type And Quality Level Of A Video Sequence	Issued	Silicon Image, Inc.
09/478,122	7,203,557	United States	Audio Signal Delay Apparatus And Method	Issued	Silicon Image, Inc.
10/663,413	7,408,992	United States	Detection And Repair Of MPEG-2 Chroma Upconversion Artifacts	Issued	Silicon Image, Inc.
09/905,318	7,123,307	United States	Clock Jitter Limiting Scheme In Video Transmission Through Multiple Stages	Issued	Silicon Image, Inc.
09/905,615	6,944,804	United States	System And Method For Measuring Pseudo Pixel Error Rate	Issued	Silicon Image, Inc.
09/904,783	6,625,560	United States	Method Of Testing Serial Interface	Issued	Silicon Image, Inc.
09/989,590	6,845,461	United States	High-Speed Bus With Embedded Clock Signals	Issued	Silicon Image, Inc.
09/989,645	6,809,567	United States	System And Method For Multiple-Phase Clock Generation	Issued	Silicon Image, Inc.
09/905,511	7,062,004	United States	Method And Apparatus For Adaptive Control Of PLL Loop Bandwidth	Issued	Silicon Image, Inc.
10/057,823	7,023,487	United States	Deinterlacing Of Video Sources Via Image Feature Edge Detection	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/954,663	7,558,326	United States	Method And Apparatus For Sending Auxiliary Data On A TMDS-Like Link	Issued	Silicon Image, Inc.
10/036,234	7,359,437	United States	Encoding Method And System For Reducing Inter-Symbol Interference Effects In Transmission Over A Serial Link	Issued	Silicon Image, Inc.
10/095,422	7,257,163	United States	Method And System For Reducing Inter-Symbol Interference Effects In Transmission Over A Serial Link With Mapping Of Each Word In A Cluster Of Received Words To A Single Transmitted Word	Issued	Silicon Image, Inc.
10/171,860	7,088,398	United States	Method And Apparatus For Regenerating A Clock For Auxiliary Data Transmitted Over A Serial Link With Video Data	Issued	Silicon Image, Inc.
10/192,296	6,914,637	United States	Method And System For Video And Auxiliary Data Transmission Over A Serial Link	Issued	Silicon Image, Inc.
10/357,750	7,283,566	United States	Method And Circuit For Generating Time Stamp Data From An Embedded-Clock Audio Data Stream And A Video Clock	Issued	Silicon Image, Inc.
10/016,247	6,714,206	United States	Method And System For Spatial-Temporal Dithering For Displays With Overlapping Pixels	Issued	Silicon Image, Inc.
10/133,813	7,136,484	United States	Cryptosystems Using Commuting Pairs In A Monoid	Issued	Silicon Image, Inc.
10/047,772	7,109,958	United States	Supporting Circuitry And Method For Controlling Pixels	Issued	Silicon Image, Inc.
10/045,393	7,039,121	United States	Method And System For Transition-Controlled Selective Block Inversion	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Communications		
08/656,032	6,018,456	United States	Enclosure For Removable Computer Peripheral Equipment	Issued	CMD Technology Inc. and Silicon Image, Inc.
08/906,775	5,991,546	United States	System And Method For Interfacing Manually Controllable Input Devices To A Universal Computer Bus System	Issued	CMD Technology Inc. and Silicon Image, Inc.
10/171,820	7,225,282	United States	Method And Apparatus For A Two-Wire Serial Command Bus Interface	Issued	Silicon Image, Inc.
11/713,241	7,441,065	United States	Adaptive Beam-Steering Methods To Maximize Wireless Link Budget And Reduce Delay-Spread Using Multiple Transmit And Receive Antennas	Issued	Silicon Image, Inc.
10/210,839	7,171,525	United States	Method And System For Arbitrating Priority Bids Sent Over Serial Links To A Multi-Port Storage Device	Issued	Silicon Image, Inc.
09/688,536	6,380,783	United States	Cyclic Phase Signal Generation From A Single Clock Source Using Current Phase Interpolation	Issued	Silicon Image, Inc.
09/847,837	6,535,029	United States	Fully Differential Continuous-Time Current-Mode High Speed CMOS Comparator	Issued	Silicon Image, Inc.
10/270,882	7,009,827	United States	Voltage Swing Detection Circuit For Hot Plug Event Or Device Detection Via A Differential Link	Issued	Silicon Image, Inc.
10/162,046	6,843,674	United States	Method And Apparatus For Connecting Serial ATA Storage Components	Issued	Silicon Image, Inc.
09/945,278	7,131,004	United States	Method And Apparatus For Encrypting Data Transmitted Over A Serial Link	Issued	Silicon Image, Inc.
11/499,124	7,900,047	United States	Method And Apparatus For Encrypting Data Transmitted	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Over A Serial Link		Inc.
11/543,501	7,757,085	United States	Method And Apparatus For Encrypting Data Transmitted Over A Serial Link	Issued	Silicon Image, Inc.
10/224,995	7,218,737	United States	System And Method For An Adaptive State Machine To Control Signal Filtering In A Serial Link	Issued	Silicon Image, Inc.
09/991,057	7,242,766	United States	Method And System For Encrypting And Decrypting Data Using An External Agent	Issued	Silicon Image, Inc.
10/085,177	7,035,290	United States	Method And System For Temporary Interruption Of Video Data Transmission	Issued	Silicon Image, Inc.
10/036,794	6,976,201	United States	Method And System For Host Handling Of Communications Errors	Issued	Silicon Image, Inc.
10/053,461	7,113,507	United States	Method And System For Communicating Control Information Via Out-Of-Band Symbols	Issued	Silicon Image, Inc.
10/045,625	7,746,798	United States	Method And System For Integrating Packet Type Information With Synchronization Symbols	Issued	Silicon Image, Inc.
10/035,911	7,154,905	United States	Method And System For Nesting Of Communications Packets	Issued	Silicon Image, Inc.
10/045,600	6,771,192	United States	Method And System For DC-Balancing At The Physical Layer	Issued	Silicon Image, Inc.
10/045,601	7,340,558	United States	Multisection Memory Bank System	Issued	Silicon Image, Inc.
09/989,647	7,058,121	United States	Logic Gates Including Diode-Connected Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) To Control Input Threshold Voltage Levels And Switching Transients Of	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Output Logic Signals		
09/989,487	6,985,005	United States	Differential Amplifiers Using Asymmetric Transfer Characteristics To Suppress Input Noise In Output Logic Signals	Issued	Silicon Image, Inc.
11/330,047	7,456,648	United States	Differential Amplifiers Using Asymmetric Transfer Characteristics To Suppress Input Noise In Output Logic Signals	Issued	Silicon Image, Inc.
12/275,686	7,847,583	United States	Transmitter And Receiver Using Asymmetric Transfer Characteristics In Differential Amplifiers To Suppress Noise	Issued	Silicon Image, Inc.
10/403,477	6,819,166	United States	Continuous-Time, Low-Frequency-Gain/High-Frequency-Boosting	Issued	Silicon Image, Inc.
10/417,712	7,348,991	United States	Video Graphics Text Mode Enhancement Method For Digitally Processed Data	Issued	Silicon Image, Inc.
10/287,976	6,873,341	United States	Detection Of Video Windows And Graphics Windows	Issued	Silicon Image, Inc.
10/298,722	7,539,304	United States	Integrated Circuit Having Self Test Capability Using Message Digest And Method For Testing Integrated Circuit Having Message Digest Generation Circuitry	Issued	Silicon Image, Inc.
10/215,936	6,717,468	United States	Dynamically Biased Full-Swing Operation Amplifier For An Active Matrix Liquid Crystal Display Driver	Issued	Silicon Image, Inc.
10/268,832	7,412,053	United States	Cryptographic Device With Stored Key Data And Method For Using Stored Key Data To Perform An Authentication Exchange Of Self Test	Issued	Silicon Image, Inc.
11/950,088	7,797,536	United States	Cryptographic Device With Stored Key Data And Method	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			For Using Stored Key Data To Perform An Authentication Exchange Of Self Test		
10/244,152	6,814,583	United States	Through-Broad PCB Edge Connector, System And Method	Issued	Silicon Image, Inc.
10/247,675	8,064,508	United States	Equalizer With Controllably Weighted Parallel High Pass And Low Pass Filters And Receiver Including Such An Equalizer	Issued	Silicon Image, Inc.
11/796,175	8,275,026	United States	Equalizer With Controllably Weighted Parallel High Pass And Low Pass Filters And Receiver Including Such An Equalizer	Issued	Silicon Image, Inc.
10/651,500	7,551,909	United States	CMOS Transceiver With Dual Current Path VCO	Issued	Silicon Image, Inc.
10/099,533	7,158,593	United States	Combining A Clock Signal And A Data Signal	Issued	Silicon Image, Inc.
10/642,259	7,409,031	United States	Data Sampling Method And Apparatus With Alternating Edge Sampling Phase Detection For Loop Characteristic Stabilization	Issued	Silicon Image, Inc.
10/459,989	7,187,307	United States	Method And System For Encapsulation Of Multiple Levels Of Communication Protocol Functionality Within Line Codes	Issued	Silicon Image, Inc.
10/794,015	7,502,411	United States	Method And Circuit For Adaptive Equalization Of Multiple Signals In Response To A Control Signal Generated From One Of The Equalized Signals	Issued	Silicon Image, Inc.
10/459,992	6,747,580	United States	Method And Apparatus For Encoding Or Decoding Data In Accordance With An Nb/(N+1)B Block Code, And Method For Determining Such A Block Code	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/781,405	7,269,673	United States	Cable With Circuitry For Asserting Stored Cable Data Or Other Information To An External Device Or User	Issued	Silicon Image, Inc.
11/848,758	7,500,032	United States	Cable With Circuitry For Asserting Stored Cable Data Or Other Information To An External Device Or User	Issued	Silicon Image, Inc.
11/123,353	7,375,960	United States	Apparatus For Removably Securing Storage Components In An Enclosure	Issued	Silicon Image, Inc.
10/763,905	7,236,553	United States	Reduced Dead-Cycle, Adaptive Phase Tracking Method And Apparatus	Issued	Silicon Image, Inc.
10/835,301	6,897,793	United States	Method And Apparatus For Run Length Limited TMDS-Like Encoding Of Data	Issued	Silicon Image, Inc.
10/842,231	7,991,096	United States	Data Sampling Method And Apparatus Using Through-Transition Counts To Reject Worst Sampling Position	Issued	Silicon Image, Inc.
10/439,446	7,031,858	United States	Method And Circuit For DC Measurement Of Phase Uniformity Of Multi-Phase Clocks	Issued	Silicon Image, Inc.
10/302,436	7,274,690	United States	An Age Selection Switching Scheme For Data Traffic In A Crossbar Switch	Issued	Silicon Image, Inc.
10/645,786	7,505,422	United States	Preference Programmable First-One Detector And Quadrature Based Random Grant Generator	Issued	Silicon Image, Inc.
10/645,787	7,461,167	United States	A Method For Multicast Service In A Crossbar Switch	Issued	Silicon Image, Inc.
10/762,950	7,352,764	United States	Content Addressable Merged Queue Architecture For Switching Data	Issued	Silicon Image, Inc.
10/434,785	7,519,066	United States	A Method For Switching Data In A Crossbar Switch	Issued	Silicon Image, Inc.
11/372,866	7,694,204	United States	Error Detection In Physical	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Interfaces For Point-To-Point Communications Between Integrated Circuits		Inc.
12/712,124	7,937,644	United States	Error Detection In Physical Interfaces For Point-To-Point Communications Between Integrated Circuits	Issued	Silicon Image, Inc.
13/099,254	8,099,648	United States	Error Detection In Physical Interfaces For Point-To-Point Communications Between Integrated Circuits	Issued	Silicon Image, Inc.
11/669,416	7,844,762	United States	Parallel Interface Bus To Communicate Video Data Encoded For Serial Data Links	Issued	Silicon Image, Inc.
11/056,995	7,102,446	United States	Phase Lock Loop With Coarse Control Loop Having Frequency Lock Detector And Device Including Same	Issued	Silicon Image, Inc.
11/643,388	7,589,559	United States	Current Mode Circuitry To Modulate A Common Mode Voltage	Issued	Silicon Image, Inc.
12/555,300	7,872,498	United States	Current Mode Circuitry to Modulate a Common Mode Voltage	Issued	Silicon Image, Inc.
11/477,049	7,793,179	United States	Test Clock Control Structures To Generate Configurable Test Clocks For Scan-Based Testing Of Electronic Circuits Using Programmable Test Clock Controllers	Issued	Silicon Image, Inc.
11/856,640	7,782,934	United States	Parameter Scanning For Signal Over-Sampling	Issued	Silicon Image, Inc.
11/592,792	7,450,038	United States	Determining Oversampled Data To Be Included In Unit Intervals	Issued	Silicon Image, Inc.
11/510,254	8,595,434	United States	Smart Scalable Storage Switch Architecture	Issued	Silicon Image, Inc.
14/067,363		United States	Smart Scalable Storage Switch Architecture	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/314,162	7,571,269	United States	A Covert Channel For Conveying Supplemental Messages In A Protocol-Defined Link For A System Of Storage Devices	Issued	Silicon Image, Inc.
11/637,254	7,602,253	United States	Adaptive Bandwidth Phase Locked Loop With Feedforward Divider	Issued	Silicon Image, Inc.
11/656,331	7,984,369	United States	Concurrent Code Checker And Hardware Efficient High-Speed I/O Having Built-In Self-Test And Debug Features	Issued	Silicon Image, Inc.
11/694,819	7,949,863	United States	Multi-Port Memory Device Having Variable Port Speeds	Issued	Silicon Image, Inc.
11/694,813	7,639,561	United States	Power-Saving Clocking Technique	Issued	Silicon Image, Inc.
11/690,629	7,831,778	United States	Mechanism For Streaming Media Data Over Wideband Wireless Networks	Issued	Silicon Image, Inc.
11/476,457	7,840,861	United States	Scan-Based Testing Of Devices Implementing A Test Clock Control Structure (â€œTCCSâ€)	Issued	Silicon Image, Inc.
11/861,175	8,160,192	United States	Signal Interleaving for Serial Clock and Data Recovery	Issued	Silicon Image, Inc.
11/690,642	7,908,501	United States	Shared Nonvolatile Memory Architecture	Issued	Silicon Image, Inc.
11/742,358	7,698,088	United States	Interface Test Circuitry And Methods	Issued	Silicon Image, Inc.
11/848,641	8,233,432	United States	Ensuring Physical Locality Of Entities Sharing Data	Issued	Silicon Image, Inc.
11/683,608	7,831,877	United States	Method And Apparatus For A Two-Wire Serial Command Bus Interface	Issued	Silicon Image, Inc.
11/690,659	7,849,339	United States	Progressive Power Control Of A Multi-Port Memory Device	Issued	Silicon Image, Inc.
11/567,514	7,365,659	United States	Method Of Context Adaptive Binary Arithmetic Coding	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			And Coding Apparatus Using The Same		
12/778,882		United States	Multi-Level Port Expansion For Port Multipliers	Pending	Silicon Image, Inc.
12/147,248	7,836,223	United States	Operation Of Media Interface To Provide Bidirectional Communications	Issued	Silicon Image, Inc.
11/849,163	8,695,034	United States	Delivering On Screen Display Data To Existing Display Devices	Issued	Silicon Image, Inc.
11/828,219	8,599,315	United States	On Screen Displays Associated With Remote Video Source Devices	Issued	Silicon Image, Inc.
14/070,373		United States	On Screen Displays Associated With Remote Video Source Devices	Pending	Silicon Image, Inc.
11/829,800	7,903,550	United States	Bandwidth Reservation For Data Flows In Interconnection Networks	Issued	Silicon Image, Inc.
11/828,223	8,149,711	United States	Data Stream Control For Network Devices	Issued	Silicon Image, Inc.
13/541,390	8,924,509	United States	Automated Service Discovery And Dynamic Connection Management	Issued	Silicon Image, Inc.
11/836,082	8,468,212	United States	Network Repository For Metadata	Issued	Silicon Image, Inc.
13/919,773		United States	Network Repository For Metadata	Pending	Silicon Image, Inc.
11/829,790	7,911,956	United States	Packet Level Prioritization In Interconnection Networks	Issued	Silicon Image, Inc.
11/828,226		United States	Streaming Data Content In A Network	Pending	Silicon Image, Inc.
11/848,153	7,936,790	United States	Synchronizing Related Data Streams In Interconnection Networks	Issued	Silicon Image, Inc.
11/952,052	8,001,334	United States	Bank Sharing And Refresh In A Shared Multi-Port Memory Device	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/075,954	7,979,589	United States	Method, Apparatus, And System For Port Multiplier Enhancement	Issued	Silicon Image, Inc.
13/298,001		United States	Iddq Testing Of CMOS Devices	Pending	Silicon Image, Inc.
10/788,704	6,944,086	United States	Semiconductor Memory Device	Issued	Silicon Image, Inc.
10/876,231	7,016,255	United States	Multi-Port Memory Device	Issued	Silicon Image, Inc.
10/877,318	7,089,465	United States	Multi-Port Memory Device Having Serial I/O Interface	Issued	Silicon Image, Inc.
12/075,906	7,904,566	United States	Method, Apparatus, And System For Employing An Enhanced Port Multiplier	Issued	Silicon Image, Inc.
12/497,391	8,386,867	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
13/776,508	8,667,354	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
14/145,751	8,924,805	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
12/197,020	8,086,886	United States	Group Power Management Of Network Devices	Issued	Silicon Image, Inc.
12/683,365	8,543,873	United States	Multi-Site Testing Of Computer Memory Devices And Serial I/O Ports	Issued	Silicon Image, Inc.
14/035,795	8,839,058	United States	Multi-Site Testing Of Computer Memory Devices And Serial I/O Ports	Issued	Silicon Image, Inc.
11/969,847	8,090,030	United States	Method, Apparatus And System For Generating And Facilitating Mobile High-Definition Multimedia Interface	Issued	Silicon Image, Inc.
11/969,852	7,856,520	United States	Control Bus For Connection Of Electronic Devices	Issued	Silicon Image, Inc.
11/969,865	7,921,231	United States	Discovery Of Electronic Devices Utilizing A Control	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Bus		
12/172,187	8,238,653	United States	Methods And Mechanisms For Probabilistic Color Correction	Issued	Silicon Image, Inc.
12/392,000		United States	Method, Apparatus, And System For Pre-Authentication And Processing Of Data Streams	Pending	Silicon Image, Inc.
12/391,987	8,644,504	United States	Method, Apparatus, And System For Deciphering Media Content Stream	Issued	Silicon Image, Inc.
12/605,134	8,407,427	United States	Method And System For Improving Serial Port Memory Communication Latency And Reliability	Issued	Silicon Image, Inc.
13/850,147	8,892,825	United States	Method and System for Improving Serial Port Memory Communication Latency and Reliability	Issued	Silicon Image, Inc.
12/260,970	8,036,248	United States	Method, Apparatus, And System For Automatic Data Aligner For Multiple Serial Receivers	Issued	Silicon Image, Inc.
12/359,025	8,026,726	United States	Fault Testing For Interconnections	Issued	Silicon Image, Inc.
12/486,969	8,793,723	United States	Detection Of Encryption Utilizing Error Detection For Received Data	Issued	Silicon Image, Inc.
12/570,874	8,644,334	United States	Messaging To Provide Data Link Integrity	Issued	Silicon Image, Inc.
12/260,972	7,777,652	United States	Coding System For Memory Systems Employing High-Speed Serial Links	Issued	Silicon Image, Inc.
12/847,416	7,978,099	United States	17b/20b Coding System	Issued	Silicon Image, Inc.
12/351,698	8,374,346	United States	Method, Apparatus, And System For Pre-Authentication And Keep-Authentication Of Content Protected Ports	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/316,305	8,347,081	United States	Method, Apparatus And System For Employing A Content Protection System	Issued	Silicon Image, Inc.
12/577,707	8,275,914	United States	Method And System For Transmitting Or Receiving N-Bit Video Data Over A Serial Link	Issued	Silicon Image, Inc.
12/606,096	8,176,214	United States	Transmission Of Alternative Content Over Standard Device Connectors	Issued	Silicon Image, Inc.
12/351,712	8,185,739	United States	Method And System For Detecting Successful Authentication Of Multiple Ports In A Time Based Roving Architecture	Issued	Silicon Image, Inc.
12/512,877	8,458,343	United States	Signaling For Transitions Between Modes Of Data Transmission	Issued	Silicon Image, Inc.
12/983,233	8,489,784	United States	Adaptive Interconnection Scheme For Multimedia Devices	Issued	Silicon Image, Inc.
13/004,359	8,755,431	United States	Transmission And Detection Of Multi-Channel Signals In Reduced Channel Format	Issued	Silicon Image, Inc.
12/650,357		United States	Method, Apparatus, And System For Simultaneously Previewing Contents From Multiple Protected Sources	Pending	Silicon Image, Inc.
12/712,933	8,692,937	United States	Video Frame Synchronization	Issued	Silicon Image, Inc.
12/966,194		United States	Transmission And Handling Of Three-Dimensional Video Content	Pending	Silicon Image, Inc.
12/873,124	8,325,757	United States	De-Encapsulation Of Data Streams Into Multiple Links	Issued	Silicon Image, Inc.
12/704,417	8,510,487	United States	Hybrid Interface For Serial And Parallel Communication	Issued	Silicon Image, Inc.
13/934,147	8,751,709	United States	Hybrid Interface For Serial And Parallel Communication	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/842,165	8,930,692	United States	Mechanism For Internal Processing Of Content Through Partial Authentication On Secondary Channel	Issued	Silicon Image, Inc.
12/842,190		United States	Mechanism For Partial Encryption Of Data Streams	Pending	Silicon Image, Inc.
13/021,958		United States	Determination Of Physical Connectivity Status Of Devices Based On Electrical Measurement	Allowed	Silicon Image, Inc.
12/898,528	8,598,898	United States	Testing Of High-Speed Input-Output Devices	Issued	Silicon Image, Inc.
13/434,273		United States	Method, Apparatus And System For Transitioning An Audio/Video Device Between A Source Mode And A Sink Mode	Pending	Silicon Image, Inc.
12/848,037	8,624,960	United States	Multi-View Display System	Issued	Silicon Image, Inc.
14/094,668		United States	Multi-View Display System	Pending	Silicon Image, Inc.
12/816,437	8,698,958	United States	Mechanism For Memory Reduction In Picture-In-Picture Video Generation	Issued	Silicon Image, Inc.
13/753,408		United States	Communication Bridging Between Devices Via Multiple Bridge Elements	Pending	Silicon Image, Inc.
13/198,584		United States	Conversion Of Multimedia Data Streams For Use By Connected Devices	Pending	Silicon Image, Inc.
12/906,939	8,537,201	United States	Combining Video Data Streams Of Differing Dimensionality For Concurrent Display	Issued	Silicon Image, Inc.
13/172,745	8,484,387	United States	Detection Of Cable Connections For Electronic Devices	Issued	Silicon Image, Inc.
13/172,742	8,601,173	United States	Detection Of Cable Connections For Electronic	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Devices		
13/362,930		United States	Mechanism For Low Power Standby Mode Control Circuit	Allowed	Silicon Image, Inc.
13/217,138	8,379,145	United States	Conversion And Processing Of Deep Color Video In A Single Clock Domain	Issued	Silicon Image, Inc.
12/979,995	8,874,820	United States	Mechanism For Facilitating A Configurable Port-Type Peripheral Component Interconnect Express/Serial Advanced Technology Attachment Host Controller Architecture	Issued	Silicon Image, Inc.
12/950,850	8,504,672	United States	Discovery Of Electronic Devices In A Combined Network	Issued	Silicon Image, Inc.
13/959,592	8,799,443	United States	Discovery of Electronic Devices in a Combined Network	Issued	Silicon Image, Inc.
13/348,378		United States	Proxy Device Operation In Command And Control Network	Pending	Silicon Image, Inc.
12/950,867		United States	Transfer Of Control Bus Signaling On Packet-Switched Network	Pending	Silicon Image, Inc.
13/339,339		United States	Mechanism For Recovering Clock For Streaming Content Over A Packetized Network	Pending	Silicon Image, Inc.
13/302,452		United States	Multimedia I/O System Architecture for Advanced Digital Television	Pending	Silicon Image, Inc.
13/107,031		United States	Audio And Video Data Multiplexing For Multimedia Stream Switch	Pending	Silicon Image, Inc.
13/174,630		United States	Single-Ended Configurable Multi-Mode Driver	Pending	Silicon Image, Inc.
13/173,302		United States	Fine-Grained Self Refresh Control For DRAM Devices	Pending	Silicon Image, Inc.
13/174,616	8,760,188	United States	Configurable Multi-Dimensional Driver And	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Receiver		Inc.
13/083,399	8,611,486	United States	Adjustment Of Clock Signals Regenerated From A Data Stream	Issued	Silicon Image, Inc.
11/437,357	7,982,798	United States	Edge Detection	Issued	Silicon Image, Inc.
13/153,230	8,446,525	United States	Edge Detection	Issued	Silicon Image, Inc.
10/753,909	7,400,359	United States	Video Stream Routing And Format Conversion Unit With Audio Delay	Issued	Silicon Image, Inc.
10/889,855	7,710,501	United States	Time Base Correction And Frame Rate Conversion	Issued	Silicon Image, Inc.
11/487,144	8,004,606	United States	Original Scan Line Detection	Issued	Silicon Image, Inc.
11/941,050	8,086,067	United States	Noise Cancellation	Issued	Silicon Image, Inc.
11/512,754	8,120,703	United States	Source-Adaptive Video Deinterlacer	Issued	Silicon Image, Inc.
12/204,760	8,559,746	United States	System, Method And Apparatus For Smoothing Of Edges In Images To Remove Irregularities	Issued	Silicon Image, Inc.
14/054,575		United States	System, Method and Apparatus for Smoothing of Edges in Images to Remove Irregularities	Pending	Silicon Image, Inc.
12/703,623	8,452,117	United States	Block Noise Detection And Filtering	Issued	Silicon Image, Inc.
13/899,222	8,891,897	United States	Block Noise Detection And Filtering	Issued	Silicon Image, Inc.
13/335,398		United States	Ringing Suppression In Video Scalers	Pending	Silicon Image, Inc.
13/546,904		United States	Transmission Of Multiple Protocol Data Elements Via An Interface Utilizing A Data Tunnel	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/202,995	7,904,117	United States	Wireless Communication Device Using Adaptive Beamforming	Issued	SiBEAM, Inc.
11/706,711	7,710,319	United States	HD Physical Layer Of A Wireless Communication Device	Issued	SiBEAM, Inc.
12/748,276	7,982,669	United States	Adaptive Beam-Steering Methods To Maximize Wireless Link Budget And Reduce Delay-Spread Using Multiple Transmit And Receive Antennas	Issued	SiBEAM, Inc.
11/706,470	8,014,416	United States	Inter-Port Communication In A Multi-Port Memory Device	Issued	Silicon Image, Inc.
11/689,386	7,881,258	United States	Circuitry To Prevent Peak Power Problems During Scan Shift	Issued	SiBEAM, Inc.
11/726,874	8,155,712	United States	Low Power Very High-Data Rate Device	Issued	SiBEAM, Inc.
11/588,472	8,022,887	United States	Planar Antenna	Issued	SiBEAM, Inc.
11/752,073		United States	A Compact Millimeter Wave Vertical Interconnection Scheme By Combining Flip-Chip, Layer Transition	Pending	SiBEAM, Inc.
11/752,083	7,675,465	United States	Surface Mountable Integrated Circuit Packaging Scheme	Issued	SiBEAM, Inc.
12/215,959		United States	Mechanism For Communication With Multiple Wireless Video Area Networks	Pending	SiBEAM, Inc.
11/981,935		United States	Wireless HD Mac Frame Format	Pending	SiBEAM, Inc.
11/938,126	8,170,522	United States	Multi-Transformer Architecture For An RF Active Circuit	Issued	SiBEAM, Inc.
11/999,810	8,750,241	United States	Concurrent Association With Multiple WVAN Network	Issued	SiBEAM, Inc.
12/079,133	8,831,225	United States	Data Security	Issued	SiBEAM, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/011,404	7,948,961	United States	Wireless Proximity Estimation	Issued	SiBEAM, Inc.
11/982,209	8,279,784	United States	Wireless HD AV Packet Format	Issued	SiBEAM, Inc.
12/055,160	8,170,617	United States	Extensions To Adaptive BeamSteering Method	Issued	SiBEAM, Inc.
12/164,757		United States	Exchanging Information Between Components Coupled With An I2C Bus Via Separate Banks	Pending	SiBEAM, Inc.
12/167,195	8,229,352	United States	Wireless Architecture For 60 GHz	Issued	SiBEAM, Inc.
11/901,069	7,986,753	United States	Modified Branch Metric For Decoders And Equalizers	Issued	SiBEAM, Inc.
12/059,757	7,915,909	United States	RF Integrated Circuit Test Methodology And System	Issued	SiBEAM, Inc.
12/164,907		United States	Dispatch Capability Using A Single Physical Interface	Pending	SiBEAM, Inc.
12/165,468		United States	Bitmap Device Identification In A Wireless Communication System	Pending	SiBEAM, Inc.
12/165,472	8,897,719	United States	Initializing A Transceiver In A Wireless Communication System	Issued	SiBEAM, Inc.
12/164,849	8,341,271	United States	Device Discovery In A Wireless Communication System	Issued	SiBEAM, Inc.
12/164,810	8,116,333	United States	Connection Control In A Wireless Communication System	Issued	SiBEAM, Inc.
12/699,758	8,588,193	United States	Enhanced Wireless Data Rates Using Multiple Beams	Issued	SiBEAM, Inc.
12/699,781	8,457,026	United States	Enhanced Wireless Data Rates Using Multiple Beams	Issued	SiBEAM, Inc.
13/113,318		United States	Apparatus, System, And Method For A Compact Symmetrical Transition Structure For Radio	Allowed	SiBEAM, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Frequency Applications		
14/128,551		United States	Method To Drive HDMI Or MHL Or USB Data Through One Set Of Pins	Pending	Silicon Image, Inc.
13/984,018		United States	Concept And Method Of Reducing Data Dependent Jitter	Pending	Silicon Image, Inc.
13/269,450		United States	Identification And Handling Of Data Streams Using Coded Preambles	Allowed	Silicon Image, Inc.
13/611,786		United States	Combining Video And Audio Streams Utilizing Pixel Repetition Bandwidth	Pending	Silicon Image, Inc.
14/118,832		United States	Compensation Scheme For MHL Common Mode Clock Swing	Pending	Silicon Image, Inc.
13/773,534		United States	Transmitting Multiple Differential Signals Over a Reduced Number of Physical Channels	Pending	Silicon Image, Inc.
13/460,393		United States	Cost-Efficient And Low-Latency Motion Picture Encoding For Limited Channel Bandwidth	Pending	Silicon Image, Inc.
13/791,494	8,925,003	United States	Mechanism For Facilitating Syncronization Of Audio And Video Between Multiple Media Devices	Issued	Silicon Image, Inc.
13/622,286	8,885,435	United States	Interfacing Between Integrated Circuits With Asymmetric Voltage Swing	Issued	Silicon Image, Inc.
13/770,984		United States	Configurable Single Ended Driver	Pending	Silicon Image, Inc.
13/779,372	8,920,188	United States	Integrated Connector/Flex Cable	Issued	Silicon Image, Inc.
13/834,927		United States	Simultaneous Transmission Of Clock And Bidirectional Data Over A Communication Channel	Allowed	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
13/605,708	8,841,974	United States	Test Solution For Ring Oscillators	Issued	Silicon Image, Inc.
14/193,932		United States	Test Solution for a Random Number Generator	Pending	Silicon Image, Inc.
13/787,664		United States	Auxiliary Data Encoding In Video Data	Pending	Silicon Image, Inc.
13/738,768		United States	Method And Apparatus For Reducing Digital Video Image Data	Pending	Silicon Image, Inc.
13/736,765	8,832,338	United States	Mechanism For Facilitating Dynamic Timestamp-Less Clock Regeneration For Transmitting Media Streams Over Shared Channels	Issued	Silicon Image, Inc.
14/123,037		United States	Timing Controlled Cascade Feed-Through High Speed Line Driver	Pending	Silicon Image, Inc.
13/776,577		United States	Apparatus, System And Method For Providing Clock And Data Signaling	Pending	Silicon Image, Inc.
13/940,038		United States	Integrated Mobile Desktop	Pending	Silicon Image, Inc.
13/915,586		United States	Multiple Protocol Tunneling Using Time Division Operations	Pending	Silicon Image, Inc.
13/891,842	8,786,776	United States	Method, Apparatus And System For Communicating Sideband Data With Non-Compressed Video	Issued	Silicon Image, Inc.
13/671,527		United States	Methods And Apparatuses To Provide And Electro-Optical Alignment	Pending	Silicon Image, Inc.
14/371,973		United States	Charge Pump Calibration for Dual-Path Phase-Locked Loop	Pending	Silicon Image, Inc.
14/115,324		United States	Mechanism for Facilitating Dynamic Phase Detection with High Jitter Tolerance for Images of Media Streams	Allowed	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/135,470		United States	Apparatus, System and Method for Formatting Audio-Video Information	Pending	Silicon Image, Inc.
13/839,671		United States	Full Frame Buffer To Improve Video Performance In Low- Latency Video Communication Systems	Pending	Silicon Image, Inc.
12/057,051		United States	Bi-Directional Digital Interface For Video And Audio (DIVA)	Pending	Silicon Image, Inc.
11/760,164	7,940,809	United States	Digital Video Interface With Bi-Directional Half-Duplex Clock Channel Used As Auxiliary Data Channel	Issued	Silicon Image, Inc.
11/865,621	7,916,780	United States	Adaptive Equalizer For Use With Clock And Data Recovery Circuit Of Serial Communication Link	Issued	Silicon Image, Inc.
12/222,745	7,737,802	United States	Passive Equalizer With Negative Impedance To Increase A Gain	Issued	Silicon Image, Inc.
12/636,063	8,680,712	United States	Power Delivery Over Digital Interactive Interface For Video And Audio (DIIVA)	Issued	Silicon Image, Inc.
13/521,739		United States	Multi-Media USB Data Transfer Over Digital Interaction Interface for Video and Audio (DIIVA)	Pending	Silicon Image, Inc.
13/521,762		United States	Video Management And Control In Home Multimedia Network	Pending	Silicon Image, Inc.
14/381,186		United States	Linear Regulator with Improved Power Supply Ripple Rejection	Pending	Silicon Image, Inc.
13/844,152		United States	Electronic Alignment Of Optical Signals	Pending	Silicon Image, Inc.
14/391,382		United States	Frequency Response Compensation in a Digital to Analog Converter	Pending	Silicon Image, Inc.
14/165,340		United States	Apparatus, System and	Pending	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Method for Providing Switching with a T-Coil Circuit		Inc.
13/836,895	8,928,411	United States	Integration Of Signal Sampling Within Transistor Amplifier Stage	Issued	Silicon Image, Inc.
14/165,345		United States	Apparatus, Method and System for Asymmetric Full-Duplex Communication	Pending	Silicon Image, Inc.
14/209,785		United States	Method And Apparatus For Implementing Wide Data Range And Wide Common-Mode Receivers	Pending	Silicon Image, Inc.
14/296,377		United States	Transmitting Apparatus with Source Termination	Pending	Silicon Image, Inc.
14/368,781		United States	Caching of Capabilities Information of Counterpart Device for Efficient Handshaking Operation	Pending	Silicon Image, Inc.
14/163,981		United States	Mechanism for Facilitating Dynamic Counter Synchronization and Packetization in High-Definition Multimedia Interface and Mobile High-Definition Link	Pending	Silicon Image, Inc.
14/253,808		United States	Communication of Multimedia Data Streams Over Multiple Communication Lanes	Pending	Silicon Image, Inc.
14/279,316		United States	HDCP2.2 Authentication Engine and Stream Cipher Engine Sharing in Digital Content Protection Architectures	Pending	Silicon Image, Inc.
14/383,865		United States	Techniques for Fractional-N Phase Locked Loops	Pending	Silicon Image, Inc.
61/949,901		United States	Compressed Video Transfer Over HDMI and MHL	Pending	Silicon Image, Inc.
14/563,797		United States	Electrical Duplex to Optical Conversion	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/470,750		United States	Arbitration Signaling within a Multimedia High Definition Link (MHL 3) Device	Pending	Silicon Image, Inc.
14/275,692		United States	Error Detection and Mitigation in Video Channels	Pending	Silicon Image, Inc.
14/339,393		United States	Phase-Modulated On-Off Keying for Millimeter Wave Spectrum Control	Pending	Silicon Image, Inc.
14/145,715		United States	Messaging to Provide Data Link Integrity	Pending	Silicon Image, Inc.
14/145,736	8,854,548	United States	Mechanism for Memory Reduction in Picture-In-Picture Video Generation	Issued	Silicon Image, Inc.
14/470,613		United States	Compressed Video Transfer Over a Multimedia Link	Pending	Silicon Image, Inc.
14/184,647		United States	Video Frame Synchronization	Pending	Silicon Image, Inc.
14/181,446		United States	Power Delivery Over Digital Interaction Interface for Video and Audio (DiiVA)	Pending	Silicon Image, Inc.
14/470,804		United States	Phase Relationship Control for Control Channel of a Multimedia Communication Link	Pending	Silicon Image, Inc.
14/470,809		United States	Retry Disparity for Control Channel of a Multimedia Communication Link	Pending	Silicon Image, Inc.
61/943,267		United States	Pre-Processor and Post-Processor for Compression of 4:2:0 Encoded Video Streams with Video Compression Codecs Embedded within an Audio/Video Standard	Pending	Silicon Image, Inc.
14/278,255		United States	Encoding Guard Band Data for Transmission Via a Communications Interface Utilizing Transition-Minimized Differential Signaling (Tmds) Coding	Pending	Silicon Image, Inc.
14/322,753		United States	Calibration Of Single-Ended	Pending	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			High-Speed Interfaces		Inc.
61/947,704		United States	Reversible Connector	Pending	Silicon Image, Inc.
14/460,737		United States	System and Method for Transcoding Data	Pending	Silicon Image, Inc.
14/502,928		United States	Electrical Connector with Optical Channel	Pending	Silicon Image, Inc.
14/322,753		United States	Cable with Circuitry for Communicating Performance Information	Pending	Silicon Image, Inc.
61/973,837		United States	Error Correction for Transmission of Compressed Video Data Over Standards-Defined Coded Audio/Video Links	Pending	Silicon Image, Inc.
61/975,517		United States	(MHL) Connector Cable Detect, Cable Orientation Detect and/or Lane Re-Mapping	Pending	Silicon Image, Inc.
61/979,477		United States	MHL3 Router without HDCP2.2 Decryption and Encryption Operation	Pending	Silicon Image, Inc.
61/979,483		United States	TDD over 5-Pin Interface	Pending	Silicon Image, Inc.
14/470,620		United States	Compressed Blanking Period Transfer Over a Multimedia Link	Pending	Silicon Image, Inc.
14/273,400		United States	Transmission and Detection of Multi-Channel Signals in Reduced Channel Format	Pending	Silicon Image, Inc.
61/989,409		United States	System for Dynamic Capabilities, Status, and Metadata Exchange	Pending	Silicon Image, Inc.
14/300,166		United States	Configurable Multi-Dimensional Driver and Receiver	Pending	Silicon Image, Inc.
14/483,013		United States	Enhanced Communication Link Using Synchronization Signal as Link Command	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
62/043,218		United States	Run Length Programmable Unified Built-In Self-Test (BIST) Scheme for Various High-Speed Serial IO Standards	Pending	Silicon Image, Inc.
14/559,523		United States	Determination of Physical Connectivity Status of Devices Based on Electrical Measurement	Pending	Silicon Image, Inc.
14/516,136		United States	Method and System for Improving Serial Port Memory Communication Latency and Reliability	Pending	Silicon Image, Inc.
62/061,630		United States	Secure Control Communication Between an Application Processor and a Transmitter	Pending	Silicon Image, Inc.
62/075,554		United States	Metadata Transfer for HDMI/MHL	Pending	Silicon Image, Inc.
14/570,817		United States	Mechanism for Facilitating Dynamic Phase Detection with High Jitter Tolerance for Images of Media Streams	Pending	Silicon Image, Inc.
14/589,889		United States	Displaying Multiple Videos on Sink Device Using Display Information of Source Device	Pending	Silicon Image, Inc.
14/589,925		United States	Lower Power Operations in a Wireless Tunneling Transceiver	Pending	Silicon Image, Inc.
14/591,845		United States	Simultaneous Transmission of Clock and Bidirectional Data Over a Communication Channel	Pending	Silicon Image, Inc.
14/449095	20150036756	United States	Radio Frequency Interference Reduction In Multimedia Interfaces	Pending	Silicon Image, Inc.

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PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5533419

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
JEFFERIES FINANCE LLC	05/17/2019

RECEIVING PARTY DATA

Name:	LATTICE SEMICONDUCTOR CORPORATION
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	SILICON IMAGE, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	SIBEAM, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	DVDO, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124

PROPERTY NUMBERS Total: 1143

Property Type	Number
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Application Number:	14449095
Application Number:	12842190

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SIGNATURE:	/Urmila Karandikar/
DATE SIGNED:	05/21/2019
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 97

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RELEASE OF A SECURITY INTEREST -- PATENTS

May 17, 2019

WHEREAS, pursuant to that certain (i) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035222, Frame 0866, (ii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035308, Frame 0428, (iii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035223, Frame 0001, (iv) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035226, Frame 0289, (v) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035223, Frame 0387, (vi) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035226, Frame 0147, (vii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035220, Frame 0048, (viii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035220, Frame 0226, (ix) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035309, Frame 0142, (x) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035308, Frame 0345, (xi) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035225, Frame 0839 and (xii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035225, Frame 0352, LATTICE SEMICONDUCTOR CORPORATION, SILICON IMAGE, INC., SIBEAM, INC. and DVDO, INC., each a Delaware corporation (each, a "Releasee"), granted to JEFFERIES FINANCE LLC, as collateral agent for the ratable benefit of the Secured Creditors (the "Releasor"), a continuing security interest in all right, title and interest of the Releasees in, to and under United States Patents listed on the attached Schedule A (the "Patents"), and all Proceeds in respect thereof (with all of the Releasee's rights listed above being collectively referred to as the "Collateral") to secure the payment, performance and observance of the Obligations;

WHEREAS, the Releasees have satisfied their Obligations; and

WHEREAS, the Releasee has requested and the Releasor has agreed to provide a document suitable for recording in the United States Patent and Trademark Office evidencing and effecting the release, relinquishment and discharge of its security interest in the Collateral.

NOW, THEREFORE, in consideration of and in exchange for good and valuable consideration, the Releasor hereby agrees as follows:

1. Defined Terms. All capitalized terms used but not otherwise defined herein have the meanings given to them in the Grants of Security Interests in United States Patents.

2. Release of Security Interest. The Releasor hereby, without any representation and warranty and without any recourse to the Releasor, releases, relinquishes and discharges all of its security interest in the Collateral.

[Signature Page Follows]

IN WITNESS WHEREOF, the undersigned has executed and delivered this Release as of the date first written above.

JEFFERIES FINANCE LLC,
as Collateral Agent and Releasor

By: _____
Name: Paul Chisholm
Title: Managing Director

[Signature Page to Release of Patent Security Interest]

SCHEDULE A

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/396,994	5574678	United States	Continuous Time Programmable Analog Block Architecture	Issued	Lattice Semiconductor Corporation
08/403,359	5510738	United States	CMOS Programmable Resistor-Based Transconductor	Issued	Lattice Semiconductor Corporation
08/403,354	5493205	United States	Low Distortion Differential Transconductor Output Current Mirror	Issued	Lattice Semiconductor Corporation
08/403,352	5617064	United States	Active Resistor For Stability Compensation [of Transconductor & Op-Amp Based Gain & Filter Stages]	Issued	Lattice Semiconductor Corporation
08/403,595	5670907	United States	VBB Reference for Pumped Substrates	Issued	Lattice Semiconductor Corporation
08/423,303	5490074	United States	Constant delay interconnect for coupling configurable logic blocks	Issued	Lattice Semiconductor Corporation
08/427,117	5596524	United States	CMOS memory cell with gate oxide of both NMOS and PMOS transistors as tunneling window for program and erase	Issued	Lattice Semiconductor Corporation
08/444,306	5491433	United States	Cascode array cell partitioning for a sense amplifier of a programmable logic device	Issued	Lattice Semiconductor Corporation
08/449,384	5756367	United States	Method of making a spacer based antifuse structure for low capacitance and high reliability	Issued	Lattice Semiconductor Corporation
08/447,991	5594687	United States	Completely complementary MOS memory cell with tunneling through the NMOS and PMOS transistors during program and erase	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/453,184	5570046	United States	Lead frame with noisy and quiet Vss and Vdd leads	Issued	Lattice Semiconductor Corporation
08/453,479	5583451	United States	Polarity control circuit which may be used with a ground bounce limiting buffer	Issued	Lattice Semiconductor Corporation
08/456,946	5621650	United States	Programmable gate array with improved interconnect structure, input/output structure and configurable logic block	Issued	Lattice Semiconductor Corporation
08/459,960	5521529	United States	Very high-density complex programmable logic device with a multi-tiered hierarchical switch matrix and optimized flexible logic allocation	Issued	Lattice Semiconductor Corporation
08/459,230	5818254	United States	Multi-tiered hierarchical high speed switch matrix structure for very high-density complex programmable logic devices	Issued	Lattice Semiconductor Corporation
08/459,234	5781030	United States	Programmable uniform symmetrical distribution logic allocator for a high-density complex PLD	Issued	Lattice Semiconductor Corporation
08/459,786	5638018	United States	P-type flip flop	Issued	Lattice Semiconductor Corporation
08/458,865	5589782	United States	Macrocell and clock signal allocation circuit for a programmable logic device (PLD) enabling PLD resources to provide multiple functions	Issued	Lattice Semiconductor Corporation
08/459,570	6531890	United States	Programmable optimized-distribution logic allocator for a high-density complex PLD	Issued	Lattice Semiconductor Corporation
08/461,196	5586044	United States	Array of configurable logic blocks including cascadable lookup tables	Issued	Lattice Semiconductor Corporation
08/462,934	5469368	United States	Array of configurable logic blocks each including a first	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			lookup table coupled to selectively replace an output of second lookup with an alternate function output		Corporation
08/486,178	5764078	United States	Family of multiple segmented programmable logic blocks interconnected by a high speed centralized switch matrix	Issued	Lattice Semiconductor Corporation
08/474,629	5612631	United States	An I/O macrocell for a programmable logic device	Issued	Lattice Semiconductor Corporation
08/479,872	5869981	United States	A High density programmable logic device	Issued	Lattice Semiconductor Corporation
08/486,174	5594365	United States	Architecture of a multiple array high density programmable logic device with a plurality of programmable switch matrices	Issued	Lattice Semiconductor Corporation
08/474,635	5811986	United States	Flexible synchronous/asynchronous cell structure for a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/466,438	5754471	United States	Reference for CMOS memory cell having PMOS and NMOS transistors with a common floating gate	Issued	Lattice Semiconductor Corporation
08/466,438	5754471	United States	Low power CMOS array for a PLD with program and erase using controlled avalanche injection	Issued	Lattice Semiconductor Corporation
08/473,620	5594657	United States	Field Programmable Gate Array Using Look-Up Tables, Multiplexers and Decoders	Issued	Lattice Semiconductor Corporation
08/483,623	5617042	United States	Multiple array programmable logic device with a plurality of programmable switch matrices	Issued	Lattice Semiconductor Corporation
08/492,604	5526278	United States	System for Synthesizing Field Programmable Gate Array	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Implementations From High Level Circuit Descriptions		Corporation
08/493,640	5679599	United States	Isolation using self-aligned trench formation and conventional LOCOS	Issued	Lattice Semiconductor Corporation
08/494,271	5565794	United States	Voltage range tolerant CMOS output buffer with reduced input capacitance	Issued	Lattice Semiconductor Corporation
08/497,992	5742542	United States	Nonvolatile memory cells using only positive charge to store data	Issued	Lattice Semiconductor Corporation
08/500,295	5700698	United States	Method for screening non-volatile memory and programmable logic devices	Issued	Lattice Semiconductor Corporation
08/501,230	5604370	United States	Field Implant For Semiconductor Device	Issued	Lattice Semiconductor Corporation
08/505,837	5635855	United States	Method for Simultaneous Programming of In-System Programmable Integrated Circuits	Issued	Lattice Semiconductor Corporation
08/507,893	5570039	United States	Method and Apparatus for Converting Field-Programmable Gate Array Implementations Into Mask-Programmable Logic Cell Implementations	Issued	Lattice Semiconductor Corporation
08/507,957	5559450	United States	Programmable Function Unit As Parallel Multiplier Cell	Issued	Lattice Semiconductor Corporation
08/528,030	5581126	United States	Interlaced layout configuration for differential pairs of interconnect lines	Issued	Lattice Semiconductor Corporation
08/535,362	5528170	United States	Low-Skew Signal Routing In A Programmable Array	Issued	Lattice Semiconductor Corporation
08/551,974	5615150	United States	control gate-addressed cmos non-volatile cell that programs through gates of CMOS transistors	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/554,092	5587945	United States	CMOS EEPROM cell with tunneling window in the read path	Issued	Lattice Semiconductor Corporation
08/560,038	5666309	United States	Memory cell for a programmable logic device (PLD) avoiding pumping programming voltage above an NMOS threshold	Issued	Lattice Semiconductor Corporation
08/560,933	5587921	United States	Array of configurable logic blocks each including a lookup table having inputs coupled to a first multiplexer and having outputs to a second multiplexer	Issued	Lattice Semiconductor Corporation
08/561,306	5672521	United States	Method of forming multiple gate oxide thicknesses on a wafer substrate	Issued	Lattice Semiconductor Corporation
08/573,622	5809522	United States	Microprocessor system with process identification tag entries to reduce cache flushing after a context switch	Issued	Lattice Semiconductor Corporation
08/574,776	5739713	United States	Deconvolution input buffer compensating for capacitance of a switch matrix of a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/575,898	5736888	United States	Capacitance elimination circuit	Issued	Lattice Semiconductor Corporation
08/575,852	5719516	United States	Clock generator circuit for use with a dual edge register that provides a separate enable for each edge over an input clock signal	Issued	Lattice Semiconductor Corporation
08/596,679	5598346	United States	Array of configurable logic blocks including network means for broadcasting clock signals to different pluralities of logic blocks	Issued	Lattice Semiconductor Corporation
08/606,702	5623217	United States	Field Programmable Gate Array With Write-Port Enabled Memory	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/614,728	5926841	United States	Segment descriptor cache for a processor	Issued	Lattice Semiconductor Corporation
08/625,403	5646901	United States	CMOS memory cell with tunneling during program and erase through the NMOS and PMOS transistors and a pass gate separating the NMOS and PMOS transistors	Issued	Lattice Semiconductor Corporation
08/632,811	5751163	United States	Parallel Programming of ISP Devices Using An Automatic Tester	Issued	Lattice Semiconductor Corporation
08/635,184	5666087	United States	Active Resistor For Stability Compensation [of Transconductor & Op-Amp Based Gain & Filter Stages]	Issued	Lattice Semiconductor Corporation
08/643,807	5748525	United States	Array cell circuit with split read/write line	Issued	Lattice Semiconductor Corporation
08/643,291	5864486	United States	Method And Apparatus For In-System Programming of A Programmable Logic Device Using a Two-Wire Interface	Issued	Lattice Semiconductor Corporation
08/653,186	5789939	United States	Very high-density complex programmable logic device with a multi-tiered hierarchical switch matrix and optimized flexible logic allocation	Issued	Lattice Semiconductor Corporation
08/659,279	5723984	United States	Field programmable gate array (FPGA) with interconnect encoding	Issued	Lattice Semiconductor Corporation
08/659,941	5808942	United States	Field programmable gate array (FPGA) having an improved configuration memory and look up table	Issued	Lattice Semiconductor Corporation
08/664,190	5830795	United States	Simplified masking process for programmable logic device manufacture	Issued	Lattice Semiconductor Corporation
08/666,193	5760609	United States	Clock signal providing circuit with enable and a pulse generator with enable for use	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			in a block clock circuit of a programmable logic device		
08/668,141	5796295	United States	Reference for CMOS memory cell having PMOS and NMOS transistors with a common floating gate	Issued	Lattice Semiconductor Corporation
08/668,896	5751164	United States	Programmable logic device with multi-level power control	Issued	Lattice Semiconductor Corporation
08/683,685	5734275	United States	Programmable logic device having a sense amplifier with virtual ground	Issued	Lattice Semiconductor Corporation
08/683,373	5818294	United States	Temperature insensitive current source	Issued	Lattice Semiconductor Corporation
08/690,768	5801551	United States	Depletion mode pass gates with controlling decoder and negative power supply for a programmable logic device	Issued	Lattice Semiconductor Corporation
08/689,523	5942780	United States	An integrated circuit having, and process providing, different oxide layer thicknesses on a substrate	Issued	Lattice Semiconductor Corporation
08/696,444	5796750	United States	Method for Programming a PLD In An Automatic Tester	Issued	Lattice Semiconductor Corporation
08/700,616	5740069	United States	Logic device (PLD) having direct connections between configurable logic blocks (CLBs) and configurable input/output blocks (IOBs)	Issued	Lattice Semiconductor Corporation
08/699,401	5960274	United States	Oxide formation process for manufacturing programmable logic device	Issued	Lattice Semiconductor Corporation
08/702,846	5959336	United States	Decoder circuit with short channel depletion transistors	Issued	Lattice Semiconductor Corporation
08/710,445	5862365	United States	Configuration Pin Emulation Circuit For a Field Programmable Array	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/723,082	5760605	United States	Programmable high speed routing switch	Issued	Lattice Semiconductor Corporation
08/726,512	5761116	United States	Vpp only scalable EEPROM memory cell having transistors with thin tunnel gate oxide	Issued	Lattice Semiconductor Corporation
08/729,117	5991907	United States	Method for Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/734,888	5805607	United States	Method for user-controlled I/O switching during in-circuit programming of CPLDs through the IEEE 1149.1 test access port	Issued	Lattice Semiconductor Corporation
08/740,948	5811987	United States	Block clock and initialization circuit for a complex high density PLD	Issued	Lattice Semiconductor Corporation
08/748,041	5892962	United States	FPGA-based Processor	Issued	Lattice Semiconductor Corporation
08/745,410	5717342	United States	Output buffer incorporating shared intermediate nodes	Issued	Lattice Semiconductor Corporation
08/781,882	6028993	United States	Timed Circuit Simulation In Hardware Using FPGAs	Issued	Lattice Semiconductor Corporation
08/785,096	5841701	United States	Method of charging and discharging floating gage transistors to reduce leakage current	Issued	Lattice Semiconductor Corporation
08/799,153	5904575	United States	Method and apparatus incorporating nitrogen selectively for differential oxide growth	Issued	Lattice Semiconductor Corporation
08/799,235	5885904	United States	Method to incorporate, and a device having, oxide enhancement dopants using gas immersion laser doping (GILD) for selectively growing an oxide layer	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/823,953	6190966	United States	Process for fabricating semiconductor memory device with high data retention including silicon nitride etch stop layer formed at high temperature with low hydrogen ion	Issued	Lattice Semiconductor Corporation
08/828,520	5905385	United States	Memory bits used to couple look up table inputs to facilitate increased availability to routing resources particularly for variable sized look up tables for a field programmable gate array (FPGA)	Issued	Lattice Semiconductor Corporation
08/831,372	5844912	United States	Fast verify for CMOS memory cell	Issued	Lattice Semiconductor Corporation
08/827,671	5835405	United States	Application Specific Modules in a Programmable Logic Device	Issued	Lattice Semiconductor Corporation
08/843,150	6087275	United States	Reduction of n-channel parasitic transistor leakage by using low power/low pressure phosphosilicate glass	Issued	Lattice Semiconductor Corporation
08/838,487	6034541	United States	In-System Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
08/856,926	5949279	United States	Devices for sourcing constant supply current from power supply in system with integrated circuit having variable supply current requirement	Issued	Lattice Semiconductor Corporation
08/859,761	5989957	United States	Process for fabricating semiconductor memory device with high data retention including silicon nitride etch stop layer formed at high temperature with low hydrogen ion concentration	Issued	Lattice Semiconductor Corporation
08/871,589	5978272	United States	Nonvolatile memory structure for programmable logic devices	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/899,428	6028447	United States	FPGA Having Predictable Open-Drain Drive Mode	Issued	Lattice Semiconductor Corporation
08/912,763	6072351	United States	Output buffer for making a high voltage (5.0 volt) compatible input/output in a low voltage (2.5 volt) semiconductor process	Issued	Lattice Semiconductor Corporation
08/931,798	6359466	United States	Circuitry to provide fast carry	Issued	Lattice Semiconductor Corporation
08/938,550	6020755	United States	Hybrid Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/948,306	6097212	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/947,888	5854114	United States	Data retention of EEPROM cell with shallow trench isolation using thicker liner oxide	Issued	Lattice Semiconductor Corporation
08/949,992	6028463	United States	Programmable Clock Manager For A Programmable Logic Device that Can Generate At Least Two Different Output Clocks	Issued	Lattice Semiconductor Corporation
08/950,444	6216191	United States	Field Programmable Gate Array Having A Dedicated Processor Interface	Issued	Lattice Semiconductor Corporation
08/950,446	5986471	United States	Bi-directional Buffers and Supplemental Logic and Interconnect Cells for Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
08/950,448	6060902	United States	A Programmable Clock Manager For A Programmable Logic Device that Can Be Programmed Without Reconfiguring the Device	Issued	Lattice Semiconductor Corporation
08/950,624	6049224	United States	Programmable Logic Device With Logic Cells Having A Flexible Input Structure	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/951,128	6043677	United States	Programmable Clock Manager For A Programmable Logic Device that Can Implement Delay-Locked Loop Functions	Issued	Lattice Semiconductor Corporation
08/964,421	6389321	United States	Simultaneous Wired and Wireless Remote In-System Programming of Multiple Remote Systems	Issued	Lattice Semiconductor Corporation
08/974,799	6003150	United States	Method for Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/996,361	6275064	United States	Symmetrical, extended and fast direct connections between variable grain blocks in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/996,049	6127843	United States	Dual port SRAM memory for run time use in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,615	6034544	United States	Programmable input/output block (IOB) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,614	5982193	United States	Input/output block (IOB) connections to MAXL lines, NOR lines and dendrites in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,612	5990702	United States	Flexible direct connections between input/output blocks (IOBs) and variable grain blocks (VBGs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/997,221	6107823	United States	Programmable control multiplexing for input/output blocks (IOBs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/996,119	5986480	United States	Multiple input zero power and/nor gate for use in a field programmable gate array (FPGA)	Issued	Lattice Semiconductor Corporation
08/996,530	6134703	United States	A Process for Programming PLDs and Embedded Non-Volatile Memories	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/998,978	6102963	United States	Electrically erasable and reprogrammable, nonvolatile integrated storage device with in-system programming and verification (ISPAV) capabilities for supporting in-system reconfiguring of PLD's	Issued	Lattice Semiconductor Corporation
09/008,762	6130551	United States	Synthesis-friendly FPGA architecture with variable length and variable timing interconnect	Issued	Lattice Semiconductor Corporation
09/010,000	6034538	United States	Virtual Logic System For Reconfigurable Hardware	Issued	Lattice Semiconductor Corporation
09/023,669	6025637	United States	Spacer based antifuse structure for low capacitance and high reliability and method of fabrication thereof	Issued	Lattice Semiconductor Corporation
09/023,506	6023570	United States	Sequential and Simultaneous Manufacturing Programming of Multiple In-System Programmable Systems Through a Data Network	Issued	Lattice Semiconductor Corporation
09/026,814	6093946	United States	EEPROM cell with field-edgeless tunnel window using shallow trench isolation process	Issued	Lattice Semiconductor Corporation
09/037,095	6128770	United States	Configurable logic array including IOB to longlines interconnect means for providing selectable access to plural longlines from each IOB (input/output block)	Issued	Lattice Semiconductor Corporation
09/045,128	6064225	United States	Global Signal Distribution With Reduced Routing Tracks In An FPGA	Issued	Lattice Semiconductor Corporation
09/046,404	5982683	United States	Enhanced method of testing semiconductor devices having nonvolatile elements	Issued	Lattice Semiconductor Corporation
09/053,251	6556154	United States	Offset Voltage Calibration DAC With Reduced Sensitivity To Mismatch	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Errors		
09/059,552	6108806	United States	Method of Testing and Diagnosing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/067,320	6154050	United States	Internal tristate bus with arbitration logic	Issued	Lattice Semiconductor Corporation
09/067,318	6104207	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/069,035	6133750	United States	Combination of global clock and localized clocks	Issued	Lattice Semiconductor Corporation
09/069,768	6002610	United States	Non-Volatile Memory Element For Programmable Logic Applications and Operational Methods Therefor	Issued	Lattice Semiconductor Corporation
09/080,906	6225821	United States	Package migration for related programmable logic devices	Issued	Lattice Semiconductor Corporation
09/083,335	6304099	United States	Method and structure for dynamic in-system programming	Issued	Lattice Semiconductor Corporation
09/083,336	6066977	United States	Programmable Output Voltage Levels	Issued	Lattice Semiconductor Corporation
09/083,205	6255847	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/086,437	6087696	United States	Stacked tunneling dielectric technology for improving data retention of EEPROM cell	Issued	Lattice Semiconductor Corporation
09/109,123	6202182	United States	Method and Apparatus For Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/114,385	6028758	United States	Electrostatic discharge (ESD) protection for a 5.0 volt compatible input/output (I/O) in a 2.5 volt semiconductor process	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/114,717	6091595	United States	Electrostatic discharge (ESD) protection for NMOS pull up transistors of a 5.0 volt compatible output buffer using 2.5 volt process transistors	Issued	Lattice Semiconductor Corporation
09/114,718	6043969	United States	Ballast resistors with parallel stacked NMOS transistors used to prevent secondary breakdown during ESD with 2.5 volt process transistors	Issued	Lattice Semiconductor Corporation
09/115,683	6124732	United States	Signaling Voltage Range Discriminator	Issued	Lattice Semiconductor Corporation
09/118,200	6028446	United States	Flexible Synchronous and Asynchronus Circuits for A Very High Density Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/134,174	6064105	United States	Data retention of EEPROM cell with shallow trench isolation using thicker liner oxide	Issued	Lattice Semiconductor Corporation
09/145,793	6087854	United States	High Speed Line Driver With Direct and Complementary Outputs	Issued	Lattice Semiconductor Corporation
09/169,848	6347387	United States	Test Circuits For Multiple FPGA Systems	Issued	Lattice Semiconductor Corporation
09/169,492	6424003	United States	EEPROM cell with self-aligned tunneling window	Issued	Lattice Semiconductor Corporation
09/187,691	6228696	United States	Semiconductor-oxide-semiconductor capacitor formed in integrated circuit	Issued	Lattice Semiconductor Corporation
09/187,689	6154051	United States	Tileable and compact layout for super variable grain blocks within FPGA device	Issued	Lattice Semiconductor Corporation
09/186,917	6229336	United States	Programmable integrated circuit device with slew control and skew control	Issued	Lattice Semiconductor Corporation
09/188,778	6169432	United States	High voltage switch for	Issued	Lattice

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			providing voltages higher than 2.5 volts with transistors made using a 2.5 volt process		Semiconductor Corporation
09/192,094	6291327	United States	Optimization of S/D annealing to minimize random S/D shorts in memory array	Issued	Lattice Semiconductor Corporation
09/192,096	6221733	United States	Reduction of mechanical stress in shallow trench isolation process	Issued	Lattice Semiconductor Corporation
09/196,449	6191612	United States	Enhanced I/O control flexibility for generating control signals	Issued	Lattice Semiconductor Corporation
09/196,080	5912550	United States	Power converter with 2.5 semiconductor process components	Issued	Lattice Semiconductor Corporation
09/198,796	6218857	United States	Variable sized line driving amplifiers for input/output blocks (IOBs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/200,395	6261944	United States	Semiconductor device having high reliability passivation and fabrication method	Issued	Lattice Semiconductor Corporation
09/198,653	6009033	United States	Method of programming and erasing an EEPROM device under an elevated temperature and apparatus thereof	Issued	Lattice Semiconductor Corporation
09/199,664	6353352	United States	Clock tree topology	Issued	Lattice Semiconductor Corporation
09/201,081	6133769	United States	Phase locked loop with a lock detector	Issued	Lattice Semiconductor Corporation
09/203,149	6404006	United States	EEPROM cell with tunneling across entire separated channels	Issued	Lattice Semiconductor Corporation
09/217,647	5969992	United States	EEPROM cell using p-well for	Issued	Lattice Semiconductor Corporation
09/207,558	6175266	United States	Operational amplifier with CMOS transistors made using	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			2.5 volt process transistors		Corporation
09/208,203	6163168	United States	Efficient interconnect network for use in FPGA device having variable grain architecture	Issued	Lattice Semiconductor Corporation
09/212,022	6124730	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/212,330	6100715	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/212,331	6081473	United States	FPGA integrated circuit having embedded SRAM memory blocks each with statically and dynamically controllable read mode	Issued	Lattice Semiconductor Corporation
09/216,662	6204686	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	Issued	Lattice Semiconductor Corporation
09/216,051	6214666	United States	Method of forming a non-volatile memory device	Issued	Lattice Semiconductor Corporation
09/217,648	6232631	United States	Floating gate memory cell structure with programming mechanism outside the read path	Issued	Lattice Semiconductor Corporation
09/217,646	6282123	United States	Method of fabricating, programming, and erasing a dual pocket two sided program/erase non-volatile memory cell	Issued	Lattice Semiconductor Corporation
09/218,987	6294810	United States	EEPROM cell with tunneling at separate edge and channel regions	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/220,469	6157568	United States	Avalanche programmed floating gate memory cell structure with program element in first polysilicon layer	Issued	Lattice Semiconductor Corporation
09/221,360	6294809	United States	Avalanche programmed floating gate memory cell structure with program element in polysilicon	Issued	Lattice Semiconductor Corporation
09/226,702	6215700	United States	PMOS avalanche programmed floating gate memory cell structure	Issued	Lattice Semiconductor Corporation
09/227,981	6197638	United States	Oxide formation process for manufacturing programmable logic device	Issued	Lattice Semiconductor Corporation
09/235,356	6097664	United States	Multi-port SRAM cell array having plural write paths including for writing through addressable port and through serial boundary scan	Issued	Lattice Semiconductor Corporation
09/235,351	6181163	United States	FPGA integrated circuit having embedded SRAM memory blocks and interconnect channel for broadcasting address and control	Issued	Lattice Semiconductor Corporation
09/235,615	6211695	United States	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	Issued	Lattice Semiconductor Corporation
09/239,072	5999449	United States	Two transistor EEPROM cell using P-well for tunneling across a channel	Issued	Lattice Semiconductor Corporation
09/240,560	6297128	United States	Process for manufacturing shallow trenches filled with dielectric material having low mechanical stress	Issued	Lattice Semiconductor Corporation
09/245,813	6294811	United States	Two transistor EEPROM cell	Issued	Lattice Semiconductor Corporation
09/255,410	6075724	United States	Method for sorting	Issued	Lattice

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			semiconductor devices having a plurality of non-volatile memory cells		Semiconductor Corporation
09/255,053	6255169	United States	Process for fabricating a high-endurance non-volatile memory device	Issued	Lattice Semiconductor Corporation
09/256,245	6133164	United States	Fabrication of oxide regions having multiple thicknesses using minimized number of thermal cycles	Issued	Lattice Semiconductor Corporation
09/261,776	6256758	United States	Fault Tolerance Operation of Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/263412	6075293	United States	Semiconductor device having a multi-layer metal interconnect structure	Issued	Lattice Semiconductor Corporation
09/268,897	6207989	United States	Non-volatile memory device having a high-reliability composite insulation layer	Issued	Lattice Semiconductor Corporation
09/276,991	6031365	United States	Band gap reference using a low voltage power supply	Issued	Lattice Semiconductor Corporation
09/276,990	6163175	United States	High voltage detector to control a power supply voltage pump for a 2.5 volt semiconductor process device	Issued	Lattice Semiconductor Corporation
09/277,441	6326663	United States	Avalanche injection EEPROM memory cell with p-type control gate	Issued	Lattice Semiconductor Corporation
09/280,887	6172392	United States	Boron doped silicon capacitor plate	Issued	Lattice Semiconductor Corporation
09/286,830	6284626	United States	Angled nitrogen ion implantation for minimizing mechanical stress on side walls of an isolation trench	Issued	Lattice Semiconductor Corporation
09/288,062	6265900	United States	High Speed Logical OR Circuit	Issued	Lattice Semiconductor Corporation
09/287,976	6413826	United States	Gate insulator process for	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			nanometer MOSFETs		Corporation
09/310,071	6424000	United States	Floating gate memory apparatus and method for selected programming thereof	Issued	Lattice Semiconductor Corporation
09/316,241	6274898	United States	Triple-well EEPROM cell using p-well for tunneling across a channel	Issued	Lattice Semiconductor Corporation
09/318,570	6552595	United States	High Voltage Discharge Scheme	Issued	Lattice Semiconductor Corporation
09/320389	6118693	United States	Electrically erasable non-volatile memory cell with integrated SRAM to reduce testing time	Issued	Lattice Semiconductor Corporation
09/320,392	6067252	United States	Electrically erasable non-volatile memory cell with no static power dissipation	Issued	Lattice Semiconductor Corporation
09/326,940	6184713	United States	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	Issued	Lattice Semiconductor Corporation
09/326,140	6150841	United States	Enhanced storage macrocell module for high density CPLD architectures	Issued	Lattice Semiconductor Corporation
09/330,753	6628660	United States	Finite State Machine with Associated Memory	Issued	Lattice Semiconductor Corporation
09/334,051	6028789	United States	Zero-power CMOS non-volatile memory cell having an avalanche injection element	Issued	Lattice Semiconductor Corporation
09/334,052	6034893	United States	Non-volatile memory cell having dual avalanche injection elements	Issued	Lattice Semiconductor Corporation
09/400,029	6404226	United States	Integrated Circuit With Standard Cell Logic and Spare Gates	Issued	Lattice Semiconductor Corporation
09/405,958	6550030	United States	On-Line Testing of the Programmable Logic Blocks In Field Programmable Gate	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Arrays		
09/406,219	6574761	United States	On-Line Testing of the Programmable Interconnect Network In Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/433,642	6191609	United States	Combination of global clock and localized clocks	Issued	Lattice Semiconductor Corporation
09/440,460	6294925	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/440,207	6278311	United States	Method for minimizing instantaneous currents when driving bus signals	Issued	Lattice Semiconductor Corporation
09/441,220	6208559	United States	Method of operating EEPROM memory cells having transistors with thin gate oxide and reduced disturb	Issued	Lattice Semiconductor Corporation
09/452,017	6137738	United States	Method For In-System Programming of Serially Configured EEPROMS Using a JTAG Interface of an FPGA	Issued	Lattice Semiconductor Corporation
09/454,322	6326808	United States	Inversion of Product Term Line Before or Logic in a Programmable Logic Device (PLD)	Issued	Lattice Semiconductor Corporation
09/472,645	6150842	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/506,180	6362684	United States	Amplifier Having an Adjustable Resistor Network	Issued	Lattice Semiconductor Corporation
09/507,580	6424209	United States	Integrated Programmable Continuous Time Filter with Programmable Capacitor Arrays	Issued	Lattice Semiconductor Corporation
09/548,171	6351157	United States	Output buffer for making a high voltage (5.0 volt) compatible input/output in a low voltage (2.5 volt)	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			semiconductor process		
09/567,898	6288937	United States	Decoded Generic Routing Pool	Issued	Lattice Semiconductor Corporation
09/578,086	6570212	United States	Complementary avalanche injection EEPROM cell	Issued	Lattice Semiconductor Corporation
09/603,119	6292930	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/603,807	6216257	United States	FPGA device and method that includes a variable grain function architecture for implementing configuration logic blocks and a complimentary variable length interconnect architecture for providing configurable routing between configuration logic blocks	Issued	Lattice Semiconductor Corporation
09/611,449	6530049	United States	On-line Fault Tolerant Operation Via Incremental Reconfiguration of Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/626,094	6380759	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/632,319	6567969	United States	Configurable Logic Array Including Lookup Table Means For Generating Functions of Different Numbers Of Input Terms	Issued	Lattice Semiconductor Corporation
09/643,279	6627947	United States	Compact single-poly two-transistor EEPROM cell	Issued	Lattice Semiconductor Corporation
09/651,689	6433602	United States	High speed schmitt trigger with low supply voltage	Issued	Lattice Semiconductor Corporation
09/660,707	6370071	United States	High Voltage CMOS switch	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
09/661,585	6462576	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/668,896	6701340	United States	Double Differential Comparator and Programmable Analog Block Architecture Using Same	Issued	Lattice Semiconductor Corporation
09/669,186	6249144	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/671,853	6631487	United States	On-Line Testing of Field Programmable Gate Array Resources	Issued	Lattice Semiconductor Corporation
09/692,694	6470485	United States	Scalable and parallel processing methods and structures for testing configurable interconnect network in FPGA device	Issued	Lattice Semiconductor Corporation
09/704,487	6507212	United States	Wide input programmable logic system and method	Issued	Lattice Semiconductor Corporation
09/651,805	6455912	United States	Process for manufacturing shallow trenches filled with dielectric material having low mechanical stress	Issued	Lattice Semiconductor Corporation
09/712,000	6356107	United States	Method and structure for dynamic in-system programming	Issued	Lattice Semiconductor Corporation
09/721,153	6348813	United States	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	Issued	Lattice Semiconductor Corporation
09/732,216	6735706	United States	Programmable power management system and method	Issued	Lattice Semiconductor Corporation
09/731,184	6524911	United States	Combination of BPTEOS oxide film with CMP and RTA to achieve good data	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			retention		
09/731,185	6287916	United States	Method for forming a semiconductor device using LPCVD nitride to protect floating gate from charge loss	Issued	Lattice Semiconductor Corporation
09/733,878	6526558	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	Issued	Lattice Semiconductor Corporation
09/775,488	6462602	United States	Voltage Level Translator Systems And Methods	Issued	Lattice Semiconductor Corporation
09/775,489	6414521	United States	Improved sense amplifier systems and methods	Issued	Lattice Semiconductor Corporation
09/818,257	6496969	United States	Programming Programmable Logic Devices Using Hidden Switches	Issued	Lattice Semiconductor Corporation
09/841,209	6590415	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/863,656	6535043	United States	Clock Signal Selection System, Method of Generating A Clock Signal And Programmable Clock Manager Including Same	Issued	Lattice Semiconductor Corporation
09/864,276	6486705	United States	Signal Distribution Scheme In Field Programmable Gate Array (FPGA) or Field Programmable Systems Chip (FPSC) Including Cycle Stealing Units	Issued	Lattice Semiconductor Corporation
09/864,284	6472904	United States	Double Data Rate Input And Output In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/864,289	6480026	United States	Multi-functional I/O Buffers In a Field Programmable Gate	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Array (FPGA)		Corporation
09/864,277	6483342	United States	Multi-Master Multi-Slave Bus In Field Programmable Gate Array (FPGA)	Issued	Lattice Semiconductor Corporation
09/864,290	6772230	United States	Field Programmable Gate Array (FPGA) Bit Stream Format	Issued	Lattice Semiconductor Corporation
09/870,877	6498538	United States	Low Jitter Integrated Phase Locked Loop With Broad Tuning Range	Issued	Lattice Semiconductor Corporation
09/870,541	6455375	United States	EEPROM tunnel window for program injection via P+ contacted inversion	Issued	Lattice Semiconductor Corporation
09/881,950	6614291	United States	Low Voltage, High Speed CMOS CML Latch and MUX Devices	Issued	Lattice Semiconductor Corporation
09/885,243	6429692	United States	High Speed Data Sampling With Reduced Metastability	Issued	Lattice Semiconductor Corporation
09/927,289	6492877	United States	Improved Coupling For LC-Based VCO	Issued	Lattice Semiconductor Corporation
09/927,612	6525617	United States	Buffering For LC-Based Stage	Issued	Lattice Semiconductor Corporation
09/927,793	6653860	United States	Enhanced logic macrocell with expanded PT (product term) sharing capability for Use in High Density CPLD Architectures	Issued	Lattice Semiconductor Corporation
09/941,454	6489835	United States	Low Voltage Bandgap Reference Circuit	Issued	Lattice Semiconductor Corporation
09/949,112	6593222	United States	Method to improve the reliability of thermosonic gold to aluminum wire bonds	Issued	Lattice Semiconductor Corporation
09/966,967	6832231	United States	Multiple Width Random Number Generation	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/011,549	6693830	United States	Single Poly Two-Transistor EEPROM Cell With Differentially Doped Floating Gate	Issued	Lattice Semiconductor Corporation
10/053,004	6989551	United States	Test structure for determining the minimum tunnel opening size in a non-volatile memory cell	Issued	Lattice Semiconductor Corporation
10/010,011	6515899	United States	Non-Volatile Memory Cell With Enhanced Cell Drive Current	Issued	Lattice Semiconductor Corporation
09/991,245	6611463	United States	Zero Power Programmable Memory Cell	Issued	Lattice Semiconductor Corporation
09/992,493	6489806	United States	Zero power logic cell for use in programmable logic devices	Issued	Lattice Semiconductor Corporation
10/006,559	7003066	United States	Digital Phase locked Loop with Phase Selector having Minimized Number of Phase Interpolators	Issued	Lattice Semiconductor Corporation
10/006,610	6999543	United States	Clock Data Recovery Deserializer With Programmable Sync Detect Logic	Issued	Lattice Semiconductor Corporation
10/006,516	6993108	United States	Digital Phase Locked Loop With Programmable Digital Filter	Issued	Lattice Semiconductor Corporation
10/021,873	6661254	United States	Programmable Interconnect Circuit With A Phase-Locked Loop	Issued	Lattice Semiconductor Corporation
10/017,725	6674303	United States	Programmable I/O cell with bidirectional and shift register capabilities	Issued	Lattice Semiconductor Corporation
10/017,859	6605959	United States	Structure and Method for Implementing Wide Multiplexers	Issued	Lattice Semiconductor Corporation
10/022,464	7154298	United States	Block oriented architecture for programmable interconnect circuit	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/021,844	6703860	United States	I/O Block for Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/023,053	6653861	United States	Multi-level Routing Structure for a Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/023,226	6650141	United States	High Speed Interface For a Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/059,624	6636442	United States	Non-volatile memory element having a cascoded transistor scheme to reduce oxide field stress	Issued	Lattice Semiconductor Corporation
10/061,057	6845044	United States	Method of preventing high Icc at start-up in zero-power EEPROM cells for PLD applications	Issued	Lattice Semiconductor Corporation
10/066,031	6680625	United States	Symmetrical CML Logic Gate System	Issued	Lattice Semiconductor Corporation
10/082,050	6781170	United States	Integrated Circuit Base Transistor Structure And Associated Programmable Cell Library	Issued	Lattice Semiconductor Corporation
10/083,728	6600188	United States	An EEPROM with neutralized doping at tunnel window edge	Issued	Lattice Semiconductor Corporation
10/090,209	6621298	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
10/103,100	6795959	United States	Integrated Delay Discriminator For Use With a Field- Programmable Gate Array and A Method of Determining a Time Delay Thereof	Issued	Lattice Semiconductor Corporation
10/106,509	6907439	United States	FFT address generation method and apparatus	Issued	Lattice Semiconductor Corporation
10/108,401	6976047	United States	Skipped carry incrementer for FFT address generation	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/112,370	6639431	United States	Differential Input Comparator	Issued	Lattice Semiconductor Corporation
10/128,943	6660579	United States	Zero Power Memory Cell With Improved Data Retention	Issued	Lattice Semiconductor Corporation
10/131,883	7032162	United States	Polynomial Expander for Generating Coefficients of a Polynomial from Roots of the Polynomial	Issued	Lattice Semiconductor Corporation
10/133,016	6765408	United States	Device and Method with Generic Logic Blocks	Issued	Lattice Semiconductor Corporation
10/135,308	6814296	United States	Integrated Circuit and Associated Design Method With Antenna Error Control Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/135,325	6600341	United States	Integrated Circuit and Associated Design Method Using Spare Gate Islands	Issued	Lattice Semiconductor Corporation
10/146,739	6714048	United States	Input Buffer With Selectable PCL, GTL, or PECL Compatibility	Issued	Lattice Semiconductor Corporation
10/146,826	6657458	United States	Output Buffer With Feedback From An Input Buffer To Provide Selectable PCL, GTL, or PECL Compatability	Issued	Lattice Semiconductor Corporation
10/146,769	6870391	United States	Input Buffer With CMOS Driver Gate Current Control Enabling Selectable PCL, GTL, or PECL Compatibility	Issued	Lattice Semiconductor Corporation
10/147,199	6714043	United States	Output Buffer Having Programmable Drive Current And Output Voltage Limits	Issued	Lattice Semiconductor Corporation
10/146,734	6720755	United States	Band Gap Reference Circuit	Issued	Lattice Semiconductor Corporation
10/147,011	6760209	United States	Electrostatic Discharge Protection Circuit	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/151,753	6798244	United States	Output Buffer With Overvoltage Protection	Issued	Lattice Semiconductor Corporation
10/150,410	6848095	United States	Method of Assigning Logic Functions To Macrocells In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/159,009	6583652	United States	Highly linear programmable transconductor with large input-signal range	Issued	Lattice Semiconductor Corporation
10/159,089	6717451	United States	Precision analog level shifter with programmable options	Issued	Lattice Semiconductor Corporation
10/159,681	6806771	United States	Multimode output stage converting differential to single-ended signals using current-mode input signals	Issued	Lattice Semiconductor Corporation
10/162,337	6596587	United States	Shallow junction EEPROM Device and Process for Fabricating the Device	Issued	Lattice Semiconductor Corporation
10/160,855	6794236	United States	EEPROM Device with Improved Capacitive Coupling and Fabrication Process	Issued	Lattice Semiconductor Corporation
10/161,283	6716705	United States	EEPROM Device having a Retrograde Program Junction Region And Process for Fabrication the Device	Issued	Lattice Semiconductor Corporation
10/164,484	6703305	United States	Semiconductor Device Having Metallized Interconnect Structure And Method Of Fabricaton	Issued	Lattice Semiconductor Corporation
10/187,236	6844757	United States	Converting Bits to Vectors In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/191,888	6650143	United States	FPGA Based Upon Transistor gate Oxide Breakdown	Issued	Lattice Semiconductor Corporation
10/194,771	7028281	United States	FPGA With Register-Intensive Architecture	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/200,645	6714066	United States	Integrated Programmable Continuous Time Filter with Programmable Capacitor Arrays	Issued	Lattice Semiconductor Corporation
10/207,292	6683477	United States	Wide input programmable logic system and method	Issued	Lattice Semiconductor Corporation
10/210,367	6938197	United States	CRC Calculation System And Method For A Packet Arriving On An N-Byte Wide Bus	Issued	Lattice Semiconductor Corporation
10/211,125	6545313	United States	EEPROM tunnel window for program injection via P+ contacted inversion	Issued	Lattice Semiconductor Corporation
10/219,046	6650142	United States	Enhanced CPLD Macrocell Module Having Selectable Bypass of Steering-based Resource Allocation and Methods of Use	Issued	Lattice Semiconductor Corporation
10/233,021	7043511	United States	Performing Conditional Operations In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/232,912	6841447	United States	EEPROM Device Having An Isolation -Bounded Tunnel Capacitor And Fabrication Process	Issued	Lattice Semiconductor Corporation
10/235,380	6725442	United States	Scalable and parallel processing methods and structures for testing configurable interconnect network in FPGA device	Issued	Lattice Semiconductor Corporation
10/236,829	6842372	United States	EEPROM Cell Having Floating Gate Transistor Within a Cell Well And a Process For Fabricating the Memory Cell	Issued	Lattice Semiconductor Corporation
10/236,114	6833602	United States	Device Having Electrically Isolated Low Voltage And High Voltage Regions And Process For Fabricating the Device	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/236,718	6649514	United States	EEPROM Device Having Improved Data Retention And Process for Fabricating The Device	Issued	Lattice Semiconductor Corporation
10/242,809	6738306	United States	Multiport SRAM Cell	Issued	Lattice Semiconductor Corporation
10/243,014	6917536	United States	Memory access Circuit and Method for reading and writing data with the same clock signal	Issued	Lattice Semiconductor Corporation
10/251,608	6700154	United States	EEPROM cell with trench coupling capacitor	Issued	Lattice Semiconductor Corporation
10/255,474	6907592	United States	Method of Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,875	6809551	United States	Method of Optimizing Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,499	6803787	United States	State Machine In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,656	6812738	United States	Vector Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/263,251	6748575	United States	Programming Programmable Logic Devices Using Hidden Switches	Issued	Lattice Semiconductor Corporation
10/263,507	6846714	United States	Voltage Limted EEPROM Device And Process For Fabricating the Device	Issued	Lattice Semiconductor Corporation
10/266,361	6639434	United States	Low voltage differential signaling systems and methods	Issued	Lattice Semiconductor Corporation
10/269,804	7111183	United States	Expansion method for complex power-sequencing applications	Issued	Lattice Semiconductor Corporation
10/269,450	6791394	United States	Power Supply Control Circuits	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/269,439	6762618	United States	Innovative verify scheme for two level GRP fuse in programmable bus switching family	Issued	Lattice Semiconductor Corporation
10/272,582	6901572	United States	Power Sequence Controller Programming Technique	Issued	Lattice Semiconductor Corporation
10/278,415	6639449	United States	Asynchronous glitch-free clock multiplexer	Issued	Lattice Semiconductor Corporation
10/282,524	7051261	United States	Turbo Encoder With Reduced Processing Delay	Issued	Lattice Semiconductor Corporation
10/283,765	6700823	United States	Programmable common mode termination for differential input/output circuits	Issued	Lattice Semiconductor Corporation
10/288,667	7000210	United States	Adaptive Adjustment Of Constraints During PLD Placement Processing	Issued	Lattice Semiconductor Corporation
10/288,668	6813754	United States	Placement Processing For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/300,190	6825733	United States	Low Jitter Integrated Phase Locked Loop With Broad Tuning Range	Issued	Lattice Semiconductor Corporation
10/302,439	6797568	United States	Flash Technology Transistors and Method For Forming Same	Issued	Lattice Semiconductor Corporation
10/308,420	6710641	United States	Low Voltage Bandgap Reference Circuit	Issued	Lattice Semiconductor Corporation
10/309,302	6650188	United States	Improved Coupling For LC-Based VCO	Issued	Lattice Semiconductor Corporation
10/334,642	6777979	United States	FIFO memory architecture	Issued	Lattice Semiconductor Corporation
10/338,619	6753696	United States	Programmable optimized-distribution logic allocator for	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			a high-density complex PLD		Corporation
10/365,083	7034596	United States	Adaptive input logic for phase adjustments	Issued	Lattice Semiconductor Corporation
10/368,023	6915323	United States	Macrocells Supporting A Carry Cascade	Issued	Lattice Semiconductor Corporation
10/366,956	6788101	United States	Programmable input buffer for differential and single-ended signals	Issued	Lattice Semiconductor Corporation
10/367,323	6812869	United States	Noise Reduction Techniques For Programmable I/O Circuits	Issued	Lattice Semiconductor Corporation
10/370,232	6861870	United States	Dynamic Cross point Switch With Shadow Memory Architecture	Issued	Lattice Semiconductor Corporation
10/377,320	6859066	United States	Bank based input/output buffers in field programmable gate arrays with multiple reference voltages	Issued	Lattice Semiconductor Corporation
10/387,814	7305047	United States	Automatic lane assignment for Receiver	Issued	Lattice Semiconductor Corporation
10/387,243	7339952	United States	Pointer Processing For Optical Communication Systems	Issued	Lattice Semiconductor Corporation
10/391,094	6870395	United States	PLDs With Integrated Standard Cell Logic Blocks	Issued	Lattice Semiconductor Corporation
10/392,751	RE39510	United States	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	Issued	Lattice Semiconductor Corporation
10/397,669	6967500	United States	Electronic Circuit With OnChip Programmable Terminations	Issued	Lattice Semiconductor Corporation
10/400,705	6873187	United States	Method and Apparatus for Controlling Signal Distribution In An Electronic	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Circuit		
10/406,050	7000212	United States	Hierarchical General Interconnect Architecture For High Density FPGA's	Issued	Lattice Semiconductor Corporation
10/409,543	6986004	United States	FIFO memory with programmable data port widths	Issued	Lattice Semiconductor Corporation
10/417,290	6879184	United States	Programmable logic device architecture based on arrays of LUT-based Boolean terms	Issued	Lattice Semiconductor Corporation
10/425,863	6903575	United States	Scalable device architecture for high-speed interfaces	Issued	Lattice Semiconductor Corporation
10/425,862	6894530	United States	Programmable And Fixed Logic Circuitry For High-Speed Interfaces	Issued	Lattice Semiconductor Corporation
10/428,889	6879182	United States	CPLD with multi-function blocks and distributed memory	Issued	Lattice Semiconductor Corporation
10/428,885	6861871	United States	Cascaded logic block architecture for complex programmable logic devices	Issued	Lattice Semiconductor Corporation
10/428,888	6864713	United States	Multi-Stage Interconnect Architecture For Complex Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/428,982	6922078	United States	Enhanced wide and deep logic capability for high density, high performance CPLDs	Issued	Lattice Semiconductor Corporation
10/439,602	6828823	United States	Non-volatilie and reconfigurable PLDs	Issued	Lattice Semiconductor Corporation
10/441,814	7039842	United States	Measuring Propagation Delays of Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/447,120	7301996	United States	skew cancellation for source synchronous clock and data signals	Issued	Lattice Semiconductor Corporation
10/447,451	7009433	United States	Digitally Controlled Delay Cells	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/457,630	7304863	United States	Integrated Circuit Including External Electronic Components With Low Insertion Loss	Issued	Lattice Semiconductor Corporation
10/459,091	6879598	United States	Flexible Media Access Control Architecture	Issued	Lattice Semiconductor Corporation
10/460,385	6856171	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
10/463,781	6861868	United States	High Speed Interface For A Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/464,083	6882555	United States	Bi-directional buffering for memory data lines	Issued	Lattice Semiconductor Corporation
10/600,042	6822477	United States	Integrated Circuit And Associated Design Method Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/610,253	6977408	United States	High-Performance Non-volatile Memory Device and Fabrication Process	Issued	Lattice Semiconductor Corporation
10/613,460	7132903	United States	Noise-shielding, switch-controlled load circuitry for oscillators and the like	Issued	Lattice Semiconductor Corporation
10/613,462	6952115	United States	Programmable I/O Interfaces For FPGAs And Other PLDs	Issued	Lattice Semiconductor Corporation
10/617,980	6958625	United States	PLD With Hardwired Microsequencer	Issued	Lattice Semiconductor Corporation
10/619,711	6903573	United States	Programmable Logic Device With Enhanced Wide Input Product Term Cascading	Issued	Lattice Semiconductor Corporation
10/620,286	6919736	United States	FPGA having partitionable embedded memory with configurable depth and width	Issued	Lattice Semiconductor Corporation
10/619,645	7098685	United States	Scalable Serializer-Deserializer Architecture and	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Programmable Interface		Corporation
10/620,147	7032203	United States	Algorithm to increase logic input width by cascading product terms	Issued	Lattice Semiconductor Corporation
10/624,965	6940309	United States	Programmable Logic Device With A Memory-Based Finite State Machine	Issued	Lattice Semiconductor Corporation
10/626,089	6737702	United States	Zero Power Memory Cell with Reduced Threshold Voltage	Issued	Lattice Semiconductor Corporation
10/628,656	6970047	United States	Programmable lock detector and corrector	Issued	Lattice Semiconductor Corporation
10/628,657	6924659	United States	Programmable Signal Termination for FPGAs and the Like	Issued	Lattice Semiconductor Corporation
10/629,223	7019577	United States	Clock Generator	Issued	Lattice Semiconductor Corporation
10/629,512	6903574	United States	Memory Access Via Serial Memory Interface	Issued	Lattice Semiconductor Corporation
10/629,221	6885227	United States	Clock Generator With Skew Control	Issued	Lattice Semiconductor Corporation
10/640,804	6877667	United States	Integrated Circuit And Associated Design Method With Antenna Error Control Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/640,828	6838904	United States	Enhanced CPLD Macrocell Module Having Selectable Bypass of Steering-Based Resource Allocation	Issued	Lattice Semiconductor Corporation
10/641,260	6940779	United States	Programmable broadcasting initialization of embedded memory blocks on FPGA	Issued	Lattice Semiconductor Corporation
10/642,370	6924664	United States	FPGA	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/655,686	6842037	United States	Shared Transmission Line Communication System and Method	Issued	Lattice Semiconductor Corporation
10/660,814	7038490	United States	Delay matched ASIC conversion of a PLD	Issued	Lattice Semiconductor Corporation
10/665,920	6970022	United States	Controlled hysteresis comparator with rail-to-rail input	Issued	Lattice Semiconductor Corporation
10/671,378	6943583	United States	Programmable I/O structure for FPGAs and the like having reduced pad capacitance	Issued	Lattice Semiconductor Corporation
10/671,363	6943582	United States	Programmable I/O structure for FPGAs and the Like Having Shared Circuitry	Issued	Lattice Semiconductor Corporation
10/671,756	6909663	United States	Multiport Memory With Twisted Bitlines	Issued	Lattice Semiconductor Corporation
10/676,536	7269771	United States	Semiconductor Device Adapted For Forming Multiple Scan Chains	Issued	Lattice Semiconductor Corporation
10/687,468	6809674	United States	Analog-to-digital converters	Issued	Lattice Semiconductor Corporation
10/699,321	7067883	United States	Lateral High-Voltage Junction Device	Issued	Lattice Semiconductor Corporation
10/701,005	7091763	United States	Clock generation	Issued	Lattice Semiconductor Corporation
10/704,025	7088134	United States	PLD With Flexible Memory Allocation And Routing	Issued	Lattice Semiconductor Corporation
10/726,972	7100058	United States	Programmable Power Management System And Method	Issued	Lattice Semiconductor Corporation
10/728,685	7187157	United States	Power supply remote voltage sensing	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/737,514	6981381	United States	Linear Thermoelectric Device Driver	Issued	Lattice Semiconductor Corporation
10/744,353	7132864	United States	Method for configuring multiple-output phase-locked loop frequency synthesizer	Issued	Lattice Semiconductor Corporation
10/769,174	7024646	United States	Electrostatic Discharge Simulation	Issued	Lattice Semiconductor Corporation
10/768,643	7019584	United States	Output Stages For High Current Low Noise Bandgap Reference Circuit Implementations	Issued	Lattice Semiconductor Corporation
10/782,564	6972986	United States	Combination FPGA	Issued	Lattice Semiconductor Corporation
10/783,886	7081771	United States	Upgradeable And Reconfigurable Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/791,073	7191388	United States	Fast diagonal interleaved parity (DIP) calculator	Issued	Lattice Semiconductor Corporation
10/794,079	7257727	United States	Timer Systems and Methods	Issued	Lattice Semiconductor Corporation
10/794,524	7017063	United States	systems and methods for controlling voltage regulator module power supplies	Issued	Lattice Semiconductor Corporation
10/794,498	7028201	United States	Powering up a device having digital and analog circuitry	Issued	Lattice Semiconductor Corporation
10/797,759	7068556	United States	Sense Amplifier Systems and Methods	Issued	Lattice Semiconductor Corporation
10/809,180	7234030	United States	Table based scheduler for FIFOs and the like	Issued	Lattice Semiconductor Corporation
10/809,658	7095247	United States	Configuring FPGAs and the like using one or more serial memory devices	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/815,403	7167032	United States	Self-adjusting schmitt trigger	Issued	Lattice Semiconductor Corporation
10/817,215	7081781	United States	Charge pump for a low-voltage wide-tuning range phase-locked loop	Issued	Lattice Semiconductor Corporation
10/829,865	6998896	United States	Dynamic gain adjustment systems and method for metastability resistance	Issued	Lattice Semiconductor Corporation
10/834,528	6998906	United States	Low pass filter systems and methods	Issued	Lattice Semiconductor Corporation
10/837,086	7307319	United States	High Voltage Protection Device And Process	Issued	Lattice Semiconductor Corporation
10/842,345	7002418	United States	Control Signal Generation ...	Issued	Lattice Semiconductor Corporation
10/841,987	7224213	United States	switched-capacitor ripple-smoothing filter	Issued	Lattice Semiconductor Corporation
10/843,708	7061269	United States	IO buffer architecture for programmable devices	Issued	Lattice Semiconductor Corporation
10/856,100	7196551	United States	Current Mode Logic Buffer	Issued	Lattice Semiconductor Corporation
10/857,667	7064973	United States	Combination FPGA	Issued	Lattice Semiconductor Corporation
10/885,419	7116585	United States	Memory Systems And Methods	Issued	Lattice Semiconductor Corporation
10/910,091	7215591	United States	Byte enable logic for memory	Issued	Lattice Semiconductor Corporation
10/912,943	7471752	United States	Data Transmission Synchronization	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/928,563	7078286	United States	Process for fabricating a semiconductor device having electrically isolated low voltage and high voltage regions	Issued	Lattice Semiconductor Corporation
10/929,199	7484144	United States	Testing embedded memory in an integrated circuit	Issued	Lattice Semiconductor Corporation
10/944,978	7135886	United States	FPGA Using Both Volatile and NonVolatile Memory Cell Properties	Issued	Lattice Semiconductor Corporation
10/974,453	7307912	United States	Variable data width memory systems and methods	Issued	Lattice Semiconductor Corporation
10/973,750	7149129	United States	memory output data systems and methods with feedback	Issued	Lattice Semiconductor Corporation
10/974,107	7164290	United States	FPGA Logic Unit	Issued	Lattice Semiconductor Corporation
10/974,305	7129749	United States	PLD Having A Configurable DRAM With Transparent Refresh	Issued	Lattice Semiconductor Corporation
10/978,899	7376872	United States	Testing embedded memory in integrated circuits such as progammable logic circuits	Issued	Lattice Semiconductor Corporation
10/996,283	7161862	United States	Low power asynchronous sense amp	Issued	Lattice Semiconductor Corporation
11/007,954	7230810	United States	Dynamic over-voltage protection scheme for integrated circuit devices	Issued	Lattice Semiconductor Corporation
11/012,550	7215149	United States	Interface circuitry for electrical systems	Issued	Lattice Semiconductor Corporation
11/012,548	7215148	United States	Programmable current LVDS output buffer	Issued	Lattice Semiconductor Corporation
11/015,265	7177221	United States	Method of initializing configurable multi-port	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			embedded memory blocks in an FPGA		Corporation
11/016,665	7187203	United States	Cascadable memory	Issued	Lattice Semiconductor Corporation
11/015,369	7177207	United States	Sense amplifier timing	Issued	Lattice Semiconductor Corporation
11/036,630	7257750	United States	Self-verification of configuration memory in PLDs	Issued	Lattice Semiconductor Corporation
11/036,738	7242053	United States	EEPROM Device with voltage-limiting charge pump circuit	Issued	Lattice Semiconductor Corporation
11/040,772	7208975	United States	Serdes with programmable I/O architecture	Issued	Lattice Semiconductor Corporation
11/041,319	7183798	United States	Synchronous memory	Issued	Lattice Semiconductor Corporation
11/044,089	7109754	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
11/044,149	7109756	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
11/044,508	7034599	United States	Clock Generator With Skew Control	Issued	Lattice Semiconductor Corporation
11/054,011	7221607	United States	Mult-port memory systems and methods for bit line coupling	Issued	Lattice Semiconductor Corporation
11/055,280	6975137	United States	PLDs With Integrated Standard Cell Logic Blocks	Issued	Lattice Semiconductor Corporation
11/054,750	7382293	United States	Data Decompression	Issued	Lattice Semiconductor Corporation
11/054,855	7589648	United States	Data Decompression	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/064,477	7532646	United States	Distributed multiple channel alignment scheme	Issued	Lattice Semiconductor Corporation
11/071,356	7245154	United States	Differential Input Receiver with Programmable Failsafe	Issued	Lattice Semiconductor Corporation
11/070,926	7057397	United States	Output Impedance Measurement Techniques	Issued	Lattice Semiconductor Corporation
11/083,625	7376204	United States	Detection of Unknown symbol rate in a digitally modulated signal	Issued	Lattice Semiconductor Corporation
11/098,713	7265578	United States	In-System Programming Of a Non-Compliant Device Using Multiple Interfaces Of A PLD	Issued	Lattice Semiconductor Corporation
11/100,718	7397274	United States	In-System Programming Of a Non-Compliant Device Using Multiple Interfaces Of A PLD	Issued	Lattice Semiconductor Corporation
11/108,927	7193436	United States	Fast Processing Path Using FPGA Logic Units	Issued	Lattice Semiconductor Corporation
11/109,301	7630464	United States	Analog-to-digital systems and methods	Issued	Lattice Semiconductor Corporation
11/109,966	6977521	United States	FPGA	Issued	Lattice Semiconductor Corporation
11/121,326	7400171	United States	Electronic Switch Having Extended Voltage Range	Issued	Lattice Semiconductor Corporation
11/134,152	7009423	United States	Programmable I/O Interfaces For FPGAs And Other PLDs	Issued	Lattice Semiconductor Corporation
11/157,345	7685483	United States	Design-For-Test features for a memory in an FPGA	Issued	Lattice Semiconductor Corporation
11/157,349	7378879	United States	Decoding systems and methods	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/165,709	7256613	United States	Programmable Interconnect Architecture for PLDs	Issued	Lattice Semiconductor Corporation
11/165,853	7342838	United States	PLD With A Double Data Rate SDRAM Interface	Issued	Lattice Semiconductor Corporation
11/185,242	7519139	United States	Signal monitoring systems and methods	Issued	Lattice Semiconductor Corporation
11/187,179	7342846	United States	address decoding systems and methods	Issued	Lattice Semiconductor Corporation
11/187,114	7253674	United States	Fine output clock phase alignment circuitry	Issued	Lattice Semiconductor Corporation
11/189,067	7505752	United States	Receiver used for differential signaling and reference voltage signaling with programmable common mode	Issued	Lattice Semiconductor Corporation
11/194,871	7414913	United States	Bitline twisting scheme for a multiport memory	Issued	Lattice Semiconductor Corporation
11/194,356	7262630	United States	Dynamic programmable termination for parallel and differential schemes	Issued	Lattice Semiconductor Corporation
11/199,287	7599457	United States	clock-and-data-recovery system having a multi-phase clock generator for one or more channel circuits	Issued	Lattice Semiconductor Corporation
11/200,983	7295035	United States	Programmable Logic Device With Enhanced Logic Block Architecture	Issued	Lattice Semiconductor Corporation
11/200,941	7411419	United States	I/O Systems and Methods	Issued	Lattice Semiconductor Corporation
11/202,149	7606851	United States	Correlator having user-defined processing	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/201,620	7187586	United States	Flash memory erase verification systems and methods	Issued	Lattice Semiconductor Corporation
11/206,282	RE40311	United States	Zero Power Programmable Memory Cell	Issued	Lattice Semiconductor Corporation
11/226,695	7301182	United States	Circuit layout for improved performance while preserving or improving density	Issued	Lattice Semiconductor Corporation
11/230,087	7167405	United States	Data transfer verification systems and methods	Issued	Lattice Semiconductor Corporation
11/235,616	7376037	United States	PLD with power-saving architecture	Issued	Lattice Semiconductor Corporation
11/236,967	7405446	United States	Electrostatic Protection Systems and Methods	Issued	Lattice Semiconductor Corporation
11/243,255	7088132	United States	Configuring FPGAs and the like using one or more serial memory devices	Issued	Lattice Semiconductor Corporation
11/251,682	7196963	United States	Address isolation for user-defined configuration memory in programmable devices	Issued	Lattice Semiconductor Corporation
11/252,094	7263024	United States	Clock reset address decoder for block memory	Issued	Lattice Semiconductor Corporation
11/252,126	7061275	United States	FPGA	Issued	Lattice Semiconductor Corporation
11/257,137	7685215	United States	Fast-carry arithmetic circuit using a multi-input LUT	Issued	Lattice Semiconductor Corporation
11/257,641	7317343	United States	PULSE-GENERATION CIRCUIT HAVING PULSE GENERATORS AND SET-RESET LATCHES	Issued	Lattice Semiconductor Corporation
11/260,097	7212051	United States	Control signal generation for a low jitter switched-capacitor frequency synthesizer	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/281,651	7495495	United States	Digital I/O Timing Control	Issued	Lattice Semiconductor Corporation
11/287,720	7327159	United States	Interface Block Architectures	Issued	Lattice Semiconductor Corporation
11/290,205	7242634	United States	Pseudo-dynamic word-line driver	Issued	Lattice Semiconductor Corporation
11/293,941	7538574	United States	Transparent Field Reconfiguration for PLDs	Issued	Lattice Semiconductor Corporation
11/302,097	7620839	United States	Jitter Tolerant Delay-Locked Loop Circuit	Issued	Lattice Semiconductor Corporation
11/300,886	7495467	United States	Temperature independent, linear on-chip termination resistance	Issued	Lattice Semiconductor Corporation
11/332,986	7382169	United States	Systems and Methods for Reducing Static Phase Error	Issued	Lattice Semiconductor Corporation
11/335,890	7439783	United States	Phase-Locked Loop Systems And Methods	Issued	Lattice Semiconductor Corporation
11/345,713	7547995	United States	dynamic over voltage protection scheme for interface circuitry	Issued	Lattice Semiconductor Corporation
11/346,817	7554357	United States	Efficient Configuration of Daisy-Chained Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
11/350,436	7375549	United States	Reconfiguration of PLDs	Issued	Lattice Semiconductor Corporation
11/356,805	7277348	United States	Memory Cell Comprising And OTP NV Memory Unit And SRAM Unit	Issued	Lattice Semiconductor Corporation
11/360,337	7355441	United States	PLD with distributed memory and non-volatile memory	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/361,584	7596744	United States	Auto recovery from volatile soft error upsets (SEUs)	Issued	Lattice Semiconductor Corporation
11/362,289	7759926	United States	dynamic phase offset measurement	Issued	Lattice Semiconductor Corporation
11/361,643	7446573	United States	Comparator Systems And Methods	Issued	Lattice Semiconductor Corporation
11/398,437	7459931	United States	PLDs with transparent field reconfiguration	Issued	Lattice Semiconductor Corporation
11/397,985	7554358	United States	PLDs with user non-volatile memory	Issued	Lattice Semiconductor Corporation
11/416,881	7623378	United States	Selective programming of non-volatile memory facilitated by security fuses	Issued	Lattice Semiconductor Corporation
11/435,956	7102934	United States	Sense Amplifier Systems and Methods	Issued	Lattice Semiconductor Corporation
11/442,186	7411417	United States	Selective loading of configuration data into configuration memory cells	Issued	Lattice Semiconductor Corporation
11/446,548	7378873	United States	PLD providing a serial peripheral interface	Issued	Lattice Semiconductor Corporation
11/445,620	7378872	United States	PLD architecture with multiple slice types	Issued	Lattice Semiconductor Corporation
11/446,542	7385417	United States	Dual slice architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/446,351	7397276	United States	Logic block control architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/446,308	7546498	United States	PLDs with custom identification systems and methods	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/446,309	7495970	United States	Flexible memory architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/447,591	7631223	United States	PLD methods and systems for providing multi-boot configuration data support	Issued	Lattice Semiconductor Corporation
11/452,714	7463060	United States	PLD and method of testing	Issued	Lattice Semiconductor Corporation
11/455,315	7215139	United States	Upgradeable And Reconfigurable Programmable Logic Device	Issued	Lattice Semiconductor Corporation
11/425,273	7702100	United States	Key generation for advanced encryption standard (AES) decryption and the like	Issued	Lattice Semiconductor Corporation
11/425,881	7657773	United States	Clock distribution chip for generating both zero-delay and non-zero-delay clock signals	Issued	Lattice Semiconductor Corporation
11/477,759	7348914	United States	Methods and systems to align output signals of an analog-to-digital converter	Issued	Lattice Semiconductor Corporation
11/487,647	7636259	United States	Flash memory array with independently erasable sectors	Issued	Lattice Semiconductor Corporation
11/487,751	7512015	United States	Negative voltage blocking for embedded memories	Issued	Lattice Semiconductor Corporation
11/492,687	7466190	United States	Charge pump with four-well transistors	Issued	Lattice Semiconductor Corporation
11/494,862	7521969	United States	Switch sequencing circuit systems and methods	Issued	Lattice Semiconductor Corporation
11/461,222	7411432	United States	Integrated circuits and complementary CMOS circuits for frequency dividers	Issued	Lattice Semiconductor Corporation
11/498,645	7675313	United States	Methods and systems for storing a security key using programmable fuses	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/498,646	7605606	United States	Area efficient routing architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/530,620	7456672	United States	Clock systems and methods	Issued	Lattice Semiconductor Corporation
11/533,188	7511641	United States	Efficient bitstream compression	Issued	Lattice Semiconductor Corporation
11/551,459	7831754	United States	Multiple Communication Channel Configuration Systems And Methods	Issued	Lattice Semiconductor Corporation
11/556,528	7663401	United States	Multiplexer initialization systems and methods	Issued	Lattice Semiconductor Corporation
11/593,274	7535258	United States	Programmable Voltage LVDS Output Buffer	Issued	Lattice Semiconductor Corporation
11/557,808	7725803	United States	PLD programming verification systems and methods	Issued	Lattice Semiconductor Corporation
11/638,156	7429875	United States	Low Static Current Drain Logic Circuit	Issued	Lattice Semiconductor Corporation
11/643,288	7443192	United States	Output buffer with digital slew control	Issued	Lattice Semiconductor Corporation
11/624,021	7623391	United States	Data transfer verification systems and methods	Issued	Lattice Semiconductor Corporation
11/671,948	7576563	United States	Flexible High Fan-out Signal Routing Systems and Methods	Issued	Lattice Semiconductor Corporation
11/675,246	7313025	United States	Flash memory erase verification systems and methods	Issued	Lattice Semiconductor Corporation
11/676,071	7430706	United States	Fast diagonal interleaved parity (DIP) calculator	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/680,526	7598765	United States	Redundancy for Configuration RAM	Issued	Lattice Semiconductor Corporation
11/691,003	7536615	United States	Logic analyzer systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/691,040	7743296	United States	Logic analyzer systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/737,702	7509598	United States	Clock Boosting Systems and Methods	Issued	Lattice Semiconductor Corporation
11/750,790	7401280	United States	Self-verification of configuration memory in PLDs	Issued	Lattice Semiconductor Corporation
11/750,616	7632011	United States	Integrated Circuit Temperature Sensors Systems and Methods	Issued	Lattice Semiconductor Corporation
11/760,411	8065574	United States	Real Soft Error Detect Scheme for Testing	Issued	Lattice Semiconductor Corporation
11/761,221	7570078	United States	PLD Providing A Serial Peripheral Interfaces	Issued	Lattice Semiconductor Corporation
11/778,457	7573770	United States	Distributed front-end FIFO for source-synchronized interfaces with non-continuous clocks	Issued	Lattice Semiconductor Corporation
11/779,246	7446679	United States	FPGA data compression using combined RLE BE, LZ, Row LZ and BE ROW encoding	Issued	Lattice Semiconductor Corporation
11/863,016	7681160	United States	Weight based look up table collapsing for programmable logic devices	Issued	Lattice Semiconductor Corporation
11/865,556	7539076	United States	Variable data width memory systems and methods	Issued	Lattice Semiconductor Corporation
11/869,019	7616029	United States	Hysteresis-based processing for applications such as signal bias monitors	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/872,950	7586344	United States	Dynamic delay or advance adjustment of oscillating signal phase	Issued	Lattice Semiconductor Corporation
11/875,748	7757198	United States	Scan chain systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/877,434	7411414	United States	Single-Ended Output Driver Buffer	Issued	Lattice Semiconductor Corporation
11/924,088	8132040	United States	Channel-to-channel deskew systems and methods	Issued	Lattice Semiconductor Corporation
11/934,711	7573291	United States	Programmable Logic Device With Enhanced Logic Block Architecture	Issued	Lattice Semiconductor Corporation
11/937,328	7788620	United States	An IO placement systems and methods to reduce SSO noise	Issued	Lattice Semiconductor Corporation
11/937,300	7895555	United States	Simultaneous Switching Output Noise Estimation and Reduction Systems and Methods	Issued	Lattice Semiconductor Corporation
11/939,787	7863931	United States	Flexible Delay Cell Architecture	Issued	Lattice Semiconductor Corporation
11/941,031	7902865	United States	Compression and decompression of configuration data using repeated data frames	Issued	Lattice Semiconductor Corporation
11/941,006	7535253	United States	Method of Retaining Register Data during Field Update of PLD	Issued	Lattice Semiconductor Corporation
11/947,662	7788623	United States	Composite wire indexing for PLDs	Issued	Lattice Semiconductor Corporation
11/949,130	7586325	United States	IC having independent voltage and process/temperature control	Issued	Lattice Semiconductor Corporation
12/001,600	7728625	United States	Serial interface for PLDs	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/957,598	7605609	United States	A programmable level shifter optimized for high performance and low power.	Issued	Lattice Semiconductor Corporation
11/959,329	7630259	United States	PLD with built in self test	Issued	Lattice Semiconductor Corporation
11/970,212	7646643	United States	Process charging monitor for nonvolatile memory	Issued	Lattice Semiconductor Corporation
12/019,526	7787326	United States	PLD With Mult-Rate SDRAM Interface	Issued	Lattice Semiconductor Corporation
12/021,202	8069329	United States	Dynamic Multiple Pattern Configuration Scheme For Volatile FPGAs	Issued	Lattice Semiconductor Corporation
12/044,842	7652500	United States	Reconfiguration of PLDs	Issued	Lattice Semiconductor Corporation
12/055,170	7890913	United States	Wire Mapping For PLDs	Issued	Lattice Semiconductor Corporation
12/060,776	7459935	United States	PLD With Distributed Memory	Issued	Lattice Semiconductor Corporation
12/061,885	7831856	United States	Detection of Timing Errors in Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/099,933	7661878	United States	On-Chip Temperature Sensor For An Integrated Circuit	Issued	Lattice Semiconductor Corporation
12/100,859	7558143	United States	Programmable Logic Device With Power-Saving Architecture	Issued	Lattice Semiconductor Corporation
12/105,146	7557606	United States	Synchronization Of Data Signals And Clock Signals For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/105,959	7696784	United States	PLD With Multiple Slice	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Types		Corporation
12/107,883	7560953	United States	Power Management Systems And Methods for PLDs	Issued	Lattice Semiconductor Corporation
12/122,489	7897448	United States	Formation Of High Voltage Transistor With High Breakdown Voltage	Issued	Lattice Semiconductor Corporation
12/146,042	8463832	United States	Digital Signal Processing Block Architecture For PLD	Issued	Lattice Semiconductor Corporation
12/164,265	7592834	United States	Logic Block Control Architectures For PLDs	Issued	Lattice Semiconductor Corporation
12/182,940	8261160	United States	Serial data recovery out of 8 samples with FPGAs	Issued	Lattice Semiconductor Corporation
12/186,027	7579865	United States	Selective Loading Of Configuration Data Into Configuration Memory Cells	Issued	Lattice Semiconductor Corporation
12/188,120	7605602	United States	Low-Power Output Driver Buffer Circuit	Issued	Lattice Semiconductor Corporation
12/238,959	7911229	United States	Programmable Signal Routing Systems	Issued	Lattice Semiconductor Corporation
12/273,868	7663419	United States	Clock Systems And Methods	Issued	Lattice Semiconductor Corporation
12/277,217	8112731	United States	Congestion-driven placement based on region interconnection for FPGA	Issued	Lattice Semiconductor Corporation
12/323,974	7992120	United States	congestion estimation based on pass probability net estimation process	Issued	Lattice Semiconductor Corporation
12/327,128	7656193	United States	Programmable Logic Device And Method Of Testing	Issued	Lattice Semiconductor Corporation
12/337,502	8856718	United States	Precise Congestion Estimation for FPGA Router	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
12/341,929	8181139	United States	Multi-Priority Placement	Issued	Lattice Semiconductor Corporation
12/370,039	7714608	United States	Temperature-Independent, Linear On-Chip Termination Resistance	Issued	Lattice Semiconductor Corporation
12/389,149	7957208	United States	Flexible memory architectures for PLDs	Issued	Lattice Semiconductor Corporation
12/402,751	7844243	United States	Receiver used for differential signaling and reference voltage signaling with programmable common mode	Issued	Lattice Semiconductor Corporation
12/406,772	8069431	United States	An alternative method for pin swapping in FPGA routing	Issued	Lattice Semiconductor Corporation
12/408,047	8086986	United States	Clock Boosting Systems And Methods	Issued	Lattice Semiconductor Corporation
12/409,757	7675321	United States	Dual-Slice Architectures For PLDs	Issued	Lattice Semiconductor Corporation
12/413,787	7808405	United States	Efficient Bitstream Compression	Issued	Lattice Semiconductor Corporation
12/430,848	7741865	United States	Soft Error Upset Hardened Integrated Circuit Systems And Methods	Issued	Lattice Semiconductor Corporation
12/464,822	7876125	United States	Method of Retaining Register Data during Field Update of PLD	Issued	Lattice Semiconductor Corporation
12/465,444	7868654	United States	Economical way to improve volatile FPGA boot up data throughput by utilizing one or more SPI boot PROMs w/o sacrificing additional FPGA pins	Issued	Lattice Semiconductor Corporation
12/467,800	7737723	United States	Transparent Field Reconfiguration for PLDs	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
12/476,155	8044682	United States	FPGA Having Low Power, Fast Carry Chain	Issued	Lattice Semiconductor Corporation
12/480,565	7702977	United States	PLDs with custom identification systems and methods	Issued	Lattice Semiconductor Corporation
12/494,822	8165164	United States	Circuit For In-System Reconfigurable Mapping Of IQ Data Into A CPRI Basic Frame	Issued	Lattice Semiconductor Corporation
12/502,141	7724029	United States	Power Management For Integrated Circuits Such As Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/511,388	7768300	United States	PLD Providing A Serial Peripheral Interfaces	Issued	Lattice Semiconductor Corporation
12/512,944	8255733	United States	Method of selecting precise delay or skew shifts	Issued	Lattice Semiconductor Corporation
12/512,961	7969248	United States	VCO digital center frequency coarse tune algorithm	Issued	Lattice Semiconductor Corporation
12/538,810	7808855	United States	Distributed front-end FIFO for source-synchronized interfaces with non-continuous clocks	Issued	Lattice Semiconductor Corporation
12/561,140	8010871	United States	Auto recovery from volatile soft error upsets (SEUs)	Issued	Lattice Semiconductor Corporation
12/564,781	7746107	United States	Redundancy for Configuration RAM	Issued	Lattice Semiconductor Corporation
12/578,470	8122277	United States	Clock distribution chip	Issued	Lattice Semiconductor Corporation
12/578,492	8112656	United States	Clock distribution chip	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/607,868	7989911	United States	STI with trench liner of increased thickness	Issued	Lattice Semiconductor Corporation
12/607,333	7985656	United States	STI with trench liner of increased thickness	Issued	Lattice Semiconductor Corporation
12/611,262	8059470	United States	Flash memory array with independently erasable sectors	Issued	Lattice Semiconductor Corporation
12/626,289	7944765	United States	PLD with built in self test	Issued	Lattice Semiconductor Corporation
12/630,163	8060784	United States	PLD And Methods For Providing Multi-Boot Configuration Data Support	Issued	Lattice Semiconductor Corporation
12/637,884	8200179	United States	Combined Variable Gain Amplifier And Linear Equalizer With Independent Gain And Frequency Control	Issued	Lattice Semiconductor Corporation
12/698,283	8040152	United States	IO Ring Configuration Scheme with sharing of BC7 register	Issued	Lattice Semiconductor Corporation
12/706,227	7924054	United States	Latency measurement circuit for wireless communications applications	Issued	Lattice Semiconductor Corporation
12/709,685	7834652	United States	Methods and systems for storing a security key using programmable fuses	Issued	Lattice Semiconductor Corporation
12/729,952	8040159	United States	High Speed Comparator with Data Dependent Jitter Mitigation	Issued	Lattice Semiconductor Corporation
12/752,455	8384427	United States	Serial Peripheral Interface Daisy Chaining using a Flow-Through Option	Issued	Lattice Semiconductor Corporation
12/757,087	8664774	United States	A Method for Arranging IC Bondwires for the Reduction of Crosstalk	Issued	Lattice Semiconductor Corporation
12/786,359	8108754	United States	PLD programming verification systems and methods	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/813,540	8164499	United States	Shared-Array Multiple-Output Digital to Analog Converter	Issued	Lattice Semiconductor Corporation
12/813,573	8441292	United States	Method of delaying data from clock in 1UI steps	Issued	Lattice Semiconductor Corporation
12/818,544	7868646	United States	Soft Error Upset Hardened Integrated Circuit Systems And Methods	Issued	Lattice Semiconductor Corporation
12/871,764	8286116	United States	Composite Wire Indexing For PLDs	Issued	Lattice Semiconductor Corporation
12/977,011	8522126	United States	Method Of Blocking PLC Distributed SRAM Readback In User Mode	Issued	Lattice Semiconductor Corporation
12/976,412	8351287	United States	Bitline Floating Circuit For Power Reduction On SRAM Array	Issued	Lattice Semiconductor Corporation
12/976,520	8477549	United States	Strobed And Latched Readback Of SRAM Bits In A FPGA	Issued	Lattice Semiconductor Corporation
12/987,393	8274412	United States	Low Power SerDes With Built- In Word Alignment For Odd And Even Gearing Ratios	Issued	Lattice Semiconductor Corporation
13/006,622	8384428	United States	Programmable IO Pad - embedded function block	Issued	Lattice Semiconductor Corporation
13/007,804	8248136	United States	Low Power And Glitch-less Delay Element For High Speed Receiver Interface	Issued	Lattice Semiconductor Corporation
13/007,688	8324934	United States	Programmable Ratio Input Buffer	Issued	Lattice Semiconductor Corporation
13/026,555	8104009	United States	Wire Mapping For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
13/034,174	8058898	United States	Compression and Decompression Of Configuration Data Using	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Repeated Data Frames		
13/038,259	8368424	United States	Wakeup from sleep mode using slave I2C port or slave SPI port with powered down core logic	Issued	Lattice Semiconductor Corporation
13/038,270	8816718	United States	Slow Respond Mode Protocol For Synchronous Read	Issued	Lattice Semiconductor Corporation
13/037,703	8654600	United States	Current Sense Amplifier With Low Voltage Operation	Issued	Lattice Semiconductor Corporation
13/052,142	8553463	United States	Positive-To-Negative Voltage Discharge Circuit	Issued	Lattice Semiconductor Corporation
13/076,300	8319521	United States	Safe programming of key information into NV memory	Issued	Lattice Semiconductor Corporation
13/079,578	8314634	United States	Power Saving Standby Mode With Glitch-Less Output Controls	Issued	Lattice Semiconductor Corporation
13/079,595	8531222	United States	PLL Switchable Feedback Loops Among Internal And External Feedback Paths	Issued	Lattice Semiconductor Corporation
13/083,889	8138790	United States	Latency measurement circuit for wireless communications applications	Issued	Lattice Semiconductor Corporation
13/154,885	8441284	United States	Flexible Way To Incrementally Update Multi-Bit Data Registers	Issued	Lattice Semiconductor Corporation
13/155,547	8547075	United States	Filter And Stability Capacitor Reuse For On-Chip Dual Output Voltage Regulators	Issued	Lattice Semiconductor Corporation
13/164,108	8555217	United States	Cross-Probing Technology Between Software Plug-In Modules	Issued	Lattice Semiconductor Corporation
13/178,599	8539409	United States	Multiple silicon products from a common base set of masks	Issued	Lattice Semiconductor Corporation
13/178,536	8495264	United States	Packet And Control Symbol	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Alignment Circuit For SRIO		Corporation
13/193,984	8314632	United States	Placing ICs Into Ultra-Low Voltage Mode For Standby Purposes	Issued	Lattice Semiconductor Corporation
13/212,121	8451679	United States	Bit-Line Clamping Circuit To Improve Write Performance Of Dual-Port SRAM	Issued	Lattice Semiconductor Corporation
13/275,102	8169237	United States	High Speed Comparator with Data Dependent Jitter Mitigation	Issued	Lattice Semiconductor Corporation
13/299,507	8370691	United States	Testing of Soft Error Detection Logic For PLDs	Issued	Lattice Semiconductor Corporation
13/452,060	8823561	United States	In-System Reconfigurable Circuit For Mapping Data Words Of Different Lengths	Issued	Lattice Semiconductor Corporation
13/585,142	8461894	United States	Low Power And Glitch-less Delay Element For High Speed Receiver Interface	Issued	Lattice Semiconductor Corporation
13/616,173	8912933	United States	Low Power SerDes With Built- In Word Alignment For Odd And Even Gearing Ratios	Issued	Lattice Semiconductor Corporation
13/653,827	8710898	United States	Bandgap Reference Circuit Design With Triple-Trim Methodology For Mass Production	Issued	Lattice Semiconductor Corporation
13/680,947	8643398	United States	Placing ICs Into Low Voltage Mode For Standby Purposes	Issued	Lattice Semiconductor Corporation
13/685,385	8643168	United States	Input Capacitance Compensation In Package	Issued	Lattice Semiconductor Corporation
13/721,867	8686773	United States	In-System Margin Measurement Circuit	Issued	Lattice Semiconductor Corporation
13/738,265	8797064	United States	Low power, optimized H-bridge and CML driver	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
13/764,221	RE45200	United States	Programmable Signal Routing Systems Having Low Static Leakage	Issued	Lattice Semiconductor Corporation
13/857,919	8786482	United States	Analog-To-Digital-Converter	Issued	Lattice Semiconductor Corporation
13/892,948	8648636	United States	Method of Delaying Data from Clock in 1UI steps	Issued	Lattice Semiconductor Corporation
14/040,955	8829944	United States	Dynamic Power Supply Switching For Clock Signals	Issued	Lattice Semiconductor Corporation
13/155,261		United States	JTAG Based Parallel Measuring And Trimming for Time Based Parameters	Pending	Lattice Semiconductor Corporation
13/412,408		United States	Double Rate Throughput Processing Booster For DSP Slices	Pending	Lattice Semiconductor Corporation
13/466,463		United States	Early Match FIFO	Pending	Lattice Semiconductor Corporation
13/681,782		United States	Multi-channel transmitter synchronization circuitry	Pending	Lattice Semiconductor Corporation
13/777,243		United States	RAM Data Path Sense Leakage Abatement Circuit	Pending	Lattice Semiconductor Corporation
13/858,422		United States	Method To Enable And Disable Scan Test Mode Reliably Through JTAG Port With Maximum Scan Coverage	Pending	Lattice Semiconductor Corporation
13/868,738		United States	Loss of signal detection in high-speed serial link	Pending	Lattice Semiconductor Corporation
13/901,853		United States	Dual-Port SRAM With Bit Line Clamping	Pending	Lattice Semiconductor Corporation
13/904,861		United States	Bring up sequence for configurable PCIe IP in an	Pending	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			FPGA		Corporation
13/947,553		United States	Method For Hot Swapping Or Hot Plugging With Stable Supply-Side Reference Over Wide Voltage Range	Pending	Lattice Semiconductor Corporation
14/021,513		United States	Phase Locked Loop Circuit With Selectable Feedback Paths	Pending	Lattice Semiconductor Corporation
14/043,920		United States	Robust Serialized State-machine Interface Architecture Optimized for Implementation in Programmable Devices	Pending	Lattice Semiconductor Corporation
14/053,026		United States	ASB SW modeling methodology	Pending	Lattice Semiconductor Corporation
14/070,975		United States	Method to enable system board pin escape for tight ball pitch packages	Pending	Lattice Semiconductor Corporation
14/095,310		United States	A Novel ESD Implementation for 40nm FPGA	Pending	Lattice Semiconductor Corporation
14/136,482		United States	Automatic Quadrant Clock Assignment For Programmable Logic Devices	Pending	Lattice Semiconductor Corporation
14/137,443		United States	Using Critical Groups in FPGA Routing	Pending	Lattice Semiconductor Corporation
14/147,796		United States	A Hot Socket Implementation for General Purpose IO for 40nm FPGA	Pending	Lattice Semiconductor Corporation
14/172,678		United States	All Mosfet Circuit for Generating Accurate Collector Currents	Pending	Lattice Semiconductor Corporation
14/179,651		United States	LOW-VOLTAGE CURRENT SENSE AMPLIFIER	Pending	Lattice Semiconductor Corporation
14/194,484		United States	Logic Element Placement with Repacking Optimization	Pending	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/220,377		United States	DPHY using FPGA differential & single ended I/Os	Pending	Lattice Semiconductor Corporation
14/223,096		United States	DPHY using FPGA differential & single ended I/Os	Pending	Lattice Semiconductor Corporation
14/245,920		United States	Deterministic Dynamic Element Matching for Generating Precise Current Ratios	Pending	Lattice Semiconductor Corporation
14/271,331		United States	Inline Defect To Sort Test Correlation In Semiconductor Manufacturing	Pending	Lattice Semiconductor Corporation
14/271,955		United States	Performance-focused Adaptive Automatic Incremental Flow	Pending	Lattice Semiconductor Corporation
14/283,329		United States	Configuration logic controlled memory BIST (built-in self-test) for back-to-back initialization and readback of embedded block RAMs in FPGAs	Pending	Lattice Semiconductor Corporation
14/308,747		United States	A novel Output Driver drive strength and termination resistor continuously calibrating PVT compensation scheme	Pending	Lattice Semiconductor Corporation
14/313,443		United States	FPGA Hardware debug during post-config power-up and before logic analyzer connect	Pending	Lattice Semiconductor Corporation
14/313,778		United States	IOLOGIC Delay Cell Stealing for Holdtime Correction	Pending	Lattice Semiconductor Corporation
14/316,049		United States	Mapping Constant Multipliers To ICE Devices	Pending	Lattice Semiconductor Corporation
14/319,481		United States	Incrementer Absorption into Multiplier Logic	Pending	Lattice Semiconductor Corporation
14/320,169		United States	Method to Implement Mixed-	Pending	Lattice

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Width Mode Memory in Fixed-Mode Memory Architecture with Masking		Semiconductor Corporation
14/320,074		United States	Two Level Voltage Regulator scheme for SRAM Operation	Pending	Lattice Semiconductor Corporation
14/327,811		United States	Implementing Dual Boot For XO2 and Multiple ASCs	Pending	Lattice Semiconductor Corporation
14/339,164		United States	A unique method to optimize clock to out path	Pending	Lattice Semiconductor Corporation
14/339,229		United States	New method on bus-based clock_to_out timing optimization	Pending	Lattice Semiconductor Corporation
14/482,001		United States	Physically-aware Programmable Multiport Memory BIST with on-the-fly ATE-configurable memory tests	Pending	Lattice Semiconductor Corporation
14/509,564		United States	Dont-care based mux absorption into ice40 carry chain	Pending	Lattice Semiconductor Corporation
14/525,240		United States	Level shifter that eliminates static power dissipation	Pending	Lattice Semiconductor Corporation
14/535,454		United States	Low power and high performance class AB amplifier control common mode in SerDes Transmitter	Pending	Lattice Semiconductor Corporation
14/535,351		United States	ICO metastability prevention during start-up	Pending	Lattice Semiconductor Corporation
14/558,851		United States	Low Power and Flexible TX FFE With Programmable Tap Positions And Coefficients Driver Architecture	Pending	Lattice Semiconductor Corporation
14/576,348		United States	Reconfigurable and Scalable Hardware Management Architecture	Pending	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/576,245		United States	Methodology that allows multiple hardware or hardware-software controllers with different bus interfaces to share a common resource	Pending	Lattice Semiconductor Corporation
14/604,515		United States	Enhancement of FPGA hardware debugger to be used as a design controller/exerciser with user registers	Pending	Lattice Semiconductor Corporation
14/609,181		United States	Algorithm to Optimize Hot Swapping	Pending	Lattice Semiconductor Corporation
14/610,074		United States	Ripple Mode using 3-LUT for Generate	Pending	Lattice Semiconductor Corporation
14/610,127		United States	Combine OFX with LUT output and SUM into a single output to reduce number of signals to routing block	Pending	Lattice Semiconductor Corporation
14/611,069		United States	High speed complementary NMOS LUT logic	Pending	Lattice Semiconductor Corporation
14/611,095		United States	Shared Logic for Multiple Registers with asynchronous initialization with preload	Pending	Lattice Semiconductor Corporation
11/949,454	7,427,874	United States	Interface block architectures	Issued	Lattice Semiconductor Corporation
11/676,196	7,327,160	United States	SERDES with programmable I/O architecture	Issued	Lattice Semiconductor Corporation
6,786,564	6,786,564	United States	Inkjet printer, drive method and drive device for same	Issued	Lattice Semiconductor Corporation
11/839,107	7,856,050	United States	Receiver and transmitter calibration to compensate for frequency dependent I/Q imbalance	Issued	Lattice Semiconductor Corporation
07/679,370	5,255,221	United States	Fully configurable versatile field programmable function	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			element		Corporation
06/551,735	4,642,797	United States	High speed first-in-first-out memory	Issued	Lattice Semiconductor Corporation
08/042,533	5,394,037	United States	Sense amplifiers and sensing methods	Issued	Lattice Semiconductor Corporation
08/115,533	5,404,055	United States	Input routing pool	Issued	Lattice Semiconductor Corporation
08/115,723	5,394,033	United States	Structure and method for implementing hierarchical routing pools in a programmable logic circuit	Issued	Lattice Semiconductor Corporation
08/342,675	5,506,517	United States	Output enable structure and method for a programmable logic device	Issued	Lattice Semiconductor Corporation
07/911,841	5,357,156	United States	Active clamp circuit scheme for CMOS devices	Issued	Lattice Semiconductor Corporation
08/179,887	5,886,378	United States	Single polysilicon layer flash E.sup.2 PROM cell	Issued	Lattice Semiconductor Corporation
07/853,453	5,231,316	United States	Temperature compensated CMOS voltage to current converter	Issued	Lattice Semiconductor Corporation
08/108,363	5,353,246	United States	Programmable semiconductor antifuse structure and method of fabricating	Issued	Lattice Semiconductor Corporation
07/785,442	5,281,906	United States	Tunable voltage reference circuit to provide an output voltage with a predetermined temperature coefficient independent of variation in supply voltage	Issued	Lattice Semiconductor Corporation
07/696,453	5,251,169	United States	Non-volatile erasable and programmable interconnect cell	Issued	Lattice Semiconductor Corporation
07/538,211	5,255,203	United States	Interconnect structure for programmable logic device	Issued	Lattice Semiconductor

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
08/106,263	5,412,260	United States	Multiplexed control pins for in-system programming and boundary scan state machines in a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/033,934	5,418,390	United States	Single polysilicon layer E.sup.2 PROM cell	Issued	Lattice Semiconductor Corporation
07/993,711	5,452,229	United States	Programmable integrated-circuit switch	Issued	Lattice Semiconductor Corporation
07/957,311	5,329,179	United States	Arrangement for parallel programming of in-system programmable IC logical devices	Issued	Lattice Semiconductor Corporation
07/288,945	4,896,296	United States	Programmable logic device configurable input/output cell	Issued	Lattice Semiconductor Corporation
06/882,602	4,887,239	United States	One-time programmable data security system for programmable logic device	Issued	Lattice Semiconductor Corporation
06/871,063	4,766,569	United States	Programmable logic array	Issued	Lattice Semiconductor Corporation
06/862,815	4,879,688	United States	In-system programmable logic device	Issued	Lattice Semiconductor Corporation
06/707,670	4,833,646	United States	Programmable logic device with limited sense currents and noise reduction	Issued	Lattice Semiconductor Corporation
07/236,348	4,852,044	United States	Programmable data security circuit for programmable logic device	Issued	Lattice Semiconductor Corporation
11/400,924	7411424	United States	Programmable logic function generator using non-volatile programmable memory switches	Issued	Lattice Semiconductor Corporation
13/403,146		United States	Surface Mountable Integrated Circuit Packaging Scheme	Pending	SiBEAM, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/242,665		United States	High Speed Integrated Circuit Interface	Pending	SiBEAM, Inc.
14/196,978		United States	Calibration of Single-Ended High-Speed Interfaces	Pending	Silicon Image, Inc.
14/474,005		United States	Inter-Device Conflict Resolution on a Multimedia Link	Pending	Silicon Image, Inc.
61/989,417		United States	Control Target Selection	Pending	Silicon Image, Inc.
61/988,812		United States	Lip Sync Delay Compensation	Pending	Silicon Image, Inc.
61/989,415		United States	Streaming Data and Metadata Synchronization	Pending	Silicon Image, Inc.
61/991,126		United States	Stream Creation with Limited Topology Information	Pending	Silicon Image, Inc.
61/989,411		United States	Topology Discovery	Pending	Silicon Image, Inc.
14/463,146		United States	Radio Frequency Interference Reduction In Multimedia Interfaces	Pending	Silicon Image, Inc.
14/578,266		United States	Control Target Selection	Pending	Silicon Image, Inc.
14/578,257		United States	System for Dynamic Audio Visual Capabilities Exchange	Pending	Silicon Image, Inc.
62/089,767		United States	High-Bandwidth Digital Content Protection over Audio Return Channel	Pending	Silicon Image, Inc.
12/573,492	8482462	United States	MULTI-ANTENNA BEAM-FORMING SYSTEM FOR TRANSMITTING CONSTANT ENVELOPE SIGNALS DECOMPOSED FROM A VARIABLE ENVELOPE SIGNAL	Issued	Silicon Image, Inc.
12/678,463	8207892	United States	TECHNIQUE FOR DETERMINING AN ANGLE OF ARRIVAL IN A COMMUNICATION SYSTEM	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/675,269	8374558	United States	ANTENNA ARRAY WITH FLEXIBLE INTERCONNECT FOR A MOBILE WIRELESS DEVICE	Issued	Silicon Image, Inc.
12/333,134	8213872	United States	TECHNIQUE FOR LOW-POWER OPERATION OF A WIRELESS DEVICE	Issued	Silicon Image, Inc.
12/933,876	8256123	United States	DISPLACEMENT SENSING USING A FLEXIBLE SUBSTRATE	Issued	Silicon Image, Inc.
14/196,993		United States	Calibration of Single-Ended High-Speed Interfaces	Pending	Silicon Image, Inc.
13/988,047		United States	INTEGRATED PHASE-SHIFTING-AND-COMBINING CIRCUITRY TO SUPPORT MULTIPLE ANTENNAS	Pending	Silicon Image, Inc.
14/002,353		United States	TRACKING SYSTEM WITH ORTHOGONAL POLARIZATIONS AND A RETRO-DIRECTIVE ARRAY	Pending	Silicon Image, Inc.
13/726,822		United States	HIGH-ACCURACY DETECTION IN COLLABORATIVE TRACKING SYSTEMS	Pending	Silicon Image, Inc.
13/859,764		United States	ANTENNA SELECTION AND PILOT COMPRESSION IN MIMO SYSTEMS	Pending	Silicon Image, Inc.
62/100,841		United States	I/Q Imbalance Correction for the Combination of Multiple Radio Frequency Frontends	Pending	Silicon Image, Inc.
12/532,107	8571126	United States	MULTI-ANTENNA TRANSMITTER FOR MULTI-TONE SIGNALING	Issued	Silicon Image, Inc.
14/065,420		United States	MULTI-ANTENNA TRANSMITTER FOR MULTI-TONE SIGNALING	Pending	Silicon Image, Inc.
12/679,764	8605823	United States	COMMUNICATION USING	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			CONTINUOUS-PHASE MODULATED SIGNALS		Inc.
14/101,274		United States	COMMUNICATION USING CONTINUOUS-PHASE MODULATED SIGNALS	Pending	Silicon Image, Inc.
12/746,526	8484277	United States	TRANSFORMING SIGNALS USING PASSIVE CIRCUITS	Issued	Silicon Image, Inc.
13/498,884	8610474	United States	SIGNAL DISTRIBUTION NETWORKS AND RELATED MET	Issued	Silicon Image, Inc.
14/089,094		United States	SIGNAL DISTRIBUTION NETWORKS AND RELATED METHODS	Pending	Silicon Image, Inc.
13/519,302		United States	Phase Detection Circuits and Methods	Pending	Silicon Image, Inc.
13/574,586	8795082	United States	DIRECTIONAL BEAM STEERING SYSTEM AND METHOD TO DETECT LOCATION AND MOTION	Issued	Silicon Image, Inc.
14/331,144		United States	DIRECTIONAL BEAM STEERING SYSTEM AND METHOD TO DETECT LOCATION AND MOTION	Pending	Silicon Image, Inc.
13/704,564		United States	Methods and Systems for Near-Field MIMO Communications	Pending	Silicon Image, Inc.
14/235,783		United States	HIGH-ACCURACY AND LOW-POWER TRACKING SYSTEM FOR MOBILE DEVICES	Pending	Silicon Image, Inc.
14/234,623		United States	LOW-COST TRACKING SYSTEM	Pending	Silicon Image, Inc.
14/240,405		United States	CALIBRATING A RETRO-DIRECTIVE ARRAY FOR AN ASYMMETRIC WIRELESS LINK	Pending	Silicon Image, Inc.
14/364,002		United States	COLLABORATIVE CHANNEL SOUNDING IN MULTI-ANTENNA	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			SYSTEMS		
08/815,486	6,157,360	United States	System And Method For Driving Columns Of An Active Matrix Display	Issued	Silicon Image, Inc.
08/920,336	5,955,929	United States	Voltage-Controlled Oscillator Resistant To Supply Voltage Noise	Issued	Silicon Image, Inc.
09/007,707	5,969,552	United States	Dual Loop Delay-Locked Loop	Issued	Silicon Image, Inc.
09/298,647	6,259,427	United States	Scaling Multi-Dimensional Signals Using Variable Weighting Factors	Issued	Silicon Image, Inc.
09/298,369	6,374,361	United States	Skew-Insensitive Low Voltage Differential Receiver	Issued	Silicon Image, Inc.
09/393,849	6,738,417	United States	Method And Apparatus For Bidirectional Data Transfer Between A Digital Display And A Computer	Issued	Silicon Image, Inc.
09/326,503	6,940,496	United States	Display Module Driving System And Digital To Analog Converter For Driving Display	Issued	Silicon Image, Inc.
09/392,229	6,564,269	United States	Bi-Directional Data Transfer Using The Video Blanking Period In A Digital Data Stream	Issued	Silicon Image, Inc.
09/393,234	6,307,543	United States	Bi-Directional Data Transfer Using Two Pair Of Differential Lines As A Single Additional Differential Pair	Issued	Silicon Image, Inc.
09/947,008	6,492,984	United States	Bi-Directional Data Transfer Using Two Pair Of Differential Lines As A Single Additional Differential Pair	Issued	Silicon Image, Inc.
09/759,624	6,891,910	United States	Baud-Rate Timing Recovery	Issued	Silicon Image, Inc.
09/574,571	6,326,826	United States	Wide Frequency-Range Delay- Locked Loop Circuit	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/881,271	6,954,491	United States	Methods And Systems For Sending Side-Channel Data During Data Inactive Period	Issued	Silicon Image, Inc.
09/922,990	6,961,095	United States	Digital Display Jitter Correction Apparatus And Method	Issued	Silicon Image, Inc.
11/219,323	7,557,863	United States	Digital Display Jitter Correction Apparatus And Method	Issued	Silicon Image, Inc.
09/989,587	6,717,478	United States	Multi-Phase Voltage Controlled Oscillator (VCO) With Common Mode Control	Issued	Silicon Image, Inc.
10/371,220	7,231,009	United States	Data Synchronization Across An Asynchronous Boundary Using, For Example, Multi-Phase Clocks	Issued	Silicon Image, Inc.
09/989,580	7,103,013	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
11/441,669	7,599,316	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
12/573,847	8,116,240	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
10/045,297	7,257,129	United States	Memory Architecture With Multiple Serial Communications Ports	Issued	Silicon Image, Inc.
11/828,286	7,903,684	United States	Communications Architecture For Transmission Of Data Between Memory Bank Caches And Ports	Issued	Silicon Image, Inc.
09/167,527	6,380,978	United States	Digital Video System And Methods For Providing Same	Issued	DVDO, INC. and Silicon Image, Inc.
10/032,136	7,215,376	United States	Digital Video System And Methods For Providing Same	Issued	DVDO, INC. and Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/942,740	7,359,624	United States	Portable DVD Player	Issued	Silicon Image, Inc.
09/372,713	6,489,998	United States	Method And Apparatus For Deinterlacing Digital Video	Issued	Silicon Image, Inc.
09/941,949	6,909,469	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
10/251,642	7,027,099	United States	Method And Apparatus For Deinterlacing Digital Video Images	Issued	Silicon Image, Inc.
11/054,748	7,391,481	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
11/357,364	7,499,103	United States	Method And Apparatus For Detecting Frequency In Digital Video Images	Issued	Silicon Image, Inc.
11/932,808	7,633,559	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
09/410,543	6,700,622	United States	Method And Apparatus For Detecting The Source Format Of Video Images	Issued	Silicon Image, Inc.
09/396,993	6,515,706	United States	Method And Apparatus For Detecting And Smoothing Diagonal Features In Video Images	Issued	Silicon Image, Inc.
10/191,764	6,829,013	United States	Method And Apparatus For Detecting And Smoothing Diagonal Features In Video Images	Issued	Silicon Image, Inc.
09/363,312	6,681,059	United States	Method And Apparatus For Efficient Video Scaling	Issued	Silicon Image, Inc.
09/359,530	6,587,158	United States	Method And Apparatus For Reducing On-Chip Memory In Vertical Video Processing	Issued	Silicon Image, Inc.
09/226,776	6,219,747	United States	Methods And Apparatus For Variable Length SDRAM	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Transfers		
09/805,588	6,385,692	United States	Methods and Apparatus for Variable Length SDRAM Transfers	Issued	Silicon Image, Inc.
09/227,502	6,393,505	United States	Methods And Apparatus For Data Bus Arbitration	Issued	Silicon Image, Inc.
09/226,381	6,473,476	United States	Method And Apparatus For Providing Deterministic Resets For Clock Divider Systems	Issued	Silicon Image, Inc.
09/837,894	6,867,814	United States	Method, System And Article Of Manufacture For Identifying The Source Type And Quality Level Of A Video Sequence	Issued	Silicon Image, Inc.
09/478,122	7,203,557	United States	Audio Signal Delay Apparatus And Method	Issued	Silicon Image, Inc.
10/663,413	7,408,992	United States	Detection And Repair Of MPEG-2 Chroma Upconversion Artifacts	Issued	Silicon Image, Inc.
09/905,318	7,123,307	United States	Clock Jitter Limiting Scheme In Video Transmission Through Multiple Stages	Issued	Silicon Image, Inc.
09/905,615	6,944,804	United States	System And Method For Measuring Pseudo Pixel Error Rate	Issued	Silicon Image, Inc.
09/904,783	6,625,560	United States	Method Of Testing Serial Interface	Issued	Silicon Image, Inc.
09/989,590	6,845,461	United States	High-Speed Bus With Embedded Clock Signals	Issued	Silicon Image, Inc.
09/989,645	6,809,567	United States	System And Method For Multiple-Phase Clock Generation	Issued	Silicon Image, Inc.
09/905,511	7,062,004	United States	Method And Apparatus For Adaptive Control Of PLL Loop Bandwidth	Issued	Silicon Image, Inc.
10/057,823	7,023,487	United States	Deinterlacing Of Video Sources Via Image Feature Edge Detection	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/954,663	7,558,326	United States	Method And Apparatus For Sending Auxiliary Data On A TMDS-Like Link	Issued	Silicon Image, Inc.
10/036,234	7,359,437	United States	Encoding Method And System For Reducing Inter-Symbol Interference Effects In Transmission Over A Serial Link	Issued	Silicon Image, Inc.
10/095,422	7,257,163	United States	Method And System For Reducing Inter-Symbol Interference Effects In Transmission Over A Serial Link With Mapping Of Each Word In A Cluster Of Received Words To A Single Transmitted Word	Issued	Silicon Image, Inc.
10/171,860	7,088,398	United States	Method And Apparatus For Regenerating A Clock For Auxiliary Data Transmitted Over A Serial Link With Video Data	Issued	Silicon Image, Inc.
10/192,296	6,914,637	United States	Method And System For Video And Auxiliary Data Transmission Over A Serial Link	Issued	Silicon Image, Inc.
10/357,750	7,283,566	United States	Method And Circuit For Generating Time Stamp Data From An Embedded-Clock Audio Data Stream And A Video Clock	Issued	Silicon Image, Inc.
10/016,247	6,714,206	United States	Method And System For Spatial-Temporal Dithering For Displays With Overlapping Pixels	Issued	Silicon Image, Inc.
10/133,813	7,136,484	United States	Cryptosystems Using Commuting Pairs In A Monoid	Issued	Silicon Image, Inc.
10/047,772	7,109,958	United States	Supporting Circuitry And Method For Controlling Pixels	Issued	Silicon Image, Inc.
10/045,393	7,039,121	United States	Method And System For Transition-Controlled Selective Block Inversion	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Communications		
08/656,032	6,018,456	United States	Enclosure For Removable Computer Peripheral Equipment	Issued	CMD Technology Inc. and Silicon Image, Inc.
08/906,775	5,991,546	United States	System And Method For Interfacing Manually Controllable Input Devices To A Universal Computer Bus System	Issued	CMD Technology Inc. and Silicon Image, Inc.
10/171,820	7,225,282	United States	Method And Apparatus For A Two-Wire Serial Command Bus Interface	Issued	Silicon Image, Inc.
11/713,241	7,441,065	United States	Adaptive Beam-Steering Methods To Maximize Wireless Link Budget And Reduce Delay-Spread Using Multiple Transmit And Receive Antennas	Issued	Silicon Image, Inc.
10/210,839	7,171,525	United States	Method And System For Arbitrating Priority Bids Sent Over Serial Links To A Multi-Port Storage Device	Issued	Silicon Image, Inc.
09/688,536	6,380,783	United States	Cyclic Phase Signal Generation From A Single Clock Source Using Current Phase Interpolation	Issued	Silicon Image, Inc.
09/847,837	6,535,029	United States	Fully Differential Continuous-Time Current-Mode High Speed CMOS Comparator	Issued	Silicon Image, Inc.
10/270,882	7,009,827	United States	Voltage Swing Detection Circuit For Hot Plug Event Or Device Detection Via A Differential Link	Issued	Silicon Image, Inc.
10/162,046	6,843,674	United States	Method And Apparatus For Connecting Serial ATA Storage Components	Issued	Silicon Image, Inc.
09/945,278	7,131,004	United States	Method And Apparatus For Encrypting Data Transmitted Over A Serial Link	Issued	Silicon Image, Inc.
11/499,124	7,900,047	United States	Method And Apparatus For Encrypting Data Transmitted	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Over A Serial Link		Inc.
11/543,501	7,757,085	United States	Method And Apparatus For Encrypting Data Transmitted Over A Serial Link	Issued	Silicon Image, Inc.
10/224,995	7,218,737	United States	System And Method For An Adaptive State Machine To Control Signal Filtering In A Serial Link	Issued	Silicon Image, Inc.
09/991,057	7,242,766	United States	Method And System For Encrypting And Decrypting Data Using An External Agent	Issued	Silicon Image, Inc.
10/085,177	7,035,290	United States	Method And System For Temporary Interruption Of Video Data Transmission	Issued	Silicon Image, Inc.
10/036,794	6,976,201	United States	Method And System For Host Handling Of Communications Errors	Issued	Silicon Image, Inc.
10/053,461	7,113,507	United States	Method And System For Communicating Control Information Via Out-Of-Band Symbols	Issued	Silicon Image, Inc.
10/045,625	7,746,798	United States	Method And System For Integrating Packet Type Information With Synchronization Symbols	Issued	Silicon Image, Inc.
10/035,911	7,154,905	United States	Method And System For Nesting Of Communications Packets	Issued	Silicon Image, Inc.
10/045,600	6,771,192	United States	Method And System For DC-Balancing At The Physical Layer	Issued	Silicon Image, Inc.
10/045,601	7,340,558	United States	Multisection Memory Bank System	Issued	Silicon Image, Inc.
09/989,647	7,058,121	United States	Logic Gates Including Diode-Connected Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) To Control Input Threshold Voltage Levels And Switching Transients Of	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Output Logic Signals		
09/989,487	6,985,005	United States	Differential Amplifiers Using Asymmetric Transfer Characteristics To Suppress Input Noise In Output Logic Signals	Issued	Silicon Image, Inc.
11/330,047	7,456,648	United States	Differential Amplifiers Using Asymmetric Transfer Characteristics To Suppress Input Noise In Output Logic Signals	Issued	Silicon Image, Inc.
12/275,686	7,847,583	United States	Transmitter And Receiver Using Asymmetric Transfer Characteristics In Differential Amplifiers To Suppress Noise	Issued	Silicon Image, Inc.
10/403,477	6,819,166	United States	Continuous-Time, Low-Frequency-Gain/High-Frequency-Boosting	Issued	Silicon Image, Inc.
10/417,712	7,348,991	United States	Video Graphics Text Mode Enhancement Method For Digitally Processed Data	Issued	Silicon Image, Inc.
10/287,976	6,873,341	United States	Detection Of Video Windows And Graphics Windows	Issued	Silicon Image, Inc.
10/298,722	7,539,304	United States	Integrated Circuit Having Self Test Capability Using Message Digest And Method For Testing Integrated Circuit Having Message Digest Generation Circuitry	Issued	Silicon Image, Inc.
10/215,936	6,717,468	United States	Dynamically Biased Full-Swing Operation Amplifier For An Active Matrix Liquid Crystal Display Driver	Issued	Silicon Image, Inc.
10/268,832	7,412,053	United States	Cryptographic Device With Stored Key Data And Method For Using Stored Key Data To Perform An Authentication Exchange Of Self Test	Issued	Silicon Image, Inc.
11/950,088	7,797,536	United States	Cryptographic Device With Stored Key Data And Method	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			For Using Stored Key Data To Perform An Authentication Exchange Of Self Test		
10/244,152	6,814,583	United States	Through-Broad PCB Edge Connector, System And Method	Issued	Silicon Image, Inc.
10/247,675	8,064,508	United States	Equalizer With Controllably Weighted Parallel High Pass And Low Pass Filters And Receiver Including Such An Equalizer	Issued	Silicon Image, Inc.
11/796,175	8,275,026	United States	Equalizer With Controllably Weighted Parallel High Pass And Low Pass Filters And Receiver Including Such An Equalizer	Issued	Silicon Image, Inc.
10/651,500	7,551,909	United States	CMOS Transceiver With Dual Current Path VCO	Issued	Silicon Image, Inc.
10/099,533	7,158,593	United States	Combining A Clock Signal And A Data Signal	Issued	Silicon Image, Inc.
10/642,259	7,409,031	United States	Data Sampling Method And Apparatus With Alternating Edge Sampling Phase Detection For Loop Characteristic Stabilization	Issued	Silicon Image, Inc.
10/459,989	7,187,307	United States	Method And System For Encapsulation Of Multiple Levels Of Communication Protocol Functionality Within Line Codes	Issued	Silicon Image, Inc.
10/794,015	7,502,411	United States	Method And Circuit For Adaptive Equalization Of Multiple Signals In Response To A Control Signal Generated From One Of The Equalized Signals	Issued	Silicon Image, Inc.
10/459,992	6,747,580	United States	Method And Apparatus For Encoding Or Decoding Data In Accordance With An Nb/(N+1)B Block Code, And Method For Determining Such A Block Code	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/781,405	7,269,673	United States	Cable With Circuitry For Asserting Stored Cable Data Or Other Information To An External Device Or User	Issued	Silicon Image, Inc.
11/848,758	7,500,032	United States	Cable With Circuitry For Asserting Stored Cable Data Or Other Information To An External Device Or User	Issued	Silicon Image, Inc.
11/123,353	7,375,960	United States	Apparatus For Removably Securing Storage Components In An Enclosure	Issued	Silicon Image, Inc.
10/763,905	7,236,553	United States	Reduced Dead-Cycle, Adaptive Phase Tracking Method And Apparatus	Issued	Silicon Image, Inc.
10/835,301	6,897,793	United States	Method And Apparatus For Run Length Limited TMDS-Like Encoding Of Data	Issued	Silicon Image, Inc.
10/842,231	7,991,096	United States	Data Sampling Method And Apparatus Using Through-Transition Counts To Reject Worst Sampling Position	Issued	Silicon Image, Inc.
10/439,446	7,031,858	United States	Method And Circuit For DC Measurement Of Phase Uniformity Of Multi-Phase Clocks	Issued	Silicon Image, Inc.
10/302,436	7,274,690	United States	An Age Selection Switching Scheme For Data Traffic In A Crossbar Switch	Issued	Silicon Image, Inc.
10/645,786	7,505,422	United States	Preference Programmable First-One Detector And Quadrature Based Random Grant Generator	Issued	Silicon Image, Inc.
10/645,787	7,461,167	United States	A Method For Multicast Service In A Crossbar Switch	Issued	Silicon Image, Inc.
10/762,950	7,352,764	United States	Content Addressable Merged Queue Architecture For Switching Data	Issued	Silicon Image, Inc.
10/434,785	7,519,066	United States	A Method For Switching Data In A Crossbar Switch	Issued	Silicon Image, Inc.
11/372,866	7,694,204	United States	Error Detection In Physical	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Interfaces For Point-To-Point Communications Between Integrated Circuits		Inc.
12/712,124	7,937,644	United States	Error Detection In Physical Interfaces For Point-To-Point Communications Between Integrated Circuits	Issued	Silicon Image, Inc.
13/099,254	8,099,648	United States	Error Detection In Physical Interfaces For Point-To-Point Communications Between Integrated Circuits	Issued	Silicon Image, Inc.
11/669,416	7,844,762	United States	Parallel Interface Bus To Communicate Video Data Encoded For Serial Data Links	Issued	Silicon Image, Inc.
11/056,995	7,102,446	United States	Phase Lock Loop With Coarse Control Loop Having Frequency Lock Detector And Device Including Same	Issued	Silicon Image, Inc.
11/643,388	7,589,559	United States	Current Mode Circuitry To Modulate A Common Mode Voltage	Issued	Silicon Image, Inc.
12/555,300	7,872,498	United States	Current Mode Circuitry to Modulate a Common Mode Voltage	Issued	Silicon Image, Inc.
11/477,049	7,793,179	United States	Test Clock Control Structures To Generate Configurable Test Clocks For Scan-Based Testing Of Electronic Circuits Using Programmable Test Clock Controllers	Issued	Silicon Image, Inc.
11/856,640	7,782,934	United States	Parameter Scanning For Signal Over-Sampling	Issued	Silicon Image, Inc.
11/592,792	7,450,038	United States	Determining Oversampled Data To Be Included In Unit Intervals	Issued	Silicon Image, Inc.
11/510,254	8,595,434	United States	Smart Scalable Storage Switch Architecture	Issued	Silicon Image, Inc.
14/067,363		United States	Smart Scalable Storage Switch Architecture	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/314,162	7,571,269	United States	A Covert Channel For Conveying Supplemental Messages In A Protocol-Defined Link For A System Of Storage Devices	Issued	Silicon Image, Inc.
11/637,254	7,602,253	United States	Adaptive Bandwidth Phase Locked Loop With Feedforward Divider	Issued	Silicon Image, Inc.
11/656,331	7,984,369	United States	Concurrent Code Checker And Hardware Efficient High-Speed I/O Having Built-In Self-Test And Debug Features	Issued	Silicon Image, Inc.
11/694,819	7,949,863	United States	Multi-Port Memory Device Having Variable Port Speeds	Issued	Silicon Image, Inc.
11/694,813	7,639,561	United States	Power-Saving Clocking Technique	Issued	Silicon Image, Inc.
11/690,629	7,831,778	United States	Mechanism For Streaming Media Data Over Wideband Wireless Networks	Issued	Silicon Image, Inc.
11/476,457	7,840,861	United States	Scan-Based Testing Of Devices Implementing A Test Clock Control Structure (â€œTCCSâ€)	Issued	Silicon Image, Inc.
11/861,175	8,160,192	United States	Signal Interleaving for Serial Clock and Data Recovery	Issued	Silicon Image, Inc.
11/690,642	7,908,501	United States	Shared Nonvolatile Memory Architecture	Issued	Silicon Image, Inc.
11/742,358	7,698,088	United States	Interface Test Circuitry And Methods	Issued	Silicon Image, Inc.
11/848,641	8,233,432	United States	Ensuring Physical Locality Of Entities Sharing Data	Issued	Silicon Image, Inc.
11/683,608	7,831,877	United States	Method And Apparatus For A Two-Wire Serial Command Bus Interface	Issued	Silicon Image, Inc.
11/690,659	7,849,339	United States	Progressive Power Control Of A Multi-Port Memory Device	Issued	Silicon Image, Inc.
11/567,514	7,365,659	United States	Method Of Context Adaptive Binary Arithmetic Coding	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			And Coding Apparatus Using The Same		
12/778,882		United States	Multi-Level Port Expansion For Port Multipliers	Pending	Silicon Image, Inc.
12/147,248	7,836,223	United States	Operation Of Media Interface To Provide Bidirectional Communications	Issued	Silicon Image, Inc.
11/849,163	8,695,034	United States	Delivering On Screen Display Data To Existing Display Devices	Issued	Silicon Image, Inc.
11/828,219	8,599,315	United States	On Screen Displays Associated With Remote Video Source Devices	Issued	Silicon Image, Inc.
14/070,373		United States	On Screen Displays Associated With Remote Video Source Devices	Pending	Silicon Image, Inc.
11/829,800	7,903,550	United States	Bandwidth Reservation For Data Flows In Interconnection Networks	Issued	Silicon Image, Inc.
11/828,223	8,149,711	United States	Data Stream Control For Network Devices	Issued	Silicon Image, Inc.
13/541,390	8,924,509	United States	Automated Service Discovery And Dynamic Connection Management	Issued	Silicon Image, Inc.
11/836,082	8,468,212	United States	Network Repository For Metadata	Issued	Silicon Image, Inc.
13/919,773		United States	Network Repository For Metadata	Pending	Silicon Image, Inc.
11/829,790	7,911,956	United States	Packet Level Prioritization In Interconnection Networks	Issued	Silicon Image, Inc.
11/828,226		United States	Streaming Data Content In A Network	Pending	Silicon Image, Inc.
11/848,153	7,936,790	United States	Synchronizing Related Data Streams In Interconnection Networks	Issued	Silicon Image, Inc.
11/952,052	8,001,334	United States	Bank Sharing And Refresh In A Shared Multi-Port Memory Device	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/075,954	7,979,589	United States	Method, Apparatus, And System For Port Multiplier Enhancement	Issued	Silicon Image, Inc.
13/298,001		United States	Iddq Testing Of CMOS Devices	Pending	Silicon Image, Inc.
10/788,704	6,944,086	United States	Semiconductor Memory Device	Issued	Silicon Image, Inc.
10/876,231	7,016,255	United States	Multi-Port Memory Device	Issued	Silicon Image, Inc.
10/877,318	7,089,465	United States	Multi-Port Memory Device Having Serial I/O Interface	Issued	Silicon Image, Inc.
12/075,906	7,904,566	United States	Method, Apparatus, And System For Employing An Enhanced Port Multiplier	Issued	Silicon Image, Inc.
12/497,391	8,386,867	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
13/776,508	8,667,354	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
14/145,751	8,924,805	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
12/197,020	8,086,886	United States	Group Power Management Of Network Devices	Issued	Silicon Image, Inc.
12/683,365	8,543,873	United States	Multi-Site Testing Of Computer Memory Devices And Serial I/O Ports	Issued	Silicon Image, Inc.
14/035,795	8,839,058	United States	Multi-Site Testing Of Computer Memory Devices And Serial I/O Ports	Issued	Silicon Image, Inc.
11/969,847	8,090,030	United States	Method, Apparatus And System For Generating And Facilitating Mobile High-Definition Multimedia Interface	Issued	Silicon Image, Inc.
11/969,852	7,856,520	United States	Control Bus For Connection Of Electronic Devices	Issued	Silicon Image, Inc.
11/969,865	7,921,231	United States	Discovery Of Electronic Devices Utilizing A Control	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Bus		
12/172,187	8,238,653	United States	Methods And Mechanisms For Probabilistic Color Correction	Issued	Silicon Image, Inc.
12/392,000		United States	Method, Apparatus, And System For Pre-Authentication And Processing Of Data Streams	Pending	Silicon Image, Inc.
12/391,987	8,644,504	United States	Method, Apparatus, And System For Deciphering Media Content Stream	Issued	Silicon Image, Inc.
12/605,134	8,407,427	United States	Method And System For Improving Serial Port Memory Communication Latency And Reliability	Issued	Silicon Image, Inc.
13/850,147	8,892,825	United States	Method and System for Improving Serial Port Memory Communication Latency and Reliability	Issued	Silicon Image, Inc.
12/260,970	8,036,248	United States	Method, Apparatus, And System For Automatic Data Aligner For Multiple Serial Receivers	Issued	Silicon Image, Inc.
12/359,025	8,026,726	United States	Fault Testing For Interconnections	Issued	Silicon Image, Inc.
12/486,969	8,793,723	United States	Detection Of Encryption Utilizing Error Detection For Received Data	Issued	Silicon Image, Inc.
12/570,874	8,644,334	United States	Messaging To Provide Data Link Integrity	Issued	Silicon Image, Inc.
12/260,972	7,777,652	United States	Coding System For Memory Systems Employing High-Speed Serial Links	Issued	Silicon Image, Inc.
12/847,416	7,978,099	United States	17b/20b Coding System	Issued	Silicon Image, Inc.
12/351,698	8,374,346	United States	Method, Apparatus, And System For Pre-Authentication And Keep-Authentication Of Content Protected Ports	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/316,305	8,347,081	United States	Method, Apparatus And System For Employing A Content Protection System	Issued	Silicon Image, Inc.
12/577,707	8,275,914	United States	Method And System For Transmitting Or Receiving N-Bit Video Data Over A Serial Link	Issued	Silicon Image, Inc.
12/606,096	8,176,214	United States	Transmission Of Alternative Content Over Standard Device Connectors	Issued	Silicon Image, Inc.
12/351,712	8,185,739	United States	Method And System For Detecting Successful Authentication Of Multiple Ports In A Time Based Roving Architecture	Issued	Silicon Image, Inc.
12/512,877	8,458,343	United States	Signaling For Transitions Between Modes Of Data Transmission	Issued	Silicon Image, Inc.
12/983,233	8,489,784	United States	Adaptive Interconnection Scheme For Multimedia Devices	Issued	Silicon Image, Inc.
13/004,359	8,755,431	United States	Transmission And Detection Of Multi-Channel Signals In Reduced Channel Format	Issued	Silicon Image, Inc.
12/650,357		United States	Method, Apparatus, And System For Simultaneously Previewing Contents From Multiple Protected Sources	Pending	Silicon Image, Inc.
12/712,933	8,692,937	United States	Video Frame Synchronization	Issued	Silicon Image, Inc.
12/966,194		United States	Transmission And Handling Of Three-Dimensional Video Content	Pending	Silicon Image, Inc.
12/873,124	8,325,757	United States	De-Encapsulation Of Data Streams Into Multiple Links	Issued	Silicon Image, Inc.
12/704,417	8,510,487	United States	Hybrid Interface For Serial And Parallel Communication	Issued	Silicon Image, Inc.
13/934,147	8,751,709	United States	Hybrid Interface For Serial And Parallel Communication	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/842,165	8,930,692	United States	Mechanism For Internal Processing Of Content Through Partial Authentication On Secondary Channel	Issued	Silicon Image, Inc.
12/842,190		United States	Mechanism For Partial Encryption Of Data Streams	Pending	Silicon Image, Inc.
13/021,958		United States	Determination Of Physical Connectivity Status Of Devices Based On Electrical Measurement	Allowed	Silicon Image, Inc.
12/898,528	8,598,898	United States	Testing Of High-Speed Input-Output Devices	Issued	Silicon Image, Inc.
13/434,273		United States	Method, Apparatus And System For Transitioning An Audio/Video Device Between A Source Mode And A Sink Mode	Pending	Silicon Image, Inc.
12/848,037	8,624,960	United States	Multi-View Display System	Issued	Silicon Image, Inc.
14/094,668		United States	Multi-View Display System	Pending	Silicon Image, Inc.
12/816,437	8,698,958	United States	Mechanism For Memory Reduction In Picture-In-Picture Video Generation	Issued	Silicon Image, Inc.
13/753,408		United States	Communication Bridging Between Devices Via Multiple Bridge Elements	Pending	Silicon Image, Inc.
13/198,584		United States	Conversion Of Multimedia Data Streams For Use By Connected Devices	Pending	Silicon Image, Inc.
12/906,939	8,537,201	United States	Combining Video Data Streams Of Differing Dimensionality For Concurrent Display	Issued	Silicon Image, Inc.
13/172,745	8,484,387	United States	Detection Of Cable Connections For Electronic Devices	Issued	Silicon Image, Inc.
13/172,742	8,601,173	United States	Detection Of Cable Connections For Electronic	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Devices		
13/362,930		United States	Mechanism For Low Power Standby Mode Control Circuit	Allowed	Silicon Image, Inc.
13/217,138	8,379,145	United States	Conversion And Processing Of Deep Color Video In A Single Clock Domain	Issued	Silicon Image, Inc.
12/979,995	8,874,820	United States	Mechanism For Facilitating A Configurable Port-Type Peripheral Component Interconnect Express/Serial Advanced Technology Attachment Host Controller Architecture	Issued	Silicon Image, Inc.
12/950,850	8,504,672	United States	Discovery Of Electronic Devices In A Combined Network	Issued	Silicon Image, Inc.
13/959,592	8,799,443	United States	Discovery of Electronic Devices in a Combined Network	Issued	Silicon Image, Inc.
13/348,378		United States	Proxy Device Operation In Command And Control Network	Pending	Silicon Image, Inc.
12/950,867		United States	Transfer Of Control Bus Signaling On Packet-Switched Network	Pending	Silicon Image, Inc.
13/339,339		United States	Mechanism For Recovering Clock For Streaming Content Over A Packetized Network	Pending	Silicon Image, Inc.
13/302,452		United States	Multimedia I/O System Architecture for Advanced Digital Television	Pending	Silicon Image, Inc.
13/107,031		United States	Audio And Video Data Multiplexing For Multimedia Stream Switch	Pending	Silicon Image, Inc.
13/174,630		United States	Single-Ended Configurable Multi-Mode Driver	Pending	Silicon Image, Inc.
13/173,302		United States	Fine-Grained Self Refresh Control For DRAM Devices	Pending	Silicon Image, Inc.
13/174,616	8,760,188	United States	Configurable Multi-Dimensional Driver And	Issued	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Receiver		Inc.
13/083,399	8,611,486	United States	Adjustment Of Clock Signals Regenerated From A Data Stream	Issued	Silicon Image, Inc.
11/437,357	7,982,798	United States	Edge Detection	Issued	Silicon Image, Inc.
13/153,230	8,446,525	United States	Edge Detection	Issued	Silicon Image, Inc.
10/753,909	7,400,359	United States	Video Stream Routing And Format Conversion Unit With Audio Delay	Issued	Silicon Image, Inc.
10/889,855	7,710,501	United States	Time Base Correction And Frame Rate Conversion	Issued	Silicon Image, Inc.
11/487,144	8,004,606	United States	Original Scan Line Detection	Issued	Silicon Image, Inc.
11/941,050	8,086,067	United States	Noise Cancellation	Issued	Silicon Image, Inc.
11/512,754	8,120,703	United States	Source-Adaptive Video Deinterlacer	Issued	Silicon Image, Inc.
12/204,760	8,559,746	United States	System, Method And Apparatus For Smoothing Of Edges In Images To Remove Irregularities	Issued	Silicon Image, Inc.
14/054,575		United States	System, Method and Apparatus for Smoothing of Edges in Images to Remove Irregularities	Pending	Silicon Image, Inc.
12/703,623	8,452,117	United States	Block Noise Detection And Filtering	Issued	Silicon Image, Inc.
13/899,222	8,891,897	United States	Block Noise Detection And Filtering	Issued	Silicon Image, Inc.
13/335,398		United States	Ringing Suppression In Video Scalers	Pending	Silicon Image, Inc.
13/546,904		United States	Transmission Of Multiple Protocol Data Elements Via An Interface Utilizing A Data Tunnel	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/202,995	7,904,117	United States	Wireless Communication Device Using Adaptive Beamforming	Issued	SiBEAM, Inc.
11/706,711	7,710,319	United States	HD Physical Layer Of A Wireless Communication Device	Issued	SiBEAM, Inc.
12/748,276	7,982,669	United States	Adaptive Beam-Steering Methods To Maximize Wireless Link Budget And Reduce Delay-Spread Using Multiple Transmit And Receive Antennas	Issued	SiBEAM, Inc.
11/706,470	8,014,416	United States	Inter-Port Communication In A Multi-Port Memory Device	Issued	Silicon Image, Inc.
11/689,386	7,881,258	United States	Circuitry To Prevent Peak Power Problems During Scan Shift	Issued	SiBEAM, Inc.
11/726,874	8,155,712	United States	Low Power Very High-Data Rate Device	Issued	SiBEAM, Inc.
11/588,472	8,022,887	United States	Planar Antenna	Issued	SiBEAM, Inc.
11/752,073		United States	A Compact Millimeter Wave Vertical Interconnection Scheme By Combining Flip-Chip, Layer Transition	Pending	SiBEAM, Inc.
11/752,083	7,675,465	United States	Surface Mountable Integrated Circuit Packaging Scheme	Issued	SiBEAM, Inc.
12/215,959		United States	Mechanism For Communication With Multiple Wireless Video Area Networks	Pending	SiBEAM, Inc.
11/981,935		United States	Wireless HD Mac Frame Format	Pending	SiBEAM, Inc.
11/938,126	8,170,522	United States	Multi-Transformer Architecture For An RF Active Circuit	Issued	SiBEAM, Inc.
11/999,810	8,750,241	United States	Concurrent Association With Multiple WVAN Network	Issued	SiBEAM, Inc.
12/079,133	8,831,225	United States	Data Security	Issued	SiBEAM, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/011,404	7,948,961	United States	Wireless Proximity Estimation	Issued	SiBEAM, Inc.
11/982,209	8,279,784	United States	Wireless HD AV Packet Format	Issued	SiBEAM, Inc.
12/055,160	8,170,617	United States	Extensions To Adaptive BeamSteering Method	Issued	SiBEAM, Inc.
12/164,757		United States	Exchanging Information Between Components Coupled With An I2C Bus Via Separate Banks	Pending	SiBEAM, Inc.
12/167,195	8,229,352	United States	Wireless Architecture For 60 GHz	Issued	SiBEAM, Inc.
11/901,069	7,986,753	United States	Modified Branch Metric For Decoders And Equalizers	Issued	SiBEAM, Inc.
12/059,757	7,915,909	United States	RF Integrated Circuit Test Methodology And System	Issued	SiBEAM, Inc.
12/164,907		United States	Dispatch Capability Using A Single Physical Interface	Pending	SiBEAM, Inc.
12/165,468		United States	Bitmap Device Identification In A Wireless Communication System	Pending	SiBEAM, Inc.
12/165,472	8,897,719	United States	Initializing A Transceiver In A Wireless Communication System	Issued	SiBEAM, Inc.
12/164,849	8,341,271	United States	Device Discovery In A Wireless Communication System	Issued	SiBEAM, Inc.
12/164,810	8,116,333	United States	Connection Control In A Wireless Communication System	Issued	SiBEAM, Inc.
12/699,758	8,588,193	United States	Enhanced Wireless Data Rates Using Multiple Beams	Issued	SiBEAM, Inc.
12/699,781	8,457,026	United States	Enhanced Wireless Data Rates Using Multiple Beams	Issued	SiBEAM, Inc.
13/113,318		United States	Apparatus, System, And Method For A Compact Symmetrical Transition Structure For Radio	Allowed	SiBEAM, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Frequency Applications		
14/128,551		United States	Method To Drive HDMI Or MHL Or USB Data Through One Set Of Pins	Pending	Silicon Image, Inc.
13/984,018		United States	Concept And Method Of Reducing Data Dependent Jitter	Pending	Silicon Image, Inc.
13/269,450		United States	Identification And Handling Of Data Streams Using Coded Preambles	Allowed	Silicon Image, Inc.
13/611,786		United States	Combining Video And Audio Streams Utilizing Pixel Repetition Bandwidth	Pending	Silicon Image, Inc.
14/118,832		United States	Compensation Scheme For MHL Common Mode Clock Swing	Pending	Silicon Image, Inc.
13/773,534		United States	Transmitting Multiple Differential Signals Over a Reduced Number of Physical Channels	Pending	Silicon Image, Inc.
13/460,393		United States	Cost-Efficient And Low-Latency Motion Picture Encoding For Limited Channel Bandwidth	Pending	Silicon Image, Inc.
13/791,494	8,925,003	United States	Mechanism For Facilitating Syncronization Of Audio And Video Between Multiple Media Devices	Issued	Silicon Image, Inc.
13/622,286	8,885,435	United States	Interfacing Between Integrated Circuits With Asymmetric Voltage Swing	Issued	Silicon Image, Inc.
13/770,984		United States	Configurable Single Ended Driver	Pending	Silicon Image, Inc.
13/779,372	8,920,188	United States	Integrated Connector/Flex Cable	Issued	Silicon Image, Inc.
13/834,927		United States	Simultaneous Transmission Of Clock And Bidirectional Data Over A Communication Channel	Allowed	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
13/605,708	8,841,974	United States	Test Solution For Ring Oscillators	Issued	Silicon Image, Inc.
14/193,932		United States	Test Solution for a Random Number Generator	Pending	Silicon Image, Inc.
13/787,664		United States	Auxiliary Data Encoding In Video Data	Pending	Silicon Image, Inc.
13/738,768		United States	Method And Apparatus For Reducing Digital Video Image Data	Pending	Silicon Image, Inc.
13/736,765	8,832,338	United States	Mechanism For Facilitating Dynamic Timestamp-Less Clock Regeneration For Transmitting Media Streams Over Shared Channels	Issued	Silicon Image, Inc.
14/123,037		United States	Timing Controlled Cascade Feed-Through High Speed Line Driver	Pending	Silicon Image, Inc.
13/776,577		United States	Apparatus, System And Method For Providing Clock And Data Signaling	Pending	Silicon Image, Inc.
13/940,038		United States	Integrated Mobile Desktop	Pending	Silicon Image, Inc.
13/915,586		United States	Multiple Protocol Tunneling Using Time Division Operations	Pending	Silicon Image, Inc.
13/891,842	8,786,776	United States	Method, Apparatus And System For Communicating Sideband Data With Non-Compressed Video	Issued	Silicon Image, Inc.
13/671,527		United States	Methods And Apparatuses To Provide And Electro-Optical Alignment	Pending	Silicon Image, Inc.
14/371,973		United States	Charge Pump Calibration for Dual-Path Phase-Locked Loop	Pending	Silicon Image, Inc.
14/115,324		United States	Mechanism for Facilitating Dynamic Phase Detection with High Jitter Tolerance for Images of Media Streams	Allowed	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/135,470		United States	Apparatus, System and Method for Formatting Audio-Video Information	Pending	Silicon Image, Inc.
13/839,671		United States	Full Frame Buffer To Improve Video Performance In Low- Latency Video Communication Systems	Pending	Silicon Image, Inc.
12/057,051		United States	Bi-Directional Digital Interface For Video And Audio (DIVA)	Pending	Silicon Image, Inc.
11/760,164	7,940,809	United States	Digital Video Interface With Bi-Directional Half-Duplex Clock Channel Used As Auxiliary Data Channel	Issued	Silicon Image, Inc.
11/865,621	7,916,780	United States	Adaptive Equalizer For Use With Clock And Data Recovery Circuit Of Serial Communication Link	Issued	Silicon Image, Inc.
12/222,745	7,737,802	United States	Passive Equalizer With Negative Impedance To Increase A Gain	Issued	Silicon Image, Inc.
12/636,063	8,680,712	United States	Power Delivery Over Digital Interactive Interface For Video And Audio (DIIVA)	Issued	Silicon Image, Inc.
13/521,739		United States	Multi-Media USB Data Transfer Over Digital Interaction Interface for Video and Audio (DIIVA)	Pending	Silicon Image, Inc.
13/521,762		United States	Video Management And Control In Home Multimedia Network	Pending	Silicon Image, Inc.
14/381,186		United States	Linear Regulator with Improved Power Supply Ripple Rejection	Pending	Silicon Image, Inc.
13/844,152		United States	Electronic Alignment Of Optical Signals	Pending	Silicon Image, Inc.
14/391,382		United States	Frequency Response Compensation in a Digital to Analog Converter	Pending	Silicon Image, Inc.
14/165,340		United States	Apparatus, System and	Pending	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Method for Providing Switching with a T-Coil Circuit		Inc.
13/836,895	8,928,411	United States	Integration Of Signal Sampling Within Transistor Amplifier Stage	Issued	Silicon Image, Inc.
14/165,345		United States	Apparatus, Method and System for Asymmetric Full-Duplex Communication	Pending	Silicon Image, Inc.
14/209,785		United States	Method And Apparatus For Implementing Wide Data Range And Wide Common-Mode Receivers	Pending	Silicon Image, Inc.
14/296,377		United States	Transmitting Apparatus with Source Termination	Pending	Silicon Image, Inc.
14/368,781		United States	Caching of Capabilities Information of Counterpart Device for Efficient Handshaking Operation	Pending	Silicon Image, Inc.
14/163,981		United States	Mechanism for Facilitating Dynamic Counter Synchronization and Packetization in High-Definition Multimedia Interface and Mobile High-Definition Link	Pending	Silicon Image, Inc.
14/253,808		United States	Communication of Multimedia Data Streams Over Multiple Communication Lanes	Pending	Silicon Image, Inc.
14/279,316		United States	HDCP2.2 Authentication Engine and Stream Cipher Engine Sharing in Digital Content Protection Architectures	Pending	Silicon Image, Inc.
14/383,865		United States	Techniques for Fractional-N Phase Locked Loops	Pending	Silicon Image, Inc.
61/949,901		United States	Compressed Video Transfer Over HDMI and MHL	Pending	Silicon Image, Inc.
14/563,797		United States	Electrical Duplex to Optical Conversion	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/470,750		United States	Arbitration Signaling within a Multimedia High Definition Link (MHL 3) Device	Pending	Silicon Image, Inc.
14/275,692		United States	Error Detection and Mitigation in Video Channels	Pending	Silicon Image, Inc.
14/339,393		United States	Phase-Modulated On-Off Keying for Millimeter Wave Spectrum Control	Pending	Silicon Image, Inc.
14/145,715		United States	Messaging to Provide Data Link Integrity	Pending	Silicon Image, Inc.
14/145,736	8,854,548	United States	Mechanism for Memory Reduction in Picture-In-Picture Video Generation	Issued	Silicon Image, Inc.
14/470,613		United States	Compressed Video Transfer Over a Multimedia Link	Pending	Silicon Image, Inc.
14/184,647		United States	Video Frame Synchronization	Pending	Silicon Image, Inc.
14/181,446		United States	Power Delivery Over Digital Interaction Interface for Video and Audio (DiiVA)	Pending	Silicon Image, Inc.
14/470,804		United States	Phase Relationship Control for Control Channel of a Multimedia Communication Link	Pending	Silicon Image, Inc.
14/470,809		United States	Retry Disparity for Control Channel of a Multimedia Communication Link	Pending	Silicon Image, Inc.
61/943,267		United States	Pre-Processor and Post-Processor for Compression of 4:2:0 Encoded Video Streams with Video Compression Codecs Embedded within an Audio/Video Standard	Pending	Silicon Image, Inc.
14/278,255		United States	Encoding Guard Band Data for Transmission Via a Communications Interface Utilizing Transition-Minimized Differential Signaling (Tmds) Coding	Pending	Silicon Image, Inc.
14/322,753		United States	Calibration Of Single-Ended	Pending	Silicon Image,

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			High-Speed Interfaces		Inc.
61/947,704		United States	Reversible Connector	Pending	Silicon Image, Inc.
14/460,737		United States	System and Method for Transcoding Data	Pending	Silicon Image, Inc.
14/502,928		United States	Electrical Connector with Optical Channel	Pending	Silicon Image, Inc.
14/322,753		United States	Cable with Circuitry for Communicating Performance Information	Pending	Silicon Image, Inc.
61/973,837		United States	Error Correction for Transmission of Compressed Video Data Over Standards-Defined Coded Audio/Video Links	Pending	Silicon Image, Inc.
61/975,517		United States	(MHL) Connector Cable Detect, Cable Orientation Detect and/or Lane Re-Mapping	Pending	Silicon Image, Inc.
61/979,477		United States	MHL3 Router without HDCP2.2 Decryption and Encryption Operation	Pending	Silicon Image, Inc.
61/979,483		United States	TDD over 5-Pin Interface	Pending	Silicon Image, Inc.
14/470,620		United States	Compressed Blanking Period Transfer Over a Multimedia Link	Pending	Silicon Image, Inc.
14/273,400		United States	Transmission and Detection of Multi-Channel Signals in Reduced Channel Format	Pending	Silicon Image, Inc.
61/989,409		United States	System for Dynamic Capabilities, Status, and Metadata Exchange	Pending	Silicon Image, Inc.
14/300,166		United States	Configurable Multi-Dimensional Driver and Receiver	Pending	Silicon Image, Inc.
14/483,013		United States	Enhanced Communication Link Using Synchronization Signal as Link Command	Pending	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
62/043,218		United States	Run Length Programmable Unified Built-In Self-Test (BIST) Scheme for Various High-Speed Serial IO Standards	Pending	Silicon Image, Inc.
14/559,523		United States	Determination of Physical Connectivity Status of Devices Based on Electrical Measurement	Pending	Silicon Image, Inc.
14/516,136		United States	Method and System for Improving Serial Port Memory Communication Latency and Reliability	Pending	Silicon Image, Inc.
62/061,630		United States	Secure Control Communication Between an Application Processor and a Transmitter	Pending	Silicon Image, Inc.
62/075,554		United States	Metadata Transfer for HDMI/MHL	Pending	Silicon Image, Inc.
14/570,817		United States	Mechanism for Facilitating Dynamic Phase Detection with High Jitter Tolerance for Images of Media Streams	Pending	Silicon Image, Inc.
14/589,889		United States	Displaying Multiple Videos on Sink Device Using Display Information of Source Device	Pending	Silicon Image, Inc.
14/589,925		United States	Lower Power Operations in a Wireless Tunneling Transceiver	Pending	Silicon Image, Inc.
14/591,845		United States	Simultaneous Transmission of Clock and Bidirectional Data Over a Communication Channel	Pending	Silicon Image, Inc.
14/449095	20150036756	United States	Radio Frequency Interference Reduction In Multimedia Interfaces	Pending	Silicon Image, Inc.

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61/979,483	04/14/2014		260	30850-26578/US		

CONFIRMATION NO. 3383

120363
Silicon Image/FENWICK
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FILING RECEIPT

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Date Mailed: 04/30/2014

Receipt is acknowledged of this provisional patent application. It will not be examined for patentability and will become abandoned not later than twelve months after its filing date. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

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If Required, Foreign Filing License Granted: 04/29/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 61/979,483**

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

Title

TDD over 5-Pin Interface

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	30850-26578/US
	Application Number	
Title of Invention	TDD over 5-Pin Interface	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Ju	Hwan	Yi	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Sunnyvale	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	Silicon Image, Inc.
Address 2	1140 East Arques Avenue

City	Sunnyvale	State/Province	CA
Postal Code	94085	Country i	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Young	Il	Kim	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Sunnyvale	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	Silicon Image, Inc.
Address 2	1140 East Arques Avenue

City	Sunnyvale	State/Province	CA
Postal Code	94085	Country i	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Gijung		Ahn	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	30850-26578/US
	Application Number	
Title of Invention	TDD over 5-Pin Interface	

City	San Jose	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	Silicon Image, Inc.		
Address 2	1140 East Arques Avenue		
City	Sunnyvale	State/Province	CA
Postal Code	94085	Country i	US

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Min-Kyu		Kim	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	Sunnyvale	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	Silicon Image, Inc.		
Address 2	1140 East Arques Avenue		
City	Sunnyvale	State/Province	CA
Postal Code	94085	Country i	US

Inventor 5 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Daeyun		Shim	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	Saratoga	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	Silicon Image, Inc.		
Address 2	1140 East Arques Avenue		
City	Sunnyvale	State/Province	CA
Postal Code	94085	Country i	US

Inventor 6 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Gyudong		Kim	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	Sunnyvale	State/Province	CA	Country of Residence i	US

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	30850-26578/US
	Application Number	
Title of Invention	TDD over 5-Pin Interface	

Mailing Address of Inventor:

Address 1	Silicon Image, Inc.		
Address 2	1140 East Arques Avenue		
City	Sunnyvale	**State/Province**	CA
Postal Code	94085	**Country** i	US

Inventor 7 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hoon		Choi	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	Mountain View	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	Silicon Image, Inc.		
Address 2	1140 East Arques Avenue		
City	Sunnyvale	**State/Province**	CA
Postal Code	94085	**Country** i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	120363		
Email Address	ptoc@fenwick.com	Add Email	Remove Email

Application Information:

Title of the Invention	TDD over 5-Pin Interface		
Attorney Docket Number	30850-26578/US	**Small Entity Status Claimed**	☐
Application Type	Provisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)		**Suggested Figure for Publication (if any)**	

Filing By Reference :

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	30850-26578/US
	Application Number	
Title of Invention	TDD over 5-Pin Interface	

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	120363		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	30850-26578/US
	Application Number	
Title of Invention	TDD over 5-Pin Interface	

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) [i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country [i]	Filing Date (YYYY-MM-DD)	Access Code [i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	30850-26578/US
	Application Number	
Title of Invention	TDD over 5-Pin Interface	

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◯ Assignee	◯ Legal Representative under 35 U.S.C. 117	◯ Joint Inventor
◯ Person to whom the inventor is obligated to assign.	◯ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	Silicon Image, Inc.

Mailing Address Information:

Address 1	1140 East Arques Avenue		
Address 2			
City	Sunnyvale	**State/Province**	CA
Country [i]	US	Postal Code	94085
Phone Number		Fax Number	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	30850-26578/US
	Application Number	
Title of Invention	TDD over 5-Pin Interface	

Email Address	

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/Michael W. Farn/			Date (YYYY-MM-DD)	2014-04-14
First Name	Michael W.	Last Name	Farn	Registration Number	41015

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	30850-26578/US
	Application Number	
Title of Invention	TDD over 5-Pin Interface	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

TDD over 5-Pin Interface

CONTENTS

[0001] This disclosure includes the following sets of figures:

[0002] "MHL3plus" – which describes an overall architecture for MHL3plus.

[0003] "TDD based Full Duplex" – which describes a TDD based full duplex approach.

DELL/HP/LENOVO EXHIBIT 1031, Page 276

What is claimed is:

1. A method for TDD based full-duplex communication.

2. A method for TDD based communication over 5-pin interface.

DELL/HP/LENOVO EXHIBIT 1031, Page 277

MHL3plus

- **MHL3Plus**
  - Architecture Overview
  - Design Target
    - Micro-packet structure for A/V-data and USB-data
    - Initialization
  - Details
    - TxPLL
    - TP1 eye
    - Pre-emphasis, Cable, and Reference EQ
    - Fast phase locking of CDR
    - Auto-EQ
- **Summary**

DELL/HP/LENOVO EXHIBIT 1031, Page 279

Architecture Overview [1]

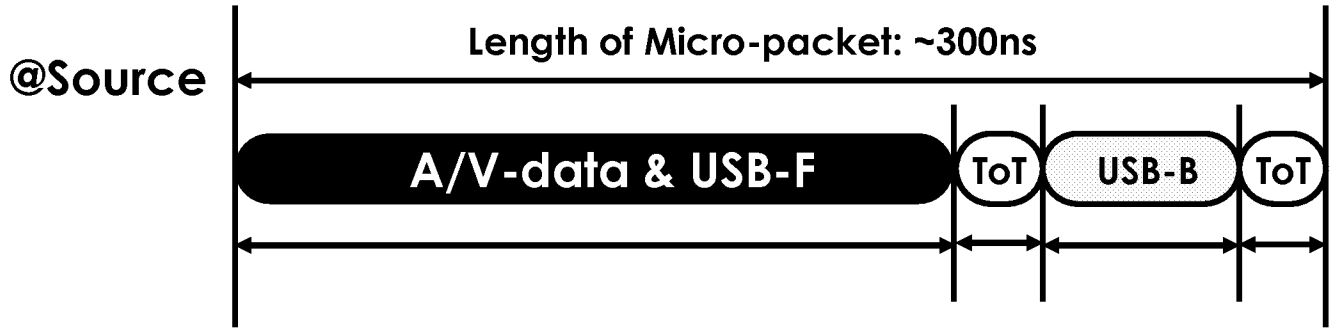
- **Definition of "MHL3Plus"**
  - MHL3-single-lane + USB2.0 simultaneous transfer over D+/D- (of μUSB) using Time-Division-Multiplexing (TDM)

  - Data types in MHL3Plus
    - **MHL3-SL Over "D+/D-"**
      - A/V data bandwidth up to 6Gbps
        - Transfer "Uni-directional" A/V data, compressed or non-compressed, from the Source to the Sink
    - **MHL3-SL Over "eCBUS_S"**
      - Clock (source-synchronous or clock-forwarding)
        - Transfer "Reference Clock" from the source to the Sink
      - Side-band channel up to 75Mbps
        - Transfer control data between the Source and the Sink as FULL bi-directional way
    - **Possibly plus Simultaneous USB2.0 data transfer over D+/D-**
      - USB2.0 data (half-duplex by nature) up to 480Mbps per each direction
        - Transfer 600Mbps of USB2.0 after coding in each direction by using micro-packet (or Packetization) in "Full-duplex & TDM" manner (Not Half-duplex)

DELL/HP/LENOVO EXHIBIT 1031, Page 280

Architecture Overview [2]

- **TDM (Time-Division Multiplexing) & Micro-packet**
  - Merge A/V and {USB-forward + USB-backward} into Micro-packet
    - Micro-packet is comprised of
      - #1. Forward data (A/V + USB-Forward), from the Source to the Sink
      - #2. **Turn-over-Time (ToT)**
      - #3. Backward data (USB-Backward), from the Sink to the Source
      - #4. **Turn-over-Time (ToT)**
  - The length of Micro-packet determines the latency of USB data
    - In one implementation, packet length is **not be bigger than 300ns**!
  - The source and the sink are Frequency-locked thru eCBUS-S
    - So, fast Turn-Over can be doable w/o requiring frequency re-lock

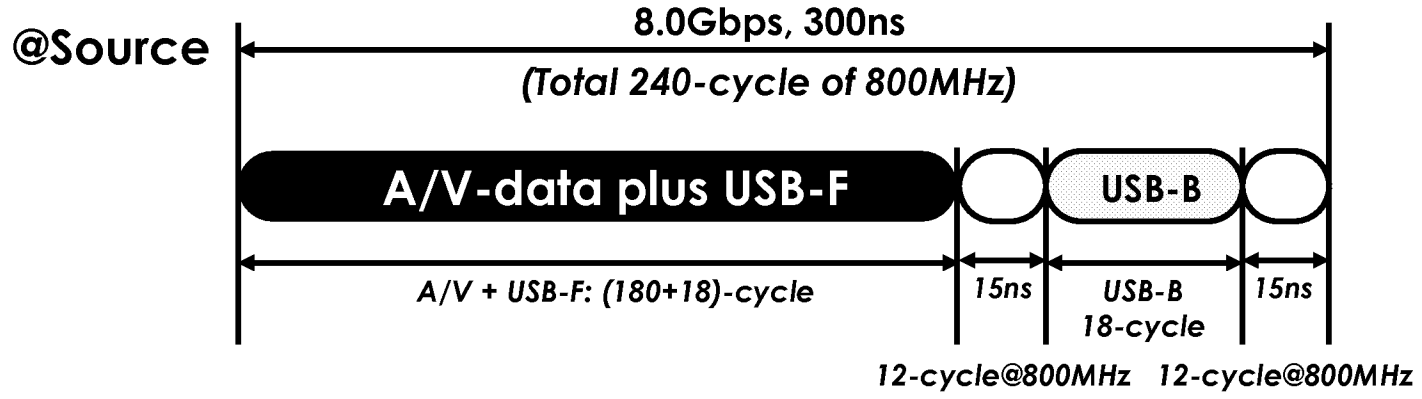


Drawing of Micro-packetization of MHL3Plus

DELL/HP/LENOVO EXHIBIT 1031, Page 281

Architecture Overview [3]

- TMD & Micro-packet **(Cont.)**
  - Link-speed of MHL3Plus depends on Bandwidth of A/V data and ToT
    - Bandwidth of A/V data of MHL3-SL
      - Up to 1080P60, uncompressed: <4.5Gbps
      - Up to WQXGA@60, uncompressed: <5.4Gbps
      - Up to 4K@30, uncompressed: <6.0Gbps
    - USB2.0 data:
      - 600Mbps (or 0.6Gbps) per each direction: ~1.2Gbps,max,Total
    - So, minimum link-speed of MHL3Plus becomes
      - 4.5/5.4/6.0Gbps + 2*(0.6Gbps) + 2*ToT
      - [Note] ToT determines cable length: ~4.5ns/meter
  - Micro-packet structure (A/V-BW: 6Gbps)

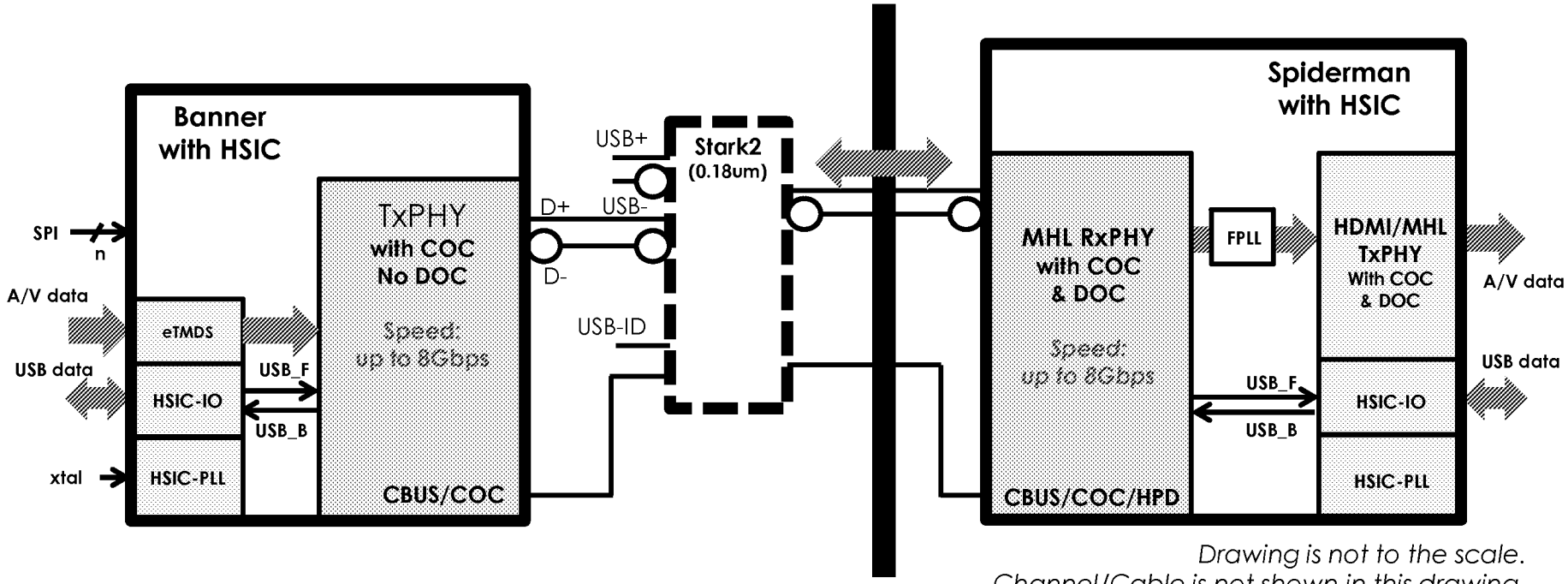


DELL/HP/LENOVO EXHIBIT 1031, Page 282

Architecture Overview

[4]

MHL3Plus System view (Banner to Spiderman)



Drawing is not to the scale.
Channel/Cable is not shown in this drawing.

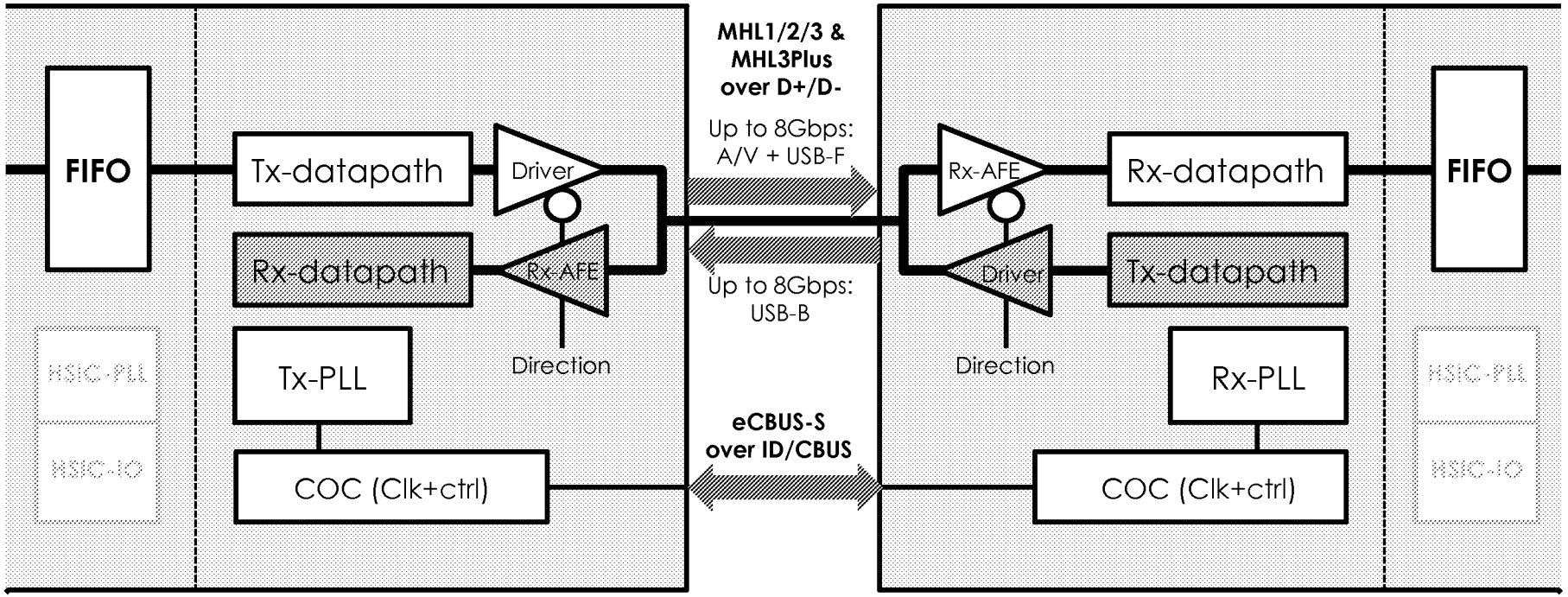
- Banner and Spiderman are MHL3Plus chips.

DELL/HP/LENOVO EXHIBIT 1031, Page 283

Architecture Overview

[5]

- **MHL3Plus More details on PHYs and Interface to Logic**
  - MHL3Plus_Tx to MHL3Plus_Rx; Banner TxPHY to Spiderman RxPHY

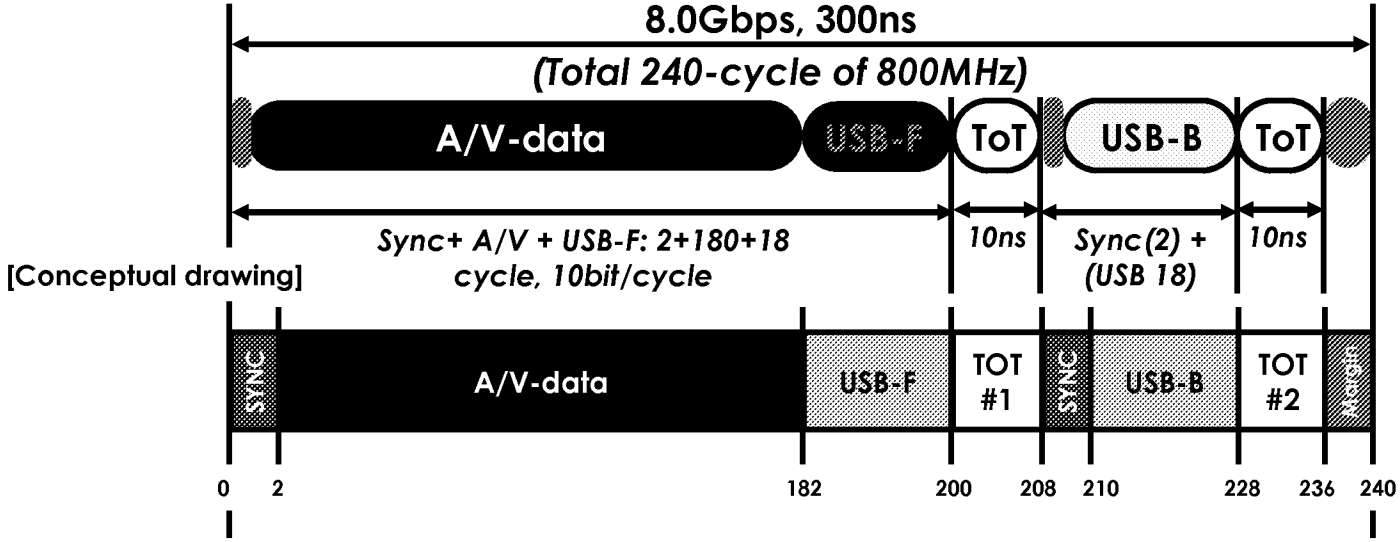


- Banner: Improved Titan plus one lane of Rx-path
- Spiderman: Improved Rogue plus one lane of Tx-path
- [Note] eCBUS-S makes Banner/Spiderman "Frequency-Locked"

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Design Target [1]

- **Structure of Micro-Packet (Revisited)**
  - Clarify SYNC, Data, ToT, and Margin
  - TDM may have "3" mode of operations depending on Max A/V-BW

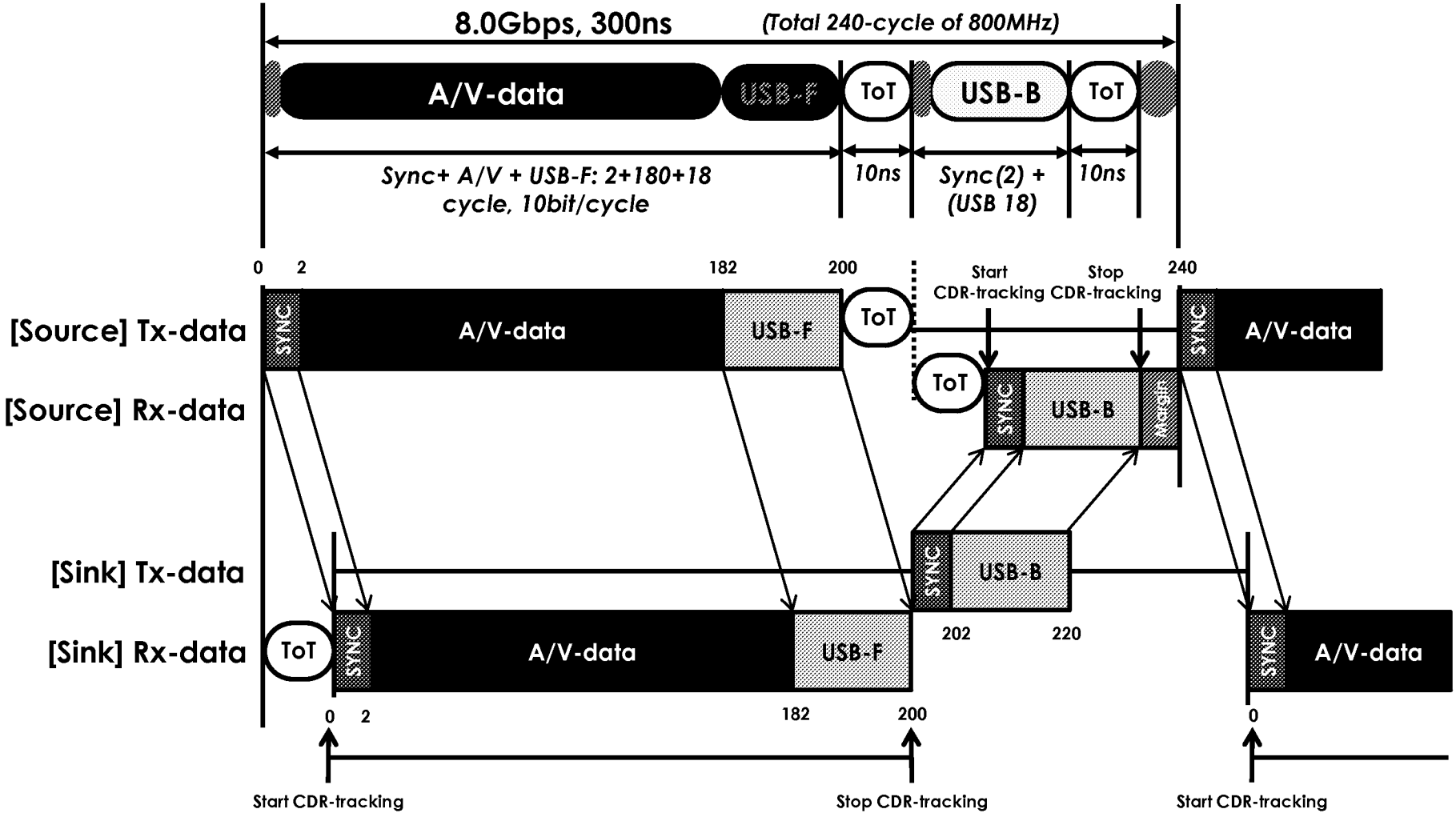


A/V Bandwidth	Packet length	Link speed	A/V Sync (Byte)	A/V-data (Byte)	USB-F Data (Byte)	TOT #1 (Byte)	USB-B Sync (Byte)	USB-B Data (Byte)	TOT #2 (Byte)	Margin	Total (Byte)
<6.0Gbps	300ns	8.0Gbps	2	180	18	8 (10ns)	2	18	8 (10ns)	4	240
<5.4Gbps	300ns	7.6Gbps	2	162	18	11 (14ns)	2	18	11 (14ns)	4	228
		7.467Gbps	2	162	18	9 (11ns)	2	18	9 (11ns)	4	224
<4.5Gbps	300ns	6.6Gbps	2	135	18	10 (14ns)	2	18	10 (14ns)	4	198

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Design Target [2]

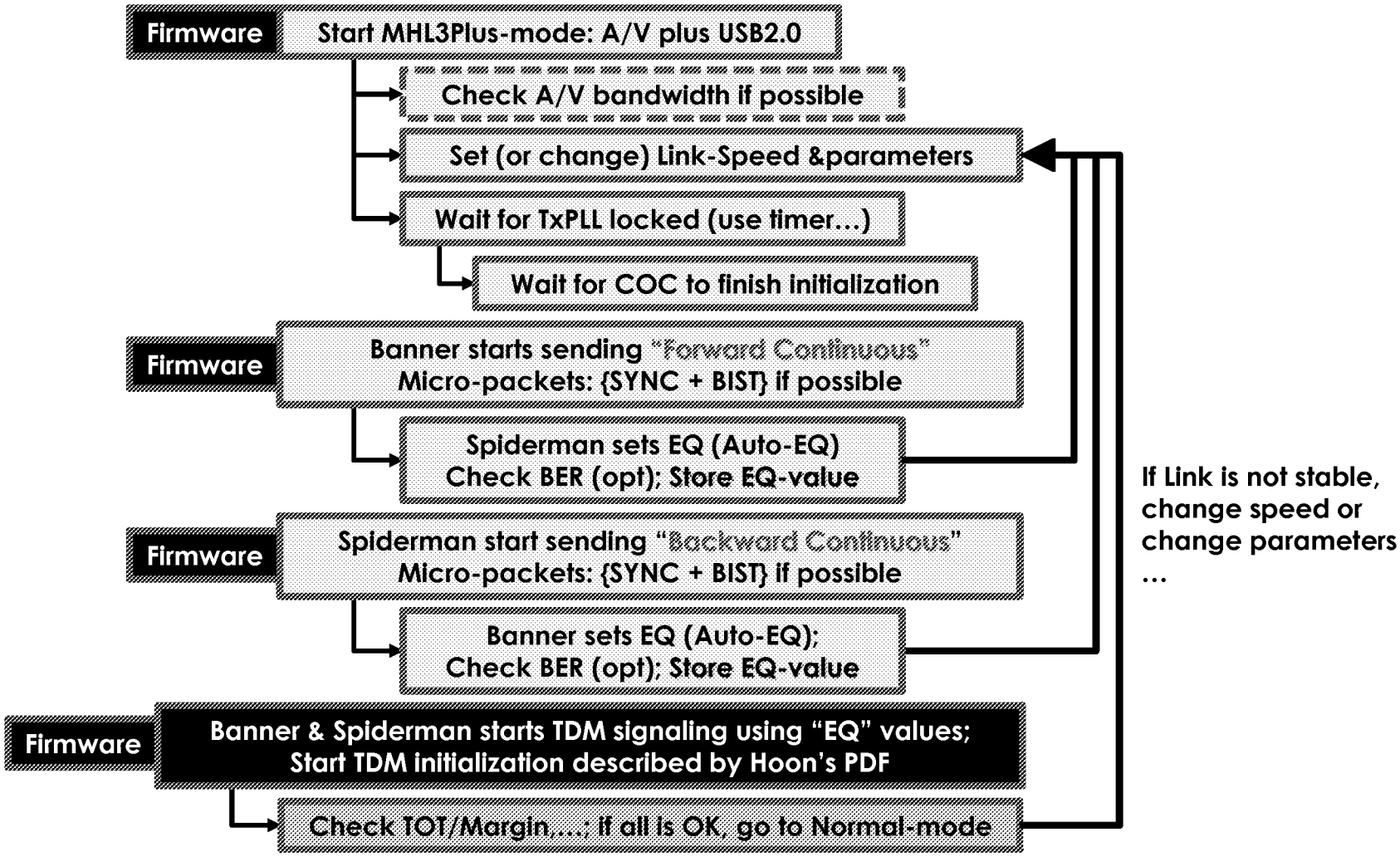
- Structure of Micro-Packet **(Cont.)**
  - Illustration of Packets seen at the Source and the Sink, for 8Gbps case



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Design Target [3]

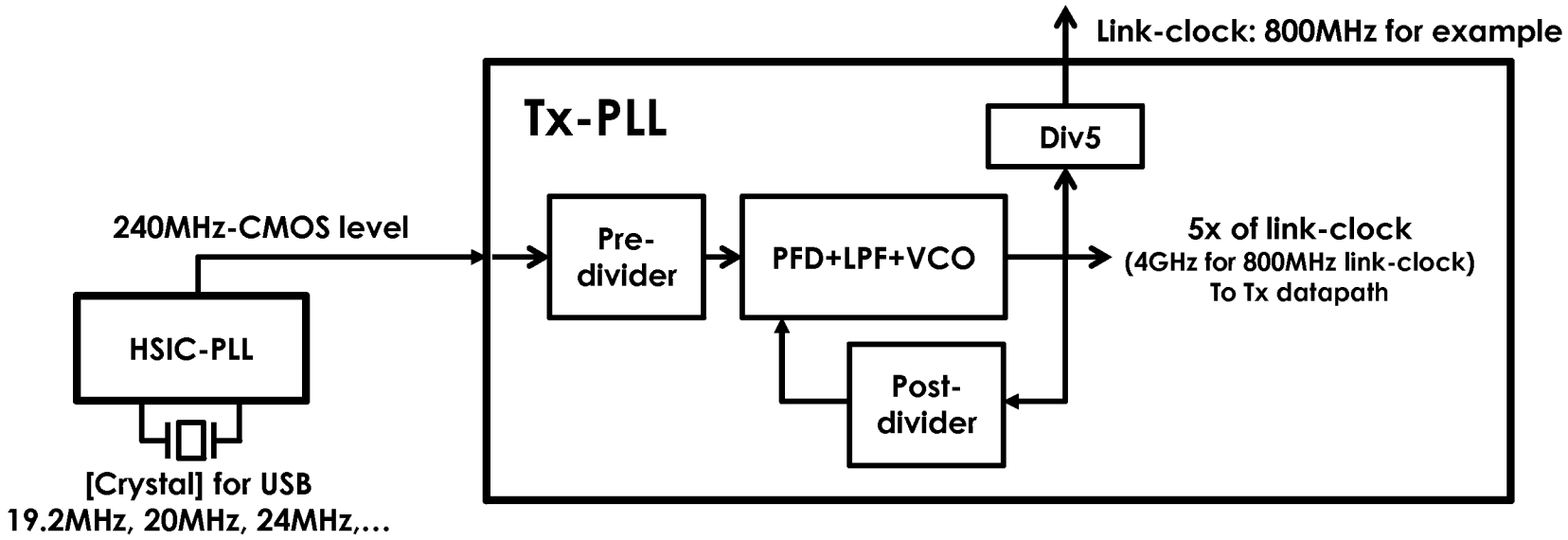
- **Initialization procedure example**
  - Set EQ, TDM_Init_define, and to go into the Normal TDM mode



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TxPLL

- **Generating Link-clock frequency from 240MHz**
  - Examples of target link-clock-frequency (the lower, the better)
    - Candidates for 6Gbps-A/V-BW: 800MHz, 810MHz, 820MHz, 840MHz
    - ***For 800MHz → 240MHz*[100/6] → Pre-divider of "6" and multiplication of "100"***
    - For 820MHz → 240MHz*[205/12] → Pre-divider of "12" and Multi of "205" (=5*41)
    - For 840MHz → 240MHz*[**70/4**] → Pre-divider of "4" and multiplication of "70"
    - Candidates for 5.4Gbps-A/V-BW: **750MHz**, **760MHz**, 780MHz
    - For 750MHz → 240MHz*[125/8] → Pre-divider of "8" and multiplication of "125"
    - ***For 760MHz → 240MHz*[95/6] → Pre-divider of "6" and multiplication of "95" (=5*19)***
    - ***For 746.6667MHz → 480MHz*[14*5/9] → Using 480MHz; Div 9 and Multi 70.***
    - For 780MHz → 240MHz*[65/4] → Pre-divider of "4" and multiplication of "65" (=5*13)
    - Candidates for 4.5Gbps-A/V-BW: 650MHz, **660MHz**, 670MHz
    - For 650MHz → 240MHz*[65/24]
    - ***For 660MHz → 240MHz*[55/4] → Pre-divider of "4" and Multiplication of 55 (=5*11)***

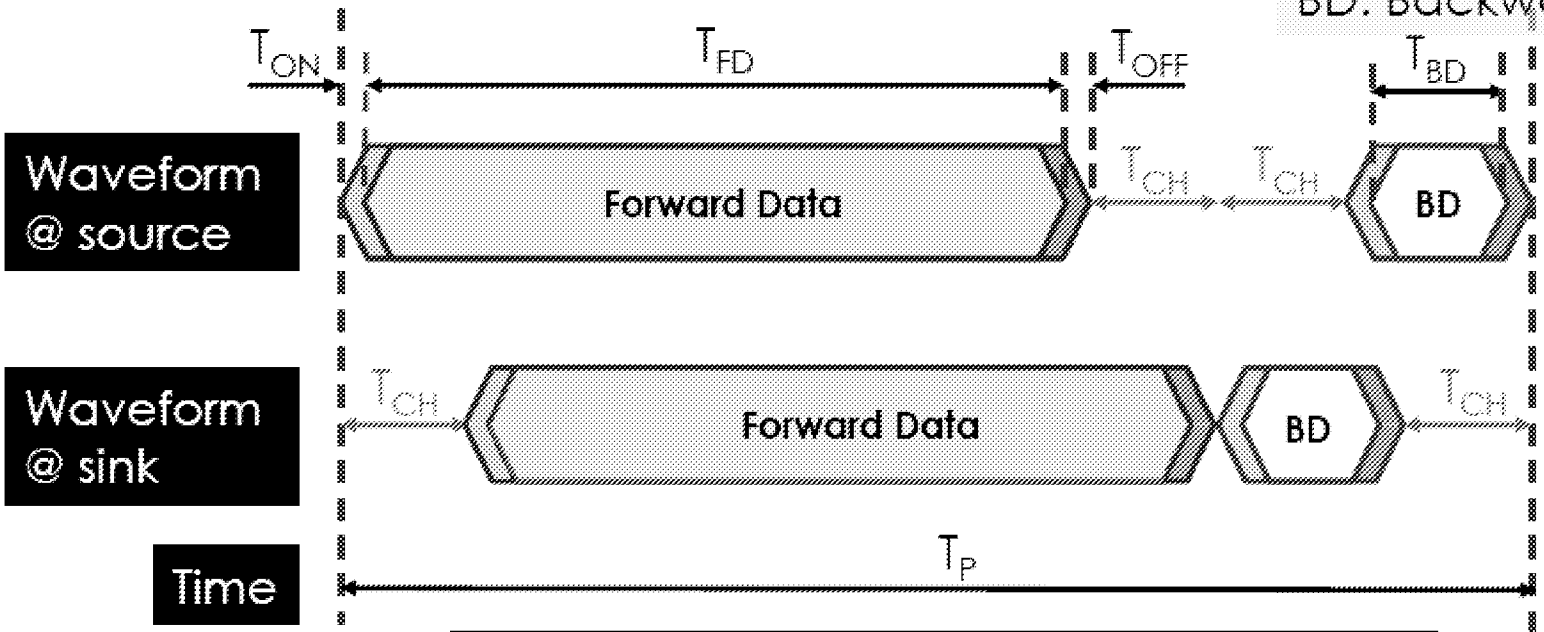


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TDD based Full-Duplex

Waveform and Timing @ Source & Sink

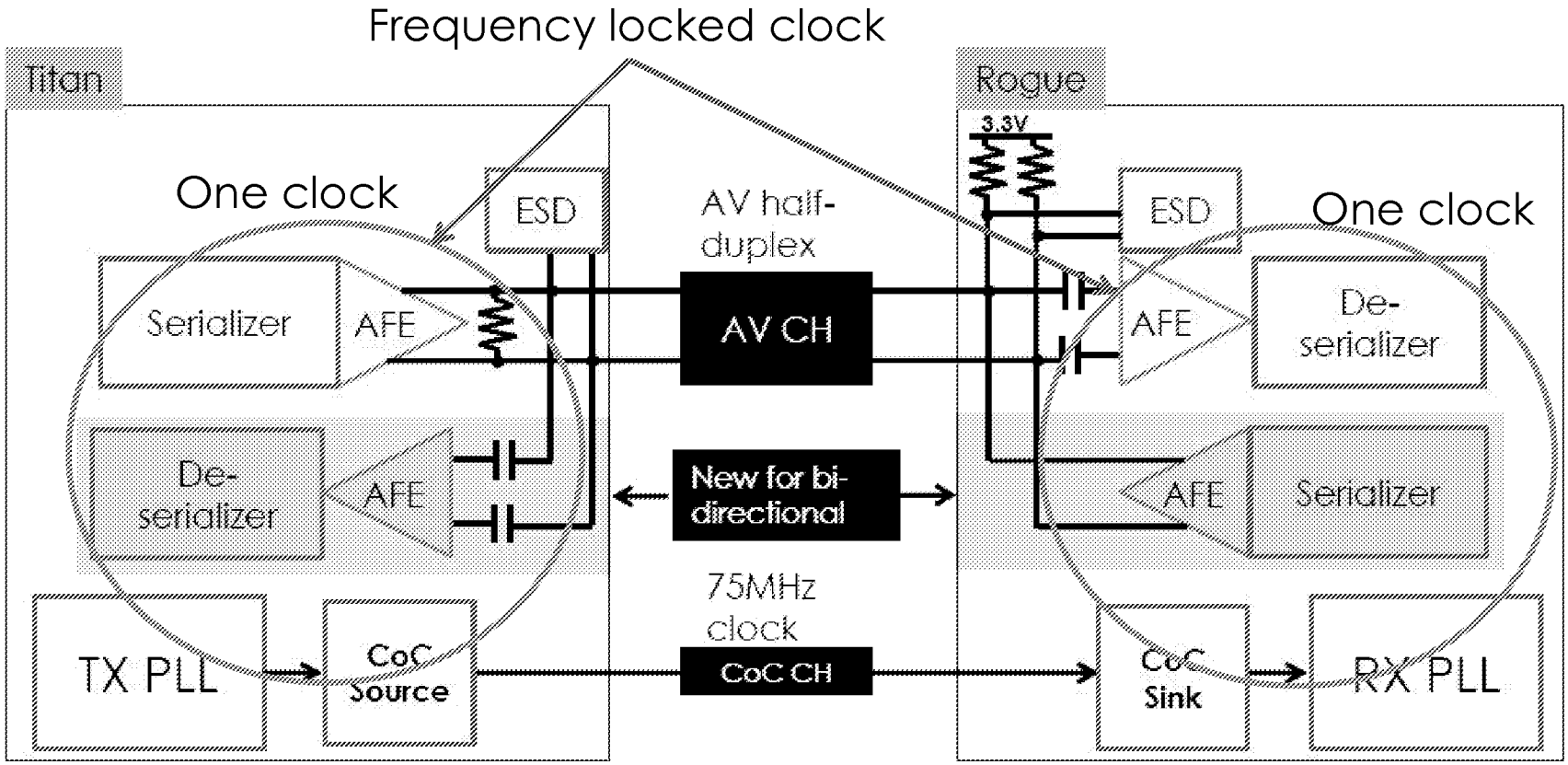
BD: Backward Data



Symbol	Definition
T_P	Period of Time Division Multiplexing
T_{CH}	Channel delay time
T_{FD}	Forward data time slot
T_{BD}	Backward data time slot
T_{ON}	Driver ON time
T_{OFF}	Driver OFF time
ToT	$T_{ON}+T_{OFF}+T_{CH}$

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Clock Relationship



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TDM Slot Calculation

- USB packet should not be "empty" in order not to increase the latency. This means that in one TDM cycle time (T_p), there should be an integer # of 8b USB raw data
  - T_p = 1/60M * n_1 where 1/60M is the USB slot time (i.e., one byte of USB data to fill one of TDM slot) and n_1 is the number of USB data
- TDM cycle time does not need to be an integer multiple relationship w/ AV data due to the packet structure for AV that allows IDLEs, splits, etc.
  - $T_p \neq 1/f_{av} * n$
- One TDM cycle includes integer number of TDM slots
  - $T_{link} = T_p/n_2$ where T_{link} is one TDM slot time and n_2 is the number of slots to cover AV, forward USB, backward USB, 2ToTs, 2 of symbol SYNC time, packet overhead, and margin
  - $n_2 \geq AV + F\text{-}USB + B\text{-}USB + 2SYNC + 2ToTs = n_{av} + 2n_1 + n_{2ToT} + 2n_{sync} + n_{margin}$

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TDM Slot Calculation (Cont'd)

- Link clock comes from a PLL using 24MHz as a reference (USB reference clock)
  - $f_{link} = 1/T_{link} = 24MHz * m_3/n_3$
  - Since $T_{link} = T_p/n_2$ and $T_p=n_1/60MHz$, $f_{link} = n_2/T_p = n_2/n_1 * 60MHz = 24MHz * m_3/n_3$
  - Thus, $m_3/n_3 = n_2/n_1 * 60/24 = n_2/n_1 * 5/2$
- For example, for $T_p \approx 300ns$, $2ToT \approx 20ns$, $f_{link} \approx 800MHz$ (for 8Gbps; one slot is about 1.25ns), and 6.237Gbps AV
  - $n_1 = 300ns * 60MHz = 18$ slots
  - $n_2 \geq AV + 2n_1 + 2ToTs$ = slots for 6.273Gbps AV for T_p + 36 + slots for 20ns ≈ 300ns * 627.3MHz + 36 + 16 = 188.19 + 36 + 16 = 241
    - SYNC time and margin time are ignored for simplicity
  - $f_{link} = n_2/n_1 * 60MHz = 241/18*60 = 803.333... = 24MHz * m_3/n_3$ where $m_3=n_2*5=1205$ and $n_3=n_1*2=36$

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TDM Slot Calculation (Cont'd)

- Use TDD_latency excel sheet
  - Put the numbers in green boxes. Excel will do three iterations of calculation and emits the final values

1st iteration				
Target values	BW_{link}	Link BW (Gbps)	7.9	Inputs From Sheet1X27
	T_{2TOT}	Time for 2 of ToT (ns)	20	
	BW_{av}	BW for AV (Gbps)	5.4	
	n_1	# of 8b USB raw data in one TDM cycle time; # of slots for USB data in T_p	18	Recommended value = 18
	BW_{usb}	USB BW before 10b coding (Mbps)	480	USB2.0
	n_{sync}	# of slots for symbol sync	4	
	n_{margin}	# of slots for margin	4	
Results	f_{link}	# of link slots per sec (MHz)	790	BW_{link}/10 for 10b coding
	T_p	TDM cycle time; u-packet size (ns)	300	$n_1/(BW_{usb}/8)$; should be less than 300ns for latency
	f_{av}	# of slots for AV per sec (MHz)	536	BW_{av}/10 for 10b coding
	n_{av}	# of AV slots needed in T_p	161	Roundup(f_{av} * T_p)
	n_{2TOT}	# of slots for 2 of ToT	16	Roundup(T_{2TOT}/T_{link})
	T_{2TOT}	Time for 2 of ToT (ns)	20.3	
	$n_{2\text{-}min}$	min # of total link slots in T_p	221	$n_{av}+2n_1+n_{2TOT}+2n_{sync}$
	n_2	# of total link slots in T_p	225	$n_{2\text{-}min}+n_{margin}$
	f_{link}	# of link slots per sec (MHz)	750.0	n_2/n_1*60MHz
	m_3	$f_{linkslot}$=24MHz * m_3/n_3 (PLL division ratio)	1125	n_2*5
	n_3	$f_{linkslot}$=24MHz * m_3/n_3 (PLL division ratio)	36	n_1*2
Summary				
	BW_{av}	BW for AV (Gbps)	5.4	
	T_{2TOT}	Time for 2 of ToT (ns)	20.1	
	T_p	TDM cycle time; u-packet size (ns)	300	
	BW_{link}	Link BW (Gbps)	7.5	
	n_{av}	# of AV slots needed in T_p	161	
	n_{usb}	# of USB slots in T_p for fwd/bwd	18	
	n_{2TOT}	# of slots for 2 of ToT	15	
	n_{fwd}	# of slots in forward time	179	
	n_{bwd}	# of slots in backward time	18	
	n_{sync}	# of slots for symbol sync	4	
	n_{margin}	# of slots for margin	4	
	n_{total}	# of total slots in T_p	224	$n_{fwd}+n_{bwd}+n_{2TOT}+2n_{sync}+n_{margin}$
	f_{link}	# of link slots per sec (MHz)	746.7	
	m_3	$f_{linkslot}$=24MHz * m_3/n_3 (PLL division ratio)	1120	
	n_3	$f_{linkslot}$=24MHz * m_3/n_3 (PLL division ratio)	36	

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TDM Slot Calculation (Cont'd)

- Examples

BW_{av}	BW for AV (Gbps)	6.0
T_{2TOT}	Time for 2 of ToT (ns)	20.8
T_p	TDM cycle time; u-packet size (ns)	300
BW_{link}	Link BW (Gbps)	8.2
n_{av}	# of AV slots needed in T_p	180
n_{usb}	# of USB slots in T_p for fwd/bwd	18
n_{2TOT}	# of slots for 2 of ToT	17
n_{fwd}	# of slots in forward time	198
n_{bwd}	# of slots in backward time	18
n_{sync}	# of slots for symbol sync	4
n_{margin}	# of slots for margin	4
n_{total}	# of total slots in T_p	245
f_{link}	# of link slots per sec (MHz)	816.7
m_3	$f_{linkslot}$=24MHz * m_3/n_3 (PLL division ratio)	1225
n_3	$f_{linkslot}$=24MHz * m_3/n_3 (PLL division ratio)	36

BW_{av}	BW for AV (Gbps)	4.5
T_{2TOT}	Time for 2 of ToT (ns)	21.3
T_p	TDM cycle time; u-packet size (ns)	300
BW_{link}	Link BW (Gbps)	6.6
n_{av}	# of AV slots needed in T_p	135
n_{usb}	# of USB slots in T_p for fwd/bwd	18
n_{2TOT}	# of slots for 2 of ToT	14
n_{fwd}	# of slots in forward time	153
n_{bwd}	# of slots in backward time	18
n_{sync}	# of slots for symbol sync	4
n_{margin}	# of slots for margin	4
n_{total}	# of total slots in T_p	197
f_{link}	# of link slots per sec (MHz)	656.7
m_3	$f_{linkslot}$=24MHz * m_3/n_3 (PLL division ratio)	985
n_3	$f_{linkslot}$=24MHz * m_3/n_3 (PLL division ratio)	36

BW_{av}	BW for AV (Gbps)	5.4
T_{2TOT}	Time for 2 of ToT (ns)	21.2
T_p	TDM cycle time; u-packet size (ns)	300
BW_{link}	Link BW (Gbps)	7.5
n_{av}	# of AV slots needed in T_p	162
n_{usb}	# of USB slots in T_p for fwd/bwd	18
n_{2TOT}	# of slots for 2 of ToT	16
n_{fwd}	# of slots in forward time	180
n_{bwd}	# of slots in backward time	18
n_{sync}	# of slots for symbol sync	4
n_{margin}	# of slots for margin	4
n_{total}	# of total slots in T_p	226
f_{link}	# of link slots per sec (MHz)	753.3
m_3	$f_{linkslot}$=24MHz * m_3/n_3 (PLL division ratio)	1130
n_3	$f_{linkslot}$=24MHz * m_3/n_3 (PLL division ratio)	36

	Format	No comp	2x comp	3x comp
4K60	444	18.0	9.0	6.0
	422 PP	12.0	6.0	4.0
4K30	444	9.0	4.5	3.0
	422 PP	6.0	3.0	2.0
1080p	444	4.5	2.3	1.5
	422 PP	3.0	1.5	1.0
WQXGA RB	444	8.0	4.0	2.7
	422 PP	5.4	2.7	1.8
QHD	444	9.4	4.7	3.1
	422 PP	6.2	3.1	2.1

YCbCr 422 PP can't be compressed using FBC/DSC

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Host and Device FSM

- FSM of Host and that of Device are asymmetric
- Host decides the TDM period and Device re-syncs each time to follow the TDM period of Host
- Tx and Rx of Host use the same single clock
  - Tx sends out packet based on the clock
  - Rx PLL generates OSD using the clock and gives the OSD to DPLL that is running on the same clock
  - Same to those of Device
- The clock used in Host and that used in Device are frequency locked but can be different in phase
- The symbol boundary of incoming data for Rx won't be aligned w/ that of outgoing data (i.e., TDM of Tx and that of Rx won't be aligned) since the symbol boundary in Rx side is decided by the Rx clock, channel delay, etc. So, the TDM slot will be skewed. However, still the clock in Tx and Rx are the same in Host/Device (due to oversampling architecture, i.e., only data recovery)

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Host FSM

- 1: Initial state
- 2: Send a long SYNC for Rx to be ready for starting
- 3: Tx mode
  - Starts TDM for Tx packet (reference TDM of Host)
  - Send SYNC, AV, and FWD-USB
- 4: Rx mode
  - Turn on T/O counter and wait for incoming SYNC
  - If SYNC comes in
    - SYNC aligns symbol boundary for Rx DPLL
    - Starts TDM for Rx packet
      - This TDM may not be aligned w/ that of Tx due to flight time, etc. though clock itself is same to that of Tx (only one clock is used)
      - This TDM is to know the end of BWD packet
    - Receives BWD-Data
  - If there comes no SYNC till T/O, go to #5
- 5: Wait for the Tx-TDM (reference TDM) reaches T_p
- 6: Go to #3

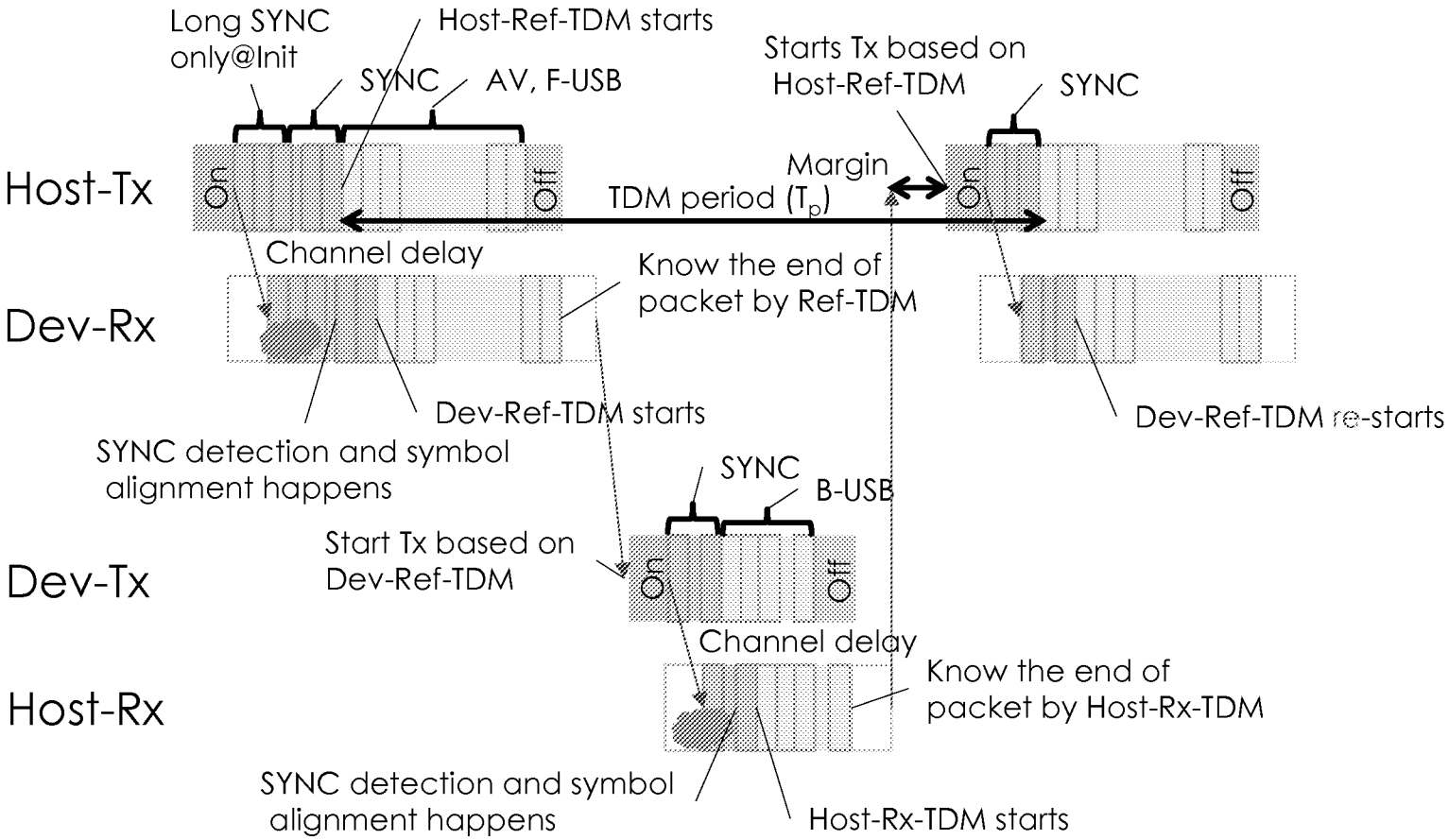
DELL/HP/LENOVO EXHIBIT 1031, Page 297

Device FSM

- 1: Initial state
- 2: Wait for a long SYNC
- 3: Rx mode
  - Wait for incoming SYNC
    - There is no time out. Device waits here till SYNC comes in
  - If SYNC comes in
    - SYNC aligns symbol boundary for Rx DPLL
    - Starts TDM for Rx packet (reference TDM)
      - This TDM is to used as a reference TDM till the end of TX mode. A new TDM starts in the next Rx mode
    - Receives AV and FWD-Data
    - Based on the TDM, if packet ends, move to #4
- 4: Tx mode
  - Send SYNC, AV, and FWD-USB
- 5: Go to #3

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Host and Device TDM



- Host's ref-TDM is not readjusted – master TDM
  - Host-Rx-TDM is just for the detection of the end of incoming packet
- Device's ref-TDM readjusts every time when it gets incoming packet
- Rx TDM and Tx TDM are not aligned

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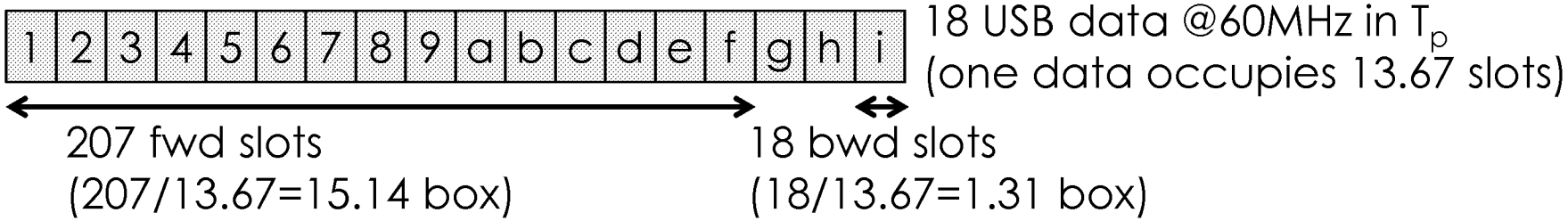
Buffering of USB data in Tx side

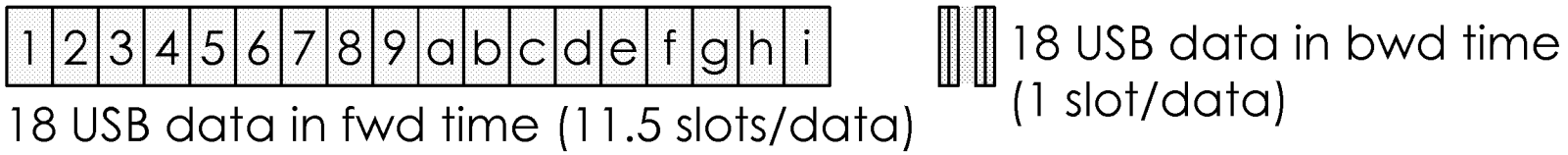
- How many USB data to accumulate before staring to fill the slots in TDM?
  - If we wait for a whole Tp, safe but add too much latency
  - If we wait too much less, in the middle of transaction, there will be no USB data to send over a USB slot
- Same to Tx latency

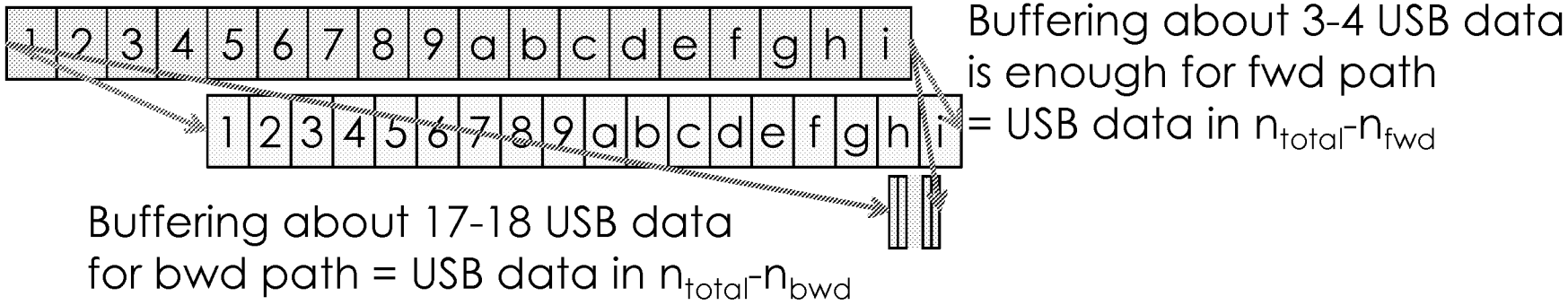
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Buffering of USB data in Tx side (Cont'd)

- For n_{total} = 246, n_{fwd}=207 (189 for AV and 18 for USB), n_{bwd}=18, n_{margin}=4, n_{2tot}=17 case

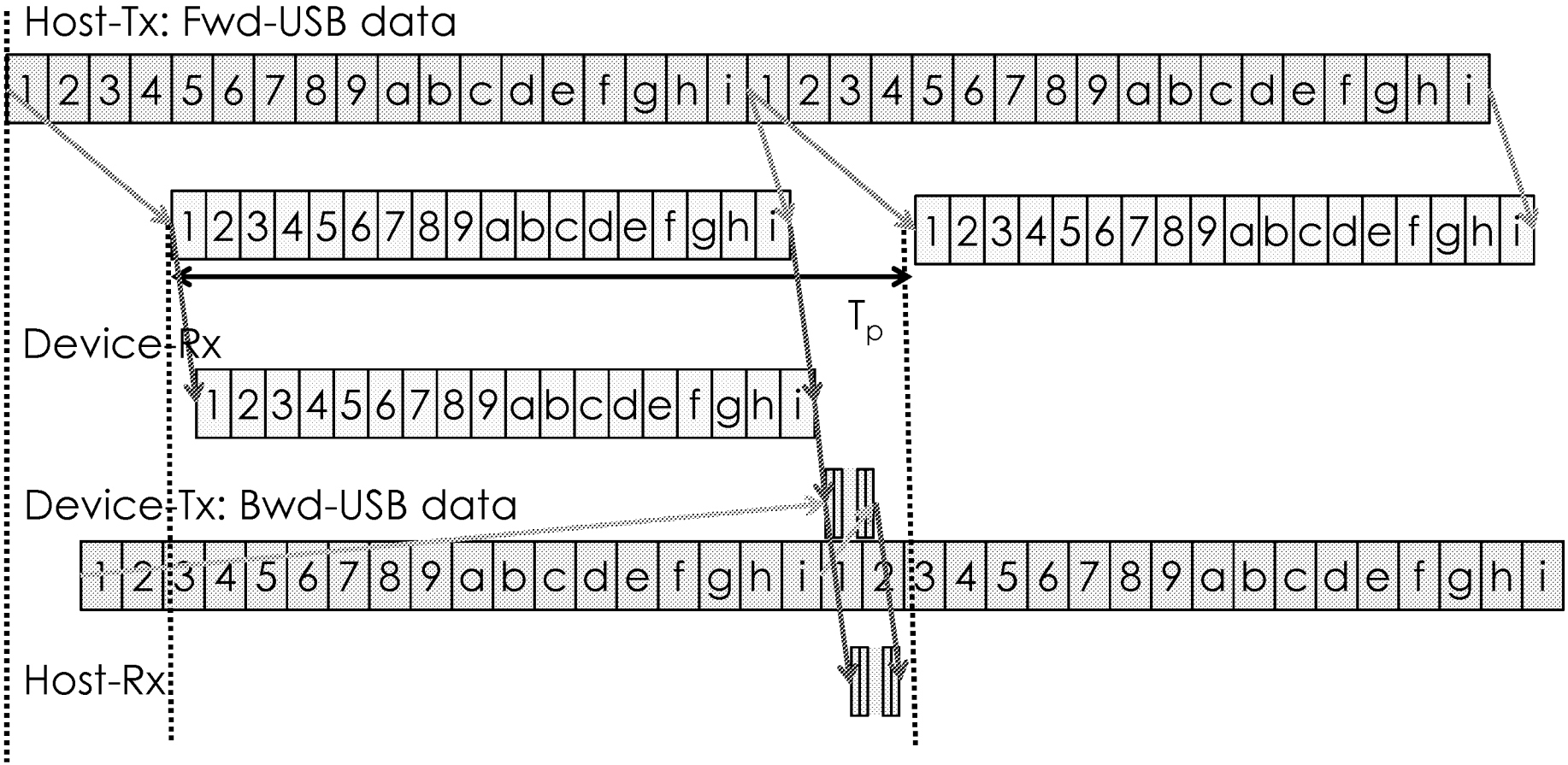






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Buffering of USB data in Tx side (Cont'd)



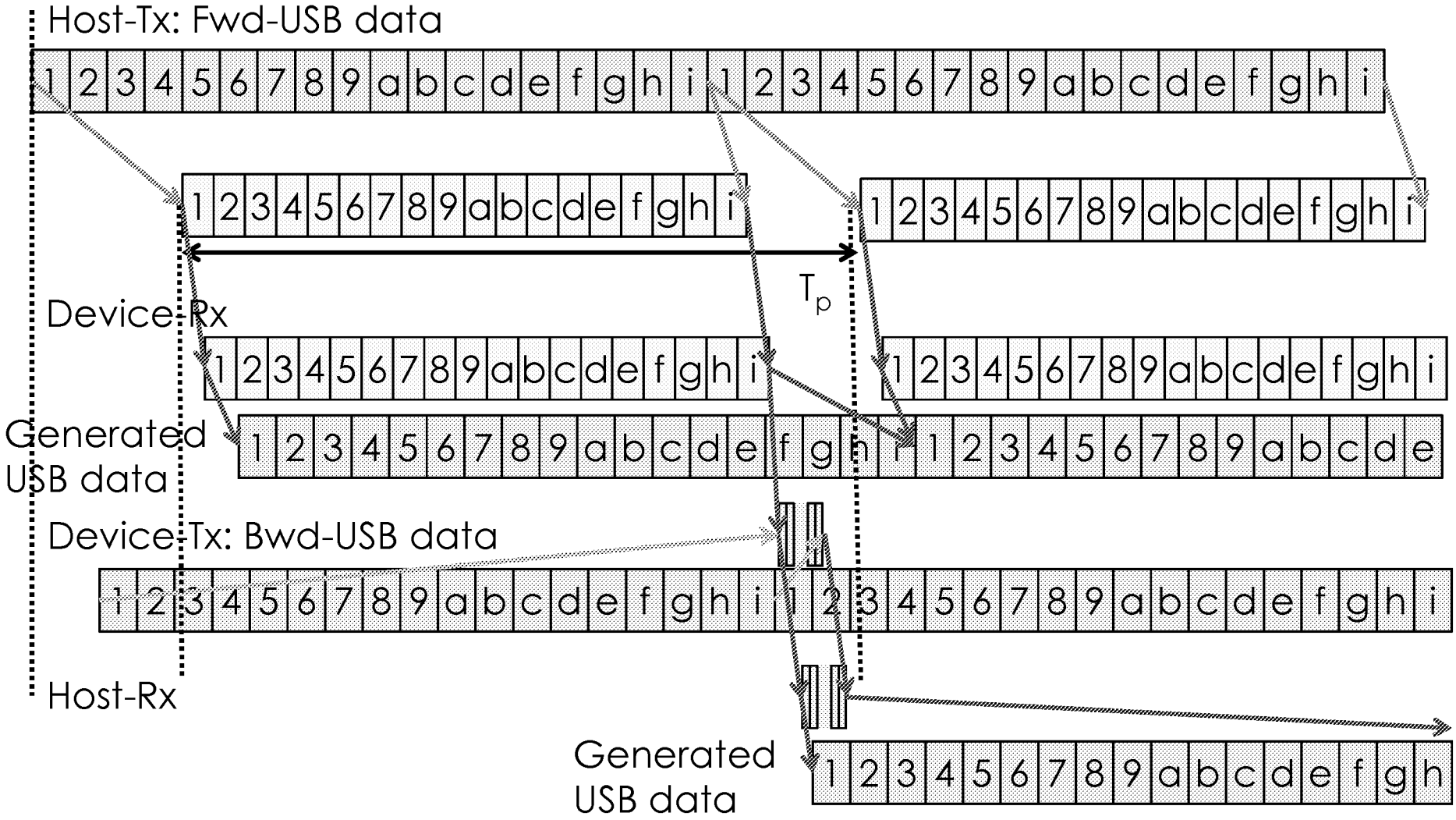
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Buffering of USB data in Rx side

- How many USB data coming over the link should be accumulated before Rx starts to generate the USB data?
  - Due to the fast speed of slots, Rx can start to generate USB data as soon as it gets USB slot
- Same to Rx latency

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Buffering of USB data in Rx side (Cont'd)



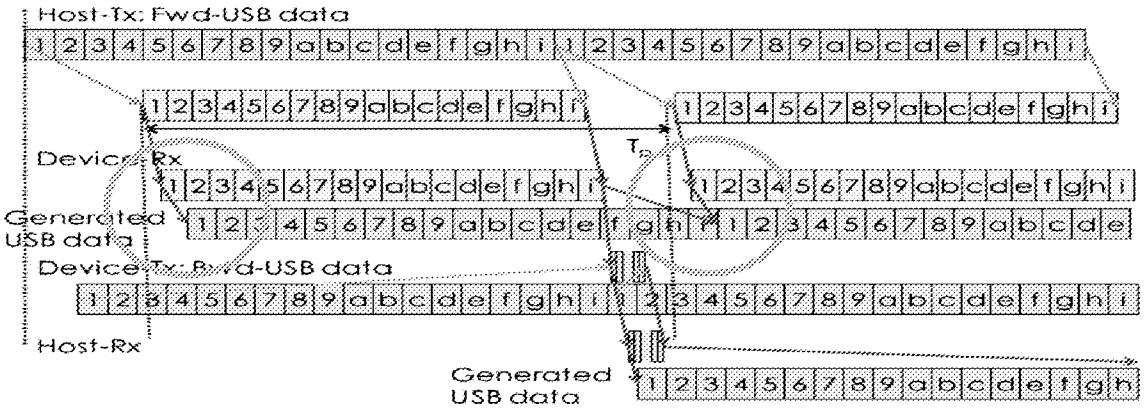
DELL/HP/LENOVO EXHIBIT 1031, Page 304

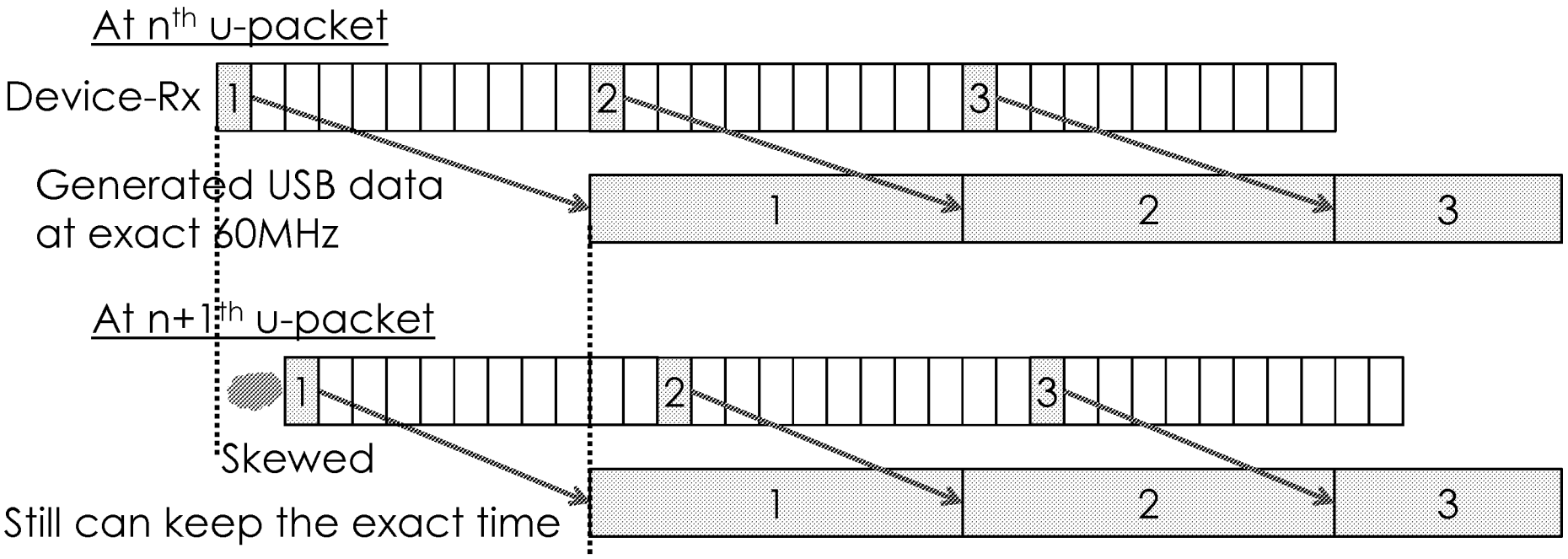
Buffering of USB data in Rx side (Cont'd)

- Due to the delay of cable, jitter of Rx clock, phase relationship between Rx clock and Tx clock, etc. the SYNC detection time can be skewed some clock cycles and it can skew Rx slot position by one slot position
- This skew is not a permanent skew. It's more likely a temporal wandering because clock is frequency locked
- For forward data, 1 USB data comes at about every 11 slots. So, 1-2 slot delay doesn't matter as long as we have time till the USB data generation time
- For backward data, 1 USB data comes at every slot. We prefer to have some margin time between the USB slot and the generation time. If the margin time is more than the variation, we are ok, i.e., not add additional latency
- Additional Rx latency

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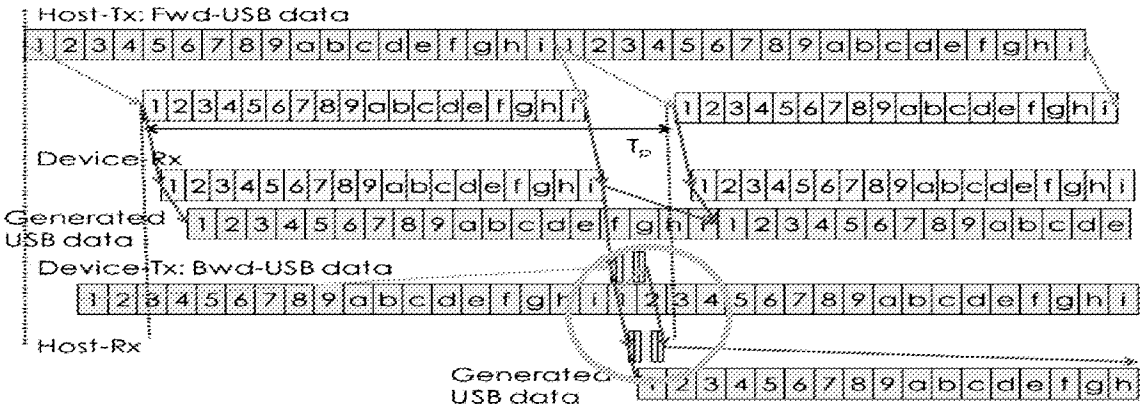
Buffering of USB data in Rx side (Cont'd)

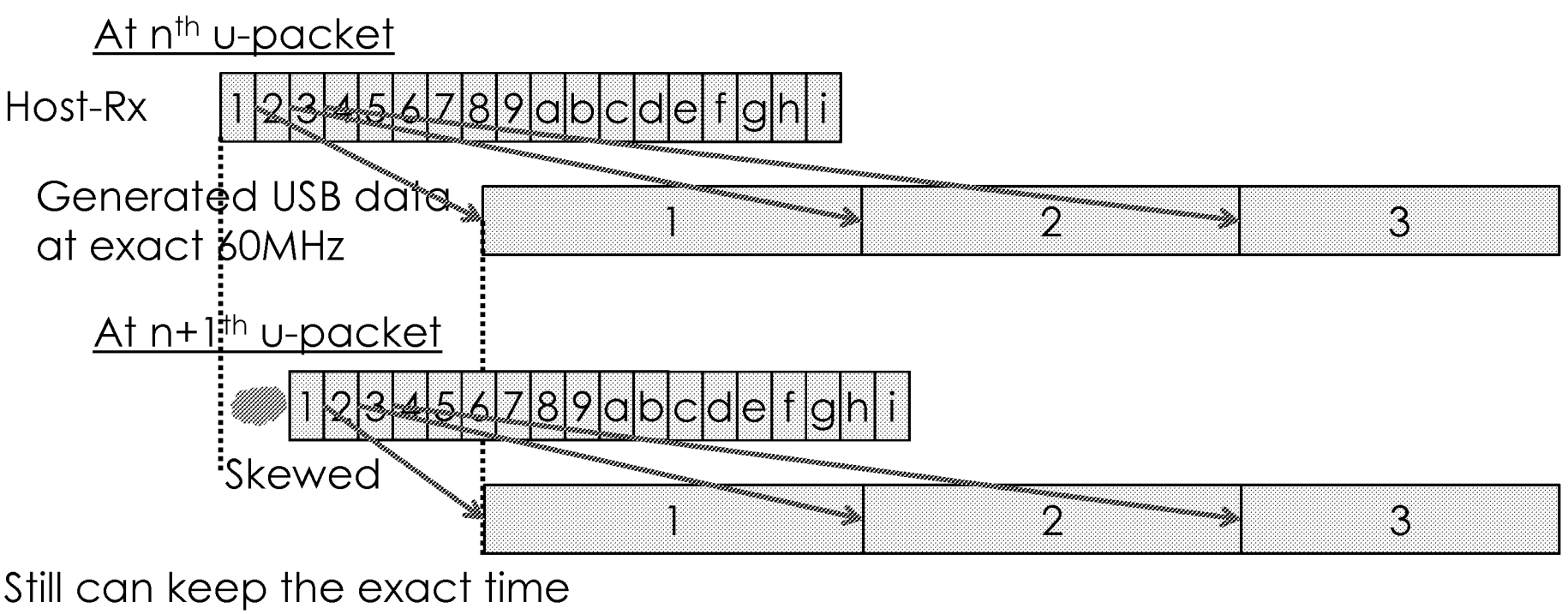




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Buffering of USB data in Rx side (Cont'd)





Still can keep the exact time

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SYNC time

- This time is used to detect the symbol boundary after the corresponding direction turns on
- TMDS uses 3 SYNCs detected in Rx. So, the min # of slots for SYNC symbol is 3+2
- 8b10b code uses 1 SYNC detected in Rx. The min # of slots may be 1+2
- We can use preamble instead of SYNC. This is possible since we have "state" information saying that this is the time to detect symbol boundary
  - Simple preamble such as "01010101..0100" may be enough
  - This reduces the # of slots needed for SYNC time
  - Can change DPLL side to align to preamble in a specific state only. After that state, preamble is ignored
  - About 2 slots will be enough – 0101010101_0101010100
- Can use a preamble (if we want to keep TMDS) or 8b10b

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Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	TDD over 5-Pin Interface
First Named Inventor/Applicant Name:	Hoon Choi
Filer:	Michael Wayne Farn
Attorney Docket Number:	30850-26578

Filed as Large Entity

Provisional Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Provisional Application Filing	1005	1	260	260
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**260**

Electronic Acknowledgement Receipt

EFS ID:	18761066
Application Number:	61979483
International Application Number:	
Confirmation Number:	3383
Title of Invention:	TDD over 5-Pin Interface
First Named Inventor/Applicant Name:	Hoon Choi
Customer Number:	120363
Filer:	Michael Wayne Farn
Filer Authorized By:	
Attorney Docket Number:	30850-26578
Receipt Date:	14-APR-2014
Filing Date:	
Time Stamp:	21:49:37
Application Type:	Provisional

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$260
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Application Data Sheet	26578_US_ADS.PDF	1561136 2828475bc0b77bfaa61914ab39267fa159187494	no	9
Warnings:					
Information:					
2	Specification	spec.pdf	84208 e20d353fb14481410abc89e2870206cbb32d3ef3	no	2
Warnings:					
Information:					
3	Drawings-other than black and white line drawings	CPEC58.pdf	1234772 51f7971c705bb9b336611c9d1f636a75a231f633	no	31
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	29050 5f320dc589c5d9529f41eb89308951bd009f214a	no	2
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		Total Files Size (in bytes):	2909166		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.