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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Attorney Docket No.	371798018US
First Inventor	Yeshik Shin
Title	METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS
Express Mail Label No.	EL669108811US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☐ Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. ☐ Applicant claims small entity status. See 37 CFR 1.27
3. ☒ Specification [*Total Pages* 68]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. ☒ Drawing(s) *(35 U.S.C.113)* [*Total Sheets* 58]
5. Oath or Declaration [*Total Pages*]
   a. ☐ Newly executed (original or copy)
   b. ☐ Copy from a prior application (37 CFR 1.63 (d)) *(for a continuation/divisional with Box 18 completed)*
      i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☐ Application Data Sheet See 37 CFR 1.76

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7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
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      i. ☐ CD-ROM or CD-R (2 copies); or
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9. ☒ Assignment Papers (cover sheet & document(s))
10. ☒ 37 C.F.R.§3.73(b) Statement ☒ Power of Attorney *(when there is an assignee)*
11. ☐ English Translation Document *(if applicable)*
12. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
13. ☐ Preliminary Amendment
14. ☒ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
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☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: ____ / ____

Prior application information: *Examiner* ____ *Group / Art Unit:* ____

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☒ Claims the benefit of Provisional Application No. 60/252,724 filed November 22, 2000

17. CORRESPONDENCE ADDRESS

☒ *Customer Number or Bar Code Label* 25096 PATENT TRADEMARK OFFICE *or* ☐ *Correspondence address below*

Name (Print/Type)	Maurice J. Pirio	*Registration No. (Attorney/Agent)*	33,273
Signature	Maurice J. Pirio	*Date*	November 7, 2001

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J1057 U.S. PTO 11/07/01

JC968 U.S. PTO 10/045625 11/07/01

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NONPUBLICATION REQUEST UNDER ~~35 U.S.C. 122(b)(2)(B)(i)~~	First Named Inventor	Yeshik Shin
	Title	METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS
	Atty Docket Number	371798018US

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing.

I hereby request that the attached application not be published under 35 U.S.C. 122(b).

November 7, 2001
Date

Maurice J. Pirio
Signature

Maurice J. Pirio
Typed or printed name

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing.**

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First Inventor	Yeshik Shin
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☒ Claims the benefit of Provisional Application No. 60/252,724 filed November 22, 2000

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Name (Print/Type)	Maurice J. Pirio	*Registration No. (Attorney/Agent)*	33,273
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	Atty Docket Number	371798018US

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I hereby request that the attached application not be published under 35 U.S.C. 122(b).

November 7, 2001
Date

Maurice J. Pirio
Signature

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Typed or printed name

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing.**

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METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/252,724 entitled "METHOD AND APPARATUS FOR STORAGE I/O WITH FULL-DUPLEX ONE-TIME BLOCK I/O TRANSFER AND ADAPTIVE PAYLOAD SIZING," filed November 22, 2000, and is related to U.S. Patent Application No. _____ entitled "METHOD AND SYSTEM FOR PLESIOSYNCHRONOUS COMMUNICATIONS WITH NULL INSERTION AND REMOVAL" (Attorney Docket No. 371798002US); U.S. Patent Application No. __, entitled "METHOD AND SYSTEM FOR TRANSITION-CONTROLLED SELECTIVE BLOCK INVERSION COMMUNICATIONS" (Attorney Docket No. 371798007US); U.S. Patent Application No. _____ entitled "COMMUNICATIONS ARCHITECTURE FOR STORAGE-BASED DEVICES" (Attorney Docket No. 371798008US1); U.S. Patent Application No. _____ entitled "METHOD AND SYSTEM FOR PACKET ORDERING BASED ON PACKET TYPE" (Attorney Docket No. 371798013US); U.S. Patent Application No. _____ entitled "METHOD AND SYSTEM FOR HOST HANDLING OF COMMUNICATIONS ERRORS" (Attorney Docket No. 371798014US); U.S. Patent Application No. _____ entitled "METHOD AND SYSTEM FOR DYNAMIC SEGMENTATION OF COMMUNICATIONS PACKETS" (Attorney Docket No. 371798015US); U.S. Patent Application No. _____ entitled "METHOD AND SYSTEM FOR ASYMMETRIC PACKET ORDERING BETWEEN COMMUNICATIONS DEVICES" (Attorney Docket No. 371798016US); U.S. Patent Application No. _____ entitled "METHOD AND SYSTEM FOR COMMUNICATING CONTROL INFORMATION VIA OUT-OF-BAND SYMBOLS" (Attorney Docket No. 371798017US); U.S. Patent Application No. _____ entitled "METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE

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INFORMATION WITH SYNCHRONIZATION SYMBOLS" (Attorney Docket No. 371798018US); U.S. Patent Application No. _____ entitled "METHOD AND SYSTEM FOR NESTING OF COMMUNICATIONS PACKETS" (Attorney Docket No. 371798019US); U.S. Patent Application No. _____ entitled "COMMUNICATIONS ARCHITECTURE FOR MEMORY-BASED DEVICES" (Attorney Docket No. 371798012US); U.S. Patent Application No. _____ entitled "METHOD AND SYSTEM FOR DC-BALANCING AT THE PHYSICAL LAYER" (Attorney Docket No. 371798020US); and U.S. Patent Application No. _____ entitled "MULTISECTION MEMORY BANK SYSTEM" (Attorney Docket No. 371798021US, which are all hereby incorporated by reference in their entirety.

BACKGROUND

[0002] The described technology relates generally to communications techniques and particularly to communications between hosts and data store devices.

[0003] The speed and capacity of the data store devices, such as disk drives and memories, have increased significantly over the past several years. As a result of their improved performance, these data store devices are being used in many new applications, such as database servers, Web servers, personal video recorders, and digital displays. These applications often require large amounts of data to be communicated between data store accessing devices ("hosts") and data store devices. (Hosts may include computers, CPUs, or any logic for accessing a data store device.) Moreover, as host speed increases, the speed in communicating between hosts and data store devices can have a significant impact on the overall performance of the application. In particular, even though the speed of hosts and data store devices has increased significantly, the speed of communications between hosts and data store devices has not increased as significantly, especially for communications over long distances (e.g., greater than one meter). Thus, the communications speed presents a bottleneck in many new applications.

[0004] Current communications techniques typically communicate between hosts and certain types of data store devices, such as disk drives, using a bus with

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many parallel lines or using a single serial communications link. The Integrated Disk Electronics ("IDE") bus and the Small Computer Systems Interface ("SCSI") bus are examples of bus-based parallel communications techniques. These communications techniques, however, present many problems. Performance of bus-based communications techniques is generally improved by increasing the number of lines in the bus, which may significantly increase the cost of such techniques. In addition, bus-based communications techniques generally provide arbitration so that multiple hosts and data store devices can share the same bus. The use of arbitration can significantly increase the cost of such a bus. The cost of such bus-based communication techniques is further increased because their design needs to address additional problems such as cross-talk and clock skew. In particular, as the communications speed increases, the solution to cross-talk and clock skew become much more complex.

[0005] Some serial communications techniques have been developed to address some of the problems of bus-based communications techniques. Current serial communications techniques, however, have problems of their own. Serial AT, Attachment, which is intended to replace IDE, does not scale well and only operates in a half duplex mode. Fibre Channel, currently used to support storage area networks ("SANs"), is very generic and therefore, not optimized for any particular application. In particular, Fibre Channel has a relatively small packet size with a large header. As a result, use of Fibre Channel often results in an unacceptably large overhead. For example, data transmitted to disk drives is typically sent in very large blocks (e.g., 216 bytes). With Fibre Channel, such large blocks need to be divided in many (e.g., 32) packets, which results in a high overhead in the amount of redundant header information and in the redundant processing performed as a packet is routed to its destination. Thus, Fibre Channel may not be appropriate for many applications.

[0006] Current memory devices, such as SDRAM and RDRAM, are typically designed to be synchronous with the accessing processing unit. The hosts and the memory devices are synchronous in that they share the same clock signal.

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These memory devices are typically optimized for access patterns that are both temporally and spatially related. In particular, these memory devices are optimized to read and write arrays (or streams) of data. There is a setup overhead (e.g., 5 clock cycles) when accessing the first word of an array in memory, but access of subsequent words in the array occurs at the synchronized clock rate (e.g., 1 access per clock cycle). Since the access patterns of central processing units and graphics processors are typically temporally and spatially related, they can access such memory devices efficiently.

[0007] Existing memory devices that are designed to support access patterns with a high temporal and spatial relationship may not be appropriate for uses having access patterns with a lower spatial relationship. The setup overhead for each access may be too high. There are, indeed, many uses for memory devices with access patterns that are not as spatially or temporally related as those of a central processing unit or a graphics processor. For example, a switch may have a memory device in which packets of data received via an input port are stored before they are transmitted via an output port. Traditionally, switches used crossbars to provide the switching function and FIFOs to provide a buffering function. When a memory device is used on a switch in place of a crossbar, then all the input and output ports need access to the memory device. The accesses by the different ports are, however, not particularly spatially related. Moreover, when the packet size is small (e.g., 53 bytes in the case of an ATM switch), the spatial relationship of accesses by a single port may not be significant. Other uses in which there may not be a significant spatial relationship of accesses include network processors and caches for storage area networks. In such uses, the data is received from disparate sources at disparate times and may not be spatially related.

[0008] Many existing memory devices are not particularly suitable for many uses because the memory devices typically allow access by only one accessing device at a time and because the memory devices typically operate at different clock rates than the accessing devices. Because such memory devices can only be

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accessed by one device at a time, the accessing devices may need to enter a wait state because the memory device is busy or a memory controller may need to have a buffering component. Of course, the use of a wait state may result in unacceptable performance. Also, the addition of a buffering component may increase complexity and cost. In addition, when multiple accessing devices access the same memory device through a single bus (e.g., one writing to the memory device and the other reading from the memory device), then all the devices that access the memory device need to be synchronized with the memory device. Because the accessing devices may have different underlying clock rates, complex and costly logic is needed to support the mapping to the bus clock rate.

[0009] Existing communications protocols, such as Fibre Channel, may have an unacceptable overhead for communicating with memory devices. The communications from a host to a memory device may occur in relatively short blocks (e.g., 32 bytes). Each block needs to be transmitted in a separate packet with a relatively large header. In some packets, the header may be larger than the data itself, which can significantly reduce the overall bandwidth and speed of transmission. More generally, communications between devices typically occurs in a synchronous or an asynchronous mode. In a synchronous mode, the transmitting and receiving devices use the same clock signal. The transmitting device can send the clock signal to the receiving device either as a separate signal or as a signal that can be derived from the data signals. When the clock is sent as a separate signal, problems arise resulting from the different delays in the data signals and the clock signal. These delays and resulting problems are increased as the transmission speed and distance are increased. It is very difficult and costly to account for these delays. In addition, the receiving device will have an asynchronous clock boundary. That is, a portion of the receiving device will operate at the clock frequency based on the transmitting device's clock frequency (i.e., the transmitter's clock domain) and another portion will operate at the receiving device's local clock frequency (i.e., the receiver's clock domain). As a result of the asynchronous boundary, the receiving device typically needs to

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buffer control and data signals sent between the clock domains using elastic buffers, which adds to the complexity and cost of the receiving devices. These elastic buffers require substantial space (e.g., chip area), and when a single chip has multiple communications ports, the design is complicated because each port needs its own elastic buffer. When the clock is derived from the data signal, the problems of the delay are reduced somewhat, but there are still the problems associated with an asynchronous clock boundary.

[0010] A plesiosynchronous clocking technique can be used to avoid the need to transmit a separate clock signal or derive the clock signal from the data signal. With plesiosynchronous clocking (also known as "plesiochronous" clocking), the transmitting and receiving devices have clocks with nominally the same clock frequency. If the clock frequencies were exactly the same, then transmitting and receiving devices would be synchronized and the receiving device could accurately identify the transmitted data (in the case of serial transmission). Also, since the receiving device operates only at its local clock frequency, there is no asynchronous clock boundary. In practice, however, clock frequencies are not exactly the same but vary, for example, by 100 ppm. The receiving device can use techniques as described in U.S. Patent No. 6,229,859, entitled "System and Method for High-Speed, Synchronized Data Communication," which is hereby incorporated by reference, to account for clock variations. Those techniques use an oversampling of the data by the receiving device to detect edge boundaries of the transmitted data. The receiving device can vary the number of bits of data detected during an interval to compensate for the variations in frequency.

[0011] It would be desirable to have a communications architecture that provides high-performance for applications (e.g., data storage-based applications and memory-based applications) at a low cost. Such a communications architecture would allow for communications techniques to be tailored to particular applications.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Figure 1 is a block diagram illustrating components of the Storage Link architecture in one embodiment.

[0013] Figure 2 is a block diagram illustrating components of the transport layer, link layer, and physical layer in one embodiment.

[0014] Figure 3 is a block diagram illustrating components of the physical layer in one embodiment.

[0015] Figure 4 is a block diagram illustrating the format of a packet in one embodiment.

[0016] Figure 5 is a block diagram illustrating the organization of a data packet and a segmented data packet in one embodiment.

[0017] Figure 6 is a block diagram illustrating a receive packet memory before and after merging of a received packet.

[0018] Figure 7 is a logic diagram illustrating the segmentation of a data packet by the transport layer in one embodiment.

[0019] Figure 8 is a logic diagram illustrating the merging of data packets by the transport layer in one embodiment.

[0020] Figure 9A is a diagram illustrating the use of a synchronization primitive encoded with the packet type in one embodiment.

[0021] Figure 9B illustrates the identification of synchronization symbols in one embodiment.

[0022] Figure 9C is a block diagram illustrating a component of a link layer for inserting a synchronization symbol into a stream of symbols.

[0023] Figure 10 is a block diagram illustrating an organization of a packet memory in one embodiment.

[0024] Figure 11 is a logic diagram illustrating the process of storing packets in a transmit packet memory in one embodiment.

[0025] Figure 12 is a logic diagram illustrating the transport layer processing of packets stored in the packet memory in one embodiment.

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[0026] Figure 13 is a diagram illustrating the preemption of a packet in one embodiment.

[0027] Figure 14 is a logic diagram illustrating the processing of packet preemption by a transmitting communications node in one embodiment.

[0028] Figure 15 is a logic diagram illustrating the processing of packet preemption by a receiving communications node in one embodiment.

[0029] Figure 16 is a block diagram illustrating asymmetric packet ordering in one embodiment.

[0030] Figure 17 is a diagram illustrating transaction-based asymmetric packet ordering in one embodiment.

[0031] Figure 18 is a logic diagram illustrating processing by a switch that ensures packet ordering within a transaction in one embodiment.

[0032] Figure 19A is a block diagram illustrating error handling during transmission from a host to a data store device in one embodiment.

[0033] Figure 19B is a block diagram illustrating the handling of errors during the transmission from a data store device to a host in one embodiment.

[0034] Figure 19C is a logic diagram illustrating the processing of a communications node detecting an error in one embodiment.

[0035] Figure 20 illustrates an alternate bit inversion encoding technique in one embodiment.

[0036] Figure 21A is a diagram illustrating the selective block inversion encoding technique in one embodiment.

[0037] Figure 21B is a block diagram illustrating selective block inversion with a programmable block size in one embodiment.

[0038] Figure 21C is a block diagram illustrating transition inversion and polarity inversion in one embodiment.

[0039] Figure 22 is a diagram illustrating the format of a primitive in one embodiment.

[0040] Figure 23 is a logic diagram illustrating transition control and selective block inversion encoding in one embodiment.

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[0041] Figure 24 is a logic diagram illustrating transition control optimization in one embodiment.

[0042] Figure 25 is a logic diagram illustrating block inversion in one embodiment.

[0043] Figure 26 is a logic diagram illustrating transition control and selective block inversion decoding in one embodiment.

[0044] Figure 27 is a logic diagram illustrating the undoing of block inversion in one embodiment.

[0045] Figure 28 is a logic diagram illustrating the undoing of transition control optimization in one embodiment.

[0046] Figure 29 is a logic diagram illustrating the processing of a primitive in one embodiment.

[0047] Figure 30 is a block diagram illustrating the overall architecture of a multiport memory device in one embodiment.

[0048] Figure 31 is a block diagram illustrating the use of a single phase lock loop for the physical layer of a multiport memory device in one embodiment.

[0049] Figure 32 is a block diagram illustrating contents of a bank cache in one embodiment.

[0050] Figure 33 is a logic diagram illustrating processing of the access layer when it receives data from a host in one embodiment.

[0051] Figure 34 is a logic diagram illustrating the processing of a write command by the access layer in one embodiment.

[0052] Figure 35 is a logic diagram illustrating processing of the access layer when it is to provide data to the transport layer in one embodiment.

[0053] Figure 36 is a block diagram of a multisection memory bank in one embodiment.

[0054] Figure 37A is a block diagram illustrating a variable strength line driver in one embodiment.

[0055] Figure 37B is a block diagram illustrating the circuit of a variable-strength line driver in one embodiment.

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[0056] Figure 38A is a block diagram of a plesiosynchronous communications system in one embodiment.

[0057] Figure 38B is a block diagram illustrating a switch supporting multiple data store devices in one embodiment.

[0058] Figure 39A is a block diagram illustrating a prior art synchronous clocking system.

[0059] Figure 39B is a block diagram illustrating resolution of an asynchronous clock boundary in the physical layer in one embodiment.

[0060] Figure 40 is a block diagram illustrating NULL insertion and deletion at the physical layer in one embodiment.

[0061] Figure 41 is a block diagram illustrating the frame aligner in one embodiment.

[0062] Figures 42A, 42B, and 42C illustrate the loading of the bit buffer in one embodiment.

[0063] Figure 43 is a diagram illustrating the detection of a synchronization primitive by the sync and null detector in one embodiment.

[0064] Figure 44 is a diagram illustrating the portion of the bit buffer that contains the next symbol to be extracted in one embodiment.

[0065] Figure 45 is a state diagram of the symbol pointer tracker in one embodiment.

[0066] Figure 46 is a diagram illustrating movement of the start-of-symbol pointer due to overrun or underrun in one embodiment.

[0067] Figures 47A and 47B are diagrams illustrating NULL detection while the start-of-symbol pointer is not within the overrun or underrun extend regions in one embodiment.

[0068] Figures 48A and 48B are diagrams illustrating NULL detection while the start-of-symbol pointer is in the underrun extend region.

[0069] Figures 49A and 49B are diagrams illustrating NULL detection while the start-of-symbol pointer is in the overrun extend region.

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DETAILED DESCRIPTION

[0070] A serial communications architecture for communicating between hosts and data store devices is provided. Aspects of the serial communications architecture, referred to as "Storage Link," are specially adapted for communications with storage devices, such as disk drives. Other aspects of the serial communications architecture, referred to as "Memory Link," are specially adapted for communications with memory devices, such as RAM devices. In addition, Storage Link and Memory Link may use an improved plesiosynchronous technique when receiving data transmitted via a serial communications link.

[0071] In one embodiment, the Storage Link architecture is specially adapted to support communications between multiple hosts and storage devices via a switching network, such as a storage area network. The Storage Link architecture specifies various communications techniques that can be combined to reduce the overall cost and increase the overall performance of communications. The Storage Link architecture defines a hierarchy of transport, link, and physical layers such that each layer in the hierarchy is aware of and can take advantage of characteristics of lower layers in the hierarchy. For example, the transport layer, which is responsible for handling packets, may receive signals from the link layer that indicate when an end of packet is received. Traditional communications architectures prohibit a lower layer from being aware of the functions of a higher layer. The Storage Link architecture may provide packet ordering based on packet type, dynamic segmentation of packets, asymmetric packet ordering, packet nesting, variable-sized packet headers, and use of out-of-band symbols to transmit control information as described below in more detail. The Storage Link architecture may also specify encoding techniques to optimize transitions and to ensure DC-balance. The Storage Link architecture may also use the NULL insertion and removal techniques with plesiosynchronous clocking as described below in detail. The Storage Link architecture thus provides an improved way to access storage devices that reduces cost and increases communications speed.

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[0072] In one embodiment, the Memory Link architecture also provides various communications techniques that can be combined to reduce the overall cost and increase the overall performance of communications between a host and a memory device. Like the Storage Link architecture, the Memory Link architecture uses a hierarchy of layers in which each layer can take advantage of the characteristics of a lower layer in the hierarchy. The Memory Link architecture in one embodiment provides a multiport memory device for serial communications. Each port may use a plesiosynchronous technique when receiving data and may share the same phase lock loop to control sampling of the received data. The Memory Link architecture may also use a physical layer D-C balancing technique that provides an additional driving of a communications link to offset the running disparity. The Memory Link architecture may also use an improved plesiosynchronous clock technique that inserts and removes special symbols from the received symbols to compensate for variations in clock frequencies between a transmitting and receiving device. Various combinations of the Memory Link architecture allow for the cost of designing, developing, and manufacturing memory-based systems to be reduced and the speed of memory access to be increased.

[0073] In one embodiment, the plesiosynchronous clocking technique uses the insertion and removal of symbols by the physical layer of a receiving communications node to compensate for variations in clock frequency between the transmitter and receiver. The receiver maintains a small buffer (e.g., 27 bits of the received data) at the physical layer. When the receiver detects a synchronization symbol, it initializes a start-of-symbol pointer in the buffer. As subsequent bits of data are received, the start-of-symbol pointer is adjusted to account for the variation in clock frequencies of the transmitter and the receiver. In particular, if the transmitter's clock frequency is faster ("an overrun condition"), then the pointer is progressively moved backward in the buffer (i.e., toward the last received bits). Analogously, if the transmitter's clock frequency is slower ("an underrun condition"), then the pointer is progressively moved forwards in the

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buffer (i.e., toward the first received bits). When the receiver detects a special symbol of a certain type (e.g., a NULL symbol) and the pointer has moved to near the beginning or end of the buffer, then the receiver removes the special symbol from the buffer to account for the overrun condition or inserts a special symbol into the buffer to account for the underrun condition. In this way, the receiver stays synchronized with the transmitter even though their clock frequencies vary. Also, asynchronous clock boundaries are avoided in the receivers.

[0074] In the following, aspects of the serial communications architecture are described using block diagrams and logic diagrams. One skilled in the art will appreciate that the serial communications architecture can be implemented using different combinations of logic circuits and/or firmware. In particular, the logic diagrams illustrate processing that may be performed in parallel using duplicate logic circuits (e.g., one for each communications link) or may be performed in serial using a single logic circuit. The particular logic designs can be tailored to meet the cost and performance objectives of the implementation of the serial communications architecture. One skilled in the art will be able to readily design logic circuits based on the following descriptions.

1. STORAGE LINK ARCHITECTURE

[0075] Figure 1 is a block diagram illustrating components of the Storage Link architecture in one embodiment. The hosts 110 and data store devices 120 are interconnected to switching network 130 via serial communications links 140. The hosts may include computer systems that access the data store devices. The data store devices may include storage area network devices (e.g., disk drives), high-speed memory devices, and other devices for storing data. The Storage Link architecture, however, is designed to support block-oriented data store devices, such as disk drives. The switching network may include multiple switches that are interconnected so that communications paths, especially between hosts and data store devices, can be established.

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[0076] Each host, data store device, and switch is a communications node that includes one or more communications interfaces 115, 125, and 135 with a transport layer, a link layer, and a physical layer. The hosts and data store devices have an upper layer that communicate to each other via transactions. When transmitting data, the upper layer provides the data for the transaction to the transport layer. The transport layer receives the data of the transaction and generates packets (i.e., packetizes the data) for transmission. The transport layer then provides each code (e.g., each byte) of the packets to the link layer for transmission to the destination. When receiving data, the transport layer receives the codes of transaction from the link layer and identifies the packets. The transport layer then combines the data of the packets of the transaction (i.e., depacketizes the data) and provides the data of the transaction to the upper layer. Each host and data store device may include an application upper layer that provides the data of a transaction to the transport layer to be transmitted to a destination and receives the data of a transaction from the transport layer that was transmitted by a source. Each packet includes a header section and a payload section. The header section identifies the source and destination and a packet type (e.g., data or command). Each switch may include a communications interface for each port of the switch. Each port may be connected to a serial communications link comprising a receive and transmit link. The switches and their interconnecting communications links form the switching network. The transport layer of a switch may not packetize and depacketize the data, rather it may direct packets received via one port to be transmitted via another port to affect the routing of the packets from the source to the destination as indicated in the header section.

[0077] The link layer encodes the codes to be transmitted via its communications link into symbols and decodes symbols received via its communications link into codes. The link layer receives codes to be transmitted from the transport layer, encodes those codes into symbols, and provides those symbols to the physical layer. The link layer also receives symbols from the physical layer, decodes those

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symbols into codes, and provides those codes to the transport layer. The encoding may include mapping the codes to symbols to optimize bit transitions and to ensure DC-balance. The physical layer receives the symbols from the link layer, serializes the symbols, and transmits the serialized symbols via the communications link. The physical layer receives serialized symbols via the communications link, deserializes the symbols, and provides the symbols to the link layer.

[0078] Figure 2 is a block diagram illustrating components of the transport layer, link layer, and physical layer in one embodiment. Each layer includes transmit components 201 and receive components 202. The transport layer includes transmit components, such as a transmit memory 211, a packetizer 212, and a transmit controller 213, and receive components, such as a receive memory 215, a depacketizer 216, and a receive controller 217. The data of the transaction to be transmitted is stored in the transmit memory. The transmit controller controls the packetizer to retrieve data of a transaction from the transmit memory, packetize the data, and provide each code of the packets to the link layer. The receive controller controls the depacketizer to receive codes provided by the link layer, identify the packets, and store the codes as packets in the receive memory.

[0079] The link layer includes transmit components, such as an encoder 221, a data selector 222, and a control symbol generator 223, and receive components, such as a decoder 225 and a control symbol identifier 226. The link layer may be responsible for generating and transmitting and for receiving and identifying, control symbols, synchronization symbols, timing symbols, and so on, as described below in more detail. In one embodiment, however, the physical layer is responsible for detecting control symbols and synchronization symbols. The transport layer may indicate to the link layer when to transmit control symbols, and the link layer may indicate to the transport layer when control symbols are received. For example, the transmit layer may notify the link layer when the receive memory is full. In such a case, the link layer may transmit a control symbol (e.g., XOFF) notifying the other end of the communications link not to

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transmit any more data. When such transmitted control symbol is received, the link layer of the other end may indicate to its transport layer to stop transmitting data. The data selector selects symbols encoded from codes provided by the transport layer or symbols generated by the control symbol generator. The data selector effectively inserts control symbols and synchronization symbols into the sequence of symbols that are to be transmitted. Various possible encoding techniques for the codes are described below in detail. The data decoder receives symbols from the physical layer and decodes them into codes that are provided to the transport layer. The control symbol identifier identifies control symbols and signals the transport layer as appropriate.

[0080] The physical layer includes a transmitter 231 and receiver 235. The transmitter serializes the symbols provided by the link layer and transmits the serialized symbols onto the communications link. The receiver receives the serialized symbols via the communications link, deserializes the symbols, and provides the symbols to the link layer.

[0081] The transmit components and the receive components can transmit and receive packets in full duplex mode. That is, a packet received by the transport layer can be transmitted by the transmit components simultaneously with a packet being received by the receive components. As discussed below in detail, the encoding techniques enable transmitting of control symbols by the link layer for link control (e.g., flow control) even while packets are being transmitted in full duplex mode. That is, link control symbols can be inserted into a sequence of symbols generated from codes provided by the transport layer. Thus, a communications link can be simultaneously transmitting and receiving data symbols, and control symbols can be inserted for link control. Prior transmission techniques typically transmitted in half-duplex mode because the receiving link was reserved for transmission of control information. Thus, the Storage Link architecture has a significant bandwidth advantage because of its full-duplex mode.

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[0082] Figure 3 is a block diagram illustrating components of the physical layer in one embodiment. The physical layer uses a plesiosynchronous timing mechanism to control the transmission and reception of the symbols. A plesiosynchronous-based physical layer is described in U.S. Patent Number 6,229,859, entitled "System and Method for High-Speed Synchronized Data Communication," which is hereby incorporated by reference.

[0083] Improvements to the plesiosynchronous timing mechanism are described below in detail. For example, one improvement is the insertion and removal of NULL symbols, which renders the use of elastic buffers unnecessary. Another improvement is the sharing of a single phase lock loop by multiple ports, which avoids the complexity and cost of having one phase lock loop for each port. The physical layer 230 includes a transmitter 231, a receiver 235, a phase lock loop 301, and a clock 302. The phase lock loop provides a timing signal to the transmitter for serial transmission of the symbols and provides multiple timing signals with different phases to the receiver for receiving the serially transmitted symbols. One skilled in the art will appreciate that a delay lock loop, or more generally any multiphase clock generating device, can be used in place of the phase lock loop. The receiver may include an oversampler 303, a digital phase lock loop 304, and a frame aligner 305. The digital phase lock loop selects the best sample by a process known as majority voting. Majority voting counts transitions from one oversampled bit to another. In one embodiment, each bit is oversampled three times and the position with the highest number of transitions is selected. The digital phase lock loop thus identifies the bit values of the received symbols, and the frame aligner aligns the bits into symbols and provides the deserialized symbols.

[0084] Figure 4 is a block diagram illustrating the format of a packet in one embodiment. The packet 400 includes a header section 410 and a payload section 420. The header section includes reserved fields 411 and 412 (e.g., 16 bits each), a destination address field 413 (e.g., 16 bits), a source address field 414 (e.g., 16 bits), a type field 415 (e.g., 8 bits), a protocol field 416 (e.g., 8 bits), a

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class specific control field ("CSF") 417 (e.g., 8 bits), and a transaction (or queue) index field 418 (e.g., 8 bits). One skilled in the art will appreciate that the actual size of the fields can vary depending on the desired performance characteristics. For example, the destination and source address fields can be limited to 4 bits when there are at most 16 hosts or data store devices. The class-specific control field contains the control field of the interface class (e.g., SCSI, ATA), which may be unused in some interface classes. The protocol field identifies the appropriate protocol for the upper layer and identifies the protocol of the storage media (e.g., SCSI, ATA, or Storage Link). The destination address field identifies the host or data store device to which the packet is to be transmitted. The source address field identifies the host or data store device that originated the transmission of the packet. In one embodiment, the reserved fields may be used in conjunction with the source address field and the destination address field to permit 32-bit addresses. The type field identifies the type of the packet. The types of packets may include a data packet, a command packet, a status packet, and a message packet. The command packet, status packet, and message packet are "control" packets. Control packets are generally much smaller than data packets. The type field further specifies the direction of the packet transmission (i.e., whether it is being transmitted from a host to a data store device, or vice versa) and specifies whether the packet is intended for the physical layer, link layer, transport layer, or application layer. For example, an application layer packet may be a command packet sent from a host device to a data store device requesting that data be retrieved from the data store device. The payload section contains type-specific information. For example, the payload section of a command packet for retrieving data from a data store device may include the starting address of the data to be retrieved and the number of bytes of data to be retrieved. The payload section of a data packet transmitted in response to receiving a command packet may contain the retrieved data in the payload section. The control field contains type-specific information that may be used to control the data store device. The transaction index field identifies a series of packets that correspond to the same

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transaction. For example, a transaction may be the writing of data to a data store device. A host may transmit the data to be written in multiple packets that form a single transaction. Each packet within the transaction contains the same transaction index so that the data store device can identify that the packets belong to the same transaction. Although not shown, a packet may also include a cyclic redundancy check (CRC) field after the payload section.

[0085] In various embodiments, the size of the header portion can vary based on the number of hosts and data store devices that are addressable. For example, if a single host is directly connected to a single data store device, then a small header including the type field, control field, protocol field, a class specification control field and transaction index field would be sufficient. The destination and source address fields and reserved fields would not be needed. When there are either multiple hosts or multiple data store devices, then the destination and source address fields would be included in the header. If more hosts and data store devices are addressable than can be addressed by 16 bits, then the reserved fields can be included in the header. Thus, the size of the header can vary depending on the number of possible sources and destinations. In one embodiment, the transport layer may be configurable to include a small, medium, or large header depending on the number of possible sources and destinations.

[0086] A packet that is transmitted on a serial communications link typically comprises in-band symbols with certain desirable characteristics, such as with its number of bit transitions optimized, as described below in more detail. The physical layer continually transmits symbols onto the serial communications link. If a packet is not available to be transmitted, then the link layer provides IDLE symbols to the physical layer for transmission. In one embodiment, an IDLE symbol is an out-of-band symbol, which is a symbol that does not normally appear within a packet because it may not have the same desirable characteristic as an in-band symbol (e.g., bit transitions not optimized). A receiving link layer identifies the start of a packet by a transition from receiving IDLE symbols to receiving in-band symbols. Similarly, a receiving link layer identifies the end of a packet by a

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transition from receiving in-band symbols to receiving IDLE symbols. In one embodiment, a IDLE symbol is actually a sequence of two out-of-band symbols for reasons described below in detail. More generally, a sequence of two out-of-band symbols is a primitive that is used to exchange control information (e.g., XON and XOFF) between link layers as described below in detail. Because control information is encoded as out-of-band symbols, the control symbols can be inserted into a sequence of in-band symbols and readily detected as control symbols when received. The control symbols can be interspersed with the transmission of symbols of a packet so that one end of a communications link can provide link control information to the other end even while packets are being transmitted in both directions (i.e., full-duplex mode)

1.1 Packet Segmentation

[0087] In one embodiment, a packet (e.g., long packets, such as data packets) may be dynamically divided or segmented into multiple packets by a communications node (e.g., a host, data store device, or switch) as the packet is being transmitted from a source to a destination. The dynamic segmentation of packets allows for the efficient transmission of large packets via a single path when the switching network is not congested and allows for the efficient transmission of segmented packets on different paths when congestion prevents use of a single path. In addition, dynamic segmentation may avoid the resending of portions of the payload when segmenting a packet.

[0088] A packet may be segmented by a communications node when, for example, the next communications node in the path indicates that it cannot receive any more symbols of a packet. The transmitting communications node may receive an XOFF signal from the receiving communications node (e.g., because of a buffer overflow at the receiving communications node) in the middle of transmitting a packet. The transmitting communications node stops transmitting the packet until an XON signal is received from the receiving communications node or unless it can start transmitting the remainder of the packet on a different communications link (i.e., through a different port). In either

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case, the transmitting communications node transmits a new header with the remainder of the packet, which results in the segmentation of the packet into a first packet with a first header and a second packet with a second header. The packet segmentation is performed by the transport layer based on signals provided by the link layer (e.g., in response to receiving an XOFF signal).

[0089] Figure 5 is a block diagram illustrating the organization of a data packet and a segmented data packet in one embodiment. The payload section of a data packet may include a target address and blocks of data to be stored at the target address. For example, if the data store device is a disk drive, then the target address may be a sector address of the disk drive and the blocks of data may each correspond to a sector of data. In one embodiment, the blocks have a fixed size (e.g., the sector size). Packet 510 includes a header section 500 and a payload section 511 that includes an address 500a and blocks 501-506. When a communications node is transmitting packet 510, it may transmit the header section and address 500a and blocks 501-503 of the payload section. During transmission of block 504, the transmitting communications node may receive an XOFF signal from the receiving communications node. (The receiving communications node may transmit an XOFF control primitive.) The transmitting communications node completes the transmission of block 504 and then stops transmitting the packet on that serial communications link. (The link layer then starts transmitting an IDLE symbol on the communications link.) When the transmitting communications node eventually receives an XON signal from the receiving communications node, it transmits a new header section 531 plus a payload section indicating a new address 531a and blocks 505 and 506 to complete the transmitting of the packet. The new address may be represented by an offset that is added to a start address to generate the new address. The new header may contain the same header information as the previously transmitted header, but the address (e.g., as an offset) of the payload section is updated to reflect the starting address at which the remaining blocks of the packet are to be stored. For example, if packet 510 is segmented after block 504 and the starting

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address for that packet is address 211, then the starting address for the packet containing blocks 505 and 506 is 215 (i.e., 211+4). Packet 510 is thus segmented into packets 520 and 530. When a packet is segmented, the transport layer may route the remaining packet on a different communications link to the destination. The use of different communications links helps to optimize the use of available bandwidth.

[0090] In addition to segmenting packets, the transport layer may merge packets that were previously segmented. For example, if packet 520 is currently stored in a receive memory of a switch awaiting transmission and packet 530 is received at the switch, then the transport layer may recognize that the packets are part of the same transaction (e.g., based on source addresses, destination address, and transaction index) and that their blocks are contiguous as indicated by their target addresses. The transport layer can merge packets 520 and 530 to form packet 510. One skilled in the art will appreciate that packets 520 and 530 can be merged regardless of the order in which they were received at the switch. Also, one skilled in the art will appreciate that if a switch is in the process of transmitting packet 520 and packet 530 is received, the packets can be merged by transmitting blocks 505 and 506 immediately after block 504. One skilled in the art will also appreciate that a transport layer can merge packets stored in a transmit memory. In this way, packets received via different ports of a switch can be merged. The merging of packets allows data of the same transaction to be more efficiently transmitted when traffic on the switch network allows.

[0091] Figure 6 is a block diagram illustrating a receive packet memory before and after merging of a received packet. Packet 600 forming transaction T1 initially contains 8 blocks. During transmission, it is segmented into packets 614, 630, and 612. Packets 614 and 612 are currently buffered at a switch which then receives packet 630. Because the switch has all three packets, they can be merged into a single packet. Before the merge, packet memory 610 contains 4 packets. Packet 611 is part of transaction T3 and contains 5 blocks of data to be stored starting at address 25. Packet 612 is part of transaction T1 and contains 3

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blocks of data to be stored starting at address 4. Packet 613 is part of transaction T2 and contains 10 blocks of data to be stored starting at address 50. Packet 614 is part of transaction T1 and contains 2 blocks of data to be stored starting at address 0. Packets 612 and 614 are both part of transaction T1. These packets, however, are not contiguous packets within transaction T1 and thus cannot be merged together. Packet 630 represents a packet just received that is part of transaction T1 and contains 2 blocks to be stored starting at address 2. Packet 630 is contiguous to both packets 614 and 612. That is, packet 630 can be merged onto the end of packet 614 and packet 612 can be merged onto the end of packet 630. Packet memory 620 contains the packets after the merge. Packets 611 and 613 have been left unchanged. Packet 614, however, has been modified to add the blocks from packet 630 and from packet 612. Packet 614 indicates that is the part of transaction T1 and contains 7 blocks of data to be stored starting at address 0. Packet 612 has been deleted from the packet memory because it has been merged with packet 614, and packet 630 has not been separately added to the packet memory because it has been merged with packet 614.

[0092] Figure 7 is a logic diagram illustrating the segmentation of a data packet by the transport layer in one embodiment. In block 701, a component of the transport layer waits for a block of data. In decision block 702, if an XOFF signal has been received, then the component waits for an XON signal in block 703, else the component continues at block 704. In block 704, the component sends the header to the link layer for transmission. In blocks 705-707, the component transmits successive blocks of the packet and segments the packet when an XOFF signal is received from the link layer. In block 705, the component transmits the next block of the packet. In decision block 706, if an XOFF signal is pending as indicated by the link layer, then the component continues to segment the packet at block 708, else the component continues at block 707. In decision block 707, if the next block is ready, then the component loops to block 705 to transmit the next block, else the component segments (or ends) the packet at

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block 708. In block 708, the component transmits the CRC to end the packet and waits for the next block in 701.

[0093] Figure 8 is a logic diagram illustrating the merging of data packets by the transport layer in one embodiment. In block 801, a component of the transport layer receives a data packet from the link layer. In blocks 802-807, the component checks to see if the data packet can be merged with a previously received data packet that is stored in the receive memory. In block 802, the component selects the next data packet in the receive memory. In decision block 803, if all the data packets of the receive memory have already been selected, then the component continues at block 808, else the component continues at block 804. In decision block 804, if the selected and received data packets are contiguous, then the component continues at block 805, else the component selects the next data packet in the receive memory. In block 806, the component adds the blocks of the selected packet to the receive packet to affect the merging of the blocks. In block 807, the component removes the selected packet from the receive memory. The component then selects the next data packet because there may be another data packet that can be merged at the beginning or end of the received data packet. In block 808, the component adds the received data packet to the receive memory and then completes.

1.2 Synchronization Primitive and Packet Type

[0094] In one embodiment, the serial communications architecture defines multiple primitives to operate as synchronization signals. A synchronization signal is typically used by the physical layer to help ensure correct alignment of symbols. A transmitting communications node periodically transmits synchronization primitives so that the receiving communications node can properly align with that synchronization primitive. When a communications node receives a synchronization primitive, it knows that the primitive is correctly aligned on a symbol boundary. The use of multiple synchronization primitives allows for encoding packet type within a synchronization primitive. In particular, the transport layer provides the packet type to the link layer. The link layer can then

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transmit a synchronization primitive that indicates packet type immediately before the packet itself. The receiving communications node can take the appropriate action based on the packet type encoded in the synchronization primitive without having to parse the packet header. Indeed, the packet header may not need to separately include the packet type. The use of a synchronization primitive with encoded packet type may be well adapted to use in an environment where the transmission time of a packet through the switching network may be long relative to the time needed to store the packet at the data store device. For example, the time to transmit a packet through the switching network may be longer than the time needed to store the data of the packet in a memory-based data store device. The rapid detection of packet type through a synchronization primitive, rather than through a packet header, can reduce the processing time of a switch. Also, when a synchronization primitive encodes the packet type, then the link layer, rather than the transport layer, can detect packet type, which can enhance the overall processing speed.

[0095] Figure 9A is a diagram illustrating the use of a synchronization primitive encoded with the packet type in one embodiment. Serial link content diagram 900 indicates the information transmitted on a serial link over a period of time. Initially, an IDLE primitive is transmitted onto the communications link. (An IDLE primitive may be a synchronization primitive that does not encode any packet type.) Immediately prior to transmitting control packet 902 (e.g., command, status, or message packets), the transport layer of the transmitting communications node signals the link layer that a control packet is to be transmitted next. The link layer then transmits a synchronization primitive 901 encoded with a packet type of control. After the packet has been transmitted, the link layer of the transmitting communications node starts transmitting the idle primitive. Immediately before the transport layer transmits data packet 904, it notifies the link layer that a data packet is to be transmitted. The link layer transmits a synchronization primitive 903 encoded with a packet type of data. After the data packet is transmitted, the link layer starts transmitting the IDLE primitive. The receiving communications

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node uses the synchronization primitive encoded with packet type to align its symbol boundaries and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers.

[0096] As described above, the primitives are pairs of out-of-band symbols. (In the following, a symbol is assumed to have nine bits.) In one embodiment, when the in-band symbols are transition maximized, then the symbols of the control primitives have three transitions each and the symbols of the synchronization primitives have two transitions each. When the in-band symbols are transition minimized, then the symbols of the control primitives have five transitions each and the synchronization primitives have one symbol with five transitions and another symbol with seven transitions.

[0097] Table 1 illustrates control primitives in one embodiment when the in-band symbols are transition maximized. Each control primitive comprises two symbols in which the first symbol is a polarity inversion of the second symbol. As a result, the disparity (described below) of each control primitive is 0. The control primitives such as XON, XOFF, preempt, and continue are selected from this table of control primitives.

Table 1: Control primitives in transition maximization mode

0.	000010111 – 111101000
1.	000011011 – 111100100
2.	000011101 – 111100010
3.	000100111 – 111011000
4.	000110011 – 111001100
5.	000111001 – 111000110
6.	001000111 – 110111000
7.	001100011 – 110011100
8.	001110001 – 110001110
9.	010000111 – 101111000
10.	011000011 – 100111100
11.	011100001 – 100011110
12.	100001110 – 011110001
13.	100011100 – 011100011
14.	100111000 – 011000111
15.	101110000 – 010001111
16.	110000110 – 001111001
17.	110001100 – 001110011
18.	110011000 – 001100111

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19.	110110000 – 001001111
20.	111000010 – 000111101
21.	111000100 – 000111011
22.	111001000 – 000110111
23.	111010000 – 000101111

[0098] Table 2 illustrates control primitives in one embodiment when the in-band symbols are transition minimized.

Table 2 - Control primitives in transition minimization mode

0.	000010101 – 111101010
1.	000100101 – 111011010
2.	000101001 – 111010110
3.	000101011 – 111010100
4.	000101101 – 111010010
5.	000110101 – 111001010
6.	001000101 – 110111010
7.	001001001 – 110110110
8.	001001011 – 110110100
9.	001001101 – 110110010
10.	001010001 – 110101110
11.	001010011 – 110101100
12.	001011001 – 110100110
13.	001100101 – 110011010
14.	001101001 – 110010110
15.	010000101 – 101111010
16.	010001001 – 101110110
17.	010001011 – 101110100
18	010001101 – 101110010
19.	010010001 – 101101110
20.	010010011 – 101101100
21.	010011001 – 101100110
22.	010100001 – 101011110
23.	010100011 – 101011100
24.	010110001 – 101001110
25.	011000101 – 100111010
26.	011001001 – 100110110
27.	011010001 – 100101110
28.	100001010 – 011110101
29.	100010010 – 011101101
30.	100010100 – 011101011
31.	100010110 – 011101001
32.	100011010 – 011100101
33.	100100010 – 011011101
34.	100100100 – 011011011
35.	100100110 – 011011001
36.	100101000 – 011010111

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37.	100101100 – 011010011
38.	100110010 – 011001101
39.	100110100 – 011001011
40.	101000010 – 010111101
41.	101000100 – 010111011
42.	101000110 – 010111001
43.	101001000 – 010110111
44.	101001100 – 010110011
45.	101010000 – 010101111
46.	101011000 – 010100111
47.	101100010 – 010011101
48.	101100100 – 010011011
49.	101101000 – 010010111
50.	110001010 – 001110101
51.	110010010 – 001101101
52.	110010100 – 001101011
53.	110100010 – 001011101
54.	110100100 – 001011011
55.	110101000 – 001010111

[0099] The synchronization primitives are distinct from the control primitives. The synchronization primitives are selected to have the characteristic that when two synchronization primitives are transmitted sequentially the receiving device can unambiguously identify the synchronization primitives regardless of what is transmitted before or after the synchronization primitives. The synchronization primitives have a unique number of transitions that is not found in any control primitive or in-band symbol. In one embodiment, the synchronization primitive can be detected by looking for a sequence of symbols with that number of transitions. In one embodiment, the synchronization primitives are selected to start with a falling edge (i.e., "10"), a rising edge (i.e., "01"), a high level (i.e., "11"), or a low level (i.e., "00"). The selection of the start of the synchronization primitives is referred to as the "synchronization detection mode." Table 3 contains synchronization primitives in transition maximization mode that start with a falling edge and a rising edge. Each symbol in Table 3 contains two transitions resulting in synchronization primitives with four transitions. Table 4 contains synchronization primitives in transition minimization mode that start with a low level and a high level. Each synchronization primitive in Table 4 has

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13 transitions. The high-level and low-level synchronization primitives have five transitions in one symbol, seven transitions in the other symbol, and one transition from their first to second symbol.

Table 3

	Falling Edge	Rising Edge
0	100000001 – 100111111	011000000 – 011111110
1	100000011 – 100011111	011100000 – 011111100
2	100000111 – 100001111	011110000 – 011111000
3	100001111 – 100000111	011111000 – 011110000
4	100011111 – 100000011	011111100 – 011100000
5	100111111 – 100000001	011111110 – 011000000

Table 4

	High Level	Low Level
0	110101000 – 110101010	001010101 – 001010111
1	110100010 – 110101010	001010101 – 001011101
2	110001010 – 110101010	001010101 – 001110101
3	110100100 – 110101010	001010101 – 001011011
4	110010100 – 110101010	001010101 – 001101011
5	110101010 – 110101000	001010111 – 001010101
6	110101010 – 110100010	001011101 – 001010101
7	110101010 – 110001010	001110101 – 001010101
8	110101010 – 110100100	001011011 – 001010101
9	110101010 – 110010100	001101011 – 001010101

[00100] Table 5 lists the transition distribution of the low and high polarity symbols of the synchronization primitives.

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Table 5

Sync Detect Mode	Transition Distribution in Low Polarity	Transition Distribution in High Polarity	Total # of Transitions in a Sync Primitive
Falling edge ("10")	one "10" and one "01"	one "10" and one "01"	4
Rising edge ("01")	one "01" and one "10"	one "01" and one "10"	4
High level ("11")	one "11" and two "00"	one "11" and no "00"	13
Low level ("00")	one "00" and no "11"	one "00" and two "11"	13

[00101] In one embodiment, the synchronization primitives are detected by buffering three symbols (e.g., 27 bits). The synchronization primitives are selected so that any time the buffer has exactly three of the synchronization detection mode bits (e.g., "10" for falling edge) that are each 9 bits apart then the bits are at the beginning of a synchronization symbol. The bit buffer contains 27 bits, A[8:0], B[8:0], and C[8:0], in which bit A[8] was received first and bit C[0] was received last. In this example, the content of bits A[6]:B[7] represent synchronization symbol "100000001" and B[6]:C[7] represent synchronization symbol "100111111." The starting points of the synchronization symbols ("synchronization markers") are A[6], B[6], and C[6].

[00102] Figure 9C is a block diagram illustrating a component of a link layer for inserting a synchronization symbol into a stream of symbols. The link layer 910 is provided with the bits of the code ("Data") to be transmitted and with an indication of a control primitive ("CTL-S") to transmit. The idle inserter 910 of the link layer automatically inserts an IDLE primitive (e.g., synchronization primitive) to ensure that not too may data symbols have been sent without sending a synchronization primitive. In one embodiment, the transmitter may send an IDLE primitive after every block of a packet. If packets are short, the inter-packet gap ("IPG") is sufficient for clock compensation. That is, the receiver will receive synchronization primitives often enough to maintain proper synchronization. If a packet is long, however, the link layer can periodically insert a synchronization primitive to ensure

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that the receiver maintains proper synchronization. The multiplexer of the link layer selects the appropriate symbol to send to the physical layer.

1.3 Transmission Order Based on Packet Type

[00103] In one embodiment, a communications node transmits packets of certain types before packets of other types regardless of the order in which the packets are received or generated by the communications node. For example, a switch may transmit control packets (e.g., command packets, status packets, and message packets) before transmitting data packets. The transmitting of control packets before data packets may help ensure that the control packets are not unnecessarily delayed by data packets, which may have a tendency to be quite large. For example, a command packet requesting a read from a data store device may be transmitted before a data packet even through the control packet was received after the data packet. The data store device can thus start processing the read request without having to wait until the data packet is transmitted. A communications node may store control packets and data packets in separate areas of the packet memory and only select packets from the data packet area when the control packet area is empty. Alternatively, the communications node may use various algorithms to select control or data packets to be transmitted. For example, the algorithm may select a data packet that has been in the packet memory for certain amount of time even though there may be a control packet in the control area. In this way, a sequence of many control packets will not delay the data packet more than that certain amount of time. One skilled in the art will appreciate that there may be multiple packet types with different transmission orders. For example, a status packet might be transmitted before a command packet, and a command packet might be transmitted before a data packet.

[00104] Figure 10 is a block diagram illustrating an organization of a packet memory in one embodiment. The transmit packet memory 211 may include control queue 1010 and data queue 1020. The control queue contains the control packets 1011, and the data queue contains the data packets 1021. Packets to be

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transmitted are stored either in the control queue or the data queue based on packet type (which may be encoded in a synchronization primitive). When a transmitting communications node is ready to transmit the next packet, it retrieves the next packet from the control queue. If the control queue is empty, then the transmitting communications node retrieves the next packet from the data queue.

[00105] Figure 11 is a logic diagram illustrating a process of storing packets in a transmit memory in one embodiment. Similar logic can be used to store packets in the receive memory of a communications node. In block 1101, a component of the transport layer receives the next packet from an upper layer. In decision block 1102, if the received packet is a control packet, then the component continues at block 1103, else the component continues at block 1104. The component may determine the type of the packet either from the type field of the packet header or, when the packet is received from another communications node, from a synchronization primitive encoded with the packet type. When the link layer detects a synchronization primitive designating packet type, it signals the transport layer so that the type of packet can be used when the packet is stored in the receive memory, retrieved from the receive memory, stored in the transmit memory, and retrieved from the transmit memory. In block 1103, the component stores the packet in the control queue. In block 1104, the component stores the packet in the data queue. The component then retrieves the next packet.

[00106] Figure 12 is a logic diagram illustrating the transport layer processing of packets stored in the packet memory in one embodiment. In decision block 1201, if the control queue is empty, then the component continues to block 1203, else the component retrieves a control packet from the control queue in block 1202 and continues at block 1205. In decision block 1203, if the data queue is empty, then the component again checks for a packet in the control queue, else the component retrieves a packet from the data queue in block 1204 and continues at block 1205. In blocks 1205-1207, the component selects the codes of the retrieved packet. In block 1205, the component selects the next code of the retrieved packet. In decision block 1206, if all codes have already been selected,

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then the component continues at block 1201 to check for the next packet, else the component continues at block 1207. In block 1207, the component provides the selected code to the link layer and then continues at block 1205 to select the next code of the packet.

1.4 Packet Preemption

[00107] In one embodiment, a communications node may preempt or interrupt the transmission of a packet when a packet with a higher priority is to be transmitted on the same communications link. Packet preemption helps ensure that data store devices receive control packets as soon as possible without being slowed by network congestion as a result of data packets. In particular, the transmission of a data packet, which may be large, may be preempted so that a control packet, which is typically small, may be transmitted. When a data packet is to be preempted, the transport layer of the communications node stops providing the codes of the data packet to the link layer, signals the link layer to transmit a preempt primitive, and then starts providing the code of the control packet to the link layer for transmission as a preempting packet. When the preempting packet has been completely transmitted, the transport layer of the communications node signals the link layer to transmit a continue primitive and then resumes providing the remainder of the codes of the data packet to the link layer. The link layer of the receiving communications node detects the preempt primitive while it is receiving the codes of the data packet and signals its transport layer. The transport layer then starts storing the subsequent codes as a control packet. When the link layer detects the continue primitive, it signals the transport layer, which continues receiving the preempted data packet. The preempt and continue primitives, which are control primitives, serve to delimit transmission of a preempting packet. One skilled in the art will appreciate that packet preemption could be nested to any level. For example, a status packet might preempt a command packet that already preempted a data packet.

[00108] Figure 13 is a diagram illustrating the preemption of a packet in one embodiment. Serial link content diagram 1300 illustrates a data packet that is

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preempted by a control packet. Initially, the transmitting communications node transmits the first portion of data packet 1301. When the packet is to be preempted, the communications node then transmits the preempt primitive 1302. After transmitting the preempt primitive, the transmitting communications node transmits the preempting control packet 1303. After the control packet is transmitted, the communications node transmits the continue primitive 1304, and then resumes transmitting the remainder of the preempted data packet 1305.

[00109] Figure 14 is a logic diagram illustrating the processing of packet preemption by a transmitting communications node in one embodiment. In block 1401, the component of the transport layer retrieves the next packet from the transmit memory. In block 1402, the component retrieves the next code of the retrieved packet. In decision block 1403, if all the codes have already been retrieved from the packet, then the component continues at block 1401 to retrieve the next packet, else the component continues at block 1404. In block 1404, the component provides the retrieved code to the link layer. In decision block 1405, if a preempt signal has been raised (e.g., as a result of being provided a control packet by an upper layer), then the component continues at block 1406, else the component continues at block 1402 to retrieve the next code of the packet. In block 1406, the component notifies the link layer to transmit a preempt primitive. In blocks 1407-1409, the component provides each code of the preempting packet to the link layer. In block 1407, the component selects the next code of the preempting packet. In decision block 1408, if all the codes of the preempting packet have already been selected, then the component continues at block 1410, else the component continues at block 1409. In block 1409, the component provides the selected code to the link layer and then continues at block 1407 to select the next code of the preempting packet. In block 1410, the component signals the link layer to transmit a continue primitive and then continues processing the preempted packet at block 1402.

[00110] Figure 15 is a logic diagram illustrating processing of packet preemption by a receiving communications node in one embodiment. In block 1501, the

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component of the transport layer retrieves the next code from the link layer. In decision block 1502, if the link layer signals that a preempt primitive has been received, then the component continues at block 1504, else the component continues at block 1503. In block 1503, the component adds the code to the current packet and retrieves the next code in block 1501. In block 1504, the component saves current packet information so that it can continue storing codes in the packet after the preemption is complete. In block 1505, the component processes the preempting packet. The processing includes receiving each code and storing the codes in a preempting packet until the link layer indicates that it received a continue primitive. In block 1505, the component restores the saved packet information so that subsequent received codes can be stored in the preempted packet. The component then selects the next code of the preempted packet in block 1501.

1.5 Asymmetric Packet Ordering

[00111] In one embodiment, the serial communications architecture may guarantee that packets (in particular packets of the same transaction) transmitted from a host to a data store device are received at the data store device in the order in which they were transmitted from the host. In contrast, the serial communications architecture might not guarantee that packets transmitted from a data store device to a host are received at the host in the same order that they were transmitted from the data store device. The guarantee of order in one direction, but not in the other direction, is referred to as asymmetric packet ordering. Because the packets are received at the data store device in order, the data store device does not need the hardware or software necessary to reorder packets that are received out-of-order. As a result, the overall cost of the data store device can be reduced. The guarantee of order may be provided by requiring that all packets of the same transaction transmitted from a host to a data store device travel on the same path. In contrast, packets of the same transaction transmitted from a data store device to a host may each travel on different paths. Because the packets transmitted from a host to a data store device travel along the same path, the actual time to

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transmit the packets may take longer than if alternate paths could be used. For example, one communications link in the path may become congested with no alternative but to wait for the congestion to end, whereas if an alternate path was used, the remaining packets could be routed to avoid the congestion; thus, the packets would arrive sooner, but possibly out-of-order. In one embodiment, the serial communications architecture may only guarantee the order of packets transmitted from a host to a data store device within each transaction. Packets within a transaction have a sequential order. The guarantee of order within a transaction may be provided by requiring that all the packets of each transaction to be transmitted from a host to a data store device along the same path. The packets of different transactions can, however, be transmitted along different paths. In this way, a packet within a later transmitted transaction may arrive at the data store device before a packet of an earlier transmitted transaction.

[00112] A host may be a computer system running application programs, and the data store device may be a disk drive. In such an environment, the speed at which data is transmitted to a disk drive may not be as important as the speed at which the data is transmitted to the computer system. In particular, when an application program writes data to a disk drive, the data is normally cached by the computer system before transmission to the disk drive so that the application program can continue its processing without having to suspend its execution. In contrast, when an application program reads data from a disk drive, the application normally suspends its execution until the data is received. Thus, the speed of transmitting data from the disk drive is more important than the speed of transmitting data to a disk drive because it can reduce the time a program is suspended. The asymmetric packet ordering takes advantage of this variation in the need for speed.

[00113] Figure 16 is a block diagram illustrating asymmetric packet ordering in one embodiment. Packets of the same transaction, transmitted from a host 1610 to a data store device 1620 all travel along the same path: switch 1631, switch 1634, and switch 1636. Since the data packets are processed in a first-in-first-out

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manner by each switch, packet ordering is preserved in transit. In contrast, packets of the same transaction transmitted from a data store device 1620 to a host 1610 may travel along two different paths: (1) a path including switch 1636, switch 1633, and switch 1631 and (2) path including switch 1636, switch 1635, switch 1632, and switch 1631. Packets traveling on different paths may arrive out-of-order at the host.

[00114] Figure 17 is a diagram illustrating transaction-based asymmetric packet ordering in one embodiment. Illustration 1701 illustrates preserving packet ordering within a transaction transmitted from a host to a data store device. In this example, transaction 1 includes packets 1 and 2 and transaction 2 includes packets 1, 2, 3, and 4. Transaction 1 is transmitted from the host before transaction 2. The data store device received the packets of each transaction in order within their transaction, but some of the packets of transaction 2 arrived before the some of the packets of transaction 1. For example, packet 1 of transaction 2 arrived before packet 1 of transaction 1, but after packet 1 of transaction 2. Illustration 1702 illustrates transmitting without preserving packet ordering within a transaction. In this example, transactions 1 and 2 are transmitted from the data store device to the host. The host receives the packets of the transactions out of order. For example, packet 2 of transaction 2 arrived before packet 1 of transaction 2.

[00115] Figure 18 is a logic diagram illustrating processing by a switch that ensures packet ordering within a transaction in one embodiment. In block 1801, a component of the switching layer retrieves the next data packet to be routed. In decision block 1802, if another packet of the same transaction has been transmitted by the switch, then the component identifies the same communications link in block 1803, else the component identifies a communications link for the first packet of that transaction.

1.6 Host Error Handling

[00116] In one embodiment, the communications nodes detect errors but do not attempt to correct or handle the errors. Rather, communications nodes forward

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error messages to the communications node that initiated the transaction associated with the error. For example, a host may request a data store device, such as a disk drive, to provide data stored at the data store device. If an error occurs (e.g., a CRC error) while the data is being transmitted from the data store device to the host, the communications node (e.g., a switch) that detects the error transmits an error message to the initiating host. The initiating host can then handle to the error as appropriate. For example, the initiating host may retransmit the request to retrieve the data from the data store device. Because the communications node (e.g., data store device or switch) does not attempt to handle errors, the complexity of these communications nodes is reduced. Although the handling of the error by the initiating host may be slow, the slowness may be acceptable because errors are expected to be relatively uncommon.

[00117] Figure 19A is a block diagram illustrating the handling of errors during transmission from a host to a data store device in one embodiment. The host 1901 transmits a packet 1904 to switch 1902. The switch detects an error, transmits an error message packet 1905 to the host reporting the error, and suppresses further transmission of the packet to the data store device 1903. When the host receives the error message packet, it forwards an error message 1906 to the upper layer for processing. Similarly, when the data store device detects an error in the transmission of packet 1907 from the switch, it transmits an error message packet 1908 reporting the error to the switch, which is then transmitted as an error message packet 1909 to the host, and the error message 1910 is eventually reported to the upper layer of the host.

[00118] Figure 19B is a block diagram illustrating the handling of errors during the transmission from a data store device to a host in one embodiment. The switch 1902 detects an error in the transmission of packet 1911 from the data store device 1903. Rather than transmitting an error message packet 1912 to the data store device, the switch transmits an error message packet 1913 to the host 1901 that initiated the transaction of the packet 1911 for which the error was detected. Upon receiving the error message packet, the host forwards an error message

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1914 to an upper layer for handling. Similarly, when the host detects an error in transmission of packet 1915, it does not transmit error message packet 1916 to the switch 1902, rather it forwards an error message 1917 to the upper layer. As can be seen from Figures 19A and 19B, the switches and data store devices merely generate and forward error message packet, and do not perform error handling to correct the error.

[00119] Figure 19C is a logic diagram illustrating the processing of a communications node detecting an error in one embodiment. In block 1921, a component of a transport layer receives an error signal from the link layer such as from a line indicating a CRC error. In block 1922, the component retrieves packet identifier information associated with the error. The packet identifier information includes the address of the initiating host. In block 1923, the component generates an error packet to transmit to the initiating host. In block 1924, the component transmits the error packet to the initiating host.

1.7 Transition Control & Selective Block Inversion

[00120] In one embodiment, the link layer of a communications node encodes codes into symbols in order to optimize transition control and to ensure DC-balance. Transition control may be optimized to either maximize or minimize the number of transitions in symbols that are to be transmitted. A transition is defined as a bit value of 1 followed by a bit value of 0 or a bit value of 0 followed by a bit value of 1. When the number of transitions is maximized, clock information may be more accurately derived from the transmitted symbols. When the number of transitions is minimized, overall electromagnetic interference may be minimized. One skilled in the art will appreciate that the link layer may be designed to minimize or maximize transitions depending on the overall design objectives. In the following, the described encoding technique attempts to maximize the number of transitions in symbols to be transmitted. In an alternate embodiment, the transitions can be maximized at times and minimized at other times to balance the objectives of deriving a clock signal and reducing electromagnetic interference.

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[00121] The encoding technique in one embodiment encodes an 8-bit code based on the number of transitions in that code. The maximum possible number of transitions in an 8-bit code is seven and occurs when the bit values alternate between 0 and 1 (e.g., "10101010"). The minimum possible number of transitions in an 8-bit code is zero and occurs when all the bit values are the same (e.g., "11111111"). To maximize the number of transitions, the encoding technique inverts the bit value of alternate bits in each code with less than four transitions. This alternate bit inversion, also referred to as transition inversion, results in a code that previously had "n" transitions to now have |n-7| transitions. For example, the result of alternate bit inversion of a code with zero transitions (e.g., "11111111") is a code with seven transitions (e.g., "01010101"), and the result of alternate bit inversion of the code with three transitions (e.g., "00010111") is a code with four transitions (e.g., "10111101"). The encoding technique adds a ninth bit (i.e., a transition inversion indicating bit) to the 8-bit code to indicate whether the alternate bits of the code were inverted, which results in a 9-bit symbol. For example, a bit value of 0 in the ninth bit indicates that the code did not have its alternate bits inverted, and a bit value of 1 in the ninth bit indicates that the code did have its alternate bits inverted. The symbol "010111101" has a bit value of 0 in its ninth bit, which indicates that alternate bits were not inverted. In contrast, the symbol "110111101" has a bit value of 1 in its ninth bit, which indicates that alternate bits were inverted. One skilled in the art will appreciate that the ninth bit can be stored at any bit position within the symbol. In this description, the ninth bit is represented as the most significant bit of the symbols.

[00122] When a symbol is received at a communications node, the ninth bit is used to determine whether the symbol needs to have its alternate bits inverted to decode the symbol. Since the symbol "010111101" has a bit value of 0 in its ninth bit, its alternate bits were not inverted and the resulting decoded code is "10111101." Conversely, since the symbol "110111101" has a bit value of 1 in its ninth bit, its alternate bits were inverted and the resulting decoded code is "00010111." All the symbols generated by alternate bit inversion encoding are

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referred to as "in-band symbols" because they are 9-bit symbols with at least four transitions. All 9-bit symbols with three or less transitions are referred to as "out-of-band symbols." This alternate bit inversion encoding technique generates only in-band symbols.

[00123] Figure 20 illustrates an alternate bit inversion encoding technique in one embodiment. The left column represents the 8-bit codes, and the right column represents the 9-bit symbols. The alternate bit inversion encoding technique is referred to as an 8b/9b encoding, which is a more efficient encoding than standard 8b/10b encodings. Transition control encoding is described in U.S. Patent No. 5,999,571, entitled "Transition-Controlled Digital Encoding and Signal Transmission System," which is hereby incorporated by reference.

[00124] The encoding technique may also help ensure DC-balance by using selective block inversion encoding on symbols that have been transition optimized. Selective block inversion refers to an encoding technique that inverts certain bit values in a block of symbols to help ensure DC-balance is maintained. In one embodiment, selective block inversion may perform polarity inversion (i.e., inverting each bit of a symbol) on all but one symbol of a block to help ensure DC-balance and transition inversion on that one symbol in the block to indicate that the other symbols of the block have been polarity inverted. Although the encoding technique performs selective block inversion on blocks of four symbols, one skilled in the art will appreciate that a block can contain any number of symbols. Conventional encoding techniques, in contrast, typically process only one symbol at a time when attempting to ensure DC-balance. Because the selective block inversion encoding technique evaluates DC-balance over multiple symbols, DC-balance is more likely assured and there is essentially no bandwidth used to indicate whether a symbol has been inverted.

[00125] The selective block inversion encoding technique tracks the running disparity on symbol boundaries of the symbols that have been transmitted so far. The running disparity represents the difference in the overall number of 1-bit values and 0-bit values of the symbols that have been transmitted on the

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communications link. For example, if 452 1-bit values and 448 0-bit values have been transmitted (e.g., 100 symbols), then the running disparity is +4 (e.g., in the 1-direction or positive). If 448 1-bit values and 452 0-bit values have been transmitted, then the running disparity is -4 (e.g., in the 0-direction or negative). If the number of 1-bit values and 0-bit values are equal, then the running disparity is 0 (e.g., neutral). To determine whether to perform selective block inversion on a block of symbols, the encoding technique compares the running disparity of the symbols transmitted so far to the block disparity of that block. Block disparity is the difference between number of 1-bit values and 0-bit values of the symbols of a block. If the running disparity and the block disparity are both positive or both negative, then the encoding technique performs block inversion on that block.

[00126] The encoding technique inverts a block by inverting alternate bits of the first symbol in the block (i.e., transition inversion) and inverting all the bits of the other symbols in the block (i.e., polarity inversion). The inverting of the alternate bits of the first symbol results in an out-of-band symbol that is used to indicate whether the following block has been block inverted. When a block of symbols is received, the receiving communications node can determine whether the block has been block inverted by checking the first symbol of the block. If the first symbol of the block is an in-band symbol, then the block has not been block inverted. If the first symbol of the block is an out-of-band symbol, then the block has been block inverted. If the block has been block inverted, then the decoding technique undoes the alternate bit inversion of the first symbol by inverting alternate bits of the first symbol and undoes the bit inversion of the other symbols by inverting all of the bits of the other symbols. One skilled in the art will appreciate that the symbol used to indicate whether the block is block inverted need not be the first symbol of the block, but rather can be any symbol of the block so long as the receiving communications node can identify which symbol indicates selective block inversion.

[00127] Figure 21A is a diagram illustrating the selective block inversion encoding technique in one embodiment. In this example, a block is defined as having four

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symbols. One skilled in the art will appreciate that a block can have any number of two or more symbols. In this example, the block disparity is +6, because there are 21 1-bit values and 15 0-bit values in the block. If the running disparity is positive, then the encoding technique performs block inversion. The first symbol of the block has its alternate bits inverted, and the remaining symbols of the block have all their bits inverted. The resulting symbols have a block disparity of -4. Thus, the DC-balance would be improved by transmitting the inverted block, rather than the noninverted block. The encoding technique may alternatively only perform block inversion when the running disparity is outside a certain range. For example, if the running disparity is between –100 and +100, then no selective block inversion is performed. If outside the range, then selective block inversion is performed. One skilled in the art will appreciate that this range can be selected based on various characteristics of the communications link such as transmission rate or maximum transmission distance.

[00128] Figure 21B is a block diagram illustrating selective block inversion with a programmable block size in one embodiment. In this example, the block size is represented by the variable "k." The selective block inversion encoding technique processes k sequential symbols at a time as indicated by blocks 2101 and 2102. The transition from block 2101 to 2102 illustrates selective block inversion for transmission, and the transition from block 2102 to 2101 illustrates the undoing of selective block inversion upon reception. To perform block inversion, the block header symbol Ci is transition inverted (TI) resulting in symbol Bi and the symbol Ci+1 to symbol Ci+k-1 are polarity inverted (SI) resulting in symbol $\overline{C_{i+1}}$ to symbol $\overline{C_{i+k-1}}$. To undo block inversion, the block header symbol Bi is transition inverted resulting in symbol Ci and the symbols $\overline{C_{i+1}}$ to symbol $\overline{C_{i+k-1}}$ are polarity inverted resulting in symbol Ci+1 and symbol Ci+k+1.

[00129] Figure 21C is a block diagram illustrating transition inversion and polarity inversion in one embodiment. In this example, 8-bit codes are inverted. The code 2110 may be transition inverted in two ways to generate codes 2111 and 2112. Code 2111 results from inverting alternate bits starting with the first bit, and code

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2112 results from inverting alternate bits starting with the second bit. The code 2110 is polarity inverted by inverting each bit to generate code 2113. The same process is applied to codes 2111, 2112, and 2113 to generate code 2110.

[00130] As discussed above, a primitive is a sequence of two out-of-band symbols. Thus, a receiving communications node can distinguish between a primitive and the first symbol of an inverted block because a primitive is a sequence of two out-of-band symbols and one out-of-band symbol by itself represents the first symbol of an inverted block.

[00131] Figure 22 is a diagram illustrating the format of a primitive in one embodiment. A primitive is defined as a sequence of two out-of-band symbols. The out-of-band symbols are preferably selected to have minimal impact on DC-balance. In particular, the disparity of a primitive is selected to be as close to 0 as possible. To achieve this disparity, one symbol of the primitive may have a negative disparity and the other symbol of the primitive may have any positive disparity. (A symbol with an odd number of bits cannot have a 0 disparity.) When the disparity of a primitive is 0, then the primitive can be transmitted at any time without affecting the running disparity and thus with minimal impact on the DC-balance. In one embodiment, the first symbol of a primitive has the negative disparity (i.e., negative polarity) and the second symbol has the positive disparity (i.e., positive polarity), or vice versa. The receiving communications node can detect a transmission error when a sequence of two out-of-band symbols has an improper ordering for their disparity or both symbols have either a positive or a negative disparity. When a primitive has minimal or no effect on DC-balance, then the complexity of the transmitting communications node may be reduced because the logic to calculate the running disparity need not include primitives in the calculation.

[00132] Figures 23-28 are logic diagrams illustrating encoding and decoding techniques in one embodiment. Figure 23 is a logic diagram illustrating transition control and selective block inversion encoding in one embodiment. A component of the link layer receives codes to be transmitted one code at a time from the

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transport layer. In block 2301, the component performs transition control optimization to generate a symbol from the code. In block 2302, the component buffers the symbols until a complete block of symbols has been buffered. In decision block 2303, if a complete block of symbols has been buffered, then the component continues at a block 2304, else the component waits to receive the next code. In decision block 2304, if the running disparity is equal to the block disparity, then the component continues at block 2305, else the component continues at block 2306. In block 2305, the component performs block inversion on the symbols of the block. In block 2306, the component provides the symbols of the buffer to the physical layer and then waits to receive the next code from the transport layer.

[00133] Figure 24 is a logic diagram illustrating transition control optimization in one embodiment. In block 2401, the component receives a code for transition optimization. In block 2402, the component counts the number of transitions in the received code. In block 2403, if the number of transitions is less than four (assuming an 8-bit code), then the component continues at block 2405, else the component continues at block 2404. In block 2404, the component sets the ninth bit to a 0-bit value. In block 2405, the component performs alternate bit inversion on the received code by inverting every other bit. In block 2406, the component sets the ninth bit to a 1-bit value. In block 2407, the component generates the symbol as the ninth bit value plus the code.

[00134] Figure 25 is a logic diagram illustrating block inversion in one embodiment. In block 2501, the component selects the first symbol of the block. In block 2502, the component performs alternate bit inversion on the selected symbol by inverting alternate bits. In block 2503, the component selects the next symbol of the block. In decision block 2504, if all the symbols have already been selected, then the component completes, else the component continues at block 2505. In block 2505, the component inverts the selected symbol by inverting the value of each bit in the selected symbol. The component then selects the next symbol of the block.

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[00135] Figure 26 is a logic diagram illustrating transition control and selective block inversion decoding in one embodiment. The component of the link layer is provided with one symbol at a time by the physical layer. In block 2601, the component stores the symbol in a buffer. In decision block 2602, if the buffer contains a primitive, then the component continues at block 2603 to process the primitive, else the component continues at block 2604. In block 2604, if the buffer contains a complete block, then the component continues at block 2605, else the component waits for the next symbol. In decision block 2605, if the first symbol in the buffer is an out-of-band symbol, then the transmitting communications node inverted the block and the component continues at block 2606, else the component continues at block 2607. In block 2606, the component undoes the block inversion of the block. In block 2607, the component selects the next symbol of the block. In decision block 2608, if all the symbols have already been selected, then the component waits for the next symbol, else the component continues at block 2609. In block 2609, the component undoes the optimization of the transitions of the selected symbol to generate the corresponding code. In block 2610, the component provides the code to the transport layer and then processes the next symbol of the block.

[00136] Figure 27 is a logic diagram illustrating the undoing of block inversion in one embodiment. In block 2701, the component selects the first symbol of the block. In block 2702, the component inverts alternate bits of the selected symbol. In block 2703, the component selects the next symbol of the block. In decision block 2704, if all the symbols have already been selected, then the component completes, else the component continues at block 2705. In block 2705, the component inverts all the bits of the selected symbol and then processes the next symbol of the block.

[00137] Figure 28 is a logic diagram illustrating the undoing of transition control optimization in one embodiment. In decision block 2801, if the ninth bit of the symbol is one, then the component inverts alternate bits of the symbol in block 2802. The component then outputs the resulting code.

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[00138] Figure 29 is a logic diagram illustrating the processing of a primitive in one embodiment. Although not shown, the component may ensure that the disparity of the symbols of the primitive are in the correct order. In decision blocks 2901-2903, the component decodes the primitive. In blocks 2904-2906, the component raises a signal indicating the primitive that has been received. In one embodiment, the signals may be provided to the transport layer to control the packetizing of the received codes.

2. MEMORY LINK ARCHITECTURE

[00139] In one embodiment, various transport layer, link layer, and physical layer techniques can be used to provide a serial communications architecture that is well suited to support memory-based data store devices, especially multiport memory devices with random access memory. This architecture that is adapted to memory devices is referred to as "Memory Link." A multiport memory device provides multiple serial communications ports that can be connected to different hosts (e.g., any memory accessing device, such as a memory controller). Each host can independently access the memory of the memory device to read and write data. The memory may be organized into memory banks that can be simultaneously accessed by the same or different hosts. Many applications can advantageously use a multiport memory device. For example, an asynchronous transfer mode ("ATM") switch can use a multiport memory device to replace a crossbar switch. The ATM switch may have multiple input ports that store received data in the multiport memory device and multiple output ports that retrieve data from the multiport memory device. A multiport memory device may include a switch for dynamically interconnecting the memory to the ports so that each port can selectively access each memory bank. Alternatively, the ports may access memory using time-division multiplexing techniques.

[00140] Because of the way memory is typically accessed, the physical layer, link layer, and transport layer might be simplified as compared to the layers needed in a more general data store device, such as a disk drive. Each port of a multiport

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memory device is typically directly connected to a host. In such a case, packets do not need to specify a source and a destination and the headers are thus simplified. In addition, packet types can be encoded in synchronization primitives to further simplify the packet header. The transport layer of a port in a multiport memory device can be simplified or eliminated because (1) routing to another device is not needed, (2) minimal or no parsing of the header may be needed, and (3) preemption and priority ordering of packets may not be needed. In addition, the link layer may be simplified by the use of physical layer DC-balancing, rather than the use of the selective block inversion to achieve DC-balance. Physical layer DC-balancing can be used with a multiport memory device because the distance between the host and the multiport memory device is typically relatively short.

[00141] The physical layer may also be simplified because a single multiphase clock generating device, such as an analog phase lock loop ("PLL"), or a delay lock loop, can be used to provide clocking for the transmitter and receiver for each port of the multiport memory device. The use of a single multiphase clock generating device can greatly reduce the area of a multiport memory chip used by the physical layer. A single-chip, multiport memory device has traditionally been infeasible because of the need to have multiple analog phase lock loops. The physical layer may also use plesiosynchronous null insertion techniques as described below to compensate for variations in the frequency between clocks of the hosts and the clock of the multiport memory device. The multiport memory device may transmit control information using out-of-band symbols as described above. Also, commands for accessing the memory device may be encoded in synchronization symbols.

[00142] Figure 30 is a block diagram illustrating the overall architecture of a multiport memory device in one embodiment. The multiport memory device 3000 includes multiple ports 3010-3019. Each port includes a physical layer, a link layer, a transport layer (optional), and an access layer. The access layers are connected to switch 3050. The multiport memory device includes memory with

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memory banks 3320-3027. Each memory bank has associated bank cache 3030-3037. The bank caches are connected to the switch. A switch arbiter (not shown) is responsible for connecting the ports to the bank caches as needed to process the memory access requests. Each port can be independently and simultaneously connected to memory banks. Alternatively, access of the ports to the memory banks can be time-division multiplexed. With time-division multiplexing, each port has its allotted time period for communicating with the memory bank. A clock signal with a different phase for each port can be used to coordinate the access. The physical layer, link layer, and transport layer may be implemented to provide various combinations of the functions described above (e.g., transition control optimization and synchronization primitives encoded with packet types). The access layer receives commands and data from the transport layer, directs the arbiter to connect the port to the appropriate memory bank, and transmits commands and data to the memory bank. The access layer also receives data from the memory banks and provides the data to the transport layer for transmission to the host.

[00143] Figure 31 is a block diagram illustrating the use of a single phase lock loop for the physical layer of a multiport memory device in one embodiment. The physical layer 3100 of the multiport memory device includes multiple ports 3110-3119. Each port includes a serial communications line connected to a transmitter and another serial communications line connected to a receiver that comprise the serial communications link. Each port also includes a serializer and deserializer. The phase lock loop 3120 receives a clock signal from clock 3121. The phase lock loop outputs a clock signal 3122 and phase shifted clock signals 3123. The clock signal 3122 provides clocking information for the serializer. The phase shifted clock signals 3123 are provided to the deserializers to control the sampling of the input data.

[00144] Figure 32 is a block diagram illustrating contents of a bank cache in one embodiment. Each bank cache includes an input queue 3201 and an output queue 3202. Each entry of the input queue includes a port field, a read/write field,

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an address field, and a data field. The port field identifies the port (e.g., 3) that provided the command. The read/write field identifies whether the access is a read or a write (i.e., R or W). The address field identifies the memory address to be accessed (e.g., 1000). The address field may be latched from the address bus. The data field includes the data to be written to memory. Each entry of the output queue includes a valid field, a port field, and a data field. The valid field indicates whether the entry contains valid data (e.g., 0 or 1). If a memory bank has multiple sections as described below, then the valid field may have a bit indicating whether the data of each section is valid. The port field identifies the port (e.g., 3) to which the data is to be transmitted. The data field contains the data retrieved from memory. Each memory bank successively retrieves entries from the input queue and then performs the requested access. When the access is to read data from memory, the memory bank also adds entries to the output queue. The memory bank adds an entry to the output queue on every possible read cycle. The valid field is used to indicate whether the entry contains valid data.

[00145] Figure 33 is a logic diagram illustrating processing of the access layer when it receives data from a host in one embodiment. In block 3301, a component of the access layer receives the next command from the transport layer. In decision block 3302-3304, the access layer parses the command. In block 3305-3307, the component performs the processing associated with that command.

[00146] Figure 34 is a logic diagram illustrating the processing of a write command by the access layer in one embodiment. In block 3401, the component retrieves the target address for the write command. In block 3402, the component requests the arbiter to configure the switch to connect the port with the appropriate memory bank. In block 3403, the component retrieves the next byte (i.e., code) from the transport layer. In decision block 3404, if all the bytes have already been retrieved, then the write is complete, else the component continues at block 3405. In block 3405, the component stores an entry into the input queue of the memory bank. The component may need to buffer multiple bytes depending on the width

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of the word. In block 3406, the component increments the address and then reads the next byte. One skilled in the art will appreciate that when time-division multiplexing is used, the component supplies the data to the input queue during its allotted time period.

[00147] Figure 35 is a logic diagram illustrating processing of the access layer when it is to provide data to the transport layer in one embodiment. In block 3501, the component receives the next byte from the switch. In decision block 3502, if all the bytes have already been received, then the component continues at block 3504, else the component continues at block 3503. In block 3503, the component provides the byte to the transport layer and then proceeds to receive the next byte. In block 3504, the access layer signals the end of the read to the transport layer.

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2.1 Multisection Memory Banks

[00148] Figure 36 is a block diagram of a multisection memory bank in one embodiment. A multisection memory bank can significantly reduce power consumption of a memory device. A multisection memory bank subdivides each row (or word) of data in a memory bank into multiple sections. The enabling of sections can be configured on a port-by-port basis. When a section is disabled, then the amount of power consumed by the memory bank during an access is much less than if the section was enabled. In this way, each port can specify only the needed sections which can result in a significant reduction in the power consumption because only the needed sections are enabled during access. The data for all the rows for each subdivision of a memory bank is stored in a section (or a page). For example, a memory bank may have a word width of 64 bits. Such a multisection memory bank may be divided into two sections of 32 bits each that can be accessed independently and simultaneously based on configurable parameters. If a host only needs a 32-bit word, then only one section needs to be enabled whenever that host accesses the memory bank.

[00149] As shown in Figure 36, the multisection memory bank includes section 3600 and section 3610 each of which is 32 bits wide. Each wordline of each

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section includes an AND gate 3601, 3611 that is connected to a corresponding line of the row decoder 3630 and to a section enable line from configuration register 3650. The row decoder decodes the row portion of the address and enables the appropriate wordline when the corresponding section is enabled. For example, if the row portion of the address is eight bits, then the row decoder enables one of 256 wordlines. The AND gate enables the wordline for its section only when that section is enabled for the port. If a port only accesses section 3600, then whenever an access for the port is processed, section 3600 is enabled and section 3610 is disabled. Each wordline of each section may also include a sequence of latches 3602, 3612 for buffering signals. The number of latches needed depends on row access latency, column access latency, and desired level of simultaneous access. Each section also includes a column decoder and column cache 3603, 3613. The column decoder latches data into the column cache based on the column address provided by the sequence of latches 3104, 3114 for buffering column address. Because the wordlines are only enabled on a section-by-section basis and because retrieved data is only latched on a section-by-section basis, the power requirements of a multisection memory bank is lower than a memory bank that does not have multiple sections. When data is retrieved from a multisection memory bank, the valid field of the output queue indicates the divisions of the word that are valid. For example, if data is retrieved from only section 0, then the valid field may contain "10." If data is retrieved from both sections 0 and 1, then the valid field may contain "11." One skilled in the art will appreciate that a memory bank may be subdivided into a number of sections. Also, a multisection memory bank may simultaneously perform multiple access commands so long as the commands do not access the same wordline of the same section. Thus, the processing of a command to access wordline 10 of section 0 may overlap with the processing of a command to access wordline 11 of section 0. Also, the processing of a command to access wordline 10 of section 0 may be overlapped with the processing of a command to access wordline 10 of

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section 1. Thus, increasing the number of sections of a memory bank can increase the amount of parallel processing that can be performed.

2.2 Physical layer DC-balancing

[00150] In one embodiment, DC-balancing of the communications link is handled at the physical layer in memory link. The performing of DC-balancing at the physical layer can help reduce the cost and complexity of the link layer. To help ensure DC-balance, the physical layer uses a variable strength line driver that can drive a standard strength or increased strength 0-bit value or 1-bit value onto the communications link. When the running disparity is zero or positive (i.e., in the 1-direction) and a 1-bit value is to be transmitted, then a standard strength 1-bit value is driven. Similarly, when the running disparity is a zero or negative (i.e., in the 0-direction) and a 0-bit value is to be transmitted, then a standard strength 0-bit value is driven. In contrast, when the running disparity is negative and a 1-bit value is to be transmitted, then an increased strength 1-bit value (i.e., a 1-bit voltage value) is driven. This increased strength 1-bit value tends to offset the effects of a negative running disparity. Similarly, when the running disparity is positive and a 0-bit value is to be transmitted, then an increased strength 0-bit value (i.e., a 0-bit voltage value) is driven. This increased strength 0-bit value tends to offset the effects of a positive running disparity. The use of a variable-strength line driver is especially useful in controlling DC-balance over short transmission distances. In such a case, physical layer DC-balancing can be used in lieu of link layer DC-balancing.

[00151] Figure 37A is a block diagram illustrating a variable strength line driver in one embodiment. A variable strength line driver 3700 includes a fixed-strength component (or portion) 3701 and a variable-strength component 3702. The variable-strength line driver has 4 inputs: data in 3703, negative running disparity signal (RD-) 3705, positive running disparity signal (RD+) 3706, and enable signal 3707. The variable-strength line driver has one output: data out 3704. The fixed-strength component outputs a standard strength 0-bit value or 1-bit value depending on data in. The variable-strength component pulls up, pulls down, or

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has no effect on data out, depending on the running disparity and data in. If the running disparity is positive and data in is a 0-bit value, then the variable-strength component pulls down data out. If the running disparity is negative and data in is a 1-bit value, then the variable-strength component pulls up data out. More generally, the running disparity signals may indicate when the running disparity is sufficiently negative or sufficiently positive to activate the variable-strength component.

[00152] Figure 37B is a block diagram illustrating the circuit of a variable-strength line driver in one embodiment. The fixed-strength component 3701 and the variable-strength component 3702 employ the same logic to activate their pull-up and pull-down transistors. One skilled in the art will appreciate that the transistors may be selected to achieve the overall desired physical layer characteristics of the communications link. NAND gate 3710 is used to control pull-up transistor 3711, and NOR gate 3712 is used to control pull-down transistor 3713. When the data in is a 1-bit value and the driver is enabled, NAND gate 3710 outputs a 0, which turns on pull-up transistor 3711. When the data in is a 0-bit value and the driver is enabled, NOR gate 3712 outputs a 1, which turns on pull-down transistor 3713. The variable-strength component has similar control logic, except that pull-up transistor 3721 is activated only when the running disparity is negative and except that the pull-down transistor 3723 is activated only when the running disparity is positive.

3. PLESIOSYNCHRONOUS CLOCKING WITH NULL INSERTION/REMOVAL

[00153] In one embodiment, the serial communications architecture specifies that NULL symbols or NULL primitives are inserted into or removed from a stream of symbols to account for variations in clock frequency between the transmitting and receiving communications nodes when using plesiosynchronous clocking. If a transmitting communications node transmits at a slightly higher frequency than the receiving communications node receives, then the receiving communications node

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traditionally needs to buffer the received symbols to handle such an overrun. For example, if both communications nodes use clocks with a frequency of 100 Hz with a maximum variation of 1%, then it is possible that the transmitting communications node transmits at 101 Hz and the receiving communications node receives at 99 Hz. In such a case, the receiving communications node will receive an extra 2 bits approximately every second, assuming 1 bit is transmitted every clock cycle. Receiving communications nodes typically have an elastic buffer for storing and aligning these extra bits on symbol boundaries. Similarly, an underrun occurs when a transmitting communications node transmits data at a slightly lower rate than the receiving communications node receivers. The handling of an underrun can also be costly and complex. These underrun and overrun conditions were typically handled at the link layer. These complexities and costs may, however, be avoided by the physical layer of a receiving communications node periodically inserting or removing NULL symbols or NULL primitives from the received stream of symbols at a rate sufficient to compensate for variations in clock frequencies.

[00154] Figure 38A is a block diagram of a plesiosynchronous communications system in one embodiment. Communications node 3801 and communications node 3811 are connected via a bi-directional serial link. The transport layer and the link layer 3802, 3812 may be implemented in a single digital ASIC chip with other interface logic such as PCI bus interface logic. The physical layer 3803 and 3813 may be built in a separated custom analog chip.

[00155] The link layer provides symbols (i.e., N-bit encoded data) to be transmitted to the physical layer via TX_DAT lines. The link layer is provided symbols received by the physical layer via the RX_DAT lines. In one embodiment, the TX_DAT and RX_DAT lines are both synchronized to the local clock, and the setup/hold time relation between TX_DAT and RX_DAT are the same to setup/hold time relationship to the local clock. Both the transmitter 3804, 3814 and receiver 3805, 3815 of the physical layer share the same phase lock loop ("PLL") 3806, 3816. This overall architecture is described in U.S. Patent

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Application No. 6,229,859, entitled "System and Method for High-Speed, Synchronized Data Communication."

[00156] Figure 38B is a block diagram illustrating a switch supporting multiple data store devices in one embodiment. The switch 3820 has 5 ports 3821-3825. Ports 3821-3824 are shown connected to disk drives 3831-3834. The switch has one phase lock loop 3826 that is shared by all the ports. Since all the ports of the switch are synchronized to the same clock, the data can be freely (without buffering) transferred between ports. (See discussion below on asynchronous clock boundaries.)

[00157] Figure 39A is a block diagram illustrating a prior art synchronous clocking system. In this synchronous clocking system, the RX_DAT lines provided to the link layer 3920 are synchronized not to the local clock, but to the RX_CLK line provided by the physical layer. The RX_CLK line provides a clock that has been recovered from the incoming bit stream, which is synchronized to the transmitter's clock. The receiver may recover the clock from a clock signal on a separate line or from the stream of data bits transmitted by the transmitter. In the link layer, there are two clock domains, the TX clock domain 3921 that is the same as the local clock domain, and the RX clock domain 3922 that is the same as the transmitter's clock domain. Consequently, an asynchronous clock boundary 3923 is formed between the TX clock domain and the RX clock domain. When information is transferred from the TX clock domain to the RX clock domain, the FIFO 3924 is used for the data and flip-flop synchronizer 3925 is used for the control information. When information is transferred from the RX clock domain to the TX clock domain, the FIFO 3926 is used for the data and the flip-flop synchronizer 3927 is used for the control information.

[00158] Figure 39B is a block diagram illustrating resolution of an asynchronous clock boundary in the physical layer in one embodiment. The clock and data recover ("CDR") processing of the physical layer 3950 provides to the link layer RX_DAT lines that are synchronized to the local clock. Thus, the asynchronous boundary at the link layer along with the needed logic to resolve the boundary is

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avoided in the link layer. The CDR processing also provides a 1-bit control signal (DET_NULL) that indicates a NULL symbol is provided in RX_DAT (i.e., to inform the link layer that a primitive has been received) and a 1-bit control signal (DET_ERR) that indicates an error in the physical layer data recovery.

[00159] Figure 40 is a block diagram illustrating NULL insertion and deletion at the physical layer in one embodiment. Sampler 4010 in one embodiment corresponds to the over sampler 4011, digital phase lock loop 4012, and phase selector 4013 described in U.S. Patent No. 6,229,859, entitled "System and Method for High-Speed, Synchronized Data Communication." The sampler outputs N+1 bits (where N is the number of bits in a symbol) of data lines D[0:N] and two valid bits V[N-1] and V[N]. The sampler identifies a stream of data bits that are received and provides those data bits in data lines D[0:N]. The valid bits indicate whether D[N-1] and D[N] contain valid data (e.g., V[N-1] = 1 indicates that D[N-1] is valid). The data bits provided by the sampler are not, however, frame (i.e., symbol) aligned; that is, D[0] is not necessarily (and more often than not would not be) the first bit in a symbol. The valid bits indicate whether an overrun or underrun condition has occurred. An overrun occurs as a result of the transmitter's clock frequency being faster than the receiver's, and an underrun occurs as a result of the transmitter's clock frequency being slower than the receiver's. Nominally, N data bits are provided by the sampler every sample interval. In such a case D[N-1] is valid, but D[N] is invalid. If, however, there is an overrun, then the sampler provides N+1 data bits; that is, D[N-1] and D[N] are both valid. If there is an underrun, then the sampler provides N-1 data bits; that is, D[N-1] and D[N] are both invalid. The data bits and the valid bits are supplied to a frame aligner 4020. The frame aligner not only aligns the frames, but also inserts and removes NULL symbols to adjust for variations in the transmitting and receiving clock frequencies.

[00160] Figure 41 is a block diagram illustrating the frame aligner in one embodiment. The frame aligner 4100 includes bit buffer 4101, sync and null detector 4103, symbol pointer tracker 4104, and multiplexer 4102. The bit buffer

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stores the last 27 bits (e.g., 3 X N) received as provided by D[0:9], assuming that a symbol includes 9 bits. The bit buffer is organized into three buffers or regions (i.e., A, B, and C) of 9 bits each. The sync and null detector scans the bit buffer to detect whether it contains a NULL primitive and, in particular, a synchronization primitive. If a synchronization primitive is detected, it signals the symbol pointer tracker to align itself on the synchronization primitive. The sync and null detector also signals the symbol pointer tracker whether a NULL symbol should be inserted or removed from the symbol stream. The symbol tracker pointer tracks the symbol alignment over time.

[00161] The sync and null detector provides a 1-bit load data signal ("LD"), a 1-bit last half signal ("iHF"), and a 9-bit synchronization symbol pointer ("iPTR") to the symbol pointer tracker. The LD signal indicates that a synchronization symbol has been detected. The iHF signal indicates whether the synchronization symbol starts in the first or last half of one of the 9-bit buffers of the bit buffer. The iPTR signal indicates a bit position of the start of the synchronization primitive in the bit buffer.

[00162] The symbol pointer tracker provides 1-bit null selection signal ("uHF") and 9-bit start-of-symbol pointer ("uPTR") to the multiplexer. The uHF signal indicates whether to insert a NULL symbol into the stream of symbols, and the uPTR signal indicates the start bit position of a symbol. The symbol pointer tracker also provides 1-bit error signal ("DET.ERR") and 1-bit null signal ("DET.NULL") to the link layer. The multiplexer provides the 9-bit RX_DAT to the link layer.

[00163] Figures 42A, 42B, and 42C illustrate the loading of the bit buffer in one embodiment. The bit buffer contains three 9-bit buffers A[8:0], B[8:0], and C[8:0]. When the valid bits V[8:9] indicate that only D[8] is valid (i.e., V[8:9] = "10" a normal condition), then all the data in the bit buffer is rotated 9 bits to the left. In other words, the data from B[8:0] is transferred to A[8:0], the data from C[8:0] is transferred to B[8:0], and the data from D[0:8] is transferred to C[8:0] as indicated by Figure 42A. When the valid bits V[8:9] indicate that neither D[8] or D[9] is valid (i.e., V[8:9]="00" an underrun condition), then the data in the bit buffer is rotated

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8 bits to the left. In other words, A[0] is transferred to A[8], B[8:1] is transferred to A[7:0], B[0] is transferred to B[8], C[8:1] is transferred to B[7:0], C[0] is transferred to C[8], and D[0:7] is transferred to C[7:0] as illustrated by Figure 42B. When the valid data V[8:9] indicates that both D[8] and D[9] are valid (i.e., V[8:9]="11" an overrun condition), then the data in the bit buffer is rotated 10 bits to the left. In other words, B[7:0] is transferred to A[8:1], C[8] is transferred to A[0], C[7:0] is transferred B[8:1], D[0] is transferred to B[0], and D[1:9] is transferred to C[8:0] as illustrated by Figure 42C.

[00164] Figure 43 is a diagram illustrating the detection of a synchronization primitive by the sync and null detector in one embodiment. Assuming that the synchronization detection mode is falling edge, the detector determines whether there are only three falling edges in the bit buffer and whether they are 9 bits apart. If so, the detector sets the LD signal to 1, else the detector sets the LD signal to 0. If the falling edges are in the first half of the bit buffer (e.g., A[8:5]), then the detector sets the iHF signal to 0, else the detector sets the iHF signal to 1. The detector also sets the iPTR signals to indicate the position of the falling edge that starts the synchronization symbols, which indicate the start bit position of the synchronization symbol. In this example, the bit buffer 4301 contains the synchronization primitive "100000001-100111111" starting at A[6] and a portion of that synchronization primitive starts at C[6]. If A[8:7] contained a falling edge from a non-synchronization symbol, then when the next symbol of the second synchronization primitive is received from the sampler, the bit buffer would be guaranteed to contain only three falling edges. The bit buffer 4302 contains the same synchronization primitives.

[00165] Figure 44 is a diagram illustrating the portion of the bit buffer that contains the next symbol to be extracted in one embodiment. If the start of a symbol is in the first half of a region of the bit buffer (i.e., A[8:5]), then the symbol is extracted starting in the B region of the bit buffer and proceeding to the C region. If the start of a symbol is in the last half of a region of the bit buffer (i.e., A[4:0]), then the

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symbol is extracted starting in the A region of the bit buffer and proceeding to the B region.

[00166] Figure 45 is a state diagram of the symbol pointer tracker in one embodiment. The symbol pointer tracker tracks the start position of a symbol (e.g., frame) based on the start position of a synchronization symbol and the valid bits (e.g., V[8:9]) provided by the sampler. The symbol pointer tracker enters an initial state ("INIT") whenever the LD signal of the sync and null detector indicates that a synchronization symbol has been detected. The tracker stays in that initial state so long as the frame aligner is provided with 9 valid bits (i.e., N valid bits) at a time (i.e., V[8:9]="10" a normal condition). If the frame aligner is provided with 10 valid bits (i.e., V[8:9]="11" an overrun condition), then the tracker enters a first overrun state ("OVR1"), which means that the transmitter's clock frequency is faster than the receiver's clock frequency. The tracker stays in the first overrun state so long as the frame aligner is provided with 9 valid bits at a time. If the frame aligner is provided with 10 valid bits, then the tracker enters the second overrun state ("OVR2") from the first overrun state. If the frame aligner is provided with 8 valid bits, then an error has occurred (e.g., 10 bits valid followed by 8 bits valid) and enters an error state from the first overrun state. The tracker exits the second overrun state when the next bits are provided to the frame aligner. If the tracker is provided with 9 valid bits, then the tracker returns to the first overrun state, else the tracker enters an error state. Once an overrun is detected, the tracker thus expects to receive only 9 or 10 valid bits at a time and does not expect to receive two sets of 10 valid bits in a row. The receiving of two sets of 10 valid bits in a row would indicate that the transmitter's clock frequency is too high to be compensated for by the receiver. The receiving of 8 bits in an overrun state indicates that the transmitter's clock frequency now appears to be slower, which means some sort of error has occurred. The first underrun state ("UND1") and the second underrun state ("UND2") are entered in a manner that is analogous to entry into the overrun states.

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[00167] When the tracker detects an LD signal of 1, it sets the start-of-symbol pointer to the start of the synchronization symbol as indicated by the iPTR lines and enters the initial state. It then sets the extraction region for the start-of-symbol pointer to A if the iHF signal is 1 and to B if the iHF signal is 0. The extraction region indicates the region that contains the first bit of the next symbol to be extracted. When the tracker detects an LD signal of 0, it moves the start-of-symbol pointer either backward or forward, depending on whether the tracker transitions to an overrun state as a result of receiving 10 bits or transitions to an underrun state as a result of receiving 8 bits.

[00168] Figure 46 is a diagram illustrating movement of the start-of-symbol pointer due to overrun or underrun in one embodiment. When a synchronization symbol is detected (i.e., LD=1), then the start-of-symbol pointer is somewhere within the range of A[3]:B[4]. If the transmitter's local clock frequency is slightly slower than the receiver's local clock frequency (i.e., a potential underrun condition), the tracker moves the pointer forward to the C region. When the pointer is moved into the underrun extend region (e.g., B[3]:C[8]) and a NULL symbol is detected, then the tracker moves the start-of-symbol pointer backward 9 bit positions (i.e., 1 symbol position) and inserts a NULL symbol at the start-of-symbol pointer. This insertion of the NULL symbol compensates for the underrun by adding an extra symbol to the received stream. In one embodiment, a NULL symbol can be any symbol of any primitive, that is, control or synchronization. Similarly, if the transmitter's local clock frequency is slightly faster than the receiver's local clock frequency (i.e., a potential overrun condition), the tracker moves the start-of-symbol pointer backward toward the A region. When the pointer is moved into the overrun extend region (i.e., A[8:4]) and a NULL symbol is detected, then the tracker moves the pointer forward 9 bits, which effectively removes the NULL symbol. The removal of the NULL symbol compensates for the overrun. One skilled in the art will appreciate that the size of the overrun and the underrun extend regions can be adjusted based on the maximum possible differences in

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clock frequencies between the transmitter and receiver and the guarantee frequency at which a NULL primitive is to be transmitted.

[00169] Figures 47A and 47B are diagrams illustrating NULL detection while the start-of-symbol pointer is not within the overrun or underrun extend regions in one embodiment. In this example, the pointer is at B[4]. Only 8 valid bits are provided to the frame aligner (i.e., an underrun condition); as a result, the pointer is moved forward to B[4]. A NULL symbol is also detected starting at B[4]. However, since the pointer is not within the overrun or underrun extend regions, no NULL symbol is removed or inserted and the two symbols of the NULL primitive are extracted.

[00170] Figures 48A and 48B are diagrams illustrating NULL detection while the start-of-symbol pointer is in the underrun extend region. The pointer enters the underrun extend region as a result of the transmitter's clock frequency being slightly slower than the receiver's clock frequency. When the transmitter's clock frequency is slower, the receiver can receive more data than the transmitter transmits and the receiver will eventually run out of data as the start-of-symbol pointer is moved forward. When the pointer is in the underrun region, the tracker inserts a NULL symbol when another NULL symbol is detected to account for the underrun. In this example, the pointer is at B[2] when a NULL symbol is detected. The tracker moves the pointer backward to A[2] (i.e., 1 symbol position) and inserts a NULL symbol at A[2]:B[3]. The inserted NULL symbol and the two NULL symbols of the NULL primitive are then extracted. In one embodiment, the inserted NULL symbol is a duplicate of the detected NULL symbol.

[00171] Figures 49A and 49B are diagrams illustrating NULL detection, while the start-of-symbol pointer is in the overrun extend region. The pointer enters the overrun extend region as a result of the transmitter's clock frequency being slightly faster than the receiver's clock frequency. When the transmitter's local clock frequency is faster, the receiver cannot receive as much data as the transmitter transmits, and so the receiver would eventually lose some data. When the pointer is in the overrun region, the tracker removes a NULL symbol of a NULL primitive when a NULL primitive is detected to account for the overrun. In this example, the

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pointer is at A[4] when a NULL symbol is detected. The tracker moves the pointer forward 1 symbol position, which effectively removes or skips over the NULL symbol at A[4]:B[5]. As a result, only the second NULL symbol of the NULL primitive is extracted. All primitives have the characteristic that each symbol of the primitive encodes the same information. Thus, one of the symbols of a primitive can be removed without loss of information.

[00172] From the foregoing, it will be appreciated that although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited, except as by the appended claims.

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CLAIMS

I/We claim:

[c1] 1. A method for transmitting packet types of packets, the method comprising:

receiving a packet having symbols;

identifying a packet type of the packet;

transmitting a synchronization symbol that corresponds to the identified packet type, wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol; and

transmitting the symbols of the received packet.

[c2] 2. The method of claim 1 wherein the symbols of the packet include in-band symbols and the synchronization symbols are out-of-band symbols.

[c3] 3. The method of claim 2 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

[c4] 4. The method of claim 1 wherein the synchronization symbol is transmitted before transmitting the symbols of the packet.

[c5] 5. The method of claim 1 wherein the packet has a header with a field that indicates packet type and the identifying of the packet type includes checking the field of the header that indicates packet type.

[c6] 6. The method of claim 1 wherein the packet types include a data packet.

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[c7] 7. The method of claim 1 wherein the packet types include a control packet.

[c8] 8. The method of claim 1 wherein the symbols are transmitted to a switch network.

[c9] 9. A method for identifying packet types of packets of symbols, the method comprising:

receiving a synchronization symbol indicating a packet type, each packet type having a different synchronization symbol;

receiving a packet of symbols; and

indicating that the received packet of symbols has the packet type of the received synchronization symbol.

[c10] 10. The method of claim 9 wherein the symbols of the packets include in-band symbols and the synchronization symbols are out-of-band symbols.

[c11] 11. The method of claim 10 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

[c12] 12. The method of claim 9 wherein the synchronization symbol is received before the symbols of the packet are received.

[c13] 13. The method of claim 9 wherein the packet types include a data packet.

[c14] 14. The method of claim 9 wherein the packet types include a control packet.

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[c15] 15. The method of claim 9 wherein the symbols are received from a switch.

[c16] 16. A communications device for transmitting packet types of packets, comprising:

an identification component that identifies a packet type of a packet of symbols; and

a transmission component that transmits a synchronization symbol that corresponds to the identified packet type, the transmitted synchronization symbol providing synchronization information and each packet type having a different synchronization symbol, and that transmits the symbols of the packet.

[c17] 17. The communications device of claim 16 wherein the symbols of the packet include in-band symbols and the synchronization symbols are out-of-band symbols.

[c18] 18. The communications device of claim 17 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

[c19] 19. The communications device of claim 16 wherein the synchronization symbol is transmitted before transmitting the symbols of the packet.

[c20] 20. The communications device of claim 16 wherein the packet has a header with a field that indicates packet type and the identification component checks the field of the header that indicates packet type.

[c21] 21. The communications device of claim 16 wherein the packet types include a data packet.

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[c22] 22. The communications device of claim 16 wherein the packet types include a control packet.

[c23] 23. The communications device of claim 16 wherein the symbols are transmitted to a switch network.

[c24] 24. The communications device of claim 16 wherein the communications device is part of a storage area network.

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METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS

ABSTRACT OF THE DISCLOSURE

A serial communications architecture for communicating between hosts and data store devices. The Storage Link architecture is specially adapted to support communications between multiple hosts and storage devices via a switching network, such as a storage area network. The Storage Link architecture specifies various communications techniques that can be combined to reduce the overall cost and increase the overall performance of communications. The Storage Link architecture may provide packet ordering based on packet type, dynamic segmentation of packets, asymmetric packet ordering, packet nesting, variable-sized packet headers, and use of out-of-band symbols to transmit control information as described below in more detail. The Storage Link architecture may also specify encoding techniques to optimize transitions and to ensure DC-balance.

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TOZOTT "S29S+00T

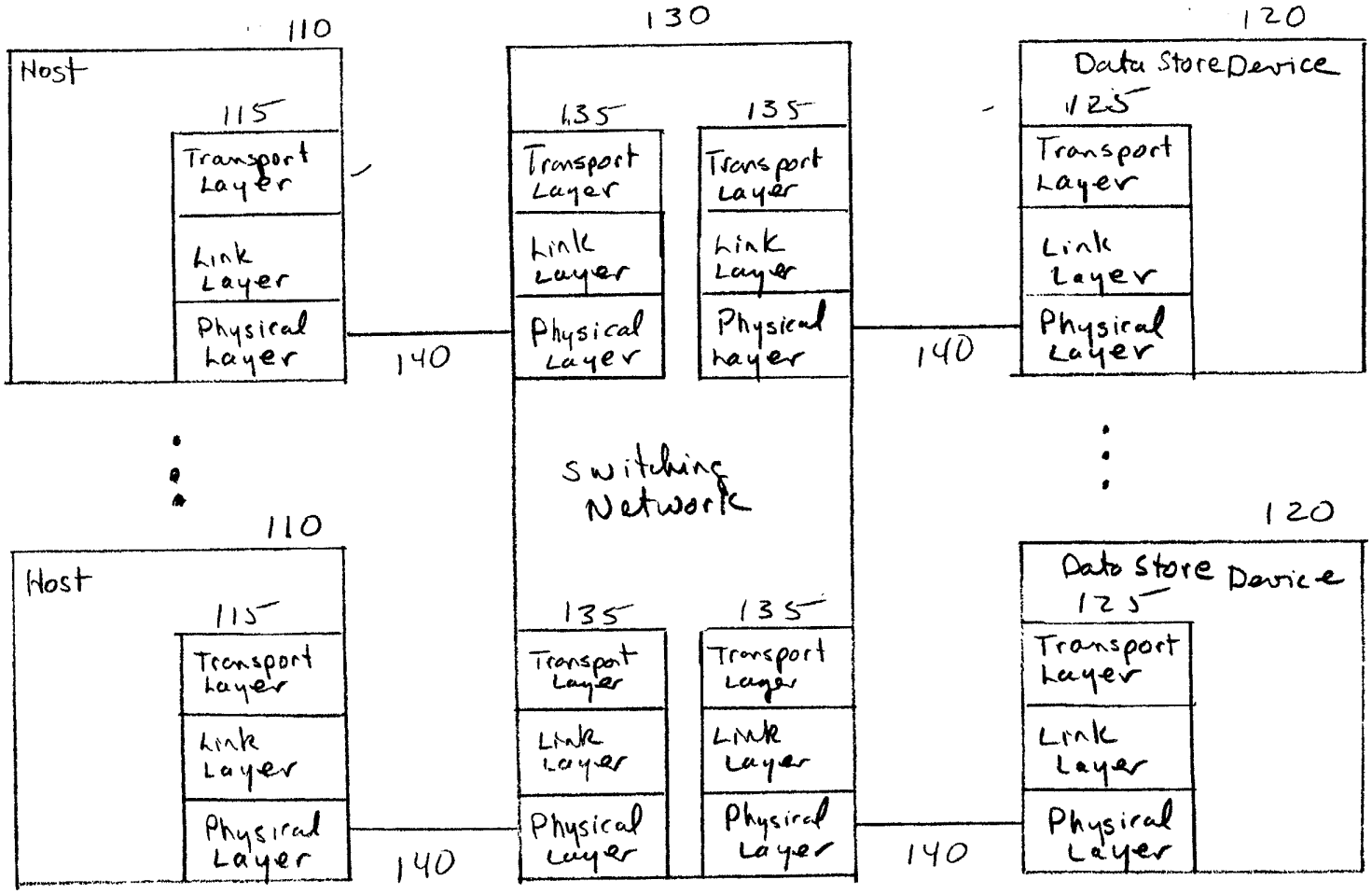


Fig 1

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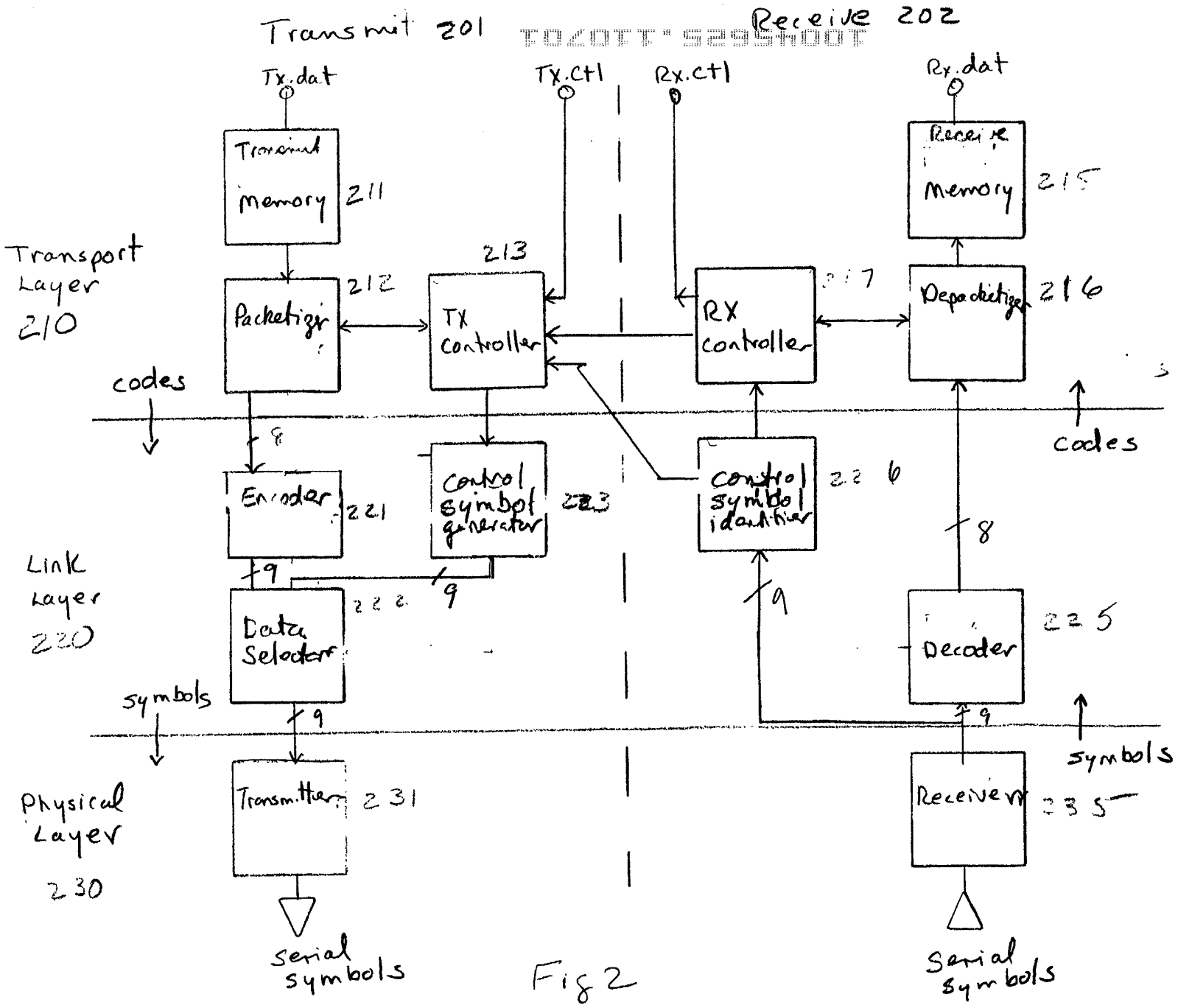


Fig 2

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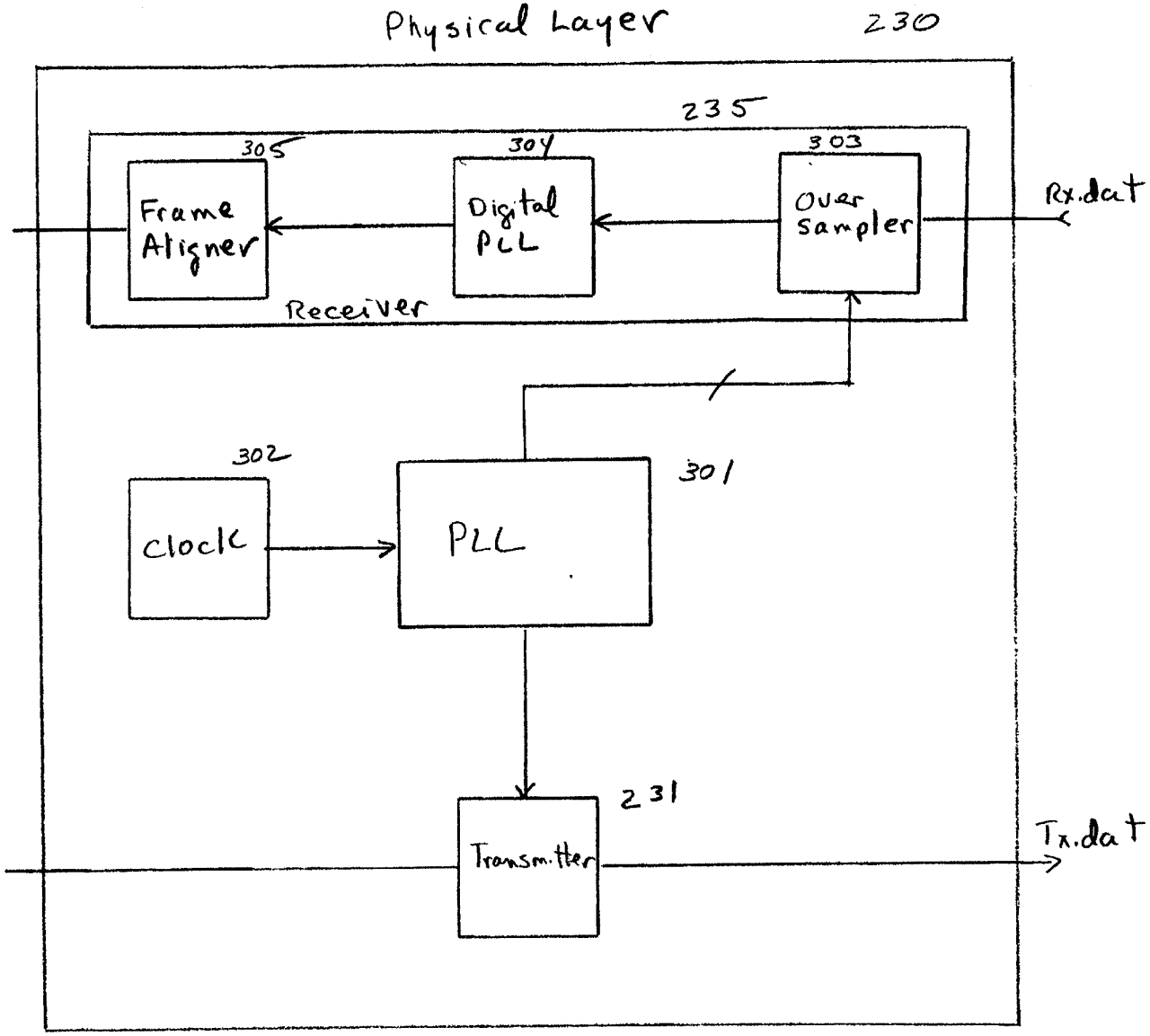


Fig 3

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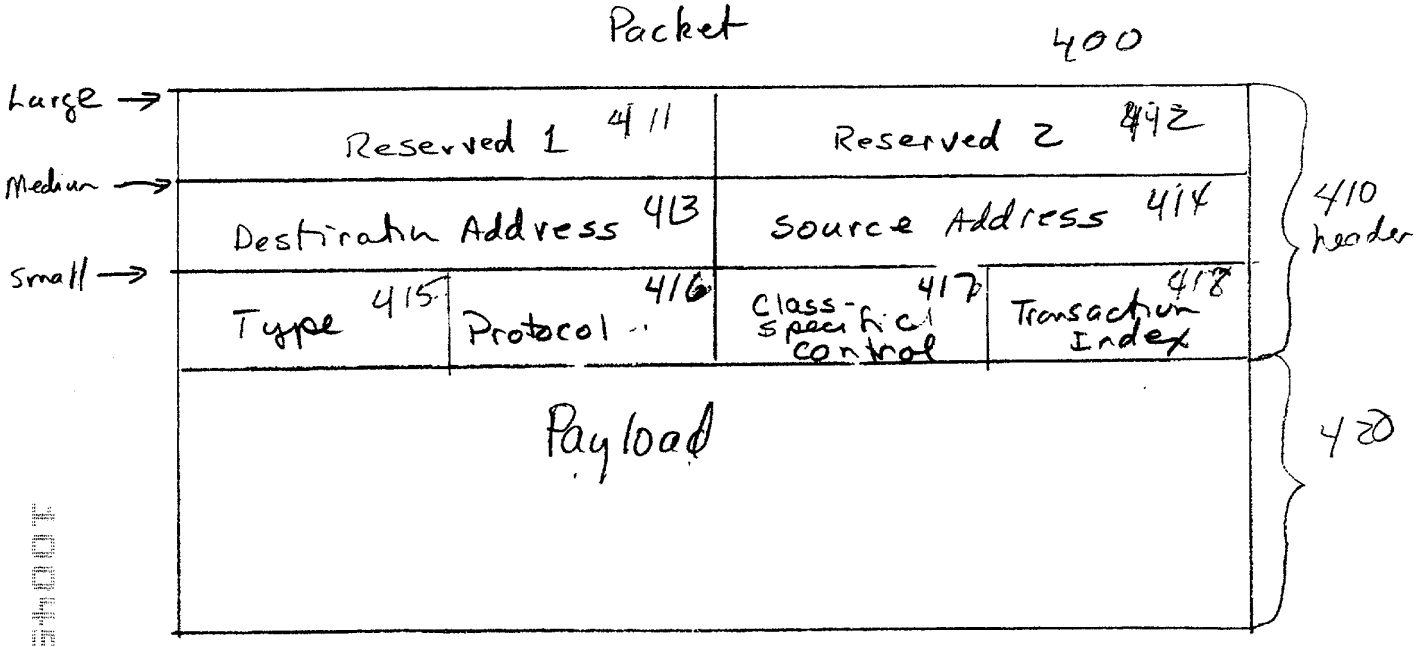


Fig 4

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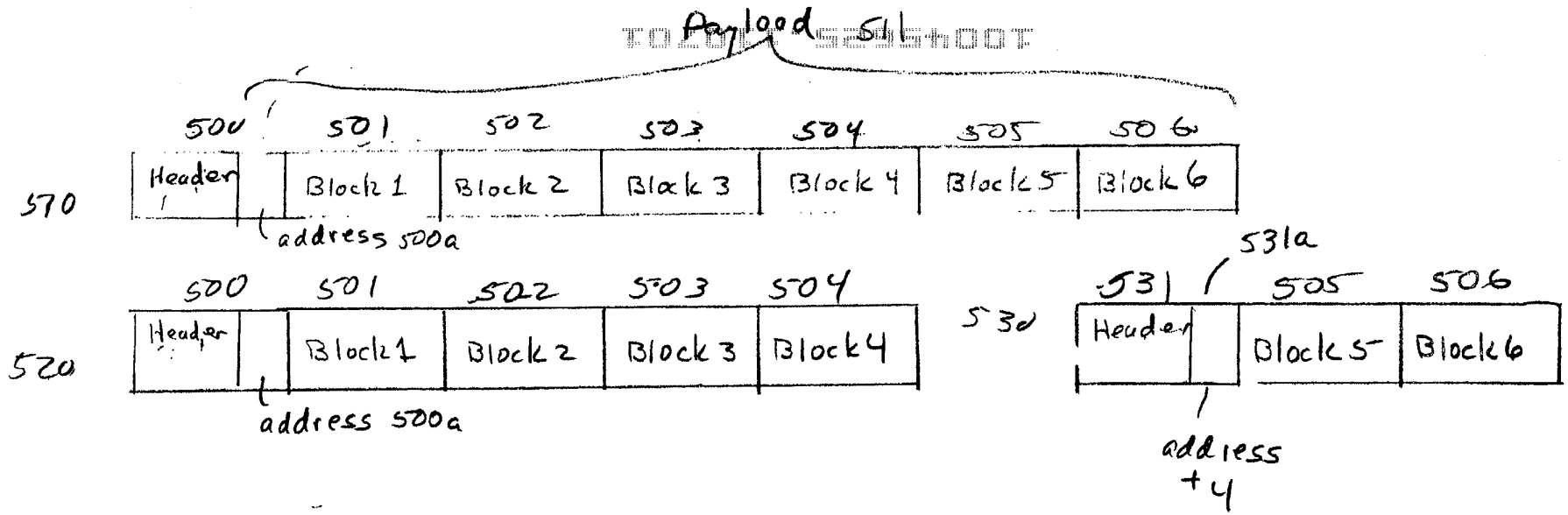


Fig 5

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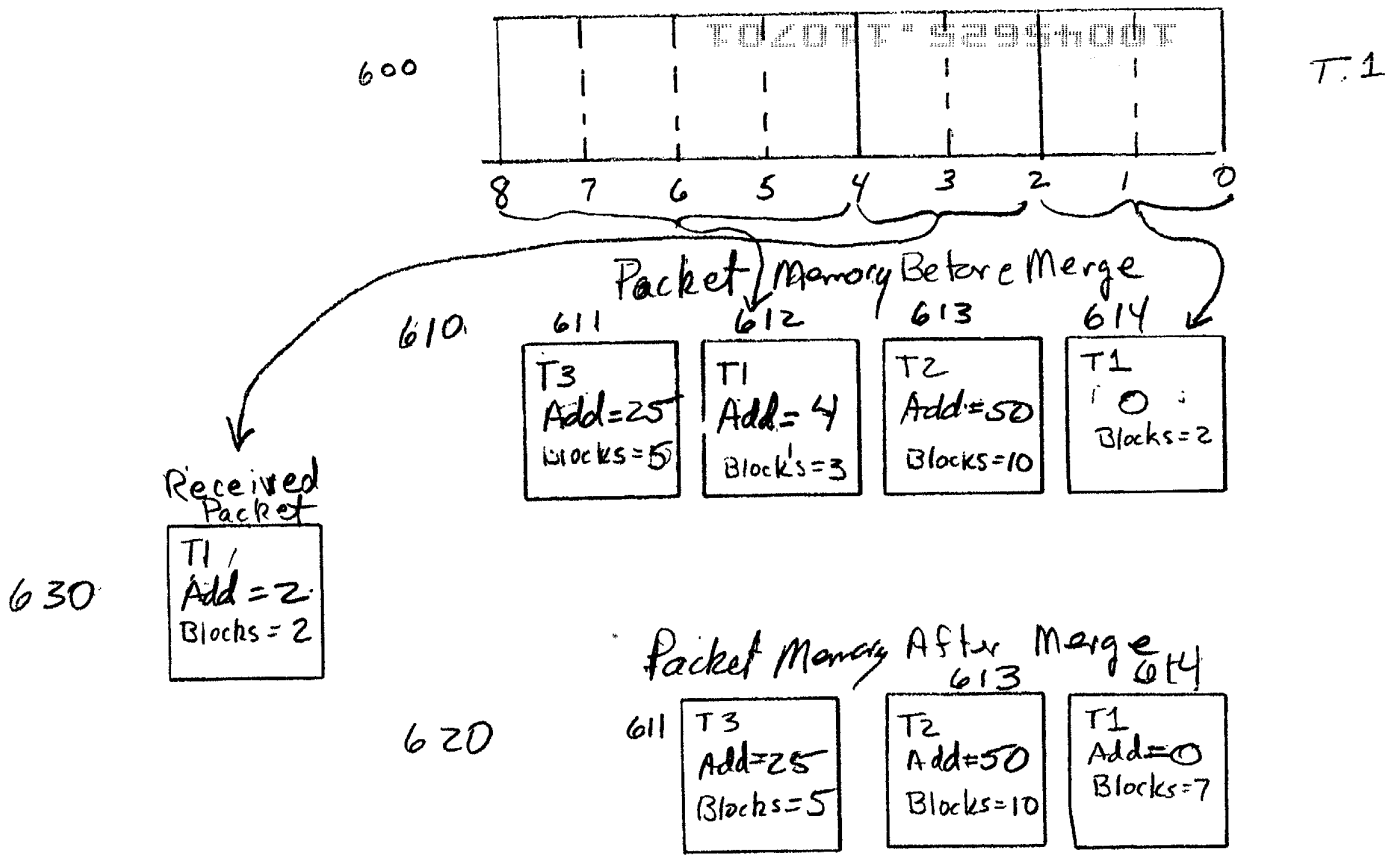


Fig 6

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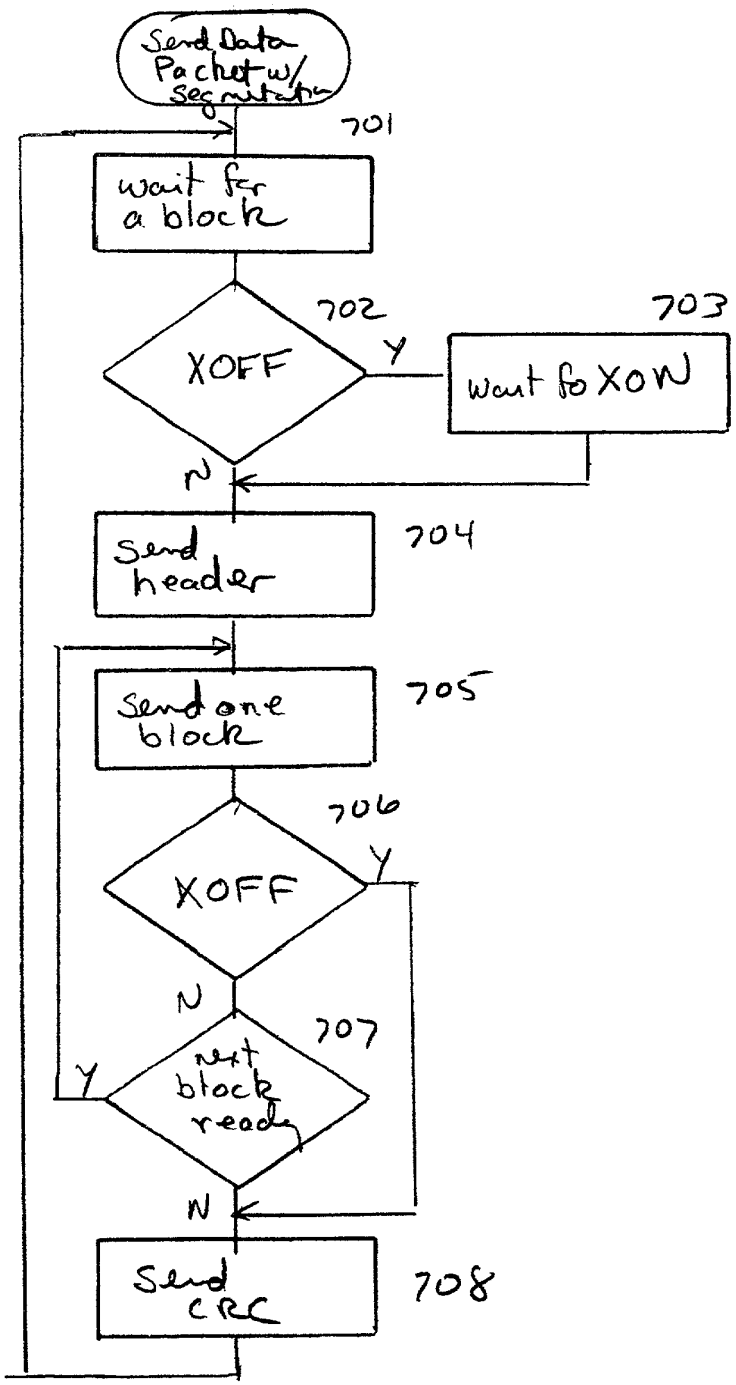
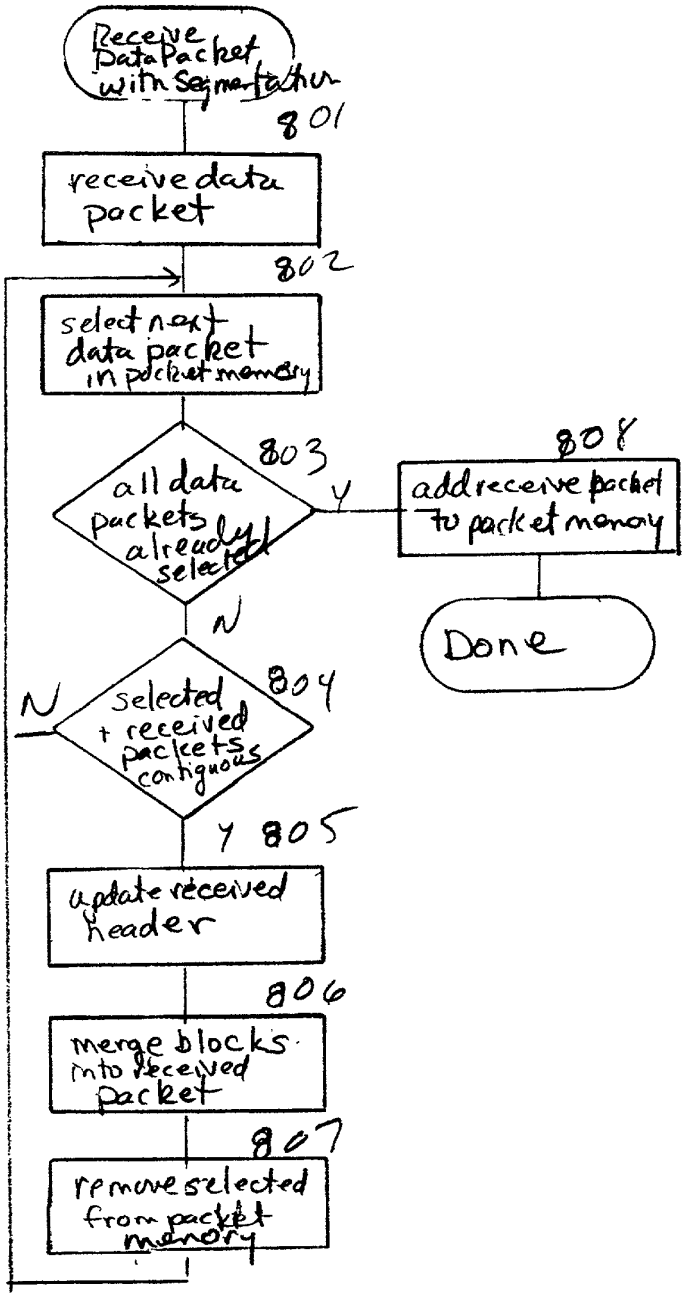


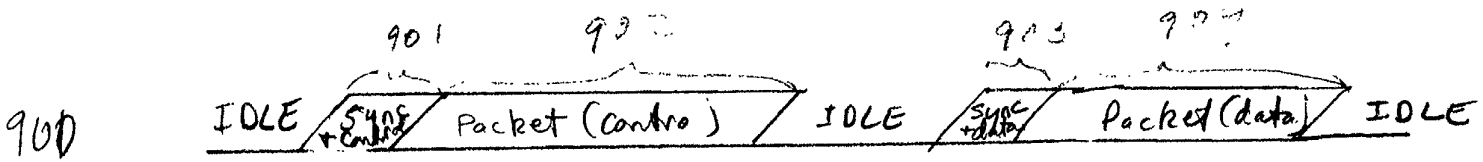
Fig 7

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F: 8

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Sync + packet type

Fig 9A

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FOCOTT "SASSHOOT

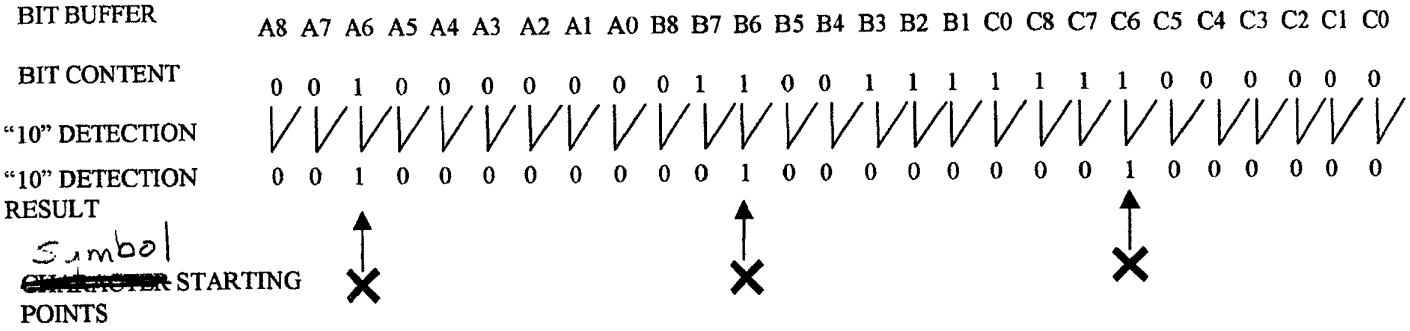


FIG.10

Fig 9B

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TOSOFT 5295+00T

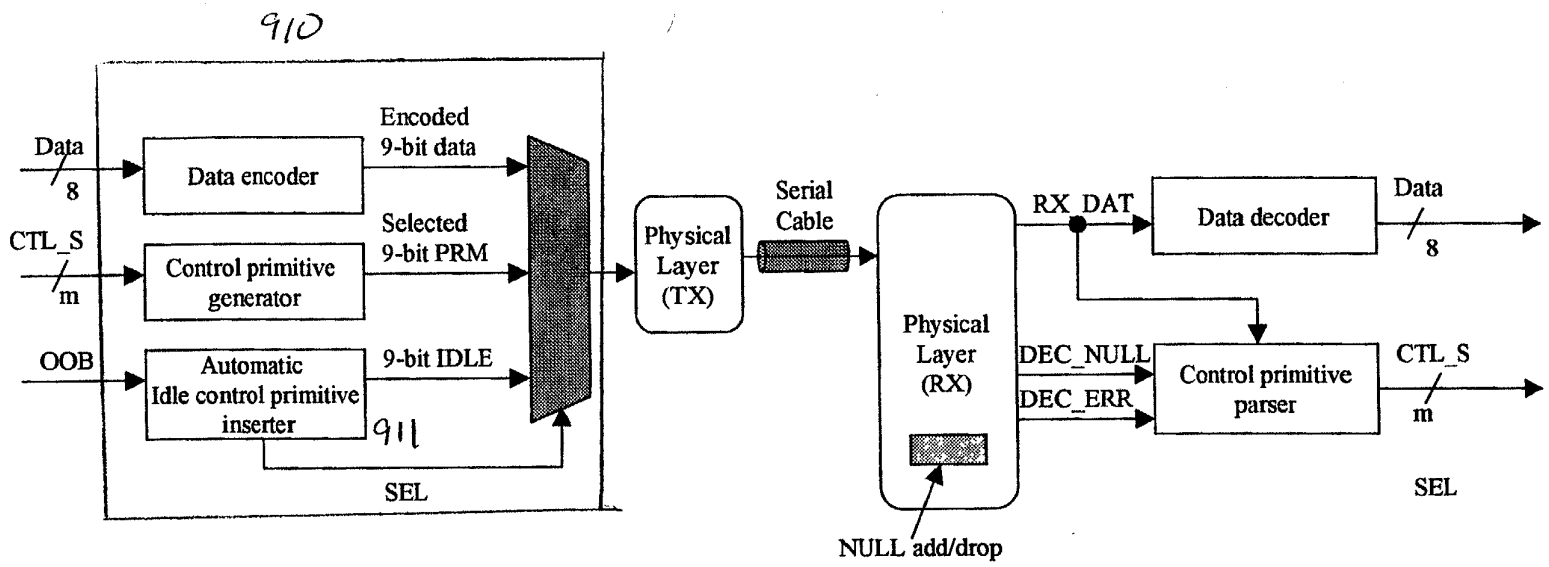


Fig. 9C

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TOZOTT "S295+00T

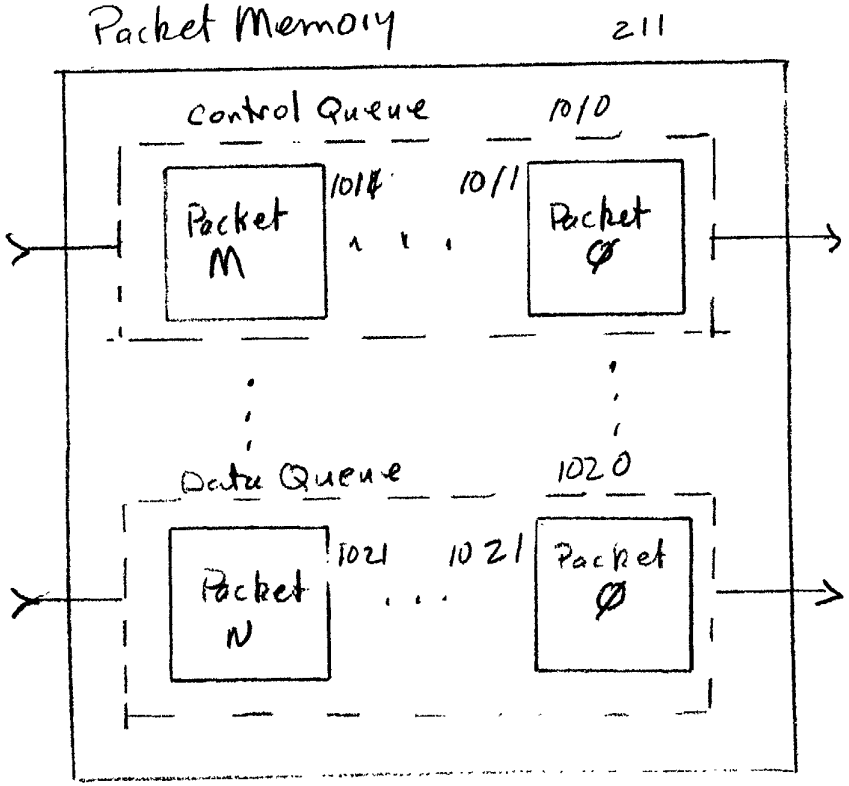


Fig 10

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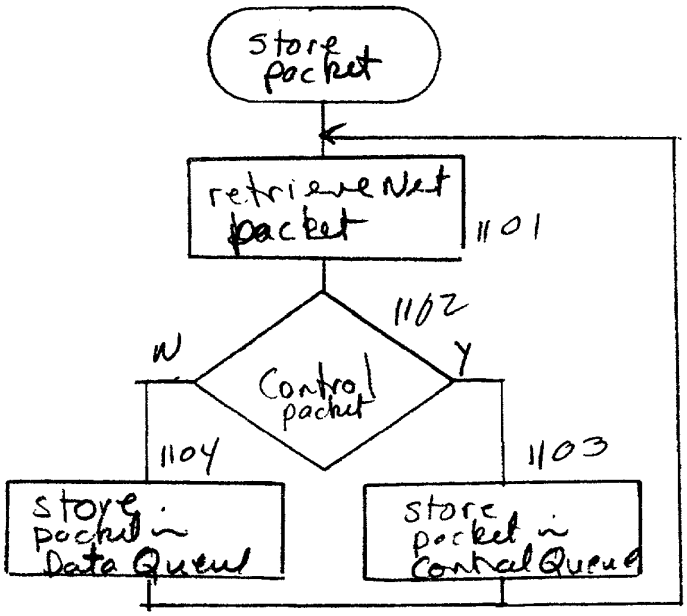

Store packet
retrieve Next packet
1101
1102
N
Y
Control packet
1104
1103
store packet in Data Queue
store packet in Control Queue

Fig 11

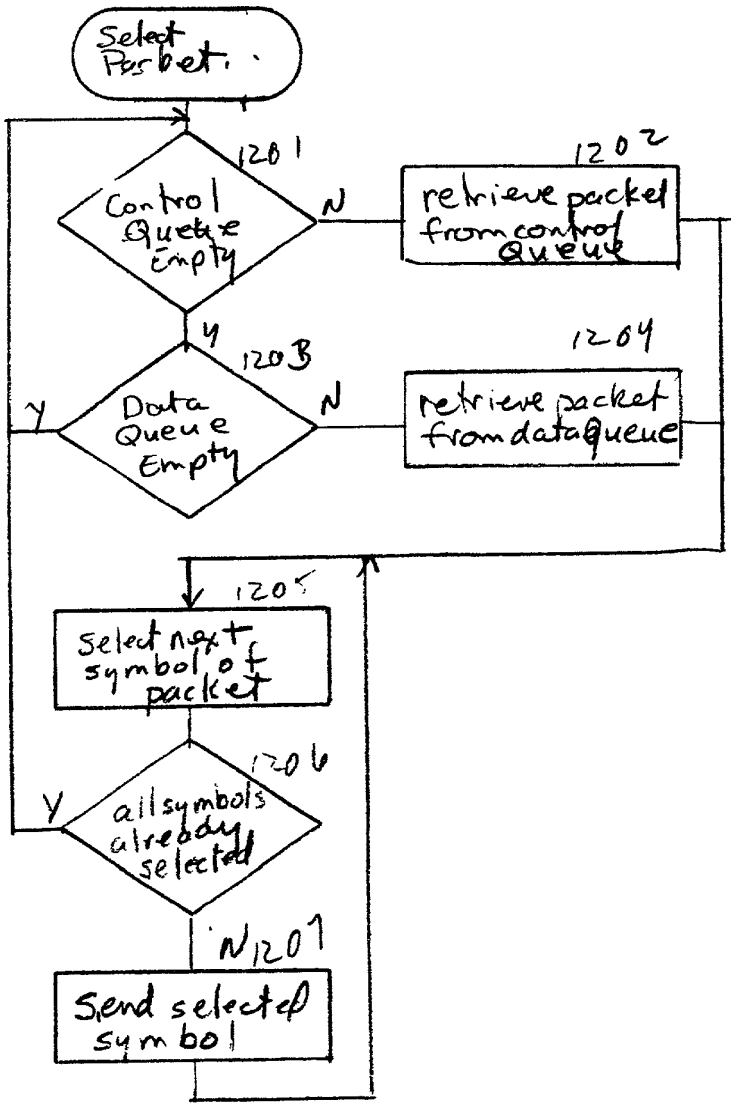

Select Packet
1201
Control Queue Empty
N
1202
retrieve packet from control Queue
Y
1203
Data Queue Empty
Y
N
1204
retrieve packet from data Queue
1205
Select next symbol of packet
1206
all symbols already selected
Y
N
1207
Send selected symbol

Fig 12

TO/OFF "S39S+00T

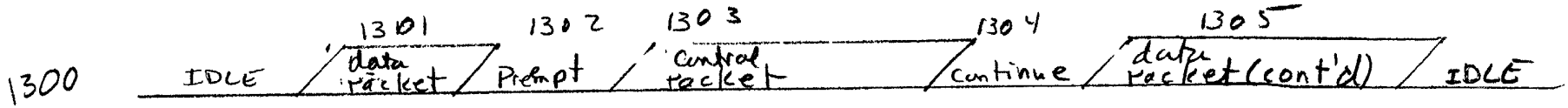


Fig 13

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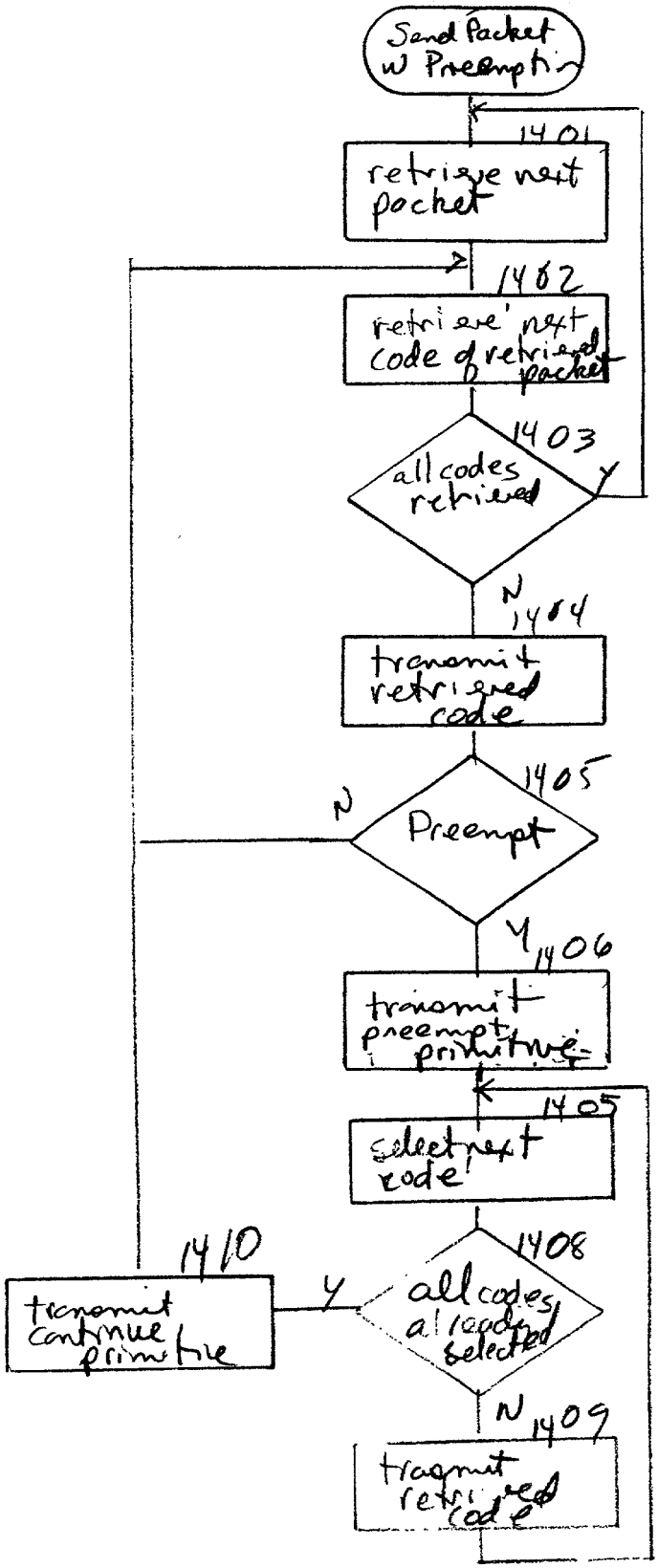


Fig 14

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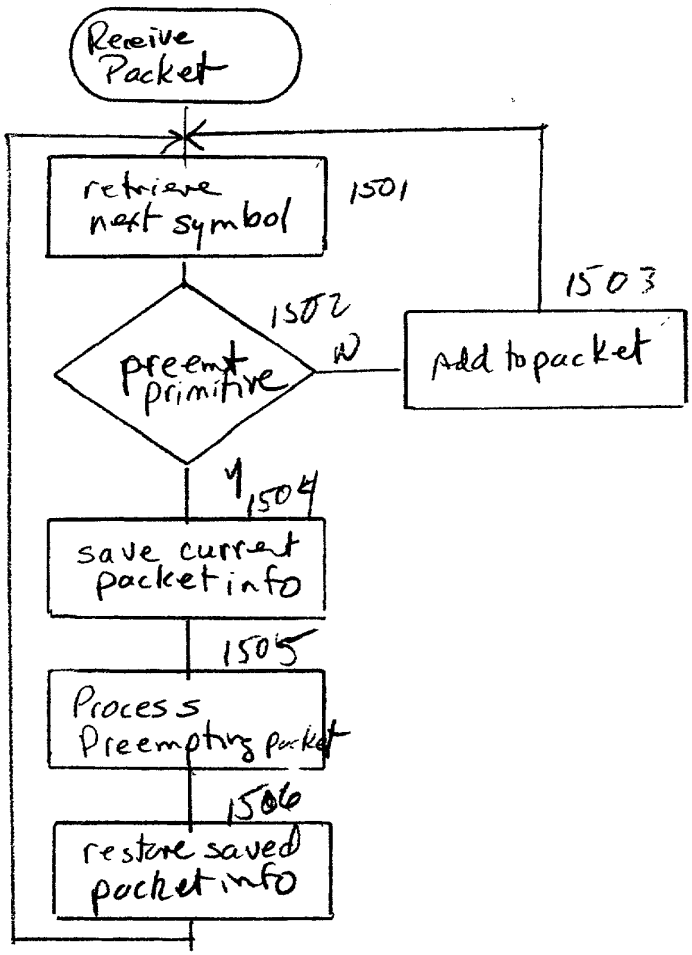


Fig 15

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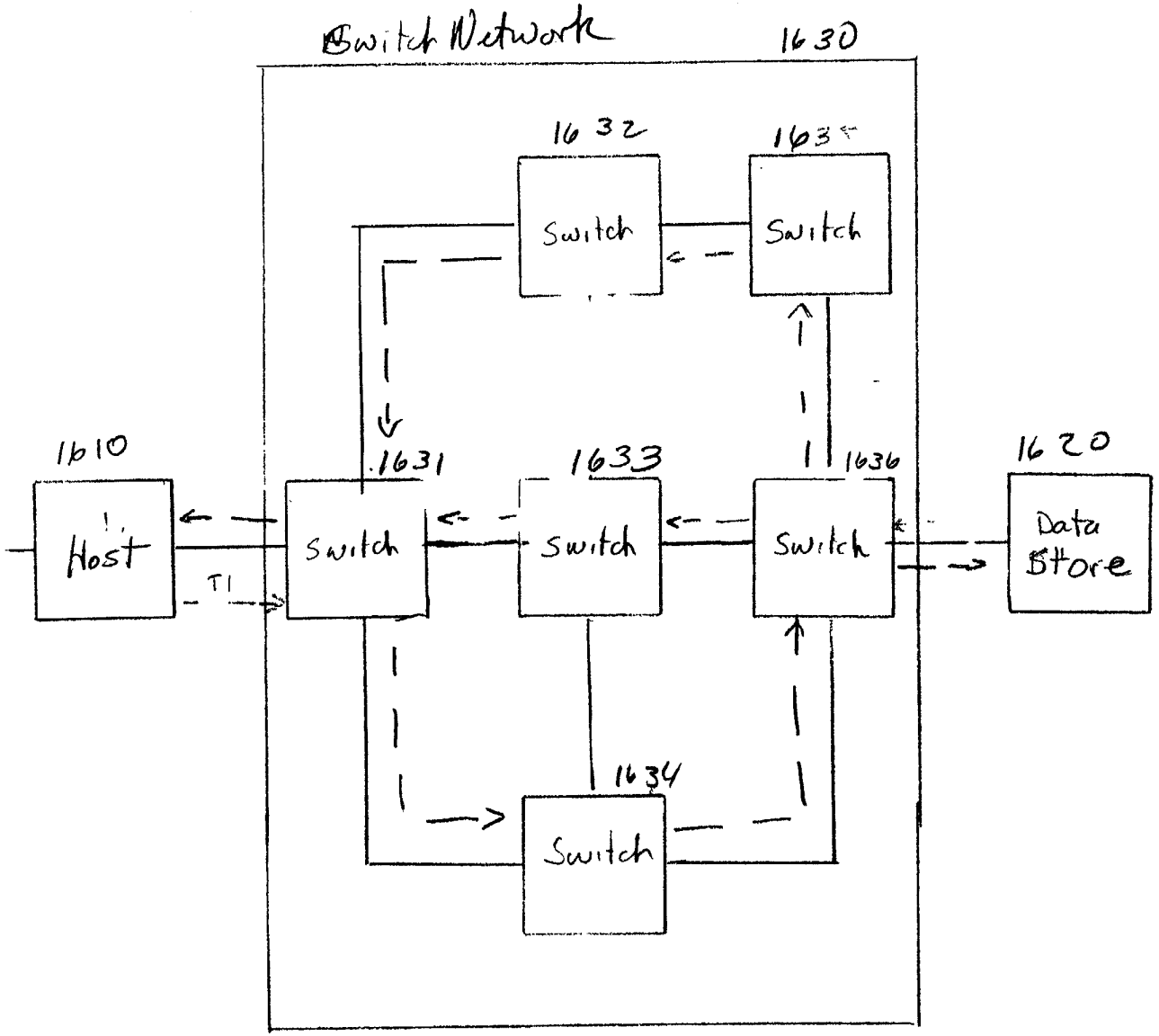


Fig 16

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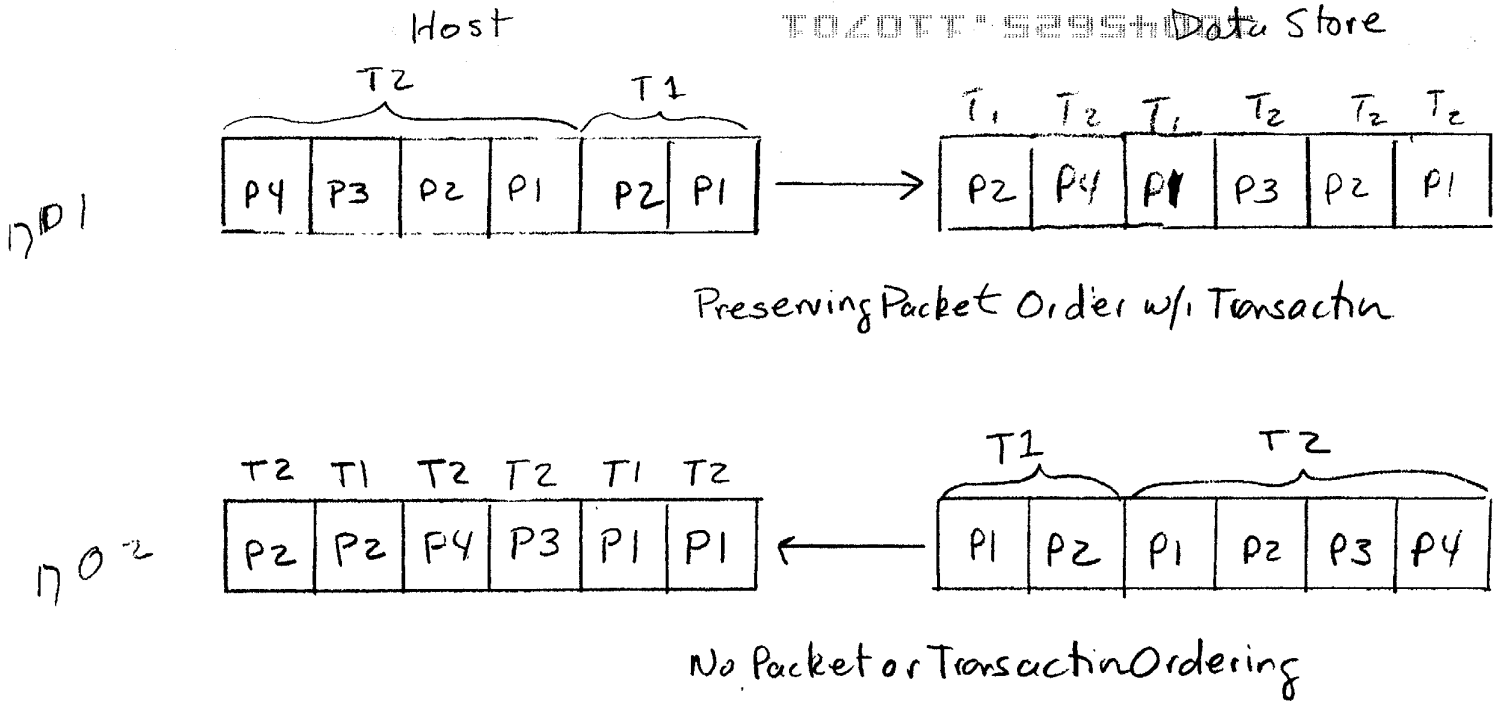


Fig 17

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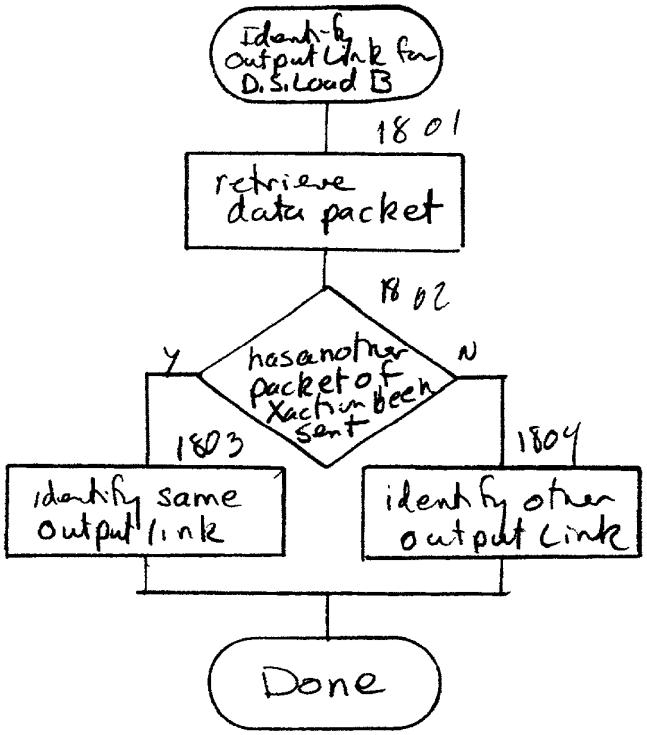


Fig 18

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TOZOTT"S29SMOOT

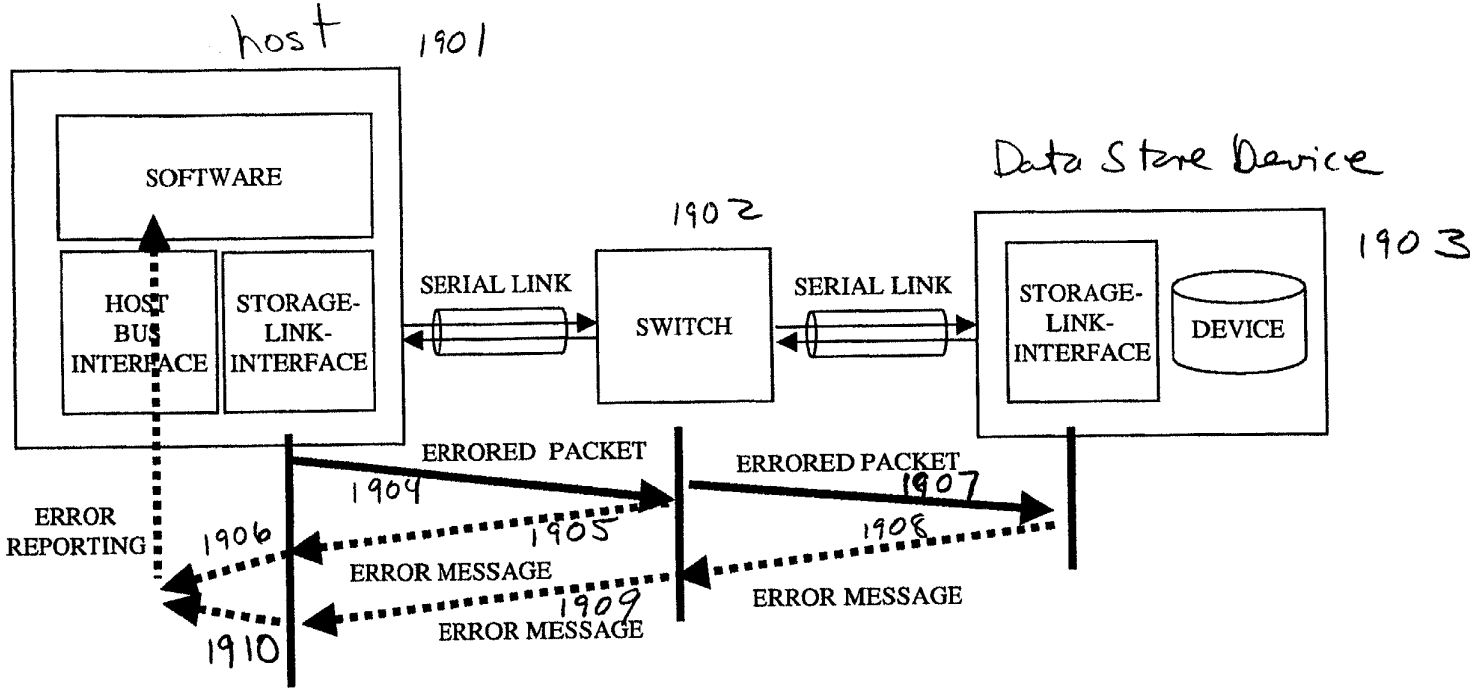


Fig 19A

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T0201T" 9295h001T

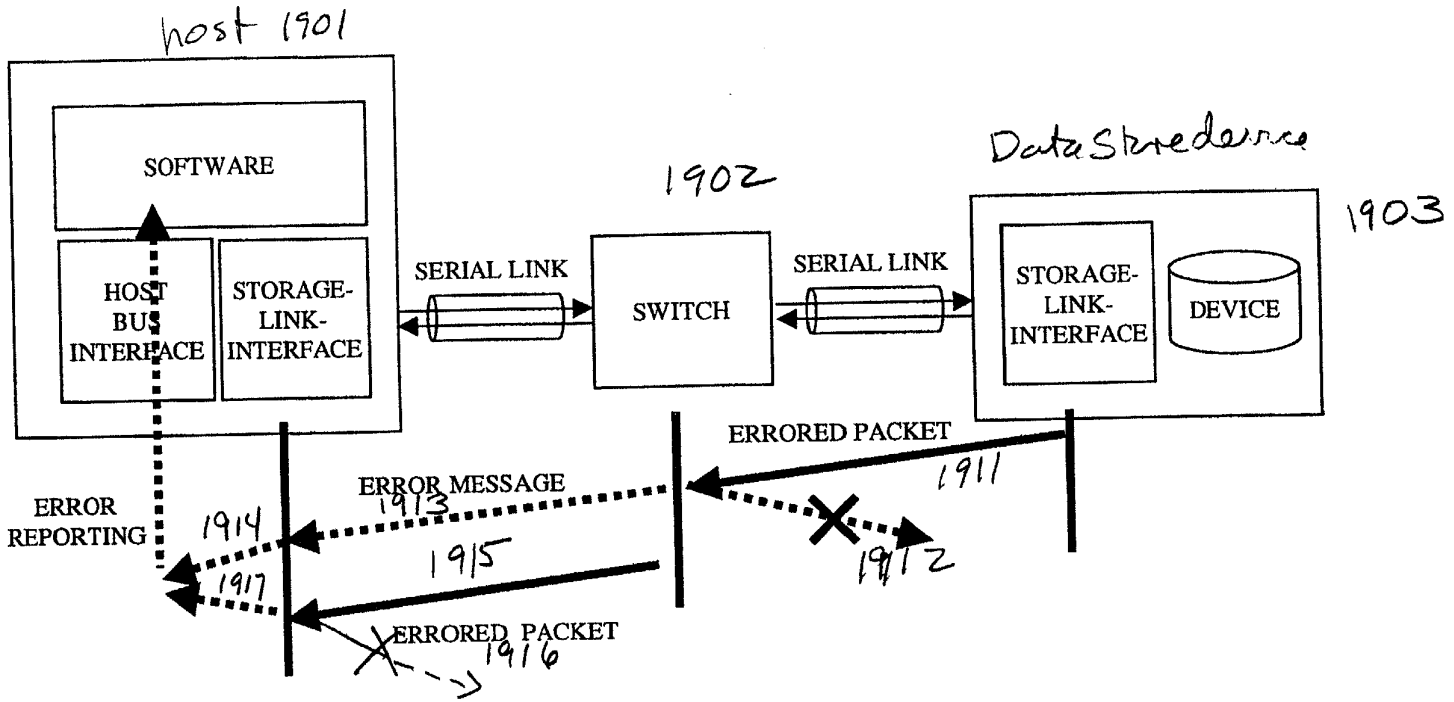
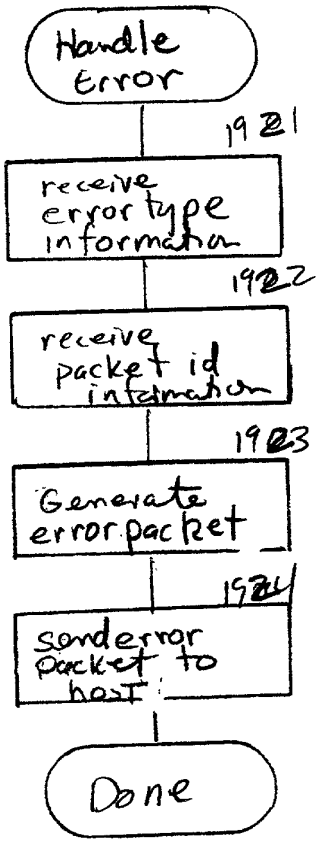


Fig 19B

FIG20

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19C

Document Generated on

TOZOTT"S29S+00T

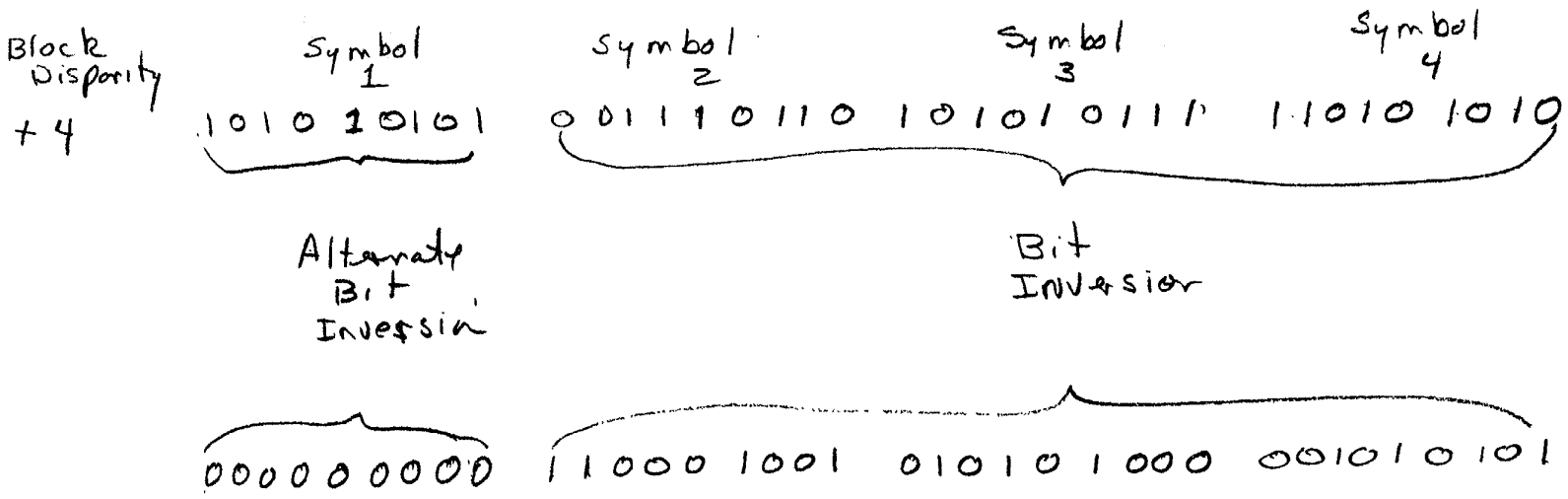


Fig 21A

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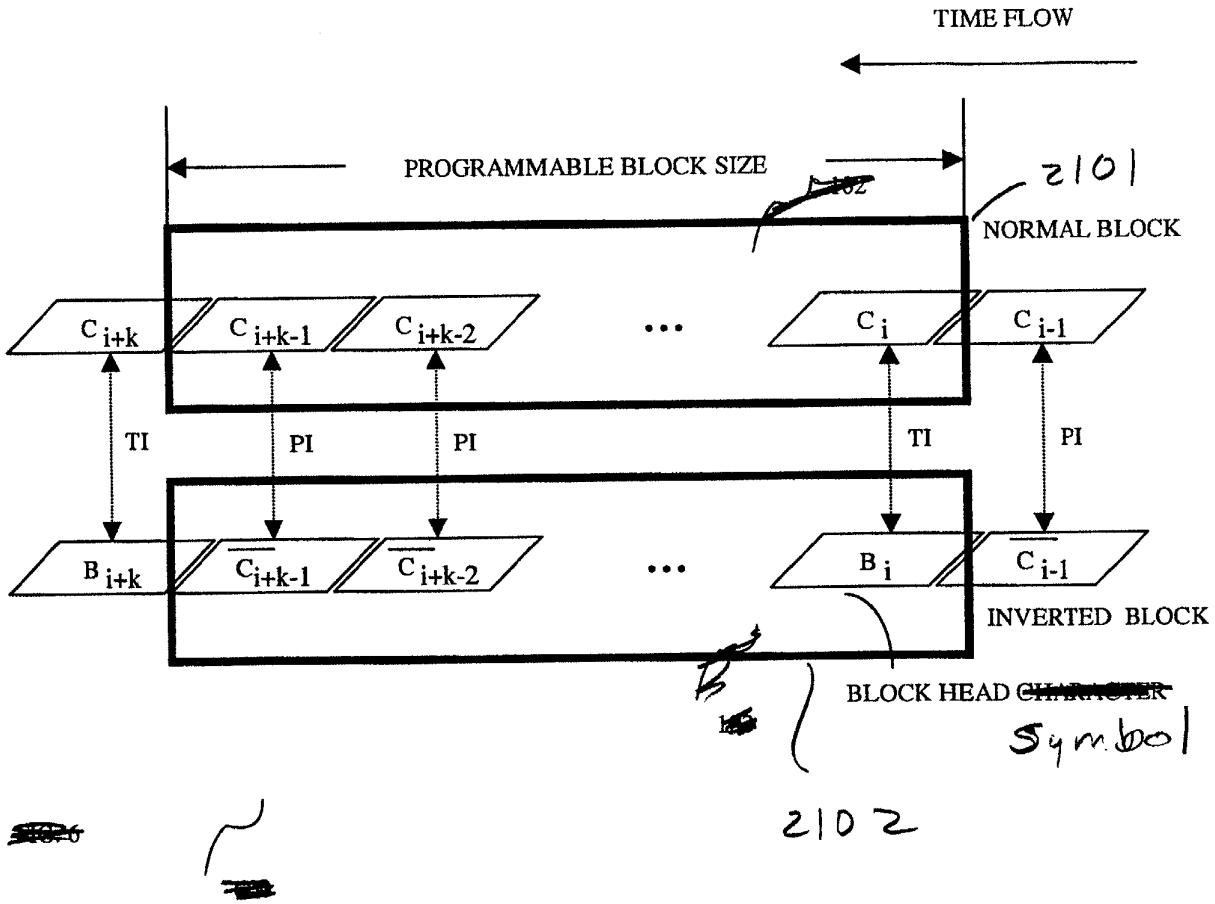


Fig 21B

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TO/OTT "5295+001

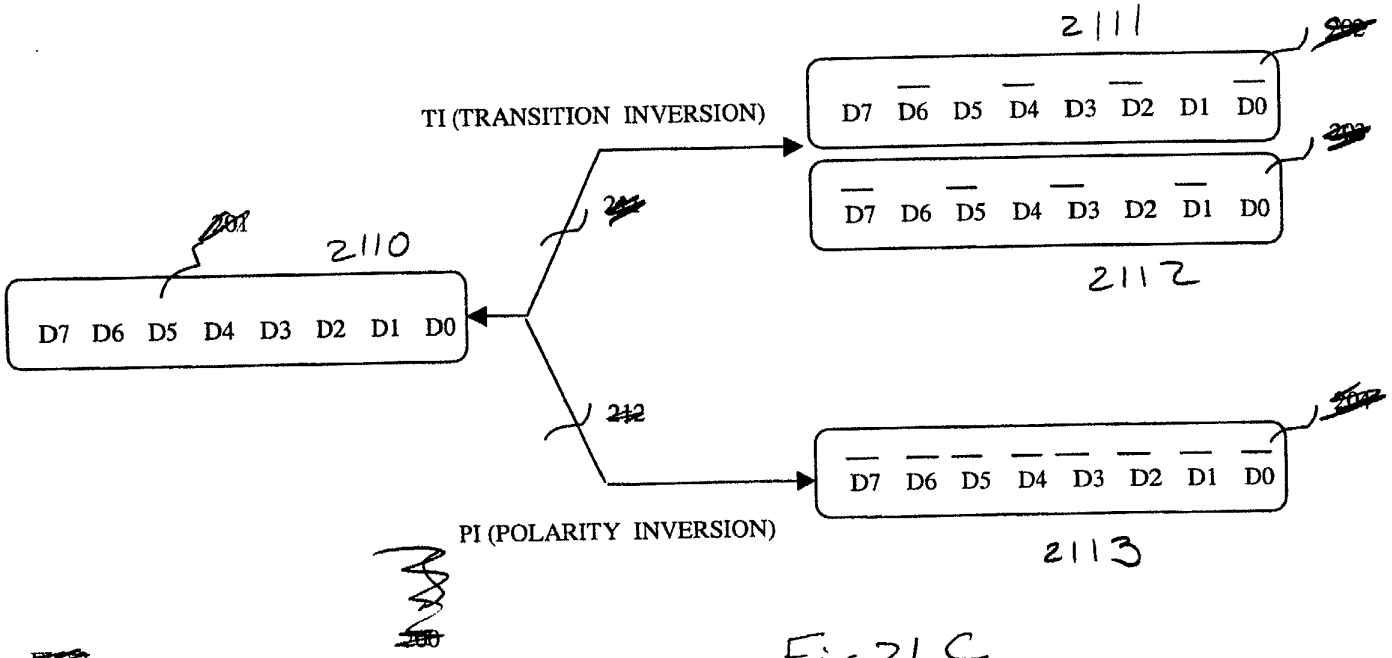


Fig 2

Fig 21 C

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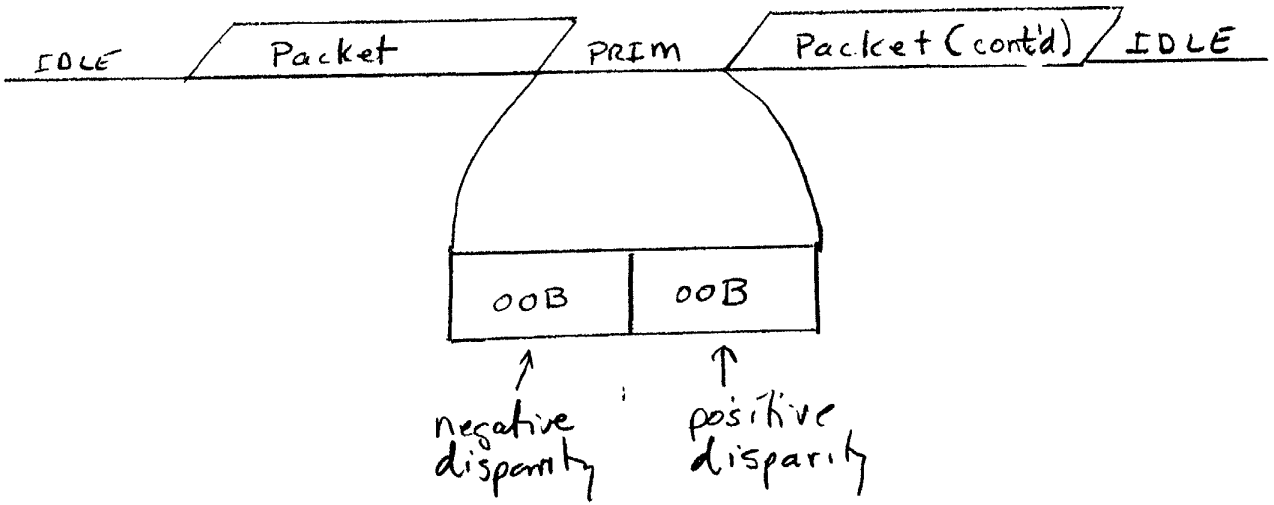


Fig 22

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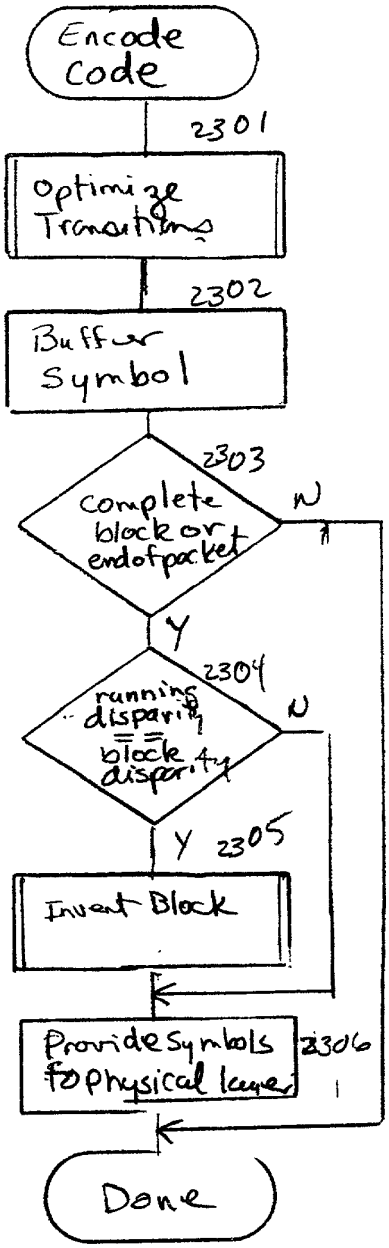


Fig 23

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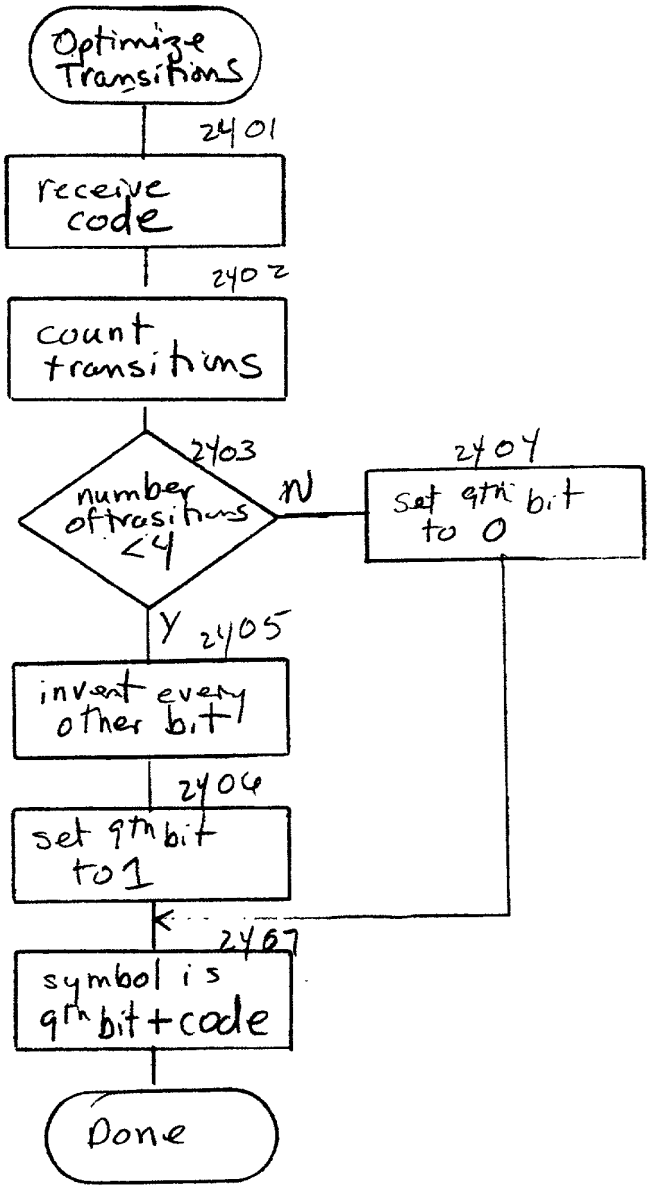


Fig 24

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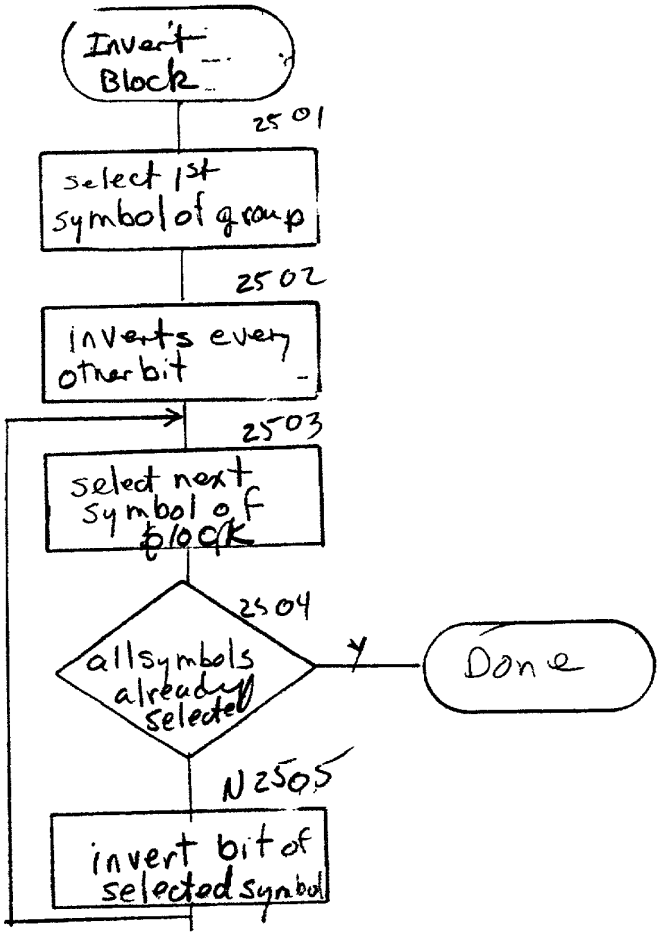


Fig 25

Docket No. FI9-2000-0018US1

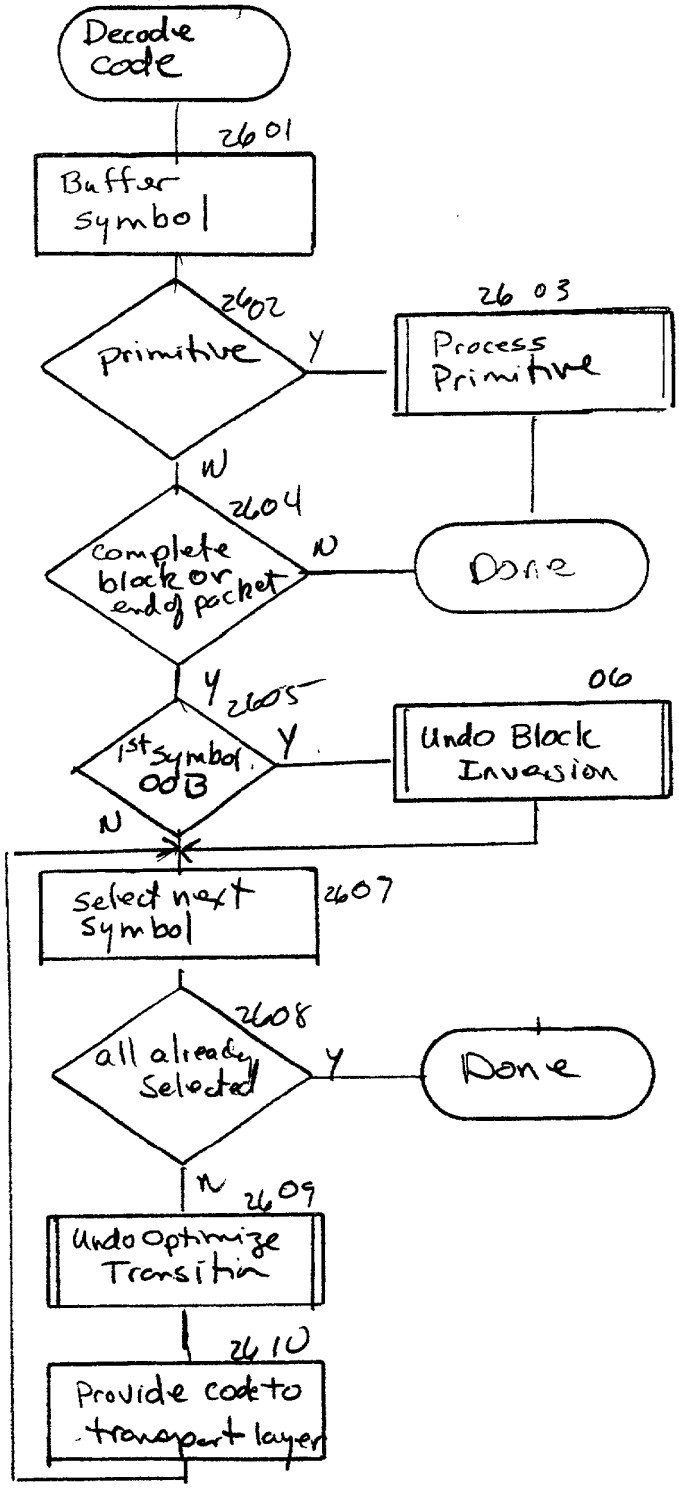


Fig 26

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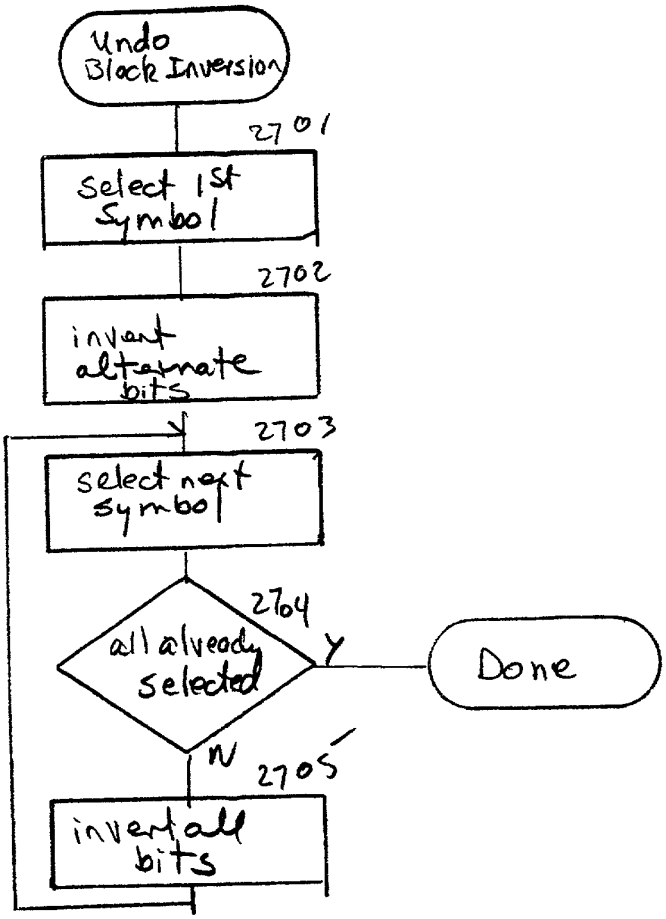


Fig 27

PATENT - 08/08/94

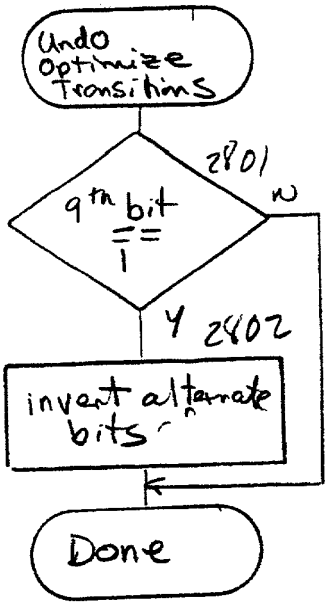


Fig 28

PATENT - 09/675,575 - 2801

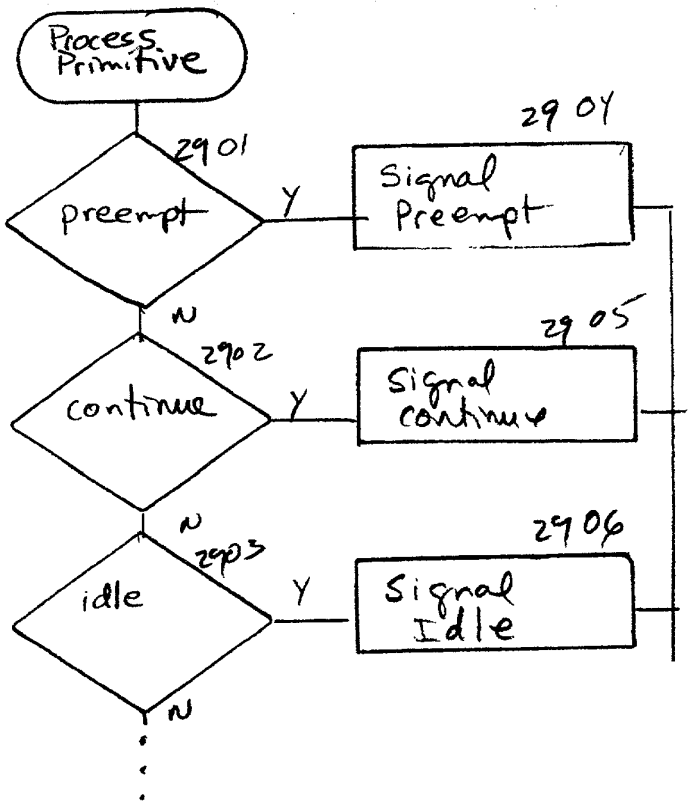


Fig 29

EXHIBIT 1002

TOZOTT "S2995NOOT

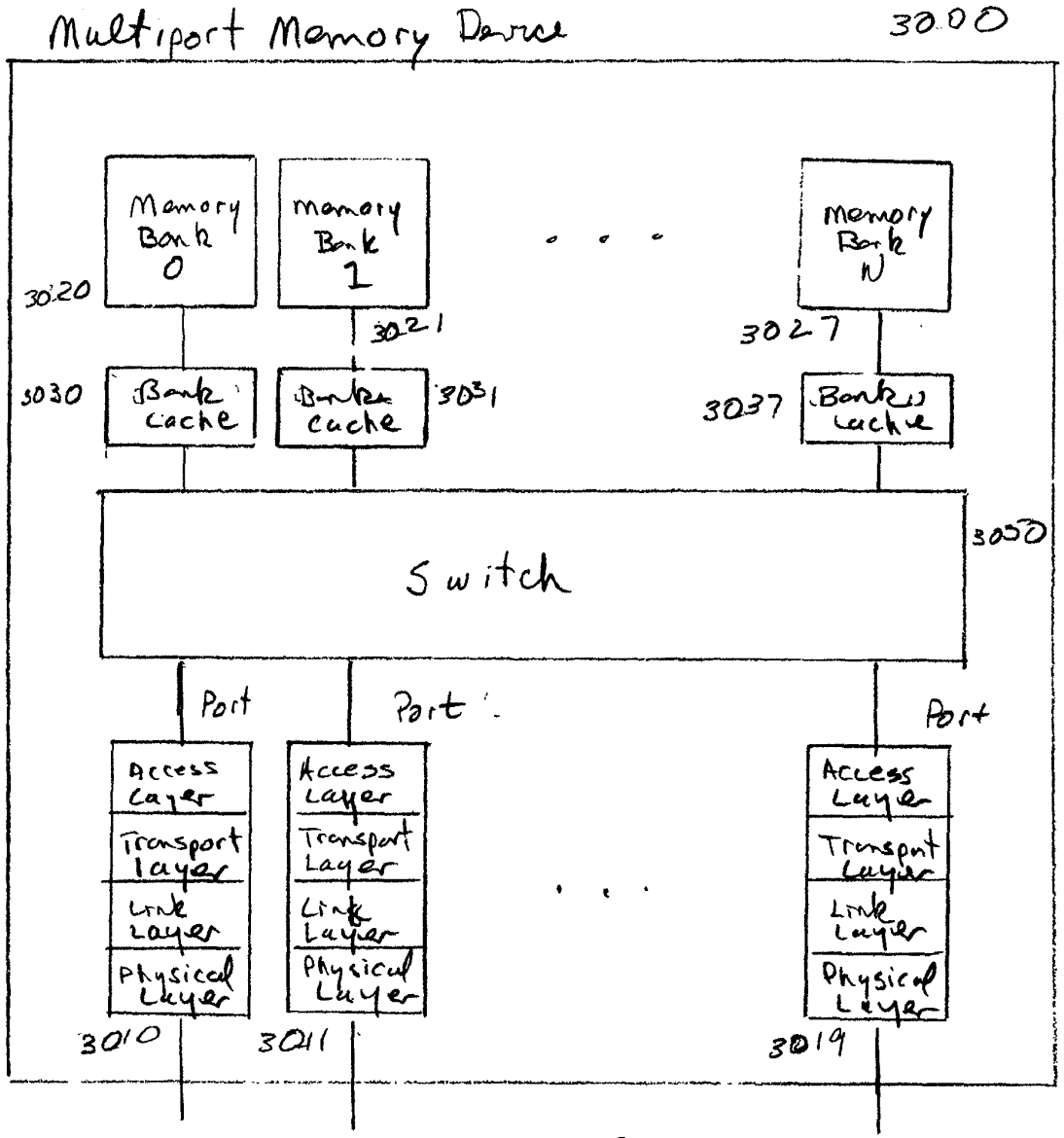


Fig 30

LENOVO EXHIBIT 1002 - 107/553

TO2OTT "S295+DOT

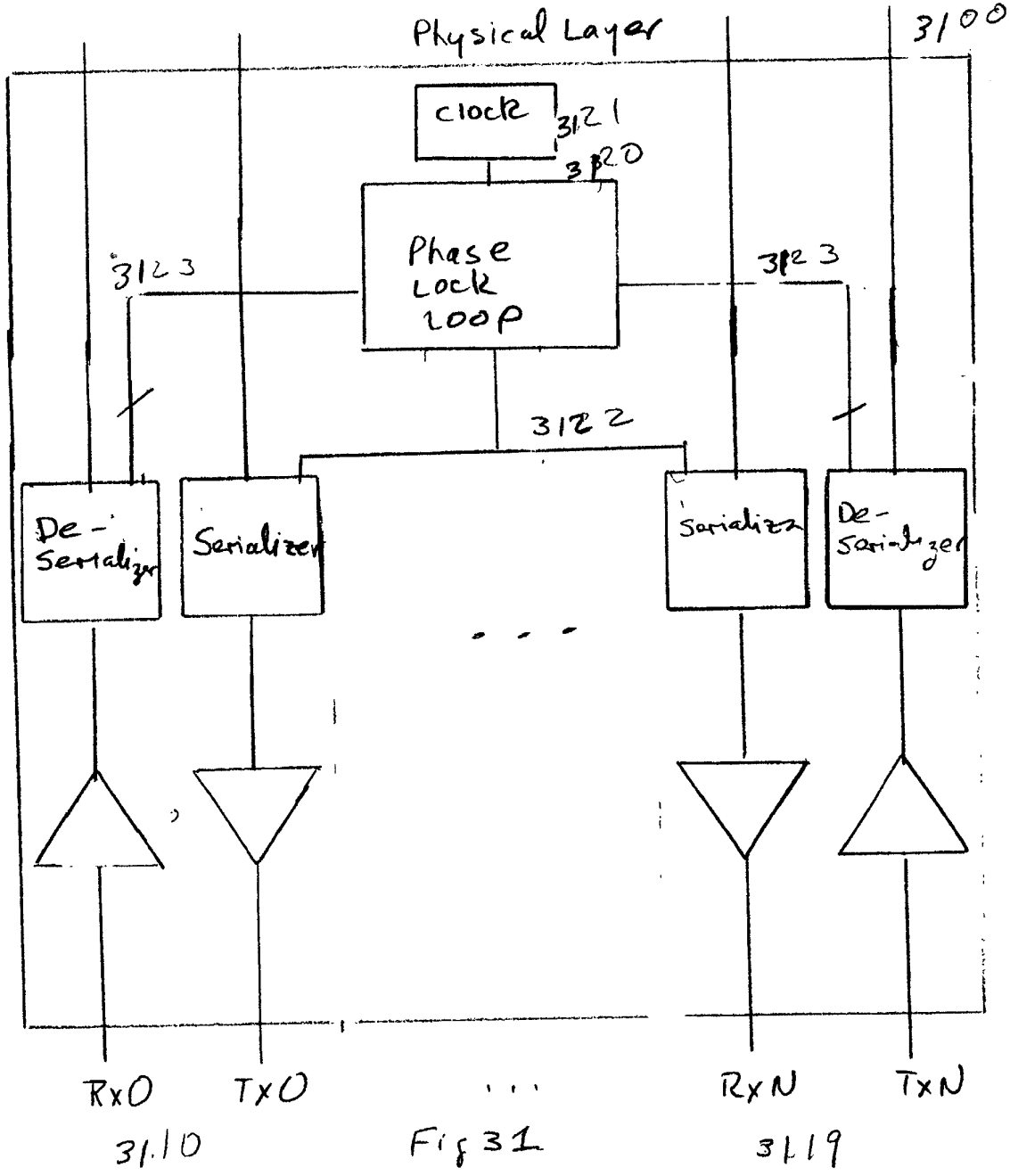


Fig 31

LENOVO EXHIBIT 1002 - 108/553

Input Queue 3201

Port	R/W	Address	Data
3	R	1000	
4	W	4000	10....1
3	W	1000	111...0
3	R	2000	
	⋮		

Output Queue 3202

Valid	Port	Data
1	3	11...0
0		
0		
1	3	101...1
	⋮	

Fig 32

LENOVO EXHIBIT 1002 - 109/553

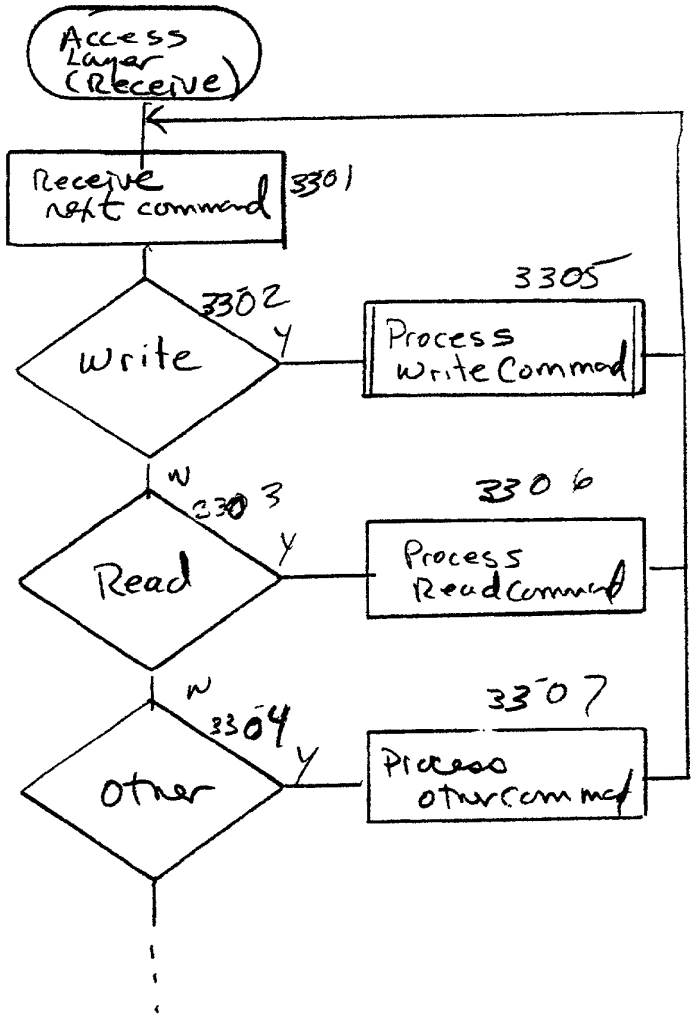


Fig 33

EXHIBIT 1002 - 110/553

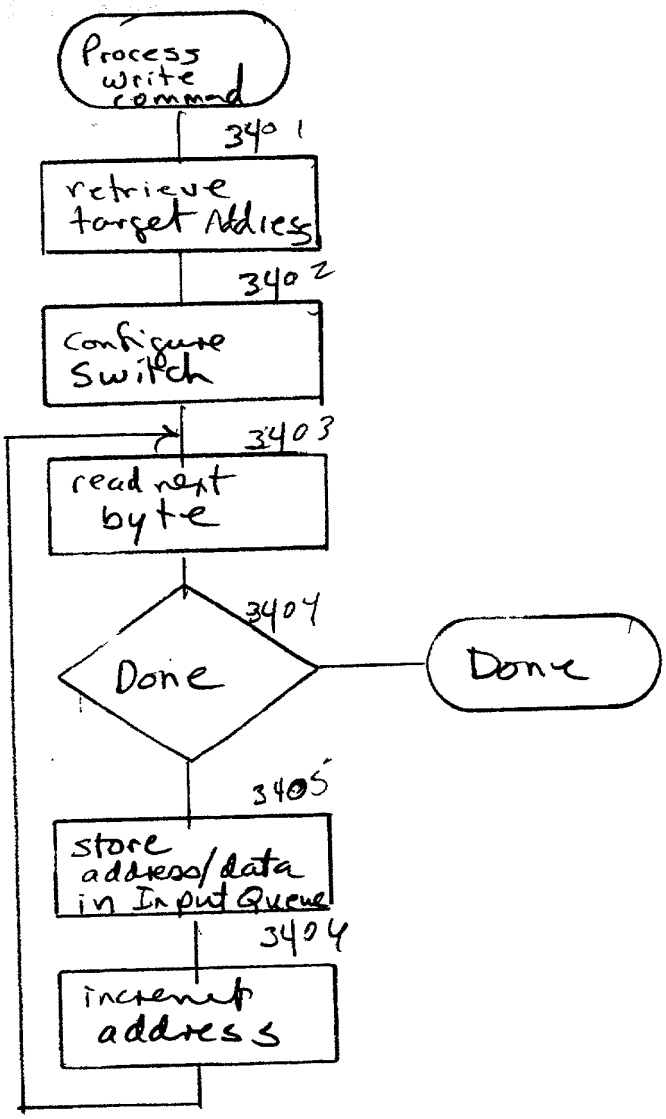


Fig 34

LENOVO EXHIBIT 1002 - 111/553

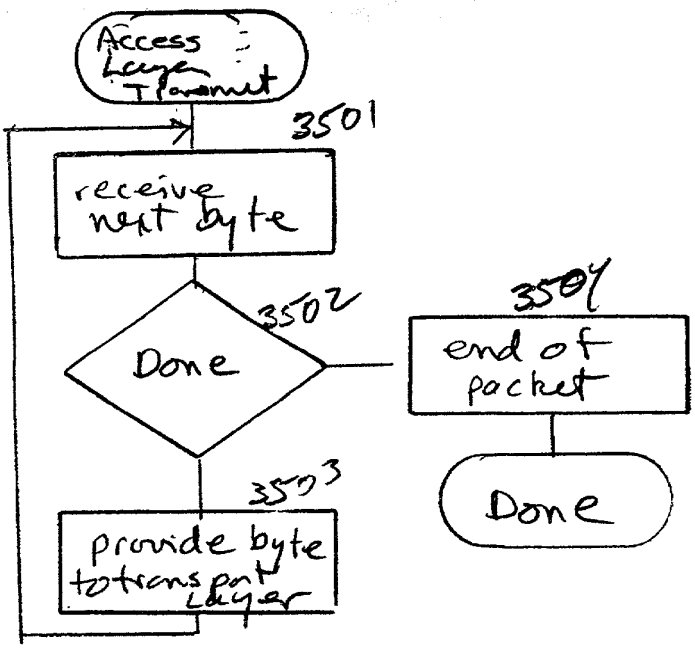

Access Layer Transmit
3501
receive next byte
3502
Done
3504
end of packet
Done
3503
provide byte to transport layer

Fig 35

TOSHIBA 5295H00E

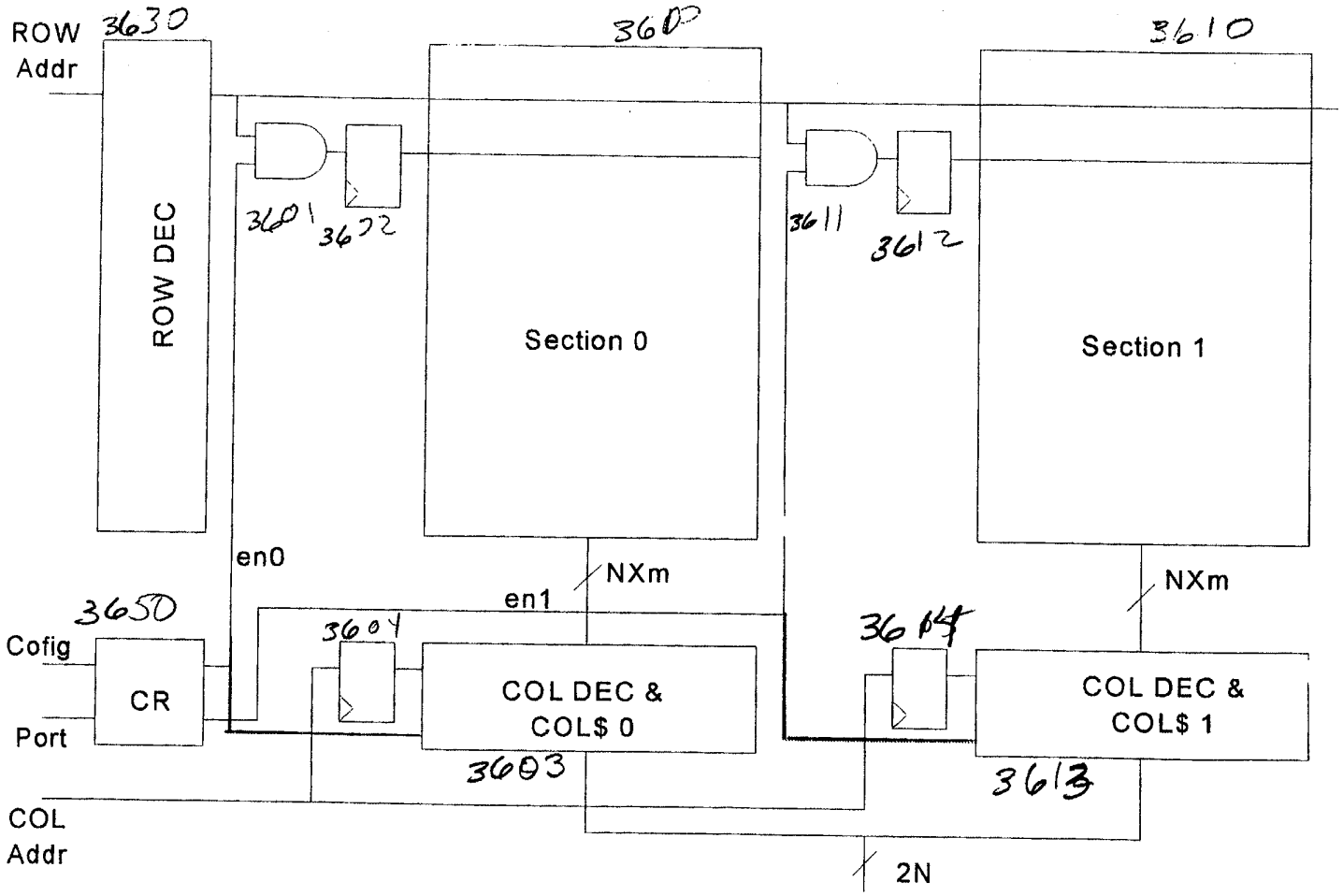
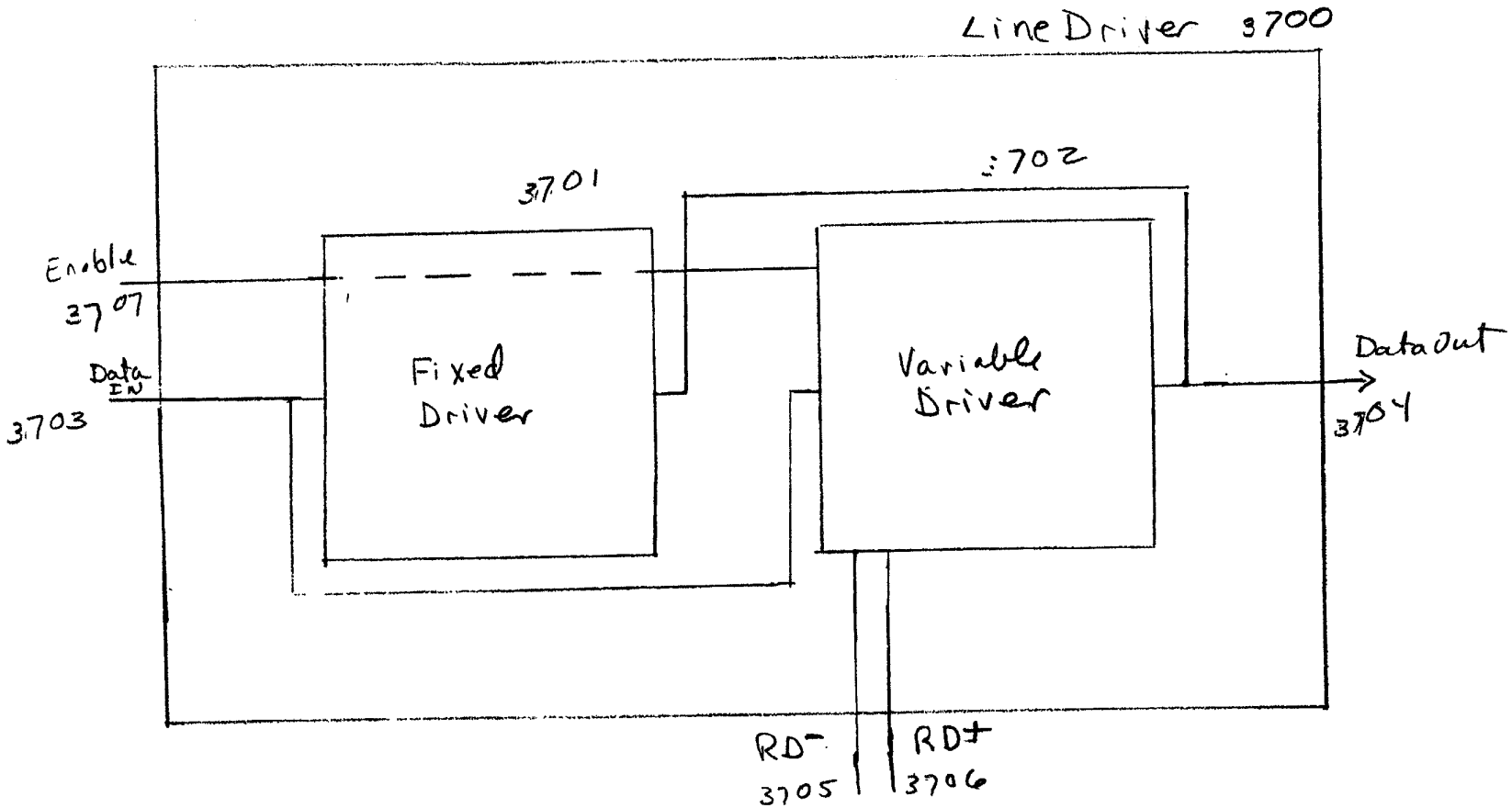


Fig 36

LENOVO EXHIBIT 1002 - 113/553

TOZOTT "S29S40OT



Variable Driver
- $RD^+ \wedge \overline{DataIN}$ = pull down
- $RD^- \wedge DataIN$ = pull up

Fig 37A

LENOVO EXHIBIT 1002 - 114/553

T0207T" 5295+00T

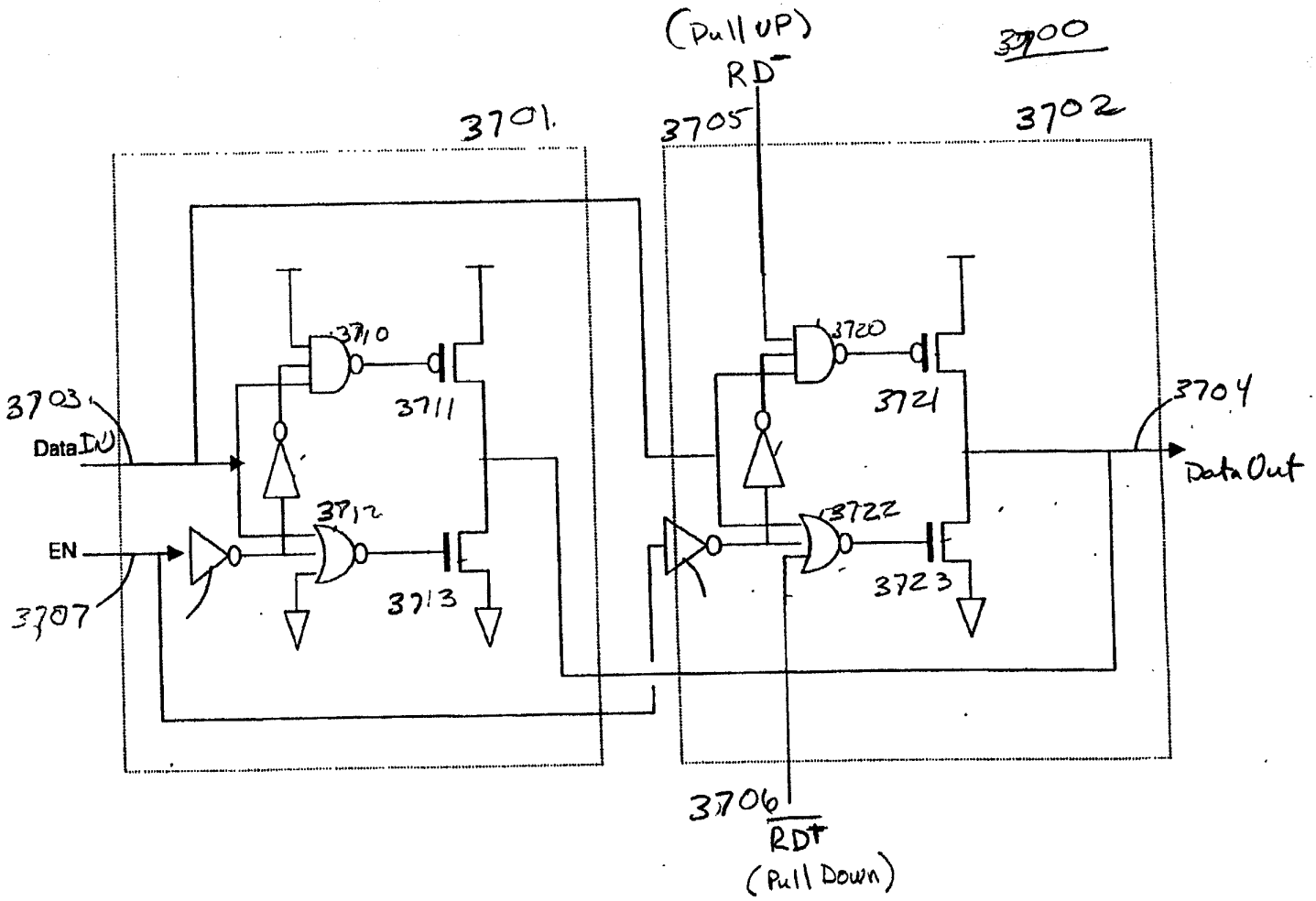


Fig 37B

LENOVO EXHIBIT 1002 - 115/553

TOSOFT 5295H00T

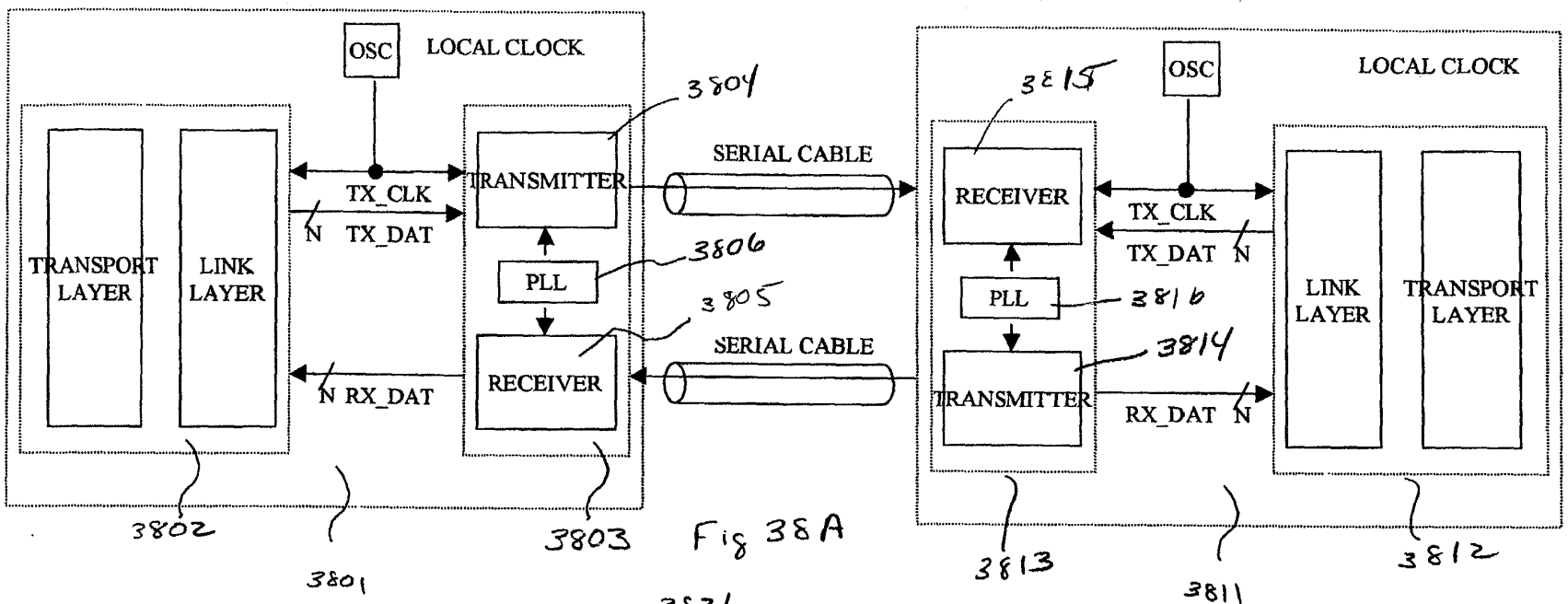


Fig 38A

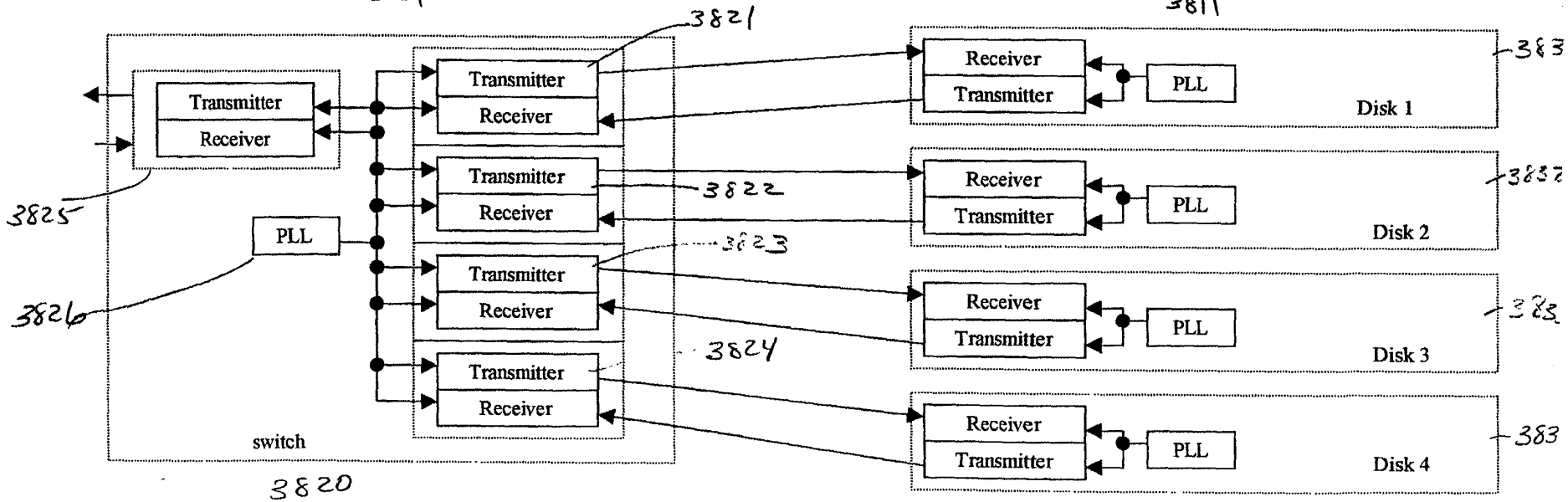


Fig 38B

LENOVO EXHIBIT 1002 - 116/553

TOZOTT 5295h00t

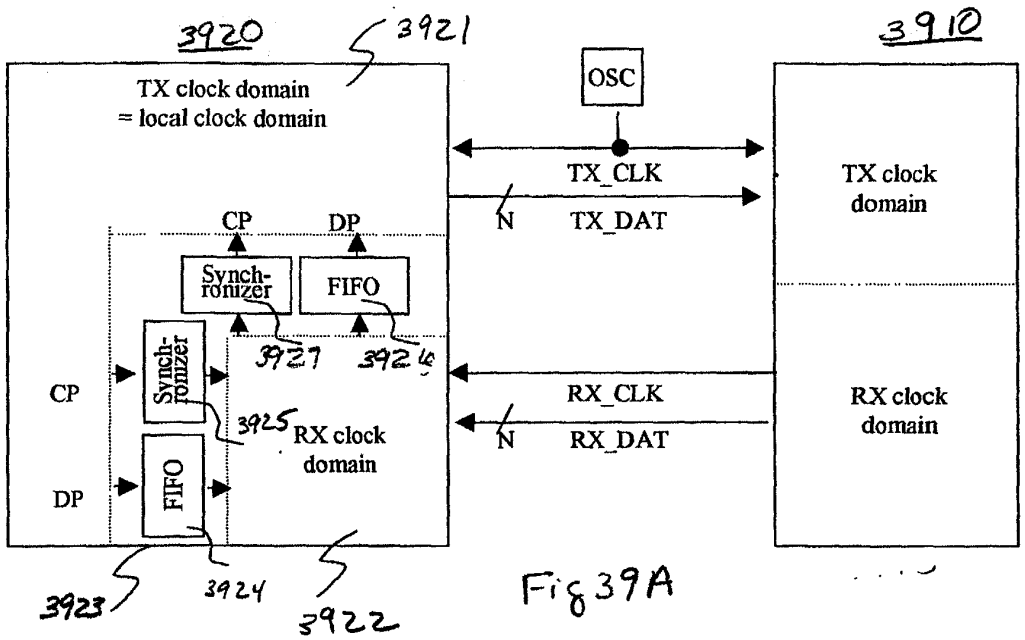


Fig 39A

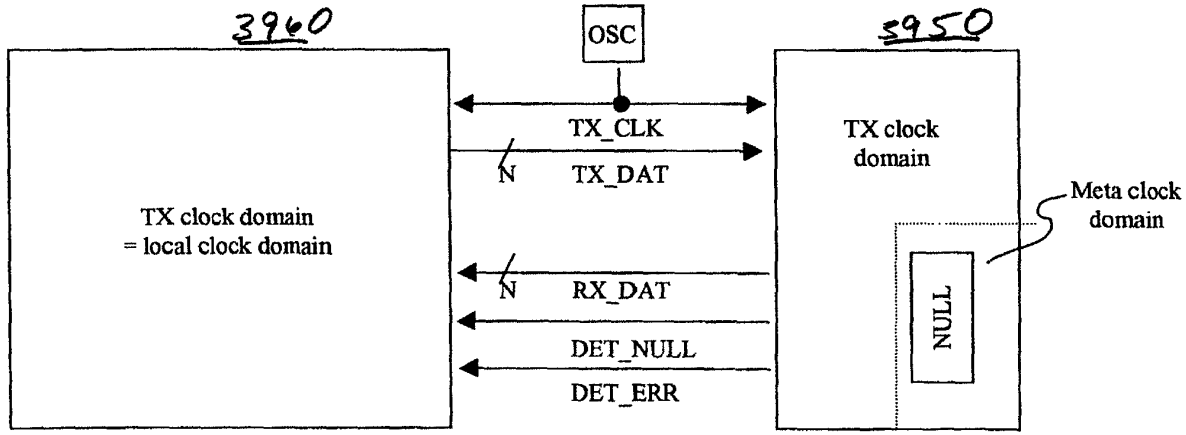


Fig 39B

LENOVO EXHIBIT 1002 - 117/553

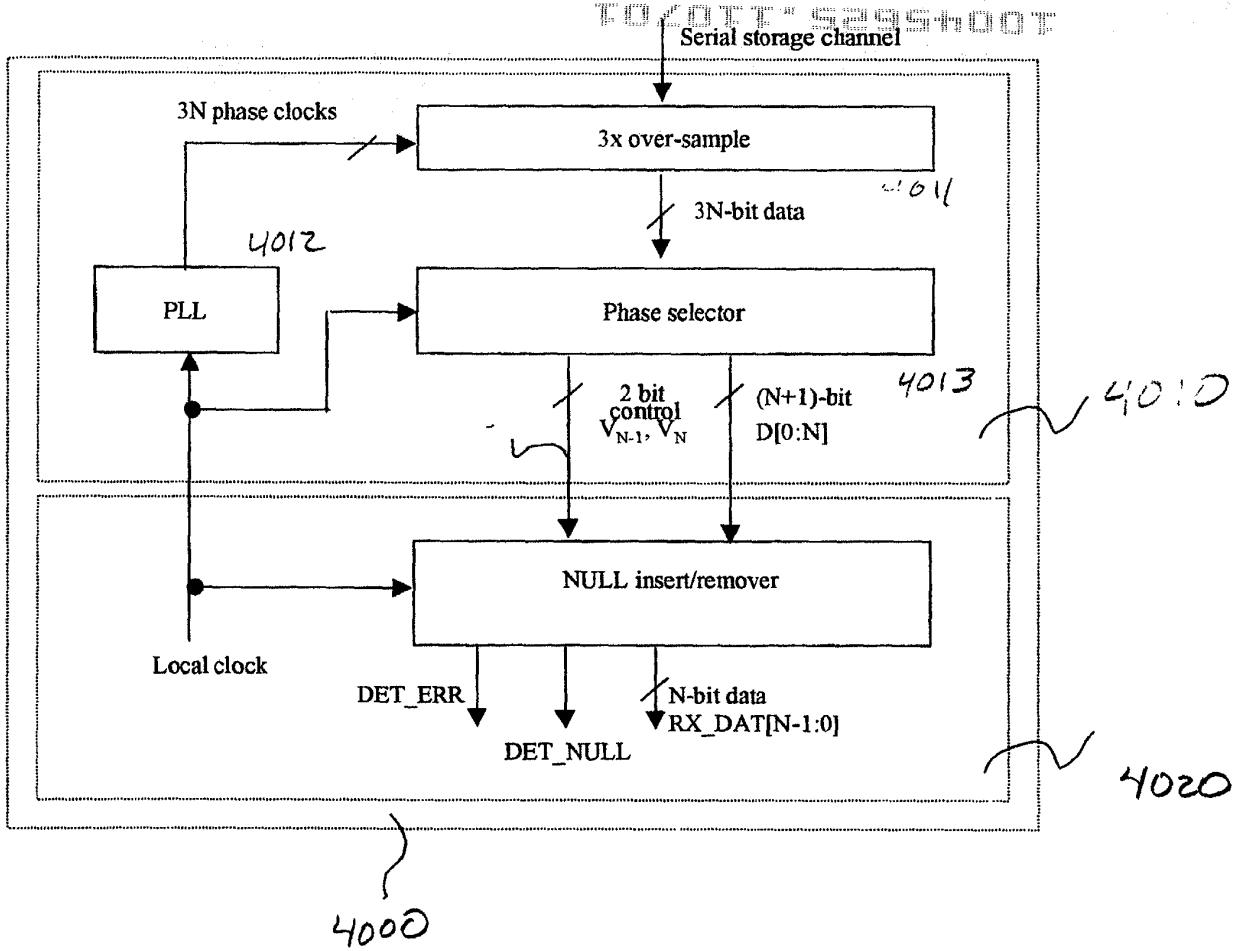


Fig 4D

LENOVO EXHIBIT 1002 - 118/553

TOSCOTT's 529shoot

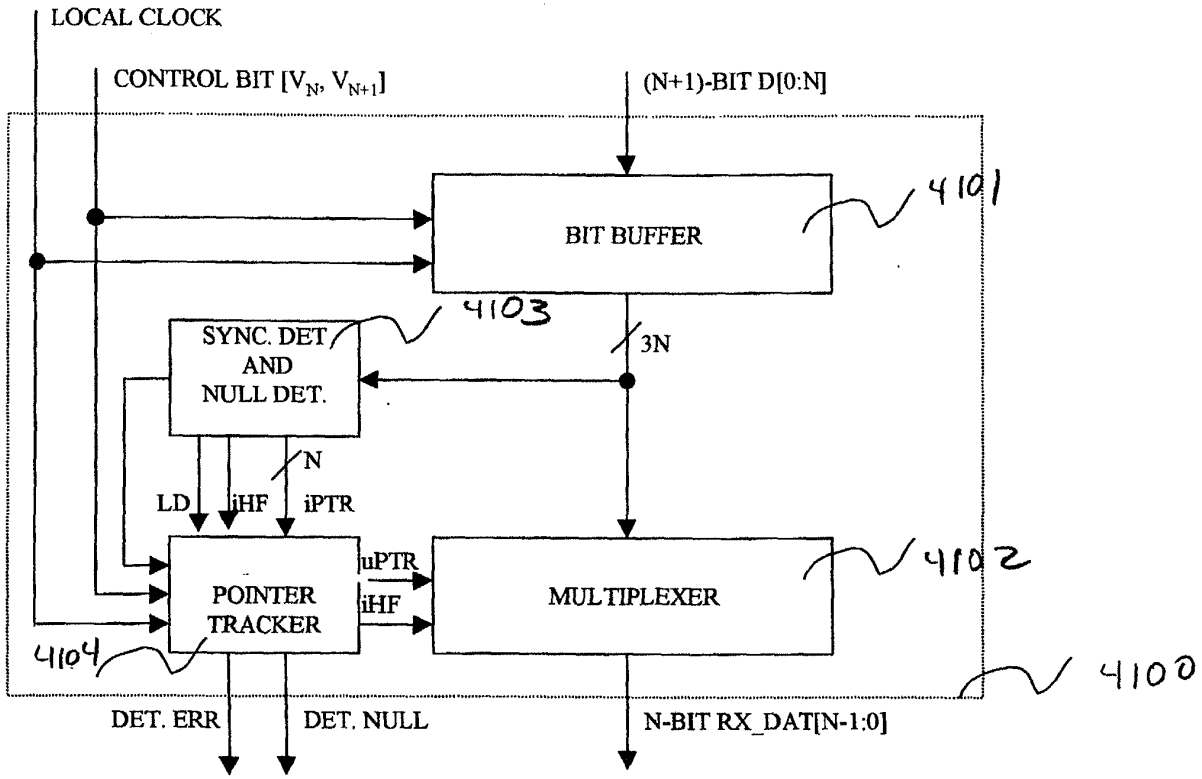


Fig 41

LENOVO EXHIBIT 1002 - 119/553

TOZOTT "S29S4hOOE

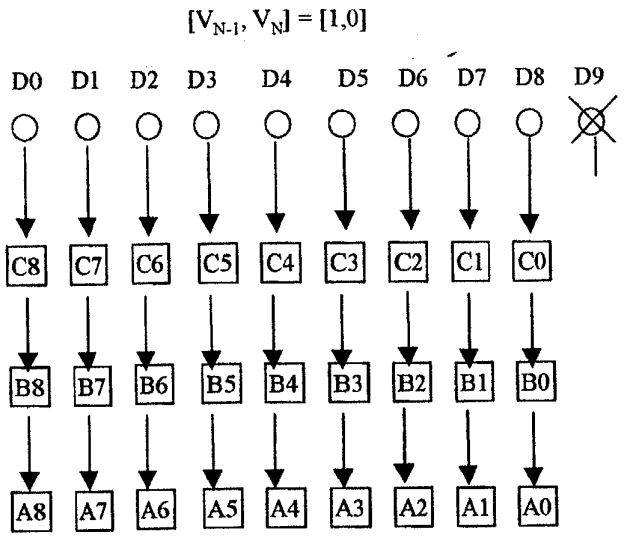


Fig 42A

LENOVO EXHIBIT 1002 - 120/553

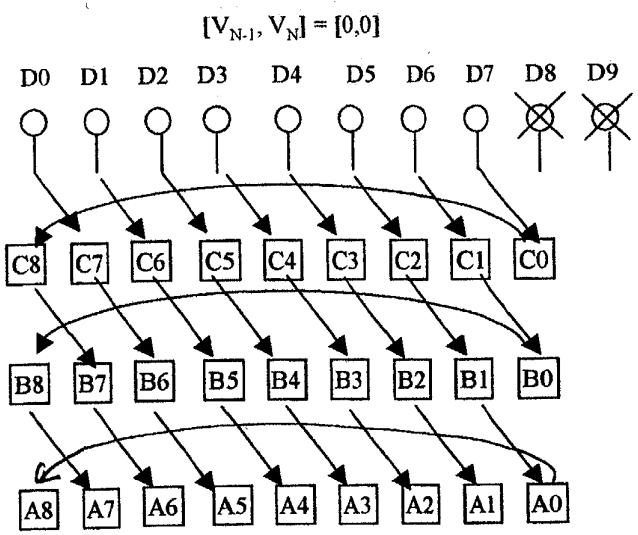


Fig 42B

LENOVO EXHIBIT 1002 - 121/553

TOZOTT "SZ9SHDOT

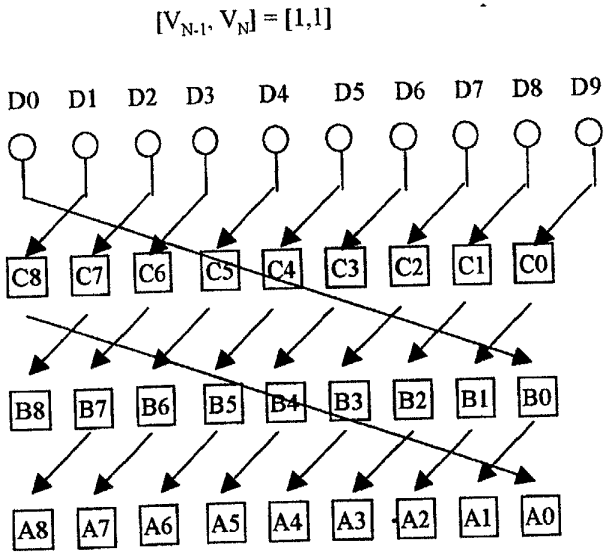


Fig 42C

LENOVO EXHIBIT 1002 - 122/553

Document Screenshot

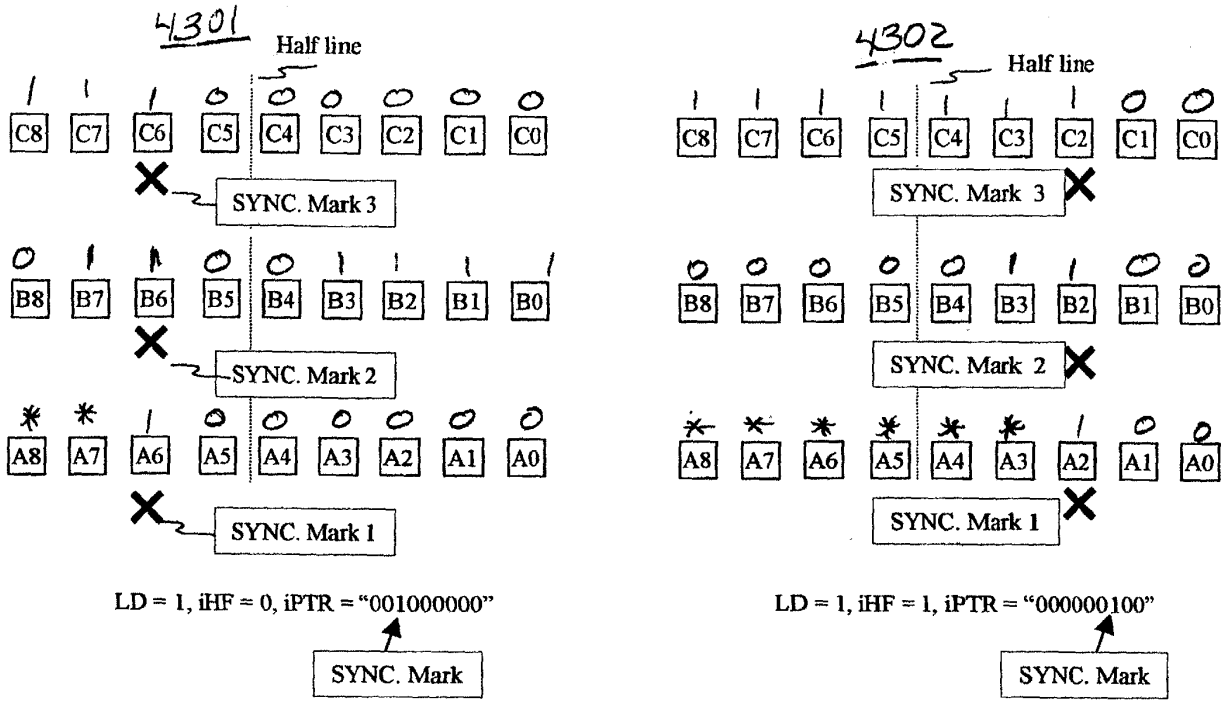
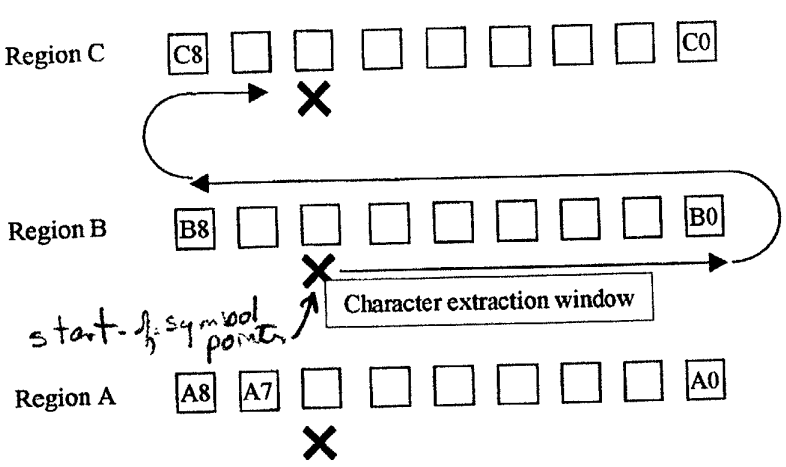


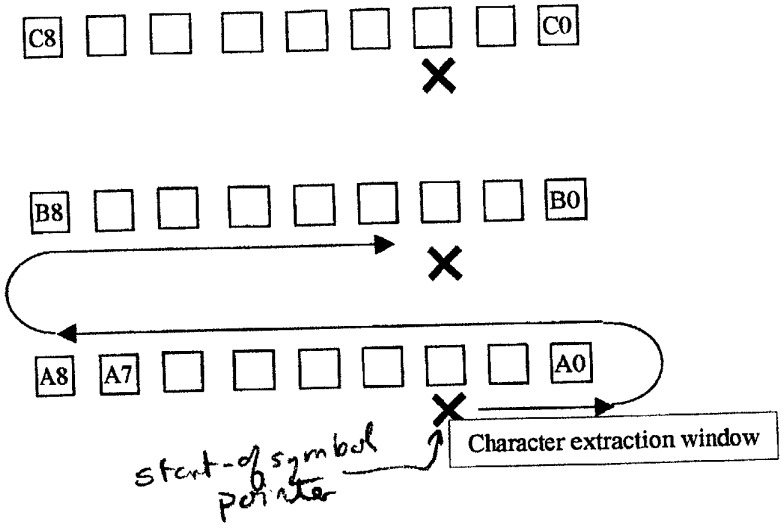
Fig. 43

LENOVO EXHIBIT 1002 - 123/553

TOSOFT "S2956001"



LD = 1, iHF = 0, iPTR = "001000000"



LD = 1, iHF = 1, iPTR = "000000100"

Fig 44

LENOVO EXHIBIT 1002 - 124/553

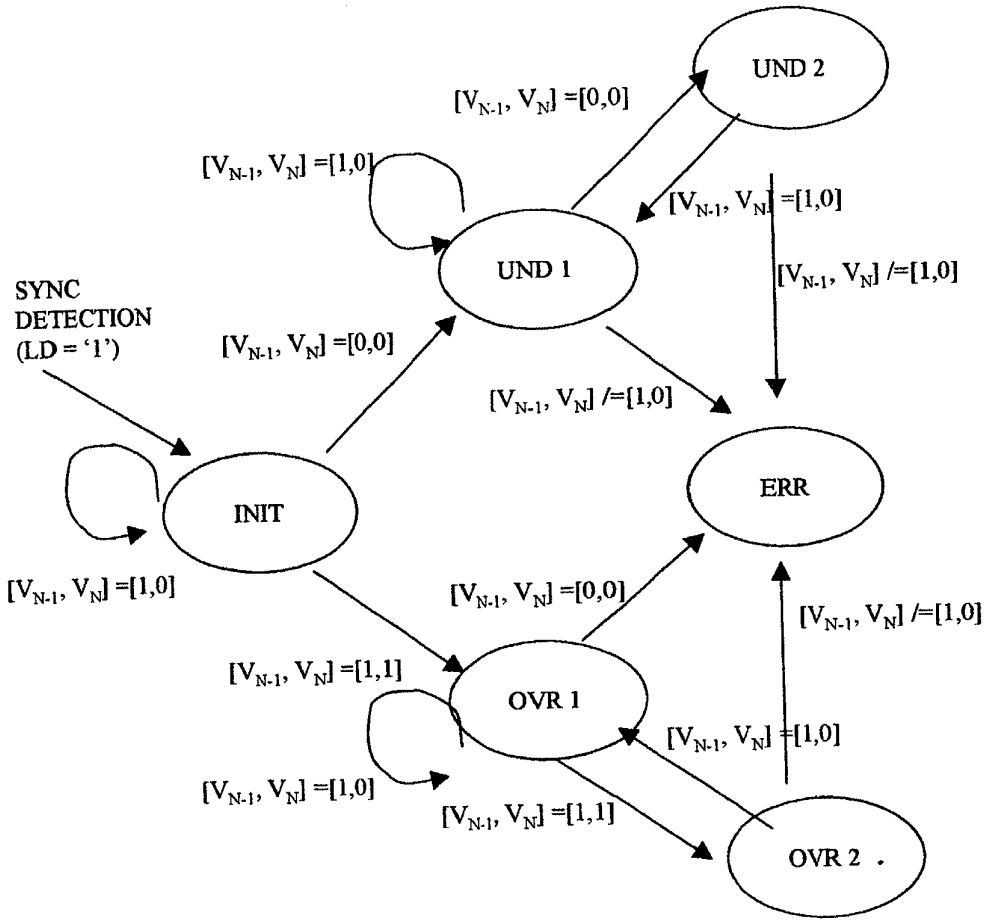


Fig 45

LENOVO EXHIBIT 1002 - 125/553

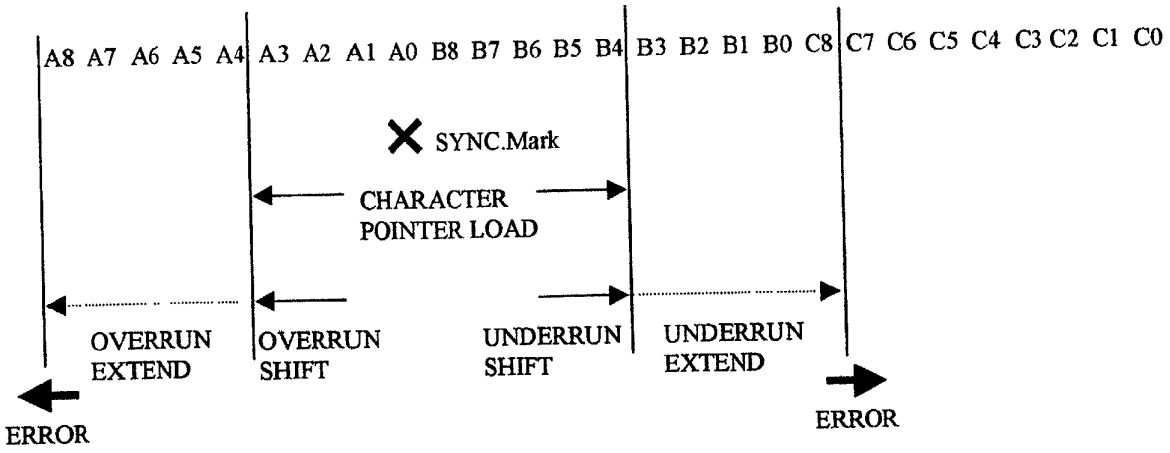


Fig 46

LENOVO EXHIBIT 1002 - 126/553

TOSHIBA Corporation

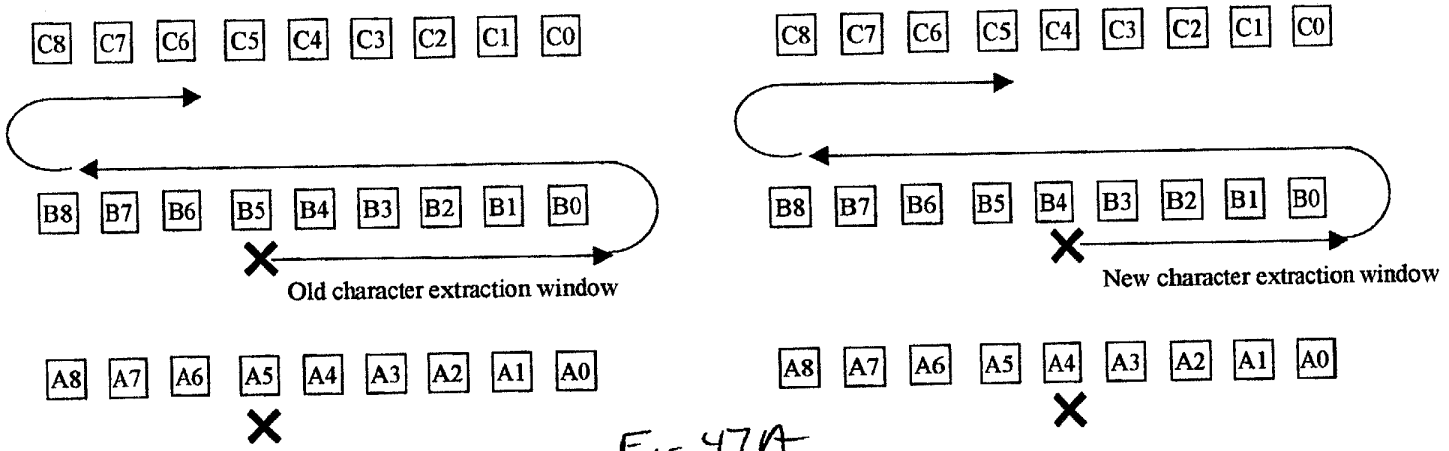


Fig 47A

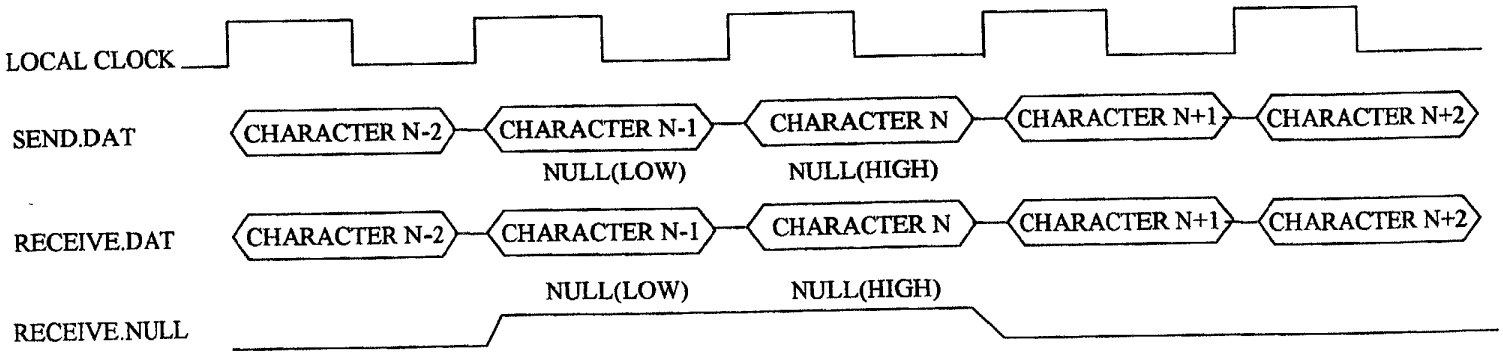


Fig 47B

LENOVO EXHIBIT 1002 - 127/553

TOZOTT "S295h00T

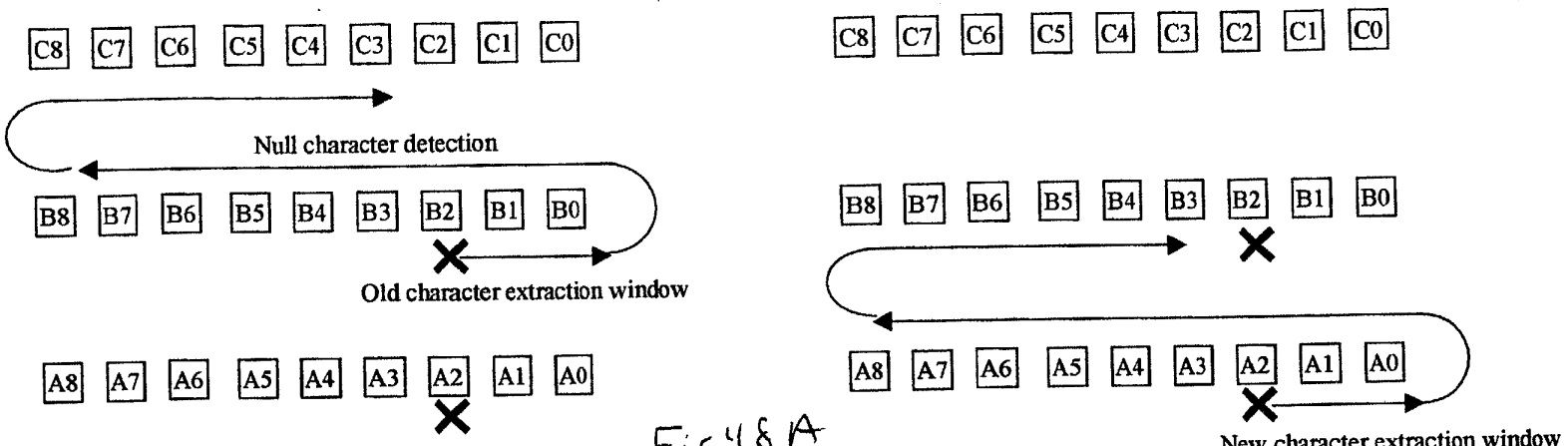


Fig 48A

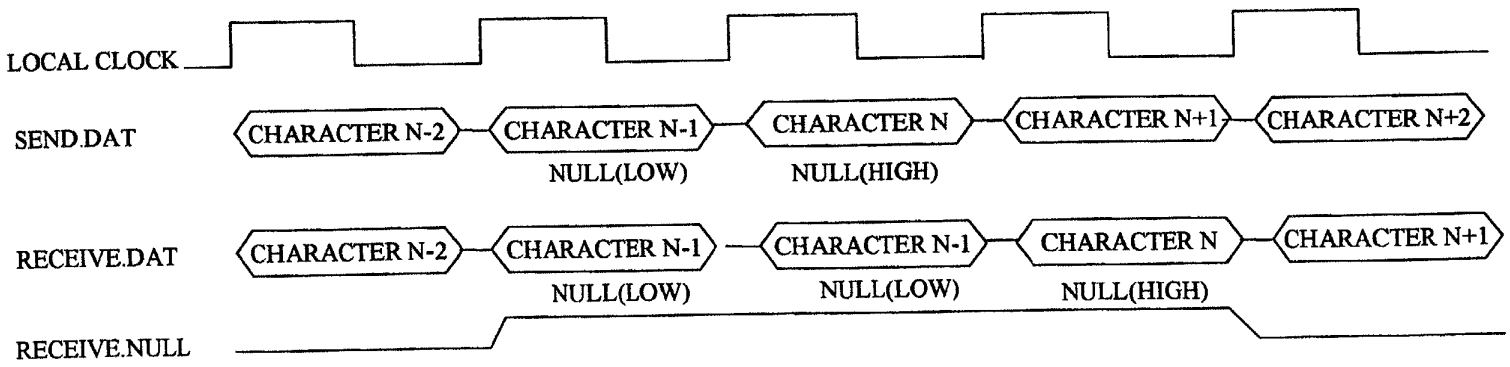


Fig 48B

LENOVO EXHIBIT 1002 - 128/553

TO2OTT" 5295h00T

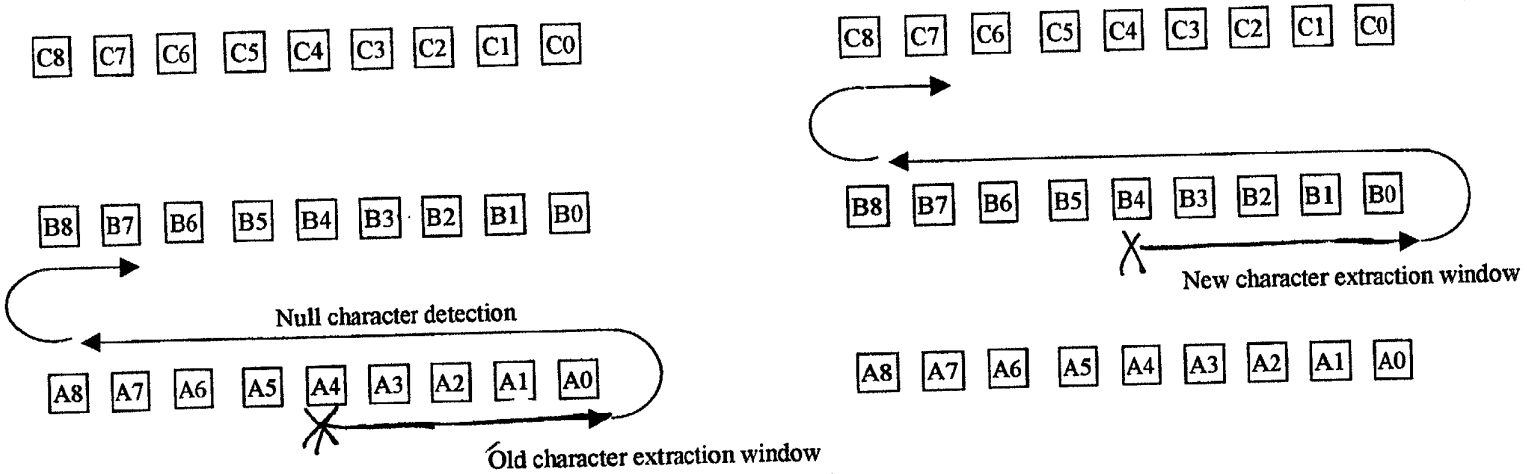


Fig. 49A

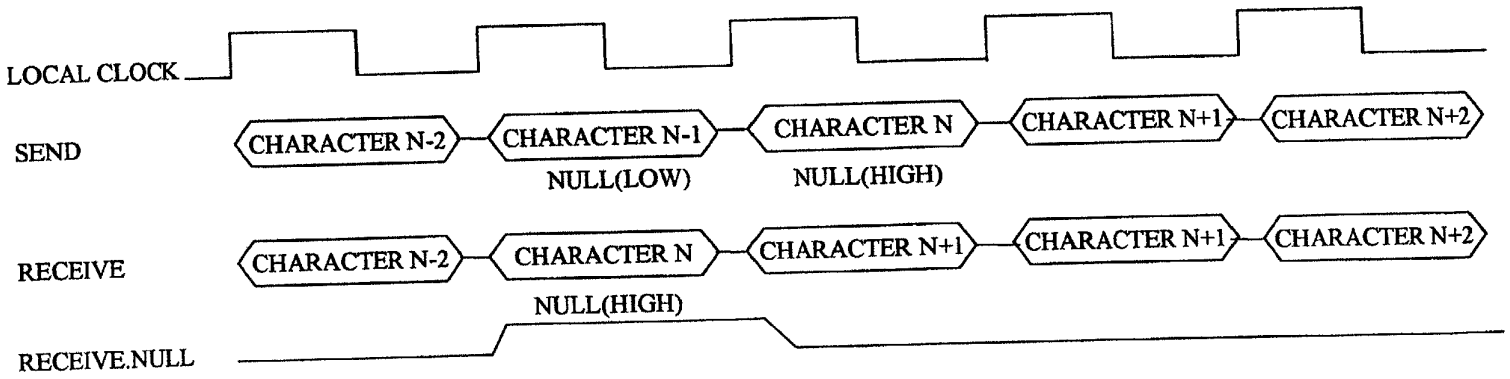


Fig 49B

LENOVO EXHIBIT 1002 - 129/553

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Yeshik Shin et al.
Filed	:	Concurrently Herewith
For	:	METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS
		Docket No. : 371798018US

Commissioner for Patents
Washington, DC 20231

ELECTION UNDER 37 C.F.R. §§ 3.71 AND 3.73
AND POWER OF ATTORNEY

Sir:

The undersigned, being Assignee of the entire interest in the above-identified application by virtue of an Assignment filed concurrently herewith, a copy of which is enclosed, hereby elects under 37 C.F.R. § 3.71, to prosecute the application to the exclusion of the inventors.

Assignee hereby appoints JERRY A. RIEDINGER, Registration No. 30,582; MAURICE J. PIRIO, Registration No. 33,273; MICHAEL D. BROADDUS, Registration No. 41,637; CATHERINE HONG TRAN, Registration No. 43,960; ROBERT G. WOOLSTON, Registration No. 37,263; PAUL T. PARKER, Registration No. 38,264; JOHN M. WECHKIN, Registration No. 42,216; CHRISTOPHER DALEY-WATSON, Registration No. 34,807; STEVEN D. LAWRENZ, Registration No. 37,376; JAMES A.D. WHITE, Registration No. 43,985; STEPHEN E. ARNETT, Registration No. 47,392; EDWARD S. HOTCHKISS, Registration No. 33,904; JAMES NICKELSON, Registration No. 46,140; MARK A. THOMAS, Registration No. 37,953; BRETON A. BOCCHIERI, Registration No. 31,739; BARBARA B. COURTNEY,

LENOVO EXHIBIT 1002 - 130/553

Registration No. 42,442; PETER J. DEHLINGER, Registration No. 28,006; LEE ANN GORTHEY, Registration No. 37,337; RICHARD L. GREGORY, Registration No. 42,607; LINDA R. JUDGE, Registration No. 42,702; MICHAEL MARTENSEN, Registration No. 46,901; JUDY M. MOHR, Registration No. 38,563; and LARRY THROWER, Registration No. 47,994, all of Perkins Coie LLP, Assignee hereby appoints ROBERT G. WOOLSTON of Perkins Coie LLP, as the principal attorney with full power of substitution, association, and revocation to prosecute said application, to transact all business in the Patent and Trademark Office connected therewith, and to receive the letters patent therefor. Please direct all correspondence to Customer Number 25096.

Bar Code:



25096

PATENT TRADEMARK OFFICE

Pursuant to 37 C.F.R. § 3.73, the undersigned duly authorized designee of Assignee certifies that the evidentiary documents have been reviewed, specifically the Assignment to Silicon Image filed concurrently herewith for recording, a copy of which is attached hereto, and certifies that to the best of my knowledge and belief, title remains in the name of the Assignee.

Silicon Image

10-29-01
Date

Badar Baqai
Badar Baqai
Executive Vice President, Engineering

CJD:jc

Enclosure:
Copy of Assignment

LENOVO EXHIBIT 1002 - 131/553

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

Bib Data Sheet

CONFIRMATION NO. 1053

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/045,625	11/07/2001 RULE	370	2665	594728118US

APPLICANTS

Yeshik Shin, Sunnyvale, CA;

David D. Lee, Palo Alto, CA;
Deog-Kyoon Jeong, Seoul, KOREA, REPUBLIC OF;Shing Kong, Brisbane, CA;

** CONTINUING DATA **********
This appln claims benefit of 60/252,724 11/22/2000

** FOREIGN APPLICATIONS **********

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 02/26/2002

Foreign Priority claimed ☐ yes ☐ no 35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance Verified and Acknowledged Examiner's Signature Initials	STATE OR COUNTRY CA	SHEETS DRAWING 59	TOTAL CLAIMS 24	INDEPENDENT CLAIMS 3

ADDRESS
25096
PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE , WA
98111-1247

TITLE
Method and system for integrating packet type information with synchronization symbols

FILING FEE	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time)

RECEIVED 942	No. _____ for following:	☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2001

Application or Docket Number: 10041625

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	24	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	24 minus 20=	* 4
INDEPENDENT CLAIMS	3 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	370.00	OR	BASIC FEE	740.00
X$ 9=		OR	X$18=	72.00
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	812.00

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LENOVO EXHIBIT 1002 - 134/553

CLAIMS ONLY

SERIAL NO. 10/095625

FILING DATE

APPLICANT(S)

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
1	/					
2		/				
3		/				
4		/				
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TOTAL IND.	3					
TOTAL DEP.	21					
TOTAL CLAIMS	24					

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	IND.	DEP.	IND.	DEP.	IND.	DEP.
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53						
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96						
97						
98						
99						
100						
TOTAL IND.						
TOTAL DEP.						
TOTAL CLAIMS						

*MAY BE USED FOR ADDITIONAL CLAIMS OR ADMENDMENTS

FORM PTO-2022 (1-98)

U.S.DEPARTMENT OF COMMERCE
Patent and Trademark Office

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REQUEST TO RESCIND PREVIOUS NONPUBLICATION REQUEST 35 U.S.C. 122(b)(2)(B)(ii)

Application Number	Unknown 10 045 625
Confirmation Number	Unknown
Filing Date	November 7, 2001
First Named Inventor	Yeshik Shin et al. ✓
Title	METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS
Atty Docket Number	371798018US ✓
Group Art Unit	
Examiner	

I hereby **rescind** the previous request that the above-identified application not be published under 35 U.S.C. 122(b).

January 7, 2002
Date

Maurice J Pirio
Signature

Maurice J. Pirio
Typed or printed name

This application was mailed via Express Mail (No. EL669108811US) to Box Patent Application, Commissioner for Patents, Washington, DC 20231 on November 7, 2001. To date, we have not received the return postcard acknowledging receipt of the application. Therefore, we do not know the application number.

This request must be signed in compliance with 37 CFR 1.33(b).

Burden Hour Statement: This collection of information is required by 37 CFR 1.213(b). The information is used by the public to rescind a previously filed request that an application not be published under 35 U.S.C. 122(b) (and the PTO to process that rescission). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 6 minutes to complete. This time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

OIPE JC149 FEB 08 2002 PATENT & TRADEMARK OFFICE

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REQUEST TO RESCIND PREVIOUS NONPUBLICATION REQUEST 35 U.S.C. 122(b)(2)(B)(ii)

Application Number	Unknown 10035911
Confirmation Number	Unknown
Filing Date	November 7, 2001
First Named Inventor	Yeshik Shin et al.
Title	METHOD AND SYSTEM FOR NESTING OF COMMUNICATIONS PACKETS
Atty Docket Number	371798019US
Group Art Unit	
Examiner	

I hereby **rescind** the previous request that the above-identified application not be published under 35 U.S.C. 122(b).

January 7, 2002
Date

Maurice J Pirio
Signature

Maurice J. Pirio
Typed or printed name

This application was mailed via Express Mail (No. EL669108842US) to Box Patent Application, Commissioner for Patents, Washington, DC 20231 on November 7, 2001. To date, we have not received the return postcard acknowledging receipt of the application. Therefore, we do not know the application number.

This request must be signed in compliance with 37 CFR 1.33(b).

Burden Hour Statement: This collection of information is required by 37 CFR 1.213(b). The information is used by the public to rescind a previously filed request that an application not be published under 35 U.S.C. 122(b) (and the PTO to process that rescission). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 6 minutes to complete. This time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/045,625	11/07/2001	Yeshik Shin	371798018US

CONFIRMATION NO. 1053

25096
PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE, WA 98111-1247

FORMALITIES LETTER

OC000000007536344

Date Mailed: 02/26/2002

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit $ **740** *to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).*
- Total additional claim fee(s) for this application is $72.
  - **$72** for **4** total claims over 20.
- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(l) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.
- **The balance due by applicant is $ 942.**

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Substitute drawings in compliance with 37 CFR 1.84 because:
  - drawing sheets do not have the appropriate margin(s) (see 37 CFR 1.84(g)). Each sheet must include a top margin of at least 2.5 cm. (1 inch), a left side margin of at least 2.5 cm. (1 inch), a right side margin of at least 1.5 cm. (5/8 inch), and a bottom margin of at least 1.0 cm. (3/8 inch);
  - Drawings must be reasonably free from erasures and must be free from alterations, overwritings, interlineations, folds, and copy marks.

A copy of this notice MUST be returned with the reply.

Tedros

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 3 - OFFICE COPY

OIPE JC48 MAY 30 2002 PATENT & TRADEMARK OFFICE

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Box Missing Parts, Commissioner for Patents, Washington, DC 20231.

5/24/02 Jeanne Connelly

Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Yeshik Shin et al.
Application No.	:	10/045,625 Confirmation No.: 1053
Filed	:	November 7, 2001
For	:	METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS
Docket No.	:	371798018US
Date	:	May 24, 2002

Box Missing Parts
Commissioner for Patents
Washington, DC 20231

RESPONSE TO NOTICE TO FILE MISSING PARTS OF APPLICATION

Sir:

In response to the Notice to File Missing Parts dated February 26, 2002, please find enclosed a Declaration, Authorization for Extensions of Time Under 37 CFR § 1.136(a)(3), and a copy of the Notice to File Missing Parts for the above-identified application.

Also enclosed is a Transmittal of Formal Drawings (Figures 1-49B)

Please find enclosed a Petition for an Extension of Time, extending the time for response from April 26, 2002 to May 26, 2002.

LENOVO EXHIBIT 1002 - 140/553

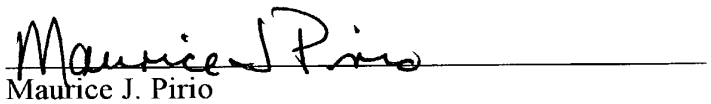
The fees have been calculated as follows:

Basic Fee	$	740.00
Total Claims (24, 4 extra)		72.00
Independent Claims (3, 0 extra)		0
Missing Parts Surcharge		130.00
Total	$	942.00
Extension-of-Time Fee		110.00
TOTAL	$	1052

Enclosed is a check in the amount of $1052.00 for the requisite fees. The Commissioner is hereby authorized to charge any additional filing fees or to credit any overpayment to Deposit Account No. 50-0665. A duplicate copy of this response is enclosed.

Respectfully submitted,

Perkins Coie LLP



Maurice J. Pirio
Registration No. 33,273

MJP:jc

Enclosures:
- Postcard
- Check
- Copy of this Response
- Declaration
- Authorization for Extensions of Time Under 37 CFR § 1.136(a)(3)
- Petition for Extension of Time (+ 2 copies)
- Transmittal of Formal Drawings
- Copy of Notice to File Missing Parts

PERKINS COIE LLP
P.O. Box 1247
Seattle, Washington 98111-1247
(206) 583-8888
FAX: (206) 583-8500

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APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/045,625	11/07/2001	Yeshik Shin	371798018US

CONFIRMATION NO. 1053

25096
PERKINS COIE LLP
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SEATTLE, WA 98111-1247

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MAR 05 2002
PERKINS COIE LLP

FORMALITIES LETTER

OC000000007536344

Date Mailed: 02/26/2002

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit $ **740** *to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).*
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- **The balance due by applicant is $ 942.**

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Substitute drawings in compliance with 37 CFR 1.84 because:
  - drawing sheets do not have the appropriate margin(s) (see 37 CFR 1.84(g)). Each sheet must include a top margin of at least 2.5 cm. (1 inch), a left side margin of at least 2.5 cm. (1 inch), a right side margin of at least 1.5 cm (5/8 inch), and a bottom margin of at least 1.0 cm. (3/8 inch);
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05/31/2002 CCHAU1 00000138 10045625
02 FC:101 740.00 OP
03 FC:103 72.00 OP
04 FC:105 130.00 OP

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

OIPE JC48 MAY 30 2002 PATENT & TRADEMARK OFFICE

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Box Missing Parts, Commissioner for Patents, Washington, DC 20231.

5/24/02 Jeanne Connelly

Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Yeshik Shin et al.
Application No.	:	10/045,625 Confirmation No.: 1053
Filed	:	November 7, 2001
For	:	METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS
Docket No.	:	371798018US
Date	:	May 24, 2002

Box Missing Parts
Commissioner for Patents
Washington, DC 20231

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LENOVO EXHIBIT 1002 - 144/553

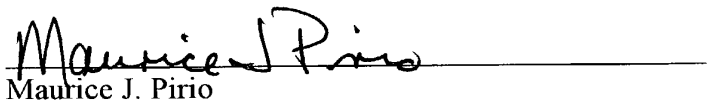
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Respectfully submitted,

Perkins Coie LLP



Maurice J. Pirio
Registration No. 33,273

MJP:jc

Enclosures:
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LENOVO EXHIBIT 1002 - 145/553

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APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/045,625	11/07/2001	Yeshik Shin	371798018US

CONFIRMATION NO. 1053

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RECEIVED
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FORMALITIES LETTER

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Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

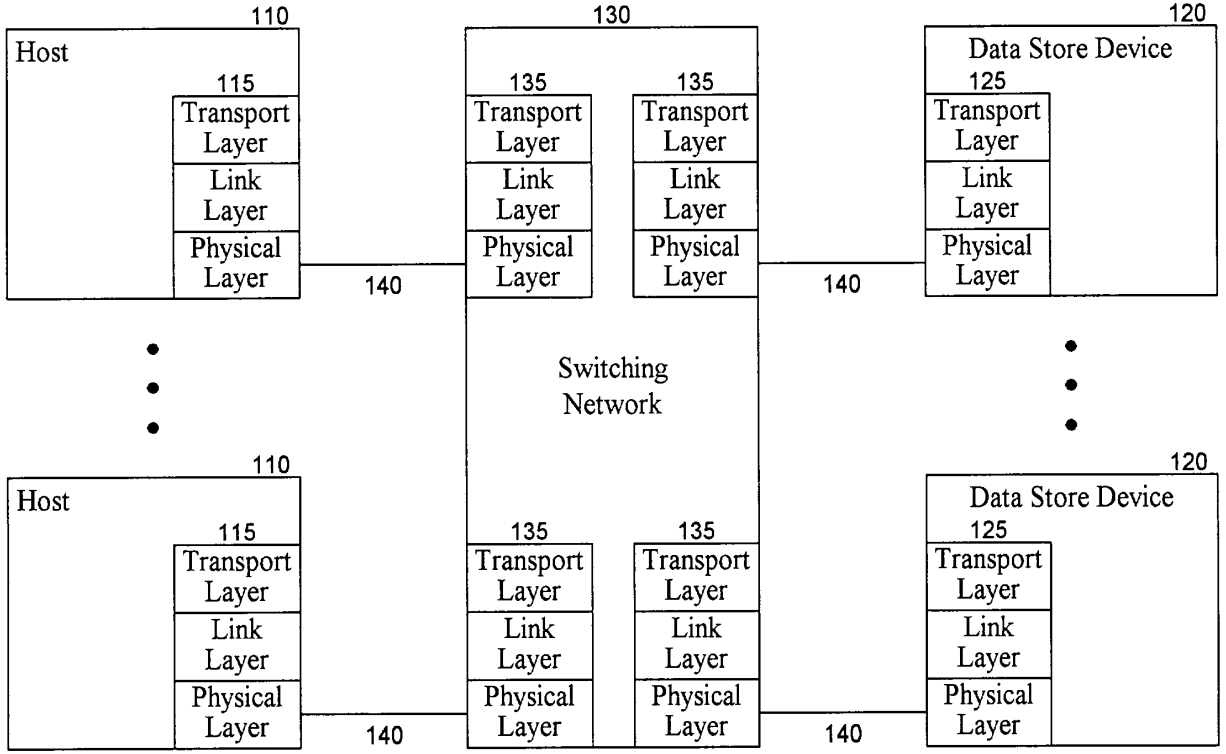


Fig. 1

LENOVO EXHIBIT 1002 - 148/553

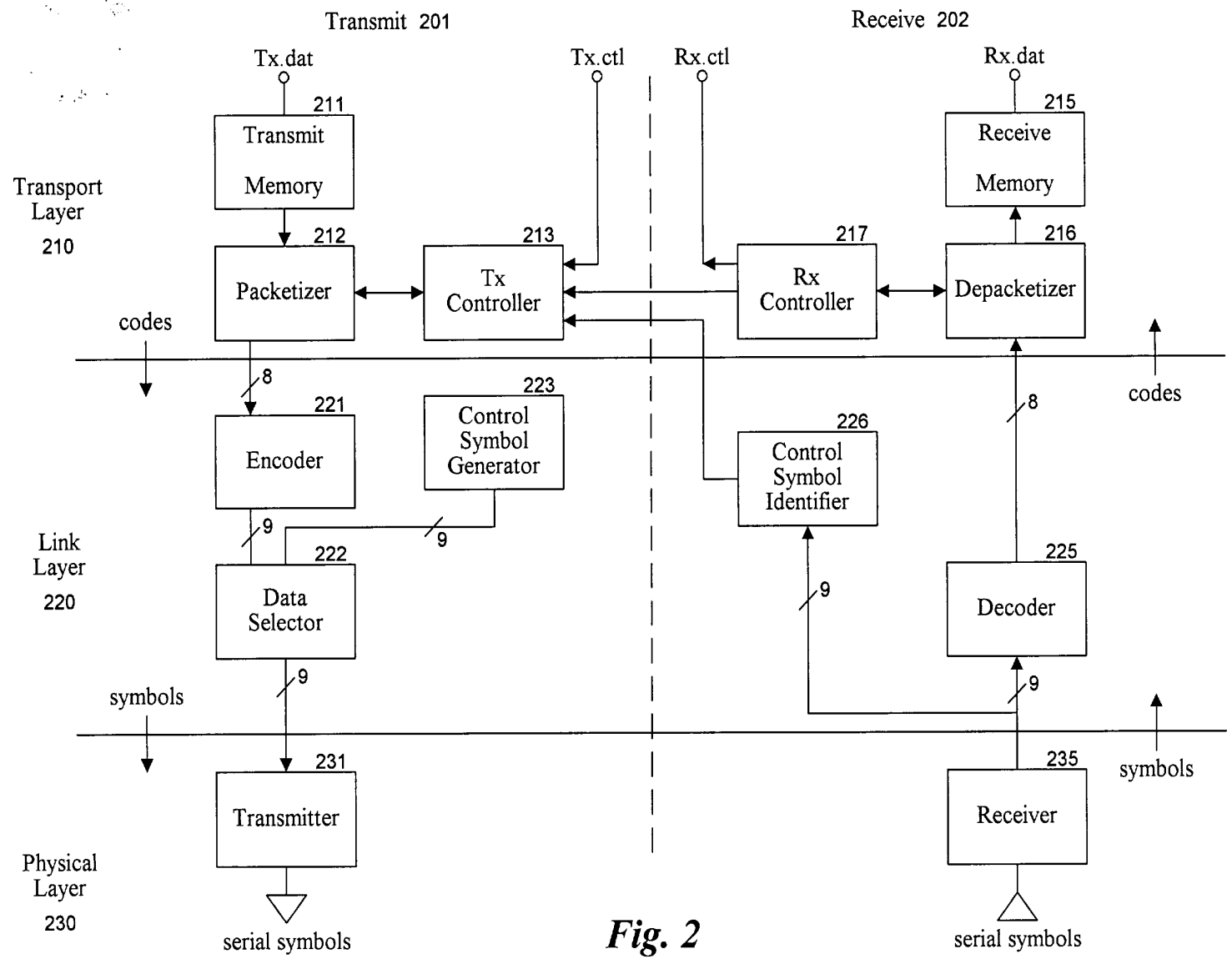


Fig. 2

LENOVO EXHIBIT 1002 - 149/553

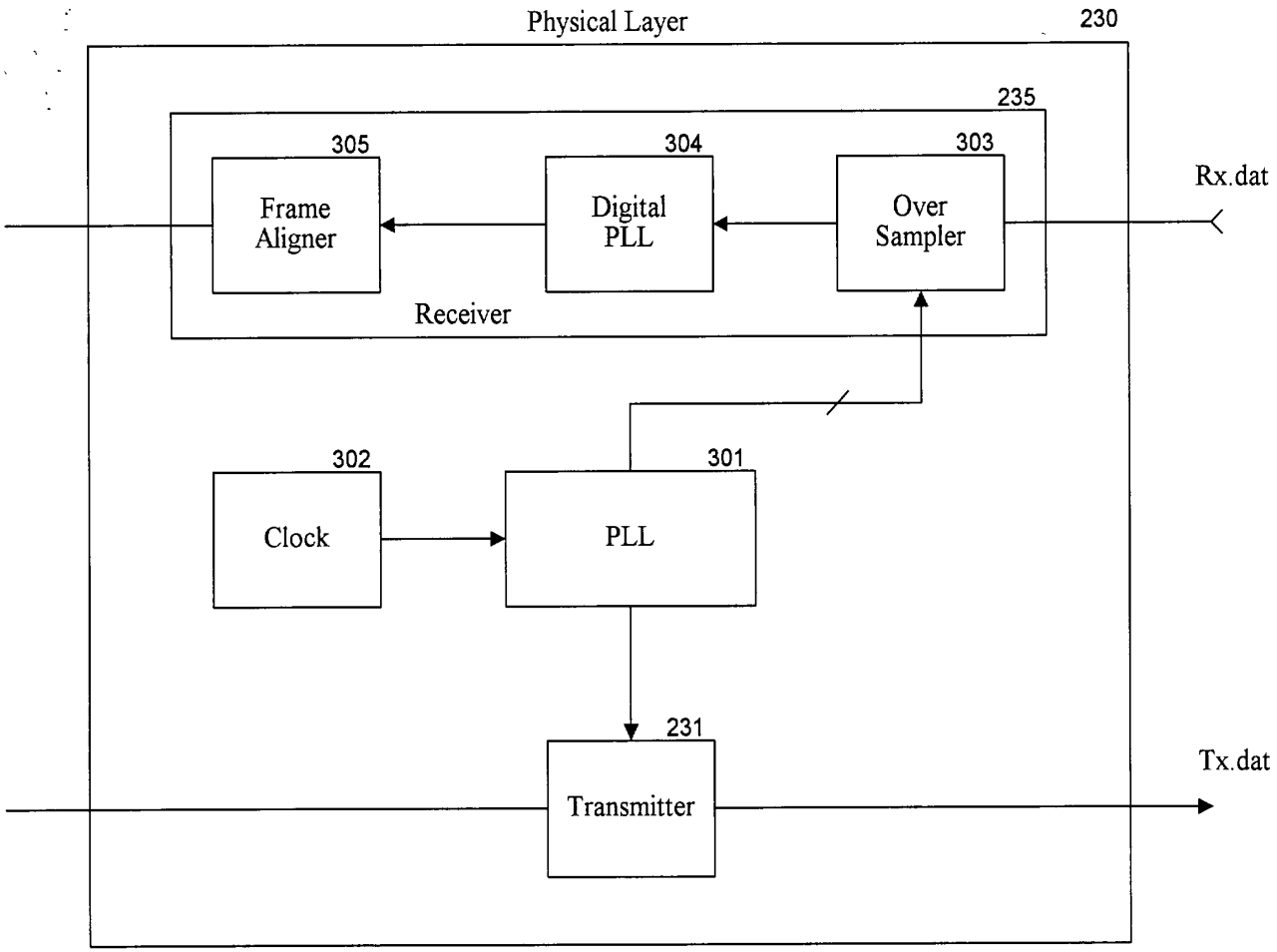


Fig. 3

LENOVO EXHIBIT 1002 - 150/553

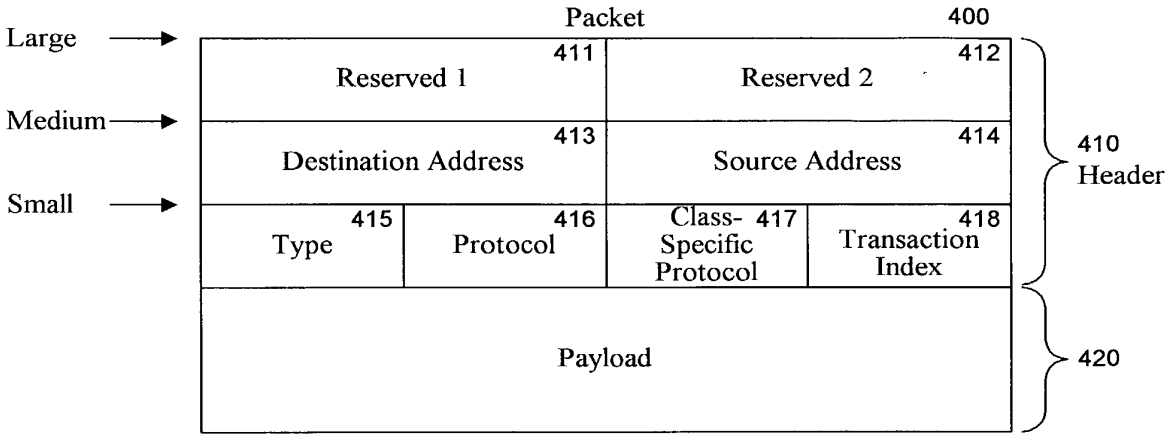

Packet
400
Large
Medium
Small
411
Reserved 1
412
Reserved 2
413
Destination Address
414
Source Address
415
Type
416
Protocol
Class-Specific Protocol
417
418
Transaction Index
410
Header
Payload
420

Fig. 4

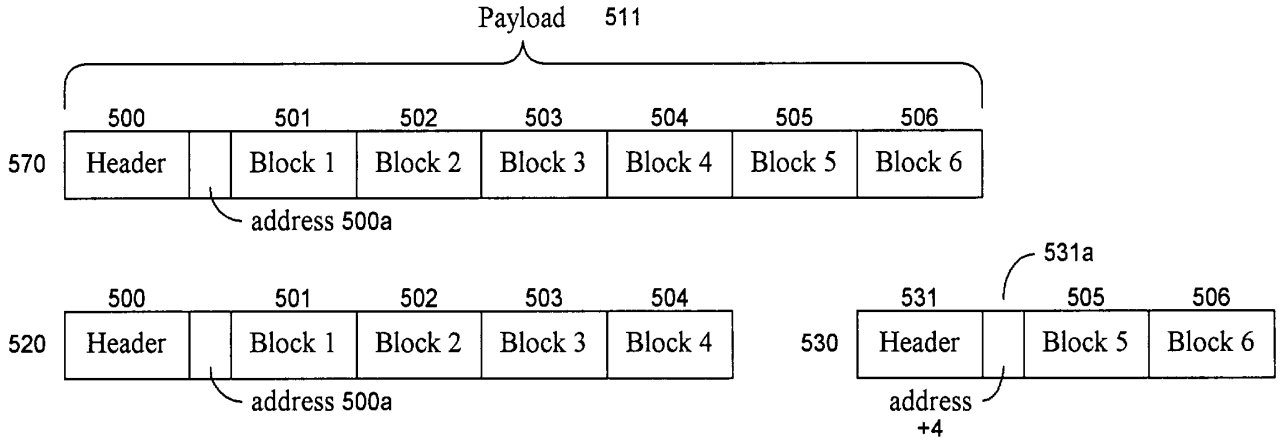


Fig. 5

LENOVO EXHIBIT 1002 - 152/553

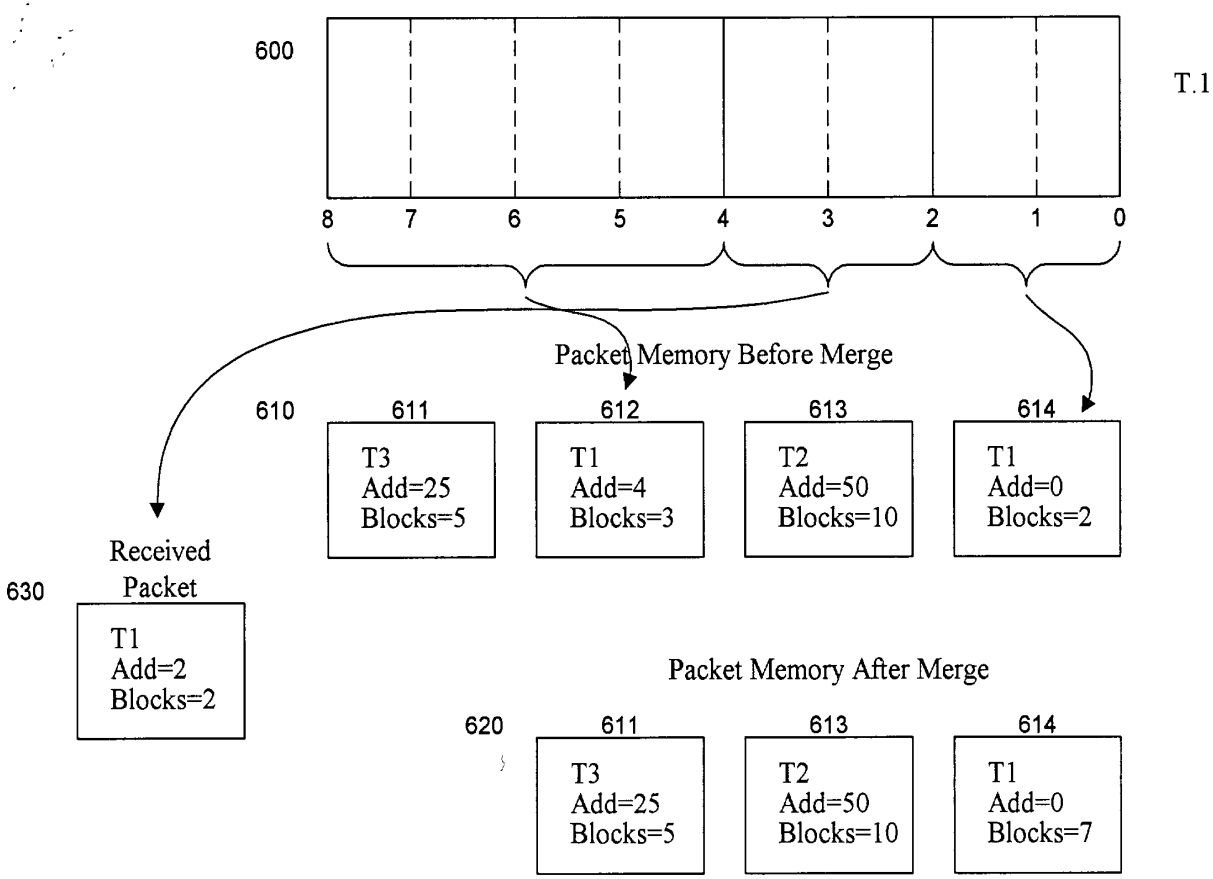


Fig. 6

LENOVO EXHIBIT 1002 - 153/553

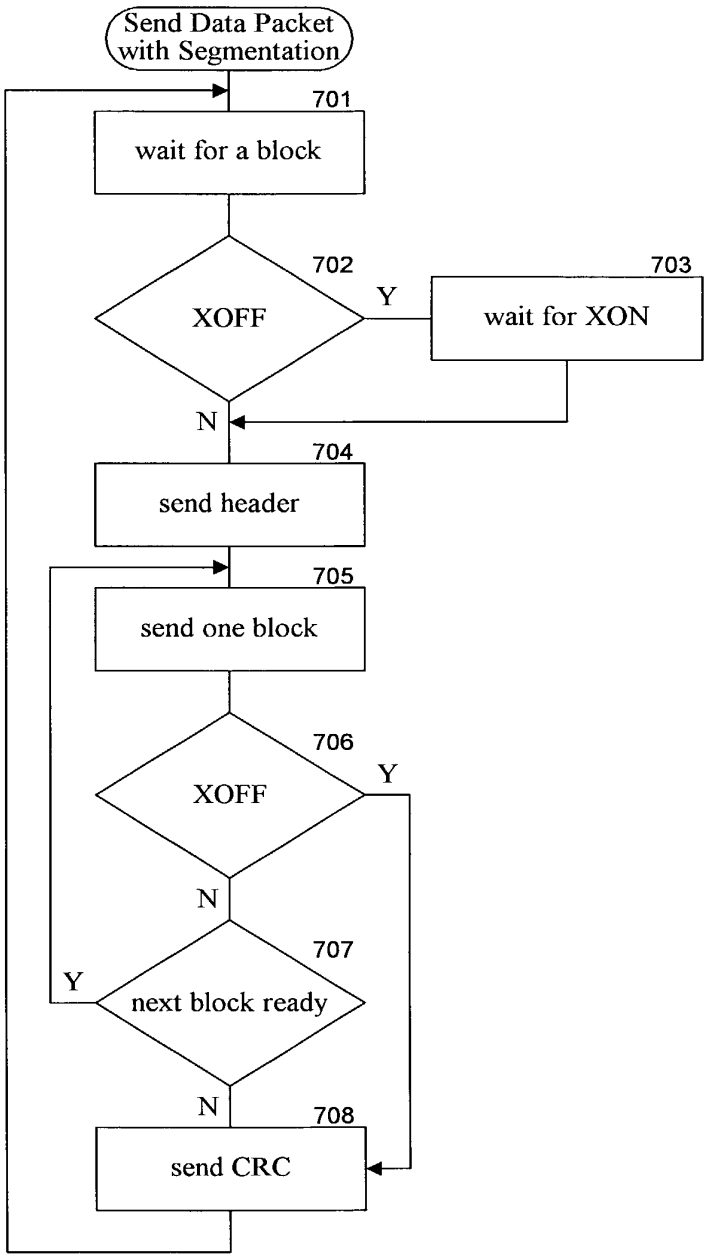

Send Data Packet with Segmentation
701
wait for a block
702
XOFF
Y
703
wait for XON
N
704
send header
705
send one block
706
XOFF
Y
N
707
Y
next block ready
N
708
send CRC

Fig. 7

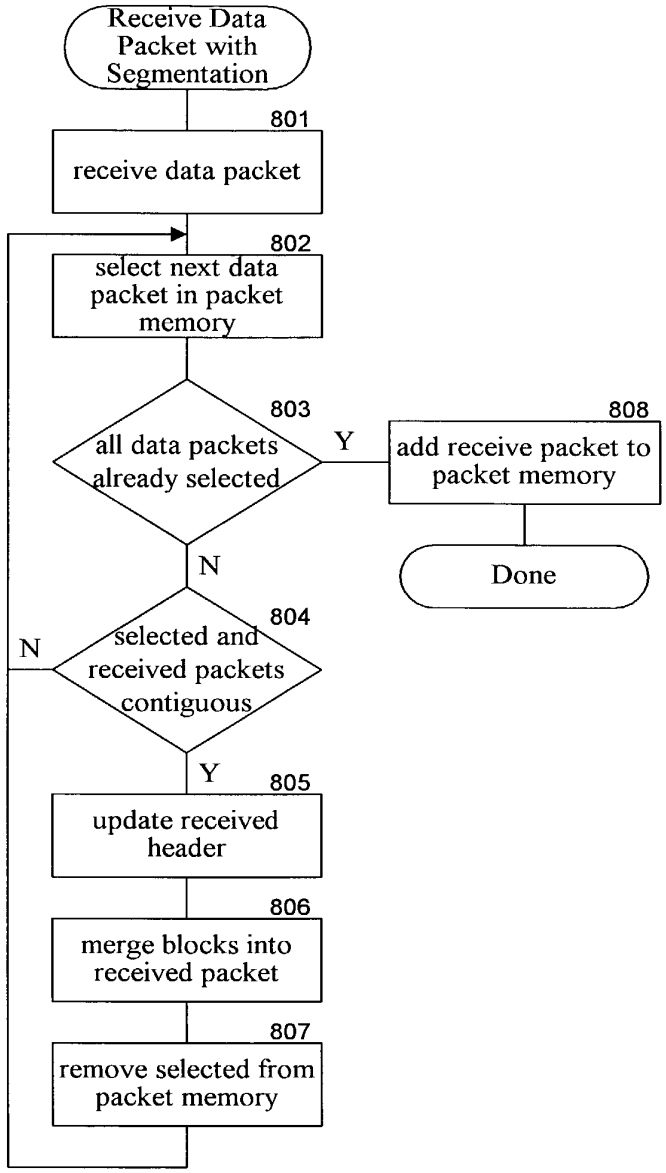
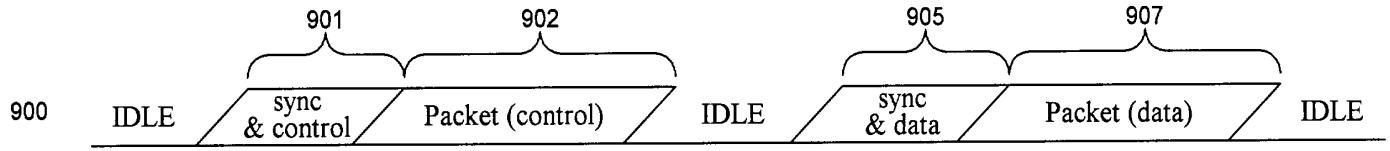

Receive Data Packet with Segmentation
801
receive data packet
802
select next data packet in packet memory
803
all data packets already selected
Y
808
add receive packet to packet memory
Done
N
804
selected and received packets contiguous
N
Y
805
update received header
806
merge blocks into received packet
807
remove selected from packet memory

Fig. 8



sync & packet type

Fig. 9A

LENOVO EXHIBIT 1002 - 156/553

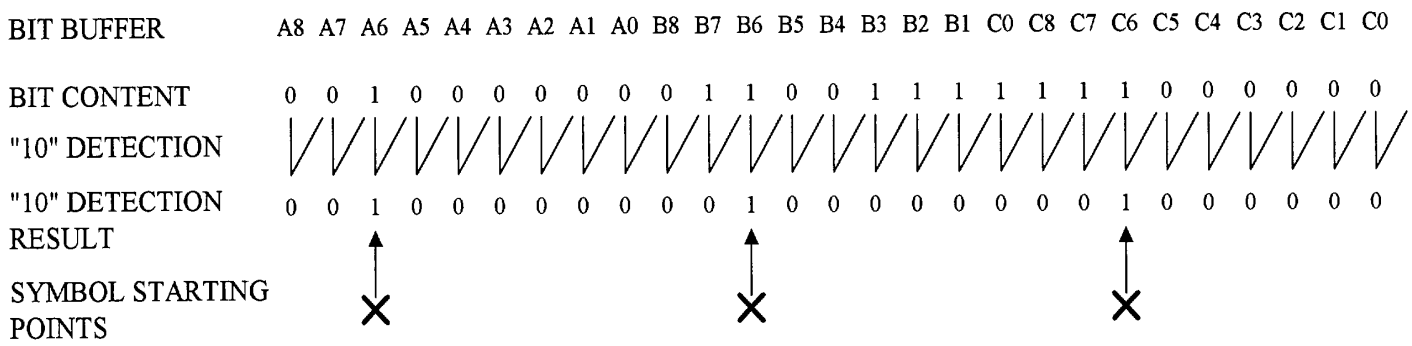


Fig. 9B

LENOVO EXHIBIT 1002 - 157/553

EP 2 565 825 B1

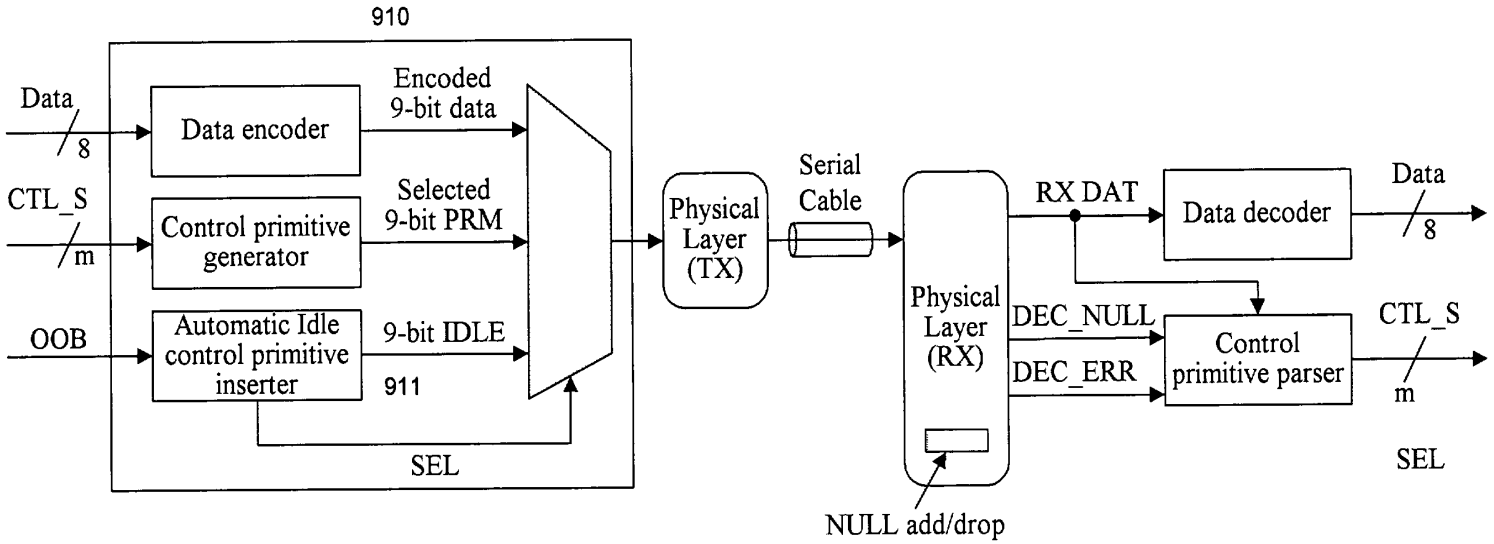


Fig. 9C

LENOVO EXHIBIT 1002 - 158/553

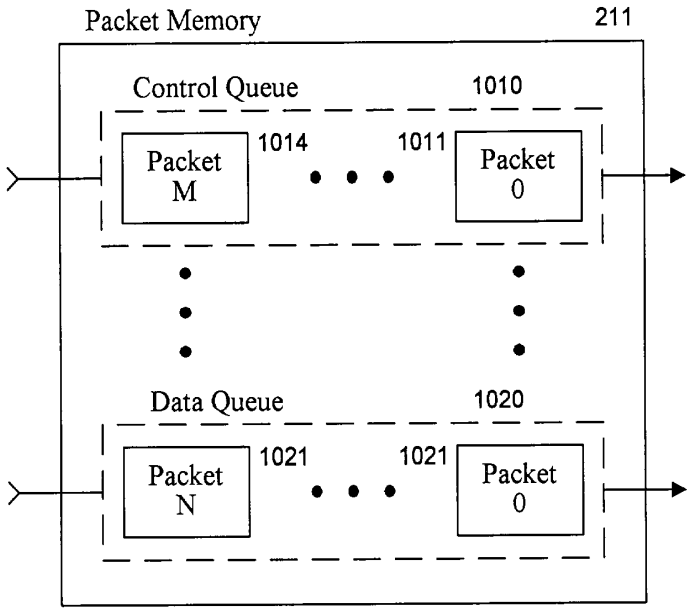


Fig. 10

LENOVO EXHIBIT 1002 - 159/553

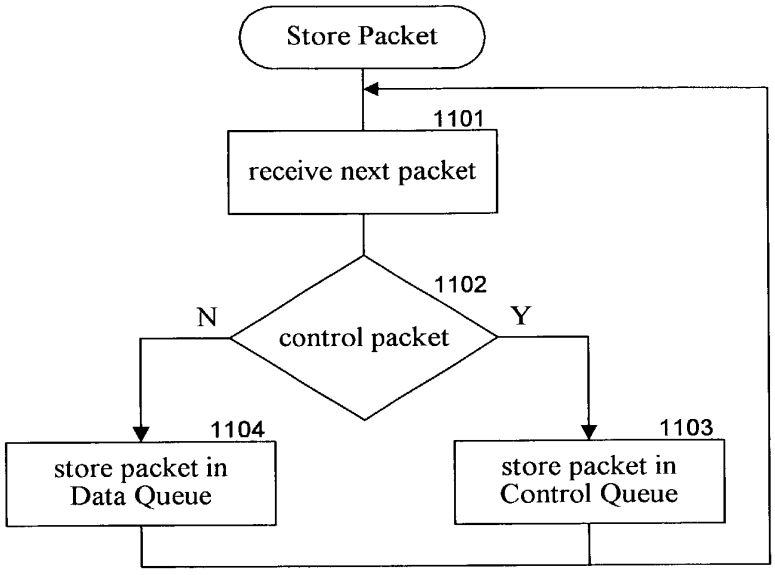

Store Packet
1101
receive next packet
1102
N
control packet
Y
1104
store packet in Data Queue
1103
store packet in Control Queue

Fig. 11

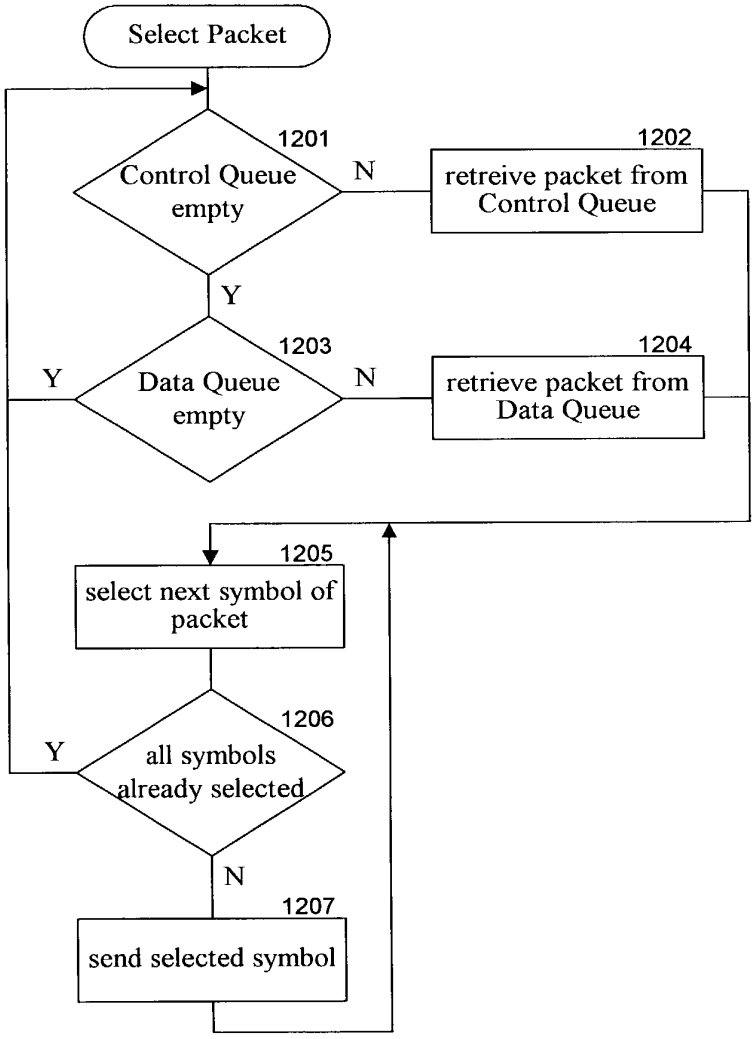

Select Packet
1201
Control Queue empty
N
1202
retreive packet from Control Queue
Y
1203
Data Queue empty
Y
N
1204
retrieve packet from Data Queue
1205
select next symbol of packet
1206
all symbols already selected
Y
N
1207
send selected symbol

Fig. 12

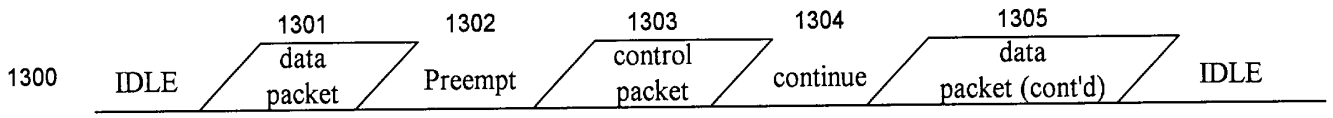


Fig. 13

LENOVO EXHIBIT 1002 - 162/553

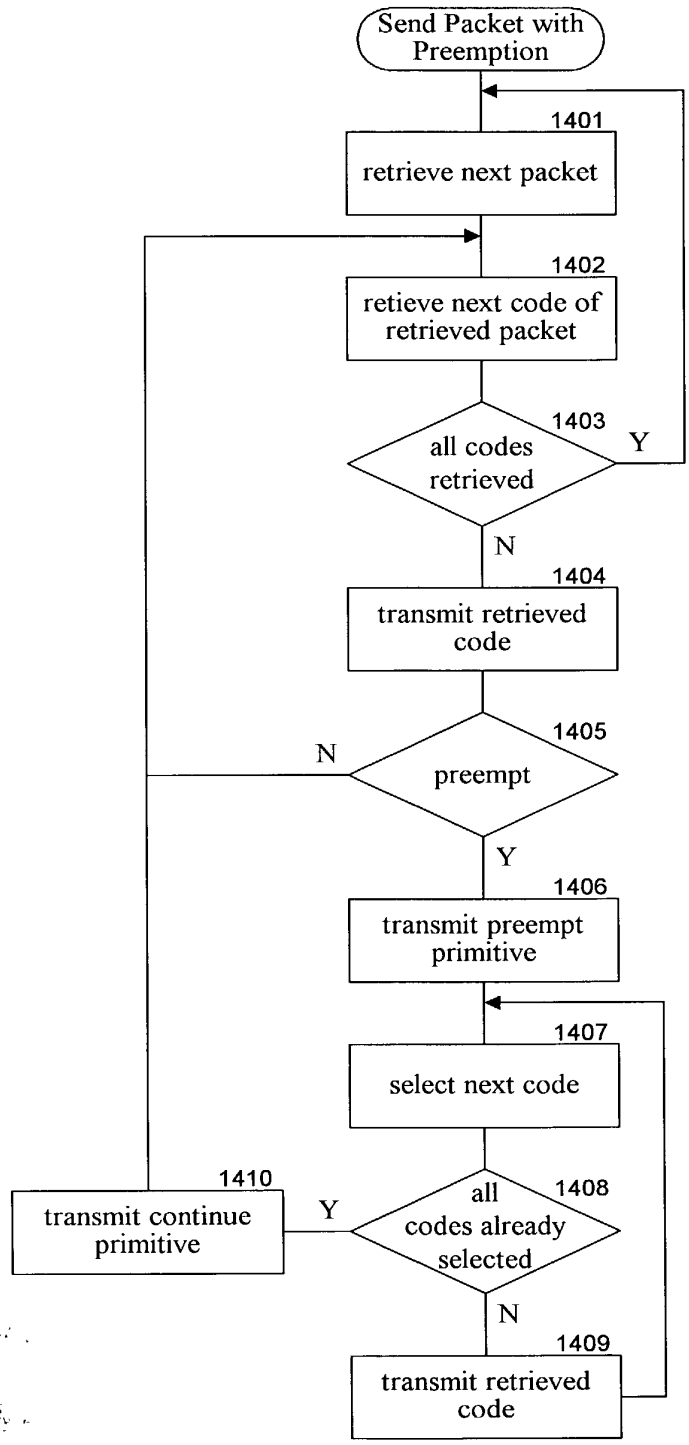

Send Packet with Preemption
1401
retrieve next packet
1402
retieve next code of retrieved packet
1403
all codes retrieved
Y
N
1404
transmit retrieved code
1405
preempt
N
Y
1406
transmit preempt primitive
1407
select next code
1408
all codes already selected
Y
1410
transmit continue primitive
N
1409
transmit retrieved code

Fig. 14

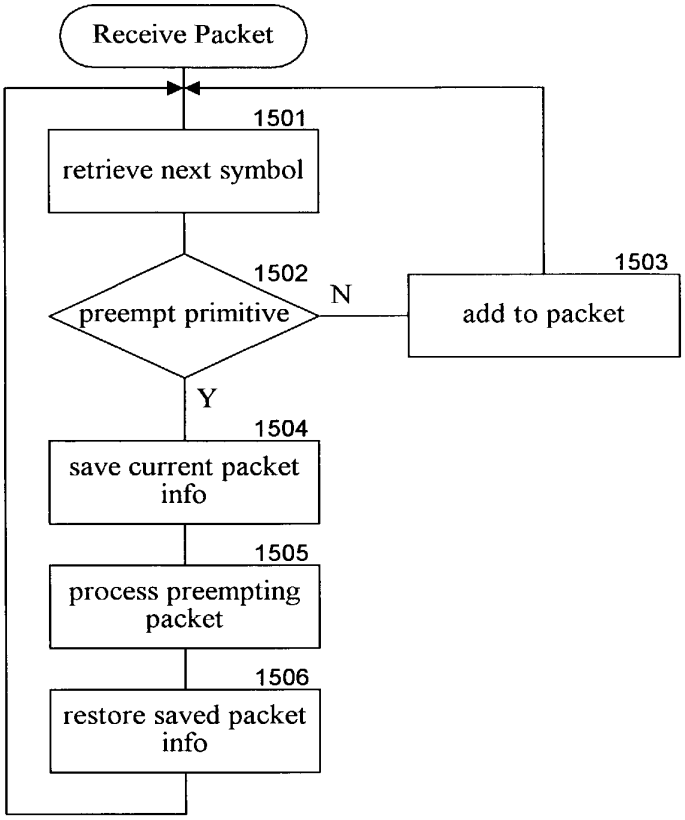

Receive Packet
1501
retrieve next symbol
1502
preempt primitive
N
1503
add to packet
Y
1504
save current packet info
1505
process preempting packet
1506
restore saved packet info

Fig. 15

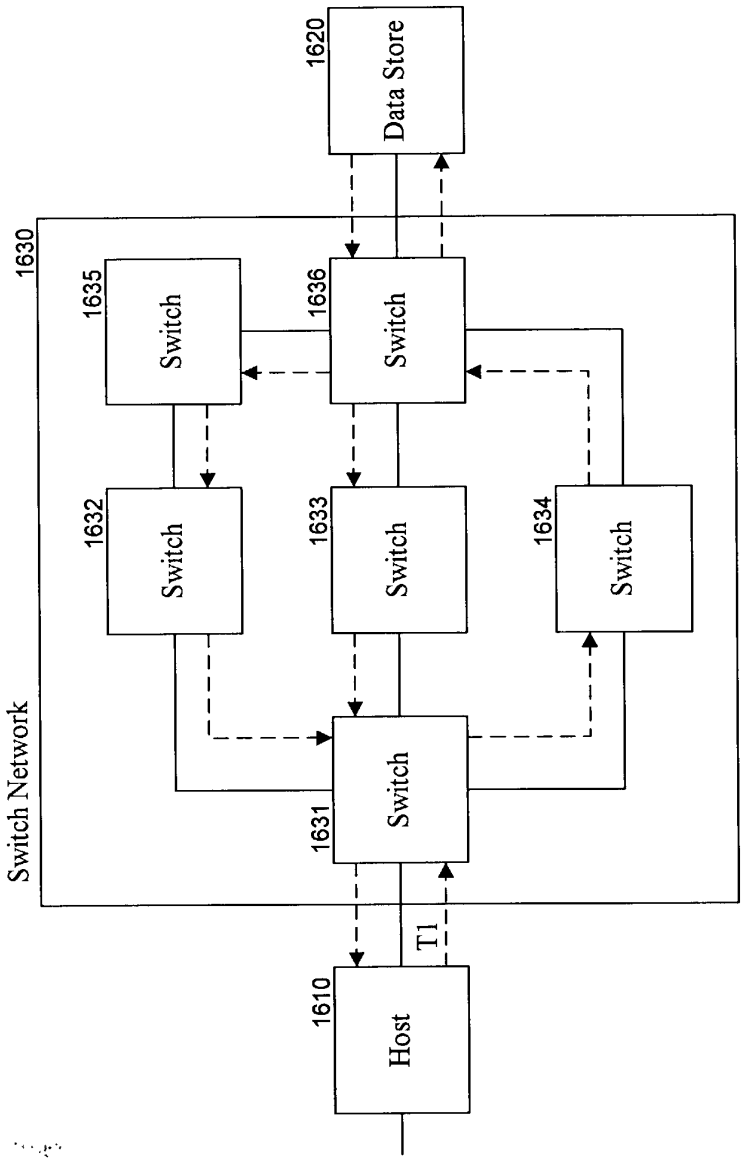

1620
Data Store
1630
Switch Network
1635
Switch
1636
Switch
1632
Switch
1633
Switch
1634
Switch
1631
Switch
T1
1610
Host

Fig. 16

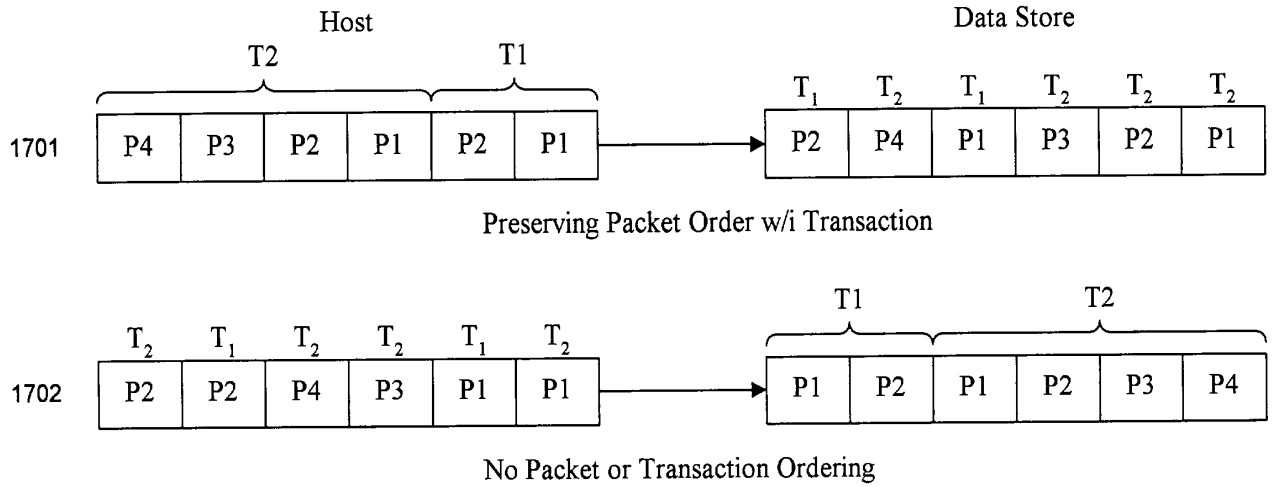


Fig. 17

LENOVO EXHIBIT 1002 - 166/553

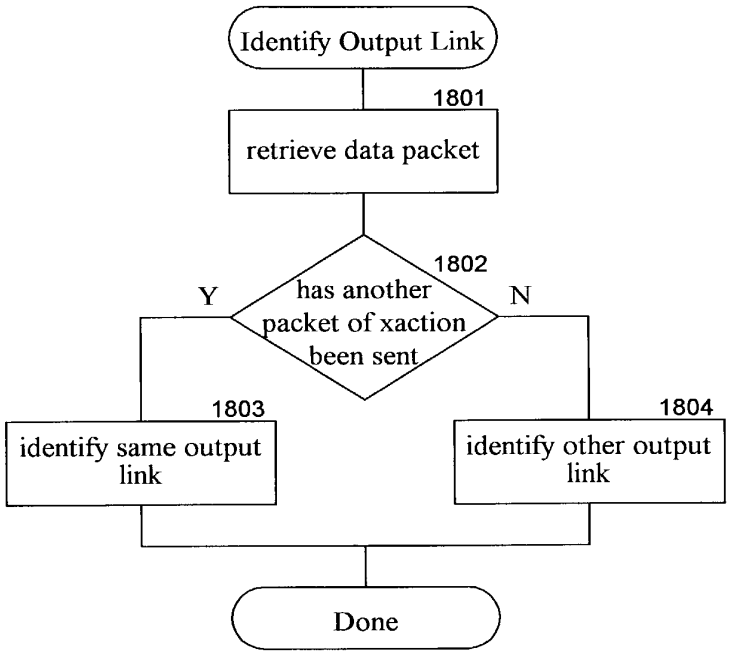

Identify Output Link
1801
retrieve data packet
1802
has another packet of xaction been sent
Y
N
1803
identify same output link
1804
identify other output link
Done

Fig. 18

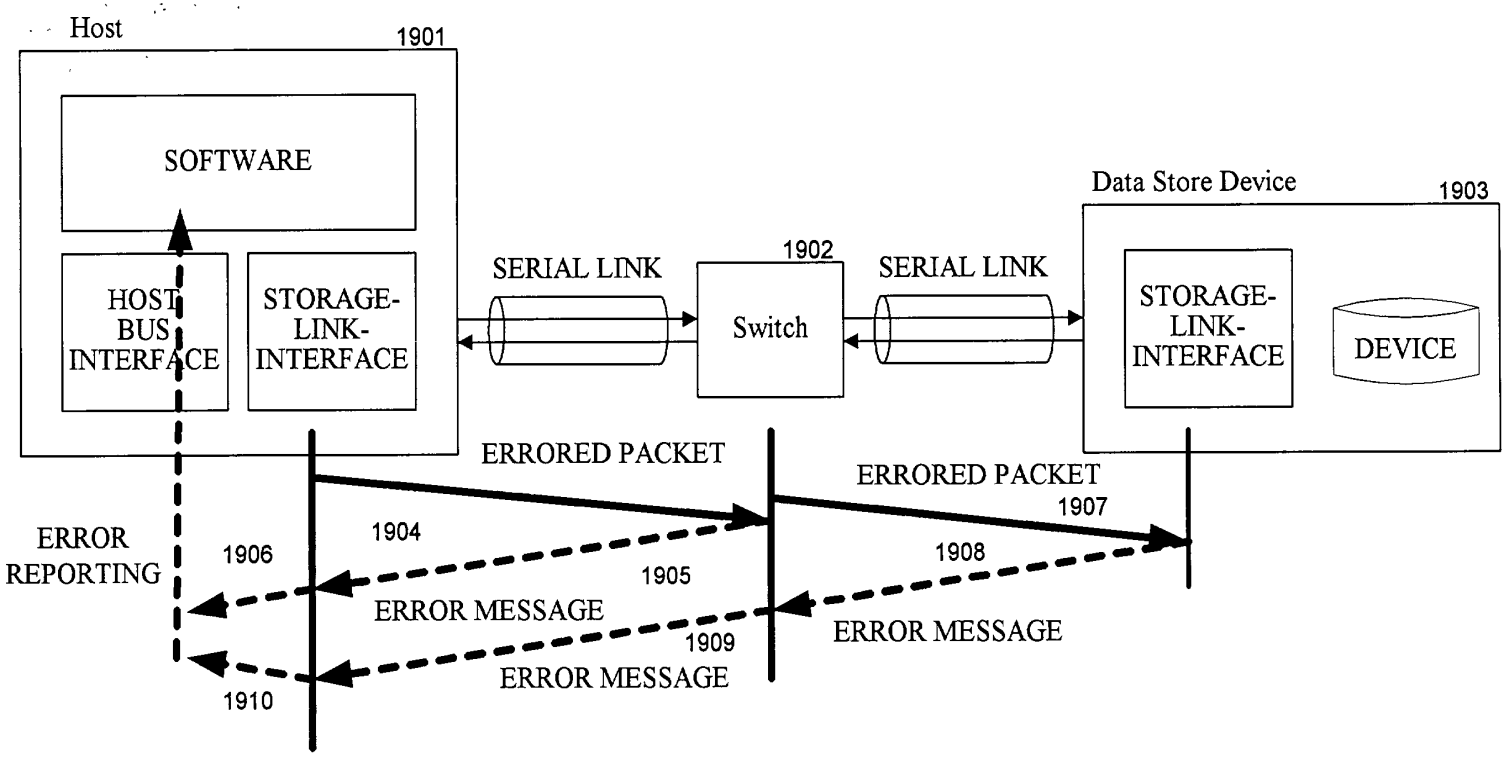


Fig. 19A

LENOVO EXHIBIT 1002 - 168/553

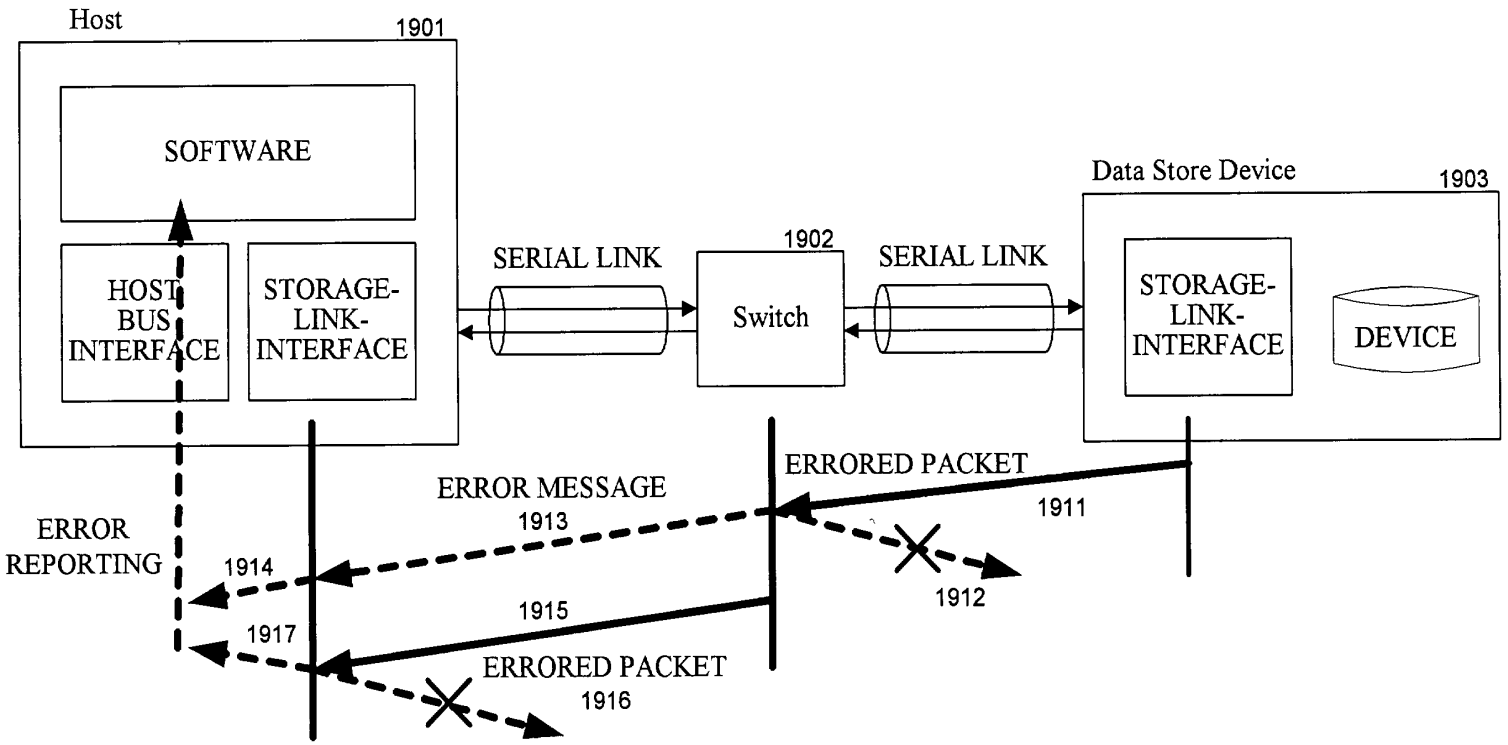


Fig. 19B

LENOVO EXHIBIT 1002 - 169/553

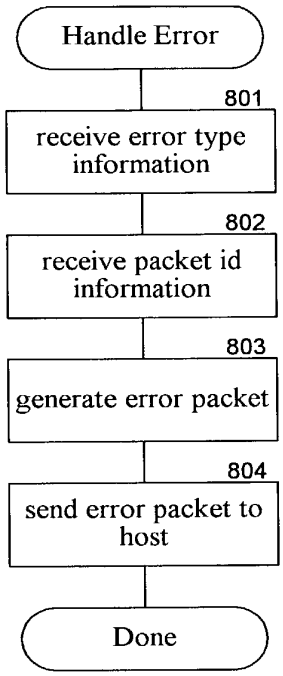

Handle Error
801
receive error type information
802
receive packet id information
803
generate error packet
804
send error packet to host
Done

Fig. 19C

8b code	9 bit symbol
0000 0000	101010101
0000 0001	101010100
0000 0010	101010111
⋮	
0101 0101	001010101
⋮	
0111 0110	001110110
0111 0111	100100010
⋮	
1111 1111	110101010

Fig. 20

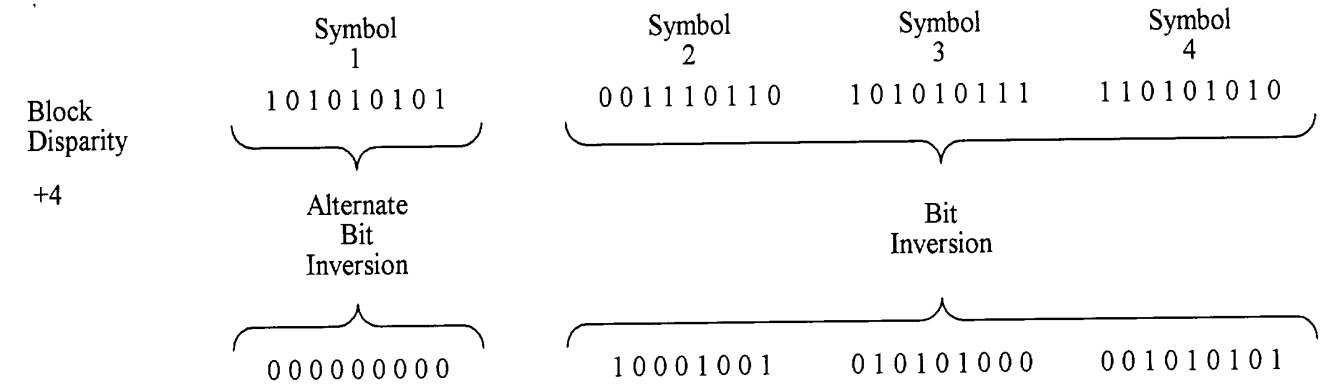


Fig. 21A

LENOVO EXHIBIT 1002 - 172/553

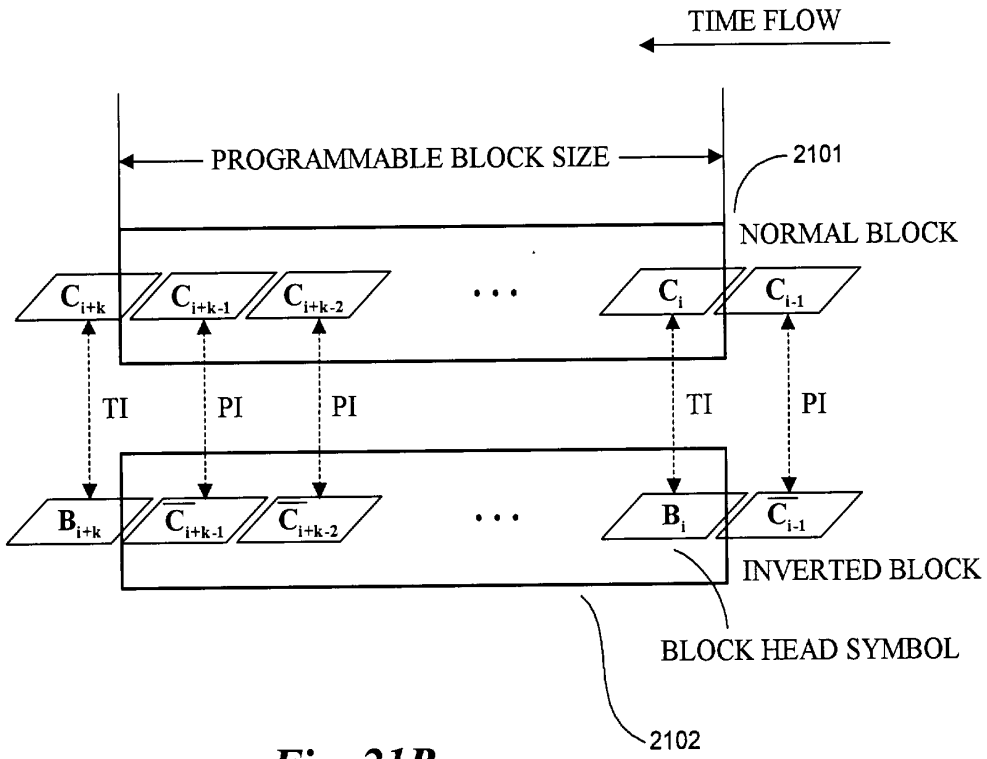


Fig. 21B

LENOVO EXHIBIT 1002 - 173/553

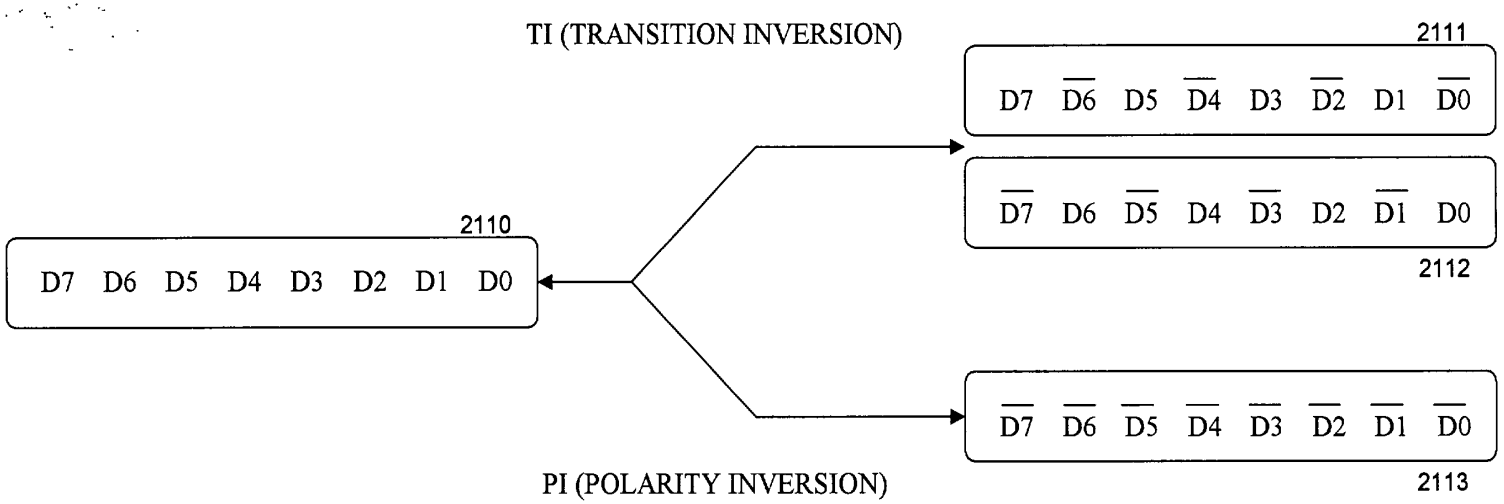


Fig. 21C

LENOVO EXHIBIT 1002 - 174/553

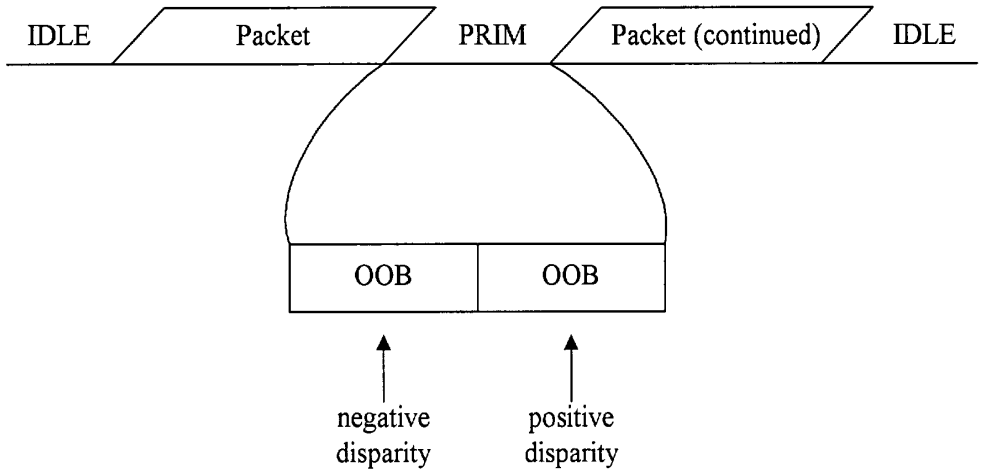


Fig. 22

LENOVO EXHIBIT 1002 - 175/553

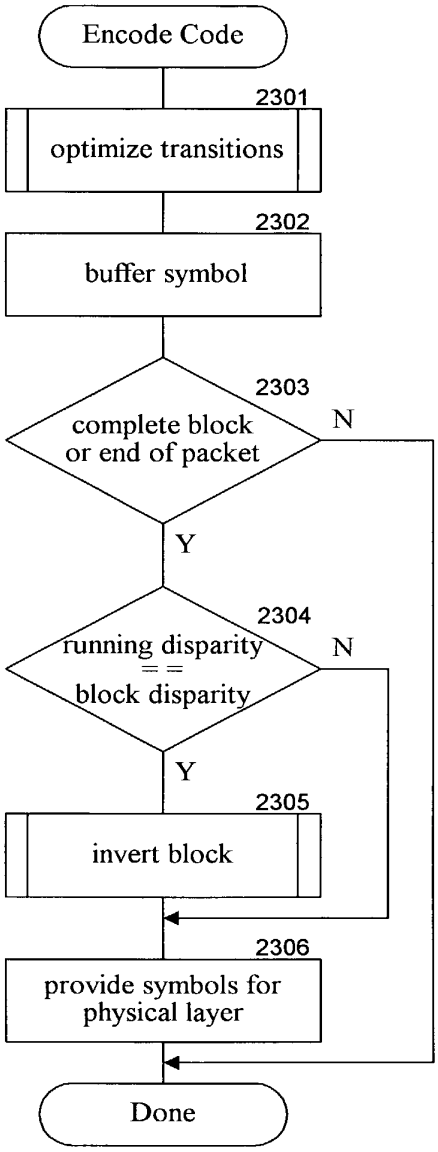

Encode Code
2301
optimize transitions
2302
buffer symbol
2303
complete block or end of packet
N
Y
2304
running disparity == block disparity
N
Y
2305
invert block
2306
provide symbols for physical layer
Done

Fig. 23

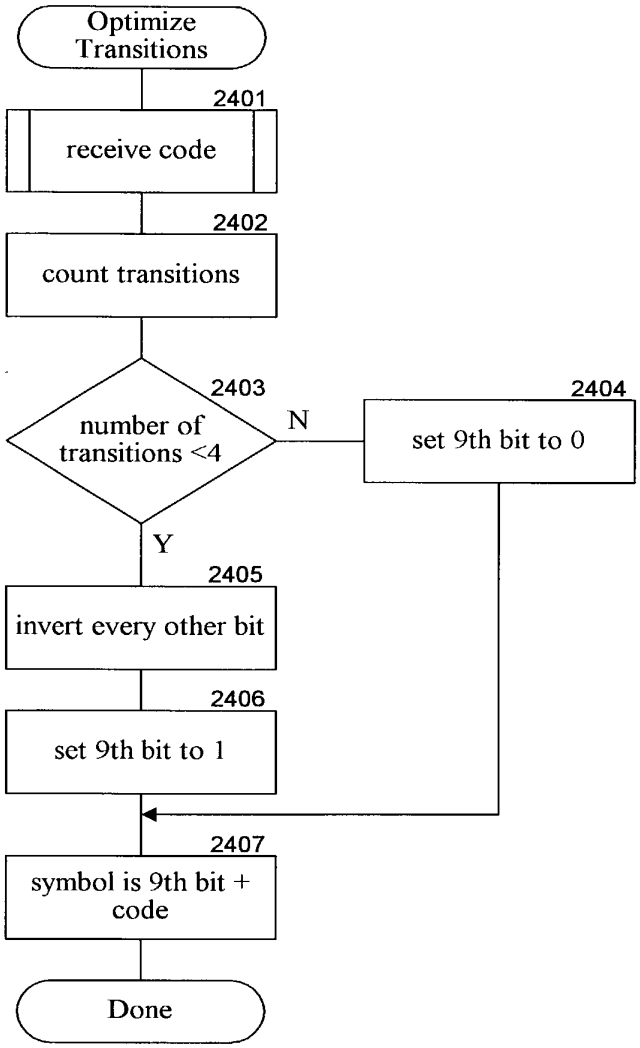

Optimize Transitions
2401
receive code
2402
count transitions
2403
number of transitions <4
N
2404
set 9th bit to 0
Y
2405
invert every other bit
2406
set 9th bit to 1
2407
symbol is 9th bit + code
Done

Fig. 24

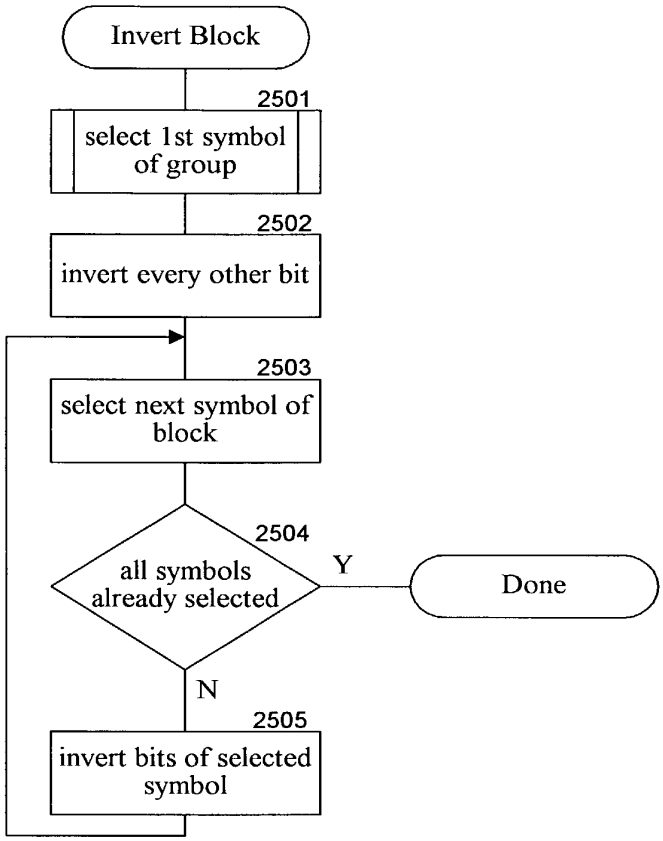

Invert Block
2501
select 1st symbol of group
2502
invert every other bit
2503
select next symbol of block
2504
all symbols already selected
Y
Done
N
2505
invert bits of selected symbol

Fig. 25

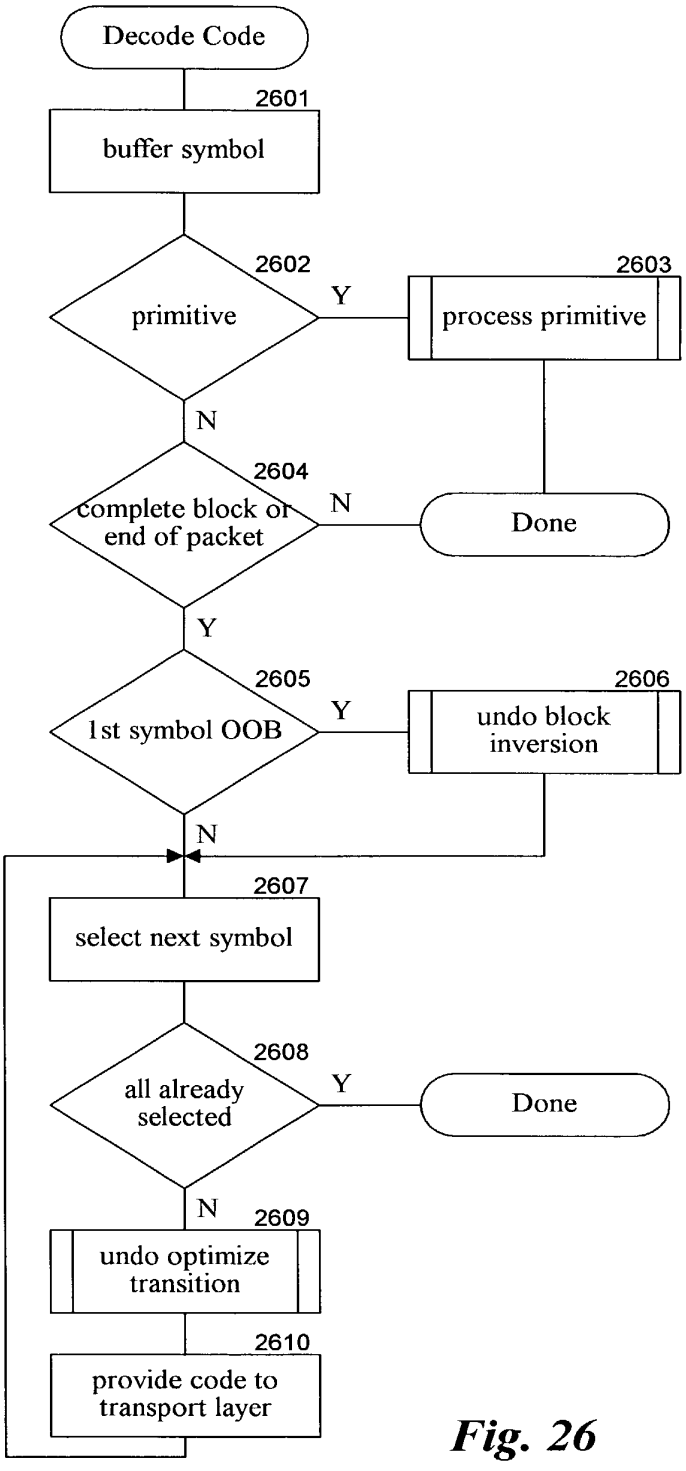

Decode Code
2601
buffer symbol
2602
primitive
Y
2603
process primitive
N
2604
complete block or end of packet
N
Done
Y
2605
1st symbol OOB
Y
2606
undo block inversion
N
2607
select next symbol
2608
all already selected
Y
Done
N
2609
undo optimize transition
2610
provide code to transport layer

Fig. 26

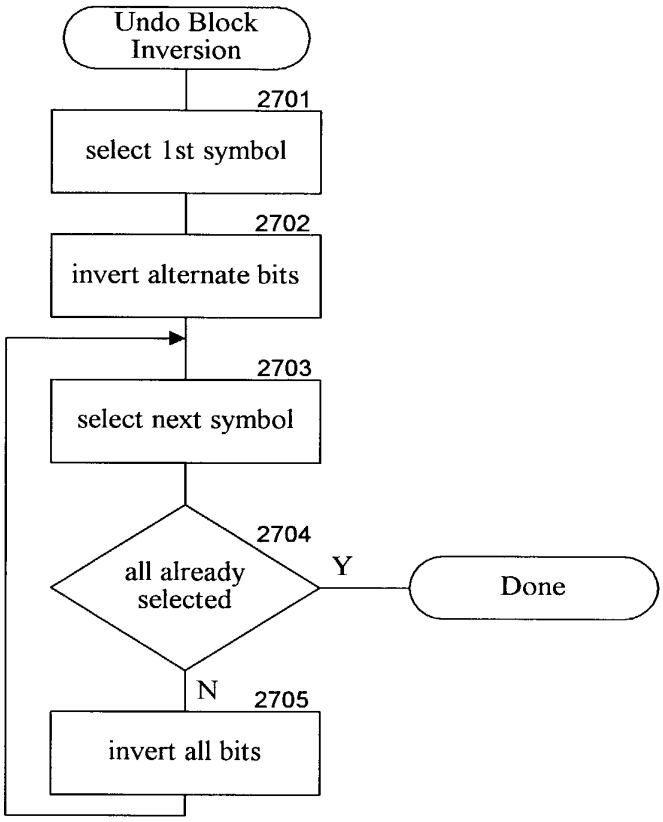

Undo Block Inversion
2701
select 1st symbol
2702
invert alternate bits
2703
select next symbol
2704
all already selected
Y
Done
N
2705
invert all bits

Fig. 27

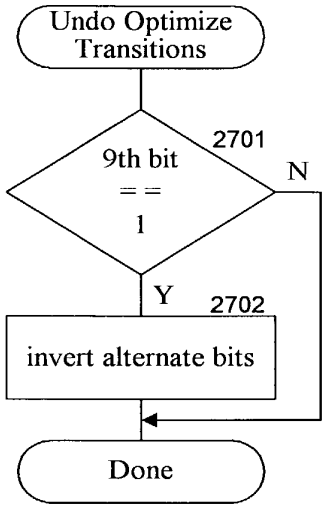

Undo Optimize Transitions
9th bit == 1
2701
N
Y
2702
invert alternate bits
Done

Fig. 28

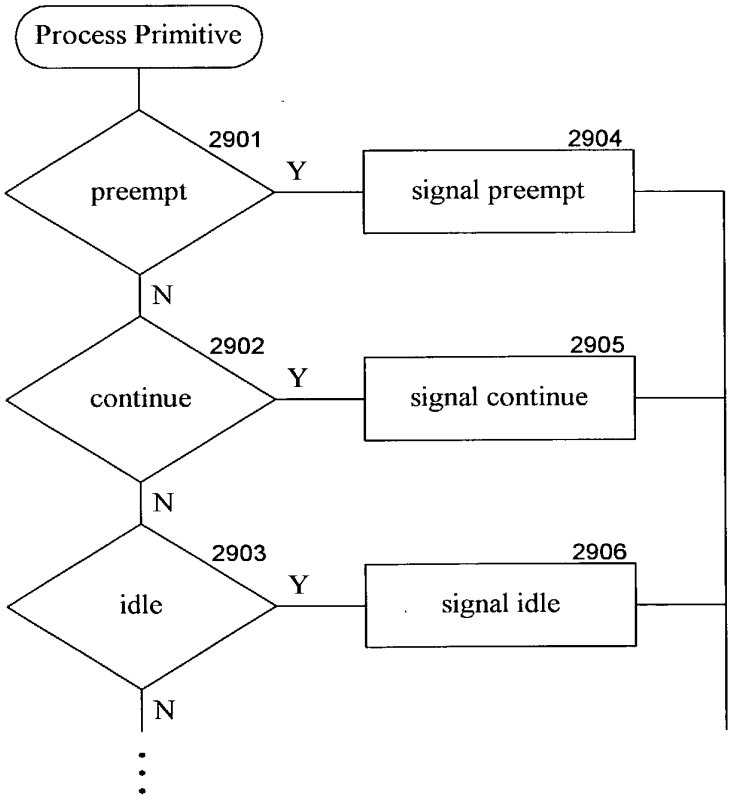

Process Primitive
2901
preempt
Y
2904
signal preempt
N
2902
continue
Y
2905
signal continue
N
2903
idle
Y
2906
signal idle
N

Fig. 29

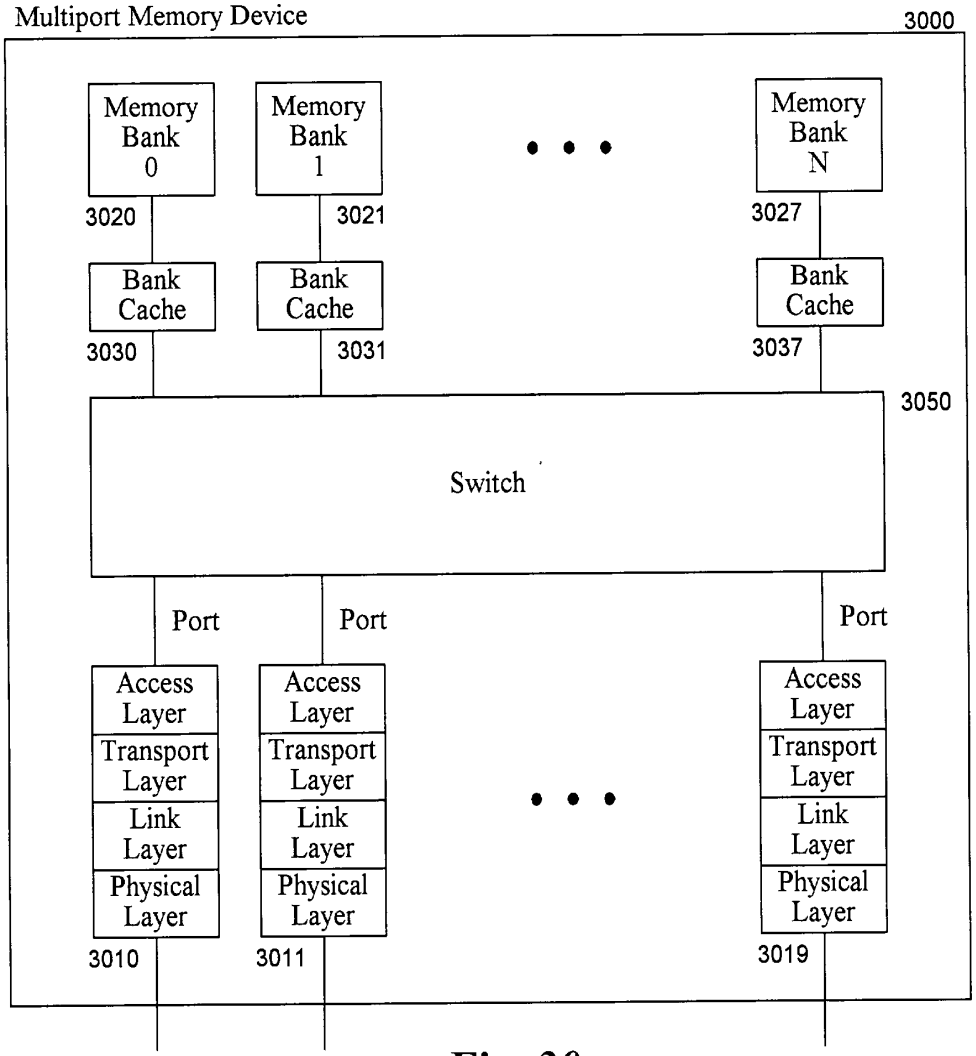


Fig. 30

LENOVO EXHIBIT 1002 - 183/553

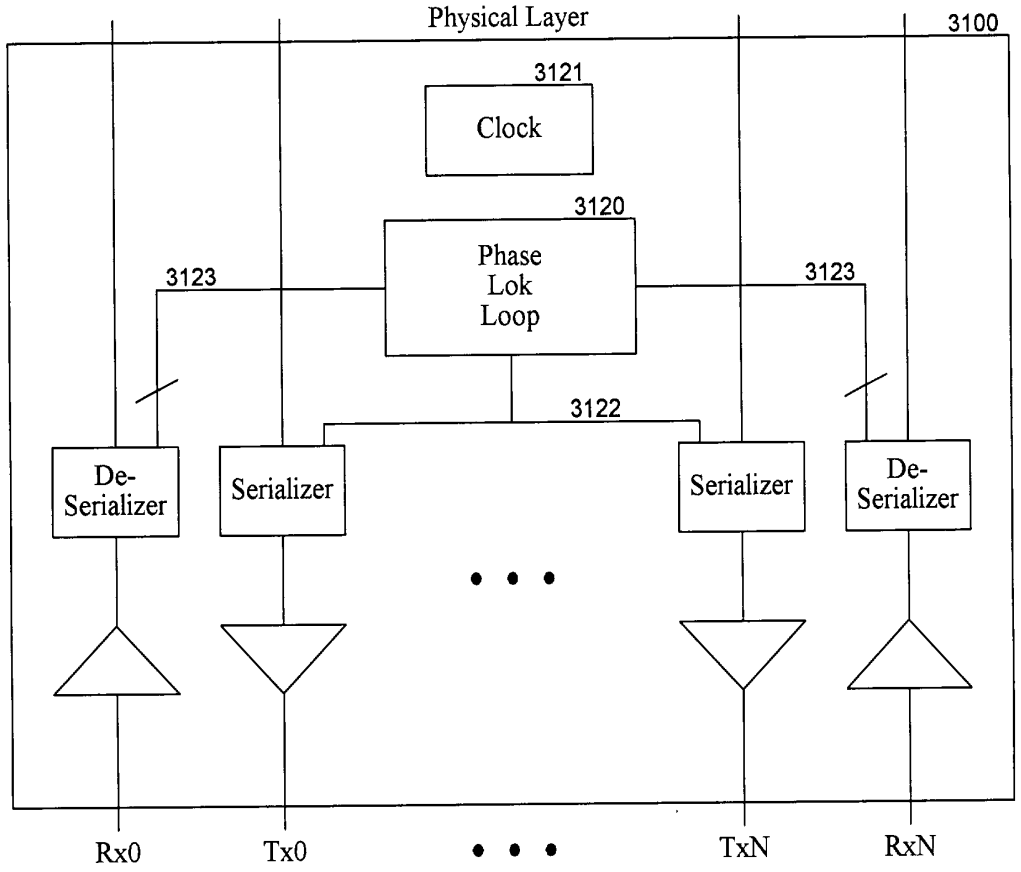


Fig. 31

LENOVO EXHIBIT 1002 - 184/553

Input Queue 3201

Port	R/W	Address	Data
3	R	1000	
4	W	4000	10....1
3	W	1000	111...0
3	R	2000	
	⋮		

Output Queue 3202

Valid	Port	Data
1	3	11...0
0		
0		
1	3	101...1
	⋮	

Fig. 32

LENOVO EXHIBIT 1002 - 185/553

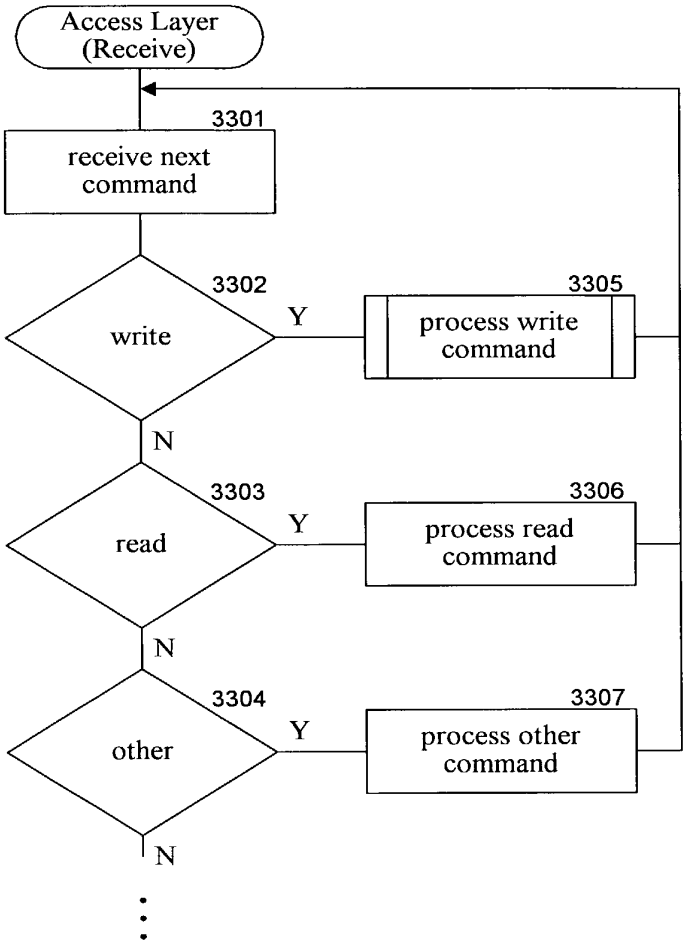

Access Layer
(Receive)
3301
receive next
command
3302
write
Y
3305
process write
command
N
3303
read
Y
3306
process read
command
N
3304
other
Y
3307
process other
command
N

Fig. 33

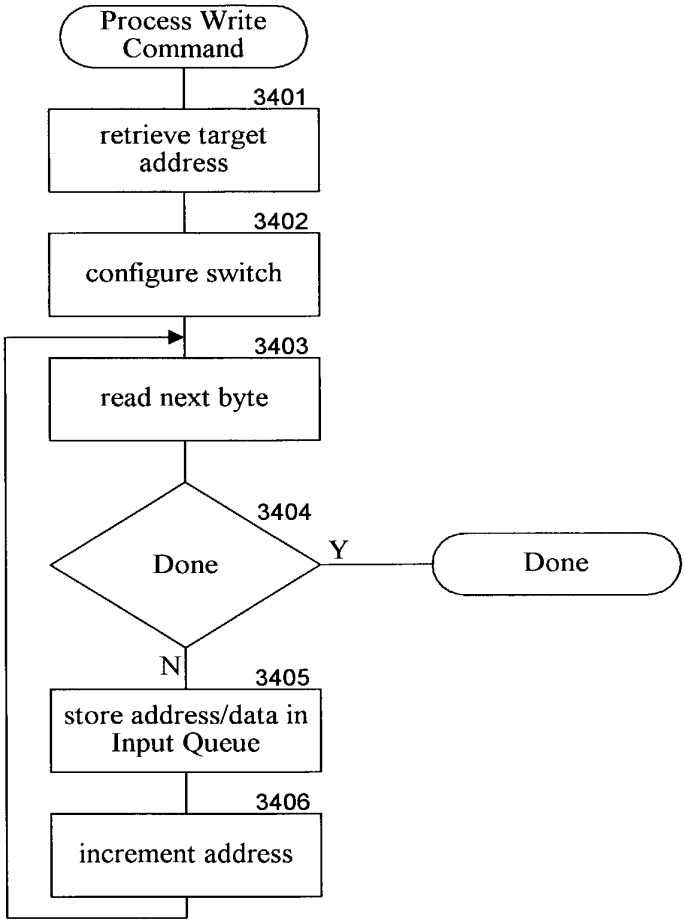

Process Write Command
3401
retrieve target address
3402
configure switch
3403
read next byte
3404
Done
Y
Done
N
3405
store address/data in Input Queue
3406
increment address

Fig. 34

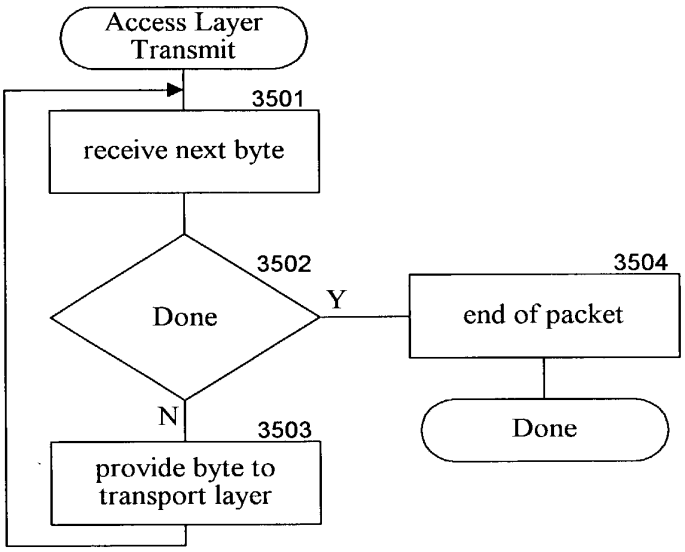

Access Layer Transmit
3501
receive next byte
3502
Done
Y
3504
end of packet
Done
N
3503
provide byte to transport layer

Fig. 35

US 6,094,715

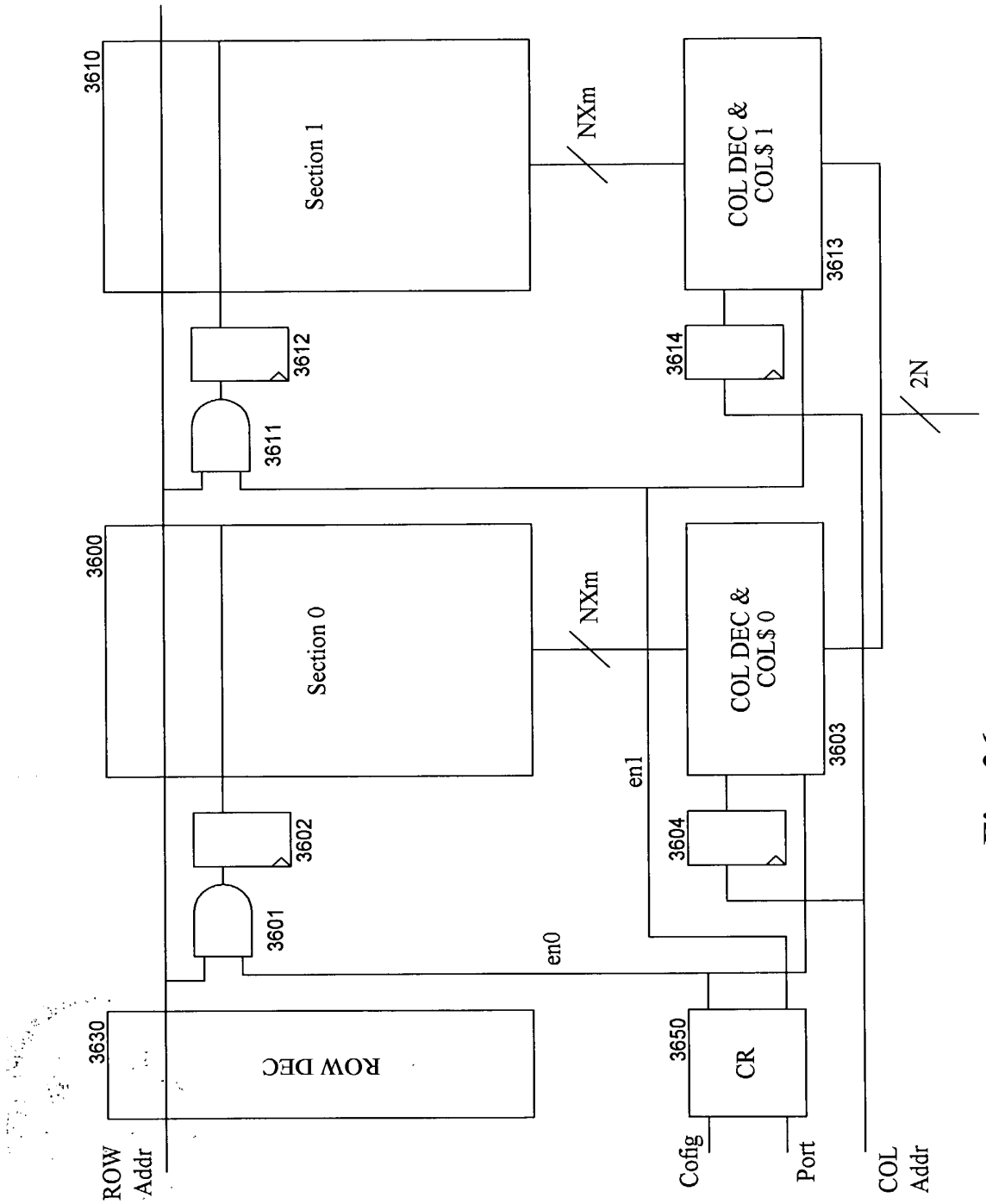
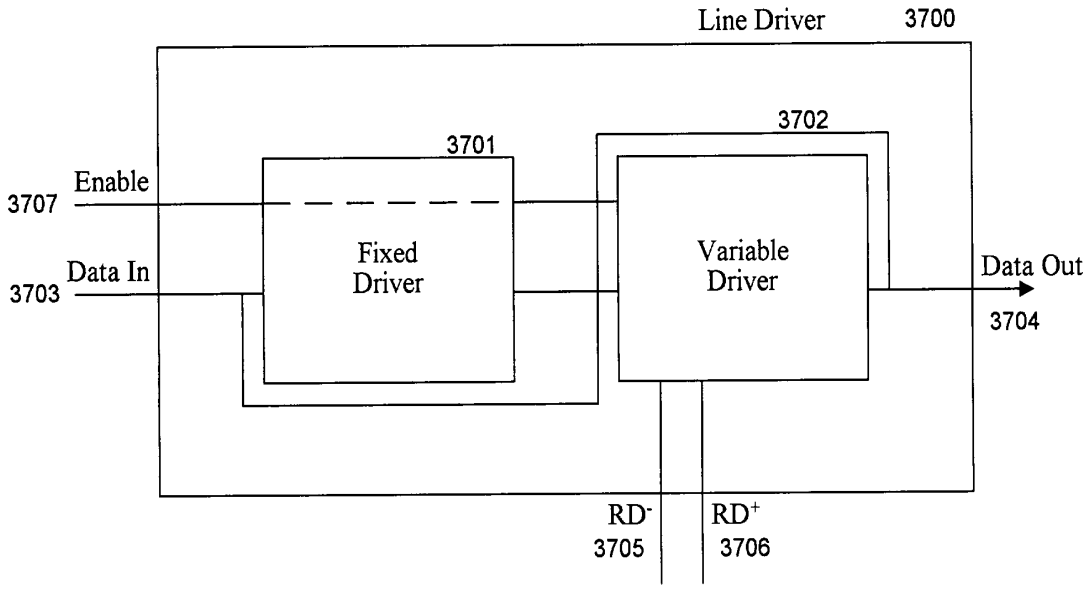


Fig. 36



Variable Driver
$\begin{cases} RD^+ \wedge \overline{DataIn} = \text{pull down} \\ RD^- \wedge DataIn = \text{pull up} \end{cases}$

Fig. 37A

LENOVO EXHIBIT 1002 - 190/553

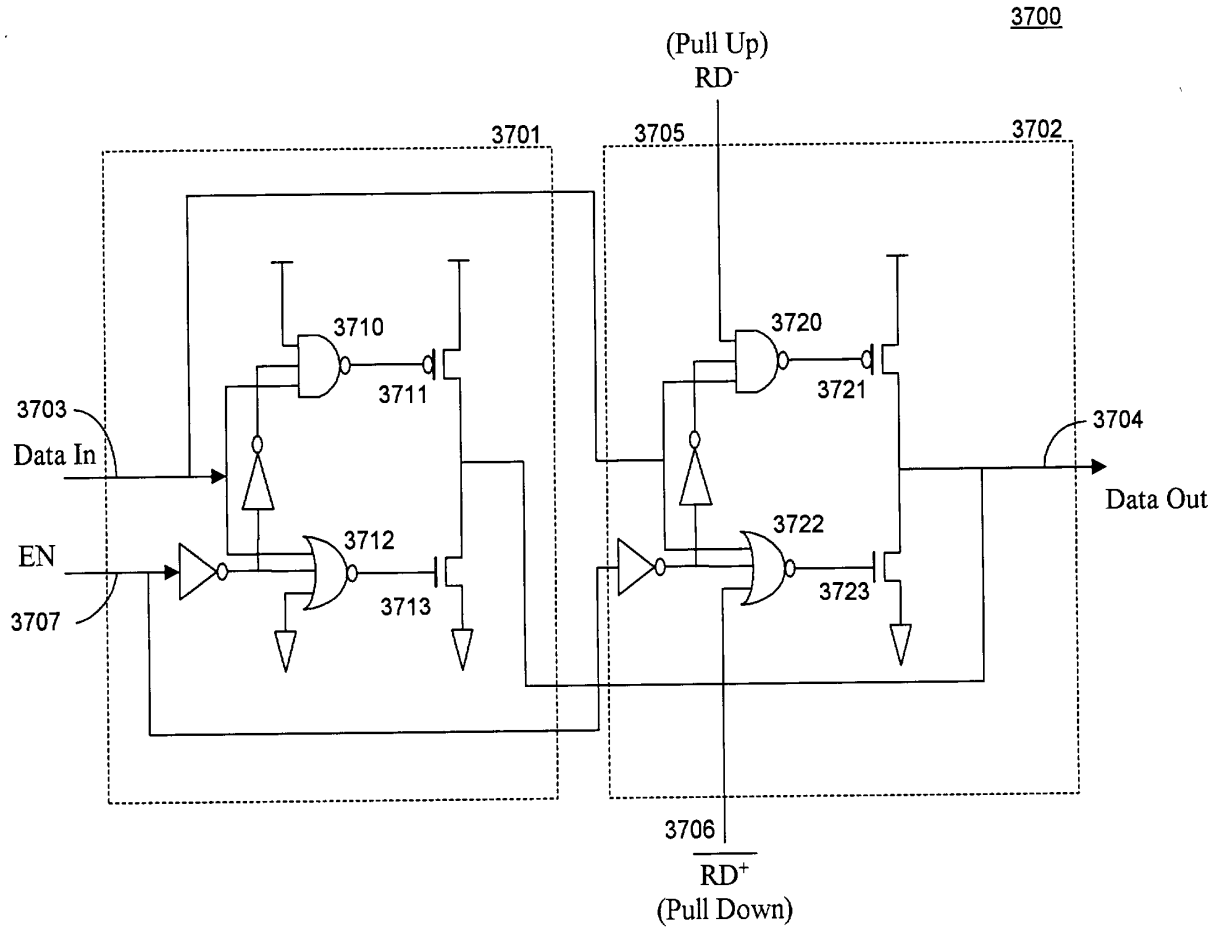


Fig. 37B

LENOVO EXHIBIT 1002 - 191/553

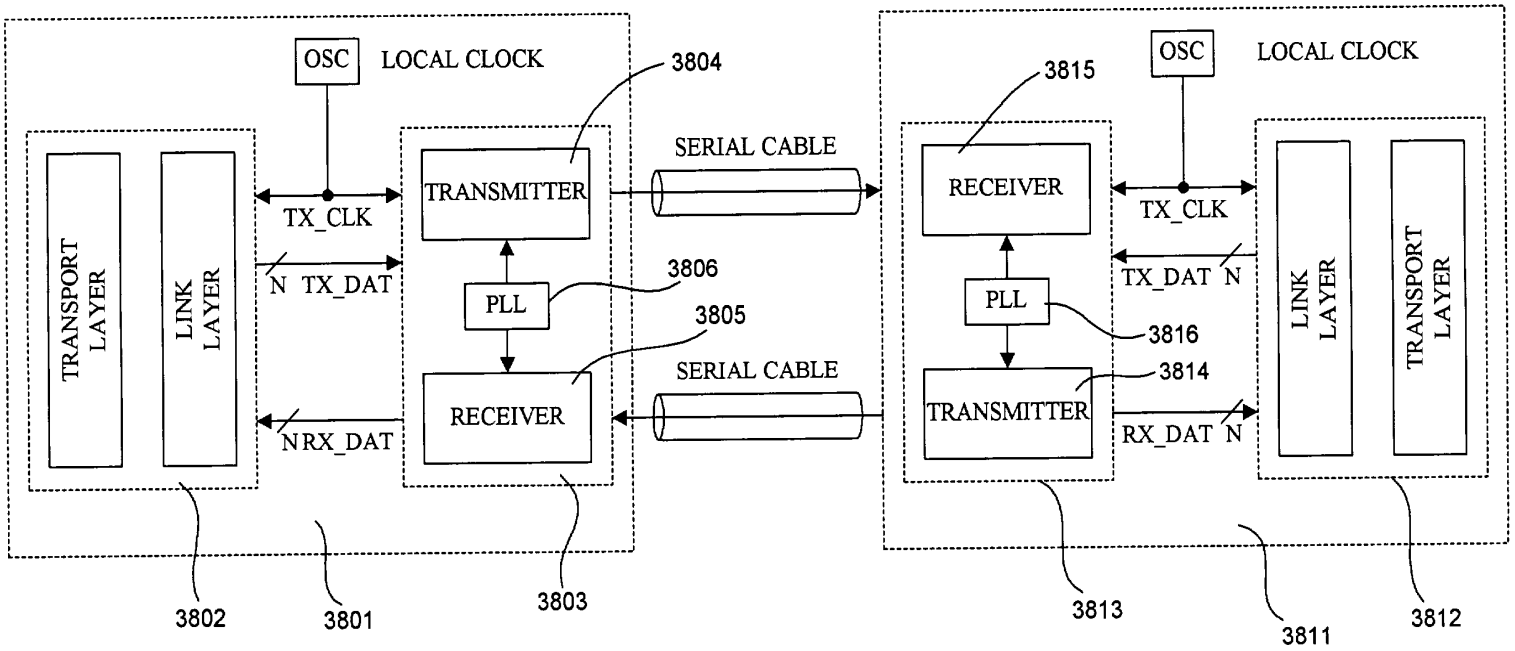


Fig. 38A

LENOVO EXHIBIT 1002 - 192/553

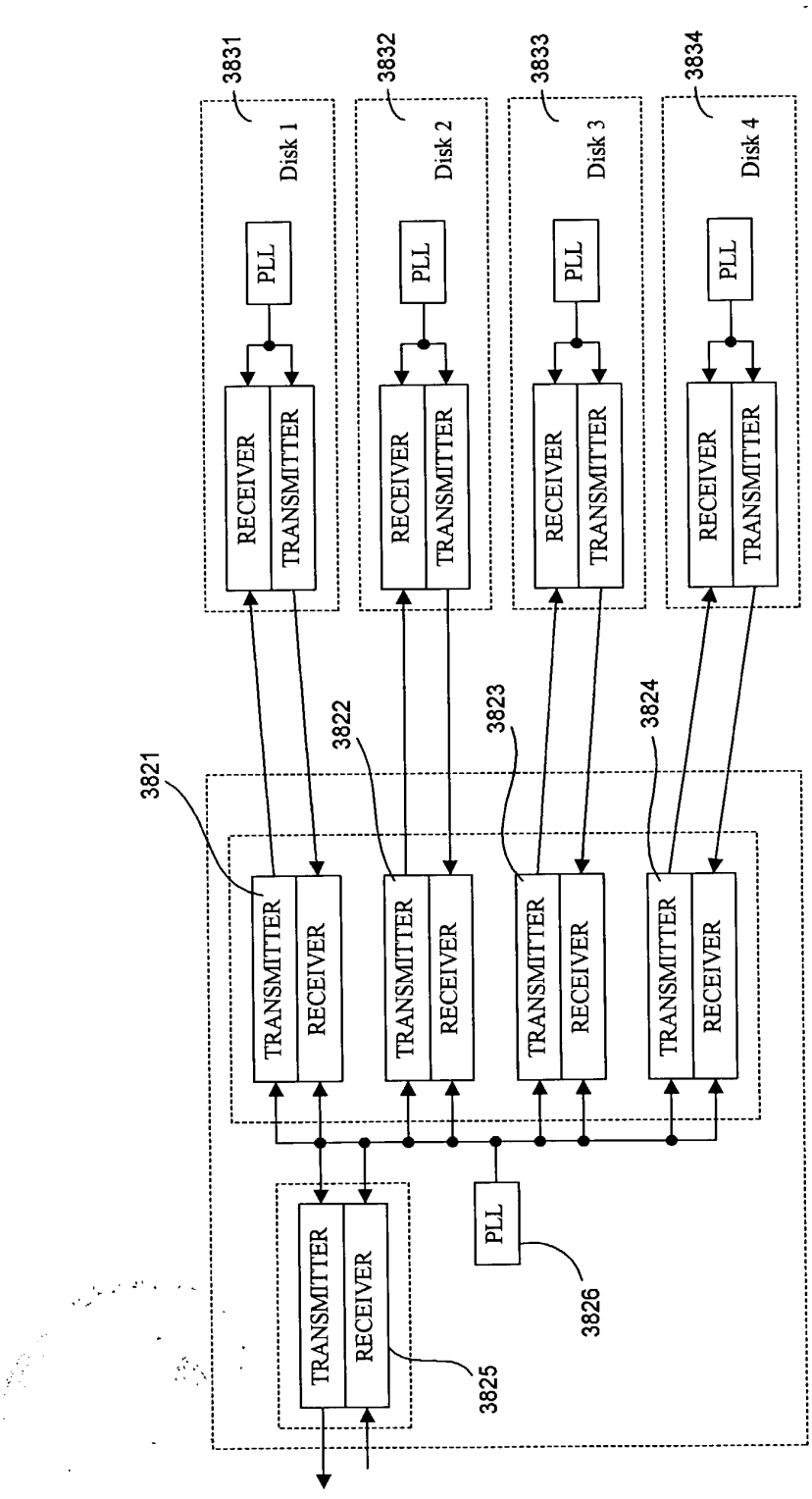

3831
Disk 1
PLL
RECEIVER
TRANSMITTER
3832
Disk 2
PLL
RECEIVER
TRANSMITTER
3833
Disk 3
PLL
RECEIVER
TRANSMITTER
3834
Disk 4
PLL
RECEIVER
TRANSMITTER
3821
3822
3823
3824
TRANSMITTER
RECEIVER
TRANSMITTER
RECEIVER
TRANSMITTER
RECEIVER
TRANSMITTER
RECEIVER
TRANSMITTER
RECEIVER
PLL
3825
3826

Fig. 38B

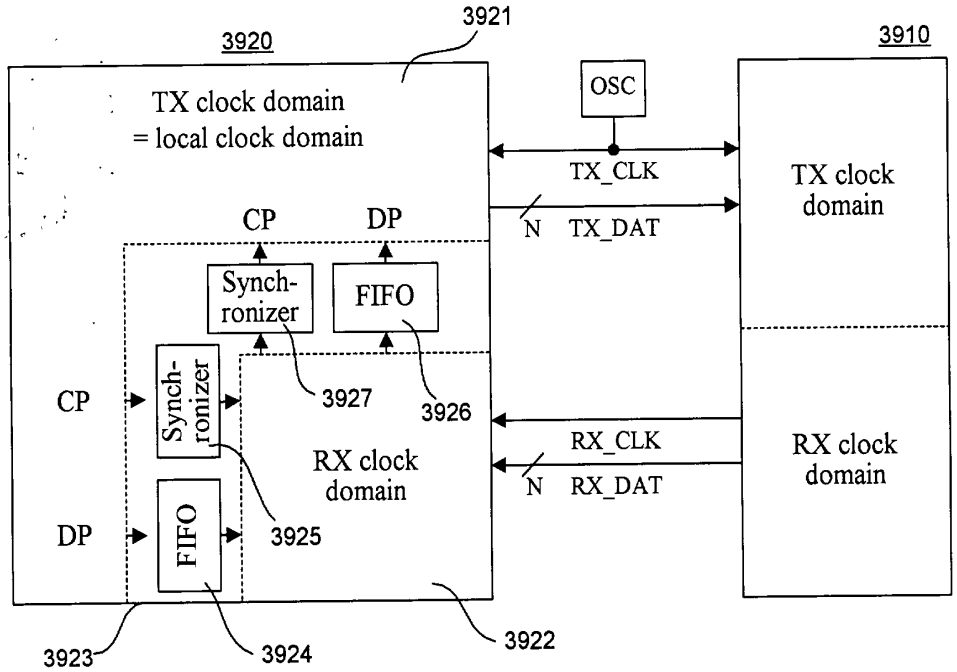


Fig. 39A

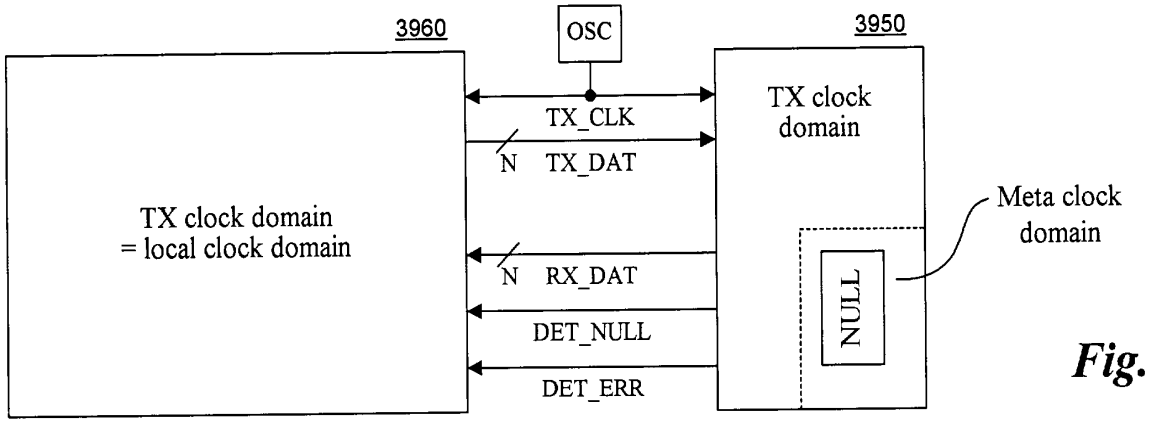


Fig. 39B

LENOVO EXHIBIT 1002 - 194/553

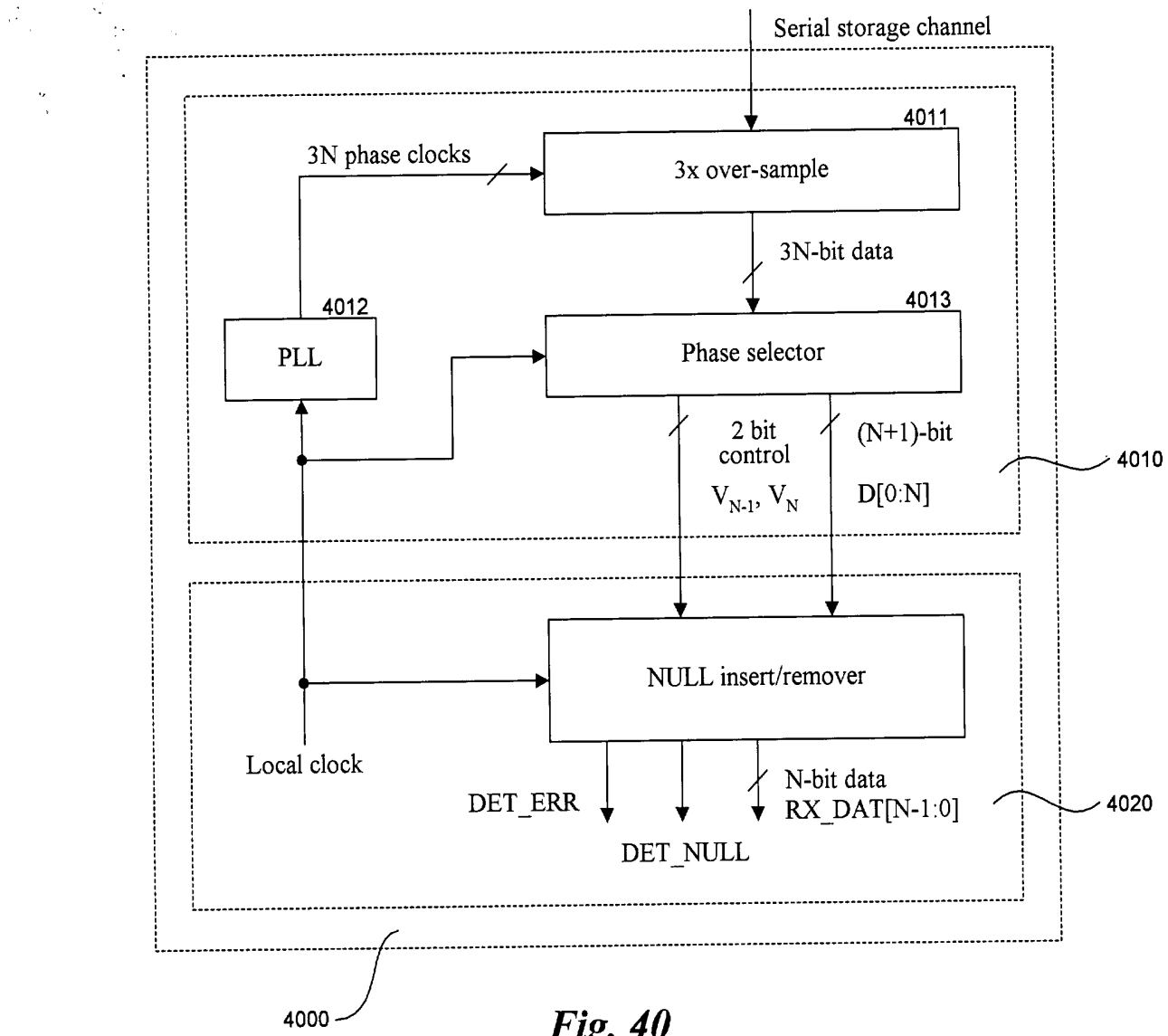


Fig. 40

LENOVO EXHIBIT 1002 - 195/553

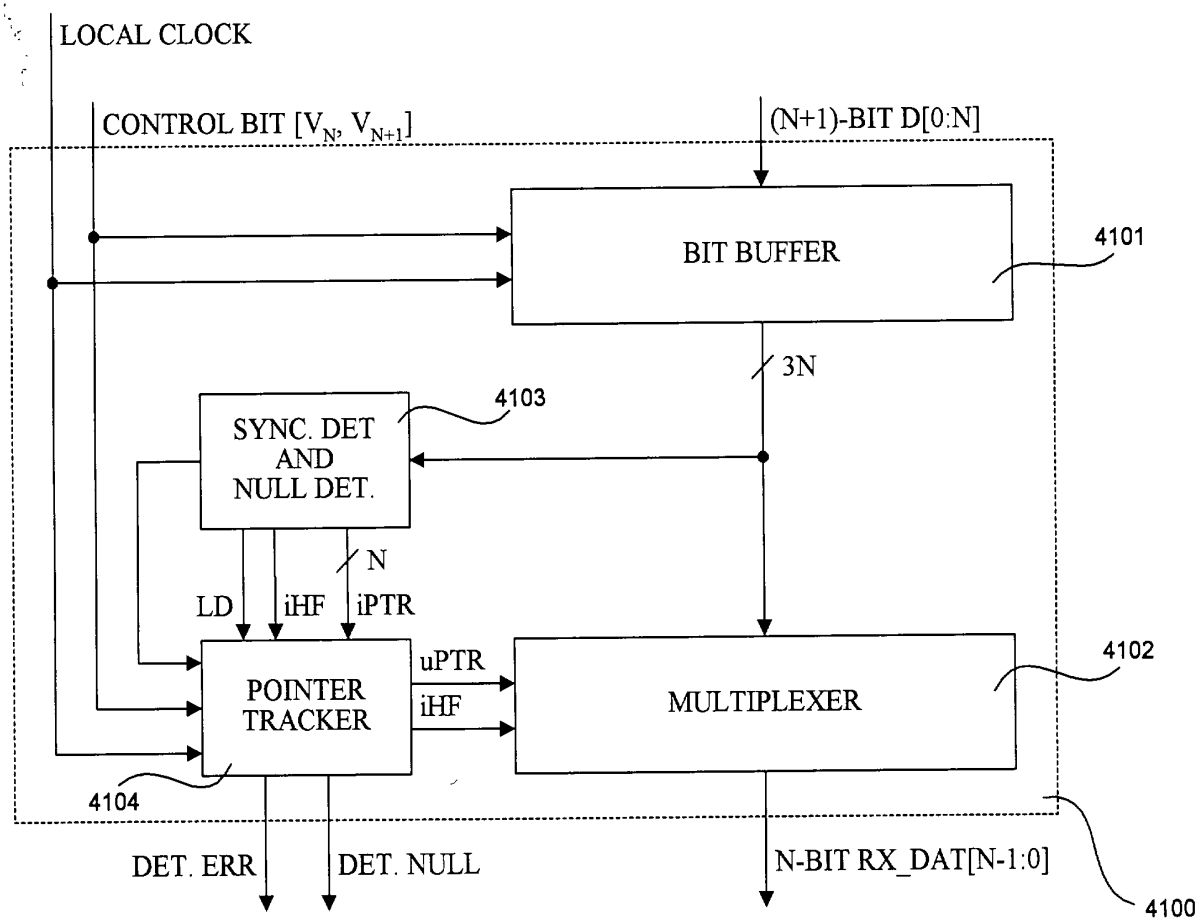


Fig. 41

LENOVO EXHIBIT 1002 - 196/553

LENOVO EXHIBIT 1002 - 197/553

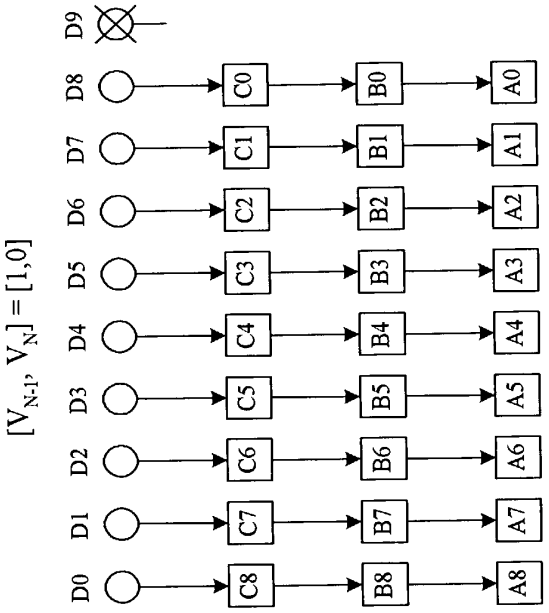


Fig. 42A

US 8,045,625 B2

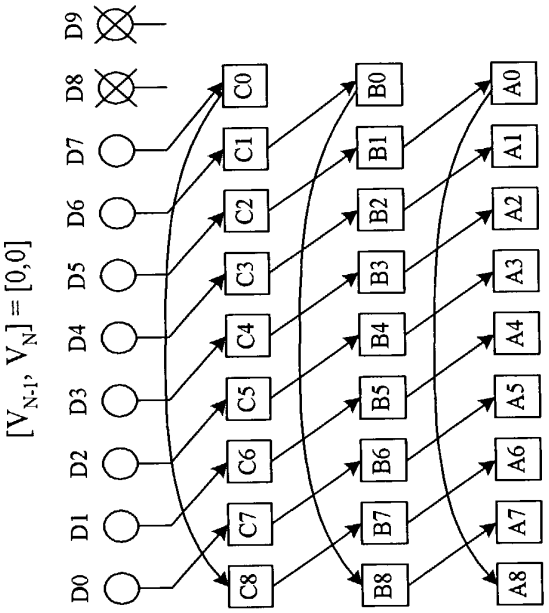


Fig. 42B

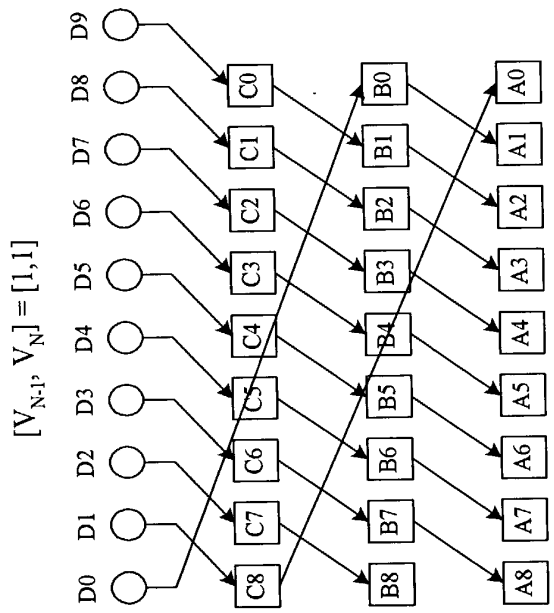

$[V_{N-1}, V_N] = [1,1]$
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
C0
C1
C2
C3
C4
C5
C6
C7
C8
B0
B1
B2
B3
B4
B5
B6
B7
B8
A0
A1
A2
A3
A4
A5
A6
A7
A8

Fig. 42C

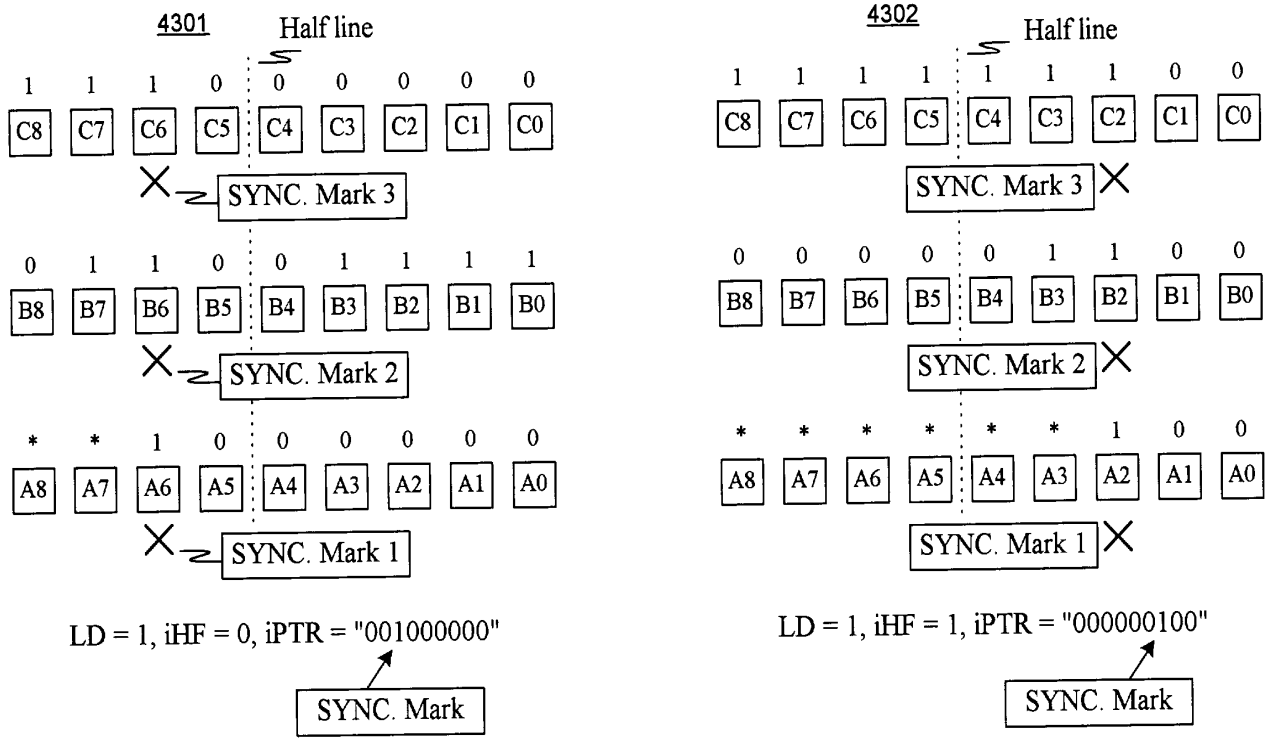
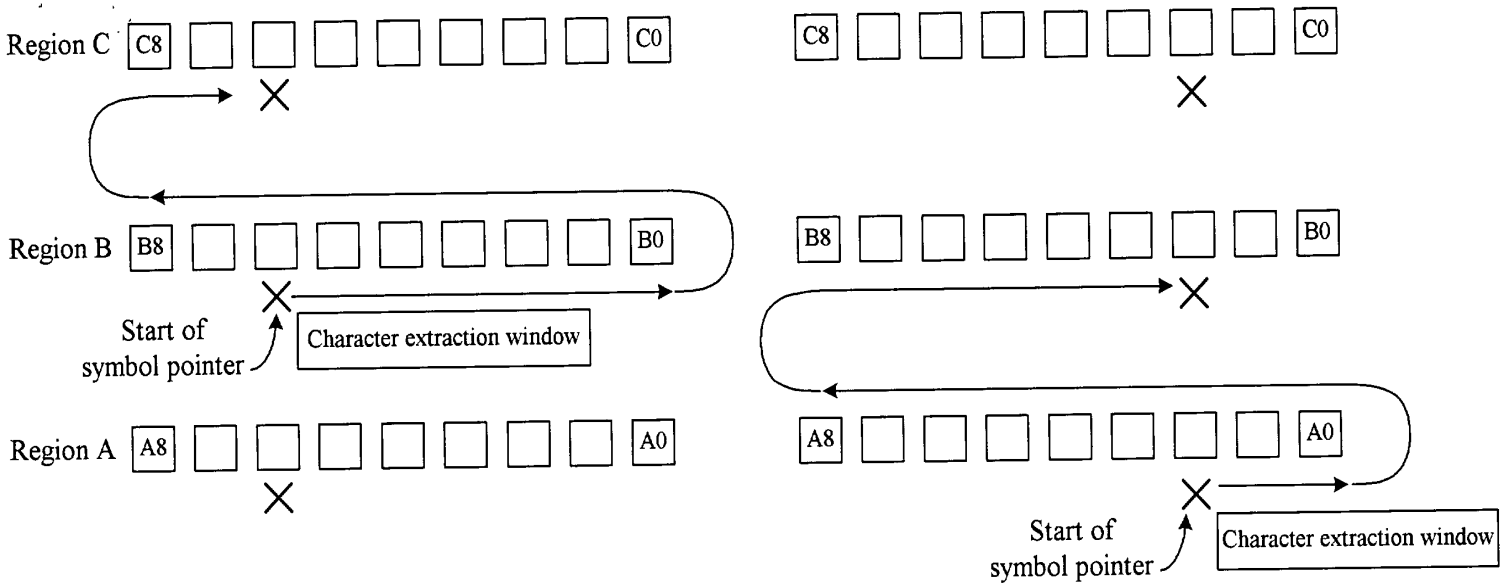


Fig. 43

LENOVO EXHIBIT 1002 - 200/553



LD = 1, iHF = 0, iPTR = "001000000"

LD = 1, iHF = 1, iPTR = "000000100"

Fig. 44

LENOVO EXHIBIT 1002 - 201/553

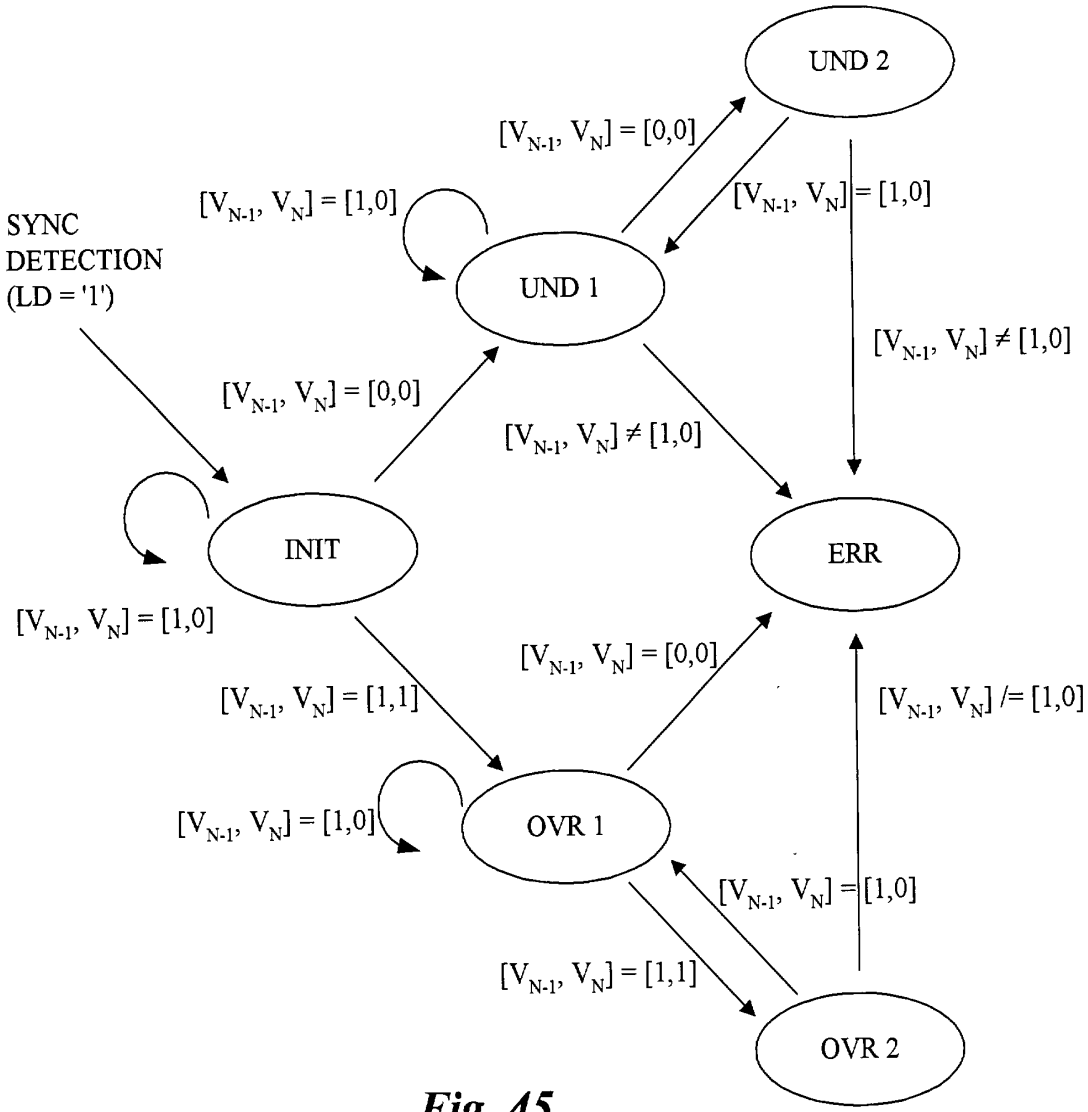


Fig. 45

LENOVO EXHIBIT 1002 - 202/553

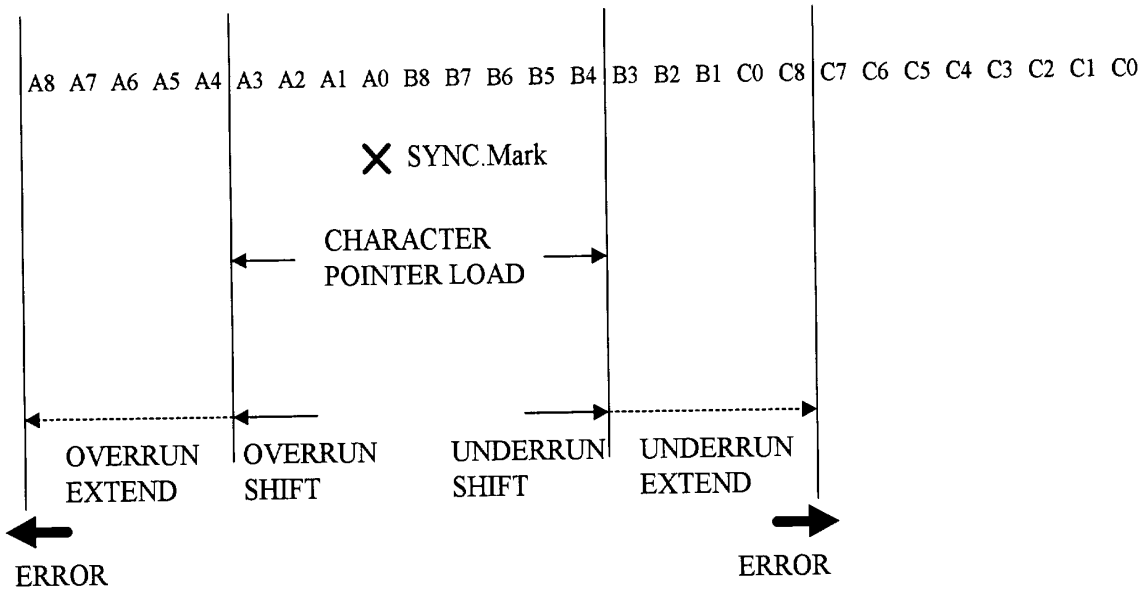


Fig. 46

LENOVO EXHIBIT 1002 - 203/553

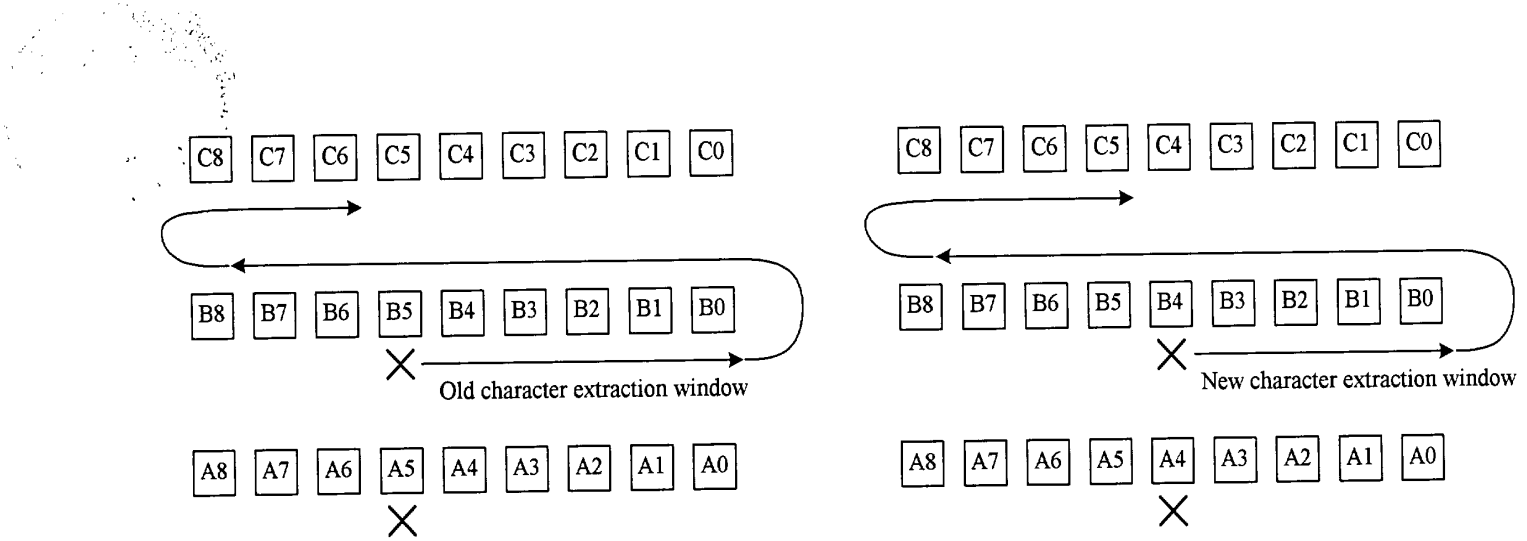


Fig. 47A

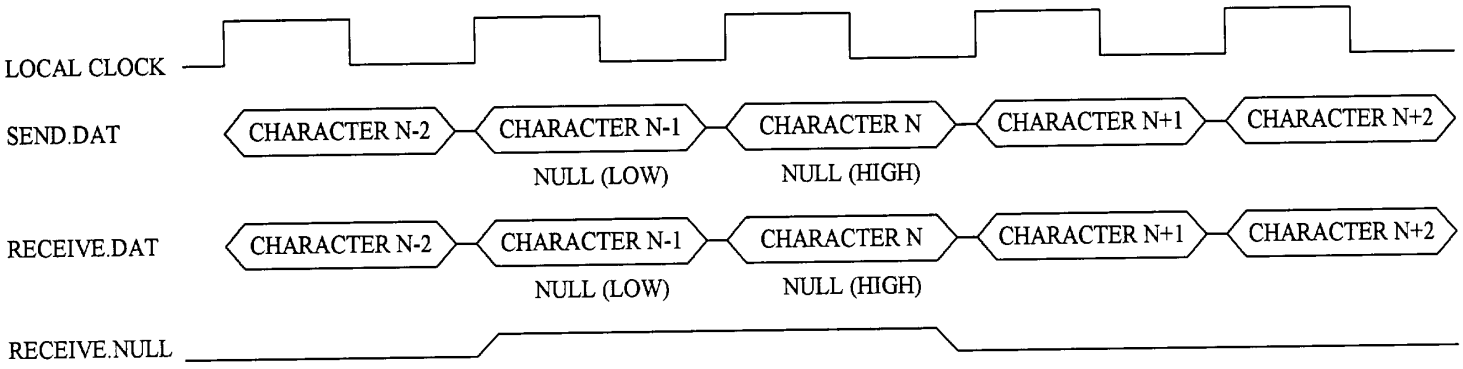


Fig. 47B

LENOVO EXHIBIT 1002 - 204/553

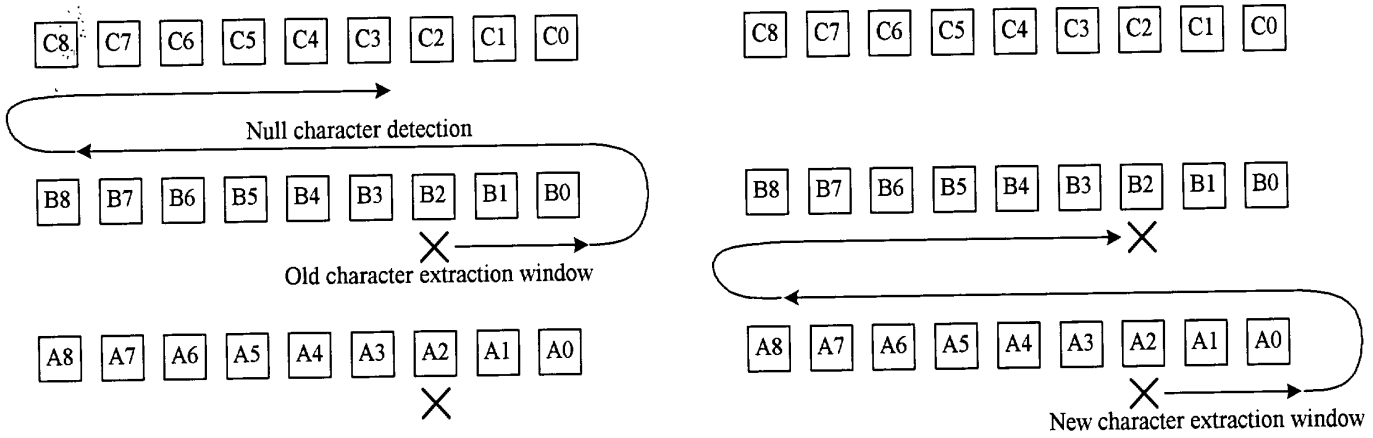


Fig. 48A

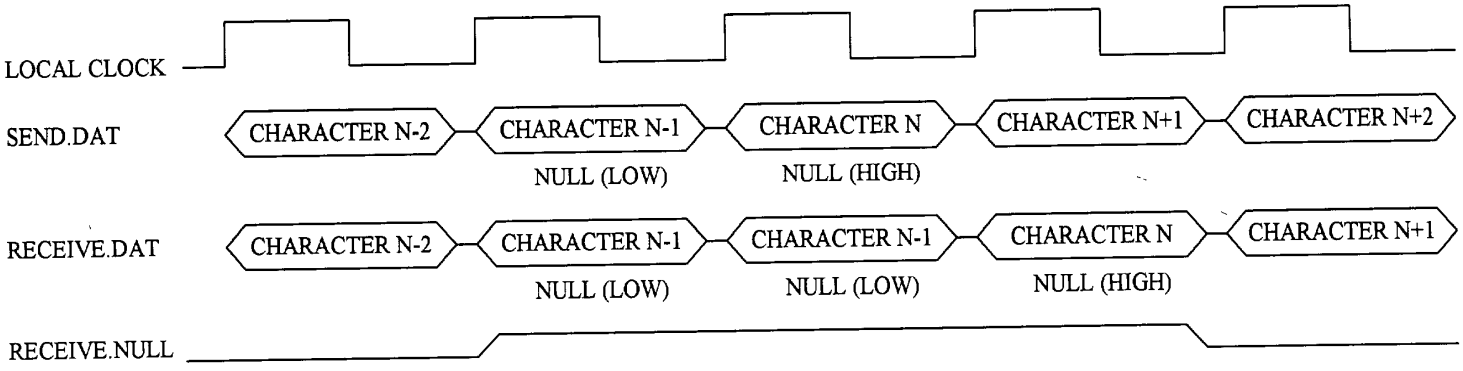


Fig. 48B

LENOVO EXHIBIT 1002 - 205/553

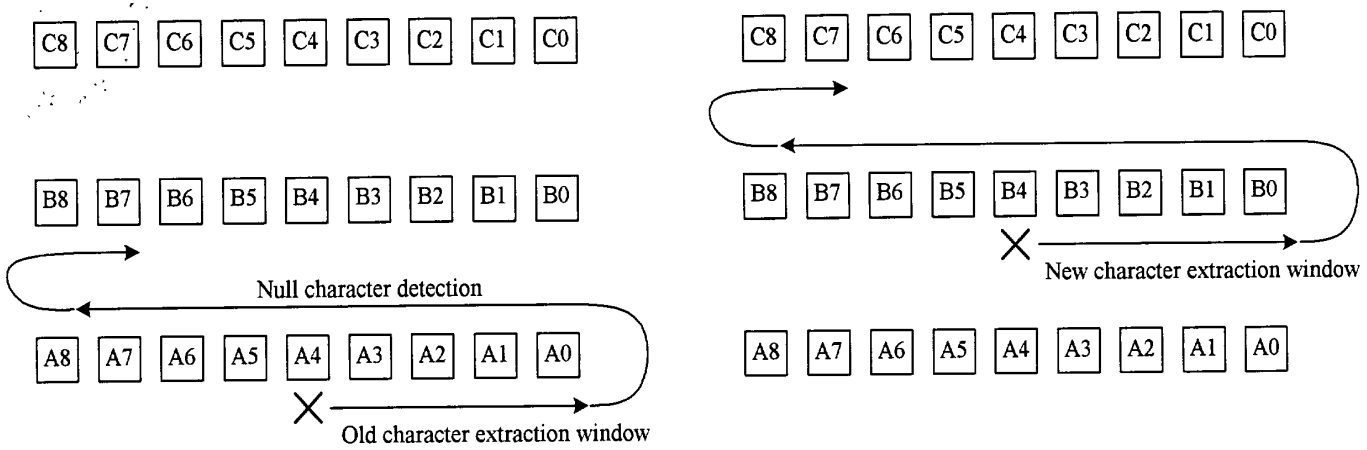


Fig. 49A

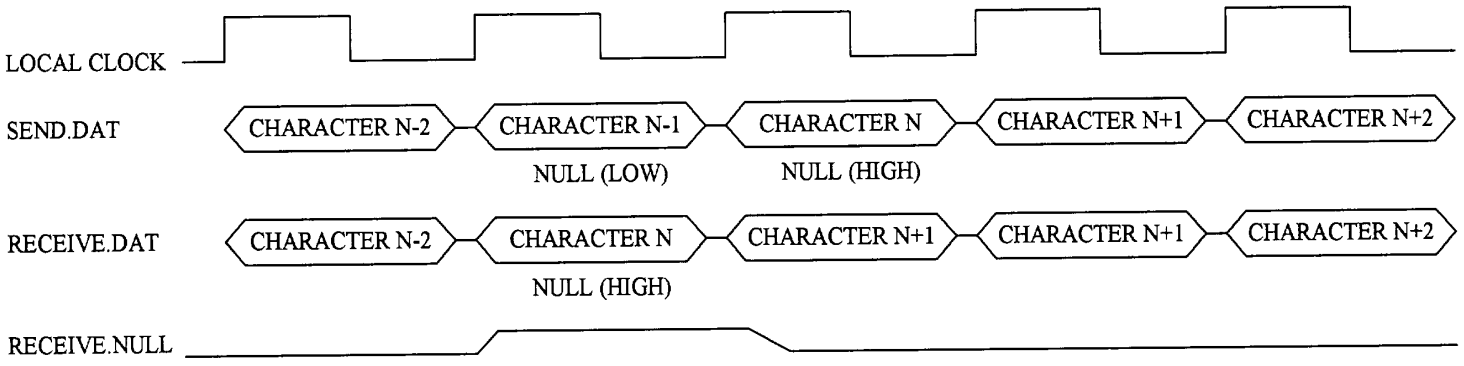


Fig. 49B

LENOVO EXHIBIT 1002 - 206/553

OIPE
MAY 3 0 2002
JC48
PATENT & TRADEMARK OFFICE

DECLARATION

As the below-named inventors, we declare that:

Our residences, post office addresses, and citizenships are as stated below under our names.

We believe we are the original, first, and joint inventors of the subject matter claimed and for which a patent is sought on the invention entitled "METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS" in the foregoing specification and claims, which claims the benefit of U.S. Provisional Application No. 60/252,724, filed November 22, 2000.

We have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to above.

We acknowledge our duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. § 1.56(a).

We further declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that the making of willfully false statements and the like is punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from this patent application.

LENOVO EXHIBIT 1002 - 207/553

Yeshik Shin

Date 11/2/2001

Residence : City of Sunnyvale
State of California

Citizenship : Korea

P.O. Address : 1035 Aster Avenue, #1116
Sunnyvale, California 94086

LENOVO EXHIBIT 1002 - 208/553

David D. Lee

Date 10-29-01

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State of California

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P.O. Address : ~~3715 Redwood Circle~~ 4180 Wallis Court DL
Palo Alto, California 94306

LENOVO EXHIBIT 1002 - 209/553

Deog-Kyoon Jeong

Date Oct. 31, 2001

Residence : City of Seoul
Country of Korea

Citizenship : Korea

P.O. Address : San 56-1 Shinlim-Dong, Kwanak-Gu
Seoul, Korea 15174-2

Shing Kong

Date 11/6/2001

Residence : City of Brisbane
State of California

Citizenship : United States of America

P.O. Address : 112 Rock Wren Lane
Brisbane, California 94005

[redacted]

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, Washington, DC 20231.

5/24/02 Jeanne Connelly
Date

OIPE
MAY 30 2002
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Yeshik Shin et al.
Application No.	:	10/045,625 Confirmation No.: 1053
Filed	:	November 7, 2001
For	:	METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS

Docket No.	:	371798018US
Date	:	May 24, 2002

Commissioner for Patents
Washington, DC 20231

TRANSMITTAL OF FORMAL DRAWINGS

Sir:

Enclosed please find 59 sheets of formal drawings (Figures 1-49B) for the above-identified application.

Respectfully submitted,
Perkins Coie LLP

Maurice J. Pirio
Registration No. 33,273

MJP:jc

Enclosures:
59 Sheets of Drawings

PERKINS COIE LLP
P.O. Box 1247
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FAX: (206) 583-8500

LENOVO EXHIBIT 1002 - 212/553

T.D

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, Washington, DC 20231.

5/24/02 — Jeanne Connelly

Date — Jeanne Connelly

MAY 30 2002 PATENT & TRADEMARK OFFICE JC48

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	:	Yeshik Shin et al.
Application No.	:	10/045,625 Confirmation No.: 1053
Filed	:	November 7, 2001
For	:	METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS
Docket No.	:	371798018US
Date	:	May 24, 2002

X6

Commissioner for Patents
Washington, DC 20231

PETITION FOR EXTENSION OF TIME UNDER 37 CFR. § 1.136(a)

Sir:

Applicants herewith petition the Commissioner of Patents under 37 CFR § 1.136(a) for a one-month extension of time for filing the response to the Notice to File Missing Parts dated February 26, 2002, from April 26, 2002 to May 26, 2002. A check is enclosed which includes the $110.00 fee. Any deficiency or overpayment should be charged or credited to Deposit Account No. 50-0665. This petition is being submitted in triplicate.

Respectfully submitted,
Perkins Coie LLP

Maurice J. Pirio
Registration No. 33,273

P.O. Box 1247
Seattle, Washington 98111-1247
(206) 583-8888
Fax: (206) 583-8500

05/31/2002 CCHAU1 00000138 10045625
01 FC:115 110.00 OP

CV

LENOVO EXHIBIT 1002 - 213/553

OIPE JC48 MAY 30 2002 PATENT & TRADEMARK OFFICE

OIPE JC48 MAY 30 2002 PATENT & TRADEMARK OFFICE

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Yeshik Shin et al.

Application No. : 10/045,625 Confirmation No.: 1053

Filed : November 7, 2001

For : METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS

Docket No. : 371798018US

Date : May 24, 2002

Commissioner for Patents
Washington, DC 20231

AUTHORIZATION FOR EXTENSIONS OF TIME UNDER 37 C.F.R. § 1.136(A)(3)

Sir:

With respect to the above-identified application, the Commissioner is authorized to treat any concurrent or future reply requiring a petition for an extension of time under 37 C.F.R. § 1.136(a)(3) for its timely submission as incorporating a petition therefor for the appropriate length of time. The Commissioner is also authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account No. 50-0665.

Date May 24, 2002

Maurice J. Pirio
Registration No. 33,273

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(206) 583-8888
FAX: (206) 583-8500

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JUL 0 3 2003
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PTO/SB/36 (05-03) (MODIFIED)
Approved for use through 04/30/2003. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

NOTICE OF RESCISSION OF PREVIOUS NONPUBLICATION REQUEST

(35 U.S.C. 122(b)(2)(B)(ii))
AND, IF APPLICABLE,

NOTICE OF FOREIGN FILING

(35 U.S.C. 122(b)(2)(B)(iii))

Send completed form to:
Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
FAX: (703) 305-8568

Application Number	10/045,625
Filing Date	11/07/2001
First Named Inventor	Yeshik Shin
Title	METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYCHRONIZATION SYMBOLS
Attorney Docket Number	594728818US
Group Art Unit	2661
Examiner	

A request that the above-identified application not be published under 35 U.S.C. 122(b) (nonpublication request) was included with the above-identified application on filing pursuant to 35 U.S.C. 122(b)(2)(B)(i). I hereby **rescind** the previous nonpublication request.

☒ I hereby notify the Director under 35 U.S.C. 122(b)(2)(B)(iii) of a foreign or international filing. This notice is being provided later than forty-five **(45)** days after the date of such foreign or international filing. A petition to revive under 37 CFR 1.137(b) is enclosed. See 37 CFR 1.137(f).

*If a notice of subsequent foreign or international filing required by 35 U.S.C. 122(b)(2)(B)(iii) and 37 CFR 1.213(c) was not filed within forty-five **(45)** days after the date of filing of the foreign or international application, the application is ABANDONED, and a petition to revive under 37 CFR 1.137(b) is required. See 37 CFR 1.137(f).*

July 3, 2003
Date

Maurice J Pirio
Signature

206-583-8548
Telephone Number

Maurice J. Pirio - Reg. No. 33,273
Typed or printed name

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JUL 1 0 2003
OFFICE OF PETITIONS

This request must be signed in compliance with 37 CFR 1.33(b).

If information or assistance is needed in completing this form, please contact the Pre-Grant Publication Division at (703) 605-4283 or by e-mail at PGPub@USPTO.gov.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as Express Mail in an envelope addressed to: Mail Stop Petition, Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or facsimile ((703) 305-8568) transmitted to the U.S. Patent and Trademark Office on the date shown below.

Name (Print/Type)	Douglas A. Gow		
Signature		*Date*	7/3/03

Burden Hour Statement: This collection of information is required by 37 CFR 1.213(b). The information is used by the public to rescind a previously filed request that an application not be published under 35 U.S.C. 122(b) (and the PTO to process that rescission). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 6 minutes to complete. This time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop PG Pub, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

[90020-0018/2nd rescind non-pub.doc]

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JUL 03 2003
PATENT & TRADEMARK OFFICE
JC95

07-07-03

#1 DAC

Attorney Docket No.: 594728818US
Express Mail Label EV 335524151 US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	SHIN, ET AL.	EXAMINER:	
APPLICATION NO.:	10/045,625	ART UNIT:	2661
FILED:	11/07/2001	CONF. NO:	1053

FOR: METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYCHRONIZATION SYMBOLS

Petition to Revive Unintentionally Abandoned Application Under 37 C.F.R. § 1.137(b)

RECEIVED
JUL 10 2003
OFFICE OF PETITIONS

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

1. The applicants hereby petition for revival of the above-identified application. An international application directed to an invention disclosed in the above-referenced application was filed with the U.S. Receiving Office on November 21, 2001. On January 7, 2002, applicants filed a Request to Rescind Previous Nonpublication Request under 35 U.S.C. 122(b)(2)(B)(ii). However, it is our understanding that the United States Patent and Trademark Office has taken the position that the application became abandoned for failure to concurrently file a Notice of Foreign Filing in compliance with 35 U.S.C. 122(b)(2)(B)(iii).

2. Notice Under 37 C.F.R. § 1.137(b)(1)

   Enclosed herewith is a Notice of Rescission of Previous Nonpublication Request and Notice of Foreign Filing in compliance with 35 U.S.C. 122(b)(2)(B)(iii). An international application directed to an invention disclosed in the above-referenced application was filed with the U.S. Receiving Office on November 21, 2001.

3. Fee Under 37 C.F.R. § 1.137(b)(2)

   Enclosed is a check covering the fee of $1300.00 under 37 C.F.R. § 1.17(m).

4. Statement Under 37 C.F.R. § 1.137(b)(3)

   The entire delay in filing the required Notice until the filing of a grantable petition pursuant to 37 C.F.R. § 1.137(b) was unintentional.

07/09/2003 CNGUYEN 00000142 10045625
01 FC:1453 1300.00 OP

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5. Duration of Abandonment (1203 OG 86-87, Oct. 21, 1997)

☒ This petition is being filed within 3 months of the date on which the Office clarified its position that a Request to Rescind Previous Nonpublication Request under 35 U.S.C. 122(b)(2)(B)(ii) [PTO/SB/36 (11-00)] is insufficient to comply with the requirements of 35 U.S.C. 122(b)(2)(B)(iii) [Notice of Foreign Filing]. See the "Reminder that Rescission of a Nonpublication Request is Not Itself a Notice of Foreign Filing" signed by Deputy Commissioner Kunin on April 11, 2003. Under current USPTO practice, further information regarding the abandonment is not required.

☐ This petition is being filed more than 3 months after the applicant was first notified of the abandonment, but within 1 year of the date of abandonment. Attached hereto is a statement by explaining how the abandonment occurred and how it was unintentional.

☐ This petition is being filed more than 1 year after the apparent date of abandonment. Attached hereto is a statement by explaining when the applicant or applicant's representative first became aware of the abandonment and how the delay in discovering the abandoned status occurred despite the exercise of due care or diligence on the part of the applicant or the applicant's representative.

6. Terminal Disclaimer under 37 C.F.R. § 1.137(b)(4) and (c)

☒ Since this application was filed on or after June 8, 1995, no terminal disclaimer is required.

☐ Since this application was filed before June 8, 1995, a terminal disclaimer is enclosed dedicating to the public a terminal part of the term of any patent granted hereon, and of any patent granted on a continuing application hereof, equivalent to the period of abandonment of this application.

7. Additional Fees

☒ Please charge any underpayment in fees for timely consideration of this Petition to Deposit Account No. 50-0665.

Respectfully submitted,
Perkins Coie LLP

Date: July 3, 2003

Maurice J. Pirio
Registration No. 33,273

Correspondence Address:
Customer No. 25096
Perkins Coie LLP
P.O. Box 1247
Seattle, Washington 98111-1247
(206) 583-8888

LENOVO EXHIBIT 1002 - 217/553

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Paper No. 9

Perkins Coie LLP
Patent-Sea
PO Box 1247
Seattle, WA 98111-1247

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AUG 1 8 2003

OFFICE OF PETITIONS

In re Application of
Shin et al.
Application No. 10/045,625
Filed: November 7, 2001
Attorney Docket No. 594728818US

DECISION GRANTING PETITION
UNDER 37 CFR 1.137(b)

This is a decision on the petition, filed July 3, 2003, which is being treated as a petition under 37 CFR 1.137(b) to revive the instant nonprovisional application for failure to timely notify the U.S. Patent and Trademark (USPTO) of the filing of an application in a foreign country, or under a multinational treaty that requires publication of applications eighteen months after filing. *See* 37 CFR 1.137(f).

The petition is **GRANTED**.

Petitioner states that the instant nonprovisional application is the subject of an application filed in an eighteen month publication country on November 21, 2001. However, the USPTO was unintentionally not notified of this filing within 45 days subsequent to the filing of the subject application in an eighteen month publication country.

In view of the above, this application became abandoned pursuant to 35 U.S.C. § 122(b)(2)(B)(iii) and 37 CFR 1.213(c) for failure to timely notify the Office of the filing of an application in a foreign country or under a multilateral international agreement that requires publication of applications 18 months after filing.

A petition to revive an application abandoned pursuant to 35 U.S.C. 122(b)(2)(B)(iii) for failure to notify the USPTO of a foreign filing must be accompanied by:

(1) the required reply which is met by the notification of such filing in a foreign country or under a multinational treaty;
(2) the petition fee as set forth in 37 CFR 1.17(m); and

(3) a statement that the entire delay in filing the required reply from the due date of the reply until the filing of a grantable petition was unintentional.

The instant petition has been found to be in compliance with 37 CFR 1.137(b). Accordingly, the failure to timely notify the USPTO of a foreign or international filing within 45 days after the date of filing of such foreign or international application as provided by 35 U.S.C. § 122(b)(2)(B)(iii) and 37 CFR 1.213(c) is accepted as having been unintentionally delayed.

The previous Request and Certification under 35 U.S.C. § 122(b)(2)(B)(i) has been rescinded.

Any inquiries concerning this decision may be directed to Latrice Bond at (703) 308-6911.

This application is being forwarded to Technology Center Art Unit 2665 for examination in due course.

Latrice Bond
Paralegal Specialist
Office of Petitions
Office of the Deputy Commissioner
for Patent Examination Policy

Marianne Morgan for
Frances Hicks
Lead Petitions Examiner

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	21	switch with control adj2 (data message) with (data packet) same (connect conneting) with data adj2 (store storage)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 11:32
L4	92	switch with control with data same (connect conneting) with data adj2 (store storage)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 11:36
L6	3	4 and packet with (type symbol)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 11:36
L10	2876	switch with control with data same data adj2 (store storage)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 11:39
L11	107	10 and packet with (type symbol)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 11:39
L12	54	11 and packet with head$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 11:39
L13	2205	switch with control with data same data adj (store storage)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 12:11
L14	91	13 and packet with (type symbol)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 11:39
L15	47	14 and packet with head$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 11:49

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L16	26	15 and (synchroniz$6 adj2 (information symbol signal) IDLE)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 11:51
L17	14	15 and synchroniz$6 adj2 (information symbol signal)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 12:22
L19	225	packet with in$band and (control synchroniz$6) with out$of$band	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 11:59
L20	13	data adj3 packet with in$band and (control adj3 packet synchroniz$6 adj2 (signal packet symbol)) with outofband	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 11:59
L21	7	switch with control with data with packet with header same data adj (store storage)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 12:15
L25	3	switch with control with packet with header same storage adj2 (network system)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 12:17
L26	9	switch with packet with header same storage adj2 (network system)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 12:18
L27	1	26 and packet adj type	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 12:18
L29	16	(in$band and out$of$band) with symbol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 12:49
L30	13	(transmit transmitting) with synchroniz$6 adj (symbol message primitive) with packet adj type	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 13:02

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L31	23	(transmit transmitting) with synchroniz$6 with packet adj type	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 13:19
L32	9	(transmit transmitting transmitted) with synchroniz$6 with before adj4 transmitting adj4 packet	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 13:19
L33	3542729	30 and synchroniz$6 before packet	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 13:03
L34	1	30 and synchroniz$6 adj4 before adj4 packet	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 13:03
L35	13	30 and synchroniz$6 with before with packet	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 17:22
L36	21	(identify identifying) adj3 packet adj type with synchroniz$6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 13:19
L37	186	(transmit transmitting transmitted receive receiving send sending) with (command write read) with before adj4 transmitting adj4(data packet)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 13:21
L38	95	(transmit transmitting transmitted receive receiving send sending) adj6 (command write read) with before adj4 transmitting adj4(data packet)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 13:21
L39	245	(transmit transmitting transmitted receive receiving send sending) adj6 (command write read) with before adj4 (transmit transmitting send sending) adj4 (data packet)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 13:22
L40	357	(transmit transmitting transmitted receive receiving send sending) adj6 (command control) with before adj4 (transmit transmitting send sending) adj4 (data packet)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 15:19

LENOVO EXHIBIT 1002 - 222/553

L41	137	39 and 40	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 13:22
L42	65	41 and switch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 13:22
L43	56	42 and storage	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 13:28
L44	22	42 and storage adj3 (network system)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 13:23
L45	56	43 not 44ge	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 13:28
L46	34	43 not 44	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 13:28
L57	2	"5574849".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 14:56
L58	1	57 and (transmit transmitting) adj2 symbol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 14:56
L59	1	(transmit transmitting send sending) adj6 (packet adj type) with before adj4 (transmit transmitting send sending) adj4 (data packet)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 15:20
L60	112	(transmit transmitting send sending) adj6 (read write) with before adj4 (transmit transmitting send sending) adj4 (data packet)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 15:21

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L61	10	(transmit transmitting send sending) adj2 (read write) near2 command with before adj4 (transmit transmitting send sending) adj4 (data packet)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 15:24
L62	67	(transmit transmitting send sending) adj2 (read write) with before adj4 (transmit transmitting send sending) adj4 (data packet)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 15:24
L63	61	(transmit transmitting send sending) adj2 (read write) with before adj2 (transmit transmitting send sending) adj4 (data packet)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 15:24
L64	44	(transmit transmitting send sending) adj2 (read write) with before adj2 (transmit transmitting send sending) adj2 (data packet)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 16:27
L65	16	packet adj type with synchroniz$6 adj symbol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 15:33
L66	137	packet adj type with synchroniz$6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 15:54
L67	36808	packet adj type with synchroniz$6 and packet adj2 preceded aadj3 synchronization adj (symbol signal sequence)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 15:34
L68	3	packet adj type with synchroniz$6 and packet adj2 preceded adj3 synchronization adj (symbol signal sequence)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 15:35
L69	8	packet adj2 (before preceded) adj3 synchronization adj (symbol signal sequence)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 15:46
L70	5	69 and packet adj type	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 15:39

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L71	8	packet adj2 (before preceded) adj3 synchronization adj (information packet symbol signal sequence)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 15:47
L72	17890	69 snd 71	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 15:47
L73	8	69 and 71	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 15:47
L74	16	packet near2 type adj2 (before preceded) adj3 packet	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 15:52
L75	16	74 not 73	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 15:50
L78	3	signal with packet adj type with (before preceded) adj3 packet	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 16:26
L79	258	(read write) with (before preceded) adj3 packet	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 16:26
L80	87	(transmit transmitting send sending) adj2 (command read write) with before adj2 (transmit transmitting send sending) adj2 (data packet)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 16:41
L82	82	80 not 44	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 16:28
L83	54239	control adj (message command packet signal) with (read write)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 16:43

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L84	13716	control adj (message command packet signal) adj3 (read write)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 16:43
L85	6959	84 and switch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 16:44
L86	358	84 and switch and storage adj (system network)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 16:43
L87	70	84 and (packet adj type)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 16:44
L88	1	84 with (packet adj type)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 16:44
L90	13	in$band with transition adj2 optimized and outofband with transition adj2 optimized	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 17:11
L91	13	in$band with transition adj2 optimized and outofband	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 17:11
L94	13	35 and switch adj network	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 17:30
L95	13	35 and switch adj network and storage	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 17:55
L96	2	"20030189922"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 17:56

LENOVO EXHIBIT 1002 - 226/553

L97	526	storage adj area adj network with switch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 18:05
L100	57	97 and synchronization	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 18:04
L101	3	97 and synchronization and packet adj type	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 17:58
L102	7	storage adj area adj network adj device with switch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2005/10/09 18:05

LENOVO EXHIBIT 1002 - 227/553

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,625	11/07/2001	Yeshik Shin	594728118US	1053

25096 7590 10/18/2005

PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE, WA 98111-1247

EXAMINER	
YANG, LINA	
ART UNIT	**PAPER NUMBER**
2665	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

LENOVO EXHIBIT 1002 - 228/553

Office Action Summary	Application No.	Applicant(s)	
	10/045,625	SHIN ET AL.	
	Examiner	Art Unit	
	Lina Yang	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 May 2002* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

LENOVO EXHIBIT 1002 - 229/553

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Sonnier et al (U. S. Patent No. 5,574,849) in view of Higurashi et al (U. S. Patent No. 5,963,703).

Regarding claims 1 and 16, Sonnier teaches a method for transmitting packet types of packets, the method comprising: receiving a packet having symbols (data or command and commands can be read or write; figs. 1A and 6; col. 11 lines 22-35, col. 17 lines 10-47 and col. 22 lines 32-34); identifying a packet type of the packet (fig. 6 col. 22 lines 32-34); transmitting a synchronization symbol (col. 22 lines 22-26; col. 26 lines 18-35; col. 27 lines 30-38 and 56-67 and col. 28 lines 1-2 and col. 28 lines 31-35), wherein the transmitted synchronization symbol provides synchronization information (col. 26 lines 18-35 and col. 28 lines 31-35); and transmitting the symbols of the received packet (data symbols transmitted out of X and Y encoders; col. 27 lines 30-38 and 56-67 and col. 28 lines 1-2).

Sonnier differs from the claimed invention in that Sonnier does not specifically teach that the synchronization symbol corresponds to the identified packet type and each packet type has a different synchronization symbol. However, Higurashi teaches that a control signal of read or write can be generated in response to the packet type information (col. 4 lines 37-40). And Sonnier suggested that synchronization symbols and/or control symbols could be transmitted before transmitting the message packet (col. 28 lines 31-35). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include, transmitting a synchronization symbol that corresponds to the identified packet type, wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol; as taught by Higurashi in the assembly of Sonnier in order to transmit the control command before transmit the message packet.

Regarding claim 9, Sonnier teaches a method for identifying packet types of packets of symbols, the method comprising: receiving a packet of symbols (col. 22 lines 31-34).

Sonnier differs from the claimed invention in that Sonnier does not specifically teach that receiving a synchronization symbol indicating a packet type, each packet type having a different synchronization symbol; and indicating that the received packet of symbols has the packet type of the received synchronization symbol. However,

Higurashi teaches that a control signal of read or write can be generated in response to the packet type information (col. 4 lines 37-40). And Sonnier suggested that synchronization symbols and/or control symbols could be transmitted before transmitting the message packet (col. 28 lines 31-35). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to make the synchronization symbol (including the control command) to include a packet type (such as read or write), each packet type having a different synchronization symbol (such as read or write); and indicating that the received packet of symbols has the packet type of the received synchronization symbol; as taught by Higurashi in the assembly of Sonnier in order to receive the control command before transmit the message packet.

Regarding claims 2, 10, and 17, Sonnier further teaches that the symbols of the packet include in-band symbols and the synchronization symbols are out-of-band symbols (col. 27 lines 30-38).

Regarding claims 3, 11 and 18, Sonnier further teaches that the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized (col. 17 lines 44-47and col. 27 lines 30-38).

Regarding claims 4, 12 and 19, Sonnier further teaches that the synchronization symbol is transmitted before transmitting the symbols of the packet (col. 28 lines 31-35).

Regarding claims 5 and 20, Sonnier further teaches that the packet has a header with a field that indicates packet type and the identifying of the packet type includes checking the field of the header that indicates packet type (figs. 3A and col. 17 lines 10-47).

Regarding claims 6, 13 and 21, Sonnier further teaches that the packet types include a data packet (col. 11 lines 27-29 and col. 17 lines 10-47).

Regarding claims 7, 14 and 22, Sonnier further teaches that the packet types include a control packet (col. 11 lines 27-29 and col. 17 lines 10-47).

Regarding claims 8, 15 and 23, Sonnier further teaches that the symbols are transmitted to a switch network (col. 1 lines 13-34 and col.; fig. 19A and col.53 lines 25-55).

2. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over by Sonnier et al (U. S. Patent No. 5,574,849) in view of Higurashi et al (U. S. Patent No. 5,963,703), and further teaches that in view of Howe (U. S. Patent application No. 20030189922).

Regarding claim 24, the combined assembly of Sonnier and Higurashi differs from the claimed invention in that the combined assembly does not specifically teach that the communications device is part of a storage area network. However, Howe teaches a communications device (Fig. 9, an integrated layer one switch having similar functions as disclosed in claim 1) is part of a storage area network ([0076]- [0077 and [0087]). Therefore, it would have been obvious to have the combined assembly of Sonnier and Higurashi configured as part of a storage area network, as taught by Howe, in order to provide a variety of applications for the packet-based communications network.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wilson et al. (US Patent No. 6,738,821 B1) teaches a network for efficiently communicating storage data through an Ethernet storage protocol (ESP) that streamlines the processing and communication of storage data and removes the overhead associated with prior art communication protocol techniques.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lina Yang whose telephone number is (571)272-3151. The examiner can normally be reached Monday through Thursday between 8:00 a.m. and 7:00 p.m. eastern standard time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 517-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LY

HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Notice of References Cited	Application/Control No. 10/045,625	Applicant(s)/Patent Under Reexamination SHIN ET AL.	
	Examiner Lina Yang	Art Unit 2665	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,574,849	11-1996	Sonnier et al.	714/12
	B	US-5,963,703	10-1999	Higurashi et al.	386/75
	C	US-2003/0189922	10-2003	Howe, Wayne R.	370/352
	D	US-6,738,821	05-2004	Wilson et al.	709/230
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	S					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

LENOVO EXHIBIT 1002 - 236/553

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Bib Data Sheet

CONFIRMATION NO. 105

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/045,625	11/07/2001 RULE	370	2665	594728118US

APPLICANTS

Yeshik Shin, Sunnyvale, CA;

David D. Lee, Palo Alto, CA;
Deog-Kyoon Jeong, Seoul, KOREA, REPUBLIC OF;Shing Kong, Brisbane, CA;

** CONTINUING DATA ********** Yes, LY
This appln claims benefit of 60/252,724 11/22/2000

** FOREIGN APPLICATIONS ********** None, LY

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 02/26/2002

Foreign Priority claimed	STATE OR	SHEETS	TOTAL	INDEPENDENT
35 USC 119 (a-d) conditions met	COUNTRY	DRAWING	CLAIMS	CLAIMS
Verified and Acknowledged	CA	59	24	3

☐ yes ☒ no
☐ yes ☐ no ☐ Met after Allowance
Examiner's Signature _____ Initials LY

ADDRESS
25096
PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE , WA
98111-1247

TITLE
Method and system for integrating packet type information with synchronization symbols

FILING FEE	FEES: Authority has been given in Paper	☐ All Fees
RECEIVED	No. _____ to charge/credit DEPOSIT ACCOUNT	☐ 1.16 Fees (Filing)
942	No. _____ for following:	☐ 1.17 Fees (Processing Ext. of time)
		☐ 1.18 Fees (Issue)
		☐ Other _____

LENOVO EXHIBIT 1002 - 237/553

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/045,625	SHIN ET AL.
Examiner	**Art Unit**
Lina Yang	2665

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	10/9/05
	1	√
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LENOVO EXHIBIT 1002 - 238/553

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/045,625	SHIN ET AL.	
	Examiner	Art Unit	
	Lina Yang	2665	

SEARCHED			
Class	Subclass	Date	Examiner

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST	10/5/2005	LY

LENOVO EXHIBIT 1002 - 239/553

OIPE IAP89 MAR 20 2006 PATENT & TRADEMARK OFFICE

03-22-06

TRW 2665 #

Express Mail No. EV 853120735 US

AMENDMENT TRANSMITTAL LETTER

Docket No. 594728818US

Application No.	Filing Date	Examiner	Art Unit
10/045,625-Conf. #1053	November 7, 2001	L. Yang	2665

Applicant(s): Shi, et al.

Invention: METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS

TO THE COMMISSIONER FOR PATENTS

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	24	- 24 =		x	
Independent Claims	3	- 3 =		x	
Multiple Dependent Claims (check if applicable)	☐				
Other fee (please specify): Extension for response within second month					450.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:					450.00

[x] Large Entity ☐ Small Entity

☐ No additional fee is required for this amendment.

☐ Please charge Deposit Account No. 50-0665 in the amount of $ _____. A duplicate copy of this sheet is enclosed.

[x] A check in the amount of $ 450.00 to cover the filing fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

[x] The Director is hereby authorized to charge and credit Deposit Account No. 50-0665 as described below. A duplicate copy of this sheet is enclosed.

[x] Credit any overpayment.

[x] Charge any additional filing or application processing fees required under 37 CFR 1.16 and 1.17.

Maurice J. Pirio

Dated: March 20, 2006

Maurice J. Pirio
Attorney/Agent Reg. No.: 33,273

PERKINS COIE LLP
P.O. Box 1247
Seattle, Washington 98111-1247
(206) 359-8000



Express Mail No. EV 853120735 US

Docket No.: 594728818US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Shin et al.

Application No.: 10/045,625

Confirmation No.: 1053

Filed: November 7, 2001

Art Unit: 2665

For: METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS

Examiner: L. Yang

RESPONSE TO NON-FINAL OFFICE ACTION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated October 18, 2005, please amend the above-identified U.S. patent application as follows:

A complete listing of the claims begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

AMENDMENTS TO THE CLAIMS

1. (Original) A method for transmitting packet types of packets, the method comprising:

receiving a packet having symbols;

identifying a packet type of the packet;

transmitting a synchronization symbol that corresponds to the identified packet type, wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol; and

transmitting the symbols of the received packet.

2. (Original) The method of claim 1 wherein the symbols of the packet include in-band symbols and the synchronization symbols are out-of-band symbols.

3. (Original) The method of claim 2 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

4. (Original) The method of claim 1 wherein the synchronization symbol is transmitted before transmitting the symbols of the packet.

5. (Original) The method of claim 1 wherein the packet has a header with a field that indicates packet type and the identifying of the packet type includes checking the field of the header that indicates packet type.

6. (Original) The method of claim 1 wherein the packet types include a data packet.

7. (Original) The method of claim 1 wherein the packet types include a control packet.

8. (Original) The method of claim 1 wherein the symbols are transmitted to a switch network.

9. (Original) A method for identifying packet types of packets of symbols, the method comprising:

receiving a synchronization symbol indicating a packet type, each packet type having a different synchronization symbol;

receiving a packet of symbols; and

indicating that the received packet of symbols has the packet type of the received synchronization symbol.

10. (Original) The method of claim 9 wherein the symbols of the packets include in-band symbols and the synchronization symbols are out-of-band symbols.

11. (Original) The method of claim 10 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

12. (Original) The method of claim 9 wherein the synchronization symbol is received before the symbols of the packet are received.

13. (Original) The method of claim 9 wherein the packet types include a data packet.

14. (Original) The method of claim 9 wherein the packet types include a control packet.

15. (Original) The method of claim 9 wherein the symbols are received from a switch.

16. (Original) A communications device for transmitting packet types of packets, comprising:

an identification component that identifies a packet type of a packet of symbols; and

a transmission component that transmits a synchronization symbol that corresponds to the identified packet type, the transmitted synchronization symbol providing synchronization information and each packet type having a different synchronization symbol, and that transmits the symbols of the packet.

17. (Original) The communications device of claim 16 wherein the symbols of the packet include in-band symbols and the synchronization symbols are out-of-band symbols.

18. (Original) The communications device of claim 17 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

19. (Original) The communications device of claim 16 wherein the synchronization symbol is transmitted before transmitting the symbols of the packet.

20. (Original) The communications device of claim 16 wherein the packet has a header with a field that indicates packet type and the identification component checks the field of the header that indicates packet type.

21. (Original) The communications device of claim 16 wherein the packet types include a data packet.

22. (Original) The communications device of claim 16 wherein the packet types include a control packet.

23. (Original) The communications device of claim 16 wherein the symbols are transmitted to a switch network.

24. (Original) The communications device of claim 16 wherein the communications device is part of a storage area network.

REMARKS

Claims 1-23 stand rejected as being unpatentable over U.S. Patent No. 5,574,849 to Sonnier et al. in view of U.S. Patent No. 5,963,703 to Higurashi et al. Additionally, claim 24 stands rejected as being unpatentable over Sonnier, Higurashi, and further in view of U.S. Patent Application Publication No. 2003/0189922 to Howe. Applicant respectfully disagrees.

Each independent claim (claims 1, 9, and 16) describes transmitting or receiving one or more synchronization symbol(s) that correspond to (or indicate) an identified packet type. For example, claim 1 recites a method of transmitting packet types of packets, the method including "identifying a packet type" and "transmitting a synchronization symbol that corresponds to the identified packet type, wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol."

Neither Sonnier nor Higurashi show synchronization symbols that correspond to packet types. As the Examiner admits, "Sonnier does not specifically teach that the synchronization symbol to the identified packet type and each packet type has a different synchronization symbol" (Office Action, Oct. 18, 2005, p. 3), and looks to Higurashi to remedy the deficiency.

Higurashi is directed to a method of recording and reproducing packet data. For example, audio packets and video packets are separated from an input stream of packets that includes audio packets and video packets. The audio packets are recorded on tracks that are different from tracks on which the video packets are recorded (Higurashi, Abstract). Packets are identified based on information contained within the header of the packet (Id., 3: 52-56). Signals such as read or write control signals control the reading and writing of audio and video packets to a buffer system. Additionally, time stamp signals may be used with the read or write control signals. The time signals, which control time

stamping, may be generated after detecting reference time information from a packet header.

It is the Examiner's position that, because Higurashi discusses generating control signals in response to packet type information, "it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include, transmitting a synchronization symbol that corresponds to the identified packet type, wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol" (Office Action, Oct. 18, 2005, p. 3). Applicants respectfully disagree.

As clearly shown in Figure 1 of Higurashi, the read and write control signals are not part of the stream of packets, and are used merely to read out and write packets into the buffer system. These signals are not used to synchronize a packet stream. Instead, two different signals are used to control two different buffers, one for audio packets (buffer 4) and one for video packets (buffer 5).

In sum, obtaining reference time information from packet headers and incorporating this information into timing signals for reading or writing packets into specific buffers, as disclosed by Higurashi, would not lead one of ordinary skill in the art to incorporate packet type information into the synchronization symbols of Sonnier. As such, Sonnier in view if Higurashi does not teach each and every element of claim 1, and, for at least these reasons, cannot render the claim obvious.

Claims 9 and 16 (and all the dependent claims) recite similar elements to those of claim 1, and are therefore patentable for at least the reasons discussed above. Moreover, the claims recite a novel combination of elements that is neither taught not suggested by the relied-upon references.

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In view of the above amendment, applicant believes the pending application is in condition for allowance and respectfully requests its early allowance.

Applicant has submitted herewith the requisite extension of time fee and believes no additional fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-0665, under Order No. 594728818US from which the undersigned is authorized to draw.

Dated:

3-20-06

Respectfully submitted,

By Maurice J Pirio

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PTO/SB/06 (08-03)
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PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number: 10/045625

CLAIMS AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE	SMALL ENTITY FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY FEE
BASIC FEE (37 CFR 1.16(a))				$	OR		$
TOTAL CLAIMS (37 CFR 1.16(c))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(b))	minus 3 =	*	X $ =		OR	X $ =	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(d))			+ $ =		OR	+ $ =	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL		OR	TOTAL	

CLAIMS AS AMENDED – PART II

3-20-06

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
Total (37 CFR 1.16(c))	* 24	Minus	** 24	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(b))	* 3	Minus	*** 3	=	X $ =		OR	X $ =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $ =		OR	+ $ =	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
Total (37 CFR 1.16(c))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(b))	*	Minus	***	=	X $ =		OR	X $ =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $ =		OR	+ $ =	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
Total (37 CFR 1.16(c))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(b))	*	Minus	***	=	X $ =		OR	X $ =	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					+ $ =		OR	+ $ =	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

LENOVO EXHIBIT 1002 - 249/553

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S14	0	identfied with packet with type	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 18:49
S15	1123	identified with packet with type	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 18:49
S16	0	identified with packet with type and prepend44	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 18:50
S17	29	identified with packet with type and prepend$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 18:52
S18	256	identified with packet with type and encapsulat$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 18:53
S19	147	identified with packet near2 type and encapsulat$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 18:54
S20	4	identified with packet near2 type and append$3 with packet near2 type	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 18:55
S21	0	identified with packet near2 type and fllow$3 with packet near2 type	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 18:55
S22	92	identified with packet near2 type and follow$3 with packet near2 type	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 18:58
S23	33	identified with packet near2 type and packet adj sync	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:01
S24	267	identified with packet near2 type and control adj information	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:01

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EAST Search History

S25	207	packet near2 type with control adj information	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:02
S26	3	packet near2 type with control adj information with regard$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:06
S27	201	packet near2 type with regard$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:15
S28	322	packet near2 type with encapsulat$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:15
S29	3	identified with packet near2 type with encapsulat$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:15
S30	26	identified with packet near2 type same encapsulat$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:16
S31	5	identified with packet near2 type same prepend$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:17
S32	11	(identif$3 determin$3) with packet near2 type same prepend$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:19
S33	1	(identif$3 determin$3) with packet near2 type same pre-pend$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:19
S34	51	(identif$3 determin$3) with packet near2 type same append$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:23
S35	154	(identif$3 determin$3) with packet near2 type same encapsulat$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:23

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EAST Search History

S36	146	S35 not S34	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/30 09:38

LENOVO EXHIBIT 1002 - 252/553

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,625	11/07/2001	Yeshik Shin	594728118US	1053

25096 7590 06/07/2006

PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE, WA 98111-1247

EXAMINER	
NGUYEN, STEVEN H D	
ART UNIT	**PAPER NUMBER**
2616	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/045,625	SHIN ET AL.	
	Examiner	Art Unit	
	Steven HD Nguyen	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

The applicant should insert the application number into the blanks of the Para [001].

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 9-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Burnett (USP5703875).

Regarding claim 9, Burnet discloses a method for identifying packet types of packets of symbols comprising receiving a synchronization symbol indicating a packet type (Col. 2, lines 40-49), each packet type having a different synchronization symbol (Col. 2, lines 40-49); receiving a packet of symbols (Col. 2, lines 40-49); and indicating that the received packet of symbols has the packet type of the received synchronization symbol (Col. 2, lines 40-49, Fig 2, Ref 12 and 13, the state control word is used to stored the data or control packet into correct buffer).

Regarding claim 10, Burnett discloses the symbols of the packet include in-band symbols (Fig 2, ref 12) and the synchronization symbols are out-of-band symbols (Col. 2, lines 40-49, control words for control or data type message).

Regarding claim 11, Burnet discloses the in-band symbols are transition optimized (Fig 2, ref 12) and the out-of-band synchronization symbols are not transition optimized (Col. 2, lines 40-49).

Regarding claim 12, Burnet discloses the synchronization symbol is transmitted before transmitting the symbols of the packet (Col. 2, lines 40-49).

Regarding claim 13, Burnet discloses packet types include a data packet (Fig 2, Ref 13).

Regarding claim 14, Burnet discloses packet types include a control packet (Fig 2, Ref 12).

Regarding claim 15, Burnet discloses the symbols are received from a switch (Fig 1).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-8 and 16-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burnett (USP 5703875) in view of Deb (USP 6172990).

Regarding claims 1 and 16, Burnet discloses a method for transmitting packet types of packets comprising the steps of receiving a packet having symbols, transmitting a synchronization symbol that corresponds to the identified packet type (Col. 2, lines 40-49), wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol; and transmitting the symbols of the received packet (Col. 2, lines 40-49, each type of message is associated with a different state control word and the state control world is transmitted before transmitting its associated message). However, Burnett does not fully disclose identifying a packet type of the packet based on the received packet. In the same field of endeavor, Deb discloses a method for receiving a packet and identified the type of received packet and transmitting appended index that associated with the packet before transmitting packet (Col. 16, lines 24-58, col. 17, lines 22-37 and Fig 8, col. 21, line 30 to col. 22, line 19).

Since, a method for identifying a type of packet is well known and expected in the art. Therefore, it would have been obvious to one of ordinary skill in the art to apply a method for identifying a type of packet as disclosed by Deb into Burnett's system and method. The motivation would have been to reduce delay time when transmitting a packet from source to destination.

Regarding claims 2 and 17, Burnett discloses the symbols of the packet include in-band symbols (Fig 2, ref 12) and the synchronization symbols are out-of-band symbols (Col. 2, lines 40-49, control words for control or data type message).

Regarding claims 3 and 18, Burnet discloses the in-band symbols are transition optimized (Fig 2, ref 12) and the out-of-band synchronization symbols are not transition optimized (Col. 2, lines 40-49).

Regarding claims 4 and 19, Burnet discloses the synchronization symbol is transmitted before transmitting the symbols of the packet (Col. 2, lines 40-49).

Regarding claims 5 and 20, Deb discloses the packet has a header with a field that indicates packet type (Fig 1b, Ref 36) and the identifying of the packet type includes checking the field of the header that indicates packet type (Col. 16, lines 24-58, col. 17, lines 22-37 and Fig 8, col. 21, line 30 to col. 22, line 19).

Regarding claims 6 and 21, Burnet discloses the packet types include a data packet (Fig 2, Ref 13).

Regarding claims 7 and 22, Burnet discloses the packet types include a control packet (Fig 2, Ref 12).

Regarding claims 8 and 23, Burnett discloses the symbols are transmitted to a switch network (Fig 1).

Regarding claim 24, Deb discloses the communications device is part of a storage area network (Fig 10, Ref 1010 is hard drive).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bussiere (USP 6041042) discloses a method and system for determining a type of packet, then encapsulating a header that includes a type of packet.

Hendel (USP 6014380) discloses a method and system for transmitting control information regarding packet type of the received packet and transmitting the control information before the received packet.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven HD Nguyen whose telephone number is (571) 272-3159. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on (571) 272-3134. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven HD Nguyen
Primary Examiner
Art Unit 2616
May 30, 2006

Notice of References Cited	Application/Control No. 10/045,625	Applicant(s)/Patent Under Reexamination SHIN ET AL.	
	Examiner Steven HD Nguyen	Art Unit 2616	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,014,380	01-2000	Hendel et al.	370/401
*	B	US-6,041,042	03-2000	Bussiere, Richard	370/401
*	C	US-6,172,990	01-2001	Deb et al.	370/466
*	D	US-5,703,875	12-1997	Burnett, Robert W.	370/412
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

LENOVO EXHIBIT 1002 - 261/553

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/045,625	SHIN ET AL.
Examiner	**Art Unit**
Lina Yang	2665

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	+	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	10/9/05
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Claim		Date
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LENOVO EXHIBIT 1002 - 262/553

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/045,625	SHIN ET AL.	
	Examiner	Art Unit	
	Lina Yang	2665	

SEARCHED			
Class	Subclass	Date	Examiner

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST	10/5/2005	LY
11	8/4/06	

LENOVO EXHIBIT 1002 - 263/553

OIPE IAP68
DEC 07 2006
PATENT & TRADEMARK OFFICE

Express Mail No. EV 813996935 US

Docket No.: 594728818US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Shin et al.

Application No.: 10/045,625

Confirmation No.: 1053

Filed: November 7, 2001

Art Unit: 2616

For: METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS

Examiner: S. H. D. Nguyen

RESPONSE TO NON-FINAL OFFICE ACTION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated June 7, 2006, please consider the following remarks in the above-identified U.S. patent application:

The pending Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

AMENDMENTS TO THE CLAIMS

1. (Original) A method for transmitting packet types of packets, the method comprising:

receiving a packet having symbols;

identifying a packet type of the packet;

transmitting a synchronization symbol that corresponds to the identified packet type, wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol; and

transmitting the symbols of the received packet.

2. (Original) The method of claim 1 wherein the symbols of the packet include in-band symbols and the synchronization symbols are out-of-band symbols.

3. (Original) The method of claim 2 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

4. (Original) The method of claim 1 wherein the synchronization symbol is transmitted before transmitting the symbols of the packet.

5. (Original) The method of claim 1 wherein the packet has a header with a field that indicates packet type and the identifying of the packet type includes checking the field of the header that indicates packet type.

6. (Original) The method of claim 1 wherein the packet types include a data packet.

7. (Original) The method of claim 1 wherein the packet types include a control packet.

8. (Original) The method of claim 1 wherein the symbols are transmitted to a switch network.

9. (Original) A method for identifying packet types of packets of symbols, the method comprising:

receiving a synchronization symbol indicating a packet type, each packet type having a different synchronization symbol;

receiving a packet of symbols; and

indicating that the received packet of symbols has the packet type of the received synchronization symbol.

10. (Original) The method of claim 9 wherein the symbols of the packets include in-band symbols and the synchronization symbols are out-of-band symbols.

11. (Original) The method of claim 10 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

12. (Original) The method of claim 9 wherein the synchronization symbol is received before the symbols of the packet are received.

13. (Original) The method of claim 9 wherein the packet types include a data packet.

14. (Original) The method of claim 9 wherein the packet types include a control packet.

15. (Original) The method of claim 9 wherein the symbols are received from a switch.

16. (Original) A communications device for transmitting packet types of packets, comprising:

an identification component that identifies a packet type of a packet of symbols; and

a transmission component that transmits a synchronization symbol that corresponds to the identified packet type, the transmitted synchronization symbol providing synchronization information and each packet type having a different synchronization symbol, and that transmits the symbols of the packet.

17. (Original) The communications device of claim 16 wherein the symbols of the packet include in-band symbols and the synchronization symbols are out-of-band symbols.

18. (Original) The communications device of claim 17 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

19. (Original) The communications device of claim 16 wherein the synchronization symbol is transmitted before transmitting the symbols of the packet.

20. (Original) The communications device of claim 16 wherein the packet has a header with a field that indicates packet type and the identification component checks the field of the header that indicates packet type.

21. (Original) The communications device of claim 16 wherein the packet types include a data packet.

22. (Original) The communications device of claim 16 wherein the packet types include a control packet.

23. (Original) The communications device of claim 16 wherein the symbols are transmitted to a switch network.

24. (Original) The communications device of claim 16 wherein the communications device is part of a storage area network.

REMARKS

Claims 9-15 stand rejected under 35 U.S.C. 102(b) over U.S. Patent No. 5,703,875 to Burnett. Additionally, claims 1-8 and 16-24 stand rejected under 35 U.S.C. 103(a) over U.S. Patent No. 5,703,875 to Burnett and U.S. Patent No. 6,172,990 to Deb et al. Applicants respectfully disagree.

Each independent claim (claims 1, 9, and 16) describes transmitting or receiving one or more synchronization symbol(s) that correspond to (or indicate) an identified packet type. For example, claim 1 recites a method of transmitting packet types of packets, the method including "identifying a packet type" and "transmitting a synchronization symbol that corresponds to the identified packet type, wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol."

Burnett does not disclose synchronization symbols that correspond to (or indicate) packet types. Burnett discloses that "one approach is for the first switch 10a to send a state control word to the second switch 10b when the first switch 10a is about to begin sending a message. The state control word indicates to the second switch 10b which FIFO buffer 12, 13 to store the input words into." Burnett at 2: 40-49. Thus, a "state control word," as intended by Burnett, is transmitted by the first switch to instruct the second switch into which buffer subsequently transmitted packets are to be stored. There is no indication or suggestion in Burnett that the state control words disclosed by Burnett are involved in any synchronization.

Deb also does not disclose synchronization symbols that correspond to (or indicate) packet types. The Office Action states that "Deb discloses a method for receiving a packet and identified [sic] the type of received packet." Office Action at paragraph 6. Deb discusses methods for "processing packet data received from a physical layer." Deb at Abstract. Deb does not disclose synchronization symbols, nor does the Office Action rely on Deb to support synchronization or synchronization symbols.

In contrast, each of the independent claims recite features that relate synchronization symbols with packet types. Therefore, for at least these reasons, applicants respectfully submit that claims 1-24 are patentable over the cited references, and request their early allowance.

Applicant submits herewith an extension of time fee and believes no additional fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-0665, under Order No. 594728818US from which the undersigned is authorized to draw.

Dated: December 7, 2006

Respectfully submitted,

By 

Michael J. Smith
Registration No.: 56,702
PERKINS COIE LLP
P.O. Box 1247
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Attorneys for Applicant

OIPE IAP66
DEC 07 2006
PATENT & TRADEMARK OFFICE

PTO/SB/22 (07-06)
Approved for use through 09/30/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless if displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) FY 2005 (Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).)	Docket Number (Optional) 594728818US
Application Number 10/045,625-Conf. #1053	Filed November 7, 2001
For METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS	
Art Unit 2616	Examiner S. H. D. Nguyen

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

		Fee	Small Entity Fee	
[ ]	One month (37 CFR 1.17(a)(1))	$120	$60	$
[ ]	Two months (37 CFR 1.17(a)(2))	$450	$225	$
[X]	Three months (37 CFR 1.17(a)(3))	$1020	$510	$ 1,020.00
[ ]	Four months (37 CFR 1.17(a)(4))	$1590	$795	$
[ ]	Five months (37 CFR 1.17(a)(5))	$2160	$1080	$

[ ] Applicant claims small entity status. See 37 CFR 1.27.

[X] A check in the amount of the fee is enclosed.

[ ] Payment by credit card. Form PTO-2038 is attached.

[ ] The Director has already been authorized to charge fees in this application to a Deposit Account.

[X] The Director is hereby authorized to charge any deficiencies, or credit any overpayment, to Deposit Account Number 50-0665 . I have enclosed a duplicate copy of this sheet.

I am the

[ ] applicant/inventor.

[ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

[X] attorney or agent of record. Registration Number 56,702

[ ] attorney or agent under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____ .

Signature — December 7, 2006 (Date)

Michael J. Smith (Typed or printed name) — (206) 359-8000 (Telephone Number)

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

[X] Total of 1 forms are submitted.

12/11/2006 EFLORES 00000059 10045625

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I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV813996935US, on the date shown below in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: 12/7/06 Signature: _____ (Peter Sher)

OIPE IAP66 DEC 07 2006 PATENT & TRADEMARK OFFICE

12-08-06 IFW 2616 $

AMENDMENT TRANSMITTAL LETTER

Docket No. 594728818US

Application No.	Filing Date	Examiner	Art Unit
10/045,625-Conf. #1053	November 7, 2001	S. H. D. Nguyen	2616

Applicant(s): Shin et al.

Invention: METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS

TO THE COMMISSIONER FOR PATENTS

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	24	- 24 =		x	
Independent Claims	3	- 3 =		x	
Multiple Dependent Claims (check if applicable)	☐				
Other fee (please specify):	Extension for response within third month				1,020.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:					1,020.00

☒ Large Entity ☐ Small Entity

☐ No additional fee is required for this amendment.

☐ Please charge Deposit Account No. 50-0665 in the amount of $ _____. A duplicate copy of this sheet is enclosed.

☒ A check in the amount of $ 1,020.00 to cover the filing fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☒ The Director is hereby authorized to charge and credit Deposit Account No. 50-0665 as described below. A duplicate copy of this sheet is enclosed.

☒ Credit any overpayment.

☒ Charge any additional filing or application processing fees required under 37 CFR 1.16 and 1.17.

Dated: December 7, 2006

Michael J. Smith
Attorney/Agent Reg. No.: 56,702

PERKINS COIE LLP
P.O. Box 1247
Seattle, Washington 98111-1247
(206) 359-8000

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV813996935US, on the date shown below in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: 12/7/06 Signature: _____ (Peter Sher)

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,625	11/07/2001	Yeshik Shin	59472-8818US	1053

25096 7590 03/06/2007

PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE, WA 98111-1247

EXAMINER	
NGUYEN, STEVEN H D	
ART UNIT	PAPER NUMBER
2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

LENOVO EXHIBIT 1002 - 273/553

SY

Office Action Summary	Application No.	Applicant(s)	
	10/045,625	SHIN ET AL.	
	Examiner	Art Unit	
	Steven HD Nguyen	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

The applicant should insert the application number into the blanks of the Para [001].

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 9-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Burnett (USP5703875).

Regarding claim 9, Burnet discloses a method for identifying packet types of packets of symbols comprising receiving a synchronization symbol indicating a packet type (Col. 2, lines 40-49), each packet type having a different synchronization symbol (Col. 2, lines 40-49); receiving a packet of symbols (Col. 2, lines 40-49); and indicating that the received packet of symbols has the packet type of the received synchronization symbol (Col. 2, lines 40-49, Fig 2, Ref 12 and 13, the state control word is used to stored the data or control packet into correct buffer).

Regarding claim 10, Burnett discloses the symbols of the packet include in-band symbols (Fig 2, ref 12) and the synchronization symbols are out-of-band symbols (Col. 2, lines 40-49, control words for control or data type message).

Regarding claim 11, Burnet discloses the in-band symbols are transition optimized (Fig 2, ref 12) and the out-of-band synchronization symbols are not transition optimized (Col. 2, lines 40-49).

Regarding claim 12, Burnet discloses the synchronization symbol is transmitted before transmitting the symbols of the packet (Col. 2, lines 40-49).

Regarding claim 13, Burnet discloses packet types include a data packet (Fig 2, Ref 13).

Regarding claim 14, Burnet discloses packet types include a control packet (Fig 2, Ref 12).

Regarding claim 15, Burnet discloses the symbols are received from a switch (Fig 1).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-8 and 16-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burnett (USP 5703875) in view of Deb (USP 6172990).

Regarding claims 1 and 16, Burnet discloses a method for transmitting packet types of packets comprising the steps of receiving a packet having symbols, transmitting a synchronization symbol that corresponds to the identified packet type (Col. 2, lines 40-49), wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol; and transmitting the symbols of the received packet (Col. 2, lines 40-49, each type of message is associated with a different state control word and the state control world is transmitted before transmitting its associated message). However, Burnett does not fully disclose identifying a packet type of the packet based on the received packet. In the same field of endeavor, Deb discloses a method for receiving a packet and identified the type of received packet and transmitting appended index that associated with the packet before transmitting packet (Col. 16, lines 24-58, col. 17, lines 22-37 and Fig 8, col. 21, line 30 to col. 22, line 19).

Since, a method for identifying a type of packet is well known and expected in the art. Therefore, it would have been obvious to one of ordinary skill in the art to apply a method for identifying a type of packet as disclosed by Deb into Burnett's system and method. The motivation would have been to reduce delay time when transmitting a packet from source to destination.

Regarding claims 2 and 17, Burnett discloses the symbols of the packet include in-band symbols (Fig 2, ref 12) and the synchronization symbols are out-of-band symbols (Col. 2, lines 40-49, control words for control or data type message).

Regarding claims 3 and 18, Burnet discloses the in-band symbols are transition optimized (Fig 2, ref 12) and the out-of-band synchronization symbols are not transition optimized (Col. 2, lines 40-49).

Regarding claims 4 and 19, Burnet discloses the synchronization symbol is transmitted before transmitting the symbols of the packet (Col. 2, lines 40-49).

Regarding claims 5 and 20, Deb discloses the packet has a header with a field that indicates packet type (Fig 1b, Ref 36) and the identifying of the packet type includes checking the field of the header that indicates packet type (Col. 16, lines 24-58, col. 17, lines 22-37 and Fig 8, col. 21, line 30 to col. 22, line 19).

Regarding claims 6 and 21, Burnet discloses the packet types include a data packet (Fig 2, Ref 13).

Regarding claims 7 and 22, Burnet discloses the packet types include a control packet (Fig 2, Ref 12).

Regarding claims 8 and 23, Burnett discloses the symbols are transmitted to a switch network (Fig 1).

Regarding claim 24, Deb discloses the communications device is part of a storage area network (Fig 10, Ref 1010 is hard drive).

Response to Arguments

7. Applicant's arguments filed 12/7/06 have been fully considered but they are not persuasive.

In response to page 6, the applicant states that Burnett fails to disclose synchronization symbols that correspond to packet types. In Reply, the examiner respectfully disagrees with the applicant because Burnett disclose a method and system for allowing a sender to determine the message type of the received messages which include control and data message based on the header. The sender informs the receiver which type of message being transmitted by the sender by using control words "synchronization symbols" which corresponds to message "packet" types (See col. 2, lines 40 to col. 3, lines 35, state control word used to synchronize the state of transmitting/receiving between the sender and receiver in order to store the information at the receiver).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

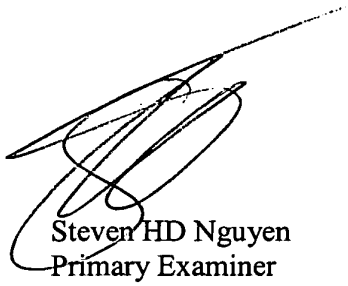
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven HD Nguyen whose telephone number is (571) 272-3159. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on (571) 272-3134. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Steven HD Nguyen
Primary Examiner
Art Unit 2616

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/045,625		2616	26L1

Correspondence Address / Fee Address Change

The following fields have been set to Customer Number 63170 on 03/16/2007

- Correspondence Address

The address of record for Customer Number 63170 is:
PERKINS COLE LLP
P.O. BOX 2168
MENLO PARK,CA 94026

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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/045,625		2616	26L1

Correspondence Address / Fee Address Change

The following fields have been set to Customer Number 63170 on 04/11/2007

- Correspondence Address

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/045,625		2616	26L1

Correspondence Address / Fee Address Change

The following fields have been set to Customer Number 63170 on 05/17/2007

- Correspondence Address

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MENLO PARK,CA 94026

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/045,625		2616	26L1

Correspondence Address / Fee Address Change

The following fields have been set to Customer Number 63170 on 06/12/2007

- Correspondence Address

The address of record for Customer Number 63170 is:
PERKINS COLE LLP
P.O. BOX 2168
MENLO PARK,CA 94026

PTO/SB/31 (04-07)
Approved for use through 09/30/2007. OMB 0651-0031
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NOTICE OF APPEAL FROM THE EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES	Docket Number (Optional) 594728818US

In re Application of Shin et al.		
Application Number 10/045,625-Conf. #1053	Filed November 7, 2001	
For METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS		
Art Unit 2616	Examiner S. H. D. Nguyen	

Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the examiner.

The fee for this Notice of Appeal is (37 CFR 41.20(b)(1)) $ 500.00

[ ] Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by half, and the resulting fee is: $ _____

[ ] A check in the amount of the fee is enclosed.

[x] Payment in the amount of the fee is submitted via EFT Account No. SEA1PIRM.

[ ] The Director has already been authorized to charge fees in this application to a Deposit Account. I have enclosed a duplicate copy of this sheet.

[x] The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 50-0665 . I have enclosed a duplicate copy of this sheet.

[x] A petition for an extension of time under 37 CFR 1.136(a) (PTO/SB/22) is enclosed.

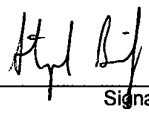
I am the

[ ] applicant /inventor.

[ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

[x] attorney or agent of record.
Registration number 38,829

[ ] attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34. _____


Signature

Stephen Bishop
Typed or printed name

(206) 359-8000
Telephone number

August 6, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

[ ] *Total of 1 forms are submitted.

LENOVO EXHIBIT 1002 - 285/553

PTO/SB/22 (04-07)
Approved for use through 09/30/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless if displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) FY 2006 (Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).)	Docket Number (Optional) 594728818US
Application Number 10/045,625-Conf. #1053	Filed November 7, 2001
For METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS	
Art Unit 2616	Examiner S. H. D. Nguyen

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

		Fee	Small Entity Fee	
[ ]	One month (37 CFR 1.17(a)(1))	$120	$60	$
[ ]	Two months (37 CFR 1.17(a)(2))	$450	$225	$
[X]	Three months (37 CFR 1.17(a)(3))	$1020	$510	$ 1,020.00
[ ]	Four months (37 CFR 1.17(a)(4))	$1590	$795	$
[ ]	Five months (37 CFR 1.17(a)(5))	$2160	$1080	$

[ ] Applicant claims small entity status. See 37 CFR 1.27.

[ ] A check in the amount of the fee is enclosed.

[X] Payment by EFT Account No. SEA1PIRM.

[ ] The Director has already been authorized to charge fees in this application to a Deposit Account.

[X] The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-0665 . I have enclosed a duplicate copy of this sheet.

I am the

[ ] applicant/inventor.

[ ] assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

[X] attorney or agent of record. Registration Number 38,829

[ ] attorney or agent under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

Signature — August 6, 2007 (Date)

Stephen Bishop (Typed or printed name) — (206) 359-8000 (Telephone Number)

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

[ ] Total of 1 forms are submitted.

LENOVO EXHIBIT 1002 - 286/553

Electronic Patent Application Fee Transmittal

Application Number:	10045625
Filing Date:	07-Nov-2001
Title of Invention:	Method and system for integrating packet type information with synchronization symbols
First Named Inventor/Applicant Name:	Yeshik Shin
Filer:	Robert G. Woolston/Mike Navarro
Attorney Docket Number:	59472-8818US

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Notice of appeal	1401	1	500	500
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 3 months with $0 paid	1253	1	1020	1020
Miscellaneous:				
		Total in USD ($)		**1520**

Electronic Acknowledgement Receipt

EFS ID:	2053630
Application Number:	10045625
International Application Number:	
Confirmation Number:	1053
Title of Invention:	Method and system for integrating packet type information with synchronization symbols
First Named Inventor/Applicant Name:	Yeshik Shin
Customer Number:	63170
Filer:	Robert G. Woolston/Mike Navarro
Filer Authorized By:	Robert G. Woolston
Attorney Docket Number:	59472-8818US
Receipt Date:	06-AUG-2007
Filing Date:	07-NOV-2001
Time Stamp:	19:32:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$1520
RAM confirmation Number	3284
Deposit Account	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)

1		Notice.pdf	76851 cd966feb5ae502273211ef997b542cc33aa631cc	yes	2

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Notice of Appeal Filed	1	1
Extension of Time	2	2

Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	8343 9c633434895925253a59765c4a507d5c6c13ab41	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	85194		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No.: 594728818US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Shin et al.

Application No.:	10/045,625	Confirmation No.:	1053
Filed:	November 07, 2001	Art Unit:	2616
For: METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS		Examiner:	Steven Nguyen

APPELLANT'S BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on August 6, 2007.

The fees required under 37 C.F.R. § 41.20(b)(2) and any required petition for extension of time for filing this brief and fees therefore are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37:

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I. REAL PARTY IN INTEREST

The real party of interest is Silicon Image, Inc.

II. RELATED APPEALS AND INTERFERENCES

The appellant, the appellant's legal representative, and the real party in interest are unaware of any appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 24 claims pending in the application.

B. Current Status of Claims

1. Claims canceled: None.

2. Claims withdrawn from consideration but not canceled: None.

3. Claims pending: 1-24.

4. Claims allowed: None.

5. Claims rejected: 1-24.

C. Claims On Appeal

The claims on appeal are claims 1-24.

IV. STATUS OF AMENDMENTS

The appellant has not filed any amendments after the last Office Action of April 6, 2007.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claimed subject matter is directed to a method and device for transmitting synchronization symbols that include an indication of a type of packet to be transmitted after the synchronization symbol.

Independent claim 1:

Independent claim 1 is directed to a method for transmitting packet types of packets. The method receives a packet having symbols, and identifies a packet type of the packet. The method transmits a synchronization symbol that corresponds to the identified packet type. The synchronization symbol provides synchronization information, and each packet type has a different synchronization symbol. The method then transmits the symbols of the received packet.

Support may be found, for example, in paragraphs [0094], [0095], [0099] and Figure 9A of the specification.

Independent claim 9:

Independent claim 9 is directed to a method for identifying packet types of packets of symbols. The method receives a synchronization symbol indicating a packet type, where each packet type has a different synchronization symbol. The method receives a packet of symbols, and indicates that the received packet of symbols has the packet type of the received synchronization symbol.

Support may be found, for example, in paragraphs [0094], [0095], [0097], [0098] and Figure 9A of the specification

Independent claim 16:

Independent claim 16 is directed to a communications device for transmitting packet types of packets. The device includes an identification component that identifies

a packet type of a packet of symbols. The device also includes a transmission component that transmits a synchronization symbol that corresponds to the identified packet type. The synchronization symbol provides synchronization information. Each packet type has a different synchronization symbol. The transmission component also transmits the symbols of the packet.

Support may be found, for example, in paragraphs [0094], [00101], [00102] and Figure 9C of the specification.

VI. GROUNDS OF REJECTION TO BE REVIEWED UPON APPEAL

A. The Examiner's Rejections

Claims 9-15 stand rejected under 35 U.S.C. 102(b) in view of U.S. Patent No. 5,703,875 to Burnett. Claims 1-8 and 16-24 stand rejected under 35 U.S.C. 103(a) in view of U.S. Patent No. 5,703,875 to Burnett and U.S. Patent No. 6,172,990 to Deb et al.

B. The Issues on Appeal

There are two grounds of rejection to be reviewed on appeal:

1. Whether Burnett discloses synchronization symbols that correspond and/or indicate a packet type of a transmitted packet.

2. Whether the combination of Burnett and Deb disclose synchronization symbols that correspond and/or indicate a packet type of a transmitted packet.

VII. ARGUMENTS

A. Rejections under 35 U.S.C. § 102(b)

1. Legal requirements for anticipation

35 U.S.C. § 102(b) provides:

> A person shall be entitled to a patent unless (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

As noted by the Federal Circuit, " A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

2. The Burnett Reference

Burnett is directed to an integrated control and data message network that contains a "switch for communicating short control messages and longer data messages" (Burnett at Abstract). As disclosed in Burnett:

> ...when data is sent over a link 23c, e.g., from a first switch 10a to a second switch 10b (or from a sender 21 to a switch 10a), it is necessary to inform the receiving switch 10b whether control message words or data message words are being transmitted. Various approaches may be used to accomplish this. One approach is for the first switch 10a to send a state control word to the second switch when the first switch 10a is about to begin sending a message. The state control word indicates to the second switch 10b which FIFO buffer 12, 13 to store the input words into... (Burnett at 2: 40-49, emphasis added).

Thus, Burnett discloses that a "state control word" is used in the control and data message network to indicate in which buffer to store data and control messages.

3. Claims 9-16: Burnett does not teach each and every element of the claims

Claims 9-16 are taken as a group for the purposes of this appeal[1]

Independent claim 9 (and dependent claims 10-16) recites a method for identifying packet types of packets, comprising, inter *alia*:

> "receiving a synchronization symbol indicating a packet type, each packet type having a different synchronization symbol."

Burnett does not disclose synchronization symbols that correspond to (or indicate) packet types. Instead, Burnett discloses a "state control word." The Office Action incorrectly equates the state control word disclosed by Burnett with the synchronization symbol as recited in claim 9. For example, at paragraph 7, the Office Action asserts "see col. 2, lines 40 to col. 3, lines 35, state control word used to synchronize the state of transmitting/receiving between the sender and receiver in order to store the information at the receiver." This is incorrect. The "state control wordas disclosed by Burnett are used to "signal the start and end of a message" (Burnett at 3: 20-21) and to specify whether data or control message words are being transmitted. The state control words are not used for synchronization, i.e., the coordination of events in time[2]. Indeed, Burnett discloses that a "clock signal may be sent along with the data, or other self-clocking schemes may be employed" (Burnett 3: 42-44). The sending of a

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[1] The appellant has grouped the claims to simplify issues on appeal. The appellant, however, does not admit that the claims in any group stand or fall together for purposes other than this appeal. In particular, the appellant reserves the right to argue the patentability of each claim separately in a subsequent action, such as reopened prosecution or litigation.

[2] The appellant's specification provides an example of synchronization at Paragraph [0094]: "A synchronization signal is typically used by the physical layer to help ensure correct alignment of symbols. A transmitting communications node periodically transmits synchronization primitives so that the receiving communications node can properly align with that synchronization primitive. When a communications node receives a synchronization primitive, it knows that the primitive is correctly aligned on a symbol boundary. The use of multiple synchronization primitives allows for encoding packet type within a synchronization primitive."

clock signal obviates the need to perform any synchronization with the state control words.

Thus, a "state control word," as intended by Burnett, is transmitted by the first switch to instruct the second switch into which buffer subsequently transmitted packets are to be stored and to signal the start and end of a message. There is no indication or suggestion in Burnett that the state control words disclosed by Burnett are involved in any synchronization. Instead, Burnett discloses other mechanisms (e.g., transmission of a clock signal) that perform synchronization.

Thus, Burnett does not teach each and every element of independent claim 9. For at least these reasons, claim 9 and dependent claims 10-16 are patentable over Burnett.

B. Rejections under 35 U.S.C. § 103(a)

1. Legal requirements for obviousness

35 U.S.C. § 103(a) provides:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Supreme Court in *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 U.S.P.Q. 459 (1966), stated:

> Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined. Such secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin

of the subject matter sought to be patented. As indicia of obviousness or nonobviousness, these inquires may have relevancy.

The recent Supreme Court decision in *KSR Int'l v. Teleflex, Inc.*, 550 U.S. ___ (2007) reaffirmed the holdings of *Graham*, and clarified several aspects of the manner in which obviousness should be determined. *KSR*, p. 11. First, "the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results," but "when the prior art teaches away from combining certain elements, discovery of a successful means of combining them is more likely to be nonobvious." *KSR*, p. 12. Second, "a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art," rather, "it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does." *KSR*, p. 14-15. The Court recognizes that many significant advances will combine familiar elements: "inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known." *KSR*, p. 15.

Following the decision in *KSR*, the USPTO issued a memorandum to all Examiners. The memorandum directs Examiners to continue to determine why a person of ordinary skill in the art would make the combination, "in formulating a rejection under 35 U.S.C. 103(a) based upon a combination of prior art elements, it remains necessary to identify the reason why a person of ordinary skill in the art would have combined the prior art elements in the manner claimed." "Supreme Court decision on *KSR Int'l v. Teleflex, Inc.*," May 3, 2007, p. 2.

Additionally, *KSR* instructs that "one of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims" *KSR*, p. 16.

2. The applied references

Deb discloses a media access control micro-RISC stream processor, including methods for "processing packet data received from a physical layer" (Deb at Abstract). Deb seeks to address the "need for methods and apparatuses for media access control layer processing that is well suited to increase transmit and receive packet processing rates while reducing a host CPU's processing burden" (Deb at 3: 55-60).

As described above, Burnett discloses an integrated control and data message network that contains a "switch for communicating short control messages and longer data messages" and uses "state control words" to indicate the start and end of a transmission of either control messages or data messages (Burnett at Abstract).

3. Claims 1-8, 16-24: The combination of Burnett and Deb does not teach each and every element of the claims

Claims 1-8 and 16-24 are taken as a group for the purposes of this appeal.

Independent claim 1 stands rejected over Deb and Burnett. Claim 1 recites a method for transmitting packet types of packets, comprising, *inter alia*:

> ...transmitting a synchronization symbol that corresponds to the identified packet type, wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol.

Similarly, independent claim 16 recites a communications device for transmitting packet types of packets, comprising, *inter alia*:

> ...a transmission component that transmits a synchronization symbol that corresponds to the identified packet type, the transmitted synchronization symbol providing synchronization information and each packet type having a different synchronization symbol, and that transmits the symbols of the packet.

Both independent claims describe transmitting or receiving one or more synchronization symbol(s) that correspond to an identified packet type. As described above, Burnett does not disclose transmitting or receiving synchronization symbols that

correspond to packet type. Deb also does not disclose synchronization symbols that correspond to (or indicate) packet types. Instead, Deb is concerned with methods of processing packet data received from a physical layer, including "appending [a] data structure to packet data before the packet is streamed to the upper layer" (Deb at Abstract). Deb does not disclose any techniques related to synchronization. In fact, there is no instance of the words "synchronization," "sync" or "clock" in the disclosure of Deb.

Thus, because each reference individually fails to disclose or suggest the transmission of a synchronization symbol that corresponds to a packet type, it is impossible for the combination of references to disclose or suggest transmitting or receiving a synchronization symbol that corresponds to a packet type. Each of the appellant's claims recites features that relate synchronization symbols with packet types. Therefore, for at least these reasons, the appellant respectfully submits that claims 1-8 and 16-24 are patentable over the combination of Burnett and Deb.

4. Claims 1-8, 16-24: There is no suggestion or motivation to combine reference teachings

Furthermore, there is no teaching or suggestion in the references or the prior art that would motivate one of ordinary skill to combine the Deb and Burnett references. The Office Action, at paragraph 6, asserts that "Since, a method for identifying a type of packet is well know and expected in the art. Therefore, it would have been obvious to one or ordinary skill in the art to apply a method for identifying a type of packet as disclosed by Deb into Burnett's system and method. The motivation would have been to reduce delay time when transmitting a packet from source to destination." The appellant respectfully disagrees.

First, the system of Deb does not attempt to reduce delay time in transmitting a packet from source to destination. The system of Deb attempts to reduce the processing time once packets are received. Thus, the motivation asserted by the Office

Action is incorrect and one of ordinary skill in the art would not look to Deb for that purpose.

Second, Burnett clearly teaches away from such a combination. As described above, Burnett discloses a system that sends "state control words" before transmitting data to a switch that instructs the switch to transmit the data into different buffers according to indicators within the state control words. That is, the system of Burnett does not lack a mechanism for identifying received packet data, as packets are stored in buffers according to type as identified within the state control words. Thus, any additional component from Deb would be unnecessary.

Additionally, the combination of Deb and Burnett addresses neither the problem solved by the appellant's claimed technology, nor the solution. For example, paragraph [0094] of the appellant's specification discloses: "The time needed to transmit a packet through the switching network may be longer than the time needed to store the data of the packet in a memory-based data store device. The rapid detection of packet type through a synchronization primitive, rather than through a packet header, can reduce the processing time of a switch." There is no disclosure in Burnett that processing time within a switch is burdensome to Burnett's system. Similarly, Deb is also not concerned with processing time through a switch. Instead, Deb is concerned with the processing of packet reception in a physical layer. The combination of Burnett and Deb discloses neither the claimed subject matter nor any problems addressed by the claimed subject matter. Thus, according to page 16 of *KSR,* the claimed subject matter would not be obvious over the combination of Burnett and Deb, because there was not a "known problem for which there was an obvious solution encompassed by the patent's claims."

Therefore, the appellant contends that there is no suggestion in the cited references, or knowledge in the art, that would motivate one of ordinary skill in the art to combine Deb and Burnett. For at least these reasons, the appellant respectfully asserts that claims 1-8 and 16-24 are patentable over the combination of references. The

appellant respectfully requests that the Examiner's rejections under 35 U.S.C. § 103 be reversed based on failure to establish a *prima facie* case of obviousness.

In sum, neither Burnett nor Deb taken alone teaches each and every element of the independent claims. Furthermore, any combination of the two references is improper, because the combination does not teach each and every element of the independent claims and one or ordinary skill in the art would not be motivated to make such a combination to arrive at the claimed technology.

VIII. CLAIMS APPENDIX

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

IX. EVIDENCE APPENDIX

The evidence appendix is attached hereto as Appendix B.

X. RELATED PROCEEDINGS APPENDIX

The related proceedings appendix is attached hereto as Appendix C.

The appellant encloses payment of all fees believed to owing in connection with this paper by charge to EFT Account SEA1PIRM. However, if additional fees are due, please charge our Deposit Account No. 50-0665, under Order No. 594728813US from which the undersigned is authorized to draw.

Dated: October 8, 2007

Respectfully submitted,

By_____

Michael J. Smith
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APPENDIX A: Claims

Claims Involved in the Appeal of Application Serial No. 10/045,625

1. (Original) A method for transmitting packet types of packets, the method comprising:

receiving a packet having symbols;

identifying a packet type of the packet;

transmitting a synchronization symbol that corresponds to the identified packet type, wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol; and

transmitting the symbols of the received packet.

2. (Original) The method of claim 1 wherein the symbols of the packet include in-band symbols and the synchronization symbols are out-of-band symbols.

3. (Original) The method of claim 2 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

4. (Original) The method of claim 1 wherein the synchronization symbol is transmitted before transmitting the symbols of the packet.

5. (Original) The method of claim 1 wherein the packet has a header with a field that indicates packet type and the identifying of the packet type includes checking the field of the header that indicates packet type.

6. (Original) The method of claim 1 wherein the packet types include a data packet.

7. (Original) The method of claim 1 wherein the packet types include a control packet.

8. (Original) The method of claim 1 wherein the symbols are transmitted to a switch network.

9. (Original) A method for identifying packet types of packets of symbols, the method comprising:

receiving a synchronization symbol indicating a packet type, each packet type having a different synchronization symbol;

receiving a packet of symbols; and

indicating that the received packet of symbols has the packet type of the received synchronization symbol.

10. (Original) The method of claim 9 wherein the symbols of the packets include in-band symbols and the synchronization symbols are out-of-band symbols.

11. (Original) The method of claim 10 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

12. (Original) The method of claim 9 wherein the synchronization symbol is received before the symbols of the packet are received.

13. (Original) The method of claim 9 wherein the packet types include a data packet.

14. (Original) The method of claim 9 wherein the packet types include a control packet.

15. (Original) The method of claim 9 wherein the symbols are received from a switch.

16. (Original) A communications device for transmitting packet types of packets, comprising:

an identification component that identifies a packet type of a packet of symbols; and

a transmission component that transmits a synchronization symbol that corresponds to the identified packet type, the transmitted synchronization symbol providing synchronization information and each packet type having a different synchronization symbol, and that transmits the symbols of the packet.

17. (Original) The communications device of claim 16 wherein the symbols of the packet include in-band symbols and the synchronization symbols are out-of-band symbols.

18. (Original) The communications device of claim 17 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

19. (Original) The communications device of claim 16 wherein the synchronization symbol is transmitted before transmitting the symbols of the packet.

20. (Original) The communications device of claim 16 wherein the packet has a header with a field that indicates packet type and the identification component checks the field of the header that indicates packet type.

21. (Original) The communications device of claim 16 wherein the packet types include a data packet.

22. (Original) The communications device of claim 16 wherein the packet types include a control packet.

23. (Original) The communications device of claim 16 wherein the symbols are transmitted to a switch network.

24. (Original) The communications device of claim 16 wherein the communications device is part of a storage area network.

APPENDIX B: Evidence

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

APPENDIX C: Related Proceedings

There are no related proceedings.

Electronic Patent Application Fee Transmittal

Application Number:	10045625
Filing Date:	07-Nov-2001
Title of Invention:	Method and system for integrating packet type information with synchronization symbols
First Named Inventor/Applicant Name:	Yeshik Shin
Filer:	Robert G. Woolston/Nicole Fye
Attorney Docket Number:	59472-8818US

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Filing a brief in support of an appeal	1402	1	510	510
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 2 months with $0 paid	1252	1	460	460
Miscellaneous:				
		Total in USD ($)		**970**

Electronic Acknowledgement Receipt

EFS ID:	2552365
Application Number:	10045625
International Application Number:	
Confirmation Number:	1053
Title of Invention:	Method and system for integrating packet type information with synchronization symbols
First Named Inventor/Applicant Name:	Yeshik Shin
Customer Number:	63170
Filer:	Robert G. Woolston/Nicole Fye
Filer Authorized By:	Robert G. Woolston
Attorney Docket Number:	59472-8818US
Receipt Date:	05-DEC-2007
Filing Date:	07-NOV-2001
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)

1		2007-12-05AppealBrief.pdf	739076 c14fa7cb104e35d759a16e8b8f377395e51f45a0	yes	22

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Miscellaneous Incoming Letter	1	1
Extension of Time	2	2
Appeal Brief Filed	3	22

Warnings:

Information:

2	Fee Worksheet (PTO-06)	fee-info.pdf	8357 e79a3e62f640571116d08c5a2c3104af0bf93b38c	no	2

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

TRANSMITTAL OF APPEAL BRIEF			Docket No. 594728818US
In re Application of: Shin et al.			
Application No. 10/045,625-Conf. #1053	Filing Date November 7, 2001	Examiner S. Nguyen	Group Art Unit 2616
Invention: METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS			

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: August 6, 2007 .

The fee for filing this Appeal Brief is $ 510.00 .

[X] Large Entity [ ] Small Entity

[X] A petition for extension of time is also enclosed.

The fee for the extension of time is $ 460.00 .

[ ] A check in the amount of _____ is enclosed.

[ ] Charge the amount of the fee to Deposit Account No. _____ .
This sheet is submitted in duplicate.

[X] Payment by EFT Account No. SEA1PIRM.

[X] The Director is hereby authorized to charge any additional fees that may be required or credit any overpayment to Deposit Account No. 50-0665 .

Dated: December 5, 2007

Michael J. Smith
Attorney Reg. No. : 56,702
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LENOVO EXHIBIT 1002 - 315/553

PTO/SB/22 (11-07)
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PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) FY 2008 *(Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).)*	Docket Number (Optional) 594728818US
Application Number 10/045,625-Conf. #1053	Filed November 7, 2001
For METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS	
Art Unit 2616	Examiner S. Nguyen

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

		Fee	Small Entity Fee	
☐	One month (37 CFR 1.17(a)(1))	$120	$60	$
☒	Two months (37 CFR 1.17(a)(2))	$460	$230	$ 460.00
☐	Three months (37 CFR 1.17(a)(3))	$1050	$525	$
☐	Four months (37 CFR 1.17(a)(4))	$1640	$820	$
☐	Five months (37 CFR 1.17(a)(5))	$2230	$1115	$

☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☒ Payment by EFT Account No. SEA1PIRM.

☒ The Director is hereby authorized to charge additional fees that may be required, or credit overpayment, to Deposit Account Number 50-0665 .

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☒ attorney or agent of record. Registration Number 56,702

☐ attorney or agent under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____



Signature — December 5, 2007 (Date)

Michael J. Smith (Typed or printed name) — (206) 359-8000 (Telephone Number)

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☒ Total of 1 forms are submitted.

LENOVO EXHIBIT 1002 - 316/553

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,625	11/07/2001	Yeshik Shin	59472-8818US	1053

63170 7590 12/18/2007

SILICON IMAGE, INC.
P.O. BOX 2168
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EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 12/18/2007

Please find below and/or attached an Office communication concerning this application or proceeding.

LENOVO EXHIBIT 1002 - 317/553

Notification of Non-Compliant Appeal Brief (37 CFR 41.37)	Application No.	Applicant(s)	
	10/045,625	SHIN ET AL.	
	Examiner	Art Unit	
	Steven Nguyen	2619	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The Appeal Brief filed on *05 December 2007* is defective for failure to comply with one or more provisions of 37 CFR 41.37.

To avoid dismissal of the appeal, applicant must file anamended brief or other appropriate correction (see MPEP 1205.03) within **ONE MONTH or THIRTY DAYS** from the mailing date of this Notification, whichever is longer. **EXTENSIONS OF THIS TIME PERIOD MAY BE GRANTED UNDER 37 CFR 1.136.**

1. ☐ The brief does not contain the items required under 37 CFR 41.37(c), or the items are not under the proper heading or in the proper order.

2. ☐ The brief does not contain a statement of the status of all claims, (e.g., rejected, allowed, withdrawn, objected to, canceled), or does not identify the appealed claims (37 CFR 41.37(c)(1)(iii)).

3. ☐ At least one amendment has been filed subsequent to the final rejection, and the brief does not contain a statement of the status of each such amendment (37 CFR 41.37(c)(1)(iv)).

4. ☐ (a) The brief does not contain a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, referring to the specification by page and line number and to the drawings, if any, by reference characters; and/or (b) the brief fails to: (1) identify, for each independent claim involved in the appeal and for each dependent claim argued separately, every means plus function and step plus function under 35 U.S.C. 112, sixth paragraph, and/or (2) set forth the structure, material, or acts described in the specification as corresponding to each claimed function with reference to the specification by page and line number, and to the drawings, if any, by reference characters (37 CFR 41.37(c)(1)(v)).

5. ☐ The brief does not contain a concise statement of each ground of rejection presented for review (37 CFR 41.37(c)(1)(vi))

6. ☐ The brief does not present an argument under a separate heading for each ground of rejection on appeal (37 CFR 41.37(c)(1)(vii)).

7. ☐ The brief does not contain a correct copy of the appealed claims as an appendix thereto (37 CFR 41.37(c)(1)(viii)).

8. ☐ The brief does not contain copies of the evidence submitted under 37 CFR 1.130, 1.131, or 1.132 or of any other evidence entered by the examiner **and relied upon by appellant in the appeal**, along with a statement setting forth where in the record that evidence was entered by the examiner, as an appendix thereto (37 CFR 41.37(c)(1)(ix)).

9. ☐ The brief does not contain copies of the decisions rendered by a court or the Board in the proceeding identified in the Related Appeals and Interferences section of the brief as an appendix thereto (37 CFR 41.37(c)(1)(x)).

10. ☒ Other (including any explanation in support of the above items):

The brief filed December 5, 2007, is defective because it is unsigned. A ratification properly signed is required .

Bridget C. Monroe

BRIDGET C. MONROE
PATENT APPEAL CENTER SPECIALIST

LENOVO EXHIBIT 1002 - 318/553

Docket No.: 594728818US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Shin et al.

Application No.:	10/045,625	Confirmation No.:	1053
Filed:	November 07, 2001	Art Unit:	2616
For: METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS		Examiner:	Steven Nguyen

APPELLANT'S BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on August 6, 2007.

The fees required under 37 C.F.R. § 41.20(b)(2) and any required petition for extension of time for filing this brief and fees therefore are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37:

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I. REAL PARTY IN INTEREST

The real party of interest is Silicon Image, Inc.

II. RELATED APPEALS AND INTERFERENCES

The appellant, the appellant's legal representative, and the real party in interest are unaware of any appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 24 claims pending in the application.

B. Current Status of Claims

1. Claims canceled: None.

2. Claims withdrawn from consideration but not canceled: None.

3. Claims pending: 1-24.

4. Claims allowed: None.

5. Claims rejected: 1-24.

C. Claims On Appeal

The claims on appeal are claims 1-24.

IV. STATUS OF AMENDMENTS

The appellant has not filed any amendments after the last Office Action of April 6, 2007.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claimed subject matter is directed to a method and device for transmitting synchronization symbols that include an indication of a type of packet to be transmitted after the synchronization symbol.

Independent claim 1:

Independent claim 1 is directed to a method for transmitting packet types of packets. The method receives a packet having symbols, and identifies a packet type of the packet. The method transmits a synchronization symbol that corresponds to the identified packet type. The synchronization symbol provides synchronization information, and each packet type has a different synchronization symbol. The method then transmits the symbols of the received packet.

Support may be found, for example, in paragraphs [0094], [0095], [0099] and Figure 9A of the specification.

Independent claim 9:

Independent claim 9 is directed to a method for identifying packet types of packets of symbols. The method receives a synchronization symbol indicating a packet type, where each packet type has a different synchronization symbol. The method receives a packet of symbols, and indicates that the received packet of symbols has the packet type of the received synchronization symbol.

Support may be found, for example, in paragraphs [0094], [0095], [0097], [0098] and Figure 9A of the specification

Independent claim 16:

Independent claim 16 is directed to a communications device for transmitting packet types of packets. The device includes an identification component that identifies

a packet type of a packet of symbols. The device also includes a transmission component that transmits a synchronization symbol that corresponds to the identified packet type. The synchronization symbol provides synchronization information. Each packet type has a different synchronization symbol. The transmission component also transmits the symbols of the packet.

Support may be found, for example, in paragraphs [0094], [00101], [00102] and Figure 9C of the specification.

VI. GROUNDS OF REJECTION TO BE REVIEWED UPON APPEAL

A. The Examiner's Rejections

Claims 9-15 stand rejected under 35 U.S.C. 102(b) in view of U.S. Patent No. 5,703,875 to Burnett. Claims 1-8 and 16-24 stand rejected under 35 U.S.C. 103(a) in view of U.S. Patent No. 5,703,875 to Burnett and U.S. Patent No. 6,172,990 to Deb et al.

B. The Issues on Appeal

There are two grounds of rejection to be reviewed on appeal:

1. Whether Burnett discloses synchronization symbols that correspond and/or indicate a packet type of a transmitted packet.

2. Whether the combination of Burnett and Deb disclose synchronization symbols that correspond and/or indicate a packet type of a transmitted packet.

VII. ARGUMENTS

A. Rejections under 35 U.S.C. § 102(b)

1. Legal requirements for anticipation

35 U.S.C. § 102(b) provides:

> A person shall be entitled to a patent unless (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

As noted by the Federal Circuit, " A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

2. The Burnett Reference

Burnett is directed to an integrated control and data message network that contains a "switch for communicating short control messages and longer data messages" (Burnett at Abstract). As disclosed in Burnett:

> ...when data is sent over a link 23c, e.g., from a first switch 10a to a second switch 10b (or from a sender 21 to a switch 10a), it is necessary to inform the receiving switch 10b whether control message words or data message words are being transmitted. Various approaches may be used to accomplish this. One approach is for the first switch 10a to send a state control word to the second switch when the first switch 10a is about to begin sending a message. The state control word indicates to the second switch 10b which FIFO buffer 12, 13 to store the input words into... (Burnett at 2: 40-49, emphasis added).

Thus, Burnett discloses that a "state control word" is used in the control and data message network to indicate in which buffer to store data and control messages.

3. Claims 9-16: Burnett does not teach each and every element of the claims

Claims 9-16 are taken as a group for the purposes of this appeal[1]

Independent claim 9 (and dependent claims 10-16) recites a method for identifying packet types of packets, comprising, inter *alia*:

> "receiving a synchronization symbol indicating a packet type, each packet type having a different synchronization symbol."

Burnett does not disclose synchronization symbols that correspond to (or indicate) packet types. Instead, Burnett discloses a "state control word." The Office Action incorrectly equates the state control word disclosed by Burnett with the synchronization symbol as recited in claim 9. For example, at paragraph 7, the Office Action asserts "see col. 2, lines 40 to col. 3, lines 35, state control word used to synchronize the state of transmitting/receiving between the sender and receiver in order to store the information at the receiver." This is incorrect. The "state control wordas disclosed by Burnett are used to "signal the start and end of a message" (Burnett at 3: 20-21) and to specify whether data or control message words are being transmitted. The state control words are not used for synchronization, i.e., the coordination of events in time[2]. Indeed, Burnett discloses that a "clock signal may be sent along with the data, or other self-clocking schemes may be employed" (Burnett 3: 42-44). The sending of a

---

[1] The appellant has grouped the claims to simplify issues on appeal. The appellant, however, does not admit that the claims in any group stand or fall together for purposes other than this appeal. In particular, the appellant reserves the right to argue the patentability of each claim separately in a subsequent action, such as reopened prosecution or litigation.

[2] The appellant's specification provides an example of synchronization at Paragraph [0094]: "A synchronization signal is typically used by the physical layer to help ensure correct alignment of symbols. A transmitting communications node periodically transmits synchronization primitives so that the receiving communications node can properly align with that synchronization primitive. When a communications node receives a synchronization primitive, it knows that the primitive is correctly aligned on a symbol boundary. The use of multiple synchronization primitives allows for encoding packet type within a synchronization primitive."

clock signal obviates the need to perform any synchronization with the state control words.

Thus, a "state control word," as intended by Burnett, is transmitted by the first switch to instruct the second switch into which buffer subsequently transmitted packets are to be stored and to signal the start and end of a message. There is no indication or suggestion in Burnett that the state control words disclosed by Burnett are involved in any synchronization. Instead, Burnett discloses other mechanisms (e.g., transmission of a clock signal) that perform synchronization.

Thus, Burnett does not teach each and every element of independent claim 9. For at least these reasons, claim 9 and dependent claims 10-16 are patentable over Burnett.

B. Rejections under 35 U.S.C. § 103(a)

1. Legal requirements for obviousness

35 U.S.C. § 103(a) provides:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Supreme Court in *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 U.S.P.Q. 459 (1966), stated:

> Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined. Such secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin

of the subject matter sought to be patented. As indicia of obviousness or nonobviousness, these inquires may have relevancy.

The recent Supreme Court decision in *KSR Int'l v. Teleflex, Inc.*, 550 U.S. ___ (2007) reaffirmed the holdings of *Graham*, and clarified several aspects of the manner in which obviousness should be determined. *KSR*, p. 11. First, "the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results," but "when the prior art teaches away from combining certain elements, discovery of a successful means of combining them is more likely to be nonobvious." *KSR*, p. 12. Second, "a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art," rather, "it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does." *KSR*, p. 14-15. The Court recognizes that many significant advances will combine familiar elements: "inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known." *KSR*, p. 15.

Following the decision in *KSR*, the USPTO issued a memorandum to all Examiners. The memorandum directs Examiners to continue to determine why a person of ordinary skill in the art would make the combination, "in formulating a rejection under 35 U.S.C. 103(a) based upon a combination of prior art elements, it remains necessary to identify the reason why a person of ordinary skill in the art would have combined the prior art elements in the manner claimed." "Supreme Court decision on *KSR Int'l v. Teleflex, Inc.*," May 3, 2007, p. 2.

Additionally, *KSR* instructs that "one of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims" *KSR*, p. 16.

2. The applied references

Deb discloses a media access control micro-RISC stream processor, including methods for "processing packet data received from a physical layer" (Deb at Abstract). Deb seeks to address the "need for methods and apparatuses for media access control layer processing that is well suited to increase transmit and receive packet processing rates while reducing a host CPU's processing burden" (Deb at 3: 55-60).

As described above, Burnett discloses an integrated control and data message network that contains a "switch for communicating short control messages and longer data messages" and uses "state control words" to indicate the start and end of a transmission of either control messages or data messages (Burnett at Abstract).

3. Claims 1-8, 16-24: The combination of Burnett and Deb does not teach each and every element of the claims

Claims 1-8 and 16-24 are taken as a group for the purposes of this appeal.

Independent claim 1 stands rejected over Deb and Burnett. Claim 1 recites a method for transmitting packet types of packets, comprising, *inter alia*:

> ...transmitting a synchronization symbol that corresponds to the identified packet type, wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol.

Similarly, independent claim 16 recites a communications device for transmitting packet types of packets, comprising, *inter alia*:

> ...a transmission component that transmits a synchronization symbol that corresponds to the identified packet type, the transmitted synchronization symbol providing synchronization information and each packet type having a different synchronization symbol, and that transmits the symbols of the packet.

Both independent claims describe transmitting or receiving one or more synchronization symbol(s) that correspond to an identified packet type. As described above, Burnett does not disclose transmitting or receiving synchronization symbols that

correspond to packet type. Deb also does not disclose synchronization symbols that correspond to (or indicate) packet types. Instead, Deb is concerned with methods of processing packet data received from a physical layer, including "appending [a] data structure to packet data before the packet is streamed to the upper layer" (Deb at Abstract). Deb does not disclose any techniques related to synchronization. In fact, there is no instance of the words "synchronization," "sync" or "clock" in the disclosure of Deb.

Thus, because each reference individually fails to disclose or suggest the transmission of a synchronization symbol that corresponds to a packet type, it is impossible for the combination of references to disclose or suggest transmitting or receiving a synchronization symbol that corresponds to a packet type. Each of the appellant's claims recites features that relate synchronization symbols with packet types. Therefore, for at least these reasons, the appellant respectfully submits that claims 1-8 and 16-24 are patentable over the combination of Burnett and Deb.

4. Claims 1-8, 16-24: There is no suggestion or motivation to combine reference teachings

Furthermore, there is no teaching or suggestion in the references or the prior art that would motivate one of ordinary skill to combine the Deb and Burnett references. The Office Action, at paragraph 6, asserts that "Since, a method for identifying a type of packet is well know and expected in the art. Therefore, it would have been obvious to one or ordinary skill in the art to apply a method for identifying a type of packet as disclosed by Deb into Burnett's system and method. The motivation would have been to reduce delay time when transmitting a packet from source to destination." The appellant respectfully disagrees.

First, the system of Deb does not attempt to reduce delay time in transmitting a packet from source to destination. The system of Deb attempts to reduce the processing time once packets are received. Thus, the motivation asserted by the Office

Action is incorrect and one of ordinary skill in the art would not look to Deb for that purpose.

Second, Burnett clearly teaches away from such a combination. As described above, Burnett discloses a system that sends "state control words" before transmitting data to a switch that instructs the switch to transmit the data into different buffers according to indicators within the state control words. That is, the system of Burnett does not lack a mechanism for identifying received packet data, as packets are stored in buffers according to type as identified within the state control words. Thus, any additional component from Deb would be unnecessary.

Additionally, the combination of Deb and Burnett addresses neither the problem solved by the appellant's claimed technology, nor the solution. For example, paragraph [0094] of the appellant's specification discloses: "The time needed to transmit a packet through the switching network may be longer than the time needed to store the data of the packet in a memory-based data store device. The rapid detection of packet type through a synchronization primitive, rather than through a packet header, can reduce the processing time of a switch." There is no disclosure in Burnett that processing time within a switch is burdensome to Burnett's system. Similarly, Deb is also not concerned with processing time through a switch. Instead, Deb is concerned with the processing of packet reception in a physical layer. The combination of Burnett and Deb discloses neither the claimed subject matter nor any problems addressed by the claimed subject matter. Thus, according to page 16 of *KSR,* the claimed subject matter would not be obvious over the combination of Burnett and Deb, because there was not a "known problem for which there was an obvious solution encompassed by the patent's claims."

Therefore, the appellant contends that there is no suggestion in the cited references, or knowledge in the art, that would motivate one of ordinary skill in the art to combine Deb and Burnett. For at least these reasons, the appellant respectfully asserts that claims 1-8 and 16-24 are patentable over the combination of references. The

appellant respectfully requests that the Examiner's rejections under 35 U.S.C. § 103 be reversed based on failure to establish a *prima facie* case of obviousness.

In sum, neither Burnett nor Deb taken alone teaches each and every element of the independent claims. Furthermore, any combination of the two references is improper, because the combination does not teach each and every element of the independent claims and one or ordinary skill in the art would not be motivated to make such a combination to arrive at the claimed technology.

VIII. CLAIMS APPENDIX

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

IX. EVIDENCE APPENDIX

The evidence appendix is attached hereto as Appendix B.

X. RELATED PROCEEDINGS APPENDIX

The related proceedings appendix is attached hereto as Appendix C.

The appellant encloses payment of all fees believed to owing in connection with this paper by charge to EFT Account SEA1PIRM. However, if additional fees are due, please charge our Deposit Account No. 50-0665, under Order No. 594728813US from which the undersigned is authorized to draw.

Dated: ~~October 8, 2007~~ January 18, 2008

Respectfully submitted,

By _____
~~Michael J. Smith~~ Stephen C. Bishop
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LENOVO EXHIBIT 1002 - 332/553

APPENDIX A: Claims

Claims Involved in the Appeal of Application Serial No. 10/045,625

1. (Original) A method for transmitting packet types of packets, the method comprising:

receiving a packet having symbols;

identifying a packet type of the packet;

transmitting a synchronization symbol that corresponds to the identified packet type, wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol; and

transmitting the symbols of the received packet.

2. (Original) The method of claim 1 wherein the symbols of the packet include in-band symbols and the synchronization symbols are out-of-band symbols.

3. (Original) The method of claim 2 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

4. (Original) The method of claim 1 wherein the synchronization symbol is transmitted before transmitting the symbols of the packet.

5. (Original) The method of claim 1 wherein the packet has a header with a field that indicates packet type and the identifying of the packet type includes checking the field of the header that indicates packet type.

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6. (Original) The method of claim 1 wherein the packet types include a data packet.

7. (Original) The method of claim 1 wherein the packet types include a control packet.

8. (Original) The method of claim 1 wherein the symbols are transmitted to a switch network.

9. (Original) A method for identifying packet types of packets of symbols, the method comprising:

receiving a synchronization symbol indicating a packet type, each packet type having a different synchronization symbol;

receiving a packet of symbols; and

indicating that the received packet of symbols has the packet type of the received synchronization symbol.

10. (Original) The method of claim 9 wherein the symbols of the packets include in-band symbols and the synchronization symbols are out-of-band symbols.

11. (Original) The method of claim 10 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

12. (Original) The method of claim 9 wherein the synchronization symbol is received before the symbols of the packet are received.

13. (Original) The method of claim 9 wherein the packet types include a data packet.

14. (Original) The method of claim 9 wherein the packet types include a control packet.

15. (Original) The method of claim 9 wherein the symbols are received from a switch.

16. (Original) A communications device for transmitting packet types of packets, comprising:

an identification component that identifies a packet type of a packet of symbols; and

a transmission component that transmits a synchronization symbol that corresponds to the identified packet type, the transmitted synchronization symbol providing synchronization information and each packet type having a different synchronization symbol, and that transmits the symbols of the packet.

17. (Original) The communications device of claim 16 wherein the symbols of the packet include in-band symbols and the synchronization symbols are out-of-band symbols.

18. (Original) The communications device of claim 17 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

19. (Original) The communications device of claim 16 wherein the synchronization symbol is transmitted before transmitting the symbols of the packet.

20. (Original) The communications device of claim 16 wherein the packet has a header with a field that indicates packet type and the identification component checks the field of the header that indicates packet type.

21. (Original) The communications device of claim 16 wherein the packet types include a data packet.

22. (Original) The communications device of claim 16 wherein the packet types include a control packet.

23. (Original) The communications device of claim 16 wherein the symbols are transmitted to a switch network.

24. (Original) The communications device of claim 16 wherein the communications device is part of a storage area network.

APPENDIX B: Evidence

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

APPENDIX C: Related Proceedings

There are no related proceedings.

Electronic Acknowledgement Receipt

EFS ID:	2741951
Application Number:	10045625
International Application Number:	
Confirmation Number:	1053
Title of Invention:	Method and system for integrating packet type information with synchronization symbols
First Named Inventor/Applicant Name:	Yeshik Shin
Customer Number:	63170
Filer:	Robert G. Woolston/Nicole Fye
Filer Authorized By:	Robert G. Woolston
Attorney Docket Number:	59472-8818US
Receipt Date:	18-JAN-2008
Filing Date:	07-NOV-2001
Time Stamp:	20:44:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		2008-01-18ResponseNonCompliantAppealBrief.pdf	744359 708b58d32ea6fa578f84ab8ff9dd814fcfb8dd33	yes	22

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Post Allowance Communication - Incoming	1	2
	Appeal Brief Filed	3	22
Warnings:			
Information:			
	Total Files Size (in bytes):	744359	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No.: 594728818US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Shin et al.

Application No.: 10/045,625 | Confirmation No.: 1053

Filed: November 7, 2001 | Art Unit: 2616

For: METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS | Examiner: Steven Nguyen

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Sir:

This paper is being filed in response to the Notification of Non-Compliant Appeal Brief mailed December 18, 2007, noting that the Appellant's Brief filed December 5, 2007, was defective because it was unsigned. Attached is a duplicate copy of the Appellant's Brief, as filed December 5, 2007. The attached duplicate copy of the Appellant's Brief includes the following corrections:

- Today's date, January 18, 2008, has been inserted manually on page 12.
- Appellant's Attorney, Stephen C. Bishop, has signed the brief on page 12.

Should you require anything further to satisfy the provisions of 37 CFR 41.37, please contact the undersigned.

Appellants believe no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-0665, under Order No. 594728818US, from which the undersigned is authorized to draw.

Dated: January 18, 2008

Respectfully submitted,

By _____

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,625	11/07/2001	Yeshik Shin	59472-8818US	1053

63170 7590 04/18/2008

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EXAMINER	
NGUYEN, STEVEN H D	
ART UNIT	**PAPER NUMBER**
2619	

MAIL DATE	DELIVERY MODE
04/18/2008	PAPER

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The time period for reply, if any, is set in the attached communication.

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/045,625
Filing Date: November 07, 2001
Appellant(s): SHIN ET AL.

Stephen C. Bishop
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 1/18/2008 appealing from the Office action mailed 3/6/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,172,990	Deb	9-2001
5,703,875	Burnett	12-1997

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 9-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Burnett (USP5703875).

Regarding claim 9, Burnet discloses a method for identifying packet types of packets of symbols comprising receiving a synchronization symbol indicating a packet type (Col. 2, lines 40-49), each packet type having a different synchronization symbol (Col. 2, lines 40-49); receiving a packet of symbols (Col. 2, lines 40-49); and indicating that the received packet of symbols has the packet type of the received synchronization symbol (Col. 2, lines 40-49, Fig 2, Ref 12 and 13, the state control word is used to stored the data or control packet into correct buffer).

Regarding claim 10, Burnett discloses the symbols of the packet include in-band symbols (Fig 2, ref 12) and the synchronization symbols are out-of-band symbols (Col. 2, lines 40-49, control words for control or data type message).

Regarding claim 11, Burnet discloses the in-band symbols are transition optimized (Fig 2, ref 12) and the out-of-band synchronization symbols are not transition optimized (Col. 2, lines 40-49).

Regarding claim 12, Burnet discloses the synchronization symbol is transmitted before transmitting the symbols of the packet (Col. 2, lines 40-49).

Regarding claim 13, Burnet discloses packet types include a data packet (Fig 2, Ref 13).

Regarding claim 14, Burnet discloses packet types include a control packet (Fig 2, Ref 12).

Regarding claim 15, Burnet discloses the symbols are received from a switch (Fig 1).

Claims 1-8 and 16-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burnett (USP 5703875) in view of Deb (USP 6172990).

Regarding claims 1 and 16, Burnet discloses a method for transmitting packet types of packets comprising the steps of receiving a packet having symbols, transmitting a synchronization symbol that corresponds to the identified packet type (Col. 2, lines 40-49), wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol; and transmitting the symbols of the received packet (Col. 2, lines 40-49, each type of message is associated with a different state control word and the state control world is transmitted before transmitting its associated message). However, Burnett does not fully disclose identifying a packet type of the packet based on the received packet. In the same field of endeavor, Deb discloses a method for receiving a packet and identified the type of received packet and transmitting appended index that associated with the packet before transmitting packet (Col. 16, lines 24-58, col. 17, lines 22-37 and Fig 8, col. 21, line 30 to col. 22, line 19).

Since identifying the type of a packet was well known and widely used in the art, it would have been obvious to one of ordinary skill in the art to apply a method for identifying a type of packet as disclosed by Deb into Burnett's system and method. The motivation would have been to provide necessary processes for different packet types and to reduce delay time when transmitting a packet from source to destination.

Regarding claims 2 and 17, Burnett discloses the symbols of the packet include in-band symbols (Fig 2, ref 12) and the synchronization symbols are out-of-band symbols (Col. 2, lines 40-49, control words for control or data type message).

Regarding claims 3 and 18, Burnet discloses the in-band symbols are transition optimized (Fig 2, ref 12) and the out-of-band synchronization symbols are not transition optimized (Col. 2, lines 40-49).

Regarding claims 4 and 19, Burnet discloses the synchronization symbol is transmitted before transmitting the symbols of the packet (Col. 2, lines 40-49).

Regarding claims 5 and 20, Deb discloses the packet has a header with a field that indicates packet type (Fig 1b, Ref 36) and the identifying of the packet type includes checking the field of the header that indicates packet type (Col. 16, lines 24-58, col. 17, lines 22-37 and Fig 8, col. 21, line 30 to col. 22, line 19).

Regarding claims 6 and 21, Burnet discloses the packet types include a data packet (Fig 2, Ref 13).

Regarding claims 7 and 22, Burnet discloses the packet types include a control packet (Fig 2, Ref 12).

Regarding claims 8 and 23, Burnett discloses the symbols are transmitted to a switch network (Fig 1).

Regarding claim 24, Deb discloses the communications device is part of a storage area network (Fig 10, Ref 1010 is hard drive).

(10) Response to Argument

In the appeal brief, the appellant states that (1) Burnett does not disclose "receiving a synchronization symbol indicating a packet type, each packet type having a different

synchronization symbol"; (2) the combination of Burnett and Deb does not teach "transmitting a synchronization symbol that corresponds to the identified packet type, wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol; (3) the combination of Burnett and Deb does not teach a transmission component that transmits a synchronization symbol that corresponds to the identified packet type, the transmitted synchronization symbol providing synchronization information and each packet type having a different synchronization symbol, and that transmits the symbols of the packet and (4) there is no suggestion or motivation to combine reference teachings.

With respect to (1) Burnett does not disclose "receiving a synchronization symbol indicating a packet type, each packet type having a different synchronization symbol". The examiner disagrees with the appellant because Burnett discloses a method and system for receiving a state control word "synchronization symbol" indicating a message type "packet type", each message type having a different state control word "different synchronization symbol". The state control word read on the synchronization symbol because synchronization does not indicate what type of synchronization which the signal will perform for example time synchronization, ordered synchronization, data synchronization, etc….". Therefore, the synchronization symbol, in the claim, just mean a packet type which is used to identify what type of packet the receiving switch will be received after it received the (packet type) state control word in order to allow it to store the receiving message in its associated queue "control queue or data queue". The state control word reads on synchronization symbol because it is used to identify the type of message following the state control word. The state control word and

message must be synchronized with each other in order to allow the receiver to use the state control word to store the message in a control queue or data queue. Burnett clearly disclose each message such as data message and control message has its own state control word "packet type" which indicates the message type (See col. 2, lines 19-60 and col. 3, lines 18-35). Therefore, the state control word is used to data storage synchronization between the storage of receiver and transmitter.

With respect to (2) the combination of Burnett and Deb does not teach “transmitting a synchronization symbol that corresponds to the identified packet type, wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol. The examiner disagrees with the appellant because Burnett discloses a switch for transmitting a state control word "synchronization symbol" that corresponds to the identified message type "packet type", the transmitted synchronization symbol provides synchronization information “state control word is used to indicate what type of message the receiver will be received. The receiver used this information to store the message in a control or data queue, for example, if the transmitter retrieves and transmits a control message from a control queue after transmitting a state control word, the receiver stores the control message into a receiver control queue after receiving the state control word and message”; wherein each data or control message “packet type” has a different synchronization symbol “state control word for data or control message (See col. 2, lines 19-60 and col. 3, lines 18-35). Therefore, the state control word is used to data storage synchronization between the storage of receiver and transmitter.

With respect to (3) the combination of Burnett and Deb does not teach a transmission component that transmits a synchronization symbol that corresponds to the identified packet type, the transmitted synchronization symbol providing synchronization information and each packet type having a different synchronization symbol, and that transmits the symbols of the packet. The examiner disagrees with the appellant because Burnett discloses a switch for transmitting a state control word "synchronization symbol" that corresponds to the identified message type "packet type", the transmitted synchronization symbol provides synchronization information “state control word is used to indicate what type of message the receiver will be received. The receiver used this information to store the message in a control or data queue, for example, if the transmitter retrieves and transmits a control message from a control queue after transmitting a state control word, the receiver stores the control message into a receiver control queue after receiving the state control word and message”. Each data or control message “packet type” has a different synchronization symbol “state control word for data or control message” and that transmits the symbols of the packet (See col. 2, lines 19-60 and col. 3, lines 18-35). Therefore, the state control word is used to data storage synchronization between the storage of receiver and transmitter.

With respect to (4) there is no suggestion or motivation to combine reference teachings. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5

USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Burnett discloses a method and system for transmitting a state control word that indicates the message type in front of a message to the receiver wherein each state control word has a different message type word (See col. 2, lines 19-55 and col. 3, lines 18-35) and receiver includes a device for identifying type of packet based on the information in the header (Col. 2, lines 55-60). Deb discloses a method for receiving a packet and identified the type of received packet before forwarding the packet (Col. 16, lines 24-58, col. 17, lines 22-37, Fig 8 and col. 21, line 30 to col. 22, line 19).

Since, a method for identifying a type of packet is well known and expected in the art and Burnett suggests a buffer register used to allow the receiver to detect a message type (Col. 2, lines 55-60). Therefore, it would have been obvious to one of ordinary skill in the art to apply a well-known method such as identifying a type of packet as disclosed by Deb into Burnett's system and method. The motivation would have been to reduce delay time when transmitting a packet from source to destination.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Steven H.D Nguyen/

Primary Examiner, Art Unit 2619

Conferees:

/CHAU T. NGUYEN/
Supervisory Patent Examiner, Art Unit 2619
/Ricky Ngo/
Supervisory Patent Examiner, Art Unit 2616

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,625	11/07/2001	Yeshik Shin	59472-8818US	1053

63170 7590 09/05/2008

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EXAMINER	
NGUYEN, STEVEN H D	
ART UNIT	**PAPER NUMBER**
2619	

MAIL DATE	DELIVERY MODE
09/05/2008	PAPER

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SEATTLE, WA 98111-1208

Appeal No: 2008-5290
Application: 10/045,625
Appellant: Yeshik Shin et al.

Board of Patent Appeals and Interferences
Docketing Notice

Application 10/045,625 was received from the Technology Center at the Board on July 09, 2008 and has been assigned Appeal No: 2008-5290.

A review of the file indicates that the following documents have been filed by appellant:

Appeal Brief filed on:	January 18, 2008
Reply Brief filed on:	NONE
Request for Hearing filed on:	NONE

In all future communications regarding this appeal, please include both the application number and the appeal number.

The mailing address for the Board is:

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ALEXANDRIA, VIRGINIA 22313-1450

The facsimile number of the Board is 571-273-0052. Because of the heightened security in the Washington D.C. area, facsimile communications are recommended. Telephone inquiries can be made by calling 571-272-9797 and should be directed to a Program and Resource Administrator.

By order of the Board of Patent Appeals and Interferences

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,625	11/07/2001	Yeshik Shin	59472-8818US	1053

63170 7590 09/24/2008

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EXAMINER	
NGUYEN, STEVEN H D	
ART UNIT	**PAPER NUMBER**
2619	

MAIL DATE	DELIVERY MODE
09/24/2008	PAPER

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PERKINS COIE LLP
P.O. BOX 1208
SEATTLE, WA 98111-1208

Appeal No: 2008-5290
Application: 10/045,625
Appellant: Yeshik Shin et al.

Board of Patent Appeals and Interferences
Docketing Notice

Application 10/045,625 was received from the Technology Center at the Board on July 09, 2008 and has been assigned Appeal No: 2008-5290.

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Request for Hearing filed on:	NONE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,625	11/07/2001	Yeshik Shin	59472-8818US	1053

63170 7590 02/25/2009

PERKINS COIE LLP
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NGUYEN, STEVEN H D	
ART UNIT	PAPER NUMBER
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YESHIK SHIN, DAVID D. LEE, and DEOG-KYOON JEONG

Appeal 2008-5290
Application 10/045,625
Technology Center 2600

Decided[1]: February 25, 2009

Before JOSEPH F. RUGGIERO, MARC S. HOFF, and ELENI MANTIS-MERCADER, *Administrative Patent Judges*.

RUGGIERO, *Administrative Patent Judge*.

---

[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 from the Final Rejection of claims 1-24, which are all of the pending claims. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Appellants' claimed invention relates to a method and device for transmitting synchronization symbols which indicate a type of packet that is to be transmitted after the synchronization symbol (Spec. ¶ [0094], Figure 9A).

Claim 1 is illustrative of the invention and reads as follows:

1. A method for transmitting packet types of packets, the method comprising:

receiving a packet having symbols;

identifying a packet type of the packet;

transmitting a synchronization symbol that corresponds to the identified packet type, wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol; and

transmitting the symbols of the received packet.

The Examiner relies on the following prior art references to show unpatentability:

Burnett	US 5,703,875	Dec. 30, 1997
Deb	US 6,172,990 B1	Jan. 9, 2001 (filed Nov. 12, 1997)

Claims 9-15 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Burnett.

Claims 1-8 and 16-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Burnett in view of Deb.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Brief and Answer for the respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Brief have not been considered and are deemed to be waived [*see* 37 C.F.R. § 41.37(c)(1)(vii)].

ISSUES

(i) Under 35 U.S.C. § 102(b), does Burnett have a disclosure which anticipates the invention set forth in claims 9-15?

The pivotal issue before us in making this determination is whether Appellants have demonstrated that the Examiner erred in determining that Burnett discloses the use of synchronization symbols which indicate the type of message packet to be transmitted.

(ii) Under 35 U.S.C. § 103(a), with respect to appealed claims 1-8 and 16-24, would one of ordinary skill in the art at the time of the invention have found it obvious to combine Burnett with Deb to render the claimed invention unpatentable?

The pivotal issue before us is in making this determination is whether Appellants have demonstrated that the Examiner erred in determining that the combination of Burnett and Deb provides a teaching or suggestion of

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using synchronization symbols to indicate the type of message packet that is being transmitted.

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence:

1. Appellants have invented a method and device for transmitting synchronization symbols that include an indication of the type of message packet to be transmitted after the synchronization symbol. A communication node periodically transmits synchronization primitives to enable a receiving node to properly align with the synchronization primitives. Upon receipt of the synchronization primitive, the communication node will know that the primitive is correctly aligned on a symbol boundary. (Spec. ¶¶ [0094]-[0096], Figure 9A).

2. Burnett discloses (col. 2, ll. 39-47) a method for identifying the types of transmitted message packets, such as control messages or data messages, by using "state control words" when, for example, a first switch is about to send a message to a second switch.

3. The "state control word" described by Burnett (col. 2, ll. 47-49, Figure 2) indicates to the receiving second switch into which of the buffers (control message buffer 12 or data message buffer 13) the received message is to be stored.

4. Burnett further discloses (col. 3, ll. 18-21) that the "state control words" can be used to signal the start and end of a message.

5. Deb discloses (col. 21, l. 30 through col. 22, l. 19) a system which is directed to the identifying of a type of received packet and a

LENOVO EXHIBIT 1002 - 362/553

transmitted appended index associated with the packet before transmission of the packet.

PRINCIPLES OF LAW

1. ANTICIPATION

It is axiomatic that anticipation of a claim under § 102 can be found if the prior art reference discloses every element of the claim. *See In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986) and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.,* 730 F.2d 1452, 1457 (Fed. Cir. 1984).

In rejecting claims under 35 U.S.C. § 102, a single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation. *Perricone v. Medicis Pharmaceutical Corp.*, 432 F.3d 1368, 1375-76 (Fed. Cir. 2005), citing *Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565 (Fed. Cir. 1992). Anticipation of a patent claim requires a finding that the claim at issue "reads on" a prior art reference. *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999) ("In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.") (internal citations omitted).

2. OBVIOUSNESS

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of

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obviousness. *See In re Fine*, 837 F.2d 1071, 1073 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). "[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). Furthermore, "'there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness' . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007)(quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

ANALYSIS

35 U.S.C. § 102(b) REJECTION

Appellants' arguments in response to the Examiner's anticipation rejection, based on Burnett, of independent claim 9 assert that the Examiner has not shown how each of the claimed features is present in the disclosure of Burnett so as to establish a prima facie case of anticipation. Appellants' arguments (App. Br. 5-6) focus on the contention that, in contrast to the requirements of appealed independent claim 9, Burnett does not disclose the use of any synchronization symbols which correspond to or indicate message packet types.

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We agree with Appellants. We do note that the Examiner has correctly determined that the "state control words" in Burnett are used to indicate message packet types, such as control messages or data messages, as do Appellants' synchronization symbols. We simply do not find, however, any support in the disclosure of Burnett for the Examiner's finding that Burnett's "state control words" correspond to the claimed synchronization symbols since there is no indication that such "state control words" in Burnett are used for synchronization of any kind.

As explained and defined by Appellants (Spec. ¶ [0094]), the claimed synchronization symbols permit a receiving node to properly align with the synchronization primitive so that the synchronization primitive, which is made up of a sequence of bit-string synchronization symbols (Spec. ¶¶ [0097-0099] and Tables 3-4), is correctly aligned on a symbol boundary. The "state control words" in Burnett, however, as pointed out by Appellants (App. Br. 6), are primarily used to indicate whether a transmitted message is a control message or data message and to instruct a switch as to which buffer transmitted packets are to be stored (col. 2, ll. 39-49 and col. 3, ll. 18-35).

We recognize that the Examiner, in the responsive arguments portion of the Answer at page 6, further explains the reasoning behind the stated rejection by calling attention to the fact that the type of synchronization performed by the Appellants' claimed synchronization symbols are not set forth in claim 9. While this is correct, the simple fact remains that the disclosure of Burnett provides no indication, nor has the Examiner provided any valid line of reasoning, to support the contention that any coordination of events that would indicate synchronization of any kind is being performed by the "state control words" in Burnett.

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In view of the above discussion, in order for us to sustain the Examiner's rejection, we would need to resort to impermissible speculation or unfounded assumptions or rationales to supply deficiencies in the factual basis of the rejection before us. *In re Warner*, 379 F.2d 1011, 1017 (CCPA 1967). Accordingly, since Appellants' arguments have demonstrated that the Examiner erred in determining that all of the claim limitations are not present in the disclosure of Burnett, we do not sustain the Examiner's 35 U.S.C. § 102(b) rejection of appealed independent claim 9, nor of claims 14-15 dependent thereon.

35 U.S.C. § 103(a) REJECTION

The Examiner's obviousness rejection of independent claims 1 and 16, and their respective dependent claims 2-8 and 16-24, based on the combination of Burnett and Deb is also not sustained. Independent claims 24 and 32 also include the feature set forth in previously discussed independent claim 9 requiring a synchronization symbol that indicates message packet type, but with the further qualifying limitation that packet type identification is based on a received packet.

In addressing the claimed limitations, the Examiner has applied, to Burnett, the teachings of the Deb reference, which is directed (col. 21, l. 30 through col. 22, l. 19) to identifying a type of received packet and a transmitted appended index associated with the packet before transmitting the packet. We find nothing, however, in the disclosure of Deb which overcomes the basic deficiency of Burnett in disclosing the use of a synchronization symbol for identifying the types of transmitted message packets as presently claimed.

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CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that Appellants have shown that the Examiner erred in rejecting claims 9-15 for anticipation under 35 U.S.C. § 102(b), and in rejecting claims 1-8 and 16-24 for obviousness under 35 U.S.C. § 103(a).

DECISION

The Examiner's decision rejecting claims 9-15 under 35 U.S.C. § 102(b) and claims 1-8 and 16-24 under 35 U.S.C. § 103(a) is reversed.

REVERSED

gvw

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,625	11/07/2001	Yeshik Shin	59472-8818US	1053

63170 7590 06/11/2009

PERKINS COIE LLP
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SEATTLE, WA 98111-1208

EXAMINER	
NGUYEN, STEVEN H D	
ART UNIT	PAPER NUMBER
2416	
MAIL DATE	DELIVERY MODE
06/11/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/045,625	SHIN ET AL.	
	Examiner	Art Unit	
	Steven Nguyen	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Reopening of Prosecution after the Board Decision

The prosecution of this case is being reopened after the Board decision reversing the examiner.

According to MPEP 1214.04:
If the examiner has specific knowledge of the existence of a particular reference or references which indicate nonpatentability of any of the appealed claims as to which the examiner was reversed, he or she should submit the matter to the Technology Center (TC) Director for authorization to reopen prosecution under 37 CFR 1.198 for the purpose of entering the new rejection. See MPEP § 1002.02(c) and MPEP § 1214.07.

1. In this case, Examiner is now aware of a reference (Austin – US 6498568) that teaches the limitation that the Board found lacking in the Burnett patent and on which the reversal of the Examiner was based.

2. The TC Director has approved this action reopening prosecution.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4-9, 12-16, 19-23 rejected under 35 U.S.C. 103(a) as being unpatentable over Burnett (USP 5703875) in view of Austin (USP 6498568).

As claims 1 and 16, Burnet discloses a method and a communication device for transmitting packet types of packets comprising the steps of receiving a packet having symbols, identifying a packet type of the packet based on the received packet and transmitting a control

word that corresponds to the identified packet type (Col. 2, lines 55-60, the packet is received by port which identifies a type of packet of the received packet and forwarding a control word which corresponds to the identified packet type, Col. 2, lines 45-47); and transmitting the symbols of the received packet (Col. 2, lines 45-47, each type of message is associated with a different state control word and the state control word is transmitted before transmitting its associated message). However, Burnet does not disclose that the control word is used for synchronization in addition to indicating a packet type. In the same fields of endeavor, Austin discloses a protocol which uses a synchronization word for synchronizing and identifying a packet type wherein each synchronization word corresponds to a packet type (Col. 4, lines 37-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a synchronization word for identifying a packet type as disclosed by Austin into the teaching of Burnet which discloses a control word for identifying the packet type. The motivation would have been to reduce overhead to maintain a throughput after modifying the system.

As claims 4 and 19, Burnet discloses the control word is transmitted before transmitting the symbols of the packet (Col. 2, lines 45-47).

As claims 5 and 20, Burnet discloses the packet has a header with a field that indicates packet type (Col. 2, lines 57-60 a header with message type) and the identifying of the packet type includes checking the field of the header that indicates packet type (Col. 2, lines 57-60, the message type used to identify a type of packet).

As claims 6 and 21, Burnet discloses the packet types include a data packet (Fig 2, Ref 13).

As claims 7 and 22, Burnet discloses the packet types include a control packet (Fig 2, Ref 12).

As claims 8 and 23, Burnett discloses the symbols are transmitted to a switch network (Col. 2, lines 45-49).

As claim 9, Burnet discloses a method for identifying packet types of packets of symbols comprising receiving a control word indicating a packet type (Col. 2, lines 45-47), each packet type having a different control word (Col. 2, lines 40-49); receiving a packet of symbols (Col. 2, lines 45-49, the second switch receives the message); and indicating that the received packet of symbols has the packet type of the received control word (Col. 2, lines 45-49, the state control word is used to stored the data or control packet into correct buffer). However, Burnet does not disclose that the state control word is used for synchronization and indication of packet type. In the same fields of endeavor, Austin discloses a protocol which uses a synchronization word for synchronizing and identifying a packet type wherein each synchronization word corresponds to a packet type (Col. 4, lines 37-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a synchronization word for identifying a packet type as disclosed by Austin into the teaching of Burnet which discloses a control word for identifying the packet type. The motivation would have been to reduce overhead to maintain a throughput after modifying the system.

As claim 12, Burnet discloses the control word is received before the symbols of the packet are received (Col. 2, lines 45-49).

As claim 13, Burnet discloses packet types include a data packet (Fig 2, Ref 13).

As claim 14, Burnet discloses packet types include a control packet (Fig 2, Ref 12).

As claim 15, Burnet discloses the symbols are received from a switch (Fig 1).

5. Claims 2-3, 10-11 and 17-18 rejected under 35 U.S.C. 103(a) as being unpatentable over Burnett and Austin as applied to claims 1, 9 and 16 above, and further in view of Thomas (US 4924463).

As claims 2-3, 10-11 and 17-18, Burnett and Austin fail to disclose the symbols of the packet include in-band symbols which are transition optimized and the synchronization symbols which are not are transition optimized, are out-of-band symbols. In the same field of endeavor, Thomas discloses the symbols of the packet include in-band symbols which are transition optimized, and the synchronization symbols which are not transition optimized are out-of-band symbols (Col. 5, lines 6-9, the synchronization symbols are not transition optimized because it is outside of the packet and in-band symbols are transition optimized because it is inside packet **as disclosed in the applicant spec, page 7, Sec 88**).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply the teaching of Thomas to the method/device taught by Burnett and Austin such that in-band symbols which are transition optimized are used to encode data and out of band symbol which are not transition optimized are used to transmit synchronization symbols outside of the packet as disclosed by Thomas. The motivation would have been to improve data encoding.

6. Claim 24 rejected under 35 U.S.C. 103(a) as being unpatentable over Burnett and Austin as applied to claim16 above, and further in view of Heil (USP 6944152).

As claim 24, Burnett and Austin fail to disclose the communications device is part of a storage area network. In the same field of endeavor, Heil shows that communications devices forming a storage area network are well known in the art (Fig 3 sow a storage area network or SAN comprising multiple devices such as Host Devices 114 and switches comprised in Network 116. Col. 7, lines 17-21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply the teaching of Burnett and Austin to devices of a storage area network such as those disclosed by Heil. The motivation would have been to increase the efficiency of the network by taking advantage of the overhead reduction resulting from using synchronization symbols to indicate packet types.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Nguyen whose telephone number is (571) 272-3159. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kizou Hassan can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

6/11/2009
/Steven Nguyen/
Primary Examiner, Art Unit 2419

/Timothy P Callahan/
Director, Technology Center 2400

Notice of References Cited	Application/Control No. 10/045,625	Applicant(s)/Patent Under Reexamination SHIN ET AL.	
	Examiner Steven Nguyen	Art Unit 2419	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,498,568	12-2002	Austin et al.	340/854.5
*	B	US-4,924,463	05-1990	Thomas et al.	370/520
*	C	US-6,944,152	09-2005	Heil, Tom	370/360
*	D	US-5,703,875	12-1997	Burnett, Robert W.	370/412
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10045625	SHIN ET AL.
	Examiner	**Art Unit**
	Steven Nguyen	2419

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	04/21/2009								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
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	19	✓								
	20	✓								
	21	✓								
	22	✓								
	23	✓								
	24	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10045625	SHIN ET AL.
	Examiner	**Art Unit**
	Steven Nguyen	2419

SEARCHED			
Class	**Subclass**	**Date**	**Examiner**

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
See East text search	4/21/2009	ST

INTERFERENCE SEARCH			
Class	**Subclass**	**Date**	**Examiner**

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	219	idle adj symbol and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 22:28
S2	117	idle with data and @ad<"20001120" and Storage with area with network	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 22:32
S3	11	idle with data and @ad<"20001120" and resume with preempt$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 22:33
S4	1244	idle with data and @ad<"20001120" and stop with start	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 22:34
S5	4	idle with data and @ad<"20001120" and stop with start with congest$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 22:34
S6	35	idle adj symbol and @ad<"20001120" and in-band	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 22:36
S7	595191	idle with insert$3 control with data and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 22:41
S8	90	idle with insert$3 with control with data and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 22:41
S9	55	idle and preempt$3 with resume and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 22:47
S10	5	idle adj2 (word symbol) and preempt$3 with resume and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 22:48
S11	0	idle adj2 (word symbol) and pre-empt$3 with resume and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 22:48
S12	55	idle adj2 (word symbol) and out adj2 band and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 22:49
S13	50	idle adj2 (word symbol) same storage and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 22:54

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S14	492	idle with data with stream and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 23:13
S15	451	idle with data with stream and @ad<"20001120"	USPAT	OR	ON	2009/05/09 23:13
S16	291	idle with data with stream and @ad<"20001120" and serial	USPAT	OR	ON	2009/05/09 23:15
S17	226	idle with data with transition and @ad<"20001120" and serial	USPAT	OR	ON	2009/05/09 23:30
S18	38	idle with data with transition and @ad<"20001120" and optimized	USPAT	OR	ON	2009/05/09 23:31
S19	0	idle with data with transition and @ad<"20001120" and transition with optimized	USPAT	OR	ON	2009/05/09 23:33
S20	0	idle adj (word symbol) and @ad<"20001120" and transition with optimized	USPAT	OR	ON	2009/05/09 23:33
S21	0	idle adj (word symbol) and @ad<"20001120" and transition with optimiz$3	USPAT	OR	ON	2009/05/09 23:33
S22	190	idle adj (word symbol) and @ad<"20001120" and (packet message) with (word symbol)	USPAT	OR	ON	2009/05/09 23:34
S23	5	silicon.as. and hsu.xp.	USPAT	OR	ON	2009/05/09 23:42
S24	8	("4267592" | "4891806" | "5400323" | "5574849" | "5583872" | "6016510" | "6400730" | "6438128"). PN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/09 23:43
S25	84	idle with data with serial with link	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/09 23:44
S26	44	idle with data and brenda near2 pham	US-PGPUB; USPAT; USOCR	OR	ON	2009/05/09 23:46
S27	3	"5608755" and in-band	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 23:49
S28	0	"5608755" and in-band with symbol and out adj band with symbol	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 23:51
S29	5	in-band with symbol and out adj band with symbol	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 23:51

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S30	40	in-band with symbol and out adj2 band with symbol	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 23:51
S31	4	in-band with symbol and out adj2 band with symbol and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/09 23:54
S32	2	in-band with symbol and out adj2 band with symbol and @ad<"20001120" and (packet message)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2009/05/10 00:07
S33	531836	additional adj3 (subchannel sub-channel slot sub-slot) with power gain	US-PGPUB; USPAT	OR	ON	2009/05/10 20:44
S34	1	"20040221312" and software	US-PGPUB; USPAT	OR	ON	2009/05/10 20:44
S35	1	"20040221312" and (software program$5)	US-PGPUB; USPAT	OR	ON	2009/05/10 20:45
S36	1593	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot) and (assign$4 allocat$3) with (subchannel sub-channel slot sub-slot)	US-PGPUB; USPAT	OR	ON	2009/05/10 20:56
S37	631	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot) same (assign$4 allocat$3) with (subchannel sub-channel slot sub-slot)	US-PGPUB; USPAT	OR	ON	2009/05/10 20:57
S38	202	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot) same (assign$4 allocat$3) with (subchannel sub-channel slot sub-slot) same (interference noise rate)	US-PGPUB; USPAT	OR	ON	2009/05/10 20:57
S39	52	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot) same (assign$4 allocat$3) with (subchannel sub-channel slot sub-slot) same (interference noise rate) same base adj station	US-PGPUB; USPAT	OR	ON	2009/05/10 20:57

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S40	23	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot) same (assign$4 allocat$3) with (additional more) with (subchannel sub-channel slot sub-slot) same (interference noise rate) same base adj station	US-PGPUB; USPAT	OR	ON	2009/05/10 21:04
S41	111	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot) same (assign$4 allocat$3) with (additional more) with (subchannel sub-channel slot sub-slot) same (interference noise rate)	US-PGPUB; USPAT	OR	ON	2009/05/10 21:29
S42	80	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot) same (assign$4 allocat$3) with (additional more) with (subchannel sub-channel slot sub-slot) same (interference noise rate) and @ad<"20051128"	US-PGPUB; USPAT	OR	ON	2009/05/10 21:30
S43	91	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot) same (assign$4 allocat$3) with (additional more) adj3 (subchannel sub-channel slot sub-slot) and @ad<"20051128"	US-PGPUB; USPAT	OR	ON	2009/05/10 21:51
S44	110	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot subcarrier sub-carrier) same (assign$4 allocat$3) with (additional more) adj3 (subchannel sub-channel slot sub-slot subcarrier sub-carrier) and @ad<"20051128"	US-PGPUB; USPAT	OR	ON	2009/05/10 21:52
S45	19	S44 not S43	US-PGPUB; USPAT	OR	ON	2009/05/10 21:52

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S46	17	(additional more increas $3) adj2 (power gain energy) with (subchannel sub-channel slot sub-slot) same (assign$4 allocat$3) with (additional more) adj3 (subchannel sub-channel slot sub-slot) and @ad<"20051128"	US-PGPUB; USPAT	OR	ON	2009/05/10 22:20
S47	36	(additional more increas $3) adj2 (power gain energy) with (subchannel sub-channel slot sub-slot subcarrier sub-carrier) same (assign$4 allocat$3) with (additional more) adj3 (subchannel sub-channel slot sub-slot subcarrier sub-carrier)	US-PGPUB; USPAT	OR	ON	2009/05/10 22:23
S48	110	(additional more increas $3) adj2 (power gain energy) with (subchannel sub-channel slot sub-slot) same (additional more) adj3 (subchannel sub-channel slot sub-slot) and @ad<"20051128"	US-PGPUB; USPAT	OR	ON	2009/05/10 22:23
S49	110	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot subcarrier sub-carrier) same (assign$4 allocat$3) with (additional more) adj3 (subchannel sub-channel slot sub-slot subcarrier sub-carrier) and @ad<"20051128"	US-PGPUB; USPAT	OR	ON	2009/05/10 22:24
S50	370	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot subcarrier sub-carrier) same (additional more) adj1 (subchannel sub-channel slot sub-slot subcarrier sub-carrier) and @ad<"20051128"	US-PGPUB; USPAT	OR	ON	2009/05/10 22:27

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S51	337	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot subcarrier sub-carrier) with (additional more) adj1 (subchannel sub-channel slot sub-slot subcarrier sub-carrier) and @ad<"20051128"	US-PGPUB; USPAT	OR	ON	2009/05/10 22:27
S52	54	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot subcarrier sub-carrier) with (additional more) adj1 (subchannel sub-channel slot sub-slot subcarrier sub-carrier) and @ad<"20051128" and OFDM	US-PGPUB; USPAT	OR	ON	2009/05/10 22:28
S53	7	(("7069009") or ("20060078059") or ("20040127223") or ("7012912") or ("20060126749") or ("20020114269") or ("20050099937")).PN.	US-PGPUB; USPAT	OR	OFF	2009/05/10 22:30
S54	4	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot subcarrier sub-carrier) with (additional more) adj1 (subchannel sub-channel slot sub-slot subcarrier sub-carrier) and @ad<"20051128" and S53	US-PGPUB; USPAT	OR	ON	2009/05/10 22:30
S55	7	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot subcarrier sub-carrier) same (assign$4 allocat$3) with (additional more) adj3 (subchannel sub-channel slot sub-slot subcarrier sub-carrier) and @ad<"20051128" and S53	US-PGPUB; USPAT	OR	ON	2009/05/10 22:32

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S56	1	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot subcarrier sub-carrier) with CSI and @ad<"20051128" and S53	US-PGPUB; USPAT	OR	ON	2009/05/10 22:59
S57	10	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot subcarrier sub-carrier) with CSI and @ad<"20051128"	US-PGPUB; USPAT	OR	ON	2009/05/10 22:59
S58	12	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot subcarrier sub-carrier) with state adj information and @ad<"20051128"	US-PGPUB; USPAT	OR	ON	2009/05/10 23:00
S59	0	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot subcarrier sub-carrier) with state adj information and priority with user and @ad<"20051128"	US-PGPUB; USPAT	OR	ON	2009/05/10 23:04
S60	127	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot subcarrier sub-carrier) and priority with user and @ad<"20051128"	US-PGPUB; USPAT	OR	ON	2009/05/10 23:04
S61	30	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot subcarrier sub-carrier) and priority with user and @ad<"20051128" and OFDM	US-PGPUB; USPAT	OR	ON	2009/05/10 23:05
S62	11660	SAN and primitive	US-PGPUB; USPAT	OR	ON	2009/05/10 23:33
S63	162	SAN and primitive and control adj packet	US-PGPUB; USPAT	OR	ON	2009/05/10 23:33
S64	144	SAN and primitive and control adj packet and data adj packet	US-PGPUB; USPAT	OR	ON	2009/05/10 23:34

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S65	37	SAN and primitive and control adj packet and data adj packet and @ad<"20001120"	US-PGPUB; USPAT	OR	ON	2009/05/10 23:34
S66	2	storage adj area adj network and control adj packet and data adj packet and @ad<"20001120"	US-PGPUB; USPAT	OR	ON	2009/05/10 23:35
S67	0	storage adj area adj network and synchronization adj symbol and @ad<"20001120"	US-PGPUB; USPAT	OR	ON	2009/05/10 23:37
S68	0	storage adj area adj network and synchroniz$5 adj symbol and @ad<"20001120"	US-PGPUB; USPAT	OR	ON	2009/05/10 23:37
S69	0	storage adj area adj network and synchroniz$5 adj word and @ad<"20001120"	US-PGPUB; USPAT	OR	ON	2009/05/10 23:38
S70	88	storage adj area adj network and synchroniz$5 and @ad<"20001120"	US-PGPUB; USPAT	OR	ON	2009/05/10 23:38
S71	21	storage adj area adj network and control adj (packet message) and @ad<"20001120"	US-PGPUB; USPAT	OR	ON	2009/05/10 23:40
S72	24	storage adj area adj network and primitive and @ad<"20001120"	US-PGPUB; USPAT	OR	ON	2009/05/10 23:42
S73	12	storage adj area adj network and control adj (packet message frame cell) and (data information) adj (packet message frame cell) and @ad<"20001120"	US-PGPUB; USPAT	OR	ON	2009/05/10 23:47
S74	191	storage adj area adj network and switches and @ad<"20001120"	US-PGPUB; USPAT	OR	ON	2009/05/10 23:58
S75	89	storage adj area adj network and switches and client and @ad<"20001120"	US-PGPUB; USPAT	OR	ON	2009/05/10 23:58

5/19/2009 1:02:26 PM
C:\Documents and Settings\SNguyen\My Documents\EAST\Workspaces\10045625.wsp

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I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4).

Dated: 12/4/09 Signature: _____ (Joe Clark)

Docket No.: 59472-8818.US00
SIMG-0110 (PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Shin et al.

Application No.: 10/045,625 Confirmation No.: 1053

Filed: November 7, 2001 Art Unit: 2416

For: METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS Examiner: S. H. Nguyen

AMENDMENT IN RESPONSE TO NON-FINAL OFFICE ACTION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated June 11, 2009, please amend the above-identified U.S. patent application as below. A Petition for 3-Month Extension of Time accompanies this Amendment:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

AMENDMENTS TO THE CLAIMS

Following is a complete listing of the claims pending in the application, as amended:

1. (Currently Amended) A method for transmitting packet types of packets, the method comprising:

receiving a packet having symbols;

identifying a packet type of the packet;

transmitting a synchronization symbol that corresponds to the identified packet type, wherein the transmitted synchronization symbol provides synchronization information and wherein each packet type has a different synchronization symbol, and the synchronization symbol permitting an external receiving node to properly align with a synchronization primitive to be correctly aligned on a symbol boundary; and

transmitting the symbols of the received packet.

2. (Original) The method of claim 1 wherein the symbols of the packet include in-band symbols and the synchronization symbols are out-of-band symbols.

3. (Original) The method of claim 2 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

4. (Original) The method of claim 1 wherein the synchronization symbol is transmitted before transmitting the symbols of the packet.

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5. (Original) The method of claim 1 wherein the packet has a header with a field that indicates packet type and the identifying of the packet type includes checking the field of the header that indicates packet type.

6. (Original) The method of claim 1 wherein the packet types include a data packet.

7. (Original) The method of claim 1 wherein the packet types include a control packet.

8. (Original) The method of claim 1 wherein the symbols are transmitted to a switch network.

9. (Currently Amended) A method for identifying packet types of packets of symbols, the method comprising:

receiving a synchronization symbol by a receiver indicating a packet type, each packet type having a different synchronization symbol;

receiving a packet of symbols; [[and]]

indicating that the received packet of symbols has the packet type of the received synchronization symbol; and

the synchronization symbol permitting properly alignment upon receiving with a synchronization primitive to be correctly aligned on a symbol boundary.

10. (Original) The method of claim 9 wherein the symbols of the packets include in-band symbols and the synchronization symbols are out-of-band symbols.

11. (Original) The method of claim 10 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

12. (Original) The method of claim 9 wherein the synchronization symbol is received before the symbols of the packet are received.

13. (Original) The method of claim 9 wherein the packet types include a data packet.

14. (Original) The method of claim 9 wherein the packet types include a control packet.

15. (Original) The method of claim 9 wherein the symbols are received from a switch.

16. (Currently Amended) A communications device for transmitting packet types of packets, comprising:

an identification component that identifies a packet type of a packet of symbols; and

a transmission component that transmits a synchronization symbol that corresponds to the identified packet type, the transmitted synchronization symbol providing synchronization information and each packet type having a different synchronization symbol and permitting an external receiving node to properly align with a synchronization primitive to be correctly aligned on a symbol boundary, and that transmits the symbols of the packet.

17. (Original) The communications device of claim 16 wherein the symbols of the packet include in-band symbols and the synchronization symbols are out-of-band symbols.

18. (Original) The communications device of claim 17 wherein the in-band symbols are transition optimized and the out-of-band synchronization symbols are not transition optimized.

19. (Original) The communications device of claim 16 wherein the synchronization symbol is transmitted before transmitting the symbols of the packet.

20. (Original) The communications device of claim 16 wherein the packet has a header with a field that indicates packet type and the identification component checks the field of the header that indicates packet type.

21. (Original) The communications device of claim 16 wherein the packet types include a data packet.

22. (Original) The communications device of claim 16 wherein the packet types include a control packet.

23. (Original) The communications device of claim 16 wherein the symbols are transmitted to a switch network.

24. (Original) The communications device of claim 16 wherein the communications device is part of a storage area network.

Add Claims 25 - 28 as follows:

25. (New) The method of claim 1 wherein the synchronization primitive is made up of a sequence of bit-string synchronization symbols.

26. (New) The method of claim 9 wherein the synchronization primitive is made up of a sequence of bit-string synchronization symbols.

27. (New) The communications device of claim 16 wherein the synchronization primitive is made up of a sequence of bit-string synchronization symbols.

28. (New) The method of claim 1, wherein:

multiple primitives are defined to operate as synchronization signals, and the use of multiple synchronization primitives allows for encoding packet type within a synchronization primitive;

the transmitting periodically transmits synchronization primitives so that a receiving communications node can properly align with that synchronization primitive; and

when a communications node receives a synchronization primitive it knows that the synchronization primitive is correctly aligned on a symbol boundary.

REMARKS

Claims 1-27 are pending in this application. Claims 1-24 have been rejected, claims 25-28 are added herein.

Reconsideration and withdrawal of the rejections set forth in the Office Action dated June 11, 2009 are respectfully requested. The applicant petitions the Commissioner for a three-month extension of time: a separate petition accompanies this amendment.

Amendments

Amendments to claims have been made to independent claims 1, 9, and 16. Support for these amendments can be found in the application as filed, including at paragraphs [0095] – [0099]. Accordingly, no new matter has been added by these amendments.

Rejections under 35 U.S.C. §103

Claims 1, 4-9, 12-16, 19-23 were rejected under 35 U.S.C. §103 as allegedly being unpatentable over USP 5,703,875, Burnett et al. in view of USP 6,498,568, Austin.

Claims 2-3, 10-11 and 17-18 were rejected under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,703,875, Burnett et al. and U.S. Patent No. 6,498,568, Austin, as applied to claims 1, 9 and 16 as previously discussed, and further in view of USP 4,924,463, Thomas.

Applicant notes the long and protracted period of pendency of this application from the filing date of 11/07/2001 (more than 9 years). Applicant further notes the Reversal of the Examiner's Final Rejection in the Decision decided 02/25/2009.

Applicant further references the issues, findings of fact, and analysis set forth in that Decision.

Without admitting the propriety of the 35 USC 103 rejections set forth in the new non-final office action, applicant has for business reasons unrelated to patentability amended each of independent claims 1, 9, and 16 to further characterize the features of the synchronization and synchronization symbols in accordance with a particular disclosed embodiment. Applicant reserves the right to present the original claims, or a differently amended version of the original claims, in a related application.

Independent claim 1 now includes the further limitation that "the synchronization symbol permitting an external receiving node to properly align with a synchronization primitive to be correctly aligned on a symbol boundary". Amended independent claim 9, now includes the further limitation that "the synchronization symbol permitting properly alignment upon receiving with a synchronization primitive to be correctly aligned on a symbol boundary". Independent claim 16, now includes the further limitation that "... the transmitted synchronization symbol ... permitting an external receiving node to properly align with a synchronization primitive to be correctly aligned on a symbol boundary, ...".

With reference to each of these claims (and the claims dependent there from), Applicant submits that Burnett fails to disclose the underlying features as argued earlier by applicant and that Austin does not make up for these deficiencies.

Applicant submits that at most (See Austin at Col. 4, lines 37-45) discloses "5 pre-defined packet sizes" and "16 user defined data message types". Austin also states that "[t]he system uses standard run in and byte synchronization techniques" and that "[t]he byte synchronization word used is 32 _bits long and there are 5_different words used, one to identify each of the different packet types."

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Applicant submits that neither Burnett nor Austin teaches, discloses, suggests, or provides any motivation for the combination of elements recited in the independent claims including the added limitations that "the synchronization symbol permitting an external receiving node to properly align with a synchronization primitive to be correctly aligned on a symbol boundary" (Claim 1), "the synchronization symbol permitting properly alignment upon receiving with a synchronization primitive to be correctly aligned on a symbol boundary" (Claim 9), or "... the transmitted synchronization symbol ... permitting an external receiving node to properly align with a synchronization primitive to be correctly aligned on a symbol boundary" (Claim 16).

Applicant further submits that there is confusion or ambiguity in the disclosure of Austin between message types, packet sizes, packet types, and that these ambiguities and confusion would tend to teach away from rather than toward Applicant's claims even if there was the purported teaching or suggestion.

Finally, the examiner suggests, based on his interpretation of Austin and Burnett, that it would have been obvious to apply a synchronization word for identifying a packet type as disclosed by Austin into the teaching of Burnet which discloses a control word for identifying the packet type, where the suggested motivation would have been to reduce overhead to maintain a throughput after modifying the system.

Applicant again must respectfully disagree and submits that it would not be obvious to combine Burnett and Austin. Burnett has been differentiated in Applicant's earlier responses and Appeal Brief.

Austin is directed toward a pipeline communication system, that uses the pipeline and the adjacent ground and includes branches with junctions. Governor modules and transformers/rectifiers form part of the network. Monitors periodically provide information to the network controller. The system control receives information by way of an outstation to provide two-way communication and control using the pipeline and

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adjacent ground as conductors. Typically, the information in the form of fast frequency shift keying modulation is superimposed on the cathodic pipe protection system. (See Austin Abstract).

Austin also describes in minimal detail, a protocol used for "data operation over a remote monitoring network between the monitor and the system control". Austin further states that "This system uses up to 5 pre-defined data packet sizes and up to 16 user defined data message types within each packet. Each packet has Forward Error Connection (FEC) and bit interleaving applied to it on transmission. Error checking is performed using a standard CRC. The system uses standard run in and byte synchronization techniques. The byte synchronization word used is 32 _bits long and there are 5_different words used, one to identify each of the different packet types." Austin further states that "[t]he number of packets and user defined messages has been chosen to suit the present Gas Market."

Austin does not disclose, suggest, or motivate any need for the particular synchronization now set forth in each independent claim. Even if Burnet and Austin were combined, the combination of Burnett and Austin would not result in the structure or method of Applicant's amended claims. The required synchronization as recited in Applicant's claims is not present in the combination.

For at least these reasons, Applicant submits that each of the now pending independent Claims 1, 9, and 16 are patentable over the cited art. Furthermore, each of the claims dependent from these independent claims (Claims 2-8, 10-15, and 17-24, as well as newly added dependent claims 25-28) are patentable over the cited art for at least the same reasons as the underlying independent claims and further because each adds additional distinguishing limitations.

Applicant submits that each of the added dependent claims 25-28 add further features respective of the particular synchronization that are supported by the

application as filed and not disclosed, suggested, or motivated by Burnett, Austin, or a combination of these references.

Conclusion

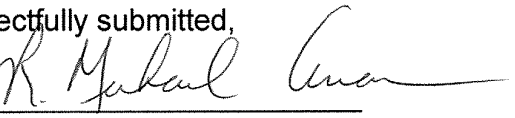
In view of the foregoing, the applicant submits that the claims pending in the application comply with the requirements of 35 U.S.C. §112 and patentably define over the prior art. A Notice of Allowance is therefore respectfully requested.

If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-2207, under Order No. 59472-8818.US00 from which the undersigned is authorized to draw.

Dated: **December 11, 2009**

Respectfully submitted,

By 

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Correspondence Address:
Customer No. 63170

Electronic Patent Application Fee Transmittal

Application Number:	10045625
Filing Date:	07-Nov-2001
Title of Invention:	Method and system for integrating packet type information with synchronization symbols
First Named Inventor/Applicant Name:	Yeshik Shin
Filer:	R. Michael Ananian/Joe Clark
Attorney Docket Number:	59472-8818US

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in excess of 20	1202	4	52	208
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 3 months with $0 paid	1253	1	1110	1110
Miscellaneous:				
		Total in USD ($)		**1318**

Electronic Acknowledgement Receipt

EFS ID:	6623030
Application Number:	10045625
International Application Number:	
Confirmation Number:	1053
Title of Invention:	Method and system for integrating packet type information with synchronization symbols
First Named Inventor/Applicant Name:	Yeshik Shin
Customer Number:	63170
Filer:	R. Michael Ananian/Joe Clark
Filer Authorized By:	R. Michael Ananian
Attorney Docket Number:	59472-8818US
Receipt Date:	11-DEC-2009
Filing Date:	07-NOV-2001
Time Stamp:	17:47:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1318
RAM confirmation Number	4046
Deposit Account	502207
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		59472_8818_US00_Amd.pdf	702087 95e3b6b97a87c437549237ca8a0b7520ff26fb2b	yes	12

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Extension of Time	1	1
	Amendment/Req. Reconsideration-After Non-Final Reject	2	2
	Claims	3	7
	Applicant Arguments/Remarks Made in an Amendment	8	12

Warnings:

Information:

2	Fee Worksheet (PTO-875)	fee-info.pdf	32070 7bfe8cbeeb5d363fdf04c67a5c81b75b34742ad7	no	2

Warnings:

Information:

Total Files Size (in bytes):	734157

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/22 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless if displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) FY 2009 *(Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).)*	Docket Number (Optional) 59472-8818.US
Application Number 10/045,625-Conf. #1053	Filed November 7, 2001
For METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS	
Art Unit 2416	Examiner Steven H.D. Nguyen

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

		Fee	Small Entity Fee	
☐	One month (37 CFR 1.17(a)(1))	$130	$65	$
☐	Two months (37 CFR 1.17(a)(2))	$490	$245	$
X	Three months (37 CFR 1.17(a)(3))	$1110	$555	$ $1110.00
☐	Four months (37 CFR 1.17(a)(4))	$1730	$865	$
☐	Five months (37 CFR 1.17(a)(5))	$2350	$1175	$

☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

X The Director has already been authorized to charge fees in this application to a Deposit Account.

X The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-2207 .

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

X attorney or agent of record. Registration Number 35,050

☐ attorney or agent under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

R. Michael Ananian — December 11, 2009
Signature — Date

R. Michael Ananian — (650) 838-4300
Typed or printed name — Telephone Number

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

X Total of 1 Form is submitted.

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4).

Dated: December 11, 2009 Signature: _____ (Joe Clark)

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/045,625	11/07/2001	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
12/11/2009										
	Total (37 CFR 1.16(i))	* 28	Minus	** 24	= 4	X $ =		OR	X $52=	208
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	**208**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/LINDA HUMES/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,625	11/07/2001	Yeshik Shin	59472-8818US	1053

63170 7590 12/16/2009

PERKINS COIE LLP
P.O. BOX 1208
SEATTLE, WA 98111-1208

EXAMINER	
NGUYEN, STEVEN H D	
ART UNIT	PAPER NUMBER
2473	
MAIL DATE	DELIVERY MODE
12/16/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Interview Summary	Application No.	Applicant(s)	
	10/045,625	SHIN ET AL.	
	Examiner	Art Unit	
	Steven HD Nguyen	2473	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Steven Nguyen*. (3)_____.

(2) *Joseph Clark*. (4)_____.

Date of Interview: *12 December 2009*.

Type: a)☐ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☐ No.
If Yes, brief description: _____.

Claim(s) discussed: *the claims*.

Identification of prior art discussed: *the prior arts which is used to reject the claims*.

Agreement with respect to the claims f)☐ was reached. g)☒ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *the applicant and examiner discusses the different between the prior arts and the claimed invention*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

/Steven HD Nguyen/ Primary Examiner, Art Unit 2473	

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

———

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

63170 7590 02/16/2010

PERKINS COIE LLP
P.O. BOX 1208
SEATTLE, WA 98111-1208

EXAMINER	
NGUYEN, STEVEN H D	
ART UNIT	PAPER NUMBER
2473	

DATE MAILED: 02/16/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,625	11/07/2001	Yeshik Shin	59472-8818US	1053

TITLE OF INVENTION: METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	05/17/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

LENOVO EXHIBIT 1002 - 407/553

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

63170 7590 02/16/2010

PERKINS COIE LLP
P.O. BOX 1208
SEATTLE, WA 98111-1208

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,625	11/07/2001	Yeshik Shin	59472-8818US	1053

TITLE OF INVENTION: METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	05/17/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, STEVEN H D	2473	370-252000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

LENOVO EXHIBIT 1002 - 408/553

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,625	11/07/2001	Yeshik Shin	59472-8818US	1053

63170 7590 02/16/2010

PERKINS COIE LLP
P.O. BOX 1208
SEATTLE, WA 98111-1208

EXAMINER	
NGUYEN, STEVEN H D	
ART UNIT	PAPER NUMBER
2473	

DATE MAILED: 02/16/2010

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 1290 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 1290 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

LENOVO EXHIBIT 1002 - 409/553

Notice of Allowability	Application No.	Applicant(s)	
	10/045,625	SHIN ET AL.	
	Examiner	Art Unit	
	Steven HD Nguyen	2473	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/11/2009*.

2. ☐ The allowed claim(s) is/are *1-28*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Steven HD Nguyen/
Primary Examiner, Art Unit 2473

LENOVO EXHIBIT 1002 - 410/553

Issue Classification

Application/Control No.	Applicant(s)/Patent Under Reexamination
10045625	SHIN ET AL.
Examiner	**Art Unit**
Steven H Nguyen	2473

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
370	252	H 0 4 L 12 / 18 (2006.01.01)	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
370	411	503	528		

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	20	17												
2	2	21	18												
3	3	22	19												
4	4	23	20												
5	5	24	21												
6	6	25	22												
7	7	26	23												
8	8	27	24												
11	9	9	25												
12	10	18	26												
13	11	28	27												
14	12	10	28												
15	13														
16	14														
17	15														
19	16														

NONE

(Assistant Examiner) (Date)

Total Claims Allowed: 28

/Steven H Nguyen/
Primary Examiner.Art Unit 2473

(Primary Examiner) (Date)

O.G. Print Claim(s)	O.G. Print Figure
1	9a

LENOVO EXHIBIT 1002 - 411/553

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10045625	SHIN ET AL.
	Examiner	**Art Unit**
	Steven Nguyen	2419

SEARCHED			
Class	**Subclass**	**Date**	**Examiner**

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
See East text search	4/21/2009	ST
See east text search	2/3/2010	ST

INTERFERENCE SEARCH			
Class	**Subclass**	**Date**	**Examiner**
	See east text search	2/3/2010	st

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L6	219	idle adj symbol and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L7	117	idle with data and @ad<"20001120" and Storage with area with network	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L8	11	idle with data and @ad<"20001120" and resume with preempt$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L9	1246	idle with data and @ad<"20001120" and stop with start	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L10	4	idle with data and @ad<"20001120" and stop with start with congest$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L11	35	idle adj symbol and @ad<"20001120" and in-band	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L12	595823	idle with insert$3 control with data and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L13	90	idle with insert$3 with control with data and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L14	55	idle and preempt$3 with resume and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L15	5	idle adj2 (word symbol) and preempt$3 with resume and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L16	0	idle adj2 (word symbol) and pre-empt$3 with resume and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L17	55	idle adj2 (word symbol) and out adj2 band and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L18	50	idle adj2 (word symbol) same storage and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05

LENOVO EXHIBIT 1002 - 413/553

L19	493	idle with data with stream and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L20	452	idle with data with stream and @ad<"20001120"	USPAT	OR	ON	2010/02/04 00:05
L21	291	idle with data with stream and @ad<"20001120" and serial	USPAT	OR	ON	2010/02/04 00:05
L22	226	idle with data with transition and @ad<"20001120" and serial	USPAT	OR	ON	2010/02/04 00:05
L23	38	idle with data with transition and @ad<"20001120" and optimized	USPAT	OR	ON	2010/02/04 00:05
L24	0	idle with data with transition and @ad<"20001120" and transition with optimized	USPAT	OR	ON	2010/02/04 00:05
L25	0	idle adj (word symbol) and @ad<"20001120" and transition with optimized	USPAT	OR	ON	2010/02/04 00:05
L26	0	idle adj (word symbol) and @ad<"20001120" and transition with optimiz$3	USPAT	OR	ON	2010/02/04 00:05
L27	190	idle adj (word symbol) and @ad<"20001120" and (packet message) with (word symbol)	USPAT	OR	ON	2010/02/04 00:05
L28	3	"5608755" and in-band	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L29	0	"5608755" and in-band with symbol and out adj band with symbol	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L30	5	in-band with symbol and out adj band with symbol	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L31	45	in-band with symbol and out adj2 band with symbol	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L32	4	in-band with symbol and out adj2 band with symbol and @ad<"20001120"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05
L33	2	in-band with symbol and out adj2 band with symbol and @ad<"20001120" and (packet message)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/02/04 00:05

LENOVO EXHIBIT 1002 - 414/553

L34	92	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot) same (assign$4 allocat$3) with (additional more) adj3 (subchannel sub-channel slot sub-slot) and @ad<"20051128"	US-PGPUB; USPAT	OR	ON	2010/02/04 00:05
L35	114	(additional more increas $3) with (power gain energy) with (subchannel sub-channel slot sub-slot subcarrier sub-carrier) same (assign$4 allocat$3) with (additional more) adj3 (subchannel sub-channel slot sub-slot subcarrier sub-carrier) and @ad<"20051128"	US-PGPUB; USPAT	OR	ON	2010/02/04 00:05
L36	7	(("7069009") or ("20060078059") or ("20040127223") or ("7012912") or ("20060126749") or ("20020114269") or ("20050099937")).PN.	US-PGPUB; USPAT	OR	OFF	2010/02/04 00:05
L37	2	(("4924463") or ("6944152")).PN.	USPAT; USOCR	OR	OFF	2010/02/04 00:05

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2178	(packet frame message) with type with synchron$7 and @ad<"20001120"	USPAT; UPAD	OR	ON	2010/02/03 23:59
L2	32	(packet frame message) with type with synchron$7 with symbol and @ad<"20001120"	USPAT; UPAD	OR	ON	2010/02/04 00:00
L3	0	((packet frame message) near2 type and synchron$7 with symbol and align$7). clm. and @ad<"20001120"	USPAT; UPAD	OR	ON	2010/02/04 00:04
L4	20	((packet frame message) near2 type and synchron$7 and align$7).clm. and @ad<"20001120"	USPAT; UPAD	OR	ON	2010/02/04 00:04

LENOVO EXHIBIT 1002 - 415/553

L5	0	((packet frame message) near2 type and synchron$7 and align$7 same symbol). clm. and @ad< "20001120"	USPAT; UPAD	OR	ON	2010/02/04 00:04

2/ 4/ 2010 12:24:22 AM
C:\ Documents and Settings\ SNguyen\ My Documents\ EAST\ Workspaces\ 10045625all.wsp

LENOVO EXHIBIT 1002 - 416/553

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

63170 7590 02/16/2010

PERKINS COIE LLP
P.O. BOX 1208
SEATTLE, WA 98111-1208

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

EFS

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Joe Clark	(Depositor's name)
	(Signature)
13 May 2010	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,625	11/07/2001	Yeshik Shin	59472-8818US	1053

TITLE OF INVENTION: METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	05/17/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, STEVEN H D	2473	370-252000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 PERKINS COIE LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: SILICON IMAGE, INC.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): SUNNYVALE, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 502207 (enclose an extra copy of this form).

any additional fees

5. Change in Entity Status (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature R. Michael Ananian Date 5/13/2010

Typed or printed name R. Michael Ananian Registration No. 35,050

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

LENOVO EXHIBIT 1002 - 417/553

Electronic Patent Application Fee Transmittal

Application Number:	10045625
Filing Date:	07-Nov-2001
Title of Invention:	METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS
First Named Inventor/Applicant Name:	Yeshik Shin
Filer:	R. Michael Ananian/Joe Clark
Attorney Docket Number:	59472-8818US

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1810**

Electronic Acknowledgement Receipt

EFS ID:	7610008
Application Number:	10045625
International Application Number:	
Confirmation Number:	1053
Title of Invention:	METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS
First Named Inventor/Applicant Name:	Yeshik Shin
Customer Number:	63170
Filer:	R. Michael Ananian/Joe Clark
Filer Authorized By:	R. Michael Ananian
Attorney Docket Number:	59472-8818US
Receipt Date:	13-MAY-2010
Filing Date:	07-NOV-2001
Time Stamp:	18:32:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1810
RAM confirmation Number	4648
Deposit Account	502207
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	594728818US00_Issue_Fee.pdf	342638 74ef4306137b1e03ddaa67a115890a5bb50f46fe	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	32448 789cdb13d97c7fb54277fe05eb37ad977889f1d1	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	375086		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,625	06/29/2010	7746798	59472-8818US	1053

63170 7590 06/09/2010

PERKINS COIE LLP
P.O. BOX 1208
SEATTLE, WA 98111-1208

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 2511 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Yeshik Shin, Sunnyvale, CA;
David D. Lee, Palo Alto, CA;
Deog-Kyoon Jeong, Seoul, KOREA, REPUBLIC OF;
Shing Kong, Brisbane, CA;

LENOVO EXHIBIT 1002 - 422/553

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5533419

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
JEFFERIES FINANCE LLC	05/17/2019

RECEIVING PARTY DATA

Name:	LATTICE SEMICONDUCTOR CORPORATION
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	SILICON IMAGE, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	SIBEAM, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	DVDO, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124

PROPERTY NUMBERS Total: 1143

Property Type	Number
Patent Number:	5574678
Patent Number:	5510738
Patent Number:	5493205
Patent Number:	5617064
Patent Number:	5670907

Property Type	Number
Patent Number:	5490074
Patent Number:	5596524
Patent Number:	5491433
Patent Number:	5756367
Patent Number:	5594687
Patent Number:	5570046
Patent Number:	5583451
Patent Number:	5621650
Patent Number:	5521529
Patent Number:	5818254
Patent Number:	5781030
Patent Number:	5638018
Patent Number:	5589782
Patent Number:	6531890
Patent Number:	5586044
Patent Number:	5469368
Patent Number:	5764078
Patent Number:	5612631
Patent Number:	5869981
Patent Number:	5594365
Patent Number:	5811986
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Patent Number:	5594657
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Patent Number:	5679599
Patent Number:	5565794
Patent Number:	5742542
Patent Number:	5700698
Patent Number:	5604370
Patent Number:	5635855
Patent Number:	5570039
Patent Number:	5559450
Patent Number:	5581126
Patent Number:	5528170
Patent Number:	5615150
Patent Number:	5587945
Patent Number:	5666309

Property Type	Number
Patent Number:	5587921
Patent Number:	5672521
Patent Number:	5809522
Patent Number:	5739713
Patent Number:	5736888
Patent Number:	5719516
Patent Number:	5598346
Patent Number:	5623217
Patent Number:	5926841
Patent Number:	5646901
Patent Number:	5751163
Patent Number:	5666087
Patent Number:	5748525
Patent Number:	5864486
Patent Number:	5789939
Patent Number:	5723984
Patent Number:	5808942
Patent Number:	5830795
Patent Number:	5760609
Patent Number:	5796295
Patent Number:	5751164
Patent Number:	5734275
Patent Number:	5818294
Patent Number:	5801551
Patent Number:	5942780
Patent Number:	5796750
Patent Number:	5740069
Patent Number:	5960274
Patent Number:	5959336
Patent Number:	5862365
Patent Number:	5760605
Patent Number:	5761116
Patent Number:	5991907
Patent Number:	5805607
Patent Number:	5811987
Patent Number:	5892962
Patent Number:	5717342
Patent Number:	6028993

Property Type	Number
Patent Number:	5841701
Patent Number:	5904575
Patent Number:	5885904
Patent Number:	6190966
Patent Number:	5905385
Patent Number:	5844912
Patent Number:	5835405
Patent Number:	6087275
Patent Number:	6034541
Patent Number:	5949279
Patent Number:	5989957
Patent Number:	5978272
Patent Number:	6028447
Patent Number:	6072351
Patent Number:	6359466
Patent Number:	6020755
Patent Number:	6097212
Patent Number:	5854114
Patent Number:	6028463
Patent Number:	6216191
Patent Number:	5986471
Patent Number:	6060902
Patent Number:	6049224
Patent Number:	6043677
Patent Number:	6389321
Patent Number:	6003150
Patent Number:	6275064
Patent Number:	6127843
Patent Number:	6034544
Patent Number:	5982193
Patent Number:	5990702
Patent Number:	6107823
Patent Number:	5986480
Patent Number:	6134703
Patent Number:	6102963
Patent Number:	6130551
Patent Number:	6034538
Patent Number:	6025637

Property Type	Number
Patent Number:	6023570
Patent Number:	6093946
Patent Number:	6128770
Patent Number:	6064225
Patent Number:	5982683
Patent Number:	6556154
Patent Number:	6108806
Patent Number:	6154050
Patent Number:	6104207
Patent Number:	6133750
Patent Number:	6002610
Patent Number:	6225821
Patent Number:	6304099
Patent Number:	6066977
Patent Number:	6255847
Patent Number:	6087696
Patent Number:	6202182
Patent Number:	6028758
Patent Number:	6091595
Patent Number:	6043969
Patent Number:	6124732
Patent Number:	6028446
Patent Number:	6064105
Patent Number:	6087854
Patent Number:	6347387
Patent Number:	6424003
Patent Number:	6228696
Patent Number:	6154051
Patent Number:	6229336
Patent Number:	6169432
Patent Number:	6291327
Patent Number:	6221733
Patent Number:	6191612
Patent Number:	5912550
Patent Number:	6218857
Patent Number:	6261944
Patent Number:	6009033
Patent Number:	6353352

Property Type	Number
Patent Number:	6133769
Patent Number:	6404006
Patent Number:	5969992
Patent Number:	6175266
Patent Number:	6163168
Patent Number:	6124730
Patent Number:	6100715
Patent Number:	6081473
Patent Number:	6204686
Patent Number:	6214666
Patent Number:	6232631
Patent Number:	6282123
Patent Number:	6294810
Patent Number:	6157568
Patent Number:	6294809
Patent Number:	6215700
Patent Number:	6197638
Patent Number:	6097664
Patent Number:	6181163
Patent Number:	6211695
Patent Number:	5999449
Patent Number:	6297128
Patent Number:	6294811
Patent Number:	6075724
Patent Number:	6255169
Patent Number:	6133164
Patent Number:	6256758
Patent Number:	6075293
Patent Number:	6207989
Patent Number:	6031365
Patent Number:	6163175
Patent Number:	6326663
Patent Number:	6172392
Patent Number:	6284626
Patent Number:	6265900
Patent Number:	6413826
Patent Number:	6424000
Patent Number:	6274898

Property Type	Number
Patent Number:	6552595
Patent Number:	6118693
Patent Number:	6067252
Patent Number:	6184713
Patent Number:	6150841
Patent Number:	6628660
Patent Number:	6028789
Patent Number:	6034893
Patent Number:	6404226
Patent Number:	6550030
Patent Number:	6574761
Patent Number:	6191609
Patent Number:	6294925
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Patent Number:	6507212
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Patent Number:	6348813
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Patent Number:	6832231
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Patent Number:	6515899
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Patent Number:	7003066
Patent Number:	6999543
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Patent Number:	6661254
Patent Number:	6674303
Patent Number:	6605959
Patent Number:	7154298

Property Type	Number
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Patent Number:	6653861
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Patent Number:	6636442
Patent Number:	6845044
Patent Number:	6680625
Patent Number:	6781170
Patent Number:	6600188
Patent Number:	6621298
Patent Number:	6795959
Patent Number:	6907439
Patent Number:	6976047
Patent Number:	6639431
Patent Number:	6660579
Patent Number:	7032162
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Patent Number:	6600341
Patent Number:	6714048
Patent Number:	6657458
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Patent Number:	6717451
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Property Type	Number
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Patent Number:	6841447
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Property Type	Number
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Patent Number:	6859066
Patent Number:	7305047
Patent Number:	7339952
Patent Number:	6870395
Application Number:	10392751
Patent Number:	6967500
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Patent Number:	7098685
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Patent Number:	6737702
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Patent Number:	6909663
Patent Number:	7269771
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Patent Number:	7224213
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Patent Number:	7161862
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Patent Number:	7265578
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Patent Number:	7256613
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Application Number:	11206282
Patent Number:	7301182
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Patent Number:	7631223
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Patent Number:	7657773
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Patent Number:	7675313
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Patent Number:	7831754
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Patent Number:	7725803
Patent Number:	7429875
Patent Number:	7443192
Patent Number:	7623391
Patent Number:	7576563
Patent Number:	7313025
Patent Number:	7430706
Patent Number:	7598765
Patent Number:	7536615
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Patent Number:	7539076
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Patent Number:	7788620
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Patent Number:	7863931
Patent Number:	7902865
Patent Number:	7535253
Patent Number:	7788623
Patent Number:	7586325
Patent Number:	7728625
Patent Number:	7605609

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Patent Number:	7646643
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Patent Number:	8069329
Patent Number:	7652500
Patent Number:	7890913
Patent Number:	7459935
Patent Number:	7831856
Patent Number:	7661878
Patent Number:	7558143
Patent Number:	7557606
Patent Number:	7696784
Patent Number:	7560953
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Patent Number:	7741865
Patent Number:	7876125
Patent Number:	7868654
Patent Number:	7737723
Patent Number:	8044682

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Patent Number:	8255733
Patent Number:	7969248
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Patent Number:	8319521
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Patent Number:	8539409
Patent Number:	8495264
Patent Number:	8314632
Patent Number:	8451679
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Patent Number:	8370691
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Patent Number:	8912933
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Patent Number:	8643398
Patent Number:	8643168
Patent Number:	8686773
Patent Number:	8797064
Application Number:	13764221
Patent Number:	8786482
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Patent Number:	8829944
Application Number:	13155261
Application Number:	13412408
Application Number:	13466463
Application Number:	13681782
Application Number:	13777243
Application Number:	13858422
Application Number:	13868738
Application Number:	13901853
Application Number:	13904861
Application Number:	13947553

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Application Number:	14021513
Application Number:	14043920
Application Number:	14053026
Application Number:	14070975
Application Number:	14095310
Application Number:	14136482
Application Number:	14137443
Application Number:	14147796
Application Number:	14172678
Application Number:	14179651
Application Number:	14194484
Application Number:	14220377
Application Number:	14223096
Application Number:	14245920
Application Number:	14271331
Application Number:	14271955
Application Number:	14283329
Application Number:	14308747
Application Number:	14313443
Application Number:	14313778
Application Number:	14316049
Application Number:	14319481
Application Number:	14320169
Application Number:	14320074
Application Number:	14327811
Application Number:	14339164
Application Number:	14339229
Application Number:	14482001
Application Number:	14509564
Application Number:	14525240
Application Number:	14535454
Application Number:	14535351
Application Number:	14558851
Application Number:	14576348
Application Number:	14576245
Application Number:	14604515
Application Number:	14609181
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Property Type	Number
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Application Number:	14611069
Application Number:	14611095
Patent Number:	7427874
Patent Number:	7327160
Patent Number:	6786564
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Application Number:	13403146
Application Number:	12242665
Application Number:	14196978
Application Number:	14474005
Application Number:	61989417
Application Number:	61988812
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Property Type	Number
Application Number:	61991126
Application Number:	61989411
Application Number:	14463146
Application Number:	14578266
Application Number:	14578257
Application Number:	62089767
Patent Number:	8482462
Patent Number:	8207892
Patent Number:	8374558
Patent Number:	8213872
Patent Number:	8256123
Application Number:	14196993
Application Number:	13988047
Application Number:	14002353
Application Number:	13726822
Application Number:	13859764
Application Number:	62100841
Patent Number:	8571126
Application Number:	14065420
Patent Number:	8605823
Application Number:	14101274
Patent Number:	8484277
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Application Number:	14089094
Application Number:	13519302
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Application Number:	14331144
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Application Number:	14235783
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Application Number:	14240405
Application Number:	14364002
Patent Number:	6157360
Patent Number:	5955929
Patent Number:	5969552
Patent Number:	6259427
Patent Number:	6374361
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Property Type	Number
Patent Number:	6940496
Patent Number:	6564269
Patent Number:	6307543
Patent Number:	6492984
Patent Number:	6891910
Patent Number:	6326826
Patent Number:	6954491
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Patent Number:	6587158
Patent Number:	6219747
Patent Number:	6385692
Patent Number:	6393505
Patent Number:	6473476
Patent Number:	6867814
Patent Number:	7203557
Patent Number:	7408992
Patent Number:	7123307

Property Type	Number
Patent Number:	6944804
Patent Number:	6625560
Patent Number:	6845461
Patent Number:	6809567
Patent Number:	7062004
Patent Number:	7023487
Patent Number:	7558326
Patent Number:	7359437
Patent Number:	7257163
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Patent Number:	6714206
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Patent Number:	7113507
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Patent Number:	7340558
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Property Type	Number
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Patent Number:	7456648
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Patent Number:	6819166
Patent Number:	7348991
Patent Number:	6873341
Patent Number:	7539304
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Patent Number:	7937644
Patent Number:	8099648
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Property Type	Number
Patent Number:	7793179
Patent Number:	7782934
Patent Number:	7450038
Patent Number:	8595434
Application Number:	14067363
Patent Number:	7571269
Patent Number:	7602253
Patent Number:	7984369
Patent Number:	7949863
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Patent Number:	7849339
Patent Number:	7365659
Application Number:	12778882
Patent Number:	7836223
Patent Number:	8695034
Patent Number:	8599315
Application Number:	14070373
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Patent Number:	7911956
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Patent Number:	7936790
Patent Number:	8001334
Patent Number:	7979589
Application Number:	13298001
Patent Number:	6944086
Patent Number:	7016255
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Property Type	Number
Patent Number:	7904566
Patent Number:	8386867
Patent Number:	8667354
Patent Number:	8924805
Patent Number:	8086886
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Application Number:	12966194
Patent Number:	8325757
Patent Number:	8510487
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Application Number:	13021958
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Property Type	Number
Application Number:	13434273
Patent Number:	8624960
Application Number:	14094668
Patent Number:	8698958
Application Number:	13753408
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Patent Number:	8537201
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Patent Number:	8559746
Application Number:	14054575
Patent Number:	8452117
Patent Number:	8891897
Application Number:	13335398
Application Number:	13546904
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Property Type	Number
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Patent Number:	8014416
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Patent Number:	8155712
Patent Number:	8022887
Application Number:	11752073
Patent Number:	7675465
Application Number:	12215959
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Patent Number:	8170522
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Patent Number:	8831225
Patent Number:	7948961
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Application Number:	12164757
Patent Number:	8229352
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Patent Number:	7915909
Application Number:	12164907
Application Number:	12165468
Patent Number:	8897719
Patent Number:	8341271
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Patent Number:	8588193
Patent Number:	8457026
Application Number:	13113318
Application Number:	14128551
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Application Number:	13460393
Patent Number:	8925003
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Application Number:	13770984
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Property Type	Number
Application Number:	13834927
Patent Number:	8841974
Application Number:	14193932
Application Number:	13787664
Application Number:	13738768
Patent Number:	8832338
Application Number:	14123037
Application Number:	13776577
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Patent Number:	8786776
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Patent Number:	7916780
Patent Number:	7737802
Patent Number:	8680712
Application Number:	13521739
Application Number:	13521762
Application Number:	14381186
Application Number:	13844152
Application Number:	14391382
Application Number:	14165340
Patent Number:	8928411
Application Number:	14165345
Application Number:	14209785
Application Number:	14296377
Application Number:	14368781
Application Number:	14163981
Application Number:	14253808
Application Number:	14279316
Application Number:	14383865
Application Number:	61949901
Application Number:	14563797

Property Type	Number
Application Number:	14470750
Application Number:	14275692
Application Number:	14339393
Application Number:	14145715
Patent Number:	8854548
Application Number:	14470613
Application Number:	14184647
Application Number:	14181446
Application Number:	14470804
Application Number:	14470809
Application Number:	61943267
Application Number:	14278255
Application Number:	14322753
Application Number:	61947704
Application Number:	14460737
Application Number:	14502928
Application Number:	61973837
Application Number:	61975517
Application Number:	61979477
Application Number:	61979483
Application Number:	14470620
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Application Number:	61989409
Application Number:	14300166
Application Number:	14483013
Application Number:	62043218
Application Number:	14559523
Application Number:	14516136
Application Number:	62061630
Application Number:	62075554
Application Number:	14570817
Application Number:	14589889
Application Number:	14589925
Application Number:	14591845
Application Number:	14449095
Application Number:	12842190

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NAME OF SUBMITTER:	URMILA KARANDIKAR
SIGNATURE:	/Urmila Karandikar/
DATE SIGNED:	05/21/2019
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 97

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RELEASE OF A SECURITY INTEREST -- PATENTS

May 17, 2019

WHEREAS, pursuant to that certain (i) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035222, Frame 0866, (ii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035308, Frame 0428, (iii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035223, Frame 0001, (iv) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035226, Frame 0289, (v) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035223, Frame 0387, (vi) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035226, Frame 0147, (vii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035220, Frame 0048, (viii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035220, Frame 0226, (ix) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035309, Frame 0142, (x) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035308, Frame 0345, (xi) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035225, Frame 0839 and (xii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035225, Frame 0352, LATTICE SEMICONDUCTOR CORPORATION, SILICON IMAGE, INC., SIBEAM, INC. and DVDO, INC., each a Delaware corporation (each, a "Releasee"), granted to JEFFERIES FINANCE LLC, as collateral agent for the ratable benefit of the Secured Creditors (the "Releasor"), a continuing security interest in all right, title and interest of the Releasees in, to and under United States Patents listed on the attached Schedule A (the "Patents"), and all Proceeds in respect thereof (with all of the Releasee's rights listed above being collectively referred to as the "Collateral") to secure the payment, performance and observance of the Obligations;

WHEREAS, the Releasees have satisfied their Obligations; and

WHEREAS, the Releasee has requested and the Releasor has agreed to provide a document suitable for recording in the United States Patent and Trademark Office evidencing and effecting the release, relinquishment and discharge of its security interest in the Collateral.

NOW, THEREFORE, in consideration of and in exchange for good and valuable consideration, the Releasor hereby agrees as follows:

1. Defined Terms. All capitalized terms used but not otherwise defined herein have the meanings given to them in the Grants of Security Interests in United States Patents.

2. Release of Security Interest. The Releasor hereby, without any representation and warranty and without any recourse to the Releasor, releases, relinquishes and discharges all of its security interest in the Collateral.

[Signature Page Follows]

LENOVO EXHIBIT 1002 - 457/553

IN WITNESS WHEREOF, the undersigned has executed and delivered this Release as of the date first written above.

JEFFERIES FINANCE LLC,
as Collateral Agent and Releasor

By: _____
Name: Paul Chisholm
Title: Managing Director

LENOVO EXHIBIT 1002 - 458/553

SCHEDULE A

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/396,994	5574678	United States	Continuous Time Programmable Analog Block Architecture	Issued	Lattice Semiconductor Corporation
08/403,359	5510738	United States	CMOS Programmable Resistor-Based Transconductor	Issued	Lattice Semiconductor Corporation
08/403,354	5493205	United States	Low Distortion Differential Transconductor Output Current Mirror	Issued	Lattice Semiconductor Corporation
08/403,352	5617064	United States	Active Resistor For Stability Compensation [of Transconductor & Op-Amp Based Gain & Filter Stages]	Issued	Lattice Semiconductor Corporation
08/403,595	5670907	United States	VBB Reference for Pumped Substrates	Issued	Lattice Semiconductor Corporation
08/423,303	5490074	United States	Constant delay interconnect for coupling configurable logic blocks	Issued	Lattice Semiconductor Corporation
08/427,117	5596524	United States	CMOS memory cell with gate oxide of both NMOS and PMOS transistors as tunneling window for program and erase	Issued	Lattice Semiconductor Corporation
08/444,306	5491433	United States	Cascode array cell partitioning for a sense amplifier of a programmable logic device	Issued	Lattice Semiconductor Corporation
08/449,384	5756367	United States	Method of making a spacer based antifuse structure for low capacitance and high reliability	Issued	Lattice Semiconductor Corporation
08/447,991	5594687	United States	Completely complementary MOS memory cell with tunneling through the NMOS and PMOS transistors during program and erase	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/453,184	5570046	United States	Lead frame with noisy and quiet Vss and Vdd leads	Issued	Lattice Semiconductor Corporation
08/453,479	5583451	United States	Polarity control circuit which may be used with a ground bounce limiting buffer	Issued	Lattice Semiconductor Corporation
08/456,946	5621650	United States	Programmable gate array with improved interconnect structure, input/output structure and configurable logic block	Issued	Lattice Semiconductor Corporation
08/459,960	5521529	United States	Very high-density complex programmable logic device with a multi-tiered hierarchical switch matrix and optimized flexible logic allocation	Issued	Lattice Semiconductor Corporation
08/459,230	5818254	United States	Multi-tiered hierarchical high speed switch matrix structure for very high-density complex programmable logic devices	Issued	Lattice Semiconductor Corporation
08/459,234	5781030	United States	Programmable uniform symmetrical distribution logic allocator for a high-density complex PLD	Issued	Lattice Semiconductor Corporation
08/459,786	5638018	United States	P-type flip flop	Issued	Lattice Semiconductor Corporation
08/458,865	5589782	United States	Macrocell and clock signal allocation circuit for a programmable logic device (PLD) enabling PLD resources to provide multiple functions	Issued	Lattice Semiconductor Corporation
08/459,570	6531890	United States	Programmable optimized-distribution logic allocator for a high-density complex PLD	Issued	Lattice Semiconductor Corporation
08/461,196	5586044	United States	Array of configurable logic blocks including cascadable lookup tables	Issued	Lattice Semiconductor Corporation
08/462,934	5469368	United States	Array of configurable logic blocks each including a first	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 460/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			lookup table coupled to selectively replace an output of second lookup with an alternate function output		Corporation
08/486,178	5764078	United States	Family of multiple segmented programmable logic blocks interconnected by a high speed centralized switch matrix	Issued	Lattice Semiconductor Corporation
08/474,629	5612631	United States	An I/O macrocell for a programmable logic device	Issued	Lattice Semiconductor Corporation
08/479,872	5869981	United States	A High density programmable logic device	Issued	Lattice Semiconductor Corporation
08/486,174	5594365	United States	Architecture of a multiple array high density programmable logic device with a plurality of programmable switch matrices	Issued	Lattice Semiconductor Corporation
08/474,635	5811986	United States	Flexible synchronous/asynchronous cell structure for a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/466,438	5754471	United States	Reference for CMOS memory cell having PMOS and NMOS transistors with a common floating gate	Issued	Lattice Semiconductor Corporation
08/466,438	5754471	United States	Low power CMOS array for a PLD with program and erase using controlled avalanche injection	Issued	Lattice Semiconductor Corporation
08/473,620	5594657	United States	Field Programmable Gate Array Using Look-Up Tables, Multiplexers and Decoders	Issued	Lattice Semiconductor Corporation
08/483,623	5617042	United States	Multiple array programmable logic device with a plurality of programmable switch matrices	Issued	Lattice Semiconductor Corporation
08/492,604	5526278	United States	System for Synthesizing Field Programmable Gate Array	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 461/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Implementations From High Level Circuit Descriptions		Corporation
08/493,640	5679599	United States	Isolation using self-aligned trench formation and conventional LOCOS	Issued	Lattice Semiconductor Corporation
08/494,271	5565794	United States	Voltage range tolerant CMOS output buffer with reduced input capacitance	Issued	Lattice Semiconductor Corporation
08/497,992	5742542	United States	Nonvolatile memory cells using only positive charge to store data	Issued	Lattice Semiconductor Corporation
08/500,295	5700698	United States	Method for screening non-volatile memory and programmable logic devices	Issued	Lattice Semiconductor Corporation
08/501,230	5604370	United States	Field Implant For Semiconductor Device	Issued	Lattice Semiconductor Corporation
08/505,837	5635855	United States	Method for Simultaneous Programming of In-System Programmable Integrated Circuits	Issued	Lattice Semiconductor Corporation
08/507,893	5570039	United States	Method and Apparatus for Converting Field-Programmable Gate Array Implementations Into Mask-Programmable Logic Cell Implementations	Issued	Lattice Semiconductor Corporation
08/507,957	5559450	United States	Programmable Function Unit As Parallel Multiplier Cell	Issued	Lattice Semiconductor Corporation
08/528,030	5581126	United States	Interlaced layout configuration for differential pairs of interconnect lines	Issued	Lattice Semiconductor Corporation
08/535,362	5528170	United States	Low-Skew Signal Routing In A Programmable Array	Issued	Lattice Semiconductor Corporation
08/551,974	5615150	United States	control gate-addressed cmos non-volatile cell that programs through gates of CMOS transistors	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 462/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/554,092	5587945	United States	CMOS EEPROM cell with tunneling window in the read path	Issued	Lattice Semiconductor Corporation
08/560,038	5666309	United States	Memory cell for a programmable logic device (PLD) avoiding pumping programming voltage above an NMOS threshold	Issued	Lattice Semiconductor Corporation
08/560,933	5587921	United States	Array of configurable logic blocks each including a lookup table having inputs coupled to a first multiplexer and having outputs to a second multiplexer	Issued	Lattice Semiconductor Corporation
08/561,306	5672521	United States	Method of forming multiple gate oxide thicknesses on a wafer substrate	Issued	Lattice Semiconductor Corporation
08/573,622	5809522	United States	Microprocessor system with process identification tag entries to reduce cache flushing after a context switch	Issued	Lattice Semiconductor Corporation
08/574,776	5739713	United States	Deconvolution input buffer compensating for capacitance of a switch matrix of a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/575,898	5736888	United States	Capacitance elimination circuit	Issued	Lattice Semiconductor Corporation
08/575,852	5719516	United States	Clock generator circuit for use with a dual edge register that provides a separate enable for each edge over an input clock signal	Issued	Lattice Semiconductor Corporation
08/596,679	5598346	United States	Array of configurable logic blocks including network means for broadcasting clock signals to different pluralities of logic blocks	Issued	Lattice Semiconductor Corporation
08/606,702	5623217	United States	Field Programmable Gate Array With Write-Port Enabled Memory	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/614,728	5926841	United States	Segment descriptor cache for a processor	Issued	Lattice Semiconductor Corporation
08/625,403	5646901	United States	CMOS memory cell with tunneling during program and erase through the NMOS and PMOS transistors and a pass gate separating the NMOS and PMOS transistors	Issued	Lattice Semiconductor Corporation
08/632,811	5751163	United States	Parallel Programming of ISP Devices Using An Automatic Tester	Issued	Lattice Semiconductor Corporation
08/635,184	5666087	United States	Active Resistor For Stability Compensation [of Transconductor & Op-Amp Based Gain & Filter Stages]	Issued	Lattice Semiconductor Corporation
08/643,807	5748525	United States	Array cell circuit with split read/write line	Issued	Lattice Semiconductor Corporation
08/643,291	5864486	United States	Method And Apparatus For In-System Programming of A Programmable Logic Device Using a Two-Wire Interface	Issued	Lattice Semiconductor Corporation
08/653,186	5789939	United States	Very high-density complex programmable logic device with a multi-tiered hierarchical switch matrix and optimized flexible logic allocation	Issued	Lattice Semiconductor Corporation
08/659,279	5723984	United States	Field programmable gate array (FPGA) with interconnect encoding	Issued	Lattice Semiconductor Corporation
08/659,941	5808942	United States	Field programmable gate array (FPGA) having an improved configuration memory and look up table	Issued	Lattice Semiconductor Corporation
08/664,190	5830795	United States	Simplified masking process for programmable logic device manufacture	Issued	Lattice Semiconductor Corporation
08/666,193	5760609	United States	Clock signal providing circuit with enable and a pulse generator with enable for use	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 464/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			in a block clock circuit of a programmable logic device		
08/668,141	5796295	United States	Reference for CMOS memory cell having PMOS and NMOS transistors with a common floating gate	Issued	Lattice Semiconductor Corporation
08/668,896	5751164	United States	Programmable logic device with multi-level power control	Issued	Lattice Semiconductor Corporation
08/683,685	5734275	United States	Programmable logic device having a sense amplifier with virtual ground	Issued	Lattice Semiconductor Corporation
08/683,373	5818294	United States	Temperature insensitive current source	Issued	Lattice Semiconductor Corporation
08/690,768	5801551	United States	Depletion mode pass gates with controlling decoder and negative power supply for a programmable logic device	Issued	Lattice Semiconductor Corporation
08/689,523	5942780	United States	An integrated circuit having, and process providing, different oxide layer thicknesses on a substrate	Issued	Lattice Semiconductor Corporation
08/696,444	5796750	United States	Method for Programming a PLD In An Automatic Tester	Issued	Lattice Semiconductor Corporation
08/700,616	5740069	United States	Logic device (PLD) having direct connections between configurable logic blocks (CLBs) and configurable input/output blocks (IOBs)	Issued	Lattice Semiconductor Corporation
08/699,401	5960274	United States	Oxide formation process for manufacturing programmable logic device	Issued	Lattice Semiconductor Corporation
08/702,846	5959336	United States	Decoder circuit with short channel depletion transistors	Issued	Lattice Semiconductor Corporation
08/710,445	5862365	United States	Configuration Pin Emulation Circuit For a Field Programmable Array	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 465/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/723,082	5760605	United States	Programmable high speed routing switch	Issued	Lattice Semiconductor Corporation
08/726,512	5761116	United States	Vpp only scalable EEPROM memory cell having transistors with thin tunnel gate oxide	Issued	Lattice Semiconductor Corporation
08/729,117	5991907	United States	Method for Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/734,888	5805607	United States	Method for user-controlled I/O switching during in-circuit programming of CPLDs through the IEEE 1149.1 test access port	Issued	Lattice Semiconductor Corporation
08/740,948	5811987	United States	Block clock and initialization circuit for a complex high density PLD	Issued	Lattice Semiconductor Corporation
08/748,041	5892962	United States	FPGA-based Processor	Issued	Lattice Semiconductor Corporation
08/745,410	5717342	United States	Output buffer incorporating shared intermediate nodes	Issued	Lattice Semiconductor Corporation
08/781,882	6028993	United States	Timed Circuit Simulation In Hardware Using FPGAs	Issued	Lattice Semiconductor Corporation
08/785,096	5841701	United States	Method of charging and discharging floating gage transistors to reduce leakage current	Issued	Lattice Semiconductor Corporation
08/799,153	5904575	United States	Method and apparatus incorporating nitrogen selectively for differential oxide growth	Issued	Lattice Semiconductor Corporation
08/799,235	5885904	United States	Method to incorporate, and a device having, oxide enhancement dopants using gas immersion laser doping (GILD) for selectively growing an oxide layer	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 466/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/823,953	6190966	United States	Process for fabricating semiconductor memory device with high data retention including silicon nitride etch stop layer formed at high temperature with low hydrogen ion	Issued	Lattice Semiconductor Corporation
08/828,520	5905385	United States	Memory bits used to couple look up table inputs to facilitate increased availability to routing resources particularly for variable sized look up tables for a field programmable gate array (FPGA)	Issued	Lattice Semiconductor Corporation
08/831,372	5844912	United States	Fast verify for CMOS memory cell	Issued	Lattice Semiconductor Corporation
08/827,671	5835405	United States	Application Specific Modules in a Programmable Logic Device	Issued	Lattice Semiconductor Corporation
08/843,150	6087275	United States	Reduction of n-channel parasitic transistor leakage by using low power/low pressure phosphosilicate glass	Issued	Lattice Semiconductor Corporation
08/838,487	6034541	United States	In-System Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
08/856,926	5949279	United States	Devices for sourcing constant supply current from power supply in system with integrated circuit having variable supply current requirement	Issued	Lattice Semiconductor Corporation
08/859,761	5989957	United States	Process for fabricating semiconductor memory device with high data retention including silicon nitride etch stop layer formed at high temperature with low hydrogen ion concentration	Issued	Lattice Semiconductor Corporation
08/871,589	5978272	United States	Nonvolatile memory structure for programmable logic devices	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 467/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/899,428	6028447	United States	FPGA Having Predictable Open-Drain Drive Mode	Issued	Lattice Semiconductor Corporation
08/912,763	6072351	United States	Output buffer for making a high voltage (5.0 volt) compatible input/output in a low voltage (2.5 volt) semiconductor process	Issued	Lattice Semiconductor Corporation
08/931,798	6359466	United States	Circuitry to provide fast carry	Issued	Lattice Semiconductor Corporation
08/938,550	6020755	United States	Hybrid Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/948,306	6097212	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/947,888	5854114	United States	Data retention of EEPROM cell with shallow trench isolation using thicker liner oxide	Issued	Lattice Semiconductor Corporation
08/949,992	6028463	United States	Programmable Clock Manager For A Programmable Logic Device that Can Generate At Least Two Different Output Clocks	Issued	Lattice Semiconductor Corporation
08/950,444	6216191	United States	Field Programmable Gate Array Having A Dedicated Processor Interface	Issued	Lattice Semiconductor Corporation
08/950,446	5986471	United States	Bi-directional Buffers and Supplemental Logic and Interconnect Cells for Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
08/950,448	6060902	United States	A Programmable Clock Manager For A Programmable Logic Device that Can Be Programmed Without Reconfiguring the Device	Issued	Lattice Semiconductor Corporation
08/950,624	6049224	United States	Programmable Logic Device With Logic Cells Having A Flexible Input Structure	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/951,128	6043677	United States	Programmable Clock Manager For A Programmable Logic Device that Can Implement Delay-Locked Loop Functions	Issued	Lattice Semiconductor Corporation
08/964,421	6389321	United States	Simultaneous Wired and Wireless Remote In-System Programming of Multiple Remote Systems	Issued	Lattice Semiconductor Corporation
08/974,799	6003150	United States	Method for Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/996,361	6275064	United States	Symmetrical, extended and fast direct connections between variable grain blocks in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/996,049	6127843	United States	Dual port SRAM memory for run time use in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,615	6034544	United States	Programmable input/output block (IOB) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,614	5982193	United States	Input/output block (IOB) connections to MAXL lines, NOR lines and dendrites in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,612	5990702	United States	Flexible direct connections between input/output blocks (IOBs) and variable grain blocks (VBGs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/997,221	6107823	United States	Programmable control multiplexing for input/output blocks (IOBs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/996,119	5986480	United States	Multiple input zero power and/nor gate for use in a field programmable gate array (FPGA)	Issued	Lattice Semiconductor Corporation
08/996,530	6134703	United States	A Process for Programming PLDs and Embedded Non-Volatile Memories	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/998,978	6102963	United States	Electrically erasable and reprogrammable, nonvolatile integrated storage device with in-system programming and verification (ISPAV) capabilities for supporting in-system reconfiguring of PLD's	Issued	Lattice Semiconductor Corporation
09/008,762	6130551	United States	Synthesis-friendly FPGA architecture with variable length and variable timing interconnect	Issued	Lattice Semiconductor Corporation
09/010,000	6034538	United States	Virtual Logic System For Reconfigurable Hardware	Issued	Lattice Semiconductor Corporation
09/023,669	6025637	United States	Spacer based antifuse structure for low capacitance and high reliability and method of fabrication thereof	Issued	Lattice Semiconductor Corporation
09/023,506	6023570	United States	Sequential and Simultaneous Manufacturing Programming of Multiple In-System Programmable Systems Through a Data Network	Issued	Lattice Semiconductor Corporation
09/026,814	6093946	United States	EEPROM cell with field-edgeless tunnel window using shallow trench isolation process	Issued	Lattice Semiconductor Corporation
09/037,095	6128770	United States	Configurable logic array including IOB to longlines interconnect means for providing selectable access to plural longlines from each IOB (input/output block)	Issued	Lattice Semiconductor Corporation
09/045,128	6064225	United States	Global Signal Distribution With Reduced Routing Tracks In An FPGA	Issued	Lattice Semiconductor Corporation
09/046,404	5982683	United States	Enhanced method of testing semiconductor devices having nonvolatile elements	Issued	Lattice Semiconductor Corporation
09/053,251	6556154	United States	Offset Voltage Calibration DAC With Reduced Sensitivity To Mismatch	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 470/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Errors		
09/059,552	6108806	United States	Method of Testing and Diagnosing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/067,320	6154050	United States	Internal tristate bus with arbitration logic	Issued	Lattice Semiconductor Corporation
09/067,318	6104207	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/069,035	6133750	United States	Combination of global clock and localized clocks	Issued	Lattice Semiconductor Corporation
09/069,768	6002610	United States	Non-Volatile Memory Element For Programmable Logic Applications and Operational Methods Therefor	Issued	Lattice Semiconductor Corporation
09/080,906	6225821	United States	Package migration for related programmable logic devices	Issued	Lattice Semiconductor Corporation
09/083,335	6304099	United States	Method and structure for dynamic in-system programming	Issued	Lattice Semiconductor Corporation
09/083,336	6066977	United States	Programmable Output Voltage Levels	Issued	Lattice Semiconductor Corporation
09/083,205	6255847	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/086,437	6087696	United States	Stacked tunneling dielectric technology for improving data retention of EEPROM cell	Issued	Lattice Semiconductor Corporation
09/109,123	6202182	United States	Method and Apparatus For Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/114,385	6028758	United States	Electrostatic discharge (ESD) protection for a 5.0 volt compatible input/output (I/O) in a 2.5 volt semiconductor process	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 471/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/114,717	6091595	United States	Electrostatic discharge (ESD) protection for NMOS pull up transistors of a 5.0 volt compatible output buffer using 2.5 volt process transistors	Issued	Lattice Semiconductor Corporation
09/114,718	6043969	United States	Ballast resistors with parallel stacked NMOS transistors used to prevent secondary breakdown during ESD with 2.5 volt process transistors	Issued	Lattice Semiconductor Corporation
09/115,683	6124732	United States	Signaling Voltage Range Discriminator	Issued	Lattice Semiconductor Corporation
09/118,200	6028446	United States	Flexible Synchronous and Asynchronus Circuits for A Very High Density Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/134,174	6064105	United States	Data retention of EEPROM cell with shallow trench isolation using thicker liner oxide	Issued	Lattice Semiconductor Corporation
09/145,793	6087854	United States	High Speed Line Driver With Direct and Complementary Outputs	Issued	Lattice Semiconductor Corporation
09/169,848	6347387	United States	Test Circuits For Multiple FPGA Systems	Issued	Lattice Semiconductor Corporation
09/169,492	6424003	United States	EEPROM cell with self-aligned tunneling window	Issued	Lattice Semiconductor Corporation
09/187,691	6228696	United States	Semiconductor-oxide-semiconductor capacitor formed in integrated circuit	Issued	Lattice Semiconductor Corporation
09/187,689	6154051	United States	Tileable and compact layout for super variable grain blocks within FPGA device	Issued	Lattice Semiconductor Corporation
09/186,917	6229336	United States	Programmable integrated circuit device with slew control and skew control	Issued	Lattice Semiconductor Corporation
09/188,778	6169432	United States	High voltage switch for	Issued	Lattice

LENOVO EXHIBIT 1002 - 472/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			providing voltages higher than 2.5 volts with transistors made using a 2.5 volt process		Semiconductor Corporation
09/192,094	6291327	United States	Optimization of S/D annealing to minimize random S/D shorts in memory array	Issued	Lattice Semiconductor Corporation
09/192,096	6221733	United States	Reduction of mechanical stress in shallow trench isolation process	Issued	Lattice Semiconductor Corporation
09/196,449	6191612	United States	Enhanced I/O control flexibility for generating control signals	Issued	Lattice Semiconductor Corporation
09/196,080	5912550	United States	Power converter with 2.5 semiconductor process components	Issued	Lattice Semiconductor Corporation
09/198,796	6218857	United States	Variable sized line driving amplifiers for input/output blocks (IOBs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/200,395	6261944	United States	Semiconductor device having high reliability passivation and fabrication method	Issued	Lattice Semiconductor Corporation
09/198,653	6009033	United States	Method of programming and erasing an EEPROM device under an elevated temperature and apparatus thereof	Issued	Lattice Semiconductor Corporation
09/199,664	6353352	United States	Clock tree topology	Issued	Lattice Semiconductor Corporation
09/201,081	6133769	United States	Phase locked loop with a lock detector	Issued	Lattice Semiconductor Corporation
09/203,149	6404006	United States	EEPROM cell with tunneling across entire separated channels	Issued	Lattice Semiconductor Corporation
09/217,647	5969992	United States	EEPROM cell using p-well for	Issued	Lattice Semiconductor Corporation
09/207,558	6175266	United States	Operational amplifier with CMOS transistors made using	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			2.5 volt process transistors		Corporation
09/208,203	6163168	United States	Efficient interconnect network for use in FPGA device having variable grain architecture	Issued	Lattice Semiconductor Corporation
09/212,022	6124730	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/212,330	6100715	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/212,331	6081473	United States	FPGA integrated circuit having embedded SRAM memory blocks each with statically and dynamically controllable read mode	Issued	Lattice Semiconductor Corporation
09/216,662	6204686	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	Issued	Lattice Semiconductor Corporation
09/216,051	6214666	United States	Method of forming a non-volatile memory device	Issued	Lattice Semiconductor Corporation
09/217,648	6232631	United States	Floating gate memory cell structure with programming mechanism outside the read path	Issued	Lattice Semiconductor Corporation
09/217,646	6282123	United States	Method of fabricating, programming, and erasing a dual pocket two sided program/erase non-volatile memory cell	Issued	Lattice Semiconductor Corporation
09/218,987	6294810	United States	EEPROM cell with tunneling at separate edge and channel regions	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 474/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/220,469	6157568	United States	Avalanche programmed floating gate memory cell structure with program element in first polysilicon layer	Issued	Lattice Semiconductor Corporation
09/221,360	6294809	United States	Avalanche programmed floating gate memory cell structure with program element in polysilicon	Issued	Lattice Semiconductor Corporation
09/226,702	6215700	United States	PMOS avalanche programmed floating gate memory cell structure	Issued	Lattice Semiconductor Corporation
09/227,981	6197638	United States	Oxide formation process for manufacturing programmable logic device	Issued	Lattice Semiconductor Corporation
09/235,356	6097664	United States	Multi-port SRAM cell array having plural write paths including for writing through addressable port and through serial boundary scan	Issued	Lattice Semiconductor Corporation
09/235,351	6181163	United States	FPGA integrated circuit having embedded SRAM memory blocks and interconnect channel for broadcasting address and control	Issued	Lattice Semiconductor Corporation
09/235,615	6211695	United States	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	Issued	Lattice Semiconductor Corporation
09/239,072	5999449	United States	Two transistor EEPROM cell using P-well for tunneling across a channel	Issued	Lattice Semiconductor Corporation
09/240,560	6297128	United States	Process for manufacturing shallow trenches filled with dielectric material having low mechanical stress	Issued	Lattice Semiconductor Corporation
09/245,813	6294811	United States	Two transistor EEPROM cell	Issued	Lattice Semiconductor Corporation
09/255,410	6075724	United States	Method for sorting	Issued	Lattice

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			semiconductor devices having a plurality of non-volatile memory cells		Semiconductor Corporation
09/255,053	6255169	United States	Process for fabricating a high-endurance non-volatile memory device	Issued	Lattice Semiconductor Corporation
09/256,245	6133164	United States	Fabrication of oxide regions having multiple thicknesses using minimized number of thermal cycles	Issued	Lattice Semiconductor Corporation
09/261,776	6256758	United States	Fault Tolerance Operation of Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/263412	6075293	United States	Semiconductor device having a multi-layer metal interconnect structure	Issued	Lattice Semiconductor Corporation
09/268,897	6207989	United States	Non-volatile memory device having a high-reliability composite insulation layer	Issued	Lattice Semiconductor Corporation
09/276,991	6031365	United States	Band gap reference using a low voltage power supply	Issued	Lattice Semiconductor Corporation
09/276,990	6163175	United States	High voltage detector to control a power supply voltage pump for a 2.5 volt semiconductor process device	Issued	Lattice Semiconductor Corporation
09/277,441	6326663	United States	Avalanche injection EEPROM memory cell with p-type control gate	Issued	Lattice Semiconductor Corporation
09/280,887	6172392	United States	Boron doped silicon capacitor plate	Issued	Lattice Semiconductor Corporation
09/286,830	6284626	United States	Angled nitrogen ion implantation for minimizing mechanical stress on side walls of an isolation trench	Issued	Lattice Semiconductor Corporation
09/288,062	6265900	United States	High Speed Logical OR Circuit	Issued	Lattice Semiconductor Corporation
09/287,976	6413826	United States	Gate insulator process for	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			nanometer MOSFETs		Corporation
09/310,071	6424000	United States	Floating gate memory apparatus and method for selected programming thereof	Issued	Lattice Semiconductor Corporation
09/316,241	6274898	United States	Triple-well EEPROM cell using p-well for tunneling across a channel	Issued	Lattice Semiconductor Corporation
09/318,570	6552595	United States	High Voltage Discharge Scheme	Issued	Lattice Semiconductor Corporation
09/320389	6118693	United States	Electrically erasable non-volatile memory cell with integrated SRAM to reduce testing time	Issued	Lattice Semiconductor Corporation
09/320,392	6067252	United States	Electrically erasable non-volatile memory cell with no static power dissipation	Issued	Lattice Semiconductor Corporation
09/326,940	6184713	United States	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	Issued	Lattice Semiconductor Corporation
09/326,140	6150841	United States	Enhanced storage macrocell module for high density CPLD architectures	Issued	Lattice Semiconductor Corporation
09/330,753	6628660	United States	Finite State Machine with Associated Memory	Issued	Lattice Semiconductor Corporation
09/334,051	6028789	United States	Zero-power CMOS non-volatile memory cell having an avalanche injection element	Issued	Lattice Semiconductor Corporation
09/334,052	6034893	United States	Non-volatile memory cell having dual avalanche injection elements	Issued	Lattice Semiconductor Corporation
09/400,029	6404226	United States	Integrated Circuit With Standard Cell Logic and Spare Gates	Issued	Lattice Semiconductor Corporation
09/405,958	6550030	United States	On-Line Testing of the Programmable Logic Blocks In Field Programmable Gate	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Arrays		
09/406,219	6574761	United States	On-Line Testing of the Programmable Interconnect Network In Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/433,642	6191609	United States	Combination of global clock and localized clocks	Issued	Lattice Semiconductor Corporation
09/440,460	6294925	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/440,207	6278311	United States	Method for minimizing instantaneous currents when driving bus signals	Issued	Lattice Semiconductor Corporation
09/441,220	6208559	United States	Method of operating EEPROM memory cells having transistors with thin gate oxide and reduced disturb	Issued	Lattice Semiconductor Corporation
09/452,017	6137738	United States	Method For In-System Programming of Serially Configured EEPROMS Using a JTAG Interface of an FPGA	Issued	Lattice Semiconductor Corporation
09/454,322	6326808	United States	Inversion of Product Term Line Before or Logic in a Programmable Logic Device (PLD)	Issued	Lattice Semiconductor Corporation
09/472,645	6150842	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/506,180	6362684	United States	Amplifier Having an Adjustable Resistor Network	Issued	Lattice Semiconductor Corporation
09/507,580	6424209	United States	Integrated Programmable Continuous Time Filter with Programmable Capacitor Arrays	Issued	Lattice Semiconductor Corporation
09/548,171	6351157	United States	Output buffer for making a high voltage (5.0 volt) compatible input/output in a low voltage (2.5 volt)	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			semiconductor process		
09/567,898	6288937	United States	Decoded Generic Routing Pool	Issued	Lattice Semiconductor Corporation
09/578,086	6570212	United States	Complementary avalanche injection EEPROM cell	Issued	Lattice Semiconductor Corporation
09/603,119	6292930	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/603,807	6216257	United States	FPGA device and method that includes a variable grain function architecture for implementing configuration logic blocks and a complimentary variable length interconnect architecture for providing configurable routing between configuration logic blocks	Issued	Lattice Semiconductor Corporation
09/611,449	6530049	United States	On-line Fault Tolerant Operation Via Incremental Reconfiguration of Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/626,094	6380759	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/632,319	6567969	United States	Configurable Logic Array Including Lookup Table Means For Generating Functions of Different Numbers Of Input Terms	Issued	Lattice Semiconductor Corporation
09/643,279	6627947	United States	Compact single-poly two-transistor EEPROM cell	Issued	Lattice Semiconductor Corporation
09/651,689	6433602	United States	High speed schmitt trigger with low supply voltage	Issued	Lattice Semiconductor Corporation
09/660,707	6370071	United States	High Voltage CMOS switch	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
09/661,585	6462576	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/668,896	6701340	United States	Double Differential Comparator and Programmable Analog Block Architecture Using Same	Issued	Lattice Semiconductor Corporation
09/669,186	6249144	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/671,853	6631487	United States	On-Line Testing of Field Programmable Gate Array Resources	Issued	Lattice Semiconductor Corporation
09/692,694	6470485	United States	Scalable and parallel processing methods and structures for testing configurable interconnect network in FPGA device	Issued	Lattice Semiconductor Corporation
09/704,487	6507212	United States	Wide input programmable logic system and method	Issued	Lattice Semiconductor Corporation
09/651,805	6455912	United States	Process for manufacturing shallow trenches filled with dielectric material having low mechanical stress	Issued	Lattice Semiconductor Corporation
09/712,000	6356107	United States	Method and structure for dynamic in-system programming	Issued	Lattice Semiconductor Corporation
09/721,153	6348813	United States	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	Issued	Lattice Semiconductor Corporation
09/732,216	6735706	United States	Programmable power management system and method	Issued	Lattice Semiconductor Corporation
09/731,184	6524911	United States	Combination of BPTEOS oxide film with CMP and RTA to achieve good data	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 480/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			retention		
09/731,185	6287916	United States	Method for forming a semiconductor device using LPCVD nitride to protect floating gate from charge loss	Issued	Lattice Semiconductor Corporation
09/733,878	6526558	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	Issued	Lattice Semiconductor Corporation
09/775,488	6462602	United States	Voltage Level Translator Systems And Methods	Issued	Lattice Semiconductor Corporation
09/775,489	6414521	United States	Improved sense amplifier systems and methods	Issued	Lattice Semiconductor Corporation
09/818,257	6496969	United States	Programming Programmable Logic Devices Using Hidden Switches	Issued	Lattice Semiconductor Corporation
09/841,209	6590415	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/863,656	6535043	United States	Clock Signal Selection System, Method of Generating A Clock Signal And Programmable Clock Manager Including Same	Issued	Lattice Semiconductor Corporation
09/864,276	6486705	United States	Signal Distribution Scheme In Field Programmable Gate Array (FPGA) or Field Programmable Systems Chip (FPSC) Including Cycle Stealing Units	Issued	Lattice Semiconductor Corporation
09/864,284	6472904	United States	Double Data Rate Input And Output In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/864,289	6480026	United States	Multi-functional I/O Buffers In a Field Programmable Gate	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Array (FPGA)		Corporation
09/864,277	6483342	United States	Multi-Master Multi-Slave Bus In Field Programmable Gate Array (FPGA)	Issued	Lattice Semiconductor Corporation
09/864,290	6772230	United States	Field Programmable Gate Array (FPGA) Bit Stream Format	Issued	Lattice Semiconductor Corporation
09/870,877	6498538	United States	Low Jitter Integrated Phase Locked Loop With Broad Tuning Range	Issued	Lattice Semiconductor Corporation
09/870,541	6455375	United States	EEPROM tunnel window for program injection via P+ contacted inversion	Issued	Lattice Semiconductor Corporation
09/881,950	6614291	United States	Low Voltage, High Speed CMOS CML Latch and MUX Devices	Issued	Lattice Semiconductor Corporation
09/885,243	6429692	United States	High Speed Data Sampling With Reduced Metastability	Issued	Lattice Semiconductor Corporation
09/927,289	6492877	United States	Improved Coupling For LC-Based VCO	Issued	Lattice Semiconductor Corporation
09/927,612	6525617	United States	Buffering For LC-Based Stage	Issued	Lattice Semiconductor Corporation
09/927,793	6653860	United States	Enhanced logic macrocell with expanded PT (product term) sharing capability for Use in High Density CPLD Architectures	Issued	Lattice Semiconductor Corporation
09/941,454	6489835	United States	Low Voltage Bandgap Reference Circuit	Issued	Lattice Semiconductor Corporation
09/949,112	6593222	United States	Method to improve the reliability of thermosonic gold to aluminum wire bonds	Issued	Lattice Semiconductor Corporation
09/966,967	6832231	United States	Multiple Width Random Number Generation	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 482/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/011,549	6693830	United States	Single Poly Two-Transistor EEPROM Cell With Differentially Doped Floating Gate	Issued	Lattice Semiconductor Corporation
10/053,004	6989551	United States	Test structure for determining the minimum tunnel opening size in a non-volatile memory cell	Issued	Lattice Semiconductor Corporation
10/010,011	6515899	United States	Non-Volatile Memory Cell With Enhanced Cell Drive Current	Issued	Lattice Semiconductor Corporation
09/991,245	6611463	United States	Zero Power Programmable Memory Cell	Issued	Lattice Semiconductor Corporation
09/992,493	6489806	United States	Zero power logic cell for use in programmable logic devices	Issued	Lattice Semiconductor Corporation
10/006,559	7003066	United States	Digital Phase locked Loop with Phase Selector having Minimized Number of Phase Interpolators	Issued	Lattice Semiconductor Corporation
10/006,610	6999543	United States	Clock Data Recovery Deserializer With Programmable Sync Detect Logic	Issued	Lattice Semiconductor Corporation
10/006,516	6993108	United States	Digital Phase Locked Loop With Programmable Digital Filter	Issued	Lattice Semiconductor Corporation
10/021,873	6661254	United States	Programmable Interconnect Circuit With A Phase-Locked Loop	Issued	Lattice Semiconductor Corporation
10/017,725	6674303	United States	Programmable I/O cell with bidirectional and shift register capabilities	Issued	Lattice Semiconductor Corporation
10/017,859	6605959	United States	Structure and Method for Implementing Wide Multiplexers	Issued	Lattice Semiconductor Corporation
10/022,464	7154298	United States	Block oriented architecture for programmable interconnect circuit	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/021,844	6703860	United States	I/O Block for Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/023,053	6653861	United States	Multi-level Routing Structure for a Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/023,226	6650141	United States	High Speed Interface For a Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/059,624	6636442	United States	Non-volatile memory element having a cascoded transistor scheme to reduce oxide field stress	Issued	Lattice Semiconductor Corporation
10/061,057	6845044	United States	Method of preventing high Icc at start-up in zero-power EEPROM cells for PLD applications	Issued	Lattice Semiconductor Corporation
10/066,031	6680625	United States	Symmetrical CML Logic Gate System	Issued	Lattice Semiconductor Corporation
10/082,050	6781170	United States	Integrated Circuit Base Transistor Structure And Associated Programmable Cell Library	Issued	Lattice Semiconductor Corporation
10/083,728	6600188	United States	An EEPROM with neutralized doping at tunnel window edge	Issued	Lattice Semiconductor Corporation
10/090,209	6621298	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
10/103,100	6795959	United States	Integrated Delay Discriminator For Use With a Field- Programmable Gate Array and A Method of Determining a Time Delay Thereof	Issued	Lattice Semiconductor Corporation
10/106,509	6907439	United States	FFT address generation method and apparatus	Issued	Lattice Semiconductor Corporation
10/108,401	6976047	United States	Skipped carry incrementer for FFT address generation	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 484/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/112,370	6639431	United States	Differential Input Comparator	Issued	Lattice Semiconductor Corporation
10/128,943	6660579	United States	Zero Power Memory Cell With Improved Data Retention	Issued	Lattice Semiconductor Corporation
10/131,883	7032162	United States	Polynomial Expander for Generating Coefficients of a Polynomial from Roots of the Polynomial	Issued	Lattice Semiconductor Corporation
10/133,016	6765408	United States	Device and Method with Generic Logic Blocks	Issued	Lattice Semiconductor Corporation
10/135,308	6814296	United States	Integrated Circuit and Associated Design Method With Antenna Error Control Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/135,325	6600341	United States	Integrated Circuit and Associated Design Method Using Spare Gate Islands	Issued	Lattice Semiconductor Corporation
10/146,739	6714048	United States	Input Buffer With Selectable PCL, GTL, or PECL Compatibility	Issued	Lattice Semiconductor Corporation
10/146,826	6657458	United States	Output Buffer With Feedback From An Input Buffer To Provide Selectable PCL, GTL, or PECL Compatability	Issued	Lattice Semiconductor Corporation
10/146,769	6870391	United States	Input Buffer With CMOS Driver Gate Current Control Enabling Selectable PCL, GTL, or PECL Compatibility	Issued	Lattice Semiconductor Corporation
10/147,199	6714043	United States	Output Buffer Having Programmable Drive Current And Output Voltage Limits	Issued	Lattice Semiconductor Corporation
10/146,734	6720755	United States	Band Gap Reference Circuit	Issued	Lattice Semiconductor Corporation
10/147,011	6760209	United States	Electrostatic Discharge Protection Circuit	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/151,753	6798244	United States	Output Buffer With Overvoltage Protection	Issued	Lattice Semiconductor Corporation
10/150,410	6848095	United States	Method of Assigning Logic Functions To Macrocells In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/159,009	6583652	United States	Highly linear programmable transconductor with large input-signal range	Issued	Lattice Semiconductor Corporation
10/159,089	6717451	United States	Precision analog level shifter with programmable options	Issued	Lattice Semiconductor Corporation
10/159,681	6806771	United States	Multimode output stage converting differential to single-ended signals using current-mode input signals	Issued	Lattice Semiconductor Corporation
10/162,337	6596587	United States	Shallow junction EEPROM Device and Process for Fabricating the Device	Issued	Lattice Semiconductor Corporation
10/160,855	6794236	United States	EEPROM Device with Improved Capacitive Coupling and Fabrication Process	Issued	Lattice Semiconductor Corporation
10/161,283	6716705	United States	EEPROM Device having a Retrograde Program Junction Region And Process for Fabrication the Device	Issued	Lattice Semiconductor Corporation
10/164,484	6703305	United States	Semiconductor Device Having Metallized Interconnect Structure And Method Of Fabricaton	Issued	Lattice Semiconductor Corporation
10/187,236	6844757	United States	Converting Bits to Vectors In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/191,888	6650143	United States	FPGA Based Upon Transistor gate Oxide Breakdown	Issued	Lattice Semiconductor Corporation
10/194,771	7028281	United States	FPGA With Register-Intensive Architecture	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 486/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/200,645	6714066	United States	Integrated Programmable Continuous Time Filter with Programmable Capacitor Arrays	Issued	Lattice Semiconductor Corporation
10/207,292	6683477	United States	Wide input programmable logic system and method	Issued	Lattice Semiconductor Corporation
10/210,367	6938197	United States	CRC Calculation System And Method For A Packet Arriving On An N-Byte Wide Bus	Issued	Lattice Semiconductor Corporation
10/211,125	6545313	United States	EEPROM tunnel window for program injection via P+ contacted inversion	Issued	Lattice Semiconductor Corporation
10/219,046	6650142	United States	Enhanced CPLD Macrocell Module Having Selectable Bypass of Steering-based Resource Allocation and Methods of Use	Issued	Lattice Semiconductor Corporation
10/233,021	7043511	United States	Performing Conditional Operations In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/232,912	6841447	United States	EEPROM Device Having An Isolation -Bounded Tunnel Capacitor And Fabrication Process	Issued	Lattice Semiconductor Corporation
10/235,380	6725442	United States	Scalable and parallel processing methods and structures for testing configurable interconnect network in FPGA device	Issued	Lattice Semiconductor Corporation
10/236,829	6842372	United States	EEPROM Cell Having Floating Gate Transistor Within a Cell Well And a Process For Fabricating the Memory Cell	Issued	Lattice Semiconductor Corporation
10/236,114	6833602	United States	Device Having Electrically Isolated Low Voltage And High Voltage Regions And Process For Fabricating the Device	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/236,718	6649514	United States	EEPROM Device Having Improved Data Retention And Process for Fabricating The Device	Issued	Lattice Semiconductor Corporation
10/242,809	6738306	United States	Multiport SRAM Cell	Issued	Lattice Semiconductor Corporation
10/243,014	6917536	United States	Memory access Circuit and Method for reading and writing data with the same clock signal	Issued	Lattice Semiconductor Corporation
10/251,608	6700154	United States	EEPROM cell with trench coupling capacitor	Issued	Lattice Semiconductor Corporation
10/255,474	6907592	United States	Method of Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,875	6809551	United States	Method of Optimizing Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,499	6803787	United States	State Machine In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,656	6812738	United States	Vector Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/263,251	6748575	United States	Programming Programmable Logic Devices Using Hidden Switches	Issued	Lattice Semiconductor Corporation
10/263,507	6846714	United States	Voltage Limted EEPROM Device And Process For Fabricating the Device	Issued	Lattice Semiconductor Corporation
10/266,361	6639434	United States	Low voltage differential signaling systems and methods	Issued	Lattice Semiconductor Corporation
10/269,804	7111183	United States	Expansion method for complex power-sequencing applications	Issued	Lattice Semiconductor Corporation
10/269,450	6791394	United States	Power Supply Control Circuits	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 488/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/269,439	6762618	United States	Innovative verify scheme for two level GRP fuse in programmable bus switching family	Issued	Lattice Semiconductor Corporation
10/272,582	6901572	United States	Power Sequence Controller Programming Technique	Issued	Lattice Semiconductor Corporation
10/278,415	6639449	United States	Asynchronous glitch-free clock multiplexer	Issued	Lattice Semiconductor Corporation
10/282,524	7051261	United States	Turbo Encoder With Reduced Processing Delay	Issued	Lattice Semiconductor Corporation
10/283,765	6700823	United States	Programmable common mode termination for differential input/output circuits	Issued	Lattice Semiconductor Corporation
10/288,667	7000210	United States	Adaptive Adjustment Of Constraints During PLD Placement Processing	Issued	Lattice Semiconductor Corporation
10/288,668	6813754	United States	Placement Processing For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/300,190	6825733	United States	Low Jitter Integrated Phase Locked Loop With Broad Tuning Range	Issued	Lattice Semiconductor Corporation
10/302,439	6797568	United States	Flash Technology Transistors and Method For Forming Same	Issued	Lattice Semiconductor Corporation
10/308,420	6710641	United States	Low Voltage Bandgap Reference Circuit	Issued	Lattice Semiconductor Corporation
10/309,302	6650188	United States	Improved Coupling For LC-Based VCO	Issued	Lattice Semiconductor Corporation
10/334,642	6777979	United States	FIFO memory architecture	Issued	Lattice Semiconductor Corporation
10/338,619	6753696	United States	Programmable optimized-distribution logic allocator for	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 489/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			a high-density complex PLD		Corporation
10/365,083	7034596	United States	Adaptive input logic for phase adjustments	Issued	Lattice Semiconductor Corporation
10/368,023	6915323	United States	Macrocells Supporting A Carry Cascade	Issued	Lattice Semiconductor Corporation
10/366,956	6788101	United States	Programmable input buffer for differential and single-ended signals	Issued	Lattice Semiconductor Corporation
10/367,323	6812869	United States	Noise Reduction Techniques For Programmable I/O Circuits	Issued	Lattice Semiconductor Corporation
10/370,232	6861870	United States	Dynamic Cross point Switch With Shadow Memory Architecture	Issued	Lattice Semiconductor Corporation
10/377,320	6859066	United States	Bank based input/output buffers in field programmable gate arrays with multiple reference voltages	Issued	Lattice Semiconductor Corporation
10/387,814	7305047	United States	Automatic lane assignment for Receiver	Issued	Lattice Semiconductor Corporation
10/387,243	7339952	United States	Pointer Processing For Optical Communication Systems	Issued	Lattice Semiconductor Corporation
10/391,094	6870395	United States	PLDs With Integrated Standard Cell Logic Blocks	Issued	Lattice Semiconductor Corporation
10/392,751	RE39510	United States	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	Issued	Lattice Semiconductor Corporation
10/397,669	6967500	United States	Electronic Circuit With OnChip Programmable Terminations	Issued	Lattice Semiconductor Corporation
10/400,705	6873187	United States	Method and Apparatus for Controlling Signal Distribution In An Electronic	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 490/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Circuit		
10/406,050	7000212	United States	Hierarchical General Interconnect Architecture For High Density FPGA's	Issued	Lattice Semiconductor Corporation
10/409,543	6986004	United States	FIFO memory with programmable data port widths	Issued	Lattice Semiconductor Corporation
10/417,290	6879184	United States	Programmable logic device architecture based on arrays of LUT-based Boolean terms	Issued	Lattice Semiconductor Corporation
10/425,863	6903575	United States	Scalable device architecture for high-speed interfaces	Issued	Lattice Semiconductor Corporation
10/425,862	6894530	United States	Programmable And Fixed Logic Circuitry For High-Speed Interfaces	Issued	Lattice Semiconductor Corporation
10/428,889	6879182	United States	CPLD with multi-function blocks and distributed memory	Issued	Lattice Semiconductor Corporation
10/428,885	6861871	United States	Cascaded logic block architecture for complex programmable logic devices	Issued	Lattice Semiconductor Corporation
10/428,888	6864713	United States	Multi-Stage Interconnect Architecture For Complex Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/428,982	6922078	United States	Enhanced wide and deep logic capability for high density, high performance CPLDs	Issued	Lattice Semiconductor Corporation
10/439,602	6828823	United States	Non-volatilie and reconfigurable PLDs	Issued	Lattice Semiconductor Corporation
10/441,814	7039842	United States	Measuring Propagation Delays of Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/447,120	7301996	United States	skew cancellation for source synchronous clock and data signals	Issued	Lattice Semiconductor Corporation
10/447,451	7009433	United States	Digitally Controlled Delay Cells	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 491/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/457,630	7304863	United States	Integrated Circuit Including External Electronic Components With Low Insertion Loss	Issued	Lattice Semiconductor Corporation
10/459,091	6879598	United States	Flexible Media Access Control Architecture	Issued	Lattice Semiconductor Corporation
10/460,385	6856171	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
10/463,781	6861868	United States	High Speed Interface For A Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/464,083	6882555	United States	Bi-directional buffering for memory data lines	Issued	Lattice Semiconductor Corporation
10/600,042	6822477	United States	Integrated Circuit And Associated Design Method Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/610,253	6977408	United States	High-Performance Non-volatile Memory Device and Fabrication Process	Issued	Lattice Semiconductor Corporation
10/613,460	7132903	United States	Noise-shielding, switch-controlled load circuitry for oscillators and the like	Issued	Lattice Semiconductor Corporation
10/613,462	6952115	United States	Programmable I/O Interfaces For FPGAs And Other PLDs	Issued	Lattice Semiconductor Corporation
10/617,980	6958625	United States	PLD With Hardwired Microsequencer	Issued	Lattice Semiconductor Corporation
10/619,711	6903573	United States	Programmable Logic Device With Enhanced Wide Input Product Term Cascading	Issued	Lattice Semiconductor Corporation
10/620,286	6919736	United States	FPGA having partitionable embedded memory with configurable depth and width	Issued	Lattice Semiconductor Corporation
10/619,645	7098685	United States	Scalable Serializer-Deserializer Architecture and	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 492/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Programmable Interface		Corporation
10/620,147	7032203	United States	Algorithm to increase logic input width by cascading product terms	Issued	Lattice Semiconductor Corporation
10/624,965	6940309	United States	Programmable Logic Device With A Memory-Based Finite State Machine	Issued	Lattice Semiconductor Corporation
10/626,089	6737702	United States	Zero Power Memory Cell with Reduced Threshold Voltage	Issued	Lattice Semiconductor Corporation
10/628,656	6970047	United States	Programmable lock detector and corrector	Issued	Lattice Semiconductor Corporation
10/628,657	6924659	United States	Programmable Signal Termination for FPGAs and the Like	Issued	Lattice Semiconductor Corporation
10/629,223	7019577	United States	Clock Generator	Issued	Lattice Semiconductor Corporation
10/629,512	6903574	United States	Memory Access Via Serial Memory Interface	Issued	Lattice Semiconductor Corporation
10/629,221	6885227	United States	Clock Generator With Skew Control	Issued	Lattice Semiconductor Corporation
10/640,804	6877667	United States	Integrated Circuit And Associated Design Method With Antenna Error Control Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/640,828	6838904	United States	Enhanced CPLD Macrocell Module Having Selectable Bypass of Steering-Based Resource Allocation	Issued	Lattice Semiconductor Corporation
10/641,260	6940779	United States	Programmable broadcasting initialization of embedded memory blocks on FPGA	Issued	Lattice Semiconductor Corporation
10/642,370	6924664	United States	FPGA	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/655,686	6842037	United States	Shared Transmission Line Communication System and Method	Issued	Lattice Semiconductor Corporation
10/660,814	7038490	United States	Delay matched ASIC conversion of a PLD	Issued	Lattice Semiconductor Corporation
10/665,920	6970022	United States	Controlled hysteresis comparator with rail-to-rail input	Issued	Lattice Semiconductor Corporation
10/671,378	6943583	United States	Programmable I/O structure for FPGAs and the like having reduced pad capacitance	Issued	Lattice Semiconductor Corporation
10/671,363	6943582	United States	Programmable I/O structure for FPGAs and the Like Having Shared Circuitry	Issued	Lattice Semiconductor Corporation
10/671,756	6909663	United States	Multiport Memory With Twisted Bitlines	Issued	Lattice Semiconductor Corporation
10/676,536	7269771	United States	Semiconductor Device Adapted For Forming Multiple Scan Chains	Issued	Lattice Semiconductor Corporation
10/687,468	6809674	United States	Analog-to-digital converters	Issued	Lattice Semiconductor Corporation
10/699,321	7067883	United States	Lateral High-Voltage Junction Device	Issued	Lattice Semiconductor Corporation
10/701,005	7091763	United States	Clock generation	Issued	Lattice Semiconductor Corporation
10/704,025	7088134	United States	PLD With Flexible Memory Allocation And Routing	Issued	Lattice Semiconductor Corporation
10/726,972	7100058	United States	Programmable Power Management System And Method	Issued	Lattice Semiconductor Corporation
10/728,685	7187157	United States	Power supply remote voltage sensing	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 494/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/737,514	6981381	United States	Linear Thermoelectric Device Driver	Issued	Lattice Semiconductor Corporation
10/744,353	7132864	United States	Method for configuring multiple-output phase-locked loop frequency synthesizer	Issued	Lattice Semiconductor Corporation
10/769,174	7024646	United States	Electrostatic Discharge Simulation	Issued	Lattice Semiconductor Corporation
10/768,643	7019584	United States	Output Stages For High Current Low Noise Bandgap Reference Circuit Implementations	Issued	Lattice Semiconductor Corporation
10/782,564	6972986	United States	Combination FPGA	Issued	Lattice Semiconductor Corporation
10/783,886	7081771	United States	Upgradeable And Reconfigurable Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/791,073	7191388	United States	Fast diagonal interleaved parity (DIP) calculator	Issued	Lattice Semiconductor Corporation
10/794,079	7257727	United States	Timer Systems and Methods	Issued	Lattice Semiconductor Corporation
10/794,524	7017063	United States	systems and methods for controlling voltage regulator module power supplies	Issued	Lattice Semiconductor Corporation
10/794,498	7028201	United States	Powering up a device having digital and analog circuitry	Issued	Lattice Semiconductor Corporation
10/797,759	7068556	United States	Sense Amplifier Systems and Methods	Issued	Lattice Semiconductor Corporation
10/809,180	7234030	United States	Table based scheduler for FIFOs and the like	Issued	Lattice Semiconductor Corporation
10/809,658	7095247	United States	Configuring FPGAs and the like using one or more serial memory devices	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 495/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/815,403	7167032	United States	Self-adjusting schmitt trigger	Issued	Lattice Semiconductor Corporation
10/817,215	7081781	United States	Charge pump for a low-voltage wide-tuning range phase-locked loop	Issued	Lattice Semiconductor Corporation
10/829,865	6998896	United States	Dynamic gain adjustment systems and method for metastability resistance	Issued	Lattice Semiconductor Corporation
10/834,528	6998906	United States	Low pass filter systems and methods	Issued	Lattice Semiconductor Corporation
10/837,086	7307319	United States	High Voltage Protection Device And Process	Issued	Lattice Semiconductor Corporation
10/842,345	7002418	United States	Control Signal Generation ...	Issued	Lattice Semiconductor Corporation
10/841,987	7224213	United States	switched-capacitor ripple-smoothing filter	Issued	Lattice Semiconductor Corporation
10/843,708	7061269	United States	IO buffer architecture for programmable devices	Issued	Lattice Semiconductor Corporation
10/856,100	7196551	United States	Current Mode Logic Buffer	Issued	Lattice Semiconductor Corporation
10/857,667	7064973	United States	Combination FPGA	Issued	Lattice Semiconductor Corporation
10/885,419	7116585	United States	Memory Systems And Methods	Issued	Lattice Semiconductor Corporation
10/910,091	7215591	United States	Byte enable logic for memory	Issued	Lattice Semiconductor Corporation
10/912,943	7471752	United States	Data Transmission Synchronization	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/928,563	7078286	United States	Process for fabricating a semiconductor device having electrically isolated low voltage and high voltage regions	Issued	Lattice Semiconductor Corporation
10/929,199	7484144	United States	Testing embedded memory in an integrated circuit	Issued	Lattice Semiconductor Corporation
10/944,978	7135886	United States	FPGA Using Both Volatile and NonVolatile Memory Cell Properties	Issued	Lattice Semiconductor Corporation
10/974,453	7307912	United States	Variable data width memory systems and methods	Issued	Lattice Semiconductor Corporation
10/973,750	7149129	United States	memory output data systems and methods with feedback	Issued	Lattice Semiconductor Corporation
10/974,107	7164290	United States	FPGA Logic Unit	Issued	Lattice Semiconductor Corporation
10/974,305	7129749	United States	PLD Having A Configurable DRAM With Transparent Refresh	Issued	Lattice Semiconductor Corporation
10/978,899	7376872	United States	Testing embedded memory in integrated circuits such as progammable logic circuits	Issued	Lattice Semiconductor Corporation
10/996,283	7161862	United States	Low power asynchronous sense amp	Issued	Lattice Semiconductor Corporation
11/007,954	7230810	United States	Dynamic over-voltage protection scheme for integrated circuit devices	Issued	Lattice Semiconductor Corporation
11/012,550	7215149	United States	Interface circuitry for electrical systems	Issued	Lattice Semiconductor Corporation
11/012,548	7215148	United States	Programmable current LVDS output buffer	Issued	Lattice Semiconductor Corporation
11/015,265	7177221	United States	Method of initializing configurable multi-port	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			embedded memory blocks in an FPGA		Corporation
11/016,665	7187203	United States	Cascadable memory	Issued	Lattice Semiconductor Corporation
11/015,369	7177207	United States	Sense amplifier timing	Issued	Lattice Semiconductor Corporation
11/036,630	7257750	United States	Self-verification of configuration memory in PLDs	Issued	Lattice Semiconductor Corporation
11/036,738	7242053	United States	EEPROM Device with voltage-limiting charge pump circuit	Issued	Lattice Semiconductor Corporation
11/040,772	7208975	United States	Serdes with programmable I/O architecture	Issued	Lattice Semiconductor Corporation
11/041,319	7183798	United States	Synchronous memory	Issued	Lattice Semiconductor Corporation
11/044,089	7109754	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
11/044,149	7109756	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
11/044,508	7034599	United States	Clock Generator With Skew Control	Issued	Lattice Semiconductor Corporation
11/054,011	7221607	United States	Mult-port memory systems and methods for bit line coupling	Issued	Lattice Semiconductor Corporation
11/055,280	6975137	United States	PLDs With Integrated Standard Cell Logic Blocks	Issued	Lattice Semiconductor Corporation
11/054,750	7382293	United States	Data Decompression	Issued	Lattice Semiconductor Corporation
11/054,855	7589648	United States	Data Decompression	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/064,477	7532646	United States	Distributed multiple channel alignment scheme	Issued	Lattice Semiconductor Corporation
11/071,356	7245154	United States	Differential Input Receiver with Programmable Failsafe	Issued	Lattice Semiconductor Corporation
11/070,926	7057397	United States	Output Impedance Measurement Techniques	Issued	Lattice Semiconductor Corporation
11/083,625	7376204	United States	Detection of Unknown symbol rate in a digitally modulated signal	Issued	Lattice Semiconductor Corporation
11/098,713	7265578	United States	In-System Programming Of a Non-Compliant Device Using Multiple Interfaces Of A PLD	Issued	Lattice Semiconductor Corporation
11/100,718	7397274	United States	In-System Programming Of a Non-Compliant Device Using Multiple Interfaces Of A PLD	Issued	Lattice Semiconductor Corporation
11/108,927	7193436	United States	Fast Processing Path Using FPGA Logic Units	Issued	Lattice Semiconductor Corporation
11/109,301	7630464	United States	Analog-to-digital systems and methods	Issued	Lattice Semiconductor Corporation
11/109,966	6977521	United States	FPGA	Issued	Lattice Semiconductor Corporation
11/121,326	7400171	United States	Electronic Switch Having Extended Voltage Range	Issued	Lattice Semiconductor Corporation
11/134,152	7009423	United States	Programmable I/O Interfaces For FPGAs And Other PLDs	Issued	Lattice Semiconductor Corporation
11/157,345	7685483	United States	Design-For-Test features for a memory in an FPGA	Issued	Lattice Semiconductor Corporation
11/157,349	7378879	United States	Decoding systems and methods	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 499/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/165,709	7256613	United States	Programmable Interconnect Architecture for PLDs	Issued	Lattice Semiconductor Corporation
11/165,853	7342838	United States	PLD With A Double Data Rate SDRAM Interface	Issued	Lattice Semiconductor Corporation
11/185,242	7519139	United States	Signal monitoring systems and methods	Issued	Lattice Semiconductor Corporation
11/187,179	7342846	United States	address decoding systems and methods	Issued	Lattice Semiconductor Corporation
11/187,114	7253674	United States	Fine output clock phase alignment circuitry	Issued	Lattice Semiconductor Corporation
11/189,067	7505752	United States	Receiver used for differential signaling and reference voltage signaling with programmable common mode	Issued	Lattice Semiconductor Corporation
11/194,871	7414913	United States	Bitline twisting scheme for a multiport memory	Issued	Lattice Semiconductor Corporation
11/194,356	7262630	United States	Dynamic programmable termination for parallel and differential schemes	Issued	Lattice Semiconductor Corporation
11/199,287	7599457	United States	clock-and-data-recovery system having a multi-phase clock generator for one or more channel circuits	Issued	Lattice Semiconductor Corporation
11/200,983	7295035	United States	Programmable Logic Device With Enhanced Logic Block Architecture	Issued	Lattice Semiconductor Corporation
11/200,941	7411419	United States	I/O Systems and Methods	Issued	Lattice Semiconductor Corporation
11/202,149	7606851	United States	Correlator having user-defined processing	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/201,620	7187586	United States	Flash memory erase verification systems and methods	Issued	Lattice Semiconductor Corporation
11/206,282	RE40311	United States	Zero Power Programmable Memory Cell	Issued	Lattice Semiconductor Corporation
11/226,695	7301182	United States	Circuit layout for improved performance while preserving or improving density	Issued	Lattice Semiconductor Corporation
11/230,087	7167405	United States	Data transfer verification systems and methods	Issued	Lattice Semiconductor Corporation
11/235,616	7376037	United States	PLD with power-saving architecture	Issued	Lattice Semiconductor Corporation
11/236,967	7405446	United States	Electrostatic Protection Systems and Methods	Issued	Lattice Semiconductor Corporation
11/243,255	7088132	United States	Configuring FPGAs and the like using one or more serial memory devices	Issued	Lattice Semiconductor Corporation
11/251,682	7196963	United States	Address isolation for user-defined configuration memory in programmable devices	Issued	Lattice Semiconductor Corporation
11/252,094	7263024	United States	Clock reset address decoder for block memory	Issued	Lattice Semiconductor Corporation
11/252,126	7061275	United States	FPGA	Issued	Lattice Semiconductor Corporation
11/257,137	7685215	United States	Fast-carry arithmetic circuit using a multi-input LUT	Issued	Lattice Semiconductor Corporation
11/257,641	7317343	United States	PULSE-GENERATION CIRCUIT HAVING PULSE GENERATORS AND SET-RESET LATCHES	Issued	Lattice Semiconductor Corporation
11/260,097	7212051	United States	Control signal generation for a low jitter switched-capacitor frequency synthesizer	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 501/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/281,651	7495495	United States	Digital I/O Timing Control	Issued	Lattice Semiconductor Corporation
11/287,720	7327159	United States	Interface Block Architectures	Issued	Lattice Semiconductor Corporation
11/290,205	7242634	United States	Pseudo-dynamic word-line driver	Issued	Lattice Semiconductor Corporation
11/293,941	7538574	United States	Transparent Field Reconfiguration for PLDs	Issued	Lattice Semiconductor Corporation
11/302,097	7620839	United States	Jitter Tolerant Delay-Locked Loop Circuit	Issued	Lattice Semiconductor Corporation
11/300,886	7495467	United States	Temperature independent, linear on-chip termination resistance	Issued	Lattice Semiconductor Corporation
11/332,986	7382169	United States	Systems and Methods for Reducing Static Phase Error	Issued	Lattice Semiconductor Corporation
11/335,890	7439783	United States	Phase-Locked Loop Systems And Methods	Issued	Lattice Semiconductor Corporation
11/345,713	7547995	United States	dynamic over voltage protection scheme for interface circuitry	Issued	Lattice Semiconductor Corporation
11/346,817	7554357	United States	Efficient Configuration of Daisy-Chained Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
11/350,436	7375549	United States	Reconfiguration of PLDs	Issued	Lattice Semiconductor Corporation
11/356,805	7277348	United States	Memory Cell Comprising And OTP NV Memory Unit And SRAM Unit	Issued	Lattice Semiconductor Corporation
11/360,337	7355441	United States	PLD with distributed memory and non-volatile memory	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 502/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/361,584	7596744	United States	Auto recovery from volatile soft error upsets (SEUs)	Issued	Lattice Semiconductor Corporation
11/362,289	7759926	United States	dynamic phase offset measurement	Issued	Lattice Semiconductor Corporation
11/361,643	7446573	United States	Comparator Systems And Methods	Issued	Lattice Semiconductor Corporation
11/398,437	7459931	United States	PLDs with transparent field reconfiguration	Issued	Lattice Semiconductor Corporation
11/397,985	7554358	United States	PLDs with user non-volatile memory	Issued	Lattice Semiconductor Corporation
11/416,881	7623378	United States	Selective programming of non-volatile memory facilitated by security fuses	Issued	Lattice Semiconductor Corporation
11/435,956	7102934	United States	Sense Amplifier Systems and Methods	Issued	Lattice Semiconductor Corporation
11/442,186	7411417	United States	Selective loading of configuration data into configuration memory cells	Issued	Lattice Semiconductor Corporation
11/446,548	7378873	United States	PLD providing a serial peripheral interface	Issued	Lattice Semiconductor Corporation
11/445,620	7378872	United States	PLD architecture with multiple slice types	Issued	Lattice Semiconductor Corporation
11/446,542	7385417	United States	Dual slice architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/446,351	7397276	United States	Logic block control architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/446,308	7546498	United States	PLDs with custom identification systems and methods	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 503/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/446,309	7495970	United States	Flexible memory architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/447,591	7631223	United States	PLD methods and systems for providing multi-boot configuration data support	Issued	Lattice Semiconductor Corporation
11/452,714	7463060	United States	PLD and method of testing	Issued	Lattice Semiconductor Corporation
11/455,315	7215139	United States	Upgradeable And Reconfigurable Programmable Logic Device	Issued	Lattice Semiconductor Corporation
11/425,273	7702100	United States	Key generation for advanced encryption standard (AES) decryption and the like	Issued	Lattice Semiconductor Corporation
11/425,881	7657773	United States	Clock distribution chip for generating both zero-delay and non-zero-delay clock signals	Issued	Lattice Semiconductor Corporation
11/477,759	7348914	United States	Methods and systems to align output signals of an analog-to-digital converter	Issued	Lattice Semiconductor Corporation
11/487,647	7636259	United States	Flash memory array with independently erasable sectors	Issued	Lattice Semiconductor Corporation
11/487,751	7512015	United States	Negative voltage blocking for embedded memories	Issued	Lattice Semiconductor Corporation
11/492,687	7466190	United States	Charge pump with four-well transistors	Issued	Lattice Semiconductor Corporation
11/494,862	7521969	United States	Switch sequencing circuit systems and methods	Issued	Lattice Semiconductor Corporation
11/461,222	7411432	United States	Integrated circuits and complementary CMOS circuits for frequency dividers	Issued	Lattice Semiconductor Corporation
11/498,645	7675313	United States	Methods and systems for storing a security key using programmable fuses	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 504/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/498,646	7605606	United States	Area efficient routing architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/530,620	7456672	United States	Clock systems and methods	Issued	Lattice Semiconductor Corporation
11/533,188	7511641	United States	Efficient bitstream compression	Issued	Lattice Semiconductor Corporation
11/551,459	7831754	United States	Multiple Communication Channel Configuration Systems And Methods	Issued	Lattice Semiconductor Corporation
11/556,528	7663401	United States	Multiplexer initialization systems and methods	Issued	Lattice Semiconductor Corporation
11/593,274	7535258	United States	Programmable Voltage LVDS Output Buffer	Issued	Lattice Semiconductor Corporation
11/557,808	7725803	United States	PLD programming verification systems and methods	Issued	Lattice Semiconductor Corporation
11/638,156	7429875	United States	Low Static Current Drain Logic Circuit	Issued	Lattice Semiconductor Corporation
11/643,288	7443192	United States	Output buffer with digital slew control	Issued	Lattice Semiconductor Corporation
11/624,021	7623391	United States	Data transfer verification systems and methods	Issued	Lattice Semiconductor Corporation
11/671,948	7576563	United States	Flexible High Fan-out Signal Routing Systems and Methods	Issued	Lattice Semiconductor Corporation
11/675,246	7313025	United States	Flash memory erase verification systems and methods	Issued	Lattice Semiconductor Corporation
11/676,071	7430706	United States	Fast diagonal interleaved parity (DIP) calculator	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 505/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/680,526	7598765	United States	Redundancy for Configuration RAM	Issued	Lattice Semiconductor Corporation
11/691,003	7536615	United States	Logic analyzer systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/691,040	7743296	United States	Logic analyzer systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/737,702	7509598	United States	Clock Boosting Systems and Methods	Issued	Lattice Semiconductor Corporation
11/750,790	7401280	United States	Self-verification of configuration memory in PLDs	Issued	Lattice Semiconductor Corporation
11/750,616	7632011	United States	Integrated Circuit Temperature Sensors Systems and Methods	Issued	Lattice Semiconductor Corporation
11/760,411	8065574	United States	Real Soft Error Detect Scheme for Testing	Issued	Lattice Semiconductor Corporation
11/761,221	7570078	United States	PLD Providing A Serial Peripheral Interfaces	Issued	Lattice Semiconductor Corporation
11/778,457	7573770	United States	Distributed front-end FIFO for source-synchronized interfaces with non-continuous clocks	Issued	Lattice Semiconductor Corporation
11/779,246	7446679	United States	FPGA data compression using combined RLE BE, LZ, Row LZ and BE ROW encoding	Issued	Lattice Semiconductor Corporation
11/863,016	7681160	United States	Weight based look up table collapsing for programmable logic devices	Issued	Lattice Semiconductor Corporation
11/865,556	7539076	United States	Variable data width memory systems and methods	Issued	Lattice Semiconductor Corporation
11/869,019	7616029	United States	Hysteresis-based processing for applications such as signal bias monitors	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 506/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/872,950	7586344	United States	Dynamic delay or advance adjustment of oscillating signal phase	Issued	Lattice Semiconductor Corporation
11/875,748	7757198	United States	Scan chain systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/877,434	7411414	United States	Single-Ended Output Driver Buffer	Issued	Lattice Semiconductor Corporation
11/924,088	8132040	United States	Channel-to-channel deskew systems and methods	Issued	Lattice Semiconductor Corporation
11/934,711	7573291	United States	Programmable Logic Device With Enhanced Logic Block Architecture	Issued	Lattice Semiconductor Corporation
11/937,328	7788620	United States	An IO placement systems and methods to reduce SSO noise	Issued	Lattice Semiconductor Corporation
11/937,300	7895555	United States	Simultaneous Switching Output Noise Estimation and Reduction Systems and Methods	Issued	Lattice Semiconductor Corporation
11/939,787	7863931	United States	Flexible Delay Cell Architecture	Issued	Lattice Semiconductor Corporation
11/941,031	7902865	United States	Compression and decompression of configuration data using repeated data frames	Issued	Lattice Semiconductor Corporation
11/941,006	7535253	United States	Method of Retaining Register Data during Field Update of PLD	Issued	Lattice Semiconductor Corporation
11/947,662	7788623	United States	Composite wire indexing for PLDs	Issued	Lattice Semiconductor Corporation
11/949,130	7586325	United States	IC having independent voltage and process/temperature control	Issued	Lattice Semiconductor Corporation
12/001,600	7728625	United States	Serial interface for PLDs	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 507/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/957,598	7605609	United States	A programmable level shifter optimized for high performance and low power.	Issued	Lattice Semiconductor Corporation
11/959,329	7630259	United States	PLD with built in self test	Issued	Lattice Semiconductor Corporation
11/970,212	7646643	United States	Process charging monitor for nonvolatile memory	Issued	Lattice Semiconductor Corporation
12/019,526	7787326	United States	PLD With Mult-Rate SDRAM Interface	Issued	Lattice Semiconductor Corporation
12/021,202	8069329	United States	Dynamic Multiple Pattern Configuration Scheme For Volatile FPGAs	Issued	Lattice Semiconductor Corporation
12/044,842	7652500	United States	Reconfiguration of PLDs	Issued	Lattice Semiconductor Corporation
12/055,170	7890913	United States	Wire Mapping For PLDs	Issued	Lattice Semiconductor Corporation
12/060,776	7459935	United States	PLD With Distributed Memory	Issued	Lattice Semiconductor Corporation
12/061,885	7831856	United States	Detection of Timing Errors in Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/099,933	7661878	United States	On-Chip Temperature Sensor For An Integrated Circuit	Issued	Lattice Semiconductor Corporation
12/100,859	7558143	United States	Programmable Logic Device With Power-Saving Architecture	Issued	Lattice Semiconductor Corporation
12/105,146	7557606	United States	Synchronization Of Data Signals And Clock Signals For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/105,959	7696784	United States	PLD With Multiple Slice	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 508/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Types		Corporation
12/107,883	7560953	United States	Power Management Systems And Methods for PLDs	Issued	Lattice Semiconductor Corporation
12/122,489	7897448	United States	Formation Of High Voltage Transistor With High Breakdown Voltage	Issued	Lattice Semiconductor Corporation
12/146,042	8463832	United States	Digital Signal Processing Block Architecture For PLD	Issued	Lattice Semiconductor Corporation
12/164,265	7592834	United States	Logic Block Control Architectures For PLDs	Issued	Lattice Semiconductor Corporation
12/182,940	8261160	United States	Serial data recovery out of 8 samples with FPGAs	Issued	Lattice Semiconductor Corporation
12/186,027	7579865	United States	Selective Loading Of Configuration Data Into Configuration Memory Cells	Issued	Lattice Semiconductor Corporation
12/188,120	7605602	United States	Low-Power Output Driver Buffer Circuit	Issued	Lattice Semiconductor Corporation
12/238,959	7911229	United States	Programmable Signal Routing Systems	Issued	Lattice Semiconductor Corporation
12/273,868	7663419	United States	Clock Systems And Methods	Issued	Lattice Semiconductor Corporation
12/277,217	8112731	United States	Congestion-driven placement based on region interconnection for FPGA	Issued	Lattice Semiconductor Corporation
12/323,974	7992120	United States	congestion estimation based on pass probability net estimation process	Issued	Lattice Semiconductor Corporation
12/327,128	7656193	United States	Programmable Logic Device And Method Of Testing	Issued	Lattice Semiconductor Corporation
12/337,502	8856718	United States	Precise Congestion Estimation for FPGA Router	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 509/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
12/341,929	8181139	United States	Multi-Priority Placement	Issued	Lattice Semiconductor Corporation
12/370,039	7714608	United States	Temperature-Independent, Linear On-Chip Termination Resistance	Issued	Lattice Semiconductor Corporation
12/389,149	7957208	United States	Flexible memory architectures for PLDs	Issued	Lattice Semiconductor Corporation
12/402,751	7844243	United States	Receiver used for differential signaling and reference voltage signaling with programmable common mode	Issued	Lattice Semiconductor Corporation
12/406,772	8069431	United States	An alternative method for pin swapping in FPGA routing	Issued	Lattice Semiconductor Corporation
12/408,047	8086986	United States	Clock Boosting Systems And Methods	Issued	Lattice Semiconductor Corporation
12/409,757	7675321	United States	Dual-Slice Architectures For PLDs	Issued	Lattice Semiconductor Corporation
12/413,787	7808405	United States	Efficient Bitstream Compression	Issued	Lattice Semiconductor Corporation
12/430,848	7741865	United States	Soft Error Upset Hardened Integrated Circuit Systems And Methods	Issued	Lattice Semiconductor Corporation
12/464,822	7876125	United States	Method of Retaining Register Data during Field Update of PLD	Issued	Lattice Semiconductor Corporation
12/465,444	7868654	United States	Economical way to improve volatile FPGA boot up data throughput by utilizing one or more SPI boot PROMs w/o sacrificing additional FPGA pins	Issued	Lattice Semiconductor Corporation
12/467,800	7737723	United States	Transparent Field Reconfiguration for PLDs	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 510/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
12/476,155	8044682	United States	FPGA Having Low Power, Fast Carry Chain	Issued	Lattice Semiconductor Corporation
12/480,565	7702977	United States	PLDs with custom identification systems and methods	Issued	Lattice Semiconductor Corporation
12/494,822	8165164	United States	Circuit For In-System Reconfigurable Mapping Of IQ Data Into A CPRI Basic Frame	Issued	Lattice Semiconductor Corporation
12/502,141	7724029	United States	Power Management For Integrated Circuits Such As Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/511,388	7768300	United States	PLD Providing A Serial Peripheral Interfaces	Issued	Lattice Semiconductor Corporation
12/512,944	8255733	United States	Method of selecting precise delay or skew shifts	Issued	Lattice Semiconductor Corporation
12/512,961	7969248	United States	VCO digital center frequency coarse tune algorithm	Issued	Lattice Semiconductor Corporation
12/538,810	7808855	United States	Distributed front-end FIFO for source-synchronized interfaces with non-continuous clocks	Issued	Lattice Semiconductor Corporation
12/561,140	8010871	United States	Auto recovery from volatile soft error upsets (SEUs)	Issued	Lattice Semiconductor Corporation
12/564,781	7746107	United States	Redundancy for Configuration RAM	Issued	Lattice Semiconductor Corporation
12/578,470	8122277	United States	Clock distribution chip	Issued	Lattice Semiconductor Corporation
12/578,492	8112656	United States	Clock distribution chip	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 511/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/607,868	7989911	United States	STI with trench liner of increased thickness	Issued	Lattice Semiconductor Corporation
12/607,333	7985656	United States	STI with trench liner of increased thickness	Issued	Lattice Semiconductor Corporation
12/611,262	8059470	United States	Flash memory array with independently erasable sectors	Issued	Lattice Semiconductor Corporation
12/626,289	7944765	United States	PLD with built in self test	Issued	Lattice Semiconductor Corporation
12/630,163	8060784	United States	PLD And Methods For Providing Multi-Boot Configuration Data Support	Issued	Lattice Semiconductor Corporation
12/637,884	8200179	United States	Combined Variable Gain Amplifier And Linear Equalizer With Independent Gain And Frequency Control	Issued	Lattice Semiconductor Corporation
12/698,283	8040152	United States	IO Ring Configuration Scheme with sharing of BC7 register	Issued	Lattice Semiconductor Corporation
12/706,227	7924054	United States	Latency measurement circuit for wireless communications applications	Issued	Lattice Semiconductor Corporation
12/709,685	7834652	United States	Methods and systems for storing a security key using programmable fuses	Issued	Lattice Semiconductor Corporation
12/729,952	8040159	United States	High Speed Comparator with Data Dependent Jitter Mitigation	Issued	Lattice Semiconductor Corporation
12/752,455	8384427	United States	Serial Peripheral Interface Daisy Chaining using a Flow-Through Option	Issued	Lattice Semiconductor Corporation
12/757,087	8664774	United States	A Method for Arranging IC Bondwires for the Reduction of Crosstalk	Issued	Lattice Semiconductor Corporation
12/786,359	8108754	United States	PLD programming verification systems and methods	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 512/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/813,540	8164499	United States	Shared-Array Multiple-Output Digital to Analog Converter	Issued	Lattice Semiconductor Corporation
12/813,573	8441292	United States	Method of delaying data from clock in 1UI steps	Issued	Lattice Semiconductor Corporation
12/818,544	7868646	United States	Soft Error Upset Hardened Integrated Circuit Systems And Methods	Issued	Lattice Semiconductor Corporation
12/871,764	8286116	United States	Composite Wire Indexing For PLDs	Issued	Lattice Semiconductor Corporation
12/977,011	8522126	United States	Method Of Blocking PLC Distributed SRAM Readback In User Mode	Issued	Lattice Semiconductor Corporation
12/976,412	8351287	United States	Bitline Floating Circuit For Power Reduction On SRAM Array	Issued	Lattice Semiconductor Corporation
12/976,520	8477549	United States	Strobed And Latched Readback Of SRAM Bits In A FPGA	Issued	Lattice Semiconductor Corporation
12/987,393	8274412	United States	Low Power SerDes With Built- In Word Alignment For Odd And Even Gearing Ratios	Issued	Lattice Semiconductor Corporation
13/006,622	8384428	United States	Programmable IO Pad - embedded function block	Issued	Lattice Semiconductor Corporation
13/007,804	8248136	United States	Low Power And Glitch-less Delay Element For High Speed Receiver Interface	Issued	Lattice Semiconductor Corporation
13/007,688	8324934	United States	Programmable Ratio Input Buffer	Issued	Lattice Semiconductor Corporation
13/026,555	8104009	United States	Wire Mapping For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
13/034,174	8058898	United States	Compression and Decompression Of Configuration Data Using	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 513/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Repeated Data Frames		
13/038,259	8368424	United States	Wakeup from sleep mode using slave I2C port or slave SPI port with powered down core logic	Issued	Lattice Semiconductor Corporation
13/038,270	8816718	United States	Slow Respond Mode Protocol For Synchronous Read	Issued	Lattice Semiconductor Corporation
13/037,703	8654600	United States	Current Sense Amplifier With Low Voltage Operation	Issued	Lattice Semiconductor Corporation
13/052,142	8553463	United States	Positive-To-Negative Voltage Discharge Circuit	Issued	Lattice Semiconductor Corporation
13/076,300	8319521	United States	Safe programming of key information into NV memory	Issued	Lattice Semiconductor Corporation
13/079,578	8314634	United States	Power Saving Standby Mode With Glitch-Less Output Controls	Issued	Lattice Semiconductor Corporation
13/079,595	8531222	United States	PLL Switchable Feedback Loops Among Internal And External Feedback Paths	Issued	Lattice Semiconductor Corporation
13/083,889	8138790	United States	Latency measurement circuit for wireless communications applications	Issued	Lattice Semiconductor Corporation
13/154,885	8441284	United States	Flexible Way To Incrementally Update Multi-Bit Data Registers	Issued	Lattice Semiconductor Corporation
13/155,547	8547075	United States	Filter And Stability Capacitor Reuse For On-Chip Dual Output Voltage Regulators	Issued	Lattice Semiconductor Corporation
13/164,108	8555217	United States	Cross-Probing Technology Between Software Plug-In Modules	Issued	Lattice Semiconductor Corporation
13/178,599	8539409	United States	Multiple silicon products from a common base set of masks	Issued	Lattice Semiconductor Corporation
13/178,536	8495264	United States	Packet And Control Symbol	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 514/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Alignment Circuit For SRIO		Corporation
13/193,984	8314632	United States	Placing ICs Into Ultra-Low Voltage Mode For Standby Purposes	Issued	Lattice Semiconductor Corporation
13/212,121	8451679	United States	Bit-Line Clamping Circuit To Improve Write Performance Of Dual-Port SRAM	Issued	Lattice Semiconductor Corporation
13/275,102	8169237	United States	High Speed Comparator with Data Dependent Jitter Mitigation	Issued	Lattice Semiconductor Corporation
13/299,507	8370691	United States	Testing of Soft Error Detection Logic For PLDs	Issued	Lattice Semiconductor Corporation
13/452,060	8823561	United States	In-System Reconfigurable Circuit For Mapping Data Words Of Different Lengths	Issued	Lattice Semiconductor Corporation
13/585,142	8461894	United States	Low Power And Glitch-less Delay Element For High Speed Receiver Interface	Issued	Lattice Semiconductor Corporation
13/616,173	8912933	United States	Low Power SerDes With Built- In Word Alignment For Odd And Even Gearing Ratios	Issued	Lattice Semiconductor Corporation
13/653,827	8710898	United States	Bandgap Reference Circuit Design With Triple-Trim Methodology For Mass Production	Issued	Lattice Semiconductor Corporation
13/680,947	8643398	United States	Placing ICs Into Low Voltage Mode For Standby Purposes	Issued	Lattice Semiconductor Corporation
13/685,385	8643168	United States	Input Capacitance Compensation In Package	Issued	Lattice Semiconductor Corporation
13/721,867	8686773	United States	In-System Margin Measurement Circuit	Issued	Lattice Semiconductor Corporation
13/738,265	8797064	United States	Low power, optimized H-bridge and CML driver	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 515/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
13/764,221	RE45200	United States	Programmable Signal Routing Systems Having Low Static Leakage	Issued	Lattice Semiconductor Corporation
13/857,919	8786482	United States	Analog-To-Digital-Converter	Issued	Lattice Semiconductor Corporation
13/892,948	8648636	United States	Method of Delaying Data from Clock in 1UI steps	Issued	Lattice Semiconductor Corporation
14/040,955	8829944	United States	Dynamic Power Supply Switching For Clock Signals	Issued	Lattice Semiconductor Corporation
13/155,261		United States	JTAG Based Parallel Measuring And Trimming for Time Based Parameters	Pending	Lattice Semiconductor Corporation
13/412,408		United States	Double Rate Throughput Processing Booster For DSP Slices	Pending	Lattice Semiconductor Corporation
13/466,463		United States	Early Match FIFO	Pending	Lattice Semiconductor Corporation
13/681,782		United States	Multi-channel transmitter synchronization circuitry	Pending	Lattice Semiconductor Corporation
13/777,243		United States	RAM Data Path Sense Leakage Abatement Circuit	Pending	Lattice Semiconductor Corporation
13/858,422		United States	Method To Enable And Disable Scan Test Mode Reliably Through JTAG Port With Maximum Scan Coverage	Pending	Lattice Semiconductor Corporation
13/868,738		United States	Loss of signal detection in high-speed serial link	Pending	Lattice Semiconductor Corporation
13/901,853		United States	Dual-Port SRAM With Bit Line Clamping	Pending	Lattice Semiconductor Corporation
13/904,861		United States	Bring up sequence for configurable PCIe IP in an	Pending	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 516/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			FPGA		Corporation
13/947,553		United States	Method For Hot Swapping Or Hot Plugging With Stable Supply-Side Reference Over Wide Voltage Range	Pending	Lattice Semiconductor Corporation
14/021,513		United States	Phase Locked Loop Circuit With Selectable Feedback Paths	Pending	Lattice Semiconductor Corporation
14/043,920		United States	Robust Serialized State-machine Interface Architecture Optimized for Implementation in Programmable Devices	Pending	Lattice Semiconductor Corporation
14/053,026		United States	ASB SW modeling methodology	Pending	Lattice Semiconductor Corporation
14/070,975		United States	Method to enable system board pin escape for tight ball pitch packages	Pending	Lattice Semiconductor Corporation
14/095,310		United States	A Novel ESD Implementation for 40nm FPGA	Pending	Lattice Semiconductor Corporation
14/136,482		United States	Automatic Quadrant Clock Assignment For Programmable Logic Devices	Pending	Lattice Semiconductor Corporation
14/137,443		United States	Using Critical Groups in FPGA Routing	Pending	Lattice Semiconductor Corporation
14/147,796		United States	A Hot Socket Implementation for General Purpose IO for 40nm FPGA	Pending	Lattice Semiconductor Corporation
14/172,678		United States	All Mosfet Circuit for Generating Accurate Collector Currents	Pending	Lattice Semiconductor Corporation
14/179,651		United States	LOW-VOLTAGE CURRENT SENSE AMPLIFIER	Pending	Lattice Semiconductor Corporation
14/194,484		United States	Logic Element Placement with Repacking Optimization	Pending	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 517/553

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/220,377		United States	DPHY using FPGA differential & single ended I/Os	Pending	Lattice Semiconductor Corporation
14/223,096		United States	DPHY using FPGA differential & single ended I/Os	Pending	Lattice Semiconductor Corporation
14/245,920		United States	Deterministic Dynamic Element Matching for Generating Precise Current Ratios	Pending	Lattice Semiconductor Corporation
14/271,331		United States	Inline Defect To Sort Test Correlation In Semiconductor Manufacturing	Pending	Lattice Semiconductor Corporation
14/271,955		United States	Performance-focused Adaptive Automatic Incremental Flow	Pending	Lattice Semiconductor Corporation
14/283,329		United States	Configuration logic controlled memory BIST (built-in self-test) for back-to-back initialization and readback of embedded block RAMs in FPGAs	Pending	Lattice Semiconductor Corporation
14/308,747		United States	A novel Output Driver drive strength and termination resistor continuously calibrating PVT compensation scheme	Pending	Lattice Semiconductor Corporation
14/313,443		United States	FPGA Hardware debug during post-config power-up and before logic analyzer connect	Pending	Lattice Semiconductor Corporation
14/313,778		United States	IOLOGIC Delay Cell Stealing for Holdtime Correction	Pending	Lattice Semiconductor Corporation
14/316,049		United States	Mapping Constant Multipliers To ICE Devices	Pending	Lattice Semiconductor Corporation
14/319,481		United States	Incrementer Absorption into Multiplier Logic	Pending	Lattice Semiconductor Corporation
14/320,169		United States	Method to Implement Mixed-	Pending	Lattice

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Width Mode Memory in Fixed-Mode Memory Architecture with Masking		Semiconductor Corporation
14/320,074		United States	Two Level Voltage Regulator scheme for SRAM Operation	Pending	Lattice Semiconductor Corporation
14/327,811		United States	Implementing Dual Boot For XO2 and Multiple ASCs	Pending	Lattice Semiconductor Corporation
14/339,164		United States	A unique method to optimize clock to out path	Pending	Lattice Semiconductor Corporation
14/339,229		United States	New method on bus-based clock_to_out timing optimization	Pending	Lattice Semiconductor Corporation
14/482,001		United States	Physically-aware Programmable Multiport Memory BIST with on-the-fly ATE-configurable memory tests	Pending	Lattice Semiconductor Corporation
14/509,564		United States	Dont-care based mux absorption into ice40 carry chain	Pending	Lattice Semiconductor Corporation
14/525,240		United States	Level shifter that eliminates static power dissipation	Pending	Lattice Semiconductor Corporation
14/535,454		United States	Low power and high performance class AB amplifier control common mode in SerDes Transmitter	Pending	Lattice Semiconductor Corporation
14/535,351		United States	ICO metastability prevention during start-up	Pending	Lattice Semiconductor Corporation
14/558,851		United States	Low Power and Flexible TX FFE With Programmable Tap Positions And Coefficients Driver Architecture	Pending	Lattice Semiconductor Corporation
14/576,348		United States	Reconfigurable and Scalable Hardware Management Architecture	Pending	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/576,245		United States	Methodology that allows multiple hardware or hardware-software controllers with different bus interfaces to share a common resource	Pending	Lattice Semiconductor Corporation
14/604,515		United States	Enhancement of FPGA hardware debugger to be used as a design controller/exerciser with user registers	Pending	Lattice Semiconductor Corporation
14/609,181		United States	Algorithm to Optimize Hot Swapping	Pending	Lattice Semiconductor Corporation
14/610,074		United States	Ripple Mode using 3-LUT for Generate	Pending	Lattice Semiconductor Corporation
14/610,127		United States	Combine OFX with LUT output and SUM into a single output to reduce number of signals to routing block	Pending	Lattice Semiconductor Corporation
14/611,069		United States	High speed complementary NMOS LUT logic	Pending	Lattice Semiconductor Corporation
14/611,095		United States	Shared Logic for Multiple Registers with asynchronous initialization with preload	Pending	Lattice Semiconductor Corporation
11/949,454	7,427,874	United States	Interface block architectures	Issued	Lattice Semiconductor Corporation
11/676,196	7,327,160	United States	SERDES with programmable I/O architecture	Issued	Lattice Semiconductor Corporation
6,786,564	6,786,564	United States	Inkjet printer, drive method and drive device for same	Issued	Lattice Semiconductor Corporation
11/839,107	7,856,050	United States	Receiver and transmitter calibration to compensate for frequency dependent I/Q imbalance	Issued	Lattice Semiconductor Corporation
07/679,370	5,255,221	United States	Fully configurable versatile field programmable function	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			element		Corporation
06/551,735	4,642,797	United States	High speed first-in-first-out memory	Issued	Lattice Semiconductor Corporation
08/042,533	5,394,037	United States	Sense amplifiers and sensing methods	Issued	Lattice Semiconductor Corporation
08/115,533	5,404,055	United States	Input routing pool	Issued	Lattice Semiconductor Corporation
08/115,723	5,394,033	United States	Structure and method for implementing hierarchical routing pools in a programmable logic circuit	Issued	Lattice Semiconductor Corporation
08/342,675	5,506,517	United States	Output enable structure and method for a programmable logic device	Issued	Lattice Semiconductor Corporation
07/911,841	5,357,156	United States	Active clamp circuit scheme for CMOS devices	Issued	Lattice Semiconductor Corporation
08/179,887	5,886,378	United States	Single polysilicon layer flash E.sup.2 PROM cell	Issued	Lattice Semiconductor Corporation
07/853,453	5,231,316	United States	Temperature compensated CMOS voltage to current converter	Issued	Lattice Semiconductor Corporation
08/108,363	5,353,246	United States	Programmable semiconductor antifuse structure and method of fabricating	Issued	Lattice Semiconductor Corporation
07/785,442	5,281,906	United States	Tunable voltage reference circuit to provide an output voltage with a predetermined temperature coefficient independent of variation in supply voltage	Issued	Lattice Semiconductor Corporation
07/696,453	5,251,169	United States	Non-volatile erasable and programmable interconnect cell	Issued	Lattice Semiconductor Corporation
07/538,211	5,255,203	United States	Interconnect structure for programmable logic device	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
08/106,263	5,412,260	United States	Multiplexed control pins for in-system programming and boundary scan state machines in a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/033,934	5,418,390	United States	Single polysilicon layer E.sup.2 PROM cell	Issued	Lattice Semiconductor Corporation
07/993,711	5,452,229	United States	Programmable integrated-circuit switch	Issued	Lattice Semiconductor Corporation
07/957,311	5,329,179	United States	Arrangement for parallel programming of in-system programmable IC logical devices	Issued	Lattice Semiconductor Corporation
07/288,945	4,896,296	United States	Programmable logic device configurable input/output cell	Issued	Lattice Semiconductor Corporation
06/882,602	4,887,239	United States	One-time programmable data security system for programmable logic device	Issued	Lattice Semiconductor Corporation
06/871,063	4,766,569	United States	Programmable logic array	Issued	Lattice Semiconductor Corporation
06/862,815	4,879,688	United States	In-system programmable logic device	Issued	Lattice Semiconductor Corporation
06/707,670	4,833,646	United States	Programmable logic device with limited sense currents and noise reduction	Issued	Lattice Semiconductor Corporation
07/236,348	4,852,044	United States	Programmable data security circuit for programmable logic device	Issued	Lattice Semiconductor Corporation
11/400,924	7411424	United States	Programmable logic function generator using non-volatile programmable memory switches	Issued	Lattice Semiconductor Corporation
13/403,146		United States	Surface Mountable Integrated Circuit Packaging Scheme	Pending	SiBEAM, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/242,665		United States	High Speed Integrated Circuit Interface	Pending	SiBEAM, Inc.
14/196,978		United States	Calibration of Single-Ended High-Speed Interfaces	Pending	Silicon Image, Inc.
14/474,005		United States	Inter-Device Conflict Resolution on a Multimedia Link	Pending	Silicon Image, Inc.
61/989,417		United States	Control Target Selection	Pending	Silicon Image, Inc.
61/988,812		United States	Lip Sync Delay Compensation	Pending	Silicon Image, Inc.
61/989,415		United States	Streaming Data and Metadata Synchronization	Pending	Silicon Image, Inc.
61/991,126		United States	Stream Creation with Limited Topology Information	Pending	Silicon Image, Inc.
61/989,411		United States	Topology Discovery	Pending	Silicon Image, Inc.
14/463,146		United States	Radio Frequency Interference Reduction In Multimedia Interfaces	Pending	Silicon Image, Inc.
14/578,266		United States	Control Target Selection	Pending	Silicon Image, Inc.
14/578,257		United States	System for Dynamic Audio Visual Capabilities Exchange	Pending	Silicon Image, Inc.
62/089,767		United States	High-Bandwidth Digital Content Protection over Audio Return Channel	Pending	Silicon Image, Inc.
12/573,492	8482462	United States	MULTI-ANTENNA BEAM-FORMING SYSTEM FOR TRANSMITTING CONSTANT ENVELOPE SIGNALS DECOMPOSED FROM A VARIABLE ENVELOPE SIGNAL	Issued	Silicon Image, Inc.
12/678,463	8207892	United States	TECHNIQUE FOR DETERMINING AN ANGLE OF ARRIVAL IN A COMMUNICATION SYSTEM	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/675,269	8374558	United States	ANTENNA ARRAY WITH FLEXIBLE INTERCONNECT FOR A MOBILE WIRELESS DEVICE	Issued	Silicon Image, Inc.
12/333,134	8213872	United States	TECHNIQUE FOR LOW-POWER OPERATION OF A WIRELESS DEVICE	Issued	Silicon Image, Inc.
12/933,876	8256123	United States	DISPLACEMENT SENSING USING A FLEXIBLE SUBSTRATE	Issued	Silicon Image, Inc.
14/196,993		United States	Calibration of Single-Ended High-Speed Interfaces	Pending	Silicon Image, Inc.
13/988,047		United States	INTEGRATED PHASE-SHIFTING-AND-COMBINING CIRCUITRY TO SUPPORT MULTIPLE ANTENNAS	Pending	Silicon Image, Inc.
14/002,353		United States	TRACKING SYSTEM WITH ORTHOGONAL POLARIZATIONS AND A RETRO-DIRECTIVE ARRAY	Pending	Silicon Image, Inc.
13/726,822		United States	HIGH-ACCURACY DETECTION IN COLLABORATIVE TRACKING SYSTEMS	Pending	Silicon Image, Inc.
13/859,764		United States	ANTENNA SELECTION AND PILOT COMPRESSION IN MIMO SYSTEMS	Pending	Silicon Image, Inc.
62/100,841		United States	I/Q Imbalance Correction for the Combination of Multiple Radio Frequency Frontends	Pending	Silicon Image, Inc.
12/532,107	8571126	United States	MULTI-ANTENNA TRANSMITTER FOR MULTI-TONE SIGNALING	Issued	Silicon Image, Inc.
14/065,420		United States	MULTI-ANTENNA TRANSMITTER FOR MULTI-TONE SIGNALING	Pending	Silicon Image, Inc.
12/679,764	8605823	United States	COMMUNICATION USING	Issued	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			CONTINUOUS-PHASE MODULATED SIGNALS		Inc.
14/101,274		United States	COMMUNICATION USING CONTINUOUS-PHASE MODULATED SIGNALS	Pending	Silicon Image, Inc.
12/746,526	8484277	United States	TRANSFORMING SIGNALS USING PASSIVE CIRCUITS	Issued	Silicon Image, Inc.
13/498,884	8610474	United States	SIGNAL DISTRIBUTION NETWORKS AND RELATED MET	Issued	Silicon Image, Inc.
14/089,094		United States	SIGNAL DISTRIBUTION NETWORKS AND RELATED METHODS	Pending	Silicon Image, Inc.
13/519,302		United States	Phase Detection Circuits and Methods	Pending	Silicon Image, Inc.
13/574,586	8795082	United States	DIRECTIONAL BEAM STEERING SYSTEM AND METHOD TO DETECT LOCATION AND MOTION	Issued	Silicon Image, Inc.
14/331,144		United States	DIRECTIONAL BEAM STEERING SYSTEM AND METHOD TO DETECT LOCATION AND MOTION	Pending	Silicon Image, Inc.
13/704,564		United States	Methods and Systems for Near-Field MIMO Communications	Pending	Silicon Image, Inc.
14/235,783		United States	HIGH-ACCURACY AND LOW-POWER TRACKING SYSTEM FOR MOBILE DEVICES	Pending	Silicon Image, Inc.
14/234,623		United States	LOW-COST TRACKING SYSTEM	Pending	Silicon Image, Inc.
14/240,405		United States	CALIBRATING A RETRO-DIRECTIVE ARRAY FOR AN ASYMMETRIC WIRELESS LINK	Pending	Silicon Image, Inc.
14/364,002		United States	COLLABORATIVE CHANNEL SOUNDING IN MULTI-ANTENNA	Pending	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			SYSTEMS		
08/815,486	6,157,360	United States	System And Method For Driving Columns Of An Active Matrix Display	Issued	Silicon Image, Inc.
08/920,336	5,955,929	United States	Voltage-Controlled Oscillator Resistant To Supply Voltage Noise	Issued	Silicon Image, Inc.
09/007,707	5,969,552	United States	Dual Loop Delay-Locked Loop	Issued	Silicon Image, Inc.
09/298,647	6,259,427	United States	Scaling Multi-Dimensional Signals Using Variable Weighting Factors	Issued	Silicon Image, Inc.
09/298,369	6,374,361	United States	Skew-Insensitive Low Voltage Differential Receiver	Issued	Silicon Image, Inc.
09/393,849	6,738,417	United States	Method And Apparatus For Bidirectional Data Transfer Between A Digital Display And A Computer	Issued	Silicon Image, Inc.
09/326,503	6,940,496	United States	Display Module Driving System And Digital To Analog Converter For Driving Display	Issued	Silicon Image, Inc.
09/392,229	6,564,269	United States	Bi-Directional Data Transfer Using The Video Blanking Period In A Digital Data Stream	Issued	Silicon Image, Inc.
09/393,234	6,307,543	United States	Bi-Directional Data Transfer Using Two Pair Of Differential Lines As A Single Additional Differential Pair	Issued	Silicon Image, Inc.
09/947,008	6,492,984	United States	Bi-Directional Data Transfer Using Two Pair Of Differential Lines As A Single Additional Differential Pair	Issued	Silicon Image, Inc.
09/759,624	6,891,910	United States	Baud-Rate Timing Recovery	Issued	Silicon Image, Inc.
09/574,571	6,326,826	United States	Wide Frequency-Range Delay- Locked Loop Circuit	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/881,271	6,954,491	United States	Methods And Systems For Sending Side-Channel Data During Data Inactive Period	Issued	Silicon Image, Inc.
09/922,990	6,961,095	United States	Digital Display Jitter Correction Apparatus And Method	Issued	Silicon Image, Inc.
11/219,323	7,557,863	United States	Digital Display Jitter Correction Apparatus And Method	Issued	Silicon Image, Inc.
09/989,587	6,717,478	United States	Multi-Phase Voltage Controlled Oscillator (VCO) With Common Mode Control	Issued	Silicon Image, Inc.
10/371,220	7,231,009	United States	Data Synchronization Across An Asynchronous Boundary Using, For Example, Multi-Phase Clocks	Issued	Silicon Image, Inc.
09/989,580	7,103,013	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
11/441,669	7,599,316	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
12/573,847	8,116,240	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
10/045,297	7,257,129	United States	Memory Architecture With Multiple Serial Communications Ports	Issued	Silicon Image, Inc.
11/828,286	7,903,684	United States	Communications Architecture For Transmission Of Data Between Memory Bank Caches And Ports	Issued	Silicon Image, Inc.
09/167,527	6,380,978	United States	Digital Video System And Methods For Providing Same	Issued	DVDO, INC. and Silicon Image, Inc.
10/032,136	7,215,376	United States	Digital Video System And Methods For Providing Same	Issued	DVDO, INC. and Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/942,740	7,359,624	United States	Portable DVD Player	Issued	Silicon Image, Inc.
09/372,713	6,489,998	United States	Method And Apparatus For Deinterlacing Digital Video	Issued	Silicon Image, Inc.
09/941,949	6,909,469	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
10/251,642	7,027,099	United States	Method And Apparatus For Deinterlacing Digital Video Images	Issued	Silicon Image, Inc.
11/054,748	7,391,481	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
11/357,364	7,499,103	United States	Method And Apparatus For Detecting Frequency In Digital Video Images	Issued	Silicon Image, Inc.
11/932,808	7,633,559	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
09/410,543	6,700,622	United States	Method And Apparatus For Detecting The Source Format Of Video Images	Issued	Silicon Image, Inc.
09/396,993	6,515,706	United States	Method And Apparatus For Detecting And Smoothing Diagonal Features In Video Images	Issued	Silicon Image, Inc.
10/191,764	6,829,013	United States	Method And Apparatus For Detecting And Smoothing Diagonal Features In Video Images	Issued	Silicon Image, Inc.
09/363,312	6,681,059	United States	Method And Apparatus For Efficient Video Scaling	Issued	Silicon Image, Inc.
09/359,530	6,587,158	United States	Method And Apparatus For Reducing On-Chip Memory In Vertical Video Processing	Issued	Silicon Image, Inc.
09/226,776	6,219,747	United States	Methods And Apparatus For Variable Length SDRAM	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Transfers		
09/805,588	6,385,692	United States	Methods and Apparatus for Variable Length SDRAM Transfers	Issued	Silicon Image, Inc.
09/227,502	6,393,505	United States	Methods And Apparatus For Data Bus Arbitration	Issued	Silicon Image, Inc.
09/226,381	6,473,476	United States	Method And Apparatus For Providing Deterministic Resets For Clock Divider Systems	Issued	Silicon Image, Inc.
09/837,894	6,867,814	United States	Method, System And Article Of Manufacture For Identifying The Source Type And Quality Level Of A Video Sequence	Issued	Silicon Image, Inc.
09/478,122	7,203,557	United States	Audio Signal Delay Apparatus And Method	Issued	Silicon Image, Inc.
10/663,413	7,408,992	United States	Detection And Repair Of MPEG-2 Chroma Upconversion Artifacts	Issued	Silicon Image, Inc.
09/905,318	7,123,307	United States	Clock Jitter Limiting Scheme In Video Transmission Through Multiple Stages	Issued	Silicon Image, Inc.
09/905,615	6,944,804	United States	System And Method For Measuring Pseudo Pixel Error Rate	Issued	Silicon Image, Inc.
09/904,783	6,625,560	United States	Method Of Testing Serial Interface	Issued	Silicon Image, Inc.
09/989,590	6,845,461	United States	High-Speed Bus With Embedded Clock Signals	Issued	Silicon Image, Inc.
09/989,645	6,809,567	United States	System And Method For Multiple-Phase Clock Generation	Issued	Silicon Image, Inc.
09/905,511	7,062,004	United States	Method And Apparatus For Adaptive Control Of PLL Loop Bandwidth	Issued	Silicon Image, Inc.
10/057,823	7,023,487	United States	Deinterlacing Of Video Sources Via Image Feature Edge Detection	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/954,663	7,558,326	United States	Method And Apparatus For Sending Auxiliary Data On A TMDS-Like Link	Issued	Silicon Image, Inc.
10/036,234	7,359,437	United States	Encoding Method And System For Reducing Inter-Symbol Interference Effects In Transmission Over A Serial Link	Issued	Silicon Image, Inc.
10/095,422	7,257,163	United States	Method And System For Reducing Inter-Symbol Interference Effects In Transmission Over A Serial Link With Mapping Of Each Word In A Cluster Of Received Words To A Single Transmitted Word	Issued	Silicon Image, Inc.
10/171,860	7,088,398	United States	Method And Apparatus For Regenerating A Clock For Auxiliary Data Transmitted Over A Serial Link With Video Data	Issued	Silicon Image, Inc.
10/192,296	6,914,637	United States	Method And System For Video And Auxiliary Data Transmission Over A Serial Link	Issued	Silicon Image, Inc.
10/357,750	7,283,566	United States	Method And Circuit For Generating Time Stamp Data From An Embedded-Clock Audio Data Stream And A Video Clock	Issued	Silicon Image, Inc.
10/016,247	6,714,206	United States	Method And System For Spatial-Temporal Dithering For Displays With Overlapping Pixels	Issued	Silicon Image, Inc.
10/133,813	7,136,484	United States	Cryptosystems Using Commuting Pairs In A Monoid	Issued	Silicon Image, Inc.
10/047,772	7,109,958	United States	Supporting Circuitry And Method For Controlling Pixels	Issued	Silicon Image, Inc.
10/045,393	7,039,121	United States	Method And System For Transition-Controlled Selective Block Inversion	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Communications		
08/656,032	6,018,456	United States	Enclosure For Removable Computer Peripheral Equipment	Issued	CMD Technology Inc. and Silicon Image, Inc.
08/906,775	5,991,546	United States	System And Method For Interfacing Manually Controllable Input Devices To A Universal Computer Bus System	Issued	CMD Technology Inc. and Silicon Image, Inc.
10/171,820	7,225,282	United States	Method And Apparatus For A Two-Wire Serial Command Bus Interface	Issued	Silicon Image, Inc.
11/713,241	7,441,065	United States	Adaptive Beam-Steering Methods To Maximize Wireless Link Budget And Reduce Delay-Spread Using Multiple Transmit And Receive Antennas	Issued	Silicon Image, Inc.
10/210,839	7,171,525	United States	Method And System For Arbitrating Priority Bids Sent Over Serial Links To A Multi-Port Storage Device	Issued	Silicon Image, Inc.
09/688,536	6,380,783	United States	Cyclic Phase Signal Generation From A Single Clock Source Using Current Phase Interpolation	Issued	Silicon Image, Inc.
09/847,837	6,535,029	United States	Fully Differential Continuous-Time Current-Mode High Speed CMOS Comparator	Issued	Silicon Image, Inc.
10/270,882	7,009,827	United States	Voltage Swing Detection Circuit For Hot Plug Event Or Device Detection Via A Differential Link	Issued	Silicon Image, Inc.
10/162,046	6,843,674	United States	Method And Apparatus For Connecting Serial ATA Storage Components	Issued	Silicon Image, Inc.
09/945,278	7,131,004	United States	Method And Apparatus For Encrypting Data Transmitted Over A Serial Link	Issued	Silicon Image, Inc.
11/499,124	7,900,047	United States	Method And Apparatus For Encrypting Data Transmitted	Issued	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Over A Serial Link		Inc.
11/543,501	7,757,085	United States	Method And Apparatus For Encrypting Data Transmitted Over A Serial Link	Issued	Silicon Image, Inc.
10/224,995	7,218,737	United States	System And Method For An Adaptive State Machine To Control Signal Filtering In A Serial Link	Issued	Silicon Image, Inc.
09/991,057	7,242,766	United States	Method And System For Encrypting And Decrypting Data Using An External Agent	Issued	Silicon Image, Inc.
10/085,177	7,035,290	United States	Method And System For Temporary Interruption Of Video Data Transmission	Issued	Silicon Image, Inc.
10/036,794	6,976,201	United States	Method And System For Host Handling Of Communications Errors	Issued	Silicon Image, Inc.
10/053,461	7,113,507	United States	Method And System For Communicating Control Information Via Out-Of-Band Symbols	Issued	Silicon Image, Inc.
10/045,625	7,746,798	United States	Method And System For Integrating Packet Type Information With Synchronization Symbols	Issued	Silicon Image, Inc.
10/035,911	7,154,905	United States	Method And System For Nesting Of Communications Packets	Issued	Silicon Image, Inc.
10/045,600	6,771,192	United States	Method And System For DC-Balancing At The Physical Layer	Issued	Silicon Image, Inc.
10/045,601	7,340,558	United States	Multisection Memory Bank System	Issued	Silicon Image, Inc.
09/989,647	7,058,121	United States	Logic Gates Including Diode-Connected Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) To Control Input Threshold Voltage Levels And Switching Transients Of	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Output Logic Signals		
09/989,487	6,985,005	United States	Differential Amplifiers Using Asymmetric Transfer Characteristics To Suppress Input Noise In Output Logic Signals	Issued	Silicon Image, Inc.
11/330,047	7,456,648	United States	Differential Amplifiers Using Asymmetric Transfer Characteristics To Suppress Input Noise In Output Logic Signals	Issued	Silicon Image, Inc.
12/275,686	7,847,583	United States	Transmitter And Receiver Using Asymmetric Transfer Characteristics In Differential Amplifiers To Suppress Noise	Issued	Silicon Image, Inc.
10/403,477	6,819,166	United States	Continuous-Time, Low-Frequency-Gain/High-Frequency-Boosting	Issued	Silicon Image, Inc.
10/417,712	7,348,991	United States	Video Graphics Text Mode Enhancement Method For Digitally Processed Data	Issued	Silicon Image, Inc.
10/287,976	6,873,341	United States	Detection Of Video Windows And Graphics Windows	Issued	Silicon Image, Inc.
10/298,722	7,539,304	United States	Integrated Circuit Having Self Test Capability Using Message Digest And Method For Testing Integrated Circuit Having Message Digest Generation Circuitry	Issued	Silicon Image, Inc.
10/215,936	6,717,468	United States	Dynamically Biased Full-Swing Operation Amplifier For An Active Matrix Liquid Crystal Display Driver	Issued	Silicon Image, Inc.
10/268,832	7,412,053	United States	Cryptographic Device With Stored Key Data And Method For Using Stored Key Data To Perform An Authentication Exchange Of Self Test	Issued	Silicon Image, Inc.
11/950,088	7,797,536	United States	Cryptographic Device With Stored Key Data And Method	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			For Using Stored Key Data To Perform An Authentication Exchange Of Self Test		
10/244,152	6,814,583	United States	Through-Broad PCB Edge Connector, System And Method	Issued	Silicon Image, Inc.
10/247,675	8,064,508	United States	Equalizer With Controllably Weighted Parallel High Pass And Low Pass Filters And Receiver Including Such An Equalizer	Issued	Silicon Image, Inc.
11/796,175	8,275,026	United States	Equalizer With Controllably Weighted Parallel High Pass And Low Pass Filters And Receiver Including Such An Equalizer	Issued	Silicon Image, Inc.
10/651,500	7,551,909	United States	CMOS Transceiver With Dual Current Path VCO	Issued	Silicon Image, Inc.
10/099,533	7,158,593	United States	Combining A Clock Signal And A Data Signal	Issued	Silicon Image, Inc.
10/642,259	7,409,031	United States	Data Sampling Method And Apparatus With Alternating Edge Sampling Phase Detection For Loop Characteristic Stabilization	Issued	Silicon Image, Inc.
10/459,989	7,187,307	United States	Method And System For Encapsulation Of Multiple Levels Of Communication Protocol Functionality Within Line Codes	Issued	Silicon Image, Inc.
10/794,015	7,502,411	United States	Method And Circuit For Adaptive Equalization Of Multiple Signals In Response To A Control Signal Generated From One Of The Equalized Signals	Issued	Silicon Image, Inc.
10/459,992	6,747,580	United States	Method And Apparatus For Encoding Or Decoding Data In Accordance With An Nb/(N+1)B Block Code, And Method For Determining Such A Block Code	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/781,405	7,269,673	United States	Cable With Circuitry For Asserting Stored Cable Data Or Other Information To An External Device Or User	Issued	Silicon Image, Inc.
11/848,758	7,500,032	United States	Cable With Circuitry For Asserting Stored Cable Data Or Other Information To An External Device Or User	Issued	Silicon Image, Inc.
11/123,353	7,375,960	United States	Apparatus For Removably Securing Storage Components In An Enclosure	Issued	Silicon Image, Inc.
10/763,905	7,236,553	United States	Reduced Dead-Cycle, Adaptive Phase Tracking Method And Apparatus	Issued	Silicon Image, Inc.
10/835,301	6,897,793	United States	Method And Apparatus For Run Length Limited TMDS-Like Encoding Of Data	Issued	Silicon Image, Inc.
10/842,231	7,991,096	United States	Data Sampling Method And Apparatus Using Through-Transition Counts To Reject Worst Sampling Position	Issued	Silicon Image, Inc.
10/439,446	7,031,858	United States	Method And Circuit For DC Measurement Of Phase Uniformity Of Multi-Phase Clocks	Issued	Silicon Image, Inc.
10/302,436	7,274,690	United States	An Age Selection Switching Scheme For Data Traffic In A Crossbar Switch	Issued	Silicon Image, Inc.
10/645,786	7,505,422	United States	Preference Programmable First-One Detector And Quadrature Based Random Grant Generator	Issued	Silicon Image, Inc.
10/645,787	7,461,167	United States	A Method For Multicast Service In A Crossbar Switch	Issued	Silicon Image, Inc.
10/762,950	7,352,764	United States	Content Addressable Merged Queue Architecture For Switching Data	Issued	Silicon Image, Inc.
10/434,785	7,519,066	United States	A Method For Switching Data In A Crossbar Switch	Issued	Silicon Image, Inc.
11/372,866	7,694,204	United States	Error Detection In Physical	Issued	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Interfaces For Point-To-Point Communications Between Integrated Circuits		Inc.
12/712,124	7,937,644	United States	Error Detection In Physical Interfaces For Point-To-Point Communications Between Integrated Circuits	Issued	Silicon Image, Inc.
13/099,254	8,099,648	United States	Error Detection In Physical Interfaces For Point-To-Point Communications Between Integrated Circuits	Issued	Silicon Image, Inc.
11/669,416	7,844,762	United States	Parallel Interface Bus To Communicate Video Data Encoded For Serial Data Links	Issued	Silicon Image, Inc.
11/056,995	7,102,446	United States	Phase Lock Loop With Coarse Control Loop Having Frequency Lock Detector And Device Including Same	Issued	Silicon Image, Inc.
11/643,388	7,589,559	United States	Current Mode Circuitry To Modulate A Common Mode Voltage	Issued	Silicon Image, Inc.
12/555,300	7,872,498	United States	Current Mode Circuitry to Modulate a Common Mode Voltage	Issued	Silicon Image, Inc.
11/477,049	7,793,179	United States	Test Clock Control Structures To Generate Configurable Test Clocks For Scan-Based Testing Of Electronic Circuits Using Programmable Test Clock Controllers	Issued	Silicon Image, Inc.
11/856,640	7,782,934	United States	Parameter Scanning For Signal Over-Sampling	Issued	Silicon Image, Inc.
11/592,792	7,450,038	United States	Determining Oversampled Data To Be Included In Unit Intervals	Issued	Silicon Image, Inc.
11/510,254	8,595,434	United States	Smart Scalable Storage Switch Architecture	Issued	Silicon Image, Inc.
14/067,363		United States	Smart Scalable Storage Switch Architecture	Pending	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/314,162	7,571,269	United States	A Covert Channel For Conveying Supplemental Messages In A Protocol-Defined Link For A System Of Storage Devices	Issued	Silicon Image, Inc.
11/637,254	7,602,253	United States	Adaptive Bandwidth Phase Locked Loop With Feedforward Divider	Issued	Silicon Image, Inc.
11/656,331	7,984,369	United States	Concurrent Code Checker And Hardware Efficient High-Speed I/O Having Built-In Self-Test And Debug Features	Issued	Silicon Image, Inc.
11/694,819	7,949,863	United States	Multi-Port Memory Device Having Variable Port Speeds	Issued	Silicon Image, Inc.
11/694,813	7,639,561	United States	Power-Saving Clocking Technique	Issued	Silicon Image, Inc.
11/690,629	7,831,778	United States	Mechanism For Streaming Media Data Over Wideband Wireless Networks	Issued	Silicon Image, Inc.
11/476,457	7,840,861	United States	Scan-Based Testing Of Devices Implementing A Test Clock Control Structure (â€œTCCSâ€)	Issued	Silicon Image, Inc.
11/861,175	8,160,192	United States	Signal Interleaving for Serial Clock and Data Recovery	Issued	Silicon Image, Inc.
11/690,642	7,908,501	United States	Shared Nonvolatile Memory Architecture	Issued	Silicon Image, Inc.
11/742,358	7,698,088	United States	Interface Test Circuitry And Methods	Issued	Silicon Image, Inc.
11/848,641	8,233,432	United States	Ensuring Physical Locality Of Entities Sharing Data	Issued	Silicon Image, Inc.
11/683,608	7,831,877	United States	Method And Apparatus For A Two-Wire Serial Command Bus Interface	Issued	Silicon Image, Inc.
11/690,659	7,849,339	United States	Progressive Power Control Of A Multi-Port Memory Device	Issued	Silicon Image, Inc.
11/567,514	7,365,659	United States	Method Of Context Adaptive Binary Arithmetic Coding	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			And Coding Apparatus Using The Same		
12/778,882		United States	Multi-Level Port Expansion For Port Multipliers	Pending	Silicon Image, Inc.
12/147,248	7,836,223	United States	Operation Of Media Interface To Provide Bidirectional Communications	Issued	Silicon Image, Inc.
11/849,163	8,695,034	United States	Delivering On Screen Display Data To Existing Display Devices	Issued	Silicon Image, Inc.
11/828,219	8,599,315	United States	On Screen Displays Associated With Remote Video Source Devices	Issued	Silicon Image, Inc.
14/070,373		United States	On Screen Displays Associated With Remote Video Source Devices	Pending	Silicon Image, Inc.
11/829,800	7,903,550	United States	Bandwidth Reservation For Data Flows In Interconnection Networks	Issued	Silicon Image, Inc.
11/828,223	8,149,711	United States	Data Stream Control For Network Devices	Issued	Silicon Image, Inc.
13/541,390	8,924,509	United States	Automated Service Discovery And Dynamic Connection Management	Issued	Silicon Image, Inc.
11/836,082	8,468,212	United States	Network Repository For Metadata	Issued	Silicon Image, Inc.
13/919,773		United States	Network Repository For Metadata	Pending	Silicon Image, Inc.
11/829,790	7,911,956	United States	Packet Level Prioritization In Interconnection Networks	Issued	Silicon Image, Inc.
11/828,226		United States	Streaming Data Content In A Network	Pending	Silicon Image, Inc.
11/848,153	7,936,790	United States	Synchronizing Related Data Streams In Interconnection Networks	Issued	Silicon Image, Inc.
11/952,052	8,001,334	United States	Bank Sharing And Refresh In A Shared Multi-Port Memory Device	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/075,954	7,979,589	United States	Method, Apparatus, And System For Port Multiplier Enhancement	Issued	Silicon Image, Inc.
13/298,001		United States	Iddq Testing Of CMOS Devices	Pending	Silicon Image, Inc.
10/788,704	6,944,086	United States	Semiconductor Memory Device	Issued	Silicon Image, Inc.
10/876,231	7,016,255	United States	Multi-Port Memory Device	Issued	Silicon Image, Inc.
10/877,318	7,089,465	United States	Multi-Port Memory Device Having Serial I/O Interface	Issued	Silicon Image, Inc.
12/075,906	7,904,566	United States	Method, Apparatus, And System For Employing An Enhanced Port Multiplier	Issued	Silicon Image, Inc.
12/497,391	8,386,867	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
13/776,508	8,667,354	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
14/145,751	8,924,805	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
12/197,020	8,086,886	United States	Group Power Management Of Network Devices	Issued	Silicon Image, Inc.
12/683,365	8,543,873	United States	Multi-Site Testing Of Computer Memory Devices And Serial I/O Ports	Issued	Silicon Image, Inc.
14/035,795	8,839,058	United States	Multi-Site Testing Of Computer Memory Devices And Serial I/O Ports	Issued	Silicon Image, Inc.
11/969,847	8,090,030	United States	Method, Apparatus And System For Generating And Facilitating Mobile High-Definition Multimedia Interface	Issued	Silicon Image, Inc.
11/969,852	7,856,520	United States	Control Bus For Connection Of Electronic Devices	Issued	Silicon Image, Inc.
11/969,865	7,921,231	United States	Discovery Of Electronic Devices Utilizing A Control	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Bus		
12/172,187	8,238,653	United States	Methods And Mechanisms For Probabilistic Color Correction	Issued	Silicon Image, Inc.
12/392,000		United States	Method, Apparatus, And System For Pre-Authentication And Processing Of Data Streams	Pending	Silicon Image, Inc.
12/391,987	8,644,504	United States	Method, Apparatus, And System For Deciphering Media Content Stream	Issued	Silicon Image, Inc.
12/605,134	8,407,427	United States	Method And System For Improving Serial Port Memory Communication Latency And Reliability	Issued	Silicon Image, Inc.
13/850,147	8,892,825	United States	Method and System for Improving Serial Port Memory Communication Latency and Reliability	Issued	Silicon Image, Inc.
12/260,970	8,036,248	United States	Method, Apparatus, And System For Automatic Data Aligner For Multiple Serial Receivers	Issued	Silicon Image, Inc.
12/359,025	8,026,726	United States	Fault Testing For Interconnections	Issued	Silicon Image, Inc.
12/486,969	8,793,723	United States	Detection Of Encryption Utilizing Error Detection For Received Data	Issued	Silicon Image, Inc.
12/570,874	8,644,334	United States	Messaging To Provide Data Link Integrity	Issued	Silicon Image, Inc.
12/260,972	7,777,652	United States	Coding System For Memory Systems Employing High-Speed Serial Links	Issued	Silicon Image, Inc.
12/847,416	7,978,099	United States	17b/20b Coding System	Issued	Silicon Image, Inc.
12/351,698	8,374,346	United States	Method, Apparatus, And System For Pre-Authentication And Keep-Authentication Of Content Protected Ports	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/316,305	8,347,081	United States	Method, Apparatus And System For Employing A Content Protection System	Issued	Silicon Image, Inc.
12/577,707	8,275,914	United States	Method And System For Transmitting Or Receiving N-Bit Video Data Over A Serial Link	Issued	Silicon Image, Inc.
12/606,096	8,176,214	United States	Transmission Of Alternative Content Over Standard Device Connectors	Issued	Silicon Image, Inc.
12/351,712	8,185,739	United States	Method And System For Detecting Successful Authentication Of Multiple Ports In A Time Based Roving Architecture	Issued	Silicon Image, Inc.
12/512,877	8,458,343	United States	Signaling For Transitions Between Modes Of Data Transmission	Issued	Silicon Image, Inc.
12/983,233	8,489,784	United States	Adaptive Interconnection Scheme For Multimedia Devices	Issued	Silicon Image, Inc.
13/004,359	8,755,431	United States	Transmission And Detection Of Multi-Channel Signals In Reduced Channel Format	Issued	Silicon Image, Inc.
12/650,357		United States	Method, Apparatus, And System For Simultaneously Previewing Contents From Multiple Protected Sources	Pending	Silicon Image, Inc.
12/712,933	8,692,937	United States	Video Frame Synchronization	Issued	Silicon Image, Inc.
12/966,194		United States	Transmission And Handling Of Three-Dimensional Video Content	Pending	Silicon Image, Inc.
12/873,124	8,325,757	United States	De-Encapsulation Of Data Streams Into Multiple Links	Issued	Silicon Image, Inc.
12/704,417	8,510,487	United States	Hybrid Interface For Serial And Parallel Communication	Issued	Silicon Image, Inc.
13/934,147	8,751,709	United States	Hybrid Interface For Serial And Parallel Communication	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/842,165	8,930,692	United States	Mechanism For Internal Processing Of Content Through Partial Authentication On Secondary Channel	Issued	Silicon Image, Inc.
12/842,190		United States	Mechanism For Partial Encryption Of Data Streams	Pending	Silicon Image, Inc.
13/021,958		United States	Determination Of Physical Connectivity Status Of Devices Based On Electrical Measurement	Allowed	Silicon Image, Inc.
12/898,528	8,598,898	United States	Testing Of High-Speed Input-Output Devices	Issued	Silicon Image, Inc.
13/434,273		United States	Method, Apparatus And System For Transitioning An Audio/Video Device Between A Source Mode And A Sink Mode	Pending	Silicon Image, Inc.
12/848,037	8,624,960	United States	Multi-View Display System	Issued	Silicon Image, Inc.
14/094,668		United States	Multi-View Display System	Pending	Silicon Image, Inc.
12/816,437	8,698,958	United States	Mechanism For Memory Reduction In Picture-In-Picture Video Generation	Issued	Silicon Image, Inc.
13/753,408		United States	Communication Bridging Between Devices Via Multiple Bridge Elements	Pending	Silicon Image, Inc.
13/198,584		United States	Conversion Of Multimedia Data Streams For Use By Connected Devices	Pending	Silicon Image, Inc.
12/906,939	8,537,201	United States	Combining Video Data Streams Of Differing Dimensionality For Concurrent Display	Issued	Silicon Image, Inc.
13/172,745	8,484,387	United States	Detection Of Cable Connections For Electronic Devices	Issued	Silicon Image, Inc.
13/172,742	8,601,173	United States	Detection Of Cable Connections For Electronic	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Devices		
13/362,930		United States	Mechanism For Low Power Standby Mode Control Circuit	Allowed	Silicon Image, Inc.
13/217,138	8,379,145	United States	Conversion And Processing Of Deep Color Video In A Single Clock Domain	Issued	Silicon Image, Inc.
12/979,995	8,874,820	United States	Mechanism For Facilitating A Configurable Port-Type Peripheral Component Interconnect Express/Serial Advanced Technology Attachment Host Controller Architecture	Issued	Silicon Image, Inc.
12/950,850	8,504,672	United States	Discovery Of Electronic Devices In A Combined Network	Issued	Silicon Image, Inc.
13/959,592	8,799,443	United States	Discovery of Electronic Devices in a Combined Network	Issued	Silicon Image, Inc.
13/348,378		United States	Proxy Device Operation In Command And Control Network	Pending	Silicon Image, Inc.
12/950,867		United States	Transfer Of Control Bus Signaling On Packet-Switched Network	Pending	Silicon Image, Inc.
13/339,339		United States	Mechanism For Recovering Clock For Streaming Content Over A Packetized Network	Pending	Silicon Image, Inc.
13/302,452		United States	Multimedia I/O System Architecture for Advanced Digital Television	Pending	Silicon Image, Inc.
13/107,031		United States	Audio And Video Data Multiplexing For Multimedia Stream Switch	Pending	Silicon Image, Inc.
13/174,630		United States	Single-Ended Configurable Multi-Mode Driver	Pending	Silicon Image, Inc.
13/173,302		United States	Fine-Grained Self Refresh Control For DRAM Devices	Pending	Silicon Image, Inc.
13/174,616	8,760,188	United States	Configurable Multi-Dimensional Driver And	Issued	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Receiver		Inc.
13/083,399	8,611,486	United States	Adjustment Of Clock Signals Regenerated From A Data Stream	Issued	Silicon Image, Inc.
11/437,357	7,982,798	United States	Edge Detection	Issued	Silicon Image, Inc.
13/153,230	8,446,525	United States	Edge Detection	Issued	Silicon Image, Inc.
10/753,909	7,400,359	United States	Video Stream Routing And Format Conversion Unit With Audio Delay	Issued	Silicon Image, Inc.
10/889,855	7,710,501	United States	Time Base Correction And Frame Rate Conversion	Issued	Silicon Image, Inc.
11/487,144	8,004,606	United States	Original Scan Line Detection	Issued	Silicon Image, Inc.
11/941,050	8,086,067	United States	Noise Cancellation	Issued	Silicon Image, Inc.
11/512,754	8,120,703	United States	Source-Adaptive Video Deinterlacer	Issued	Silicon Image, Inc.
12/204,760	8,559,746	United States	System, Method And Apparatus For Smoothing Of Edges In Images To Remove Irregularities	Issued	Silicon Image, Inc.
14/054,575		United States	System, Method and Apparatus for Smoothing of Edges in Images to Remove Irregularities	Pending	Silicon Image, Inc.
12/703,623	8,452,117	United States	Block Noise Detection And Filtering	Issued	Silicon Image, Inc.
13/899,222	8,891,897	United States	Block Noise Detection And Filtering	Issued	Silicon Image, Inc.
13/335,398		United States	Ringing Suppression In Video Scalers	Pending	Silicon Image, Inc.
13/546,904		United States	Transmission Of Multiple Protocol Data Elements Via An Interface Utilizing A Data Tunnel	Pending	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/202,995	7,904,117	United States	Wireless Communication Device Using Adaptive Beamforming	Issued	SiBEAM, Inc.
11/706,711	7,710,319	United States	HD Physical Layer Of A Wireless Communication Device	Issued	SiBEAM, Inc.
12/748,276	7,982,669	United States	Adaptive Beam-Steering Methods To Maximize Wireless Link Budget And Reduce Delay-Spread Using Multiple Transmit And Receive Antennas	Issued	SiBEAM, Inc.
11/706,470	8,014,416	United States	Inter-Port Communication In A Multi-Port Memory Device	Issued	Silicon Image, Inc.
11/689,386	7,881,258	United States	Circuitry To Prevent Peak Power Problems During Scan Shift	Issued	SiBEAM, Inc.
11/726,874	8,155,712	United States	Low Power Very High-Data Rate Device	Issued	SiBEAM, Inc.
11/588,472	8,022,887	United States	Planar Antenna	Issued	SiBEAM, Inc.
11/752,073		United States	A Compact Millimeter Wave Vertical Interconnection Scheme By Combining Flip-Chip, Layer Transition	Pending	SiBEAM, Inc.
11/752,083	7,675,465	United States	Surface Mountable Integrated Circuit Packaging Scheme	Issued	SiBEAM, Inc.
12/215,959		United States	Mechanism For Communication With Multiple Wireless Video Area Networks	Pending	SiBEAM, Inc.
11/981,935		United States	Wireless HD Mac Frame Format	Pending	SiBEAM, Inc.
11/938,126	8,170,522	United States	Multi-Transformer Architecture For An RF Active Circuit	Issued	SiBEAM, Inc.
11/999,810	8,750,241	United States	Concurrent Association With Multiple WVAN Network	Issued	SiBEAM, Inc.
12/079,133	8,831,225	United States	Data Security	Issued	SiBEAM, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/011,404	7,948,961	United States	Wireless Proximity Estimation	Issued	SiBEAM, Inc.
11/982,209	8,279,784	United States	Wireless HD AV Packet Format	Issued	SiBEAM, Inc.
12/055,160	8,170,617	United States	Extensions To Adaptive BeamSteering Method	Issued	SiBEAM, Inc.
12/164,757		United States	Exchanging Information Between Components Coupled With An I2C Bus Via Separate Banks	Pending	SiBEAM, Inc.
12/167,195	8,229,352	United States	Wireless Architecture For 60 GHz	Issued	SiBEAM, Inc.
11/901,069	7,986,753	United States	Modified Branch Metric For Decoders And Equalizers	Issued	SiBEAM, Inc.
12/059,757	7,915,909	United States	RF Integrated Circuit Test Methodology And System	Issued	SiBEAM, Inc.
12/164,907		United States	Dispatch Capability Using A Single Physical Interface	Pending	SiBEAM, Inc.
12/165,468		United States	Bitmap Device Identification In A Wireless Communication System	Pending	SiBEAM, Inc.
12/165,472	8,897,719	United States	Initializing A Transceiver In A Wireless Communication System	Issued	SiBEAM, Inc.
12/164,849	8,341,271	United States	Device Discovery In A Wireless Communication System	Issued	SiBEAM, Inc.
12/164,810	8,116,333	United States	Connection Control In A Wireless Communication System	Issued	SiBEAM, Inc.
12/699,758	8,588,193	United States	Enhanced Wireless Data Rates Using Multiple Beams	Issued	SiBEAM, Inc.
12/699,781	8,457,026	United States	Enhanced Wireless Data Rates Using Multiple Beams	Issued	SiBEAM, Inc.
13/113,318		United States	Apparatus, System, And Method For A Compact Symmetrical Transition Structure For Radio	Allowed	SiBEAM, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Frequency Applications		
14/128,551		United States	Method To Drive HDMI Or MHL Or USB Data Through One Set Of Pins	Pending	Silicon Image, Inc.
13/984,018		United States	Concept And Method Of Reducing Data Dependent Jitter	Pending	Silicon Image, Inc.
13/269,450		United States	Identification And Handling Of Data Streams Using Coded Preambles	Allowed	Silicon Image, Inc.
13/611,786		United States	Combining Video And Audio Streams Utilizing Pixel Repetition Bandwidth	Pending	Silicon Image, Inc.
14/118,832		United States	Compensation Scheme For MHL Common Mode Clock Swing	Pending	Silicon Image, Inc.
13/773,534		United States	Transmitting Multiple Differential Signals Over a Reduced Number of Physical Channels	Pending	Silicon Image, Inc.
13/460,393		United States	Cost-Efficient And Low-Latency Motion Picture Encoding For Limited Channel Bandwidth	Pending	Silicon Image, Inc.
13/791,494	8,925,003	United States	Mechanism For Facilitating Syncronization Of Audio And Video Between Multiple Media Devices	Issued	Silicon Image, Inc.
13/622,286	8,885,435	United States	Interfacing Between Integrated Circuits With Asymmetric Voltage Swing	Issued	Silicon Image, Inc.
13/770,984		United States	Configurable Single Ended Driver	Pending	Silicon Image, Inc.
13/779,372	8,920,188	United States	Integrated Connector/Flex Cable	Issued	Silicon Image, Inc.
13/834,927		United States	Simultaneous Transmission Of Clock And Bidirectional Data Over A Communication Channel	Allowed	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
13/605,708	8,841,974	United States	Test Solution For Ring Oscillators	Issued	Silicon Image, Inc.
14/193,932		United States	Test Solution for a Random Number Generator	Pending	Silicon Image, Inc.
13/787,664		United States	Auxiliary Data Encoding In Video Data	Pending	Silicon Image, Inc.
13/738,768		United States	Method And Apparatus For Reducing Digital Video Image Data	Pending	Silicon Image, Inc.
13/736,765	8,832,338	United States	Mechanism For Facilitating Dynamic Timestamp-Less Clock Regeneration For Transmitting Media Streams Over Shared Channels	Issued	Silicon Image, Inc.
14/123,037		United States	Timing Controlled Cascade Feed-Through High Speed Line Driver	Pending	Silicon Image, Inc.
13/776,577		United States	Apparatus, System And Method For Providing Clock And Data Signaling	Pending	Silicon Image, Inc.
13/940,038		United States	Integrated Mobile Desktop	Pending	Silicon Image, Inc.
13/915,586		United States	Multiple Protocol Tunneling Using Time Division Operations	Pending	Silicon Image, Inc.
13/891,842	8,786,776	United States	Method, Apparatus And System For Communicating Sideband Data With Non-Compressed Video	Issued	Silicon Image, Inc.
13/671,527		United States	Methods And Apparatuses To Provide And Electro-Optical Alignment	Pending	Silicon Image, Inc.
14/371,973		United States	Charge Pump Calibration for Dual-Path Phase-Locked Loop	Pending	Silicon Image, Inc.
14/115,324		United States	Mechanism for Facilitating Dynamic Phase Detection with High Jitter Tolerance for Images of Media Streams	Allowed	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/135,470		United States	Apparatus, System and Method for Formatting Audio-Video Information	Pending	Silicon Image, Inc.
13/839,671		United States	Full Frame Buffer To Improve Video Performance In Low- Latency Video Communication Systems	Pending	Silicon Image, Inc.
12/057,051		United States	Bi-Directional Digital Interface For Video And Audio (DIVA)	Pending	Silicon Image, Inc.
11/760,164	7,940,809	United States	Digital Video Interface With Bi-Directional Half-Duplex Clock Channel Used As Auxiliary Data Channel	Issued	Silicon Image, Inc.
11/865,621	7,916,780	United States	Adaptive Equalizer For Use With Clock And Data Recovery Circuit Of Serial Communication Link	Issued	Silicon Image, Inc.
12/222,745	7,737,802	United States	Passive Equalizer With Negative Impedance To Increase A Gain	Issued	Silicon Image, Inc.
12/636,063	8,680,712	United States	Power Delivery Over Digital Interactive Interface For Video And Audio (DIIVA)	Issued	Silicon Image, Inc.
13/521,739		United States	Multi-Media USB Data Transfer Over Digital Interaction Interface for Video and Audio (DIIVA)	Pending	Silicon Image, Inc.
13/521,762		United States	Video Management And Control In Home Multimedia Network	Pending	Silicon Image, Inc.
14/381,186		United States	Linear Regulator with Improved Power Supply Ripple Rejection	Pending	Silicon Image, Inc.
13/844,152		United States	Electronic Alignment Of Optical Signals	Pending	Silicon Image, Inc.
14/391,382		United States	Frequency Response Compensation in a Digital to Analog Converter	Pending	Silicon Image, Inc.
14/165,340		United States	Apparatus, System and	Pending	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Method for Providing Switching with a T-Coil Circuit		Inc.
13/836,895	8,928,411	United States	Integration Of Signal Sampling Within Transistor Amplifier Stage	Issued	Silicon Image, Inc.
14/165,345		United States	Apparatus, Method and System for Asymmetric Full-Duplex Communication	Pending	Silicon Image, Inc.
14/209,785		United States	Method And Apparatus For Implementing Wide Data Range And Wide Common-Mode Receivers	Pending	Silicon Image, Inc.
14/296,377		United States	Transmitting Apparatus with Source Termination	Pending	Silicon Image, Inc.
14/368,781		United States	Caching of Capabilities Information of Counterpart Device for Efficient Handshaking Operation	Pending	Silicon Image, Inc.
14/163,981		United States	Mechanism for Facilitating Dynamic Counter Synchronization and Packetization in High-Definition Multimedia Interface and Mobile High-Definition Link	Pending	Silicon Image, Inc.
14/253,808		United States	Communication of Multimedia Data Streams Over Multiple Communication Lanes	Pending	Silicon Image, Inc.
14/279,316		United States	HDCP2.2 Authentication Engine and Stream Cipher Engine Sharing in Digital Content Protection Architectures	Pending	Silicon Image, Inc.
14/383,865		United States	Techniques for Fractional-N Phase Locked Loops	Pending	Silicon Image, Inc.
61/949,901		United States	Compressed Video Transfer Over HDMI and MHL	Pending	Silicon Image, Inc.
14/563,797		United States	Electrical Duplex to Optical Conversion	Pending	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/470,750		United States	Arbitration Signaling within a Multimedia High Definition Link (MHL 3) Device	Pending	Silicon Image, Inc.
14/275,692		United States	Error Detection and Mitigation in Video Channels	Pending	Silicon Image, Inc.
14/339,393		United States	Phase-Modulated On-Off Keying for Millimeter Wave Spectrum Control	Pending	Silicon Image, Inc.
14/145,715		United States	Messaging to Provide Data Link Integrity	Pending	Silicon Image, Inc.
14/145,736	8,854,548	United States	Mechanism for Memory Reduction in Picture-In-Picture Video Generation	Issued	Silicon Image, Inc.
14/470,613		United States	Compressed Video Transfer Over a Multimedia Link	Pending	Silicon Image, Inc.
14/184,647		United States	Video Frame Synchronization	Pending	Silicon Image, Inc.
14/181,446		United States	Power Delivery Over Digital Interaction Interface for Video and Audio (DiiVA)	Pending	Silicon Image, Inc.
14/470,804		United States	Phase Relationship Control for Control Channel of a Multimedia Communication Link	Pending	Silicon Image, Inc.
14/470,809		United States	Retry Disparity for Control Channel of a Multimedia Communication Link	Pending	Silicon Image, Inc.
61/943,267		United States	Pre-Processor and Post-Processor for Compression of 4:2:0 Encoded Video Streams with Video Compression Codecs Embedded within an Audio/Video Standard	Pending	Silicon Image, Inc.
14/278,255		United States	Encoding Guard Band Data for Transmission Via a Communications Interface Utilizing Transition-Minimized Differential Signaling (Tmds) Coding	Pending	Silicon Image, Inc.
14/322,753		United States	Calibration Of Single-Ended	Pending	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			High-Speed Interfaces		Inc.
61/947,704		United States	Reversible Connector	Pending	Silicon Image, Inc.
14/460,737		United States	System and Method for Transcoding Data	Pending	Silicon Image, Inc.
14/502,928		United States	Electrical Connector with Optical Channel	Pending	Silicon Image, Inc.
14/322,753		United States	Cable with Circuitry for Communicating Performance Information	Pending	Silicon Image, Inc.
61/973,837		United States	Error Correction for Transmission of Compressed Video Data Over Standards-Defined Coded Audio/Video Links	Pending	Silicon Image, Inc.
61/975,517		United States	(MHL) Connector Cable Detect, Cable Orientation Detect and/or Lane Re-Mapping	Pending	Silicon Image, Inc.
61/979,477		United States	MHL3 Router without HDCP2.2 Decryption and Encryption Operation	Pending	Silicon Image, Inc.
61/979,483		United States	TDD over 5-Pin Interface	Pending	Silicon Image, Inc.
14/470,620		United States	Compressed Blanking Period Transfer Over a Multimedia Link	Pending	Silicon Image, Inc.
14/273,400		United States	Transmission and Detection of Multi-Channel Signals in Reduced Channel Format	Pending	Silicon Image, Inc.
61/989,409		United States	System for Dynamic Capabilities, Status, and Metadata Exchange	Pending	Silicon Image, Inc.
14/300,166		United States	Configurable Multi-Dimensional Driver and Receiver	Pending	Silicon Image, Inc.
14/483,013		United States	Enhanced Communication Link Using Synchronization Signal as Link Command	Pending	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
62/043,218		United States	Run Length Programmable Unified Built-In Self-Test (BIST) Scheme for Various High-Speed Serial IO Standards	Pending	Silicon Image, Inc.
14/559,523		United States	Determination of Physical Connectivity Status of Devices Based on Electrical Measurement	Pending	Silicon Image, Inc.
14/516,136		United States	Method and System for Improving Serial Port Memory Communication Latency and Reliability	Pending	Silicon Image, Inc.
62/061,630		United States	Secure Control Communication Between an Application Processor and a Transmitter	Pending	Silicon Image, Inc.
62/075,554		United States	Metadata Transfer for HDMI/MHL	Pending	Silicon Image, Inc.
14/570,817		United States	Mechanism for Facilitating Dynamic Phase Detection with High Jitter Tolerance for Images of Media Streams	Pending	Silicon Image, Inc.
14/589,889		United States	Displaying Multiple Videos on Sink Device Using Display Information of Source Device	Pending	Silicon Image, Inc.
14/589,925		United States	Lower Power Operations in a Wireless Tunneling Transceiver	Pending	Silicon Image, Inc.
14/591,845		United States	Simultaneous Transmission of Clock and Bidirectional Data Over a Communication Channel	Pending	Silicon Image, Inc.
14/449095	20150036756	United States	Radio Frequency Interference Reduction In Multimedia Interfaces	Pending	Silicon Image, Inc.

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