# United States Patent [19]

**Dieterich**

[11] **4,308,557**

[45] **Dec. 29, 1981**


[54] **VIDEO DISC SYSTEM**


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[73] Assignee: **RCA Corporation**, New York, N.Y.



[21] Appl. No.: **84,393**

[22] Filed: **Oct. 12, 1979**

[51] **Int. Cl.**[3] ..... **H04N 5/76**; G11C 29/00; G06F 11/10; G11B 15/18

[52] **U.S. Cl.** ..... **358/128.5**; 371/38; 371/40; 360/72.2; 360/33; 369/47; 369/53; 369/221

[58] **Field of Search** ..... 371/38, 40; 358/128.5, 358/128.6; 360/72.2, 75, 77, 78, 33; 179/100.3 V; 369/47, 53, 221



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The Problem of Automatic Correction of Grouped Errors on Magnetic Tape Lapin—Problemy Peredachi Informatsii, vol. 4, No. 1, pp. 28–34/1968.



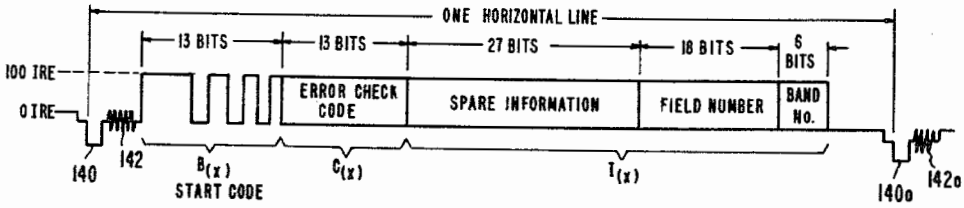
*Primary Examiner*—Aristotelis M. Psitos
*Attorney, Agent, or Firm*—E. M. Whitacre; J. S. Tripoli; E. P. Herrmann



[57] **ABSTRACT**

In a video disc recording and playback system, the video fields on the disc are identified by digital information recorded during the vertical blanking interval. The recorded digital information includes in the order named, a Barker start code sequence, an error detection coset code and information bits which include a field number corresponding to the video field being recorded. The arrangement results in improved noise immunity and simpler decoding hardware in the video disc player. The digital information is utilized to control a number of functions during the playing of a video disc record such as the calculation and display of elapsed playing time, lifting the stylus at the end of the program, and the detection and correction of locked groove conditions.


**24 Claims, 11 Drawing Figures**



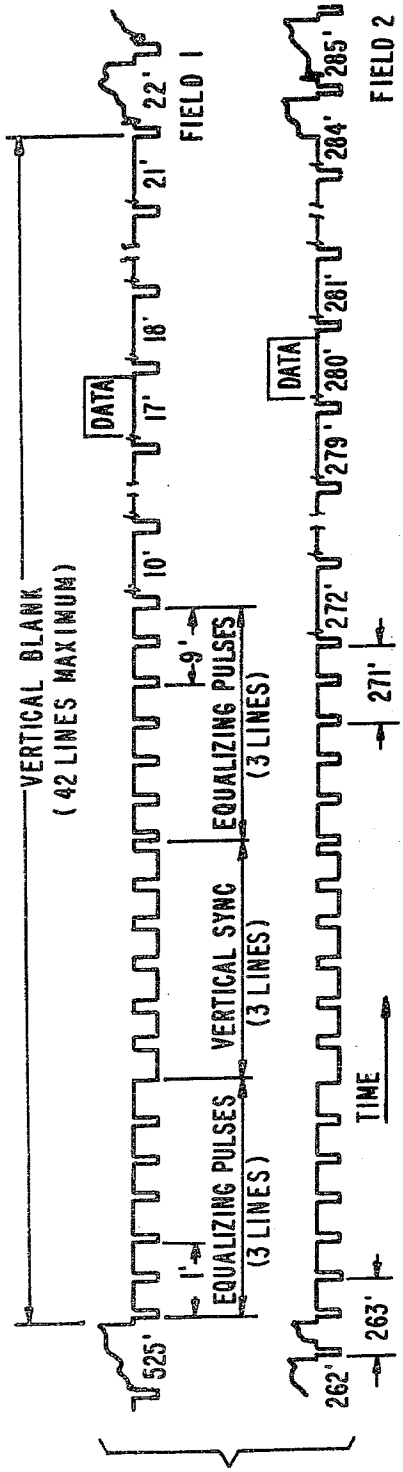

VERTICAL BLANK
(42 LINES MAXIMUM)
FIELD 1
FIELD 2
DATA
DATA
EQUALIZING PULSES
(3 LINES)
VERTICAL SYNC
(3 LINES)
EQUALIZING PULSES
(3 LINES)
TIME
525'
1'
9'
10'
17'
18'
21'
22'
262'
263'
271'
272'
279'
280'
281'
284'
285'

Fig. 1.

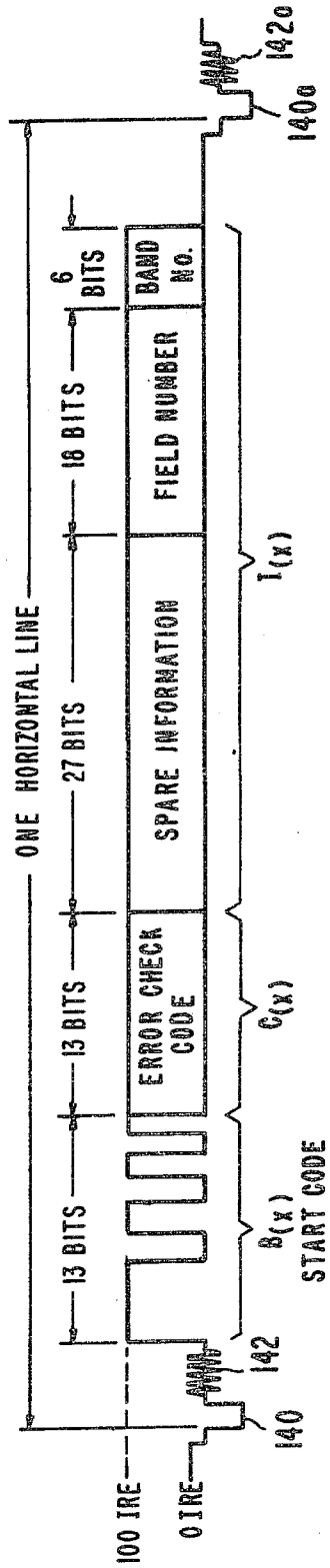

ONE HORIZONTAL LINE
13 BITS
13 BITS
27 BITS
18 BITS
6 BITS
ERROR CHECK CODE
SPARE INFORMATION
FIELD NUMBER
BAND No.
B(x)
START CODE
C(x)
I(x)
100 IRE
0 IRE
140
142
140a
142a

Fig. 2.

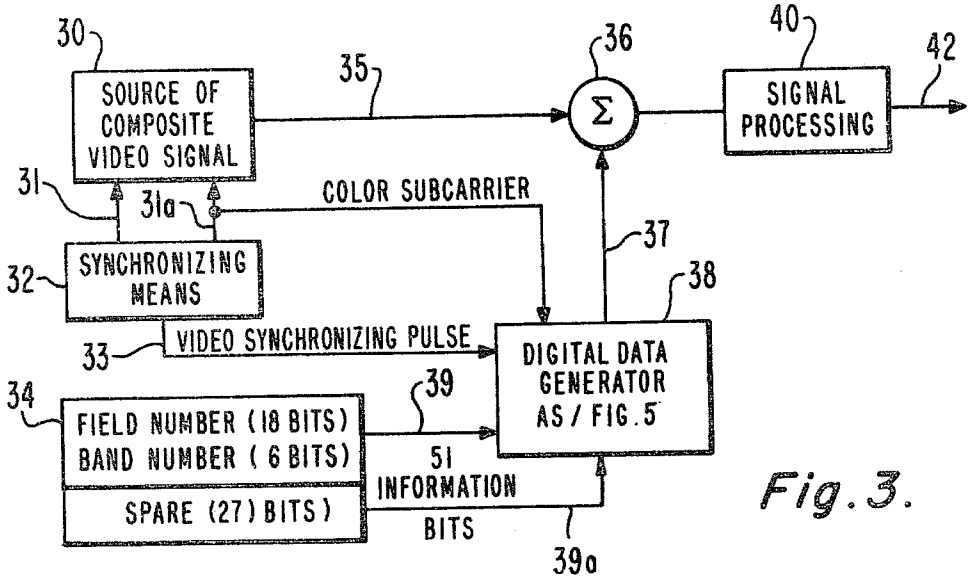

30
SOURCE OF COMPOSITE VIDEO SIGNAL
35
36
Σ
40
SIGNAL PROCESSING
42
31
31a
COLOR SUBCARRIER
37
32
SYNCHRONIZING MEANS
38
33
VIDEO SYNCHRONIZING PULSE
DIGITAL DATA GENERATOR AS / FIG. 5
34
FIELD NUMBER (18 BITS)
BAND NUMBER (6 BITS)
39
51
INFORMATION
SPARE (27) BITS)
BITS
39a

Fig. 3.

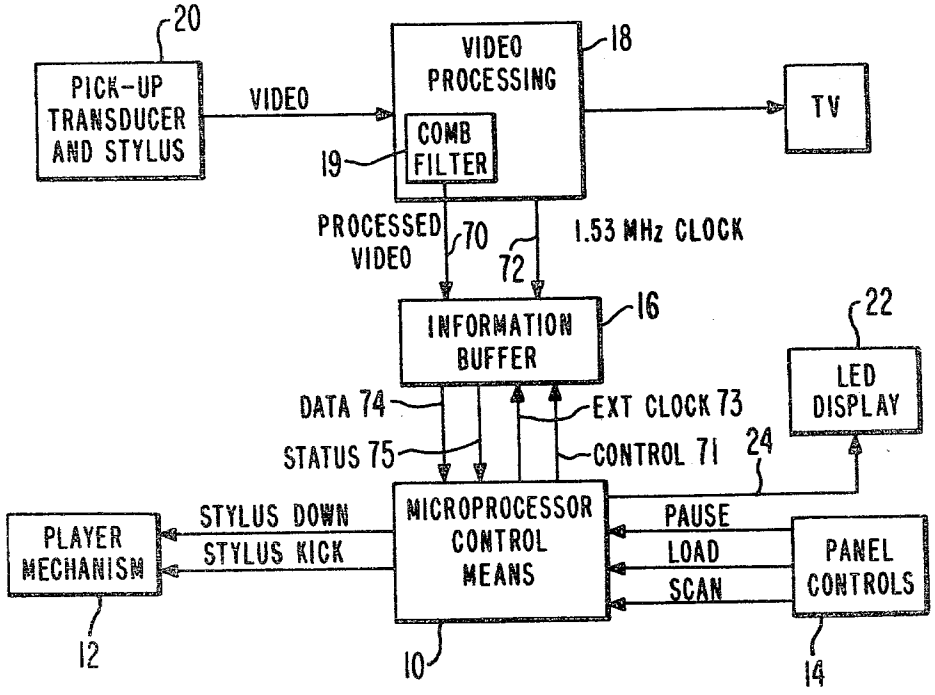

20
PICK-UP TRANSDUCER AND STYLUS
VIDEO
VIDEO PROCESSING
18
COMB FILTER
19
TV
PROCESSED VIDEO
70
72
1.53 MHz CLOCK
INFORMATION BUFFER
16
22
LED DISPLAY
DATA 74
EXT CLOCK 73
STATUS 75
CONTROL 71
24
PLAYER MECHANISM
STYLUS DOWN
STYLUS KICK
MICROPROCESSOR CONTROL MEANS
PAUSE
LOAD
SCAN
PANEL CONTROLS
12
10
14

Fig. 4.

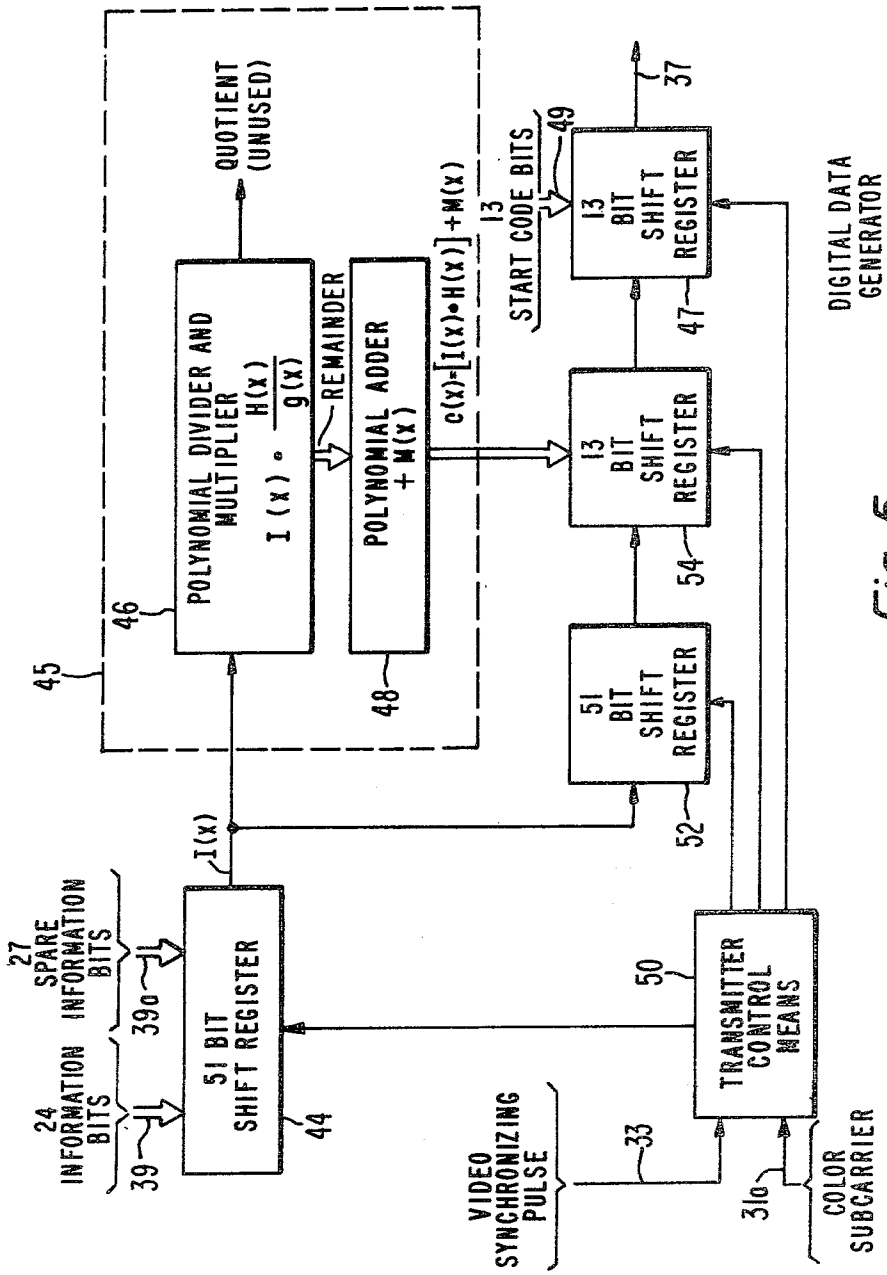

QUOTIENT (UNUSED)
POLYNOMIAL DIVIDER AND MULTIPLIER
I(x) • H(x)/g(x)
REMAINDER
POLYNOMIAL ADDER + M(x)
c(x)=[I(x)•H(x)]+M(x)
13 START CODE BITS
49
13 BIT SHIFT REGISTER
37
47
DIGITAL DATA GENERATOR
13 BIT SHIFT REGISTER
54
51 BIT SHIFT REGISTER
52
45
46
48
I(x)
27 SPARE INFORMATION BITS
39o
24 INFORMATION BITS
39
51 BIT SHIFT REGISTER
44
50
TRANSMITTER CONTROL MEANS
VIDEO SYNCHRONIZING PULSE
33
31o
COLOR SUBCARRIER

Fig. 5.

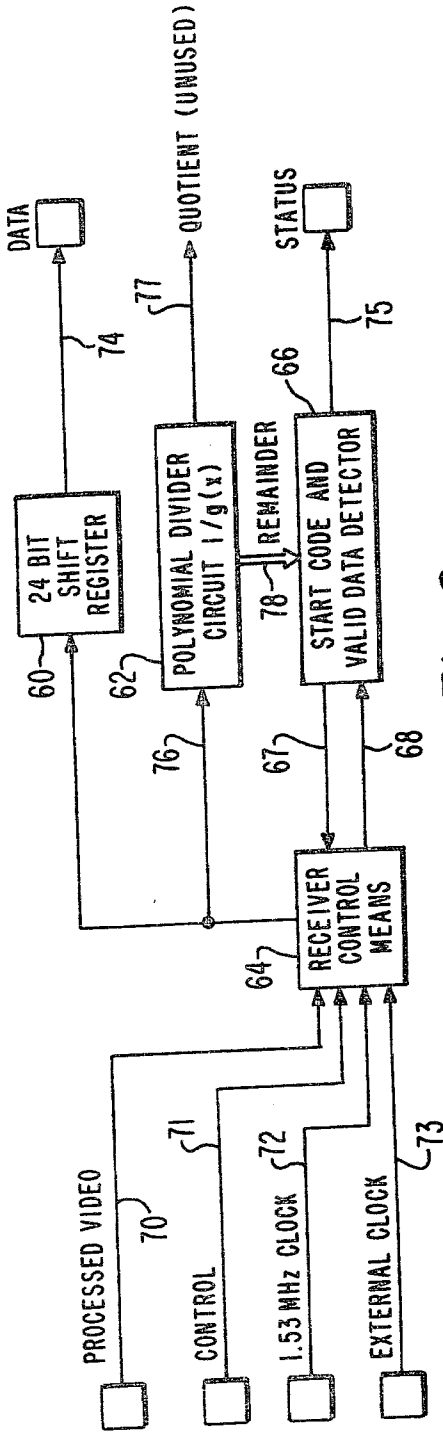

DATA
QUOTIENT (UNUSED)
STATUS
24 BIT SHIFT REGISTER
POLYNOMIAL DIVIDER CIRCUIT 1/g(x)
REMAINDER
START CODE AND VALID DATA DETECTOR
RECEIVER CONTROL MEANS
PROCESSED VIDEO
CONTROL
1.53 MHz CLOCK
EXTERNAL CLOCK
60
62
64
66
67
68
70
71
72
73
74
75
76
77
78

Fig. 6.

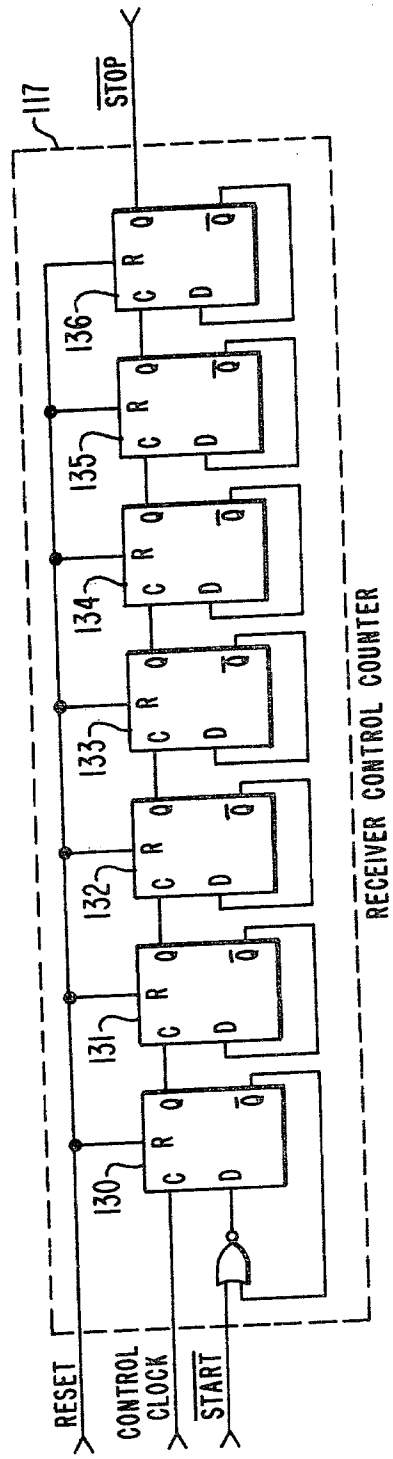

STOP
RESET
CONTROL CLOCK
START
RECEIVER CONTROL COUNTER
117
130
131
132
133
134
135
136

Fig. 9.

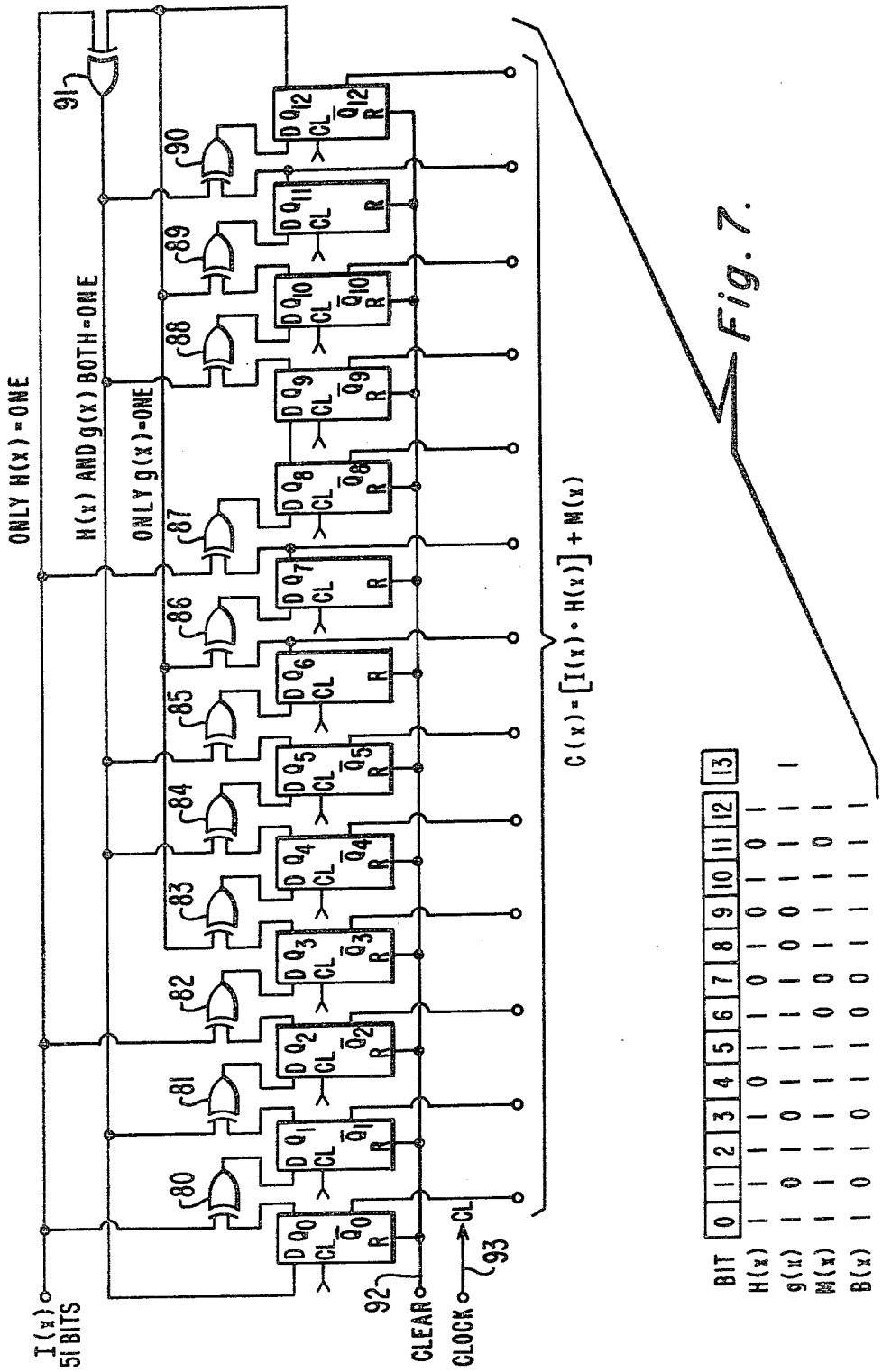

ONLY H(x)=ONE
H(x) AND g(x) BOTH=ONE
ONLY g(x)=ONE
I(x)
51 BITS
CLEAR
CLOCK
CL
C(x)=[I(x)•H(x)]+M(x)
BIT
H(x)
g(x)
M(x)
B(x)

Fig. 7.

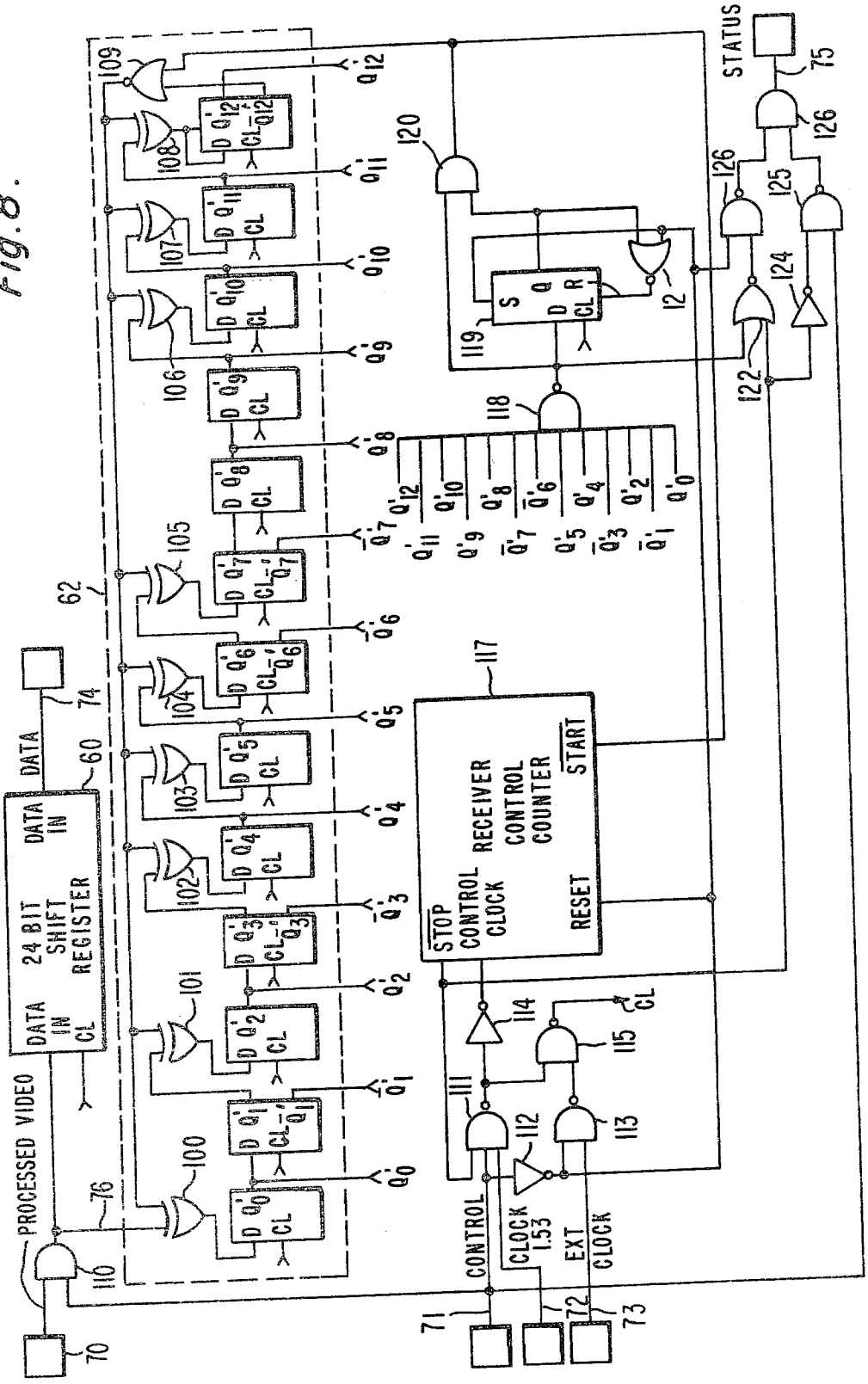

24 BIT SHIFT REGISTER
DATA IN
CL
DATA
DATA IN
RECEIVER CONTROL COUNTER
START
STOP
CONTROL
CLOCK
RESET
PROCESSED VIDEO
CONTROL
CLOCK 1.53
EXT CLOCK
STATUS
CL

Fig. 8.

STATE DIAGRAM

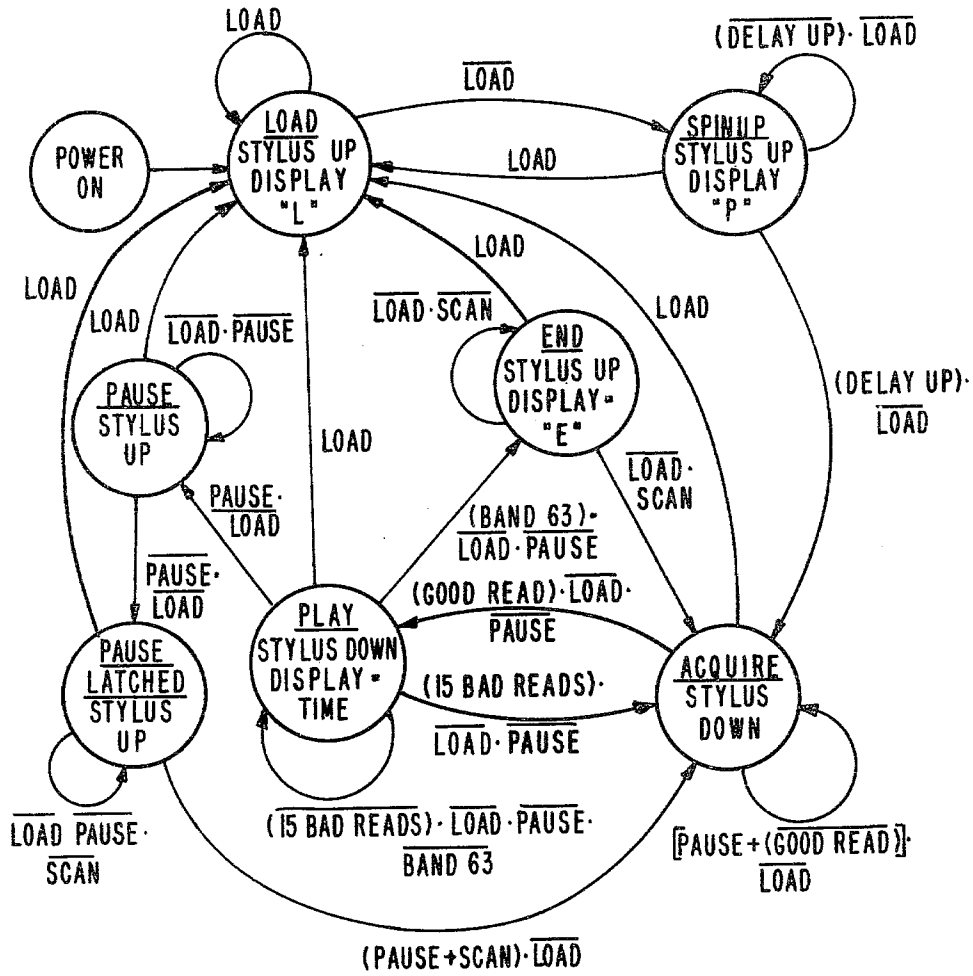



*Fig. 10.*

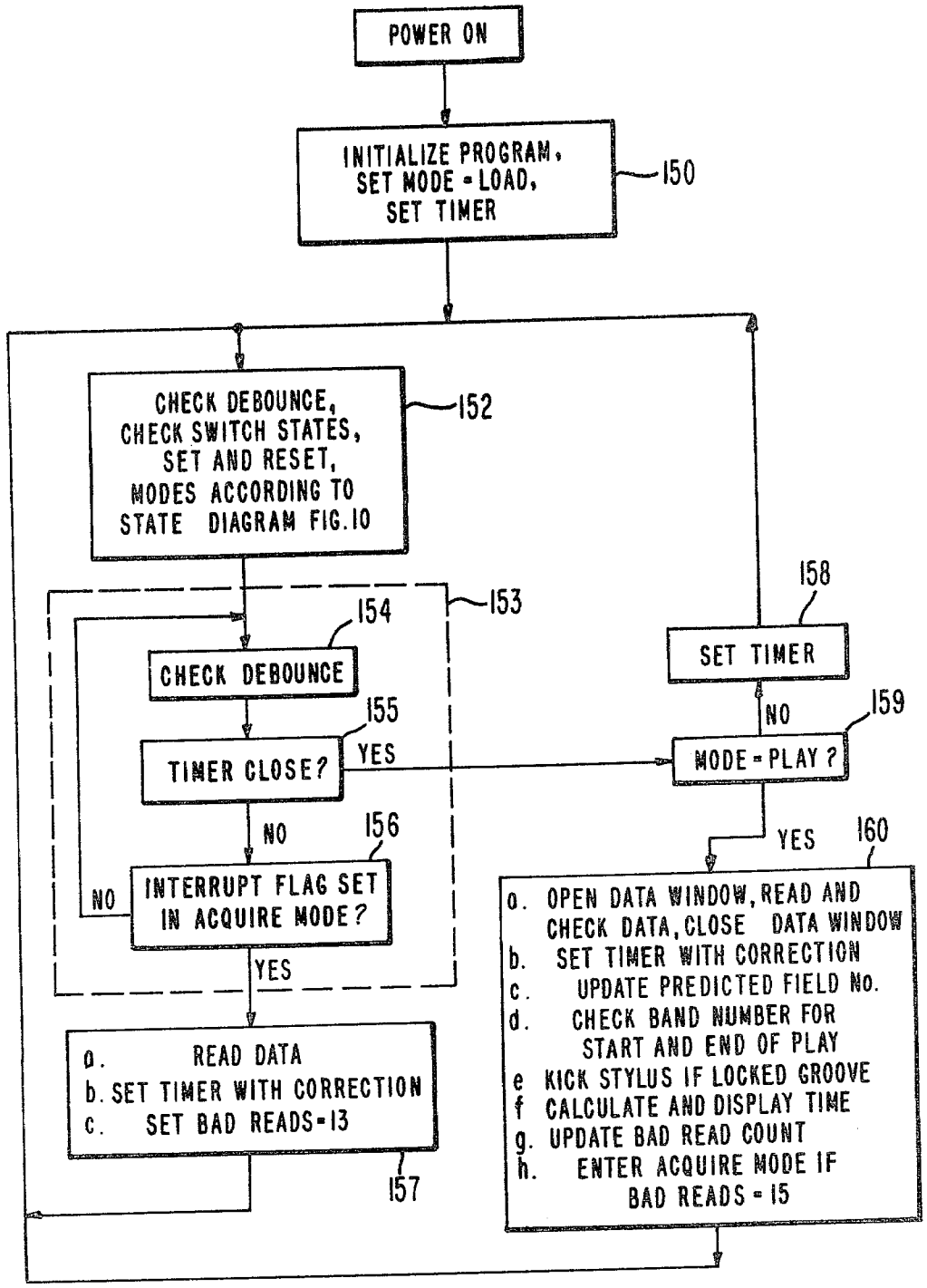

POWER ON
INITIALIZE PROGRAM, SET MODE = LOAD, SET TIMER
150
CHECK DEBOUNCE, CHECK SWITCH STATES, SET AND RESET, MODES ACCORDING TO STATE DIAGRAM FIG.10
152
153
154
CHECK DEBOUNCE
155
TIMER CLOSE?
YES
NO
156
INTERRUPT FLAG SET IN ACQUIRE MODE?
NO
YES
a. READ DATA
b. SET TIMER WITH CORRECTION
c. SET BAD READS = 13
157
158
SET TIMER
NO
159
MODE = PLAY ?
YES
160
a. OPEN DATA WINDOW, READ AND CHECK DATA, CLOSE DATA WINDOW
b. SET TIMER WITH CORRECTION
c. UPDATE PREDICTED FIELD No.
d. CHECK BAND NUMBER FOR START AND END OF PLAY
e KICK STYLUS IF LOCKED GROOVE
f CALCULATE AND DISPLAY TIME
g. UPDATE BAD READ COUNT
h. ENTER ACQUIRE MODE IF BAD READS = 15

*Fig. 11.*

## VIDEO DISC SYSTEM

This invention relates to video disc systems, and more particularly to video disc systems in which groove or field identification numbers are included in a blanking interval of the video signal recorded on the disc.

In order to implement certain features in a video disc player, it is desirable to record digital information signals along with the video signal. See copending patent applications "TRACK ERROR CORRECTION SYSTEM, AS FOR VIDEO DISC PLAYER" by J. Rustman and M. Mindel and "IMPROVED DIGITAL ON VIDEO RECORDING AND PLAYBACK SYSTEM" by C. Dieterich and T. Christopher, both filed concurrently herewith and assigned to the assignee of the present invention.

In a system for encoding digital data on a video disc medium, previously known to the present inventor, the digital format includes a start bit, followed by information bits, followed by a group error code. The information bits include a groove identification number to indicate the position of a playback stylus on the video disc. The complete digital message is encoded on the video signal during one line of the vertical blanking interval.

In the known system, in order to decode such recorded digital data in the player, the line in the vertical blanking interval containing data is gated to a decoding circuit. After sensing the start bit, the decoder clocks each successive bit into a data register and checks the received group error code for received errors, if any. A group error code, after decoding, has a particular error check result (herein referred to as a remainder), equal to zero when beginning with zero in the decoder, assuming no errors are detected.

The above-described data system can be disrupted by any of several types of noise-induced errors. These errors include framing errors, where the received message is shifted one or more bits away from its proper position, and error code failures, where the error code check indicates validity in the presence of noise-induced errors. These noise induced errors as well as certain other disadvantages of the above-described data system can be diminished by the use of an improved method for encoding the digital data.

The method for encoding digital data in accordance with the present invention includes generating a start code at the beginning of each digital message, generating a coset error code following the start code, and generating information bits at the end of each digital message. A Barker sequence is generated as the start code to improve self-synchronization and reduce framing errors.

A coset error code is similar to a group error code except that either the remainder after decoding, or the beginning contents of the remainder register before decoding, or both, is non-zero. In other words, the situation which is avoided by using a coset code is one where all zeros appear as a valid error-free message.

Use of an error code with a non-zero remainder results in a lower rate of undetected errors than would be the case for a group code with a zero remainder. This result is believed to be due to the particular nature of a video signal and the way in which the digital information is recorded thereon. The decoder searches for a digital message during the vertical blanking interval where the transmitted lines are at black level (logical zero). During this time, logical zeros are more likely to



occur than ones. Therefore, noting that the remainder of zero is zero (after decoding), noise is more likely to cause a zero remainder than any other non-zero remainder. For example, in the previous system described, if a noise burst occurs equal to the start code followed by a black level (all zeros) then a zero remainder would result. The present data system, wherein the decoding process begins with a non-zero number and/or ends with a non-zero number, is not subject to such errors.

Placing the information bits at the end of the message is advantageous in that it facilitates a simpler decoder in the video disc playback apparatus, which embodies another aspect of the present invention. As will become clear in the following description of a preferred playback apparatus embodying this aspect of the invention, the receiver control means in the decoder need not distinguish between the error code bits and the information bits, but need only generate a simple time interval after detection of the start code to the end of the message. Such simplified control is achieved without otherwise increasing the data storage elements or other portions of the decoder apparatus.

IN THE DRAWING:

FIG. **1** is a graphical representation of a television signal including the vertical blanking interval between odd and even fields;

FIG. **2** is a graphical representation of the digital data format used in the recording method of the present invention;

FIG. **3** is a block diagram of a video disc encoder in accordance with the present invention;

FIG. **4** is a block diagram of a video disc player embodying the present invention;

FIG. **5** is a block diagram showing more detail of the digital data generator of the video disc encoder of FIG. **3**;

FIG. **6** is a block diagram showing more detail of the information buffer for the video disc player of FIG. **4**;

FIG. **7** is a schematic diagram of a means for generating an error check code from the information bits for the video disc encoder of FIG. **5**;

FIG. **8** is a schematic diagram, shown partially in block form, of the information buffer for the video disc player of FIG. **4**;

FIG. **9** is an embodiment of a receiver control counter for the information buffer shown in FIG. **8**;

FIG. **10** is a state transition diagram for the microprocessor control means of FIG. **4**; and

FIG. **11** is a flow chart representing a program algorithm for the microprocessor control means of FIG. **4**.

## SIGNAL FORMAT

Particular details of an NTSC type television signal formatted in accordance with the buried subcarrier technique as described in U.S. Pat. No. 3,872,498, "Color information translating systems," to D. Pritchard, are shown in FIG. **1**. A vertical blanking interval separates the interlaced odd and even fields. Those skilled in the television arts will readily recognize the standard vertical blanking interval containing a first equalizing pulse interval, a vertical sync interval, a second equalizing pulse interval, followed by a number of horizontal line intervals at the start of each new field. As shown in FIG. **1**, the video signal information begins on line **22'** of field **1**, and on line **284'** of field **2**.

The digital information representative of the field number appears at line **17'** of field **1**, and line **280'** of field **2**. Digital information could, as well, be inserted in

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other lines of the vertical blanking interval. To show the details of the digital signal format, FIG. **2** expands the time scale during the horizontal line containing data (line **17'** or line **280'**).

Data are represented in terms of luminance level: **100** IRE units is a logical "one" and **0** IRE units (blank) is a logical "zero". The first data bit follows the standard horizontal sync pulse **140** and color burst **142**. The frequency of the burst **142** is about 1.53 MHz, the frequency of the buried subcarrier. Each data bit is transmitted synchronously with the 1.53 MHz buried subcarrier signal. As shown in FIG. **2**, the digital message comprises a 13-bit start code termed B(x), a 13-bit redundant error check code termed C(x), and 51 information bits termed I(x). The beginning of the next horizontal line is indicated by the next horizontal sync pulse **140***a* and color burst **142***a*. Thus, the individual data bits are synchronous with the color subcarrier, and the overall digital message is synchronous with the vertical sync pulse. Note that the data rate can be a multiple or submultiple of any convenient subcarrier frequency. Also, other values of luminance may be assigned to logic one and zero, or more than one bit may be associated with a given luminance level.

A start code is used in the present system to synchronize the data system to the digital message thereby avoiding the need to detect the edge of horizontal or vertical sync. Synchronizing errors in a serial digital data system result in framing errors, i.e. where received data is shifted by one or more bits from its proper position. Previously known systems for recording digital data on a video disc encoded signal have shown that the edges of sync signals are not reliable as a time reference and have resulted in framing errors. Start codes have proven to be more reliable.

The specific start code chosen, 1111100110101, is one of the Barker codes known in radar and sonar technology. See "Group Synchronization of Binary Digital Systems", by R. H. Barker, published 1953 by Academic Press, New York, N.Y. Barker codes are designed such that the auto-correlation function, of a signal containing a Barker code shifted with respect to itself, is maximized when coincidence occurs, and minimized elsewhere. That is, if one assigns a value of +1 or −1 to each bit in the start code and computes the sum of the respective bit products for each shifted position of the start code with respect to itself, such auto-correlation function will produce a sharp maximum when coincidence occurs. Specifically, a Barker code shifted any odd number of places with respect to itself produces an auto-correlation of 0. A Barker code shifted any even number of places with respect to itself produces an auto-correlation of −1. However, when there is coincidence, the auto-correlation is N, where N is the number of bits in the Barker code. In other words, a Barker code shifted any number of places with respect to itself differs in a maximum number of bit positions. In the presence of noise, this characteristic reduces the probability of a false start code detection, as compared to an arbitrarily chosen start code.

The information bits, I(x), include a field number, a band number, and spare information bits for future expansion. Field numbers identify each field of the video signal by a unique 18-bit binary number. At the beginning of the video disc, the first field of the video program is field "zero". Thereafter, each field is consecutively numbered in ascending order. Band numbers refer to recorded video signal in a group of adjacent convolutions of the spiral grooves which form a band-like shape. All of the material in such band of grooves is identified by having a common band number. As an example of band number utility, the video signal after the end of the video program material is recorded having band number "sixty-three". The video disc player senses band sixty-three as the end of program and responds by lifting the stylus from the record.

The error check code C(x) is computed from I(x) in the video disc recording apparatus. To this end, I(x) is multiplied by a constant, H(x). The resulting product is divided by another constant g(x). After such division, the remainder (the quotient is unused) is added to a third constant M(x). The result is C(x).

In the video disc player, the received message is checked for errors by dividing the entire message, including the start code, by the constant g(x) mentioned above. If the remainder is equal to the start code, B(x), then the message is considered error free. The constants H(x) and M(x) are chosen so that the remainder of the entire message will in fact be the start code. The constant g(x), used in both the video disc recording apparatus and the video disc player is called the generator polynomial of the code. A specific g(x) is chosen which generates a code having error detection properties particularly advantageous as applied to the video disc medium. In the system described herein, the addition, multiplication, and division operations referred to above are performed according to special rules to accomodate the hardware available for carrying them out. The error coding will be discussed in greater detail hereinafter in conjunction with the encoding and decoding hardware.

A block diagram of a video disc encoder is shown in FIG. **3**. A composite video signal from source **30** is linearly combined in adder **36** with a digital data bit stream on conductor **37** supplied by the digital data generator **38**. Synchronizing means **32** supplies a color subcarrier and synchronizing pulses so that the data bits generated by the digital data generator **38** are synchronous with the color subcarrier appearing at terminal **31***a* and so that the digital message is encoded on the proper horizontal line in the vertical blanking interval. Information bits, appearing at data bus **39** and representing the video field number and band number, are provided by apparatus **34**. The use of field number and band number information will be discussed in conjunction with the microprocessor program (FIGS. **10** and **11**). The digital data and the video signal are combined in the adder **36**. Further signal processing means **40** conditions the composite video for the recording medium. The composite video signal is of the buried subcarrier type and is recorded using FM modulation techniques.

In the video disc player of FIG. **4**, the FM signal is detected using pickup transducer and stylus assembly **20** and converted in video processing circuitry **18** to a standard television signal for viewing on an ordinary television receiver. Video processing circuitry **18** includes means responsive to the color burst signal to phase lock a 1.53 MHz local color oscillator to the color subcarrier. The color oscillator, in addition to its usual use for demodulating the buried subcarrier wave, is also used to provide the digital clock signal and this signal appears on conductor **72**. The video processing circuitry **18** further includes means for demodulating the video carrier and comb filtering the recovered video signal. Comb filter **19** subtracts two adjacent field lines, which result appears on conductor **70** as processed video. Since line **16'**, which is at the black level, is sub-

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tracted from line 17', which is modulated with digital data, the processed video on conductor 70 is the recovered digital data. Naturally, line 16' may be any constant luminance level. Note that if the subsequent line 18' to the data line 17' is a constant luminance line (also black) the subsequent output of the comb filter during line 18' is again recovered digital data, but the data is inverted. By subtracting one line from a constant luminance adjacent line, the recovered digital signal is self-referenced, thereby eliminating data errors due to shifts in the d-c level of the video signal. If it were desired to place data on consecutive lines, as compared to placing data adjacent to constant luminance lines, then means for referencing the video signal to a predetermined luminance level, or a d-c reference level would be necessary in order to separate the digital data stream from the video signal.

As shown in FIG. 4, the information buffer 16 is responsive to processed video on conductor 70 and the 1.53 MHz clock signal on conductor 72 to extract digital data from the video signal. The buffer 16 is controlled by a digital binary control signal on conductor 71 from the microprocessor 10. In one binary state, the control signal on conductor 71 causes the information buffer 16 to acquire data. In the other binary state, the control signal on conductor 71 conditions the information buffer 16 to transfer the received data to the microprocessor 10. In particular, when the control signal on conductor 71 is high, the information buffer 16 opens to sample incoming data on the processed video signal conductor 70 using the 1.53 MHz signal on conductor 72 as a clock. After a complete message is received, the status signal on conductor 75 furnishes an indication that a message is complete. To transfer the message to the microprocessor memory, the control signal on conductor 71 is set low. This action closes the information buffer 16, resets the internal control circuits, and gates the results of the message error code check onto status conductor 75. If the status signal indicates the message is valid (i.e. error code check indicates validity), the microprocessor 10 is programmed to transfer the data in the information buffer 16 to the microprocessor 10. The microprocessor supplies an external clock signal on conductor 73 to transfer data from the information buffer 16. For each clock pulse, one bit of data on conductor 74 is shifted out of the information buffer and into the microprocessor 10. When all the data is transferred to the microprocessor 10, and the program is ready for another digital message, control conductor 71 is again returned to a high state and the process is repeated.

The microprocessor 10, via the information buffer 16, controls the gating of line 17' (or line 280') out of the video signal. The first digital message is obtained by continuously searching the video signal for a start code. Thereafter, the information buffer 16 is closed. Then, based on the time of arrival of the first digital message, the information buffer is opened approximately six lines before the next digital message is expected. If no valid message is found, the information buffer 16 is closed approximately six lines after such expected time of arrival. If a valid digital message is found, the information buffer 16 is closed and a new time of arrival for the next digital message is calculated based on the time of arrival of the current digital message. In such manner, the microprocessor 10 opens a gate, or "data window", approximately twelve lines wide and centered about the expected data. The time interval from the center of one data window to the next is approximately one video field time interval. The width of the data window is chosen so that under worst case timing conditions the expected data will fall within the data window. Sources of timing error, as explained below, are: finite resolution of the digital timer; the drift rate of the timer; program uncertainty in determining time of arrival of present data; and timing differences between odd and even interlaced fields. Use of a alternate microprocessor and/or timer may be accommodated by adjusting the data window width accordingly. The microprocessor program which controls the logic for searching for data and centering the data window is discussed hereinafter in conjunction with FIGS. 10 and 11.

The microprocessor 10 is also responsive to the player panel controls 14 (load, pause, and scan) to operate the player mechanism 12 and drive the player display 22 in accordance with a predetermined program, as discussed hereinafter. The player mechanism is further provided with at least one stylus "kicker" operable by the microprocessor 10. A kicker is a means, piezoelectric, electromagnetic, or otherwise, for impulsively moving the signal pickup means to adjacent grooves or signal tracks on the video disc medium. The use of the kicker to break out of locked grooves will be discussed hereinafter in conjunction with the flow diagrams of FIGS. 10 and 11.

## ERROR CODE

As mentioned above, the video disc recording apparatus uses the information bits I(x) to compute C(x). Because of the large number of potential combinations—I(x) and C(x) together are 64 bits long—and the desire to determine the error detection and correction characteristics of a given code without resorting to enumeration, error codes are treated mathematically. A general mathematical development of ring theory and Galois Fields $GF(2^m)$, applicable to error codes in general, can be found in "Error Correcting Codes" by W. Wesley Peterson, published by MIT Press, Cambridge, Mass. For present purposes, the error coding in the video disc may be best understood in terms of a few simple definitions.

A digital message, comprising ones and zeros, can be considered as representing an algebraic polynominal comprising powers of x. The coefficients of the respective powers of x are the individual bits of the message. For example, the 4 bit message 1011, can be represented by the polynominal P(x), where

$$P(x) = 1 \cdot x^3 + 0 \cdot x^2 + 1 \cdot x + 1 \cdot X^0$$
$$= x^3 + x + 1$$

Applying this notation to the start code, 1111100110101, then

$$B(x)=x^{12}+x^{11}+x^{10}+x^9+x^8+x^5+x^4x^2+1$$

The highest power of x is called the degree of the polynominal. In the above example, B(x) is a polynominal of degree 12.

Polynominals may be added, subtracted, multiplied, and divided using the ordinary rules of algebra except for expressing coeficients in modulo 2 terms. A shorthand notation for the remainder of a polynominal after division by another polynominal is indicated by brackets. That is, if

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$$\frac{P(x)}{g(x)} = Q(x) + \frac{r(x)}{g(x)}$$

where the remainder, r(x), has a degree less than the divisor, g(x), then

$$[P(x)] = r(x)$$

In the video disc recording apparatus, the total message recorded on the video disc is represented by a polynominal, T(x). From FIG. 2,

$$T(x) = B(x)x^{64} + C(x)x^{51} + I(x) \quad (1)$$

The term $x^{64}$ shifts B(x) by 64 bits, because B(x) is at the beginning of the data format. Similarly, the term $x^{51}$ shifts C(x) 51 bits to represent that C(x) is recorded before I(x). In accordance with the apparatus being described, the recording apparatus computes a value for C(x) so that the total message, T(x), has a remainder equal to B(x) after being divided by g(x). That is, assuming C(x) to be of the form

$$C(x) = [I(x) \cdot H(x)] + M(x), \quad (2)$$

then H(x) and M(x) are constant polynominals chosen so that

$$[T(x)] = B(x) \quad (3)$$

It can be shown that equations (1), (2), and (3), when solved for the constant polynominals H(x) and M(x), yield

$$H(x) = [x^{127}]$$

$$M(x) = [B(x)x^{13} + B(x)x^{127}]$$

FIG. 7 includes a table enumerating the chosen values for B(x) and g(x), as well as the derived values for H(x) and M(x). Note that the table in FIG. 7 shows high order bits on the right, so that they are in the same order as the flip flop storage elements appear in the logic diagram of the same figure.

In the video disc player, the recorded digital message is read by the player electronics. The data recorded on the video disc is T(x). The data read by the player is R(x). If no errors are generated between recording and playback then $T(x) = R(x)$. The received message, R(x), is checked for errors by dividing R(x) by g(x). If the remainder is equal to B(x), the start code, then the message is considered error-free. On the other hand, if the remainder does not equal B(x), then an error is thereby indicated.

The characteristics of a code generated in the above manner depend on the choice of g(x), which is called the generator polynominal. The particular g(x) chosen for the video disc medium is one from the computer generated codes demonstrated by Tadao Kasami in "Optimum Shortened Cyclic Codes for Burst Error Correction" published in IEEE Transations on Information Theory 1963. A burst error in a digital system is a type of error where adjacent bits in the digital message are lost. Burst errors are considered a likely type of transmission error in the video disc medium. As shown by Kasami in the aforementioned reference, a code which can correct single burst errors of 6 bits or less, can be implemented using a generator polynominal given by

$$g(x) = x^{13} + x^{12} + x^{11} + x^{10} + x^7 + x^6 + x^5 + x^4 + x^2 + 1$$

Furthermore, it may be shown that for the g(x) given above, all single burst errors of 13 bits or less will be detected, and 99.988 percent of all single burst errors longer than 13 bits will be detected as well. The video disc player, as described herein, uses only the error detection capabilities of the chosen code.

As a specific example of error code generation, consider the case where the field number is 25,000, the band number is 17, and the spare bits are 0. Since, 25,000 in binary representation is 000 110 000 110 101 000, and 17 in binary representation is 010 001 (high order bits are on the left), the 51 information bits are 000 000 000 000 000 000 000 000 000 000 110 000 110 101 000 010 001. The order of trasmission is spare bits first, followed by field number, and then band number, wherein the most significant bit is transmitted first. The error code for the above specific I(x), computed as the remainder of I(x) times H(x), plus M(x), is represented by 0111100100010. The next video field is 25,001 or 000 110 000 110 101 001 in binary representation. For the corresponding information bits, 000 000 000 000 000 000 000 000 000 000 110 000 110 101 001 010 001, the proper error code is 1000101101110. The complete digital message for field 25,001 including the start code is therefore, 1111100110101 1000101101110 000 000 000 000 000 000 000 000 000 000 110 000 110 101 001, 010 001, shown in order of transmission. The start code is the first 13 bits, the error code is the next 13 bits, and the 51 information bits are last. In the video disc player, the above digital message is checked for errors by dividing the received message by g(x). If no errors are detected, the remainder is 1111100110101, which is exactly the start code.

## HARDWARE

A block diagram of a means for generating T(x) is shown in FIG. 5. Under the control of the transmitter control means **50**, 24 information bits are loaded via data bus **39**, and 27 spare information bits are loaded via data bus **39***a* into a 51 bit shift register **44**. I(x), which comprises these 51 bits, is then shifted into another 51 bit shift register **52**.

At the same time, during the 51 shift pulses, an encoder **45** computes C(x) in the following way. Polynominal dividing and multiplying means **46** is responsive to the 51 bit serial transmission of I(x) to compute the remainder of I(x) times H(x) divided by g(x). M(x) is then added in parallel in polynominal adder **48**. The resulting code C(x) is loaded into a 13-bit shift register **54**, and B(x), the start code, is loaded via data bus **49** into another 13 bit shift register **47**. Since the start code is a constant digital value, such loading is preferrably accomplished by fixed connections to the parallel load inputs of shift register **47** as opposed to a software implementation. In positive logic notation, the corresponding parallel inputs to shift register **47** are connected to ground potential wherever the start code has a zero, and to a positive potential wherever the start code has a one. Transmitter control means **50** controls the total message T(x), contained in the three shift registers **52**, **54**, **47**, being shifted out serially in synchronism with the color subcarrier on conductor **31***a*. A video synchronizing pulse applied on conductor **33** provides transmitter control means **50** with a time reference so

that the digital message is transmitted at the proper time with respect to the video signal.

A specific embodiment of the encoder (**45** of FIG. **5**) is shown in FIG. **7**. Clocked flip flops having output terminals $Q_0$ through $Q_{12}$ form a remainder register. Multiplication by H(x) and division by g(x) is performed simultaneously in bit serial fashion. Afterwards, the remainder is held in the remainder register outputs $Q_0$ through $Q_{12}$. See Chapter 7, pages 107–114 of the above-mentioned Peterson reference for a general treatment of such circuits. To appreciate the simplicity of the circuit in FIG. **7** for multiplying and dividing polynomials, it is noted that both addition and subtraction (of coefficients of terms of like power) is performed by an exclusive OR gate. Multiplication of I(x) by H(x) is performed by appropriate connections to one or more exclusive OR gates **80** through **91**. In particular, wherever a coefficient of H(x), but not g(x), is equal to 1, (bit positions **1**, **3**, and **8**) input I(x) is connected to an input of an exclusive OR gate **80**, **82**, and **87**, respectively. Division of I(x) by g(x) is performed by multiplying the output of $Q_{12}$ by g(x), and subtracting the resulting product from the contents of register $Q_0$ through $Q_{12}$. In particular, wherever a coefficient of g(x), but not H(x), is equal to 1, (bit positions **4**, **7** and **11**) the output of $Q_{12}$ is connected to an input of exclusive OR gate **83**, **86**, and **89**, respectively. Where H(x) and g(x) are both equal to 1 (bit positions **0**, **2**, **5**, **6**, **10** and **12**) the output of exclusive OR gate **91** is connected to an input of exclusive OR gates **81**, **84**, **85**, **88**, and **90**, respectively. After 51 clock pulses, one for each bit of I(x), the contents of register $Q_0$ through $Q_{12}$ is the remainder of I(x).H(x) after division by g(x).

Note how M(x) is added to the contents of the remainder register. Addition of coefficients is in modulo **2** arithmetic performed ad the exclusive OR function. Wherever M(x) has coefficients of +1, the complement output, $\bar{Q}$, of the corresponding flip flop is used; wherever M(x) has coefficients of 0, the uncomplemented output, Q, is used.

A block diagram of a means for decoding the received message, R(x), appears in FIG. **6**, which is an embodiment of the information buffer **16** of FIG. **4**, discussed above. Control signal on conductor **71**, an input, conditions the receiver decoder of FIG. **6** either to receive data from the video signal, or transfer data to the microprocessor.

In the receive state, each bit is simultaneously shifted into two separate registers. One such register **60** is for data, and the other **62** is for error checking. The error check register **62** is a polynomial divider. However, when acquiring new data, the divider feedback path is disabled so it functions as a straight shift register. The operation of divider register **62** will be discussed subsequently in greater detail in conjunction with FIG. **8**. For present purposes, register **62** is responsive to the receiver control means **64** to either shift in successive bits of R(x), or divide successive bits of R(x) by g(x). In either case, the contents of register **62** is available on data bus **78** and provided to the start code and valid data detector **66**.

The receive operation begins with register **62** conditioned to operate as a shift register. After B(x) is detected by detector **66**, control means **64** conditions register **62** to operate as a polynomial divider. Thus, polynomial division by g(x) begins with B(x) in the divider register **62**. The receiver control means **64** is further responsive to the detection of B(x) to time out a period equal to the remaining message bits (64 clock pulses). After the time out period, the divider **62** contains the remainder of R(x) modulo g(x), which should be B(x) if the message is valid. During the error check process, data register **60** has been shifting in data bits. At the end of the time out period, the data register **60** stores only the last 24 bits. However, since the 24 information bits are placed at the end of the message, register **60** will contain the assigned information bits. If it is desired to utilize the spare information bits, additional shift register stages may be added.

Interpretation of the output status signal on conductor **75** depends on the state of control signal on conductor **71**. When the control signal on conductor **71** conditions the receiver for acquiring data (receive state) the status signal on conductor **75** is defined as "message received". When the control signal on conductor **71** conditions the receiver for transferring data (transfer state), status signal conductor **75** indicates "data valid." The control signal on conductor **71** also resets the receiver control means **64** and gates the results of the remainder check onto the status signal on conductor **75**.

The received information is transferred out of shift register **60** in response to external clocks supplied by the microprocessor on conductor **73**. After the data is shifted out, the control signal on conductor **71** may be returned to its previous state which will again condition the receiver-decoder to continuously search for another start code.

FIG. **8** shows a logic diagram, partially in block form, of the receiver decoder of FIG. **6**. The flip flops having output terminals $Q_0'$ through $Q_{12}'$ form a remainder register. Polynomial division by g(x) is performed by multiplying successive register output terms from $Q_{12}'$ by g(x) and subtracting the product (via exclusive OR gates **100** through **108**) from the contents of the remainder register. A feedback connector from $\bar{Q}_{12}'$ (through NOR gate **109**) is made to an exclusive OR gate wherever g(x) has coefficients of 1, except for bit **13**. Since the coefficients of g(x) are 1 for bit positions **0**, **2**, **4**, **5**, **6**, **7**, **10**, **11**, **12**, an exclusive OR gate is placed at the data input of each respective flip flop of the remainder register as shown. NAND gate **118** detects B(x), which is both the start code and the valid error check code. The receiver control counter **117**, begins counting responsive to a start signal from AND gate **120**, counts 63 clock periods and supplies a stop signal which is used by NAND gate **111** to stop the clock to all decoder flip flops. A representative embodiment of the receiver control counter **117** is shown in FIG. **9** comprising seven flip flops **130** through **136**.

The sequence of operations in receiving data is as follows. When the control signal on conductor **71** is high, data is gated to divider **62** through AND gate **110**. Flip flop **119** has been previously set, which disables the feedback signals in divider **62** by blocking NOR gate **109**. Register **62** now functions as a shift register. Upon detecting B(x), the output of NAND gate **118** goes low, and the Q output of flip flop **119** goes low one clock period later. Therefore, feedback is enabled for polynomial division by the output of AND gate **120** via NOR gate **109** when B(x) is detected in the remainder register. After 63 clock periods, the receiver control counter **117** stops and the status signal on conductor **75** goes high, indicating "message received". Shift register **60** holds the last 24 bits of I(x). To transfer data, the control signal on conductor **71** is made low. The inverted output of NAND gate **118**, which is low if the remainder

after division is B(x), is gated onto the status signal on conductor **75**. External clock pulses on conductor **73** cause successive shifts of data in register **60** to the output data signal on conductor **74**. The external clock pulses also clear the remainder register by shifting in zeros.

The preferred embodiment, above, shows a remainder register beginning and ending with the same nonzero constant. However, it will be understood that other arrangements are possible when using a coset code. For instance, after detecting B(x), the remainder register can be set to a first arbitrary constant. Then, after division, the remainder register is checked for a proper second constant. The first constant, or the second constant, may be zero; both constants may not be zero.

Observe the simplified hardware which results from the error code format described herein. By ending with the start code, B(x), as a valid remainder, the start code detector (NAND gate **118**) also serves as a valid code detector. By beginning division with the start code in the divider, a control step is eliminated in not having to clear the remainder register.

Typically, error codes are placed at the end of a message. In accordance with the present invention, by placing the error code before the information bits, the receiver controller is further simplified in not having to distinguish information bits from error code bits with regard to the data storage register **60**. In addition, the receiver controller, as shown in FIG. **8**, is a simple counter **117**, having a start terminal, a stop terminal, and providing a timing out for a single time interval.

## MICROPROCESSOR IMPLEMENTATION

Digital information, including band number and field number, are recorded on the video signal, and utilized by the player to achieve a variety of features. Band number information is used by the player to detect end of play (band sixty three). Field number information in ascending order is used to calculate and display the program playing time on LED display means **22** in FIG. **1**. If the length of program material is known, field number information can be used to compute the remaining program playing time. For NTSC type signals, elapsed program time in minutes may be obtained by calculating the field number divided by 3600. If desired, the remaining program time may be derived from the previous calculation. This feature is useful to the viewer when scanning for a desired point in the program. A particularly useful feature, derived from field number information, is locked groove correction which will be discussed hereinafter in conjunction with the more general case, track error correction.

Field numbers represent actual stylus position. Thus, whenever the stylus re-enters a groove, whether after jumping tracks or after the scan mechanism is operated, the actual stylus position can be determined from the first valid field number read. Both the track error correction system and the program playing time display means use field number data, and therefore share the decoding portion of the video disc digital data system. The particular embodiment of track error correction system discussed herein after uses field number data (stylus position) to keep the stylus at or ahead of its expected position assuming a predetermined stylus/-record relative velocity. The program playing time display uses field number data for an indication of playing time, which is actually another representation of stylus position.

The microprocessor controller has several internal modes. FIG. **10** is a state transition diagram indicating the mode logic performed by the microprocessor program. Each of the circles represent a machine mode: LOAD, SPINUP, ACQUIRE, PLAY, PAUSE, PAUSE LATCHED, and END. For each mode, the position of the stylus and the status of the display is indiated inside each respective circle. The arrows between modes indicate the logical combination of signals, supplied by the panel controls (load, pause, scan), that cause a transition from one mode to another. The load signal indicates that the player mechanism is in a condition to receive a video disc. The pause signal is derived from a corresponding control panel switch, and the scan signal indicates the operation of the scan mechanism.

After power is turned on, the system goes into LOAD mode. A video disc may be loaded onto the turntable in this mode. After loading, the player enters SPINUP mode for several seconds, allowing the turntable to be brought up to the full speed of 450 RPM. At the end of SPINUP mode, the ACQUIRE mode is entered.

In ACQUIRE mode, the digital subsystem lowers the stylus and continuously searches for a "good read". In ACQUIRE mode, a "good read" is defined as a valid start code and a valid error check remainder. After finding a "good read" the system enters PLAY mode.

In PLAY mode, the microprocessor establishes in memory an expected, or predicted, next field number. The predicted field number is incremented or updated each field. For all subsequent reads, the microprocessor uses the predicted field number in performing two additional checks to further improve the integrity of the data.

The first additional check is a sector check. The video disc in the embodiment under consideration contains eight fields in every revolution, dividing the disc into eight sectors. Since the relative physical position of the sectors is fixed, the sectors follow a periodic recurring order as the disc rotates, even if the stylus jumps over a number of grooves. Although the digital information cannot be read for one or more fields, (sectors) while the stylus is skipping to a new groove, the microprocessor keeps time, and increments the predicted field number accordingly. When the stylus settles in a new groove and picks up a new digital message, the new field number is checked by comparison to the predicted field number. If the sector is wrong, the data is considered a "bad read".

Field number is represented by an 18 bit binary number. Sector information may be obtained from field number by finding the remainder after dividing the field number by eight. However, it is noted that the three least significant bits of a binary number counts modulo eight. Therefore the least significant three bits of each new field number must equal the least significant three bits of the predicted field number to pass the sector check.

A second check of data integrity is the range check, a test of the maximum range of stylus movement along the radius of the disc. No more than 63 grooves are expected to be jumped when encountering worst case conditions in any mode. Groove numbers are represented by the most significant 15 bits of the field number. The microprocessor substracts the present groove

number from the predicted groove number. If the difference is greater than the acceptable range of 63 grooves, then the present data is considered a "bad read". All other reads are regarded as good reads and are used to update the predicted field number. After fifteen consecutive bad reads, the system re-enters the ACQUIRE mode. The presence of a scan signal in certain modes, as shown in FIG. **10**, will also cause a transition to ACQUIRE mode.

When going from ACQUIRE mode to PLAY mode the microprocessor sets the bad read count to thirteen. This means that when entering PLAY mode from ACQUIRE mode, one of the next two fields must supply a good read or the bad read count will reach fifteen causing a return to ACQUIRE mode.

If the pause button is pressed during PLAY mode, the system enters PAUSE mode. In this mode the stylus is off the record and is held in its then radial position over the record. When the pause button is released, PAUSE LATCHED mode is entered and held. Pressing the pause button again releases the PAUSE LATCHED mode, causing a transition to ACQUIRE mode. END mode is entered from PLAY mode when band number sixty three is detected.

FIG. **11** is a flow chart of the program executed by the microprocessor. The microprocessor hardware includes one interrupt line and a programmable timer. A commercially available microprocessor suitable for the present system is the Fairchild Semiconductor model F8.

The microprocessor uses the timer to control the window in time that the information buffer searches for data. This "data window" is approximately twelve horizontal lines wide and is centered about the expected data. When no data is found, the timer maintains internal program synchronization to one field time interval.

The microprocessor interrupt is coupled to the status signal on conductor **75** (FIG. **4**). Interrupts are enabled only in ACQUIRE mode when the system continuously searches for data. The program is interrupted when a digital message is received. The interrupt service routine (not shown) sets an interrupt flag if the error code check indicates validity. Thereafter, in PLAY mode, the programmable timer is used to indicate the estimated time of arrival of the next digital message.

Switch inputs (load, scan, and pause) are conditioned to prevent switch bounce from causing undesired player response. The microprocessor program includes logic to debounce switch inputs. Debounced switch values are stored in memory. A separate debounce count is maintained for each switch. To check debounce **154** the switches are sampled and compared to the stored switch value. If the sampled state and the stored state are the same, the debounce count for that switch is set to zero. Switch states are sampled as often as possible. Each field, (every 16 milliseconds for NTSC), all debounce counts are incremented unconditionally. If the resulting debounce count is equal to or greater than 2, the stored state is updated to the new (debounced) value. The new switch state is then acted upon.

The first programmed step (FIG. **11**), after power is turned on, is initialization **150** of all program parameters. The timer is set to time out one video field. Mode is set to LOAD.

The next step **152** is a program to carry out the state transition logic represented in FIG. **10**. Debounce counts are normally incremented at this time, and tested to determine whether a new switch state is fully debounced.

After the mode selection logic **152**, the program enters a tight loop **153** to (1) sample switches setting debounce counts to zero, if required **154**, and (2) check if the timer is close to time out **155**, and (3) check if the interrupt flag has been set **156**.

If the interrupt flag is set **156**, the program transfers data, **157***a*, from the information buffer and sets the timer, **157***b*, to time out a new field interval. When the interrupt service routine sets the interrupt flag, the contents of the timer are saved in memory. The program now uses the previously stored timer contents to set the timer, **157***b*, with a corrected value predicting the approximate time of occurrence of the next digital message. As previously noted, even though the data represents the first good read in ACQUIRE mode, the bad read count is set, **157***c*, to 13.

If the interrupt flag is not set, the program branches as the timer gets close to time out, **155**. If the machine is not in PLAY mode **159**, then the timer is set to time out another field interval, **158**. If the machine is in PLAY mode, **159**, then a number of time critical tasks, **160**, are performed. The data window is opened, **160***a*, (by setting control signal on conductor **71** in FIGS. **1** and **8** to a logical one) approximately six horizontal lines before the expected data. Received data is read and checked as previously described. After data is received, or if no data is received, the data window is closed. Timer content, which represents the actual time of arrival of the digital message, is used as a correction factor to set the timer again, **160***b*. The timer is therefore set to center the next data window over the predicted time of arrival of the next digital message based on the actual time of arrival of the present digital message.

Expected field number is updated, **160***c*, band number is checked for start (band 0) and end of play (band sixty three), and the bad read count is incremented, **160***g*, for a bad read. For valid field data in the program viewing material, time is calculated and displayed, **160***f*. If valid field data indicates that the stylus has skipped backward, the stylus kicker means is activated, **160***e*, and ACQUIRE mode is entered. Also, if the bad read count reaches 15, ACQUIRE mode is directly entered. Throughout the time utilized for critical tasks **160**, the switch debounce check routine is repeated periodically so that switches are tested as often as is feasible. The program unconditionally returns through the mode selection logic **152** to the tight loop **153** and waits for the timer test **155**, or the interrupt check **156**, to indicate the arrival of the next digital message.

The timer may be set by loading the timer directly via programmed instructions. However, rather than use a sequence of instructions, it is best to "set" the timer by establishing a location in memory (a mark) which corresponds to a time out condition of the timer. The timer, then, is free running. Time out, or closeness to the time out, is detected by comparing the contents of the timer to the mark set in memory. The next desired time out condition is set by adding the next desired time interval to the previous timer contents and storing the result in memory. The timer is thus "set" each time valid data is received, or if no data is received within the data window, by setting a new mark in memory corresponding to the next time out condition.

The programmable timer in the microprocessor used in the present embodiment is conditioned by the program to divide cycles of the input 1.53 MHz clock by a

factor of 200. The timer thus counts once for every 200 cycles of the 1.53 MHz clock. One vertical field (1/60 second for NTSC) is then approximately 128 timer counts. One may alternatively use a timer which counts a different multiple of the 1.53 MHz clock, or one that uses a timing source independent of the video signal.

The data window is made wide enough to allow for several sources of timing error. Timer uncertainty due to the finite resolution of the timer is equal to one least significant bit, which corresponds to two horizontal lines. Accumulated drift error, because 128 timer counts is not exactly one vertical field, is somewhat less than one line after 16 consecutive fields in which no valid message is found. It is noted that since the 1.53 MHz color subcarrier clock is an odd multiple of one half of the line frequency, a timer which counts a corresponding multiple of the color subcarrier clock would have zero drive rate. In the particular embodiment described herein, program uncertainty in determining the time of arrival of the data, is approximately 97 microseconds, or about 1.5 lines. Finally, because alternate fields are interlaced, the time from one digital message to the next is either 262 lines or 263 lines, depending on whether the present field is odd or even. Although the program could keep track of odd and even fields, it is simpler to just widen the data window by one additional line. Combining the above factors, it can be shown that a data window extending three timer counts (about 6 lines) both before and after the start of expected data is adequate to allow for worst case timing conditions.

## TRACK ERROR CORRECTION

As mentioned earlier, field number information may be used to detect locked grooves. If the new field number (after sector and range check) is less than the expected field number, then the stylus has skipped backward and is repeating the tracking of a previously played convolution(s), i.e. a locked groove has been encountered. If the new field number is greater than the expected field number, the stylus has skipped forward, i.e. toward record center. In the present application, skipped grooves are ignored; if the new field number is greater (but still passes sector and range check) then the expected field is updated to the new field. In certain other applications, such as where the video disc is used to record digital information on many horizontal lines, it may be necessary to detect and correct skipped grooves as well. However, for the present video application, a locked groove is corrected by operating a stylus "kicker" until the stylus is returned to the expected track. Eventually, the stylus will be advanced past the locked groove defect.

In a more general sense, the use of field number information in accordance with the present disclosure provides an accurate means for detecting general tracking errors. In any video disc system having spiral or circular tracks, including optical and grooveless systems, tracking errors due to defects and contaminants are always possible. The present system provides a means for detecting and correcting such tracking errors in a video disc player. For positive tracking, a bi-directional kicker means is provided for moving the pickup backward or forward in the program material. Thus, when a tracking error is detected, whether a skipped track or a locked track, the pickup is moved in such direction so as to correct the tracking error. Although the regular pickup servo could be used for track error correction purposes, a separate kicker, or pickup repositioning means, is preferable. The regular servo is generally adapted for stable tracking of the spiral signal track, and may not have the proper characteristics to respond to abrupt tracking errors. A separate kicker, on the other hand, can be specifically adapted to provide the fast response needed to correct tracking errors. A specific example of a kicker suitable for use with the disclosed apparatus may be found in U.S. patent application Ser. No. 39,358, for E. Simshauser entitled "TRACK SKIPPER APPARATUS FOR VIDEO DISC PLAYER," filed May 15, 1979 and assigned to the assignee of the present invention.

Several control algorithms are possible. The pickup apparatus may be returned directly to the correct track by producing stylus motion proportional to the magnitude of the detected tracking error. Or, a kicker may be operated in response to a series of pulses, wherein the number of pulses is proportional to the magnitude of the detected tracking error. The pickup is moved a given number of tracks per pulse until the stylus is back on the expected track. For certain applications (e.g. retrieving digital data stored on the video disc medium) it may be desirable to return the pickup to the point of departure and attempt a second read, rather than return the pickup to the expected track. In any event, it is seen that by the use of a kicker and suitable control logic, successful tracking can be obtained even though the video disc contains defects or contaminants which would otherwise cause unacceptable tracking errors.

In a digital track correction system, security against undetected data errors is particularly important to prevent noisy signals from advancing or retarding the pickup unnecessarily. The present data system reduces the probability of an undetected read error to a negligible level.

To a rough approximation, one can estimate the probability that a random digital input will appear to the data system as a valid message containing a non-sequential field number, thereby actuating the stylus kicker. The random probability of a good start code is 1 in $2^{13}$. The random probability of a good error code is also 1 in $2^{13}$. The random probability of a good field number is calculated as follows. Field numbers containing 18 bits. Since there are eight sectors on the disc of the system under consideration, the least significant 3 bits of each field number indicate the sector number, which must match the expected sector number. The remaining fifteen bits, which represent groove number, can vary over the allowable range (plus or minus 63 grooves). Therefore only 126 out of $2^{18}$ random field numbers will pass the sector and range checks. Combining all safeguards, the probability of an undetected error is 126 in $2^{44}$.

The above estimate is based on an assumption of a truly random input, and it does not take into account several factors which further reduce the probability of an undetected error.

For example, on a video disc track, burst noise, where the erroneous bits are adjacent to each other, is more likely than other types of noise. As previously noted, the particular error code chosen detects all single burst errors up to 13 bits, and a high percentage of all longer bursts as well. Also, as previously explained, the choice of a non-zero remainder for the error check code (a coset code) further reduces the probability of an undetected error. Furthermore, the particular start code chosen, a Barker code, reduces the probability that noise will cause a false start code detection.

The disclosed data system, as applied to the video disc system, results in a rate of undetected errors which is relatively low and false alarms which would otherwise cause unnecessary stylus movement are significantly reduced. The data security provided by the disclosed system improves the stability of many player functions, such as display of program playing time, which depend on recorded digital data for proper operation.

What is claimed is:

1. In a video disc recording apparatus for encoding an information word on a video signal, the combination comprising:
- means for generating a video signal;
- means for generating a first data sequence corresponding to a start code;
- means for generating a second data sequence corresponding to an error code over at least a portion of said information word;
- means for serially concatenating the first and second data sequences and the information word in the order recited; and
- means for modulating said video signal in accordance with the concatenated data sequences and information word.

2. In a video disc recording apparatus for encoding an information word on a video signal, the combination comprising:
- means for generating a video signal;
- means for generating a first data sequence corresponding to a start code;
- means for generating a second data sequence corresponding to an error code over at least a portion of said information word; and
- means for modulating said video signal in accordance with a recorded data word comprising said start code, said error code, and said information word in the order recited, wherein said error code is a coset code over at least a portion of said recorded data word.

3. In a video disc recording apparatus for encoding a recorded data word on a composite video signal, the combination comprising:
- means for genrating a video signal including a subcarrier signal;
- means for generating a first data word corresponding to a start code;
- means for generating a second data word corresponding to an error code over at least a portion of said recorded data word;
- means for generating a third data word corresponding to information bits to be recorded on said video signal, said third data word including field number information corresponding to a video field being encoded;
- synchronizing means, responsive to said means for generating a video signal, for generating a synchronizing signal in synchronism with at least one field of said video signal;
- means responsive to said synchronizing signal for generating said recorded data word in the form of a serial sequence of said first, second, and third data words in synchronism with said subcarrier signal; and
- means for modulating said video signal in accordance with said serial sequence during a horizontal line of the field corresponding to said field number information.

4. In a video disc recording apparatus for encoding a recorded data word on a composite video signal, the combination comprising:
- means for generating a video signal including a subcarrier signal;
- means for generating a first data word corresponding to a start code;
- means for generating a second data word corresponding to an error code over at least a portion of said recorded data word;
- means for generating a third data word corresponding to a number of spare information bits;
- means for combining said second and said third data words to produce a fourth data word;
- means for generating a fifth data word corresponding to the field number of a video field being encoded;
- means for generating a sixth data word corresponding to the band number of the video program material being encoded;
- synchronizing means, responsive to said means for generating a video signal, for generating a synchronizing signal in synchronism with at least one field of said video signal;
- means responsive to said synchronizing signal for generating said recorded data word in the form of a serial sequence of said first, fourth, fifth, and sixth data words in synchronism with said subcarrier signal; and
- means for modulating said video signal in accordance with said serial sequence during a horizontal line of the field corresponding to said field number information.

5. A recording apparatus as set forth in claims 1 or 2 or 3 or 4, wherein said start code is represented in a binary format by

1111100110101.

6. The combination as set forth in claims 1 or 2 or 3 or 4 further comprising polynomial arithmetic means for generating said error code over the entire recorded data word.

7. The combination as set forth in claim 6 wherein said polynomial arithmetic means includes means for performing polynomial division and multiplication by constant polynomials g(x) and H(x) respectively, and means for adding a constant polynomial M(x).

8. The combination as set forth in claim 7 wherein said polynomial constant g(x) is given by

$$g(x)=x^{13}+x^{12}+x^{11}+x^{10}+x^{7}+x^{6}+x^{5}+x^{4}+x^{2}+1.$$

9. A video disc playback decoder apparatus for decoding an information word from a video signal including a subcarrier signal, wherein said video signal is modulated synchronously with said subcarrier signal in accordance with a recorded data word comprising a start code, an error code and information bits in the recited order, said decoder apparatus comprising:
- digital data receiving means responsive to said video signal for sampling said video signal synchronously with said subcarrier signal, said digital data receiving means having a received data word output corresponding to the bits of said recorded data word;
- first decoder means coupled to said digital data receiving means for detecting said start code;
- receiver control means responsive to said first decoder means, said receiver control means including means for generating a first signal defining a time interval subsequent to the detection of said start

code by said first decoder means to a time substantially equal to the end of said recorded data word;

shift register means coupled to said digital data receiving means and responsive to said first signal from said receiver control means for storing at least a portion of said recorded data word corresponding to said information bits;

polynomial divider means including an error check register, said polynomial divider means coupled to said digital data receiving means for sequentially dividing at least a portion of said received data word by a constant polynomial to produce an error check result in said error check register; and

means responsive to said error check result for generating a status control signal when the error check result is equal to a predetermined constant and indicative of the information bits stored in said shift register being valid.

**10**. A video disc playback decoder apparatus for decoding an information word from a video signal, wherein said video signal is modulated in accordance with a recorded data word comprising a start code, an error code word and information bits in the recited order, said decoder apparatus comprising:

digital data receiving means responsive to said video signal, said receiving means having a received data word output corresponding to the bits of said recorded data word;

first decoder means coupled to said receiving means for detecting said start code;

polynomial divider means coupled to said receiving means, said polynomial divider means including an error check register for dividing sequentially at least a portion of said received data word including said error code word and said information bits by a constant polynomial g(x); and

receiver control means responsive to said first decoder means and said error check register, said receiver control means including means for setting said error check register to a first predetermined constant before division, and means for indicating that said received data word is valid if said error check register contains a second predetermined constant after division, wherein at least one of said first and second predetermined constants is not zero.

**11**. A decoder apparatus for decoding an information word from a video signal said video signal including a subcarrier, wherein said video signal is modulated during a horizontal line during the vertical blanking interval thereof in accordance with a recorded data word, said recorded data word including sequentially an error code and an information word, said decoder apparatus comprising:

receiving means responsive to said modulated video signal for detecting individual bits of a received data word;

polynomial divider means coupled to said receiving means and synchronized with said subcarrier for sequentially dividing at least a portion of said error code and said information word by a constant polynomial g(x), said polynomial divider means having a remainder output; and

control means responsive to said remainder output, for indicating that said received data word is valid if said remainder output of said polynomial divider is equal to a predetermined value, wherein said predetermined value is not equal to zero.

**12**. A decoding apparatus as set forth in claim **9** or **10** wherein said start code is represented in a binary format by,

1111100110101.

**13**. A decoding apparatus as set forth in claims **10** and **11** wherein said constant polynomial g(x) is given by

$$g(x)=x^{13}+x^{12}+x^{11}+x^{10}+x^{7}+x^{6}+x^{5}+x^{4}+x^{2}+1.$$

**14**. A decoder apparatus as set forth in claims **10** or **11** wherein said control means includes a receiver control counter for establishing desired timing periods and wherein said polynomial divider means is responsive to said timing periods for dividing the entire received data word.

**15**. A decoder apparatus as set forth in claims **10** or **11** wherein said control means includes a receiver control counter for establishing a particular timing period to enable said polynomial divider means for dividing said combined information and error code of said received data word.

**16**. In a video disc recording apparatus for recording a video signal on a video disc, an improved method for encoding an information word on said video signal, said method comprising:

generating a first data sequence corresponding to a start code;

generating a second data sequence corresponding to an error code over at least a portion of said information bits;

concatenating the first and second data sequences and the information word in the other recited; and

modulating said video signal in accordance with the concatenated data sequences and information word.

**17**. In a video disc recording apparatus for recording a video signal on a video disc, an improved method for encoding an information word on said video signal, said method comprising:

generating a first data sequence corresponding to a start code;

generating a second data sequence corresponding to an error code over at least a portion of said information word;

modulating said video signal in accordance with a recorded data word comprising said start code, said error code, and said information word in the recited order, wherein said error code is a coset code over at least a portion of said recorded data word.

**18**. In a video disc recording apparatus for recording a composite video signal on a video disc, an improved method for encoding a recorded data word on said composite video signal, said method comprising:

generating said composite video signal including a subcarrier signal;

generating a first data word corresponding to a start code;

generating a second data word corresponding to an error code over at least a portion of said recorded data word;

generating a third data word corresponding to information bits to be recorded on said composite video signal, said third data word including field number information corresponding to a video field being encoded;

generating a serial sequence of said first, second, and third data words in synchronism with said subcarrier signal; and

modulating said composite video signal in accordance with said serial sequence during a horizontal line of the field corresponding to said field number information.

**19**. In a video disc recording apparatus for recording a composite video signal on a video disc, an improved method for encoding a recorded data word on said composite video signal, said method comprising:

generating said composite video signal including a subcarrier signal;

generating a first data word corresponding to a start code;

generating a second data word corresponding to an error code over at least a portion of said recorded data word;

generating a third data word corresponding to a number of spare information bits;

combining said second and said third data words to produce a fourth data word;

generating a fifth data word corresponding to the field number of a video field being encoded;

generating a sixth data word corresponding to the band number of the video program material being encoded;

generating a serial sequence of said first, fourth, fifth, and sixth data words in synchronism with said subcarrier signal; and

modulating said composite video signal in accordance with said serial sequence during a horizontal line of the field corresponding to said field number information.

**20**. The method as set forth in claim **16** or **17** or **18** or **19** wherein said start code is represented in a binary format by

1111100110101.

**21**. The method as set forth in claims **16** or **17** or **18** or **19** wherein said error code is generated by polynomial arithmetic means over the entire recorded data word.

**22**. In a video disc recording apparatus for recording a video signal on a video disc, an improved method for encoding an information word, I(x), on a horizontal line of said video signal during the vertical blanking interval thereof, said method comprising:

generating an error code, C(x), using a generator polynomial g(x), said error coded being of the form

$$C(x)=[I(x)\cdot H(x)]+M(x)$$

where H(x) and M(x) are each constant polynomials;

modulating said video signal during a horizontal line during the vertical blanking interval thereof in accordance with a recorded word T(x), including said error code preceding said information word,

wherein H(x) and M(x) are chosen so that $[T(x)]@0$ and $[T(x)]$ is the resulting remainder after division of T(x) by g(x).

**23**. In a video disc playback apparatus for playing a video disc having encoding thereon a video signal including a subcarrier signal, wherein said video signal is modulated synchronously with said subcarrier signal during a horizontal line during the vertical blanking interval of said video signal in accordance with a recorded data word, said recorded data word including a start code, an error code, and an information word in the recited order, an improved means for frame synchronization of said video disc player to said recorded data word, the improvement comprising:

receiving means for sampling said video signal synchronously with said subcarrier signal for detecting the individual bits of a received data word;

start code detector means responsive to said receiving means for detecting the occurrence of said start code and for providing a frame synchronizing signal in response to said detecion, said start code corresponding to a Barker sequence; and

means responsive to said frame synchronization signal for storing at least a portion of said data word in said playback apparatus.

**24**. A video disc playback decoder apparatus for decoding an information word from a video signal, wherein said video signal is modulated in accordance with a recorded word comprising a start code, an error code and information bits in the recited order, said decoder apparatus comprising:

digital data receiving means responsive to said video signal said receiving means having a received data word output corresponding to the bits of said recorded data word;

shift register means having selectively enabled feedback means to prescribed stages of said register, said shift register having an input terminal serially connected to receive said received word output and having parallel output connections at respective register stages;

first decoder means coupled to respective ones of said shift register parallel output connections for generating a control signal responsive to detection of said start code and wherein said control signal enables said feedback means;

second decoder means connected to respective ones of said shift register parallel output connections for generating a status control signal responsive to detecting the presence of a prescribed error check result remaining in said shift register after division of at least a portion of the received data word therein by a prescribed polynomial g(x) by virtue of the feedback connections, said status control signal indicating that the received information bits are valid; and

receiver control means responsive to the control signal from said first decoder means for determining the portion of the received data word over which division is performed in said shift register.

* * * * *

LENOVO EXHIBIT 1011 - 20/21

UNITED STATES PATENT AND TRADEMARK OFFICE

# CERTIFICATE OF CORRECTION

PATENT NO. : 4,308,557

DATED : Dec. 29, 1981

INVENTOR(S) : Charles B. Dieterich

It is certified that error appears in the above—identified patent and that said Letters Patent is hereby corrected as shown below:

The title, "VIDEO DISC SYSTEM" should be --ERROR CODING FOR A VIDEO DISC SYSTEM--.

Col. 8, line 19, "trasmission" should be --transmission--.

Col. 9, line 36, "ad" should be --as--.

Col. 12, line 10, "indiated" should be --indicated--.

Col. 15, line 18, "drive" should be --drift--.

Col. 17, line 44, "genrating" should be --generating.

Signed and Sealed this

Thirteenth Day of July 1982

[SEAL]

Attest:

GERALD J. MOSSINGHOFF

Attesting Officer

Commissioner of Patents and Trademarks