PATENT APPLICATION

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FOR

CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES

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CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES

TECHNICAL FIELD

[0001] Embodiments of the invention generally relate to the field of electronic devices and, more particularly, to a method and apparatus for a control bus for connection of electronic devices.

BACKGROUND

[0002] Multiple electronic devices are increasingly connected together to communication date. In one example, entertainment and multi-media devices may be interconnected to transfer or share digital information. The connection of such devices generally requires some form of standard bus or interface to allow the devices to easily connect communicate with each other.

[0003] In one example, the HDMI™ (High-Definition Multimedia Interface) provides an interface that allows for the transfer of uncompressed digital high-definition video and audio, together with associated control signals. (HDMI is a trademark of HDMI Licensing, LLC) HDMI includes the High-Definition Multimedia Specification 1.3 (Hitachi, Ltd., Matsushita Electric Industrial Co., Ltd., Philips Consumer Electronics, International B.V., Silicon Image, Inc., Sony Corporation, Thomson Inc., and Toshiba Corporation) (June 22, 2006), as well as earlier versions of HDMI. Multimedia devices may include any devices capable of providing, storing, or displaying multimedia data, including television monitors, cable and satellite set-top boxes, video players, including DVD (Digital Versatile Disk), HD (High-Definition) DVD, and Blu-Ray players, audio players, digital video recorders, and other similar devices.

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[0004] However, the use of any interface may be affected by physical size of devices. For example, media devices may be portable or handheld. The use of an interface designed for a standard device may be difficult for smaller devices. In addition, there is physical limit on how many connections may be reasonably added to a smaller device. The addition of an interface in addition to, for example, a USB (Universal Serial Bus) connection to a device may result in excessive connections to the device, thus making it less likely that manufacturers will includes such an interface in manufactured device.

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SUMMARY

[0005] A method and apparatus are provided for a control bus for connection of electronic devices.

[0006] In a first aspect of the invention, a method includes coupling a transmitting device to a receiving device. The coupling of the devices includes connecting a control bus between the transmitting device and the receiving device, the control bus being a bi-directional, single-line bus. Control of the control bus is obtained for either the transmitting device or the receiving device, with the device obtaining control becoming an initiator and the other device becoming a follower. One or more control signals are converted to one or more data packets, with each of the one or more control signals representing one of multiple different types of control signals. The generated data packets are transmitted from the initiator to the follower via the control bus.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Embodiments of the invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

[0008] **Figure 1** is an illustration of an embodiment of a transmitting device coupled with a receiving device;

[0009] **Figure 2** is a flowchart to illustrate an embodiment of a process for providing control signals between a transmitting device and a receiving device;

[0010] **Figure 3** is an illustration of an arbitration process for a bi-directional, single-bit control bus;

[0011] **Figure 4** is an illustration of an embodiment of a mobile device coupled with a standard device via a control bus;

[0012] **Figure 5** is an illustration of an embodiment of a connection between two mobile devices;

[0013] **Figure 6** illustrates an embodiment of a cable that may be utilized to connect a transmitter and a receiver;

[0014] **Figure 7** is an illustration of an embodiment of cable signal assignments for transmitter and receiver;

[0015] **Figure 8** illustrates an embodiment of a data packet for transfer of control data; and

[0016] **Figure 9** is an illustration of the header and control fields utilized in an embodiment of a control data packet.

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DETAILED DESCRIPTION

[0017] Embodiments of the invention are generally directed to a control bus for connection of electronic devices.

[0018] As used herein:

[0019] "Mobile device" means any mobile electronic device. The term "mobile device" includes, but is not limited to, a cellular telephone, smartphone, PDA (personal digital device), MP3 or other format music player, digital camera, video recorder, digital storage device, and other similar devices.

[0020] In some embodiments, a system provides an interface to connect a mobile device to other devices. In some embodiments, a mobile device utilizes a modified protocol to allow connection with other devices, which may utilize a standard protocol. In some embodiments, a connection between a mobile device and another device includes the merging of multiple control signals on to a single bus, where such control signals would have utilized multiple buses under the standard protocol. In some embodiments, a mobile transmitting device utilizing a modified protocol may be connectable with a dual mode receiving device, wherein the receiving device may receive data from either the mobile transmitting device or a standard transmitting device.

[0021] In a particular embodiment, data being transferred between devices may be multimedia data and associated commands, including HDMI data and commands. For example, a mobile device containing high-definition video data and related commands may be connected to a standard HDMI device (such as, for example, a television monitor). However, embodiments of the invention are not limited to any particular type of data or device. As used herein, HDMI-M is utilized here to indicate a

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mobile device utilizing a modified protocol. The HDMI-M device may include the use of USB (Universal Serial Bus) protocol data, utilizing USB-OTG (USB On-The-Go, a standard for portable devices that allows dual-mode operation in which a device may be connected to a personal computer or to another portable device). HDMI-E is utilized here to designate a dual-mode device that can be interfaced with a modified protocol mobile device or a standard protocol device.

[0022] In some embodiments, a link layer describes a method and protocol for sending and receiving data between two devices using a bi-directional, 1-bit (single wire) data line. In some embodiments, a translation layer will describe how standard control protocols may be mapped to the 1-bit line. In a particular embodiment in which an HDMI system is involved, the translation layer describes how CEC (Consumer Electronics Control), DDC I2C (Display Data Channel), and any other protocols may be mapped to the 1-bit data line. In HDMI, DDC is used for configuration and status exchange between a single source (a "source" being a device providing HDMI output) and a single "sink" (a sink being a device receiving an HDMI input). Further, CEC is an optional protocol that provides high-level control functions between all of the various audiovisual products in a user's environment. In an embodiment, a "private channel" of the control bus may be used to carry out housekeeping tasks between the transmitter and the receiver. The private channel also used as a communications channel between the transmitter and receiver firmware.

[0023] In some embodiments, the link layer is a point-to-point bi-directional bus using "bi-phase mark encoding" to transmit bits. In bi-phase mark encoding, each bit of data is represented by two logical states. The first state of a symbol is always different

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from the last state of the previous symbol. Further, the last state of a symbol is identical to the first state if the bit to the transmitted is a logical '0', and the last state of a symbol is different than to the first state if the bit is a logical '1'. Using bi-phase mark code assists in synchronization by ensuring that at least one transition occurs on a channel for every bit of data.

[0024] In some embodiments, standard control commands and data are converted into data packets for transmission on the single bit control bus, with the data packets identifying the types of commands and data being transmitted. In some embodiments, the protocol for the control bus is byte-oriented to address the bytes of standard protocol commands and data. In an example, the byte-oriented protocol may be used to align with both DDC and CEC for HDMI, which are also byte-oriented. In some embodiments, the start of each data packet is signaled by a clock (sync) pulse, followed by 2 bits of header, 1 control bit, 8 bits of data, and 1 bit of parity. There is further 1 bit for a received ACK (acknowledge). In this example, the byte structure provides a total of 13 bit times per byte transfer, followed by an ACK. The link layer interfaces to the translation layer, which in turn interfaces to the relevant control protocols, such as, in this example, DDC and CEC state machines for HDMI operations.

[0025] In some embodiments, upon power-on, a bus control logic enters a discovery and wake-enable phase in which the logic detects its connectivity and functionality. The bus control logic may then move to an arbitration phase to gain control of the bus, which is described in more detail below. Finally, in the active phase, data may be written from the initiator (the device gaining control of the bus) to the follower (the other device in the transaction). In some embodiments, an initiator may

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transmit multiple packets on the control bus after gaining control of the bus. In an example, if an initiator has transmitted a packet, a subsequent data packet from the same initiator may start immediately after the ACK from the follower.

[0026] In an embodiment, an existing connection may be utilized for the single-bit control bus, with a pad for the existing use being shared with the pad for the control bus. In one embodiment, a hot plug detection pad may be shared with a single bit-control bus pad. In an embodiment, the receiver and transmitter may be switchable to allow operation over the single-bit control bus while also operating within the parameters of the standard protocol. For example, for HDMI, there is a pull-up circuit for the transmitter and a pull-down circuit for the receiver on the control bus. In an embodiment, the pull-up and pull-down circuits are switchable (providing a choice between pull-up (or pull-down) and off) to support applications outside of the HDMI specification, such as the connection of a mobile device.

[0027] In some embodiments, a local oscillator is utilized to provide the necessary time base for either side of the bus, rather than utilizing a clock signal transmission. In an embodiment, a control bus implementation accommodates a broad range of time variation (such as, for example, 2X variation) in the local oscillator frequency, which may result from PVT (process, voltage, and temperature) variations in electronic circuits. Because multiple types of control signals are merged onto a single bus, a faster clock time is required. In a particular example, a local oscillator is divided down to provide a 1 us (1 MHz) timebase for the bit time for the transport of HDMI data. In an embodiment, this timebase is accurate to within +/- 40% in order to maintain the frequency variation within the 2X variation range.

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[0028] In an embodiment, the inclusion of a mobile device provides two possible modes of operation, and each may utilize a different cable. In a first case, a mobile transmitting device is connected to a standard protocol, dual-mode receiving device. The receiving device thus would include a standard cable input that is adapted for use with the mobile device. In a second case, a mobile transmitting device may be coupled with another mobile device.

[0029] In a first example, when an HDMI-M transmitter and an HDMI-E dual-mode receiver are connected via a Type-M to Type-E cable (indicating a cable from an HDMI-M transmitter to an HDMI-E receiver), then both HDMI and USB protocols can be operational. In this example, the control bus initiates discovery on the receiver side, followed by hot plug detect on the transmitter side. The control bus is used to provide an ID assignment to the USB-OTG PHY (physical layer) on the transmitter side of the connection.

[0030] In a second example in which two HDMI-M devices are connected together, this may be done via a Type-M to Type-M cable (indicating a cable from a first HDMI-M device, a transmitting device, to a second HDMI-M device, a receiving device). In this instance, only the USB-OTG connection is operational. The control bus is not connected between the devices, and is only used to provide an ID assignment to the USB-OTG PHY on either side of the connection. In this example, the Type-M to Type-M cable would not physically have any wires connecting the TMDS clock, data, and control bus lines. However, one end of the cable would have its control bus pin shorted to GND, in the manner of a USB-OTG cable. Further, in this example the HDMI-M transmitter chip should provide an ID output to the USB PHY. This output

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would normally be driven high, even in low-power state. In an embodiment, the HDMI-M receiving chip does not need to provide an ID output to the USB PHY on the receiver side because the receiver device will always be configured as a host.

[0031] In some embodiments, the control bus is bi-directional and either device may gain control of the control bus for transmission. In an embodiment, the control bus may be implemented such that either device will obtain control if the other device is not competing, and such that one of the devices (generally the transmitter) will win the arbitration if both devices attempt to gain control of the control bus at approximately the same time.

[0032] In some embodiments, a potential initiator must first check if the line is busy. If the control bus has been idle (remaining high, in an example) for a certain time period the device may start arbitration. In one example, data transmission may be required to start from 6 to 9 bit times after arbitration is won. The initiator will start sending packets of data, each packet followed by an acknowledge (ACK) from the follower. Arbitration is needed if the bus has been idle for over a certain number of cycles.

[0033] In one implementation, to arbitrate, a transmitting device drives the bus low for 4 bit times. In contrast, a receiving device should drive the bus low for the 1st bit time and high for the 2nd, 3rd, and 4th bit times. In one implementation, to reduce the electrical contention between high and low driven simultaneously on the control bus by two devices, "drive high" refers to driving a signal high for a short time at the beginning of a bit time and then releasing the bus. In this implementation, the pull up resister on the control bus acts to pull up and maintain the high signal level unless there is a signal

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driven low by the other device on the bus. The receiver checks the state of the bus during the 2nd, 3rd and 4th bit times. Because the receiver drives high for a short time at the start of each bit time and then releases the bus, the bus becomes low if the transmitter drives the bus low to obtain the bus. If the receiver detects that the bus is low during the any of these bit times the receiver can conclude that it has lost the arbitration. The receiver and transmitter bit times can differ by a factor of 2 from each other, which is the reason for requiring the transmitter to drive the bus low for 4 bit times. If the transmitter is two times faster than the receiver, the receiver would still see the bus stay low during the 2nd bit time.

[0034] In an embodiment, an initiator, after winning arbitration, should wait no more than a certain period (a maximum of 9 bit times) to send the SYNC pulse. If the follower does not see any activity for the time period (18 bit times after the end of arbitration, assuming the clocks could be up to two times different from each other) follower can assume that the initiator has given up the bus.

[0035] In an embodiment, if the transmitter and receiver arbitrate at about the same time, the transmitter always wins the arbitration. However, each side may be guaranteed to obtain the control bus in time if a limit on the number of packets one side can send before allowing the other side to take control of the bus (such as a maximum packet count of 24) is implemented. In an embodiment, this is a link-layer feature and is independent of any flow control that may be implemented in the translation layer.

[0036] In an embodiment, once an initiator completes a transaction, the initiator does not attempt a new transaction for a certain period, such as a time period of 6 bit times. This time period is utilized to allow the follower enough time for the follower

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to claim the bus for it is own transaction and became the initiator. In this example, the follower may be allowed to start a transaction 3 bit times after the final ACK. If it does so, it gains control of the bus and can send up to 24 packets. If the follower does *not* start a transaction within 6 bit times after the final ACK, the initiator can recover the bus and start its next set of 24 transactions beginning at the 6th bit time. If neither the initiator nor the follower starts a transaction within 9 bit times after the final ACK, the bus becomes inactive. If the bus is inactive, either side needs to arbitrate to gain control of it. Because the initiator and the follower have timebases that may be different by a factor of 2x, during a bus turn-around the follower may be required to maintain its calibration to the timebase of the initiator for 9 bit times, until and unless it takes control of the bus in the 3rd bit time.

[0037] In some embodiments, devices connected via a control bus engage in calibration using the control bus. In some embodiments the frequencies of the receiver and transmitter oscillator clocks may be vary by as much as two times, and thus a method of calibrating the follower's bit time based on the initiator may be implemented. The calibration is provided so that the following device is capable of sampling the received data at the appropriate point in the bit time.

[0038] In some embodiments, a sync pulse from the initiating device, such as the sync pulse provided at the beginning of a data packet, is used by the follower to calibrate the follower's bit time to the initiator. In some embodiments, this calibration may be updated at every subsequent transition on the control bus. In some embodiments, the sync pulse could have more than one bit time in order to increase calibration accuracy.

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[0039] In some embodiments, because the duty cycle on a control bus (which may be engaged in bi-phase mark encoding) may tend to be skewed away from 50%, the follower may maintain separate calibrations for the high time and low time of the sync pulse. The edge timings may move due to spread-spectrum variation, and thus the follower may be required to average out these variations through use of the separate high and low signals.

[0040] **Figure 1** is an illustration of an embodiment of a transmitting device coupled with a receiving device. In this illustration, a transmitter 102 is coupled to a receiver 110 via a cable 120. In this illustration, the receiver 110 may be standard protocol device 112, which may include a dual mode HDMI receiving device. In some embodiments, the dual mode HDMI receiving device would be capable of communicating with both an HDMI transmitter and an HDMI-M transmitter. In some embodiments, the transmitter 102 may be one of multiple types of devices. In this illustration the transmitter may be a first type of transmitting device, shown as a standard protocol device 104, such as a HDMI transmitting device, or a second type of device, which is shown as a mobile protocol device 106. The mobile protocol device 106 may be an HDMI-M transmitting device, such as handheld or other mobile media device. In some embodiments, the cable 120 may be either a standard protocol cable 122 for the connection of protocol devices (such as an HDMI compatible cable), or a mobile protocol cable 124 (such as an HDMI-M compatible cable), including a single control cable and a power cable. In some embodiments, the receiver 110 utilizes the signals received on the cable 120 to discover a connection with the transmitter 102, and the transmitter utilizes

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the signals on the cable 120 to assist in establishing a connection, such as a hot plug connection, with the receiver 110.

[0041] In a particular implementation, a control bus may have an operating frequency of 1 MHz to enable transmission of multiple HDMI protocols. In the implementation, the control bus may include control of internal registers, providing reading and writing capability. For HDMI, the control bus provides a bridge to the DDC I2C interface and a bridge to the CEC interface, and is expandable to other future protocols. In an embodiment, the control bus may be able to work while the rest of the system is in power down mode. Because of the cooperative operations between the transmitter and the receiver, the system does not require calibration or interruption of the outside micro-controller, and utilizes a ring oscillator or external clock for timing. The system does not need to maintain bit-accurate timing for either DDC or CEC protocols.

[0042] **Figure 2** is a flowchart to illustrate an embodiment of a process for providing control signals between a transmitting device and a receiving device. In this illustration, a transmitter and a receiver are connected together 202. In some embodiments, the transmitter is a mobile protocol device and the receiver is a standard protocol device. The receiver may be a dual-mode device that is capable of communicating with both a standard protocol device and a mobile protocol device. In a particular embodiment, the transmitter is an HDMI-M protocol device, and the receiver is an HDMI protocol device. The transmitter and receiver are connected by a mobile protocol cable, such as a HDMI-M compatible cable. In an embodiment, the transmitter and receiver utilize a bi-directional, single-bit control bus. In an embodiment, the control bus is a bus utilizing bi-phase mark encoding.

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[0043] In an embodiment, the transmitter and receiver engage in a discovery/hot plug process to identify each other, and initialize communication 204. In this instance, there is a determination that the receiving device is connected with a mobile device, and thus is utilizing a bi-directional, single-bit control bus. In an embodiment, the transmitter and receiver engage in an arbitration process to determine the ownership of the bus. The arbitration process may be the arbitration process illustrated in Figure 3. In this instance, the transmitter wins the arbitration, and is the initiator of the transaction. In an embodiment, the transmitter, as initiator, provides a signal to the receiver to calibrate the clocks of the transmitter and receiver 208.

[0044] In some embodiments, multiple control signals are multiplexed onto the control bus 210. In an embodiment, the multiple control signals are subjected to an arbitration process to determine which control signal is placed on the control bus. In some embodiments, the control signals are converted from bytes of data to data packets that identify the type of data within each packet. In one particular example, HDMI control signals are multiplexed together on the control bus on a byte by byte basis. For example, CEC, DDC, and private channel instructions are multiplexed together on the control bus. If there is a control signal to be transmitted 212, the signal is converted into a data packet for transmission. In an embodiment, the data packet may be a data packet as shown in Figure 8. The data packet is then transmitted from the transmitter to the receiver over the single-bit control bus 216. The process may continue as long as the transmitter has control signals to transmit, with the process then stopping 218.

[0045] For the receiver, one or more data packets containing command data may be received on the single-bit control bus 220. The receiver will read the header of

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each received data packet and determine the control type 222, and will handle each command as required under the standard protocol 224, such as, for example, HDMI.

[0046] **Figure 3** is an illustration of an arbitration process for a bi-directional, single-bit control bus. A transmitter and receiver are connected, with the connection including a bi-directional, single-bit bus 302. At some point in operation, either or both of the devices may wish to take control of the bus. In this process, there is determination of the status of the control bus 304. If it is determined that the CBUS is idle (having been unused for a certain number of cycles) or has been unused by the other device for a certain number of cycles (indicating that it is the device's turn to utilize the control bus) 306, then it is determined that the bus is still in use by the other device 308, then the use of the bus may be arbitrated 310. Otherwise, the device may determine that the control bus is in use by the other device. In an embodiment, if the transmitter and receiver seek to control the bus at approximately the same time, the transmitter will win the arbitration. If the transmitter seeks to control the bus, the transmitter will drive the bus low for a certain number of cycles (four cycles, in this example) 312, which will provide notice to the receiver that the transmitter is seeking control of the bus. The transmitter will then take control of the bus 314. If the receiver seeks control of the bus, then the receiver will drive the bus low for a cycle, and then drive the bus high for a short pulse 316. If the transmitter is not driving the bus, then the signal will stay high, and if the transmitter is driving the bus low the signal will go low. Based on this behavior, the receiver will check the signal on the CBUS during a certain period (during the second through fourth cycles in an example) 318. If the signal has remained high, this is an indication that the transmitter is not seeking control of the bus, and the receiver will take control 322. If the

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signal does not remain high, this is an indication that the transmitter is driving the signal low and is seeking control of the bus, and the transmitter again will take control 314.

[0047] **Figure 4** is an illustration of an embodiment of a mobile device coupled with a standard device via a control bus. In this illustration, a mobile HDMI transmitting device (HDMI-M TX board 410) is coupled with a dual-mode HDMI receiving device (HDMI-E RX board 430). The devices are coupled via a control bus/hot plug 402 (referred to herein as the CBUS), a 5 volt power source VBUS provided by the receiver 430 to the transmitter 410, and a USB connection 406. In some embodiments, the transmitter has a switchable pull-up circuit 414 (illustrated as part of the HDMI-M transmitter chip 412) and the receiver has a switchable pull-down circuit 436 (illustrated as part of the HDMI-E receiver chip 432) on the CBUS. Also illustrated is a series impedance 434 of receiver 430. The VBUS 404 is connected between a power/wake enable node 416 for the transmitter 410 and a power switch 438 for the receiver 430. The USB bus 406 is connected between a USB PHY (physical layer) 418 for the transmitter 410 and a USB PHY 440 for the receiver 430.

[0048] In an embodiment of the invention, the CBUS 402 is a bi-directional, single-bit control bus. In an embodiment, the CBUS operates utilizing bi-phase mark encoding. The CBUS is utilized to transport multiple different types of control signals between the transmitter 410 and the receiver 430, the control signals being multiplexed together for transmission. In an embodiment, either the transmitter 410 or the receiver 430 may take control of the CBUS 402, with the control of the CBUS being established by an arbitration process

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[0049] **Figure 5** is an illustration of an embodiment of a connection between two mobile devices. In this illustration, a first mobile device 510 (a first HDMI-M side) may be connected to a second mobile device 530 (a second HDMI-M side). As these are mobile devices, both devices include a pull-up circuit 514 and 534. The devices are connected via a VBUS 504, which is not powered, and a USB connection 506. The devices may further include a TMDS (Transition Minimized Differential Signaling) bus 508. The USB bus 506 connects a first USB PHY 518 to a second USB PHY 540. However, the connection of the two mobile devices results in a disconnected control bus.

[0050] **Figure 6** illustrates an embodiment of a cable that may be utilized to connect a transmitter and a receiver. In this example, an HDMI cable 610 may include a clock channel, three data channels (Blue 616, Green 618, and Red 614), a DDC channel 622 (the DDC channel having two wires), and a CEC channel 620 (the CEC channel having a single wire). (The cable may include other lines, such as a +5V power signal line, a hot plug detect, and a USB data channel, which are not illustrated here.) However, in some embodiments the HDMI-M cable may utilize fewer lines because of the smaller device size, including a clock channel 632, a merged data channel 632, and a single-bit control channel 640. In some embodiments, the single-bit control channel is a bi-directional channel that is operated at an increased speed to include merged control data from both a transmitter and a receiver.

[0051] **Figure 7** is an illustration of an embodiment of cable signal assignments for transmitter and receiver. Figure 7 illustrates a particular example of a cable connection implementation. In an embodiment, the assignments show the pins 710 for an HDMI-M device 720 that is connected to an HDMI device 730. In an

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embodiment, the HDMI device is a dual-mode device that is capable of communicating with both a standard HDMI device and an HDMI-M device. In this example, two of the data channels of the HDMI device 730 are not connected to HDMI-M device (pins 1-6), and thus the data is carried over the one data channel (pins 7-9). Further, the control data that would be transported via the DDC (pins 15-17, which lines are used for USB data) and CEC data are carried over the control bus (pin 19, which is used with the hot plug detect of the HDMI device)

[0052] **Figure 8** illustrates an embodiment of a data packet for transfer of control data. In an embodiment, control data from multiple sources is merged or multiplexed onto a single-bit control bus. In an embodiment, control data bytes are formed into data packets for transfer on the control bus. In an example, the data packet may be data packet 800. The fields contained in data packet 800 may vary in different embodiments. In this example, data packet 802 includes a 1-bit sync signal 802, followed by a 2-bit header 804 to indicate the type of data packet contained in the data packet 800 and a 1-bit control field 806 to indicate whether the data packet contains data or a command. The numbers of bits included in each field may vary in different implementations. In one example, the sync signal 802 may include more than one bit in order to increase calibration accuracy.

[0053] The header 804 and control field 806 may, for example, be encoded as provided in Figure 9. The control field is followed by 8 bits of translation layer data or command 808. Following the data 808 is a parity bit 810. The parity covers both the header and the data, and even parity is used. The use of even parity then ensures that the bus has transitioned to a high level prior to start of an acknowledge ACK 812.

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[0054] Thus, in an embodiment, a packet starts from a high state for the control bus (indicating an idle bus) with a sync pulse, and the control bus ends in a high state with an ACK. Aside from these two bits, there should be an even number of 0's in the packet in order for the bus level to end up at a high state at the end. (In bi-phase mark encoding, as used here, the bus level at the end of a '1' is the same as that at the beginning; the bus level at the end of a '0' is the opposite of that at the beginning.) Because there is an even number of bits, an even number of '1's are needed, and thus even parity.

[0055] **Figure 9** is an illustration of the header and control fields utilized in an embodiment of a control data packet. In a data packet carrying control data, such as the data packet 800 illustrated in Figure 8, two bits of a header 910 may be utilized to indicate whether the data packet includes a DDC packet (header field '00'), a CEC packet (header field '01'), or private channel data for the control bus (header field '10'). In this illustration, header field '11' is reserved for future uses. Further, a bit of a control field 920 may be utilized to indicate that the data bits (such as data 808 illustrated in Figure 8) represent translation layer data (control field '0') or a translation layer command (control field '1').

[0056] In the description above, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without some of these specific details. In other instances, well-known structures and devices are shown in block diagram form. There may be intermediate

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structure between illustrated components. The components described or illustrated herein may have additional inputs or outputs which are not illustrated or described.

[0057] Various embodiments of the present invention may include various processes. These processes may be performed by hardware components or may be embodied in computer program or machine-executable instructions, which may be used to cause a general-purpose or special-purpose processor or logic circuits programmed with the instructions to perform the processes. Alternatively, the processes may be performed by a combination of hardware and software.

[0058] Portions of various embodiments of the present invention may be provided as a computer program product, which may include a computer-readable medium having stored thereon computer program instructions, which may be used to program a computer (or other electronic devices) to perform a process according to the embodiments of the present invention. The machine-readable medium may include, but is not limited to, floppy diskettes, optical disks, compact disk read-only memory (CD-ROM), and magneto-optical disks, read-only memory (ROM), random access memory (RAM), erasable programmable read-only memory (EPROM), electrically-erasable programmable read-only memory (EEPROM), magnet or optical cards, flash memory, or other type of media/machine-readable medium suitable for storing electronic instructions. Moreover, the present invention may also be downloaded as a computer program product, wherein the program may be transferred from a remote computer to a requesting computer.

[0059] Many of the methods are described in their most basic form, but processes can be added to or deleted from any of the methods and information can be

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added or subtracted from any of the described messages without departing from the basic scope of the present invention. It will be apparent to those skilled in the art that many further modifications and adaptations can be made. The particular embodiments are not provided to limit the invention but to illustrate it. The scope of the embodiments of the present invention is not to be determined by the specific examples provided above but only by the claims below.

[0060] If it is said that an element "A" is coupled to or with element "B," element A may be directly coupled to element B or be indirectly coupled through, for example, element C. When the specification or claims state that a component, feature, structure, process, or characteristic A "causes" a component, feature, structure, process, or characteristic B, it means that "A" is at least a partial cause of "B" but that there may also be at least one other component, feature, structure, process, or characteristic that assists in causing "B." If the specification indicates that a component, feature, structure, process, or characteristic "may", "might", or "could" be included, that particular component, feature, structure, process, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, this does not mean there is only one of the described elements.

[0061] An embodiment is an implementation or example of the present invention. Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all

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referring to the same embodiments. It should be appreciated that in the foregoing description of exemplary embodiments of the present invention, various features are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed invention requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims are hereby expressly incorporated into this description, with each claim standing on its own as a separate embodiment of this invention.

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CLAIMS

What is claimed is:

1. A method comprising:

coupling a transmitting device to a receiving device, coupling of the devices including connecting a control bus between the transmitting device and the receiving device, the control bus being a bi-directional, single-line bus;

obtaining control of the control bus for either the transmitting device or the receiving device, the device obtaining control becoming an initiator and the other device becoming a follower;

converting one or more control signals to one or more data packets, each of the one or more control signals representing one of a plurality of different types of control signals; and

transmitting the generated data packets from the initiator to the follower via the control bus.

2. The method of claim 1, wherein the signaling for the control bus utilizes bi-phase mark encoding.

3. The method of claim 1, wherein obtaining control of the control bus includes arbitrating between the transmitting device and the control device for control of the control bus.

4. The method of claim 3, wherein, for the transmitting device, arbitrating for control of the control bus includes:

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determining the control bus is idle or unused for a certain period;

if the control bus is been idle or used, then sending a low signal for a first number of cycles; and

after the conclusion of the first number of cycles, then taking control the control bus.

5. The method of claim 3, wherein, for the receiving device, arbitrating for control of the control bus includes:

determining the control bus is idle or unused for a certain period;

if the control bus is idle or unused, then sending a low signal followed by a high signal for a first number of cycles;

during the first number of cycles, checking a status of the control bus;

if the status of the control bus is a high signal, taking control of the control bus.

6. The method of claim 1, wherein the receiving device is a device utilizing a standard protocol and the transmitting device is a device utilizing a modified protocol.

7. The method of claim 6, wherein the standard protocol is HDMI (High-Definition Multimedia Interface).

8. The method of claim 6, wherein the receiving device is a dual-mode device that is capable of communicating with a device that is compatible with the standard protocol device or a device that is compatible with the modified protocol.

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9. The method of claim 6, wherein the plurality of different types of control signals would be transmitted over a plurality of control buses according to the standard protocol.

10. The method of claim 1, wherein transmitting the data packets includes arbitrating between a plurality of requestors to place the data packets on the control bus.

11. A transmitting device comprising:

a connection to a single control bus, the control bus being a bi-directional, single-line bus, the transmitting device to be coupled with a receiving device via the control bus;

logic to convert each of one or more control signals into a data packet, each of the one or more control signals being one of a plurality of different types of control signals; and

a transmitter, the transmitter to transmit the data packets to the receiving device on the control bus.

12. The transmitting device of claim 11, wherein the transmitter is to drive the control bus in a bi-phase mark signaling manner.

13. The transmitting device of claim 11, wherein transmitting the one or more data packets includes transmitting a sync pulse to the receiving device to synchronize a clock of the receiving device to a clock of the transmitting device.

14. The transmitting device of claim 11, further comprising a switchable pull-up circuit coupled with the control bus.

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15. The transmitting device of claim 11, further comprising logic to arbitrate use of the control bus with the receiving device.

16. The transmitting device of claim 11, wherein the receiving device is a device utilizing a standard protocol and the transmitting device is a device utilizing a modified protocol.

17. The transmitting device of claim 16, wherein the standard protocol is HDMI (High-Definition Multimedia Interface).

18. The transmitting device of claim 11, further comprising a USB-OTG (Universal Serial Bus On-The-Go) PHY.

19. A receiving device comprising:

a connection to a single control bus, the control bus being a bi-directional, single-line bus, the receiving device to be coupled with a transmitting device via the control bus;

a receiver to receive one or more data packets on the control bus, each of the one or more data packets representing one of a plurality of different types of control signals; and

logic to convert each of the one or more data packets into a control signal.

20. The receiving device of claim 19, wherein the receiver is to decode the one or more received data packets according to bi-phase mark encoding.

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21. The receiving device of claim 19, wherein the receiver is to receive a sync pulse from the receiving device, the receiving device to synchronize a clock of the receiving device to a clock of the transmitting device.

22. The receiving device of claim 19, further comprising a switchable pull-down circuit coupled with the control bus.

23. The receiving device of claim 19, further comprising logic to arbitrate use of the control bus with the transmitting device.

24. The receiving device of claim 19, wherein the receiving device is a device utilizing a standard protocol and the transmitting device is a device utilizing a modified protocol.

25. The receiving device of claim 24, wherein the standard protocol is HDMI (High-Definition Multimedia Interface).

26. The receiving device of claim 24, wherein the receiving device is a dual-mode device that is capable of communicating with a standard protocol device or a modified protocol device.

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ABSTRACT

A method and apparatus for a control bus for connection of electronic devices. An embodiment of a method includes coupling a transmitting device to a receiving device, including connecting a control bus between the transmitting device and the receiving device, with the control bus being a bi-directional, single-line bus. The method further includes obtaining control of the control bus for either the transmitting device or the receiving device, with the device obtaining control becoming an initiator and the other device becoming a follower. One or more control signals are converted to one or more data packets, with each of the one or more control signals representing one of multiple different types of control signals. The generated data packets are transmitted from the initiator to the follower via the control bus.

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Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Shrikant Ranade
Filer:	Mark C. Van Ness/gayle bekish
Attorney Docket Number:	8029P038

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	310	310
Utility Search Fee	1111	1	510	510
Utility Examination Fee	1311	1	210	210
Pages:				
Claims:				
Claims in excess of 20	1202	6	50	300
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1330**

Electronic Acknowledgement Receipt

EFS ID:	2674270
Application Number:	11969852
International Application Number:	
Confirmation Number:	1782
Title of Invention:	CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Shrikant Ranade
Customer Number:	65702
Filer:	Mark C. Van Ness/gayle bekish
Filer Authorized By:	Mark C. Van Ness
Attorney Docket Number:	8029P038
Receipt Date:	04-JAN-2008
Filing Date:	
Time Stamp:	20:33:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1330
RAM confirmation Number	3411
Deposit Account	022666
Authorized User	

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Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		8029P038_Final_Patent_Application.pdf	147672 2a3da14eb45a453448ecb6960ba6aca19493381a	yes	30

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Specification	1	24
Claims	25	29
Abstract	30	30

Warnings:					
Information:					
2	Drawings-only black and white line drawings	8029P038_Final_Patent_Drawings.pdf	744589 14430619c14b90da283d9ac599b6c4dad2cce9de	no	9
Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	8476 00f751d820aa7a8d2b48e13ffb36899b6a803e09	no	2
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National Stage of an International Application under 35 U.S.C. 371
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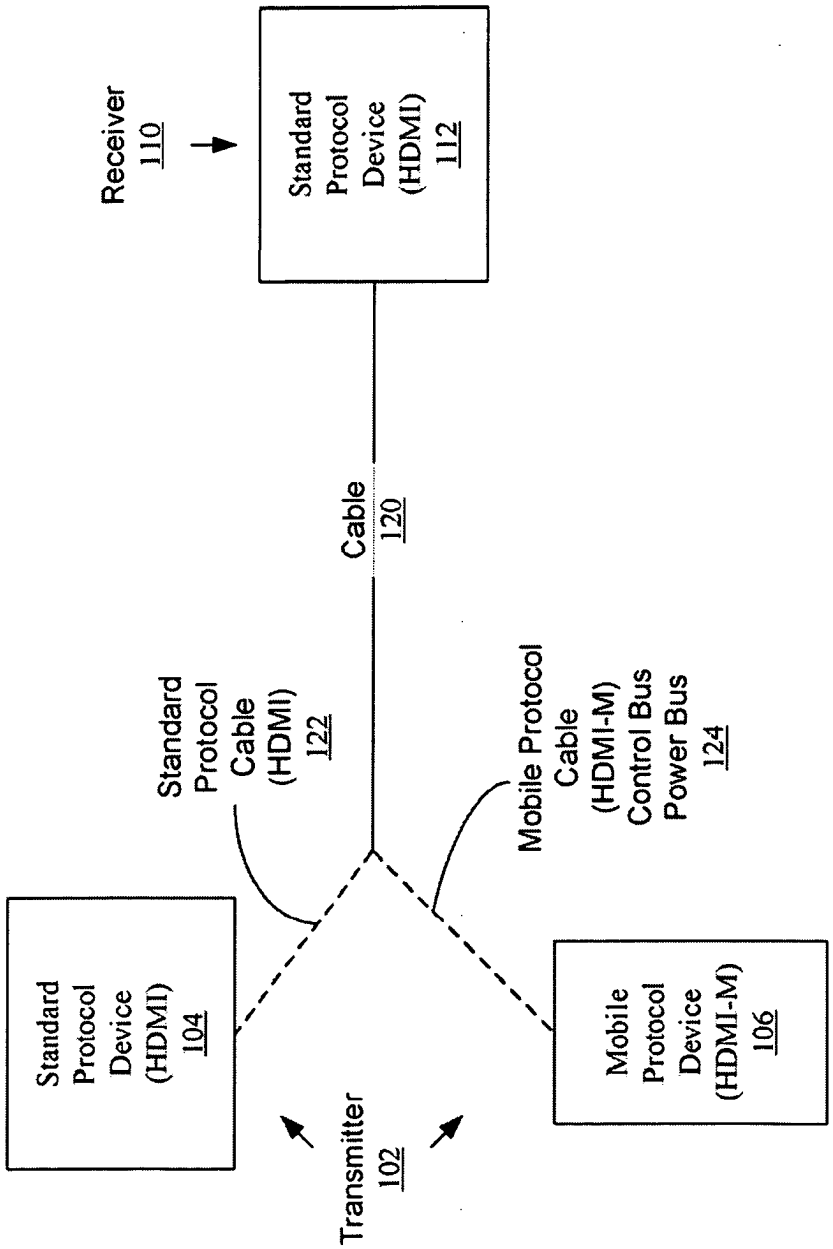

Receiver
110
Standard Protocol Device (HDMI)
112
Cable
120
Standard Protocol Cable (HDMI)
122
Mobile Protocol Cable (HDMI-M) Control Bus Power Bus
124
Standard Protocol Device (HDMI)
104
Transmitter
102
Mobile Protocol Device (HDMI-M)
106

Fig. 1

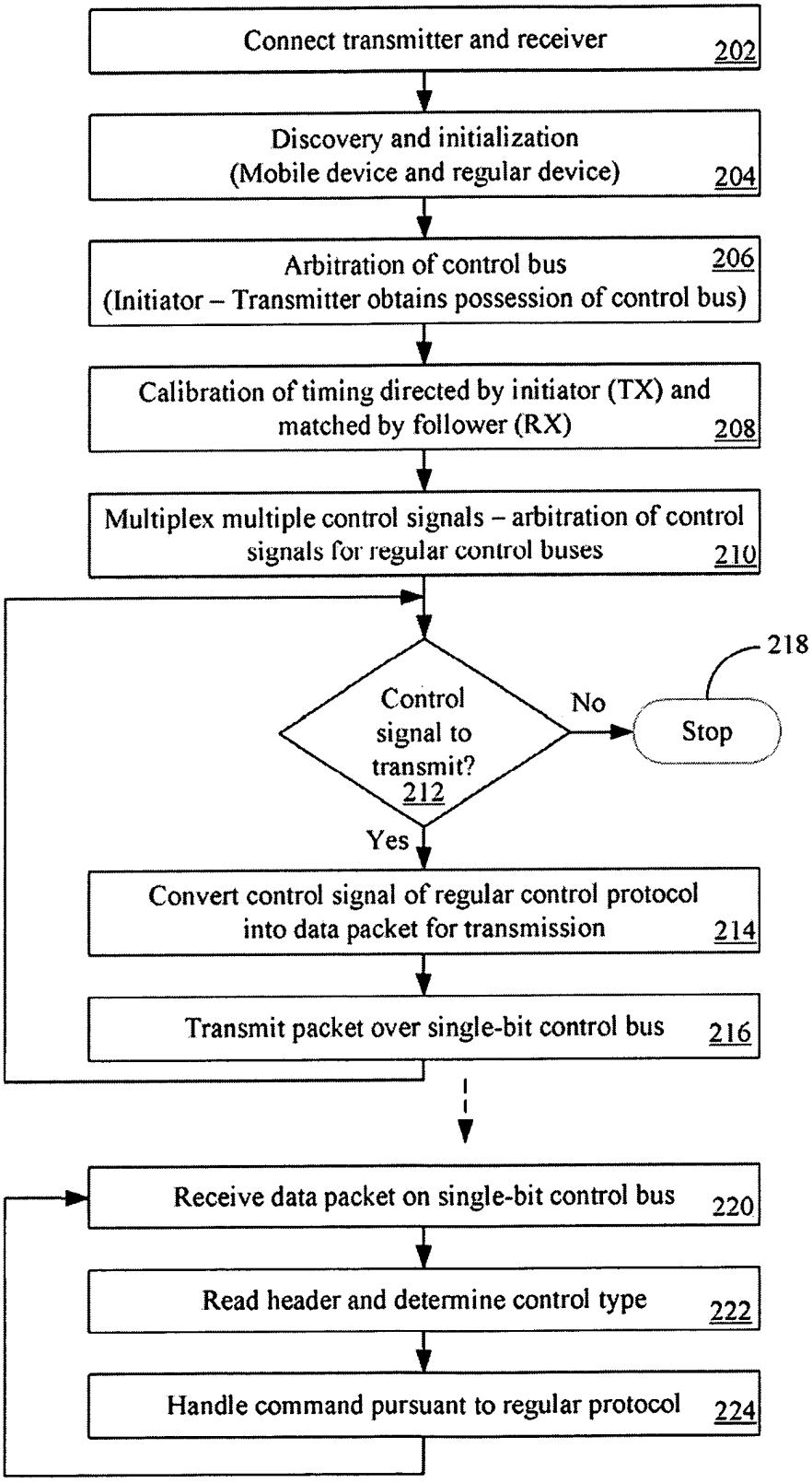

Connect transmitter and receiver 202
Discovery and initialization (Mobile device and regular device) 204
Arbitration of control bus 206
(Initiator – Transmitter obtains possession of control bus)
Calibration of timing directed by initiator (TX) and matched by follower (RX) 208
Multiplex multiple control signals – arbitration of control signals for regular control buses 210
Control signal to transmit? 212
No
Stop
218
Yes
Convert control signal of regular control protocol into data packet for transmission 214
Transmit packet over single-bit control bus 216
Receive data packet on single-bit control bus 220
Read header and determine control type 222
Handle command pursuant to regular protocol 224

Fig. 2

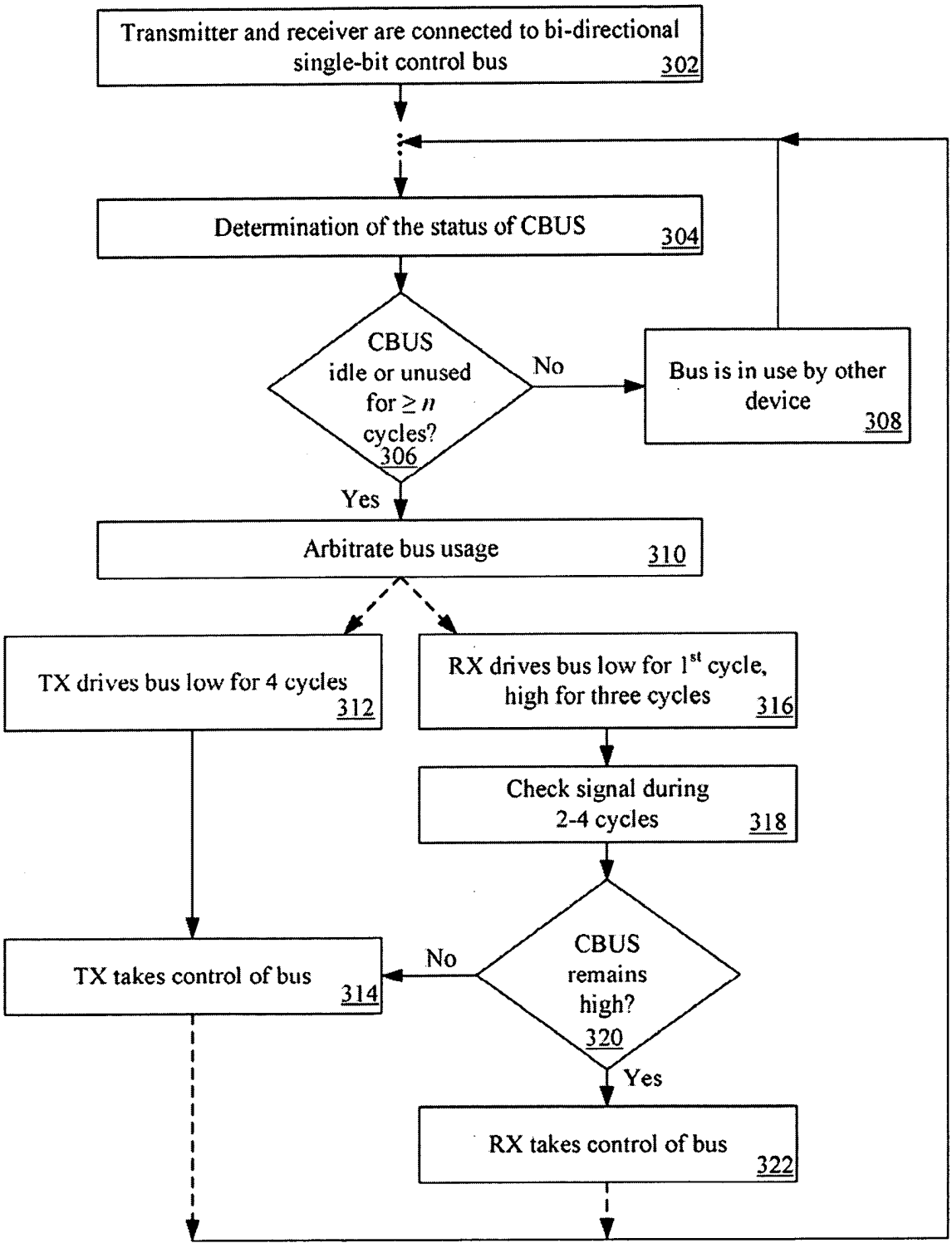

Transmitter and receiver are connected to bi-directional single-bit control bus 302
Determination of the status of CBUS 304
CBUS idle or unused for ≥ n cycles? 306
No
Bus is in use by other device 308
Yes
Arbitrate bus usage 310
TX drives bus low for 4 cycles 312
RX drives bus low for 1st cycle, high for three cycles 316
Check signal during 2-4 cycles 318
CBUS remains high? 320
No
TX takes control of bus 314
Yes
RX takes control of bus 322

Fig. 3

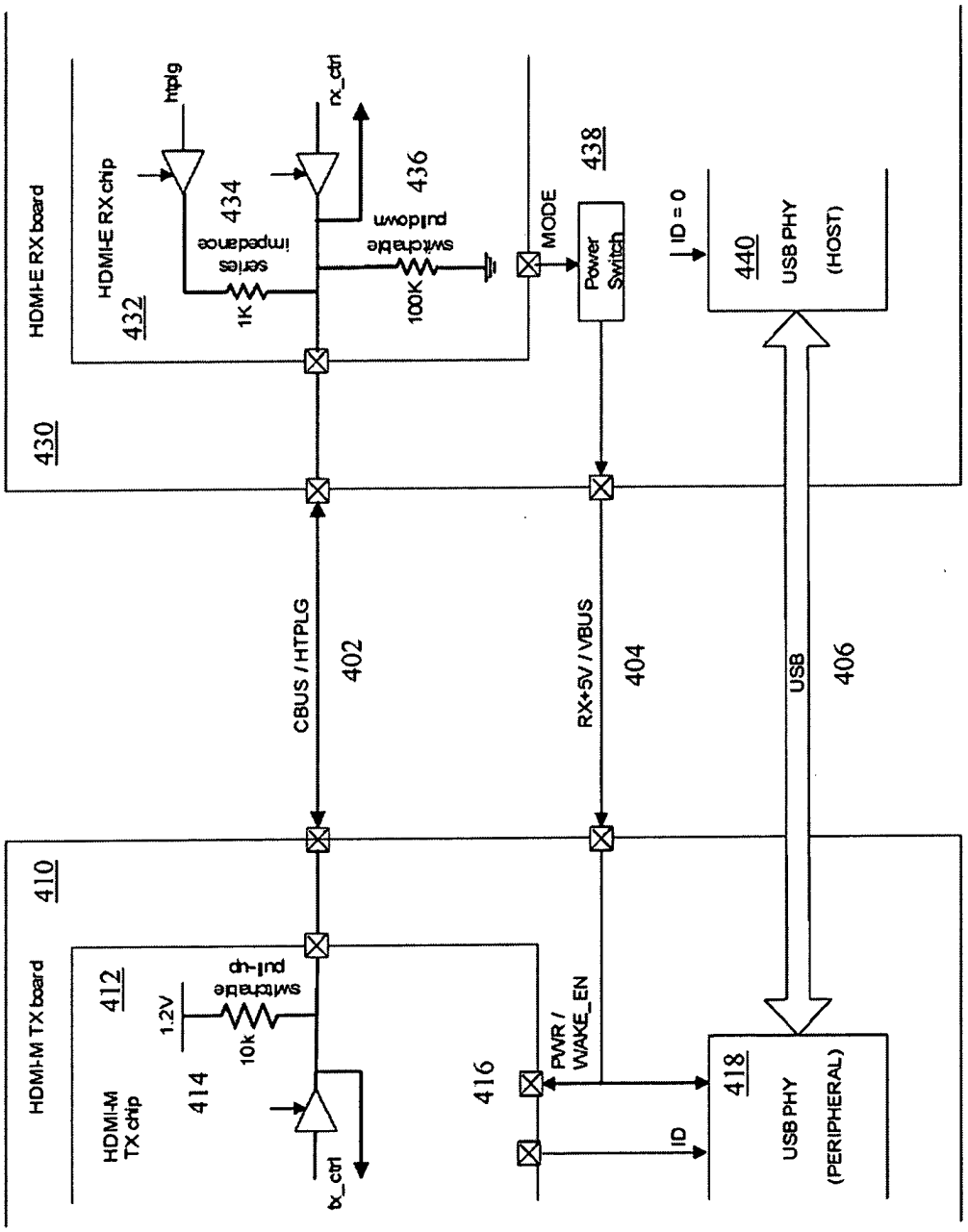

HDMI-E RX board
430
HDMI-E RX chip
432
htplg
rx_ctrl
434
436
series impedance
1K
switchable pulldown
100K
MODE
438
Power Switch
ID = 0
440
USB PHY
(HOST)
CBUS / HTPLG
402
RX+5V / VBUS
404
USB
406
HDMI-M TX board
410
HDMI-M TX chip
412
414
1.2V
switchable pull-up
10k
tx_ctrl
416
PWR / WAKE_EN
ID
418
USB PHY
(PERIPHERAL)

Fig. 4

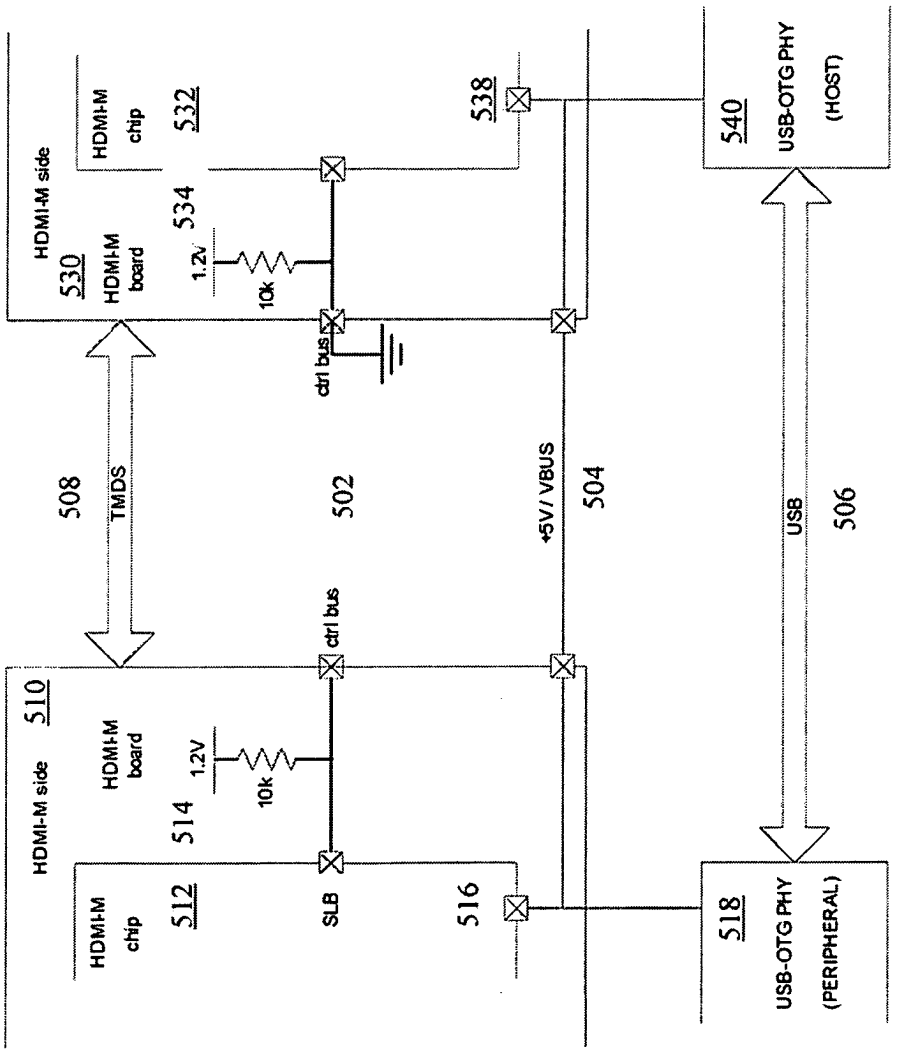
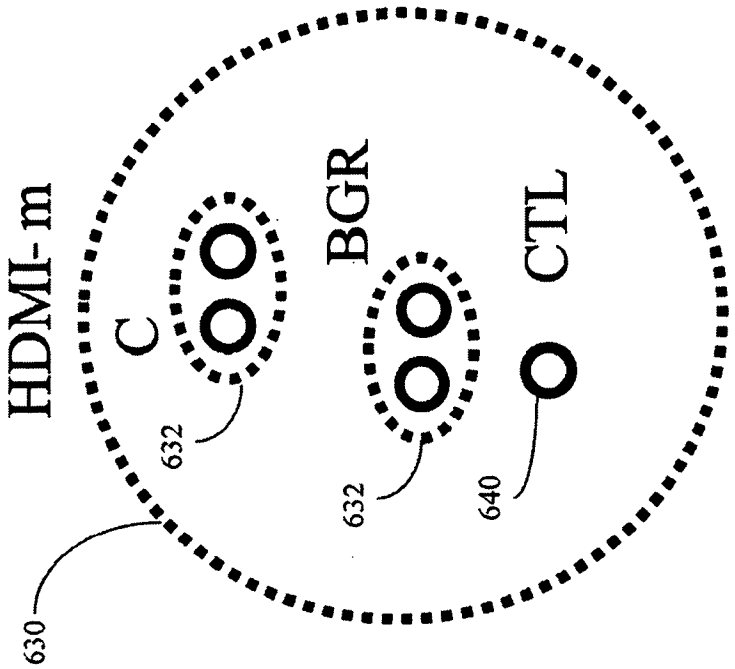

HDMI-M side
530
HDMI-M board
HDMI-M chip
532
534
1.2V
10k
ctrl bus
538
540
USB-OTG PHY
(HOST)
508
TMDS
502
+5V/ VBUS
504
USB
506
510
HDMI-M side
HDMI-M board
1.2V
10k
514
ctrl bus
HDMI-M chip
512
SLB
516
518
USB-OTG PHY
(PERIPHERAL)

Fig. 5


HDMI- m
C
BGR
CTL
632
632
640
630

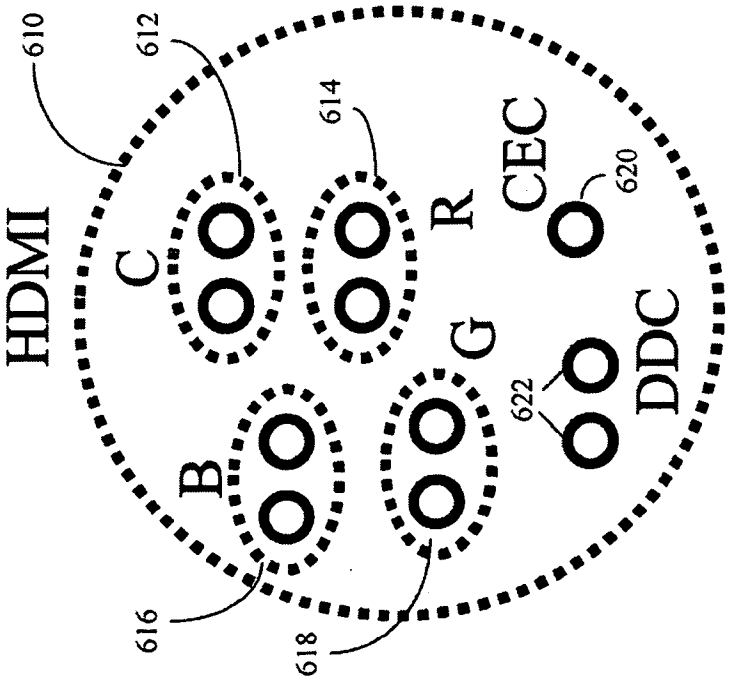

HDMI
C
B
R
G
CEC
DDC
610
612
614
616
618
620
622

Fig. 6

710 720 730

PIN	HDMI-M Signal assignment	Standard HDMI Signal assignment
1	NC	TMDS Data2+
2	NC	TMDS Data2 Shield
3	NC	TMDS Data2-
4	NC	TMDS Data1+
5	NC	TMDS Data1 Shield
6	NC	TMDS Data1-
7	TMDS Data+	TMDS Data0+
8	TMDS Data Shield	TMDS Data0 Shield
9	TMDS Data-	TMDS Data0-
10	TMDS Clock+	TMDS Clock+
11	TMDS Clock Shield	TMDS Clock Shield
12	TMDS Clock-	TMDS Clock-
13	NC	CEC
14	5V power from RX	Reserved (NC)
15	USB Data+	DDC SCL
16	USB Data-	DDC SDA
17	GND	DDC/CEC GND
18	NC	+5V power from TX
19	Ctrl Bus	Hot Plug Detect

Fig. 7

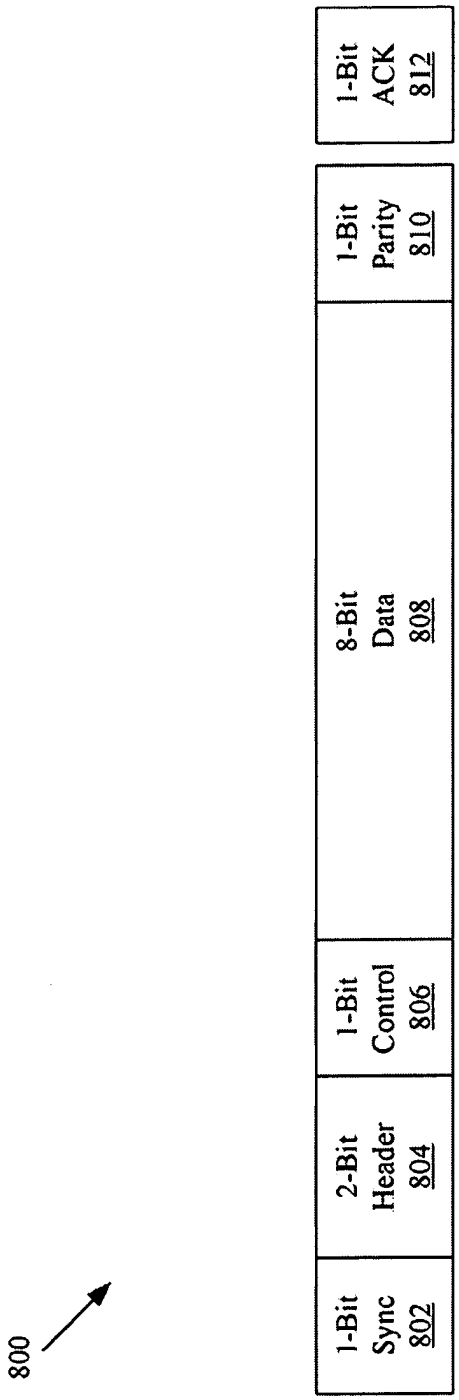

800
1-Bit Sync 802
2-Bit Header 804
1-Bit Control 806
8-Bit Data 808
1-Bit Parity 810
1-Bit ACK 812

Fig. 8

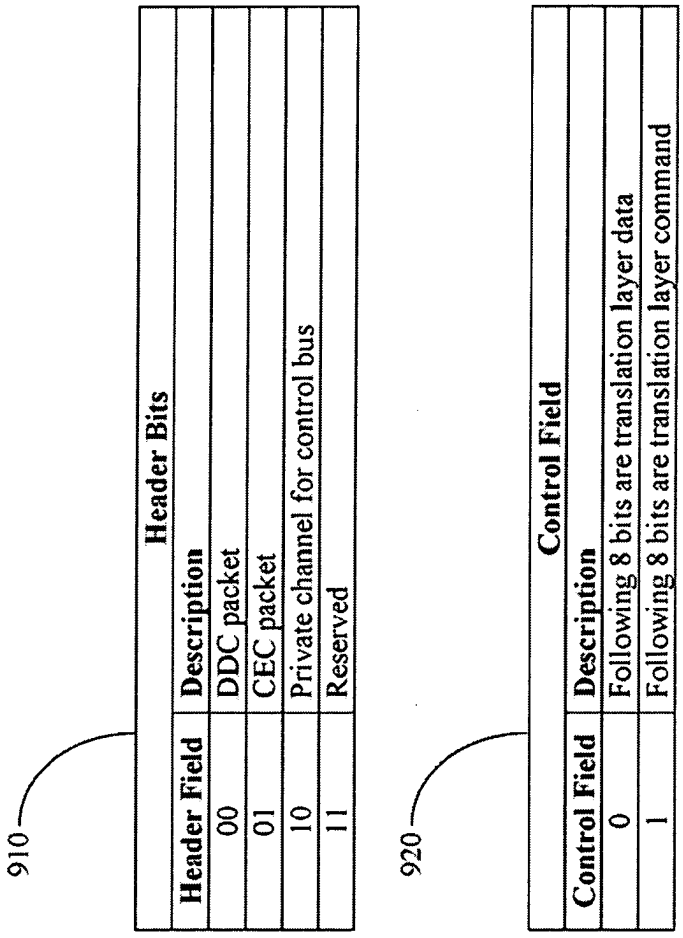

910
Header Bits
Header Field
Description
00
DDC packet
01
CEC packet
10
Private channel for control bus
11
Reserved
920
Control Field
Control Field
Description
0
Following 8 bits are translation layer data
1
Following 8 bits are translation layer command

Fig. 9

PTO/SB/06 (12-04)

01/04/08

Approved for use through 7/31/2006. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 11/969,852

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	**310**
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	**510**
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	**210**
TOTAL CLAIMS (37 CFR 1.16(i))	**26** minus 20 =	* **6**	X 25=		OR	X 50=	**300**
INDEPENDENT CLAIMS (37 CFR 1.16(h))	**3** minus 3 =	*	X 105=			X 210=	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $260 ($130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			N/A			N/A	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	**1330**

APPLICATION AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/969,852	01/04/2008	Shrikant Ranade	8029P038

CONFIRMATION NO. 1782

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025-1026

FORMALITIES LETTER

OC000000027888273

Date Mailed: 01/25/2008

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of $**130** for a non-small entity, must be submitted with the missing items identified in this notice.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is $**130** for a non-small entity
- $**130** Surcharge.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
11/969,852	01/04/2008	2111	1330	8029P038	26	3

CONFIRMATION NO. 1782

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025-1026

FILING RECEIPT



Date Mailed: 01/25/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Shrikant Ranade, Residence Not Provided;

Power of Attorney: None

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 01/23/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 11/969,852**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

LENOVO EXHIBIT 1002 - 47/502

Title

CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES

Preliminary Class

710

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

LENOVO EXHIBIT 1002 - 48/502

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

LENOVO EXHIBIT 1002 - 49/502

Electronic Patent Application Fee Transmittal

Application Number:	11969852
Filing Date:	04-Jan-2008
Title of Invention:	CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Shrikant Ranade
Filer:	Mark C. Van Ness
Attorney Docket Number:	8029P038

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Late filing fee for oath or declaration	1051	1	130	130
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**130**

Electronic Acknowledgement Receipt

EFS ID:	2993044
Application Number:	11969852
International Application Number:	
Confirmation Number:	1782
Title of Invention:	CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Shrikant Ranade
Correspondence Address:	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP - SEVENTH FLOOR 12400 WILSHIRE BOULEVARD LOS ANGELES CA 90025-1026 US 503 439 8778 -
Filer:	Mark C. Van Ness/gayle bekish
Filer Authorized By:	Mark C. Van Ness
Attorney Docket Number:	8029P038
Receipt Date:	13-MAR-2008
Filing Date:	04-JAN-2008
Time Stamp:	13:54:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$130

RAM confirmation Number	10461
Deposit Account	022666
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	8029P038_Response_MP_03132008.pdf	344140 32c4e78cbba12bbb558d11f8ad5cc90adf8b9685	no	3
Warnings:					
Information:					
2	Oath or Declaration filed	8029P038_Signed_Declaration.pdf	653457 d09b08067d2cb1767b91c06eaa697b7a29f2db3a	no	4
Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	8155 0add3b9289d6f1e1811181ac84eea68c04652d50	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1005752		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

ATTORNEY DOCKET NO.: 8029P038

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

SHRIKANT RANADE, ET AL.

Application No.: 11/969852

Filed: January 4, 2008

For: **CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES**

Art Group: TBD

Examiner: TBD

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE TO FILE MISSING PARTS

Sir:

In response to the Notice to File Missing Parts mailed January 25, 2008, please find enclosed:

- a duly executed Declaration and Power of Attorney with payment in the amount of $130.00 for the surcharge of 37 CFR § 1.16(e);

and

- copy of the Notice to File Missing Parts of Application.

If any additional fee is required, please charge Deposit Account No. 02-2666. An extra copy of the Fee Transmittal is enclosed for deposit account charging purposes.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: March 13, 2008

/Mark C. Van Ness/

Mark C. Van Ness, Reg. No. 39,865

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
Telephone: (503) 439-8778

/Gayle Bekish/ 03/13/08

Gayle Bekish *Date*

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
PO Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/969,852	01/04/2008	Shrikant Ranade	8029P038

CONFIRMATION NO. 1782

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025-1026

FORMALITIES LETTER



Date Mailed: 01/25/2008

JAN 2 5 2008

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of **$130** for a non-small entity, must be submitted with the missing items identified in this notice.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$130** for a non-small entity
- **$130** Surcharge.

JAN 30 2008

LENOVO EXHIBIT 1002 - 55/502

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/fly/

Office of Initial Patent Examination (571) 272-4000 or 1-800-PTO-9199

LENOVO EXHIBIT 1002 - 56/502

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (37 CFR 1.63)		
☐ Declaration Submitted with Initial Filing OR ☒ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16(e)) required)	Attorney Docket Number	8029P038
	First Named Inventor	Shrikant Ranade
	COMPLETE IF KNOWN	
	Application Number	11/969852
	Filing Date	January 4, 2008
	Art Unit	TBD
	Examiner Name	TBD

As a below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below, next to my name.

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES

(Title of the Invention)

the specification of which

☐ is attached hereto.

OR

☒ was filed on (if applicable):

or 01/04/2008 as United States Application Number 11/969852

as PCT International Application Number _____

and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment specifically referred to above.

I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application. I do not know and do not believe that the claimed invention was in public use or on sale in the United States of America more than one year prior to this application, nor do I know or believe that the invention has been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

LENOVO EXHIBIT 1002 - 57/502

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, or inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s):

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?
			☐	☐ Yes ☐ No
			☐	☐ Yes ☐ No
			☐	☐ Yes ☐ No
			☐	☐ Yes ☐ No
			☐	☐ Yes ☐ No

Appointment of Practitioners:
I hereby appoint the practitioners associated with Customer Number: **65702** as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected herewith.

If this patent application is assigned, then the undersigned hereby authorizes the patent attorneys and patent agents named herein to accept and follow instructions from the assignee(s) as to any action to be taken in the United States Patent and Trademark Office regarding this application without direct communication between the patent attorneys and patent agents and the undersigned. In the event of a change in the persons from whom instructions may be taken, at least one patent attorney or patent agent named herein will be so notified by the undersigned.

Correspondence:
Direct all correspondence to Customer Number **65702**,

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

NAME OF SOLE OR FIRST INVENTOR: ☐ A petition has been filed for this undersigned inventor

Full Name: **Shrikant Ranade**
(First, Middle [if any], Family Name (or Surname), and Suffix [if any])

Inventor's Signature S. Ranade Date 2/7/2008

Residence Campbell, California United States Citizenship United States
(City, State, Country) *(Country)*

Mailing Address 917 Kara Way
Campbell, California 95008 United States

LENOVO EXHIBIT 1002 - 58/502

NAME OF SECOND INVENTOR: ☐ A petition has been filed for this undersigned inventor

Full Name: Alexander Peysakhovich
(First, Middle [if any], Family Name (or Surname), and Suffix [if any])

Inventor's Signature [signature] Date 2-7-08

Residence San Jose, California United States Citizenship United States
(City, State, Country) *(Country)*

Mailing Address 1975 Catrina Court
San Jose, California 95124 United States

NAME OF THIRD INVENTOR: ☐ A petition has been filed for this undersigned inventor

Full Name: Hyuck Jae Lee
(First, Middle [if any], Family Name (or Surname), and Suffix [if any])

Inventor's Signature [signature] Date 2-7-08

Residence San Francisco, California United States Citizenship Korea
(City, State, Country) *(Country)*

Mailing Address 301 Parnassus Ave, #202
San Francisco, California 94117 United States

NAME OF FOURTH INVENTOR: ☐ A petition has been filed for this undersigned inventor

Full Name: Hoon Choi
(First, Middle [if any], Family Name (or Surname), and Suffix [if any])

Inventor's Signature [signature] Date 2/7/2008

Residence Mountain View, California United States Citizenship Korea
(City, State, Country) *(Country)*

Mailing Address 49 Showers Drive, No. C455
Mountain View, California 94040 United States

NAME OF FIFTH INVENTOR: ☐ A petition has been filed for this undersigned inventor

Full Name:
(First, Middle [if any], Family Name (or Surname), and Suffix [if any])

Inventor's Signature Date

Residence Citizenship
(City, State, Country) *(Country)*

Mailing Address

LENOVO EXHIBIT 1002 - 59/502

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
11/969,852	01/04/2008	2111	1460	8029P038	26	3

CONFIRMATION NO. 1782

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025-1026

UPDATED FILING RECEIPT



Date Mailed: 03/20/2008

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Applicant(s)

Shrikant Ranade, Campbell, CA;
Alexander Peysakhovich, San Jose, CA;
Hyuck Jae Lee, San Francisco, CA;
Hoon Choi, Mountain View, CA;

Power of Attorney: The patent practitioners associated with Customer Number 65702

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 01/23/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 11/969,852**

Projected Publication Date: 07/09/2009

Non-Publication Request: No

Early Publication Request: No

LENOVO EXHIBIT 1002 - 60/502

Title

CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES

Preliminary Class

710

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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LENOVO EXHIBIT 1002 - 61/502

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

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The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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UNITED STATES PATENT AND TRADEMARK OFFICE

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Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/969,852	01/04/2008	Shrikant Ranade	8029P038

CONFIRMATION NO. 1782

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA90025-1026

Date Mailed. 03/20/2008

NOTICE OF NEW OR REVISED PROJECTED PUBLICATION DATE

The above-identified application has a new or revised projected publication date. The current projected publication date for this application is 07/09/2009. If this is a new projected publication date (there was no previous projected publication date), the application has been cleared by Licensing & Review or a secrecy order has been rescinded and the application is now in the publication queue.

If this is a revised projected publication date (one that is different from a previously communicated projected publication date), the publication date has been revised due to processing delays in the USPTO or the abandonment and subsequent revival of an application. The application is anticipated to be published on a date that is more than six weeks different from the originally-projected publication date.

More detailed publication information is available through the private side of Patent Application Information Retrieval (PAIR) System. The direct link to access PAIR is currently http://pair.uspto.gov. Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Questions relating to this Notice should be directed to the Office of Patent Publication at 1-888-786-0101.

PART 1 - ATTORNEY/APPLICANT COPY

PATENT COOPERATION TREATY

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From the INTERNATIONAL SEARCHING AUTHORITY

PCT

To:
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Attn. Vincent, Lester J.
1279 Oakmead Parkway
Sunnyvale CA 94085-4040
ETATS-UNIS D'AMERIQUE

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Applicant's or agent's file reference 8029P038PCT	Date of mailing *(day/month/year)* 09/03/2009 **FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US2008/085288	International filing date *(day/month/year)* 02/12/2008
Applicant SILICON IMAGE, INC.	

1. [x] The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the International Application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the International Search Report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Fascimile No.: (41-22) 338.82.70

   For more detailed instructions, see the notes on the accompanying sheet.

2. [ ] The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. [ ] **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   [ ] the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   [ ] no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the International Searching Authority	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Victoria Strijdhagen-Namagembe 3-11-09

Form PCT/ISA/220 (October 2005) *(See notes on accompanying sheet)*

NOTES TO FORM PCT/ISA/220

These Notes are intended to give the basic instructions concerning the filing of amendments under article 19. The Notes are based on the requirements of the Patent Cooperation Treaty, the Regulations and the Administrative Instructions under that Treaty. In case of discrepancy between these Notes and those requirements, the latter are applicable. For more detailed information, see also the *PCT Applicant's Guide*, a publication of WIPO.

In these Notes, "Article", "Rule", and "Section" refer to the provisions of the PCT, the PCT Regulations and the PCT Administrative Instructions, respectively.

INSTRUCTIONS CONCERNING AMENDMENTS UNDER ARTICLE 19

The applicant has, after having received the international search report and the written opinion of the International Searching Authority, one opportunity to amend the claims of the international application. It should however be emphasized that, since all parts of the international application (claims,description and drawings) may be amended during the international preliminary examination procedure, there is usually no need to file amendments of the claims under Article 19 except where, e.g. the applicant wants the latter to be published for the purposes of provisional protection or has another reason for amending the claims before international publication. Furthermore, it should be emphasized that provisional protection is available in some States only (see *PCT Applicant's Guide*, Volume I/A, Annexes B1 and B2).

The attention of the applicant is drawn to the fact that amendments to the claims under Article 19 are not allowed where the International Searching Authority has declared, under Article 17(2), that no international search report would be established (see *PCT Applicant's Guide*, Volume I/A, paragraph 296).

What parts of the international application may be amended?

Under Article 19, only the claims may be amended.

During the international phase, the claims may also be amended (or further amended) under Article 34 before the International Preliminary Examining Authority. The description and drawings may only be amended under Article 34 before the International Examining Authority.

Upon entry into the national phase, all parts of the international application may be amended under Article 28 or, where applicable, Article 41.

When? Within 2 months from the date of transmittal of the international search report or 16 months from the priority date, whichever time limit expires later. It should be noted, however, that the amendments will be considered as having been received on time if they are received by the International Bureau after the expiration of the applicable time limit but before the completion of the technical preparations for international publication (Rule 46.1).

Where not to file the amendments?

The amendments may only be filed with the International Bureau and not with the receiving Office or the International Searching Authority (Rule 46.2).

Where a demand for international preliminary examination has been/is filed, see below.

How? Either by cancelling one or more entire claims, by adding one or more new claims or by amending the text of one or more of the claims as filed.

A replacement sheet must be submitted for each sheet of the claims which, on account of an amendment or amendments, differs from the sheet originally filed.

All the claims appearing on a replacement sheet must be numbered in Arabic numerals. Where a claim is cancelled, no renumbering of the other claims is required. In all cases where claims are renumbered, they must be renumbered consecutively (Section 205(b)).

The amendments must be made in the language in which the international application is to be published.

What documents must/may accompany the amendments?

Letter (Section 205(b)):

The amendments must be submitted with a letter.

The letter will not be published with the international application and the amended claims. It should not be confused with the "Statement under Article 19(1)" (see below, under "Statement under Article 19(1)").

The letter must be in English or French, at the choice of the applicant. However, if the language of the international application is English, the letter must be in English; if the language of the international application is French, the letter must be in French.

NOTES TO FORM PCT/ISA/220 (continued)

The letter must indicate the differences between the claims as filed and the claims as amended. It must, in particular, indicate, in connection with each claim appearing in the international application (it being understood that identical indications concerning several claims may be grouped),whether

(i) the claim is unchanged;

(ii) the claim is cancelled;

(iii) the claim is new;

(iv) the claim replaces one or more claims as filed;

(v) the claim is the result of the division of a claim as filed.

The following examples illustrate the manner in which amendments must be explained in the accompanying letter:

1. [Where originally there were 48 claims and after amendment of some claims there are 51]:
"Claims 1 to 29, 31, 32, 34, 35, 37 to 48 replaced by amended claims bearing the same numbers; claims 30, 33 and 36 unchanged; new claims 49 to 51 added."

2. [Where originally there were 15 claims and after amendment of all claims there are 11]:
"Claims 1 to 15 replaced by amended claims 1 to 11."

3. [Where originally there were 14 claims and the amendments consist in cancelling some claims and in adding new claims]:
"Claims 1 to 6 and 14 unchanged; claims 7 to 13 cancelled; new claims 15, 16 and 17 added." or
"Claims 7 to 13 cancelled; new claims 15, 16 and 17 added; all other claims unchanged."

4. [Where various kinds of amendments are made]:
"Claims 1–10 unchanged; claims 11 to 13, 18 and 19 cancelled; claims 14, 15 and 16 replaced by amended claim 14; claim 17 subdivided into amended claims 15, 16 and 17; new claims 20 and 21 added."

"Statement under article 19(1)" (Rule 46.4)

The amendments may be accompanied by a statement explaining the amendments and indicating any impact that such amendments might have on the description and the drawings (which cannot be amended under Article 19(1)).

The statement will be published with the international application and the amended claims.

It must be in the language in which the international application is to be published.

It must be brief, not exceeding 500 words if in English or if translated into English.

It should not be confused with and does not replace the letter indicating the differences between the claims as filed and as amended. It must be filed on a separate sheet and must be identified as such by a heading, preferably by using the words "Statement under Article 19(1)."

It may not contain any disparaging comments on the international search report or the relevance of citations contained in that report. Reference to citations, relevant to a given claim, contained in the international search report may be made only in connection with an amendment of that claim.

Consequence if a demand for international preliminary examination has already been filed

If, at the time of filing any amendments and any accompanying statement, under Article 19, a demand for international preliminary examination has already been submitted, the applicant must preferably, at the time of filing the amendments (and any statement) with the International Bureau, also file with the International Preliminary Examining Authority a copy of such amendments (and of any statement) and, where required, a translation of such amendments for the procedure before that Authority (see Rules 55.3(a) and 62.2, first sentence). For further information, see the Notes to the demand form (PCT/IPEA/401).

If a demand for international preliminary examination is made, the written opinion of the International Searching Authority will, except in certain cases where the International Preliminary Examining Authority did not act as International Searching Authority and where it has notified the International Bureau under Rule 66.1*bis*(b), be considered to be a written opinion of the International Preliminary Examining Authority. If a demand is made, the applicant may submit to the International Preliminary Examining Authority a reply to the written opinion together, where appropriate, with amendments before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later (Rule 43*bis*.1(c)).

Consequence with regard to translation of the international application for entry into the national phase

The applicant's attention is drawn to the fact that, upon entry into the national phase, a translation of the claims as amended under Article 19 may have to be furnished to the designated/elected Offices, instead of, or in addition to, the translation of the claims as filed.

For further details on the requirements of each designated/elected Office, see the *PCT Applicant's Guide*, Volume II.

LENOVO EXHIBIT 1002 - 66/502

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
8029P038PCT		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2008/085288	02/12/2008	04/01/2008
Applicant		
SILICON IMAGE, INC.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language,** the international search was carried out on the basis of:
      [X] the international application in the language in which it was filed
      [ ] a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. [ ] This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. [ ] With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. [ ] **Certain claims were found unsearchable** (See Box No. II)

3. [ ] **Unity of invention is lacking** (see Box No III)

4. With regard to the **title,**
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority

6. With regard to the **drawings,**
   a. the figure of the **drawings** to be published with the abstract is Figure No. 1
      [ ] as suggested by the applicant
      [X] as selected by this Authority, because the applicant failed to suggest a figure
      [ ] as selected by this Authority, because this figure better characterizes the invention
   b. [ ] none of the figures is to be published with the abstract

LENOVO EXHIBIT 1002 - 67/502

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/085288

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F3/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F G09G H04N H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and. where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/286246 A1 (KOBAYASHI OSAMU [US]) 13 December 2007 (2007-12-13) paragraphs [0072], [0116]; figure 30 paragraph [0075] - paragraph [0076] paragraph [0067] figures 18,19	1-26
X	EP 1 473 701 A (GENESIS MICROCHIP INC [US]) 3 November 2004 (2004-11-03) figures 12,14,18,19	1-4
A	US 7 187 307 B1 (SCHMIDT BRIAN K [US] ET AL) 6 March 2007 (2007-03-06)	

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 February 2009	09/03/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Le Chapelain, B

Form PCT/ISA/210 (second sheet) (April 2005)

LENOVO EXHIBIT 1002 - 68/502

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2008/085288

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007286246 A1	13-12-2007	CN 101303639 A	12-11-2008
		EP 1990797 A1	12-11-2008
		JP 2009009106 A	15-01-2009
		KR 20080100147 A	14-11-2008
		SG 148091 A1	31-12-2008
EP 1473701 A	03-11-2004	CN 1551626 A	01-12-2004
		JP 2005018743 A	20-01-2005
		KR 20040094615 A	10-11-2004
		SG 135028 A1	28-09-2007
		US 2004221315 A1	04-11-2004
US 7187307 B1	06-03-2007	NONE	

LENOVO EXHIBIT 1002 - 69/502

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY
(PCT Rule 43*bis*.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2008/085288	02.12.2008	04.01.2008

International Patent Classification (IPC) or both national classification and IPC
INV. G06F3/14

Applicant
SILICON IMAGE, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☒ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA:

European Patent Office - P.B. 5818 Patentlaan 2
NL-2280 HV Rijswijk - Pays Bas
Tel. +31 70 340 - 2040 Tx: 31 651 epo nl
Fax: +31 70 340 - 3016

Date of completion of this opinion
see form PCT/ISA/210

Authorized Officer

Le Chapelain, B

Telephone No. +31 70 340-9545

LENOVO EXHIBIT 1002 - 70/502

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material:

      ☐ a sequence listing

      ☐ table(s) related to the sequence listing

   b. format of material:

      ☐ on paper

      ☐ in electronic form

   c. time of filing/furnishing:

      ☐ contained in the international application as filed.

      ☐ filed together with the international application in electronic form.

      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Box No. II Priority

1. ☒ The validity of the priority claim has not been considered because the International Searching Authority does not have in its possession a copy of the earlier application whose priority has been claimed or, where required, a translation of that earlier application. This opinion has nevertheless been established on the assumption that the relevant date (Rules 43*bis*.1 and 64.1) is the claimed priority date.

2. ☐ This opinion has been established as if no priority had been claimed due to the fact that the priority claim has been found invalid (Rules 43*bis*.1 and 64.1). Thus for the purposes of this opinion, the international filing date indicated above is considered to be the relevant date.

3. Additional observations, if necessary:

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	4,5,7-10,14,17-18,22,25-26
	No:	Claims	1-3, 6,11-13,15,16,19,20,21,23,24
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-26
Industrial applicability (IA)	Yes:	Claims	1-26
	No:	Claims	

2. Citations and explanations

see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1 Reference is made to the following documents:
D1 : US 2007/286246 A1 (KOBAYASHI OSAMU [US]) 13 December 2007 (2007-12-13)

2 INDEPENDENT CLAIM 1

The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claim 1 is not new in the sense of Article 33(2) PCT.

2.1 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claim 1 is not new in the sense of Article 33(2) PCT.

Document D1 discloses (the references in parentheses applying to this document):

coupling a transmitting device (fig. 30: 3002) to a receiving device (fig. 30: 3004), coupling of the devices including connecting a control bus between the transmitting device and the receiving device, the control bus being a bi-directional (fig. 30: 3014), single-line bus (par. 72; fig. 14);

obtaining control of the control bus for either the transmitting device or the receiving device, the device obtaining control becoming an initiator and the other device becoming a follower (par. 116; claim 19);

converting one or more control signals to one or more data packets, each of the one or more control signals representing one of a plurality of different types of control signals (par. 75, 76); and

transmitting the generated data packets from the initiator to the follower via the control bus (par. 67; fig. 30: 3014).

The subject-matter of claim 1 is therefore known from D1.

3 DEPENDENT CLAIMS 2-10

Dependent claims 2-10 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty

and/or inventive step, see document D1 and the corresponding passages cited in the search report.

3.1 CLAIM 2
Document D1 further discloses the signalling for the control bus utilizes bi-phase mark encoding (par. 72, MANCHESTER encoding).
The subject-matter of claim 2 is therefore known from D1.

3.2 CLAIM 3
Document D1 further discloses obtaining control of the control bus includes arbitrating between the transmitting device and the control device for control of the control bus (par. 67: traffic, bandwidth).
The subject-matter of claim 3 is therefore known from D1.

3.3 CLAIMS 4-5
Document D1 further discloses some states machines to activate/de-activate control bus (fig. 18,19).

3.4 CLAIMS 6-10
Document D1 further discloses utilizing a standard protocol (display port) and the transmitting device is a device utilizing a modified protocol (USB) (par. 116).
Document D1 doest not disclose the standard protocol is HDMI but the person skilled in the art knowing D1 would adapted the knowledge of D1 to a HDMI interface without inventive skills and according to the situation.

4 CLAIMS 11-26
The subject-matter of claims 11-26 refers to transmitting device and a receiving device for video and substantially correspond to the subject-matter of claims 1-10. The reasoning given in par. 1-3.4 above therefore applies to claims 11-26 accordingly.
The subject-matter of 11-26 is therefore obvious/known from D1.

Possible steps after receipt of the international search report (ISR) and written opinion of the International Searching Authority (WO-ISA)

General information	For all international applications filed on or after 01/01/2004 the competent ISA will establish an ISR. It is accompanied by the WO-ISA. Unlike the former written opinion of the IPEA (Rule 66.2 PCT), the WO-ISA is not meant to be responded to, but to be taken into consideration for further procedural steps. This document explains about the possibilities.
Amending claims under Art. 19 PCT	Within 2 months after the date of mailing of the ISR and the WO-ISA the applicant may file amended claims under Art. 19 PCT directly with the International Bureau of WIPO. The PCT reform of 2004 did not change this procedure. For further information please see Rule 46 PCT as well as form PCT/ISA/220 and the corresponding Notes to form PCT/ISA/220.
Filing a demand for international preliminary examination	In principle, the WO-ISA will be considered as the written opinion of the IPEA. This should, in many cases, make it unnecessary to file a demand for international preliminary examination. If the applicant nevertheless wishes to file a demand this must be done before expiry of 3 months after the date of mailing of the ISR/WO-ISA or 22 months after priority date, whichever expires later (Rule 54bis PCT). Amendments under Art. 34 PCT can be filed with the IPEA as before, normally at the same time as filing the demand (Rule 66.1 (b) PCT). If a demand for international preliminary examination is filed and no comments/amendments have been received the WO-ISA will be transformed by the IPEA into an IPRP (International Preliminary Report on Patentability) which would merely reflect the content of the WO-ISA. The demand can still be withdrawn (Art. 37 PCT).
Filing informal comments	After receipt of the ISR/WO-ISA the applicant may file informal comments on the WO-ISA directly with the International Bureau of WIPO. These will be communicated to the designated Offices together with the IPRP (International Preliminary Report on Patentability) at 30 months from the priority date. Please also refer to the next box.
End of the international phase	At the end of the international phase the International Bureau of WIPO will transform the WO-ISA or, if a demand was filed, the written opinion of the IPEA into the IPRP, which will then be transmitted together with possible informal comments to the designated Offices. The IPRP replaces the former IPER (international preliminary examination report).
Relevant PCT Rules and more information	Rule 43 PCT, Rule 43bis PCT, Rule 44 PCT, Rule 44bis PCT, PCT Newsletter 12/2003, OJ 11/2003, OJ 12/2003

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 473 701 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
03.11.2004 Bulletin 2004/45

(51) Int Cl.[7]: **G09G 5/00**

(21) Application number: **04252205.2**

(22) Date of filing: **15.04.2004**

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC NL PL PT RO SE SI SK TR
Designated Extension States:
AL HR LT LV MK

(30) Priority: **01.05.2003 US 467804 P**
28.05.2003 US 474084 P
28.05.2003 US 474085 P
18.09.2003 US 504060 P
02.12.2003 US 726441

(71) Applicant: **Genesis Microchip, Inc.**
Alviso, CA 95002 (US)

(72) Inventor: **Kobayashi, Osamu**
Los Altos, CA 94024 (US)

(74) Representative: **Alton, Andrew**
Urquhart-Dykes & Lord LLP
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Leeds LS2 8PA (GB)

(54) Video interface arranged to provide pixel data independent of a link character clock

(57) A packet based display interface arranged to couple a multimedia source device to a multimedia sink device is disclosed that includes a transmitter unit coupled to the source device arranged to receive a source packet data stream in accordance with a native stream rate, a receiver unit coupled to the sink device, and a linking unit coupling the transmitter unit and the receiver unit arranged to transfer the video data in the form of a number of main link characters at a link character clock rate that is independent of the native stream rate such that video data and the link character clock are asynchronous to each other.

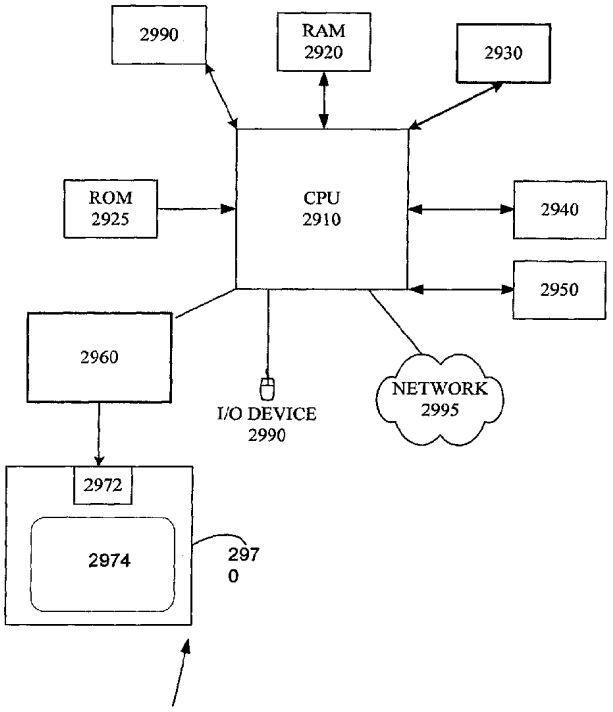


Fig. 29

EP 1 473 701 A2

LENOVO EXHIBIT 1002 - 76/502

Description

FIELD OF THE INVENTION

[0001] The invention relates to display devices. More specifically, the invention relates to digital display interface suitable for coupling video sources to video display devices.

BACKGROUND OF THE INVENTION

[0002] Currently, video display technology is divided into analog type display devices (such as cathode ray tubes) and digital type display devices (such as liquid crystal display, or LCD, plasma screens, etc.), each of which must be driven by specific input signals in order to successfully display an image. For example, a typical analog system includes an analog source (such as a personal computer, DVD player, etc.) coupled directly to a display device (sometimes referred to as a video sink) by way of a communication link. The communication link typically takes the form of a cable (such as an analog VGA cable in the case of a PC, otherwise referred to as VGA DB15 cable) well known to those of skill in the art. For example, the VGA DB15 cable includes 15 pins, each of which is arranged to carry a specific signal.

[0003] One of the advantages of the VGA DB15 cable is the ubiquitous nature of the cable, due to the large and ever-expanding installed base. As long as the analog systems described above predominate, there is little incentive to migrate away from any other cable form than the VGA DB15.

[0004] However, in recent years, the exploding growth of digital systems has made the use of digital capable cables such as Digital Visual Interface (DVI) cable more desirable. It is well known that DVI is a digital interface standard created by the Digital Display Working Group (DDWG). Data are transmitted using the transition minimized differential signaling (TMDS) protocol, providing a digital signal from the PC's graphics subsystem to the display. DVI handles bandwidths in excess of 160 MHz and thus supports UXGA and HDTV with a single set of links.

[0005] Today's display interconnect landscape includes the VGA (analog) and DVI (digital) for desktop display interconnect applications as well as LVDS (digital) for internal connectivity applications within laptops and other all-in-one devices. Graphics IC vendors, display controller IC vendors, monitor manufacturers and PC OEMs as well as desktop PC consumers, to one degree or another, must factor interface choice into their design, product definition, manufacturing, marketing and purchase decisions. For example, if a consumer purchases a PC with an analog VGA interface then the consumer must either purchase an analog monitor or a digital monitor in which the analog video signal provided by the VGA interface has been digitized by way of an inline analog to digital converter (ADC) or an ADC built into the particular monitor.

[0006] Therefore, it would be desirable to have a digital interface that is more cost effective that current interfaces (such as DVI) for coupling video sources and video displays. In some cases, the digital interface would also be backward compatible with analog video, such as VGA.

SUMMARY OF THE INVENTION

[0007] A packet based display interface arranged to couple a multimedia source device to a multimedia sink device is disclosed that includes a transmitter unit coupled to the source device arranged to receive a source packet data stream in accordance with a native stream rate, a receiver unit coupled to the sink device, and a linking unit coupling the transmitter unit and the receiver unit arranged to transfer the video data in the form of a number of main link characters at a link character clock rate that is independent of the native stream rate such that video data and the link character clock are asynchronous to each other.

[0008] In another embodiment, a packet based method of coupling a multimedia source device to a multimedia sink device is disclosed. The method includes the operations of receiving source video data in accordance with a native video data rate and transferring the video data in the form of a number of main link characters at a link character clock rate that is independent of the native stream rate such that video data and the link character clock are asynchronous to each other.

[0009] In another embodiment, computer program product for coupling a multimedia source device to a multimedia sink device is disclosed. The computer program product includes computer code for receiving source video data in accordance with a native video data rate, computer code for transferring the video data in the form of a number of main link characters at a link character clock rate that is independent of the native stream rate such that video data and the link character clock are asynchronous to each other, and computer readable medium for storing the computer code.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0010]

Fig. 1 shows a generalized representation of a cross platform display interface 100 in accordance with an embodiment of the invention.
Figs. 2A - 2C illustrates a video interface system that is used to connect a video source and a video display unit in accordance with a number of embodiments of the invention.
Fig. 3 shows exemplary main link rates in accordance with an embodiment of the invention.
Fig. 4A shows a main link data packet in accordance with an embodiment of the invention.
Fig. 4B shows a main link packet header in accordance with an embodiment of the invention.
Fig. 5A shows a system arranged to provide sub-packet enclosure and multiple-packet multiplexing in accordance with an embodiment of the invention.
Fig. 5B shows another implementation of the system shown in Fig. 5A.
Fig. 6 shows a high-level diagram of the multiplexed main link stream as an example of the stream shown in Fig. 5.
Fig. 7 show another example of a data stream in accordance with the invention.
Fig. 8 shows yet another example of a multiplexed data stream in accordance with an embodiment of the invention.
Fig. 9A shows a representative sub-packet in accordance with an embodiment of the invention.
Fig. 9B shows a representative main link data packet in accordance with an embodiment of the invention.
Fig. 10 shows an example of a selectively refreshed graphics image.
Fig. 11 shows an exemplary link training pattern in accordance with an embodiment of the invention.
Fig. 12 illustrates a logical layering of the system in accordance with an embodiment of the invention.
Fig. 13 shows an exemplary special character mapping using 8B/10B in accordance with an embodiment of the invention.
Fig. 14 shows an exemplary Manchester 11 encoding scheme in accordance with an embodiment of the invention.
Fig. 15 shows a representative auxiliary channel electrical sub layer in accordance with an embodiment of the invention.
Fig. 16 shows a representative main link electrical sub layer in accordance with an embodiment of the invention.
Fig. 17 shows a representative connector in accordance with an embodiment of the invention.
Fig. 18 shows a source state diagram in accordance with an embodiment of the invention.
Fig. 19 shows a display state diagram in accordance with an embodiment of the invention.
Figs. 20 - 24 illustrate various computer based implementations of the invention.
Fig. 25 shows a flowchart detailing a process for determining an operational mode of the interface in accordance with an embodiment of the invention.
Fig. 26 shows a flowchart detailing a process for providing a real time video image quality check in accordance with some aspects of the invention.
Fig. 27 shows a flowchart for a link set up process in accordance with an embodiment of the invention.
Fig. 28 shows a flowchart detailing a process for performing a training session in accordance with an embodiment of the invention.
Fig. 29 illustrates a computer system employed to implement the invention.

DETAILED DESCRIPTION OF SELECTED EMBODIMENTS

[0011] Reference will now be made in detail to a particular embodiment of the invention an example of which is illustrated in the accompanying drawings. While the invention will be described in conjunction with the particular embodiment, it will be understood that it is not intended to limit the invention to the described embodiment. To the contrary, it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims.

[0012] The inventive interface is a point-to-point, packet-based, plug & play, serial digital display interface that is both open and scalable that is suitable for use with, but not limited to, desktop monitors as well as providing LCD connectivity within notebook/all-in-one PC's, and consumer electronics display devices including HDTV displays and the like. Unlike conventional display interfaces that transmit a single video raster plus timing signals such as Vsync, Hsync, DE, etc., the inventive interface provides a system of multi-stream packet transfer capable of transferring one or more packet streams simultaneously in the form of "virtual pipes" established within a physical link.

[0013] For example, Fig. 1 shows a generalized representation of a cross platform packet based digital video display interface 100 in accordance with an embodiment of the invention. The interface 100 connects a transmitter 102 to a receiver 104 by way of a physical link 106 (also referred to as a pipe). In the described embodiment, a number of data streams 108 - 112 are received at the transmitter 102 that, if necessary, packetizes each into a corresponding number

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of data packets 114. These data packets are then formed into corresponding data streams each of which are passed by way of an associated virtual pipe 116 - 120 to the receiver 104. It should be noted that the link rate (i.e., the data packet transfer rate) for each virtual link can be optimized for the particular data stream resulting in the physical link 106 carrying data streams each having an associated link rate (each of which could be different from each other depending upon the particular data stream). The data streams 110 - 114 can take any number of forms such as video, graphic, audio, etc.

[0014] Typically, when the source is a video source, the data streams 110 - 114 include various video signals that can have any number and type of well-known formats, such as composite video, serial digital, parallel digital, RGB, or consumer digital video. The video signal can be an analog video signal provided the source 102 includes some form of an analog video source such as for example, an analog television, still camera, analog VCR, DVD player, camcorder, laser disk player, TV tuner, set top box (with satellite DSS or cable signal) and the like. The source 102 can also include a digital image source such as for example a digital television (DTV), digital still camera, and the like. The digital video signal can be any number and type of well known digital formats such as, SMPTE 274M-1995 (1920 x 1080 resolution, progressive or interlaced scan), SMPTE 296M-1997 (1280 x 720 resolution, progressive scan), as well as standard 480 progressive scan video.

[0015] In the case where the source 102 provides an analog image signal, an analog-to-digital converter (A/D) converts an analog voltage or current signal into a discrete series of digitally encoded numbers (signal) forming in the process an appropriate digital image data word suitable for digital processing. Any of a wide variety of A/D converters can be used. By way of example, other A/D converters include, for example those manufactured by: Philips, Texas Instrument, Analog Devices, Brooktree, and others.

[0016] For example, if the data stream 110 is an analog type signal, the an analog to digital converter (not shown) included in or coupled to the transmitter 102 will digitize the analog data which is then packetize by a packetizer that converts the digitized data stream 110 into a number of data packets 114 each of which will be transmitted to the receiver 104 by way of the virtual link 116. The receiver 104 will then reconstitute the data stream 110 by appropriately recombining the data packets 114 into their original format. It should be noted that the link rate is independent of the native stream rates. The only requirement is that the link bandwidth of the physical link 106 be higher than the aggregate bandwidth of data stream(s) to be transmitted . In the described embodiment, the incoming data (such as pixel data in the case of video data) is packed over the respective virtual link based upon a data mapping definition. In this way, the physical link 106 (or any of the constituent virtual links) does not, as does conventional interconnects such as DVI, carry one pixel data per link character clock.

[0017] In this way, the interface 100 provides a scaleable medium for the transport of not only video and graphics data, but also audio and other application data as may be required. In addition, the invention supports hot-plug event detection and automatically sets the physical link (or pipe) to its optimum transmission rate. The invention provides for a low pin count, purely digital display interconnect for all displays suitable for multiple platforms. Such platforms include host to display, laptop/all-in-one as well as HDTV and other consumer electronics applications.

[0018] In addition to providing video and graphics data, display timing information can be embedded in the digital stream providing essentially perfect and instant display alignment, obviating the need for features like "Auto-Adjust" and the like. The packet based nature of the inventive interface provides scalability to support multiple, digital data streams such as multiple video/graphics streams and audio streams for multimedia applications. In addition, a universal serial bus (USB) transport for peripheral attachment and display control can be provided without the need for additional cabling.

[0019] Other embodiments of the inventive display interface will be discussed below.

[0020] Fig. 2 illustrates a system 200 based upon the system 100 shown in Fig.1 that is used to connect a video source 202 and a video display unit 204. In the illustrated embodiment, the video source 202 can include either or both a digital image (or digital video source) 206 and an analog image (or analog video source) 208. In the case of the digital image source 206, a digital data stream 210 is provided to the transmitter 102 whereas in the case of the analog video source 208, an A/D converter unit 212 coupled thereto, converts an analog data stream 213 to a corresponding digital data stream 214. The digital data stream 214 is then processed in much the same manner as the digital data stream 210 by the transmitter 102. The display unit 204 can be an analog type display or a digital type display or in some cases can process either analog or digital signals provided thereto. In any case, the display unit 204 includes a display interface 216 that interfaces the receiver 104 with a display 218 and a D/A converter unit 220 in the case of an analog type display. In the described embodiment, the video source 202 can take any number of forms (such as a personal desktop computer, digital or analog TV, set top box, etc.) whereas the video display unit 104 can take the form of a video display (such as an LCD type display, CRT type display, etc.).

[0021] Regardless of the type of video source or video sink, however, the various data streams are digitized (if necessary) and packetized prior to transmission over the physical link 106 which includes a uni-directional main link 222 for isochronous data streams and a bi-directional auxiliary channel 224 for link setup and other data traffic (such as various link management information, Universal serial bus (USB) data, etc.) between the video source 202 and the

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video display 204.

[0022] The main link 222 is thereby capable of simultaneously transmitting multiple isochronous data streams (such as multiple video/graphics streams and multi-channel audio streams). In the described embodiment, the main link 222 includes a number of different virtual channels, each capable of transferring isochronous data streams (such as uncompressed graphics/video and audio data) at multiple gigabits per second (Gbps). From a logical viewpoint, therefore, the main link 222 appears as a single physical pipe and within this single physical pipe, multiple virtual pipes can be established. In this way, logical data streams are not assigned to physical channels rather, each logical data stream is carried in its own logical pipe (i.e., virtual channel described above).

[0023] In the described embodiment, the speed, or transfer rate, of the main link 222 is adjustable to compensate for link conditions. For example, in one implementation, the speed of the main link 222 can be adjusted in a range approximated by a slowest speed of about 1.0 Gbps to about 2.5 Gbps per channel in approximately 0.4Gbps increments (see Fig. 3). At 2.5 Gbps per channel, the main link 222 can support SXGA 60Hz with a color depth of 18 bits per pixel over a single channel. It should be noted that a reduction in the number of channels reduces not only the cost of interconnect, but also reduces the power consumption which is an important consideration (and desirable) for power sensitive applications such as portable devices and the like. However, by increasing the number of channels to four, the main link 222 can support WQSXGA (3200 x 2048 image resolution) with a color depth of 24-bits per pixel at 60Hz. or QSXGA (2560 x 2048) with a color depth of 18-bits per pixel at 60Hz, without data compression. Even at the lowest rate of 1.0 Gbps per channel, only two channels are required to support an uncompressed HDTV (i.e., 1080i or 720p) data stream.

[0024] In the described embodiment, a main link data rate is chosen whose bandwidth exceeds the aggregate bandwidth of the constituent virtual links. Data sent to the interface arrives at the transmitter at its native rate. A time-base recovery (TBR) unit 226 within the receiver 104 regenerates the stream's original native rate using time stamps embedded in the main link data packets, if necessary. It should be noted, however, that for appropriately configured digital display devices 232 shown in Fig. 2B, time base recovery is unnecessary since display data is be sent to the display driver electronics at the link character clock rate, thereby greatly reducing the number of channels required with a commensurate reduction in complexity and cost for the display. For example, Fig. 2C illustrates an exemplary LCD panel 232 configured in such a way that no time base recovery since display data is essentially pipelined to the various column drivers 234 that are used in combination with row drivers 236 to drive selected display elements 238 in the array 240.

[0025] Other embodiments describe a simple enumeration method for the link rate and the pixel/audio clock rate. It has been researched and understood that all the standard pixel/audio clock frequencies that exist today are a subset of the following master frequency:

$$23.76\text{GHz} = 210 \times 33 \times 57 \times 111\ \text{Hz}$$

This means that a pixel (or audio) clock rate can be expressed with four parameters, A, B, C, and D as:

$$\text{Pixel clock rate} = 2A * 3B \times 5C \times 11D$$

$$A = 4\ \text{bits},\ B = 2\ \text{bits},\ C = 3\ \text{bits, and}\ D = 1\ \text{bit.}$$

[0026] Even for a link whose link rate (which is the serial link bit rate / 10 for a link that uses 10-bit character such as 8B/10B characters) may be different from the pixel clock rate, there is a benefit in defining the link rate with these four parameters, A', B', C', and D': The benefit is the simplicity in regenerating pixel/audio clocks from a link clock. For example, let's say the link rate is set as A' = 6, B' = 3, C' = 7, and D' = 0 and the corresponding link rate is 135MHz. However, suppose the pixel clock rate is set as A = 8, B = 3, C = 6, and D = 0 (= 108MHz), then the pixel clock can be generated from link clock as pixel clock rate is equal to the link rate * 22 / 51 .

[0027] Referring back to those systems requiring time base recovery, the time-base recovery unit 226 may be implemented as a digital clock synthesizer. For an uncompressed video stream, the time stamp is stored in the packet header which as described in more detail below, is a 20-bit value. For a given stream, four of 20 bits are stored in each header successively (TS3-0, TS7-4, TS11-8, TS15-12, TS19-16). Native stream frequency (Freq_native) is obtained from link character clock frequency (Freq_link_char) as:

$$\text{Eq(1)} \qquad \text{Freq\_native} = \text{Freq\_link\_char} * (\text{TS19-0})/220$$

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[0028] The transmitter 102 generates this time stamp by counting the number of native stream clocks in 220 cycles of the link character clock frequency period. The counter updates the value every 220 cycles of the link character clock. Since these two clocks are asynchronous with each other, the time stamp value will change by 1 over time. Between updates, the transmitter 102 will repeatedly send the same time stamp in the header of the given packet stream. A sudden change of the time stamp value (by more than 1 count) may be interpreted by the receiver as an indication of an unstable condition of the stream source.

[0029] It should be noted that, no time stamp is communicated for an audio stream. In this case, the source device informs the display device of the audio sample rate and number of bits per sample. By determining the audio rate based upon Eq(2) and the link character rate, the display device regenerates the original audio stream rate.

Eq(2) Audio rate = (audio sample rate) x (# bits per sample) x (# channels)

[0030] A main link data packet 400 shown in Fig. 4A includes a main link packet header 402 as shown in Fig. 4B that is formed of 16 bits where bits 3-0 are the Stream ID (SID) (indicating that maximum stream count is 16), bit 4 is the Time Stamp (TS) LSB. When bit 4 is equal to 1, this packet header has the least significant 4 bits of Time Stamp value (used only for uncompressed video stream). Bit 5 is a Video frame sequence bit which acts as the least significant bit of the frame counter which toggles from "0" to "1" or from "1" to "0" at the video frame boundary (used only for uncompressed video stream). Bits 7 and 6 are reserved whereas bits 8 through 10 are a 4-bit CRC (CRC) that checks errors for the previous eight bits. Bits 15-12 are Time Stamp/Stream ID Inversion. (TSP/SIDn) which for uncompressed video are used as four bits of 20-bit Time Stamp value.

[0031] One of the advantages of the inventive interface is the ability to multiplex different data streams each of which can be different formats as well as have certain main link data packets include a number of sub packets. For example, Fig. 5 shows a system 500 arranged to provide sub-packet enclosure and multiple-packet multiplexing in accordance with an embodiment of the invention. It should be noted that the system 500 is a particular embodiment of the system 200 shown in Fig. 2 and should therefore not be construed as limiting either the scope or intent of the invention. The system 500 includes a stream source multiplexer 502 included in the transmitter 102 used to combine a stream 1 supplemental data stream 504 with the data stream 210 to form a multiplexed data stream 506. The multiplexed data stream 506 is then forwarded to a link layer multiplexer 508 that combines any of a number of data streams to form a multiplexed main link stream 510 formed of a number of data packets 512 some of which may include any of a number of sub packets 514 enclosed therein. A link layer de-multiplexer 516 splits the multiplexed data stream 510 into its constituent data streams based on the stream IDs (SIDs) and associated sub packet headers while a stream sink de-multiplexer 518 further splits off the stream 1 supplemental data stream contained in the sub-packets.

[0032] Fig. 6 shows a high-level diagram of the multiplexed main link stream 600 as an example of the stream 510 shown in Fig. 5 when three streams are multiplexed over the main link 222. The three streams in this example are: UXGA graphics (Stream ID = 1), 1280x720p video (Stream ID = 2), and audio (Stream ID = 3). The small packet header size of main link packet 400 minimizes the packet overhead, which results in the very high link efficiency. The reason the packet header can be so small is that the packet attributes are communicated via the auxiliary channel 224 prior to the transmission of the packets over main link 222.

[0033] Generally speaking, the sub-packet enclosure is an effective scheme when the main packet stream is an uncompressed video since an uncompressed video data stream has data idle periods corresponding to the video-blanking period. Therefore, main link traffic formed of an uncompressed video stream will include series of Null special character packets during this period. By capitalizing on the ability to multiplex various data streams, certain implementations of the present invention use various methods to compensate for differences between the main link rate and the pixel data rate when the source stream is a video data stream. For example, as illustrated in Fig. 7, the pixel data rate is .5 Gb/sec, such that a bit of pixel data is transmitted every 2 ns. In this example, the link rate has been set to 1.25 Gb/sec, such that a bit of pixel data is transmitted each .8 ns. Here, transmitter 102 intersperses special characters between pixel data as illustrated in Fig. 8. Two special characters are disposed between a first bit of pixel data P1 and a second bit of pixel data P2. The special characters allow receiver 104 to distinguish each bit of pixel data. Interspersing the special characters between bits of pixel data also creates a steady stream of data that allows the link to maintain synchronization. In this example, the special characters are Null characters. No line buffer is needed for such methods, only a small FIFO, because the link rate is sufficiently fast. However, relatively more logic is required on the receiving side to reconstruct the video signal. The receiver needs to recognize when the special characters begin and end.

[0034] An alternative to the interspersing method is to alternate consecutive bits of pixel data with special characters, such as null values. For example, P1 through P4 could be fed into a line buffer included in the transmitter 104, then one or more null values could be fed into the buffer until more pixel data are available. Such implementations require a relatively larger buffer space than the interspersing methods described above. In many such implementations, the time required to fill the line buffer will exceed the time required to transmit the data after the line buffer is full, due to

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the relatively high link speeds.

[0035] As discussed with reference to Fig. 5A, one of the advantages of the inventive interface is the ability to not only multiplex various data streams, but also the enclosing of any of a number of sub packets within a particular main link data packet. Fig. 9A shows a representative sub-packet 900 in accordance with an embodiment of the invention. The sub-packet 900 includes a sub-packet header 902 that in the described embodiment is 2 bytes and is accompanied by SPS (Sub-Packet Start) special character. If the main link data packet in which the sub-packet 900 is enclosed contains a packet payload in addition to the sub-packet 900, the end of the sub-packet 900 must be marked by SPE (Sub-Packet End) special character. Otherwise, the end of the main packet (as indicated by ensuing COM character in the example shown in Fig. 9B) marks the end of both the sub-packet 902 and the main packet into which it is enclosed. However, a sub-packet does not need to end with SPE when its enclosing main packet has no payload. Fig 9B shows an exemplary sub-packet format within a main link packet in accordance with an embodiment of the invention. It should be noted that the definition of the header field and sub-packet payload is dependent on the specific application profile that uses the sub-packet 902.

[0036] A particularly useful example of sub-packet enclosure usage is selective refresh of an uncompressed graphics image 1000 illustrated in Fig. 10. The attributes of the entire frame 1002 (Horizontal/Vertical Total, Image Width/Height, etc.) will be communicated via the auxiliary channel 224 since those attributes stay constant as long as the stream remains valid. In selective refresh operation, only a portion 1004 of the image 1000 is updated per video frame. The four X-Y coordinates of the updated rectangle(s) (i.e., the portion 1004) must be transmitted every frame since the values of the rectangle coordinates changes from frame to frame. Another example is the transmission of color look-up table (CLUT) data for required for 256-color graphic data where the 8-bit pixel data is an entry to the 256-entry CLUT and the content of the CLUT must be dynamically updated.

[0037] The single bi-directional auxiliary channel 224 provides a conduit to for various support functions useful for link set up and supporting main link operations as well as to carry auxiliary application data such as USB traffic. For example, with the auxiliary channel 224, a display device can inform the source device of events such as sync loss, dropped packets and the results of training sessions (described below). For example, if a particular training session fails, the transmitter 102 adjusts the main link rate based upon pre-selected or determined results of the failed training session. In this way, the closed loop created by combining an adjustable, high speed main link with a relatively slow and very reliable auxiliary channel allows for robust operation over a variety of link conditions. It should be noted that in some cases (an example of which is shown in Fig. 5B), a logical bi-directional auxiliary channel 520 can be established using a portion 522 of the bandwidth of the main link 222 to transfer data from the source device 202 to the sink device 204 and a uni-directional back channel 524 from the sink device 204 to the source device 202. In some applications, use of this logical bi-directional auxiliary channel may be more desirable than using a half-duplex bi-directional channel described in Fig. 5A.

[0038] Prior to starting the transmission of actual packet data streams the transmitter 102 establishes a stable link through a link training session that is analogous in concept to the link setup of the modem. During link training, the main link transmitter 102 sends a pre-defined training pattern so that the receiver 104 can determine whether it can achieve a solid bit/character lock. In the described embodiment, training related handshaking between the transmitter 102 and the receiver 104 is carried on the auxiliary channel. An example of a link training pattern is shown in Fig. 11 in accordance with an embodiment of the invention. As illustrated, during the training session, a phase 1 represents the shortest run length while phase 2 is the longest that are used by the receiver to optimize an equalizer. In phase 3, both bit lock and character lock are achieved as long as the link quality is reasonable. Typically, the training period is about 10 ms, in which time, approximately 107 bits of data are sent. If the receiver 104 does not achieve solid lock, it informs the transmitter 102 via the auxiliary channel 224 and the transmitter 102 reduces the link rate and repeats the training session.

[0039] In addition to providing a training session conduit, the auxiliary channel 224 can be also used to carry main link packet stream descriptions thereby greatly reducing the overhead of packet transmissions on the main link 222. Furthermore, the auxiliary channel 224 can be configured to carry Extended Display Identification Data (EDID) information replacing the Display Data Channel (DDC) found on all monitors (EDID is a VESA standard data format that contains basic information about a monitor and its capabilities, including vendor information, maximum image size, color characteristics, factory pre-set timings, frequency range limits, and character strings for the monitor name and serial number. The information is stored in the display and is used to communicate with the system through the DDC which sites between the monitor and the PC graphics adapter. The system uses this information for configuration purposes, so the monitor and system can work together). In what is referred to as an extended protocol mode, the auxiliary channel can carry both asynchronous and isochronous packets as required to support additional data types such as keyboard, mouse and microphone.

[0040] Fig. 12 illustrates a logical layering 1200 of the system 200 in accordance with an embodiment of the invention. It should be noted that while the exact implementation may vary depending upon application, generally, a source (such as the video source 202) is formed of a source physical layer 1202 that includes transmitter hardware, a source link

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layer 1204 that includes multiplexing hardware and state machine (or firmware), and a data stream source 1206 such as Audio/Visual/Graphics hardware and associated software. Similarly, a display device includes a physical layer 1208 (including various receiver hardware), a sink link layer 1210 that includes de-multiplexing hardware and state machine (or firmware) and a stream sink 1212 that includes display/timing controller hardware and optional firmware. A source application profile layer 1214 defines the format with which the source communicates with the link layer 1204 and similarly, a sink application profile layer 1216 defines the format with which the sink 1212 communicates with the sink link layer 1210.

[0041] The various layers will now be discussed in more detail.

SOURCE DEVICE PHYSICAL LAYER

[0042] In the described embodiment, the source device physical layer 1202 includes an electrical sub layer 1202-1 and a logical sub layer 1202-2. The electrical sub layer 1202-1 includes all circuitry for interface initialization/operation such as hot plug/unplug detection circuit, drivers/receivers/termination resistors, parallel-to-serial/serial-to-parallel conversions, and spread-spectrum-capable PLL's. The logical sub layer 1202-2 includes circuitry for, packetizing/de-packetizing, data scrambling/de-scrambling, pattern generation for link training, time-base recovery circuits, and data encoding/decoding such as 8B/10B (as specified in ANSI X3.230-1994, clause 11) that provides 256 link data characters and twelve control characters (an example of which is shown as Fig. 13) for the main link 222 and Manchester II for the auxiliary channel 224 (see Fig. 14).

[0043] It should be noted that the 8B/10B encoding algorithm is described, for example, in U.S. Patent Number 4,486,739, which is hereby incorporated by reference. As known by those of skill in the art, the 8B/10B code is a block code that encodes 8-bit data blocks into 10-bit code words for serial transmission. In addition, the 8B/10B transmission code converts a byte wide data stream of random 1s and 0s into a DC balanced stream of 1s and 0s with a maximum run length of 5. Such codes provide sufficient signal transitions to enable reliable clock recovery by a receiver, such as transceiver 110. Moreover, a DC balanced data stream proves to be advantageous for fiber optic and electromagnetic wire connections. The average number of 1s and 0s in the serial stream is be maintained at equal or nearly equal levels. The 8B/10B transmission code constrains the disparity between the number of 1s and 0s to be -2, 0, or 2 across 6 and 4 bit block boundaries. The coding scheme also implements additional codes for signaling, called command codes.

[0044] It should be noted that in order to avoid the repetitive bit patterns exhibited by uncompressed display data (and hence, to reduce EMI), data transmitted over main link 222 is first scrambled before 8B/10B encoding. All data except training packets and special characters will be scrambled. The scrambling function is implemented with Linear Feedback Shift Registers (LFSRs). When data encryption is enabled, the initial value of an LFSR seed is dependent on an encryption key set. If it is data scrambling without encryption, the initial value will be fixed.

[0045] Since data stream attributes are transmitted over the auxiliary channel 224, the main link packet headers serve as stream identification numbers thereby greatly reducing overhead and maximizing link bandwidth. It should also be noted that neither the main link 222 nor the auxiliary link 224 has separate clock signal lines. In this way, the receivers on main link 222 and auxiliary link 224 sample the data and extract the clock from the incoming data stream. Fast phase locking for any phase lock loop (PLLs) circuit in the receiver electrical sub layer is important for since the auxiliary channel 224 is half-duplex bi-directional and the direction of the traffic changes frequently. Accordingly, the PLL on the auxiliary channel receiver phase locks in as few as 16 data periods thanks to the frequent and uniform signal transitions of Manchester II (MII) code

[0046] At link set up time, the data rate of main link 222 is negotiated using the handshake over auxiliary channel 224. During this process, known sets of training packets are sent over the main link 222 at the highest link speed. Success or failure is communicated back to the transmitter 102 via the auxiliary channel 224. If the training fails, main link speed is reduced and training is repeated until successful. In this way, the source physical layer 1102 is made more resistant to cable problems and therefore more suitable for external host to monitor applications. However, unlike conventional display interfaces, the main channel link data rate is decoupled from the pixel clock rate. A link data rate is set so that link bandwidth exceeds the aggregate bandwidth of the transmitted streams.

SOURCE DEVICE LINK LAYER

[0047] The source link layer 1204 handles the link initialization and management. For example, upon receiving a hot plug detect event generated upon monitor power-up or connection of the monitor cable from the source physical layer 1202, the source device link layer 1204 evaluates the capabilities of the receiver via interchange over the auxiliary channel 224 to determine a maximum main link data rate as determined by a training session, the number of time-base recovery units on the receiver, available buffer size on both ends, availability of USB extensions and then notifies the stream source 1206 of an associated hot plug event. In addition, upon request from the stream source 1206, the

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source link layer 1204 reads the display capability (EDID or equivalent). During a normal operation, the source link layer 1204 sends the stream attributes to the receiver 104 via the auxiliary channel 224, notifies the stream source 1204 whether the main link 222 has enough resource for handling the requested data streams, notifies the stream source 1204 of link failure events such as sync loss and buffer overflow, and sends MCCS commands submitted by the stream source 1204 to the receiver via the auxiliary channel 224. All communications between the source link layer 1204 and the stream source/sink use the formats defined in the application profile layer 1214.

APPLICATION PROFILE LAYER (SOURCE AND SINK)

[0048] In general, the Application Profile Layer defines formats with which a stream source (or sink) will interface with the associated link layer. The formats defined by the application profile layer are divided into the following categories, Application independent formats (Link Message for Link Status inquiry) and Application dependent formats (main link data mapping, time-base recovery equation for the receiver, and sink capability/stream attribute messages sub-packet formats, if applicable). The Application Profile Layer supports the following color formats 24-bit RGB, 16-bit RG2565, 18-bit RGB, 30-bit RGB, 256-color RGB (CLUT based), 16-bit, CbCr422, 20-bit YCbCr422, and 24-bit YCbCr444.

[0049] For example, the display device application profile layer (APL) 1214 is essentially an application-programming interface (API) describing the format for Stream Source/Sink communication over the main link 222 that includes a presentation format for data sent to or received from the interface 100. Since some aspects of the APL 1214 (such as the power management command format) are baseline monitor functions, they are common to all uses of the interface 100. Whereas other non-baseline monitor functions, such as such as data mapping format and stream attribute format, are unique to an application or a type of isochronous stream that is to be transmitted. Regardless of the application, the stream source 1204 queries the source link layer 1214 to ascertain whether the main link 222 is capable of handling the pending data stream(s) prior to the start any packet stream transmission on the main link 222.

[0050] When it is determined that the main link 222 is capable of supporting the pending packet stream(s), the stream source 1206 sends stream attributes to the source link layer 1214 that is then transmitted to the receiver over the auxiliary channel 224. These attributes are the information used by the receiver to identify the packets of a particular stream, to recover the original data from the stream and to format it back to the stream's native data rate. The attributes of the data stream are application dependent.

[0051] In those cases where the desired bandwidth is not available on the main link 222, the stream source 1214 may take corrective action by, for example, reducing the image refresh rate or color depth.

DISPLAY DEVICE PHYSICAL LAYER

[0052] The display device physical layer 1216 isolates the display device link layer 1210 and the display device APL 1216 from the signaling technology used for link data transmission/reception. The main link 222 and the auxiliary channel 224 have their own physical layers, each consisting of a logical sub layer and an electrical sub layer that includes the connector specification. For example, the half-duplex, bi-directional auxiliary channel 224 has both a transmitter and a receiver at each end of the link as shown in Fig 15. An auxiliary link transmitter 1502 is provided with link characters by a logical sub layer 1208-1 that are then serialized serialized and transmitted to a corresponding auxiliary link receiver 1504. The receiver 1504, in turn, receives serialized link character from the auxiliary link 224 and de-serializes the data at a link character clock rate. It should be noted that the major functions of the source logical sub layers include signal encoding, packetizing, data scrambling (for EMI reduction), and training pattern generation for the transmitter port. While for the receiver port, the major functions of the receiver logical sub layer includes signal decoding, de-packetizing, data de-scrambling, and time-base recovery.

AUXILIARY CHANNEL

[0053] The major functions of auxiliary channel logical sub layer include data encoding and decoding, framing/de-framing of data and there are two options in auxiliary channel protocol: standalone protocol (limited to link setup/management functions in a point-to-point topology) is a lightweight protocol that can be managed by the Link Layer state-machine or firmware and extended protocol that supports other data types such as USB traffic and topologies such as daisy-chained sink devices. It should be noted that the data encoding and decoding scheme is identical regardless of the protocol whereas framing of data differs between the two.

[0054] Still referring to Fig. 15, the auxiliary channel electrical sub layer contains the transmitter 1502 and the receiver 1504. The transmitter 1502 is provided with link characters by the logical sub layer, which it serializes and transmits out. The receiver 1504 receives serialized link character from the link layer and subsequently de-serializes it at link character clock rate. The positive and negative signals of auxiliary channel 224 are terminated to ground via 50-ohm

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termination resistors at each end of the link as shown. In the described implementation, the drive current is programmable depending on the link condition and ranges from approximately 8mA to approximately 24mA resulting in a range of vdifferential_pp of approximately 400mV to approximately 1.2V. In electrical idle modes, neither the positive nor the negative signal is driven. When starting transmission from the electrical idle state, the SYNC pattern must be transmitted and the link reestablished. In the described embodiment, the SYNC pattern consists of toggling a auxiliary channel differential pair signals at clock rate 28 times followed by four 1 's in Manchester II code. The auxiliary channel master in the source device detects hot-plug and hot-unplug events by periodically driving or measuring the positive and negative signals of auxiliary channel 224.

MAIN LINK

[0055] In the described embodiment, the main link 222 supports discrete, variable link rates that are integer multiples of the local crystal frequency (see Fig 3 for a representative set of link rates consonant with a local crystal frequency of 24-MHz). As shown in Fig. 16, the main link 222 (being an unidirectional channel) has only a transmitter 1602 at the source device and only a receiver 1604 at the display device.

[0056] As shown, the cable 1604 takes the form includes a set of twisted pair wires, one for each of the Red (R), Green(G), and Blue(B) video signals provides in a typical RGB color based video system (such as PAL based TV systems). As known by those of skill in the art, twisted pair cable is a type of cable that consists of two independently insulated wires twisted around one another. One wire carries the signal while the other wire is grounded and absorbs signal interference. It should be noted that in some other systems, the signals could also be component based signals (Pb, Pr, Y) used for NTSC video TV systems. Within the cable, each twisted pair is individually shielded. Two pins for +12V power and ground are provided. The characteristics impedance of each differential pair is 100 ohms +/- 20%. The entire cable is also shielded. This outer shield and individual shields are shorted to the connector shells on both ends. The connector shells are shorted to ground in a source device. A connector 1700 as shown in Fig. 17 has 13 pins in one row having a pinout that is identical both for the connector on the source device end and that on the display device end. The source device supplies the power.

[0057] The main link 222 is terminated on both ends and since the main link 222 is AC coupled, the termination voltage can be anywhere between 0V (ground) to +3.6V. In the described implementation, the drive current is programmable depending on the link condition and ranges from approximately 8mA to approximately 24mA resulting in a range of Vdifferential_pp of approximately 400mV to approximately 1.2V. The minimum voltage swing is selected for each connection using a training pattern. An electrical idle state is provided for power management modes. In electrical idle, neither the positive nor the negative signals are driven. When starting a transmission from electrical idle state, the transmitter must conduct a training session in order reestablish the link with the receiver.

STATE DIAGRAMS

[0058] The invention will now be described in terms of state diagrams shown in Figs. 18 and 19 described below. Accordingly, Fig. 18 shows the source state diagram described below. At an off state 1802, the system is off such that the source is disabled. If the source is enabled, then the system transitions to a standby state 1804 suitable for power saving and receiver detection. In order to detect whether or not the receiver is present (i.e., hot plug/play), the auxiliary channel is periodically pulsed (such as for 1us every 10ms) and a measure of a voltage drop across the termination resistors during the driving is measured. If it is determined that a receiver is present based upon the measured voltage drop, then the system transitions to a detected receiver state 1806 indicating that a receiver has been detected, i.e, a hot plug event has been detected. If, however, there is no receiver detected, then the receiver detection is continued until such time, if ever, a receiver is detected or a timeout has elapsed. It should be noted that in some cases the source device may choose to go to "OFF" state from which no further display detection is attempted.

[0059] If at the state 1806 a display hot unplug event is detected, then the system transitions back to the standby state 1804. Otherwise the source drives the auxiliary channel with a positive and negative signal to wake up receiver and the receiver's subsequent response, if any, is checked. If there is no response received, then the receiver has not woken up and source remains in the state 1806. If, however, a signal is received from the display, then the display has woken up and the source is ready read the receiver link capabilities (such as max link rate, buffer size, and number of time-base recovery units) and the system transitions to a main link initialization state 1808 and is ready to commence a training start notification phase.

[0060] At this point, a training session is started by sending a training pattern over the main link at a set link rate and checks an associated training status. The receiver sets a pass/fail bit for each of three phases and the transmitter will proceed to the next phase upon detection of pass only such that when a pass is detected, the main link is ready at that link rate. At this point, the interface transitions to a normal operation state 1510, otherwise, the link rate is reduced and the training session is repeated. During the normal operation state 1810, the source continues to periodically

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monitor a link status index, which if fails, a hot unplug event is detected and the system transitions to the standby state 1804 and waits for a hot plug detection event. If, however, a sync loss is detected, then the system transitions to state 1808 for a main link re-initiation event.

[0061] Fig 19 shows the display state diagram 1900 described below. At a state 1902, no voltage is detected, the display goes to an OFF state. At a standby mode state 1904, both main link receiver and auxiliary channel slave are in electrical idle, a voltage drop across the termination resistors of auxiliary channel slave port are monitored for a predetermined voltage. If the voltage is detected, then the auxiliary channel slave port is turned on indicating a hot plug event and the system moves to a display state 1906, otherwise, the display remains in the standby state 1904. At the state 1906 (main link initialization phase), if a display is detected, then the auxiliary slave port is fully turned on, and the transmitter responds to a receiver link capability read command and the display state transitions to 1908, otherwise, if there is no activity on the auxiliary channel for more than a predetermined period of time then the auxiliary channel slave port is put into the to standby state 1904.

[0062] During a training start notification phase, the display responds to the training initiation by the transmitter by adjusting the equalizer using training patterns, updating the result for each phase. If the training fails, then wait for another training session and if the training passes, then go to normal operation state 1910. If there is no activity on the auxiliary channel or on the main link (for training) for more than a predetermined (10ms, for example), the auxiliary channel slave port is set to the standby state 1904.

[0063] Figs. 20 - 24 show particular implementations of the cross platform display interface.

[0064] Fig. 20 shows a PC motherboard 2000 having an on-board graphics engine 2002 that incorporates a transmitter 2004 in accordance with the invention. It should be noted that the transmitter 2004 is a particular example of the transmitter 102 shown in Fig. 1. In the described embodiment, the transmitter 2004 is coupled to an connector 2006 (along the lines of the connector 1700) mounted on the motherboard 2000 which in turn is connected to a display device 2008 by way of a twisted pair cable 2010 couples a display device 2010.

[0065] As known in the art, PCI Express (developed by Intel Corporation of Santa Clara, CA) is a high-bandwidth, low pin count, serial, interconnect technology that also maintains software compatibility with existing PCI infrastructure. In this configuration, the PCI Express port is augmented to become compliant with the requirements of the cross platform interface which can directly drive a display device either using a motherboard mounted connector as shown.

[0066] In situations where it is not practical to mount the connector on the motherboard, the signals can be routed through the SDVO slot of the PCI Express motherboard and brought to the back of the PC using a passive card connector as shown in Fig. 21. As is the case with the current generation of add-in graphics cards, a add-in graphics card can supplant the onboard graphics engine as shown in Fig. 23.

[0067] In the case of notebook applications, the transmitter on the motherboard graphics engine would drive through internal cabling, an integrated receiver/TCON which would drive the panel directly. For the most cost effective implementation, the receiver/TCON would be mounted on the panel thereby reducing the number of interconnect wires to 8 or 10 as shown in Fig. 24

[0068] All of the above examples assume integrated transmitters. However, is it quite feasible to implement as a standalone transmitter integrating into PCI and PCI Express environments through the AGP or SDVO slots, respectively. A standalone transmitter will enable output streams without any change in graphics hardware or software.

FLOWCHART EMBODIMENTS

[0069] The methodology of the invention will now be described in terms of a number of flowcharts each describing a particular process for enabling the invention. Specifically, FIGS 25 - 29 describe a number of interrelated processes that when used singly or in any combination described aspects of the invention.

[0070] Fig. 25 shows a flowchart detailing a process 2500 for determining an operational mode of the interface 100 in accordance with an embodiment of the invention. In this process, the operational mode will only be set to a digital mode if the video source and the display device are both digital. Otherwise, the operational mode will be set to analog mode. It should be noted that "analog mode" in this context can include both conventional VGA mode as well as enhanced analog mode having differential analog video with embedded alignment signal and bi-directional sideband. This enhanced analog mode will be described below.

[0071] In step 2502, a video source is interrogated to determine whether the video source supports analog or digital data. If the video source supports only analog data, the operational mode of coupling device 100 will be set to analog (step 2508), then the process will end (step 2512).

[0072] If the video source can output digital data, the process continues to step 2506. The display device is then interrogated to determine whether the display device is configured to receive digital data. If the display device supports only analog data, the operational mode of coupling device will be set to analog (step 2508), then the process will end (step 2512). Otherwise, the operational mode of the coupling device is set to digital (step 2510). For example, a processor may control switches within the coupling device to set the mode to digital. In general, the coupling device is

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configured to operate in a fully digital mode only when both the video source and the video sink are operating in a corresponding digital mode.

[0073] Fig. 26 shows a flowchart detailing a process 2600 for providing a real time video image quality check in accordance with some aspects of the invention. In this example, all determinations of process 2600 are made by a processor coupled to the display interface.

[0074] In step 2600, a video signal is received from a video source. Next, a signal quality test pattern is provided by the video source associated with the received video signal (step 2602). In step 2604, a determination of a bit error rate is made, based upon the quality test pattern. Then, a determination is made of whether the bit error rate is greater than a threshold value (step 2606). If the bit error rate is determined to not be greater than the threshold value, then a determination is made (step 2614) of whether or not there are more video frames. If it is determined that there are more video frames, then the process returns to step 2600. Otherwise, the process ends.

[0075] However, if the bit error rate is determined to be greater than the threshold value in step 2606, a determination is made (step 2608) as to whether the bit rate is greater than a minimum bit rate. If the bit rate is greater than a minimum bit rate, then the bit rate is lowered (step 2610) and the process returns to step 2606. If the bit rate is not greater than the minimum bit rate, then the mode is changed to analog mode (step 2612) and the process ends.

[0076] Fig. 27 shows a flowchart for a link set up process 2700 in accordance with an embodiment of the invention. The process 2700 begins at 2702 by the receiving of a hot plug detection event notification. At 2704 a main link inquiry is made by way of an associated auxiliary channel to determine a maximum data rate, a number of time base recovery units included in a receiver, and available buffer size. Next, at 2706, the maximum link data rate is verified by way of a training session and at 2708, a data stream source is notified of the hot plug event. At 2710, the capabilities of the display (using EDID, for example) are determined by way of the auxiliary channel and the display responds to the inquires at 2712 which, in turn, results a collaboration of the main link training session at 2714.

[0077] Next, at 2716, the stream source sends stream attributes to the receiver by way of the auxiliary channel and at 2718, the stream sources are further notified whether the main link is capable of supporting the requested number of data streams at 2720. At 2722, the various data packets are formed by adding associated packet headers and the multiplexing of a number of source streams is scheduled at 2724. At 2726 a determination is made whether or not the link status is OK. When the link status is not OK, then the source(s) are notified of a link failure event at 2728, otherwise, the link data streams are reconstructed into the native streams based upon the various packet headers at 2730. At 2732, the reconstructed native data streams are then passed to the display device.

[0078] Fig. 28 shows a flowchart detailing a process 2800 for performing a training session in accordance with an embodiment of the invention. It should be noted that the training session process 2800 is one implementation of the operation 2506 described in Fig. 25. A training session is started at 2802 by sending a training pattern over the main link at a set link rate to the receiver. A typical link training pattern is shown in Fig. 11 in accordance with an embodiment of the invention. As illustrated, during the training session, a phase 1 represents the shortest run length while phase 2 is the longest. The receiver is to use these two phases to optimize the equalizer. In phase 3, both bit lock and character lock are achieved as long as the link quality is reasonable. At 2804, the receiver checks an associated training status and based upon the training status check, the receiver sets a pass/fail bit for each of three phases and the transmitter at 2806. At each phase, the receiver will proceed to the next phase upon detection of pass only and at 2810 and if the receiver does not detect a pass then the receiver reduces the link rate and repeats the training session. The main link is ready at that link rate at which a pass is detected at 2812.

[0079] Fig. 29 illustrates a computer system 2900 employed to implement the invention. Computer system 2900 is only an example of a graphics system in which the present invention can be implemented. Computer system 2900 includes central processing unit (CPU) 1510, random access memory (RAM) 2920, read only memory (ROM) 2925, one or more peripherals 2930, graphics controller 2960, primary storage devices 2940 and 2950, and digital display unit 2970. As is well known in the art, ROM acts to transfer data and instructions uni-directionally to the CPUs 2910, while RAM is used typically to transfer data and instructions in a bi-directional manner. CPUs 2910 may generally include any number of processors. Both primary storage devices 2940 and 2950 may include any suitable computer-readable media. A secondary storage medium 880, which is typically a mass memory device, is also coupled bi-directionally to CPUs 2910 and provides additional data storage capacity. The mass memory device 880 is a computer-readable medium that may be used to store programs including computer code, data, and the like. Typically, mass memory device 880 is a storage medium such as a hard disk or a tape which generally slower than primary storage devices 2940, 2950. Mass memory storage device 880 may take the form of a magnetic or paper tape reader or some other well-known device. It will be appreciated that the information retained within the mass memory device 880, may, in appropriate cases, be incorporated in standard fashion as part of RAM 2920 as virtual memory.

[0080] CPUs 2910 are also coupled to one or more input/output devices 890 that may include, but are not limited to, devices such as video monitors, track balls, mice, keyboards, microphones, touch-sensitive displays, transducer card readers, magnetic or paper tape readers, tablets, styluses, voice or handwriting recognizers, or other well-known input devices such as, of course, other computers. Finally, CPUs 2910 optionally may be coupled to a computer or

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telecommunications network, e.g., an Internet network or an intranet network, using a network connection as shown generally at 2995. With such a network connection, it is contemplated that the CPUs 2910 might receive information from the network, or might output information to the network in the course of performing the above-described method steps. Such information, which is often represented as a sequence of instructions to be executed using CPUs 2910, may be received from and outputted to the network, for example, in the form of a computer data signal embodied in a carrier wave. The above-described devices and materials will be familiar to those of skill in the computer hardware and software arts.

[0081] Graphics controller 2960 generates analog image data and a corresponding reference signal, and provides both to digital display unit 2970. The analog image data can be generated, for example, based on pixel data received from CPU 2910 or from an external encode (not shown). In one embodiment, the analog image data is provided in RGB format and the reference signal includes the VSYNC and HSYNC signals well known in the art. However, it should be understood that the present invention can be implemented with analog image, data and/or reference signals in other formats. For example, analog image data can include video signal data also with a corresponding time reference signal.

[0082] Although only a few embodiments of the present invention have been described, it should be understood that the present invention may be embodied in many other specific forms without departing from the spirit or the scope of the present invention. The present examples are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope of the appended claims along with their full scope of equivalents.

[0083] While this invention has been described in terms of a preferred embodiment, there are alterations, permutations, and equivalents that fall within the scope of this invention. It should also be noted that there are many alternative ways of implementing both the process and apparatus of the present invention. It is therefore intended that the invention be interpreted as including all such alterations, permutations, and equivalents as fall within the true spirit and scope of the present invention.

Claims

1. A packet based display interface arranged to couple a multimedia source device to a multimedia sink device, comprising:

   a transmitter unit coupled to the source device arranged to receive a source video data stream in accordance with a native video data rate;
   a receiver unit coupled to the sink device; and
   a linking unit coupling the transmitter unit and the receiver unit arranged to transfer the video data in the form of a number of main link characters at a link character clock rate that is independent of the native stream rate such that video data and the link character clock are asynchronous to each other.

2. A packet based display interface as recited in claim 1, wherein the multimedia data packet stream is one of a number of multimedia data packet streams each having an associated adjustable data stream link rate that is independent of the native stream rate.

3. A display interface as recited in claim 1, wherein the link unit further comprises:

   a unidirectional main link arranged to carry the multimedia data packets from the transmitter unit to the receiver unit; and
   a bi-directional auxiliary channel arranged to transfer information between the transmitter unit and the receiver unit and vice versa.

4. A display interface as recited in claim 3, wherein the bi-directional auxiliary channel is formed of a uni-directional back channel configured to carry information from the sink device to the source device and a uni-directional forward channel included as part of the main channel for carrying information from the source device to the sink device in concert with the back channel.

5. A display interface as recited in claim 2, wherein the main link unit further comprises:

   a number of virtual links each being associated with a particular one of the multi media data packet streams wherein each of said virtual links has an associated virtual link bandwidth and a virtual link rate.

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6. A display interface as recited in claim 5, wherein a main link bandwidth is at least equal to an aggregate of the virtual link bandwidths.

7. A display interface as recited in 1, wherein the source data stream is packetized over the respective virtual link based upon a mapping definition.

8. A method of coupling a multimedia source device to a multimedia sink device, comprising:

receiving source video data in accordance with a native video data rate;
transferring the video data in the form of a number of main link characters at a link character clock rate that is independent of the native stream rate such that video data and the link character clock are asynchronous to each other.

9. A method as recited in claim 8, wherein the multimedia data packet stream is one of a number of multimedia data packet streams each having an associated adjustable data stream link rate that is independent of the native stream rate.

10. A method as recited in claim 8, wherein the link unit further comprises:

a unidirectional main link arranged to carry the multimedia data packets from the transmitter unit to the receiver unit; and
a bi-directional auxiliary channel arranged to transfer information between the transmitter unit and the receiver unit and vice versa.

11. A method as recited in claim 10, wherein the bi-directional auxiliary channel is formed of a uni-directional back channel configured to carry information from the sink device to the source device and a uni-directional forward channel included as part of the main channel for carrying information from the source device to the sink device in concert with the back channel.

12. A method as recited in claim 8, wherein the main link unit further comprises:

a number of virtual links each being associated with a particular one of the multi media data packet streams wherein each of said virtual links has an associated virtual link bandwidth and a virtual link rate.

13. A method as recited in claim 12, wherein a main link bandwidth is at least equal to an aggregate of the virtual link bandwidths.

14. A method as recited in claim 8, wherein the source data stream is packetized over the respective virtual link based upon a mapping definition.

15. Computer program product for coupling a multimedia source device to a multimedia sink device, comprising:

computer code for receiving source video data in accordance with a native video data rate;
computer code for transferring the video data in the form of a number of main link characters at a link character clock rate that is independent of the native stream rate such that video data and the link character clock are asynchronous to each other; and
computer readable medium for storing the computer code.

16. Computer program product as recited in claim 15, wherein the multimedia data packet stream is one of a number of multimedia data packet streams each having an associated adjustable data stream link rate that is independent of the native stream rate.

17. Computer program product as recited in claim 15, wherein the link unit further comprises:

a unidirectional main link arranged to carry the multimedia data packets from the transmitter unit to the receiver unit; and
a bi-directional auxiliary channel arranged to transfer information between the transmitter unit and the receiver unit and vice versa.

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18. Computer program product as recited in claim 17, wherein the bi-directional auxiliary channel is formed of a uni-directional back channel configured to carry information from the sink device to the source device and a uni-directional forward channel included as part of the main channel for carrying information from the source device to the sink device in concert with the back channel.

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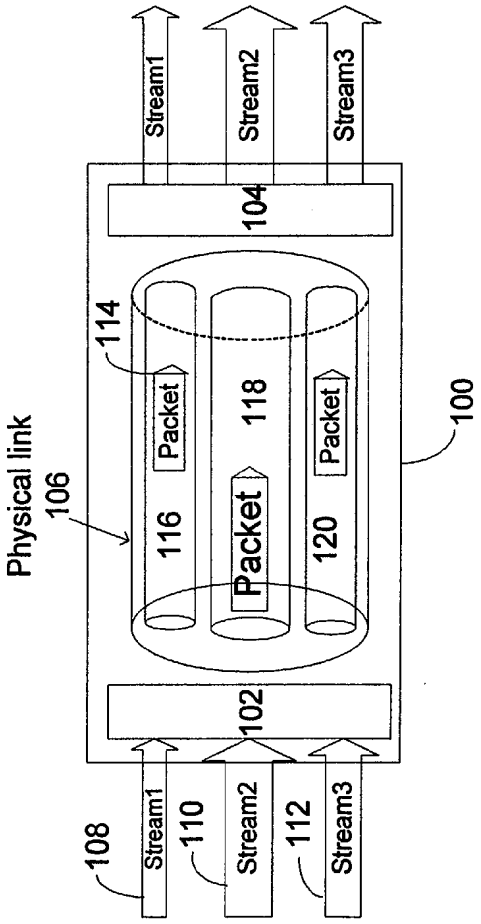
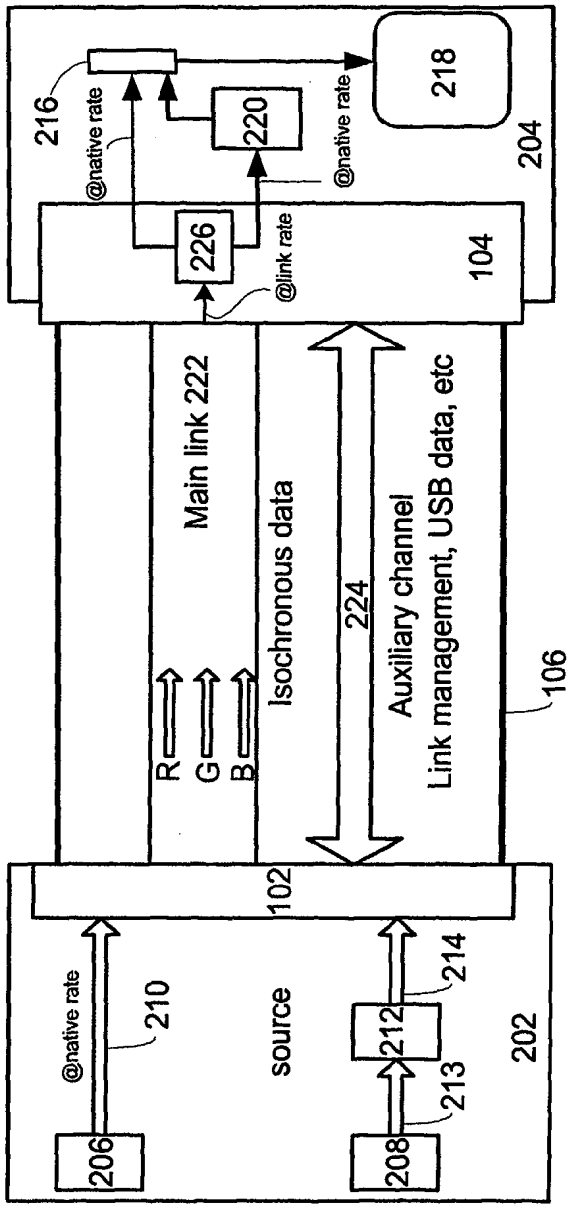


Fig. 1

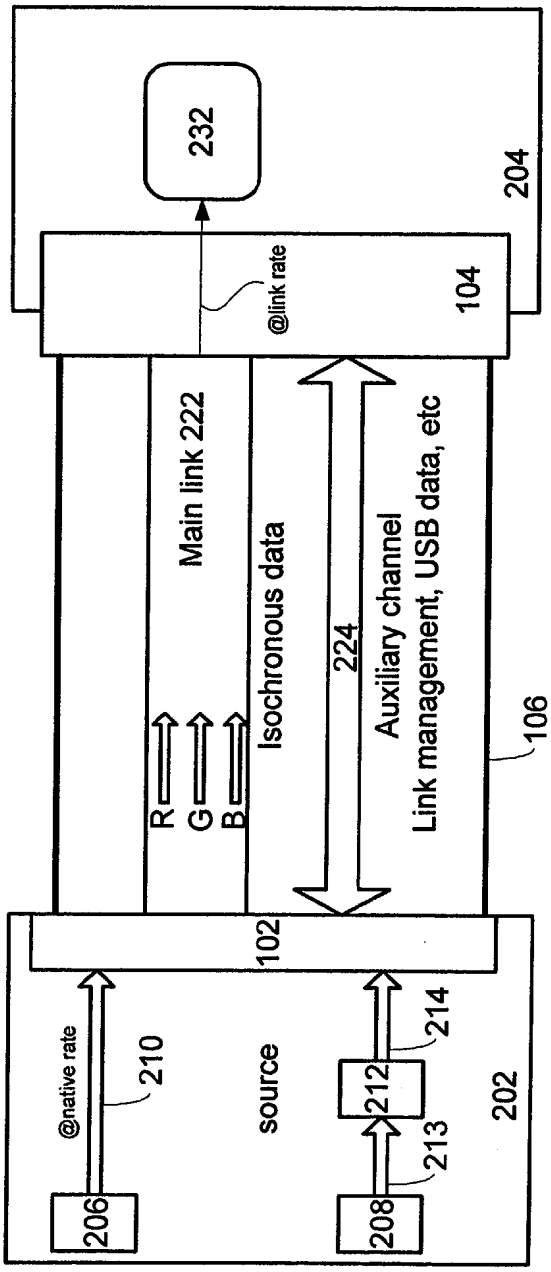
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200

Fig. 2A

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230

Fig. 2B

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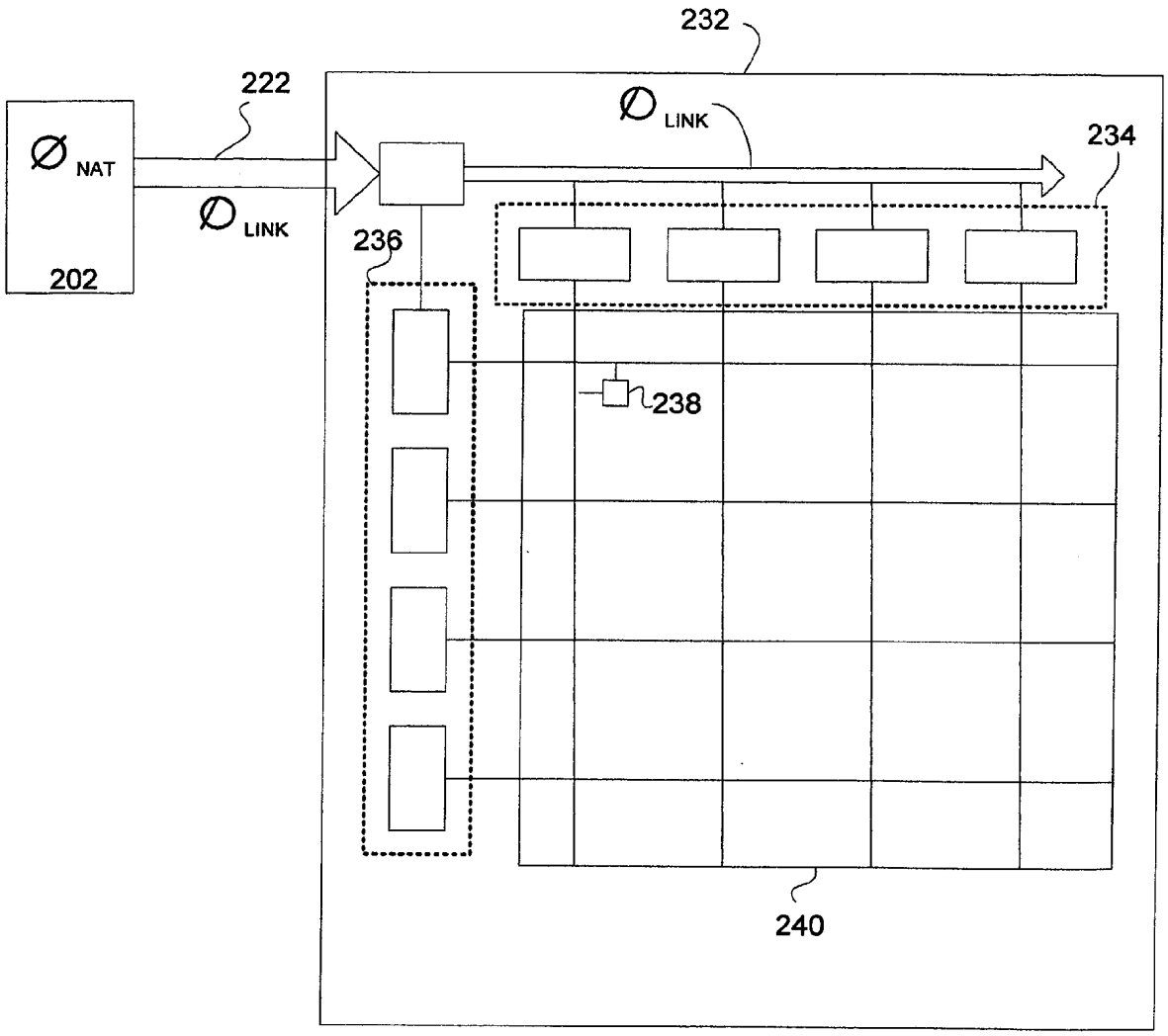


Fig. 2C

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Main Link Data Rates

Nominal Baud Rate per channel (Gbits/second)	Actual Baud Rate per channel (Gbits/second)	Clock Multiplication Factor from 24-MHz crystal
1.0	0.960	x40
1.35	1.344	x56
1.7	1.728	x72
2.1	2.112	x88
2.5	2.496	x104

Fig. 3

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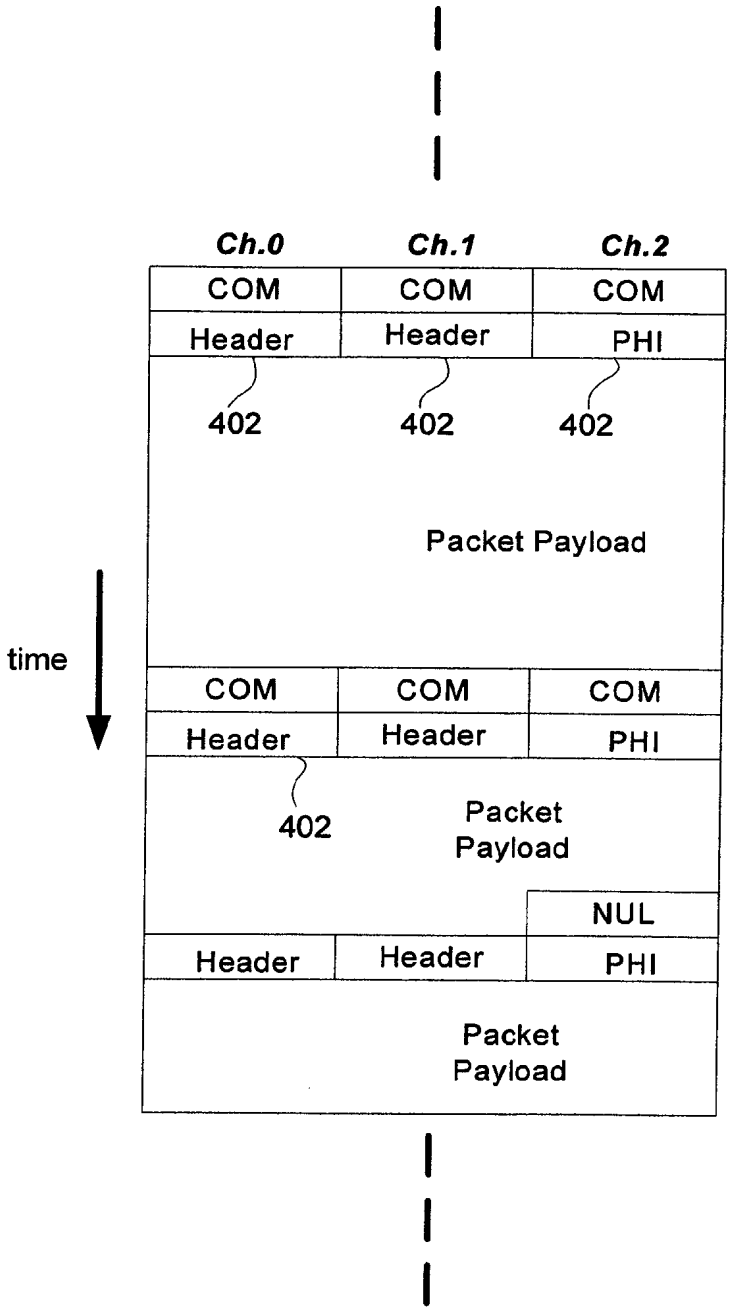


Fig. 4A

Main Link Packet Format

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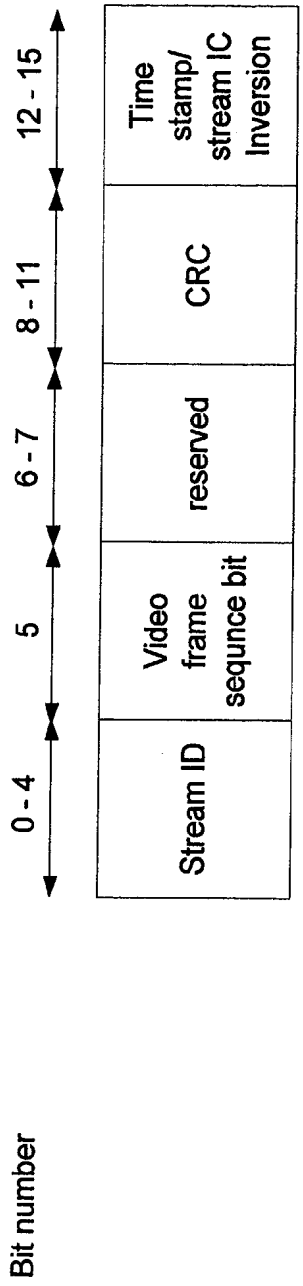
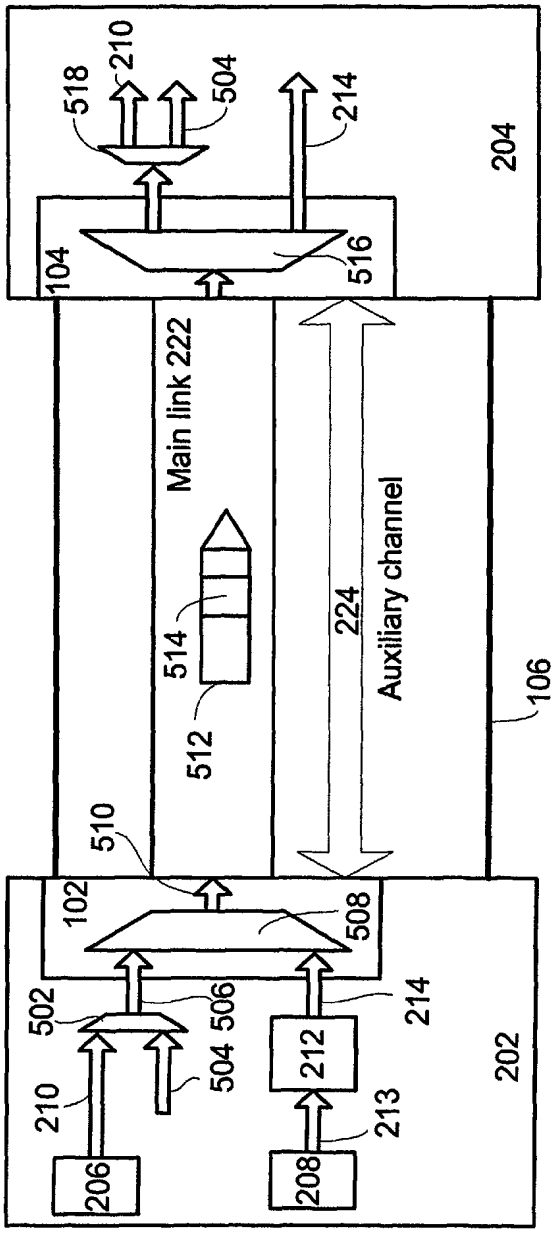


Fig. 4B

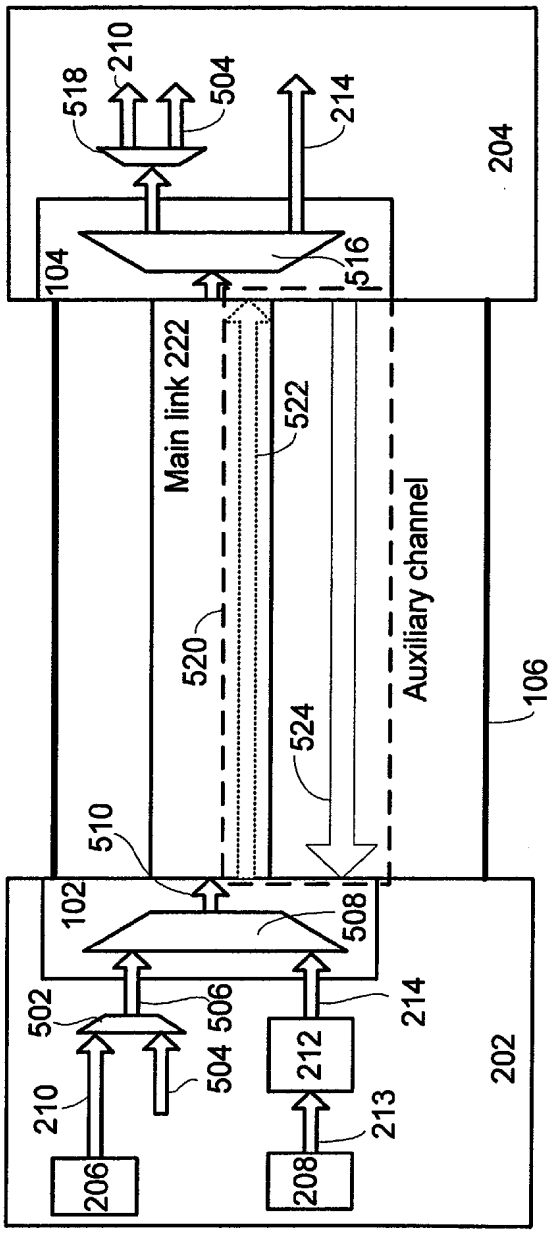
LENOVO EXHIBIT 1002 - 97/502



500

Fig. 5A

LENOVO EXHIBIT 1002 - 98/502



500

Fig. 5B

LENOVO EXHIBIT 1002 - 99/502

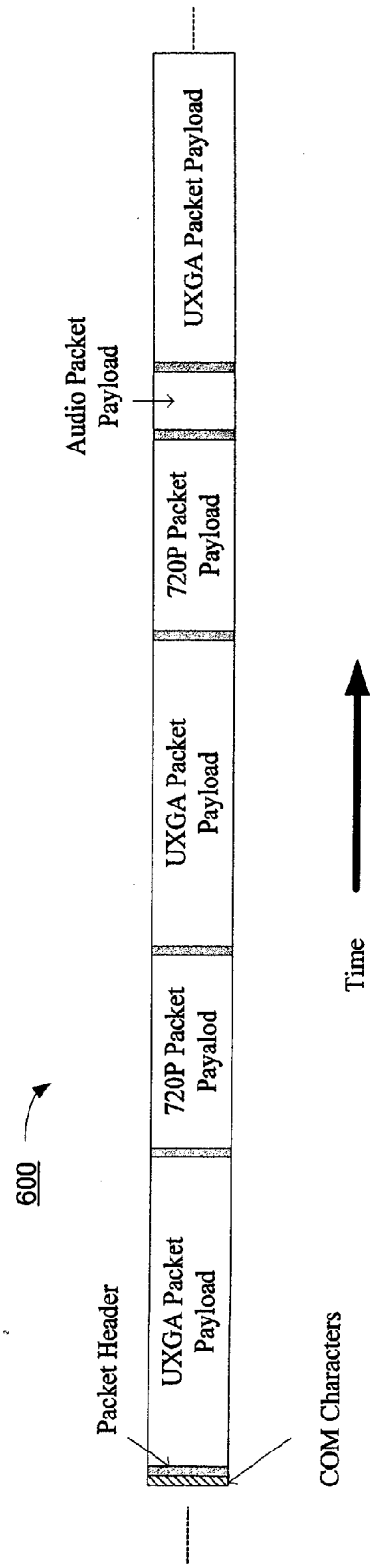


Fig. 6

High-level diagram of link traffic example with three streams

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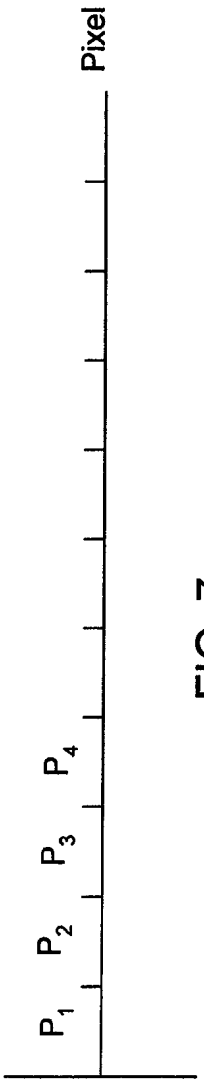


FIG. 7

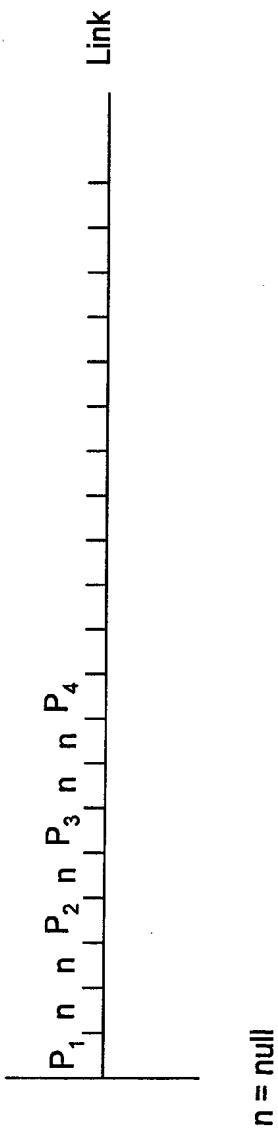


FIG. 8

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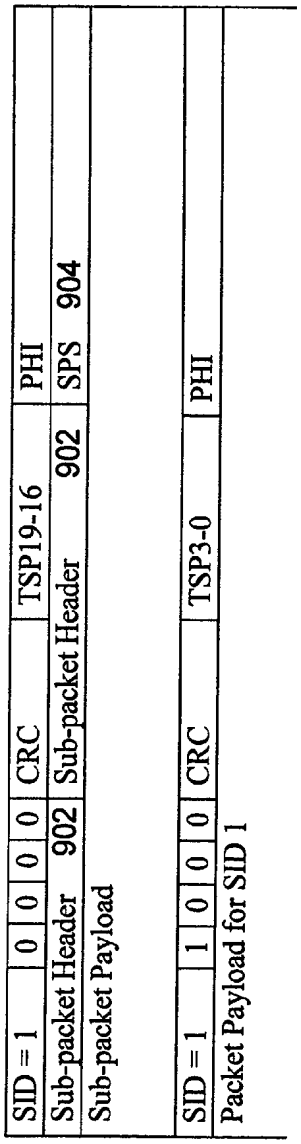


Fig. 9A

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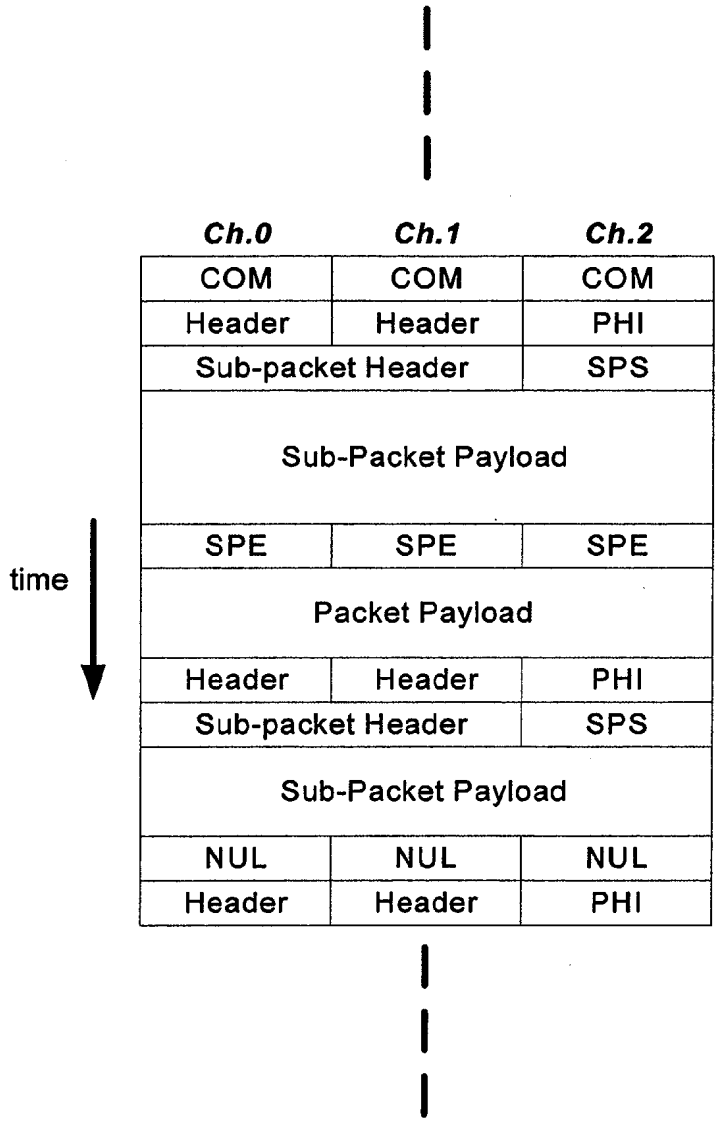


Fig. 9B

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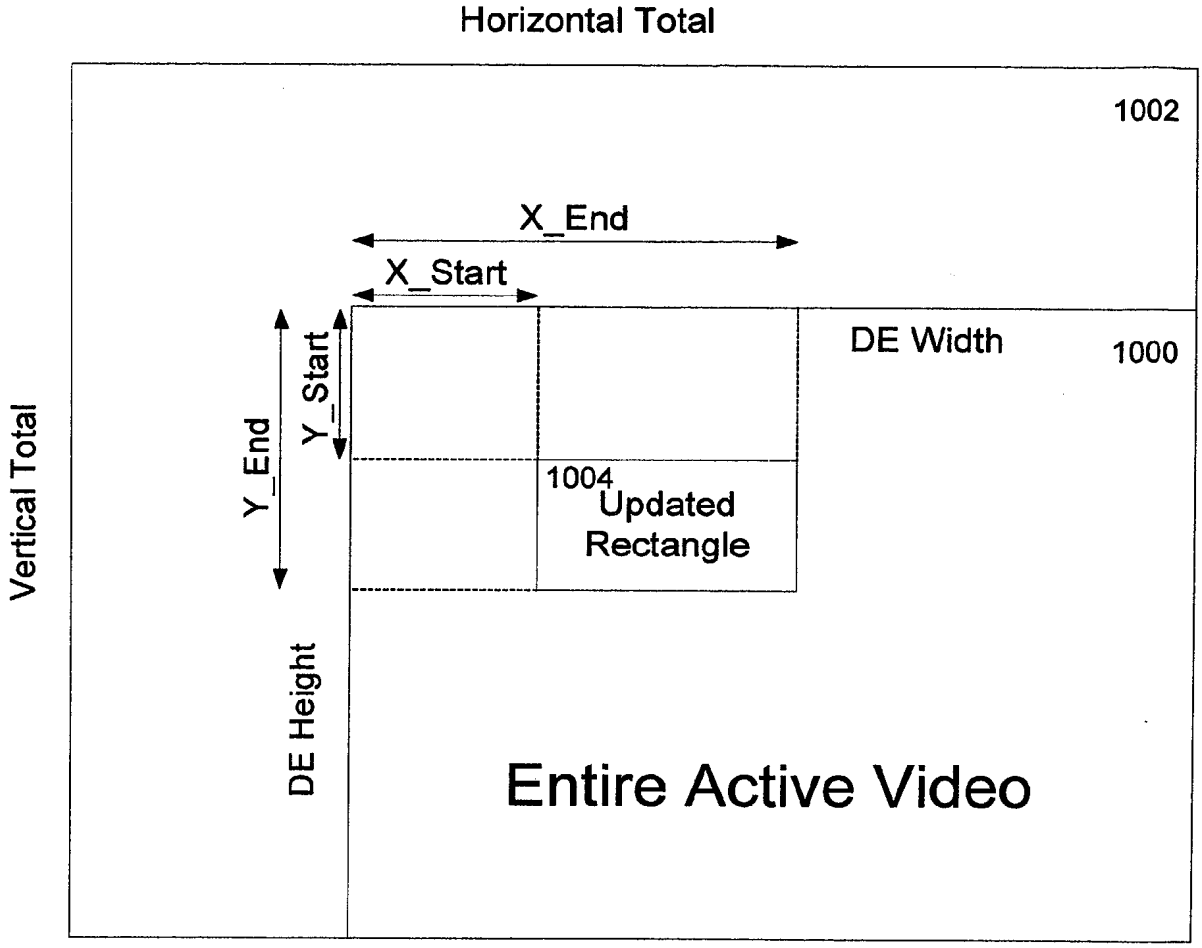


Fig. 10

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Phase	Transmitted Link Characters	Binary pattern
1	D10.2	0101010101 0101010101 0101010101 0101010101 0101010101
2	K28.7	0011111000 0011111000 0011111000 0011111000 0011111000
3	K28.5, and three D10.2	0011111010 0101010101 0101010101 0101010101 1100000101

Main Link Training Pattern

Fig. 11

LENOVO EXHIBIT 1002 - 105/502

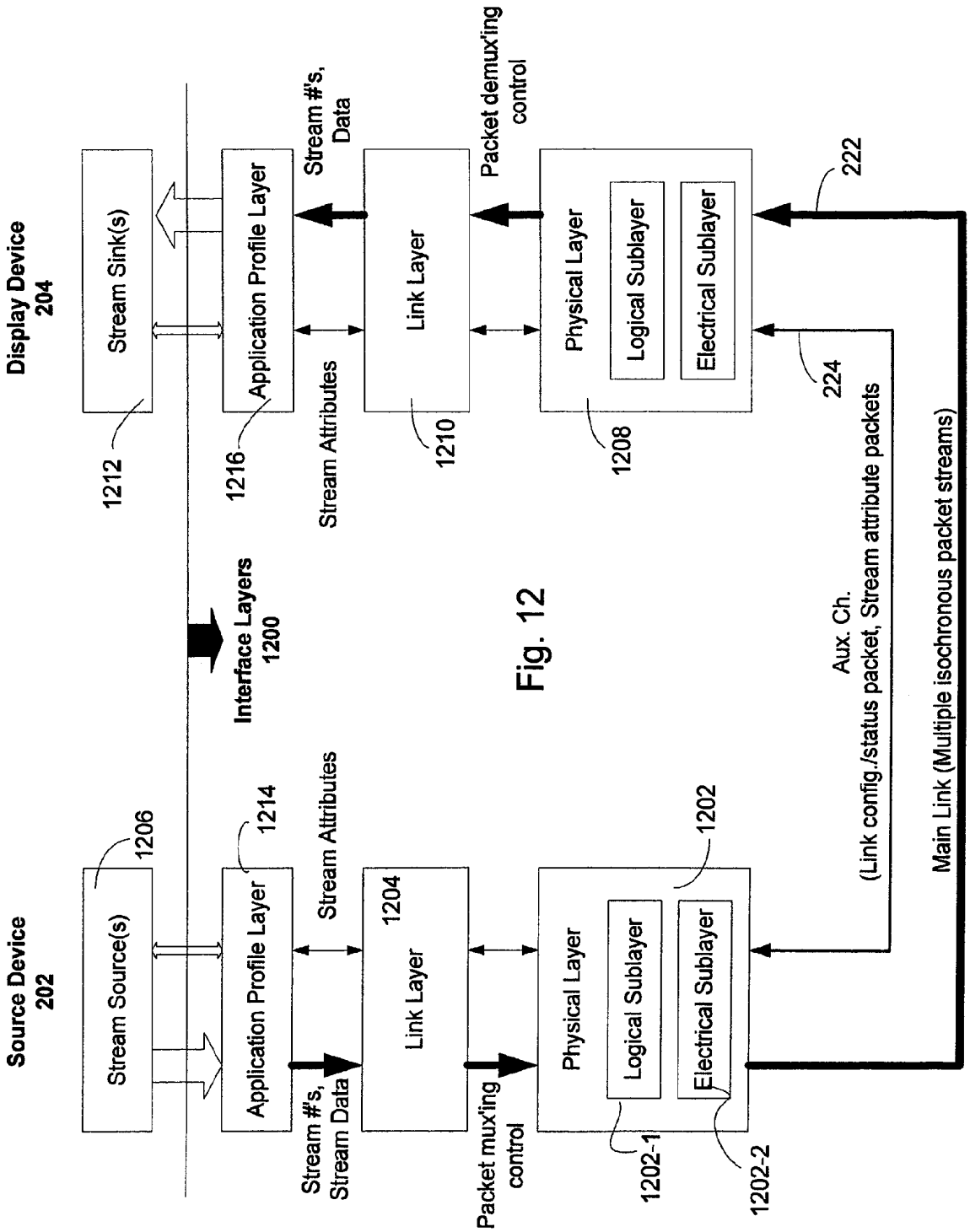


Fig. 12

LENOVO EXHIBIT 1002 - 106/502

8B/10B Special Characters Usage

Encoding	Name	Description
K28.5	Comma (COM)	Inserted between packets. Also used as part of Test Pattern
K28.7	TrainingPattern (TPN)	Sent during Training Pattern transmission for bit/byte clock lock.
K23.7	Null (NUL)	Sent within the packet period when there is no data to transmit.
K28.2	Sub-packet Start (SPS)	Indicate a start of sub-packet inserted in a packet
K29.7	Sub-packet End (SPE)	Indicate an end of sub-packet inserted in a main packet.
K28.0	PacketHeaderIndicator (PHI)	Sent along with 16 bits of header for header identification.
K28.1		Reserved
K28.3		Reserved
K28.4		Reserved
K28.6		Reserved
K25.7		Reserved
K27.7		Reserved

Fig. 13

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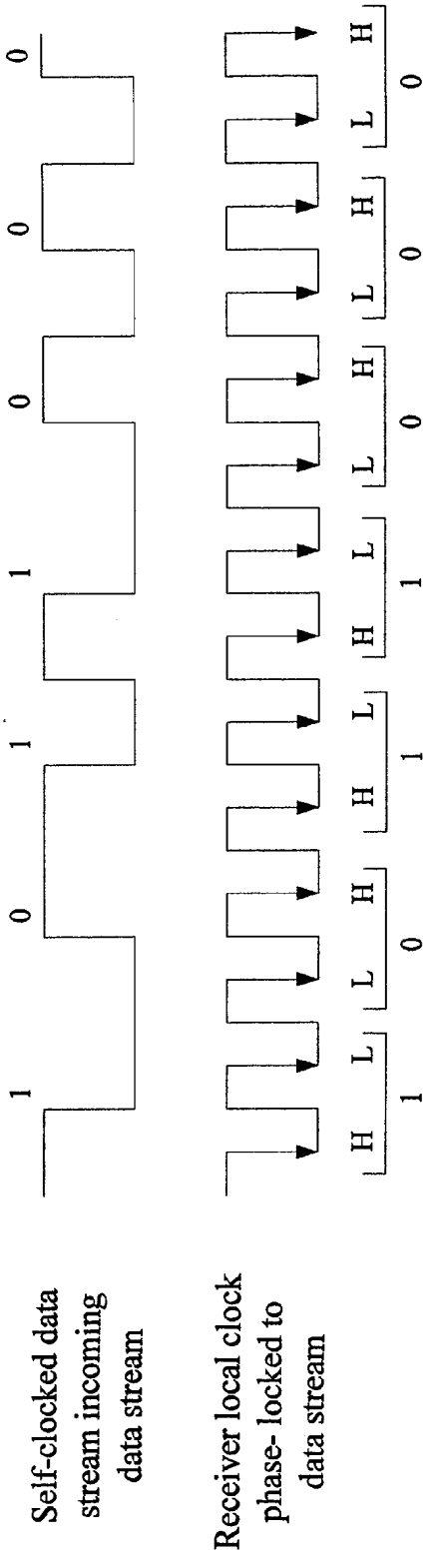


Fig. 14

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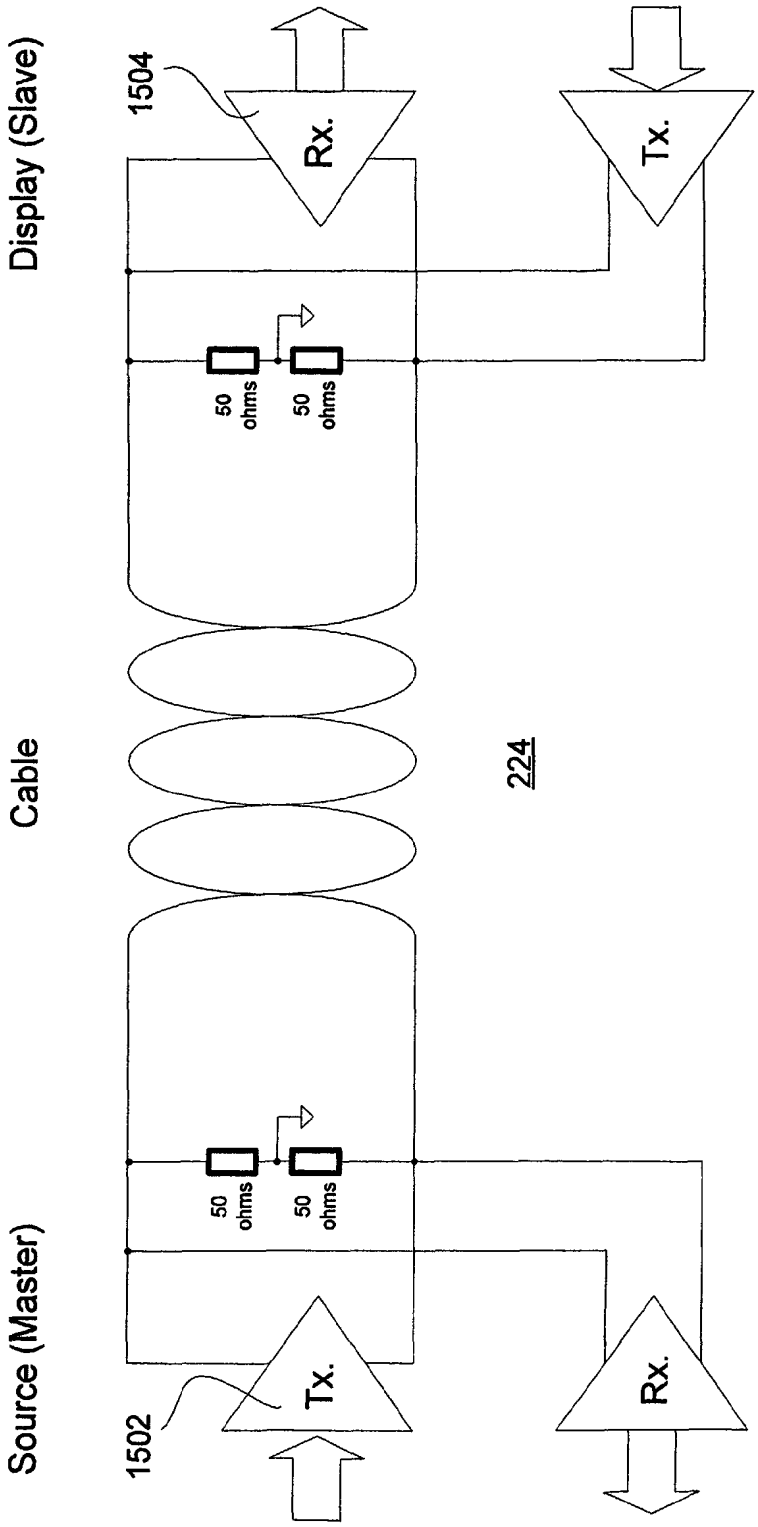
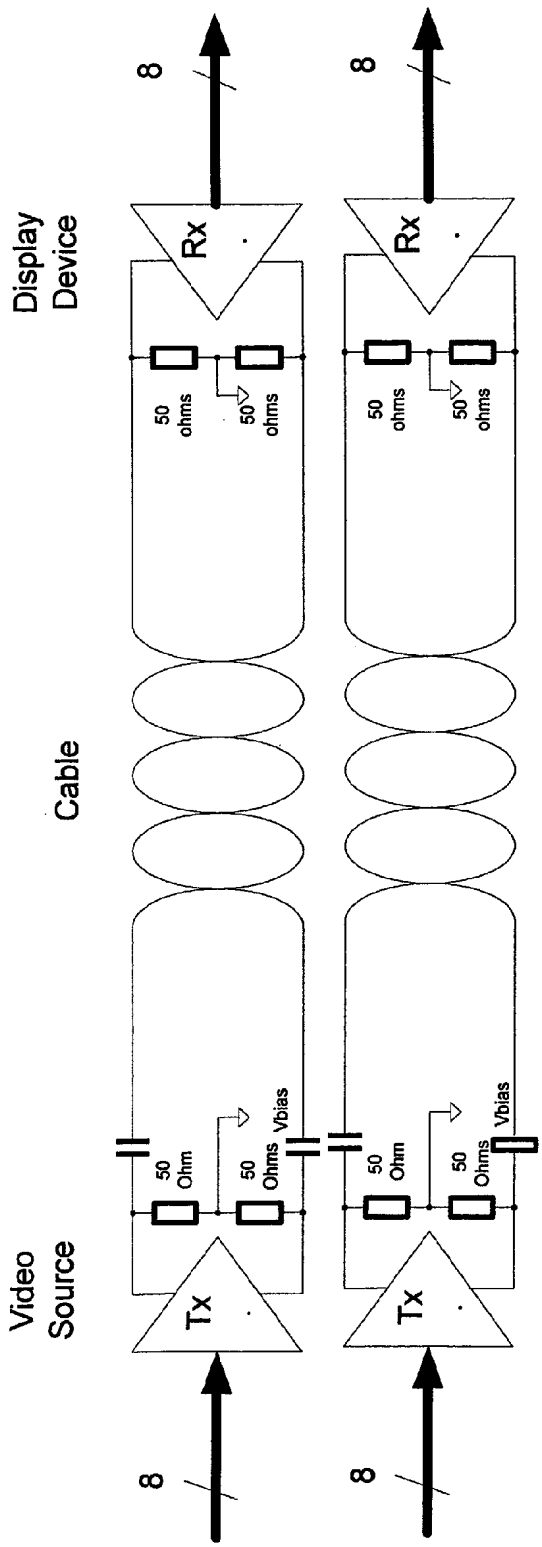


Fig. 15

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Fig. 16

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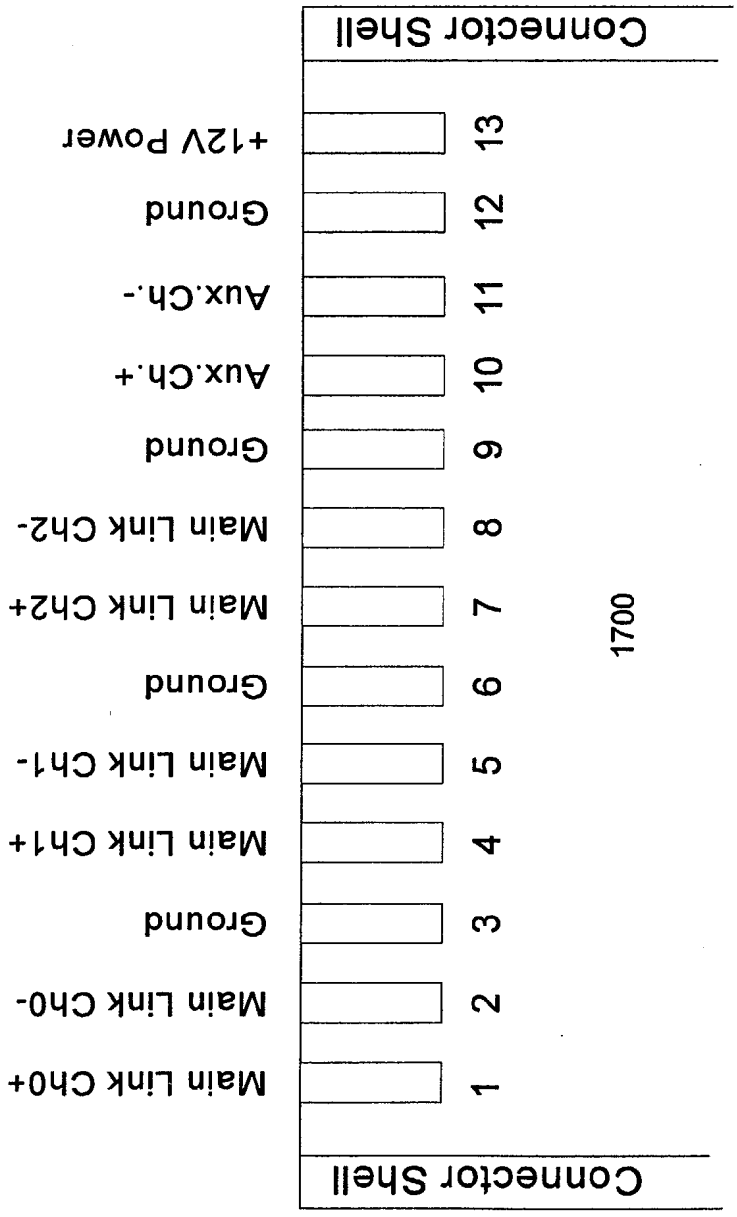


Fig. 17

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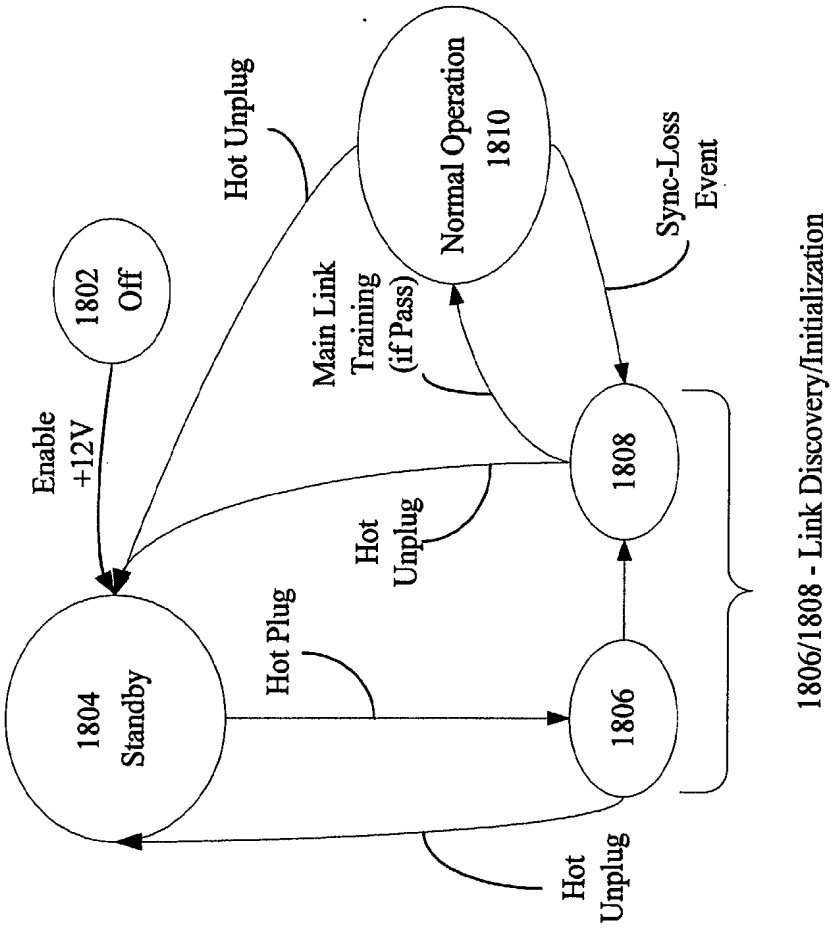


Fig. 18

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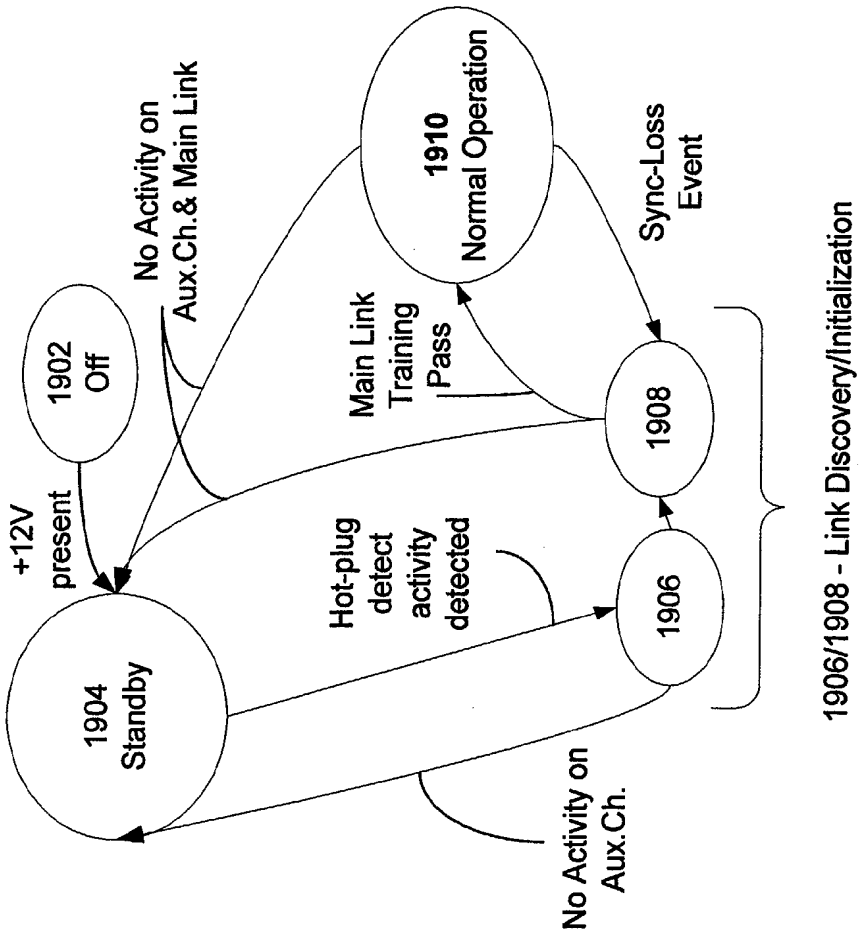
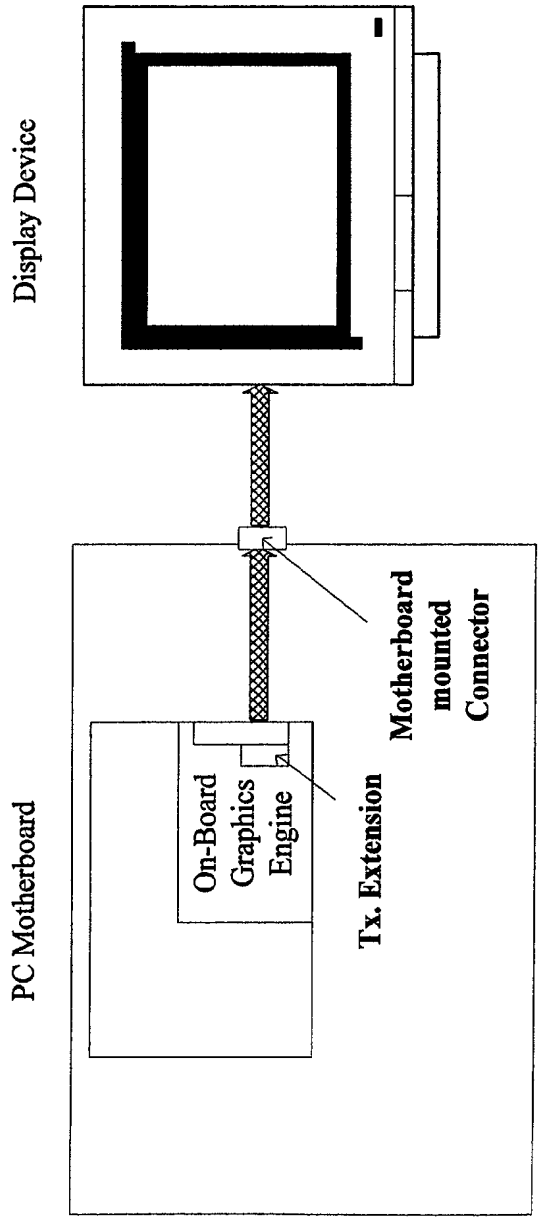


Fig. 19

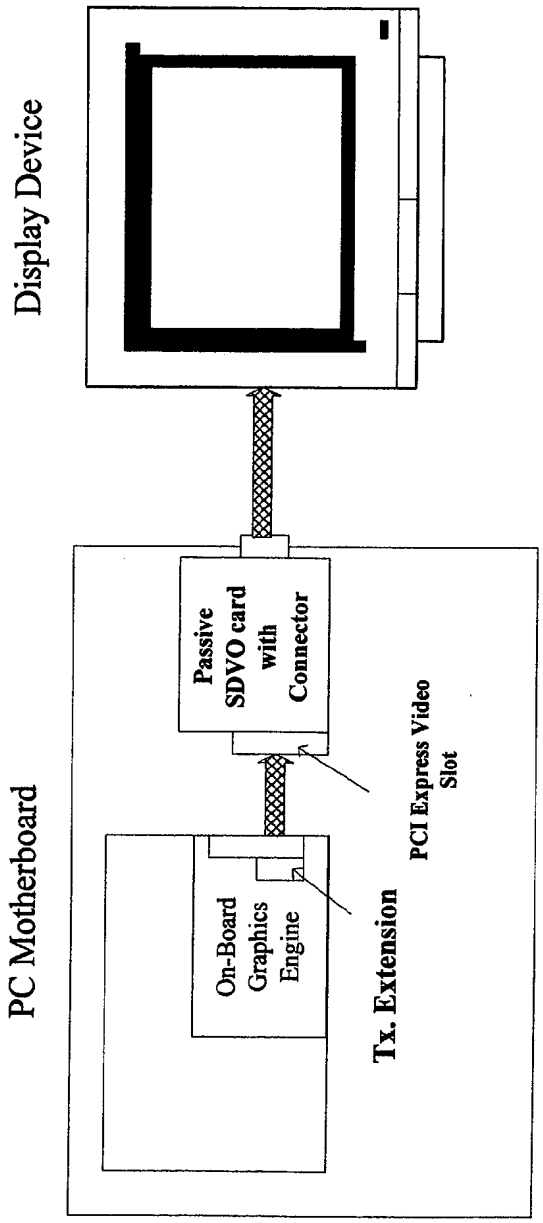
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PCI EXPRESS MOTHERBOARD WITH DEDICATED DD-EXPRESS CONNECTOR

Fig. 20

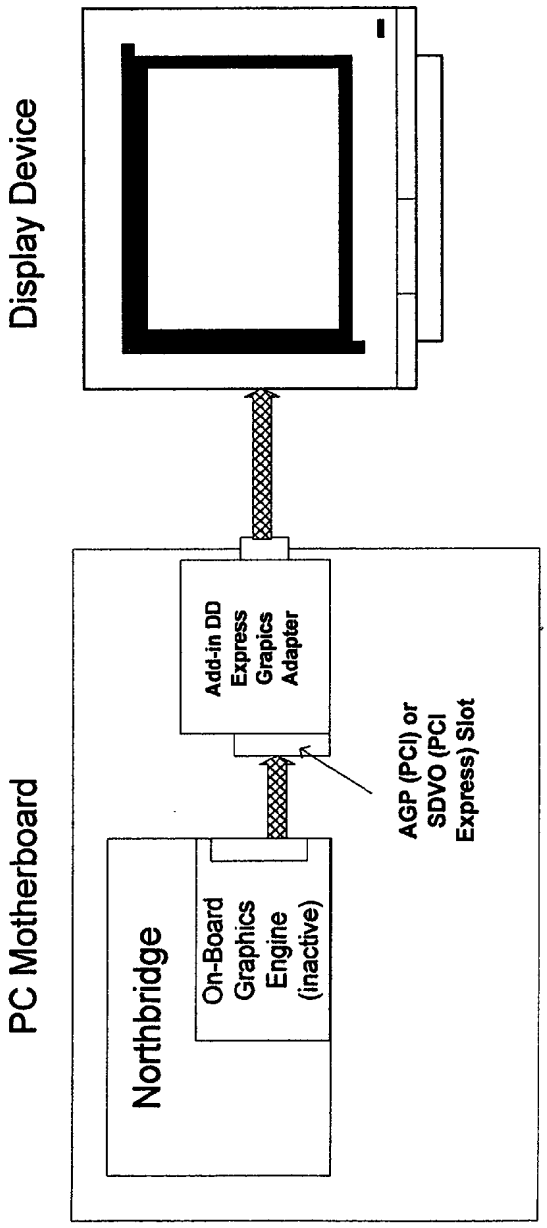
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PCI Express motherboard with passive connector card.

Fig. 21

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PCI Express motherboard with add-in DD-Express graphics card

Fig. 22

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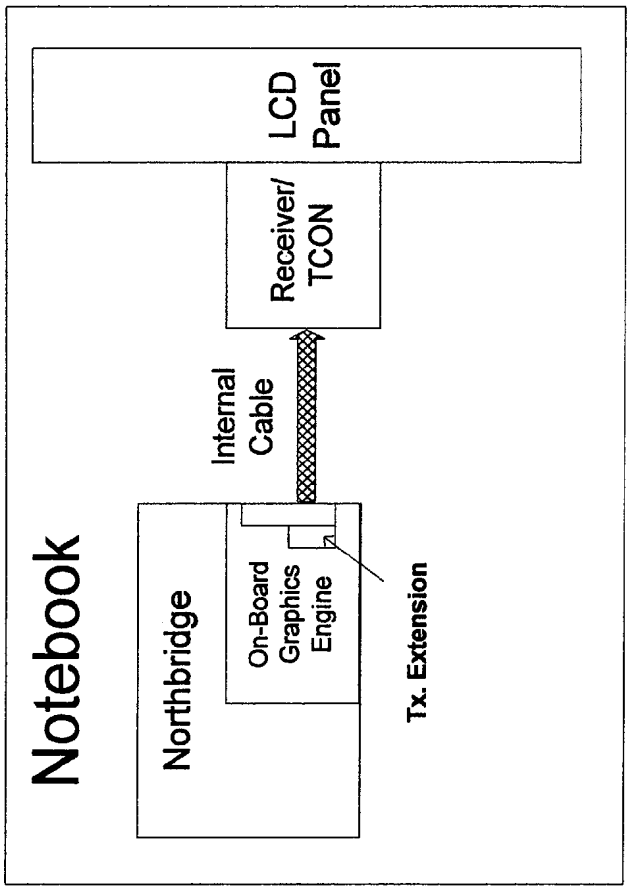
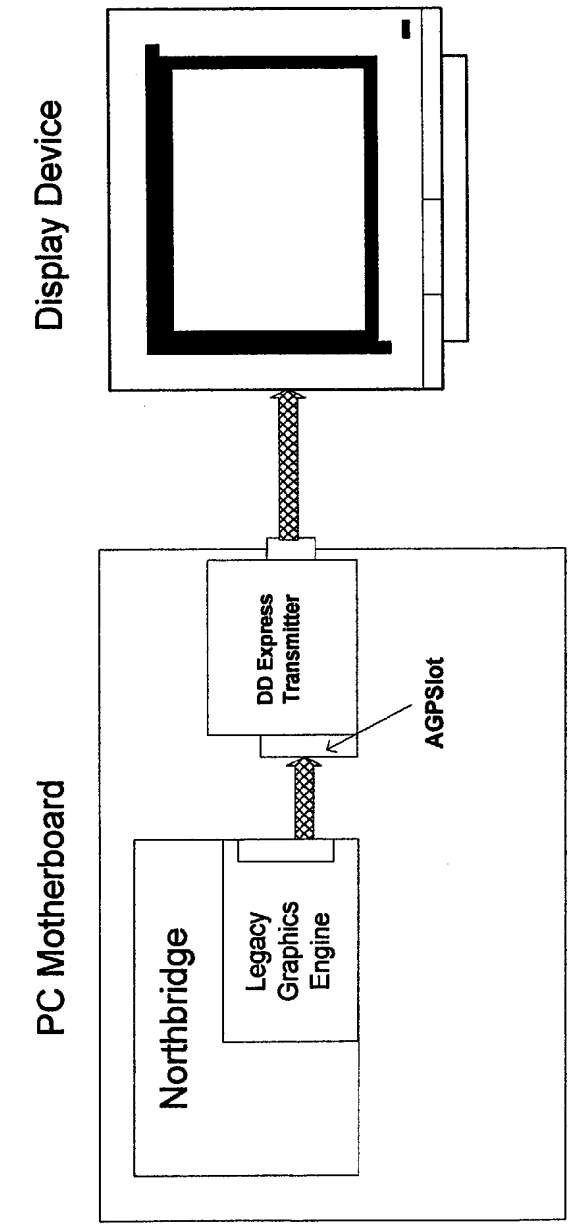


Fig. 23

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Legacy graphics accelerator bus transmitter mounted on a legacy bus card slot converts digital raster data/timing signals into main link streams

Fig. 24

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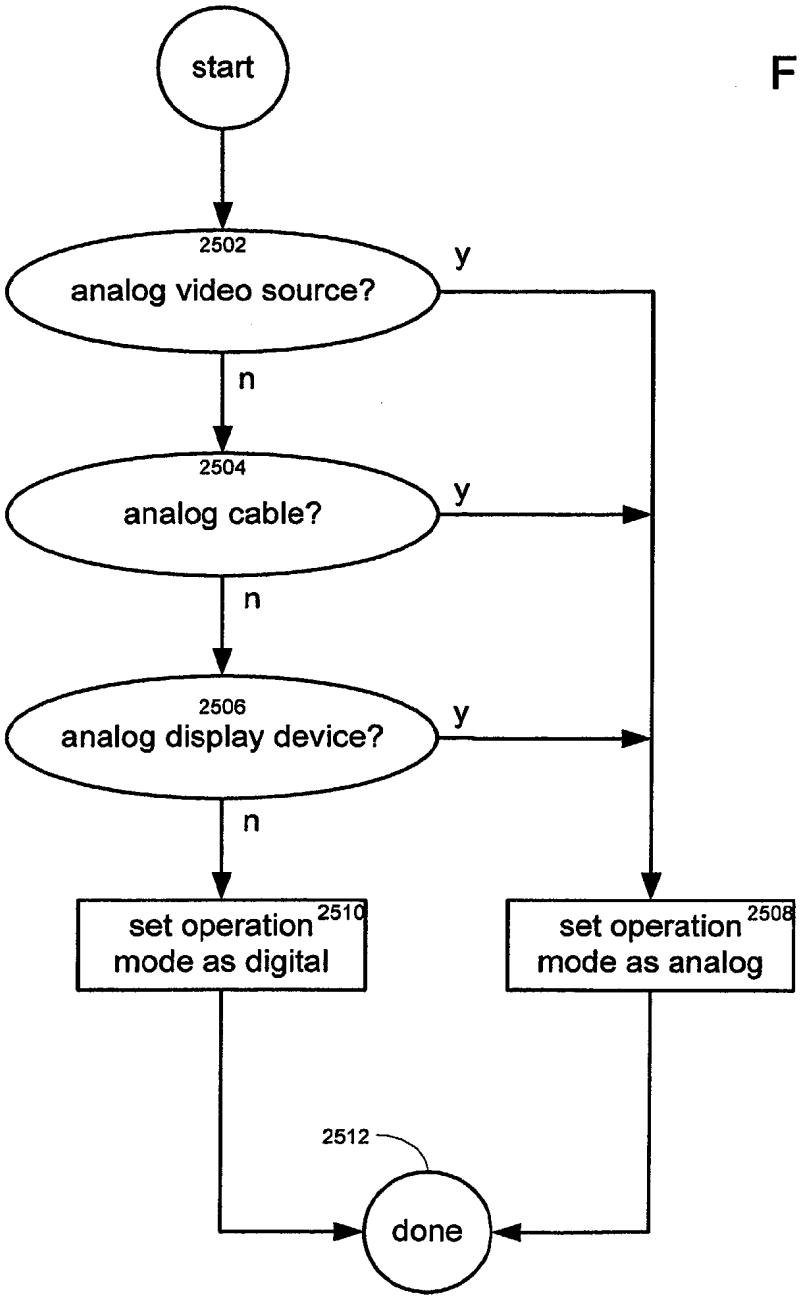


Fig. 25

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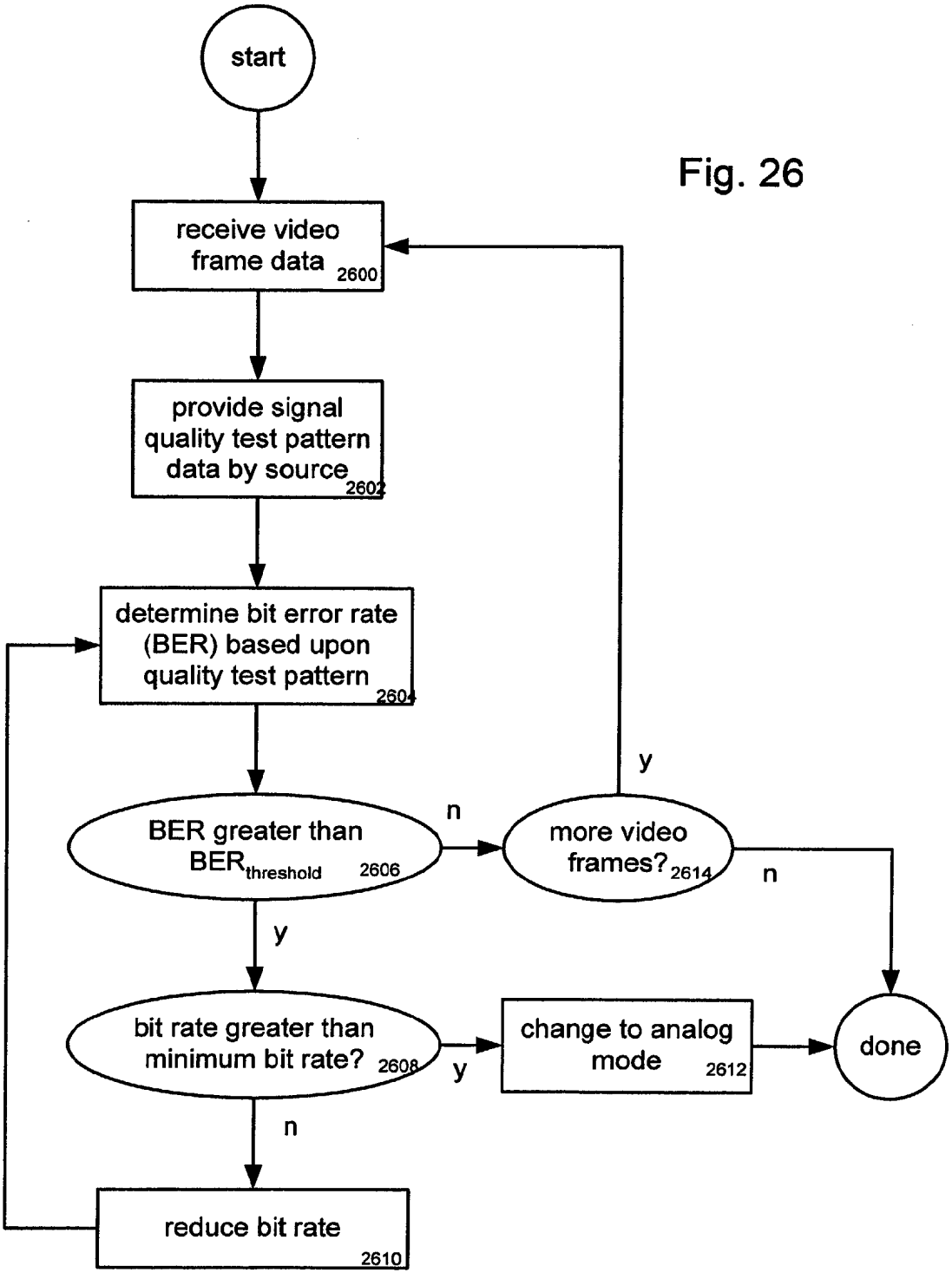


Fig. 26

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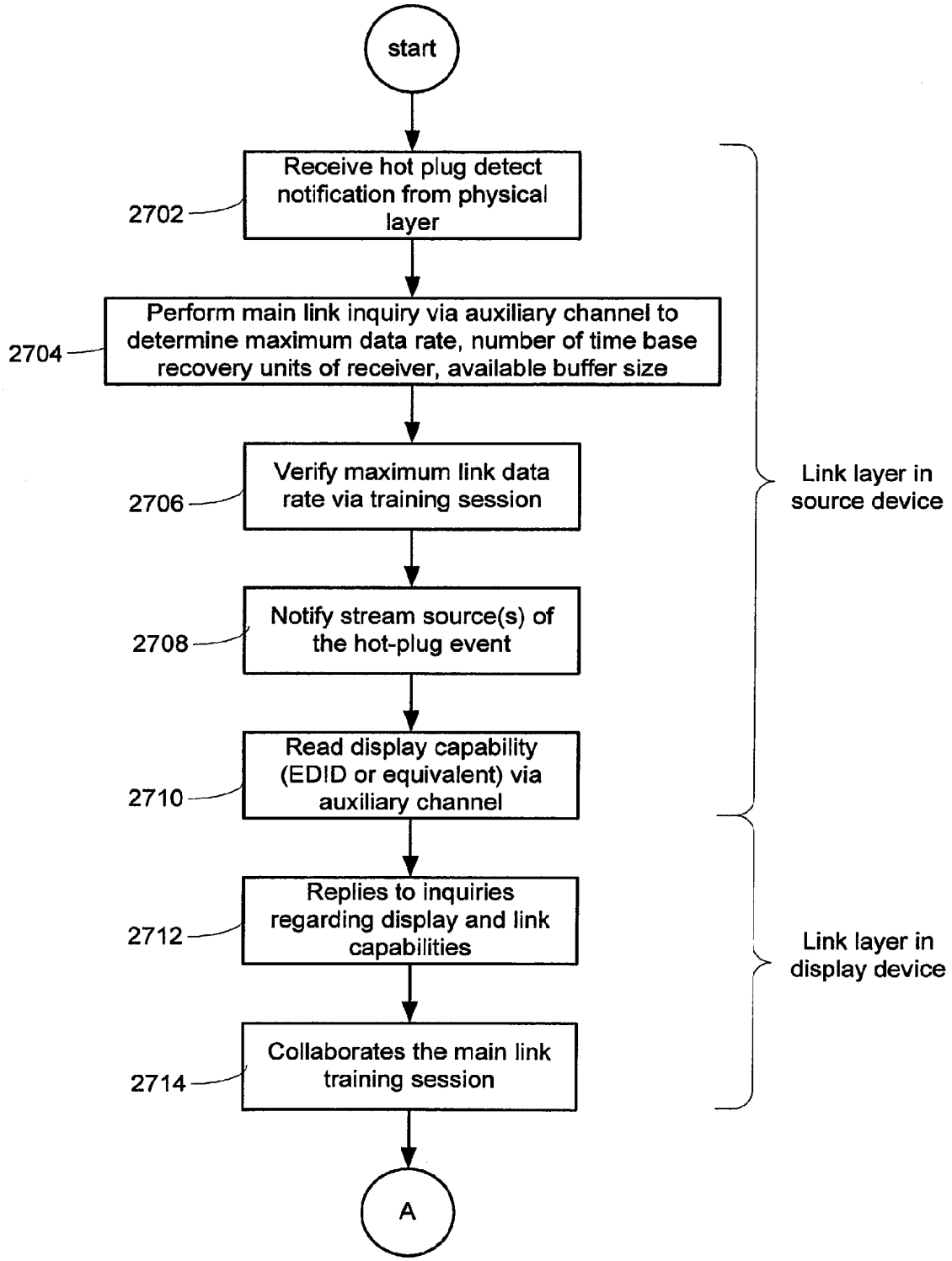


Fig. 27A

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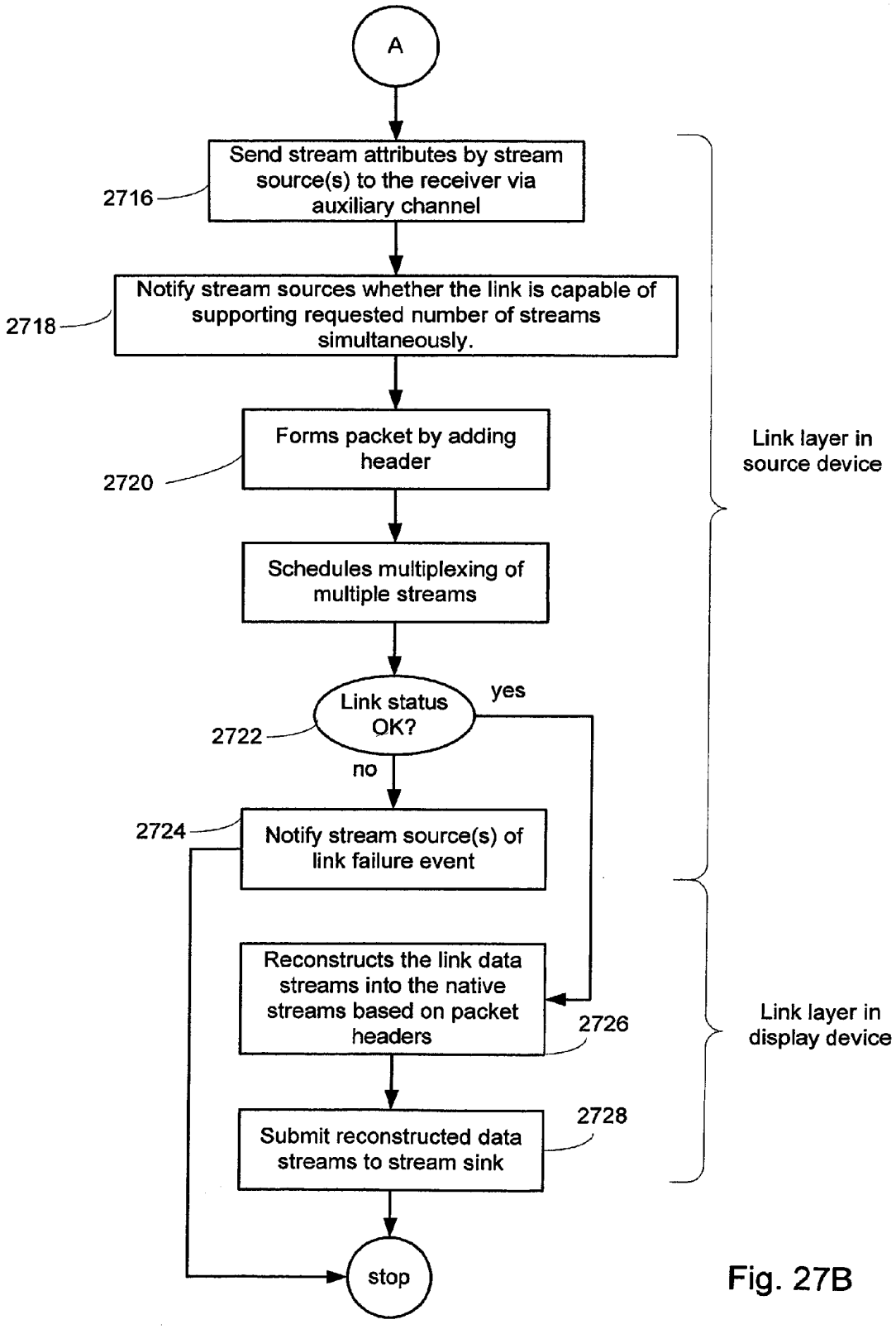


Fig. 27B

LENOVO EXHIBIT 1002 - 122/502

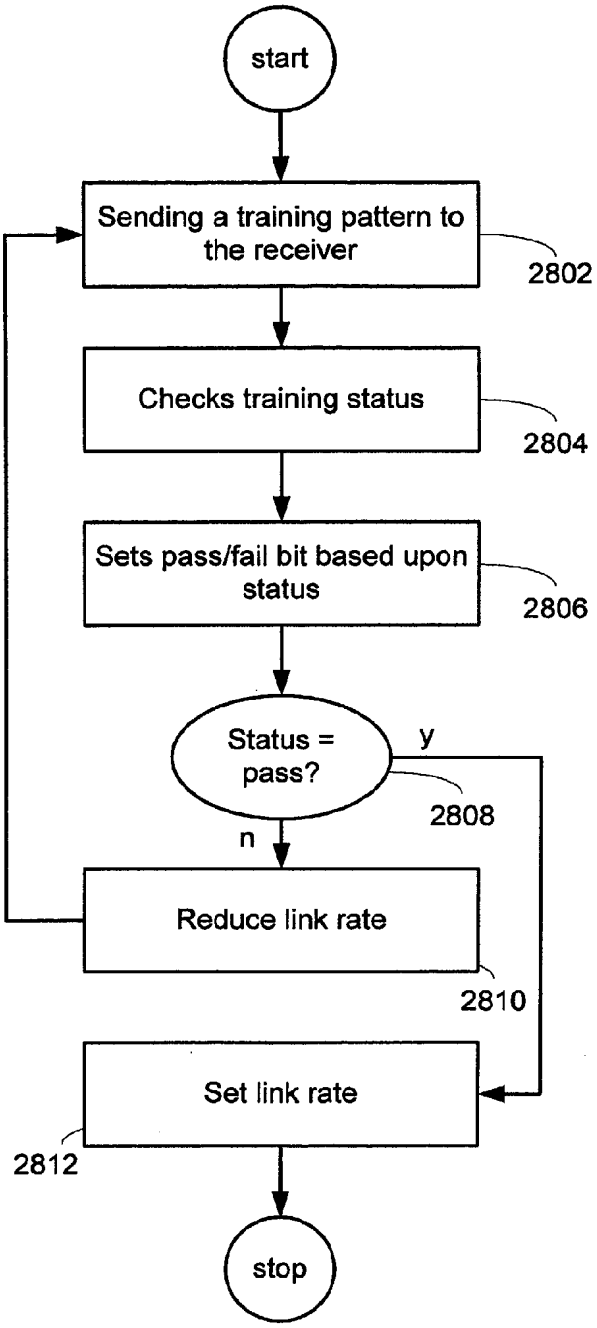


Fig. 28

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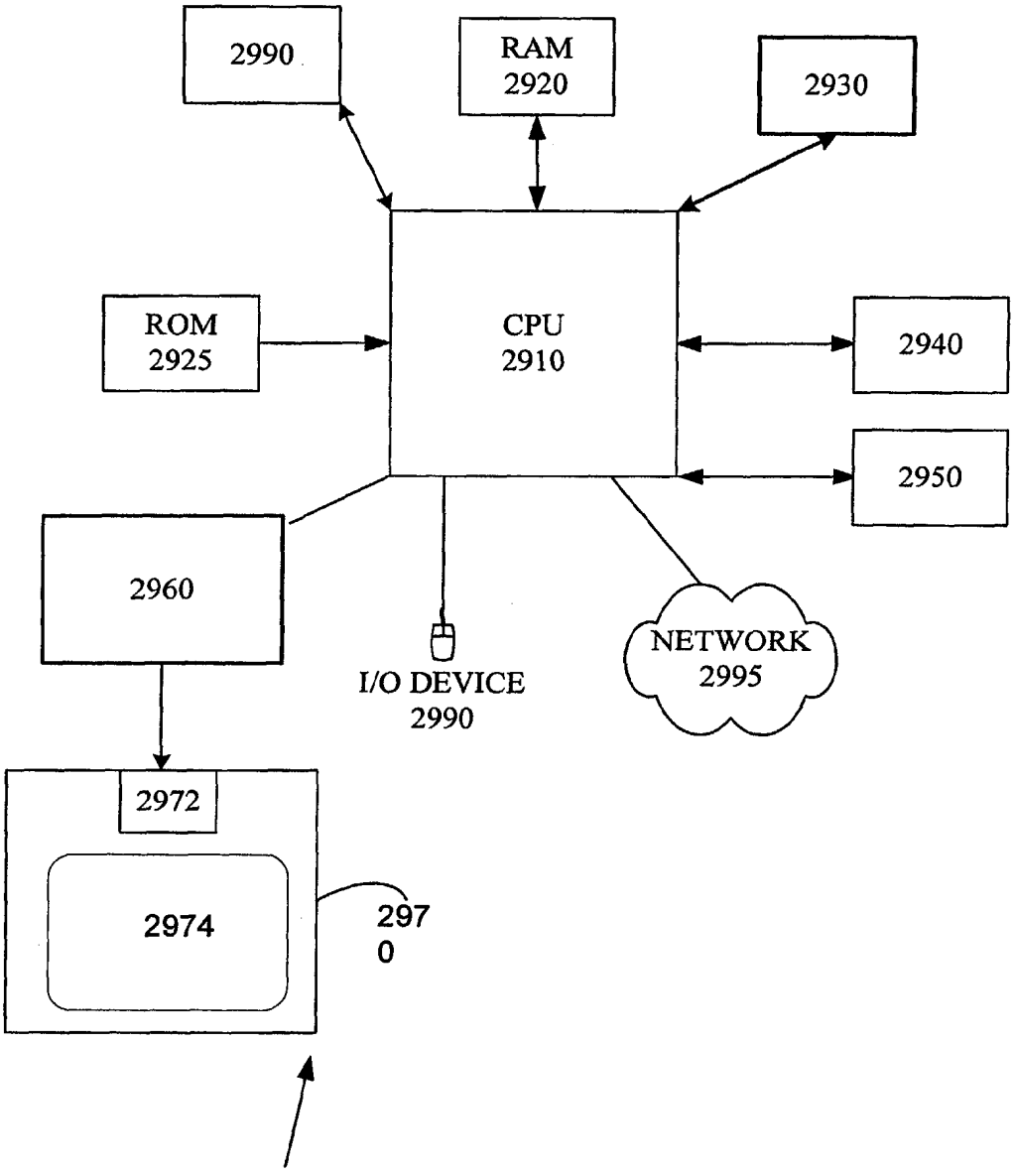


Fig. 29

LENOVO EXHIBIT 1002 - 124/502

Electronic Acknowledgement Receipt

EFS ID:	5293390
Application Number:	11969852
International Application Number:	
Confirmation Number:	1782
Title of Invention:	CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Shrikant Ranade
Correspondence Address:	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP - SEVENTH FLOOR 12400 WILSHIRE BOULEVARD LOS ANGELES CA 90025-1026 US 503 439 8778 -
Filer:	Mark C. Van Ness/gayle bekish
Filer Authorized By:	Mark C. Van Ness
Attorney Docket Number:	8029P038
Receipt Date:	07-MAY-2009
Filing Date:	04-JAN-2008
Time Stamp:	17:12:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		8029P038_IDS_05072009.pdf	275758 71c4851b2afbbebb20f71ae9b8a5dd84576ccd39	yes	2

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Transmittal Letter	1	1
Information Disclosure Statement (IDS) Filed (SB/08)	2	2

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Information:					
2	NPL Documents	8029P038PCT_ISRWO_mailed_03092009.pdf	1158646 0bafc6a744ede70a20e0d6dff77c048a4026b90f	no	12
Warnings:					
Information:					
3	Foreign Reference	EP1473701.pdf	1607424 093f1381901af09946264b2676f38b0626bef508	no	49
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	11/969,852
	Filing Date	January 4, 2008
	First Named Inventor	Ranade, Shrikant
	Group Art Unit	2111
	Examiner Name	Unknown
Sheet 1 of 1	Attorney Docket No: 8029P038	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-20070286246	12/13/2007	KOBAYASHI, Osamu	
		US-7,187,307	03/06/2007	SCHMIDT, Brian K., et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [2]
		EP-1473701	11/03/2004	GENESIS MICROCHIP, INC.,		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
		"8029P038PCT ISRWO Mailed 3/9/2009 for PCT/US2009/085288", (3/9/2009), Whole Document	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	11/969852
Filing Date	January 4, 2008
First Inventor	Shrikant Ranade, et al.
Art Unit	2111
Examiner Name	TBD
Attorney Docket No.	8029P038 Conf. No. 1782

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of a first Office Action. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The references were cited in a Search Report dated March 9, 2009 (copy enclosed herewith).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☐ The IDS Filing Fee in the amount of $180.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 02-2666.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Mark C. Van Ness/	Date (YYYY-MM-DD)	2009- 05-07
Name/Print	Mark C. Van Ness	Registration Number	39,865

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Gayle Bekish /Gayle Bekish/ *Date* *05-07-09*

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/969,852	01/04/2008	Shrikant Ranade	8029P038

CONFIRMATION NO. 1782

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025-1026

PUBLICATION NOTICE



Title:CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES

Publication No.US-2009-0177820-A1
Publication Date:07/09/2009

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In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/969,852	01/04/2008	Shrikant Ranade	8029P038	1782

7590 09/25/2009

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025-1026

EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

MAIL DATE	DELIVERY MODE
09/25/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/969,852	RANADE ET AL.	
	Examiner	Art Unit	
	THOMAS J. CLEARY	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 January 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20090507*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-5, 11, 14-15, 19, and 22-23 are rejected under 35 U.S.C. 102(b) as being anticipated by the Maxim 1-Wire network, as described in Maxim Application Note 244 “Advanced 1-Wire Network Driver” (“Maxim”).

3. In reference to Claim 1, Maxim discloses a method comprising: coupling a transmitting device to a receiving device, coupling of the devices including connecting a control bus between the transmitting device and the receiving device (See Page 1 ‘Introduction’), the control bus being a bi-directional, single-line bus (See Page 1 ‘Abstract’); obtaining control of the control bus for either the transmitting device or the receiving device, the device obtaining control becoming an initiator and the other device becoming a follower (See Page 3 'Reset Presence and Detect'); converting one or more control signals to one or more data packets, each of the one or more control signals representing one of a plurality of different types of control signals (See Pages 4-6

'Communication Time Slots'); and transmitting the generated data packets from the initiator to the follower via the control bus (See Pages 4-6 'Communication Time Slots').

4. In reference to Claim 3, Maxim discloses the limitations as applied to Claim 1 above. Maxim further discloses obtaining control of the control bus includes arbitrating between the transmitting device and the control device for control of the control bus (See Pages 3-4 'Reset Presence and Detect').

5. In reference to Claim 4, Maxim discloses the limitations as applied to Claim 3 above. Maxim further discloses that for the transmitting device, arbitrating for control of the control bus includes: determining the control bus is idle or unused for a certain period; if the control bus is been idle or used, then sending a low signal for a first number of cycles; and after the conclusion of the first number of cycles, then taking control the control bus (See Pages 3-4 'Reset Presence and Detect').

6. In reference to Claim 5, Maxim discloses the limitations as applied to Claim 3 above. Maxim further discloses that for the receiving device, arbitrating for control of the control bus includes: determining the control bus is idle or unused for a certain period; if the control bus is idle or unused, then sending a low signal followed by a high signal for a first number of cycles; during the first number of cycles, checking a status of the control bus; if the status of the control bus is a high signal, taking control of the control bus (See Pages 3-4 'Reset Presence and Detect').

.

7. Claim 11 recites limitations that are substantially equivalent to those of Claim 1 and is rejected under similar reasoning.

8. In reference to Claim 14, Maxim discloses the limitations as applied to Claim 11 above. Maxim further discloses a switchable pull-up circuit coupled with the control bus (See Pages 1-2 'Circuit Descriptions' and Figure 1).

9. Claim 15 recites limitations that are substantially equivalent to those of Claim 3 and is rejected under similar reasoning.

10. Claim 19 recites limitations that are substantially equivalent to those of Claim 1 and is rejected under similar reasoning.

11. In reference to Claim 22, Maxim discloses the limitations as applied to Claim 19 above. Maxim further discloses a switchable pull-down circuit coupled with the control bus (See Pages 1-2 'Circuit Descriptions' and Figure 1).

12. Claim 23 recites limitations that are substantially equivalent to those of Claim 3 and is rejected under similar reasoning.

13. Claims 1, 3-5, 11, 13-15, 19, and 21-23 are rejected under 35 U.S.C. 102(b) as being anticipated by the US Patent Number 6,112,275 to Curry et al. ("Curry").

14. In reference to Claim 1, Curry discloses a method comprising: coupling a transmitting device to a receiving device, coupling of the devices including connecting a control bus between the transmitting device and the receiving device (See Figure 12), the control bus being a bi-directional, single-line bus (See Abstract); obtaining control of the control bus for either the transmitting device or the receiving device, the device obtaining control becoming an initiator and the other device becoming a follower (See Column 37 Lines 3-36); converting one or more control signals to one or more data packets, each of the one or more control signals representing one of a plurality of different types of control signals (See Column 37 Lines 10-29); and transmitting the generated data packets from the initiator to the follower via the control bus (See Column 37 Lines 10-29).

15. In reference to Claim 3, Curry discloses the limitations as applied to Claim 1 above. Curry further discloses obtaining control of the control bus includes arbitrating between the transmitting device and the control device for control of the control bus (See Column 37 Lines 3-10).

16. In reference to Claim 4, Curry discloses the limitations as applied to Claim 3 above. Curry further discloses that for the transmitting device, arbitrating for control of

the control bus includes: determining the control bus is idle or unused for a certain period; if the control bus is been idle or used, then sending a low signal for a first number of cycles; and after the conclusion of the first number of cycles, then taking control the control bus (See Column 37 Lines 3-10).

17. In reference to Claim 5, Curry discloses the limitations as applied to Claim 3 above. Curry further discloses that for the receiving device, arbitrating for control of the control bus includes: determining the control bus is idle or unused for a certain period; if the control bus is idle or unused, then sending a low signal followed by a high signal for a first number of cycles; during the first number of cycles, checking a status of the control bus; if the status of the control bus is a high signal, taking control of the control bus (See Column 37 Lines 3-10).

.

18. Claim 11 recites limitations that are substantially equivalent to those of Claim 1 and is rejected under similar reasoning.

19. In reference to Claim 13, Curry discloses the limitations as applied to Claim 11 above. Curry further discloses that transmitting the one or more data packets includes transmitting a sync pulse to the receiving device to synchronize a clock of the receiving device to a clock of the transmitting device (See Column 44 Lines 8-13).

20. In reference to Claim 14, Maxim discloses the limitations as applied to Claim 11 above. Maxim further discloses a switchable pull-up circuit coupled with the control bus (See Column 42 Lines 11-20).

21. Claim 15 recites limitations that are substantially equivalent to those of Claim 3 and is rejected under similar reasoning.

22. Claim 19 recites limitations that are substantially equivalent to those of Claim 1 and is rejected under similar reasoning.

23. Claim 21 recites limitations that are substantially equivalent to those of Claim 13 and is rejected under similar reasoning.

24. In reference to Claim 22, Curry discloses the limitations as applied to Claim 19 above. Curry further discloses a switchable pull-down circuit coupled with the control bus (See Figure 12).

25. Claim 23 recites limitations that are substantially equivalent to those of Claim 3 and is rejected under similar reasoning.

26. Claims 1-3, 10-13, 15, 19-21, and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by the US Patent Application Publication Number 2004/0218599 to Kobayashi ("Kobayashi").

27. In reference to Claim 1, Kobayashi discloses a method comprising: coupling a transmitting device (See Figure 2A Number 202) to a receiving device (See Figure 2A Number 204), coupling of the devices including connecting a control bus between the transmitting device and the receiving device (See Figure 2A Number 224), the control bus being a bi-directional, single-line bus (See Figure 15 and Paragraphs 50, 68, and 83); obtaining control of the control bus for either the transmitting device or the receiving device, the device obtaining control becoming an initiator and the other device becoming a follower (See Paragraphs 68, 78, 84, and 90); converting one or more control signals to one or more data packets, each of the one or more control signals representing one of a plurality of different types of control signals (See Paragraph 68); and transmitting the generated data packets from the initiator to the follower via the control bus (See Paragraphs 68, 78, 84, and 90).

28. In reference to Claim 2, Kobayashi discloses the limitations as applied to Claim 1 above. Maxim further discloses that the signaling for the control bus utilizes bi-phase mark encoding (See Paragraphs 73 and 76).

29. In reference to Claim 3, Kobayashi discloses the limitations as applied to Claim 1 above. Kobayashi further discloses that obtaining control of the control bus includes arbitrating between the transmitting device and the control device for control of the control bus (See Paragraphs 68, 78, 84, and 90).

30. In reference to Claim 10, Kobayashi discloses the limitations as applied to Claim 1 above. Kobayashi further discloses that the control bus provides a conduit to various support functions useful for link set up as well as carrying auxiliary application data such as USB traffic (See Paragraph 68). Thus, each of the requestors associated with each of the support functions as well as the requestors associated with the USB traffic must necessarily arbitrate for access to the control bus, as failure to do so would result in collisions of data, which would result in corrupted data and an inability to operate correctly.

31. Claim 11 recites limitations that are substantially equivalent to those of Claim 1 and is rejected under similar reasoning.

32. Claim 12 recites limitations that are substantially equivalent to those of Claim 2 and is rejected under similar reasoning.

33. In reference to Claim 13, Kobayashi discloses the limitations as applied to Claim 11 above. Kobayashi further discloses that transmitting the one or more data packets

includes transmitting a sync pulse to the receiving device to synchronize a clock of the receiving device to a clock of the transmitting device (See Paragraph 85).

34. Claim 15 recites limitations that are substantially equivalent to those of Claim 3 and is rejected under similar reasoning.

35. Claim 19 recites limitations that are substantially equivalent to those of Claim 1 and is rejected under similar reasoning.

36. Claim 20 recites limitations that are substantially equivalent to those of Claim 2 and is rejected under similar reasoning.

37. Claim 21 recites limitations that are substantially equivalent to those of Claim 13 and is rejected under similar reasoning.

38. Claim 23 recites limitations that are substantially equivalent to those of Claim 3 and is rejected under similar reasoning.

Claim Rejections - 35 USC § 103

39. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

40. Claims 6-9, 16-17, and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi as applied to Claims 1, 11, and 19 above, and further in view of knowledge commonly known in the art, as evidenced by HDTV UK article "Lindy announce Mini HDMI adapter for camcorders and notebooks" ("Lindy").

41. In reference to Claims 6-8, Kobayashi discloses the limitations as applied to Claim 1 above. Kobayashi is silent as to the protocol used by main link 222, and does not explicitly disclose that the receiving device is a device using a standard protocol and the transmitting device is a device utilizing a modified protocol, as in Claim 6; that the standard protocol is HDMI (High-Definition Multimedia Interface), as in Claim 7; and that the receiving device is a dual-mode device that is capable of communicating with a device that is compatible with the standard protocol device or a device that is compatible with the modified protocol, as in Claim 8. Official Notice is taken that connecting a device having a standard protocol (HDMI) to a device having a modified protocol (mini HDMI) is well known in the art (See Paragraphs 1-4 of Lindy); and that devices capable of communicating with both a device that is compatible with a standard protocol (HDMI) and a device that is compatible with a modified protocol (mini HDMI) are well known in the art (See Paragraphs 1-4 of Lindy).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Kobayashi using an HDMI device connected to a dual mode mini HDMI device, resulting in the invention of Claims 6-8, in order to increase the types of devices that can be communicated with by allowing communications, through a single port, with both devices having an HDMI port and devices having a mini HDMI port (See Paragraphs 2-4 of Lindy).

42. In reference to Claim 9, Kobayashi and knowledge commonly known in the art disclose the limitations as applied to Claim 6 above. As is well known in the art, an HDMI interconnect, such as that of Kobayashi as modified by knowledge commonly known in the art, has a plurality of different types of control signals transmitted over a plurality of control buses.

43. Claims 16 and 24 recite limitations that are substantially equivalent to those of Claim 6 and are rejected under similar reasoning.

44. Claims 17 and 25 recite limitations that are substantially equivalent to those of Claim 7 and are rejected under similar reasoning.

45. Claim 26 recites limitations that are substantially equivalent to those of Claim 8 and is rejected under similar reasoning.

46. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi as applied to Claim 11 above, and further in view of UK Patent Application Publication Number GB 2 425 696 A to Self ("Self").

47. In reference to Claim 18, Kobayashi discloses the limitations as applied to Claim 11 above. Kobayashi further discloses that the control bus can transmit USB data, and thus the transmitting device PHY is a USB PHY (See Figure 2A Number 224, Figure 12 Number 1202 and Paragraphs 47, 50, 68, and 74). Kobayashi does not disclose that the PHY is a USB-OTG PHY. Self discloses the use of USB-OTG in place of USB (See Pages 1-3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Kobayashi with a USB-OTG PHY of Self, resulting in the invention of Claim 18, in order to allow devices to function as both a peripheral and a host (See Page 2 Paragraph 3 of Self).

Claim Rejections - 35 USC § 101

48. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

49. Claim 9 is rejected under 35 U.S.C. 101 because the disclosed invention is inoperative and therefore lacks utility.

50. Claim 9 recites the limitation of "the plurality of different types of control signals would be transmitted over a plurality of control buses according to the standard protocol". Claim 1 recites the limitation of "a control bus". The limitation "a control bus" has been interpreted, according to its broadest reasonable interpretation, as being a single (one) control bus. In a system having only one control bus, control signals could not be transmitted over a plurality of control buses.

Claim Rejections - 35 USC § 112

51. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

52. Claim 9 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

53. Claim 9 recites the limitation of "the plurality of different types of control signals would be transmitted over a plurality of control buses according to the standard protocol". Claim 1 recites the limitation of "a control bus". The limitation "a control bus"

has been interpreted, according to its broadest reasonable interpretation, as being a single (one) control bus. Neither the specification nor the drawings, as originally filed, provide any disclosure as to how control signals would be transmitted over a plurality of control buses in a system having only one control bus, nor would such a feature be apparent to one of ordinary skill in the art.

54. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

55. Claims 3-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

56. Claim 3 recites the limitation "the control device" in Line 2. There is insufficient antecedent basis for this limitation in the claim.

57. Claim 4 recites the limitation "if the control bus is been idle or used". It is unclear if this means that the control bus is idle, or that the control bus has been (but is not necessarily currently) idle. For the purposes of evaluating prior art with respect to patentability, the Examiner will interpret this limitation, in accordance with the similar limitation appearing in Claim 5, as “if the control bus is idle or unused”.

58. Claims 6, 8, 16, 24, and 26 recite the limitation “a modified protocol”. It is unclear if the modified protocol is a modified version of the standard protocol, or a modified version of another protocol. It is further unclear as to whether the modified protocol refers to a modification that is not supported by the protocol standard, or a modification which is part of the protocol standard.

59. Claim 9 recites the limitation “the plurality of different types of control signals would be transmitted over a plurality of control buses according to the standard protocol”. Claim 1 recites the limitation of “a control bus”. The limitation “a control bus” has been interpreted, according to its broadest reasonable interpretation, as being a single (one) control bus. It is unclear as to how control signals would be transmitted over a plurality of control buses in a system having only one control bus. Further, the se of the term "would" renders the claim indefinite. It is unclear as to whether the limitations following the term "would" must be present in the claimed invention, or whether these limitations are merely features which are part of the standard protocol, but modified or not used by the claimed invention.

60. Claim 11 recites the limitation “the transmitting device to be coupled…”. It is unclear if the claims require that the transmitting device is currently coupled, or that the transmitting device be coupled at a later time.

61. Claim 19 recites the limitation "the receiving device to be coupled…". It is unclear if the claims require that the receiving device is currently coupled, or that the receiving device be coupled at a later time.

62. Claim 21 recites the limitation "the receiver is to receive a sync pulse from the receiving device". It is unclear as to how the receiver can receive a sync pulse from the receiving device, as the receiver is part of the receiving device.

Information Disclosure Statement

63. The information disclosure statement (IDS) submitted on 7 May 2009 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Requirement for Information

64. Applicant and the assignee of this application are required under 37 CFR 1.105 to provide the following information that the examiner has determined is reasonably necessary to the examination of this application.

65. In response to this requirement, please provide a copy of each of the following items of art referred to in the specification: High-Definition Multimedia Specification 1.3

(Hitachi, Ltd., Matsushita Electric Industrial Col, Ltd., Philips Consumer Electronics, International B.V., Silicon Image, Inc., Sony corporation, Thomson Inc., and Toshiba Corporation) (June 22, 2006).

66. In responding to those requirements that require copies of documents, where the document is a bound text or a single article over 50 pages, the requirement may be met by providing copies of those pages that provide the particular subject matter indicated in the requirement, or where such subject matter is not indicated, the subject matter found in applicant's disclosure.

67. The fee and certification requirements of 37 CFR 1.97 are waived for those documents submitted in reply to this requirement. This waiver extends only to those documents within the scope of this requirement under 37 CFR 1.105 that are included in the applicant's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this requirement and any information disclosures beyond the scope of this requirement under 37 CFR 1.105 are subject to the fee and certification requirements of 37 CFR 1.97.

68. The applicant is reminded that the reply to this requirement must be made with candor and good faith under 37 CFR 1.56. Where the applicant does not have or cannot readily obtain an item of required information, a statement that the item is

unknown or cannot be readily obtained may be accepted as a complete reply to the requirement for that item.

69. This requirement is an attachment of the enclosed Office action. A complete reply to the enclosed Office action must include a complete reply to this requirement. The time period for reply to this requirement coincides with the time period for reply to the enclosed Office action.

Conclusion

70. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Dallas Semiconductor Application Note 148 “Guidelines for Reliable 1-Wire Networks”; US Patent Application Publication Number 2008/0315943 to Engl; US Patent Number 5,210,846 to Lee; US Patent Application Publication Number 2005/0185720; US Patent Number 5,729,547 to Dute; US Patent Number 6,697,897 to Friel et al.; US Patent Application Publication Number 2007/0073449 to Kraemer et al.; US Patent Application Publication Number 2004/0015570 to Daum et al.; US Patent Number 7,181,557 to Falik et al.; US Patent Number 5,239,732 to Cusey; and US Patent Number 6,532,506 to Dunstan et al.

71. This Office action has an attached requirement for information under 37 CFR 1.105. A complete reply to this Office action must include a complete reply to the

attached requirement for information. The time period for reply to the attached requirement coincides with the time period for reply to this Office action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to THOMAS J. CLEARY whose telephone number is (571)272-3624. The examiner can normally be reached on Monday-Thursday (7-3).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thomas J. Cleary/
Primary Examiner, Art Unit 2111

Notice of References Cited	Application/Control No. 11/969,852	Applicant(s)/Patent Under Reexamination RANADE ET AL.	
	Examiner THOMAS J. CLEARY	Art Unit 2111	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,112,275	08-2000	Curry et al.	711/100
*	B	US-2004/0218599	11-2004	Kobayashi, Osamu	370/389
*	C	US-2008/0315943	12-2008	Underhill, Michael James	327/552
*	D	US-5,210,846	05-1993	Lee, Robert D.	710/115
*	E	US-2005/0185720	08-2005	Kwok, Chung Y.	375/257
*	F	US-5,729,547	03-1998	Dute, John C.	370/447
*	G	US-6,697,897	02-2004	Friel et al.	710/105
*	H	US-2007/0073449	03-2007	Kraemer et al.	701/001
*	I	US-2004/0015570	01-2004	Daum et al.	709/220
*	J	US-7,181,557	02-2007	Falik et al.	710/110
*	K	US-5,239,732	08-1993	Steven, Zack	24/575.1
*	L	US-6,532,506	03-2003	Dunstan et al.	710/100
*	M	US-2009/0177818	07-2009	Shim et al.	710/100

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	GB 2425696 A	11-2006	United Kingdom	SELF, DALE	
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"Advanced 1-Wire Network Driver". Application Note 244. Maxim Integrated Products. 30 May 2003. Pages 1-13.
	V	"Lindy announce Mini HDMI adapter for camcorders and notebooks". HDTV UK. Online 28 September 2007. Retrieved from Internet 23 Septermber 2009. <http://www.hdtvuk.tv/2007/09/lindy_announce_1.html>.
	W	"Guidelines for Reliable 1-Wire Networks". Application Note 148. Dallas Semiconductor/Maxim. 19 June 2002. Pages 1-21.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination
11/969,852	RANADE ET AL.
Examiner	**Art Unit**
THOMAS J. CLEARY	2111

SEARCHED			
Class	Subclass	Date	Examiner
710	2,8,11,14, 300,105,1 06,107, 110		
	119		
	306,315		

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
Attached EAST BRS	9/23/2009	TJC
Google Search	9/23/2009	TJC
Inventor Search	9/23/2009	TJC
Rule 105 Request Approved	9/23/2009	MHR

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11969852	RANADE ET AL.
	Examiner	Art Unit
	THOMAS J CLEARY	2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/23/2009								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
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	8	✓								
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	23	✓								
	24	✓								
	25	✓								
	26	✓								

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L12	263	(ranade-shri$ peysakhovich-ale$ lee-hyuck$ choi-hoon$).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/23 10:05
S1	4	("20070286246" "7187307").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 08:33
S2	67	(((single adj (wire line bit)) single-wire single-line single-bit) near2 bus with (bidirectional bi-directional "bi directional")) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 08:22
S3	152	(lee.in. and dallas.as.) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 09:21
S4	121	(((one adj (wire line bit)) one-wire one-line one-bit) near2 bus with (bidirectional bi-directional "bi directional")) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 09:52
S5	2	"5045675".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 10:19
S6	2	"5729547".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 10:19

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S7	28	kraemer-rolf.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 10:46
S8	2	"20070073449".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 10:46
S9	1	WO2005/015817	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 10:46
S10	36	(((single adj (wire line bit)) single-wire single-line single-bit) near2 bus same arbitrat$3) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 10:56
S11	2	((1-wire "1 wire" 1wire) near2 bus same arbitrat $3) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 09:57
S12	2	"7181557".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:22
S13	38	((1-wire "1 wire" 1wire) near2 bus same reset$4) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:23
S14	30	(((single adj (wire line bit)) single-wire single-line single-bit) near2 bus same reset$4) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:24

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S15	67	S13 S14	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:24
S16	13	("5210846" | "5237322" | "5636342" | "5655132" | "5758282" | "5761697" | "5809518" | "5936520" | "6108751" | "6112275" | "6239732" | "6298066" | "6941451").PN. OR ("7181557").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/09/22 10:26
S17	2	"5054299".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 13:27
S18	2	"20090177820".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 22:24
S19	2	"20090177818".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 22:25
S20	7	"10726794"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 22:41
S21	2	"20040218599".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 22:42
S22	0	(hdmi-m) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 23:39

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S23	0	("dual mode" with hdmi) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 23:48
S24	0	("dual-mode" with hdmi) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 23:48
S25	0	("multi-mode" with hdmi) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 23:49
S26	0	("multi mode" with hdmi) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 23:50
S27	1	("mini hdmi") and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/23 00:09
S28	5	(usb-otg.ti.) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/23 00:42

EAST Search History (Interference)

< This search history is empty>

9/23/09 10:13:14 AM
C:\ Documents and Settings\ tcleary\ My Documents\ EAST\ Workspaces\ 11969852.wsp

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Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	11/969,852
	Filing Date	January 4, 2008
	First Named Inventor	Ranade, Shrikant
	Group Art Unit	2111
	Examiner Name	Unknown
Sheet 1 of 1	Attorney Docket No: 8029P038	

US PATENT DOCUMENTS					
Examiner Initial*	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-20070286246	12/13/2007	KOBAYASHI, Osamu	
		US-7,187,307	03/06/2007	SCHMIDT, Brian K., et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [2]
		EP-1473701	11/03/2004	GENESIS MICROCHIP, INC.,		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
		"8029P038PCT ISRWO Mailed 3/9/2009 for PCT/US2009/085288", (3/9/2009), Whole Document	

EXAMINER /Thomas J. Cleary/ **DATE CONSIDERED** 09/23/2009

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /TJC/

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	11/969,852
	Filing Date	January 4, 2008
	First Named Inventor	Ranade, Shrikant
	Group Art Unit	2111
	Examiner Name	Unknown
Sheet 1 of 1	Attorney Docket No: 8029P038	

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	**Cite No [1]**	**Foreign Patent Document** Country Code/Number/Kind Code (if known)	**Publication Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	**T [2]**

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T [2]**
		MAXIM, *1-Wire Products Design Guide*, 4th Edition, pp 1-8, Feb. 2009. www.maxim-ic.com/yes	
		O'DONNELL, B., *White Paper HDMI™: The Digital Display Link*, IDC Analyze the Future, pp. 1-21, Dec. 2006, Framingham, MA.	
		Hitachi, Ltd. et al., *High-Definition Multimedia Interface: Specification Version 1.3*, pp. 1-231, June 22, 2006.	
		MAXIM, *1-Wire® Extended Network Standard*, pp 1-5, October 26, 2006. www.maxim-ic.com/an3925	
		MAXIM, *Choosing the Right 1-Wire® Master for Embedded Applications*, pp 1-10, May 27, 2008. www.maxim-ic.com/an4206	
		MAXIM, *Overview of 1-Wire® Technology and Its Use*, pp 1-11, June 19, 2008. www.maxim-ic.com/an1796	
		MAXIM, *DS 1994 4Kb Plus Time Memory iButton®*, pp 1-23, Nov. 2009. www.maxim-ic.com	
		MAXIM, *DS 2404 EconoRAM Time Chip,* pp 1-29, January 22, 2007. www.maxim-ic.com	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Our Docket No: 8029P038

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Shrikant Ranade	Examiner: Thomas J. Cleary
Application No: 11/969,852	Art Unit: 2111
Filed: January 4, 2008	Confirmation: 1782
For: CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES	

AMENDMENT AND RESPONSE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir or Madam:

In response to the Office Action mailed September 25, 2009, the Applicant respectfully requests the Examiner to enter the following amendment and to consider the following remark.

CERTIFICATE OF MAILING/TRANSMISSION
I hereby certify that this correspondence is being submitted electronically via EFS Web prior to 11:59 PM on the date shown below.

/Natasha French / December 28, 2009
Natasha French Date

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AMENDMENTS TO THE CLAIMS

Please amend paragraph 0040 as follows:

[0040] **Figure 1** is an illustration of an embodiment of a transmitting device coupled with a receiving device. In this illustration, a transmitter 102 is coupled to a receiver 110 via a cable 120. In this illustration, the receiver 110 may be ~~standard~~ a standard protocol device 112, which may include a dual mode HDMI receiving device. In some embodiments, the dual mode HDMI receiving device would be capable of communicating with both an HDMI transmitter and an HDMI-M transmitter. In some embodiments, the transmitter 102 may be one of multiple types of devices. In this illustration the transmitter may be a first type of transmitting device, shown as a standard protocol device 104, such as a HDMI transmitting device, or a second type of device, which is shown as a mobile protocol device 106. The mobile protocol device 106 may be an HDMI-M transmitting device, such as handheld or other mobile media device. In some embodiments, the cable 120 may be either a standard protocol cable 122 for the connection of protocol devices (such as an HDMI compatible cable), or a mobile protocol cable 124 (such as an HDMI-M compatible cable), including a single control cable and a power cable. In some embodiments, the receiver 110 utilizes the signals received on the cable 120 to discover a connection with the transmitter 102, and the transmitter utilizes the signals on the cable 120 to assist in establishing a connection, such as a hot plug connection, with the receiver 110.

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Please amend paragraph 0046 as follows:

[0046] **Figure 3** is an illustration of an arbitration process for a bi-directional, single-bit control bus. A transmitter and receiver are connected, with the connection including a bi-directional, single-bit bus 302. At some point in operation, either or both of the devices may wish to take control of the bus. In this process, there is determination of the status of the control bus 304. If it is determined that the CBUS is idle (having been unused for a certain number of cycles) or has been unused by the other device for a certain number of cycles (indicating that it is the device's turn to utilize the control bus) 306, ~~then it is determined that the bus is still in use by the other device 308,~~ then the use of the bus may be arbitrated 310. Otherwise, the device may determine that the control bus is in use by the other device 308. In an embodiment, if the transmitter and receiver seek to control the bus at approximately the same time, the transmitter will win the arbitration. If the transmitter seeks to control the bus, the transmitter will drive the bus low for a certain number of cycles (four cycles, in this example) 312, which will provide notice to the receiver that the transmitter is seeking control of the bus. The transmitter will then take control of the bus 314. If the receiver seeks control of the bus, then the receiver will drive the bus low for a cycle, and then drive the bus high for a short pulse 316. If the transmitter is not driving the bus, then the signal will stay high, and if the transmitter is driving the bus low the signal will go low. Based on this behavior, the receiver will check the signal on the CBUS during a certain period (during the second through fourth cycles in an example) 318. If the signal has remained high, this is an indication that the transmitter is not seeking control of the bus, and the receiver will take control 322. If the signal does not remain high, this is an indication that the transmitter is

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driving the signal low and is seeking control of the bus, and the transmitter again will take control 314.

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AMENDMENTS TO THE CLAIMS

Please cancel claims 10, 15, and 23 without prejudice.

Please amend the claims as follows:

1. (Currently amended) A method comprising:

coupling a ~~transmitting~~ first device to a ~~receiving~~ second device, coupling of the first and second devices including connecting a first control bus between the ~~transmitting~~ first device and the ~~receiving~~ second device, the first control bus being a bi-directional, single-line bus;

determining whether the first control bus is in use by the second device;

if the first control bus is not in use by the second device, conducting arbitration for ~~obtaining~~ control of the first control bus ~~for either the transmitting device or the receiving device,~~; and

if the first device ~~obtaining~~ the first device obtains control of the first control bus through the arbitration for control of the first control bus, the first device becoming an initiator and the [[other]] second device becoming a follower[[;]], then further comprising:

converting one or more control signals for a standard protocol to one or more data packets, each of the one or more control signals representing one of a plurality of different types of control signals, each data packet including a plurality of bits to be transmitted; and

transmitting the generated data packets from the ~~initiator~~ first device to the ~~follower~~ second device via the first control bus.

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2. (Currently amended) The method of claim 1, wherein the signaling for transmitting the one or more generated data packets on the first control bus utilizes bi-phase mark encoding.

3. (Currently amended) The method of claim 1, wherein ~~obtaining control of the control bus includes arbitrating between the transmitting device and the control device for control of the control bus~~ if the second device obtains control of the first control bus, the second device becoming the initiator and the first device becoming the follower, then further comprising:

receiving at the first device the plurality of data packets transmitted from the second device.

4. (Currently amended) The method of ~~claim 3~~ claim 1, wherein, ~~for the~~ if the first device is a transmitting device for transmission of data to the second device, then arbitrating for control of the first control bus includes:

determining the first control bus is idle or unused for a ~~certain~~ first time period;

if the first control bus is [[been]] idle or [[used]] unused for the first time period, then sending a low signal for a first number of cycles; and

after the conclusion of the first number of cycles, then taking control the first control bus.

5. (Currently amended) The method of ~~claim 3~~ claim 4, wherein, ~~for the~~ if the first device is a receiving device for reception of data from the second device, then arbitrating for control of the first control bus includes:

determining the first control bus is idle or unused for a ~~certain~~ second time period;

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if the first control bus is idle or unused for the second time period, then sending a low signal followed by a high signal for a [[first]] second number of cycles;

during the [[first]] second number of cycles, checking a status of the first control bus;

if the status of the first control bus is a high signal, taking control of the first control bus.

6. (Currently amended) The method of ~~claim 1~~ claim 5, wherein the receiving device is a device utilizing [[a]] the standard protocol and the transmitting device is a mobile device utilizing a modified protocol, the modified protocol being a modification of the standard protocol that is not included in the standard protocol.

7. (Currently amended) The method of ~~claim 6~~ claim 1, wherein the standard protocol is HDMI (High-Definition Multimedia Interface).

8. (Currently amended) The method of claim 6, wherein the receiving device is a dual-mode device that is capable of communicating with a device that is compatible with the standard protocol ~~device~~ or a device that is compatible with the modified protocol.

9. (Currently amended) The method of claim 6, wherein standard protocol requires that the plurality of different types of control signals [[would]] be transmitted over a plurality of different control buses ~~according to the standard protocol~~.

10. (Canceled)

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11. (Currently amended) A transmitting device comprising:

a connection to a single first control bus, the first control bus being a bi-directional, single-line bus, wherein the transmitting device ~~to be coupled~~ is operable for coupling with a receiving device via the first control bus;

logic to convert each of one or more control signals into a data packet, each of the one or more control signals being one of a plurality of different types of control signals for a standard protocol, each data packet including a plurality of bits to be transmitted; [[and]]

a transmitter, the transmitter to transmit the data packets to the receiving device on the first control bus[[.]]; and

logic to arbitrate use of the first control bus, the logic to arbitrate use being operable to:

determine whether the control bus is in use by the receiving device, and

if the first control bus is not in use by the receiving device, conduct arbitration for control of the first control bus.

12. (Currently amended) The transmitting device of claim 11, wherein the transmitter is to drive the first control bus in a bi-phase mark signaling manner.

13. (Currently amended) The transmitting device of claim 11, wherein transmitting the one or more data packets on the first control bus includes transmitting a sync pulse to the receiving device at the beginning of each data packet to synchronize a clock of the receiving device to a clock of the transmitting device.

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14. (Currently amended) The transmitting device of claim 11, further comprising a switchable pull-up circuit coupled with the first control bus.

15. (Canceled)

16. (Currently amended) The transmitting device of claim 11, wherein the receiving device is a device utilizing [[a]] the standard protocol and the transmitting device is a device utilizing a modified protocol, the modified protocol being a modification of the standard protocol that is not included in the standard protocol.

17. (Currently amended) The transmitting device of ~~claim 16~~ claim 11, wherein the standard protocol is HDMI (High-Definition Multimedia Interface).

18. (Currently amended) The transmitting device of claim 11, further comprising a USB-OTG (Universal Serial Bus On-The-Go) PHY (physical layer).

19. (Currently amended) A receiving device comprising:

a connection to a single first control bus, the first control bus being a bi-directional, single-line bus, wherein the receiving device ~~to be coupled~~ is operable for coupling with a transmitting device via the first control bus;

a receiver to receive one or more data packets on the first control bus, each of the one or more data packets representing one of a plurality of different types of control signals; and

logic to convert each of the one or more data packets into a control signal[[.]]

logic to arbitrate use of the first control bus, the logic to arbitrate use being operable to:

determine whether the control bus is in use by the transmitting device, and if the first control bus is not in use by the transmitting device, conduct arbitration for control of the first control bus.

20. (Currently amended) The receiving device of claim 19, wherein the receiver is operable to decode the one or more received data packets according to bi-phase mark encoding.

21. (Currently amended) The receiving device of claim 19, wherein the receiver is operable to receive a sync pulse from the ~~receiving~~ transmitting device on the first control line, the receiving device to synchronize a clock of the receiving device to a clock of the transmitting device.

22. (Currently amended) The receiving device of claim 19, further comprising a switchable pull-down circuit coupled with the first control bus.

23. (Canceled)

24. (Currently amended) The receiving device of claim 19, wherein the receiving device is a device utilizing [[a]] the standard protocol and the transmitting device is a device utilizing a modified protocol, the modified protocol being a modification of the standard protocol that is not included in the standard protocol.

25. (Currently amended) The receiving device of ~~claim 24~~ claim 19, wherein the standard protocol is HDMI (High-Definition Multimedia Interface).

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26. (Currently amended) The receiving device of claim 24, wherein the receiving device is a dual-mode device that is capable of communicating with a device utilizing the standard protocol ~~device~~ or a device utilizing the modified protocol ~~device~~.

Please add the following new claims:

27. (New) The method of claim 1, wherein the transmission of a data packet by the initating device is followed by an acknowledge (ACK) message from the following device to the initiating device on the first control line.

28. (New) The method of claim 27, wherein the initating device transmits a second data packet after receipt of the ACK message from the following device.

29. (New) The method of claim 1, wherein generating each data packet includes generating a header for each data packet to indicate a type of control signal represented by the data packet.

30. (New) The transmitting device of claim 11, wherein the logic to arbitrate use of the first control bus is further operable to take control of the first control bus if the transmitting device and the receiving device arbitrate use of the first control bus at the same time.

31. (New) The receiving device of claim 19, wherein the logic to arbitrate use of the first control bus is further operable to allow the transmitting device to take control of the first control bus if the transmitting device and the receiving device arbitrate use of the first control bus at the same time.

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REMARKS

Applicant respectfully requests reconsideration of this application. Claims 1-26 are currently pending.

Claims 1-9, 11-14, 16-22, and 24-26 have been amended. Claims 10, 15, and 23 have been canceled without prejudice. Claims 27-31 have been added.

Therefore, claims 1-9, 11-14, 16-22, and 24-31 are now presented for examination.

Claim Rejections - 35 U.S.C. § 112

The Office Action rejects claim 9 under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement.

The Office Action alleges that claim 9 contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Without any concession regarding the substance of the rejection, claim 1 and dependent claims to claim 1 have been clarified to refer to a "first control bus". Claim 9 has been clarified to indicate that the standard protocol requires that the plurality of different types of control signals be transmitted over a plurality of control buses.

Rejections under 35 U.S.C. § 112

The Office Action rejects claims 3-5 were rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the invention. It appears that claim 6, 8, 9, 11, 16, 19, 21, 24, and 26 may also be rejected under 35 U.S.C. §112, second paragraph.

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Claim 3 – Claim 3 has been canceled. It is submitted that the amended claim 1 has been amended to address the rejection, with the claim referring to the "receiving device" rather than the "control device".

Claim 4 – The claim has been corrected to read "if the first control bus is idle or unused for the first time period".

Claim 5 – The Office Action discusses claim 5 in connection with claim 4 and Applicant believes that all issues are resolved, but requests clarification if there are additional issues with regard to claim 5.

Claims 6, 8, 16, 24 and 26 – Claims 6, 16, and 24 have been amended to clarify that the "modified protocol" is a modification of the standard protocol that is not included in the standard protocol. It is submitted that the amendment to the claims fully addresses the rejection of such claims.

Claim 9 – Claim 9 has been clarified to indicate that the standard protocol requires that the plurality of different types of control signals be transmitted over a plurality of control buses.

Claim 11 – Claim 11 claims a transmitting device, and the claim has been amended to clarify that the transmitting device is operable for coupling with a receiving device via the first control bus.

Claim 19 – Claim 19 claims a receiving device, and the claim has been amended to clarify that the receiving device is operable for coupling with a transmitting device via the first control bus.

Claim 21 – Claim 21 has been corrected to indicate that the receive is to receive a sync pulse from the transmitting device on the first control line.

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Rejections under 35 U.S.C. § 101

The Office Action rejects claim 9 under 35 U.S.C. § 101 allegedly being inoperative and therefore lacking unity.

Claim 1 and dependent claims have been has been clarified to refer to a "first control bus". Claim 9 has further been clarified to indicate that the standard protocol requires that the plurality of different types of control signals be transmitted over a plurality of control buses.

Rejections under 35 U.S.C. § 102

Claim 1 includes "coupling a first device to a second device, coupling of the first and second devices including connecting a first control bus between the first device and the second device, the first control bus being a bi-directional, single-line bus"; "determining whether the first control bus is in use by the second device"; and "if the first control bus is not in use by the second device, conducting arbitration for control of the first control bus".

Claim 11 includes "a connection to a single first control bus, the first control bus being a bi-directional, single-line bus, wherein the transmitting device is operable for coupling with a receiving device via the first control bus"; and "logic to arbitrate use of the first control bus", the logic being operable to "determine whether the control bus is in use by the receiving device" and "if the first control bus is not in use by the receiving device, conduct arbitration for control of the first control bus."

Claim 19 includes "a connection to a single first control bus, the first control bus being a bi-directional, single-line bus, wherein the receiving device is operable for coupling with a transmitting device via the first control bus"; and "logic to arbitrate use

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of the first control bus", the logic being operable to "determine whether the control bus is in use by the transmitting device" and "if the first control bus is not in use by the transmitting device, conduct arbitration for control of the first control bus."

It is submitted that, among other differences, the cited reference do no include all such claim elements of independent claims 1, 11, and 19.

(1) Maxim

The Office Action rejects claims 1, 3-5, 11, 14-15, 19, and 22-23 under 35 U.S.C. § 102(b) as allegedly being anticipated by "Advanced 1-Wire Network Driver", Maxim Application Note 244, by Maxim Integrated Products, Inc. (hereinafter referred to as "*Maxim AN 244*").

Maxim AN 244 describes a driver utilizing the "1-Wire" protocol, a protocol connecting a pair of wires between devices for communication. As described on page 2 of the reference, an unshielded twisted-pair data cable is recommended for 1-Wire applications.

However, as the network is described, the driver element is a master element on the line. The driver has three connections to a supervising controller, DRIVE, DPU, and SENSE. DRIVE initiates 1-Wire communication, DPU is an active low signal to activate a dynamic pullup transistor, and SENSE is a through connection from the 1-Wire lie to the microcontroller. As indicated, to perform 1-Wire communication it is necessary to properly generate DRIVE and DPU signals and read from the 1-Wire line at the appropriate times. (*Maxim AN 244*, p. 2) The possible signals are illustrated in Figure 2, in which a reset signal is driven (driving the signal low) and, if there is not an interrupt (a Type 2 interrupt) on the line, a presence pulse (G to I) may be generated, and, if there is

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not another type of interrupt (Type 1A) then a time slot begins. The time slots for write zero, write one/read, and read are shown as Figures 3-5.

The *Maxim AN 244* reference thus describes a 1-Wire system that provides a master device that controls and resets the bus. However, *Maxim AN 244* does not provide explanation regarding how the 1-Wire network operates with regard to the slave devices. In particular, the reference does not explain the operation of the slave devices in generating signals, specifically their interrupt signals, on the 1-Wire line.

With regard to interrupts, the *Maxim AN 244* reference cites on page 3 to certain data sheets, such data sheets being "4Kb Plus Time Memory iButton", Maxim Datasheet 1994 (hereinafter "*Maxim DS 1994*") and "EconoRAM Time Chip", Maxim Datasheet 2404 (hereinafter "*Maxim DS 2044*"). A review of such data sheets in light of *Maxim AN 244* demonstrates that the 1-Wire network provided by *Maxim AN 244* does not provide the elements of claim 1 with regard to arbitration of the first control link. Rather than providing an arbitration for control of the first control line for the transmission of data packets, the data sheets indicate that interrupts are provided in response to alarm conditions, and are repeated each reset pulse until the interrupt is acknowledged. As indicated by *Maxim DS 1994*:

> **If the DS1994 detects an alarm condition, it automatically sets the corresponding alarm flag in the status register.** An interrupt condition begins whenever any alarm flag is set and the flag's corresponding interrupt bit is enabled. The interrupt condition ceases when the alarm flags are cleared (i.e., the interrupt is acknowledged by reading the status register, address 200H) or if the corresponding interrupt enable bit is disabled.

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> The DS1994 can produce two types of interrupts: spontaneous interrupts, called type 1, and delayed interrupts, type 2. Spontaneous interrupts need to be armed by a reset pulse after all communication on the 1-Wire bus has finished. A single falling slope on the 1-Wire bus disarms this type of interrupt. If an alarm condition occurs while the device is disarmed, at first a type 2 interrupt is produced.
>
> ...
>
> The interrupt signaling discussed so far is valid for the first opportunity the device has to signal an interrupt. It is not required for the master to acknowledge an interrupt immediately. **If an interrupt is not acknowledged, the DS1994 continues signaling the interrupt with every reset pulse.** To do so, the DS1994 either uses the waveform of the type 2 interrupt (Figure 14) or the waveform of the type 1A interrupt (Figure 13). The waveform of the type 2 interrupt is observed after a communication to a device other than the interrupting one; after successful communication to the interrupting device (without acknowledging the interrupt), the waveform of the type 1A interrupt is found.

(*Maxim DS 1994*, pp. 18-19) (Emphasis added) Similarly, the *Maxim DS 2044* data sheet indicates:

> **If the DS2404 detects an alarm condition, it will automatically set the corresponding alarm flag (CCF, ITF or RTF) in the Status Register.** If the flag's corresponding interrupt bit (RST , ITE or RTE) is enabled (logic 0) an interrupt condition begins as the alarm goes off. The DS2404 signals the interrupt condition by pulling the open drain IRQ output low. The interrupt condition ceases when the alarm flags are cleared (i.e., the interrupt is acknowledged by reading the Status Register, address 200H) or if the corresponding interrupt enable bit is disabled (set to logic 1).

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> **Interrupts can also be generated on the 1-Wire port.** Since communication and interrupt signaling share the same pin, one has to distinguish between two types of interrupts: spontaneous interrupts, called type 1, and delayed interrupts type 2. Spontaneous interrupts that have not yet occurred need to be (re-) armed by a reset pulse after all communication on the 1-Wire bus has finished. A single falling slope on the 1-Wire bus will disarm this type of interrupt. If an alarm condition occurs while the device is disarmed, at first a type 2 interrupt will be produced.
>
> ...
>
> The interrupt signaling discussed so far is valid for the first opportunity the device has to signal an interrupt. It is not required for the master to acknowledge an interrupt immediately. **If an interrupt is not acknowledged, the DS2404 will continue signaling the interrupt with every reset pulse.** To do so, DS2404 devices of Revision B4 (earlier production parts) will always use the waveform of the Type 2 Interrupt (Figure 14). Devices of Revision B5 (current production) will either use the waveform of the Type 2 Interrupt (Figure 14) or the waveform of the Type 1A Interrupt (Figure 13). The waveform of the Type 2 Interrupt will be observed after a communication to a device other than the interrupting one; after successful communication to the interrupting device (without acknowledging the interrupt) the waveform of the Type 1A Interrupt will be found. The revision code of the DS2404 is appended to the manufacturing date code, which is printed on the top of the package right below the part number.

(*Maxim DS 2044,* p. 19) (Emphasis added) The interrupt is thus an alarm condition that does not prevent continued operation of the master device, which may continue resets to the line.

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Thus, it is submitted that 1-Wire network devices are incapable of providing the elements of claim 1. Among other differences, the network will not operate for a first device and a second device arbitrating for control of a first control line, the first control bus being a bi-directional, single-line bus.

Further, even if the interrupt were otherwise relevant, it is clear from the description of the interrupts that there is no effort to determine whether the 1-Wire network is in use by a second device – the interrupt simply occurs because the alarm condition is present, and continues with every reset pulse until acknowledged.

For at least these reasons, *Maxim AN 244* does not anticipate the elements of independent claims 1, 11, and 19.

The remaining rejected claims, while having other differences with the cited reference, are dependent claims and are allowable as being dependent on the allowable base claims.

(2) Curry, et al.

The Office Action rejects claims 1, 3-5, 11, 13-15, 19, and 22-23 under 35 U.S.C. § 102(b) as allegedly being anticipated by U. S. Patent No. 6,112,275 to Curry, et al. (hereinafter referred to as "*Curry*").

Curry regards communicating information between a host device and a module device that measures thermal accumulation over time. As indicated, the host device communicates with the portable device via a single bidirectional wire, with the single wire bus and one-wire communication protocol allowing data flow between the host and a plurality of devices connected to the single wire bus.

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The Office Action cites to the following description of Figures 21 and 23A of the *Curry* reference for the elements of the claim with regard to operations relating to the control bus:

> The overall operation of embodiment 2100 follows a three layer hierarchical procedure: in the first layer **the host sends a reset command** by holding the IO node low for at least 480 microseconds and then returning IO to high for at least 480 microseconds. **This causes embodiment 2100 to generate a presence detect signal** by pulling node IO low for at least 60 microseconds as described below in connection with FIG. 22F. The reset command also clears the command register 2104 and **sets the module in a mode for the host to write a byte (8 bits) into command register** 2104 in the next eight write cycles as illustrated in FIGS. 2A-B and described below in connection with FIGS. 22B-E. Once command register 2104 is loaded with a command byte, command byte decoder 2106 decodes the command byte to initiate one of the four allowed commands: READ ROM DATA, MATCH ROM DATA, SEARCH ROM DATA, and SKIP ROM SECTION of the second layer. (If the byte in command byte decoder 2106 fails to match one of the available commands, then the module will simply wait for a reset and ignore further commands at its inputs.) These commands employ identification data from the ROM in 2108 and incorporate the security aspects of the module. The upper portion of FIG. 23A illustrates the flow. Then after successful execution of the second layer command, the third layer commands are available for access to the secure RAM 2110. The lower portion of FIG. 23A shows the execution of these third layer commands. Note that the flow paths all end in a reset. Also, the second layer commands dealing with the 64 bit ROM in 2108 may have simple hardware support in that the entire 64 bits are always read or compared, so the addressing can be a simple incrementing with the successive comparisons just fed to a latch that switches if a mismatch occurs. The

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following preferred embodiment discussions explain these commands and variations in detail.

(*Curry*, col. 37, lines 3-36) (Emphasis added) However, an analysis of these operations demonstrates that the relevant elements of the claims not provided by the reference. Figure 21 is indicated to be a top level schematic of chips 130 and 0130' in Figures 1A and 1B of the reference. (*Curry*, col. 36, lines 52-60) (Note: Figure 1A actually includes 1030 rather than 0130.) As the operation is described, the module simply responds to received directions from the host, and takes no action to arbitrate control of a bus or control line or to send commands via the bus or control line. As indicated in the quoted portion of *Curry*, the host sends a reset command, causing the 2100 module/chip to provide a presence detect signal and clear's the chip's command register 2104 and sets the module in a mode for the host to write into command register 2104 in the next eight write cycles. Figure 23A then illustrates the execution of third layer commands, which again are commands to the module.

Thus, what are illustrated in the reference are operations of the host and responses provided by the chip or module. The chip or module does not transmit any commands and does not take any action to arbitrate for control of the bus.

Further, claim 11 of *Curry* provides the following:

> 11. A method of transmitting information over a single wire data bus between a master device and a module device for measuring the accumulation of thermal energy over time, said single wire data bus comprising a single data conductor and a ground conductor, said method comprising the steps of:
>
> pulling said single wire data bus low for at least a predetermined amount of time by said master device in order to reset said module device;

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pulling said single wire data bus high by said master device and determining if said module device pulls said single wire data bus low thereby providing a presence detect signal to said master device, said presence detect signal indicates that said module device is in a listening mode;

providing a command word from said master device to said module by said master device; and

reading a chemical equivalent time count data from at least one register in a RAM in said module device, said chemical count data being generated by a temperature controlled counter circuit comprising a temperature sensitive band-gap circuit within said module, said temperature controlled counter being connected to said RAM.

(*Curry*, claim 11) Thus, the claim in *Curry* describes a process in which the master device resets the module device, the module device responds to indicate that the module device is in a listening mode, the master provides a command to the module device, and certain data is read from the module device. There again is no teaching or suggestion of the relevant elements of the claims.

As shown above with regard to *Maxim AN 244*, the 1-Wire protocol does teach or suggest the relevant elements of claims 1, 11, and 19. "The 1-Wire protocol defines the System as a single bus master system with single or multiple slaves. In all instances, the module 2300 is a slave. The bus master is typically a microcontroller." (*Curry*, col. 43, lines 22-25) The discussion regarding the 1-Wire protocol in the reference contains no teaching or suggestion regarding the arbitration of the 1-Wire bus by a module/slave device, or the transmission of commands on the 1-Wire bus by the module/slave device.

For at least these reasons, independent claims 1, 11, and 19 are not anticipated by *Curry*.

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The remaining rejected claims, while having other differences with the cited reference, are dependent claims and are allowable as being dependent on the allowable base claims.

(3) Kobayashi, et al.

The Office Action rejects claims 1-3, 10-13, 15, 19-21 and 23 under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent Application Publication No. 2004/0218599 of Kobayashi, et al. ("*Kobayashi*").

Kobayashi regards a packet-based video display interface to couple a multi-media source device to a multimedia sink device. The system includes auxiliary channel 224 as provided in, for example, Figures 2A, 2B, 5A, 5B, 12, and 15 of *Kobayashi*.

However, the auxiliary channel is not a single-wire control bus. This control appears to be formed in various manners, none of which would be a single-wire bus. In a first possible structure, the auxiliary channel appears to be a two wire (twisted pair) cable that is driven positively and negatively, as shown in Figure 15. "The positive and negative signals of auxiliary channel 224 are terminated to ground via 50-ohm termination resistors at each end of the link as shown." (*Kobayashi* , ¶0085)

In a second possible structure, *Kobayashi* indicates that the auxiliary channel may actually be part of the bandwidth of the main channel:

> [0068] The single bi-directional auxiliary channel 224 provides a conduit to for various support functions useful for link set up and supporting main link operations as well as to carry auxiliary application data such as USB traffic. For example, with the auxiliary channel 224, a display device can inform the source device of events such as sync loss, dropped packets and the results of training sessions (described below). For example, if a particular training session fails, the transmitter 102 adjusts

> the main link rate based upon pre-selected or determined results of the failed training session. In this way, the closed loop created by combining an adjustable, high speed main link with a relatively slow and very reliable auxiliary channel allows for robust operation over a variety of link conditions. **It should be noted that in some cases (an example of which is shown in FIG. 5B), a logical bi-directional auxiliary channel 520 can be established using a portion 522 of the bandwidth of the main link 222 to transfer data from the source device 202 to the sink device 204 and a unidirectional back channel 524 from the sink device 204 to the source device 202. In some applications, use of this logical bi-directional auxiliary channel may be more desirable than using a half-duplex bi-directional channel described in FIG. 5A**.

(*Kobayashi* ¶[0068) (Emphasis added)

In an third possible structure, the reference indicates that Further, claim 24 describes a auxiliary channel that appears to include two uni-directional channels, indicating "wherein the bi-directional auxiliary channel is formed of a uni-directional back channel configured to carry information from the sink device to the source device and a uni-directional forward channel included as part of the main channel for carrying information from the source device to the sink device in concert with the back channel." (*Kobayashi*, claim 24)

Thus, there are various possible structures for the auxiliary channel, but there does not appear to be any teaching or suggestion with regard to a bidirectional, single line bus. It is thus submitted that the *Kobayashi* reference does not provide for coupling a first device to a second device, coupling of the first and second devices including connecting a first control bus between the first device and the second device, the first control bus being a bi-directional, single-line bus.

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Further, there is no discussion regarding the arbitration of a bidirectional, single-line bus by a first device and a second device. There is discussion the transmission of signals on the auxiliary bus, but, in addition to the issue discussed above, there appears to be no discussion related to arbitration for control of a single wire bus. For example, "In the described embodiment, training related handshaking between the transmitter 102 and the receiver 104 is carried on the auxiliary channel." (*Kobayashi*, ¶0069) "For example, upon receiving a hot plug detect event generated upon monitor power-up or connection of the monitor cable from the source physical layer 1202, **the source device link layer 1204 evaluates the capabilities of the receiver via interchange over the auxiliary channel 224** to determine a maximum main link data rate as determined by a training session, the number of time-base recovery units on the receiver, available buffer size on both ends, availability of USB extensions and then notifies the stream source 1206 of an associated hot plug event. In addition, upon request from the stream source 1206, the source link layer 1204 reads the display capability (EDID or equivalent). During a normal operation, **the source link layer 1204 sends the stream attributes to the receiver 104 via the auxiliary channel 224**, notifies the stream source 1204 whether the main link 222 has enough resource for handling the requested data streams, notifies the stream source 1204 of link failure events such as sync loss and buffer overflow, and sends MCCS commands submitted by the stream source 1204 to the receiver via the auxiliary channel 224." (*Kobayashi* , ¶0078) (Emphasis added)

The operation of the auxiliary channel is further described as being implemented by the channel being driven to wake up a receiver, and then used to read the device. "If at the state 1806 a display hot unplug event is detected, then the system transitions back

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to the standby state 1804. **Otherwise the source drives the auxiliary channel with a positive and negative signal to wake up receiver and the receiver's subsequent response, if any, is checked.** If there is no response received, then the receiver has not woken up and source remains in the state 1806. If, however, a signal is received from the display, then the display has woken up and **the source is ready read the receiver link capabilities** (such as max link rate, buffer size, and number of time-base recovery units) and the system transitions to a main link initialization state 1808 and is ready to commence a training start notification phase." (*Kobayashi*, ¶0090)

Thus, it is submitted that the reference does not teach or suggest a bidirectional, single wire bus. Further, the reference does not teach or suggest arbitration of a bidirectional, single wire bus.

For at least these reasons, *Kobayashi* does not anticipate the elements of independent claims 1, 11, and 19.

The remaining rejected claims, while having other differences with the cited reference, are dependent claims and are allowable as being dependent on the allowable base claims.

Rejections under 35 U.S.C. § 103

(1) Kobayashi in view of Lindy

The Office Action rejects claims 6-9, 16-17, and 24-26 under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Kobayashi* in view of subject matter alleged to be knowledge commonly known in the art as evidenced by "Lindy announce Mini HDMI adapter for camcorders and notebooks", unknown source, HDTVUK.TV website (hereinafter referred to as "*Lindy*").

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The rejected claims, while having other differences with the cited combination of references *Kobayashi* and *Lindy*, are dependent claims and are allowable as being dependent on the allowable base claims.

Further, the Applicant respectfully traverses the rejection with regard to *Lindy*. It appears that the reference is describing a technology contained within the HDMI 1.3 specification, and thus does not support the Official Notice provided in the Office action.

With regard the Mini-HDMI connector, the cited HDMI 1.3 specification illustrates the connector type C, which utilizes the same 19-pin connection as standard HDMI. As indicated in the *Lindy* reference, the intended adaptor is an HDMI female to mini HDMI male adaptor that allows a standard HDMI cable with male plug to be connected to a device with a Mini-HDMI input, with the adapter itself being HDMI compliant.

Thus, the Mini-HDMI connector shown in *Lindy* does not illustrate a modified protocol. Rather, the reference illustrates an adapator for a smaller scale connector that is provided in the HDMI specification.

(2) Kobayashi in view of Self

The Office Action rejects claim 18 under 35 U.S.C. §103(a) as allegedly being unpatentable over *Kobayashi* as applied to claim 11 above and further in view of UK Patent Application No. 2 425 696, published November 1, 2006, of applicant Sybian Software Ltd, inventor Self (hereinafter referred to as "*Self*").

In addition to any other differences with the combination of the *Kobayashi* and *Self* references, the rejected claim is a dependent claim that is allowable as being dependent on the allowable base claim.

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Requirement for Information

In response to the requirement for information, the HDMI 1.3 Specification has been submitted in an information disclosure statement, submitted herewith.

Among other elements, the HDMI 1.3 Specification includes the following elements regarding connections for devices:

Section 4.1.2 – Connector pin assignment

Section 4.1.9.1 – Type A receptacle (HDMI 19-pin)

Section 4.1.9.2 – Type A plug (HDMI 19-pin)

Section 4.1.9.3 – Type B receptacle (HDMI 29-pin)

Section 4.1.9.2 – Type B plug (HDMI 29-pin)

Section 4.1.9.5 – Type C receptacle (Mini-HDMI 19-pin)

Section 4.1.9.6 – Type C plug (Mini-HDMI 19-pin)

Conclusion

Applicant respectfully submits that the rejections have been overcome by the amendment and remark, and that the claims as amended are now in condition for allowance. Accordingly, Applicant respectfully requests the rejections be withdrawn and the claims as amended be allowed.

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Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (503) 439-8778 if there remains any issue with allowance of the case.

Request for an Extension of Time if Needed

The Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. §1.136(a) should one be needed. Please charge any fee to our Deposit Account No. 02-2666.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

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LENOVO EXHIBIT 1002 - 188/502

Electronic Patent Application Fee Transmittal

Application Number:	11969852
Filing Date:	04-Jan-2008
Title of Invention:	CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Shrikant Ranade
Filer:	Mark C. Van Ness/Natasha French
Attorney Docket Number:	8029P038

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in excess of 20	1202	2	52	104
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**284**

Electronic Acknowledgement Receipt

EFS ID:	6716591
Application Number:	11969852
International Application Number:	
Confirmation Number:	1782
Title of Invention:	CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Shrikant Ranade
Correspondence Address:	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP - SEVENTH FLOOR 12400 WILSHIRE BOULEVARD LOS ANGELES CA 90025-1026 US 503 439 8778 -
Filer:	Mark C. Van Ness
Filer Authorized By:	
Attorney Docket Number:	8029P038
Receipt Date:	29-DEC-2009
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Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$284

RAM confirmation Number	6353
Deposit Account	022666
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	8029P038_IDS-e-file.pdf	34551 4519f83e8df4a111e288cd36ca2b0c67b65bc745	no	1
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Filed (SB/08)	8029P038_PTO1449.pdf	123867 44938c6f630b252c09c51770e1c2c8e1f903ac35	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	NPL Documents	HDMI_The_Digital_Display_Link.pdf	431045 6adea9ee2fdd975e817e3c7c95b75c00a3250153	no	21
Warnings:					
Information:					
4	NPL Documents	Maxim_DS_1994.pdf	643079 614dc6d65d000bd45c61f76d9d82772a23ffb07b	no	23
Warnings:					
Information:					
5	Applicant Arguments/Remarks Made in an Amendment	SIMG0335_8029P038_Resp_OA_25Dec2009.pdf	116212 3c49c14a4dedcb78b46c64bd4849b10dc68c23e2	no	29
Warnings:					
Information:					
6	NPL Documents	1-wire_Products_Design_Guide-e-file.pdf	3268008 c6f534ca530290909e7fabf16ceb197fedce7d78	no	8
Warnings:					
Information:					
7	NPL Documents	HDMI_Spec_1_3_GM1-1-e-file.pdf	18544387 19afc4cf2fda8753a5ae7da5511117f15cefa525	no	120
Warnings:					
Information:					

8	NPL Documents	HDMI_Spec_1_3_GM1-2-e-file.pdf	18592676 8ee667ce3dd46df64e2be900cf1cd8f37ea4f769	no	117
Warnings:					
Information:					
9	NPL Documents	Maxim_1_Wire_Extended_Network_Standard_e-file.pdf	4139506 8db3f3dc7ceae1c0e13648c16d0badc76c4c2565	no	5
Warnings:					
Information:					
10	NPL Documents	Maxim_Overview_of_1_Wire_Technology_1796-e-file.pdf	6689262 1a3be353926fa7cc8beb9281cbb6f52b91ea4d96	no	11
Warnings:					
Information:					
11	NPL Documents	Maxim_Choosing_the_Right_1_Wire_Master_AN_4206_e-file.pdf	2894292 c308e484deb1310ac11751e16828ce30078ea07d	no	10
Warnings:					
Information:					
12	NPL Documents	Maxim_DS_2404_e-file.pdf	3582243 4cb93b100f1d3230978535b8bdd3ec80b9938bb2	no	29
Warnings:					
Information:					
13	Fee Worksheet (PTO-875)	fee-info.pdf	32049 f9c5f949509e42e8c54f26c31d85e3e8f8defe9e	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	59091177	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	11/969,852
Filing Date	January 4, 2008
First Inventor	Shrikant Ranade, et al.
Art Unit	2111
Examiner Name	Thomas J. Cleary
Attorney Docket No.	8029P038 Conf. No. 1782

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of a final Office Action. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☒ The IDS Filing Fee in the amount of $180.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 02-2666.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Mark C. Van Ness/	Date (MM-DD-YYYY)	12-28-2009
Name/Print	Mark C. Van Ness	Registration Number	39,865

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

/Natasha French/

Natasha French *Date* *12-28-09*

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/969,852	01/04/2008	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **12/29/2009**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 28	Minus	** 26	= 2	X $ =		OR	X $52=	104
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE	**0**	OR	TOTAL ADD'L FEE	**104**

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/EAON SMALLWOOD/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 04/08/2010

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025-1026

EXAMINER	
CLEARY, THOMAS J	
ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 04/08/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/969,852	01/04/2008	Shrikant Ranade	8029P038	1782

TITLE OF INVENTION: CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	07/08/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

LENOVO EXHIBIT 1002 - 197/502

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 04/08/2010

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025-1026

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/969,852	01/04/2008	Shrikant Ranade	8029P038	1782

TITLE OF INVENTION: CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	07/08/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
CLEARY, THOMAS J	2111	710-106000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

LENOVO EXHIBIT 1002 - 198/502

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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/969,852	01/04/2008	Shrikant Ranade	8029P038	1782

7590 04/08/2010

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025-1026

EXAMINER	
CLEARY, THOMAS J	
ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 04/08/2010

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 201 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 201 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

LENOVO EXHIBIT 1002 - 199/502

Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	11/969,852	RANADE ET AL.	
	Examiner	Art Unit	
	THOMAS J. CLEARY	2111	

All Participants:

(1) *Thomas J. Cleary - USPTO*.

(2) *Mark Van Ness*.

Status of Application: *Pending*

(3) *Natasha French*.

(4) _____.

Date of Interview: *5 April 2010*

Time: _____

Type of Interview:
☒ Telephonic
☐ Video Conference
☐ Personal (Copy given to: ☐ Applicant ☐ Applicant's representative)

Exhibit Shown or Demonstrated: ☐ Yes ☒ No
If Yes, provide a brief description: .

Part I.

Rejection(s) discussed:
N/A

Claims discussed:
1 ,6, 8, 9, 11, 16, 19, 24, and 26

Prior art documents discussed:
N/A

Part II.

SUBSTANCE OF INTERVIEW DESCRIBING THE GENERAL NATURE OF WHAT WAS DISCUSSED:
Authorization for the attached Examiner's amendment was received.

Part III.

☒ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview directly resulted in the allowance of the application. The examiner will provide a written summary of the substance of the interview in the Notice of Allowability.
☐ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview did not result in resolution of all issues. A brief summary by the examiner appears in Part II above.

/Thomas J. Cleary/
Primary Examiner, Art Unit 2111

(Applicant/Applicant's Representative Signature – if appropriate)

Notice of Allowability	Application No.	Applicant(s)	
	11/969,852	RANADE ET AL.	
	Examiner	Art Unit	
	THOMAS J. CLEARY	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *29 December 2009*.

2. ☒ The allowed claim(s) is/are *1-5,7-9,11-14,17-22 and 25-31*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 20091229
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20100405* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Thomas J. Cleary/
Primary Examiner, Art Unit 2111

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Mark Van Ness and Natasha French on 5 April 2010.

3. The application has been amended as follows:

Claim 1:

- In Line 2, following the comma and prior to the word "coupling", insert "the first device being one of a transmitting or a receiving device and the second device being the other of a transmitting or a receiving device,".
- In Line 9, following the semicolon, delete the word "and".
- In Line 10, following the word "if", delete "the first device".
- In Line 19 (the last line), following the word "bus" and prior to the period, insert "; and wherein the receiving device is a device utilizing the standard protocol and the transmitting device is a mobile device utilizing a modified

protocol, the modified protocol being a modification of the standard protocol that is not included in the standard protocol".

Claim 6:

- Cancel Claim 6.

Claim 8:

- In Line 1, following the word "claim" replace "6" with "1" (change the dependency from claim 6 to claim 1).

Claim 9:

- In Line 1, following the word "claim" replace "6" with "1" (change the dependency from claim 6 to claim 1).

Claim 11:

- In Line 11, following the semicolon, delete the word "and".
- In Line 16 (the last line), following the word "bus" and prior to the period, insert "; and wherein the receiving device is a device utilizing the standard protocol and the transmitting device is a mobile device utilizing a modified protocol, the modified protocol being a modification of the standard protocol that is not included in the standard protocol".

Claim 16:

- Cancel Claim 16.

Claim 19:

- In Line 7, following the semicolon, delete the word “and”.
- In Line 13 (the last line), following the word “bus” and prior to the period, insert “; and wherein the receiving device is a device utilizing the standard protocol and the transmitting device is a mobile device utilizing a modified protocol, the modified protocol being a modification of the standard protocol that is not included in the standard protocol”.

Claim 24:

- Cancel Claim 24.

Claim 26:

- In Line 1, following the word “claim” replace “24” with “19” (change the dependency from claim 24 to claim 19).

4. The following is an examiner’s statement of reasons for allowance: The prior art fails to disclose, either alone, or in combination, the limitation of “wherein the receiving device is a device utilizing the standard protocol and the transmitting device is a mobile device utilizing a modified protocol, the modified protocol being a modification of the

standard protocol that is not included in the standard protocol", in the combinations as claimed. The closest prior art is US Patent Number 5,579,299 to Halter et al. ("Halter"). In reference to Claim 1, Halter discloses a method comprising: coupling a first device to a second device (See Figure 1 Numbers 16a-16e), coupling of the first and second devices including connecting a first control bus between the first device and the second device (See Figure 1 Number 12), the first control bus being a bi-directional, single-line bus (See Column 1 Lines 23-25 and Column 2 Lines 59-62); determining whether the first control bus is in use by the second device (See Column 1 Lines 16-22 and Column 6 Lines 59-60); if the first control bus is not in use by the second device, conducting arbitration for obtaining control of the first control (See Column 4 Lines 41-67); and if the first device obtains control of the first control bus through the arbitration for control of the first control bus, the first device becoming an initiator and the second device becoming a follower (See Column 5 Lines 1-12), then further comprising: converting one or more control signals for a standard protocol to one or more data packets, each of the one or more control signals representing one of a plurality of different types of control signals, each data packet including a plurality of bits to be transmitted; and transmitting the generated data packets from the first device to the second device via the first control bus (See Column 1 Line 57 – Column 2 Line 5). Halter discloses substantially equivalent limitations with respect to Claims 11 and 19. Halter does not disclose that the receiving device is a device utilizing the standard protocol and the transmitting device is a mobile device utilizing a modified protocol, the modified protocol being a modification of the standard protocol that is not included in the standard protocol.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to THOMAS J. CLEARY whose telephone number is (571)272-3624. The examiner can normally be reached on Monday-Thursday (7-3).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thomas J. Cleary/
Primary Examiner, Art Unit 2111

Notice of References Cited	Application/Control No. 11/969,852	Applicant(s)/Patent Under Reexamination RANADE ET AL.	
	Examiner THOMAS J. CLEARY	Art Unit 2111	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,579,299	11-1996	Halter et al.	370/212
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11969852	RANADE ET AL.
	Examiner	Art Unit
	THOMAS J CLEARY	2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/23/2009	04/05/2010							
1	1	✓	=							
2	2	✓	=							
3	3	✓	=							
4	4	✓	=							
5	5	✓	=							
	6	✓	-							
6	7	✓	=							
7	8	✓	=							
8	9	✓	=							
	10	✓	-							
12	11	✓	=							
13	12	✓	=							
14	13	✓	=							
15	14	✓	=							
	15	✓	-							
	16	✓	-							
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21	21	✓	=							
22	22	✓	=							
	23	✓	-							
	24	✓	-							
23	25	✓	=							
24	26	✓	=							
9	27		=							
10	28		=							
11	29		=							
18	30		=							
25	31		=							

LENOVO EXHIBIT 1002 - 209/502

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	11/969,852	RANADE ET AL.	
	Examiner	Art Unit	
	THOMAS J. CLEARY	2111	

SEARCHED			
Class	Subclass	Date	Examiner

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
710	**105-107**	4/5/2010	**TJC**
710	119	4/5/2010	TJC

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
Attached EAST BRS	4/5/2010	TJC
Updated Previous Search	4/5/2010	TJC
Google Search	4/5/2010	TJC
Inventor Search	4/5/2010	TJC

Issue Classification

Application/Control No.	Applicant(s)/Patent Under Reexamination
11969852	RANADE ET AL.
Examiner	**Art Unit**
THOMAS J CLEARY	2111

ORIGINAL	
CLASS	SUBCLASS
710	106

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
710	105	107	119		

INTERNATIONAL CLASSIFICATION

CLAIMED	NON-CLAIMED
G 06F 13 / 42 (2006.01.01)	
G 06F 13 / 00 (2006.01.01)	
G 06F 13 / 368 (2006.01.01)	

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	16	17												
2	2	17	18												
3	3	19	19												
4	4	20	20												
5	5	21	21												
	6	22	22												
6	7		23												
7	8		24												
8	9	23	25												
	10	24	26												
12	11	9	27												
13	12	10	28												
14	13	11	29												
15	14	18	30												
	15	25	31												
	16														

NONE

(Assistant Examiner) (Date)

Total Claims Allowed: 25

/THOMAS J CLEARY/
Primary Examiner.Art Unit 2111 4/5/2010

(Primary Examiner) (Date)

O.G. Print Claim(s)	O.G. Print Figure
1	2

LENOVO EXHIBIT 1002 - 211/502

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BIB DATA SHEET

CONFIRMATION NO. 1782

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/969,852	01/04/2008	710	2111	8029P038

APPLICANTS

Shrikant Ranade, Campbell, CA;
Alexander Peysakhovich, San Jose, CA;
Hyuck Jae Lee, San Francisco, CA;
Hoon Choi, Mountain View, CA;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
01/23/2008

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /THOMAS J CLEARY/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	9	26	3

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UNITED STATES

TITLE

CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES

FILING FEE RECEIVED		
1564	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4	ranade-shrik$.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 15:08
L2	270	(ranade-shrik$.in. peysakhovich-alex$.in. lee-hyuck$.in. choi-hoon$.in.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 15:09
L3	2	"5391922".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L4	2	kohlman-k$.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L5	16	kohlmann-k$.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L6	18	L4 L5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L7	5	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express) same board same connectors) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L8	2	((pcix pci-x "pci x" "pci extended" pci-extended).ti. and (pcie pci-e "pci e" "pci express" pci-express).ti.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44

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L9	1	((pci?x/pci?e).ti.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L10	0	((pcix/pcie).ti.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L11	0	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express) same "first connector" same "second connector") and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L12	420	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L13	10	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express) and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L14	9	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express) and multiple with connectors) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L15	118	(enable with connector with resistor) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L16	0	((unused adj (port connector interface)) with ("not connected")) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L17	1329	((unused adj (port connector interface))) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44

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L18	6	((unused adj (port connector interface)) same disconnected) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L19	0	((unused adj (port connector interface)) same ("not connected")) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L20	0	((unused adj (component)) same "not connected") and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L21	13	((unused adj (component)) with connect $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L22	13	((unused adj (component)) with $3connect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L23	0	((unused adj (component)) same (remov$3 with resistor)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L24	1	((unused adj (component device connector interface port)) same (remov$3 with resistor)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L25	1468	((disabl$3 with (component connector device module unit interface port)) with disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L26	18	((disabl$3 with (component connector device module unit interface port)) with resistor with disconnect $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44

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L27	460	((disabl$3 near2 (component connector device module unit interface port)) with disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L28	189	((disabl$3 near (component connector device module unit interface port)) with disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L29	29	((disabl$3 near (connector interface port)) with disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L30	64	((disabl$3 near (connector interface port)) same disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L31	4	((disabl$3 near (component connector device module unit interface port)) with resistor with disconnect $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L32	5	((disabl$3 near (component connector device module unit interface port)) same resistor with disconnect $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L33	1	(((disabl$3 enabl$3) near (connector interface port)) same jumper with resistor) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L34	2	(((disabl$3 enabl$3) near (component connector device module unit interface port)) same jumper with resistor) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L35	134	(((disabl$3 enabl$3) near (component connector device module unit interface port)) same jumper) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44

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L36	56	(((disabl$3 enabl$3) near (connector interface port)) same jumper) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L37	35	(RAID same (card board) same SATA) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L38	77	((nic "network interface card") same "ethernet connector") and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L39	588	(710/300.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L40	800	(710/301.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L41	584	(710/302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L42	2071	(710/305.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L43	493	(710/2.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L44	1750	(710/8.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L45	961	(710/10.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44

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L46	434	(710/11.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L47	1138	(361/748.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L48	683	(361/785.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L49	419	(361/788.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L50	1278	(710/62.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L51	45	("dual sided" with pcb) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L52	163	(enabl$3 with resistor same (pcb "printed circuit board")) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L53	7	(disabl$3 with resistor same (pcb "printed circuit board")) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L54	239	(disabl$3 with resistor same (interface port)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L55	1278	(710/62.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44

LENOVO EXHIBIT 1002 - 218/502

L56	434	(710/11.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L57	961	(710/10.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L58	584	(710/302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L59	588	(710/300.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L60	1750	(710/8.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L61	493	(710/2.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L62	2071	(710/305.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L63	419	(361/788.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L64	1138	(361/748.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L65	683	(361/785.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44

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L66	800	(710/301.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L67	339	(("printed circuit board" pcb "circuit board" card) same jumper same enabl $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L68	162	(("printed circuit board" pcb "circuit board" card) same jumper with enabl $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L69	18	("4803485" | "5297141" | "5299195" | "5311114" | "Re33521").PN. OR ("5444856").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/05 16:44
L70	10	("4883430" | "5169337" | "5711681").PN. OR ("5810617").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/05 16:44
L71	4	("4795602" | "5882224" | "6036534").PN. OR ("6512664").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/05 16:44
L72	10	((multi-interface multiinterface ((multi multiple) adj interface) multiple-interface) and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L73	7	("20030065867" | "20040059860" | "5920731" | "6438638" | "6658516" | "6807597"). PN. OR ("7152127"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/05 16:44
L74	45	("4972470" | "5119498" | "5371892" | "5430617" | "5451933" | "5514951" | "5572409" | "5589719" | "5598318" | "5706239" | "5793989" | "5805473" | "5819107").PN. OR ("5920731").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/05 16:44
L75	14	(713/324.ccls. and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44

LENOVO EXHIBIT 1002 - 220/502

L76	43	("4716526" | "4794523" | "4999787" | "5297272" | "5310998" | "5355489" | "5410726" | "5490279" | "5515514" | "5530620" | "5530882" | "5537558" | "5551012" | "5555510" | "5579487" | "5581712" | "5586270" | "5600801" | "5644760" | "5664118" | "5678011" | "5758103" | "5805903").PN. OR ("6003100").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/05 16:44
L77	0	(713/11,14.ccls. and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L78	0	((713/11.ccls. or 710/14. ccls) and (710/301.ccls. or 710/302.ccls.)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L79	14	((710/11.ccls. or 710/14. ccls) and (710/301.ccls. or 710/302.ccls.)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L80	31	(710/11,14.ccls. and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L81	13	((multi-connector multiconnector ((multi multiple) adj connector) multiple-connector) and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L82	116	(361/785-791.ccls. and multiple near2 (connector interface)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L83	9	(361/785-791.ccls. and dual adj2 (connector interface)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44

LENOVO EXHIBIT 1002 - 221/502

L84	8	((dual adj (interface connector)) and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L85	2	"5391922".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L86	2	kohlman-k$.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L87	16	kohlmann-k$.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L88	18	L86 L87	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L89	5	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express) same board same connectors) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L90	2	((pcix pci-x "pci x" "pci extended" pci-extended). ti. and (pcie pci-e "pci e" "pci express" pci-express). ti.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L91	1	((pci?x/pci?e).ti.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L92	0	((pcix/pcie).ti.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44

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L93	0	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express) same "first connector" same "second connector") and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L94	420	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L95	10	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express) and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L96	9	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express) and multiple with connectors) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L97	118	(enable with connector with resistor) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L98	0	((unused adj (port connector interface)) with ("not connected")) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L99	1329	((unused adj (port connector interface))) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L100	6	((unused adj (port connector interface)) same disconnected) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L101	0	((unused adj (port connector interface)) same ("not connected")) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44

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L102	0	((unused adj (component)) same "not connected") and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L103	13	((unused adj (component)) with connect $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L104	13	((unused adj (component)) with $3connect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L105	0	((unused adj (component)) same (remov$3 with resistor)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L106	1	((unused adj (component device connector interface port)) same (remov$3 with resistor)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L107	1468	((disabl$3 with (component connector device module unit interface port)) with disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L108	18	((disabl$3 with (component connector device module unit interface port)) with resistor with disconnect $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L109	460	((disabl$3 near2 (component connector device module unit interface port)) with disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L110	189	((disabl$3 near (component connector device module unit interface port)) with disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44

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L111	29	((disabl$3 near (connector interface port)) with disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L112	64	((disabl$3 near (connector interface port)) same disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L113	4	((disabl$3 near (component connector device module unit interface port)) with resistor with disconnect $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L114	5	((disabl$3 near (component connector device module unit interface port)) same resistor with disconnect $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L115	1	(((disabl$3 enabl$3) near (connector interface port)) same jumper with resistor) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L116	2	(((disabl$3 enabl$3) near (component connector device module unit interface port)) same jumper with resistor) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L117	134	(((disabl$3 enabl$3) near (component connector device module unit interface port)) same jumper) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L118	56	(((disabl$3 enabl$3) near (connector interface port)) same jumper) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L119	35	(RAID same (card board) same SATA) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44

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L120	77	((nic "network interface card") same "ethernet connector") and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L121	588	(710/300.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L122	800	(710/301.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L123	584	(710/302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L124	2071	(710/305.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L125	493	(710/2.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L126	1750	(710/8.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L127	961	(710/10.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L128	434	(710/11.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L129	1138	(361/748.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44

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L130	683	(361/785.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L131	419	(361/788.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L132	1278	(710/62.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L133	45	("dual sided" with pcb) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L134	163	(enabl$3 with resistor same (pcb "printed circuit board")) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L135	7	(disabl$3 with resistor same (pcb "printed circuit board")) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L136	239	(disabl$3 with resistor same (interface port)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L137	1278	(710/62.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L138	434	(710/11.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L139	961	(710/10.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44

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L140	584	(710/302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L141	588	(710/300.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L142	1750	(710/8.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L143	493	(710/2.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L144	2071	(710/305.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L145	419	(361/788.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L146	1138	(361/748.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L147	683	(361/785.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L148	800	(710/301.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L149	339	(("printed circuit board" pcb "circuit board" card) same jumper same enabl $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44

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L150	162	(("printed circuit board" pcb "circuit board" card) same jumper with enabl $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L151	18	("4803485" | "5297141" | "5299195" | "5311114" | "Re33521").PN. OR ("5444856").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/05 16:44
L152	10	("4883430" | "5169337" | "5711681").PN. OR ("5810617").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/05 16:44
L153	4	("4795602" | "5882224" | "6036534").PN. OR ("6512664").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/05 16:44
L154	10	((multi-interface multiinterface ((multi multiple) adj interface) multiple-interface) and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L155	7	("20030065867" | "20040059860" | "5920731" | "6438638" | "6658516" | "6807597"). PN. OR ("7152127"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/05 16:44
L156	45	("4972470" | "5119498" | "5371892" | "5430617" | "5451933" | "5514951" | "5572409" | "5589719" | "5598318" | "5706239" | "5793989" | "5805473" | "5819107").PN. OR ("5920731").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/05 16:44
L157	14	(713/324.ccls. and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L158	43	("4716526" | "4794523" | "4999787" | "5297272" | "5310998" | "5355489" | "5410726" | "5490279" | "5515514" | "5530620" | "5530882" | "5537558" | "5551012" | "5555510" | "5579487" | "5581712" | "5586270" | "5600801" | "5644760" | "5664118" | "5678011" | "5758103" | "5805903").PN. OR ("6003100").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/05 16:44

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L159	0	(713/11,14.ccls. and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L160	0	((713/11.ccls. or 710/14. ccls) and (710/301.ccls. or 710/302.ccls.)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:44
L161	14	((710/11.ccls. or 710/14. ccls) and (710/301.ccls. or 710/302.ccls.)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:45
L162	31	(710/11,14.ccls. and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:45
L163	13	((multi-connector multiconnector ((multi multiple) adj connector) multiple-connector) and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:45
L164	116	(361/785-791.ccls. and multiple near2 (connector interface)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:45
L165	9	(361/785-791.ccls. and dual adj2 (connector interface)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:45
L166	8	((dual adj (interface connector)) and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 16:45
S1	2	"5391922".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 14:54
S2	2	kohlman-k$.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 07:32

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S3	16	kohlmann-k$.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 09:04
S4	18	S2 S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 07:32
S5	4	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express) same board same connectors) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/21 07:14
S6	2	((pcix pci-x "pci x" "pci extended" pci-extended). ti. and (pcie pci-e "pci e" "pci express" pci-express). ti.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 09:17
S7	1	((pci?x/pci?e).ti.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 09:21
S8	0	((pcix/pcie).ti.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 09:21
S9	0	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express) same "first connector" same "second connector") and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 09:22
S10	299	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 09:23
S11	3	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express) and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 09:23

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S12	7	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express) and multiple with connectors) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 09:51
S13	113	(enable with connector with resistor) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:03
S14	0	((unused adj (port connector interface)) with ("not connected")) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:04
S15	1186	((unused adj (port connector interface))) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:04
S16	5	((unused adj (port connector interface)) same disconnected) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:07
S17	0	((unused adj (port connector interface)) same ("not connected")) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:04
S18	0	((unused adj (component)) same "not connected") and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:07
S19	12	((unused adj (component)) with connect $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:09
S20	12	((unused adj (component)) with $3connect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:10
S21	0	((unused adj (component)) same (remov$3 with resistor)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:10

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S22	1	((unused adj (component device connector interface port)) same (remov$3 with resistor)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:18
S23	1356	((disabl$3 with (component connector device module unit interface port)) with disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:26
S24	18	((disabl$3 with (component connector device module unit interface port)) with resistor with disconnect $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:19
S25	425	((disabl$3 near2 (component connector device module unit interface port)) with disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:27
S26	174	((disabl$3 near (component connector device module unit interface port)) with disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:41
S27	27	((disabl$3 near (connector interface port)) with disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:28
S28	50	((disabl$3 near (connector interface port)) same disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:28
S29	4	((disabl$3 near (component connector device module unit interface port)) with resistor with disconnect $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:41
S30	5	((disabl$3 near (component connector device module unit interface port)) same resistor with disconnect $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:42

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S31	1	(((disabl$3 enabl$3) near (connector interface port)) same jumper with resistor) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:43
S32	2	(((disabl$3 enabl$3) near (component connector device module unit interface port)) same jumper with resistor) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:46
S33	130	(((disabl$3 enabl$3) near (component connector device module unit interface port)) same jumper) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 10:47
S34	56	(((disabl$3 enabl$3) near (connector interface port)) same jumper) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 12:54
S35	29	(RAID same (card board) same SATA) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 13:48
S36	76	((nic "network interface card") same "ethernet connector") and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/20 13:49
S37	495	(710/300.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/21 07:15
S38	696	(710/301.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/21 07:15
S39	503	(710/302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/21 07:15
S40	1824	(710/305.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/21 07:25

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S41	434	(710/2.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/21 07:25
S42	1436	(710/8.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/21 07:26
S43	796	(710/10.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/21 07:26
S44	356	(710/11.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/21 07:31
S45	1081	(361/748.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/21 07:31
S46	651	(361/785.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/21 07:31
S47	378	(361/788.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/21 07:31
S48	1052	(710/62.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/21 07:31
S49	42	("dual sided" with pcb) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/24 07:48
S50	159	(enabl$3 with resistor same (pcb "printed circuit board")) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/24 09:32

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S51	6	(disabl$3 with resistor same (pcb "printed circuit board")) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/24 09:34
S52	229	(disabl$3 with resistor same (interface port)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/24 09:34
S53	1121	(710/62.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/24 10:35
S54	375	(710/11.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/24 10:35
S55	840	(710/10.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/24 10:35
S56	539	(710/302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/24 10:35
S57	536	(710/300.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/24 10:35
S58	1525	(710/8.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/24 10:35
S59	456	(710/2.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/24 10:35
S60	1927	(710/305.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/24 10:35

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S61	389	(361/788.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/24 10:35
S62	1096	(361/748.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/24 10:35
S63	661	(361/785.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/24 10:35
S64	738	(710/301.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/24 10:35
S65	330	(("printed circuit board" pcb "circuit board" card) same jumper same enabl $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/10 14:08
S66	157	(("printed circuit board" pcb "circuit board" card) same jumper with enabl $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/10 14:08
S67	17	("4803485" | "5297141" | "5299195" | "5311114" | "Re33521").PN. OR ("5444856").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/10 14:18
S68	8	("4883430" | "5169337" | "5711681").PN. OR ("5810617").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/10 14:21
S69	4	("4795602" | "5882224" | "6036534").PN. OR ("6512664").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/10 14:41
S70	9	((multi-interface multiinterface ((multi multiple) adj interface) multiple-interface) and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/16 11:07
S71	6	("20030065867" | "20040059860" | "5920731" | "6438638" | "6658516" | "6807597").PN. OR ("7152127").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/16 11:12

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S72	41	("4972470" | "5119498" | "5371892" | "5430617" | "5451933" | "5514951" | "5572409" | "5589719" | "5598318" | "5706239" | "5793989" | "5805473" | "5819107").PN. OR ("5920731").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/16 11:15
S73	14	(713/324.ccls. and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/16 11:48
S74	41	("4716526" | "4794523" | "4999787" | "5297272" | "5310998" | "5355489" | "5410726" | "5490279" | "5515514" | "5530620" | "5530882" | "5537558" | "5551012" | "5555510" | "5579487" | "5581712" | "5586270" | "5600801" | "5644760" | "5664118" | "5678011" | "5758103" | "5805903").PN. OR ("6003100").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/16 12:00
S75	0	(713/11,14.ccls. and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/16 12:06
S76	0	((713/11.ccls. or 710/14. ccls) and (710/301.ccls. or 710/302.ccls.)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/16 12:06
S77	13	((710/11.ccls. or 710/14. ccls) and (710/301.ccls. or 710/302.ccls.)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/16 12:07
S78	29	(710/11,14.ccls. and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/16 12:07
S79	13	((multi-connector multiconnector ((multi multiple) adj connector) multiple-connector) and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/16 12:11

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S80	112	(361/785-791.ccls. and multiple near2 (connector interface)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/16 14:08
S81	9	(361/785-791.ccls. and dual adj2 (connector interface)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/16 14:14
S82	7	((dual adj (interface connector)) and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/16 14:17
S83	2	"5391922".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S84	2	kohlman-k$.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S85	16	kohlmann-k$.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S86	18	S84 S85	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S87	5	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express) same board same connectors) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S88	2	((pcix pci-x "pci x" "pci extended" pci-extended). ti. and (pcie pci-e "pci e" "pci express" pci-express). ti.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S89	1	((pci?x/pci?e).ti.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14

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S90	0	((pcix/pcie).ti.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S91	0	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express) same "first connector" same "second connector") and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S92	366	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S93	9	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express) and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S94	7	((pcix pci-x "pci x" "pci extended" pci-extended) same (pcie pci-e "pci e" "pci express" pci-express) and multiple with connectors) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S95	117	(enable with connector with resistor) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S96	0	((unused adj (port connector interface)) with ("not connected")) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S97	1270	((unused adj (port connector interface))) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S98	6	((unused adj (port connector interface)) same disconnected) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14

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S99	0	((unused adj (port connector interface)) same ("not connected")) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S100	0	((unused adj (component)) same "not connected") and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S101	13	((unused adj (component)) with connect $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S102	13	((unused adj (component)) with $3connect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S103	0	((unused adj (component)) same (remov$3 with resistor)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S104	1	((unused adj (component device connector interface port)) same (remov$3 with resistor)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S105	1422	((disabl$3 with (component connector device module unit interface port)) with disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S106	18	((disabl$3 with (component connector device module unit interface port)) with resistor with disconnect $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S107	446	((disabl$3 near2 (component connector device module unit interface port)) with disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14

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S108	184	((disabl$3 near (component connector device module unit interface port)) with disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S109	28	((disabl$3 near (connector interface port)) with disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S110	60	((disabl$3 near (connector interface port)) same disconnect$3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S111	4	((disabl$3 near (component connector device module unit interface port)) with resistor with disconnect $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S112	5	((disabl$3 near (component connector device module unit interface port)) same resistor with disconnect $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S113	1	(((disabl$3 enabl$3) near (connector interface port)) same jumper with resistor) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S114	2	(((disabl$3 enabl$3) near (component connector device module unit interface port)) same jumper with resistor) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S115	134	(((disabl$3 enabl$3) near (component connector device module unit interface port)) same jumper) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S116	56	(((disabl$3 enabl$3) near (connector interface port)) same jumper) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14

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S117	34	(RAID same (card board) same SATA) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S118	77	((nic "network interface card") same "ethernet connector") and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S119	566	(710/300.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S120	772	(710/301.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S121	563	(710/302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S122	2017	(710/305.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S123	481	(710/2.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S124	1636	(710/8.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S125	896	(710/10.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S126	404	(710/11.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14

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S127	1120	(361/748.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S128	673	(361/785.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S129	410	(361/788.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S130	1203	(710/62.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S131	43	("dual sided" with pcb) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S132	161	(enabl$3 with resistor same (pcb "printed circuit board")) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S133	6	(disabl$3 with resistor same (pcb "printed circuit board")) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S134	235	(disabl$3 with resistor same (interface port)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S135	1203	(710/62.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S136	404	(710/11.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14

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S137	896	(710/10.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S138	563	(710/302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S139	566	(710/300.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S140	1636	(710/8.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S141	481	(710/2.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S142	2017	(710/305.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S143	410	(361/788.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S144	1120	(361/748.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S145	673	(361/785.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S146	772	(710/301.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14

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S147	334	(("printed circuit board" pcb "circuit board" card) same jumper same enabl $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S148	159	(("printed circuit board" pcb "circuit board" card) same jumper with enabl $3) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S149	17	("4803485" | "5297141" | "5299195" | "5311114" | "Re33521").PN. OR ("5444856").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/17 15:14
S150	9	("4883430" | "5169337" | "5711681").PN. OR ("5810617").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/17 15:14
S151	4	("4795602" | "5882224" | "6036534").PN. OR ("6512664").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/17 15:14
S152	9	((multi-interface multiinterface ((multi multiple) adj interface) multiple-interface) and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S153	6	("20030065867" | "20040059860" | "5920731" | "6438638" | "6658516" | "6807597"). PN. OR ("7152127"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/17 15:14
S154	41	("4972470" | "5119498" | "5371892" | "5430617" | "5451933" | "5514951" | "5572409" | "5589719" | "5598318" | "5706239" | "5793989" | "5805473" | "5819107").PN. OR ("5920731").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/17 15:14
S155	14	(713/324.ccls. and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14

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S156	41	("4716526" | "4794523" | "4999787" | "5297272" | "5310998" | "5355489" | "5410726" | "5490279" | "5515514" | "5530620" | "5530882" | "5537558" | "5551012" | "5555510" | "5579487" | "5581712" | "5586270" | "5600801" | "5644760" | "5664118" | "5678011" | "5758103" | "5805903").PN. OR ("6003100").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/07/17 15:14
S157	0	(713/11,14.ccls. and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S158	0	((713/11.ccls. or 710/14. ccls) and (710/301.ccls. or 710/302.ccls.)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S159	13	((710/11.ccls. or 710/14. ccls) and (710/301.ccls. or 710/302.ccls.)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S160	29	(710/11,14.ccls. and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S161	13	((multi-connector multiconnector ((multi multiple) adj connector) multiple-connector) and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S162	112	(361/785-791.ccls. and multiple near2 (connector interface)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14
S163	9	(361/785-791.ccls. and dual adj2 (connector interface)) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14

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S164	7	((dual adj (interface connector)) and 710/301,302.ccls.) and @ad<"20050121"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/17 15:14

EAST Search History (Interference)

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4/5/10 4:51:04 PM
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LENOVO EXHIBIT 1002 - 248/502

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	11/969,852
	Filing Date	January 4, 2008
	First Named Inventor	Ranade, Shrikant
	Group Art Unit	2111
	Examiner Name	Unknown
Sheet 1 of 1	Attorney Docket No: 8029P038	

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	**Cite No [1]**	**Foreign Patent Document** Country Code/Number/Kind Code (if known)	**Publication Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	**T [2]**

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T [2]**
		MAXIM, *1-Wire Products Design Guide*, 4th Edition, pp 1-8, Feb. 2009. www.maxim-ic.com/yes	
		O'DONNELL, B., *White Paper HDMI™: The Digital Display Link*, IDC Analyze the Future, pp. 1-21, Dec. 2006, Framingham, MA.	
		Hitachi, Ltd. et al., *High-Definition Multimedia Interface: Specification Version 1.3*, pp. 1-231, June 22, 2006.	
		MAXIM, *1-Wire® Extended Network Standard*, pp 1-5, October 26, 2006. www.maxim-ic.com/an3925	
		MAXIM, *Choosing the Right 1-Wire® Master for Embedded Applications*, pp 1-10, May 27, 2008. www.maxim-ic.com/an4206	
		MAXIM, *Overview of 1-Wire® Technology and Its Use*, pp 1-11, June 19, 2008. www.maxim-ic.com/an1796	
		MAXIM, *DS 1994 4Kb Plus Time Memory iButton®*, pp 1-23, Nov. 2009. www.maxim-ic.com	
		MAXIM, *DS 2404 EconoRAM Time Chip,* pp 1-29, January 22, 2007. www.maxim-ic.com	

EXAMINER /Thomas J. Cleary/ **DATE CONSIDERED** 04/05/2010

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /TJC/

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. 1450
Alexandria, VA 22313-1450

Application No.	11/969,852
Filing Date	January 4, 2008
First Named Inventor	Shrikant Ranade
Art Unit	2111
Examiner Name	Thomas J. Cleary
Attorney Docket Number	8029P038
Confirmation Number	1782

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR § 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application.

1. **Submission required under 37 CFR 1.114** Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. ☒ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

      i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on ____

      ii. ☐ Other _____

   b. ☒ Enclosed

      i. ☒ Amendment/Reply

      ii. ☐ Affidavit(s)/Declaration(s)

      iii. ☒ Information Disclosure Statement (IDS)

      iv. ☐ Other _____

2. **Miscellaneous**

   a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

   b. ☐ Other _____

3. **Fees** The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

   a. ☒ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. 02-2666.

      i. ☒ RCE fee required under 37 CFR 1.17(e)

      ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)

      iii. ☐ Other: ($.00) _____

   b. ☐ Check in the amount of $810.00 enclosed

   c. ☐ Payment by credit card (Form PTO-2038 enclosed)

   WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	/Mark C. Van Ness/	Date	July 8, 2010
Name *(Print/Type)*	Mark C. Van Ness, 39,865	*Registration No. (Attorney/Agent)*	39,865

CERTIFICATE OF MAILING OR TRANSMISSION

This Request for Continued Examination is being submitted electronically to the United States Patent and Trademark Office via EFS-Web on **July 8, 2010**

Name *(Print/Type)*	**Lisa Riley**		
Signature	/Lisa Riley/	Date	**July 8, 2010**

Based on PTO/SB/30 (04-05) as modified by Blakely, Solokoff, Taylor & Zafman (wlr) 06/15/2007.
SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Our Docket No: 8029P038

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Shrikant Ranade et al.	Examiner: Thomas J. Cleary
Application No: 11/969,852	Art Unit: 2111
Filed: January 4, 2008	Conf. No: 1782
For: CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES	

AMENDMENT ACCOMPANYING A REQUEST FOR CONTINUED EXAMINATION

Sir or Madam:

The Applicant respectfully requests the Examiner to enter the following amendment and to consider the following remark.

CERTIFICATE OF MAILING/TRANSMISSION
I hereby certify that this correspondence is being submitted electronically via EFS Web prior to 11:59 PM on the date shown below.

/Lisa Riley/ July 8, 2010
Lisa Riley Date

LENOVO EXHIBIT 1002 - 251/502

AMENDMENTS TO THE CLAIMS

Please cancel claims 6, 16, and 24 without prejudice.

Please amend the claims as follows:

1. (Currently amended) A method comprising:

coupling a first device to a second device, the first device being one of a transmitting device or a receiving device and the second device being the other of a transmitting device or a receiving device, coupling of the first and second devices including connecting a first control bus between the first device and the second device, the first control bus being a bi-directional, single-line bus;

determining whether the first control bus is in use by the second device;

if the first control bus is not in use by the second device, conducting arbitration for control of the first control bus; and

if the first device ~~the first device~~ obtains control of the first control bus through the arbitration for control of the first control bus, the first device becoming an initiator and the second device becoming a follower, then further comprising:

converting one or more control signals for a standard protocol to one or more data packets, each of the one or more control signals representing one of a plurality of different types of control signals, each data packet including a plurality of bits to be transmitted; and

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transmitting the generated data packets from the first device to the second device via the first control bus, and wherein the receiving device is a device utilizing the standard protocol and the transmitting device is a mobile device utilizing a modified protocol, the modified protocol being a modification of the standard protocol that is not included in the standard protocol.

2. (Previously presented) The method of claim 1, wherein the signaling for transmitting the one or more generated data packets on the first control bus utilizes bi-phase mark encoding.

3. (Previously presented) The method of claim 1, wherein if the second device obtains control of the first control bus, the second device becoming the initiator and the first device becoming the follower, then further comprising:
receiving at the first device the plurality of data packets transmitted from the second device.

4. (Currently amended) The method of claim 1, wherein, if the first device is a transmitting device for transmission of data to the second device, then arbitrating for control of the first control bus includes:
determining the first control bus is idle or unused for a first time period;
if the first control bus is idle or unused for the first time period, then sending a low signal for a first number of cycles; and
after the conclusion of the first number of cycles, then taking ~~control~~ control of the first control bus.

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5. (Currently amended) The method of ~~claim 4~~ claim 1, wherein, if the first device is a receiving device for reception of data from the second device, then arbitrating for control of the first control bus includes:

determining the first control bus is idle or unused for a ~~second~~ first time period;

if the first control bus is idle or unused for the ~~second~~ first time period, then

sending a low signal followed by a high signal for a ~~second~~ first number of cycles;

during the ~~second~~ first number of cycles, checking a status of the first control bus;

if the status of the first control bus is a high signal, taking control of the first control bus.

6. (Canceled)

7. (Previously presented) The method of claim 1, wherein the standard protocol is HDMI (High-Definition Multimedia Interface).

8. (Currently amended) The method of ~~claim 6~~ claim 1, wherein the receiving device is a dual-mode device that is capable of communicating with a device that is compatible with the standard protocol or a device that is compatible with the modified protocol.

9. (Currently amended) The method of ~~claim 6~~ claim 1, wherein standard protocol requires that the plurality of different types of control signals be transmitted over a plurality of different control buses.

10. (Canceled)

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11. (Currently amended) A transmitting device comprising:

a connection to a single first control bus, the first control bus being a bi-directional, single-line bus, wherein the transmitting device is operable for coupling with a receiving device via the first control bus;

logic to convert each of one or more control signals into a data packet, each of the one or more control signals being one of a plurality of different types of control signals for a standard protocol, each data packet including a plurality of bits to be transmitted;

a transmitter, the transmitter to transmit the data packets to the receiving device on the first control bus; and

logic to arbitrate use of the first control bus, the logic to arbitrate use being operable to:

determine whether the control bus is in use by the receiving device, and

if the first control bus is not in use by the receiving device, conduct arbitration for control of the first control bus, and wherein the receiving device is a device utilizing the standard protocol and the transmitting device is a mobile device utilizing a modified protocol, the modified protocol being a modification of the standard protocol that is not included in the standard protocol.

12. (Previously presented) The transmitting device of claim 11, wherein the transmitter is to drive the first control bus in a bi-phase mark signaling manner.

13. (Previously presented) The transmitting device of claim 11, wherein transmitting the one or more data packets on the first control bus includes transmitting a sync

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pulse to the receiving device at the beginning of each data packet to synchronize a clock of the receiving device to a clock of the transmitting device.

14. (Previously presented) The transmitting device of claim 11, further comprising a switchable pull-up circuit coupled with the first control bus.

15-16. (Canceled)

17. (Previously presented) The transmitting device of claim 11, wherein the standard protocol is HDMI (High-Definition Multimedia Interface).

18. (Previously presented) The transmitting device of claim 11, further comprising a USB-OTG (Universal Serial Bus On-The-Go) PHY (physical layer).

19. (Currently amended) A receiving device comprising:

a connection to a single first control bus, the first control bus being a bi-directional, single-line bus, wherein the receiving device is operable for coupling with a transmitting device via the first control bus;

a receiver to receive one or more data packets on the first control bus, each of the one or more data packets representing one of a plurality of different types of control signals; [[and]]

logic to convert each of the one or more data packets into a control signal; and

logic to arbitrate use of the first control bus, the logic to arbitrate use being operable to:

determine whether the control bus is in use by the transmitting device, and

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if the first control bus is not in use by the transmitting device, conduct arbitration for control of the first control bus, and wherein the receiving device is a device utilizing the standard protocol and the transmitting device is a mobile device utilizing a modified protocol, the modified protocol being a modification of the standard protocol that is not included in the standard protocol.

20. (Previously presented) The receiving device of claim 19, wherein the receiver is operable to decode the one or more received data packets according to bi-phase mark encoding.

21. (Previously presented) The receiving device of claim 19, wherein the receiver is operable to receive a sync pulse from the transmitting device on the first control line, the receiving device to synchronize a clock of the receiving device to a clock of the transmitting device.

22. (Previously presented) The receiving device of claim 19, further comprising a switchable pull-down circuit coupled with the first control bus.

23-24. (Canceled)

25. (Previously presented) The receiving device of claim 19, wherein the standard protocol is HDMI (High-Definition Multimedia Interface).

26. (Currently amended) The receiving device of ~~claim 24~~ claim 19, wherein the receiving device is a dual-mode device that is capable of communicating with a device utilizing the standard protocol or a device utilizing the modified protocol.

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27. (Currently amended) The method of claim 1, wherein the transmission of a data packet by the ~~initating~~ initiating device is followed by an acknowledge (ACK) message from the following device to the initiating device on the first control line.

28. (Currently amended) The method of claim 27, wherein the ~~initating~~ initiating device transmits a second data packet after receipt of the ACK message from the following device.

29. (Previously presented) The method of claim 1, wherein generating each data packet includes generating a header for each data packet to indicate a type of control signal represented by the data packet.

30. (Previously presented) The transmitting device of claim 11, wherein the logic to arbitrate use of the first control bus is further operable to take control of the first control bus if the transmitting device and the receiving device arbitrate use of the first control bus at the same time.

31. (Previously presented) The receiving device of claim 19, wherein the logic to arbitrate use of the first control bus is further operable to allow the transmitting device to take control of the first control bus if the transmitting device and the receiving device arbitrate use of the first control bus at the same time.

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REMARKS

Applicant respectfully requests reconsideration of this application. Claims 1-9, 11-14, 16-22, and 24-31 are currently pending.

Claims 1, 4, 5, 8, 9, 11, 19, and 26-28 have been amended. Claims 6, 16, and 24 have been canceled without prejudice. No claims have been added.

Therefore, claims 1-5, 7-9, 11-14, 17-22, and 25-31 are now presented for examination.

Information Disclosure Statement

Applicant requests that the Examiner consider the references contained in the information disclosure statement filed currently herewith.

Amendments to the Claims

The claim amendments provided herewith are based on the claim amendments contained in the Notice of Allowance dated April 8, 2010, with the following modifications:

- It is submitted that the use of the word "and" in line 10 of claim 1 and line 10 of claim 11 (as the claims are amended here) is correct, and thus this word has not been deleted from these claims.
- Claim 4 has been amended to insert the missing word "of" after the phrase "take control" in line 7 of the claim.
- Claim 5 has been corrected to be dependent on claim 1, rather than claim 4, which provides an alternative embodiment. Because claim 5 is no longer dependent on

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claim 4, the "second" time period and number of cycles in claim 5 has been corrected to be the "first" time period and number of cycles.

- Claims 27 and 28 are amended to correct a misspelling of the word "initiating" in such claims.

Conclusion

Applicant respectfully submits that the claims as amended are in condition for allowance.

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Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (503) 439-8778 if there remains any issue with allowance of the case.

Request for an Extension of Time if Needed

The Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. §1.136(a) should one be needed. Please charge any fee to our Deposit Account No. 02-2666.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Date: July 8. 2010

/Mark C. Van Ness /
Mark C. Van Ness
Reg. No. 39,865

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(503) 439-8778

LENOVO EXHIBIT 1002 - 261/502

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	11/969,852
	Filing Date	January 4, 2008
	First Named Inventor	Ranade, Shrikant
	Group Art Unit	2111
	Examiner Name	Cleary, Thomas
Sheet 1 of 1	Attorney Docket No: 8029P038	

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**
		US-20070083692	04/12/2007	LIU, H. S. et al.	
		US-20070201492	08/30/2007	KOBAYASHI, Osamu	
		US-20070279408	12/06/2007	ZHENG, Dong et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	**Cite No [1]**	**Foreign Patent Document** Country Code/Number/Kind Code (if known)	**Publication Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	**T [2]**
		EP-1519581	03/30/2005	GENESIS MICROCHIP, INC.,		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T [2]**
		USPTO, Non-Final Office Action for U.S. Patent Application No 11/969,865 (Attorney Docket No 8029P039) mailed October 28, 2009	
		USPTO, Notice of Allowance for US Patent Application No. 11/969,865 (Attorney Docket No. 8029P039) mailed May 11, 2010	
		"8029P037PCT ISR and WO Mailed 3/25/2009 for PCT/US2008/085287", Whole Document	
		"8029P039PCT ISR and WO Mailed 3/13/2009 for PCT/US2008/086879", Whole Document	
		"High-Definition Multimedia Interface Specification Version 1.3", Internet Citation XP002391813 - http://www.hdmi.org/download/HDMI_Spec_1.3_GMI.pdf, (retrieved on 7/26/2006), Whole Document	
		"High-Definition Multimedia Interface Specification Version 1.3a", November 10, 2006, cover page and page 1 of 156 pages only	
		"On-The-Go Supplement to the USB 2.0 Specification Revision 1.0", December 18, 2001; cover page, pages 1, 37-41, and 47-49	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	11/969,852
Filing Date	January 4, 2008
First Inventor	Shrikant Ranade
Art Unit	2111
Examiner Name	Thomas J. Cleary
Attorney Docket No.	8029P038 Conf. No. 1782

DUTY OF DISCLOSURE STATEMENT

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OR

☒ None

☐ The IDS Filing Fee in the amount of $180.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

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SIGNATURE

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Signature	/Mark C. Van Ness/	Date (MM-DD-YYYY)	07-08-2010
Name/Print	Mark C. Van Ness	Registration Number	39,865

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Lisa Riley /Lisa Riley/ *Date* *07-08-10*

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(54) Packet based high definition high-bandwidth digital content protection

(57) A packet based high bandwidth copy protection method is described that includes the following operations. Forming a number of data packets at a source device, encrypting selected ones of the data packets based upon a set of encryption values, transmitting the encrypted data packets from the source device to a sink device coupled thereto, decrypting the encrypted data packets based in part upon the encryption values, and accessing the decrypted data packets by the sink device.

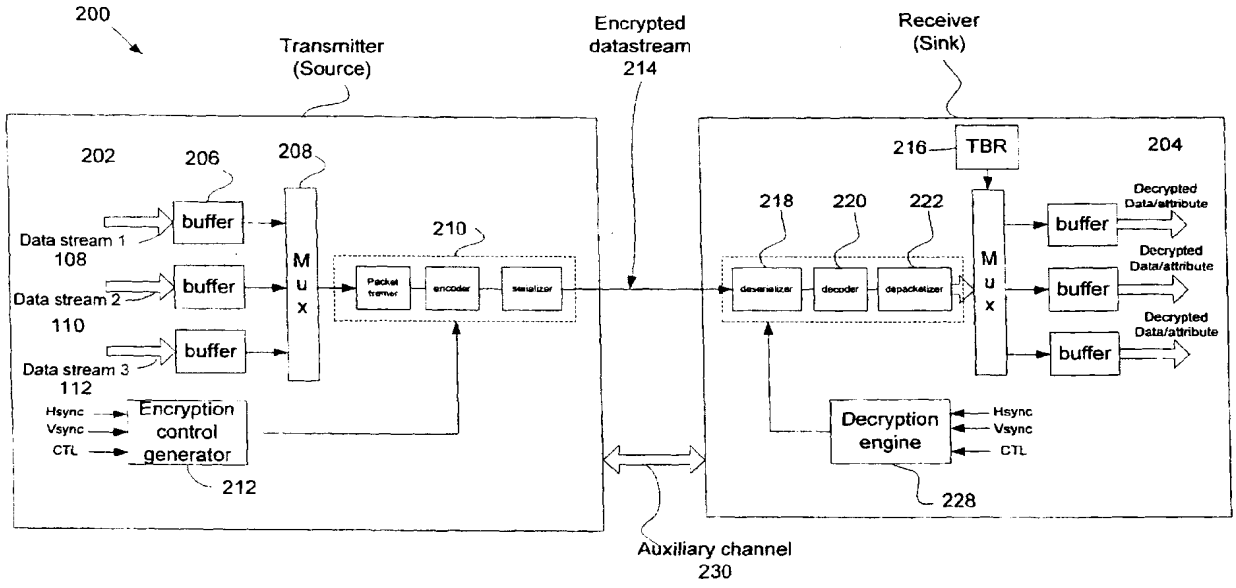


Fig. 2

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Description

[0001] The invention relates to display devices. More specifically, the invention describes a method and apparatus capable of providing a robust encryption of a audio/video data in a packet based transmission environment.

[0002] Protection of proprietary digital content has become an important consideration and more particularly, in high definition (HD), high-bandwidth applications. Especially important for HD, high-bandwidth applications, content protection provides assurances that owners of digitized content are protected from unauthorized use and copying of their proprietary content. A popular high-bandwidth digital-content protection scheme developed by Intel Corporation of Santa Clara CA commonly referred to as HDCP has been widely implemented. As currently configured, this particular HDCP protocol is specifically designed for use in Digital Visual Interface (DVI) and High-Definition Multimedia Interface (HDMI) based environments.

[0003] In general, HDCP encrypts the transmission of digital content between the video source, or transmitter -- such as a PC, DVD player or set-top box -- and the digital display, or receiver -- such as a monitor, television or projector. In this way, HDCP is designed to prevent copying or recording of digital content thereby protecting the integrity of content as it is being transmitted. For example, as required by the described HDCP protocol, during an authentication phase, the receiver will only be provided with content once it demonstrates knowledge of the authentication keys which the transceiver verifies through computation of a secret value. Furthermore, to prevent eavesdropping and stealing of the data, the transmitter and receiver will generate a shared secret value that is consistently checked throughout the transmission. Once authentication is established, the transmitter encrypts the data and sends it to the receiver for decryption.

[0004] The current implementation of the DVI standard requires the use of a set of defined characters based upon a 10 bit transmission protocol. For example, as currently configured, only 460 characters (out of a possible 1024 available) are used by the receiver for data while 4 characters are used as explicit control signals such as hsync and vsync. In this arrangement, any time the receiver receives and recognizes one of the predefined characters representing data, then the received implicitly defines a data enable signal (DE) as being active thereby indicating that the received data is true data. However, whenever one of the 4 control characters is received by the receiver, then an implicit assumption is made that data enable (DE) is inactive.

[0005] HDCP protocol uses the status of DE, H_{sync}, V_{sync} and another control signal, called CNTL3, to advance its state machine. The DE, H_{sync}, and V_{sync} signals are timing signals associated with raster video transmitted in a "streaming" manner. In a streaming transfer, the pixel data is transferred at pixel rate and the ratio of blanking period to data period is preserved. In case of a packet transfer, these timing signals may not be present. Only the pixel data may be transferred in the packet stream, while timing information is communicated in a different way. Therefore, what is required is a way to support high-definition copy protection that is compatible with existing high definition copy protection protocols such as HDCP over a link, or a transmission medium, that operates in a packet transfer mode.

[0006] What is provided, therefore, is a packet-based digital transmission medium and protocol that supports high definition copy protection that is backwards compatible with existing high definition copy protection protocols such as HDCP.

[0007] In one embodiment of the invention, a packet based high bandwidth copy protection method is described that includes the following operations. Forming a number of data packets at a source device, encrypting the data packets based upon a set of encryption values, transmitting the encrypted data packets from the source device to a sink device coupled thereto, decrypting the encrypted data packets based in part upon the encryption values, and accessing the decrypted data packets by the sink device.

[0008] In another embodiment, a system for providing packet based high bandwidth copy protection to a data stream is disclosed that includes a source unit arranged to provide a number of data packets, a sink unit coupled to the source unit arranged to receive the data packets from the source unit, an encryption unit coupled to the source unit arranged to encrypt the data packets sent from the source unit to the sink unit, a decryption unit coupled to the sink unit arranged to decrypt the encrypted data packets and an encryption/decryption values generator arranged to provide a set of encryption/decryption values used to encrypt and decrypt the appropriate data packets.

[0009] In yet another embodiment, computer program product for providing a packet based high bandwidth copy protection is disclosed that includes computer code for forming a number of data packets at a source device, computer code for encrypting the data packets based upon a set of encryption values, computer code for transmitting the encrypted data packets from the source device to a sink device coupled thereto, computer code for decrypting the encrypted data packets based in part upon the encryption values, computer code for accessing the decrypted data packets by the sink device, and computer readable medium for storing the computer code.

[0010] An embodiment of the invention will now be described in detail, by way of example only, and with reference to the accompanying drawings, in which:

Fig. 1 shows a generalized representation of a cross platform packet based digital video display interface suitable for use with any embodiment of the

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invention;

Fig. 2 shows an encryption system for encrypting audio/video content suitable for use with the system described with respect to Fig. 1;

Fig. 3 shows a representative encrypted data stream in accordance with an embodiment of the invention; and

Fig. 4 illustrates a system employed to implement the invention.

[0011] Reference will now be made in detail to a particular embodiment of the invention an example of which is illustrated in the accompanying drawings. While the invention will be described in conjunction with the particular embodiment, it will be understood that it is not intended to limit the invention to the described embodiment. To the contrary, it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims.

[0012] As currently implemented, HDCP establishes a secure channel in order to verify that the display device is licensed to receive protected content and once established, encrypts the data at the host side and decrypts at the display device in order to prevent 'eavesdropping' of the protected content. In addition, in order to identify unauthorized or comprised devices, HDCP relies upon authentication and key exchange, content encryption, and device renewability.

[0013] More specifically, HDCP protects copyrighted digital entertainment content in a Digital Video Interface (DVI) environment by encrypting its transmission between the video source and the digital display (receiver). The video source might be a PC, set-top boxes, DVD players and the like), and the digital display might be an liquid crystal display (LCD), television, plasma panel, or projector in which all authorized devices are given a set of unique secret device keys. During an authentication process, the receiver must demonstrate its knowledge of a number of secret device keys before the protected content is sent. After the receiver acknowledges the keys, both devices (the sender and receiver) generate a shared secret value that is designed to prevent eavesdroppers from stealing the content. After authentication, the content is encrypted and sent to the receiver that in turn decrypts it.

[0014] Authentication is a cryptographic process for verifying that the display device is authorized (or licensed) to receive protected content. Both the authorized host and the display device have knowledge of a set of secret keys that consist of an array of forty 56-bit secret device keys and a corresponding 40-bit binary Key Selection Vector (KSV). The host initiates authentication by sending an initiation message containing its Key Selection Vector, AKSV, and a 64-bit value An. The display device responds by sending a response message containing its Key Selection Vector, BKSV. The host confirms that the received KSV has not been revoked. At this point, the two devices can calculate a shared value, which, if both devices have a valid set of keys, will be equal. This shared value will be used in the encryption and decryption of the protected content since authentication has now been established.

[0015] Re-authentication continues at a rate of approximately once every two seconds to confirm the continued security of the link. If, at any time, equality of the shared value is lost, for example by disconnecting the display device and/or connecting an illegal recording device, the host will consider the DVI link to be unauthenticated, and end the transmission of protected content.

[0016] Content is encrypted at the source device to prevent usable, unauthorized copies of the transmitted content from being made. Encryption is the application of an algorithm, called a cipher, that transforms the content. To recover the content, the display device decrypts the content by knowledge of the correct decryption key. The HDCP cipher is a hybrid block/stream cipher. The block cipher operates during the authentication protocol. For content encryption and decryption, HDCP uses a stream cipher where encryption is accomplished by combining a data stream, generated by the HDCP cipher, with the transmitted content, through a bitwise exclusive-OR operation. In this way the content is protected pixel-by-pixel. Encrypted content viewed on a display device without decryption is seen as random noise, with no discernable content. As noted above, currently available HDCP protocols must be implemented using a DVI type connector.

[0017] The present invention provides a high definition high bandwidth copy protection protocol suitable for use in a packet based transmission medium that provides a robust digital copyright protection protocol that supports high definition copy protection that is backwards compatible with existing high definition copy protection protocols. In one embodiment of the invention the inventive HDCP protocol is carried out as a packet based high bandwidth copy protection method that includes forming a number of data packets at a source device, encrypting selected ones of the data packets based upon a set of encryption values, transmitting the encrypted data packets from the source device to a sink device coupled thereto, decrypting the encrypted data packets based in part upon the encryption values, and accessing the decrypted data packets by the sink device.

[0018] A particularly well suited packet based transmission system is described with reference to Fig. 1 that shows a generalized representation of a cross platform packet based digital video display interface 100 suitable for use with any embodiment of the invention. The interface 100 connects a transmitter 102 to a receiver 104 by way of a physical link 106 (also referred to as a pipe). In the described embodiment, a number of data streams 108 - 112 are received at the transmitter 102 that, if necessary, packetizes each into a corresponding number of data packets 114. These data packets are then

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formed into corresponding data streams each of which are passed by way of an associated virtual pipe 116 - 120 to the receiver 104. It should be noted that the data streams 108 - 112 can take any number of forms such as video, graphic, audio, etc.

[0019] Typically, when the source is a video source, the data streams 108 - 112 include various video signals that can have any number and type of well-known formats, such as composite video, serial digital, parallel digital, RGB, or consumer digital video. The video signal can be an analog video signal provided the source 102 includes some form of an analog video source such as for example, an analog television, still camera, analog VCR, DVD player, camcorder, laser disk player, TV tuner, set top box (with satellite DSS or cable signal) and the like. The source 102 can also include a digital image source such as for example a digital television (DTV), digital still camera, and the like. The digital video signal can be any number and type of well known digital formats such as, SMPTE 274M-1995 (1920 x 1080 resolution, progressive or interlaced scan), SMPTE 296M-1997 (1280 x 720 resolution, progressive scan), as well as standard 480 progressive scan video.

[0020] In the case where the source 102 provides an analog image signal, an analog-to-digital converter (A/D) converts an analog voltage or current signal into a discrete series of digitally encoded numbers (signal) forming in the process an appropriate digital image data word suitable for digital processing. Any of a wide variety of A/D converters can be used. By way of example, other A/D converters include, for example those manufactured by: Philips, Texas Instrument, Analog Devices, Brooktree, and others.

[0021] For example, if the data stream 110 is an analog type signal, the an analog to digital converter (not shown) included in or coupled to the transmitter 102 will digitize the analog data which is then packetize by a packetizer that converts the digitized data stream 110 into a number of data packets 114 each of which will be transmitted to the receiver 104 by way of the virtual link 116. The receiver 104 will then reconstitute the data stream 110 by appropriately recombining the data packets 114 into their original format. It is these data streams that are ultimately encrypted for form a set of copy protected data streams.

[0022] Fig. 2 shows an encryption system 200 for encrypting audio/video content suitable for use with the system 100 described with respect to Fig. 1. As shown in Fig. 2, a video source 202 is arranged to provide a number of data streams such as the datastreams 110 and 112. By utilizing a number of data streams, the system 200 is capable of transmitting video data, for example, consistent with any of a number of video formats concurrently. For example, the data stream 110 is formed of video data consistent with 1024 x 768 at 60 Hz whereas the datastream 112 is formed of video data consistent with 640 x 480 at 75Hz, and so on. In order for a receiver 204 (such as a monitor) to reconstruct the video in the appropriate format, the datastreams include in addition the appropriate video data associated attribute data that is used by the receiver to reconstruct the video in the appropriate format.

[0023] Accordingly, the video source 202 includes a number of buffers 206 each of which is used to buffer an associated one of the video datastreams. Each of the buffers is, in turn, coupled to a multiplexer 208 that is used to select a particular one of the data streams for transmission to a packetizer 210. The packetizer 210 parses the incident data stream into an associated number of data packets by incorporating a packet ID, optionally performing error correction, and attaching a time stamp and any of the attributes deemed important or necessary for the correct reconstruction of the video raster by the receiver 404. An encryption control generator unit 212 applies an appropriate encryption algorithm to each of the data packets based at least by inserting a control packet that conveys signals such as H_{sync}, V_{sync}, and a particular control character CNTL3 used to flag those data packets that are encrypted (and conversely those data packets that are not encrypted).

[0024] In accordance with an embodiment of the invention, the resulting encrypted data stream 214 (a particular example of which is shown in Fig. 3 as a datastream 300) is formed of a number of data packets. The data stream 300 includes a number of control packets 302 used to mark those video data packets that are encrypted (or not encrypted) as the case may be. Each video packet has an associated header 304 that includes, in part, the attribute data described above associated with the video data packet 306. For example, in the case shown in Fig. 3, the data stream 300 includes data packets for the datastream 110 and the datastream 112 conjoined into the data stream 300 such that the traffic between the video source 202 and the receiver 204 is consistent with a constant link environment.

[0025] It should be noted that in the described embodiment, the data stream 300 is time domain multiplexed, those data packets associated with the datastream 110 have a longer duration than those associated with the data stream 112. In these cases, a time-base recovery (TBR) unit 216 within the receiver 204 regenerates the stream's original native rate using time stamps embedded in the main link data packets, if necessary. Referring back to Fig. 2, at the receiver 404, a deserializer unit 218 receives the encrypted datastream 300 that provides input to a decoder unit 220 and a depacketizer 222. The decoder 220 decodes the control packet, thus feeding H_{sync}, V_{sync}, and a particular control character CNTL3provided to a decryption engine 228 that was previously used to for encryption.

[0026] Fig. 4 illustrates a system 400 employed to implement the invention. Computer system 400 is only an example of a graphics system in which the present invention can be implemented. System 400 includes central processing unit (CPU) 410, random access memory (RAM) 420, read only memory (ROM) 425, one or more

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peripherals 430, graphics controller 460, primary storage devices 440 and 450, and digital display unit 470. CPUs 410 are also coupled to one or more input/output devices 490 that may include, but are not limited to, devices such as, track balls, mice, keyboards, microphones, touch-sensitive displays, transducer card readers, magnetic or paper tape readers, tablets, styluses, voice or handwriting recognizers, or other well-known input devices such as, of course, other computers. Graphics controller 460 generates analog image data and a corresponding reference signal, and provides both to digital display unit 470. The analog image data can be generated, for example, based on pixel data received from CPU 410 or from an external encode (not shown). In one embodiment, the analog image data is provided in RGB format and the reference signal includes the V_{SYNC} and H_{SYNC} signals well known in the art. However, it should be understood that the present invention can be implemented with analog image, data and/or reference signals in other formats. For example, analog image data can include video signal data also with a corresponding time reference signal.

[0027] Although only a few embodiments of the present invention have been described, it should be understood that the present invention may be embodied in many other specific forms without departing from the the scope of the present invention. The present examples are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope of the appended claims along with their full scope of equivalents.

[0028] While this invention has been described in terms of a preferred embodiment, there are alterations, permutations, and equivalents that fall within the scope of this invention. It should also be noted that there are many alternative ways of implementing both the process and apparatus of the present invention. It is therefore intended that the invention be interpreted as including all such alterations, permutations, and equivalents as fall within the true scope of the present invention.

Claims

1. A packet based high bandwidth copy protection method comprising:

   forming a number of data packets at a source device;
   encrypting the data packets based upon a set of encryption values;
   transmitting the encrypted data packets from the source device to a sink device coupled thereto;
   decrypting the encrypted data packets based in part upon the encryption values; and
   accessing the decrypted data packets by the sink device.

2. A method as recited in claim 1, wherein the source device is a video source and wherein the sink device is a video display and wherein the number of data packets include some audio data packets and some video data packets.

3. A method as recited in claim 2, wherein the encryption/decryption control signals include a Vsync, an Hsync, and a CNTL3.

4. A method as recited in claim 3, wherein each of the data packets is associated with an particular control packet.

5. A method as recited in claim 4, wherein when the CNTL3 is active, then the corresponding data packet is encrypted and vice-versa.

6. A system for providing high bandwidth copy protection in a packet based system, comprising:

   a source unit arranged to provide a number of data packets;
   a sink unit coupled to the source unit arranged to receive the data packets from the source unit;
   an encryption unit coupled to the source unit arranged to encrypt selected ones of the data packets sent from the source unit to the sink unit;
   a decryption unit coupled to the sink unit arranged to decrypt the encrypted data packets; and
   an encryption/decryption values generator arranged to provide a set of encryption/decryption values used to encrypt and decrypt the appropriate data packets.

7. A system as recited in claim 6, wherein the source unit is an audio/video unit arranged to provide audio type data packets and/or video type data packets.

8. A system as recited in claim 7, wherein the sink unit is a display unit arranged to display processed ones of the video data packets.

9. A system as recited in claim 8, wherein the display unit includes a number of speakers arranged to transmit audio signals based upon processed ones of the audio data packets.

10. A system as recited in claim 9, wherein the set of encryption/decryption control signals include Vsynch, Hsynch corresponding to the video data packets.

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11. A system as recited in claim 10, wherein the set of encryption/decryption control signal further includes CNTL3 to flag those data packets that are encrypted.

12. Computer program product for providing a packet based high bandwidth copy protection, comprising:

computer code for forming a number of data packets at a source device;
computer code for encrypting the data packets based upon a set of encryption values;
computer code for transmitting the encrypted data packets from the source device to a sink device coupled thereto;
computer code for decrypting the encrypted data packets based in part upon the encryption values;
computer code for accessing the decrypted data packets by the sink device; and
computer readable medium for storing the computer code.

13. Computer program product as recited in claim 12, wherein the source device is a video source and wherein the sink device is a video display and wherein the number of data packets include some audio data packets and some video data packets.

14. Computer program product as recited in claim 13, wherein the encryption control signals include a Vsync, an Hsync, and a CNTL3.

15. Computer program product as recited in claim 14, wherein each of the data packets is associated with an particular control value CNTL3.

16. Computer program product as recited in claim 15, wherein when the CNTL3 is active, then the corresponding data packet is encrypted and vice-versa.

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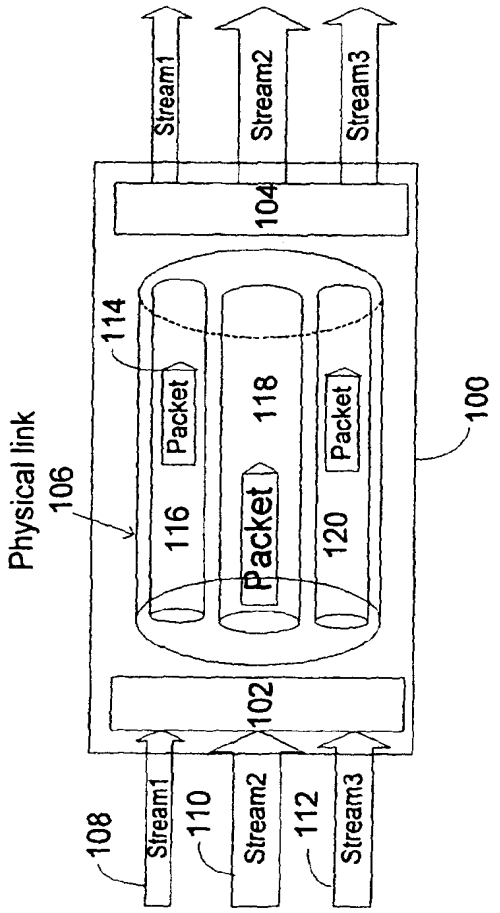


Fig. 1

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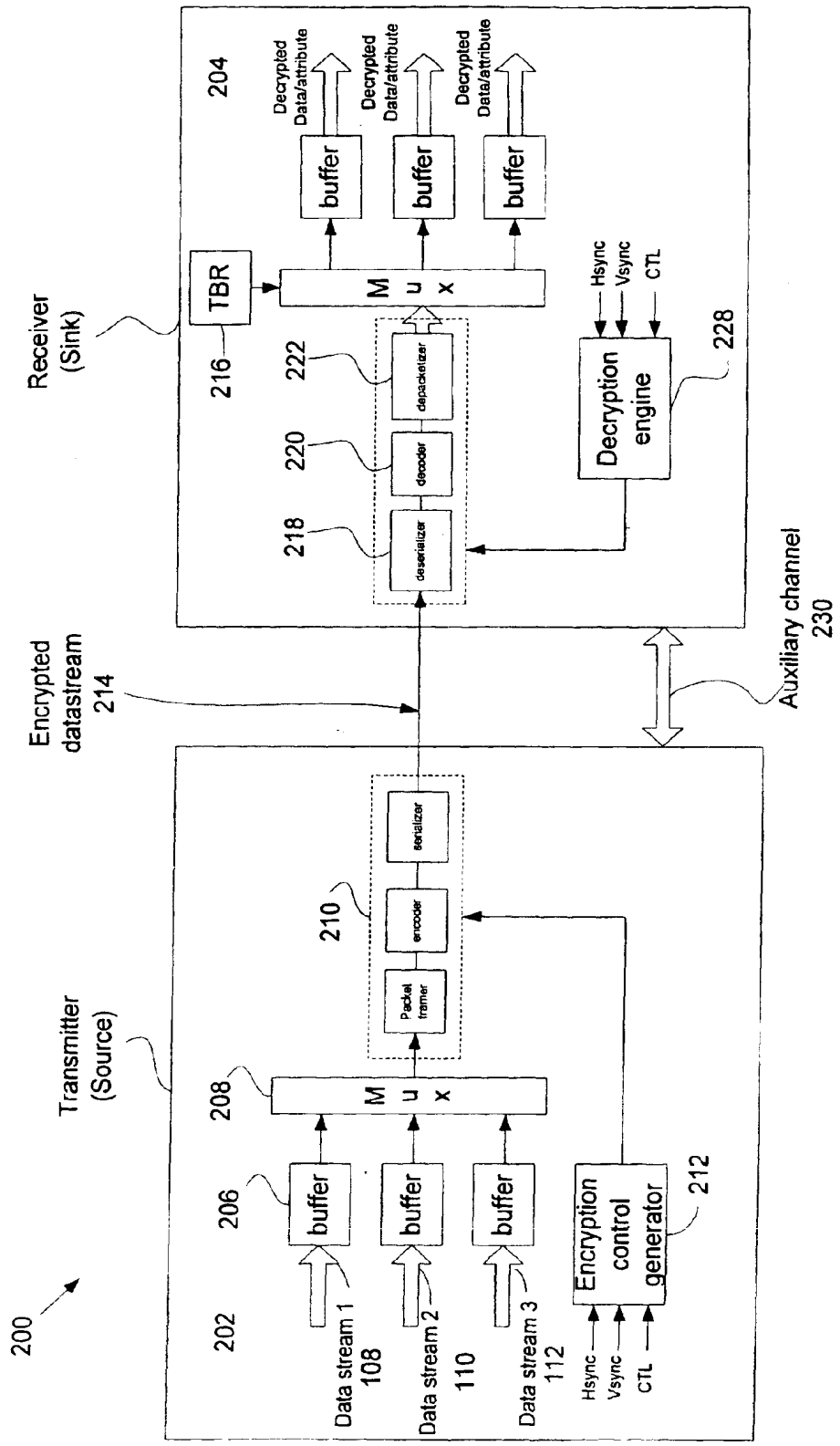


Fig. 2

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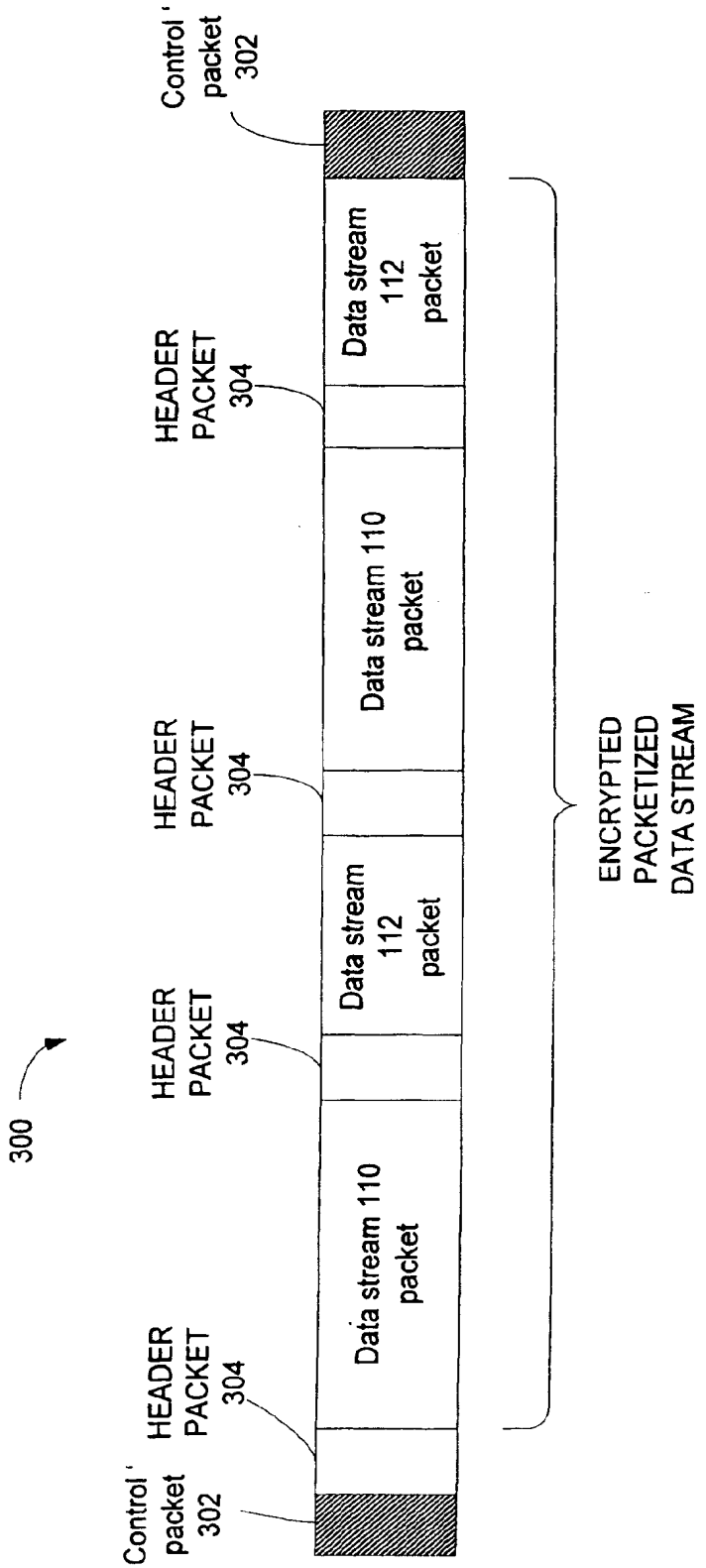


Fig. 3

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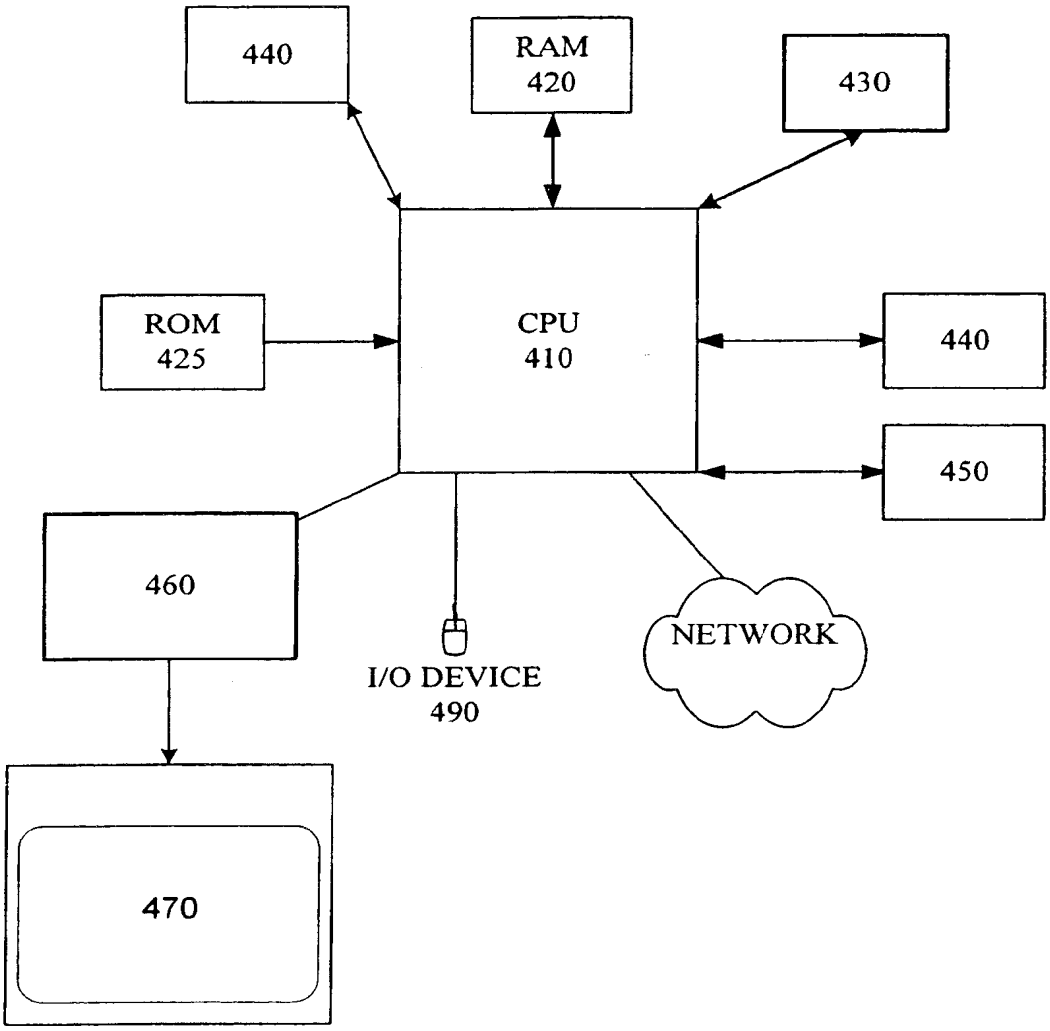


Fig. 4

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 04 25 5786

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			H04N H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	7 December 2004	Apostolescu, R

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 04 25 5786

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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		JP 2004523188 T	29-07-2004
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EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

LENOVO EXHIBIT 1002 - 275/502

BNSDOCID: <EP 1519581A1 I >

PATENT COOPERATION TREATY

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APR 01 2009
BEAVERTON

From the INTERNATIONAL SEARCHING AUTHORITY

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

To:
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Attn. Vincent, Lester J.
1279 Oakmead Parkway
Sunnyvale CA 94085-4040
ETATS-UNIS D'AMERIQUE

Date of mailing *(day/month/year)*	25/03/2009
Applicant's or agent's file reference: 8029P037PCT	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No.: PCT/US2008/085287	International filing date *(day/month/year)* 02/12/2008
Applicant: SILICON IMAGE, INC.	

1. [x] The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the International Application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the International Search Report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Fascimile No.: (41-22) 338.82.70

   For more detailed instructions, see the notes on the accompanying sheet.

2. [ ] The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. [ ] **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   [ ] the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   [ ] no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the International Searching Authority	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Annemieke Rozendaal

NOTES TO FORM PCT/ISA/220

These Notes are intended to give the basic instructions concerning the filing of amendments under article 19. The Notes are based on the requirements of the Patent Cooperation Treaty, the Regulations and the Administrative Instructions under that Treaty. In case of discrepancy between these Notes and those requirements, the latter are applicable. For more detailed information, see also the *PCT Applicant's Guide*, a publication of WIPO.

In these Notes, "Article", "Rule", and "Section" refer to the provisions of the PCT, the PCT Regulations and the PCT Administrative Instructions, respectively.

INSTRUCTIONS CONCERNING AMENDMENTS UNDER ARTICLE 19

The applicant has, after having received the international search report and the written opinion of the International Searching Authority, one opportunity to amend the claims of the international application. It should however be emphasized that, since all parts of the international application (claims,description and drawings) may be amended during the international preliminary examination procedure, there is usually no need to file amendments of the claims under Article 19 except where, e.g. the applicant wants the latter to be published for the purposes of provisional protection or has another reason for amending the claims before international publication. Furthermore, it should be emphasized that provisional protection is available in some States only (see *PCT Applicant's Guide*, Volume I/A, Annexes B1 and B2).

The attention of the applicant is drawn to the fact that amendments to the claims under Article 19 are not allowed where the International Searching Authority has declared, under Article 17(2), that no international search report would be established (see *PCT Applicant's Guide*, Volume I/A, paragraph 296).

What parts of the international application may be amended?

Under Article 19, only the claims may be amended.

During the international phase, the claims may also be amended (or further amended) under Article 34 before the International Preliminary Examining Authority. The description and drawings may only be amended under Article 34 before the International Examining Authority.

Upon entry into the national phase, all parts of the international application may be amended under Article 28 or, where applicable, Article 41.

When? Within 2 months from the date of transmittal of the international search report or 16 months from the priority date, whichever time limit expires later. It should be noted, however, that the amendments will be considered as having been received on time if they are received by the International Bureau after the expiration of the applicable time limit but before the completion of the technical preparations for international publication (Rule 46.1).

Where not to file the amendments?

The amendments may only be filed with the International Bureau and not with the receiving Office or the International Searching Authority (Rule 46.2).

Where a demand for international preliminary examination has been/is filed, see below.

How? Either by cancelling one or more entire claims, by adding one or more new claims or by amending the text of one or more of the claims as filed.

A replacement sheet must be submitted for each sheet of the claims which, on account of an amendment or amendments, differs from the sheet originally filed.

All the claims appearing on a replacement sheet must be numbered in Arabic numerals. Where a claim is cancelled, no renumbering of the other claims is required. In all cases where claims are renumbered, they must be renumbered consecutively (Section 205(b)).

The amendments must be made in the language in which the international application is to be published.

What documents must/may accompany the amendments?

Letter (Section 205(b)):

The amendments must be submitted with a letter.

The letter will not be published with the international application and the amended claims. It should not be confused with the "Statement under Article 19(1)" (see below, under "Statement under Article 19(1)").

The letter must be in English or French, at the choice of the applicant. However, if the language of the international application is English, the letter must be in English; if the language of the international application is French, the letter must be in French.

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NOTES TO FORM PCT/ISA/220 (continued)

The letter must indicate the differences between the claims as filed and the claims as amended. It must, in particular, indicate, in connection with each claim appearing in the international application (it being understood that identical indications concerning several claims may be grouped),whether

(i) the claim is unchanged;

(ii) the claim is cancelled;

(iii) the claim is new;

(iv) the claim replaces one or more claims as filed;

(v) the claim is the result of the division of a claim as filed.

The following examples illustrate the manner in which amendments must be explained in the accompanying letter:

1. [Where originally there were 48 claims and after amendment of some claims there are 51]:
"Claims 1 to 29, 31, 32, 34, 35, 37 to 48 replaced by amended claims bearing the same numbers; claims 30, 33 and 36 unchanged; new claims 49 to 51 added."

2. [Where originally there were 15 claims and after amendment of all claims there are 11]:
"Claims 1 to 15 replaced by amended claims 1 to 11."

3. [Where originally there were 14 claims and the amendments consist in cancelling some claims and in adding new claims]:
"Claims 1 to 6 and 14 unchanged; claims 7 to 13 cancelled; new claims 15, 16 and 17 added." or
"Claims 7 to 13 cancelled; new claims 15, 16 and 17 added; all other claims unchanged."

4. [Where various kinds of amendments are made]:
"Claims 1–10 unchanged; claims 11 to 13, 18 and 19 cancelled; claims 14, 15 and 16 replaced by amended claim 14; claim 17 subdivided into amended claims 15, 16 and 17; new claims 20 and 21 added."

"Statement under article 19(1)" (Rule 46.4)

The amendments may be accompanied by a statement explaining the amendments and indicating any impact that such amendments might have on the description and the drawings (which cannot be amended under Article 19(1)).

The statement will be published with the international application and the amended claims.

It must be in the language in which the international application is to be published.

It must be brief, not exceeding 500 words if in English or if translated into English.

It should not be confused with and does not replace the letter indicating the differences between the claims as filed and as amended. It must be filed on a separate sheet and must be identified as such by a heading, preferably by using the words "Statement under Article 19(1)."

It may not contain any disparaging comments on the international search report or the relevance of citations contained in that report. Reference to citations, relevant to a given claim, contained in the international search report may be made only in connection with an amendment of that claim.

Consequence if a demand for international preliminary examination has already been filed

If, at the time of filing any amendments and any accompanying statement, under Article 19, a demand for international preliminary examination has already been submitted, the applicant must preferably, at the time of filing the amendments (and any statement) with the International Bureau, also file with the International Preliminary Examining Authority a copy of such amendments (and of any statement) and, where required, a translation of such amendments for the procedure before that Authority (see Rules 55.3(a) and 62.2, first sentence). For further information, see the Notes to the demand form (PCT/IPEA/401).

If a demand for international preliminary examination is made, the written opinion of the International Searching Authority will, except in certain cases where the International Preliminary Examining Authority did not act as International Searching Authority and where it has notified the International Bureau under Rule 66.1*bis*(b), be considered to be a written opinion of the International Preliminary Examining Authority. If a demand is made, the applicant may submit to the International Preliminary Examining Authority a reply to the written opinion together, where appropriate, with amendments before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later (Rule 43*bis*.1(c)).

Consequence with regard to translation of the international application for entry into the national phase

The applicant's attention is drawn to the fact that, upon entry into the national phase, a translation of the claims as amended under Article 19 may have to be furnished to the designated/elected Offices, instead of, or in addition to, the translation of the claims as filed.

For further details on the requirements of each designated/elected Office, see the *PCT Applicant's Guide,* Volume II.

LENOVO EXHIBIT 1002 - 278/502

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
8029P037PCT		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2008/085287	02/12/2008	04/01/2008
Applicant		
SILICON IMAGE, INC.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language,** the international search was carried out on the basis of:
      [X] the international application in the language in which it was filed
      [ ] a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. [ ] This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. [ ] With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. [ ] **Certain claims were found unsearchable** (See Box No. II)

3. [ ] **Unity of invention is lacking** (see Box No III)

4. With regard to the **title,**
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority

6. With regard to the **drawings,**
   a. the figure of the **drawings** to be published with the abstract is Figure No. 7
      [X] as suggested by the applicant
      [ ] as selected by this Authority, because the applicant failed to suggest a figure
      [ ] as selected by this Authority, because this figure better characterizes the invention
   b. [ ] none of the figures is to be published with the abstract

LENOVO EXHIBIT 1002 - 279/502

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/085287

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F3/14 G09G5/00 G06F13/40 H04L29/06 H04N7/10
H04M1/725

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F G09G H04L H04N H04M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	"High-Definition Multimedia Interface Specification Version 1.3" INTERNET CITATION, [Online] XP002391813 Retrieved from the Internet: URL:http://www.hdmi.org/download/HDMI_Spec_1.3_GM1.pdf> [retrieved on 2006-07-24] the whole document	1-25
X	EP 1 519 581 A (GENESIS MICROCHIP INC [US]) 30 March 2005 (2005-03-30) the whole document	1,4-7,9, 10, 15-17, 21,23,25
X	US 2007/279408 A1 (ZHENG DONG [US] ET AL) 6 December 2007 (2007-12-06) the whole document	1,10,15, 21

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 March 2009	25/03/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Gartlan, Michael

6

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2008/085287

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 1519581 A	30-03-2005	CN 1607793 A	20-04-2005
		JP 2005110248 A	21-04-2005
		KR 20050030877 A	31-03-2005
		SG 110157 A1	28-04-2005
		US 2005069130 A1	31-03-2005
US 2007279408 A1	06-12-2007	NONE	

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PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

PCT

see form PCT/ISA/220

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY
(PCT Rule 43*bis*.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2008/085287	02.12.2008	04.01.2008

International Patent Classification (IPC) or both national classification and IPC
INV. G06F3/14 G09G5/00 G06F13/40 H04L29/06 H04N7/10 H04M1/725

Applicant
SILICON IMAGE, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA:

European Patent Office
D-80298 Munich
Tel. +49 89 2399 - 0
Fax: +49 89 2399 - 4465

Date of completion of this opinion
see form PCT/ISA/210

Authorized Officer
Gartlan, Michael
Telephone No. +49 89 2399-4732

LENOVO EXHIBIT 1002 - 282/502

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material:

      ☐ a sequence listing

      ☐ table(s) related to the sequence listing

   b. format of material:

      ☐ on paper

      ☐ in electronic form

   c. time of filing/furnishing:

      ☐ contained in the international application as filed.

      ☐ filed together with the international application in electronic form.

      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	3, 8,13, 24, 18, 19, 24
	No:	Claims	1, 2, 4, 5, 6, 7, 9, 10, 11, 12, 14, 15, 16, 17, 20, 21, 22, 23, 25
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-25
Industrial applicability (IA)	Yes:	Claims	1-25
	No:	Claims	

2. Citations and explanations

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Re Item VIII
Certain observations on the international application

1 The application does not meet the requirements of Article 6 PCT, because the following claims are not clear and concise:

1.1 Claims **1**, **10** and **15** have been drafted as **separate independent method claims**.

Claim 1 defines a device (apparatus) comprising a transmitter and a receiver coupled together. Claim 10 (system) and 15 (network) also claim a device comprising the same device features of claim 1 (merging, unmerging of channels)

Therefore, as claim 10 and 15 include all the features of claim 1, **claim 10 and 15** should be reformulated as a claim dependent on claim 1 (PCT, Article 6.4(a)(part), (b), (c))

1.2 The definition of the subject-matter of following claims is unclear, Article 6 PCT:

claim 1, 10, 17 : the wording "unmerge the sinlge channel into the multiple channels" is unclear as it can be understood as a feedback from the receiver to the transmitter (from where "the multiple channels" are first defined) - thus claim not supported by description

claim 15: The scope/meaning of the wording " a single data channel having the multiple data channels is unclear" (Note: examiner assumes same multiplexing/demultiplexing features as claimed in claim 1 and 10). Furthermore, the wording "the data channels having configured" and "and and/or auxiliary data" syntactically unclear.

claim 4, 12, 23 : wording "and control packets are carried by multiple channels of the channels over." - sentence ending with word "over" leaves reader in doubt as to meaning / scope of claim. Furthermore the term "the channels" is vague - not clear which "channels" are beign referenced. The wording "audio data, video data, and/or auxiliary data" is obscure in meaning as result of the comma before the "and/or". The wording "either together or separately" does not appear to be limiting and is thus inconcise.

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claim 8, 13, 24: the word "**if**" in the device claim is unclear. Furthermore it is noted that there is no support in the description for automatically repositioning logic i.e. the device features are fixed in function and order.

claim 9, 14, 25: the word "if" is unclear for same reason given above with respect to claims 8, 13, 24. Also these claims, in so far as they are dependent on claims 8, 13, 24 respectively, do not make technical sense - not clear the ordering of the decoding and demultiplexing logic. Claim 9, 14, 25 would be better served when dependent on claims 7, 12, 23 respectively.

Re Item V.

1 Reference is made to the following document:

D1: "High-Definition Multimedia Interface Specification Version 1.3" INTERNET CITATION, [Online] XP002391813 Retrieved from the Internet: URL:http://www.hdmi.org/download/HDMI_Spec _1.3_GM1.pdf> [retrieved on 2006-07-24]

D2: EP-A-1 519 581 (GENESIS MICROCHIP INC [US]) 30 March 2005 (2005-03-30)

D3: US 2007/279408 A1 (ZHENG DONG [US] ET AL) 6 December 2007 (2007-12-06)

2 The above-mentioned clarity problems notwithstanding, the subject-matter of **claims 1-25** does not meet the requirements of the PCT with respect to novelty and inventive step.

3 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of **independent device claims 1, 10, 15 and 21** is not new in the sense of Article 33(2) PCT.

3.1 Document **D1**, which is considered to represent the most relevant state of the art, discloses (the references in parentheses applying to this document):

An apparatus comprising:
a transmitter (*see fig. 5-1 (item source) and corresponding text*) configured to merge

multiple channels of a high-definition interface into a single channel (*see fig. 5-1 (items "channel 1", "encoder/Serializer", "Pixel component (e.g. G)", "Auxiliary data (e.g. Audio sample)") - the multiple channels (i.e. "Pixel component (e.g. G)", "Auxiliary data (e.g. Audio sample)") are merged into the single channel ("channel 1")*) to generate a mobile high-definition interface, the mobile high-definition interface configured to facilitate carrying of high-definition media content in a mobile device; and

a receiver coupled with the transmitter, the receiver configured to receive the single channel, and to unmerge the single channel into the multiple channels (*see fig. 5-1 (items "channel 1", "Recovery/decoder", "Pixel component (e.g. G)", "Auxiliary data (e.g. Audio sample)") - the single channel ("channel 1") is unmerged into the multiple channels (i.e. "Pixel component (e.g. G)", "Auxiliary data (e.g. Audio sample)")*)

The subject-matter of claim 1 is therefore known from **D1**.

3.2 **Independent device claim 10 and 15** appear to contain the same subject-matter as that claimed in claim 1 (i.e. merging / unmerging).
The subject-matter of claim 10 and 15 is therefore also known from **D1**.

3.3 **Independent method claim 21** appears to contain same subject-matter as that claimed in claim 1 (i.e. merging / unmerging), expressed in terms of method steps.
The subject-matter of claim 10 and 15 is therefore also known from **D1**.

3.4 For the sake of completeness the following points are noted:

a) The subject-matter of independent claims 1, 10, 15 and 21 is also disclosed by document **D2**(see fig. 1, 2 and corresponding text) and **D3**(see fig. 1 and corresponding text).

b) an amended independent claim which would meet the requirement of novelty with respect to **D1**, would still not appear inventive in light of the teaching of **D1** and combined with the common knowledge of the skilled person. In particular, the skilled person knows that the number of wires / pins in an interface can be reduced in order to reduce cost / space by the technique of time-division multiplexing - as exemplified by **D1** (see **D1** shares/merges/multiplexes video and audio onto same channel as

detailed above - rather than including a dedicated channel for audio (compare with well known DVI standard). Extending this teaching to reduce number of channels further does not require an inventive step - it is a standard implementation trade-off between communication bandwidth and cost. There are also many other examples in the prior are of using the time-division multiplexing technique to reduce number of pins / wires and thus space / cost (as exemplified by **D2** (see fig. 2) and **D3** (see fig. 1))

4 **Dependent claims 2-9, 11-14, 16-20, 22-25** do not appear tp contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty and/or inventive step, for the following reasons:

claim 2, 11, 22: **D1** discloses "a single control bus representing a Display Data Channel (DDC) bus" (*see fig. 8-1 (item "DDC line")*) and a Consumer Electronics Control (CEC) bus (*see fig. 8-1 (item "CEC bus")*)

claim 3: including/embedding the well known USB bus into the interface does not require the skilled person to perform an inventive activity.

claim 4, 5, 12, 23 : channels carrying video, audio, auxiliary data, HSYNC, VSYNC etc disclosed by **D1** (see fig. 5-1) and **D2** (fig. 2)

claim 6, 7, 16, 17 : use of multiplexor and demultiplexor at transmitter and receiver respectively well known to skilled person as exemplified by **D2** (fig. 2 (item "mux" in transmitter and receiver))

claim 9, 14, 25 : demultiplexing after decoding well known to skilled person as exemplified by **D3** (see fig. 1 item 151 for decoding, followed by item 158 for demultiplexing; par. 17) and **D2** (fig. 2 (items 220/decoder, "mux" in receiver/sink))

claim 8, 13, 24 : demultiplexing before decoding is an obvious alternative to skilled person, this alternative would be implemented according to circumstances (e.g. design implementation trade-off of increased silicon area of decoder (3 decoder instances instead of 1) for reduced decoder clock speed (since decoder after demultiplexor)

claim 18, 19: use of docking station as an interface adaptor well known to the skilled person

claim 20 : integrating the above features into a mobile audio/video device does not require an inventive activity

5 The industrial applicability (Article 33(4) PCT) of the subject-matter of all claims is given in an obvious manner.

Possible steps after receipt of the international search report (ISR) and written opinion of the International Searching Authority (WO-ISA)

General information	For all international applications filed on or after 01/01/2004 the competent ISA will establish an ISR. It is accompanied by the WO-ISA. Unlike the former written opinion of the IPEA (Rule 66.2 PCT), the WO-ISA is not meant to be responded to, but to be taken into consideration for further procedural steps. This document explains about the possibilities.
Amending claims under Art. 19 PCT	Within 2 months after the date of mailing of the ISR and the WO-ISA the applicant may file amended claims under Art. 19 PCT directly with the International Bureau of WIPO. The PCT reform of 2004 did not change this procedure. For further information please see Rule 46 PCT as well as form PCT/ISA/220 and the corresponding Notes to form PCT/ISA/220.
Filing a demand for international preliminary examination	In principle, the WO-ISA will be considered as the written opinion of the IPEA. This should, in many cases, make it unnecessary to file a demand for international preliminary examination. If the applicant nevertheless wishes to file a demand this must be done before expiry of 3 months after the date of mailing of the ISR/WO-ISA or 22 months after priority date, whichever expires later (Rule 54bis PCT). Amendments under Art. 34 PCT can be filed with the IPEA as before, normally at the same time as filing the demand (Rule 66.1 (b) PCT). If a demand for international preliminary examination is filed and no comments/amendments have been received the WO-ISA will be transformed by the IPEA into an IPRP (International Preliminary Report on Patentability) which would merely reflect the content of the WO-ISA. The demand can still be withdrawn (Art. 37 PCT).
Filing informal comments	After receipt of the ISR/WO-ISA the applicant may file informal comments on the WO-ISA directly with the International Bureau of WIPO. These will be communicated to the designated Offices together with the IPRP (International Preliminary Report on Patentability) at 30 months from the priority date. Please also refer to the next box.
End of the international phase	At the end of the international phase the International Bureau of WIPO will transform the WO-ISA or, if a demand was filed, the written opinion of the IPEA into the IPRP, which will then be transmitted together with possible informal comments to the designated Offices. The IPRP replaces the former IPER (international preliminary examination report).
Relevant PCT Rules and more information	Rule 43 PCT, Rule 43bis PCT, Rule 44 PCT, Rule 44bis PCT, PCT Newsletter 12/2003, OJ 11/2003, OJ 12/2003

BNSDOCID: <XS 200704010CK I >

Bitte beachten Sie, dass angeführte Nichtpatentliteratur (wie z. B. wissenschaftliche oder technische Dokumente) je nach geltendem Recht dem Urheberrechtsschutz und/oder anderen Schutzarten für schriftliche Werke unterliegen könnte. Die Vervielfältigung urheberrechtlich geschützter Texte, ihre Verwendung in anderen elektronischen oder gedruckten Publikationen und ihre Weitergabe an Dritte ist ohne ausdrückliche Zustimmung des Rechtsinhabers nicht gestattet.

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XS CPRTENFRDE

PATENT COOPERATION TREATY

RECEIVED
MAR 17 2009
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN
SUNNYVALE INTL FILING DEPT

From the INTERNATIONAL SEARCHING AUTHORITY

PCT

To:
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Attn. Vincent, Lester J.
1279 Oakmead Parkway
Sunnyvale CA 94085-4040
ETATS-UNIS D'AMERIQUE

RECEIVED
MAR 19 2009
BEAVERTON

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

	Date of mailing *(day/month/year)* 13/03/2009
Applicant's or agent's file reference 8029P039PCT	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US2008/086879	International filing date *(day/month/year)* 15/12/2008
Applicant SILICON IMAGE, INC.	

1. [x] The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the International Application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the International Search Report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Fascimile No.: (41-22) 338.82.70

   For more detailed instructions, see the notes on the accompanying sheet.

2. [ ] The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. [ ] **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   [ ] the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   [ ] no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the International Searching Authority European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Authorized officer Victoria Strijdhagen-Namagembe

Date in to SV FF: 3.17.09
Reviewed by: _____ *(See notes on accompanying sheet)*
Sent Out by SV FF on: _____

Form PCT/ISA/220 (October 2005)

NOTES TO FORM PCT/ISA/220

These Notes are intended to give the basic instructions concerning the filing of amendments under article 19. The Notes are based on the requirements of the Patent Cooperation Treaty, the Regulations and the Administrative Instructions under that Treaty. In case of discrepancy between these Notes and those requirements, the latter are applicable. For more detailed information, see also the *PCT Applicant's Guide*, a publication of WIPO.

In these Notes, "Article", "Rule", and "Section" refer to the provisions of the PCT, the PCT Regulations and the PCT Administrative Instructions, respectively.

INSTRUCTIONS CONCERNING AMENDMENTS UNDER ARTICLE 19

The applicant has, after having received the international search report and the written opinion of the International Searching Authority, one opportunity to amend the claims of the international application. It should however be emphasized that, since all parts of the international application (claims,description and drawings) may be amended during the international preliminary examination procedure, there is usually no need to file amendments of the claims under Article 19 except where, e.g. the applicant wants the latter to be published for the purposes of provisional protection or has another reason for amending the claims before international publication. Furthermore, it should be emphasized that provisional protection is available in some States only (see *PCT Applicant's Guide*, Volume I/A, Annexes B1 and B2).

The attention of the applicant is drawn to the fact that amendments to the claims under Article 19 are not allowed where the International Searching Authority has declared, under Article 17(2), that no international search report would be established (see *PCT Applicant's Guide*, Volume I/A, paragraph 296).

What parts of the international application may be amended?

Under Article 19, only the claims may be amended.

During the international phase, the claims may also be amended (or further amended) under Article 34 before the International Preliminary Examining Authority. The description and drawings may only be amended under Article 34 before the International Examining Authority.

Upon entry into the national phase, all parts of the international application may be amended under Article 28 or, where applicable, Article 41.

When?

Within 2 months from the date of transmittal of the international search report or 16 months from the priority date, whichever time limit expires later. It should be noted, however, that the amendments will be considered as having been received on time if they are received by the International Bureau after the expiration of the applicable time limit but before the completion of the technical preparations for international publication (Rule 46.1).

Where not to file the amendments?

The amendments may only be filed with the International Bureau and not with the receiving Office or the International Searching Authority (Rule 46.2).

Where a demand for international preliminary examination has been/is filed, see below.

How?

Either by cancelling one or more entire claims, by adding one or more new claims or by amending the text of one or more of the claims as filed.

A replacement sheet must be submitted for each sheet of the claims which, on account of an amendment or amendments, differs from the sheet originally filed.

All the claims appearing on a replacement sheet must be numbered in Arabic numerals. Where a claim is cancelled, no renumbering of the other claims is required. In all cases where claims are renumbered, they must be renumbered consecutively (Section 205(b)).

The amendments must be made in the language in which the international application is to be published.

What documents must/may accompany the amendments?

Letter (Section 205(b)):

The amendments must be submitted with a letter.

The letter will not be published with the international application and the amended claims. It should not be confused with the "Statement under Article 19(1)" (see below, under "Statement under Article 19(1)").

The letter must be in English or French, at the choice of the applicant. However, if the language of the international application is English, the letter must be in English; if the language of the international application is French, the letter must be in French.

LENOVO EXHIBIT 1002 - 293/502

NOTES TO FORM PCT/ISA/220 (continued)

The letter must indicate the differences between the claims as filed and the claims as amended. It must, in particular, indicate, in connection with each claim appearing in the international application (it being understood that identical indications concerning several claims may be grouped),whether

(i) the claim is unchanged;

(ii) the claim is cancelled;

(iii) the claim is new;

(iv) the claim replaces one or more claims as filed;

(v) the claim is the result of the division of a claim as filed.

The following examples illustrate the manner in which amendments must be explained in the accompanying letter:

1. [Where originally there were 48 claims and after amendment of some claims there are 51]:
"Claims 1 to 29, 31, 32, 34, 35, 37 to 48 replaced by amended claims bearing the same numbers; claims 30, 33 and 36 unchanged; new claims 49 to 51 added."

2. [Where originally there were 15 claims and after amendment of all claims there are 11]:
"Claims 1 to 15 replaced by amended claims 1 to 11."

3. [Where originally there were 14 claims and the amendments consist in cancelling some claims and in adding new claims]:
"Claims 1 to 6 and 14 unchanged; claims 7 to 13 cancelled; new claims 15, 16 and 17 added." or
"Claims 7 to 13 cancelled; new claims 15, 16 and 17 added; all other claims unchanged."

4. [Where various kinds of amendments are made]:
"Claims 1–10 unchanged; claims 11 to 13, 18 and 19 cancelled; claims 14, 15 and 16 replaced by amended claim 14; claim 17 subdivided into amended claims 15, 16 and 17; new claims 20 and 21 added."

"Statement under article 19(1)" (Rule 46.4)

The amendments may be accompanied by a statement explaining the amendments and indicating any impact that such amendments might have on the description and the drawings (which cannot be amended under Article 19(1)).

The statement will be published with the international application and the amended claims.

It must be in the language in which the international application is to be published.

It must be brief, not exceeding 500 words if in English or if translated into English.

It should not be confused with and does not replace the letter indicating the differences between the claims as filed and as amended. It must be filed on a separate sheet and must be identified as such by a heading, preferably by using the words "Statement under Article 19(1)."

It may not contain any disparaging comments on the international search report or the relevance of citations contained in that report. Reference to citations, relevant to a given claim, contained in the international search report may be made only in connection with an amendment of that claim.

Consequence if a demand for international preliminary examination has already been filed

If, at the time of filing any amendments and any accompanying statement, under Article 19, a demand for international preliminary examination has already been submitted, the applicant must preferably, at the time of filing the amendments (and any statement) with the International Bureau, also file with the International Preliminary Examining Authority a copy of such amendments (and of any statement) and, where required, a translation of such amendments for the procedure before that Authority (see Rules 55.3(a) and 62.2, first sentence). For further information, see the Notes to the demand form (PCT/IPEA/401).

If a demand for international preliminary examination is made, the written opinion of the International Searching Authority will, except in certain cases where the International Preliminary Examining Authority did not act as International Searching Authority and where it has notified the International Bureau under Rule 66.1*bis*(b), be considered to be a written opinion of the International Preliminary Examining Authority. If a demand is made, the applicant may submit to the International Preliminary Examining Authority a reply to the written opinion together, where appropriate, with amendments before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later (Rule 43*bis*.1(c)).

Consequence with regard to translation of the international application for entry into the national phase

The applicant's attention is drawn to the fact that, upon entry into the national phase, a translation of the claims as amended under Article 19 may have to be furnished to the designated/elected Offices, instead of, or in addition to, the translation of the claims as filed.

For further details on the requirements of each designated/elected Office, see the *PCT Applicant's Guide,* Volume II.

LENOVO EXHIBIT 1002 - 294/502

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
8029P039PCT		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2008/086879	15/12/2008	04/01/2008
Applicant		
SILICON IMAGE, INC.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language,** the international search was carried out on the basis of:
      [X] the international application in the language in which it was filed
      [ ] a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. [ ] This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. [ ] With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. [ ] **Certain claims were found unsearchable** (See Box No. II)

3. [ ] **Unity of invention is lacking** (see Box No III)

4. With regard to the **title,**
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**
   [X] the text is approved as submitted by the applicant
   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority

6. With regard to the **drawings,**
   a. the figure of the **drawings** to be published with the abstract is Figure No. 8
      [ ] as suggested by the applicant
      [X] as selected by this Authority, because the applicant failed to suggest a figure
      [ ] as selected by this Authority, because this figure better characterizes the invention
   b. [ ] none of the figures is to be published with the abstract

LENOVO EXHIBIT 1002 - 295/502

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/086879

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F3/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/201492 A1 (KOBAYASHI OSAMU [US]) 30 August 2007 (2007-08-30) paragraphs [0090], [0093], [0115]; figures 18,19,30	1-30

[ ] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 March 2009	13/03/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Le Chapelain, B

Form PCT/ISA/210 (second sheet) (April 2005)

LENOVO EXHIBIT 1002 - 296/502

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2008/086879

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007201492 A1	30-08-2007	CN 101295493 A	29-10-2008
		EP 1986183 A1	29-10-2008
		JP 2008278488 A	13-11-2008
		KR 20080096401 A	30-10-2008
		SG 147380 A1	28-11-2008

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2008/086879	15.12.2008	04.01.2008

International Patent Classification (IPC) or both national classification and IPC
INV. G06F3/14

Applicant
SILICON IMAGE, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☒ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA:	Date of completion of this opinion	Authorized Officer
European Patent Office - P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Tx: 31 651 epo nl Fax. +31 70 340 - 3016	see form PCT/ISA/210	Le Chapelain, B Telephone No. +31 70 340-9545

Form PCT/ISA/237 (Cover Sheet) (April 2005)

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material:

      ☐ a sequence listing

      ☐ table(s) related to the sequence listing

   b. format of material:

      ☐ on paper

      ☐ in electronic form

   c. time of filing/furnishing:

      ☐ contained in the international application as filed.

      ☐ filed together with the international application in electronic form.

      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Box No. II Priority

1. ☒ The validity of the priority claim has not been considered because the International Searching Authority does not have in its possession a copy of the earlier application whose priority has been claimed or, where required, a translation of that earlier application. This opinion has nevertheless been established on the assumption that the relevant date (Rules 43*bis*.1 and 64.1) is the claimed priority date.

2. ☐ This opinion has been established as if no priority had been claimed due to the fact that the priority claim has been found invalid (Rules 43*bis*.1 and 64.1). Thus for the purposes of this opinion, the international filing date indicated above is considered to be the relevant date.

3. Additional observations, if necessary:

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	5,14,15,17,18,24,25,26-30
	No:	Claims	1-4,6,7,8,9,10,11,12,13,18,16,19,20,22,23,26-30
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-30
Industrial applicability (IA)	Yes:	Claims	1-30
	No:	Claims	

2. Citations and explanations

see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

Reference is made to the following document:

D1: US 2007/201492 A1 (KOBAYASHI OSAMU [US]) 30 August 2007 (2007-08-30)

1 LACK OF NOVELTY

The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claims 1-4 is not new in the sense of Article 33(2) PCT.

1.1 CLAIM 1

The document D1 discloses (the references in parentheses applying to this document):
A method comprising:
connecting a receiving device to a cable (fig. 30: 3004, 3006), the cable including a control bus (fig. 30: 3014);
if the receiving device is in a disconnect state and a signal from a transmitting device is detected on the control bus, transferring the device to a state for a first type of transmitting device (par . 93, fig. 18,19: if no activity then standby and idle else if voltage drop on auxiliary channel detected then normal operation); and
if the receiving device is in either the disconnect state or the state for the first type of transmitting device and a predetermined voltage signal is received from the transmitting device, then transferring the receiving device to a state for a second type of transmitting device (par. 115: if USB request then holding any display 3004 requests and then execute).
The subject-matter of claim 1 is therefore known from D1.

1.2 CLAIMS 2 and 3

The document D1 further discloses the voltage on the power bus is no longer detected, transferring the device from the state for the first type of transmitting device or the state for the second type of transmitting device to the disconnect state (fig. 19: if no activity on

auxiliary channel then go to standby; par. 90: power saving with auxiliary channel periodically pulsed).
The subject-matter of claims 2 and 3 is therefore known from D1.

1.3 CLAIM 4
The document D1 further discloses the first type of device is a device compatible with a protocol (display port standard protocol), and the second type of device is a mobile device compatible with a modified protocol (USB protocol).

2 LACK OF INVENTIVE STEP
The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claim 5 does not involve an inventive step in the sense of Article 33(3) PCT.

2.1 CLAIM 5
Document D1 doesn't discloses the protocol is HDMI (High-Definition Multimedia Interface) but it is known by the person skilled in the art that HDMI interface could be emulated externally or internally (encapsulated) with a display port interface.
The subject-matter of claim 5 is therefore obvious in the light of D1.

3 CLAIMS 6-30
The subject-matter of claims 11-26 refers to transmitting device and a receiving device and method for emitting and receiving audio and video data and substantially correspond to the subject-matter of claims 1-5. The reasoning given in par. 1-2.1 above therefore applies to claims 6-30 accordingly.
The subject-matter of 6-30 is therefore obvious/known from D1.

Possible steps after receipt of the international search report (ISR) and written opinion of the International Searching Authority (WO-ISA)

General information	For all international applications filed on or after 01/01/2004 the competent ISA will establish an ISR. It is accompanied by the WO-ISA. Unlike the former written opinion of the IPEA (Rule 66.2 PCT), the WO-ISA is not meant to be responded to, but to be taken into consideration for further procedural steps. This document explains about the possibilities.
Amending claims under Art. 19 PCT	Within 2 months after the date of mailing of the ISR and the WO-ISA the applicant may file amended claims under Art. 19 PCT directly with the International Bureau of WIPO. The PCT reform of 2004 did not change this procedure. For further information please see Rule 46 PCT as well as form PCT/ISA/220 and the corresponding Notes to form PCT/ISA/220.
Filing a demand for international preliminary examination	In principle, the WO-ISA will be considered as the written opinion of the IPEA. This should, in many cases, make it unnecessary to file a demand for international preliminary examination. If the applicant nevertheless wishes to file a demand this must be done before expiry of 3 months after the date of mailing of the ISR/WO-ISA or 22 months after priority date, whichever expires later (Rule 54bis PCT). Amendments under Art. 34 PCT can be filed with the IPEA as before, normally at the same time as filing the demand (Rule 66.1 (b) PCT). If a demand for international preliminary examination is filed and no comments/amendments have been received the WO-ISA will be transformed by the IPEA into an IPRP (International Preliminary Report on Patentability) which would merely reflect the content of the WO-ISA. The demand can still be withdrawn (Art. 37 PCT).
Filing informal comments	After receipt of the ISR/WO-ISA the applicant may file informal comments on the WO-ISA directly with the International Bureau of WIPO. These will be communicated to the designated Offices together with the IPRP (International Preliminary Report on Patentability) at 30 months from the priority date. Please also refer to the next box.
End of the international phase	At the end of the international phase the International Bureau of WIPO will transform the WO-ISA or, if a demand was filed, the written opinion of the IPEA into the IPRP, which will then be transmitted together with possible informal comments to the designated Offices. The IPRP replaces the former IPER (international preliminary examination report).
Relevant PCT Rules and more information	Rule 43 PCT, Rule 43bis PCT, Rule 44 PCT, Rule 44bis PCT, PCT Newsletter 12/2003, OJ 11/2003, OJ 12/2003

3NSDOCID: <XS_____200704010CK_I_>

Electronic Patent Application Fee Transmittal

Application Number:	11969852
Filing Date:	04-Jan-2008
Title of Invention:	CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Shrikant Ranade
Filer:	Mark C. Van Ness/Lisa Riley
Attorney Docket Number:	8029P038

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
		Total in USD ($)		**810**

Electronic Acknowledgement Receipt

EFS ID:	7975814
Application Number:	11969852
International Application Number:	
Confirmation Number:	1782
Title of Invention:	CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Shrikant Ranade
Correspondence Address:	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP - SEVENTH FLOOR 12400 WILSHIRE BOULEVARD LOS ANGELES CA 90025-1026 US 503 439 8778 -
Filer:	Mark C. Van Ness/Lisa Riley
Filer Authorized By:	Mark C. Van Ness
Attorney Docket Number:	8029P038
Receipt Date:	08-JUL-2010
Filing Date:	04-JAN-2008
Time Stamp:	18:57:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$810

RAM confirmation Number	7229
Deposit Account	022666
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	8029P038_RCE.pdf	44980 f5e503c2c7190f557bba814122b14c43291f4a4c	no	1
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
2	Amendment Submitted/Entered with Filing of CPA/RCE	SIMG0335_8029P038_Amendment_with_RCE.pdf	50600 0b9f617ba97450c7dd1e26def99d3c882e8c06ae	no	11
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Filed (SB/08)	SIMG0335_8029P038_IDS_filed_7-8-10.pdf	64180 2b4a5027d0c1cb18f531983bc0cef19d73c30453	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
4	Foreign Reference	EP1519581.pdf	1114629 ec25067514e6c80833b0e5008ac28e5f30f84200	no	12
Warnings:					
Information:					
5	NPL Documents	SIMG0336_80229P039_OA_mailed_10-28-09.pdf	3410221 87c7ef696fd87e1a3b071750291016edf87572c8	no	15
Warnings:					
Information:					
6	NPL Documents	SIMG0336_8029P039_NALL_mailed_5-11-10.pdf	3643096 63f453d42f158862dd54cb275bd6062eac1f6890	no	23
Warnings:					
Information:					
7	NPL Documents	8029P037PCT_ISRWO_mailed_3-25-09.pdf	1445264 b43c31158d518232a9f9f65a8ef81bea57ea29f5	no	16
Warnings:					
Information:					

8	NPL Documents	8029P039PCT_ISRWO_mailed_3-13-09.pdf	1161158 279816fb0aca218ba4636ad2c8370fb625983550	no	12
Warnings:					
Information:					
9	NPL Documents	High_Definition_Multimedia_Interface_Specification_V_1_3.pdf	15477480 31ca716e73b2187293840d8bac853ecc619c0f84	no	237
Warnings:					
Information:					
10	NPL Documents	High-Definition_Multimedia_Interface_Spec_Ver_1-3a_11-10-06.pdf	473772 b53f02ae76d1b21d94f1bd17bc08a7409d772906	no	2
Warnings:					
Information:					
11	NPL Documents	On-The-Go_Supplement_to_the_USB_2-0_Specification_Rev1-0_12-18-01.pdf	2619131 1f327ff08209e2de6ac9d78915e5e1c1bd22dde9	no	10
Warnings:					
Information:					
12	Fee Worksheet (PTO-875)	fee-info.pdf	30379 a60e202b3c1386537a8a45b980f38ab0dd8c027c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	29534890		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/969,852	01/04/2008	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 07/08/2010

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 25	Minus	** 28	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/EFREM WARREN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 07/12/2010

EWARREN SALE #00000001 Mailroom Dt: 07/08/2010 022666 11969852
01 FC : 1801 810.00 DA

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 08/13/2010

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025-1026

EXAMINER	
CLEARY, THOMAS J	
ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 08/13/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/969,852	01/04/2008	Shrikant Ranade	8029P038	1782

TITLE OF INVENTION: CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	11/15/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

LENOVO EXHIBIT 1002 - 311/502

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 08/13/2010

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025-1026

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/969,852	01/04/2008	Shrikant Ranade	8029P038	1782

TITLE OF INVENTION: CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	11/15/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
CLEARY, THOMAS J	2111	710-106000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1_____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2_____ 3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

LENOVO EXHIBIT 1002 - 312/502

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/969,852	01/04/2008	Shrikant Ranade	8029P038	1782

7590 08/13/2010

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025-1026

EXAMINER	
CLEARY, THOMAS J	
ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 08/13/2010

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 201 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 201 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

LENOVO EXHIBIT 1002 - 313/502

Notice of Allowability	Application No.	Applicant(s)	
	11/969,852	RANADE ET AL.	
	Examiner	Art Unit	
	THOMAS J. CLEARY	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *8 July 2010*.

2. ☒ The allowed claim(s) is/are *1-5,7-9,11-14,17-22 and 25-31*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 20100708
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Thomas J. Cleary/
Primary Examiner, Art Unit 2111

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 8 July 2010 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Allowable Subject Matter

2. Claims 1-5, 7-9, 11-14, 17-22, and 25-31 are allowed.

3. The following is an examiner's statement of reasons for allowance: The claims are allowable for the reasons previously indicated.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to THOMAS J. CLEARY whose telephone number is (571)272-3624. The examiner can normally be reached on Monday-Thursday (7-3).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thomas J. Cleary/
Primary Examiner, Art Unit 2111

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	11/969,852	RANADE ET AL.	
	Examiner	Art Unit	
	THOMAS J. CLEARY	2111	

SEARCHED			
Class	Subclass	Date	Examiner

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
710	**105-107**	7/9/2010	**TJC**
710	119	7/9/2010	TJC

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
Attached EAST BRS	7/8/2010	TJC
Updated Previous Search	7/8/2010	TJC

Issue Classification

Application/Control No.	Applicant(s)/Patent Under Reexamination
11969852	RANADE ET AL.
Examiner	**Art Unit**
THOMAS J CLEARY	2111

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
710	106	G 0 6 F 13 / 42 (2006.0)	
CROSS REFERENCE(S)		G 0 6 F 13 / 00 (2006.0)	
		G 0 6 F 13 / 368 (2006.0)	

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
710	105	107	119		

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	16	17												
2	2	17	18												
3	3	19	19												
4	4	20	20												
5	5	21	21												
	6	22	22												
6	7		23												
7	8		24												
8	9	23	25												
	10	24	26												
12	11	9	27												
13	12	10	28												
14	13	11	29												
15	14	18	30												
	15	25	31												
	16														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	25	
/THOMAS J CLEARY/ Primary Examiner.Art Unit 2111	7/9/2010	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11969852	RANADE ET AL.
	Examiner	Art Unit
	THOMAS J CLEARY	2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/23/2009	04/05/2010	07/09/2010						
1	1	✓	=	=						
2	2	✓	=	=						
3	3	✓	=	=						
4	4	✓	=	=						
5	5	✓	=	=						
	6	✓	-	-						
6	7	✓	=	=						
7	8	✓	=	=						
8	9	✓	=	=						
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24	26	✓	=	=						
9	27		=	=						
10	28		=	=						
11	29		=	=						
18	30		=	=						
25	31		=	=						

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	6	("20070083692" "20070201492" "20070279408").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 11:19
L4	4	("20070286246" "7187307").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L5	68	(((single adj (wire line bit)) single-wire single-line single-bit) near2 bus with (bidirectional bi-directional "bi directional")) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L6	154	(lee.in. and dallas.as.) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L7	124	(((one adj (wire line bit)) one-wire one-line one-bit) near2 bus with (bidirectional bi-directional "bi directional")) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L8	2	"5045675".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L9	2	"5729547".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11

LENOVO EXHIBIT 1002 - 320/502

L10	28	kraemer-rolf.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L11	2	"20070073449".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L12	1	WO2005/015817	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L13	36	(((single adj (wire line bit)) single-wire single-line single-bit) near2 bus same arbitrat$3) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L14	2	((1-wire "1 wire" 1wire) near2 bus same arbitrat $3) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L15	2	"7181557".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L16	39	((1-wire "1 wire" 1wire) near2 bus same reset$4) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L17	35	(((single adj (wire line bit)) single-wire single-line single-bit) near2 bus same reset$4) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11

LENOVO EXHIBIT 1002 - 321/502

L18	73	L16 L17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L19	17	("5210846" | "5237322" | "5636342" | "5655132" | "5758282" | "5761697" | "5809518" | "5936520" | "6108751" | "6112275" | "6239732" | "6298066" | "6941451").PN. OR ("7181557").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/07/09 14:11
L20	2	"5054299".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L21	2	"20090177820".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L22	2	"20090177818".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L23	7	"10726794"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L24	2	"20040218599".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L25	0	(hdmi-m) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11

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L26	0	("dual mode" with hdmi) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L27	0	("dual-mode" with hdmi) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L28	0	("multi-mode" with hdmi) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L29	0	("multi mode" with hdmi) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L30	1	("mini hdmi") and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L31	5	(usb-otg.ti.) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L32	300	(ranade-shri$ peysakhovich-ale$ lee-hyuck$ choi-hoon$).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L33	36	(((single adj (wire line bit)) single-wire single-line single-bit) near2 bus same (arbitrat$4)) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11

LENOVO EXHIBIT 1002 - 323/502

L34	3	"4063220".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L35	0	(switch$4 near3 (pulldown pull-down "pull down") same ("1850" j1850)) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L36	2434	(switch$4 near3 (pulldown pull-down "pull down")) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L37	850	(switch$4 near (pulldown pull-down "pull down")) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L38	22	(switch$4 near3 (pulldown pull-down "pull down") and ("1850" j1850)) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L39	4	("20070286246" "7187307").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L40	68	(((single adj (wire line bit)) single-wire single-line single-bit) near2 bus with (bidirectional bi-directional "bi directional")) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L41	154	(lee.in. and dallas.as.) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11

LENOVO EXHIBIT 1002 - 324/502

L42	124	(((one adj (wire line bit)) one-wire one-line one-bit) near2 bus with (bidirectional bi-directional "bi directional")) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L43	2	"5045675".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L44	2	"5729547".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L45	28	kraemer-rolf.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L46	2	"20070073449".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L47	1	WO2005/015817	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L48	36	(((single adj (wire line bit)) single-wire single-line single-bit) near2 bus same arbitrat$3) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L49	2	((1-wire "1 wire" 1wire) near2 bus same arbitrat $3) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11

LENOVO EXHIBIT 1002 - 325/502

L50	2	"7181557".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L51	39	((1-wire "1 wire" 1wire) near2 bus same reset$4) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L52	35	(((single adj (wire line bit)) single-wire single-line single-bit) near2 bus same reset$4) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L53	73	L16 L17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L54	17	("5210846" | "5237322" | "5636342" | "5655132" | "5758282" | "5761697" | "5809518" | "5936520" | "6108751" | "6112275" | "6239732" | "6298066" | "6941451").PN. OR ("7181557").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/07/09 14:11
L55	2	"5054299".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L56	2	"20090177820".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L57	2	"20090177818".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11

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L58	7	"10726794"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L59	2	"20040218599".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L60	0	(hdmi-m) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L61	0	("dual mode" with hdmi) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L62	0	("dual-mode" with hdmi) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L63	0	("multi-mode" with hdmi) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L64	0	("multi mode" with hdmi) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L65	1	("mini hdmi") and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11

LENOVO EXHIBIT 1002 - 327/502

L66	5	(usb-otg.ti.) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L67	300	(ranade-shri$ peysakhovich-ale$ lee-hyuck$ choi-hoon$).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L68	36	(((single adj (wire line bit)) single-wire single-line single-bit) near2 bus same (arbitrat$4)) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L69	3	"4063220".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L70	0	(switch$4 near3 (pulldown pull-down "pull down") same ("1850" j1850)) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L71	2434	(switch$4 near3 (pulldown pull-down "pull down")) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L72	850	(switch$4 near (pulldown pull-down "pull down")) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11
L73	22	(switch$4 near3 (pulldown pull-down "pull down") and ("1850" j1850)) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/07/09 14:11

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S1	4	("20070286246" "7187307").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/16 08:33
S2	67	(((single adj (wire line bit)) single-wire single-line single-bit) near2 bus with (bidirectional bi-directional "bi directional")) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 08:22
S3	152	(lee.in. and dallas.as.) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 09:21
S4	121	(((one adj (wire line bit)) one-wire one-line one-bit) near2 bus with (bidirectional bi-directional "bi directional")) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 09:52
S5	2	"5045675".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 10:19
S6	2	"5729547".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 10:19
S7	28	kraemer-rolf.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 10:46
S8	2	"20070073449".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 10:46

LENOVO EXHIBIT 1002 - 329/502

S9	1	WO2005/015817	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 10:46
S10	36	(((single adj (wire line bit)) single-wire single-line single-bit) near2 bus same arbitrat$3) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/21 10:56
S11	2	((1-wire "1 wire" 1wire) near2 bus same arbitrat $3) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 09:57
S12	2	"7181557".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:22
S13	38	((1-wire "1 wire" 1wire) near2 bus same reset$4) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:23
S14	30	(((single adj (wire line bit)) single-wire single-line single-bit) near2 bus same reset$4) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:24
S15	67	S13 S14	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 10:24
S16	13	("5210846" | "5237322" | "5636342" | "5655132" | "5758282" | "5761697" | "5809518" | "5936520" | "6108751" | "6112275" | "6239732" | "6298066" | "6941451").PN. OR ("7181557").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/09/22 10:26

LENOVO EXHIBIT 1002 - 330/502

S17	2	"5054299".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 13:27
S18	2	"20090177820".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 22:24
S19	2	"20090177818".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 22:25
S20	7	"10726794"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 22:41
S21	2	"20040218599".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 22:42
S22	0	(hdmi-m) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 23:39
S23	0	("dual mode" with hdmi) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 23:48
S24	0	("dual-mode" with hdmi) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 23:48

LENOVO EXHIBIT 1002 - 331/502

S25	0	("multi-mode" with hdmi) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 23:49
S26	0	("multi mode" with hdmi) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/22 23:50
S27	1	("mini hdmi") and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/23 00:09
S28	5	(usb-otg.ti.) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/23 00:42
S29	263	(ranade-shri$ peysakhovich-ale$ lee-hyuck$ choi-hoon$).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/23 10:05
S30	36	(((single adj (wire line bit)) single-wire single-line single-bit) near2 bus same (arbitrat$4)) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/30 14:29
S31	3	"4063220".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/31 11:04
S32	0	(switch$4 near3 (pulldown pull-down "pull down") same ("1850" j1850)) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/01 09:55

LENOVO EXHIBIT 1002 - 332/502

S33	2405	(switch$4 near3 (pulldown pull-down "pull down")) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/01 09:55
S34	839	(switch$4 near (pulldown pull-down "pull down")) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/01 09:56
S35	22	(switch$4 near3 (pulldown pull-down "pull down") and ("1850" j1850)) and @ad<"20080104"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/01 09:56

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L74	856	710/105.ccls.	USPAT; UPAD	OR	ON	2010/07/09 14:12
L75	392	710/106.ccls.	USPAT; UPAD	OR	ON	2010/07/09 14:12
L76	1206	710/107.ccls.	USPAT; UPAD	OR	ON	2010/07/09 14:12
L77	200	710/119.ccls.	USPAT; UPAD	OR	ON	2010/07/09 14:12

7/9/10 2:26:23 PM
C:\Documents and Settings\tcleary\My Documents\EAST\Workspaces\11969852.wsp

LENOVO EXHIBIT 1002 - 333/502

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	11/969,852
	Filing Date	January 4, 2008
	First Named Inventor	Ranade, Shrikant
	Group Art Unit	2111
	Examiner Name	Cleary, Thomas
Sheet 1 of 1	Attorney Docket No: 8029P038	

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**
		US-20070083692	04/12/2007	LIU, H. S. et al.	
		US-20070201492	08/30/2007	KOBAYASHI, Osamu	
		US-20070279408	12/06/2007	ZHENG, Dong et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	**Cite No [1]**	**Foreign Patent Document** Country Code/Number/Kind Code (if known)	**Publication Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	**T [2]**
		EP-1519581	03/30/2005	GENESIS MICROCHIP, INC.,		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T [2]**
		USPTO, Non-Final Office Action for U.S. Patent Application No 11/969,865 (Attorney Docket No 8029P039) mailed October 28, 2009	
		USPTO, Notice of Allowance for US Patent Application No. 11/969,865 (Attorney Docket No. 8029P039) mailed May 11, 2010	
		"8029P037PCT ISR and WO Mailed 3/25/2009 for PCT/US2008/085287", Whole Document	
		"8029P039PCT ISR and WO Mailed 3/13/2009 for PCT/US2008/086879", Whole Document	
		"High-Definition Multimedia Interface Specification Version 1.3", Internet Citation XP002391813 - http://www.hdmi.org/download/HDMI_Spec_1.3_GMI.pdf, (retrieved on 7/26/2006), Whole Document	
		"High-Definition Multimedia Interface Specification Version 1.3a", November 10, 2006, cover page and page 1 of 156 pages only	
		"On-The-Go Supplement to the USB 2.0 Specification Revision 1.0", December 18, 2001; cover page, pages 1, 37-41, and 47-49	

EXAMINER /Thomas J. Cleary/ **DATE CONSIDERED** 07/09/2010

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /TJC/

Our Docket No: 8029P038

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Shrikant Ranade et al.	Examiner: Thomas J. Cleary
Application No: 11/969,852	Art Unit: 2111
Filed: January 4, 2008	Conf. No: 1782
For: CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES	

REQUEST FOR REFUND

Sir or Madam:

Applicants request a refund to Deposit Account No. 02-2666 in the amount of $810.00 for the fee charged to the account by the USPTO for the Request for Continued Examination filed on July 8, 2010. Applicants submitted the required fee in the amount of $810.00 via Deposit Account No. 02-2666 on July 8, 2010 as shown on the Electronic Acknowledgement Receipt, EFS ID 7975815 (submitted herewith as Exhibit A). A duplicate fee was subsequently charged to Deposit Account No. 02-2666 on July 12, 2010 as shown on the USPTO Sales Receipt for Accounting dated July 12, 2010 (submitted herewith as Attachment B).

LENOVO EXHIBIT 1002 - 335/502

The $810.00 fee required for the Request for Continued Examination filed by the Applicants on July 8, 2010 was duly paid at the time of filing and the fee subsequently charged on July 12, 2010 is due to a USPTO error. Therefore, a credit to Deposit Account No. 02-2666 in the amount of $810.00 should be granted.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Date: August 17, 2010

/Mark C. Van Ness/
Mark C. VanNess
Reg. No. 39,865

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(503) 439-8778

CERTIFICATE OF MAILING/TRANSMISSION
I hereby certify that this correspondence is being submitted electronically via EFS Web prior to 11:59 PM on the date shown below.

/Lisa Riley/ August 17, 2010
Lisa Riley Date

LENOVO EXHIBIT 1002 - 336/502

Electronic Acknowledgement Receipt

EFS ID:	7975814
Application Number:	11969852
International Application Number:	
Confirmation Number:	1782
Title of Invention:	CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Shrikant Ranade
Correspondence Address:	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP - SEVENTH FLOOR 12400 WILSHIRE BOULEVARD LOS ANGELES CA 90025-1026 US 503 439 8778 -
Filer:	Mark C. Van Ness/Lisa Riley
Filer Authorized By:	Mark C. Van Ness
Attorney Docket Number:	8029P038
Receipt Date:	08-JUL-2010
Filing Date:	04-JAN-2008
Time Stamp:	18:57:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$810

LENOVO EXHIBIT 1002 - 337/502

RAM confirmation Number	7229
Deposit Account	022666
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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This is not a USPTO supplied RCE SB30 form.					
Information:					
2	Amendment Submitted/Entered with Filing of CPA/RCE	SIMG0335_8029P038_Amendment_with_RCE.pdf	50600 0b9f617ba97450c7dd1e26def99d3c882e8c06ae	no	11
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Information:					
3	Information Disclosure Statement (IDS) Filed (SB/08)	SIMG0335_8029P038_IDS_filed_7-8-10.pdf	64180 2b4a5027d0c1cb18f531983bc0cef19d73c30453	no	2
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Information:					
6	NPL Documents	SIMG0336_8029P039_NALL_mailed_5-11-10.pdf	3643096 63f453d42f158862dd54cb275bd6062eac1f6890	no	23
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Information:					

LENOVO EXHIBIT 1002 - 338/502

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Information:					
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Warnings:					
Information:					
		Total Files Size (in bytes):	29534890		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

LENOVO EXHIBIT 1002 - 339/502

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 07/12/2010

EWARREN SALE #00000001 Mailroom Dt: 07/08/2010 022666 11969852
01 FC : 1801 810.00 DA

EXHIBIT B
Page 1 of 1

Electronic Acknowledgement Receipt

EFS ID:	8235421
Application Number:	11969852
International Application Number:	
Confirmation Number:	1782
Title of Invention:	CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Shrikant Ranade
Correspondence Address:	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP - SEVENTH FLOOR 12400 WILSHIRE BOULEVARD LOS ANGELES CA 90025-1026 US 503 439 8778 -
Filer:	Mark C. Van Ness/Lisa Riley
Filer Authorized By:	Mark C. Van Ness
Attorney Docket Number:	8029P038
Receipt Date:	17-AUG-2010
Filing Date:	04-JAN-2008
Time Stamp:	15:55:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Refund Request	SIMG0335_8029P038_Request_for_Refund_8-17-10.pdf	234202 06bc4c8a78d4b3047f5156c4de4697cc131b5f38	no	6

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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

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2010 AUG 18 AM 11:14

Our Docket No: 8029P038

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Shrikant Ranade et al.	Examiner: Thomas J. Cleary
Application No: 11/969,852	Art Unit: 2111
Filed: January 4, 2008	Conf. No: 1782
For: CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES	

REQUEST FOR REFUND

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LENOVO EXHIBIT 1002 - 343/502

The $810.00 fee required for the Request for Continued Examination filed by the Applicants on July 8, 2010 was duly paid at the time of filing and the fee subsequently charged on July 12, 2010 is due to a USPTO error. Therefore, a credit to Deposit Account No. 02-2666 in the amount of $810.00 should be granted.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Date: August 17, 2010

/Mark C. Van Ness/
Mark C. Van Ness
Reg. No. 39,865

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(503) 439-8778

CERTIFICATE OF MAILING/TRANSMISSION
I hereby certify that this correspondence is being submitted electronically via EFS Web prior to 11:59 PM on the date shown below.

/Lisa Riley/ August 17, 2010
Lisa Riley Date

LENOVO EXHIBIT 1002 - 344/502

Electronic Acknowledgement Receipt

EFS ID:	7975814
Application Number:	11969852
International Application Number:	
Confirmation Number:	1782
Title of Invention:	CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Shrikant Ranade
Correspondence Address:	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP - SEVENTH FLOOR 12400 WILSHIRE BOULEVARD LOS ANGELES CA 90025-1026 US 503 439 8778 -
Filer:	Mark C. Van Ness/Lisa Riley
Filer Authorized By:	Mark C. Van Ness
Attorney Docket Number:	8029P038
Receipt Date:	08-JUL-2010
Filing Date:	04-JAN-2008
Time Stamp:	18:57:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$810

LENOVO EXHIBIT 1002 - 345/502

RAM confirmation Number	7229
Deposit Account	022666
Authorized User	

File Listing:

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Information:					
2	Amendment Submitted/Entered with Filing of CPA/RCE	SIMG0335_8029P038_Amendment_with_RCE.pdf	50600 0b9f617ba97450c7dd1e26def99d3c882e6 c06ae	no	11
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Information:					
3	Information Disclosure Statement (IDS) Filed (SB/08)	SIMG0335_8029P038_IDS_filed_7-8-10.pdf	64180 2b4a5027d0c1cb18531983bc0cef19d73c3 0453	no	2
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4	Foreign Reference	EP1519581.pdf	1114629 ec25067514e6c80833b0a5008ac28e5f30f8 4200	no	12
Warnings:					
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5	NPL Documents	SIMG0336_80229P039_OA_mailed_10-28-09.pdf	3410221 87c7eb696dd87e1a3b071750291016ed8f5 72c8	no	15
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Information:					

LENOVO EXHIBIT 1002 - 346/502

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Information:					
9	NPL Documents	High_Definition_Multimedia_Interface_Specification_V_1_3.pdf	15477480 31ca716e73b2187293840d8bacd53ecc619 c0f84	no	237
Warnings:					
Information:					
10	NPL Documents	High-Definition_Multimedia_Interface_Spec_Ver_1-3a_11-10-06.pdf	473772 b53f02ae76d1b21d94f1bd17bc08a7409d7 72906	no	2
Warnings:					
Information:					
11	NPL Documents	On-The-Go_Supplement_to_the_USB_2-0_Specification_Rev1-0_12-18-01.pdf	2619131 1f327ff082d9e2de6ac9d78915e5e1c1bd22 dde9	no	10
Warnings:					
Information:					
12	Fee Worksheet (PTO-875)	fee-info.pdf	30379 a60e202b3c13865337a8a45b980f38ab0dd8 c027c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	29534890		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
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LENOVO EXHIBIT 1002 - 347/502

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 07/12/2010

EWARREN SALE #00000001 Mailroom Dt: 07/08/2010 022666 11969852
01 FC : 1801 810.00 DA

Adjustment date: 08/24/2010 HDESTA1
07712/2010 EWARREN 00000001 022666 11969852
01 FC:1801 810.00 CR

EXHIBIT B
Page 1 of 1

PTO/SB/47 (03-09)
Approved for use through 03/31/2012. OMB 0651-0016
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"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

- OR -

Fax to:
571-273-6500

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below**: If you have a Customer Number to represent the fee address. **When to check the second box below**: If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☑ Customer Number: 55167

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	11/969,852

Completed by (check one):

☐ Applicant/Inventor — /Mark C. Van Ness/ (Signature)

☑ Attorney or Agent of record 39,865 (Reg. No.) — Mark C. Van Ness (Typed or printed name)

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96) — 503-439-8778 (Requester's telephone number)

☐ Assignee recorded at Reel _____ Frame_____ — November 8, 2010 (Date)

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

☐ *** Total of _____forms are submitted.**

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1. 11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313- 1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Our Docket No: 8029P038

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Shrikant Ranade	Examiner: Thomas J. Cleary
Application No: 11/969,852	Art Unit: 2111
Filed: January 4, 2008	Conf. No.: 1782
For: CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES	

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE
(Pursuant to 37 CFR 1.104 (e))

Sir or Madam:

Applicant hereby provides comments on the statement of reasons for allowance in this matter.

CERTIFICATE OF TRANSMISSION
This correspondence is being submitted electronically via EFS Web prior to 11:59pm on the date shown below.

Date: November 8, 2010 */Lisa Riley/*
Lisa Riley

LENOVO EXHIBIT 1002 - 351/502

As an initial matter, the undersigned would like to thank the Examiner for the Examiner's thorough review of the above-captioned application and the allowance of claims 1-5, 7-9, 11-14, 17-22 and 25-31 in the Notice of Allowability, mailed August 13, 2010.

With regard to the Notice of Allowability, the undersigned submits herein a statement commenting on the reasons for allowance and respectfully requests that such statement be made of record.

Statement Commenting on the Reasons for Allowance

The Examiner, in the Examiner's statement of reasons for allowance, may have referenced paraphrased limitations from certain of the allowed claims. To clarify the record for anyone who may later view the file wrapper in this application, the undersigned would like to emphasize that each claim should not be construed to include the limitations listed by the Examiner in the reasons for allowance. Rather, each claim should be construed to include only those limitations explicitly recited in the language of the claim.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: November 8, 2010

/Mark C. Van Ness/
Mark C. Van Ness
Reg. No. 39,865

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(503) 439-8778

LENOVO EXHIBIT 1002 - 352/502

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 08/13/2010

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025-1026

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
This correspondence is being submitted electronically via EFS Web prior to 11:59pm on the date shown below.

Lisa Riley	(Depositor's name)
/Lisa Riley/	(Signature)
November 8, 2010	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/969,852	01/04/2008	Shrikant Ranade	8029P038	1782

TITLE OF INVENTION: CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	11/15/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
CLEARY, THOMAS J	2111	710-106000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Blakely Sokoloff Taylor & Zafman
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Silicon Image, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Sunnyvale, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 02-2666 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Mark C. Van Ness/ Date November 8, 2010

Typed or printed name Mark C. Van Ness Registration No. 39,865

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Our Docket No: 8029P038

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Shrikant Ranade et al.	Examiner: Cleary, Thomas J.
Application No: 11/969,852	Art Unit: 2111
Filed: January 4, 2008	Conf. No: 1782
For: CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES	

INFORMATION DISCLOSURE STATEMENT AFTER ALLOWANCE

In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted on or before payment of the Issue Fee. It is respectfully requested that the cited reference be placed in the file wrapper.

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Date: November 8, 2010

/Mark C. Van Ness/
Mark C. Van Ness
Reg. No. 39,865

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(503) 439-8778

CERTIFICATE OF TRANSMISSION
This correspondence is being submitted electronically via EFS Web prior to 11:59pm on the date shown below.

Date: November 8, 2010 */Lisa Riley/*
Lisa Riley

LENOVO EXHIBIT 1002 - 354/502

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	11/969,852
	Filing Date	January 4, 2008
	First Named Inventor	Ranade, Shrikant
	Group Art Unit	2111
	Examiner Name	Cleary, Thomas
Sheet 1 of 1	Attorney Docket No: 8029P038	

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	**Cite No [1]**	**Foreign Patent Document** Country Code/Number/Kind Code (if known)	**Publication Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	**T [2]**

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T [2]**
		International Bureau, International Preliminary Report on Patentability for International Application No. PCT/US2008/085288 (Attorney Docket No. 8029P038PCT) mailed July 15, 2010	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

PATENT COOPERATION TREATY

ADVANCE E-MAIL

PCT

From the INTERNATIONAL BUREAU

NOTIFICATION CONCERNING TRANSMITTAL OF COPY OF INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY (CHAPTER I OF THE PATENT COOPERATION TREATY)
(PCT Rule 44bis.1(c))

To:

VINCENT, Lester, J.
Blakely, Sokoloff, Taylor & Zafman LLP
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
ETATS-UNIS D'AMERIQUE

PCT/AU/ISA/220

JUL 26 2010

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
SUNNYVALE INTL FILING DEPT

Date of mailing *(day/month/year)*	
15 July 2010 (15.07.2010)	
Applicant's or agent's file reference	IMPORTANT NOTICE
8029P038PCT	

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2008/085288	02 December 2008 (02.12.2008)	04 January 2008 (04.01.2008)

Applicant: SILICON IMAGE, INC. et al

The International Bureau transmits herewith a copy of the international preliminary report on patentability (Chapter I of the Patent Cooperation Treaty)

RECEIVED
AUG 02 2010
BEAVERTON

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. +41 22 338 82 70

Authorized officer: Nora Lindner

e-mail: pt11.pct@wipo.int

Entered into NP
By: mtd

LENOVO EXHIBIT 1002 - 356/502

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44*bis*)

Applicant's or agent's file reference 8029P038PCT	**FOR FURTHER ACTION**	See item 4 below
International application No. PCT/US2008/085288	International filing date *(day/month/year)* 02 December 2008 (02.12.2008)	Priority date *(day/month/year)* 04 January 2008 (04.01.2008)
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant SILICON IMAGE, INC.		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 *bis*.1(a).

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☒	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44*bis*.3(c) and 93*bis*.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44*bis* .2).

	Date of issuance of this report 06 July 2010 (06.07.2010)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 338 82 70	Authorized officer Nora Lindner e-mail: pt11.pct@wipo.int

Form PCT/IB/373 (January 2004)

LENOVO EXHIBIT 1002 - 357/502

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Applicant's or agent's file reference see form PCT/ISA/220	Date of mailing *(day/month/year)* see form PCT/ISA/210 (second sheet) **FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2008/085288	02.12.2008	04.01.2008

International Patent Classification (IPC) or both national classification and IPC
INV. G06F3/14

Applicant
SILICON IMAGE, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☒ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA:	Date of completion of this opinion	Authorized Officer
European Patent Office - P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Tx: 31 651 epo nl Fax: +31 70 340 - 3016	See form PCT/ISA/210	Le Chapelain, B Telephone No. +31 70 340-9545

Form PCT/ISA/237 (Cover Sheet) (April 2005)

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material:

      ☐ a sequence listing

      ☐ table(s) related to the sequence listing

   b. format of material:

      ☐ on paper

      ☐ in electronic form

   c. time of filing/furnishing:

      ☐ contained in the international application as filed.

      ☐ filed together with the international application in electronic form.

      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Box No. II Priority

1. ☒ The validity of the priority claim has not been considered because the International Searching Authority does not have in its possession a copy of the earlier application whose priority has been claimed or, where required, a translation of that earlier application. This opinion has nevertheless been established on the assumption that the relevant date (Rules 43*bis*.1 and 64.1) is the claimed priority date.

2. ☐ This opinion has been established as if no priority had been claimed due to the fact that the priority claim has been found invalid (Rules 43*bis*.1 and 64.1). Thus for the purposes of this opinion, the international filing date indicated above is considered to be the relevant date.

3. Additional observations, if necessary:

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	4,5,7-10,14,17-18,22,25-26
	No:	Claims	1-3, 6,11-13,15,16,19,20,21,23,24
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-26
Industrial applicability (IA)	Yes:	Claims	1-26
	No:	Claims	

2. Citations and explanations

see separate sheet

LENOVO EXHIBIT 1002 - 360/502

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1 Reference is made to the following documents:
D1 : US 2007/286246 A1 (KOBAYASHI OSAMU [US]) 13 December 2007 (2007-12-13)

2 INDEPENDENT CLAIM 1

The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claim 1 is not new in the sense of Article 33(2) PCT.

2.1 The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claim 1 is not new in the sense of Article 33(2) PCT.

Document D1 discloses (the references in parentheses applying to this document):

coupling a transmitting device (fig. 30: 3002) to a receiving device (fig. 30: 3004), coupling of the devices including connecting a control bus between the transmitting device and the receiving device, the control bus being a bi-directional (fig. 30: 3014), single-line bus (par. 72; fig. 14);

obtaining control of the control bus for either the transmitting device or the receiving device, the device obtaining control becoming an initiator and the other device becoming a follower (par. 116; claim 19);

converting one or more control signals to one or more data packets, each of the one or more control signals representing one of a plurality of different types of control signals (par. 75, 76); and

transmitting the generated data packets from the initiator to the follower via the control bus (par. 67; fig. 30: 3014).

The subject-matter of claim 1 is therefore known from D1.

3 DEPENDENT CLAIMS 2-10

Dependent claims 2-10 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty

LENOVO EXHIBIT 1002 - 361/502

and/or inventive step, see document D1 and the corresponding passages cited in the search report.

3.1 CLAIM 2

Document D1 further discloses the signalling for the control bus utilizes bi-phase mark encoding (par. 72, MANCHESTER encoding).
The subject-matter of claim 2 is therefore known from D1.

3.2 CLAIM 3

Document D1 further discloses obtaining control of the control bus includes arbitrating between the transmitting device and the control device for control of the control bus (par. 67: traffic, bandwidth).
The subject-matter of claim 3 is therefore known from D1.

3.3 CLAIMS 4-5

Document D1 further discloses some states machines to activate/de-activate control bus (fig. 18,19).

3.4 CLAIMS 6-10

Document D1 further discloses utilizing a standard protocol (display port) and the transmitting device is a device utilizing a modified protocol (USB) (par. 116).
Document D1 doest not disclose the standard protocol is HDMI but the person skilled in the art knowing D1 would adapted the knowledge of D1 to a HDMI interface without inventive skills and according to the situation.

4 CLAIMS 11-26

The subject-matter of claims 11-26 refers to transmitting device and a receiving device for video and substantially correspond to the subject-matter of claims 1-10. The reasoning given in par. 1-3.4 above therefore applies to claims 11-26 accordingly.
The subject-matter of 11-26 is therefore obvious/known from D1.

LENOVO EXHIBIT 1002 - 362/502

Electronic Patent Application Fee Transmittal

Application Number:	11969852
Filing Date:	04-Jan-2008
Title of Invention:	CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Shrikant Ranade
Filer:	Mark C. Van Ness/lisa riley
Attorney Docket Number:	8029P038

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1810**

Electronic Acknowledgement Receipt

EFS ID:	8790268
Application Number:	11969852
International Application Number:	
Confirmation Number:	1782
Title of Invention:	CONTROL BUS FOR CONNECTION OF ELECTRONIC DEVICES
First Named Inventor/Applicant Name:	Shrikant Ranade
Correspondence Address:	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP - SEVENTH FLOOR 12400 WILSHIRE BOULEVARD LOS ANGELES CA 90025-1026 US 503 439 8778 -
Filer:	Mark C. Van Ness/Lisa Riley
Filer Authorized By:	Mark C. Van Ness
Attorney Docket Number:	8029P038
Receipt Date:	08-NOV-2010
Filing Date:	04-JAN-2008
Time Stamp:	17:21:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1810

RAM confirmation Number	4411
Deposit Account	022666
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	SIMG0335_8029P038_85B.pdf	5709514 b793cecdf83d9890a0866d98d41e659bb5cb866d	no	1
Warnings:					
Information:					
2	Change of Address	SIMG0335_8029P038_Fee_Address_Indication_Form.pdf	315274 4d909832532ec55ea56be37346ea24f346ebbf02	no	2
Warnings:					
Information:					
3	Post Allowance Communication - Incoming	SIMG0335_8029P038_Comments_on_reasons_for_allowance.pdf	25925 7f9a318c1a4a6d2f32b1764d61bf576c011c2fe7	no	2
Warnings:					
Information:					
4	Information Disclosure Statement (IDS) Filed (SB/08)	SIMG0355_8029P038_IDS_After_Allowance.pdf	48672 7e6845fe1ae24327fa1e61fa5556f0c3094030de	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
5	NPL Documents	8029P038PCT_IPRP_mailed_7-15-10.pdf	18272239 3ac751cde29cbd5e131762819bc7243d0370dcd9	no	7
Warnings:					
Information:					
6	Fee Worksheet (PTO-875)	fee-info.pdf	31955 1340bf45589b36f391e3d2c57a6de3886e507476	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	24403579		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/969,852	01/04/2008	Shrikant Ranade	8029P038	1782

7590 11/16/2010

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025-1026

EXAMINER
CLEARY, THOMAS J

ART UNIT	PAPER NUMBER
2111	

MAIL DATE	DELIVERY MODE
11/16/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
11969852	1/4/08	RANADE ET AL.	8029P038

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025-1026

EXAMINER	
THOMAS J.. CLEARY	
ART UNIT	**PAPER**
2111	20101109

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

1. The information disclosure statement filed 8 November 2010 fails to comply with 37 CFR 1.97(d) because it lacks a statement as specified in 37 CFR 1.97(e) and the fee set forth in 37 CFR 1.17(p). It has been placed in the application file, but the information referred to therein has not been considered. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

/Thomas J. Cleary/
Primary Examiner, Art Unit 2111

PTO-90C (Rev.04-03)

NOT CONSIDERED
/TJC/
11/09/2010

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	11/969,852
	Filing Date	January 4, 2008
	First Named Inventor	Ranade, Shrikant
	Group Art Unit	2111
	Examiner Name	Cleary, Thomas
Sheet 1 of 1	Attorney Docket No: 8029P038	

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USPTO Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
		International Bureau, International Preliminary Report on Patentability for International Application No. PCT/US2008/085288 (Attorney Docket No. 8029P038PCT) mailed July 15, 2010	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/969,852	12/21/2010	7856520	8029P038	1782

7590 12/01/2010

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025-1026

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 110 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Shrikant Ranade, Campbell, CA;
Alexander Peysakhovich, San Jose, CA;
Hyuck Jae Lee, San Francisco, CA;
Hoon Choi, Mountain View, CA;

LENOVO EXHIBIT 1002 - 371/502

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5533419

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
JEFFERIES FINANCE LLC	05/17/2019

RECEIVING PARTY DATA

Name:	LATTICE SEMICONDUCTOR CORPORATION
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	SILICON IMAGE, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	SIBEAM, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	DVDO, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124

PROPERTY NUMBERS Total: 1143

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Patent Number:	5510738
Patent Number:	5493205
Patent Number:	5617064
Patent Number:	5670907

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Patent Number:	6998896
Patent Number:	6998906

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Patent Number:	7221607
Patent Number:	6975137
Patent Number:	7382293
Patent Number:	7589648
Patent Number:	7532646
Patent Number:	7245154
Patent Number:	7057397

Property Type	Number
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Patent Number:	7265578
Patent Number:	7397274
Patent Number:	7193436
Patent Number:	7630464
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Patent Number:	7400171
Patent Number:	7009423
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Patent Number:	7342838
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Patent Number:	7342846
Patent Number:	7253674
Patent Number:	7505752
Patent Number:	7414913
Patent Number:	7262630
Patent Number:	7599457
Patent Number:	7295035
Patent Number:	7411419
Patent Number:	7606851
Patent Number:	7187586
Application Number:	11206282
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Application Number:	14589925
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Application Number:	14449095
Application Number:	12842190

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SIGNATURE:	/Urmila Karandikar/
DATE SIGNED:	05/21/2019
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 97

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RELEASE OF A SECURITY INTEREST -- PATENTS

May 17, 2019

WHEREAS, pursuant to that certain (i) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035222, Frame 0866, (ii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035308, Frame 0428, (iii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035223, Frame 0001, (iv) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035226, Frame 0289, (v) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035223, Frame 0387, (vi) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035226, Frame 0147, (vii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035220, Frame 0048, (viii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035220, Frame 0226, (ix) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035309, Frame 0142, (x) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035308, Frame 0345, (xi) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035225, Frame 0839 and (xii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035225, Frame 0352, LATTICE SEMICONDUCTOR CORPORATION, SILICON IMAGE, INC., SIBEAM, INC. and DVDO, INC., each a Delaware corporation (each, a "Releasee"), granted to JEFFERIES FINANCE LLC, as collateral agent for the ratable benefit of the Secured Creditors (the "Releasor"), a continuing security interest in all right, title and interest of the Releasees in, to and under United States Patents listed on the attached Schedule A (the "Patents"), and all Proceeds in respect thereof (with all of the Releasee's rights listed above being collectively referred to as the "Collateral") to secure the payment, performance and observance of the Obligations;

WHEREAS, the Releasees have satisfied their Obligations; and

WHEREAS, the Releasee has requested and the Releasor has agreed to provide a document suitable for recording in the United States Patent and Trademark Office evidencing and effecting the release, relinquishment and discharge of its security interest in the Collateral.

NOW, THEREFORE, in consideration of and in exchange for good and valuable consideration, the Releasor hereby agrees as follows:

1. Defined Terms. All capitalized terms used but not otherwise defined herein have the meanings given to them in the Grants of Security Interests in United States Patents.

2. Release of Security Interest. The Releasor hereby, without any representation and warranty and without any recourse to the Releasor, releases, relinquishes and discharges all of its security interest in the Collateral.

[Signature Page Follows]

IN WITNESS WHEREOF, the undersigned has executed and delivered this Release as of the date first written above.

JEFFERIES FINANCE LLC,
as Collateral Agent and Releasor

By: _____
Name: Paul Chisholm
Title: Managing Director

LENOVO EXHIBIT 1002 - 407/502

SCHEDULE A

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/396,994	5574678	United States	Continuous Time Programmable Analog Block Architecture	Issued	Lattice Semiconductor Corporation
08/403,359	5510738	United States	CMOS Programmable Resistor-Based Transconductor	Issued	Lattice Semiconductor Corporation
08/403,354	5493205	United States	Low Distortion Differential Transconductor Output Current Mirror	Issued	Lattice Semiconductor Corporation
08/403,352	5617064	United States	Active Resistor For Stability Compensation [of Transconductor & Op-Amp Based Gain & Filter Stages]	Issued	Lattice Semiconductor Corporation
08/403,595	5670907	United States	VBB Reference for Pumped Substrates	Issued	Lattice Semiconductor Corporation
08/423,303	5490074	United States	Constant delay interconnect for coupling configurable logic blocks	Issued	Lattice Semiconductor Corporation
08/427,117	5596524	United States	CMOS memory cell with gate oxide of both NMOS and PMOS transistors as tunneling window for program and erase	Issued	Lattice Semiconductor Corporation
08/444,306	5491433	United States	Cascode array cell partitioning for a sense amplifier of a programmable logic device	Issued	Lattice Semiconductor Corporation
08/449,384	5756367	United States	Method of making a spacer based antifuse structure for low capacitance and high reliability	Issued	Lattice Semiconductor Corporation
08/447,991	5594687	United States	Completely complementary MOS memory cell with tunneling through the NMOS and PMOS transistors during program and erase	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/453,184	5570046	United States	Lead frame with noisy and quiet Vss and Vdd leads	Issued	Lattice Semiconductor Corporation
08/453,479	5583451	United States	Polarity control circuit which may be used with a ground bounce limiting buffer	Issued	Lattice Semiconductor Corporation
08/456,946	5621650	United States	Programmable gate array with improved interconnect structure, input/output structure and configurable logic block	Issued	Lattice Semiconductor Corporation
08/459,960	5521529	United States	Very high-density complex programmable logic device with a multi-tiered hierarchical switch matrix and optimized flexible logic allocation	Issued	Lattice Semiconductor Corporation
08/459,230	5818254	United States	Multi-tiered hierarchical high speed switch matrix structure for very high-density complex programmable logic devices	Issued	Lattice Semiconductor Corporation
08/459,234	5781030	United States	Programmable uniform symmetrical distribution logic allocator for a high-density complex PLD	Issued	Lattice Semiconductor Corporation
08/459,786	5638018	United States	P-type flip flop	Issued	Lattice Semiconductor Corporation
08/458,865	5589782	United States	Macrocell and clock signal allocation circuit for a programmable logic device (PLD) enabling PLD resources to provide multiple functions	Issued	Lattice Semiconductor Corporation
08/459,570	6531890	United States	Programmable optimized-distribution logic allocator for a high-density complex PLD	Issued	Lattice Semiconductor Corporation
08/461,196	5586044	United States	Array of configurable logic blocks including cascadable lookup tables	Issued	Lattice Semiconductor Corporation
08/462,934	5469368	United States	Array of configurable logic blocks each including a first	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 409/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			lookup table coupled to selectively replace an output of second lookup with an alternate function output		Corporation
08/486,178	5764078	United States	Family of multiple segmented programmable logic blocks interconnected by a high speed centralized switch matrix	Issued	Lattice Semiconductor Corporation
08/474,629	5612631	United States	An I/O macrocell for a programmable logic device	Issued	Lattice Semiconductor Corporation
08/479,872	5869981	United States	A High density programmable logic device	Issued	Lattice Semiconductor Corporation
08/486,174	5594365	United States	Architecture of a multiple array high density programmable logic device with a plurality of programmable switch matrices	Issued	Lattice Semiconductor Corporation
08/474,635	5811986	United States	Flexible synchronous/asynchronous cell structure for a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/466,438	5754471	United States	Reference for CMOS memory cell having PMOS and NMOS transistors with a common floating gate	Issued	Lattice Semiconductor Corporation
08/466,438	5754471	United States	Low power CMOS array for a PLD with program and erase using controlled avalanche injection	Issued	Lattice Semiconductor Corporation
08/473,620	5594657	United States	Field Programmable Gate Array Using Look-Up Tables, Multiplexers and Decoders	Issued	Lattice Semiconductor Corporation
08/483,623	5617042	United States	Multiple array programmable logic device with a plurality of programmable switch matrices	Issued	Lattice Semiconductor Corporation
08/492,604	5526278	United States	System for Synthesizing Field Programmable Gate Array	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 410/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Implementations From High Level Circuit Descriptions		Corporation
08/493,640	5679599	United States	Isolation using self-aligned trench formation and conventional LOCOS	Issued	Lattice Semiconductor Corporation
08/494,271	5565794	United States	Voltage range tolerant CMOS output buffer with reduced input capacitance	Issued	Lattice Semiconductor Corporation
08/497,992	5742542	United States	Nonvolatile memory cells using only positive charge to store data	Issued	Lattice Semiconductor Corporation
08/500,295	5700698	United States	Method for screening non-volatile memory and programmable logic devices	Issued	Lattice Semiconductor Corporation
08/501,230	5604370	United States	Field Implant For Semiconductor Device	Issued	Lattice Semiconductor Corporation
08/505,837	5635855	United States	Method for Simultaneous Programming of In-System Programmable Integrated Circuits	Issued	Lattice Semiconductor Corporation
08/507,893	5570039	United States	Method and Apparatus for Converting Field-Programmable Gate Array Implementations Into Mask-Programmable Logic Cell Implementations	Issued	Lattice Semiconductor Corporation
08/507,957	5559450	United States	Programmable Function Unit As Parallel Multiplier Cell	Issued	Lattice Semiconductor Corporation
08/528,030	5581126	United States	Interlaced layout configuration for differential pairs of interconnect lines	Issued	Lattice Semiconductor Corporation
08/535,362	5528170	United States	Low-Skew Signal Routing In A Programmable Array	Issued	Lattice Semiconductor Corporation
08/551,974	5615150	United States	control gate-addressed cmos non-volatile cell that programs through gates of CMOS transistors	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 411/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/554,092	5587945	United States	CMOS EEPROM cell with tunneling window in the read path	Issued	Lattice Semiconductor Corporation
08/560,038	5666309	United States	Memory cell for a programmable logic device (PLD) avoiding pumping programming voltage above an NMOS threshold	Issued	Lattice Semiconductor Corporation
08/560,933	5587921	United States	Array of configurable logic blocks each including a lookup table having inputs coupled to a first multiplexer and having outputs to a second multiplexer	Issued	Lattice Semiconductor Corporation
08/561,306	5672521	United States	Method of forming multiple gate oxide thicknesses on a wafer substrate	Issued	Lattice Semiconductor Corporation
08/573,622	5809522	United States	Microprocessor system with process identification tag entries to reduce cache flushing after a context switch	Issued	Lattice Semiconductor Corporation
08/574,776	5739713	United States	Deconvolution input buffer compensating for capacitance of a switch matrix of a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/575,898	5736888	United States	Capacitance elimination circuit	Issued	Lattice Semiconductor Corporation
08/575,852	5719516	United States	Clock generator circuit for use with a dual edge register that provides a separate enable for each edge over an input clock signal	Issued	Lattice Semiconductor Corporation
08/596,679	5598346	United States	Array of configurable logic blocks including network means for broadcasting clock signals to different pluralities of logic blocks	Issued	Lattice Semiconductor Corporation
08/606,702	5623217	United States	Field Programmable Gate Array With Write-Port Enabled Memory	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 412/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/614,728	5926841	United States	Segment descriptor cache for a processor	Issued	Lattice Semiconductor Corporation
08/625,403	5646901	United States	CMOS memory cell with tunneling during program and erase through the NMOS and PMOS transistors and a pass gate separating the NMOS and PMOS transistors	Issued	Lattice Semiconductor Corporation
08/632,811	5751163	United States	Parallel Programming of ISP Devices Using An Automatic Tester	Issued	Lattice Semiconductor Corporation
08/635,184	5666087	United States	Active Resistor For Stability Compensation [of Transconductor & Op-Amp Based Gain & Filter Stages]	Issued	Lattice Semiconductor Corporation
08/643,807	5748525	United States	Array cell circuit with split read/write line	Issued	Lattice Semiconductor Corporation
08/643,291	5864486	United States	Method And Apparatus For In-System Programming of A Programmable Logic Device Using a Two-Wire Interface	Issued	Lattice Semiconductor Corporation
08/653,186	5789939	United States	Very high-density complex programmable logic device with a multi-tiered hierarchical switch matrix and optimized flexible logic allocation	Issued	Lattice Semiconductor Corporation
08/659,279	5723984	United States	Field programmable gate array (FPGA) with interconnect encoding	Issued	Lattice Semiconductor Corporation
08/659,941	5808942	United States	Field programmable gate array (FPGA) having an improved configuration memory and look up table	Issued	Lattice Semiconductor Corporation
08/664,190	5830795	United States	Simplified masking process for programmable logic device manufacture	Issued	Lattice Semiconductor Corporation
08/666,193	5760609	United States	Clock signal providing circuit with enable and a pulse generator with enable for use	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 413/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			in a block clock circuit of a programmable logic device		
08/668,141	5796295	United States	Reference for CMOS memory cell having PMOS and NMOS transistors with a common floating gate	Issued	Lattice Semiconductor Corporation
08/668,896	5751164	United States	Programmable logic device with multi-level power control	Issued	Lattice Semiconductor Corporation
08/683,685	5734275	United States	Programmable logic device having a sense amplifier with virtual ground	Issued	Lattice Semiconductor Corporation
08/683,373	5818294	United States	Temperature insensitive current source	Issued	Lattice Semiconductor Corporation
08/690,768	5801551	United States	Depletion mode pass gates with controlling decoder and negative power supply for a programmable logic device	Issued	Lattice Semiconductor Corporation
08/689,523	5942780	United States	An integrated circuit having, and process providing, different oxide layer thicknesses on a substrate	Issued	Lattice Semiconductor Corporation
08/696,444	5796750	United States	Method for Programming a PLD In An Automatic Tester	Issued	Lattice Semiconductor Corporation
08/700,616	5740069	United States	Logic device (PLD) having direct connections between configurable logic blocks (CLBs) and configurable input/output blocks (IOBs)	Issued	Lattice Semiconductor Corporation
08/699,401	5960274	United States	Oxide formation process for manufacturing programmable logic device	Issued	Lattice Semiconductor Corporation
08/702,846	5959336	United States	Decoder circuit with short channel depletion transistors	Issued	Lattice Semiconductor Corporation
08/710,445	5862365	United States	Configuration Pin Emulation Circuit For a Field Programmable Array	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 414/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/723,082	5760605	United States	Programmable high speed routing switch	Issued	Lattice Semiconductor Corporation
08/726,512	5761116	United States	Vpp only scalable EEPROM memory cell having transistors with thin tunnel gate oxide	Issued	Lattice Semiconductor Corporation
08/729,117	5991907	United States	Method for Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/734,888	5805607	United States	Method for user-controlled I/O switching during in-circuit programming of CPLDs through the IEEE 1149.1 test access port	Issued	Lattice Semiconductor Corporation
08/740,948	5811987	United States	Block clock and initialization circuit for a complex high density PLD	Issued	Lattice Semiconductor Corporation
08/748,041	5892962	United States	FPGA-based Processor	Issued	Lattice Semiconductor Corporation
08/745,410	5717342	United States	Output buffer incorporating shared intermediate nodes	Issued	Lattice Semiconductor Corporation
08/781,882	6028993	United States	Timed Circuit Simulation In Hardware Using FPGAs	Issued	Lattice Semiconductor Corporation
08/785,096	5841701	United States	Method of charging and discharging floating gage transistors to reduce leakage current	Issued	Lattice Semiconductor Corporation
08/799,153	5904575	United States	Method and apparatus incorporating nitrogen selectively for differential oxide growth	Issued	Lattice Semiconductor Corporation
08/799,235	5885904	United States	Method to incorporate, and a device having, oxide enhancement dopants using gas immersion laser doping (GILD) for selectively growing an oxide layer	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 415/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/823,953	6190966	United States	Process for fabricating semiconductor memory device with high data retention including silicon nitride etch stop layer formed at high temperature with low hydrogen ion	Issued	Lattice Semiconductor Corporation
08/828,520	5905385	United States	Memory bits used to couple look up table inputs to facilitate increased availability to routing resources particularly for variable sized look up tables for a field programmable gate array (FPGA)	Issued	Lattice Semiconductor Corporation
08/831,372	5844912	United States	Fast verify for CMOS memory cell	Issued	Lattice Semiconductor Corporation
08/827,671	5835405	United States	Application Specific Modules in a Programmable Logic Device	Issued	Lattice Semiconductor Corporation
08/843,150	6087275	United States	Reduction of n-channel parasitic transistor leakage by using low power/low pressure phosphosilicate glass	Issued	Lattice Semiconductor Corporation
08/838,487	6034541	United States	In-System Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
08/856,926	5949279	United States	Devices for sourcing constant supply current from power supply in system with integrated circuit having variable supply current requirement	Issued	Lattice Semiconductor Corporation
08/859,761	5989957	United States	Process for fabricating semiconductor memory device with high data retention including silicon nitride etch stop layer formed at high temperature with low hydrogen ion concentration	Issued	Lattice Semiconductor Corporation
08/871,589	5978272	United States	Nonvolatile memory structure for programmable logic devices	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 416/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/899,428	6028447	United States	FPGA Having Predictable Open-Drain Drive Mode	Issued	Lattice Semiconductor Corporation
08/912,763	6072351	United States	Output buffer for making a high voltage (5.0 volt) compatible input/output in a low voltage (2.5 volt) semiconductor process	Issued	Lattice Semiconductor Corporation
08/931,798	6359466	United States	Circuitry to provide fast carry	Issued	Lattice Semiconductor Corporation
08/938,550	6020755	United States	Hybrid Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/948,306	6097212	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/947,888	5854114	United States	Data retention of EEPROM cell with shallow trench isolation using thicker liner oxide	Issued	Lattice Semiconductor Corporation
08/949,992	6028463	United States	Programmable Clock Manager For A Programmable Logic Device that Can Generate At Least Two Different Output Clocks	Issued	Lattice Semiconductor Corporation
08/950,444	6216191	United States	Field Programmable Gate Array Having A Dedicated Processor Interface	Issued	Lattice Semiconductor Corporation
08/950,446	5986471	United States	Bi-directional Buffers and Supplemental Logic and Interconnect Cells for Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
08/950,448	6060902	United States	A Programmable Clock Manager For A Programmable Logic Device that Can Be Programmed Without Reconfiguring the Device	Issued	Lattice Semiconductor Corporation
08/950,624	6049224	United States	Programmable Logic Device With Logic Cells Having A Flexible Input Structure	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 417/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/951,128	6043677	United States	Programmable Clock Manager For A Programmable Logic Device that Can Implement Delay-Locked Loop Functions	Issued	Lattice Semiconductor Corporation
08/964,421	6389321	United States	Simultaneous Wired and Wireless Remote In-System Programming of Multiple Remote Systems	Issued	Lattice Semiconductor Corporation
08/974,799	6003150	United States	Method for Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/996,361	6275064	United States	Symmetrical, extended and fast direct connections between variable grain blocks in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/996,049	6127843	United States	Dual port SRAM memory for run time use in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,615	6034544	United States	Programmable input/output block (IOB) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,614	5982193	United States	Input/output block (IOB) connections to MAXL lines, NOR lines and dendrites in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,612	5990702	United States	Flexible direct connections between input/output blocks (IOBs) and variable grain blocks (VBGs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/997,221	6107823	United States	Programmable control multiplexing for input/output blocks (IOBs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/996,119	5986480	United States	Multiple input zero power and/nor gate for use in a field programmable gate array (FPGA)	Issued	Lattice Semiconductor Corporation
08/996,530	6134703	United States	A Process for Programming PLDs and Embedded Non-Volatile Memories	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 418/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/998,978	6102963	United States	Electrically erasable and reprogrammable, nonvolatile integrated storage device with in-system programming and verification (ISPAV) capabilities for supporting in-system reconfiguring of PLD's	Issued	Lattice Semiconductor Corporation
09/008,762	6130551	United States	Synthesis-friendly FPGA architecture with variable length and variable timing interconnect	Issued	Lattice Semiconductor Corporation
09/010,000	6034538	United States	Virtual Logic System For Reconfigurable Hardware	Issued	Lattice Semiconductor Corporation
09/023,669	6025637	United States	Spacer based antifuse structure for low capacitance and high reliability and method of fabrication thereof	Issued	Lattice Semiconductor Corporation
09/023,506	6023570	United States	Sequential and Simultaneous Manufacturing Programming of Multiple In-System Programmable Systems Through a Data Network	Issued	Lattice Semiconductor Corporation
09/026,814	6093946	United States	EEPROM cell with field-edgeless tunnel window using shallow trench isolation process	Issued	Lattice Semiconductor Corporation
09/037,095	6128770	United States	Configurable logic array including IOB to longlines interconnect means for providing selectable access to plural longlines from each IOB (input/output block)	Issued	Lattice Semiconductor Corporation
09/045,128	6064225	United States	Global Signal Distribution With Reduced Routing Tracks In An FPGA	Issued	Lattice Semiconductor Corporation
09/046,404	5982683	United States	Enhanced method of testing semiconductor devices having nonvolatile elements	Issued	Lattice Semiconductor Corporation
09/053,251	6556154	United States	Offset Voltage Calibration DAC With Reduced Sensitivity To Mismatch	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 419/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Errors		
09/059,552	6108806	United States	Method of Testing and Diagnosing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/067,320	6154050	United States	Internal tristate bus with arbitration logic	Issued	Lattice Semiconductor Corporation
09/067,318	6104207	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/069,035	6133750	United States	Combination of global clock and localized clocks	Issued	Lattice Semiconductor Corporation
09/069,768	6002610	United States	Non-Volatile Memory Element For Programmable Logic Applications and Operational Methods Therefor	Issued	Lattice Semiconductor Corporation
09/080,906	6225821	United States	Package migration for related programmable logic devices	Issued	Lattice Semiconductor Corporation
09/083,335	6304099	United States	Method and structure for dynamic in-system programming	Issued	Lattice Semiconductor Corporation
09/083,336	6066977	United States	Programmable Output Voltage Levels	Issued	Lattice Semiconductor Corporation
09/083,205	6255847	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/086,437	6087696	United States	Stacked tunneling dielectric technology for improving data retention of EEPROM cell	Issued	Lattice Semiconductor Corporation
09/109,123	6202182	United States	Method and Apparatus For Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/114,385	6028758	United States	Electrostatic discharge (ESD) protection for a 5.0 volt compatible input/output (I/O) in a 2.5 volt semiconductor process	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 420/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/114,717	6091595	United States	Electrostatic discharge (ESD) protection for NMOS pull up transistors of a 5.0 volt compatible output buffer using 2.5 volt process transistors	Issued	Lattice Semiconductor Corporation
09/114,718	6043969	United States	Ballast resistors with parallel stacked NMOS transistors used to prevent secondary breakdown during ESD with 2.5 volt process transistors	Issued	Lattice Semiconductor Corporation
09/115,683	6124732	United States	Signaling Voltage Range Discriminator	Issued	Lattice Semiconductor Corporation
09/118,200	6028446	United States	Flexible Synchronous and Asynchronus Circuits for A Very High Density Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/134,174	6064105	United States	Data retention of EEPROM cell with shallow trench isolation using thicker liner oxide	Issued	Lattice Semiconductor Corporation
09/145,793	6087854	United States	High Speed Line Driver With Direct and Complementary Outputs	Issued	Lattice Semiconductor Corporation
09/169,848	6347387	United States	Test Circuits For Multiple FPGA Systems	Issued	Lattice Semiconductor Corporation
09/169,492	6424003	United States	EEPROM cell with self-aligned tunneling window	Issued	Lattice Semiconductor Corporation
09/187,691	6228696	United States	Semiconductor-oxide-semiconductor capacitor formed in integrated circuit	Issued	Lattice Semiconductor Corporation
09/187,689	6154051	United States	Tileable and compact layout for super variable grain blocks within FPGA device	Issued	Lattice Semiconductor Corporation
09/186,917	6229336	United States	Programmable integrated circuit device with slew control and skew control	Issued	Lattice Semiconductor Corporation
09/188,778	6169432	United States	High voltage switch for	Issued	Lattice

LENOVO EXHIBIT 1002 - 421/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			providing voltages higher than 2.5 volts with transistors made using a 2.5 volt process		Semiconductor Corporation
09/192,094	6291327	United States	Optimization of S/D annealing to minimize random S/D shorts in memory array	Issued	Lattice Semiconductor Corporation
09/192,096	6221733	United States	Reduction of mechanical stress in shallow trench isolation process	Issued	Lattice Semiconductor Corporation
09/196,449	6191612	United States	Enhanced I/O control flexibility for generating control signals	Issued	Lattice Semiconductor Corporation
09/196,080	5912550	United States	Power converter with 2.5 semiconductor process components	Issued	Lattice Semiconductor Corporation
09/198,796	6218857	United States	Variable sized line driving amplifiers for input/output blocks (IOBs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/200,395	6261944	United States	Semiconductor device having high reliability passivation and fabrication method	Issued	Lattice Semiconductor Corporation
09/198,653	6009033	United States	Method of programming and erasing an EEPROM device under an elevated temperature and apparatus thereof	Issued	Lattice Semiconductor Corporation
09/199,664	6353352	United States	Clock tree topology	Issued	Lattice Semiconductor Corporation
09/201,081	6133769	United States	Phase locked loop with a lock detector	Issued	Lattice Semiconductor Corporation
09/203,149	6404006	United States	EEPROM cell with tunneling across entire separated channels	Issued	Lattice Semiconductor Corporation
09/217,647	5969992	United States	EEPROM cell using p-well for	Issued	Lattice Semiconductor Corporation
09/207,558	6175266	United States	Operational amplifier with CMOS transistors made using	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 422/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			2.5 volt process transistors		Corporation
09/208,203	6163168	United States	Efficient interconnect network for use in FPGA device having variable grain architecture	Issued	Lattice Semiconductor Corporation
09/212,022	6124730	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/212,330	6100715	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/212,331	6081473	United States	FPGA integrated circuit having embedded SRAM memory blocks each with statically and dynamically controllable read mode	Issued	Lattice Semiconductor Corporation
09/216,662	6204686	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	Issued	Lattice Semiconductor Corporation
09/216,051	6214666	United States	Method of forming a non-volatile memory device	Issued	Lattice Semiconductor Corporation
09/217,648	6232631	United States	Floating gate memory cell structure with programming mechanism outside the read path	Issued	Lattice Semiconductor Corporation
09/217,646	6282123	United States	Method of fabricating, programming, and erasing a dual pocket two sided program/erase non-volatile memory cell	Issued	Lattice Semiconductor Corporation
09/218,987	6294810	United States	EEPROM cell with tunneling at separate edge and channel regions	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 423/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/220,469	6157568	United States	Avalanche programmed floating gate memory cell structure with program element in first polysilicon layer	Issued	Lattice Semiconductor Corporation
09/221,360	6294809	United States	Avalanche programmed floating gate memory cell structure with program element in polysilicon	Issued	Lattice Semiconductor Corporation
09/226,702	6215700	United States	PMOS avalanche programmed floating gate memory cell structure	Issued	Lattice Semiconductor Corporation
09/227,981	6197638	United States	Oxide formation process for manufacturing programmable logic device	Issued	Lattice Semiconductor Corporation
09/235,356	6097664	United States	Multi-port SRAM cell array having plural write paths including for writing through addressable port and through serial boundary scan	Issued	Lattice Semiconductor Corporation
09/235,351	6181163	United States	FPGA integrated circuit having embedded SRAM memory blocks and interconnect channel for broadcasting address and control	Issued	Lattice Semiconductor Corporation
09/235,615	6211695	United States	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	Issued	Lattice Semiconductor Corporation
09/239,072	5999449	United States	Two transistor EEPROM cell using P-well for tunneling across a channel	Issued	Lattice Semiconductor Corporation
09/240,560	6297128	United States	Process for manufacturing shallow trenches filled with dielectric material having low mechanical stress	Issued	Lattice Semiconductor Corporation
09/245,813	6294811	United States	Two transistor EEPROM cell	Issued	Lattice Semiconductor Corporation
09/255,410	6075724	United States	Method for sorting	Issued	Lattice

LENOVO EXHIBIT 1002 - 424/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			semiconductor devices having a plurality of non-volatile memory cells		Semiconductor Corporation
09/255,053	6255169	United States	Process for fabricating a high-endurance non-volatile memory device	Issued	Lattice Semiconductor Corporation
09/256,245	6133164	United States	Fabrication of oxide regions having multiple thicknesses using minimized number of thermal cycles	Issued	Lattice Semiconductor Corporation
09/261,776	6256758	United States	Fault Tolerance Operation of Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/263412	6075293	United States	Semiconductor device having a multi-layer metal interconnect structure	Issued	Lattice Semiconductor Corporation
09/268,897	6207989	United States	Non-volatile memory device having a high-reliability composite insulation layer	Issued	Lattice Semiconductor Corporation
09/276,991	6031365	United States	Band gap reference using a low voltage power supply	Issued	Lattice Semiconductor Corporation
09/276,990	6163175	United States	High voltage detector to control a power supply voltage pump for a 2.5 volt semiconductor process device	Issued	Lattice Semiconductor Corporation
09/277,441	6326663	United States	Avalanche injection EEPROM memory cell with p-type control gate	Issued	Lattice Semiconductor Corporation
09/280,887	6172392	United States	Boron doped silicon capacitor plate	Issued	Lattice Semiconductor Corporation
09/286,830	6284626	United States	Angled nitrogen ion implantation for minimizing mechanical stress on side walls of an isolation trench	Issued	Lattice Semiconductor Corporation
09/288,062	6265900	United States	High Speed Logical OR Circuit	Issued	Lattice Semiconductor Corporation
09/287,976	6413826	United States	Gate insulator process for	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 425/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			nanometer MOSFETs		Corporation
09/310,071	6424000	United States	Floating gate memory apparatus and method for selected programming thereof	Issued	Lattice Semiconductor Corporation
09/316,241	6274898	United States	Triple-well EEPROM cell using p-well for tunneling across a channel	Issued	Lattice Semiconductor Corporation
09/318,570	6552595	United States	High Voltage Discharge Scheme	Issued	Lattice Semiconductor Corporation
09/320389	6118693	United States	Electrically erasable non-volatile memory cell with integrated SRAM to reduce testing time	Issued	Lattice Semiconductor Corporation
09/320,392	6067252	United States	Electrically erasable non-volatile memory cell with no static power dissipation	Issued	Lattice Semiconductor Corporation
09/326,940	6184713	United States	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	Issued	Lattice Semiconductor Corporation
09/326,140	6150841	United States	Enhanced storage macrocell module for high density CPLD architectures	Issued	Lattice Semiconductor Corporation
09/330,753	6628660	United States	Finite State Machine with Associated Memory	Issued	Lattice Semiconductor Corporation
09/334,051	6028789	United States	Zero-power CMOS non-volatile memory cell having an avalanche injection element	Issued	Lattice Semiconductor Corporation
09/334,052	6034893	United States	Non-volatile memory cell having dual avalanche injection elements	Issued	Lattice Semiconductor Corporation
09/400,029	6404226	United States	Integrated Circuit With Standard Cell Logic and Spare Gates	Issued	Lattice Semiconductor Corporation
09/405,958	6550030	United States	On-Line Testing of the Programmable Logic Blocks In Field Programmable Gate	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 426/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Arrays		
09/406,219	6574761	United States	On-Line Testing of the Programmable Interconnect Network In Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/433,642	6191609	United States	Combination of global clock and localized clocks	Issued	Lattice Semiconductor Corporation
09/440,460	6294925	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/440,207	6278311	United States	Method for minimizing instantaneous currents when driving bus signals	Issued	Lattice Semiconductor Corporation
09/441,220	6208559	United States	Method of operating EEPROM memory cells having transistors with thin gate oxide and reduced disturb	Issued	Lattice Semiconductor Corporation
09/452,017	6137738	United States	Method For In-System Programming of Serially Configured EEPROMS Using a JTAG Interface of an FPGA	Issued	Lattice Semiconductor Corporation
09/454,322	6326808	United States	Inversion of Product Term Line Before or Logic in a Programmable Logic Device (PLD)	Issued	Lattice Semiconductor Corporation
09/472,645	6150842	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/506,180	6362684	United States	Amplifier Having an Adjustable Resistor Network	Issued	Lattice Semiconductor Corporation
09/507,580	6424209	United States	Integrated Programmable Continuous Time Filter with Programmable Capacitor Arrays	Issued	Lattice Semiconductor Corporation
09/548,171	6351157	United States	Output buffer for making a high voltage (5.0 volt) compatible input/output in a low voltage (2.5 volt)	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 427/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			semiconductor process		
09/567,898	6288937	United States	Decoded Generic Routing Pool	Issued	Lattice Semiconductor Corporation
09/578,086	6570212	United States	Complementary avalanche injection EEPROM cell	Issued	Lattice Semiconductor Corporation
09/603,119	6292930	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/603,807	6216257	United States	FPGA device and method that includes a variable grain function architecture for implementing configuration logic blocks and a complimentary variable length interconnect architecture for providing configurable routing between configuration logic blocks	Issued	Lattice Semiconductor Corporation
09/611,449	6530049	United States	On-line Fault Tolerant Operation Via Incremental Reconfiguration of Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/626,094	6380759	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/632,319	6567969	United States	Configurable Logic Array Including Lookup Table Means For Generating Functions of Different Numbers Of Input Terms	Issued	Lattice Semiconductor Corporation
09/643,279	6627947	United States	Compact single-poly two-transistor EEPROM cell	Issued	Lattice Semiconductor Corporation
09/651,689	6433602	United States	High speed schmitt trigger with low supply voltage	Issued	Lattice Semiconductor Corporation
09/660,707	6370071	United States	High Voltage CMOS switch	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 428/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
09/661,585	6462576	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/668,896	6701340	United States	Double Differential Comparator and Programmable Analog Block Architecture Using Same	Issued	Lattice Semiconductor Corporation
09/669,186	6249144	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/671,853	6631487	United States	On-Line Testing of Field Programmable Gate Array Resources	Issued	Lattice Semiconductor Corporation
09/692,694	6470485	United States	Scalable and parallel processing methods and structures for testing configurable interconnect network in FPGA device	Issued	Lattice Semiconductor Corporation
09/704,487	6507212	United States	Wide input programmable logic system and method	Issued	Lattice Semiconductor Corporation
09/651,805	6455912	United States	Process for manufacturing shallow trenches filled with dielectric material having low mechanical stress	Issued	Lattice Semiconductor Corporation
09/712,000	6356107	United States	Method and structure for dynamic in-system programming	Issued	Lattice Semiconductor Corporation
09/721,153	6348813	United States	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	Issued	Lattice Semiconductor Corporation
09/732,216	6735706	United States	Programmable power management system and method	Issued	Lattice Semiconductor Corporation
09/731,184	6524911	United States	Combination of BPTEOS oxide film with CMP and RTA to achieve good data	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 429/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			retention		
09/731,185	6287916	United States	Method for forming a semiconductor device using LPCVD nitride to protect floating gate from charge loss	Issued	Lattice Semiconductor Corporation
09/733,878	6526558	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	Issued	Lattice Semiconductor Corporation
09/775,488	6462602	United States	Voltage Level Translator Systems And Methods	Issued	Lattice Semiconductor Corporation
09/775,489	6414521	United States	Improved sense amplifier systems and methods	Issued	Lattice Semiconductor Corporation
09/818,257	6496969	United States	Programming Programmable Logic Devices Using Hidden Switches	Issued	Lattice Semiconductor Corporation
09/841,209	6590415	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/863,656	6535043	United States	Clock Signal Selection System, Method of Generating A Clock Signal And Programmable Clock Manager Including Same	Issued	Lattice Semiconductor Corporation
09/864,276	6486705	United States	Signal Distribution Scheme In Field Programmable Gate Array (FPGA) or Field Programmable Systems Chip (FPSC) Including Cycle Stealing Units	Issued	Lattice Semiconductor Corporation
09/864,284	6472904	United States	Double Data Rate Input And Output In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/864,289	6480026	United States	Multi-functional I/O Buffers In a Field Programmable Gate	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 430/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Array (FPGA)		Corporation
09/864,277	6483342	United States	Multi-Master Multi-Slave Bus In Field Programmable Gate Array (FPGA)	Issued	Lattice Semiconductor Corporation
09/864,290	6772230	United States	Field Programmable Gate Array (FPGA) Bit Stream Format	Issued	Lattice Semiconductor Corporation
09/870,877	6498538	United States	Low Jitter Integrated Phase Locked Loop With Broad Tuning Range	Issued	Lattice Semiconductor Corporation
09/870,541	6455375	United States	EEPROM tunnel window for program injection via P+ contacted inversion	Issued	Lattice Semiconductor Corporation
09/881,950	6614291	United States	Low Voltage, High Speed CMOS CML Latch and MUX Devices	Issued	Lattice Semiconductor Corporation
09/885,243	6429692	United States	High Speed Data Sampling With Reduced Metastability	Issued	Lattice Semiconductor Corporation
09/927,289	6492877	United States	Improved Coupling For LC-Based VCO	Issued	Lattice Semiconductor Corporation
09/927,612	6525617	United States	Buffering For LC-Based Stage	Issued	Lattice Semiconductor Corporation
09/927,793	6653860	United States	Enhanced logic macrocell with expanded PT (product term) sharing capability for Use in High Density CPLD Architectures	Issued	Lattice Semiconductor Corporation
09/941,454	6489835	United States	Low Voltage Bandgap Reference Circuit	Issued	Lattice Semiconductor Corporation
09/949,112	6593222	United States	Method to improve the reliability of thermosonic gold to aluminum wire bonds	Issued	Lattice Semiconductor Corporation
09/966,967	6832231	United States	Multiple Width Random Number Generation	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 431/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/011,549	6693830	United States	Single Poly Two-Transistor EEPROM Cell With Differentially Doped Floating Gate	Issued	Lattice Semiconductor Corporation
10/053,004	6989551	United States	Test structure for determining the minimum tunnel opening size in a non-volatile memory cell	Issued	Lattice Semiconductor Corporation
10/010,011	6515899	United States	Non-Volatile Memory Cell With Enhanced Cell Drive Current	Issued	Lattice Semiconductor Corporation
09/991,245	6611463	United States	Zero Power Programmable Memory Cell	Issued	Lattice Semiconductor Corporation
09/992,493	6489806	United States	Zero power logic cell for use in programmable logic devices	Issued	Lattice Semiconductor Corporation
10/006,559	7003066	United States	Digital Phase locked Loop with Phase Selector having Minimized Number of Phase Interpolators	Issued	Lattice Semiconductor Corporation
10/006,610	6999543	United States	Clock Data Recovery Deserializer With Programmable Sync Detect Logic	Issued	Lattice Semiconductor Corporation
10/006,516	6993108	United States	Digital Phase Locked Loop With Programmable Digital Filter	Issued	Lattice Semiconductor Corporation
10/021,873	6661254	United States	Programmable Interconnect Circuit With A Phase-Locked Loop	Issued	Lattice Semiconductor Corporation
10/017,725	6674303	United States	Programmable I/O cell with bidirectional and shift register capabilities	Issued	Lattice Semiconductor Corporation
10/017,859	6605959	United States	Structure and Method for Implementing Wide Multiplexers	Issued	Lattice Semiconductor Corporation
10/022,464	7154298	United States	Block oriented architecture for programmable interconnect circuit	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 432/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/021,844	6703860	United States	I/O Block for Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/023,053	6653861	United States	Multi-level Routing Structure for a Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/023,226	6650141	United States	High Speed Interface For a Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/059,624	6636442	United States	Non-volatile memory element having a cascoded transistor scheme to reduce oxide field stress	Issued	Lattice Semiconductor Corporation
10/061,057	6845044	United States	Method of preventing high Icc at start-up in zero-power EEPROM cells for PLD applications	Issued	Lattice Semiconductor Corporation
10/066,031	6680625	United States	Symmetrical CML Logic Gate System	Issued	Lattice Semiconductor Corporation
10/082,050	6781170	United States	Integrated Circuit Base Transistor Structure And Associated Programmable Cell Library	Issued	Lattice Semiconductor Corporation
10/083,728	6600188	United States	An EEPROM with neutralized doping at tunnel window edge	Issued	Lattice Semiconductor Corporation
10/090,209	6621298	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
10/103,100	6795959	United States	Integrated Delay Discriminator For Use With a Field- Programmable Gate Array and A Method of Determining a Time Delay Thereof	Issued	Lattice Semiconductor Corporation
10/106,509	6907439	United States	FFT address generation method and apparatus	Issued	Lattice Semiconductor Corporation
10/108,401	6976047	United States	Skipped carry incrementer for FFT address generation	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 433/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/112,370	6639431	United States	Differential Input Comparator	Issued	Lattice Semiconductor Corporation
10/128,943	6660579	United States	Zero Power Memory Cell With Improved Data Retention	Issued	Lattice Semiconductor Corporation
10/131,883	7032162	United States	Polynomial Expander for Generating Coefficients of a Polynomial from Roots of the Polynomial	Issued	Lattice Semiconductor Corporation
10/133,016	6765408	United States	Device and Method with Generic Logic Blocks	Issued	Lattice Semiconductor Corporation
10/135,308	6814296	United States	Integrated Circuit and Associated Design Method With Antenna Error Control Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/135,325	6600341	United States	Integrated Circuit and Associated Design Method Using Spare Gate Islands	Issued	Lattice Semiconductor Corporation
10/146,739	6714048	United States	Input Buffer With Selectable PCL, GTL, or PECL Compatibility	Issued	Lattice Semiconductor Corporation
10/146,826	6657458	United States	Output Buffer With Feedback From An Input Buffer To Provide Selectable PCL, GTL, or PECL Compatability	Issued	Lattice Semiconductor Corporation
10/146,769	6870391	United States	Input Buffer With CMOS Driver Gate Current Control Enabling Selectable PCL, GTL, or PECL Compatibility	Issued	Lattice Semiconductor Corporation
10/147,199	6714043	United States	Output Buffer Having Programmable Drive Current And Output Voltage Limits	Issued	Lattice Semiconductor Corporation
10/146,734	6720755	United States	Band Gap Reference Circuit	Issued	Lattice Semiconductor Corporation
10/147,011	6760209	United States	Electrostatic Discharge Protection Circuit	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 434/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/151,753	6798244	United States	Output Buffer With Overvoltage Protection	Issued	Lattice Semiconductor Corporation
10/150,410	6848095	United States	Method of Assigning Logic Functions To Macrocells In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/159,009	6583652	United States	Highly linear programmable transconductor with large input-signal range	Issued	Lattice Semiconductor Corporation
10/159,089	6717451	United States	Precision analog level shifter with programmable options	Issued	Lattice Semiconductor Corporation
10/159,681	6806771	United States	Multimode output stage converting differential to single-ended signals using current-mode input signals	Issued	Lattice Semiconductor Corporation
10/162,337	6596587	United States	Shallow junction EEPROM Device and Process for Fabricating the Device	Issued	Lattice Semiconductor Corporation
10/160,855	6794236	United States	EEPROM Device with Improved Capacitive Coupling and Fabrication Process	Issued	Lattice Semiconductor Corporation
10/161,283	6716705	United States	EEPROM Device having a Retrograde Program Junction Region And Process for Fabrication the Device	Issued	Lattice Semiconductor Corporation
10/164,484	6703305	United States	Semiconductor Device Having Metallized Interconnect Structure And Method Of Fabricaton	Issued	Lattice Semiconductor Corporation
10/187,236	6844757	United States	Converting Bits to Vectors In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/191,888	6650143	United States	FPGA Based Upon Transistor gate Oxide Breakdown	Issued	Lattice Semiconductor Corporation
10/194,771	7028281	United States	FPGA With Register-Intensive Architecture	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 435/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/200,645	6714066	United States	Integrated Programmable Continuous Time Filter with Programmable Capacitor Arrays	Issued	Lattice Semiconductor Corporation
10/207,292	6683477	United States	Wide input programmable logic system and method	Issued	Lattice Semiconductor Corporation
10/210,367	6938197	United States	CRC Calculation System And Method For A Packet Arriving On An N-Byte Wide Bus	Issued	Lattice Semiconductor Corporation
10/211,125	6545313	United States	EEPROM tunnel window for program injection via P+ contacted inversion	Issued	Lattice Semiconductor Corporation
10/219,046	6650142	United States	Enhanced CPLD Macrocell Module Having Selectable Bypass of Steering-based Resource Allocation and Methods of Use	Issued	Lattice Semiconductor Corporation
10/233,021	7043511	United States	Performing Conditional Operations In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/232,912	6841447	United States	EEPROM Device Having An Isolation -Bounded Tunnel Capacitor And Fabrication Process	Issued	Lattice Semiconductor Corporation
10/235,380	6725442	United States	Scalable and parallel processing methods and structures for testing configurable interconnect network in FPGA device	Issued	Lattice Semiconductor Corporation
10/236,829	6842372	United States	EEPROM Cell Having Floating Gate Transistor Within a Cell Well And a Process For Fabricating the Memory Cell	Issued	Lattice Semiconductor Corporation
10/236,114	6833602	United States	Device Having Electrically Isolated Low Voltage And High Voltage Regions And Process For Fabricating the Device	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 436/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/236,718	6649514	United States	EEPROM Device Having Improved Data Retention And Process for Fabricating The Device	Issued	Lattice Semiconductor Corporation
10/242,809	6738306	United States	Multiport SRAM Cell	Issued	Lattice Semiconductor Corporation
10/243,014	6917536	United States	Memory access Circuit and Method for reading and writing data with the same clock signal	Issued	Lattice Semiconductor Corporation
10/251,608	6700154	United States	EEPROM cell with trench coupling capacitor	Issued	Lattice Semiconductor Corporation
10/255,474	6907592	United States	Method of Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,875	6809551	United States	Method of Optimizing Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,499	6803787	United States	State Machine In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,656	6812738	United States	Vector Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/263,251	6748575	United States	Programming Programmable Logic Devices Using Hidden Switches	Issued	Lattice Semiconductor Corporation
10/263,507	6846714	United States	Voltage Limted EEPROM Device And Process For Fabricating the Device	Issued	Lattice Semiconductor Corporation
10/266,361	6639434	United States	Low voltage differential signaling systems and methods	Issued	Lattice Semiconductor Corporation
10/269,804	7111183	United States	Expansion method for complex power-sequencing applications	Issued	Lattice Semiconductor Corporation
10/269,450	6791394	United States	Power Supply Control Circuits	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 437/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/269,439	6762618	United States	Innovative verify scheme for two level GRP fuse in programmable bus switching family	Issued	Lattice Semiconductor Corporation
10/272,582	6901572	United States	Power Sequence Controller Programming Technique	Issued	Lattice Semiconductor Corporation
10/278,415	6639449	United States	Asynchronous glitch-free clock multiplexer	Issued	Lattice Semiconductor Corporation
10/282,524	7051261	United States	Turbo Encoder With Reduced Processing Delay	Issued	Lattice Semiconductor Corporation
10/283,765	6700823	United States	Programmable common mode termination for differential input/output circuits	Issued	Lattice Semiconductor Corporation
10/288,667	7000210	United States	Adaptive Adjustment Of Constraints During PLD Placement Processing	Issued	Lattice Semiconductor Corporation
10/288,668	6813754	United States	Placement Processing For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/300,190	6825733	United States	Low Jitter Integrated Phase Locked Loop With Broad Tuning Range	Issued	Lattice Semiconductor Corporation
10/302,439	6797568	United States	Flash Technology Transistors and Method For Forming Same	Issued	Lattice Semiconductor Corporation
10/308,420	6710641	United States	Low Voltage Bandgap Reference Circuit	Issued	Lattice Semiconductor Corporation
10/309,302	6650188	United States	Improved Coupling For LC-Based VCO	Issued	Lattice Semiconductor Corporation
10/334,642	6777979	United States	FIFO memory architecture	Issued	Lattice Semiconductor Corporation
10/338,619	6753696	United States	Programmable optimized-distribution logic allocator for	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 438/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			a high-density complex PLD		Corporation
10/365,083	7034596	United States	Adaptive input logic for phase adjustments	Issued	Lattice Semiconductor Corporation
10/368,023	6915323	United States	Macrocells Supporting A Carry Cascade	Issued	Lattice Semiconductor Corporation
10/366,956	6788101	United States	Programmable input buffer for differential and single-ended signals	Issued	Lattice Semiconductor Corporation
10/367,323	6812869	United States	Noise Reduction Techniques For Programmable I/O Circuits	Issued	Lattice Semiconductor Corporation
10/370,232	6861870	United States	Dynamic Cross point Switch With Shadow Memory Architecture	Issued	Lattice Semiconductor Corporation
10/377,320	6859066	United States	Bank based input/output buffers in field programmable gate arrays with multiple reference voltages	Issued	Lattice Semiconductor Corporation
10/387,814	7305047	United States	Automatic lane assignment for Receiver	Issued	Lattice Semiconductor Corporation
10/387,243	7339952	United States	Pointer Processing For Optical Communication Systems	Issued	Lattice Semiconductor Corporation
10/391,094	6870395	United States	PLDs With Integrated Standard Cell Logic Blocks	Issued	Lattice Semiconductor Corporation
10/392,751	RE39510	United States	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	Issued	Lattice Semiconductor Corporation
10/397,669	6967500	United States	Electronic Circuit With OnChip Programmable Terminations	Issued	Lattice Semiconductor Corporation
10/400,705	6873187	United States	Method and Apparatus for Controlling Signal Distribution In An Electronic	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 439/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Circuit		
10/406,050	7000212	United States	Hierarchical General Interconnect Architecture For High Density FPGA's	Issued	Lattice Semiconductor Corporation
10/409,543	6986004	United States	FIFO memory with programmable data port widths	Issued	Lattice Semiconductor Corporation
10/417,290	6879184	United States	Programmable logic device architecture based on arrays of LUT-based Boolean terms	Issued	Lattice Semiconductor Corporation
10/425,863	6903575	United States	Scalable device architecture for high-speed interfaces	Issued	Lattice Semiconductor Corporation
10/425,862	6894530	United States	Programmable And Fixed Logic Circuitry For High-Speed Interfaces	Issued	Lattice Semiconductor Corporation
10/428,889	6879182	United States	CPLD with multi-function blocks and distributed memory	Issued	Lattice Semiconductor Corporation
10/428,885	6861871	United States	Cascaded logic block architecture for complex programmable logic devices	Issued	Lattice Semiconductor Corporation
10/428,888	6864713	United States	Multi-Stage Interconnect Architecture For Complex Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/428,982	6922078	United States	Enhanced wide and deep logic capability for high density, high performance CPLDs	Issued	Lattice Semiconductor Corporation
10/439,602	6828823	United States	Non-volatilie and reconfigurable PLDs	Issued	Lattice Semiconductor Corporation
10/441,814	7039842	United States	Measuring Propagation Delays of Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/447,120	7301996	United States	skew cancellation for source synchronous clock and data signals	Issued	Lattice Semiconductor Corporation
10/447,451	7009433	United States	Digitally Controlled Delay Cells	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 440/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/457,630	7304863	United States	Integrated Circuit Including External Electronic Components With Low Insertion Loss	Issued	Lattice Semiconductor Corporation
10/459,091	6879598	United States	Flexible Media Access Control Architecture	Issued	Lattice Semiconductor Corporation
10/460,385	6856171	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
10/463,781	6861868	United States	High Speed Interface For A Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/464,083	6882555	United States	Bi-directional buffering for memory data lines	Issued	Lattice Semiconductor Corporation
10/600,042	6822477	United States	Integrated Circuit And Associated Design Method Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/610,253	6977408	United States	High-Performance Non-volatile Memory Device and Fabrication Process	Issued	Lattice Semiconductor Corporation
10/613,460	7132903	United States	Noise-shielding, switch-controlled load circuitry for oscillators and the like	Issued	Lattice Semiconductor Corporation
10/613,462	6952115	United States	Programmable I/O Interfaces For FPGAs And Other PLDs	Issued	Lattice Semiconductor Corporation
10/617,980	6958625	United States	PLD With Hardwired Microsequencer	Issued	Lattice Semiconductor Corporation
10/619,711	6903573	United States	Programmable Logic Device With Enhanced Wide Input Product Term Cascading	Issued	Lattice Semiconductor Corporation
10/620,286	6919736	United States	FPGA having partitionable embedded memory with configurable depth and width	Issued	Lattice Semiconductor Corporation
10/619,645	7098685	United States	Scalable Serializer-Deserializer Architecture and	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 441/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Programmable Interface		Corporation
10/620,147	7032203	United States	Algorithm to increase logic input width by cascading product terms	Issued	Lattice Semiconductor Corporation
10/624,965	6940309	United States	Programmable Logic Device With A Memory-Based Finite State Machine	Issued	Lattice Semiconductor Corporation
10/626,089	6737702	United States	Zero Power Memory Cell with Reduced Threshold Voltage	Issued	Lattice Semiconductor Corporation
10/628,656	6970047	United States	Programmable lock detector and corrector	Issued	Lattice Semiconductor Corporation
10/628,657	6924659	United States	Programmable Signal Termination for FPGAs and the Like	Issued	Lattice Semiconductor Corporation
10/629,223	7019577	United States	Clock Generator	Issued	Lattice Semiconductor Corporation
10/629,512	6903574	United States	Memory Access Via Serial Memory Interface	Issued	Lattice Semiconductor Corporation
10/629,221	6885227	United States	Clock Generator With Skew Control	Issued	Lattice Semiconductor Corporation
10/640,804	6877667	United States	Integrated Circuit And Associated Design Method With Antenna Error Control Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/640,828	6838904	United States	Enhanced CPLD Macrocell Module Having Selectable Bypass of Steering-Based Resource Allocation	Issued	Lattice Semiconductor Corporation
10/641,260	6940779	United States	Programmable broadcasting initialization of embedded memory blocks on FPGA	Issued	Lattice Semiconductor Corporation
10/642,370	6924664	United States	FPGA	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 442/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/655,686	6842037	United States	Shared Transmission Line Communication System and Method	Issued	Lattice Semiconductor Corporation
10/660,814	7038490	United States	Delay matched ASIC conversion of a PLD	Issued	Lattice Semiconductor Corporation
10/665,920	6970022	United States	Controlled hysteresis comparator with rail-to-rail input	Issued	Lattice Semiconductor Corporation
10/671,378	6943583	United States	Programmable I/O structure for FPGAs and the like having reduced pad capacitance	Issued	Lattice Semiconductor Corporation
10/671,363	6943582	United States	Programmable I/O structure for FPGAs and the Like Having Shared Circuitry	Issued	Lattice Semiconductor Corporation
10/671,756	6909663	United States	Multiport Memory With Twisted Bitlines	Issued	Lattice Semiconductor Corporation
10/676,536	7269771	United States	Semiconductor Device Adapted For Forming Multiple Scan Chains	Issued	Lattice Semiconductor Corporation
10/687,468	6809674	United States	Analog-to-digital converters	Issued	Lattice Semiconductor Corporation
10/699,321	7067883	United States	Lateral High-Voltage Junction Device	Issued	Lattice Semiconductor Corporation
10/701,005	7091763	United States	Clock generation	Issued	Lattice Semiconductor Corporation
10/704,025	7088134	United States	PLD With Flexible Memory Allocation And Routing	Issued	Lattice Semiconductor Corporation
10/726,972	7100058	United States	Programmable Power Management System And Method	Issued	Lattice Semiconductor Corporation
10/728,685	7187157	United States	Power supply remote voltage sensing	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 443/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/737,514	6981381	United States	Linear Thermoelectric Device Driver	Issued	Lattice Semiconductor Corporation
10/744,353	7132864	United States	Method for configuring multiple-output phase-locked loop frequency synthesizer	Issued	Lattice Semiconductor Corporation
10/769,174	7024646	United States	Electrostatic Discharge Simulation	Issued	Lattice Semiconductor Corporation
10/768,643	7019584	United States	Output Stages For High Current Low Noise Bandgap Reference Circuit Implementations	Issued	Lattice Semiconductor Corporation
10/782,564	6972986	United States	Combination FPGA	Issued	Lattice Semiconductor Corporation
10/783,886	7081771	United States	Upgradeable And Reconfigurable Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/791,073	7191388	United States	Fast diagonal interleaved parity (DIP) calculator	Issued	Lattice Semiconductor Corporation
10/794,079	7257727	United States	Timer Systems and Methods	Issued	Lattice Semiconductor Corporation
10/794,524	7017063	United States	systems and methods for controlling voltage regulator module power supplies	Issued	Lattice Semiconductor Corporation
10/794,498	7028201	United States	Powering up a device having digital and analog circuitry	Issued	Lattice Semiconductor Corporation
10/797,759	7068556	United States	Sense Amplifier Systems and Methods	Issued	Lattice Semiconductor Corporation
10/809,180	7234030	United States	Table based scheduler for FIFOs and the like	Issued	Lattice Semiconductor Corporation
10/809,658	7095247	United States	Configuring FPGAs and the like using one or more serial memory devices	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 444/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/815,403	7167032	United States	Self-adjusting schmitt trigger	Issued	Lattice Semiconductor Corporation
10/817,215	7081781	United States	Charge pump for a low-voltage wide-tuning range phase-locked loop	Issued	Lattice Semiconductor Corporation
10/829,865	6998896	United States	Dynamic gain adjustment systems and method for metastability resistance	Issued	Lattice Semiconductor Corporation
10/834,528	6998906	United States	Low pass filter systems and methods	Issued	Lattice Semiconductor Corporation
10/837,086	7307319	United States	High Voltage Protection Device And Process	Issued	Lattice Semiconductor Corporation
10/842,345	7002418	United States	Control Signal Generation ...	Issued	Lattice Semiconductor Corporation
10/841,987	7224213	United States	switched-capacitor ripple-smoothing filter	Issued	Lattice Semiconductor Corporation
10/843,708	7061269	United States	IO buffer architecture for programmable devices	Issued	Lattice Semiconductor Corporation
10/856,100	7196551	United States	Current Mode Logic Buffer	Issued	Lattice Semiconductor Corporation
10/857,667	7064973	United States	Combination FPGA	Issued	Lattice Semiconductor Corporation
10/885,419	7116585	United States	Memory Systems And Methods	Issued	Lattice Semiconductor Corporation
10/910,091	7215591	United States	Byte enable logic for memory	Issued	Lattice Semiconductor Corporation
10/912,943	7471752	United States	Data Transmission Synchronization	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 445/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/928,563	7078286	United States	Process for fabricating a semiconductor device having electrically isolated low voltage and high voltage regions	Issued	Lattice Semiconductor Corporation
10/929,199	7484144	United States	Testing embedded memory in an integrated circuit	Issued	Lattice Semiconductor Corporation
10/944,978	7135886	United States	FPGA Using Both Volatile and NonVolatile Memory Cell Properties	Issued	Lattice Semiconductor Corporation
10/974,453	7307912	United States	Variable data width memory systems and methods	Issued	Lattice Semiconductor Corporation
10/973,750	7149129	United States	memory output data systems and methods with feedback	Issued	Lattice Semiconductor Corporation
10/974,107	7164290	United States	FPGA Logic Unit	Issued	Lattice Semiconductor Corporation
10/974,305	7129749	United States	PLD Having A Configurable DRAM With Transparent Refresh	Issued	Lattice Semiconductor Corporation
10/978,899	7376872	United States	Testing embedded memory in integrated circuits such as progammable logic circuits	Issued	Lattice Semiconductor Corporation
10/996,283	7161862	United States	Low power asynchronous sense amp	Issued	Lattice Semiconductor Corporation
11/007,954	7230810	United States	Dynamic over-voltage protection scheme for integrated circuit devices	Issued	Lattice Semiconductor Corporation
11/012,550	7215149	United States	Interface circuitry for electrical systems	Issued	Lattice Semiconductor Corporation
11/012,548	7215148	United States	Programmable current LVDS output buffer	Issued	Lattice Semiconductor Corporation
11/015,265	7177221	United States	Method of initializing configurable multi-port	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 446/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			embedded memory blocks in an FPGA		Corporation
11/016,665	7187203	United States	Cascadable memory	Issued	Lattice Semiconductor Corporation
11/015,369	7177207	United States	Sense amplifier timing	Issued	Lattice Semiconductor Corporation
11/036,630	7257750	United States	Self-verification of configuration memory in PLDs	Issued	Lattice Semiconductor Corporation
11/036,738	7242053	United States	EEPROM Device with voltage-limiting charge pump circuit	Issued	Lattice Semiconductor Corporation
11/040,772	7208975	United States	Serdes with programmable I/O architecture	Issued	Lattice Semiconductor Corporation
11/041,319	7183798	United States	Synchronous memory	Issued	Lattice Semiconductor Corporation
11/044,089	7109754	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
11/044,149	7109756	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
11/044,508	7034599	United States	Clock Generator With Skew Control	Issued	Lattice Semiconductor Corporation
11/054,011	7221607	United States	Mult-port memory systems and methods for bit line coupling	Issued	Lattice Semiconductor Corporation
11/055,280	6975137	United States	PLDs With Integrated Standard Cell Logic Blocks	Issued	Lattice Semiconductor Corporation
11/054,750	7382293	United States	Data Decompression	Issued	Lattice Semiconductor Corporation
11/054,855	7589648	United States	Data Decompression	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 447/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/064,477	7532646	United States	Distributed multiple channel alignment scheme	Issued	Lattice Semiconductor Corporation
11/071,356	7245154	United States	Differential Input Receiver with Programmable Failsafe	Issued	Lattice Semiconductor Corporation
11/070,926	7057397	United States	Output Impedance Measurement Techniques	Issued	Lattice Semiconductor Corporation
11/083,625	7376204	United States	Detection of Unknown symbol rate in a digitally modulated signal	Issued	Lattice Semiconductor Corporation
11/098,713	7265578	United States	In-System Programming Of a Non-Compliant Device Using Multiple Interfaces Of A PLD	Issued	Lattice Semiconductor Corporation
11/100,718	7397274	United States	In-System Programming Of a Non-Compliant Device Using Multiple Interfaces Of A PLD	Issued	Lattice Semiconductor Corporation
11/108,927	7193436	United States	Fast Processing Path Using FPGA Logic Units	Issued	Lattice Semiconductor Corporation
11/109,301	7630464	United States	Analog-to-digital systems and methods	Issued	Lattice Semiconductor Corporation
11/109,966	6977521	United States	FPGA	Issued	Lattice Semiconductor Corporation
11/121,326	7400171	United States	Electronic Switch Having Extended Voltage Range	Issued	Lattice Semiconductor Corporation
11/134,152	7009423	United States	Programmable I/O Interfaces For FPGAs And Other PLDs	Issued	Lattice Semiconductor Corporation
11/157,345	7685483	United States	Design-For-Test features for a memory in an FPGA	Issued	Lattice Semiconductor Corporation
11/157,349	7378879	United States	Decoding systems and methods	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 448/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/165,709	7256613	United States	Programmable Interconnect Architecture for PLDs	Issued	Lattice Semiconductor Corporation
11/165,853	7342838	United States	PLD With A Double Data Rate SDRAM Interface	Issued	Lattice Semiconductor Corporation
11/185,242	7519139	United States	Signal monitoring systems and methods	Issued	Lattice Semiconductor Corporation
11/187,179	7342846	United States	address decoding systems and methods	Issued	Lattice Semiconductor Corporation
11/187,114	7253674	United States	Fine output clock phase alignment circuitry	Issued	Lattice Semiconductor Corporation
11/189,067	7505752	United States	Receiver used for differential signaling and reference voltage signaling with programmable common mode	Issued	Lattice Semiconductor Corporation
11/194,871	7414913	United States	Bitline twisting scheme for a multiport memory	Issued	Lattice Semiconductor Corporation
11/194,356	7262630	United States	Dynamic programmable termination for parallel and differential schemes	Issued	Lattice Semiconductor Corporation
11/199,287	7599457	United States	clock-and-data-recovery system having a multi-phase clock generator for one or more channel circuits	Issued	Lattice Semiconductor Corporation
11/200,983	7295035	United States	Programmable Logic Device With Enhanced Logic Block Architecture	Issued	Lattice Semiconductor Corporation
11/200,941	7411419	United States	I/O Systems and Methods	Issued	Lattice Semiconductor Corporation
11/202,149	7606851	United States	Correlator having user-defined processing	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 449/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/201,620	7187586	United States	Flash memory erase verification systems and methods	Issued	Lattice Semiconductor Corporation
11/206,282	RE40311	United States	Zero Power Programmable Memory Cell	Issued	Lattice Semiconductor Corporation
11/226,695	7301182	United States	Circuit layout for improved performance while preserving or improving density	Issued	Lattice Semiconductor Corporation
11/230,087	7167405	United States	Data transfer verification systems and methods	Issued	Lattice Semiconductor Corporation
11/235,616	7376037	United States	PLD with power-saving architecture	Issued	Lattice Semiconductor Corporation
11/236,967	7405446	United States	Electrostatic Protection Systems and Methods	Issued	Lattice Semiconductor Corporation
11/243,255	7088132	United States	Configuring FPGAs and the like using one or more serial memory devices	Issued	Lattice Semiconductor Corporation
11/251,682	7196963	United States	Address isolation for user-defined configuration memory in programmable devices	Issued	Lattice Semiconductor Corporation
11/252,094	7263024	United States	Clock reset address decoder for block memory	Issued	Lattice Semiconductor Corporation
11/252,126	7061275	United States	FPGA	Issued	Lattice Semiconductor Corporation
11/257,137	7685215	United States	Fast-carry arithmetic circuit using a multi-input LUT	Issued	Lattice Semiconductor Corporation
11/257,641	7317343	United States	PULSE-GENERATION CIRCUIT HAVING PULSE GENERATORS AND SET-RESET LATCHES	Issued	Lattice Semiconductor Corporation
11/260,097	7212051	United States	Control signal generation for a low jitter switched-capacitor frequency synthesizer	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 450/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/281,651	7495495	United States	Digital I/O Timing Control	Issued	Lattice Semiconductor Corporation
11/287,720	7327159	United States	Interface Block Architectures	Issued	Lattice Semiconductor Corporation
11/290,205	7242634	United States	Pseudo-dynamic word-line driver	Issued	Lattice Semiconductor Corporation
11/293,941	7538574	United States	Transparent Field Reconfiguration for PLDs	Issued	Lattice Semiconductor Corporation
11/302,097	7620839	United States	Jitter Tolerant Delay-Locked Loop Circuit	Issued	Lattice Semiconductor Corporation
11/300,886	7495467	United States	Temperature independent, linear on-chip termination resistance	Issued	Lattice Semiconductor Corporation
11/332,986	7382169	United States	Systems and Methods for Reducing Static Phase Error	Issued	Lattice Semiconductor Corporation
11/335,890	7439783	United States	Phase-Locked Loop Systems And Methods	Issued	Lattice Semiconductor Corporation
11/345,713	7547995	United States	dynamic over voltage protection scheme for interface circuitry	Issued	Lattice Semiconductor Corporation
11/346,817	7554357	United States	Efficient Configuration of Daisy-Chained Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
11/350,436	7375549	United States	Reconfiguration of PLDs	Issued	Lattice Semiconductor Corporation
11/356,805	7277348	United States	Memory Cell Comprising And OTP NV Memory Unit And SRAM Unit	Issued	Lattice Semiconductor Corporation
11/360,337	7355441	United States	PLD with distributed memory and non-volatile memory	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 451/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/361,584	7596744	United States	Auto recovery from volatile soft error upsets (SEUs)	Issued	Lattice Semiconductor Corporation
11/362,289	7759926	United States	dynamic phase offset measurement	Issued	Lattice Semiconductor Corporation
11/361,643	7446573	United States	Comparator Systems And Methods	Issued	Lattice Semiconductor Corporation
11/398,437	7459931	United States	PLDs with transparent field reconfiguration	Issued	Lattice Semiconductor Corporation
11/397,985	7554358	United States	PLDs with user non-volatile memory	Issued	Lattice Semiconductor Corporation
11/416,881	7623378	United States	Selective programming of non-volatile memory facilitated by security fuses	Issued	Lattice Semiconductor Corporation
11/435,956	7102934	United States	Sense Amplifier Systems and Methods	Issued	Lattice Semiconductor Corporation
11/442,186	7411417	United States	Selective loading of configuration data into configuration memory cells	Issued	Lattice Semiconductor Corporation
11/446,548	7378873	United States	PLD providing a serial peripheral interface	Issued	Lattice Semiconductor Corporation
11/445,620	7378872	United States	PLD architecture with multiple slice types	Issued	Lattice Semiconductor Corporation
11/446,542	7385417	United States	Dual slice architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/446,351	7397276	United States	Logic block control architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/446,308	7546498	United States	PLDs with custom identification systems and methods	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 452/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/446,309	7495970	United States	Flexible memory architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/447,591	7631223	United States	PLD methods and systems for providing multi-boot configuration data support	Issued	Lattice Semiconductor Corporation
11/452,714	7463060	United States	PLD and method of testing	Issued	Lattice Semiconductor Corporation
11/455,315	7215139	United States	Upgradeable And Reconfigurable Programmable Logic Device	Issued	Lattice Semiconductor Corporation
11/425,273	7702100	United States	Key generation for advanced encryption standard (AES) decryption and the like	Issued	Lattice Semiconductor Corporation
11/425,881	7657773	United States	Clock distribution chip for generating both zero-delay and non-zero-delay clock signals	Issued	Lattice Semiconductor Corporation
11/477,759	7348914	United States	Methods and systems to align output signals of an analog-to-digital converter	Issued	Lattice Semiconductor Corporation
11/487,647	7636259	United States	Flash memory array with independently erasable sectors	Issued	Lattice Semiconductor Corporation
11/487,751	7512015	United States	Negative voltage blocking for embedded memories	Issued	Lattice Semiconductor Corporation
11/492,687	7466190	United States	Charge pump with four-well transistors	Issued	Lattice Semiconductor Corporation
11/494,862	7521969	United States	Switch sequencing circuit systems and methods	Issued	Lattice Semiconductor Corporation
11/461,222	7411432	United States	Integrated circuits and complementary CMOS circuits for frequency dividers	Issued	Lattice Semiconductor Corporation
11/498,645	7675313	United States	Methods and systems for storing a security key using programmable fuses	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 453/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/498,646	7605606	United States	Area efficient routing architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/530,620	7456672	United States	Clock systems and methods	Issued	Lattice Semiconductor Corporation
11/533,188	7511641	United States	Efficient bitstream compression	Issued	Lattice Semiconductor Corporation
11/551,459	7831754	United States	Multiple Communication Channel Configuration Systems And Methods	Issued	Lattice Semiconductor Corporation
11/556,528	7663401	United States	Multiplexer initialization systems and methods	Issued	Lattice Semiconductor Corporation
11/593,274	7535258	United States	Programmable Voltage LVDS Output Buffer	Issued	Lattice Semiconductor Corporation
11/557,808	7725803	United States	PLD programming verification systems and methods	Issued	Lattice Semiconductor Corporation
11/638,156	7429875	United States	Low Static Current Drain Logic Circuit	Issued	Lattice Semiconductor Corporation
11/643,288	7443192	United States	Output buffer with digital slew control	Issued	Lattice Semiconductor Corporation
11/624,021	7623391	United States	Data transfer verification systems and methods	Issued	Lattice Semiconductor Corporation
11/671,948	7576563	United States	Flexible High Fan-out Signal Routing Systems and Methods	Issued	Lattice Semiconductor Corporation
11/675,246	7313025	United States	Flash memory erase verification systems and methods	Issued	Lattice Semiconductor Corporation
11/676,071	7430706	United States	Fast diagonal interleaved parity (DIP) calculator	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 454/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/680,526	7598765	United States	Redundancy for Configuration RAM	Issued	Lattice Semiconductor Corporation
11/691,003	7536615	United States	Logic analyzer systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/691,040	7743296	United States	Logic analyzer systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/737,702	7509598	United States	Clock Boosting Systems and Methods	Issued	Lattice Semiconductor Corporation
11/750,790	7401280	United States	Self-verification of configuration memory in PLDs	Issued	Lattice Semiconductor Corporation
11/750,616	7632011	United States	Integrated Circuit Temperature Sensors Systems and Methods	Issued	Lattice Semiconductor Corporation
11/760,411	8065574	United States	Real Soft Error Detect Scheme for Testing	Issued	Lattice Semiconductor Corporation
11/761,221	7570078	United States	PLD Providing A Serial Peripheral Interfaces	Issued	Lattice Semiconductor Corporation
11/778,457	7573770	United States	Distributed front-end FIFO for source-synchronized interfaces with non-continuous clocks	Issued	Lattice Semiconductor Corporation
11/779,246	7446679	United States	FPGA data compression using combined RLE BE, LZ, Row LZ and BE ROW encoding	Issued	Lattice Semiconductor Corporation
11/863,016	7681160	United States	Weight based look up table collapsing for programmable logic devices	Issued	Lattice Semiconductor Corporation
11/865,556	7539076	United States	Variable data width memory systems and methods	Issued	Lattice Semiconductor Corporation
11/869,019	7616029	United States	Hysteresis-based processing for applications such as signal bias monitors	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 455/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/872,950	7586344	United States	Dynamic delay or advance adjustment of oscillating signal phase	Issued	Lattice Semiconductor Corporation
11/875,748	7757198	United States	Scan chain systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/877,434	7411414	United States	Single-Ended Output Driver Buffer	Issued	Lattice Semiconductor Corporation
11/924,088	8132040	United States	Channel-to-channel deskew systems and methods	Issued	Lattice Semiconductor Corporation
11/934,711	7573291	United States	Programmable Logic Device With Enhanced Logic Block Architecture	Issued	Lattice Semiconductor Corporation
11/937,328	7788620	United States	An IO placement systems and methods to reduce SSO noise	Issued	Lattice Semiconductor Corporation
11/937,300	7895555	United States	Simultaneous Switching Output Noise Estimation and Reduction Systems and Methods	Issued	Lattice Semiconductor Corporation
11/939,787	7863931	United States	Flexible Delay Cell Architecture	Issued	Lattice Semiconductor Corporation
11/941,031	7902865	United States	Compression and decompression of configuration data using repeated data frames	Issued	Lattice Semiconductor Corporation
11/941,006	7535253	United States	Method of Retaining Register Data during Field Update of PLD	Issued	Lattice Semiconductor Corporation
11/947,662	7788623	United States	Composite wire indexing for PLDs	Issued	Lattice Semiconductor Corporation
11/949,130	7586325	United States	IC having independent voltage and process/temperature control	Issued	Lattice Semiconductor Corporation
12/001,600	7728625	United States	Serial interface for PLDs	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 456/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/957,598	7605609	United States	A programmable level shifter optimized for high performance and low power.	Issued	Lattice Semiconductor Corporation
11/959,329	7630259	United States	PLD with built in self test	Issued	Lattice Semiconductor Corporation
11/970,212	7646643	United States	Process charging monitor for nonvolatile memory	Issued	Lattice Semiconductor Corporation
12/019,526	7787326	United States	PLD With Mult-Rate SDRAM Interface	Issued	Lattice Semiconductor Corporation
12/021,202	8069329	United States	Dynamic Multiple Pattern Configuration Scheme For Volatile FPGAs	Issued	Lattice Semiconductor Corporation
12/044,842	7652500	United States	Reconfiguration of PLDs	Issued	Lattice Semiconductor Corporation
12/055,170	7890913	United States	Wire Mapping For PLDs	Issued	Lattice Semiconductor Corporation
12/060,776	7459935	United States	PLD With Distributed Memory	Issued	Lattice Semiconductor Corporation
12/061,885	7831856	United States	Detection of Timing Errors in Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/099,933	7661878	United States	On-Chip Temperature Sensor For An Integrated Circuit	Issued	Lattice Semiconductor Corporation
12/100,859	7558143	United States	Programmable Logic Device With Power-Saving Architecture	Issued	Lattice Semiconductor Corporation
12/105,146	7557606	United States	Synchronization Of Data Signals And Clock Signals For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/105,959	7696784	United States	PLD With Multiple Slice	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 457/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Types		Corporation
12/107,883	7560953	United States	Power Management Systems And Methods for PLDs	Issued	Lattice Semiconductor Corporation
12/122,489	7897448	United States	Formation Of High Voltage Transistor With High Breakdown Voltage	Issued	Lattice Semiconductor Corporation
12/146,042	8463832	United States	Digital Signal Processing Block Architecture For PLD	Issued	Lattice Semiconductor Corporation
12/164,265	7592834	United States	Logic Block Control Architectures For PLDs	Issued	Lattice Semiconductor Corporation
12/182,940	8261160	United States	Serial data recovery out of 8 samples with FPGAs	Issued	Lattice Semiconductor Corporation
12/186,027	7579865	United States	Selective Loading Of Configuration Data Into Configuration Memory Cells	Issued	Lattice Semiconductor Corporation
12/188,120	7605602	United States	Low-Power Output Driver Buffer Circuit	Issued	Lattice Semiconductor Corporation
12/238,959	7911229	United States	Programmable Signal Routing Systems	Issued	Lattice Semiconductor Corporation
12/273,868	7663419	United States	Clock Systems And Methods	Issued	Lattice Semiconductor Corporation
12/277,217	8112731	United States	Congestion-driven placement based on region interconnection for FPGA	Issued	Lattice Semiconductor Corporation
12/323,974	7992120	United States	congestion estimation based on pass probability net estimation process	Issued	Lattice Semiconductor Corporation
12/327,128	7656193	United States	Programmable Logic Device And Method Of Testing	Issued	Lattice Semiconductor Corporation
12/337,502	8856718	United States	Precise Congestion Estimation for FPGA Router	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 458/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
12/341,929	8181139	United States	Multi-Priority Placement	Issued	Lattice Semiconductor Corporation
12/370,039	7714608	United States	Temperature-Independent, Linear On-Chip Termination Resistance	Issued	Lattice Semiconductor Corporation
12/389,149	7957208	United States	Flexible memory architectures for PLDs	Issued	Lattice Semiconductor Corporation
12/402,751	7844243	United States	Receiver used for differential signaling and reference voltage signaling with programmable common mode	Issued	Lattice Semiconductor Corporation
12/406,772	8069431	United States	An alternative method for pin swapping in FPGA routing	Issued	Lattice Semiconductor Corporation
12/408,047	8086986	United States	Clock Boosting Systems And Methods	Issued	Lattice Semiconductor Corporation
12/409,757	7675321	United States	Dual-Slice Architectures For PLDs	Issued	Lattice Semiconductor Corporation
12/413,787	7808405	United States	Efficient Bitstream Compression	Issued	Lattice Semiconductor Corporation
12/430,848	7741865	United States	Soft Error Upset Hardened Integrated Circuit Systems And Methods	Issued	Lattice Semiconductor Corporation
12/464,822	7876125	United States	Method of Retaining Register Data during Field Update of PLD	Issued	Lattice Semiconductor Corporation
12/465,444	7868654	United States	Economical way to improve volatile FPGA boot up data throughput by utilizing one or more SPI boot PROMs w/o sacrificing additional FPGA pins	Issued	Lattice Semiconductor Corporation
12/467,800	7737723	United States	Transparent Field Reconfiguration for PLDs	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 459/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
12/476,155	8044682	United States	FPGA Having Low Power, Fast Carry Chain	Issued	Lattice Semiconductor Corporation
12/480,565	7702977	United States	PLDs with custom identification systems and methods	Issued	Lattice Semiconductor Corporation
12/494,822	8165164	United States	Circuit For In-System Reconfigurable Mapping Of IQ Data Into A CPRI Basic Frame	Issued	Lattice Semiconductor Corporation
12/502,141	7724029	United States	Power Management For Integrated Circuits Such As Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/511,388	7768300	United States	PLD Providing A Serial Peripheral Interfaces	Issued	Lattice Semiconductor Corporation
12/512,944	8255733	United States	Method of selecting precise delay or skew shifts	Issued	Lattice Semiconductor Corporation
12/512,961	7969248	United States	VCO digital center frequency coarse tune algorithm	Issued	Lattice Semiconductor Corporation
12/538,810	7808855	United States	Distributed front-end FIFO for source-synchronized interfaces with non-continuous clocks	Issued	Lattice Semiconductor Corporation
12/561,140	8010871	United States	Auto recovery from volatile soft error upsets (SEUs)	Issued	Lattice Semiconductor Corporation
12/564,781	7746107	United States	Redundancy for Configuration RAM	Issued	Lattice Semiconductor Corporation
12/578,470	8122277	United States	Clock distribution chip	Issued	Lattice Semiconductor Corporation
12/578,492	8112656	United States	Clock distribution chip	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 460/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/607,868	7989911	United States	STI with trench liner of increased thickness	Issued	Lattice Semiconductor Corporation
12/607,333	7985656	United States	STI with trench liner of increased thickness	Issued	Lattice Semiconductor Corporation
12/611,262	8059470	United States	Flash memory array with independently erasable sectors	Issued	Lattice Semiconductor Corporation
12/626,289	7944765	United States	PLD with built in self test	Issued	Lattice Semiconductor Corporation
12/630,163	8060784	United States	PLD And Methods For Providing Multi-Boot Configuration Data Support	Issued	Lattice Semiconductor Corporation
12/637,884	8200179	United States	Combined Variable Gain Amplifier And Linear Equalizer With Independent Gain And Frequency Control	Issued	Lattice Semiconductor Corporation
12/698,283	8040152	United States	IO Ring Configuration Scheme with sharing of BC7 register	Issued	Lattice Semiconductor Corporation
12/706,227	7924054	United States	Latency measurement circuit for wireless communications applications	Issued	Lattice Semiconductor Corporation
12/709,685	7834652	United States	Methods and systems for storing a security key using programmable fuses	Issued	Lattice Semiconductor Corporation
12/729,952	8040159	United States	High Speed Comparator with Data Dependent Jitter Mitigation	Issued	Lattice Semiconductor Corporation
12/752,455	8384427	United States	Serial Peripheral Interface Daisy Chaining using a Flow-Through Option	Issued	Lattice Semiconductor Corporation
12/757,087	8664774	United States	A Method for Arranging IC Bondwires for the Reduction of Crosstalk	Issued	Lattice Semiconductor Corporation
12/786,359	8108754	United States	PLD programming verification systems and methods	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 461/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/813,540	8164499	United States	Shared-Array Multiple-Output Digital to Analog Converter	Issued	Lattice Semiconductor Corporation
12/813,573	8441292	United States	Method of delaying data from clock in 1UI steps	Issued	Lattice Semiconductor Corporation
12/818,544	7868646	United States	Soft Error Upset Hardened Integrated Circuit Systems And Methods	Issued	Lattice Semiconductor Corporation
12/871,764	8286116	United States	Composite Wire Indexing For PLDs	Issued	Lattice Semiconductor Corporation
12/977,011	8522126	United States	Method Of Blocking PLC Distributed SRAM Readback In User Mode	Issued	Lattice Semiconductor Corporation
12/976,412	8351287	United States	Bitline Floating Circuit For Power Reduction On SRAM Array	Issued	Lattice Semiconductor Corporation
12/976,520	8477549	United States	Strobed And Latched Readback Of SRAM Bits In A FPGA	Issued	Lattice Semiconductor Corporation
12/987,393	8274412	United States	Low Power SerDes With Built- In Word Alignment For Odd And Even Gearing Ratios	Issued	Lattice Semiconductor Corporation
13/006,622	8384428	United States	Programmable IO Pad - embedded function block	Issued	Lattice Semiconductor Corporation
13/007,804	8248136	United States	Low Power And Glitch-less Delay Element For High Speed Receiver Interface	Issued	Lattice Semiconductor Corporation
13/007,688	8324934	United States	Programmable Ratio Input Buffer	Issued	Lattice Semiconductor Corporation
13/026,555	8104009	United States	Wire Mapping For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
13/034,174	8058898	United States	Compression and Decompression Of Configuration Data Using	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 462/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Repeated Data Frames		
13/038,259	8368424	United States	Wakeup from sleep mode using slave I2C port or slave SPI port with powered down core logic	Issued	Lattice Semiconductor Corporation
13/038,270	8816718	United States	Slow Respond Mode Protocol For Synchronous Read	Issued	Lattice Semiconductor Corporation
13/037,703	8654600	United States	Current Sense Amplifier With Low Voltage Operation	Issued	Lattice Semiconductor Corporation
13/052,142	8553463	United States	Positive-To-Negative Voltage Discharge Circuit	Issued	Lattice Semiconductor Corporation
13/076,300	8319521	United States	Safe programming of key information into NV memory	Issued	Lattice Semiconductor Corporation
13/079,578	8314634	United States	Power Saving Standby Mode With Glitch-Less Output Controls	Issued	Lattice Semiconductor Corporation
13/079,595	8531222	United States	PLL Switchable Feedback Loops Among Internal And External Feedback Paths	Issued	Lattice Semiconductor Corporation
13/083,889	8138790	United States	Latency measurement circuit for wireless communications applications	Issued	Lattice Semiconductor Corporation
13/154,885	8441284	United States	Flexible Way To Incrementally Update Multi-Bit Data Registers	Issued	Lattice Semiconductor Corporation
13/155,547	8547075	United States	Filter And Stability Capacitor Reuse For On-Chip Dual Output Voltage Regulators	Issued	Lattice Semiconductor Corporation
13/164,108	8555217	United States	Cross-Probing Technology Between Software Plug-In Modules	Issued	Lattice Semiconductor Corporation
13/178,599	8539409	United States	Multiple silicon products from a common base set of masks	Issued	Lattice Semiconductor Corporation
13/178,536	8495264	United States	Packet And Control Symbol	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 463/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Alignment Circuit For SRIO		Corporation
13/193,984	8314632	United States	Placing ICs Into Ultra-Low Voltage Mode For Standby Purposes	Issued	Lattice Semiconductor Corporation
13/212,121	8451679	United States	Bit-Line Clamping Circuit To Improve Write Performance Of Dual-Port SRAM	Issued	Lattice Semiconductor Corporation
13/275,102	8169237	United States	High Speed Comparator with Data Dependent Jitter Mitigation	Issued	Lattice Semiconductor Corporation
13/299,507	8370691	United States	Testing of Soft Error Detection Logic For PLDs	Issued	Lattice Semiconductor Corporation
13/452,060	8823561	United States	In-System Reconfigurable Circuit For Mapping Data Words Of Different Lengths	Issued	Lattice Semiconductor Corporation
13/585,142	8461894	United States	Low Power And Glitch-less Delay Element For High Speed Receiver Interface	Issued	Lattice Semiconductor Corporation
13/616,173	8912933	United States	Low Power SerDes With Built- In Word Alignment For Odd And Even Gearing Ratios	Issued	Lattice Semiconductor Corporation
13/653,827	8710898	United States	Bandgap Reference Circuit Design With Triple-Trim Methodology For Mass Production	Issued	Lattice Semiconductor Corporation
13/680,947	8643398	United States	Placing ICs Into Low Voltage Mode For Standby Purposes	Issued	Lattice Semiconductor Corporation
13/685,385	8643168	United States	Input Capacitance Compensation In Package	Issued	Lattice Semiconductor Corporation
13/721,867	8686773	United States	In-System Margin Measurement Circuit	Issued	Lattice Semiconductor Corporation
13/738,265	8797064	United States	Low power, optimized H-bridge and CML driver	Issued	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 464/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
13/764,221	RE45200	United States	Programmable Signal Routing Systems Having Low Static Leakage	Issued	Lattice Semiconductor Corporation
13/857,919	8786482	United States	Analog-To-Digital-Converter	Issued	Lattice Semiconductor Corporation
13/892,948	8648636	United States	Method of Delaying Data from Clock in 1UI steps	Issued	Lattice Semiconductor Corporation
14/040,955	8829944	United States	Dynamic Power Supply Switching For Clock Signals	Issued	Lattice Semiconductor Corporation
13/155,261		United States	JTAG Based Parallel Measuring And Trimming for Time Based Parameters	Pending	Lattice Semiconductor Corporation
13/412,408		United States	Double Rate Throughput Processing Booster For DSP Slices	Pending	Lattice Semiconductor Corporation
13/466,463		United States	Early Match FIFO	Pending	Lattice Semiconductor Corporation
13/681,782		United States	Multi-channel transmitter synchronization circuitry	Pending	Lattice Semiconductor Corporation
13/777,243		United States	RAM Data Path Sense Leakage Abatement Circuit	Pending	Lattice Semiconductor Corporation
13/858,422		United States	Method To Enable And Disable Scan Test Mode Reliably Through JTAG Port With Maximum Scan Coverage	Pending	Lattice Semiconductor Corporation
13/868,738		United States	Loss of signal detection in high-speed serial link	Pending	Lattice Semiconductor Corporation
13/901,853		United States	Dual-Port SRAM With Bit Line Clamping	Pending	Lattice Semiconductor Corporation
13/904,861		United States	Bring up sequence for configurable PCIe IP in an	Pending	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 465/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			FPGA		Corporation
13/947,553		United States	Method For Hot Swapping Or Hot Plugging With Stable Supply-Side Reference Over Wide Voltage Range	Pending	Lattice Semiconductor Corporation
14/021,513		United States	Phase Locked Loop Circuit With Selectable Feedback Paths	Pending	Lattice Semiconductor Corporation
14/043,920		United States	Robust Serialized State-machine Interface Architecture Optimized for Implementation in Programmable Devices	Pending	Lattice Semiconductor Corporation
14/053,026		United States	ASB SW modeling methodology	Pending	Lattice Semiconductor Corporation
14/070,975		United States	Method to enable system board pin escape for tight ball pitch packages	Pending	Lattice Semiconductor Corporation
14/095,310		United States	A Novel ESD Implementation for 40nm FPGA	Pending	Lattice Semiconductor Corporation
14/136,482		United States	Automatic Quadrant Clock Assignment For Programmable Logic Devices	Pending	Lattice Semiconductor Corporation
14/137,443		United States	Using Critical Groups in FPGA Routing	Pending	Lattice Semiconductor Corporation
14/147,796		United States	A Hot Socket Implementation for General Purpose IO for 40nm FPGA	Pending	Lattice Semiconductor Corporation
14/172,678		United States	All Mosfet Circuit for Generating Accurate Collector Currents	Pending	Lattice Semiconductor Corporation
14/179,651		United States	LOW-VOLTAGE CURRENT SENSE AMPLIFIER	Pending	Lattice Semiconductor Corporation
14/194,484		United States	Logic Element Placement with Repacking Optimization	Pending	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 466/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/220,377		United States	DPHY using FPGA differential & single ended I/Os	Pending	Lattice Semiconductor Corporation
14/223,096		United States	DPHY using FPGA differential & single ended I/Os	Pending	Lattice Semiconductor Corporation
14/245,920		United States	Deterministic Dynamic Element Matching for Generating Precise Current Ratios	Pending	Lattice Semiconductor Corporation
14/271,331		United States	Inline Defect To Sort Test Correlation In Semiconductor Manufacturing	Pending	Lattice Semiconductor Corporation
14/271,955		United States	Performance-focused Adaptive Automatic Incremental Flow	Pending	Lattice Semiconductor Corporation
14/283,329		United States	Configuration logic controlled memory BIST (built-in self-test) for back-to-back initialization and readback of embedded block RAMs in FPGAs	Pending	Lattice Semiconductor Corporation
14/308,747		United States	A novel Output Driver drive strength and termination resistor continuously calibrating PVT compensation scheme	Pending	Lattice Semiconductor Corporation
14/313,443		United States	FPGA Hardware debug during post-config power-up and before logic analyzer connect	Pending	Lattice Semiconductor Corporation
14/313,778		United States	IOLOGIC Delay Cell Stealing for Holdtime Correction	Pending	Lattice Semiconductor Corporation
14/316,049		United States	Mapping Constant Multipliers To ICE Devices	Pending	Lattice Semiconductor Corporation
14/319,481		United States	Incrementer Absorption into Multiplier Logic	Pending	Lattice Semiconductor Corporation
14/320,169		United States	Method to Implement Mixed-	Pending	Lattice

LENOVO EXHIBIT 1002 - 467/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Width Mode Memory in Fixed-Mode Memory Architecture with Masking		Semiconductor Corporation
14/320,074		United States	Two Level Voltage Regulator scheme for SRAM Operation	Pending	Lattice Semiconductor Corporation
14/327,811		United States	Implementing Dual Boot For XO2 and Multiple ASCs	Pending	Lattice Semiconductor Corporation
14/339,164		United States	A unique method to optimize clock to out path	Pending	Lattice Semiconductor Corporation
14/339,229		United States	New method on bus-based clock_to_out timing optimization	Pending	Lattice Semiconductor Corporation
14/482,001		United States	Physically-aware Programmable Multiport Memory BIST with on-the-fly ATE-configurable memory tests	Pending	Lattice Semiconductor Corporation
14/509,564		United States	Dont-care based mux absorption into ice40 carry chain	Pending	Lattice Semiconductor Corporation
14/525,240		United States	Level shifter that eliminates static power dissipation	Pending	Lattice Semiconductor Corporation
14/535,454		United States	Low power and high performance class AB amplifier control common mode in SerDes Transmitter	Pending	Lattice Semiconductor Corporation
14/535,351		United States	ICO metastability prevention during start-up	Pending	Lattice Semiconductor Corporation
14/558,851		United States	Low Power and Flexible TX FFE With Programmable Tap Positions And Coefficients Driver Architecture	Pending	Lattice Semiconductor Corporation
14/576,348		United States	Reconfigurable and Scalable Hardware Management Architecture	Pending	Lattice Semiconductor Corporation

LENOVO EXHIBIT 1002 - 468/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/576,245		United States	Methodology that allows multiple hardware or hardware-software controllers with different bus interfaces to share a common resource	Pending	Lattice Semiconductor Corporation
14/604,515		United States	Enhancement of FPGA hardware debugger to be used as a design controller/exerciser with user registers	Pending	Lattice Semiconductor Corporation
14/609,181		United States	Algorithm to Optimize Hot Swapping	Pending	Lattice Semiconductor Corporation
14/610,074		United States	Ripple Mode using 3-LUT for Generate	Pending	Lattice Semiconductor Corporation
14/610,127		United States	Combine OFX with LUT output and SUM into a single output to reduce number of signals to routing block	Pending	Lattice Semiconductor Corporation
14/611,069		United States	High speed complementary NMOS LUT logic	Pending	Lattice Semiconductor Corporation
14/611,095		United States	Shared Logic for Multiple Registers with asynchronous initialization with preload	Pending	Lattice Semiconductor Corporation
11/949,454	7,427,874	United States	Interface block architectures	Issued	Lattice Semiconductor Corporation
11/676,196	7,327,160	United States	SERDES with programmable I/O architecture	Issued	Lattice Semiconductor Corporation
6,786,564	6,786,564	United States	Inkjet printer, drive method and drive device for same	Issued	Lattice Semiconductor Corporation
11/839,107	7,856,050	United States	Receiver and transmitter calibration to compensate for frequency dependent I/Q imbalance	Issued	Lattice Semiconductor Corporation
07/679,370	5,255,221	United States	Fully configurable versatile field programmable function	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 469/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			element		Corporation
06/551,735	4,642,797	United States	High speed first-in-first-out memory	Issued	Lattice Semiconductor Corporation
08/042,533	5,394,037	United States	Sense amplifiers and sensing methods	Issued	Lattice Semiconductor Corporation
08/115,533	5,404,055	United States	Input routing pool	Issued	Lattice Semiconductor Corporation
08/115,723	5,394,033	United States	Structure and method for implementing hierarchical routing pools in a programmable logic circuit	Issued	Lattice Semiconductor Corporation
08/342,675	5,506,517	United States	Output enable structure and method for a programmable logic device	Issued	Lattice Semiconductor Corporation
07/911,841	5,357,156	United States	Active clamp circuit scheme for CMOS devices	Issued	Lattice Semiconductor Corporation
08/179,887	5,886,378	United States	Single polysilicon layer flash E.sup.2 PROM cell	Issued	Lattice Semiconductor Corporation
07/853,453	5,231,316	United States	Temperature compensated CMOS voltage to current converter	Issued	Lattice Semiconductor Corporation
08/108,363	5,353,246	United States	Programmable semiconductor antifuse structure and method of fabricating	Issued	Lattice Semiconductor Corporation
07/785,442	5,281,906	United States	Tunable voltage reference circuit to provide an output voltage with a predetermined temperature coefficient independent of variation in supply voltage	Issued	Lattice Semiconductor Corporation
07/696,453	5,251,169	United States	Non-volatile erasable and programmable interconnect cell	Issued	Lattice Semiconductor Corporation
07/538,211	5,255,203	United States	Interconnect structure for programmable logic device	Issued	Lattice Semiconductor

LENOVO EXHIBIT 1002 - 470/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
08/106,263	5,412,260	United States	Multiplexed control pins for in-system programming and boundary scan state machines in a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/033,934	5,418,390	United States	Single polysilicon layer E.sup.2 PROM cell	Issued	Lattice Semiconductor Corporation
07/993,711	5,452,229	United States	Programmable integrated-circuit switch	Issued	Lattice Semiconductor Corporation
07/957,311	5,329,179	United States	Arrangement for parallel programming of in-system programmable IC logical devices	Issued	Lattice Semiconductor Corporation
07/288,945	4,896,296	United States	Programmable logic device configurable input/output cell	Issued	Lattice Semiconductor Corporation
06/882,602	4,887,239	United States	One-time programmable data security system for programmable logic device	Issued	Lattice Semiconductor Corporation
06/871,063	4,766,569	United States	Programmable logic array	Issued	Lattice Semiconductor Corporation
06/862,815	4,879,688	United States	In-system programmable logic device	Issued	Lattice Semiconductor Corporation
06/707,670	4,833,646	United States	Programmable logic device with limited sense currents and noise reduction	Issued	Lattice Semiconductor Corporation
07/236,348	4,852,044	United States	Programmable data security circuit for programmable logic device	Issued	Lattice Semiconductor Corporation
11/400,924	7411424	United States	Programmable logic function generator using non-volatile programmable memory switches	Issued	Lattice Semiconductor Corporation
13/403,146		United States	Surface Mountable Integrated Circuit Packaging Scheme	Pending	SiBEAM, Inc.

LENOVO EXHIBIT 1002 - 471/502

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/242,665		United States	High Speed Integrated Circuit Interface	Pending	SiBEAM, Inc.
14/196,978		United States	Calibration of Single-Ended High-Speed Interfaces	Pending	Silicon Image, Inc.
14/474,005		United States	Inter-Device Conflict Resolution on a Multimedia Link	Pending	Silicon Image, Inc.
61/989,417		United States	Control Target Selection	Pending	Silicon Image, Inc.
61/988,812		United States	Lip Sync Delay Compensation	Pending	Silicon Image, Inc.
61/989,415		United States	Streaming Data and Metadata Synchronization	Pending	Silicon Image, Inc.
61/991,126		United States	Stream Creation with Limited Topology Information	Pending	Silicon Image, Inc.
61/989,411		United States	Topology Discovery	Pending	Silicon Image, Inc.
14/463,146		United States	Radio Frequency Interference Reduction In Multimedia Interfaces	Pending	Silicon Image, Inc.
14/578,266		United States	Control Target Selection	Pending	Silicon Image, Inc.
14/578,257		United States	System for Dynamic Audio Visual Capabilities Exchange	Pending	Silicon Image, Inc.
62/089,767		United States	High-Bandwidth Digital Content Protection over Audio Return Channel	Pending	Silicon Image, Inc.
12/573,492	8482462	United States	MULTI-ANTENNA BEAM-FORMING SYSTEM FOR TRANSMITTING CONSTANT ENVELOPE SIGNALS DECOMPOSED FROM A VARIABLE ENVELOPE SIGNAL	Issued	Silicon Image, Inc.
12/678,463	8207892	United States	TECHNIQUE FOR DETERMINING AN ANGLE OF ARRIVAL IN A COMMUNICATION SYSTEM	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/675,269	8374558	United States	ANTENNA ARRAY WITH FLEXIBLE INTERCONNECT FOR A MOBILE WIRELESS DEVICE	Issued	Silicon Image, Inc.
12/333,134	8213872	United States	TECHNIQUE FOR LOW-POWER OPERATION OF A WIRELESS DEVICE	Issued	Silicon Image, Inc.
12/933,876	8256123	United States	DISPLACEMENT SENSING USING A FLEXIBLE SUBSTRATE	Issued	Silicon Image, Inc.
14/196,993		United States	Calibration of Single-Ended High-Speed Interfaces	Pending	Silicon Image, Inc.
13/988,047		United States	INTEGRATED PHASE-SHIFTING-AND-COMBINING CIRCUITRY TO SUPPORT MULTIPLE ANTENNAS	Pending	Silicon Image, Inc.
14/002,353		United States	TRACKING SYSTEM WITH ORTHOGONAL POLARIZATIONS AND A RETRO-DIRECTIVE ARRAY	Pending	Silicon Image, Inc.
13/726,822		United States	HIGH-ACCURACY DETECTION IN COLLABORATIVE TRACKING SYSTEMS	Pending	Silicon Image, Inc.
13/859,764		United States	ANTENNA SELECTION AND PILOT COMPRESSION IN MIMO SYSTEMS	Pending	Silicon Image, Inc.
62/100,841		United States	I/Q Imbalance Correction for the Combination of Multiple Radio Frequency Frontends	Pending	Silicon Image, Inc.
12/532,107	8571126	United States	MULTI-ANTENNA TRANSMITTER FOR MULTI-TONE SIGNALING	Issued	Silicon Image, Inc.
14/065,420		United States	MULTI-ANTENNA TRANSMITTER FOR MULTI-TONE SIGNALING	Pending	Silicon Image, Inc.
12/679,764	8605823	United States	COMMUNICATION USING	Issued	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			CONTINUOUS-PHASE MODULATED SIGNALS		Inc.
14/101,274		United States	COMMUNICATION USING CONTINUOUS-PHASE MODULATED SIGNALS	Pending	Silicon Image, Inc.
12/746,526	8484277	United States	TRANSFORMING SIGNALS USING PASSIVE CIRCUITS	Issued	Silicon Image, Inc.
13/498,884	8610474	United States	SIGNAL DISTRIBUTION NETWORKS AND RELATED MET	Issued	Silicon Image, Inc.
14/089,094		United States	SIGNAL DISTRIBUTION NETWORKS AND RELATED METHODS	Pending	Silicon Image, Inc.
13/519,302		United States	Phase Detection Circuits and Methods	Pending	Silicon Image, Inc.
13/574,586	8795082	United States	DIRECTIONAL BEAM STEERING SYSTEM AND METHOD TO DETECT LOCATION AND MOTION	Issued	Silicon Image, Inc.
14/331,144		United States	DIRECTIONAL BEAM STEERING SYSTEM AND METHOD TO DETECT LOCATION AND MOTION	Pending	Silicon Image, Inc.
13/704,564		United States	Methods and Systems for Near-Field MIMO Communications	Pending	Silicon Image, Inc.
14/235,783		United States	HIGH-ACCURACY AND LOW-POWER TRACKING SYSTEM FOR MOBILE DEVICES	Pending	Silicon Image, Inc.
14/234,623		United States	LOW-COST TRACKING SYSTEM	Pending	Silicon Image, Inc.
14/240,405		United States	CALIBRATING A RETRO-DIRECTIVE ARRAY FOR AN ASYMMETRIC WIRELESS LINK	Pending	Silicon Image, Inc.
14/364,002		United States	COLLABORATIVE CHANNEL SOUNDING IN MULTI-ANTENNA	Pending	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			SYSTEMS		
08/815,486	6,157,360	United States	System And Method For Driving Columns Of An Active Matrix Display	Issued	Silicon Image, Inc.
08/920,336	5,955,929	United States	Voltage-Controlled Oscillator Resistant To Supply Voltage Noise	Issued	Silicon Image, Inc.
09/007,707	5,969,552	United States	Dual Loop Delay-Locked Loop	Issued	Silicon Image, Inc.
09/298,647	6,259,427	United States	Scaling Multi-Dimensional Signals Using Variable Weighting Factors	Issued	Silicon Image, Inc.
09/298,369	6,374,361	United States	Skew-Insensitive Low Voltage Differential Receiver	Issued	Silicon Image, Inc.
09/393,849	6,738,417	United States	Method And Apparatus For Bidirectional Data Transfer Between A Digital Display And A Computer	Issued	Silicon Image, Inc.
09/326,503	6,940,496	United States	Display Module Driving System And Digital To Analog Converter For Driving Display	Issued	Silicon Image, Inc.
09/392,229	6,564,269	United States	Bi-Directional Data Transfer Using The Video Blanking Period In A Digital Data Stream	Issued	Silicon Image, Inc.
09/393,234	6,307,543	United States	Bi-Directional Data Transfer Using Two Pair Of Differential Lines As A Single Additional Differential Pair	Issued	Silicon Image, Inc.
09/947,008	6,492,984	United States	Bi-Directional Data Transfer Using Two Pair Of Differential Lines As A Single Additional Differential Pair	Issued	Silicon Image, Inc.
09/759,624	6,891,910	United States	Baud-Rate Timing Recovery	Issued	Silicon Image, Inc.
09/574,571	6,326,826	United States	Wide Frequency-Range Delay- Locked Loop Circuit	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/881,271	6,954,491	United States	Methods And Systems For Sending Side-Channel Data During Data Inactive Period	Issued	Silicon Image, Inc.
09/922,990	6,961,095	United States	Digital Display Jitter Correction Apparatus And Method	Issued	Silicon Image, Inc.
11/219,323	7,557,863	United States	Digital Display Jitter Correction Apparatus And Method	Issued	Silicon Image, Inc.
09/989,587	6,717,478	United States	Multi-Phase Voltage Controlled Oscillator (VCO) With Common Mode Control	Issued	Silicon Image, Inc.
10/371,220	7,231,009	United States	Data Synchronization Across An Asynchronous Boundary Using, For Example, Multi-Phase Clocks	Issued	Silicon Image, Inc.
09/989,580	7,103,013	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
11/441,669	7,599,316	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
12/573,847	8,116,240	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
10/045,297	7,257,129	United States	Memory Architecture With Multiple Serial Communications Ports	Issued	Silicon Image, Inc.
11/828,286	7,903,684	United States	Communications Architecture For Transmission Of Data Between Memory Bank Caches And Ports	Issued	Silicon Image, Inc.
09/167,527	6,380,978	United States	Digital Video System And Methods For Providing Same	Issued	DVDO, INC. and Silicon Image, Inc.
10/032,136	7,215,376	United States	Digital Video System And Methods For Providing Same	Issued	DVDO, INC. and Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/942,740	7,359,624	United States	Portable DVD Player	Issued	Silicon Image, Inc.
09/372,713	6,489,998	United States	Method And Apparatus For Deinterlacing Digital Video	Issued	Silicon Image, Inc.
09/941,949	6,909,469	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
10/251,642	7,027,099	United States	Method And Apparatus For Deinterlacing Digital Video Images	Issued	Silicon Image, Inc.
11/054,748	7,391,481	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
11/357,364	7,499,103	United States	Method And Apparatus For Detecting Frequency In Digital Video Images	Issued	Silicon Image, Inc.
11/932,808	7,633,559	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
09/410,543	6,700,622	United States	Method And Apparatus For Detecting The Source Format Of Video Images	Issued	Silicon Image, Inc.
09/396,993	6,515,706	United States	Method And Apparatus For Detecting And Smoothing Diagonal Features In Video Images	Issued	Silicon Image, Inc.
10/191,764	6,829,013	United States	Method And Apparatus For Detecting And Smoothing Diagonal Features In Video Images	Issued	Silicon Image, Inc.
09/363,312	6,681,059	United States	Method And Apparatus For Efficient Video Scaling	Issued	Silicon Image, Inc.
09/359,530	6,587,158	United States	Method And Apparatus For Reducing On-Chip Memory In Vertical Video Processing	Issued	Silicon Image, Inc.
09/226,776	6,219,747	United States	Methods And Apparatus For Variable Length SDRAM	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Transfers		
09/805,588	6,385,692	United States	Methods and Apparatus for Variable Length SDRAM Transfers	Issued	Silicon Image, Inc.
09/227,502	6,393,505	United States	Methods And Apparatus For Data Bus Arbitration	Issued	Silicon Image, Inc.
09/226,381	6,473,476	United States	Method And Apparatus For Providing Deterministic Resets For Clock Divider Systems	Issued	Silicon Image, Inc.
09/837,894	6,867,814	United States	Method, System And Article Of Manufacture For Identifying The Source Type And Quality Level Of A Video Sequence	Issued	Silicon Image, Inc.
09/478,122	7,203,557	United States	Audio Signal Delay Apparatus And Method	Issued	Silicon Image, Inc.
10/663,413	7,408,992	United States	Detection And Repair Of MPEG-2 Chroma Upconversion Artifacts	Issued	Silicon Image, Inc.
09/905,318	7,123,307	United States	Clock Jitter Limiting Scheme In Video Transmission Through Multiple Stages	Issued	Silicon Image, Inc.
09/905,615	6,944,804	United States	System And Method For Measuring Pseudo Pixel Error Rate	Issued	Silicon Image, Inc.
09/904,783	6,625,560	United States	Method Of Testing Serial Interface	Issued	Silicon Image, Inc.
09/989,590	6,845,461	United States	High-Speed Bus With Embedded Clock Signals	Issued	Silicon Image, Inc.
09/989,645	6,809,567	United States	System And Method For Multiple-Phase Clock Generation	Issued	Silicon Image, Inc.
09/905,511	7,062,004	United States	Method And Apparatus For Adaptive Control Of PLL Loop Bandwidth	Issued	Silicon Image, Inc.
10/057,823	7,023,487	United States	Deinterlacing Of Video Sources Via Image Feature Edge Detection	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/954,663	7,558,326	United States	Method And Apparatus For Sending Auxiliary Data On A TMDS-Like Link	Issued	Silicon Image, Inc.
10/036,234	7,359,437	United States	Encoding Method And System For Reducing Inter-Symbol Interference Effects In Transmission Over A Serial Link	Issued	Silicon Image, Inc.
10/095,422	7,257,163	United States	Method And System For Reducing Inter-Symbol Interference Effects In Transmission Over A Serial Link With Mapping Of Each Word In A Cluster Of Received Words To A Single Transmitted Word	Issued	Silicon Image, Inc.
10/171,860	7,088,398	United States	Method And Apparatus For Regenerating A Clock For Auxiliary Data Transmitted Over A Serial Link With Video Data	Issued	Silicon Image, Inc.
10/192,296	6,914,637	United States	Method And System For Video And Auxiliary Data Transmission Over A Serial Link	Issued	Silicon Image, Inc.
10/357,750	7,283,566	United States	Method And Circuit For Generating Time Stamp Data From An Embedded-Clock Audio Data Stream And A Video Clock	Issued	Silicon Image, Inc.
10/016,247	6,714,206	United States	Method And System For Spatial-Temporal Dithering For Displays With Overlapping Pixels	Issued	Silicon Image, Inc.
10/133,813	7,136,484	United States	Cryptosystems Using Commuting Pairs In A Monoid	Issued	Silicon Image, Inc.
10/047,772	7,109,958	United States	Supporting Circuitry And Method For Controlling Pixels	Issued	Silicon Image, Inc.
10/045,393	7,039,121	United States	Method And System For Transition-Controlled Selective Block Inversion	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Communications		
08/656,032	6,018,456	United States	Enclosure For Removable Computer Peripheral Equipment	Issued	CMD Technology Inc. and Silicon Image, Inc.
08/906,775	5,991,546	United States	System And Method For Interfacing Manually Controllable Input Devices To A Universal Computer Bus System	Issued	CMD Technology Inc. and Silicon Image, Inc.
10/171,820	7,225,282	United States	Method And Apparatus For A Two-Wire Serial Command Bus Interface	Issued	Silicon Image, Inc.
11/713,241	7,441,065	United States	Adaptive Beam-Steering Methods To Maximize Wireless Link Budget And Reduce Delay-Spread Using Multiple Transmit And Receive Antennas	Issued	Silicon Image, Inc.
10/210,839	7,171,525	United States	Method And System For Arbitrating Priority Bids Sent Over Serial Links To A Multi-Port Storage Device	Issued	Silicon Image, Inc.
09/688,536	6,380,783	United States	Cyclic Phase Signal Generation From A Single Clock Source Using Current Phase Interpolation	Issued	Silicon Image, Inc.
09/847,837	6,535,029	United States	Fully Differential Continuous-Time Current-Mode High Speed CMOS Comparator	Issued	Silicon Image, Inc.
10/270,882	7,009,827	United States	Voltage Swing Detection Circuit For Hot Plug Event Or Device Detection Via A Differential Link	Issued	Silicon Image, Inc.
10/162,046	6,843,674	United States	Method And Apparatus For Connecting Serial ATA Storage Components	Issued	Silicon Image, Inc.
09/945,278	7,131,004	United States	Method And Apparatus For Encrypting Data Transmitted Over A Serial Link	Issued	Silicon Image, Inc.
11/499,124	7,900,047	United States	Method And Apparatus For Encrypting Data Transmitted	Issued	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Over A Serial Link		Inc.
11/543,501	7,757,085	United States	Method And Apparatus For Encrypting Data Transmitted Over A Serial Link	Issued	Silicon Image, Inc.
10/224,995	7,218,737	United States	System And Method For An Adaptive State Machine To Control Signal Filtering In A Serial Link	Issued	Silicon Image, Inc.
09/991,057	7,242,766	United States	Method And System For Encrypting And Decrypting Data Using An External Agent	Issued	Silicon Image, Inc.
10/085,177	7,035,290	United States	Method And System For Temporary Interruption Of Video Data Transmission	Issued	Silicon Image, Inc.
10/036,794	6,976,201	United States	Method And System For Host Handling Of Communications Errors	Issued	Silicon Image, Inc.
10/053,461	7,113,507	United States	Method And System For Communicating Control Information Via Out-Of-Band Symbols	Issued	Silicon Image, Inc.
10/045,625	7,746,798	United States	Method And System For Integrating Packet Type Information With Synchronization Symbols	Issued	Silicon Image, Inc.
10/035,911	7,154,905	United States	Method And System For Nesting Of Communications Packets	Issued	Silicon Image, Inc.
10/045,600	6,771,192	United States	Method And System For DC-Balancing At The Physical Layer	Issued	Silicon Image, Inc.
10/045,601	7,340,558	United States	Multisection Memory Bank System	Issued	Silicon Image, Inc.
09/989,647	7,058,121	United States	Logic Gates Including Diode-Connected Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) To Control Input Threshold Voltage Levels And Switching Transients Of	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Output Logic Signals		
09/989,487	6,985,005	United States	Differential Amplifiers Using Asymmetric Transfer Characteristics To Suppress Input Noise In Output Logic Signals	Issued	Silicon Image, Inc.
11/330,047	7,456,648	United States	Differential Amplifiers Using Asymmetric Transfer Characteristics To Suppress Input Noise In Output Logic Signals	Issued	Silicon Image, Inc.
12/275,686	7,847,583	United States	Transmitter And Receiver Using Asymmetric Transfer Characteristics In Differential Amplifiers To Suppress Noise	Issued	Silicon Image, Inc.
10/403,477	6,819,166	United States	Continuous-Time, Low-Frequency-Gain/High-Frequency-Boosting	Issued	Silicon Image, Inc.
10/417,712	7,348,991	United States	Video Graphics Text Mode Enhancement Method For Digitally Processed Data	Issued	Silicon Image, Inc.
10/287,976	6,873,341	United States	Detection Of Video Windows And Graphics Windows	Issued	Silicon Image, Inc.
10/298,722	7,539,304	United States	Integrated Circuit Having Self Test Capability Using Message Digest And Method For Testing Integrated Circuit Having Message Digest Generation Circuitry	Issued	Silicon Image, Inc.
10/215,936	6,717,468	United States	Dynamically Biased Full-Swing Operation Amplifier For An Active Matrix Liquid Crystal Display Driver	Issued	Silicon Image, Inc.
10/268,832	7,412,053	United States	Cryptographic Device With Stored Key Data And Method For Using Stored Key Data To Perform An Authentication Exchange Of Self Test	Issued	Silicon Image, Inc.
11/950,088	7,797,536	United States	Cryptographic Device With Stored Key Data And Method	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			For Using Stored Key Data To Perform An Authentication Exchange Of Self Test		
10/244,152	6,814,583	United States	Through-Broad PCB Edge Connector, System And Method	Issued	Silicon Image, Inc.
10/247,675	8,064,508	United States	Equalizer With Controllably Weighted Parallel High Pass And Low Pass Filters And Receiver Including Such An Equalizer	Issued	Silicon Image, Inc.
11/796,175	8,275,026	United States	Equalizer With Controllably Weighted Parallel High Pass And Low Pass Filters And Receiver Including Such An Equalizer	Issued	Silicon Image, Inc.
10/651,500	7,551,909	United States	CMOS Transceiver With Dual Current Path VCO	Issued	Silicon Image, Inc.
10/099,533	7,158,593	United States	Combining A Clock Signal And A Data Signal	Issued	Silicon Image, Inc.
10/642,259	7,409,031	United States	Data Sampling Method And Apparatus With Alternating Edge Sampling Phase Detection For Loop Characteristic Stabilization	Issued	Silicon Image, Inc.
10/459,989	7,187,307	United States	Method And System For Encapsulation Of Multiple Levels Of Communication Protocol Functionality Within Line Codes	Issued	Silicon Image, Inc.
10/794,015	7,502,411	United States	Method And Circuit For Adaptive Equalization Of Multiple Signals In Response To A Control Signal Generated From One Of The Equalized Signals	Issued	Silicon Image, Inc.
10/459,992	6,747,580	United States	Method And Apparatus For Encoding Or Decoding Data In Accordance With An Nb/(N+1)B Block Code, And Method For Determining Such A Block Code	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/781,405	7,269,673	United States	Cable With Circuitry For Asserting Stored Cable Data Or Other Information To An External Device Or User	Issued	Silicon Image, Inc.
11/848,758	7,500,032	United States	Cable With Circuitry For Asserting Stored Cable Data Or Other Information To An External Device Or User	Issued	Silicon Image, Inc.
11/123,353	7,375,960	United States	Apparatus For Removably Securing Storage Components In An Enclosure	Issued	Silicon Image, Inc.
10/763,905	7,236,553	United States	Reduced Dead-Cycle, Adaptive Phase Tracking Method And Apparatus	Issued	Silicon Image, Inc.
10/835,301	6,897,793	United States	Method And Apparatus For Run Length Limited TMDS-Like Encoding Of Data	Issued	Silicon Image, Inc.
10/842,231	7,991,096	United States	Data Sampling Method And Apparatus Using Through-Transition Counts To Reject Worst Sampling Position	Issued	Silicon Image, Inc.
10/439,446	7,031,858	United States	Method And Circuit For DC Measurement Of Phase Uniformity Of Multi-Phase Clocks	Issued	Silicon Image, Inc.
10/302,436	7,274,690	United States	An Age Selection Switching Scheme For Data Traffic In A Crossbar Switch	Issued	Silicon Image, Inc.
10/645,786	7,505,422	United States	Preference Programmable First-One Detector And Quadrature Based Random Grant Generator	Issued	Silicon Image, Inc.
10/645,787	7,461,167	United States	A Method For Multicast Service In A Crossbar Switch	Issued	Silicon Image, Inc.
10/762,950	7,352,764	United States	Content Addressable Merged Queue Architecture For Switching Data	Issued	Silicon Image, Inc.
10/434,785	7,519,066	United States	A Method For Switching Data In A Crossbar Switch	Issued	Silicon Image, Inc.
11/372,866	7,694,204	United States	Error Detection In Physical	Issued	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Interfaces For Point-To-Point Communications Between Integrated Circuits		Inc.
12/712,124	7,937,644	United States	Error Detection In Physical Interfaces For Point-To-Point Communications Between Integrated Circuits	Issued	Silicon Image, Inc.
13/099,254	8,099,648	United States	Error Detection In Physical Interfaces For Point-To-Point Communications Between Integrated Circuits	Issued	Silicon Image, Inc.
11/669,416	7,844,762	United States	Parallel Interface Bus To Communicate Video Data Encoded For Serial Data Links	Issued	Silicon Image, Inc.
11/056,995	7,102,446	United States	Phase Lock Loop With Coarse Control Loop Having Frequency Lock Detector And Device Including Same	Issued	Silicon Image, Inc.
11/643,388	7,589,559	United States	Current Mode Circuitry To Modulate A Common Mode Voltage	Issued	Silicon Image, Inc.
12/555,300	7,872,498	United States	Current Mode Circuitry to Modulate a Common Mode Voltage	Issued	Silicon Image, Inc.
11/477,049	7,793,179	United States	Test Clock Control Structures To Generate Configurable Test Clocks For Scan-Based Testing Of Electronic Circuits Using Programmable Test Clock Controllers	Issued	Silicon Image, Inc.
11/856,640	7,782,934	United States	Parameter Scanning For Signal Over-Sampling	Issued	Silicon Image, Inc.
11/592,792	7,450,038	United States	Determining Oversampled Data To Be Included In Unit Intervals	Issued	Silicon Image, Inc.
11/510,254	8,595,434	United States	Smart Scalable Storage Switch Architecture	Issued	Silicon Image, Inc.
14/067,363		United States	Smart Scalable Storage Switch Architecture	Pending	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/314,162	7,571,269	United States	A Covert Channel For Conveying Supplemental Messages In A Protocol-Defined Link For A System Of Storage Devices	Issued	Silicon Image, Inc.
11/637,254	7,602,253	United States	Adaptive Bandwidth Phase Locked Loop With Feedforward Divider	Issued	Silicon Image, Inc.
11/656,331	7,984,369	United States	Concurrent Code Checker And Hardware Efficient High-Speed I/O Having Built-In Self-Test And Debug Features	Issued	Silicon Image, Inc.
11/694,819	7,949,863	United States	Multi-Port Memory Device Having Variable Port Speeds	Issued	Silicon Image, Inc.
11/694,813	7,639,561	United States	Power-Saving Clocking Technique	Issued	Silicon Image, Inc.
11/690,629	7,831,778	United States	Mechanism For Streaming Media Data Over Wideband Wireless Networks	Issued	Silicon Image, Inc.
11/476,457	7,840,861	United States	Scan-Based Testing Of Devices Implementing A Test Clock Control Structure (â€œTCCSâ€)	Issued	Silicon Image, Inc.
11/861,175	8,160,192	United States	Signal Interleaving for Serial Clock and Data Recovery	Issued	Silicon Image, Inc.
11/690,642	7,908,501	United States	Shared Nonvolatile Memory Architecture	Issued	Silicon Image, Inc.
11/742,358	7,698,088	United States	Interface Test Circuitry And Methods	Issued	Silicon Image, Inc.
11/848,641	8,233,432	United States	Ensuring Physical Locality Of Entities Sharing Data	Issued	Silicon Image, Inc.
11/683,608	7,831,877	United States	Method And Apparatus For A Two-Wire Serial Command Bus Interface	Issued	Silicon Image, Inc.
11/690,659	7,849,339	United States	Progressive Power Control Of A Multi-Port Memory Device	Issued	Silicon Image, Inc.
11/567,514	7,365,659	United States	Method Of Context Adaptive Binary Arithmetic Coding	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			And Coding Apparatus Using The Same		
12/778,882		United States	Multi-Level Port Expansion For Port Multipliers	Pending	Silicon Image, Inc.
12/147,248	7,836,223	United States	Operation Of Media Interface To Provide Bidirectional Communications	Issued	Silicon Image, Inc.
11/849,163	8,695,034	United States	Delivering On Screen Display Data To Existing Display Devices	Issued	Silicon Image, Inc.
11/828,219	8,599,315	United States	On Screen Displays Associated With Remote Video Source Devices	Issued	Silicon Image, Inc.
14/070,373		United States	On Screen Displays Associated With Remote Video Source Devices	Pending	Silicon Image, Inc.
11/829,800	7,903,550	United States	Bandwidth Reservation For Data Flows In Interconnection Networks	Issued	Silicon Image, Inc.
11/828,223	8,149,711	United States	Data Stream Control For Network Devices	Issued	Silicon Image, Inc.
13/541,390	8,924,509	United States	Automated Service Discovery And Dynamic Connection Management	Issued	Silicon Image, Inc.
11/836,082	8,468,212	United States	Network Repository For Metadata	Issued	Silicon Image, Inc.
13/919,773		United States	Network Repository For Metadata	Pending	Silicon Image, Inc.
11/829,790	7,911,956	United States	Packet Level Prioritization In Interconnection Networks	Issued	Silicon Image, Inc.
11/828,226		United States	Streaming Data Content In A Network	Pending	Silicon Image, Inc.
11/848,153	7,936,790	United States	Synchronizing Related Data Streams In Interconnection Networks	Issued	Silicon Image, Inc.
11/952,052	8,001,334	United States	Bank Sharing And Refresh In A Shared Multi-Port Memory Device	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/075,954	7,979,589	United States	Method, Apparatus, And System For Port Multiplier Enhancement	Issued	Silicon Image, Inc.
13/298,001		United States	Iddq Testing Of CMOS Devices	Pending	Silicon Image, Inc.
10/788,704	6,944,086	United States	Semiconductor Memory Device	Issued	Silicon Image, Inc.
10/876,231	7,016,255	United States	Multi-Port Memory Device	Issued	Silicon Image, Inc.
10/877,318	7,089,465	United States	Multi-Port Memory Device Having Serial I/O Interface	Issued	Silicon Image, Inc.
12/075,906	7,904,566	United States	Method, Apparatus, And System For Employing An Enhanced Port Multiplier	Issued	Silicon Image, Inc.
12/497,391	8,386,867	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
13/776,508	8,667,354	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
14/145,751	8,924,805	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
12/197,020	8,086,886	United States	Group Power Management Of Network Devices	Issued	Silicon Image, Inc.
12/683,365	8,543,873	United States	Multi-Site Testing Of Computer Memory Devices And Serial I/O Ports	Issued	Silicon Image, Inc.
14/035,795	8,839,058	United States	Multi-Site Testing Of Computer Memory Devices And Serial I/O Ports	Issued	Silicon Image, Inc.
11/969,847	8,090,030	United States	Method, Apparatus And System For Generating And Facilitating Mobile High-Definition Multimedia Interface	Issued	Silicon Image, Inc.
11/969,852	7,856,520	United States	Control Bus For Connection Of Electronic Devices	Issued	Silicon Image, Inc.
11/969,865	7,921,231	United States	Discovery Of Electronic Devices Utilizing A Control	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Bus		
12/172,187	8,238,653	United States	Methods And Mechanisms For Probabilistic Color Correction	Issued	Silicon Image, Inc.
12/392,000		United States	Method, Apparatus, And System For Pre-Authentication And Processing Of Data Streams	Pending	Silicon Image, Inc.
12/391,987	8,644,504	United States	Method, Apparatus, And System For Deciphering Media Content Stream	Issued	Silicon Image, Inc.
12/605,134	8,407,427	United States	Method And System For Improving Serial Port Memory Communication Latency And Reliability	Issued	Silicon Image, Inc.
13/850,147	8,892,825	United States	Method and System for Improving Serial Port Memory Communication Latency and Reliability	Issued	Silicon Image, Inc.
12/260,970	8,036,248	United States	Method, Apparatus, And System For Automatic Data Aligner For Multiple Serial Receivers	Issued	Silicon Image, Inc.
12/359,025	8,026,726	United States	Fault Testing For Interconnections	Issued	Silicon Image, Inc.
12/486,969	8,793,723	United States	Detection Of Encryption Utilizing Error Detection For Received Data	Issued	Silicon Image, Inc.
12/570,874	8,644,334	United States	Messaging To Provide Data Link Integrity	Issued	Silicon Image, Inc.
12/260,972	7,777,652	United States	Coding System For Memory Systems Employing High-Speed Serial Links	Issued	Silicon Image, Inc.
12/847,416	7,978,099	United States	17b/20b Coding System	Issued	Silicon Image, Inc.
12/351,698	8,374,346	United States	Method, Apparatus, And System For Pre-Authentication And Keep-Authentication Of Content Protected Ports	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/316,305	8,347,081	United States	Method, Apparatus And System For Employing A Content Protection System	Issued	Silicon Image, Inc.
12/577,707	8,275,914	United States	Method And System For Transmitting Or Receiving N-Bit Video Data Over A Serial Link	Issued	Silicon Image, Inc.
12/606,096	8,176,214	United States	Transmission Of Alternative Content Over Standard Device Connectors	Issued	Silicon Image, Inc.
12/351,712	8,185,739	United States	Method And System For Detecting Successful Authentication Of Multiple Ports In A Time Based Roving Architecture	Issued	Silicon Image, Inc.
12/512,877	8,458,343	United States	Signaling For Transitions Between Modes Of Data Transmission	Issued	Silicon Image, Inc.
12/983,233	8,489,784	United States	Adaptive Interconnection Scheme For Multimedia Devices	Issued	Silicon Image, Inc.
13/004,359	8,755,431	United States	Transmission And Detection Of Multi-Channel Signals In Reduced Channel Format	Issued	Silicon Image, Inc.
12/650,357		United States	Method, Apparatus, And System For Simultaneously Previewing Contents From Multiple Protected Sources	Pending	Silicon Image, Inc.
12/712,933	8,692,937	United States	Video Frame Synchronization	Issued	Silicon Image, Inc.
12/966,194		United States	Transmission And Handling Of Three-Dimensional Video Content	Pending	Silicon Image, Inc.
12/873,124	8,325,757	United States	De-Encapsulation Of Data Streams Into Multiple Links	Issued	Silicon Image, Inc.
12/704,417	8,510,487	United States	Hybrid Interface For Serial And Parallel Communication	Issued	Silicon Image, Inc.
13/934,147	8,751,709	United States	Hybrid Interface For Serial And Parallel Communication	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/842,165	8,930,692	United States	Mechanism For Internal Processing Of Content Through Partial Authentication On Secondary Channel	Issued	Silicon Image, Inc.
12/842,190		United States	Mechanism For Partial Encryption Of Data Streams	Pending	Silicon Image, Inc.
13/021,958		United States	Determination Of Physical Connectivity Status Of Devices Based On Electrical Measurement	Allowed	Silicon Image, Inc.
12/898,528	8,598,898	United States	Testing Of High-Speed Input-Output Devices	Issued	Silicon Image, Inc.
13/434,273		United States	Method, Apparatus And System For Transitioning An Audio/Video Device Between A Source Mode And A Sink Mode	Pending	Silicon Image, Inc.
12/848,037	8,624,960	United States	Multi-View Display System	Issued	Silicon Image, Inc.
14/094,668		United States	Multi-View Display System	Pending	Silicon Image, Inc.
12/816,437	8,698,958	United States	Mechanism For Memory Reduction In Picture-In-Picture Video Generation	Issued	Silicon Image, Inc.
13/753,408		United States	Communication Bridging Between Devices Via Multiple Bridge Elements	Pending	Silicon Image, Inc.
13/198,584		United States	Conversion Of Multimedia Data Streams For Use By Connected Devices	Pending	Silicon Image, Inc.
12/906,939	8,537,201	United States	Combining Video Data Streams Of Differing Dimensionality For Concurrent Display	Issued	Silicon Image, Inc.
13/172,745	8,484,387	United States	Detection Of Cable Connections For Electronic Devices	Issued	Silicon Image, Inc.
13/172,742	8,601,173	United States	Detection Of Cable Connections For Electronic	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Devices		
13/362,930		United States	Mechanism For Low Power Standby Mode Control Circuit	Allowed	Silicon Image, Inc.
13/217,138	8,379,145	United States	Conversion And Processing Of Deep Color Video In A Single Clock Domain	Issued	Silicon Image, Inc.
12/979,995	8,874,820	United States	Mechanism For Facilitating A Configurable Port-Type Peripheral Component Interconnect Express/Serial Advanced Technology Attachment Host Controller Architecture	Issued	Silicon Image, Inc.
12/950,850	8,504,672	United States	Discovery Of Electronic Devices In A Combined Network	Issued	Silicon Image, Inc.
13/959,592	8,799,443	United States	Discovery of Electronic Devices in a Combined Network	Issued	Silicon Image, Inc.
13/348,378		United States	Proxy Device Operation In Command And Control Network	Pending	Silicon Image, Inc.
12/950,867		United States	Transfer Of Control Bus Signaling On Packet-Switched Network	Pending	Silicon Image, Inc.
13/339,339		United States	Mechanism For Recovering Clock For Streaming Content Over A Packetized Network	Pending	Silicon Image, Inc.
13/302,452		United States	Multimedia I/O System Architecture for Advanced Digital Television	Pending	Silicon Image, Inc.
13/107,031		United States	Audio And Video Data Multiplexing For Multimedia Stream Switch	Pending	Silicon Image, Inc.
13/174,630		United States	Single-Ended Configurable Multi-Mode Driver	Pending	Silicon Image, Inc.
13/173,302		United States	Fine-Grained Self Refresh Control For DRAM Devices	Pending	Silicon Image, Inc.
13/174,616	8,760,188	United States	Configurable Multi-Dimensional Driver And	Issued	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Receiver		Inc.
13/083,399	8,611,486	United States	Adjustment Of Clock Signals Regenerated From A Data Stream	Issued	Silicon Image, Inc.
11/437,357	7,982,798	United States	Edge Detection	Issued	Silicon Image, Inc.
13/153,230	8,446,525	United States	Edge Detection	Issued	Silicon Image, Inc.
10/753,909	7,400,359	United States	Video Stream Routing And Format Conversion Unit With Audio Delay	Issued	Silicon Image, Inc.
10/889,855	7,710,501	United States	Time Base Correction And Frame Rate Conversion	Issued	Silicon Image, Inc.
11/487,144	8,004,606	United States	Original Scan Line Detection	Issued	Silicon Image, Inc.
11/941,050	8,086,067	United States	Noise Cancellation	Issued	Silicon Image, Inc.
11/512,754	8,120,703	United States	Source-Adaptive Video Deinterlacer	Issued	Silicon Image, Inc.
12/204,760	8,559,746	United States	System, Method And Apparatus For Smoothing Of Edges In Images To Remove Irregularities	Issued	Silicon Image, Inc.
14/054,575		United States	System, Method and Apparatus for Smoothing of Edges in Images to Remove Irregularities	Pending	Silicon Image, Inc.
12/703,623	8,452,117	United States	Block Noise Detection And Filtering	Issued	Silicon Image, Inc.
13/899,222	8,891,897	United States	Block Noise Detection And Filtering	Issued	Silicon Image, Inc.
13/335,398		United States	Ringing Suppression In Video Scalers	Pending	Silicon Image, Inc.
13/546,904		United States	Transmission Of Multiple Protocol Data Elements Via An Interface Utilizing A Data Tunnel	Pending	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/202,995	7,904,117	United States	Wireless Communication Device Using Adaptive Beamforming	Issued	SiBEAM, Inc.
11/706,711	7,710,319	United States	HD Physical Layer Of A Wireless Communication Device	Issued	SiBEAM, Inc.
12/748,276	7,982,669	United States	Adaptive Beam-Steering Methods To Maximize Wireless Link Budget And Reduce Delay-Spread Using Multiple Transmit And Receive Antennas	Issued	SiBEAM, Inc.
11/706,470	8,014,416	United States	Inter-Port Communication In A Multi-Port Memory Device	Issued	Silicon Image, Inc.
11/689,386	7,881,258	United States	Circuitry To Prevent Peak Power Problems During Scan Shift	Issued	SiBEAM, Inc.
11/726,874	8,155,712	United States	Low Power Very High-Data Rate Device	Issued	SiBEAM, Inc.
11/588,472	8,022,887	United States	Planar Antenna	Issued	SiBEAM, Inc.
11/752,073		United States	A Compact Millimeter Wave Vertical Interconnection Scheme By Combining Flip-Chip, Layer Transition	Pending	SiBEAM, Inc.
11/752,083	7,675,465	United States	Surface Mountable Integrated Circuit Packaging Scheme	Issued	SiBEAM, Inc.
12/215,959		United States	Mechanism For Communication With Multiple Wireless Video Area Networks	Pending	SiBEAM, Inc.
11/981,935		United States	Wireless HD Mac Frame Format	Pending	SiBEAM, Inc.
11/938,126	8,170,522	United States	Multi-Transformer Architecture For An RF Active Circuit	Issued	SiBEAM, Inc.
11/999,810	8,750,241	United States	Concurrent Association With Multiple WVAN Network	Issued	SiBEAM, Inc.
12/079,133	8,831,225	United States	Data Security	Issued	SiBEAM, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/011,404	7,948,961	United States	Wireless Proximity Estimation	Issued	SiBEAM, Inc.
11/982,209	8,279,784	United States	Wireless HD AV Packet Format	Issued	SiBEAM, Inc.
12/055,160	8,170,617	United States	Extensions To Adaptive BeamSteering Method	Issued	SiBEAM, Inc.
12/164,757		United States	Exchanging Information Between Components Coupled With An I2C Bus Via Separate Banks	Pending	SiBEAM, Inc.
12/167,195	8,229,352	United States	Wireless Architecture For 60 GHz	Issued	SiBEAM, Inc.
11/901,069	7,986,753	United States	Modified Branch Metric For Decoders And Equalizers	Issued	SiBEAM, Inc.
12/059,757	7,915,909	United States	RF Integrated Circuit Test Methodology And System	Issued	SiBEAM, Inc.
12/164,907		United States	Dispatch Capability Using A Single Physical Interface	Pending	SiBEAM, Inc.
12/165,468		United States	Bitmap Device Identification In A Wireless Communication System	Pending	SiBEAM, Inc.
12/165,472	8,897,719	United States	Initializing A Transceiver In A Wireless Communication System	Issued	SiBEAM, Inc.
12/164,849	8,341,271	United States	Device Discovery In A Wireless Communication System	Issued	SiBEAM, Inc.
12/164,810	8,116,333	United States	Connection Control In A Wireless Communication System	Issued	SiBEAM, Inc.
12/699,758	8,588,193	United States	Enhanced Wireless Data Rates Using Multiple Beams	Issued	SiBEAM, Inc.
12/699,781	8,457,026	United States	Enhanced Wireless Data Rates Using Multiple Beams	Issued	SiBEAM, Inc.
13/113,318		United States	Apparatus, System, And Method For A Compact Symmetrical Transition Structure For Radio	Allowed	SiBEAM, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Frequency Applications		
14/128,551		United States	Method To Drive HDMI Or MHL Or USB Data Through One Set Of Pins	Pending	Silicon Image, Inc.
13/984,018		United States	Concept And Method Of Reducing Data Dependent Jitter	Pending	Silicon Image, Inc.
13/269,450		United States	Identification And Handling Of Data Streams Using Coded Preambles	Allowed	Silicon Image, Inc.
13/611,786		United States	Combining Video And Audio Streams Utilizing Pixel Repetition Bandwidth	Pending	Silicon Image, Inc.
14/118,832		United States	Compensation Scheme For MHL Common Mode Clock Swing	Pending	Silicon Image, Inc.
13/773,534		United States	Transmitting Multiple Differential Signals Over a Reduced Number of Physical Channels	Pending	Silicon Image, Inc.
13/460,393		United States	Cost-Efficient And Low-Latency Motion Picture Encoding For Limited Channel Bandwidth	Pending	Silicon Image, Inc.
13/791,494	8,925,003	United States	Mechanism For Facilitating Syncronization Of Audio And Video Between Multiple Media Devices	Issued	Silicon Image, Inc.
13/622,286	8,885,435	United States	Interfacing Between Integrated Circuits With Asymmetric Voltage Swing	Issued	Silicon Image, Inc.
13/770,984		United States	Configurable Single Ended Driver	Pending	Silicon Image, Inc.
13/779,372	8,920,188	United States	Integrated Connector/Flex Cable	Issued	Silicon Image, Inc.
13/834,927		United States	Simultaneous Transmission Of Clock And Bidirectional Data Over A Communication Channel	Allowed	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
13/605,708	8,841,974	United States	Test Solution For Ring Oscillators	Issued	Silicon Image, Inc.
14/193,932		United States	Test Solution for a Random Number Generator	Pending	Silicon Image, Inc.
13/787,664		United States	Auxiliary Data Encoding In Video Data	Pending	Silicon Image, Inc.
13/738,768		United States	Method And Apparatus For Reducing Digital Video Image Data	Pending	Silicon Image, Inc.
13/736,765	8,832,338	United States	Mechanism For Facilitating Dynamic Timestamp-Less Clock Regeneration For Transmitting Media Streams Over Shared Channels	Issued	Silicon Image, Inc.
14/123,037		United States	Timing Controlled Cascade Feed-Through High Speed Line Driver	Pending	Silicon Image, Inc.
13/776,577		United States	Apparatus, System And Method For Providing Clock And Data Signaling	Pending	Silicon Image, Inc.
13/940,038		United States	Integrated Mobile Desktop	Pending	Silicon Image, Inc.
13/915,586		United States	Multiple Protocol Tunneling Using Time Division Operations	Pending	Silicon Image, Inc.
13/891,842	8,786,776	United States	Method, Apparatus And System For Communicating Sideband Data With Non-Compressed Video	Issued	Silicon Image, Inc.
13/671,527		United States	Methods And Apparatuses To Provide And Electro-Optical Alignment	Pending	Silicon Image, Inc.
14/371,973		United States	Charge Pump Calibration for Dual-Path Phase-Locked Loop	Pending	Silicon Image, Inc.
14/115,324		United States	Mechanism for Facilitating Dynamic Phase Detection with High Jitter Tolerance for Images of Media Streams	Allowed	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/135,470		United States	Apparatus, System and Method for Formatting Audio-Video Information	Pending	Silicon Image, Inc.
13/839,671		United States	Full Frame Buffer To Improve Video Performance In Low- Latency Video Communication Systems	Pending	Silicon Image, Inc.
12/057,051		United States	Bi-Directional Digital Interface For Video And Audio (DIVA)	Pending	Silicon Image, Inc.
11/760,164	7,940,809	United States	Digital Video Interface With Bi-Directional Half-Duplex Clock Channel Used As Auxiliary Data Channel	Issued	Silicon Image, Inc.
11/865,621	7,916,780	United States	Adaptive Equalizer For Use With Clock And Data Recovery Circuit Of Serial Communication Link	Issued	Silicon Image, Inc.
12/222,745	7,737,802	United States	Passive Equalizer With Negative Impedance To Increase A Gain	Issued	Silicon Image, Inc.
12/636,063	8,680,712	United States	Power Delivery Over Digital Interactive Interface For Video And Audio (DIIVA)	Issued	Silicon Image, Inc.
13/521,739		United States	Multi-Media USB Data Transfer Over Digital Interaction Interface for Video and Audio (DIIVA)	Pending	Silicon Image, Inc.
13/521,762		United States	Video Management And Control In Home Multimedia Network	Pending	Silicon Image, Inc.
14/381,186		United States	Linear Regulator with Improved Power Supply Ripple Rejection	Pending	Silicon Image, Inc.
13/844,152		United States	Electronic Alignment Of Optical Signals	Pending	Silicon Image, Inc.
14/391,382		United States	Frequency Response Compensation in a Digital to Analog Converter	Pending	Silicon Image, Inc.
14/165,340		United States	Apparatus, System and	Pending	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Method for Providing Switching with a T-Coil Circuit		Inc.
13/836,895	8,928,411	United States	Integration Of Signal Sampling Within Transistor Amplifier Stage	Issued	Silicon Image, Inc.
14/165,345		United States	Apparatus, Method and System for Asymmetric Full-Duplex Communication	Pending	Silicon Image, Inc.
14/209,785		United States	Method And Apparatus For Implementing Wide Data Range And Wide Common-Mode Receivers	Pending	Silicon Image, Inc.
14/296,377		United States	Transmitting Apparatus with Source Termination	Pending	Silicon Image, Inc.
14/368,781		United States	Caching of Capabilities Information of Counterpart Device for Efficient Handshaking Operation	Pending	Silicon Image, Inc.
14/163,981		United States	Mechanism for Facilitating Dynamic Counter Synchronization and Packetization in High-Definition Multimedia Interface and Mobile High-Definition Link	Pending	Silicon Image, Inc.
14/253,808		United States	Communication of Multimedia Data Streams Over Multiple Communication Lanes	Pending	Silicon Image, Inc.
14/279,316		United States	HDCP2.2 Authentication Engine and Stream Cipher Engine Sharing in Digital Content Protection Architectures	Pending	Silicon Image, Inc.
14/383,865		United States	Techniques for Fractional-N Phase Locked Loops	Pending	Silicon Image, Inc.
61/949,901		United States	Compressed Video Transfer Over HDMI and MHL	Pending	Silicon Image, Inc.
14/563,797		United States	Electrical Duplex to Optical Conversion	Pending	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/470,750		United States	Arbitration Signaling within a Multimedia High Definition Link (MHL 3) Device	Pending	Silicon Image, Inc.
14/275,692		United States	Error Detection and Mitigation in Video Channels	Pending	Silicon Image, Inc.
14/339,393		United States	Phase-Modulated On-Off Keying for Millimeter Wave Spectrum Control	Pending	Silicon Image, Inc.
14/145,715		United States	Messaging to Provide Data Link Integrity	Pending	Silicon Image, Inc.
14/145,736	8,854,548	United States	Mechanism for Memory Reduction in Picture-In-Picture Video Generation	Issued	Silicon Image, Inc.
14/470,613		United States	Compressed Video Transfer Over a Multimedia Link	Pending	Silicon Image, Inc.
14/184,647		United States	Video Frame Synchronization	Pending	Silicon Image, Inc.
14/181,446		United States	Power Delivery Over Digital Interaction Interface for Video and Audio (DiiVA)	Pending	Silicon Image, Inc.
14/470,804		United States	Phase Relationship Control for Control Channel of a Multimedia Communication Link	Pending	Silicon Image, Inc.
14/470,809		United States	Retry Disparity for Control Channel of a Multimedia Communication Link	Pending	Silicon Image, Inc.
61/943,267		United States	Pre-Processor and Post-Processor for Compression of 4:2:0 Encoded Video Streams with Video Compression Codecs Embedded within an Audio/Video Standard	Pending	Silicon Image, Inc.
14/278,255		United States	Encoding Guard Band Data for Transmission Via a Communications Interface Utilizing Transition-Minimized Differential Signaling (Tmds) Coding	Pending	Silicon Image, Inc.
14/322,753		United States	Calibration Of Single-Ended	Pending	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			High-Speed Interfaces		Inc.
61/947,704		United States	Reversible Connector	Pending	Silicon Image, Inc.
14/460,737		United States	System and Method for Transcoding Data	Pending	Silicon Image, Inc.
14/502,928		United States	Electrical Connector with Optical Channel	Pending	Silicon Image, Inc.
14/322,753		United States	Cable with Circuitry for Communicating Performance Information	Pending	Silicon Image, Inc.
61/973,837		United States	Error Correction for Transmission of Compressed Video Data Over Standards-Defined Coded Audio/Video Links	Pending	Silicon Image, Inc.
61/975,517		United States	(MHL) Connector Cable Detect, Cable Orientation Detect and/or Lane Re-Mapping	Pending	Silicon Image, Inc.
61/979,477		United States	MHL3 Router without HDCP2.2 Decryption and Encryption Operation	Pending	Silicon Image, Inc.
61/979,483		United States	TDD over 5-Pin Interface	Pending	Silicon Image, Inc.
14/470,620		United States	Compressed Blanking Period Transfer Over a Multimedia Link	Pending	Silicon Image, Inc.
14/273,400		United States	Transmission and Detection of Multi-Channel Signals in Reduced Channel Format	Pending	Silicon Image, Inc.
61/989,409		United States	System for Dynamic Capabilities, Status, and Metadata Exchange	Pending	Silicon Image, Inc.
14/300,166		United States	Configurable Multi-Dimensional Driver and Receiver	Pending	Silicon Image, Inc.
14/483,013		United States	Enhanced Communication Link Using Synchronization Signal as Link Command	Pending	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
62/043,218		United States	Run Length Programmable Unified Built-In Self-Test (BIST) Scheme for Various High-Speed Serial IO Standards	Pending	Silicon Image, Inc.
14/559,523		United States	Determination of Physical Connectivity Status of Devices Based on Electrical Measurement	Pending	Silicon Image, Inc.
14/516,136		United States	Method and System for Improving Serial Port Memory Communication Latency and Reliability	Pending	Silicon Image, Inc.
62/061,630		United States	Secure Control Communication Between an Application Processor and a Transmitter	Pending	Silicon Image, Inc.
62/075,554		United States	Metadata Transfer for HDMI/MHL	Pending	Silicon Image, Inc.
14/570,817		United States	Mechanism for Facilitating Dynamic Phase Detection with High Jitter Tolerance for Images of Media Streams	Pending	Silicon Image, Inc.
14/589,889		United States	Displaying Multiple Videos on Sink Device Using Display Information of Source Device	Pending	Silicon Image, Inc.
14/589,925		United States	Lower Power Operations in a Wireless Tunneling Transceiver	Pending	Silicon Image, Inc.
14/591,845		United States	Simultaneous Transmission of Clock and Bidirectional Data Over a Communication Channel	Pending	Silicon Image, Inc.
14/449095	20150036756	United States	Radio Frequency Interference Reduction In Multimedia Interfaces	Pending	Silicon Image, Inc.

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