UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES) INC., DELL TECHNOLOGIES, INC.,
DELL INC., and HP INC.,
Petitioners,

v.

UNIVERSAL CONNECTIVITY TECHNOLOGIES, INC.,
Patent Owner.

IPR2024-01482
U.S. Patent No. 7,856,520

DECLARATION OF JUNE ANN MUNFORD

1. My name is June Ann Munford. I am over the age of 18, have personal knowledge of the facts set forth herein, and am competent to testify to the same.

2. I earned a Master of Library and Information Science (MLIS) from the University of Wisconsin-Milwaukee in 2009. I have over ten years of experience in the library/information science field. Beginning in 2004, I have served in various positions in the public library sector including Assistant Librarian, Youth Services Librarian and Library Director. I have attached my Curriculum Vitae as Appendix CV.

3. During my career in the library profession, I have been responsible for materials acquisition for multiple libraries. In that position, I have cataloged, purchased and processed incoming library works. That includes purchasing materials directly from vendors, recording publishing data from the material in question, creating detailed material records for library catalogs and physically preparing that material for circulation. In addition to my experience in acquisitions, I was also responsible for analyzing large collections of library materials, tailoring library records for optimal catalog

LENOVO EXHIBIT 1009 - 2/45

search performance and creating lending agreements between libraries during my time as a Library Director.

4. I am fully familiar with the catalog record creation process in the library sector. In preparing a material for public availability, a library catalog record describing that material would be created. These records are typically written in Machine Readable Catalog (herein referred to as "MARC") code and contain information such as a physical description of the material, metadata from the material's publisher, and date of library acquisition. In particular, the 008 field of the MARC record is reserved for denoting the date of creation of the library record itself. As this typically occurs during the process of preparing materials for public access, it is my experience that an item's MARC record indicates the date of an item's public availability.

5. Typically, in creating a MARC record, a librarian would gather various bits of metadata such as book title, publisher and subject headings among others and assign each value to a relevant numerical field. For example, a book's physical description is tracked in field 300 while title/attribution is tracked in field 245. The 008 field of the MARC record is reserved for denoting the creation of the library record itself. As this is the only date reflecting the inclusion of said materials within the library's collection, it is my experience

that an item's 008 field accurately indicates the date of an item's public availability.

6. I have reviewed Exhibit 1007, which is the publication entitled "Design of a Multicode Bi-Phase Encode for Data Transmission" by Raida Al-Alawi, et al. as published in *Journal of Circuits, Systems, and Computers*, February 2006. I will refer to this publication as "the Al-Alawi publication."

7. Attached hereto as Appendix AL-ALAWI01 is a true and correct copy of the MARC record for *Journal of Circuits, Systems, and Computers* as held by the University of Illinois-Chicago library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix AL-ALAWI01 accurately describes the title, author, publisher, and ISSN number of *Journal of Circuits, Systems, and Computers.* The 'Location Items' field of this record visible on page 2 indicates this collection includes the February 2006 edition of *Journal of Circuits, Systems, and Computers* containing the Al-Alawi publication.

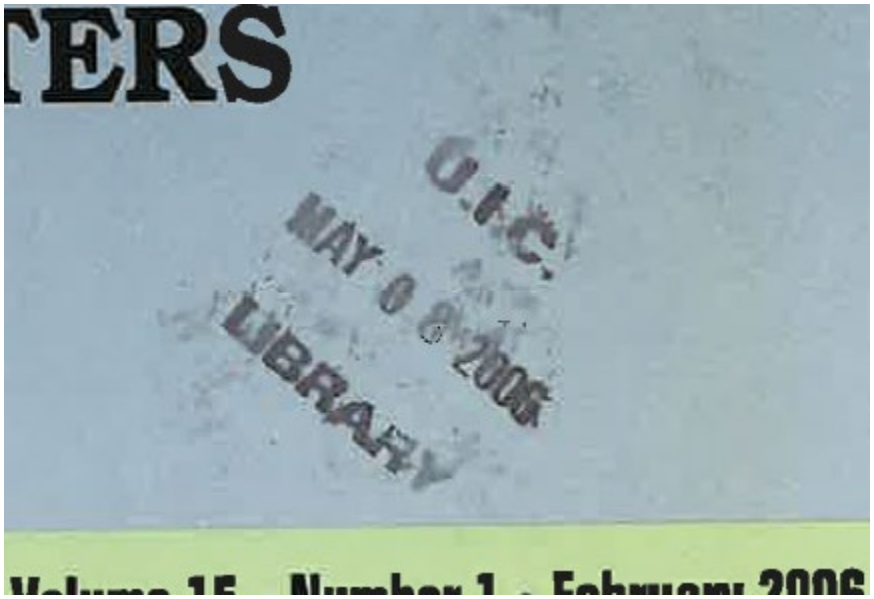
8. Attached hereto as Appendix AL-ALAWI02 is a true and correct copy of the Al-Alawi publication as published in *Journal of Circuits, Systems, and Computers* as held by the University of Illinois-Chicago library. I secured

LENOVO EXHIBIT 1009 - 4/45

these scans myself from the library's collection. In comparing Exhibit 1007 to Appendix AL-ALAWI02, it is my determination that Exhibit 1007 is a true and correct copy of the Al-Alawi publication, *i.e.*, "Design of a Multicode Bi-Phase Encode for Data Transmission" by Raida Al-Alawi, et al. as published in *Journal of Circuits, Systems, and Computers* February 2006.

9. The 008 field of the MARC record in Appendix AL-ALAWI01 indicates the date of record creation. The 008 field of Appendix AL-ALAWI01 indicates the University of Illinois-Chicago library first acquired this journal as of August 29, 1991 and held the journal in perpetuity until 2008. Considering this information, it is my determination that *Journal of Circuits, Systems, and Computers* February 2006 and therefore the Al-Alawi publication was made available to the public shortly after its initial release in February 2006.

10. In addition, I note that page 3 of the scan in Appendix AL-ALAWI02 bears a stamp of May 8, 2006 on the front cover of the February 2006 edition of *Journal of Circuits, Systems, and Computers* containing the Al-Alawi publication, as shown below:



11. This stamp colloquially known in the library science field as a "date stamp." A date stamp is applied to the work by a librarian for a handful of different reasons, with usage varying from library to library. Most commonly, date stamps are applied after the work has been cataloged but before the work is placed on the public shelves. These date stamps are sometimes marked with the word "received." Other common uses for these date stamps include noting when the work has been moved to a different location (such as an archive) or noting when the work has been bound into a larger volume. Thus, in my opinion and based on my experience, at a minimum, this date stamp indicates that the University of Illinois-Chicago library staff had this journal issue in-hand as of at least as early as May 8, 2006 and most likely

applied the stamp as part of a process to prepare the work for public availability.

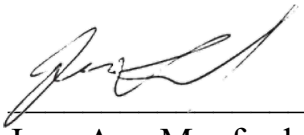
12. In my opinion and based on my experience, I estimate that the period of time between the time the library record is first received and catalogued and the time the library record being available to the public on shelves would average between 2-12 weeks. Thus, in my opinion, this May 8, 2006 date stamp indicates that the February 2006 edition of *Journal of Circuits, Systems, and Computers* containing the Al-Alawi publication was catalogued and publicly available on shelves in the library by, conservatively, no later than the end of 2006, at the absolute latest.

13. I have been retained on behalf of the Petitioner to provide assistance in the above-illustrated matter in establishing the authenticity and public availability of the documents discussed in this declaration. I am being compensated for my services in this matter at the rate of $200.00 per hour plus reasonable expenses. My statements are objective, and my compensation does not depend on the outcome of this matter.

14. I declare under penalty of perjury that the foregoing is true and correct. I hereby declare that all statements made herein of my own knowledge are

true and that all statements made on information and belief are believed to be true; and further that these statements were made the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: 9/27/2024



June Ann Munford

ATTACHMENT - CURRICULUM VITAE

June A. Munford
Curriculum Vitae

Education

University of Wisconsin-Milwaukee - MS, Library & Information Science, 2009
Milwaukee, WI

- Coursework included cataloging, metadata, data analysis, library systems, management strategies and collection development.
- Specialized in library advocacy, cataloging and public administration.

Grand Valley State University - BA, English Language & Literature, 2008
Allendale, MI

- Coursework included linguistics, documentation and literary analysis.
- Minor in political science with a focus in local-level economics and government.

Professional Experience

Researcher / Expert Witness, October 2017 – present
Freelance ● Pittsburgh, Pennsylvania & Grand Rapids, Michigan

- Material authentication and public accessibility determination. Declarations of authenticity and/or public accessibility provided upon research completion. Experienced with appeals and deposition process.

- Research provided on topics of public library operations, material publication history, digital database services and legacy web resources.

- Past clients include Alston & Bird, Arnold & Porter, Baker Botts, Fish & Richardson, Erise IP, Irell & Manella, O'Melveny & Myers, Perkins-Coie, Pillsbury Winthrop Shaw Pittman and Slayden Grubert Beard.

Library Director, February 2013 - March 2015
Dowagiac District Library ● Dowagiac, Michigan

- Executive administrator of the Dowagiac District Library. Located in

Southwest Michigan, this library has a service area of 13,000, an annual operating budget of over $400,000 and total assets of approximately $1,300,000.

● Developed careful budgeting guidelines to produce a 15% surplus during the 2013-2014 & 2014-2015 fiscal years while being audited.

● Using this budget surplus, oversaw significant library investments including the purchase of property for a future building site, demolition of existing buildings and building renovation projects on the current facility.

● Led the organization and digitization of the library's archival records.

● Served as the public representative for the library, developing business relationships with local school, museum and tribal government entities.

● Developed an objective-based analysis system for measuring library services - including a full collection analysis of the library's 50,000+ circulating items and their records.

November 2010 - January 2013
Librarian & Branch Manager, Anchorage Public Library ● Anchorage, Alaska

● Headed the 2013 Anchorage Reads community reading campaign including event planning, staging public performances and creating marketing materials for mass distribution.

● Co-led the social media department of the library's marketing team, drafting social media guidelines, creating original content and instituting long-term planning via content calendars.

● Developed business relationships with The Boys & Girls Club, Anchorage School District and the US Army to establish summer reading programs for children.

June 2004 - September 2005, September 2006 - October 2013
Library Assistant, Hart Area Public Library
Hart, MI

● Responsible for verifying imported MARC records and original MARC

cataloging for the local-level collection as well as the Michigan Electronic Library.

● Handled OCLC Worldcat interlibrary loan requests & fulfillment via ongoing communication with lending libraries.

Professional Involvement

Alaska Library Association - Anchorage Chapter
- Treasurer, 2012

Library Of Michigan
- Level VII Certification, 2008
- Level II Certification, 2013

Michigan Library Association Annual Conference 2014
- New Directors Conference Panel Member

Southwest Michigan Library Cooperative
- Represented the Dowagiac District Library, 2013-2015

Professional Development

Library Of Michigan Beginning Workshop, May 2008
Petoskey, MI
- Received training in cataloging, local history, collection management, children's literacy and reference service.

Public Library Association Intensive Library Management Training, October 2011
Nashville, TN
- Attended a five-day workshop focused on strategic planning, staff management, statistical analysis, collections and cataloging theory.

Alaska Library Association Annual Conference 2012 - Fairbanks, February 2012
Fairbanks, AK
- Attended seminars on EBSCO advanced search methods, budgeting, cataloging, database usage and marketing.

Depositions

2019 ● Fish & Richardson

Apple v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282 and 39521-00421IP2)

2019 ● Erise IP

Implicit, LLC v. Netscout Systems, Inc (Civil Action No. 2:18-cv-53-JRG)

2019 ● Perkins-Coie

Adobe Inc. v. RAH Color Technologies LLC (Cases IPR2019-00627, IPR2019-00628, IPR2019-00629 and IPR2019-00646)

2020 ● O'Melveny & Myers

Maxell, Ltd. v. Apple Inc. (Case No. 5:19-cv-00036-RWS)

2021 ● Pillsbury Winthrop Shaw Pittman LLP

Intel v. SRC (IPR2020-1449)

2022 ● Perkins-Coie

Realtek v. Future Link (IPR2021-01182)

2023 ● Fish & Richardson

Neuroderm Ltd. v. Abbvie, Inc (Case No. PGR2022-00040)

2023 ● Fish & Richardson

Nearmap US Inc. v. Pictometry International Corp. (IPR2022-00735)

2023 ● Fish & Richardson

Samsung Electronics v. MemoryWeb LLC (Case No. 39843-0136PS1)

2023 ● Pillsbury Winthrop Shaw Whitman LLP

Gravel Rating Systems v. Costco Wholesale Corp. (Civil Action No. 4:21-cv-149-ALM)

2024 ● Willkie-Farr

Netflix, Inc. v. VideoLabs. Inc. (IPR2023-00628)

Limited Case and Clientele History

Alston & Bird

- Ericsson

  v. Collision Communications (IPR2022-01233)

- Nokia

  v. Neptune Subsea, Xtera (Case No. 1:17-cv-01876)

- Universal Electronics Inc

  v. Roku Inc (IPR2022-00818)

Arnold & Porter

- Ivantis

  v. Glaukos (Case No. 8:18-cv-00620)

- Samsung

  v. Jawbone (Case No. 2:21-cv-00186)

Benesch Friedlander Coplan & Aronoff

- Voyis

  v. Cathx (Case No. 5:21-cv-00077-RWS)

Deschert LLP

- Smaxtec Animal Care

  v. ST Reproductive Technologies, LLC (IPR2024-00885)

Erise I.P.

- Apple

  v. Ericsson Inc. (IPR2022-00715)

  v. Future Link Systems (IPRs 6317804, 6622108, 6807505, and 7917680)

  v. INVT (Case No. 20-1881)

  v. Navblazer LLC (IPR2020-01253)

  v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)

  v. Quest Nettech Corp (Case No. 2:19-cv-00118-JRG)

  v. Telefonaktiebolaget LM Ericsson (IPR2022-00275)

  v. Theta IP, LLC (IPR2024-00818)

- Fanduel

  v. CGT (Case No. 19-1393)

- Garmin

  v. Phillips North America LLC (Case No. 2:19-cv-6301-AB-KS)

- Netscout
    - v. Longhorn HD LLC (Case No. 2:20-cv-00349)
    - v. Implicit, LLC (Civil Action No. 2:18-cv-53-JRG)

- Sony Interactive Entertainment LLC
    - v. Bot M8 LLC (IPR2020-01288)
    - v. Infernal Technology LLC (Case No. 2:19-CV-00248-JRG)

- Unified Patents
    - v. GE Video Compression (Civil Action No. 2:19-cv-248)

Fish & Richardson

- Apple
    - v. AliveCor (3:21-cv-03958)
    - v. LBS Innovations (Case No. 2:19-cv-00119-JRG-RSP)
    - v. Koss Corporation (IPR2021-00305)
    - v. Masimo (IPR 50095-0012IP1, 50095-0012IP2, 50095-0013IP1, 50095-0013IP2, 50095-0006IP1, 50095-0135IP1)
    - v. Neonode (Case No. 21-cv-08872-EMC)
    - v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)

- Dell
    - v. Neo Wireless (IPR2022-00616)

- Dish Network
    - v. Entropic Communications, LLC (Case No. 2:2023-CV-01043)

v. Realtime Adaptive Streaming (Case No. 1:17-CV-02097-RBJ)

v. TQ Delta LLC (Case No. 18-1798)

- Evapco Dry Cooling

  v. SPG Dry Cooling (IPR2021-00688)

- Genetec

  v. Sensormatic Electronics (Case No. 1:20-CV-00760)

- Huawei

  v. Bell Northern Research LLC (IPR2019-01174)

- Kianxis

  v. Blue Yonder (Case No. 3:20-cv-03636)

- LG Electronics

  v. Bell Northern Research LLC (Case No. 3:18-cv-2864-CAB-BLM)

- Metaswitch

  v. Sonus Networks (IPR2018-01719)

- Microsoft

  v. Throughputer Inc (IPR2022-00757)

- Mom Enterprises

  v. Ddrops Company (Case No. 1:22-cv-00332)

- MLC Intellectual Property

v. MicronTech (Case No. 3:14-cv-03657-SI)

- Nearmap Inc
  - v. EagleView Technologies (IPR2022-01009)

- Neuroderm Ltd.
  - v. Abbvie, Inc (Case No. PGR2022-00040)

- Realtek Semiconductor
  - v. Future Link (IPR2021-01182)

- Quectel
  - v. Koninklijke Philips (Case No. 1:20-cv-01710)

- Samsung
  - v. Aire Technology (IPR2022-00877)
  - v. Bell Northern Research (Case No. 2:19-cv-00286-JRG)
  - v. Communication Technologies Inc (IPR2022-01221)
  - v. Jawbone Innovations (IPR2022-00865)
  - v. MemoryWeb LLC (IPR2022-00885)
  - v. Dodots Licensing Solutions (IPR2023-00701)
  - v. Telefonaktiebolaget LM Ericsson (IPR2021-00615)

- Texas Instruments
  - v. Vantage Micro LLC (IPR2020-01261)

- Xilinx
  - v. Sentient Sensors LCC (Case No. 1:22-cv-00173)

Groombridge Wu

- Nearmap

  v. Eagle View Technologies Inc. and Pictometry International Corp. (Case No. 2:21-cv-00283-TS-DAO)

Irell & Manella

- Curium

O'Melveny & Myers

- Apple

  v. Maxell (Case No. 5:19-cv-00036-RWS)

- Disney Media & Entertainment Distribution LLC

  v. Digital Media Technology Holdings, LLC (Case No. 2:22-cv-01642)

- Micron Technology Inc.

  v. Besang Inc (IPR2023-00900)

- Samsung

  v. Daedalus Prime LLC (1335 Investigation)

Perkins-Coie

- Amazon

  v. Nokia (IPR2024-00847 and IPR2024-00848)

- Heru Industries
  - v. The UAB Research Foundation (IPR2022-01148)
- Intel Corporation
  - v. BeSang Inc. (IPR2023-00991)
  - v. BitMICRO (Case No. 5:23-cv-00625)
  - v. Telefonaktiebolaget L M Ericsson (IPR2024-00610)
- Realtek Semiconductor
  - v. Future Link (IPR2021-01182)
- Twitter Inc
  - v. VOIP-Pal.com (Case No. 3:20-cv-02397-JD)
- TCL Industries
  - v. Koninklijke Philips NV (IPR2021-00495, IPR2021-00496 and IPR2021-00497)

Pillsbury Winthrop Shaw Pittman

- Intel
  - v. FG SRC LLC (Case No. 6:20-cv-00315)
- Gravel Rating Systems
  - v. Costco (Case No. 4:21-cv-149)
  - v. Lowe's Home Centers (Case No. 4:21-cv-150)
  - v. T-Mobile USA (Case No. 4:21-cv-152)
  - v. Kohl's Inc. (Case No. 4:21-cv-258)
  - v. Under Armor (Case No. 4:21-cv-356)

Quinn Emanuel

- ServiceNow, Inc.

  v. InQuisient, Inc. (Case No. 22-900-CJB)

- Wolfspeed

  v. The Trustees of Purdue University (Case No. 1:2021-cv-00840)

Sheppard, Mullin, Richter & Hampton LLP

- Cadence Design Systems Inc.

  v. Semiconductor Design Technologies (Case No. 3:23-cv-01001)

Stern, Kessler, Goldstein & Fox

- Preliminary Research

Willkie, Farr & Gallagher LLP

- Neurent

  v. The Foundry, LLC (IPR2024-00669)

- Netflix, Inc.

  v. VideoLabs, Inc. (IPR2023-00628)

ATTACHMENT - Al-ALAWI01 - UIC MARC

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Chat with a Librarian



MULTIPLE VERSIONS

Journal of circuits, systems, and computers.

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May be requested

Details

Title	Journal of circuits, systems, and computers.
Subject	Electronics -- Periodicals › Electronic circuits -- Periodicals › Computers -- Periodicals › Systems engineering -- Periodicals ›
Related titles	Available in other form: Journal of circuits, systems, and computers. ›
Publisher	Singapore ; New Jersey : World Scientific Vol. 1, no. 1 (Mar. 1991)-
Creation Date	c1991-
Format	v. : ill. ; 25 cm.
Frequency	Quarterly
Identifier	LC : 91642755 ISSN : 0218-1266 OCLC : (OCoLC)ocm24310702
Source	Library Catalog

Virtual Browse



Industrial electronics. ...
1962-1968

IEEE student papers. ...
1975

Journal of circuits, systems, and computers. ...
c1991-

Journal of electronics and control. ...
1957-1964

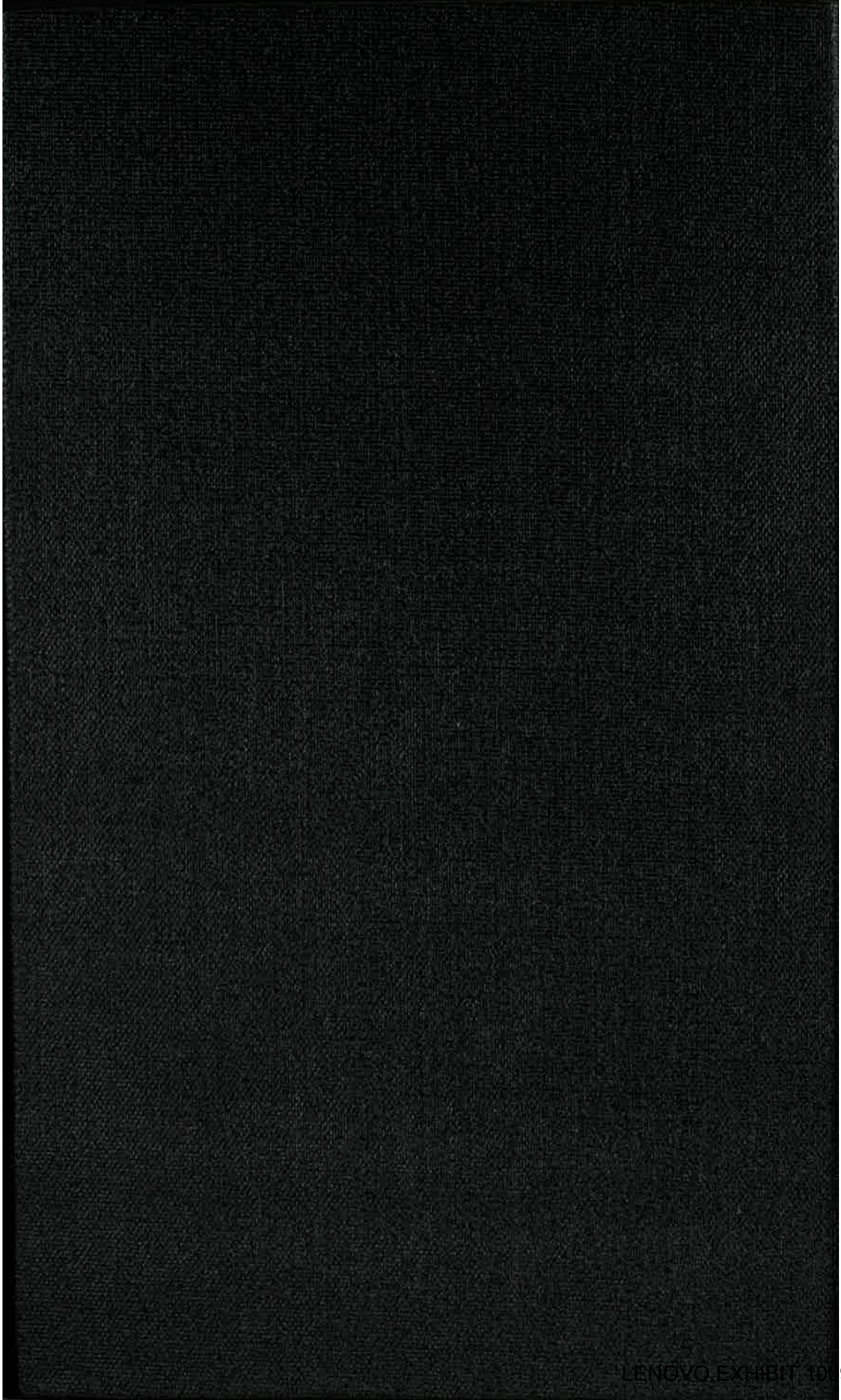
International journal of electronics.
1965-

Links

Display Source Record ›

Chat with a Librarian

ATTACHMENT AL-ALAWI02 - UIC Scans



JOURNAL OF CIRCUITS, SYSTEMS, AND COMPUTERS

15
No.1-3

2006

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DESIGN OF A MULTICODE BI-PHASE ENCODER FOR DATA TRANSMISSION

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Revised 15 August 2005

In this paper, we present a versatile Multicode Bi-Phase Encoder (MBPE) circuit capable of encoding five different Bi-Phase line codes, namely: Bi-Phase-Level (Bi-Φ-L), Bi-Phase-Mark (Bi-Φ-M), Bi-Phase-Space (Bi-Φ-S), Differential Manchester (DM) and Inverse Differential Manchester (IDM) codes. The design methodology is based on a new definition of these codes in terms of encoding rules and state diagrams, instead of the traditional way of representing them in terms of their bit transition. The operation mode of the MBPE is set by three selection lines, which can be either hardware or software controlled. This will facilitate the process of altering the data transmission protocol without the need of changing the encoder hardware. The functionality and design of the MBPE is outlined. VHDL has been used to describe the behavior of the MBPE whose operation was verified using the *ModelSim XE II* Simulation tools. Implementation and testing of the MBPE on XILINX Spartan-II FPGA showed that the MBPE circuit is capable of encoding NRZ data into any of the five codes.

Keywords: Line codes; Bi-phase codes; encoder design; data transmission.

1. Introduction

Advances in data transmission and various digital communications network architectures have resulted in an increased demand to multimedia applications where data, voice, images and video signals are to be transmitted. These networks are becoming very large, and often their nodes have several different connections between them utilizing more than one protocol. Different protocols normally employ different line (modulation) codes, and hence, it is important to develop a controller in the physical layer that can cope with multiple protocols. It is common nowadays to have off-the-shelf multiprotocol communication boards operating several line codes in order to minimize parts swapping.[1] A typical digital transmission

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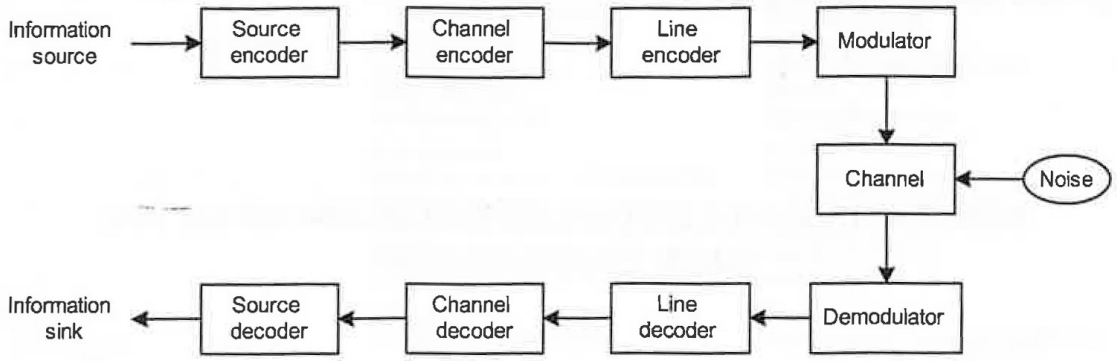


Fig. 1. Digital transmission system.

system is shown in Fig. 1. Source encoding reduces the average number of data bits for a given message to the minimum possible value while channel coding is used for error control. Line coding is used to transform blocks or sequences of symbols into physical signals well matched to the characteristics of the physical channel of the system. After passage through the channel, the decoding processes are in the reverse order. This letter is concerned with the line encoder.

Several line coding techniques suitable for data transmission have been devised. Among these codes are Bi-Phase-Level (Bi-Φ-L), Bi-Phase-Mark (Bi-Φ-M), Bi-Phase-Space (Bi-Φ-S), Differential Manchester (DM), and Inverse Differential Manchester (IDM) codes. These widely used codes belong to the Bi-Phase code family which is characterized by having at least one transition per bit time. They share many desirable properties such as DC free component, self-clocking and error detection capability. DC free prevents the transmission line from being saturated, while self-clocking is an attractive feature in several applications (such as wireless communications and local area networks "LAN") where a separate clock line is not possible and/or not practical. The absence of a transition within one bit can be used for error detection. This family of Bi-Phase codes is very popular in many data communication and data storage applications. The Bi-Φ-L code has been specified for the IEEE 802.3 standard in the Carrier Sense Multiple Access/Collision Detection (CSMA/CD) protocol used in Ethernet networks.[2] It has also been specified in the MIL-STD-1553B bus standard, which is a shielded twisted-pair bus LAN designed to ensure high integrity data exchange between unattended equipment in military airplanes, ships and land vehicles.[3] Bi-Φ-M and Bi-Φ-S are the parts of the specification in amateur satellite system.[4] Bi-Φ-M is used as an industry standard for single density magnetic floppy disk recording.[5] It is also used in some optical communications and satellite telemetry applications.[6] The LocalTalk® LAN system that implemented in Apple Macintosh uses Bi-Φ-S encoding as a transmission format.[7] DM code is popular in data communications and has been specified for use as part of the physical layer in the IEEE 802.5 Token Ring local area network.[8]

Currently, there is very little work in the open literature concerning the circuit implementation for encoding these codes, and if they exist, they generally encode a single code. Some of the design presented is based on the use of one shot and/or

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delay circuits.[9] These devices are considered inferior (more expensive and could introduce noise) to the completely synchronous circuit presented here. This work develops a design of a versatile Bi-Phase encoder circuit that can handle the change in the baseband encoding scheme without the need to swap the hardware. The circuit can encode any NRZ serial bit stream into any one of the popular Bi-Phase codes, namely, Bi-Φ-L, Bi-Φ-M, Bi-Φ-S, DM, and IDM.

The paper is organized as follows. Section 2 gives a brief classical description of the five Bi-Phase line codes. In Sec. 3, a new description for Bi-Phase codes in terms of state diagrams is presented. Section 4 shows the MBPE hardware implementation and Sec. 5 illustrates its VHDL simulation results.

2. Bi-Phase Codes Overview

Bi-Phase codes are self clocking codes in which the clocking information is embedded within the serial bit stream and can be recovered without the need for a separate clocking signal, as there is at least one transition per bit period. These codes are briefly described below.

Bi-Φ-S: This code is also called FM0[11] and classified as IFM-V6.[12] In this code a transition is present at the start of every transmitted bit, with "0" represented by an additional transition at the middle of the bit period.

Bi-Φ-M: This code is also known as FM1 code[11] and classified as FM-V6 code.[12] In this code a transition is present at the start of every transmitted bit, with "1" represented by an additional transition at the middle of the bit period.

Bi-Φ-L: This code is also known as Manchester and split-phase code.[10] In this code there is always a transition at the middle of each bit, with "0" encoded as low-to-high transition and "1" encoded as high-to-low transition.

DM: This code is also referred to as Differential Bi-Phase Space.[13] In this code a transition always occurs at the middle of the transmitted bit period with "0" represented by an extra transition at the beginning of the bit period.

IDM: In this code a transition always occurs at the middle of the transmitted bit period with "1" represented by an extra transition at the beginning of the bit period. By analogy to DM this code can also be referred to as Differential Bi-Phase Mark. A summary of operation of all of the five codes is given in Table 1.

2.1. *Encoding rule definition*

In order to lay the ground for our synchronous design (Sec. 3) new representations of the five biphase codes were developed. These representations are based on a new definition of the five bi-phase codes in terms of encoding rules as well as their state diagrams, apparently for the first time in the open literature. To accommodate middle and beginning of bit transitions, the encoded output is divided into two

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Table 1. Codes summary of operation.

	"0" trans. at		"1" trans. at	
Code	Beg	Mid	Beg	Mid
Bi-Phase-Space	↕	↕	↕	—
Bi-Phase-Mark	↕	—	↕	↕
Bi-Phase-Level	x	↑	x	↓
Differential Manchester	↕	↕	—	↕
Inverse Diff Manchester	—	↕	↕	↕

↑ = 0 to 1 transition, ↓ = 1 to 0 transition, ↕ = transition,
x = (may/may not be a transition), — = no transition.

half bits. The current output is represented by y_{1k} and y_{2k}, representing the first and second half bits, respectively. The next pulse output half bits are given by $y_{1(k+1)}$ and $y_{2(k+1)}$. The next pulse output depends on the current output (y_{1k}, y_{2k}) and the current input (x_k). The output symbols during each half bit can take the values -1 or $+1$, are recorded as $\{-$ or $+\}$ for simplicity. To satisfy the characteristics of the code (always transition in the middle), Bi-Φ-L, DM and IDM encoder do not produce $\{++\}$ or $\{--\}$ outputs, but state $\{- -\}$ occurs only once as initial condition. The standard definitions of all five codes, presented in Table 1, are translated to the coding rule listed in Table 2.

The coding rules for all five codes are translated into Eqs. (1)–(5), respectively.

$$\text{Bi-}\Phi\text{-S:} \quad y_{1(k+1)} = -y_{2k}\,, \qquad y_{2(k+1)} = -y_{2k}(2x_k - 1)\,, \tag{1}$$

$$\text{Bi-}\Phi\text{-M:} \quad y_{1(k+1)} = y_{2k}\,, \qquad y_{2(k+1)} = y_{2k}(2x_k - 1)\,, \tag{2}$$

$$\text{Bi-}\Phi\text{-L:} \quad y_{1(k+1)} = x_k\,, \qquad y_{2(k+1)} = -x_k\,, \tag{3}$$

$$\text{DM:} \quad y_{1(k+1)} = y_{2k}(2x_k - 1)\,, \qquad y_{2(k+1)} = -y_{2k}(2x_k - 1)\,, \tag{4}$$

$$\text{IDM:} \quad y_{1(k+1)} = -y_{2k}(2x_k - 1)\,, \qquad y_{2(k+1)} = y_{2k}(2x_k - 1)\,. \tag{5}$$

3. Design of the Multicode Bi-Phase Encoder

In this section the design of a Multicode Bi-Phase Encoder (MBPE) digital circuit is presented. The circuit is capable of encoding NRZ data format into five different Bi-Phase codes, namely, the Bi-Φ-L, Bi-Φ-M, Bi-Φ-S, DM, and IDM line codes. Three *code select* inputs are used to alter the encoding scheme.

3.1. *Functional description*

The block diagram of the Bi-Phase encoder is shown in Fig. 2.

The encoder accepts as an input: the three code select lines ($C_2C_1C_0$), the serial NRZ bit stream (INP), an asynchronous RESET input and a clock signal. The encoder generates a single output (Z_{out}) that represents one of the Bi-Phase codes listed in Table 1, depending on the settings of the code select lines. The clock frequency used in this encoder circuit is double the frequency of the incoming NRZ bit stream.

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Table 2. Bi-Phase coding rule.

		Bi-Φ-S				Bi-Φ-M				Bi-Φ-L				DM				IDM			
		$x_k=0$		$x_k=1$		$x_k=0$		$x_k=1$		$x_k=0$		$x_k=1$		$x_k=0$		$x_k=1$		$x_k=0$		$x_k=1$	
y_1	y_2	y_1^+	y_2^+	y_1^+	y_2^+	y_1^+	y_2^+	y_1^+	y_2^+	y_1^+	y_2^+	y_1^+	y_2^+	y_1^+	y_2^+	y_1^+	y_2^+	y_1^+	y_2^+	y_1^+	y_2^+
−	−	+	−	+	−	+	+	+	−	−	+	+	−	+	−	−	+	−	+	+	−
−	+	−	+	−	+	−	−	−	+	−	+	+	−	−	+	+	−	+	−	−	+
+	−	+	−	+	−	+	+	+	−	−	+	+	−	−	+	+	−	−	+	+	−
+	+	−	+	−	−	−	−	−	+	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx

$y_1 = y_{1k}$, $y_2 = y_{2k}$, $y_1^+ = y_{1(k+1)}$, $y_2^+ = y_{2(k+1)}$, xx = not defined.

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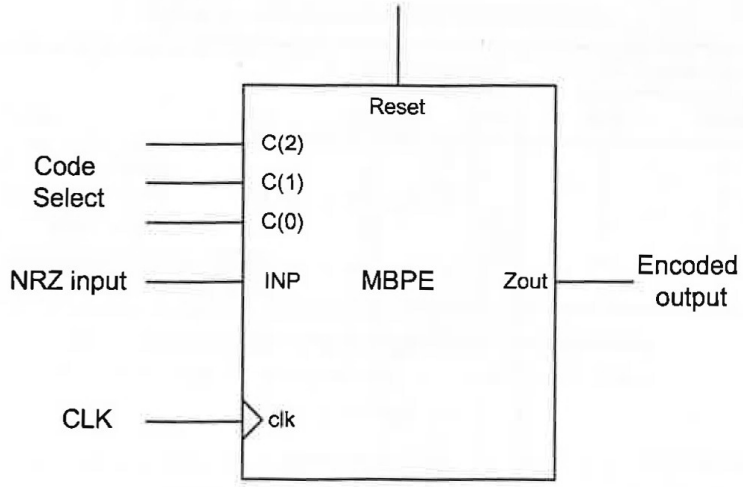


Fig. 2. MBPE block diagram.

3.2. *Behavioral description of the encoder*

The behavior of the encoder circuit can be best described by a Moore type state machine. For clarity, the state diagram for each code is drawn separately in Fig. 3.

By inspecting these state machines, it is noticed that they share a common feature where they all consist of four states, with two states having an output of "0" and the other two having an output of "1". The two states with "0" outputs are named S_0 and S_1 while the other two states (with "1" outputs) are S_2 and S_3. These five state graphs are translated into a single state table as shown in Table 3. Table 3 also shows how the control lines C_2, C_1, and C_0 are assigned to the different Bi-Phase codes.

The next step toward the design of the encoder circuit is to decide on state encoding. Research has shown that changing state assignment can dramatically affect the performance of code targeted to a specific device or architecture. Therefore, a poor state assignment will result in a state machine that uses too much logic, or is too slow, or both. Various approaches have been developed for finding the "optimal" state assignment.[14] It must be mentioned here that the method of assigning binary codes to the five Bi-Phase codes (i.e. binary assignment for inputs $C2$, $C1$, $C0$) also affects the realization cost of the encoder. By carrying on an exhaustive search to the minimum circuit realization, it was found that almost all possible combination of code-selection and state assignments lead to logic circuits having a comparable realization cost that lies between a total gate cost of 16–20 and a total number of input cost between 72 and 74. Straight binary assignment is among one of the possible state assignments that led to a minimum realization cost with a gate cost of 16 gates and total number of gate's inputs of 72. Therefore, for simplicity, straight binary assignment for the states is selected, with the code selection assignment shown in Table 3. With this state assignment, the D flip-flops

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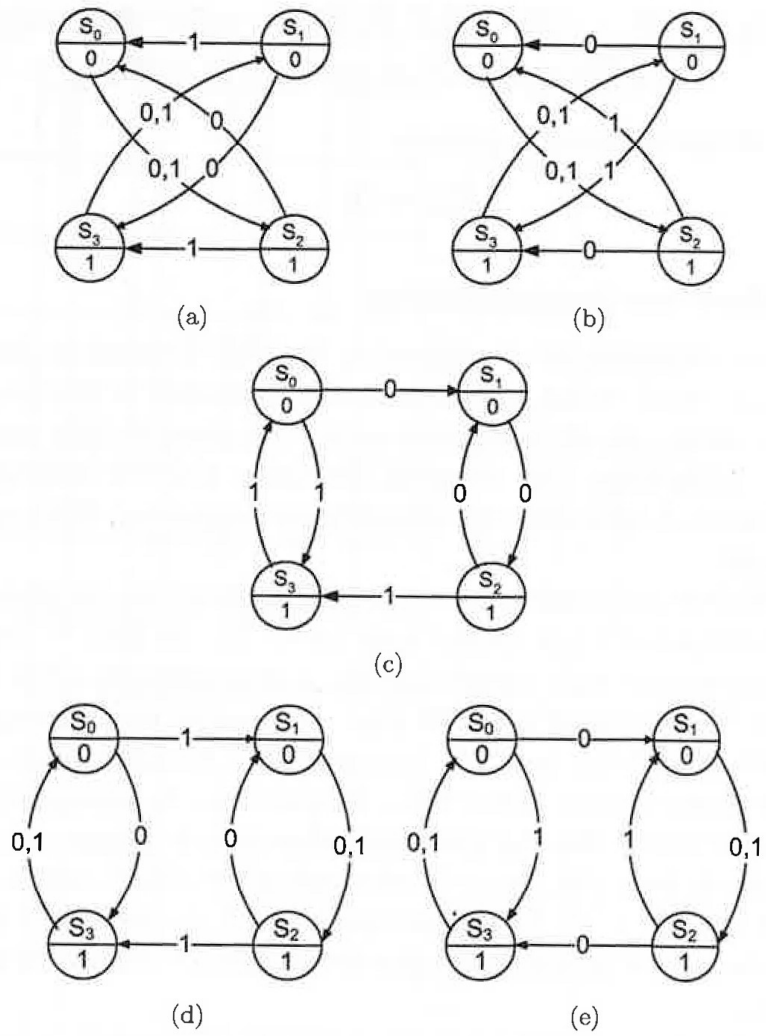


Fig. 3. State diagrams for all five Bi-Phase codes.

Table 3. State assignment for all five codes.

State assignment	Present state	$C_2C_1C_0$ IN	Next state: Bi-Φ-S 000		Bi-Φ-M 001		Bi-Φ-L 010		DM 011		IDM 100		Output
			0	1	0	1	0	1	0	1	0	1	Z
00	S0		S2	S2	S2	S2	S1	S3	S3	S1	S1	S3	0
01	S1		S3	S0	S0	S3	S2	—	S2	S2	S2	S2	0
10	S2		S0	S3	S3	S0	S1	S3	S1	S3	S3	S1	1
11	S3		S1	S1	S1	S1	—	S0	S0	S0	S0	S0	1

input equations are given by:

$$D_1 = \overline{C}_2\overline{C}_0\,\mathrm{INP}\,\overline{Q}_0 + \overline{C}_1C_0\,\overline{\mathrm{INP}}\,\overline{Q}_0 + C_1\,\mathrm{INP}\,Q_1\overline{Q}_0 + C_2\,\overline{\mathrm{INP}}\,Q_1\overline{Q}_0 + C_1C_0\,\overline{\mathrm{INP}}\,\overline{Q}_1 + \overline{C}_0\,\overline{\mathrm{INP}}\,\overline{Q}_1Q_0 + \overline{C}_2\overline{C}_1\overline{Q}_1\overline{Q}_0 + C_2\,\mathrm{INP}\,\overline{Q}_1 + C_0\,\mathrm{INP}\,\overline{Q}_1\overline{Q}_0\,, \tag{6}$$

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$$D_0 = C_1\overline{Q}_0 + C_2\overline{Q}_0 + \overline{C}_2\overline{C}_1\overline{C}_0\,\overline{\mathrm{INP}}\,Q_0 + \overline{C}_2\overline{C}_1\overline{C}_0\,\mathrm{INP}\,Q_1 + C_2\,\overline{\mathrm{INP}}\,Q_1\overline{Q}_0 + \overline{C}_1C_0\,\mathrm{INP}\,Q_0 + \overline{C}_1C_0\,\overline{\mathrm{INP}}\,Q_1\,. \quad (7)$$

The encoder output equation is given by

$$Z_{\mathrm{out}} = Q_1\,. \quad (8)$$

4. MBPE Hardware Implementation

Various digital techniques for implementing the MBPE circuit in hardware exist. The simplest is based on the derived equations presented in the previous section (Eqs. (6)–(8)) using discrete logic gates and D flip flops. In this case, the circuit requires two D flip-flops, four inverters, seventeen 4-inputs AND gates and six 4-inputs OR gates. A total of 14 SSI (Small Scale Integration) ICs is needed for the complete design.

A more efficient implementation of the MBPE circuit can be achieved by using a Programmable Array Logic (PAL) such as the 22V10 PAL.[15] The 22V10 is a versatile programmable logic device that has a programmable AND array feeding ten OR gates. The output of each OR gate is connected to programmable Marco-cells that contains a D flip flop. The logic described by Eqs. (6)–(8) can be easily accommodated into a single 22V10 PAL. This will lead to a simpler design that is smaller in size, cheaper, uses less power and more reliable. Figure 4 shows a generic connection matrix for a PAL device implementing the MBPE circuit.

An alternative approach for the implantation of the encoder is to use VHDL (VHSIC Hardware Description Language) for describing the behavior of the encoder state diagram.

VHDL is a technology independent design tool that permits the creation of a portable design and simulating it without the need of specifying the target hardware.[16] The above five state machines are combined into a single state machine whereby the transition from one state to another depends on the incoming NRZ code as well as on the code select inputs. The combined MBPE state machine has been described and simulated in VHDL.

5. VHDL Simulation Results

The MBPE circuit is coded in VHDL then simulated, tested and implemented into XILINX Spartan-II FPGA. To verify the behavior of VHDL source code of the MBPE, a VHDL test bench is generated. This test bench is applied as a stimulus to the MBPE. The design is simulated and tested using *ModelSim XILINX Edition* Simulation Environment.[17] Various test patterns are tried and it is found that the MBPE can encode the five different Bi-Phase line codes successfully. The VHDL code verification results are shown in Figs. 5–9 for the Bi-Φ-S, Bi-Φ-M, Bi-Φ-L, DM, and IDM, respectively. In these figures, the waveforms represent clock (CLK), reset, NRZ data input (INP) and encoded output (Z_{out}) signals respectively from

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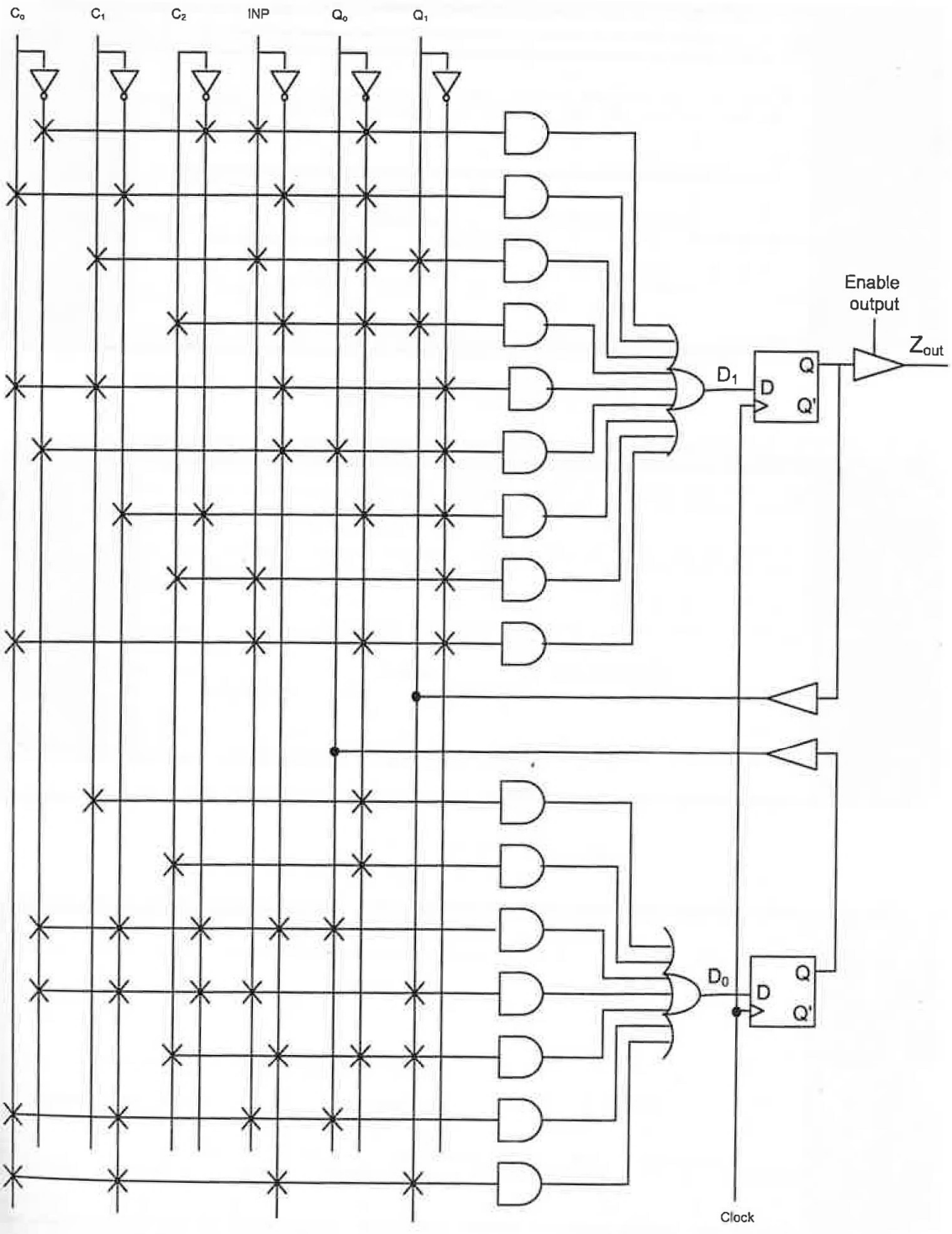


Fig. 4. Connection matrix for a PAL device realizing the MBPE circuit.

top to bottom. The results shown in these figures are for the test pattern 011010011 represented by the serial NRZ bit stream (INP). This test pattern is selected to assess the encoders under various conditions including consecutive ones and consecutive zeros. Each bit last for two clock cycles since the clock frequency (CLK) used

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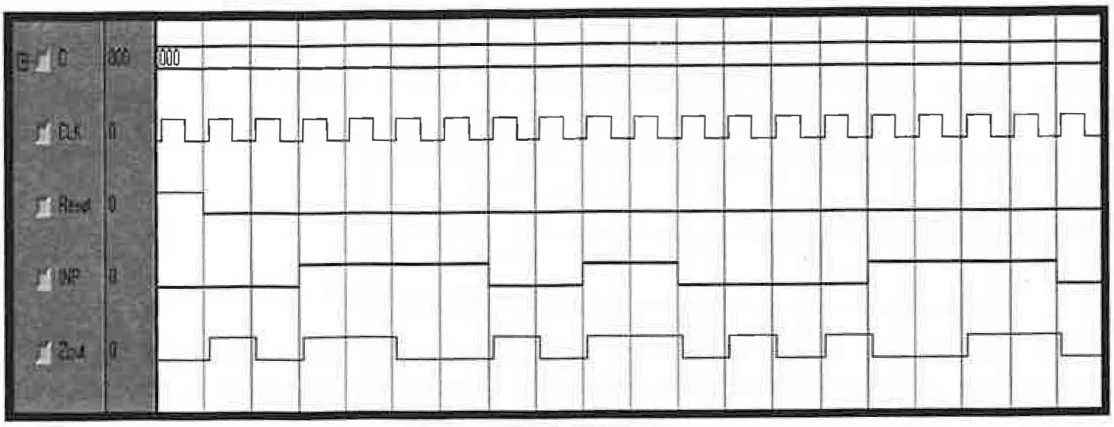


Fig. 5. Bi-Φ-S encoder output.

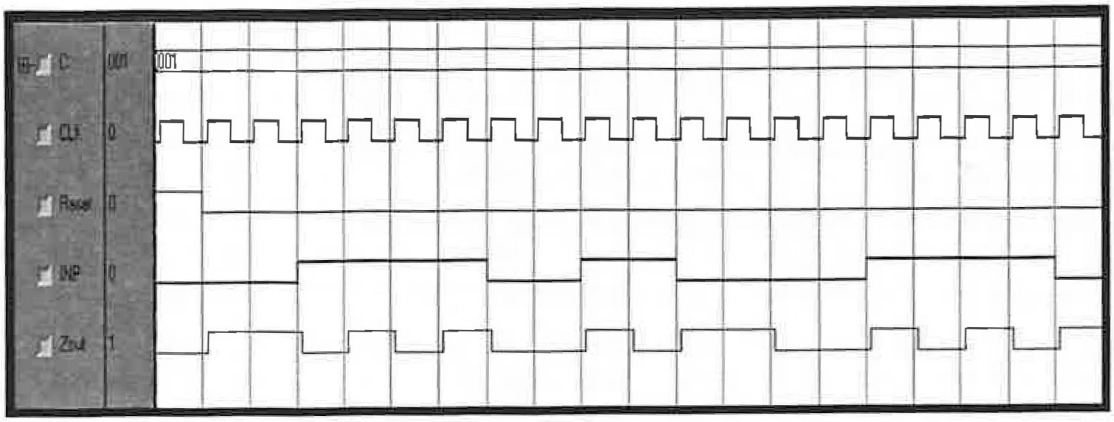


Fig. 6. Bi-Φ-M encoder output.

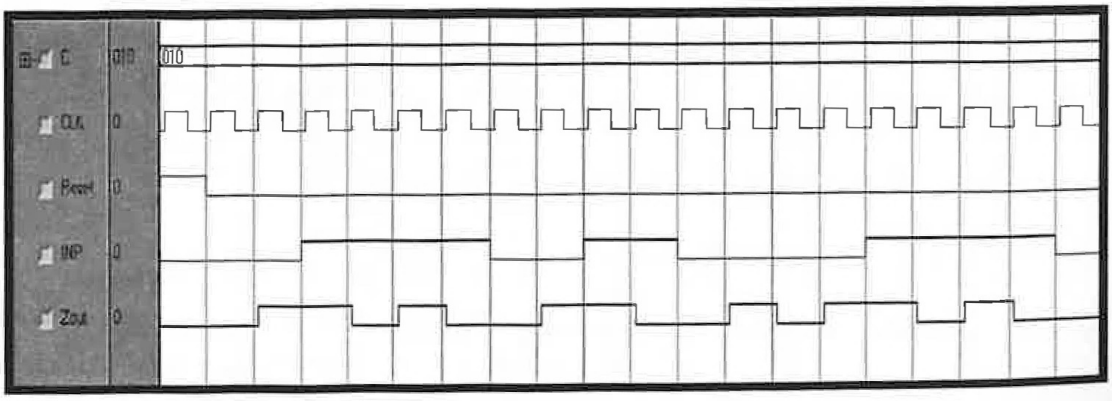


Fig. 7. Bi-Φ-L encoder output.

in this encoder circuit is double the frequency of the incoming NRZ data input. The generated encoder's output Z_{out} is synchronized with the positive edge of the CLK pulse and the generated Z_{out} waveform agrees with the expected encoder results for the five bi-phase codes.

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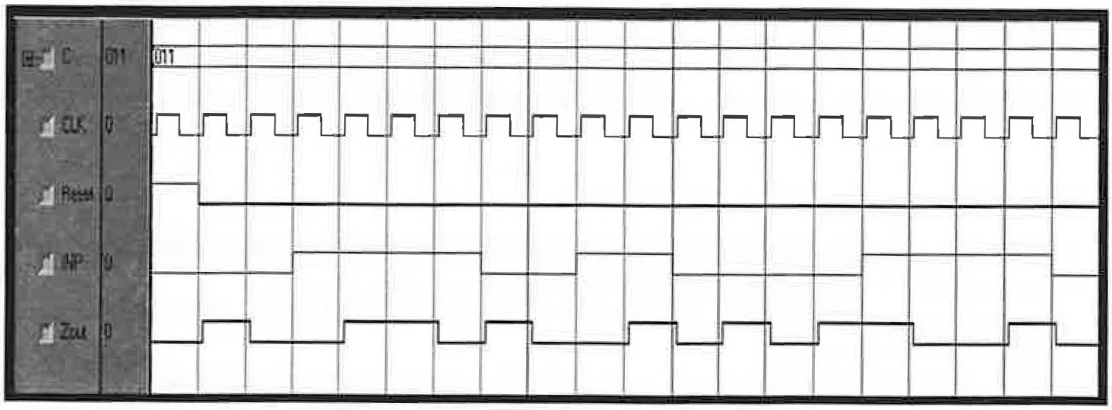


Fig. 8. DM encoder output.

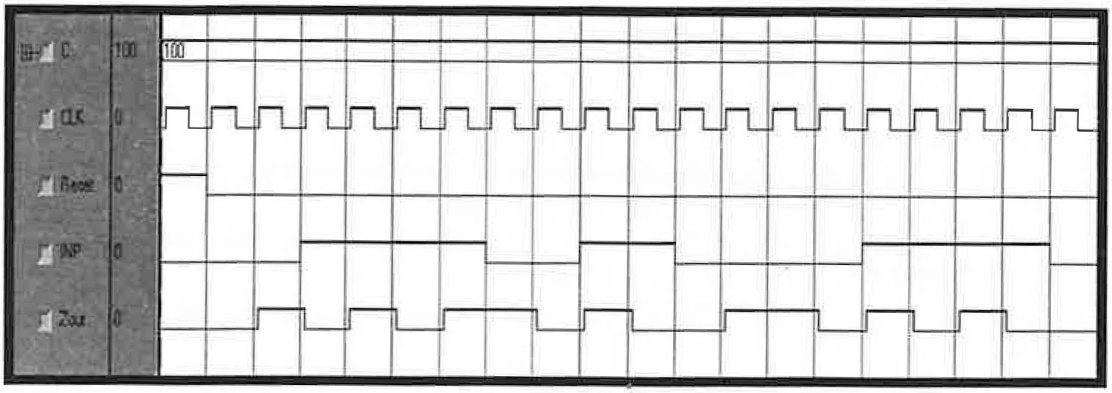


Fig. 9. IDM encoder output.

When implemented on XILINX Spartan-II FPGA, the MBPE has occupied six slices out of the 2352 total slices on chip with an equivalent gate count equals to 85.

6. Conclusions

In this paper, a new approach for designing a Muticode Bi-Phase Encoder (MBPE) is presented. The encoder is capable of encoding any NRZ bit stream into one of five Bi-Phase codes, namely, Bi-Phase-level, Bi-Phase-Mark, Bi-Phase-Space, Differential Manchester and Inverse Differential Manchester codes. The encoder design methodology is based on defining the state machine of the five codes and combining them into a single machine with code selection capability. The Behavior of the encoder is described in VHDL and simulated using *ModelSim XILINX Edition* Simulation tools. Simulation results shows that the encoder has successfully encoded the NRZ code into any of the selected Bi-Phase codes. As a result, this design can be targeted without modifying the VHDL source code towards a range of PLD devices. The significance of the proposed design is the ability to change the encoding scheme without the need for swapping hardware. Switching from one encoding

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scheme to another is performed by simply changing the inputs at the code selection lines. The proposed network can be inserted in larger communication systems that can handle multiple protocols and use bi-phase data encoding formats.

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