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17 **UNITED STATES DISTRICT COURT**
NORTHERN DISTRICT OF CALIFORNIA
18 **OAKLAND DIVISION**

19 UNIVERSAL CONNECTIVITY
TECHNOLOGIES INC.,

20 Plaintiff,

21 v.

22 HP INC.,

23 Defendant.

Case No. 4:24-cv-04097-YGR

**HP'S INVALIDITY CONTENTIONS
PERSUANT TO PATENT LOCAL RULE
3-3**

24
25 **HP'S INVALIDITY CONTENTIONS**

26 Pursuant to Patent Local Rule 3-3 and Court's Scheduling Order (Dkt. 93), defendant HP
27 Inc. ("HP" or "Defendant") respectfully submits these invalidity contentions with respect to the
28 asserted claims of U.S. Patent Nos. 7,154,905 ("the '905 Patent"), 7,187,307 ("the '307 Patent"),

HP'S INVALIDITY CONTENTIONS PERSUANT TO PATENT LOCAL RULE 3-3
Case No. 4:24-cv-04097-YGR

- 1 -

1 7,746,798 (“the ’798 Patent”), 9,232,265 (“the ’265 Patent”), 8,680,712 (“the ’712 Patent”),
2 7,856,520 (“the ’520 Patent”), 7,921,231 (“the ’231 Patent”), and 9,852,103 (“the ’103 Patent”)
3 (collectively, the “Asserted Patents”) identified by Plaintiff Universal Connectivity Technologies
4 Inc., (“UCT” or “Plaintiff”) in its Infringement Contentions.

5 The currently Asserted Claims, as reflected in Plaintiff’s Infringement Contentions, are:

- 6 • ’905 Patent: Claims 1, 8, 15, 21, 22, 23
- 7 • ’307 Patent: Claims 1, 7, 23, 25, 53, 68, 72
- 8 • ’798 Patent: Claims 11, 19, 22, 25, 28
- 9 • ’265 Patent: Claims 1, 8, 11, 14
- 10 • ’712 Patent: Claims 1, 5, 7
- 11 • ’520 Patent: Claims 1, 8, 10, 12, 13, 15, 19
- 12 • ’231 Patent: Claims 1, 2, 10, 11, 12, 13, 16
- 13 • ’103 Patent: Claims 1, 3, 11, 17, 21, 22

14 As detailed further below, the asserted claims of each Asserted Patent are anticipated by
15 and/or obvious in view of one more of the prior art references being produced concurrently pursuant
16 to 35 U.S.C. § 102 and/or § 103, are directed to ineligible subject matter under 35 U.S.C. § 101, and
17 are otherwise invalid under 35 U.S.C. § 112.

18 **I. PRELIMINARY STATEMENT**

19 These invalidity contentions and eligibility contentions are based on Defendant’s current
20 knowledge, understanding, and belief of the Asserted Patents and prior art, of Plaintiff’s
21 infringement theories (inasmuch as they can be inferred from its Infringement Contentions), and of
22 the facts and other information available as of the date of these invalidity contentions. Defendant’s
23 investigation, discovery, and analysis of information related to this action is ongoing. Additional
24 discovery, elucidation of Plaintiff’s impermissibly vague infringement contentions, Plaintiff’s
25 expert report(s) regarding infringement, and/or orders of the Court may require Defendant to amend
26 or supplement these invalidity contentions and eligibility contentions, and Defendant expressly
27 reserves the right to do so, subject to the Court’s procedures, as the case proceeds. These contentions
28 represent Defendant’s good-faith effort to provide a comprehensive identification of prior art

1 relevant to this case, but Defendant reserves the right to modify or supplement its prior art list and
2 invalidity contentions and eligibility contentions at a later time with, or based upon, pertinent
3 information that may be subsequently discovered.

4 In addition to the prior art that is charted in the attached exhibits, additional background
5 references are discussed herein and/or included in the document production accompanying these
6 Invalidity Contentions. Defendant reserves the right to rely on these background references for any
7 purpose including, for example, to demonstrate the knowledge of a POSITA at the relevant time.

8 To the extent UCT believes anything in these contentions (including the attached claim chart
9 exhibits and accompanying document production) are insufficient, Defendant invites UCT to bring
10 such issues to its attention as soon as reasonably possible.

11 **A. No Waiver**

12 Nothing in these contentions is intended, nor should be construed, as a waiver of any non-
13 infringement position or argument under 35 U.S.C. §§ 101 or 112. To the contrary, as set forth
14 herein, Defendant contends that all Asserted Claims are invalid pursuant to 35 U.S.C. §§ 101 and/or
15 112. Defendant's statements herein (including the accompanying claim charts) reflect Defendant's
16 present understanding of the purported scope of the claims as alleged by Plaintiff in its Infringement
17 Contentions (as best those contentions can be understood in light of their present deficiencies).

18 The patent claims have yet to be construed. As a result, Defendant has based these
19 contentions upon its knowledge and understanding of the potential scope of the Asserted Claims at
20 this time, and, in part, upon the apparent interpretations of the Asserted Claims advanced by Plaintiff
21 in its Infringement Contentions. Defendant may disagree with Plaintiff's interpretation of the
22 meaning of many terms and phrases in the Asserted Claims. Defendant has provided these
23 contentions based in part on its present understanding of Plaintiff's apparent constructions and
24 interpretations of the Asserted Claims. These contentions do not represent Defendant's agreement
25 or view as to the proper interpretation of any claim term contained therein. Any similarity between
26 any apparent claim interpretation in any of Defendant's charts of prior art references and Plaintiff's
27 contentions is not an admission or agreement with Plaintiff about the meaning of any claim term,
28 but rather a reflection of the fact that the subject matter Plaintiff believes is claimed is present in the

1 prior art, or that the claims are otherwise invalid. These contentions are made in the alternative, and
2 should not be interpreted to rely upon, or in any way affect, the non-infringement arguments
3 Defendant may assert in this case. Defendant reserves the right to amend, supplement, or materially
4 modify these contentions as the case proceeds, including to identify additional prior art and/or
5 additional bases for invalidity under 35 U.S.C. §§ 101 and/or 112. Defendant also reserves the right
6 to amend, supplement, or materially modify its contentions based on any infringement and/or
7 additional claim construction positions that Plaintiff may take in this case.

8 Defendant also reserves the right to amend, supplement, or materially modify its contentions
9 in response to any claim construction or interpretation positions that Plaintiff may take or based on
10 any claim construction the Court may further adopt in this case. Defendant also reserves the right
11 to assert that a claim is indefinite, not enabled, or fails to meet the written description requirement
12 of 35 U.S.C. § 112 based on any claim construction or interpretation position Plaintiff may take in
13 this case or based on any claim construction the Court may further adopt in this case.

14 **B. No Admission**

15 Nothing disclosed herein is an admission or acknowledgement that any product accused of
16 infringement by Plaintiff in its Infringement Contentions (the “Accused Products”), or any of
17 Defendant’s other products or services, infringes any of the Asserted Claims.

18 Defendant further notes that Plaintiff appears to rely upon overly broad interpretations of the
19 Asserted Claims. At the same time, Plaintiff’s Infringement Contentions are in most places too
20 general and vague to discern Plaintiff’s infringement theories and how exactly Plaintiff contends
21 each Accused Product meets or practices each element of the Asserted Claims. As a result,
22 Defendant has been prejudiced in its ability to prepare these invalidity contentions. In addition,
23 Plaintiff’s Infringement Contentions, in many cases, continue to fail to put Defendant on notice of
24 Plaintiff’s interpretation of the Asserted Claims, further prejudicing Defendant’s ability to identify
25 relevant prior art.

26 In its Contentions, Plaintiff identified no specific claim elements as allegedly being present
27 under the doctrine of equivalents. In preparing these invalidity and eligibility contentions, Defendant
28 has relied on Plaintiff’s representation that it has no doctrine of equivalents theories for any specific

1 claim element, and any attempt by Plaintiff to present an untimely doctrine of equivalents argument
2 or allegation would be severely prejudicial to Defendant. To the extent Plaintiff attempts to or is
3 later permitted by the Court to amend its contentions to pursue any currently undisclosed doctrine
4 of equivalents theories for additional claim elements, Defendant expressly reserves the right to
5 supplement or amend these invalidity contentions to account for such amendments.

6 To the extent that any of the prior art references discloses the same functionality or feature
7 of any of the Accused Products, Defendant reserves the right to argue that said feature or
8 functionality does not practice any element of any of the Asserted Claims, and to argue, in the
9 alternative, that if said feature or functionality is found to practice any element of any of the Asserted
10 Claims, then the prior art reference demonstrates that the element is not novel, is obvious, and/or is
11 otherwise not patentable.

12 Attached hereto are representative claim charts that identify examples of where the elements
13 of the Asserted Claims may be found in the prior art and further identifying why those claims are
14 not novel or non-obvious. Defendant's claim charts cite particular teachings and disclosures of the
15 prior art as applied to features of the Asserted Claims. Providing citations to portions of the prior
16 art references should not be construed to mean that other portions of the prior art references are not
17 also relevant to the validity of the claims. Other passages of the identified prior art may additionally
18 disclose, either expressly or inherently, information relevant to the validity of one or more elements
19 of the Asserted Claims. And, persons having ordinary skill in the art generally may view an item
20 of prior art in the context of other publications, literature, products, and understanding. As such,
21 Defendant reserves the right to rely on uncited portions of the prior art references and on other
22 publications and expert testimony to establish the state of the art and to aid in understanding and
23 interpreting the cited portions, as providing context thereto, showing reasons to combine references
24 and as additional evidence that the prior art discloses a claim limitation. Defendant further reserves
25 the right to rely on uncited portions of the prior art references, other publications, and testimony to
26 establish bases for combinations of certain cited references that render the asserted claims obvious.
27 Defendant also reserves the right to rely on uncited portions of the prior art references that describe
28 substantially the same functionality or features that are described in cited portions. Further, for any

1 combination, Defendant reserves the right to rely on information generally known to those skilled
2 in the art and/or common sense.

3 Where Defendant cites a particular drawing or figure in the accompanying charts, the citation
4 encompasses the description of the drawing or figure, as well as any text associated with the drawing
5 or figure (even if the associated text is not itself expressly cited). Similarly, where Defendant cites
6 particular text concerning a drawing or figure in the accompanying charts, the citation encompasses
7 that drawing or figure (even if the associated drawing or figure is not expressly cited).

8 The references cited in the attached claim charts may disclose the limitations of the Asserted
9 Claims expressly and/or inherently. Defendant may rely on inherency to demonstrate the invalidity
10 of the Asserted Claims. Moreover, certain prior art references and solutions may inherently
11 anticipate certain features of the asserted claims as construed by Plaintiff. Defendant may rely on
12 cited or uncited portions of the prior art, other documents, and expert testimony to establish the
13 inherency of certain features of the prior art to invalidate the Asserted Claims. Defendant also may
14 rely on any reference identified in these invalidity contentions or any other reference to prove that
15 the references are enabling, to provide a reason to combine the references, as an indication of the
16 state of the art, or to explain the meaning of a term used in any reference.

17 The suggested obviousness combinations may be presented in conjunction with or in the
18 alternative to Defendant's contentions regarding anticipation. These obviousness combinations
19 should not be construed to suggest that any reference included in any combination is not anticipatory
20 in its own right. Further, to the extent that Plaintiff contends that any of the references identified
21 does not constitute prior art under 35 U.S.C. § 102, Defendant reserves the right to rely upon other
22 prior art references in the same patent family with substantially identical disclosures as evidence of
23 invalidity based on the same theories as those disclosed below.

24 Throughout the charts, Defendant provides exemplary citations indicating where the cited
25 references disclose subject matter recited in the preambles of the claims, without regard to whether
26 the preambles are limitations of the claims. Defendant does not take any position at this time
27 regarding whether or not the preambles of the Asserted Claims are limitations, and will address this
28 topic, if necessary, during the scheduled claim construction process.

1 With regard to the prior art that Defendant identifies as rendering the Asserted Claims
2 obvious, non-limiting examples of the reasons why the prior art renders the Asserted Claims
3 obvious, including exemplary identification of combinations of prior art showing obviousness, are
4 provided below. Generally, for all prior art combinations addressed herein, a reason or motivation
5 to combine the prior art includes that each prior art reference is relevant to data communications
6 and/or power delivery between devices, and one of ordinary skill in the art tasked with implementing
7 such a system would have been motivated to investigate the various existing systems, patents, and
8 other publications, including those identified herein, to address his or her particular needs. The
9 combinations and modifications of the prior art to invalidate the Asserted Claims would have arisen
10 from ordinary innovation, ordinary skill, or common sense and/or would have been obvious to try
11 or otherwise predictable in the field of data communications and/or power distribution between
12 devices.

13 A person having ordinary skill in the art would have had a reason to combine the prior art
14 based on the nature of the problem to be solved, the teachings of the prior art, and the knowledge of
15 persons having ordinary skill in the art. For example, each of the prior art references cited for a
16 given Asserted Patent is relevant to the subject of the Asserted Patent, including, for example, data
17 communications methods and systems and/or power delivery systems and methods, including
18 addressing problems such as communications with multilevel functionality, synchronizing and
19 ordering data communications, negotiating power delivery, supplying power, and arbitrating control
20 of a control bus. In addressing these problems, one of ordinary skill in the art would have been
21 motivated to combine the teachings of research in the field.

22 Additionally, some prior art references cite or discuss other prior art references, illustrating
23 the close technical relationship among the prior art. To the extent that any prior art reference refers
24 to or discusses another prior art reference, either expressly or inherently, it would have been obvious
25 to combine those references for at least that reason.

26 As shown in the accompanying claim charts, numerous books and research papers show that
27 methods were being used to streamline packetized data transmission and power distribution across
28 device-to-device connections. Design incentives and other market forces would have prompted

1 combinations and modifications of the prior art. Design needs and market pressures provide ample
2 reason to combine prior art elements in the manner combined. *See KSR Int'l Co. v. Teleflex Inc.*,
3 550 U.S. 398, 401 (2007). Defendant reserves the right to supplement these disclosures if such
4 evidence of design needs and/or market pressures become apparent through discovery in this case.

5 Moreover, the Asserted Claims are also obvious because they merely arrange old elements,
6 with each performing the same function that had been known, to perform and yield no more than
7 what one having ordinary skill in the art would expect from such an arrangement.

8 Because there were a finite number of predictable solutions in the art of packetized data
9 transmission and power distribution across device-to-device connections with regard to any claimed
10 feature, it would have been obvious to a person of ordinary skill in the art to pursue the known
11 options. A person skilled in this art would have been familiar with all the claim elements that the
12 patentees used to distinguish the prior art during prosecution. The identified prior art references
13 merely use those familiar elements for their primary or well-known purposes and in a manner well
14 within the ordinary level of skill in the art. Accordingly, common sense and the knowledge of one
15 having ordinary skill in the art render the Asserted Claims invalid.

16 **C. Reservation of Rights**

17 Prior art not currently included in this disclosure may become relevant. Defendant is
18 currently unaware of the extent, if any, to which Plaintiff will contend that limitations of the
19 Asserted Claims are not disclosed in the prior art identified by Defendant or contend that prior art
20 identified by Defendant does not qualify as prior art. Defendant reserves the right to identify other
21 references that would have made the addition of the allegedly missing limitation to the disclosed
22 device or method obvious or show that the allegedly missing limitation would have been known or
23 readily apparent to one of ordinary skill in the art at the time of the invention in light of the disclosure
24 of the prior art at issue or other prior art. Defendant further reserves the right to rely on any of the
25 references produced concurrently with these contentions in order to demonstrate the state of art at
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1 the alleged times of invention and as evidence of the knowledge of one of ordinary skill in the art¹
2 in support of any motivations to modify or combine the charted prior art references with other
3 references or knowledge.

4 To the extent that Defendant charted a published patent application that later issued as a
5 patent that includes substantially the same disclosure, Defendant contends that the issued patent
6 discloses the claims for at least the same reasons explained in connection with the published
7 application and Defendant reserves its rights to rely on the issued patent to establish invalidity.
8 Similarly, to the extent that Defendant charted an issued patent the application for which was
9 previously published (and which contains substantially the same disclosure), Defendant contends
10 that the published application discloses the claims for at least the same reasons explained in
11 connection with the issued patent and Defendant reserves the right to rely on the published
12 application to establish invalidity (including to establish an earlier prior art date).

13 Consistent with Scheduling Order (Dkt. 93), and in view of the following, Defendant
14 reserves the right to supplement or otherwise amend these Invalidity Contentions. This is
15 particularly true for all claims for which Plaintiff has not provided adequate infringement
16 contentions.

17 Plaintiff may also be aware of additional prior art that is not known to Defendant. To the
18 extent Plaintiff produces additional prior art responsive to Defendant's discovery requests after these
19 contentions are served, Defendant may supplement its Invalidity Contentions with prior art
20 contained in such production once it has had a fair opportunity to review, analyze, and chart such
21 prior art. Defendant reserves the right to amend its Invalidity Contentions with any additional
22 potential prior art known by Plaintiff but not yet disclosed to Defendant.

23 Defendant provides these Invalidity Contentions only for the claims that are asserted by
24 Plaintiff, but reserves the right to seek invalidation of all claims in each of the Asserted Patents.

27 ¹ For purposes of these Invalidity Contentions, the term "general knowledge" includes the common
28 knowledge and common sense of a POSITA as well as the general knowledge of POSITAs in the
field.

1 In addition to the prior art that is set forth in the charts, additional prior art references are
2 being produced concurrently with these contentions. This additional art may be relevant to the
3 validity of the Asserted Claims depending on the positions taken by Plaintiff, and in any event may
4 be referenced to show the state and evolution of technology in these fields. Accordingly, for the
5 foregoing reasons, Defendant reserves the right to supplement these Invalidity Contentions with
6 specific claim charts and obviousness combinations with the additional references based on the
7 allegations and contentions asserted by Plaintiff as these allegations and corresponding
8 constructions of the claims become clear.

9 **D. Ongoing Investigation**

10 Defendant's investigation is ongoing, and Defendant expressly reserves the right to amend
11 its disclosures and document production to account for evidence uncovered as its investigation
12 continues. Such amendments include identifying and relying on additional references that may
13 result from Defendant's further search and analysis. Defendant reserves the right to supplement
14 these contentions in light of any additional prior art of which Plaintiff is aware and has not disclosed
15 to Defendant in discovery, or that might be subsequently disclosed by Plaintiff in response to
16 Defendant's discovery requests. An example of such prior art may include products sold and offered
17 for sale by Silicon Image and/or Lattice Semiconductor. Such products may have been offered for
18 sale or publicly shown in a manner that renders them prior art under 35 U.S.C. §§ 102 and 103.
19 Defendant reserves the right to supplement these contentions to rely on those and other products
20 from Plaintiff. Defendant's investigation into prior art systems and products is ongoing, and
21 Defendant reserves the right to amend these contentions to reflect the identification of and
22 information about such systems and products learned through discovery.

23 Defendant anticipates issuing subpoenas to third parties believed to have knowledge,
24 documentation and/or corroborating evidence concerning some of the prior art listed herein and/or
25 additional prior art. These third parties include, but are not limited to, the authors, employers of
26 inventors, assignees, or former or current employees of assignees or previous assignees, of the
27 references identified in these Invalidity Contentions. Defendant reserves the right to supplement
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1 these contentions in light of any newly discovered information produced by these or other
2 companies from which Defendant may seek discovery.

3 **E. Incorporation by Reference**

4 Defendant hereby incorporates by reference all arguments made in all IPR petitions
5 challenging any Asserted Claim, including any decision instituting IPR that is filed after the date of
6 these contentions, including the following IPR proceedings:

- 7 • IPR2024-01482;
- 8 • IPR2024-01480;
- 9 • IPR2024-01479;
- 10 • IPR2024-01478;
- 11 • IPR2024-01481;
- 12 • IPR2024-01429;
- 13 • IPR2024-01428.

14 Defendant further incorporates by reference the file history of each Asserted Patent and the
15 prior art cited therein.

16 **II. PRIORITY DATE OF THE ASSERTED PATENT CLAIMS**

17 Plaintiff asserted the following priority dates for the Asserted Claims in its Infringement
18 Contentions:

Asserted Patent	"Priority Date"
'905 Patent	"at least a priority date of November 22, 2000"
'307 Patent	"at least a priority date of June 12, 2003"
'798 Patent	"at least a priority date of November 22, 2000"
'265 Patent	"at least a priority date of March 31, 2011"
'712 Patent	"at least a priority date of December 11, 2008"
'520 Patent	"at least a priority date of January 4, 2008"
'231 Patent	"at least a priority date of January 4, 2008"
'103 Patent	"at least a priority date of April 14, 2014"

1 It is Plaintiff's burden to show entitlement to its asserted priority dates, and Defendant asserts
2 that Plaintiff has failed to meet that burden. Plaintiff has further failed in its obligations under PLR
3 3-1(f) to disclose "the priority date to which each asserted claim allegedly is entitled," at least
4 because it discloses ambiguous "priority dates" qualified with the phrase "at least as early as." See
5 UCT's Infringement Contentions at 7-8, served October 21, 2024. To the extent Plaintiff attempts
6 to rely on a different date from the specifically enumerated "Priority Dates" listed above (i.e., under
7 the "at least" language), Defendant reserves the right to supplement these contentions. Moreover,
8 because discovery has not yet been completed, Defendant has relied on Plaintiff's assertions for the
9 purposes of identifying relevant prior art in these Invalidity Contentions, but Defendant does not
10 concede that those priority dates are accurate. Defendant reserves the right to supplement these
11 Invalidity Contentions should discovery reveal that Plaintiff is not entitled to the asserted priority
12 date. In addition, Defendant also reserves the right to supplement these contentions should Plaintiff
13 subsequently attempt to amend its infringement contentions in any way, or to otherwise modify its
14 infringement allegations or seek to establish an earlier date of invention.

15 **III. THE ASSERTED CLAIMS OF THE '905 PATENT ARE INVALID**

16 **A. Identification of Prior Art**

17 Defendant contends that the prior art references charted in Exhibits A-1 through A-8,
18 discussed in any incorporated IPR petition, and/or described below anticipate and/or render obvious,
19 alone or in combination, one or more of the Asserted Claims of the '905 Patent.

20 **1. The '905 Patent Claims Are Anticipated by the Prior Art**

21 Some or all of the Asserted Claims of the '905 Patent are invalid as anticipated under 35
22 U.S.C. § 102 in view of each of the prior art references identified in the claim charts included in
23 Exhibit A-1 through A-8 and identified in each incorporated IPR petition, which identify specific
24 examples of where each limitation of the Asserted Claims is found in the prior art references. As
25 explained above, the cited portions of prior art references identified in the attached claim charts are
26 exemplary in nature and representative of the content and teaching of the prior art references, and
27 should be understood in the context of the reference as a whole and as they would be understood by
28 a person of ordinary skill in the art ("POSITA").

1 In addition to references identified in any incorporated IPR petition, Defendant identifies the
2 following references as anticipating one or more of the Asserted Claims of the '905 Patent under 35
3 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an
4 admission that any reference not listed below does not also anticipate the claims of the '905 Patent.
5 Further, Defendant contends that any prior art reference in the attached charts that is charted for
6 each limitation of any given claim, anticipates that claim, regardless of whether that prior art
7 reference is listed in the following tables.

8 **a) Prior Art Patents and Applications²**

9 Number	Published/Issued Date	Short Name	Exhibit Number
10 UK Patent App. No. GB 2344029	May 24, 2000	Banes	A-1
11 U.S. Patent No. 4,542,380	September 17, 1985	Beckner	A-2
12 U.S. Patent No. 5,557,608	September 17, 1996	Calvignac	A-3
13 U.S. Patent No. 5,845,085	December 1, 1998	Gulick	A-4
14 U.S. Patent No. 5,574,934	November 12, 1996	Mirashrafi	A-5
15 U.S. Patent No. 5,974,464	October 26, 1999	Shin '464	A-6

16 Defendant additionally identifies and relies on any system, product, or public knowledge or
17 use that embodies or otherwise incorporates any of the prior art patents and publications listed
18 above. Defendant reserves the right to identify and rely on systems that represent different versions
19 or are otherwise related variations of the identified systems. Defendant also incorporates by
20 reference any and all other prior art systems identified in any other case brought by Plaintiff and/or
21 involving the Asserted Patents.

22 To the extent any item of prior art cited above is deemed not to disclose, explicitly or
23 inherently, any limitation of an asserted claim of the '905 Patent, Defendant contends that any
24 difference between that prior art and the corresponding patent claim would have been either inherent
25 in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically
26 denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

27 ² Where the accompanying charts cite a particular drawing or figure, the citation encompasses the
28 description of the drawing or figure, as well as any text associated with the drawing or figure (even
if the associated text is not by itself expressly cited). Similarly, where the accompanying charts cite
particular text concerning a drawing or figure, the citation also encompasses that drawing or figure
(even if the associated drawing or figure is not expressly cited).

1 **b) Prior Art Systems**

2 On information and belief, the systems identified below were in public use, on sale, or
3 otherwise available to the public before the priority date of the '905 Patent. Defendant's further
4 investigation and/or subsequent discovery from Plaintiff or third parties with knowledge regarding
5 prior art systems may reveal additional relevant prior art systems and/or further information
6 regarding the systems identified below, or other relevant prior art systems. Defendant reserves the
7 right to supplement these Invalidity Contentions, based on subsequent investigation and discovery,
8 including from third parties.

9

System	Available At Least As Of	Short Name	Exhibit Number
IBM Personal Systems/2 implementing High-Level Data Link Control (HDLC) protocol	1997	PS/2	A-7
Apple Power Mac G4 (Gigabit Ethernet) implementing IEEE 802.3-1998	2000	802.3-1998	A-8

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13 Defendant additionally identifies and relies on any system, product, or public knowledge or
14 use that embodies or otherwise incorporates any of the prior art patents and publications listed
15 above. Defendant reserves the right to identify and rely on systems that represent different versions
16 or are otherwise related variations of the identified systems. Defendant also incorporates by
17 reference any and all other prior art systems identified in any other case brought by Plaintiff and/or
18 involving the Asserted Patents.

19 To the extent any item of prior art cited above is deemed not to disclose, explicitly or
20 inherently, any limitation of an asserted claim of the '905 Patent, Defendant contends that any
21 difference between that prior art and the corresponding patent claim would have been either inherent
22 in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically
23 denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

24 **2. The '905 Patent Claims Are Obvious Over the Prior Art**

25 To the extent Plaintiff argues that any limitation of the asserted claims of the '905 Patent are
26 not explicitly disclosed by an item of prior art identified above, in Exhibits A-1 through A-8, or
27 discussed in any incorporated IPR petition, any purported differences are such that the claimed
28 subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged

1 invention, in view of the state of the art and knowledge of those skilled in the art. The item of prior
2 art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

3 It also would have been obvious to combine any of the prior art in Exhibits A-1 through A-
4 8 with each other, at least because these prior art references relate to data transmission methods and
5 devices utilizing certain transmission schemes in the same field of endeavor and to solve similar
6 problems. For example, the transmission schemes disclosed by the prior art include packet ordering,
7 such as pausing, interrupting, prioritizing, and/or resuming paused transmissions of packetized data
8 designed to solve a number of problems that were known in the art. *See, e.g.*, '905 Patent, 2:59-66
9 ("Existing memory devices that are designed to support access patterns with a high temporal and
10 spatial relationship may not be appropriate for uses having access patterns with a lower spatial
11 relationship."); 3:15-19 ("[E]xisting memory devices are not particularly suitable for many uses
12 because the memory devices typically allow access by only one accessing device at a time and
13 because the memory devices typically operate at different clock rates than the accessing devices.");
14 and 3:34-36 ("Existing communications protocols, such as Fibre Channel, may have an
15 unacceptable overhead for communicating with memory devices."). Therefore, these references
16 provide interrelated teachings and one of ordinary skill would have looked to the concepts in any of
17 these references when attempting to solve the problems purportedly solved by the '905 Patent,
18 among other asserted patents.

19 Turning to the prior art, U.S. Patent No. 5,574,934 to Mirashrafi et. al ("Mirashrafi '934"),
20 issued on November 12, 1996, discloses a system for priority-based transmission of signals.
21 Mirashrafi '934 at Abstract. For instance, transmission of lower priority signals may be interrupted
22 while signals of higher priority are transmitted before resumption of the lower priority signal
23 transmission. *Id.* at 1:46-58. Signals may be transmitted in data packets over a communication link
24 such as an ISDN channel. *Id.* at 71:11-23.

25 U.S. Patent No. 5,845,085 to Dale E. Gulick ("Gulick '085"), issued on December 1, 1998,
26 discloses a data-link controller for receiving and transmitting frames of serialized data over a data-
27 link. Gulick '085 at Abstract. Gulick '085 specifically describes that data may often be transmitted
28 or received in "packets" or "frames" of information. *Id.* at 1:17-25. Gulick '085 further discusses

1 the use of flag signals to mark states or conditions for the link controller transmitter or receiver. *Id.*
2 at 2:18-44.

3 U.S. Patent No. 4,542,380 to Beckner, *et. al* (“Beckner ’380”), issued September 17, 1985,
4 discloses a method and apparatus for graceful preemption on a digital communications link. Beckner
5 ’380 at Abstract. A link controller is configured on a respective transmitting or receiving end of a
6 communications link to interrupt and resume communications according to signals such as a
7 “preemption signal” or “end preemption signal”. *Id.* at 2:10-42.

8 U.S. Patent No. 5,974,464 to Shin, *et. al* (“Shin ’464”), issued October 26, 1999, discloses
9 a high speed digital interface for transmitting information (*e.g.*, video) over various transmission
10 media. Shin ’464 at Abstract. In particular, Shin ’464 discloses an encoder and deserializer
11 configured to distinguish encoded characters based on a number of logical transitions. *Id.* at 3:55-
12 4:5. Shin ’464 further discloses encoding and transmission of in-band and out-of-band characters
13 such as control characters which can be distinguished from characters within the transmitted data
14 stream. *Id.* at 9:49-10:8.

15 UK Patent Application No. GB 2,344,029 to David Banes (“Banes ’029”), published on May
16 24, 2000, discloses a data communication network technique involving interruption of lower priority
17 data packets such that higher priority packets can be transmitted. Banes ’029 at Abstract. Banes ’029
18 specifically discloses the use of priority flags, interrupt codes, and resumption codes in order to
19 facilitate preemption and resumption of lower priority transmissions until higher priority packets
20 are sent. *Id.* at 11:18-12:18.

21 U.S. Patent No. 5,557,608 to Calvignac *et. al* (“Calvignac ’608”), issued September 17,
22 1996, discloses a method and apparatus for preempting low-priority traffic in favor of high-priority
23 traffic transmission. Calvignac ’608 at 2:25-38. Calvignac ’608 discloses transmission of pieces of
24 data in packets with headers used by each node of a packet switching network to send packets toward
25 their destination. *Id.* at 3:13-27. Calvignac ’608 further discloses the use of byte aligned flags to
26 signify starting and ending preemption. *Id.* at 4:44-49.

27 The IBM Personal System/2 personal computer system, implementing the OS/2 2.0
28 operating system, was available on the market at least as of 1992. IBM’s “Writing OS/2 Warp

1 Device Drivers in C”, third edition, discloses that IBM PS/2 systems implemented HDLC protocol,
2 which is further described in European Patent Publ. No. 0582537A2 (“Cidon ‘537”), and discloses
3 data packet transmission between nodes of a packet switching network and the use of byte aligned
4 flags to signify starting and ending preemption. Cidon ‘537 at 2:9-18, 3:5-6, 4:49-58.

5 The Apple Power Mac G4 (Gigabit Ethernet) personal computer system from was available
6 on the market at least as of August, 2000. The Power Mac G4 implements 10/100/1000BASE-T
7 Ethernet, which is governed by the IEEE 802.3 standard. The IEEE 802.3 standard was available at
8 least as of June 25, 1998. The Power Mac G4 therefore implements the IEEE 802.3 standard’s
9 physical layer and data link layer’s media access control (MAC) of wired Ethernet, including a local
10 area network (LAN) access method using carrier-sense multiple access with collision detection
11 (CSMA/CD). See Sec. 4.

12 Accordingly, because each of the identified references are directed to similar devices in the
13 similar field of endeavor, a person of ordinary skill in the art would be motivated to combine the
14 teachings of two or more references together because the references disclose similar systems that
15 solve the same problems in similar ways. Thus, it would have been obvious to one of ordinary skill
16 in the art to combine any of the foregoing references and one of ordinary skill would have expected
17 such a combination to be successful.

18 To the extent that it is determined that any of the above references do not disclose a particular
19 claim element, a person skilled in the art would have been motivated to combine any of the above
20 references or systems (as documented in the claim charts attached as Exhibits A-1 through A-8). In
21 particular, the combinations identified herein would merely have been (a) a combination of prior art
22 elements according to known methods to yield predictable results; (b) a simple substitution of one
23 known element for another to obtain predictable results; (c) a use of known technique to improve
24 similar devices or methods in the same way; (d) application of a known technique to a known device
25 or method ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known
26 work in one field of endeavor prompting variations of it for use in either the same field or a different
27 one based on design incentives or other market forces since the variations are predictable to one of
28 ordinary skill in the art. Moreover, a person of ordinary skill in the art had a reason to combine

1 these references because—at a minimum—they all pertain to data transmission methods and devices
2 utilizing certain transmission schemes.

3 As discussed above, the motivation to combine the teachings of the patents and other prior
4 art referenced above is found in the art as specified in the charts and in: (1) the nature of the problem
5 being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of
6 persons of ordinary skill in the art; and (4) the fact that the prior art is generally directed towards
7 data transmission methods and devices utilizing certain transmission schemes, and (5) the
8 predictable results obtained in combining the different elements of the prior art. The Supreme Court
9 has held that a showing of a motivation to combine within the references themselves is not required
10 to prove obviousness. *See KSR*, 550 U.S. at 401 (“Any need or problem known in the field of
11 endeavor at the time of invention may provide the motivation to combine.”).

12 For example, to the extent that it is determined that any of the above references do not
13 disclose the general concept of preempting and resuming data transmission as claimed, it would
14 further have been obvious to modify the teachings of that reference to include this feature in view
15 of the knowledge of a POSITA and the teachings of these features in at least the following references
16 and systems: *See, e.g.*, Mirashrafi ’934, Beckner ’380, Calvignac ’608, Banes ’029, PS/2, and 802.3-
17 1998. As demonstrated in the attached claim charts for these references, each discloses preemption
18 of data transmission on the basis of priority, which was well known in the art at the time of the ’905
19 Patent filing. Therefore, a POSITA would be motivated to make such a modification and/or
20 combination.

21 As an additional example, to the extent that it is determined that any of the above references
22 do not disclose transmitting or receiving “packets” as claimed, it would further have been obvious
23 to modify the teachings of that reference to include this feature in view of the knowledge of a
24 POSITA and the teachings of these features in at least the following references and systems: *See,*
25 *e.g.*, Mirashrafi ’934, Gulick ’085, Calvignac ’608, Banes ’029, PS/2, and 802.3-1998. As
26 demonstrated in the attached claim charts for these references, each discloses transmission of data
27 in various container formats including packets. For instance, Gulick ’085 describes common data-
28

1 link transmission in “packets” or “frames” of information. Gulick '085 at 1:17-25. Therefore, a
2 POSITA would be motivated to make such a modification and/or combination.

3 As an additional example, to the extent that it is determined that any of the above references
4 do not disclose transmitting or receiving indicators such as a “preempt indicator” or “continue
5 indicator” as claimed, it would further have been obvious to modify the teachings of that reference
6 to include this feature in view of the knowledge of a POSITA and the teachings of these features in
7 at least the following references and systems: *See, e.g.*, Beckner '380, Banes '029, Calvignac '608,
8 Gulick '085, PS/2, and 802.3-1998. As demonstrated in the attached claim charts for these
9 references, each discloses transmission of symbols or flags signifying preemption or resumption of
10 data transmission. For instance, Beckner '380 describes a link controller for preemption of data
11 using characters such as “PREEMP”, represented in binary as “11111110.” Beckner '380 at 4:18-
12 52. Similarly, Banes '029 discusses a priority detector and interrupt device to facilitate packet
13 interruption and resumption using an “interrupt code” and “resume code,” respectively. Banes '029
14 at 11:18-12:18. Therefore, a POSITA would be motivated to make such a modification and/or
15 combination.

16 As an additional example, to the extent that it is determined that any of the above references
17 do not disclose “in-band symbols” and “out-of-band symbols” as claimed, it would further have
18 been obvious to modify the teachings of that reference to include this feature in view of the
19 knowledge of a POSITA and the teachings of these features in at least the following references and
20 systems: *See, e.g.*, Shin '464, Beckner '380, Calvignac '608, Banes '029, Gulick '085, PS/2, and
21 802.3-1998. As demonstrated in the attached claim charts for these references, each discloses
22 symbols or characters including those that are in-band and out-of-band. For instance, Shin '464
23 describes “selected out-of-band characters easily distinguishable from in-band characters.” Shin
24 '464 at 14:37-62. Similarly, Beckner '380 describes a link controller for graceful preemption of data
25 using characters such as “PREEMP,” represented in binary as “11111110.” Beckner '380 at 4:18-
26 52. As discussed in the '905 Patent, in-band and out-of-band symbols may be distinguished by the
27 number of bit transitions occurring in their binary representation. '905 Patent at 24:33-46. Therefore,
28 a POSITA would be motivated to make such a modification and/or combination.

1 As an additional example, to the extent that it is determined that any of the above references
2 do not disclose “primitives” as claimed, it would further have been obvious to modify the teachings
3 of that reference to include this feature in view of the knowledge of a POSITA and the teachings of
4 these features in at least the following references: *See, e.g.*, Mirashrafi ’934, Shin ’464, Calvignac
5 ’608, Banes, PS/2, and 802.3-1998. As demonstrated in the attached claim charts for these
6 references, each discloses symbols or characters including in-band and out-of-band. For instance,
7 Mirashrafi ’934 describes a “set of primitives” such as “comm primitives” implemented for API
8 calls. Mirashrafi ’934 at 28:61-65. In addition, transmitting primitives for the purpose of
9 communication and synchronization between networked components was well known in the art at
10 the time of the ’905 filing. Therefore, a POSITA would be motivated to make such a modification
11 and/or combination.

12 As an additional example, to the extent that it is determined that any of the above references
13 do not disclose a “header that is transmitted only once” as claimed, it would further have been
14 obvious to modify the teachings of that reference to include this feature in view of the knowledge
15 of a POSITA and the teachings of these features in at least the following references: *See, e.g.*,
16 Calvignac ’608, Mirashrafi ’934, Banes ’029, PS/2, and 802.3-1998. As demonstrated in the
17 attached claim charts for these references, each at least inherently discloses a header that is initially
18 transmitted and is not repeated upon continuation of the packet transmission. For instance,
19 Calvignac ’608 at Fig. 5 depicts a first packet of data with a packet header, a second packet with a
20 packet header, and the continuation of the first packet data without repeating the header. As
21 discussed in the ’905 specification, merging segmented packets of the same transaction would have
22 been appreciated by a POSITA as a way to efficiently transmit packet switched data. ’905 Patent at
23 13:18-39. Additionally, Mirashrafi ’934 noted that it would be desirable for a computing system to
24 avoid “being inundated with subsequent signal packets it may not be able to handle.” *See* Mirashrafi
25 ’934, 78:9-15. To address this issue, Calvignac ’608 provides a first packet of data with a packet
26 header, a second packet with a packet header, and the continuation of the first packet data without
27 repeating the header, to achieve the technological improvements contemplated by the existing prior
28

1 art and the '905 Patent. Therefore, a POSITA would be motivated to make such a modification
2 and/or combination.

3 In addition, one of ordinary skill in the art would have been motivated to combine the prior
4 art references. One of skill in the art would have would have been motivated to combine these
5 references: (1) by their education, knowledge, and experience; (2) by the state of the prior art as a
6 whole; (3) by the nature of the problem to be solved; (4) by common sense and ordinary ingenuity;
7 and (5) by a desire to create a device, system, and method of controlling communication of computer
8 data. Moreover, one of ordinary skill in the art would have been well-equipped with sufficient
9 education, knowledge, and training to make the specific combinations with a reasonable expectation
10 of success given the simplicity of the electrical components to one of ordinary skill in the art, the
11 predictability of the arts, and the minimal level of experimentation needed to combine the various
12 teachings.

13 One of skill in the art, seeking to solve these problems, would have looked to analogous art
14 to identify ways to solve the problem. Indeed, the solution identified by the patentee had already
15 been identified by others in the field, and one of ordinary skill in the art would have been motivated
16 to combine such analogous teachings in the same manner proposed by the patentee. Additionally,
17 one of skill in the art would have had a reasonable expectation of success because the references
18 contained analogous teachings to those proposed by the patentee, the references describe relatively
19 simple electrical technologies in predictable fields, and the modifications and combinations would
20 not require undue experimentation. As such, one of skill would have been motivated to combine the
21 references.

22 Thus, in addition to the combinations discussed above, exemplary combinations which
23 render obvious some or all of the Asserted Claims of the '905 Patent are listed in **Appendix A**, Sec.
24 I.

25 **B. Invalidity of the '905 Patent Based on 35 U.S.C. § 112, ¶ 1**

26 Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of
27 the '905 Patent, to the extent such positions can be understood from Plaintiff's Infringement
28 Contentions, Defendant asserts that the Asserted Claims of the '905 Patent are invalid for failure to

1 provide a written description that enables the full scope of the Asserted Claims based on at least the
2 following claim terms, phrases, or limitations:

- 3 • **“the out-of-band symbols are not transition optimized” (claim 23):** This term is not
4 explicitly defined in the specification, and “optimization” of bit transitions within a symbol
5 is described inconsistently. For example, the ’905 Patent specification describes that
6 “transition control” may be “optimized to either maximize or minimize the number of
7 transitions in symbols that are to be transmitted.” ’905 Patent at 23:50-53. The number of
8 bit transitions per symbol described for “optimization” is conflicting, describing in-band
9 symbols as having “at least four transitions” (id., 24:41-46), but also that the transitions may
10 be “minimized” in order to “reduc[e] electromagnetic interference.” *Id.*, 23:59-67. One of
11 skill in the art would not understand how to implement out-of-band symbols that are not
12 transition optimized without undue experimentation based on the descriptions in the
13 specification. Thus, this term is invalid for lack of written description support and lack of
14 enablement.
- 15 • **“a preemption component that signals the transmission component to stop transmitting
16 the first packet, transmits a preempt indicator indicating that a second packet is to be
17 transmitted, transmits the second packet, and signals the transmission component to
18 continue transmitting the first packet” (claim 21):** The specification of the ’905 Patent
19 does not identify a preemption component, let alone a preemption component that signals a
20 transmission component to continue transmitting a first packet. Thus, the specification lacks
21 written description support for this limitation.

22 Based on Defendant’s present understanding of Plaintiff’s Infringement Contentions and
23 apparent interpretation of the scope of the Asserted Claims, at least one or more of these claim terms,
24 phrases, and limitations lack written description support, as they are not identified, described, or
25 explained in the specification of the Asserted Patent, and do not enable a person of ordinary skill in
26 the art to practice the claimed invention without undue experimentation or to distinguish all
27 operative embodiments from all nonoperative embodiments without undue experimentation.

1 In addition to Defendant's contentions regarding the specifically listed terms above,
2 Defendant contends that UCT has failed to identify specific support for each limitation of each
3 Asserted Patent in its Infringement Contentions, and instead points to the same or similar
4 information as satisfying each claim limitation. Defendant therefore contends that there is no written
5 description support for the identified, described, or explained in the specification of the Asserted
6 Patents to enable a person of ordinary skill in the art to practice the claimed invention under the
7 wide claim scope UCT appears to be contending applies.

8 The written description and enablement issues identified above apply to all claims that
9 include the identified limitations, either explicitly or through claim dependency, and are not limited
10 to the exemplary claims listed above.

11 **C. Invalidity of the '905 Patent Based on 35 U.S.C. § 112, ¶ 2**

12 Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of
13 the '905 Patent, to the extent such positions can be understood from Plaintiff's Infringement
14 Contentions, Defendant asserts that the Asserted Claims of the '905 Patent are invalid for reciting
15 at least the following claim terms, phrases, or limitations:

- 16 • **"transition optimized" (claim 23):** This term is not explicitly defined in the specification,
17 and "optimization" of bit transitions within a symbol is described inconsistently. For
18 example, the '905 Patent specification describes that "transition control" may be "optimized
19 to either maximize or minimize the number of transitions in symbols that are to be
20 transmitted." '905 Patent at 23:50-53. The number of bit transitions per symbol described
21 for "optimization" is conflicting, describing in-band symbols as having "at least four
22 transitions" (*id.*, 24:41-46), but also that the transitions may be "minimized" in order to
23 "reduc[e] electromagnetic interference." *Id.*, 23:59-67.

24 These claim terms, phrases, limitations, and all dependent claims thereof, as apparently
25 construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112 at least because they
26 fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

27 Based on Defendant's present understanding of Plaintiff's Infringement Contentions, at least
28 one or more of these claim terms, phrases, and limitations are indefinite because they are

1 inconsistent with or broader than the alleged invention disclosed in the specification and during
2 prosecution, and given Plaintiff's apparent constructions of the claims, a person of ordinary skill in
3 the art at the time of the invention would not understand what is claimed with reasonable certainty,
4 even when the claims are read in light of the specification and prosecution history.

5 Additionally, at least claim 21 (and its dependent claims) of the '905 Patent recites functions
6 without sufficient structure for performing the function, thus invoking 35 U.S.C. § 112, ¶ 6. Because
7 the specification of the '905 Patent also does not recite structure for performing the function, the
8 following terms are invalid as indefinite under 35 U.S.C. §§ 112, ¶ 2:

- 9 • "a transmission component that transmits a first packet" (claim 21)
- 10 • "a preemption component that signals the transmission component to stop transmitting the
11 first packet, transmits a preempt indicator indicating that a second packet is to be transmitted,
12 transmits the second packet, and signals the transmission component to continue transmitting
13 the first packet" (claim 21)

14 The indefiniteness issues identified above apply to all claims that include the identified
15 limitations, either explicitly or through claim dependency, and are not limited to the exemplary
16 claims listed above.

17 **IV. THE ASSERTED CLAIMS OF THE '307 PATENT ARE INVALID**

18 **A. Identification of Prior Art**

19 Defendant contends that the prior art references charted in Exhibits B-1 through B-11,
20 discussed in any incorporated IPR petition, and/or described below anticipate and/or render obvious,
21 alone or in combination, one or more of the Asserted Claims of the '307 Patent.

22 **1. The '307 Patent Claims Are Anticipated by the Prior Art**

23 Some or all of the Asserted Claims of the '307 Patent are invalid as anticipated under 35
24 U.S.C. § 102 in view of each of the prior art references identified in the claim charts included in
25 Exhibit B-1 through B-11, or identified in any incorporated IPR petition, which identify specific
26 examples of where each limitation of the Asserted Claims is found in the prior art references. As
27 explained above, the cited portions of prior art references identified in the attached claim charts are
28 exemplary in nature and representative of the content and teaching of the prior art references, and

1 should be understood in the context of the reference as a whole and as they would be understood by
2 a person of ordinary skill in the art.

3 In addition to references identified in any incorporated IPR petition, Defendant identifies the
4 following references as anticipating one or more of the Asserted Claims of the '307 Patent under 35
5 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an
6 admission that any reference not listed below does not also anticipate the claims of the '307 Patent.
7 Further, Defendant contends that any prior art reference in the attached charts that is charted for
8 each limitation of any given claim, anticipates that claim, regardless of whether that prior art
9 reference is listed in the following tables.

10 **a) Prior Art Patents and Applications³**

Number	Published/Issued Date	Short Name	Exhibit Number
WO1992/09162	May 29, 1992	Hornak	B-1
U.S. Patent Appln. No. 2002/0114348	August 22, 2002	McCrosky	B-2
U.S. Patent No. 5,313,458	May 17, 1994	Suzuki	B-3
U.S. Patent No. 6,584,535	June 24, 2003	Ouellet	B-4
International Pub. No. WO 01/58107	January 24, 2002	Azizoglu	B-5
U.S. Patent No. 4,486,739	December 4, 1984	Franaszek	B-6
European Patent No. EP 0,938,211	August 25, 1999	Blanc	
U.S. Patent Appln. No. 2002/0159450	October 31, 2002	Shin '450	B-7

21 **b) Prior Art Publications**

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
PCI-SIG	PCI Express Base Specification Revision 1.0	April 29, 2002	PCI 1.0	B-8
IEEE	802.3z Specification	March 8, 2002	802.3z	B-9

26 ³ Where the accompanying charts cite a particular drawing or figure, the citation encompasses the
27 description of the drawing or figure, as well as any text associated with the drawing or figure (even
28 if the associated text is not by itself expressly cited). Similarly, where the accompanying charts cite
particular text concerning a drawing or figure, the citation also encompasses that drawing or figure
(even if the associated drawing or figure is not expressly cited).

Mohd Yusairi et al.	<i>Hardware Design and Implementation of IP-over-1394 Protocol Stack and Its Evaluation</i> , ITE Technical Report Vol. 27, No. 18, pp. 51-85	April 22, 2003	Yusairi	See IPR 2024-01429
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Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the '307 Patent, Defendant contends that any difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

c) Prior Art Systems

On information and belief, the systems identified below were in public use, on sale, or otherwise available to the public before the priority date of the '307 Patent. Defendant's further investigation and/or subsequent discovery from Plaintiff or third parties with knowledge regarding prior art systems may reveal additional relevant prior art systems and/or further information regarding the systems identified below, or other relevant prior art systems. Defendant reserves the right to supplement these Invalidity Contentions, based on subsequent investigation and discovery, including from third parties.

System	Available At Least As Of	Short Name	Exhibit Number
HP G-Link Chipset implementing Serial-HIPPI	1992	G-Link	B-10
Silicon Image chips (such as SIL3114 and SIL3512) implementing Serial ATA 1.0	2001	SIL-SATA	B-11

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed

1 above. Defendant reserves the right to identify and rely on systems that represent different versions
2 or are otherwise related variations of the identified systems. Defendant also incorporates by
3 reference any and all other prior art systems identified in any other case brought by Plaintiff and/or
4 involving the Asserted Patents.

5 To the extent any item of prior art cited above is deemed not to disclose, explicitly or
6 inherently, any limitation of an asserted claim of the '307 Patent, Defendant contends that any
7 difference between that prior art and the corresponding patent claim would have been either inherent
8 in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically
9 denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

10 **2. The '307 Patent Claims Are Obvious Over the Prior Art**

11 To the extent Plaintiff argues that any limitation of the asserted claims of the '307 Patent are
12 not explicitly disclosed by an item of prior art identified above, in Exhibits B-1 through B-11, or
13 discussed in the incorporated IPR petition, any purported differences are such that the claimed
14 subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged
15 invention, in view of the state of the art and knowledge of those skilled in the art. The item of prior
16 art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

17 It would have been obvious to combine any of the prior art in Exhibits B-1 through B-11
18 with each other, at least because these prior art references relate to data transmission methods and
19 digital communication devices and attempt to solve a common problem of improving data
20 transmission and control. Moreover, one of ordinary skill in the art would have been well-equipped
21 with sufficient education, knowledge, and training to make the specific combinations with a
22 reasonable expectation of success given the simplicity of the electrical components to one of
23 ordinary skill in the art, the predictability of the arts, and the minimal level of experimentation
24 needed to combine the various teachings. Indeed, the patentee conceded the simplicity and
25 conventional nature of the arts by providing that "[v]arious serial links for transmitting data and
26 clock signals over various media . . . are well known." *See, e.g., '307 Patent*, 1:47-50. Therefore,
27 these references provide interrelated teachings and one of ordinary skill would have looked to the
28

1 concepts in any of these references when attempting to solve the problems in the simple technical
2 field described by the '905 Patent, among other asserted patents.

3 As one example of a prior art reference used to address these problems, U.S. Patent
4 application 2002/0159450 to Shin et al. (Application '450), published October 31, 2002, discloses
5 a serial communications architecture for communicating between devices. Application '450 at
6 Abstract. The communications on physical layer, link layer, and transport layer are disclosed in the
7 network architecture. *Id.* at [0075-0081], Figs. 1, 2, 38A. Together with data signal, control signals
8 are encoded, transferred, and decoded to perform control functions on multiple levels. *Id.* at [0128-
9 0140], Fig. 2.

10 International Patent Application Pub. No. WO 92/09162 to Hornak et al. ("Hornak '162"),
11 published on May 29, 1992, discloses a method of data communication that involves adding
12 additional bits to a data word that include an encoded master transition, data status indication, and
13 a phantom bit indication. Hornak '162 at Abstract and at p. 9 ll. 17-31. Hornak '162 discloses that
14 the phantom bit may be "a user definable bit, such as an additional data bit or some type of control
15 or indicator bit desired by the user." Hornak '162 at p. 9 ll. 17-31, and that control "signals may
16 convey additional information or they may be used to regulate the operation of the receiver itself."
17 Hornak '162 at p. 2 ll. 21-23. Hornak '162 incorporates by reference U.S. patent 5,022,051 (the '051
18 patent) issued 1/4/1991 and U.S. Patent 4,926,447 (the '447 patent) issued 5/15/1990.

19 U.S. Patent No. 5,313,458 to Hiroyuki Suzuki ("Suzuki '458"), issued May 17, 1994,
20 discloses a traffic control system 4 that connects to other traffic control systems that each connect
21 to a subscriber system 2. Suzuki '458 at Abstract and Fig. 1b. Suzuki '458 discloses a traffic control
22 system 4 operating on a frame consisting of a header and payload within the traffic control system
23 4 to perform a network level function of discarding packets when a C2 bit in the header is set. Suzuki
24 '458 at Abstract and at 6:9-32. Suzuki '458 discloses the use of the C2 bit at the link layer function
25 of allowing constant high rate communication between subscriber 2 and traffic control unit 4 by
26 indicating empty frames with the C2 bit. Suzuki '458 at 1:18-30.

27 U.S. Patent Application Pub. No. 2002/0114348 to McCrosky et. al ("McCrosky '348"),
28 published on August 22, 2002, discloses a system for receiving and transmitting from a switch to

1 various endpoints using a link interface that uses an improved standard 8B/10B transmission code.
2 McCrosky '348 at [0118-119]. McCrosky '348 discloses a J0 link level synchronization character
3 that signals the switch to write the J0 Character into a FIFO and to use a set of counters to perform
4 a synchronization operation for multiple endpoints within the switch. McCrosky '348 at [0116-117].
5 McCrosky '348 discloses the use of a J0 character to synchronize both at the character level and at
6 the frame or link level. McCrosky '348 at [0092-93].

7 U.S. Patent No. 6,584,535 to Ouellet, et. al (Ouellet '535), issued June 24, 2003, discloses a
8 configurable interconnect for use with high-speed electronic system components. Ouellet '535 at
9 Abstract. Physical layer, MAC layer, and L3 packet layer are included in the network. *Id.* at 1:52-
10 61, 2:23-26, 5:21-28. The 8B/10B encoding method is used to encode control information into the
11 data stream, controlling events of multiple levels. *Id.* at 6:30-12:18.

12 PCI Express Base Specification Revision 1.0 (PCIe v1), published April 29, 2002, discloses
13 the PCI Express architecture in terms of three discrete logical layers: the Transaction Layer, the
14 Data Link Layer, and the Physical Layer. PCIe v1 on p35-36. PCI Express uses the 8B/10B
15 transmission code system to encode and transfer special symbols for framing and link management.
16 *Id.* at p. 150-56.

17 802.3z Specification (802.3z), published March 8, 2002 by the IEEE, discloses the 802.3z
18 architecture in terms of three discrete logical layers: the MAC client (Network, Transport, session,
19 presentation, and/or application layers), the Data Link Layer, and the Physical Layer. 802.3z,
20 Section 3 at 33-34, Section 1 at 35. 802.3z uses the 8B/10B transmission code system to encode
21 and transfer special symbols for idle and packet management. 802.3z, Section 3 at 45, 36.

22 International Patent Application Pub. No. WO 01/58107 to Azizoglu et al. ("Azizoglu
23 '107"), published on August 9, 2001, discloses a method of encoding signaling information using
24 Gigabit Ethernet, *e.g.* using 8B10B encoding. Azizoglu at Abstract and p. 2 ll. 18-24.

25 European Patent No. EP 0,938,211 to Blanc et al., ("Blanc '211"), Published October 25,
26 1999, discloses a switching architecture that uses 8b/10b coding. Blanc '211 at [0001]. Blanc '211
27 specifically describes the use of one of a set of three comma characters for the purposes of flow
28 control. Blanc '211 at [0017].

1 U.S. Patent No. 4,486,739 to Franaszek et al. ("Franaszek '739"), issued on December 4,
2 1984, discloses a binary DC balanced code and an encoder circuit that forms an 8B/10B code.
3 Franaszek '739 at ABSTRACT. Franaszek '739 discloses a control character such as 28.1, 28.5, or
4 28.7 that is singular, that is, it has a COMMA property that it does not appear in data characters
5 neither in individual characters nor in overlap between adjacent characters. Franaszek '739 at 9:2-
6 14.

7 G-Link HDMP-1000 chip set (G-Link) is designed for network data transmission developed
8 by HP, first sold or offered for sale in the United States by at least October 1992, implementing
9 High-Performance Parallel Interface (HIPPI) and IEEE 802.2-6 protocols. Aspects of G-Link are
10 described in various publications, including, but not limited to:

- 11 • *HIPPI-6400 Technology Dissemination*, Hoffman (1996)
- 12 • *Hewlett-Packard Journal*, Vol. 43, No. 5 (1992)
- 13 • *HIPPI/Serial-HIPPI*, Tolmie et al. (1992)
- 14 • *High Performance Network and Channel-Based Storage*, Katz (1991)
- 15 • *Gigabit Nectar: Architecture and Performance*, Steenkiste (1995)
- 16 • *A Two-Chip 1.5-GBd Serial Link Interface*, Walker, et al. (1992)
- 17 • IEEE Std 802.3-2002, (2002)

18 SI-SATA is a computer communications interface developed by Silicon Image, first sold or
19 offered for sale in the United States by at least December 2002, implementing the SATA
20 Specification published in February 2000, through the efforts of APT Technologies, Dell, Intel,
21 Maxtor, and Seagate. Aspects of SI-SATA are described in various publications, including, but not
22 limited to:

- 23 • Serial ATA: High Speed Serialized AT Attachment (SATA 1.0), August 2001
- 24 • Serial ATA: High Speed Serialized AT Attachment (SATA 1.0a), January 2003
- 25 • *Philips, Intel and Silicon Image Demonstrate World's First DVD+RW Drive with*
26 *Integrated Serial ATA Interface,*
27 [https://web.archive.org/web/20031010134847/http://www.siimage.com/press/02_18_03_3.](https://web.archive.org/web/20031010134847/http://www.siimage.com/press/02_18_03_3.asp)
28 [asp](https://web.archive.org/web/20031010134847/http://www.siimage.com/press/02_18_03_3.asp) (February 19, 2003)

- 1 • *Sil 3114 SATALink 4-Port PCI Host Controller Datasheet*, Silicon Image (2003)
- 2 • 20th Anniversary, SATA-IO, <https://sata-io.org/20th-anniversary>
- 3 • *ASUS A7N8X Deluxe Motherboard Review*,
- 4 <https://www.overclockersclub.com/reviews/asusa7n8xmobo/> (January 18, 2003)
- 5 • *nForce2 6-way Motherboard Roundup*, <https://www.anandtech.com/show/1044/7>
- 6 (December 2002)
- 7 • *Giant Leap Over the High Speed Generation K7 Triton 400 Series GA-7VAXP Ultra VIA*
- 8 *KT400 Based Motherboard*, <https://www.gigabyte.com/Press/News/230> (November 15,
- 9 2002)
- 10 • *Sil 3512 SATALink 2-Port PCI Host Controller Datasheet*, Silicon Image (2003)
- 11 • *Silicon Image Leverages Satalink Architecture To Demonstrate New Serial ATA Port*
- 12 *Multiplier Capability*, [https://web.archive.org/web/20030402052256/http://](https://web.archive.org/web/20030402052256/http://www.siimage.com/press/02_18_03.asp)
- 13 www.siimage.com/press/02_18_03.asp, (February 18, 2003)
- 14 • *Silicon Image Unveils Performance-Leading Serial Ata Host Controller*,
- 15 [https://web.archive.org/web/20031012145907/http://www.siimage.com/press/02_18_03_2.](https://web.archive.org/web/20031012145907/http://www.siimage.com/press/02_18_03_2.asp)
- 16 [asp](http://www.siimage.com/press/02_18_03_2.asp) (February 18, 2003)
- 17 • *Silicon Image Drives SATA Market With New Satalite™ Interface Standard Designed To*
- 18 *Lower Cost Of Implementation And Enable Easy Upgrade To Next-Gen Performance*,
- 19 [https://web.archive.org/web/20030223122311/http://www.siimage.com/press/11_05_02.as](https://web.archive.org/web/20030223122311/http://www.siimage.com/press/11_05_02.asp)
- 20 [p](http://www.siimage.com/press/11_05_02.asp) (November 5, 2002)
- 21 • *Silicon Image Sets The Standard For Digital Consumer Electronics Interfaces With*
- 22 *Panellink Cinema, The World's First HDMI Transmitter And Receiver*,
- 23 [https://web.archive.org/web/20030618091306/http://www.siimage.com/press/01_09_03.as](https://web.archive.org/web/20030618091306/http://www.siimage.com/press/01_09_03.asp)
- 24 [p](http://www.siimage.com/press/01_09_03.asp) (January 9, 2003)
- 25 • *Silicon Image's Serial ATA Host Controller Wins More Than 15 Key Motherboard, Add-*
- 26 *In-Card And Raid Storage System Designs*,
- 27 [https://web.archive.org/web/20020809141406/http://www.siimage.com/press/06_03_02.as](https://web.archive.org/web/20020809141406/http://www.siimage.com/press/06_03_02.asp)
- 28 [p](http://www.siimage.com/press/06_03_02.asp) (June 3, 2002)

1 To the extent that it is determined that any of the above references do not disclose a particular
2 claim element, a person skilled in the art would have been motivated to combine any of the above
3 references (as documented in the claim charts attached as Exhibits B-1 through B-11). In particular,
4 the combinations identified herein would merely have been (a) a combination of prior art elements
5 according to known methods to yield predictable results; (b) a simple substitution of one known
6 element for another to obtain predictable results; (c) a use of known technique to improve similar
7 devices or methods in the same way; (d) application of a known technique to a known device or
8 method ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work
9 in one field of endeavor prompting variations of it for use in either the same field or a different one
10 based on design incentives or other market forces since the variations are predictable to one of
11 ordinary skill in the art. Moreover, a person of ordinary skill in the art had a reason to combine
12 these references because—at a minimum—they all pertain to data transmission methods and digital
13 communication devices.

14 As discussed above, the motivation to combine the teachings of the patents and other prior
15 art referenced above is found in the art as specified in the charts and in: (1) the nature of the problem
16 being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of
17 persons of ordinary skill in the art; and (4) the fact that the prior art is generally directed towards
18 data transmission methods and digital communication devices, and (5) the predictable results
19 obtained in combining the different elements of the prior art. The Supreme Court has held that a
20 showing of a motivation to combine within the references themselves is not required to prove
21 obviousness. *See KSR*, 550 U.S. at 401 (“Any need or problem known in the field of endeavor at
22 the time of invention may provide the motivation to combine.”).

23 Accordingly, because each of the identified references are directed to similar devices in the
24 similar field of endeavor, a person of ordinary skill in the art would be motivated to combine the
25 teachings of two or more references together because the references disclose similar systems that
26 solve the same problems in similar ways. Thus, it would have been obvious to one of ordinary skill
27 in the art to combine any of the foregoing references and one of ordinary skill would have expected
28 such a combination to be successful.

1
2 Thus, to the extent that it is determined that any of the above references do not disclose a
3 particular claim element, it would have been obvious to modify the teachings of that reference to
4 include such element as taught in any other of the above references that discloses such element (as
5 documented in the claim charts attached as Exhibits B-1 through B-11).

6 For example, to the extent it is determined that any of the above references do not disclose
7 the general concept of generating encoded data in accordance with a line code, and transmitting the
8 encoded data over the link to the second endpoint and/or encoding M-bit input words in accordance
9 with a block code to generate a code word sequence of N-bit code words, where $N > M$, it would
10 have been obvious to modify the teachings of that reference to include this feature in view of the
11 knowledge of a POSITA and the teachings of these features in at least the following references and
12 systems: *See, e.g.*, Shin '450, McCrosky '348, Ouellet '535, PCIe v1, Blanc '211, Franaszek '739,
13 802.3z, Azizoglu '107, SI-SATA, or G-Link. As demonstrated in the attached claim charts for these
14 references, each discloses the use of a DC balancing method using 8B/10B code words. Therefore,
15 a POSITA would be motivated to make such a modification to any other reference disclosing
16 transmissions of application data.

17 To the extent it is determined that any of the above references do not disclose asserting a
18 control signal indicative of at least another one of the control bits to higher level circuitry or
19 performing at least one higher level function in response to the at least one control signal, it would
20 have been obvious to modify the teachings of that reference to include this feature in view of the
21 knowledge of a POSITA and the teachings of these features in at least the following references and
22 systems: *See, e.g.*, Shin '450, Suzuki '458, 802.3z, and McCrosky '348, SI-SATA, or G-Link. As
23 demonstrated in the attached claim charts for these references, each discloses asserting a control
24 signal indicative of at least another one of the control bits to higher level circuitry and performing
25 at least one higher level function in response to the at least one control signal. For instance, Shin
26 '450 describes at paragraph [0079] a method of indicating to the transport layer when control
27 symbols are received and thus identifying a packet type or performing flow control at the transport
28

1 layer, as further detailed in Shin '450 at [0097] and [0090]. Therefore, a POSITA would be
2 motivated to make such a modification and/or combination.

3 To the extent it is determined that any of the above references do not disclose “control bits”
4 having “multiple levels of communication protocol functionality,” as claimed, it further would have
5 been obvious to modify the teachings of that reference to include this feature in view of the
6 knowledge of a POSITA and the teachings of these features in at least the following references and
7 systems: *See, e.g.*, Hornak '162, McCrosky '348, Shin '450, Suzuki '458, Blanc '211, SI-SATA, or
8 G-Link. For example, Hornak '162 describes a motivation of saving bits so that they are not required
9 at a higher layers, by providing bits in the link layer header for an arbitrary higher level, or user
10 level purpose. Hornak '162 at p. 9 ll. 17-31. As demonstrated in the attached claim charts for these
11 references, each discloses a link layer symbol functioning at both the link layer and a higher layer.
12 For instance, Suzuki '458 discloses a link layer C2 bit that also functions at a higher layer to
13 “determine whether or not the data frame is to be discarded” by the traffic control system. Suzuki
14 '458 at Abstract, 1:61-66, 6:9-32. Similarly Hornak '162 discloses a phantom bit which performs
15 the link layer function of defining a master transition, and which is provided to a higher level to
16 perform a user definable function. Hornak '162 at p. 9 ll. 17-31, and at p. 2 ll. 21-23. Additionally
17 Yusairi discloses transaction code control bits functional at both the link and transport layers.
18 Yusairi at 55, Sec. 5.2, 5.3. Therefore, a POSITA would be motivated to make such a modification
19 and/or combination.

20 To the extent it is determined that any of the above references do not explicitly disclose
21 “special characters, ... none of the special characters of the encoded data matches a bit sequence of
22 the code word sequence”/“none of the special characters of the encoded data matches a bit sequence
23 of the code word sequence,” as claimed, it would have been obvious to modify the teachings of that
24 reference to include this feature in view of the knowledge of a POSITA and the teachings of these
25 features in at least the following references and systems: *See, e.g.*, Franaszek '739 at 9:2-14,
26 McCrosky '348, Ouellet '535, PCIe v1, 802.3z, and Azizoglu '107, SI-SATA, or G-Link. As
27 demonstrated in the attached claim charts for these references, each reference at least inherently
28 discloses these features under at least UCT's apparent interpretation of the claims. For instance,

1 McCrosky '348 discloses a comma K28.5 character at Fig. 2 and [0075]. Likewise, Ouellet '535
2 discloses the K28.5 character. Ouellet '535 at [0011]. PCIe v1 discloses the K28.5 symbol. Azizoglu
3 '107 likewise teaches the use of a K-character. Azizoglu '107 at p. 16, ll. 23-25. Similarly 802.3z
4 discloses a K28.5 character. 802.3z, Section 3 at 45. One of skill in the art, seeking to solve these
5 problems, would have looked to analogous art to identify ways to solve the problem. Indeed, the
6 solution identified by the patentee had already been identified by others in the field, and one of
7 ordinary skill in the art would have been motivated to combine such analogous teachings in the same
8 manner proposed by the patentee. Additionally, one of skill in the art would have had a reasonable
9 expectation of success because the references contained analogous teachings to those proposed by
10 the patentee, the references describe relatively simple electrical technologies in predictable fields,
11 and the modifications and combinations would not require undue experimentation. As such, one of
12 skill would have been motivated to combine the references.

13 In addition to the combinations discussed above, exemplary combinations which render
14 obvious some or all of the Asserted Claims of the '307 Patent are listed in **Appendix A**, Sec. II.

15 **B. Invalidity of the '307 Patent Based on 35 U.S.C. § 112, ¶ 2**

16 Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of
17 the '307 Patent, to the extent such positions can be understood from Plaintiff's Infringement
18 Contentions, Defendant asserts that the Asserted Claims of the '307 Patent are invalid for reciting
19 at least the following claim term:

- 20 • **"The control bits have multiple levels of communication protocol functionality" (claims**
21 **23 and 68):** As described in the '307 Patent, this term could mean either that: (1) each control
22 bit must have multiple levels of functionality; or (2) that the collective group of control bits
23 have multiple levels of functionality. '307 Patent at 4:66-5:14, 18:30-44, 55:14-24. The
24 claim language does not indicate which of these two distinct and conflicting scenarios is
25 encompassed by the scope of the claims.
- 26 • **"Indicative of" (all asserted claims):** This term is not defined in the '307 Patent and is so
27 vague as to encompass myriad possible definitions of unbounded scope. For example, it is
28

1 not clear whether this term should be understood to mean “included,” “represented by,”
2 “related to,” “translated to,” “occurs as a result of,” or some other meaning.

3 These claim terms, as apparently construed by Plaintiff, violate the definiteness requirements
4 of 35 U.S.C. § 112 at least because they fail to inform, with reasonable certainty, those skilled in
5 the art about the scope of the invention. Based on Defendant’s present understanding of Plaintiff’s
6 Infringement Contentions, at least these claim terms are indefinite because they are inconsistent
7 with and/or broader than the alleged invention disclosed in the specification and during prosecution,
8 and given Plaintiff’s apparent constructions of the claims, a POSITA at the time of the invention
9 would not understand what is claimed with reasonable certainty, even when the claims are read in
10 light of the specification and prosecution history.

11 **V. THE ASSERTED CLAIMS OF THE ’798 PATENT ARE INVALID**

12 **A. Identification of Prior Art**

13 Defendant contends that the prior art references charted in Exhibits C-1 through C-11,
14 discussed in any incorporated IPR petition, and/or described below anticipate and/or render obvious,
15 alone or in combination, one or more of the Asserted Claims of the ’798 Patent.

16 **1. The ’798 Patent Claims Are Anticipated by the Prior Art**

17 Some or all of the Asserted Claims of the ’798 Patent are invalid as anticipated under 35
18 U.S.C. § 102 in view of each of the prior art references identified in the claim charts included in
19 Exhibit C-1 through C-11 and/or identified in any incorporated IPR petition, which identify specific
20 examples of where each limitation of the Asserted Claims is found in the prior art references. As
21 explained above, the cited portions of prior art references identified in the attached claim charts are
22 exemplary in nature and representative of the content and teaching of the prior art references, and
23 should be understood in the context of the reference as a whole and as they would be understood by
24 a person of ordinary skill in the art.

25 In addition to references identified in any incorporated IPR petition, Defendant identifies the
26 following references as anticipating one or more of the Asserted Claims of the ’798 Patent under 35
27 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an
28 admission that any reference not listed below does not also anticipate the claims of the ’798 Patent.

Further, Defendant contends that any prior art reference in the attached charts that is charted for each limitation of any given claim, anticipates that claim, regardless of whether that prior art reference is listed in the following tables.

a) Prior Art Patents and Applications

Number	Published/Issued Date	Short Name	Exhibit Number
U.S. Patent No. 5,592,487	Filed: Mar. 20, 1995 Issued: Jan. 7, 1997	Knecht	C-1
U.S. Patent No. 5,686,965	Filed: Sep. 18, 1995 Issued: Nov. 11, 1997	Auld	C-2
European Patent Application No. 1,137,278	Filed: Mar. 20, 2001 Pub'd: Sep. 26, 2001	Kotani	C-3
U.S. Patent No. 5,790,607	Filed: Nov. 28, 1995 Issued: Aug. 4, 1998	Burke	C-4
U.S. Patent No. 6,609,167	Filed: Mar. 15, 2000 Issued: Aug. 19, 2003	Bastiani	C-5
U.S. Patent No. 7,251,256	Filed: May 18, 2000 Issued: July 31, 2007	Barry	C-6
WIPO Patent Pub. No. 1999/023776	Filed: Oct. 31, 1997 Pub'd: May 14, 1999	Hui	C-7
U.S. Patent No. 5,917,830	Filed: Oct. 18, 1996 Issued: June 29, 1999	Chen	C-8
U.S. Patent No. 6,430,230	Filed: June 30, 1999 Issued: Aug. 6, 2002	Cunningham	
U.S. Patent No. 5,801,781	Filed: June 19, 1996 Issued: Sep. 1, 1998	Hiroshima	
WIPO Patent Pub. No. 2000/011831	Filed: Aug. 17, 1999 Pub'd: Mar. 2, 2000	Haartsen	
U.S. Patent No. 5,974,464	Filed: Sep. 30, 1996 Issued: Oct. 26, 1999	Shin	
U.S. Patent No. 6,498,568	Filed: Sep. 24, 1997 Issued: Dec. 24, 2002	Austin	
WIPO Patent Pub. No. 1992/09162	Pub'd: May 29, 1992	Hornak	C-10

b) Prior Art Publications

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
ISO (International Organization for Standardization)	Information Technology – Generic coding of moving pictures and associated audio information: Systems	April 1, 1996	MPEG-2, Part 1	See IPR 2024-01481

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the '798 Patent, Defendant contends that any difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

c) Prior Art Systems

On information and belief, systems implementing the protocols identified below were in public use, on sale, or otherwise available to the public before the priority date of the '798 Patent. Defendant's further investigation and/or subsequent discovery from Plaintiff or third parties with knowledge regarding prior art systems may reveal additional relevant prior art systems and/or further information regarding the systems identified below, or other relevant prior art systems. Defendant reserves the right to supplement these Invalidity Contentions, based on subsequent investigation and discovery, including from third parties.

System	Available At Least As Of	Short Name	Exhibit Number
Gigabit Ethernet employing IEEE 802.3z (1998)	1998	802.3z-1998	C-9

1	HP G-Link Chipset implementing Serial- HIPPI	1992	G-Link	C-11
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2 Defendant additionally identifies and relies on any system, product, or public knowledge or
3 use that embodies or otherwise incorporates any of the prior art patents and publications listed
4 above. Defendant reserves the right to identify and rely on systems that represent different versions
5 or are otherwise related variations of the identified systems. Defendant also incorporates by
6 reference any and all other prior art systems identified in any other case brought by Plaintiff and/or
7 involving the Asserted Patents.

8 To the extent any item of prior art cited above is deemed not to disclose, explicitly or
9 inherently, any limitation of an asserted claim of the '798 Patent, Defendant contends that any
10 difference between that prior art and the corresponding patent claim would have been either inherent
11 in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically
12 denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

13 **2. The '798 Patent Claims Are Obvious Over the Prior Art**

14 To the extent Plaintiff argues that any limitation of the asserted claims of the '798 Patent are
15 not explicitly disclosed by an item of prior art identified above, in Exhibits C-1 through C-11, or
16 discussed in any incorporated IPR petition, any purported differences are such that the claimed
17 subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged
18 invention, in view of the state of the art and knowledge of those skilled in the art. The item of prior
19 art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

20 It would have been obvious to combine any of the prior art in Exhibits C-1 through C-11
21 with each other, at least because all of these references relate to synchronizing serial
22 communication(s) between two devices.

23 For example, U.S. Patent No. 5,592,487 ("Knecht") teaches that "[a] communications
24 protocol is established with data packets, control packets, checksum packets, and synchronization
25 symbols. One of the control packets is transmitted after a synchronization symbol is transmitted.
26 One of the synchronization symbols, data packets, or checksum packets is transmitted after one of
27 the control packets is transmitted. One of the synchronization symbols is transmitted after one of
28 the checksum packets is transmitted, and one of the synchronization symbols or another of the data

1 packets is transmitted after one of the data packets is transmitted.” Knecht, 2:3–13. Knecht further
2 teaches that the “[c]ommunication protocol is established and maintained with four signals, namely:
3 sync symbol, data packet, control packet, and checksum packet. In the preferred embodiment,
4 control, data and checksum packets comprise 16 bits of information before encoding and 20 bits
5 after encoding.” *Id.* at 3:28–32.

6 U.S. Patent No. 5,686,965 (“Auld”) teaches that “[a]n MPEG ISO system bitstream typically
7 includes a sequence of packs 90. A typical pack 90, in turn, includes a sequence pack layer headers
8 92, a system header packet 94, a sequence of packets 96, 98, and 100, and an end code 102. The
9 pack layer header 92 contains a pack start code, or sync code, used for synchronization purposes,
10 and a system clock value. The system header packet 94 contains a variety of information commonly
11 referred to as system housekeeping data, and a system stream ID which is used to differentiate
12 among multiple system streams. A sequence of one or more packets typically contains either
13 encoded audio or encoded video stream data. The final element of a pack 90 is an end code 102. It
14 should be noted that any one packet 96, 98, 100 may carry either audio or video data, but not both
15 simultaneously. With respect to a packet containing video data, typically a video packet header and
16 one or more video frames is contained within the packet.” Auld, 10:20–36.

17 European Patent Application No. 1,137,278 (“Kotani”) teaches “the structure of a packet
18 generated by a VCR. A sync pattern of about 2 bytes, which indicates the head of the packet, and
19 an ID of about 3 bytes, which includes address information on data, are added to the packet.” Kotani,
20 ¶ 4. Kotani further teaches that “packets for commercialized household digital VCRs can be
21 classified into two types, i.e., a 12-byte sub-code packet including a 2-byte sync pattern, and a 90-
22 byte AV data packet including a 2-byte sync pattern.” *Id.* ¶ 5. Kotani further teaches that “[w]hen
23 there are two types of time-division multiplexed HD data (for example, when there are a sub-code
24 and AV data), it is necessary to add different sync patterns to the two types of data in order to
25 discriminate between each type of data.” *Id.* ¶ 35.

26 U.S. Patent No. 5,790,607 (“Burke”) teaches that “for asynchronous data transmission and
27 reception, it is highly desirable to organize the data into predetermined formats or packets for
28 accurate and reliable data reception. In addition to providing the actual data, which is highly variable

1 and essentially random, the data packet should also provide appropriate timing and synchronizing
2 information needed for accurate data reception, without creating excessive overhead and without
3 decreasing data throughput. In addition, for asynchronous data transmission and reception, an
4 apparatus and method is also necessary to quickly, reliably and accurately detect such timing and
5 synchronizing information prior to the reception of any actual data, without excessive or
6 unnecessary processor complexity, speed, and cost.” Burke, 2:38–51.

7 U.S. Patent No. 6,609,167 (“Bastiani”) teaches that “a method for communicating serial data
8 between a host computer and a peripheral device is disclosed. The packet for communication
9 between the host computer and the peripheral device includes: (a) a synchronization field; (b) a
10 packet type (PT) field following the synchronization field, the packet type field defining an error
11 correction type for the packet; (c) a byte count (BC) field for defining a length of data for the packet;
12 (d) a data type (DT) field for defining whether the data is one of link control, device control, and
13 device data; (e) a data field; and (f) a CRC field for error checking the data in the data field.”
14 Bastiani, 2:29–39.

15 U.S. Patent No. 7,251,256 (“Barry”) teaches that “[a]n LMAC-compatible link has the
16 following characteristics: (a) the two devices at the endpoints of the link are not synchronized, e.g.
17 the link is asynchronous; (b) the data transported on the link is in the form of packets, cells, or
18 frames; and (c) the MAC layer encoding of the data is such that devices called LMACs can insert
19 synchronization symbols anywhere into the data stream at the ingress end of the link and remove
20 them at the egress end so that the synchronization symbols are not visible to higher-layer
21 components that process data packets.” Barry, 3:61–4:3. Barry further teaches that “[i]n the LMAC
22 protocol, the MAC layer encoding of the data is such that devices called LMACs can insert
23 synchronization symbols anywhere into the data stream at the ingress end of an LMAC-compatible
24 link and remove them at the egress end so that the synchronization symbols are not visible to higher-
25 layer components that process data packets.” Barry, 4:65–5:4.

26 WIPO Patent Publication No. 1999/023776 (“Hui”) teaches that “[i]n data retrieval or
27 communication systems, digital data or digitized multimedia information which can be, potentially,
28 large or variable in size is normally packetized before storage or transmission. This process breaks

1 the data into smaller packets where each packet contains one or more detectable synchronization
2 patterns called sync-word, necessary information about the packet, and a payload of a smaller
3 partition of the original data. The information about the packet may consist of a packet identification
4 (ID), size of the payload contained in the current packet, timing information, and any necessary side
5 information.” Hui, 1:13–19.

6 U.S. Patent No. 5,917,830 (“Chen”) teaches “the insertion of digital video messages such as
7 commercials into a pre-existing compressed packetized data stream.” Chen, 1:7–9. Chen further
8 teaches that “a transport stream, or transport multiplex is made up of a contiguous set of fixed length
9 packets. Each packet is 188 total bytes in length, with the first four of those bytes being defined as
10 the packet header.” *Id.* at 14:47–50. Chen further discloses that “[v]arious timing and identification
11 information is provided in different portions of the transport stream. These include a packet
12 identifier (PID) found in the transport header of each transport packet” and “a program clock
13 reference (PCR) which effectively represents a sample of the system time clock (STC) time base
14 that underlies the service composed of the PIDs referenced in the service map.” *Id.* at 14:57–59,
15 15:5–8.

16 U.S. Patent No. 6,430,230 (“Cunningham”) teaches “a method of encoding payload bits for
17 transmission over a communications link such that the running disparity of the transmitted symbol
18 stream is constrained within a predetermined limit, and said payload bits comprising either data or
19 control information.” Cunningham, 1:58–63. Cunningham further teaches that “a data frame
20 intended to be communicated over an optical fibre channel 20 typically comprises a binary digital
21 message (payload) to be transferred between stations on the network; this message may comprise
22 user data, or control information for managing operation of the network and its components.” *Id.* at
23 2:65–3:3. Cunningham further teaches that “[c]ontrol information is conveyed by using selected n-
24 bit data block values, together with a distinctive value of 10 for the pair of label bits a and b to
25 indicate that the associated data block represents control information rather than actual data.” *Id.* at
26 4:23–27.

27 U.S. Patent No. 5,801,781 (“Hiroshima”) teaches “the details of the MPEG2-TS. Each
28 packet of the MPEG2-TS has a prefix length of 188 bytes. The header 194 consists of four bytes

1 and the payload 196 consists of 184 bytes. The header 194 is constructed by sync bytes 198, an error
2 indicator 200, a unit start indicator 202, a transport priority 204, a packet ID 206, a scramble control
3 208, an adaptation field control 210, a continuity counter 212, and an adaptation field 214.”
4 Hiroshima, 10:51–58. Hiroshima further teaches “a process for forming the MPEG2-TS from the
5 PES packet 82 by a multiplexing process.” *Id.* at 11:13–14.

6 WIPO Patent Publication No. 2000/011831 (“Haartsen”) teaches “a multi-part digital
7 preamble for use in transmitting digital data packets. Advantageously, a preamble according to the
8 invention substantially reduces the overall length of DC-free sequences that are transmitted with
9 each data packet in a digital FM system.” Haartsen, 5:3–6. More specifically, Haartsen teaches that
10 “a digital preamble can be strategically divided into three or more parts so that synchronization and
11 other information can be included within the preamble while still enabling accurate DC estimation.”
12 *Id.* at 12:13–16.

13 U.S. Patent No. 5,974,464 (“Shin”) teaches “a high-speed digital video signal transmission
14 system in which high-speed video transmission is effected between a host computer system and a
15 system display.” Shin, 4:56–59. Shin further teaches that “various synchronization and other
16 special characters are defined using the high-transition and low-transition sets of out-of-band
17 characters. . . . The difference in the number of transitions between in-band and out-of-band
18 characters allows selected out-of-band characters to serve as control characters, and to be readily
19 distinguished from in-band characters within the transmitted data stream.” *Id.* at 9:64–10:8.

20 U.S. Patent No. 6,498,568 (“Austin”) teaches a “system [that] uses up to 5 pre-defined data
21 packet sizes and up to 16 user defined data message types within each packet. Each packet has
22 Forward Error Connection (FEC) and bit interleaving applied to it on transmission. Error checking
23 is performed using a standard CRC. The system uses standard run in and byte synchronisation
24 techniques. The byte synchronisation word used is 32 bits long and there are 5 different words used,
25 one to identify each of the different packet types.” Austin, 4:37–45.

26 ISO/IEC 13818-1, first edition 1996-04-15 (“MPEG-2, Part 1”) is a standard specification
27 that was published in April 1996 by the International Organization for Standardization (ISO).
28 MPEG-2, Part 1 “addresses the combining of one or more elementary streams of video and audio,

1 as well as other data, into single or multiple streams which are suitable for storage or transmission.”
2 MPEG-2, Part 1 at viii. MPEG-2, Part 1 describes a “Program Stream” which “can be decoded with
3 synchronization.” *Id.* at ix. The standard further includes a specification of the “Program Stream,”
4 including its syntax and semantics. *Id.* at Section 2.5.3. Video and audio data compressed according
5 to the specification of the “Program Stream” “are packetized to produce PES [packetized elementary
6 stream] packets.” *Id.* at viii.

7 IEEE Std 802.3 (“802.3z-1998”) is a working group of standard specifications for Ethernet
8 that describes a method of packet-based physical communication in a local area network maintained
9 by the Institute of Electrical and Electronics Engineers (IEEE). Its 1998 Edition (“802.3z-1998”)
10 was first implemented in systems in the United States by at least 1998. 802.3-1998 accordingly is
11 prior art to the ’798 patent under pre-AIA 35 U.S.C. 102(a)(1), and for at least the reasons described
12 below, invalidates the asserted claim 11, 19, 22, 25, 28 of the ’798 patent. Additionally, devices
13 employing the IEEE Std 802.3 were offered for sale before the ’798 patent. For example, the
14 1000BASE-T Gigabit Ethernet Connection employing the IEEE Std 802.3 was included in Apple’s
15 Power Mac G4 no later than October 2000.

16 G-Link HDMP-1000 chip set (G-Link) is designed for network data transmission developed
17 by HP, first sold or offered for sale in the United States by at least October 1992, implementing
18 High-Performance Parallel Interface (HIPPI) and IEEE 802.2-6 protocols. Aspects of G-Link are
19 described in various publications, including, but not limited to:

- 20 • James R. Hoffman, “HIPPI-6400 Technology Dissemination,” SPIE Photonics East (Nov.
21 18, 1992) (“Hoffman”);
- 22 • “The G-Link Chipset for Gigabit-Rate Data Communication,” pp. 103-116 Hewlett-Packard
23 Journal (Oct. 1992) (“HPJ”);
- 24 • Walker et al., “A Two-Chip 1.5 G-Bd Serial Link Interface,” IEEE Journal of Solid State
25 Circuits (Dec. 1992) (“Walker”);
- 26 • Peter Steenkiste, “Gigabit Nectar: Architecture and performance” (Sept. 1995) (“Gigabit”);
- 27 • Tolmie et al., “HIPPI/Serial-HIPPI,” (1992);
- 28 • Katz, “High Performance Network and Channel-Based Storage” (1991);

- “IEEE Standard for Scalable Coherent Interface (SCI),” IEEE Std 1596-1992 (Mar. 19, 1992) (“SCI”)

Accordingly, because each of the identified references are directed to similar devices in the similar field of endeavor, a person of ordinary skill in the art would be motivated to combine the teachings of two or more references together because the references disclose similar systems that solve the same problems in similar ways. Thus, it would have been obvious to one of ordinary skill in the art to combine any of the foregoing references and one of ordinary skill would have expected such a combination to be successful.

For example, to the extent that it is determined that any of the above references do not disclose a “different synchronization symbol” for each “packet type,” it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Auld, 10:53–61 (“The packet data field of the packet layer 96 may contain emulations of the sync codes of other bitstream data, such as those comprising audio packets. The system synchronizer 62, however, analyzes the bitstream to determine whether a legitimate video packet sync code has been located, as at 126. If either the video sync code has not been located or a sync code emulation is located, the system synchronizer 62 will continue to predict the occurrence of a legitimate video sync code in the bitstream.”); Kotani, ¶ 35 (“When there are two types of time-division multiplexed HD data (for example, when there are a sub-code and AV data), it is necessary to add different sync patterns to the two types of data in order to discriminate between each type of data.”); Bastiani, 24:58–63 (“A packet type (PT) immediately follows the SYNC field of every ASP packet. A PT consists of a four bit packet type field followed by a four-bit check field as shown in FIG. 18. The PT indicates the type of packet and, by inference, the format of the packet and the type of error detection applied to the packet.”); Hui, 13:6–7 (“The sync-word is defined based on applications or packet types, and is normally a digital pattern not easily found within the payload.”); Chen, 14:56–15:3 (“Various timing and identification information is provided in different portions of the transport stream. These include a packet identifier (PID) found in the transport header of each transport packet to provide a reference number for identifying the transport packets carrying a specific service component. . . . Each type of packet will have a different PID identifying the packet

1 type.”); Cunningham, 4:23–27 (“Control information is conveyed by using selected n-bit data block
2 values, together with a distinctive value of 10 for the pair of label bits a and b to indicate that the
3 associated data block represents control information rather than actual data.”); Hiroshima, 11:16–
4 22 (“The TS header 194 is formed in a manner such that the parameters such as error indicator 200
5 indicative of the presence or absence of the bit error in the packet, unit start indicator 202 indicating
6 whether a new PES packet appears in the TS payload or not, packet ID 206 indicating whether the
7 packet in the payload is video or audio”); Haartsen, 12:19–13:2 (“Thereafter, a synchronization
8 part of the preamble, which is not necessarily DC free, but which is protected by code to prevent
9 detection errors, can be used not only to synchronize detection of a data packet, but also to carry
10 timing and/or other useful information (e.g., channel identification, destination address, time of day,
11 user identification, etc.).”); Austin, 4:42–45 (“The byte synchronisation word used is 32 _bits long
12 and there are 5_different words used, one to identify each of the different packet types.”). Therefore,
13 a person of ordinary skill in the art would be motivated to make such a combination.

14 To the extent that it is determined that any of the above references do not disclose
15 “synchronization information,” it would further have been obvious to modify the teachings of that
16 reference to include this feature in view of the following teachings: *See, e.g.*, Burke, 3:41–48 (“In
17 the preferred embodiment of the invention, data for transmission is organized into packets beginning
18 with a ‘preamble’ 101 comprising a known, predetermined bit sequence, followed by a transition
19 102 comprising an indicator that data will follow, such as synchronizing information (a SYNC word
20 preferably [sic] having a high autocorrelation), followed by a data stream 103 having a variable
21 length”); Hui, 13:6–9 (“The sync-word is defined based on applications or packet types, and is
22 normally a digital pattern not easily found within the payload. After detection of the sync-word, the
23 process checks at step 503 for the correct packet ID which may be used to differentiate packets from
24 different data sources, types, or versions.”); Haartsen, 13:16–19 (“The synchronization word 520,
25 which can include timing and/or other information and which is coded to protect against detection
26 errors, is in turn followed by a trailing DC-free sequence 530.”). Therefore, a person of ordinary
27 skill in the art would be motivated to make such a combination.

1 To the extent that it is determined that any of the above references do not disclose packets
2 containing “in-band symbols” that are “transition optimized” and synchronization symbols that are
3 “out-of-band symbols” and “not transition optimized,” it would further have been obvious to modify
4 the teachings of that reference to include this feature in view of the following teachings: *See, e.g.,*
5 Auld, 11:14–19 (“A typical sync word may be represented by a 24-bit or 32-bit word made up of
6 consecutive zeros and ending with a ‘1’ bit. Alignment involves the recognition of word or byte
7 boundaries within a system bitstream in accordance with the syntax of the selected compression
8 algorithm.”); Knecht, 4:46–49 (“The 5-bit codes, with the exception of the sync symbol, are
9 formatted in a 40/60 percent ratio of 0 and 1 bits, with either end of the 5-bit code being made up of
10 no more than two logical ‘0’ or ‘1’ bits.”), 5:37–38 (“Two representations of sync symbols namely
11 00000 and 11111 are necessary.”); Kotani, ¶ 6 (“Ten 1’s or ten 0’s are repeated in the respective
12 [sync] patterns. In this way, erroneous detection of data bits and sync patterns is prevented since the
13 number of consecutive 0’s is restricted in the data bits.”); Shin, 9:66–10:8 (“Each character
14 corresponding to one of these ‘out-of-band’ characters associated with the high-transition set
15 includes less than four logical transitions, and each of the out-of-band characters associated with the
16 low-transition set of code characters includes more than four logical transitions. The difference in
17 the number of transitions between in-band and out-of-band characters allows selected out-of-band
18 characters to serve as control characters, and to be readily distinguished from in-band characters
19 within the transmitted data stream.”). Therefore, a person of ordinary skill in the art would be
20 motivated to make such a combination.

21 To the extent that it is determined that any of the above references do not disclose packet
22 types that include a “control packet,” it would further have been obvious to modify the teachings of
23 that reference to include this feature in view of the following teachings: *See, e.g.,* Knecht, 3:28–32
24 (“Communication protocol is established and maintained with four signals, namely: sync symbol,
25 data packet, control packet, and checksum packet. In the preferred embodiment, control, data and
26 checksum packets comprise 16 bits of information before encoding and 20 bits after encoding.”);
27 Kotani, ¶ 5 (“For example, packets for commercialized household digital VCRs can be classified
28 into two types, i.e., a 12-byte sub-code packet including a 2-byte sync pattern, and a 90-byte AV

1 data packet including a 2-byte sync pattern.”); Bastiani, 26:48–50 (“Data type 1 will be used for
2 control and status of the device, and Data type 2 will be used to transfer data to the device.”); Chen,
3 14:65–15:3 (“In the case of video, audio or isochronous control data, the stream of packets labeled
4 with a single PID represents a single video, audio or isochronous data service elementary stream,
5 respectively. Each type of packet will have a different PID identifying the packet type.”);
6 Cunningham, 4:23–27 (“Control information is conveyed by using selected n-bit data block values,
7 together with a distinctive value of 10 for the pair of label bits a and b to indicate that the associated
8 data block represents control information rather than actual data.”). Therefore, a person of ordinary
9 skill in the art would be motivated to make such a combination.

10 Additionally, to the extent that it is determined that any of the above references do not
11 disclose transmitting symbols to a “switch network,” it would further have been obvious to modify
12 the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*,
13 Burke, 1:31–36 (“[D]igital data may be transmitted both in the downstream direction, from the head
14 end (connected to a network) to the individual user (subscriber access unit), and in the upstream
15 direction, from the individual user to the head end (and to the network).”); Bastiani, 6:3–6 (“ASP is
16 a star network that supports data exchange between a host computer and storage devices such as
17 disks, tapes and CD’s. The attached peripherals share ASP bandwidth through a host scheduled
18 polling based protocol.”), 6:20–23 (“In this example, the host adapter 104 is configured to include
19 ASP circuitry 104 a for processing ASP packet data and communicating between the host computer
20 102 and the ASP device 106.”); Barry, 12:17–23 (“The output of packet processor 54 enters the
21 switch fabric 50. One suitable packet switch is the MMC Networks model nP5400 Packet Switch
22 Module. In one embodiment, four such switches are connected in each switching card for faster
23 throughput. This embodiment is used on the switching card. The capabilities of this switch are not
24 critical to this specification.”); Chen, 4:63–67 (“A compressed digital packetized data stream which
25 includes the inserted message combined with the main program is output from the DAIM 130 to an
26 ATM transmitter (Tx) interface 126, and then provided to an access network (e.g., cable system
27 headend) 140.”); Cunningham, 2:65–3:1 (“Referring to FIG. 1, a data frame intended to be
28 communicated over an optical fibre channel 20 typically comprises a binary digital message

1 (payload) to be transferred between stations on the network. . . .”); Hiroshima, 5:40–43 (“The video-
2 on-demand system corresponds to MPEG2 having a transmission rate of 6.144 Mbps and transmits
3 data by a prefix bit rate of the MPEG2-TS through the network 22.”). Therefore, a person of
4 ordinary skill in the art would be motivated to make such a combination.

5 To the extent that it is determined that any of the above references do not disclose a
6 “synchronization primitive” made up of “a sequence of bit-string synchronization symbols,” it
7 would further have been obvious to modify the teachings of that reference to include this feature in
8 view of the following teachings: *See, e.g.*, Bastiani, 24:43–46 (“A minimum of two and maximum
9 of four SYNC characters must be sent to assure byte synchronization. It is used by the receive
10 circuitry to align incoming data bytes and is defined to be eight bits in length.”); Cunningham, 7:5–
11 8 (“There are many potential ways to achieve code block synchronization (i.e. correct alignment in
12 the receiver of the label and payload fields). For example, one technique would be to transmit a
13 ‘comma sequence’ during start-up.”); Shin, 15:20–26 (“During each preambing period, three
14 repetitions of the same synchronization character are produced by the encoder 18. As is described
15 herein, by processing the 21 bits most recently produced by the encoder 14, synchronization module
16 114 is able to detect at least one of the three repetitions of the synchronization character transmitted
17 during a given preambing period.”). Therefore, a person of ordinary skill in the art would be
18 motivated to make such a combination.

19 A person skilled in the art would have been motivated to combine any of the above
20 references. In particular, the combinations identified herein would merely have been (a) a
21 combination of prior art elements according to known methods to yield predictable results; (b) a
22 simple substitution of one known element for another to obtain predictable results; (c) a use of
23 known technique to improve similar devices or methods in the same way; (d) application of a known
24 technique to a known device or method ready for improvement to yield predictable results; (e)
25 obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in
26 either the same field or a different one based on design incentives or other market forces since the
27 variations are predictable to one of ordinary skill in the art. Moreover, a person of ordinary skill in
28

1 the art had a reason to combine these references because—at a minimum—they all pertain to serial
2 communication between a transmitting device and a receiving device using packets.

3 As discussed above, the motivation to combine the teachings of the patents and other prior
4 art referenced above is found in the art as specified in the charts and in: (1) the nature of the problem
5 being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of
6 persons of ordinary skill in the art; and (4) the fact that the prior art is generally directed towards
7 communication between a transmitting device and a receiving device using packets, and (5) the
8 predictable results obtained in combining the different elements of the prior art. The Supreme Court
9 has held that a showing of a motivation to combine within the references themselves is not required
10 to prove obviousness. See *KSR*, 550 U.S. at 401 (“Any need or problem known in the field of
11 endeavor at the time of invention may provide the motivation to combine.”).

12 For example, a person skilled in the art would have been motivated to combine Auld with
13 Haartsen, Kotani, Shin, and/or additional references discussed above and disclosed in Exhibits C-1
14 through C-11 for the reasons provided above. Moreover, the combination of references is no more
15 than a combination of systems all directed to serial transmission of data using packets. Additionally,
16 the combination reflects no more than a simple substitution of known elements for one another to
17 obtain predictable results. For example, a simple substitution of Haartsen’s digital preamble for
18 Auld’s sync code would achieve the predictable result of incorporating synchronization information
19 into a synchronization symbol. As another example, a person of ordinary skill in the art would have
20 been motivated to implement Kotani’s disclosure of a unique synchronization code for subcode (i.e.,
21 control) packets into Auld, which discloses a need to distinguish between packet types.
22 Additionally, the straightforward addition of Shin’s preamble sequence to Auld would enhance
23 the capability of Auld’s system to synchronize and align the transmitted data packets.

24 A person skilled in the art would have been motivated to combine Bastiani with Haartsen,
25 Kotani, Knecht, Shin, and/or additional references discussed above and disclosed in Exhibits C-1
26 through C-11 for the reasons provided above. Moreover, the combination of references is no more
27 than a combination of systems all directed to serial transmission of data using packets. Additionally,
28 the combination reflects no more than a simple substitution of known elements for one another to

1 obtain predictable results. For example, a simple substitution of Haartsen's digital preamble for the
2 non-data fields of the packets in Bastiani would achieve the predictable result of incorporating
3 synchronization information into a synchronization symbol. As another example, a person of
4 ordinary skill in the art would have been motivated to implement the out-of-band synchronization
5 symbols in Kotani and Knecht in order to avoid the erroneous detection of packets and
6 synchronization symbols. Additionally, the straightforward addition of Shin's preamble sequence
7 to Bastiani would enhance the capability of Bastiani's system to synchronize and align the
8 transmitted data packets.

9 Thus, in addition to the combinations discussed above, exemplary combinations which
10 render obvious some or all of the Asserted Claims of the '798 Patent are listed in **Appendix A**, Sec.
11 III.

12 **B. Invalidity of the '798 Patent Based on 35 U.S.C. § 112, ¶ 1**

13 Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of
14 the '798 Patent, to the extent such positions can be understood from Plaintiff's Infringement
15 Contentions, Defendant asserts that the Asserted Claims of the '798 Patent are invalid for failure to
16 provide a written description that enables the full scope of the Asserted Claims based on at least the
17 following claim terms, phrases, or limitations:

- 18 • **"synchronization symbol" (claims 11, 19, 22, 28):** To the extent UCT contends that
19 "synchronization symbol" has the same meaning as a "synchronization primitive" or
20 "synchronization information," this lacks written description support in the specification. In
21 addition, the specification of the '798 Patent does not describe a "synchronization primitive"
22 or "synchronization information," so those terms lack written description support and are
23 not enabled by the disclosure in the '798 Patent for at least this additional reason.
- 24 • **"synchronization primitive" (claims 11, 19, 28):** *See above.*
- 25 • **"synchronization information" (claim 19):** *See above.*
- 26 • **"bit-string synchronization symbols" (claim 28):** *See above.*

27 Based on Defendant's present understanding of Plaintiff's Infringement Contentions and
28 apparent interpretation of the scope of the Asserted Claims, at least one or more of these claim terms,

1 phrases, and limitations lack written description support, as they are not identified, described, or
2 explained in the specification of the Asserted Patent, and do not enable a person of ordinary skill in
3 the art to practice the claimed invention without undue experimentation or to distinguish all
4 operative embodiments from all nonoperative embodiments without undue experimentation.

5 **C. Invalidity of the '798 Patent Based on 35 U.S.C. § 112, ¶ 2**

6 Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of
7 the '798 Patent, to the extent such positions can be understood from Plaintiff's Infringement
8 Contentions, the Asserted Claims of the '798 Patent are invalid at least because they fail to inform,
9 with reasonable certainty, those skilled in the art about the scope of the invention. At least the
10 following claim language is indefinite:

- 11 • **“the synchronization symbol permitting properly alignment upon receiving with a**
12 **synchronization primitive to be correctly aligned on a symbol boundary (claim 11):** The
13 scope of this limitation is not clear, as the claim language does not describe what element
14 performs the “receiving” function and does not clearly identify what is “received.”
- 15 • **“synchronization information” (claim 19):** The '798 Patent specification does not describe
16 “synchronization information” or how the synchronization symbol provides such
17 information or how such information is different from the “synchronization symbol” or the
18 “synchronization primitive.”
- 19 • **“the transmitted synchronization symbol . . . permitting an external receiving node to**
20 **properly align with a synchronization primitive to be correctly aligned on a symbol**
21 **boundary” (claim 19):** It is not clear how a “external receiving *node*” aligns with the
22 “synchronization symbol,” “synchronization primitive,” or both, rendering this limitation
23 indefinite.

24 These claim terms, phrases, limitations, and all dependent claims thereof, as apparently
25 construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112 at least because they
26 fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

27 Based on Defendant's present understanding of Plaintiff's Infringement Contentions, one or
28 more of these claim terms, phrases, and limitations are indefinite because they are inconsistent with

1 and broader than the alleged invention disclosed in the specification and during prosecution, and
2 given Plaintiff's apparent constructions of the claims, a person of ordinary skill in the art at the time
3 of the invention would not understand what is claimed with reasonable certainty, even when the
4 claims are read in light of the specification and prosecution history.

5 Additionally, at least claim 19 (and its dependent claims) of the '798 Patent recites functions
6 without sufficient structure for performing the function, thus invoking 35 U.S.C. § 112, ¶ 6. Because
7 the specification of the '798 Patent also does not recite structure for performing the function, the
8 following terms are invalid as indefinite under 35 U.S.C. §§ 112, ¶ 2:

- 9 • "an identification component that identifies a packet type of a packet of symbols" (claim
10 19)
- 11 • "a transmission component that transmits a synchronization symbol that corresponds to the
12 identified packet type . . . and that transmits the symbols of the packet" (claim 19)

13 The indefiniteness issues identified above apply to all claims that include the identified
14 limitations, either explicitly or through claim dependency, and are not limited to the exemplary
15 claims listed above.

16 **VI. THE ASSERTED CLAIMS OF THE '265 PATENT ARE INVALID**

17 **A. Identification of Prior Art**

18 Defendant contends that the prior art references charted in Exhibits D-1 through D-12,
19 discussed in any incorporated IPR petition, discussed or cited in the prosecution history and/or any
20 reexamination proceedings, and/or described below anticipate and/or render obvious, alone or in
21 combination, one or more of the Asserted Claims of the '265 Patent.

22 **1. The '265 Patent Claims Are Anticipated by the Prior Art**

23 Some or all of the Asserted Claims of the '265 Patent are invalid as anticipated under 35
24 U.S.C. § 102 in view of each of the prior art references identified in the claim charts included in
25 Exhibit D-1 through D-12 and/or identified in any incorporated IPR petition, which identify specific
26 examples of where each limitation of the Asserted Claims is found in the prior art references. As
27 explained above, the cited portions of prior art references identified in the attached claim charts are
28 exemplary in nature and representative of the content and teaching of the prior art references, and

1 should be understood in the context of the reference as a whole and as they would be understood by
2 a person of ordinary skill in the art.

3 In addition to references identified in any incorporated IPR petition, Defendant identifies the
4 following references as anticipating one or more of the Asserted Claims of the '265 Patent under 35
5 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an
6 admission that any reference not listed below does not also anticipate the claims of the '265 Patent.
7 Further, Defendant contends that any prior art reference in the attached charts that is charted for
8 each limitation of any given claim, anticipates that claim, regardless of whether that prior art
9 reference is listed in the following tables.

10 **a) Prior Art Patents and Applications⁴**

Number	Published/Issued Date	Short Name	Exhibit Number
JP 2009060204 A	Filed: Aug. 30, 2007 Pub'd: Mar. 19, 2009	Iwamoto	D-1
U.S. Patent Publ. No. 2009/0046690 A1	Filed: Aug. 16, 2007 Pub'd: Feb. 19, 2009	Hsieh	D-2
U.S. Patent Publ. No. 2008/0028237 A1	Filed: Jul. 26, 2006 Pub'd: Jan. 31, 2008	Knight	D-3

17 **b) Prior Art Publications**

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
HDMI Founders	High-Definition Multimedia Interface Specification Version 1.4	Jun. 5, 2009	HDMI 1.4	D-4

22 **c) Prior Art Systems**

23 On information and belief, systems implementing the protocols identified below were in
24 public use, on sale, or otherwise available to the public before the priority date of the '265 Patent.

26 ⁴ Where the accompanying charts cite a particular drawing or figure, the citation encompasses the
27 description of the drawing or figure, as well as any text associated with the drawing or figure
28 (even if the associated text is not by itself expressly cited). Similarly, where the accompanying
charts cite particular text concerning a drawing or figure, the citation also encompasses that
drawing or figure (even if the associated drawing or figure is not expressly cited).

Defendant's further investigation and/or subsequent discovery from Plaintiff or third parties with knowledge regarding prior art systems may reveal additional relevant prior art systems and/or further information regarding the systems identified below, or other relevant prior art systems. Defendant reserves the right to supplement these Invalidity Contentions, based on subsequent investigation and discovery, including from third parties.

System	Available At Least As Of	Short Name	Exhibit Number
Systems employing High-Definition Multimedia Interface (HDMI) 1.4	Jun. 5, 2009	HDMI 1.4	D-4
Systems employing Universal Serial Bus (USB) On-the-Go (OTG)	Jun. 24, 2003	USB OTG	D-6
Systems employing Universal Serial Bus Specification, Revision 2.0	Apr. 27, 2000	USB 2.0	D-10
Systems employing DisplayPort 1.2 Specification	Jan. 5, 2010	DisplayPort 1.2	D-11
Devices implementing FireWire System based on IEEE 1394	1996	Firewire	D-12

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the '265 Patent, Defendant contends that any difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

d) Other Relevant References

Defendant reserves the right to rely on the prior art references identified in connection with one of the other Asserted Patents in connection with the '265 patent. In addition, Defendant hereby cites the following additional references as being relevant to the subject matter claimed in the '265 patent. Defendant is producing concurrently herewith a number of such references that are relevant

to the validity of the Asserted Patents, the state of the art, and as evidencing a motivation to combine various references. Defendant reserves the right to rely on one or more of the references produced concurrently herewith as anticipatory references under 35 U.S.C. § 102, as further evidence of obviousness under 35 U.S.C. § 103, as background references demonstrating the state of the art, as a limitation upon the doctrine of equivalents, or for any other purpose. Based on further investigation and discovery, based on positions that Plaintiff may take regarding the scope of the asserted claims, and/or based on the Court's claim construction (once issued), Defendant reserves the right to revise these contentions and to rely on these references to prove the invalidity of the '265 patent in a manner consistent with this Court's Rules and with the Federal Rules of Civil Procedure.

a) Prior Art Patents and Applications

Number	Published/Issued Date
U.S. Pat. No. 7,480,758	Filed: Mar. 7, 2007 Pub'd: Sep. 11, 2008 Issued: Jan. 20, 2009
WO 2010067243 A1	Filed: Nov. 24, 2009 Pub'd: Jun. 17, 2010
U.S. Patent Publ. No. 2003/0229749 A1	Filed: Mar. 4, 2003 Pub'd: Dec. 11, 2003
U.S. Pat. No. 9,274,739	PCT Filed: Apr. 17, 2009 PCT Pub'd: Oct. 21, 2010 Filed: Dec. 16, 2011 Issued: Mar. 1, 2016
U.S. Patent Publ. No. 2007/0242062 A1	Filed: Apr. 18, 2006 Pub'd: Oct. 18, 2007
U.S. Patent Publ. No. 2009/0179883 A1	Prov.: Jan. 15, 2008 Filed: Apr. 21, 2008 Pub'd: Jul. 16, 2009
U.S. Patent Publ. No. 2010/0183004 A1	Prov.: Jan. 16, 2009, Apr. 23, 2009, May 13, 2009 Filed: Jun. 15, 2009 Pub'd: Jul. 22, 2010
U.S. Patent Publ. No. 2014/0092305 A1	Priority: Dec. 17, 2007 Filed: Dec. 4, 2013 Pub'd: Apr. 3, 2014
JP 1992368666 A	Filed: Jun. 18, 1991 Pub'd: Dec. 21, 1992
JP 2001086416 A	Filed: Sep. 13, 1999 Pub'd: Mar. 30, 2001
U.S. Pat. No. 8,185,669	Filed: Jul. 10, 2007 Pub'd: May 1, 2008 Issued: May 22, 2012
U.S. Pat. No. 8,841,886	Filed: Sep. 9, 2010

	Pub'd: Mar. 24, 2011 Issued: Sep. 23, 2014
U.S. Pat. No. 9,124,853	Filed: Nov. 30, 2010 Pub'd: May 31, 2012 Issued: Sep. 1, 2015
U.S. Pat. No. 9,900,653	Priority: Mar. 5, 2009 Filed: Nov. 8, 2016 Pub'd: Feb. 23, 2017 Issued: Feb. 20, 2018
U.S. Patent Publ. No. 2008/0126591 A1	Filed: Nov. 13, 2007 Pub'd: May 29, 2008
U.S. Patent Publ. No. 2009/0177818 A1	Filed: Jan. 4, 2008 Pub'd: Jul. 9, 2009
U.S. Patent Publ. No. 2011/0063501 A1	Filed: Sep. 14, 2009 Pub'd: Mar. 17, 2011

b) Prior Art Publications

Author or Publisher	Title	Publication/Use Date
IEEE Computer Society	802.3af IEEE Standard for Information Technology	Jun. 18, 2003
IEEE Computer Society	1394b IEEE Standard for High-Performance Serial Bus-Amendment 2	Dec. 14, 2002

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the '265 Patent, Defendant contends that any difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

2. The '265 Patent Claims Are Obvious Over the Prior Art

To the extent Plaintiff argues that any limitation of the asserted claims of the '265 Patent are not explicitly disclosed by an item of prior art identified above, in Exhibits D-1 through D-12, or discussed in any incorporated IPR petition, any purported differences are such that the claimed

1 subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged
2 invention, in view of the state of the art and knowledge of those skilled in the art. The item of prior
3 art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

4 It would have been obvious to combine any of the prior art in Exhibits D-1 through D-12
5 with each other, at least because all of these references relate to methods and apparatuses for
6 communicating audio/visual data between a source and a sink, and/or methods and apparatuses for
7 communicating audio/visual data using a source/sink dual purpose device. The charted references
8 may further disclose methods for a source/sink dual purpose device to transition between source and
9 sink modes.

10 For example, JP 2009060204 A to Iwamoto (“Iwamoto”) teaches a “source/sink dual-
11 purpose device conforming to the HDMI standard” that can function as a source device or a sink
12 device. Iwamoto at [0016]-[0017]. The device includes a first voltage level monitor for detecting
13 the voltage level of the power line of an HDMI cable (VL1), and a second voltage level monitor for
14 detecting the voltage level of a TMDS_CLK line of the HDMI cable (VL2). Iwamoto at [0016].
15 The device uses these measurements to determine whether a connected device is a source or sink,
16 and to “automatically switch[] its own functions” accordingly. Iwamoto’s device has several modes
17 depending on VL1 and VL2. Iwamoto at [0027], Figs. 2, 3. When VL1 and VL2 are low, the dual-
18 purpose device determines that it is not connected to a second device, and operates in standby mode.
19 *Id.* at [0043]-[0044], [0072]-[0073], Fig. 3. When VL1 is high (5 V) and VL2 is low, the dual-
20 purpose device determines that the connected device is a source, and operates in sink mode. *Id.* at
21 [0043]-[0045], [0075], [0076], Fig. 3. When VL1 is low and VL2 is high (3.3 V), the dual-purpose
22 device determines that the connected device is a sink and operates in source mode. *Id.* The switching
23 process is accomplished by HDMI attribute switching processing unit 180, which outputs control
24 signals Sc1-Sc4 to power supply block 120, DDC block 140, hot plug block 130, and TMDS block
25 150 to control the device’s functions based on its operating mode. *Id.* at [0056], Fig. 1.

26 U.S. Patent App. Pub. No. 2009/0046690 A1 to Hsieh (“Hsieh”) discloses a bi-directional
27 high speed digital interface (“HSDI”) transceiver, which may be an HDMI device. Hsieh at [0001]-
28 [0004]. Hsieh explains that the device can switch its function to make itself compatible to a typical

1 source or sink, or “form a bi-directional HSDI structure coupled with another HSDI transceiver with
2 bi-directional functionality.” *Id.* at [0035]. In other words, “the first HSDI transceiver acts as a
3 source device if the interface is coupled to [a sink], and the first HSDI transceiver acts as a sink
4 device if the interface is coupled to [a source].” *Id.* at [0006]. Hsieh further teaches that “the first
5 HSDI transceiver is pre-set to be either the source device or the sink device,” and “can be chosen to
6 act as a source device or a sink device depending on the user’s requirement.” *Id.* at [0006], [0106].
7 For example, when the HSDI transceiver is a DVD recorder (typically used as a source), the default
8 function of the device is to act as a source device.” *Id.* at [0016]. Hsieh explains that the device is
9 initially set to its default function before detecting whether another device is connected. *Id.* at
10 [00176]-[0018], Fig. 3. If the attached device has the same default function, the HSDI transceiver
11 “is unable to detect the plugged-in . . . HSDI device.” *Id.* at [0017]. To overcome this issue, the
12 HSDI transceiver may toggle its function to “act as the source device and the sink device alternately”
13 in order to match with and connect to the attached device. *Id.* at [0017], [0020]; *see also* FIG. 3.

14 U.S. Patent App. Pub. No. 2008/0028237 A1 to Knight (“Knight”) also discloses a device
15 “capable of communicating power and data through a single connector to another device,” where
16 the device may be configured as a source or sink. Knight at [0024], [0039]-[0040]. Knight teaches
17 that the device may connect to multiple other devices and enable communication between them
18 according to PoE, Firewire, USB, or similar communication protocols. *Id.* at [0031]-[0032], [0001],
19 [0024]. Fig. 1 of Knight illustrates one embodiment of the system 100 including a first device 102
20 connected to remote devices 138, 140, 142, and 144 via interfaces that allow the devices to transfer
21 power and data. *Id.* at [0022], [0024], Fig. 1. The first device includes a battery 126 that may provide
22 power to, or be charged by, the remote devices. *Id.* at [0025]-[0027], [0029]. The power management
23 system 124 controls the flow of power and “may receive power from one or more of the remote
24 devices, distribute power to other remote devices, and charge or discharge the battery bank 126 as
25 appropriate.” *Id.* at [0029]. The system of Knight may follow the power management method 200
26 in Fig. 2. *Id.* at [0039]. According to that method, when a connection is made, the device “may be
27 configured to attempt to connect as a power sink initially, then attempt[] as a power source
28

1 secondarily.” *Id.* The sink/source negotiation process “may be through sensing status and
2 communicating through the power connections.” *Id.* at [0047].

3 The High-Definition Multimedia Interface Specification Version 1.4 (“HDMI 1.4”)
4 discloses an interface for “transmitting digital television audiovisual signals from DVD players, set-
5 top boxes and other audiovisual sources to television sets, projectors and other video displays.”
6 HDMI 1.4 at 1. HDMI 1.4 was incorporated into many devices. For example, Samsung’s HW-
7 D7000 entertainment system featured a combined Blue-ray player and A/V receiver. The
8 specification of HDMI 1.4 describes the “[m]echanical, electrical, behavioral and protocol
9 requirements necessary for compliance...for sources, sinks and cables.” *Id.* HDMI 1.4 explains that
10 the “HDMI system architecture is defined to consist of Sources and Sinks,” where “[e]ach HDMI
11 input...shall follow all of the rules for an HDMI Sink and each HDMI output shall follow all of the
12 rules for an HDMI Source.” *Id.* at 9. The specification further teaches that “[t]he HDMI connector
13 provides a pin allowing the Source to supply +5.0 Volts to the cable and Sink,” where “[a] Sink
14 shall assume that any voltage within the range specified for TP2 voltage in Table 4-34 indicates that
15 a Source is connected and applying power to the +5V Power signal.” *Id.* at 71. Once a sink detects
16 the +5V power line, it may assert the hot plug detect pin. *Id.* at 153. “A Source shall assume that
17 any voltage [on the hot plug detect pin] within the range specified for High voltage level in Table
18 4-39 indicates that a Sink is connected.” *Id.* at 153. The HDMI 1.4 specification further teaches that
19 HDMI sources and sinks, “upon power-up, reset, or detection of a new [] device,” shall assume that
20 the connected device is not HDMI-capable. *Id.* at 166-167. Once it is determined that the connected
21 device is HDMI-capable, the HDMI sink or source follows all HDMI requirements in the
22 specification. *Id.*

23 USB Implementers Forum, *On-The-Go Supplement to the USB 2.0 Specification, Revision*
24 *1.0a* (“USB OTG Supplement”) teaches that “USB has become a popular interface for exchanging
25 data between PC’s and peripherals. An increasing number of portable peripherals are using the USB
26 interface to communicate with the PC. Many of these portable devices would benefit from being
27 able to communicate to each other over the USB interface, yet certain aspects of USB make this
28 difficult to achieve.” USB OTG Supplement at 1. The USB OTG Supplement further teaches that

1 “this supplement to the USB 2.0 specification was developed that allows a portable device to take
2 on the role of a limited USB host, without the burden of supporting all the above functions of a PC.”
3 *Id.* The Samsung Yepp YP-D1 (“YP-D1”) was an MP3 player released by Samsung on February
4 14, 2006. It is a device equipped with USB OTG functionality, used to connect the device to other
5 devices such as computers, tablets, and cellular phones.

6 Universal Serial Bus Specification, Revision 2.0, April 27, 2000 (“USB 2.0”). USB 2.0
7 provides for packet-based, half-duplex bidirectional data communication over a single differential
8 pair of wires. Although USB 2.0 is intended for communicating a range of different data types, one
9 stated goal of USB 2.0 was to provide “[f]ull support for real-time data for voice, audio, and video.”
10 USB 2.0 at 11. Different classes of USB 2.0 devices are capable of different functions; one example
11 is the video class (discussed in more detail below). Various systems had employed the USB 2.0
12 functionality prior to the priority date of the ’265 Patent.

13 The Video Electronics Standards Association (VESA) DisplayPort Standard Version 1,
14 Revision 2 (“DisplayPort 1.2”) “define[s] a flexible system and apparatus capable of transporting
15 video, audio and other data between a Source Device and a Sink Device over a digital
16 communications interface.” DisplayPort 1.2 at 1. A DisplayPort link as defined in DisplayPort 1.2
17 “consists of a main link, an auxiliary channel (AUX CH), and a Hot Plug Detect (HPD) signal line.”
18 *Id.* at 34. “[T]he Main Link is a unidirectional, high-bandwidth and low-latency channel used to
19 transport isochronous data streams such as uncompressed video and audio. The auxiliary channel is
20 a half-duplex bidirectional channel used for link management and device control. The HPD signal
21 also serves as an interrupt request by the Sink device.” *Id.* Moreover, DisplayPort 1.2 included a
22 Fast AUX capability, which allowed bidirectional communication of USB 2.0 data over the AUX
23 channel. *Id.* at 20. Upon information and belief, example systems using DisplayPort 1.2 include
24 Apple’s MacBook Pro (Early 2011) sold or offered for sale in the United States by at least February
25 28, 2011.

26 IEEE 1394-1995 (“Firewire”) was a high-speed peer-to-peer serial interface standard. The
27 Firewire connector included six wires, including two signal pairs and one power pair. Firewire
28 included the use of tokens during configuration, arbitration, and data transmission. Additional

1 information about the operation of prior art systems implementing Firewire can be found in the
2 following documents:

- 3 • Michael Johas Teener, “Technical Introduction to IEEE 1394” (2004),
4 www.ieee802.org/802_tutorials/04-July/NewTechIntroTo1394.pdf
- 5 • John Canosa, “Fundamentals of Firewire™,” Questra Consulting,
6 <https://public.ostfalia.de/~bermbach/research/firewire/files/basics.pdf>

7 Accordingly, because each of the identified references are directed to similar devices in the
8 similar field of endeavor, a person of ordinary skill in the art would be motivated to combine the
9 teachings of two or more references together because the references disclose similar systems that
10 solve the same problems in similar ways. Thus, it would have been obvious to one of ordinary skill
11 in the art to combine any of the foregoing references and one of ordinary skill would have expected
12 such a combination to be successful.

13 To the extent that it is determined that any of the above references do not disclose a particular
14 claim element, it would have been obvious to modify the teachings of that reference to include such
15 element as taught in any other of the above references that discloses such element (as documented
16 in the claim charts attached as D-1 through D-12).

17 For example, to the extent that it is determined that any of the above references do not
18 disclose “initializing a first audio/video (AV) device to operate in a default AV sink operation mode
19 in response to a power-on-reset or powering up” and/or “the AV sink operation mode being a default
20 mode of operation for the AV device,” as recited in claim 1 and in similar form in claims 8 and 14,
21 it would have been obvious to modify the teachings of that reference to include these features in
22 view of the knowledge of a POSITA and the teachings of at least these features in at least the
23 following references and systems: *See, e.g.,* Iwamoto, Hsieh, Knight, HDMI 1.4, USB OTG, and/or
24 DisplayPort 1.2. For example, Iwamoto teaches a dual-purpose source/sink device that is in a
25 “standby” mode when disconnected. Iwamoto at [0052]. Hsieh teaches an HDMI device that can
26 switch between source and sink mode. Hsieh at [0006] and [0016]. Knight teaches an AV device
27 that may first attempt to connect as a sink, then attempt to connect as a source. Knight at [0048].
28 The HDMI 1.4 specification explains that HDMI sources and sinks default to particular settings

1 upon power-up, reset or detection of a new [] device.” HDMI 1.4 at 166-167. Therefore, a person
2 of ordinary skill in the art would be motivated to make such a modification and/or combination.

3 To the extent that it is determined that any of the above references do not disclose
4 “determining whether a first supply voltage is provided at a channel of a connector;” “in response
5 to determining that the first supply voltage is provided at the channel of the connector, configuring
6 communication logic of the first AV device to continue operating the first AV device in the AV sink
7 operation mode;” and/or “in response to determining that the first supply voltage is not provided at
8 the channel of the connector, configuring the communication logic of the first AV device to
9 transition the first AV device from the AV sink operation mode to an AV source operation mode;”
10 as recited in claim 1 and in similar form in claims 8 and 14, it would further have been obvious to
11 modify the teachings of that reference to include these features in view of the knowledge of a
12 POSITA and the teachings of at least Iwamoto and HDMI 1.4.

13 One of skill in the art, seeking to solve these problems, would have looked to analogous art
14 to identify ways to solve the problem. Indeed, the solution identified by the patentee had already
15 been identified by others in the field, and one of ordinary skill in the art would have been motivated
16 to combine such analogous teachings in the same manner proposed by the patentee. Additionally,
17 one of skill in the art would have had a reasonable expectation of success because the references
18 contained analogous teachings to those proposed by the patentee, the references describe relatively
19 simple electrical technologies in predictable fields, and the modifications and combinations would
20 not require undue experimentation. As such, one of skill would have been motivated to combine the
21 references.

22 Thus, in addition to the combinations discussed above, exemplary combinations which
23 render obvious some or all of the Asserted Claims of the ’265 Patent are listed in **Appendix A**, Sec.
24 IV.

25 **B. Invalidity of the ’265 Patent Based on 35 U.S.C. § 112, ¶ 2**

26 Based on Defendant’s present understanding of Plaintiff’s asserted scope of the claims of
27 the ’265 Patent, to the extent such positions can be understood from Plaintiff’s Infringement
28

1 Contentions, Defendant asserts that one or more of the Asserted Claims of the '265 Patent are invalid
2 for reciting at least the following claim terms, phrases, or limitations:

- 3 • **“the default operation mode” (claim 11):** This term is inconsistent with the language of
4 independent claim 8 from which claim 11 depends. For example, claim 8 recites “AV sink
5 operation mode” and “default AV sink operation mode,” but not “a default operation
6 mode.” The term is unclear as to whether it refers to “AV sink operation mode” or
7 “default AV sink operation mode,” or is altogether a new element.

8 These claim terms, phrases, limitations, and all dependent claims thereof, as apparently
9 construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112 at least because they
10 fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

11 Based on Defendant’s present understanding of Plaintiff’s Infringement Contentions, at least
12 one or more of these claim terms, phrases, and limitations are indefinite because they are
13 inconsistent with and broader than the alleged invention disclosed in the specification and during
14 prosecution, and given Plaintiff’s apparent constructions of the claims, a person of ordinary skill in
15 the art at the time of the invention would not understand what is claimed with reasonable certainty,
16 even when the claims are read in light of the specification and prosecution history.

17 Additionally, Claims 8, 11, and 14 of the '265 Patent are invalid under 35 U.S.C. §§ 112 ¶ 6
18 because the '265 Patent does not disclose sufficient structure corresponding to the function recited
19 in at least the following means-plus-function claim limitations:

- 20 • “communication logic to couple to a connector...” (claim 8)
- 21 • “circuitry configured to implement...” (claim 8)
- 22 • “control logic including circuitry to configure the communication logic...” (claim 8)
- 23 • “detector logic to detect...” (claim 11)
- 24 • “communication logic” (claim 14)
- 25 • “circuitry configured to implement...” (claim 14)
- 26 • “control logic including circuitry to configure the communication logic...” (claim 14)

1 The indefiniteness issues identified above apply to all claims that include the identified
2 limitations, either explicitly or through claim dependency, and are not limited to the exemplary
3 claims listed above.

4 **VII. THE ASSERTED CLAIMS OF THE '712 PATENT ARE INVALID**

5 **A. Identification of Prior Art**

6 Defendant contends that the prior art references charted in Exhibits E-1 through E-20,
7 discussed in any incorporated IPR petition, and/or described below anticipate and/or render obvious,
8 alone or in combination, one or more of the Asserted Claims of the '712 Patent.

9 **1. The '712 Patent Claims Are Anticipated by the Prior Art**

10 Some or all of the Asserted Claims of the '712 Patent are invalid as anticipated under 35
11 U.S.C. § 102 in view of each of the prior art references identified in the claim charts included in
12 Exhibit E-1 through E-20 and/or identified in any incorporated IPR petition, which identify specific
13 examples of where each limitation of the Asserted Claims is found in the prior art references. As
14 explained above, the cited portions of prior art references identified in the attached claim charts are
15 exemplary in nature and representative of the content and teaching of the prior art references, and
16 should be understood in the context of the reference as a whole and as they would be understood by
17 a person of ordinary skill in the art.

18 In addition to references identified in any incorporated IPR petition, Defendant identifies the
19 following references as anticipating one or more of the Asserted Claims of the '712 Patent under 35
20 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an
21 admission that any reference not listed below does not also anticipate the claims of the '712 Patent.
22 Further, Defendant contends that any prior art reference in the attached charts that is charted for
23 each limitation of any given claim, anticipates that claim, regardless of whether that prior art
24 reference is listed in the following tables.

25 **a) Prior Art Patents and Applications**

Number	Published/Issued Date	Short Name	Exhibit Number
U.S. Pat. App. Pub. No. 2006/0089230 A1	Filed: Oct. 7, 2004 Pub'd: Apr. 27, 2006	Biederman	E-1

1	U.S. Pat. App. Pub. No. 2006/0100799 A1	Filed: Nov. 5, 2004 Pub'd: May 11, 2006	Karam '799	E-2
2	U.S. Pat. App. Pub. No. 2008/0168283 A1	Filed: Jan. 5, 2007 Pub'd: Jul. 10, 2008	Penning	E-3
3	U.S. Pat. App. Pub. No. 2006/0273661 A1	Filed: Jun. 2, 2005 Pub'd: Dec. 7, 2006	Toebe	E-4
4	U.S. Patent App. Pub. No. 2008/0028237 A1	Filed: Jul. 26, 2006 Pub'd: Jan. 31, 2008	Knight	E-5
5	U.S. Pat. App. Pub. No. 2005/0268120 A1	Filed: May 13, 2004 Pub'd: Dec. 1, 2005	Schindler	E-6
6	U.S. Pat. App. Pub. No. 2006/0210057 A1	Filed: Jan. 23, 2006 Pub'd: Sep. 21, 2006	Stanford	E-7
7	U.S. Pat. App. Pub. No. 2006/0218420 A1	Prov.: Mar. 28, 2005 Filed: Nov. 23, 2005 Pub'd: Sep. 28, 2006	Camagna	E-8
8	U.S. Pat. App. Pub. No. 2008/0250255 A1	Filed: Apr. 6, 2007 Pub'd: Oct. 9, 2008	Diab '255	E-9
9	U.S. Pat. App. Pub. No. 2008/0016263 A1	Prov.: Jun. 28, 2006 Filed: Jun. 26, 2007 Pub'd: Jan. 17, 2008	Diab '263	E-10
10	U.S. Pat. App. Pub. No. 2006/0168459 A1	Filed: Nov. 15, 2005 Pub'd: Jul. 27, 2006	Dwelley	E-11
11	U.S. Pat. App. Pub. No. 2008/0235523 A1	Prov. Mar. 20, 2007 Filed: Mar. 20, 2008 Pub'd: Sep. 25, 2008	Hussain	E-12
12	U.S. Pat. App. Pub. No. 2007/0220280 A1	Filed: Mar. 14, 2006 Pub'd: Sep. 20, 2007	Karam '280	E-13
13	U.S. Pat. App. Pub. No. 2008/0005598 A1	Filed: Jun. 30, 2006 Pub'd: Jan. 3, 2008	Landry	E-14
14	U.S. Pat. App. Pub. No. 2005/0044431 A1	Filed: May 24, 2004 Pub'd: Feb. 24, 2005	Lang	E-15
15	U.S. Pat. App. Pub. No. 2007/0278857 A1	Filed: Oct. 6, 2006 Pub'd: Dec. 6, 2007	Robbins	E-16

b) Prior Art Publications

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
IEEE Computer Society	802.3af-2003 IEEE Standard for Information Technology	Jun. 18, 2003	IEEE 802.3af	E-17
Maxim Integrated Products	+48V, Single-Port Network Power Switch For Power-Over-LAN	Apr. 2003	MAX5922	E-18

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
Texas Instruments	IEEE 802.3af Power Interface Switch For Power Over Ethernet (PoE) Powered Devices	Mar. 2004	TPS2370	E-19

c) Prior Art Systems

On information and belief, the systems identified below and the systems implementing the protocols identified below were in public use, on sale, or otherwise available to the public before the priority date of the '712 Patent. Defendant's further investigation and/or subsequent discovery from Plaintiff or third parties with knowledge regarding prior art systems may reveal additional relevant prior art systems and/or further information regarding the systems identified below, or other relevant prior art systems. Defendant reserves the right to supplement these Invalidity Contentions, based on subsequent investigation and discovery, including from third parties.

System	Available At Least As Of	Short Name	Exhibit Number
Systems employing On-The-Go Supplement to the USB 2.0 Specification Revision 1.0a	June 24, 2003	USB-OTG 1.0a	E-20

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the '712 Patent, Defendant contends that any difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

d) Other Relevant References

Defendant reserves the right to rely on the prior art references identified in connection with one of the other Asserted Patents in connection with the '712 patent. In addition, Defendant hereby

1 cites the following additional references as being relevant to the subject matter claimed in the '712
2 patent. In addition to these references, Defendant is producing concurrent herewith a number of
3 other references that are relevant to the validity of the Asserted Patents, the state of the art, and as
4 evidencing a motivation to combine various references. Defendant reserves the right to rely on one
5 or more of the references produced concurrently herewith as anticipatory references under 35 U.S.C.
6 § 102, as further evidence of obviousness under 35 U.S.C. § 103, as background references
7 demonstrating the state of the art, as a limitation upon the doctrine of equivalents, or for any other
8 purpose. Based on further investigation and discovery, based on positions that Plaintiff may take
9 regarding the scope of the asserted claims, and/or based on the Court's claim construction (once
10 issued), Defendant reserves the right to revise these contentions and to rely on these references to
11 prove the invalidity of the '712 patent in a manner consistent with this Court's Rules and with the
12 Federal Rules of Civil Procedure.

13 **i. Prior Art Patents and Applications**

Number	Published/Issued Date
U.S. Pat. App. Pub. No. 2009/0222678	Filed: Feb. 29, 2008 Pub'd: Sep. 3, 2009
WO 2006/126160 A1	Filed May 22, 2006 Pub'd: Nov. 30, 2006
U.S. Patent No. 6,496,103	Filed: Feb. 4, 2000 Issued: Dec. 17, 2002
U.S. Patent No. 6,535,983	Filed: Nov. 8, 1999 Issued: Mar. 18, 2003

19 **ii. Prior Art Publications**

Author or Publisher	Title	Publication/Use Date
USB-IF	Universal Serial Bus Specification, Revision 2.0	Apr. 27, 2000
IEEE Computer Society	1394b IEEE Standard for High-Performance Serial Bus- Amendment 2	Dec. 14, 2002
Roger Karam	Power Classification for the PD	Sep. 29, 2003
Maxim Integrated Products	IEEE 802.3af PD Interface Controller for Power-Over- Ethernet	Feb. 2006
Maxim Integrated Products	Quad Network Power Controller for Power-Over- LAN	Sep. 2005

Galit Mendelson	All You Need to Know About Power over Ethernet (PoE) and the IEEE 802.3af Standard	Jun. 2004
USB Implementers Forum	USB 2.0 Specification, Revision 1.0a ("USB OTG 1.0a")	Jun. 2003

2. The '712 Patent Claims Are Obvious Over the Prior Art

To the extent Plaintiff argues that any limitation of the asserted claims of the '712 Patent is not explicitly disclosed by an item of prior art identified above, in Exhibits E-1 through E-20, or discussed in any incorporated IPR petition, any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. The item of prior art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

It would have been obvious to combine any of the prior art in Exhibits E-1 through E-20 with each other, at least because all of these references relate to systems and methods for delivering power to devices connected in a network via Power over Ethernet ("PoE"), including means for detecting connected devices and determining their power requirements. Several of these references are specifically directed to the provision of power to devices connected in a daisy-chain configuration.

a) The PoE Standard

PoE is governed by the 802.3af-2003 IEEE Standard for Information Technology ("IEEE 802.3af"). The IEEE 802.3af standard "defines the functional and electrical characteristics of...a Powered Device (PD) and Power Sourcing Equipment (PSE)," which "allow devices to supply/draw power using the same generic cabling as is used for data transmission." IEEE 802.3af at 27. The standard provides "[a] protocol allowing the detection of a device that requires power," "a method to classify devices based on their power needs," and "[a] method for scaling supplied power back to the detect level when power is no longer requested or required." *Id.* The PSE's "main functions are to search the link section for a PD, optionally classify the PD, supply power to the link section (only if a PD is detected), monitor the power on the link section, and scale power back to the detect level when power is no longer requested or required." *Id.* at 29. One example of when power is no

1 longer required is “[a]n unplugged link section.” *Id.* A PSE may also detect a PD but opt not to
2 power it. *Id.* at 37. A PD “is a device that is either drawing power or requesting power by
3 participating in the PD detection algorithm.” *Id.* at 49. A PD may be able to draw power from an
4 alternate source, in which case the PD may not require power from the PSE. *Id.*

5 During the detection process, the PSE checks for a valid signature resistance in the PD. *Id.*
6 at 38-39. The PD “shall present a valid detection signature...while it is in a state where it will accept
7 power” from the PSE. *Id.* at 51. The PD will present a non-valid signature “while it is in a state where
8 it will not accept power” from the PSE. *Id.* A valid PD detection signature is between 23.75K Ω and
9 26.25 K Ω . *Id.* at 52, Table 33-8. IEEE 802.3af provides the Thevenin equivalent of the detection
10 circuit, stating that “PSE requirements are stated for a Thevenin circuit only; they may be

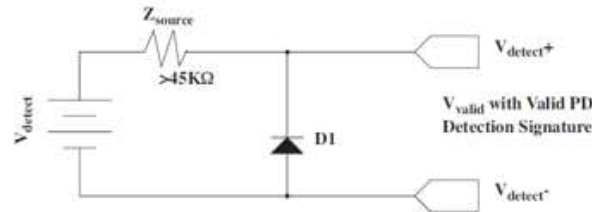


Figure 33-8—PSE detection source

16 transformed via circuit theory into other circuit parameters in specific implementations.” *Id.* at 38,
17 Fig. 33-8. The PSE may detect the signature via “voltage or current measurement.” *See Id.* at 39.
18 The IEEE 802.3af standard explains that this detection process is vital and “should not be
19 overlooked” because, [g]iven the large number of legacy devices (both IEEE 802.3 and other types
20 of devices) that could be connected...and the possible consequences of powering such devices, the
21 protocol to distinguish compatible devices and noncompatible devices is important to prevent
22 damage to non-compatible devices.” *Id.* at 27.

23 After detection, the PSE may classify the maximum power required by the PD during
24 operation. *Id.* at 53. The PSE performs classification of a PD by “applying voltage and measuring
25 current.” *Id.* at 40. “The PSE shall measure I_{Class} and classify the PD based on the observed current
26 according to Table 33-4,” which defines classes 0 through 4 based on current ranges. *Id.* at 40, 53.

IEEE 802.3af further defines the power requirements for each class in Table 33-10; as one example, default class O requires .44 to 12.95 Watts. *Id.* at 53, Table 33-10.

b) Daisy Chained PoE Devices

U.S. Pat. App. Pub. No. 2006/0089230 A1 to Biederman et al. (“Biederman”), U.S. Pat. App. Pub. No. 2006/0100799 A1 to Karam (“Karam ’799”), U.S. Pat. App. Pub. No. 2007/0220280 A1 to Karam et al. (“Karam ’280”), U.S. Pat. App. Pub. No. 2008/0168283 A1 to Penning (“Penning”), U.S. Pat. App. Pub. No. 2006/0273661 A1 to Toebe et al. (“Toebe”), and U.S. Pat. App. Pub. No. 2007/0278857 A1 to Robbins (“Robbins”) are each directed to the provision of power to devices in a daisy chain configuration via PoE. Each reference refers to the IEEE 802.3af standard, and Penning and Robbins explicitly incorporate it by reference.

i. Biederman

Biederman teaches a networked device that “may operate as a powered device (PD) under certain circumstances, may be off for power purposes under other circumstances and may operate as a power Sourcing equipment (PSE) under yet other circumstances.” Biederman at [0033]. In Fig. 2, Biederman illustrates media dependent interfaces (“MDI”) 14a and 14b, each with a PD functional block and a PSE functional block. *Id.* at [0034]. The MDI connected to the PSE has the PD block activated, while the MDI connected to the PD has the PSE block activated. *Id.* Biederman teaches that the PSE portion of the device includes a 48-volt power supply 70 to power a connected PD, and that the device includes a controller for selectively activating the PD block, the PSE block, neither, or both via switching circuitry which may include “diodes, transistors, relays, and the like.” *Id.* at fig. 5, [0038].

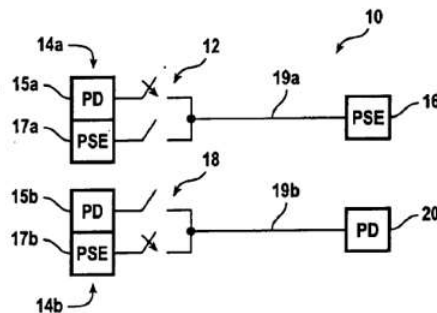


FIG. 2

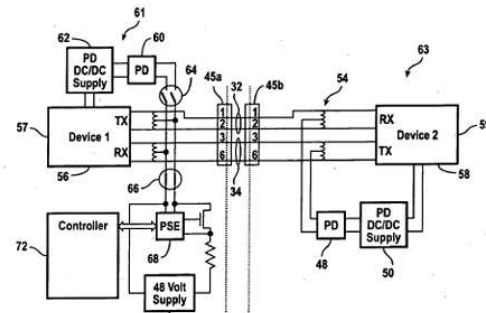
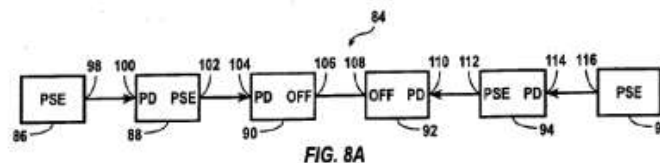


FIG. 5

Biederman at Figs. 2 and 5.

Biederman also teaches that “the power requirements of a PD may change from time to time depending upon how it is used,” so “it would be desirable to adjust the power delivered to the PD from time to time to meet these new requirements, either by increasing the power delivered or decreasing it, as appropriate.” *Id.* at [0042]. Biederman explains that “[a] number of mechanisms are provided by the present invention to accomplish this,” and that “[t]hose of ordinary skill in the art will [] realize that other equivalent mechanisms are available to periodically revise the amount of power made available by the PSE to the PD.” *Id.* at [0042]. As one example, Biederman notes that “[t]here are mechanisms within the IEEE 802.3af standard to allocate a requested amount of power.” *Id.* at [0014].

Finally, Biederman teaches that the combination PD/PSE units may be arranged in a daisy chain configuration to provide redundant data and inline power so that data or power interruption does not occur if the cabling is cut. *Id.* at [0043]-[0045]. In the below example, port 100 of device 88 is configured as a PD to receive power from PSE 826, and port 102 of device 88 is configured as a PSE to send power to device 90. *Id.* at [0044]. When a cable in the chain is cut, the adjacent devices reconfigure themselves—as illustrated below, when devices 88 and 90 are disconnected, port 104 of device 90 is turned off and port 108 of device 92 is turned on and configured to operate as a PSE. *Id.* at [0045].



Biederman at Fig. 8A.

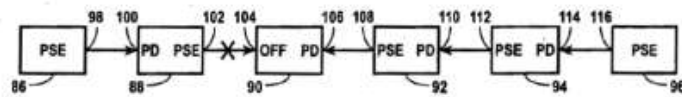


FIG. 8B

Biederman at Fig. 8B.

ii. Karam '799

Karam '799 teaches "a method and apparatus for managing an Inline Power relationship between a network device and a Powered Device (PD) where the network device is acting as power sourcing equipment (PSE) to provide Inline Power to a first PD (PD1) which is, in turn, powering

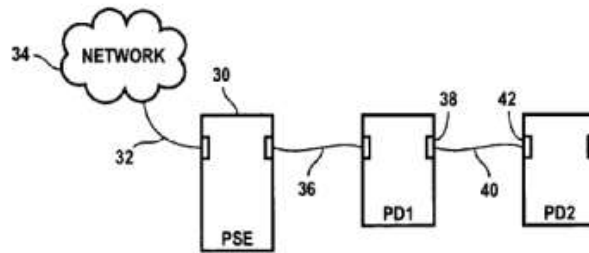


FIG. 2A

another PD (PD2)." Karam '799 at [0039], Fig. 2A. The PSE may also provide power to a longer daisy chain of PD devices. *Id.* at [0046] and Fig. 2D ("In FIG. 2D an arrangement is shown where a PSE provides power and data to three PDs: PD1, PD2 and PD3. This is again accomplished over a series of single 8 conductor (4 pair) cables daisy-chained between the various devices."). The first PD, PD1, receives power from a voltage source in the PSE. *Id.* at [0044].

Karam '799 at Fig. 2A.

Karam '799 explains that "[i]n order to provide regular Inline Power to a PD from a PSE it is a general requirement that two processes first be accomplished. First, a 'discovery' process must be accomplished to verify that the candidate PD is, in fact, adapted to receive Inline Power. Second, a 'classification' process must be accomplished to determine an amount of Inline Power to allocate to the PD, the PSE having a finite amount of Inline Power resources available for allocation to coupled PDs." *Id.* at [0018]. Referencing the IEEE 802.3af standard, Karam '799 explains that the

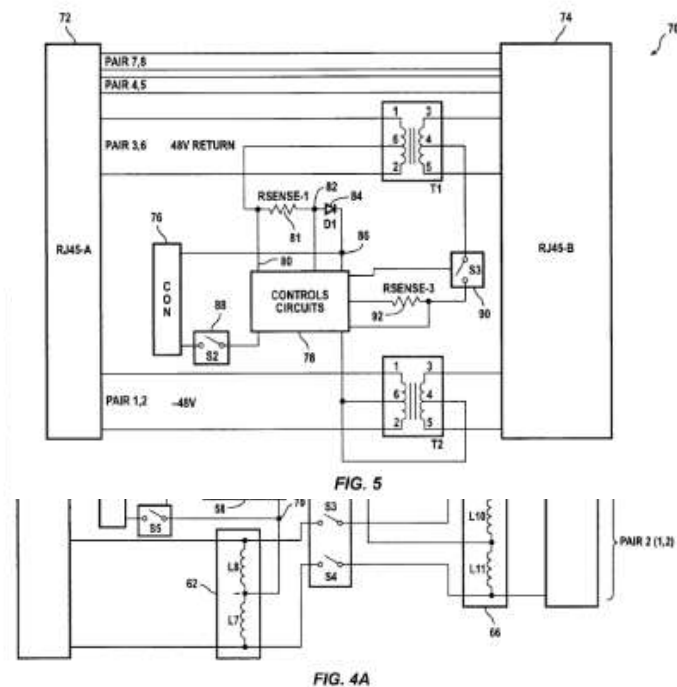
1 discovery process looks for an “identity network” in the PD, which is a 25,000Ω resistor. *Id.* at
2 [0019]. To detect the identity network, the PSE applies voltage discovery signals, measures the
3 “return currents responsive to application of the discovery signals,” and calculates the resistance.
4 *Id.* at [0020]. If the resistance is the proper value, classification may begin. *Id.* Again referencing
5 the IEEE 802.3af standard, Karam ’799 explains that the classification process involves applying a
6 voltage to the PD, which responds by sending a classification current back to the PSE. *Id.* at [0021].
7 This current corresponds to a “class,” which represents a device’s power requirements. *Id.* at [0021],
8 Table I.

9 Karam ’799 teaches that the first PD 50 in the chain includes a connector 52 to connect to
10 the PSE, a second connector 54 which may be coupled to another device, and a third connector 56
11 for providing power to another device, such as a cell phone. *Id.* at [0051], Fig. 4A. Karam ’799
12 explains that, in order to supply power to device 50, “the PSE port must see the proper identity
13 network characteristics,” which, “in accordance with the IEEE 802.3af standard,” is a 25,000Ω
14 resistance in response to “certain discovery voltage signals.” *Id.* Accordingly, the controller 58 of
15 the device 50 provides the identity network signal back to the PSE so that inline power may be
16 provided. *Id.* at [0052]. The device 50 is also adapted to “act as a PSE device to determine if an
17 attached device at a second connector 54 has an appropriate identity network so that inline power
18 may be provided to it.” *Id.* The device 50 senses the identify network via current sensor R2SENSE.
19 *Id.* at Fig. 4A, [0058]. If the device 50 does not verify that the attached device can receive power, it
20 may leave switches S1-S4 open, cutting off data and power to second connector 54. *Id.* Karam ’799
21 further explains that the controller 58 may keep switch S5 to third connector 56 closed “only when
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1 current [is] being drawn from third connector 56 so that if the device were unplugged from third
2 connector 56 the power would turn off.” *Id.* at [0051].

3 Karam ’799 at Fig. 4A.

4 In another, similar embodiment, Karam ’799 teaches that the PD 70 will measure power used
5 by third port 76 using current sensor 81. *Id.* at [0058], Fig. 5. Switch 88, under control of control
6 circuitry 78, provides power to the third port to power an accessory device such as a cell phone. *Id.*
7 Similarly, current sensor 92 measures the power used by second port 74. *Id.* If power is being applied



21 to port 74, and the current sensor 92 detects that the current has gone to zero—i.e., “device at second
22 port 74 is off or disconnected”—control circuitry 78 forces switch 90 closed to “mak[e] sure that a
23 ‘hot cable’ situation is not created at second port 74 by removing the inline power to second port
24 74.” *Id.* To begin providing power again, the control circuitry 78 must identify the appropriate
25 identify network, which may be achieved “by control circuitry 78 reducing the applied voltage and
26 closing switch 90 to carry out a conventional inline power discovery process which may also be
27 followed up by a classification process, if desired in the particular application.” *Id.*

28 Karam ’799 at Fig. 5.

1 **iii. Penning**

2 Penning teaches a system for powering multiple devices connected over a network that may
3 employ PoE network connections. Penning at [0028]-[0030]. The system includes a data distribution
4 device 105, an independent power supply 115, a remote data distribution device 110, network
5 devices 125-1 to 125-N, and externally powered network devices 120-1 to 120-N. *Id.* at [0029], Fig.
6 1. Remote data distribution device 110 acts as a PSE providing data and power to data distribution
7 device 105, which can then provide data and power to network devices 125-1 through 125-N. *Id.*
8 “Data distribution device 105 may sense the amount of power required by one or more network
9 devices 125-1-125-N, and provide power accordingly.” *Id.* Network devices 125-1 through 125-N
10 may also be powered by a local AC/DC wall adapter, instead of data distribution device 105. *Id.* at
11 [0039]-[0040].

12 Data distribution device 105 may power itself and network devices 125-1 through 125-N
13 from one of several power sources, including remote data distribution device 110 and independent
14 power supply 115. *Id.* at [0032]. The device 105 switches between power supplies using “relays,
15 transistors, or any other known switching device.” *Id.* More specifically, as illustrated in Fig. 3,
16 power detectors 350 and 355 of the exemplary data distribution device 205, which may be “voltage
17 or current detectors...of any appropriate type known to one of ordinary skill in the art,” indicate
18 whether power is available from independent power supply 115 or uplink port 350, respectively, by
19 sending a signal to process controller 340. *Id.* at [0049], [0056], Fig. 3. After process controller 340
20 determines which power supply to use, it sends a command signal to switch 380, “which may be a
21 relay, one or more transistors, or any other type of switch which may be controlled by an electronic
22 signal.” *Id.* at [0051], [0047]. If the data distribution device is powered locally by the independent
23 power supply, process controller 340 signals PoE controller 360 to set a signature resistance on
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uplink port 320 in accordance with IEEE 802.3af to inform closet gigabit switch 210 that device 205 does not require power. *Id.* at [0056].

Penning at Fig. 1.

Penning further teaches that the “[p]rocess controller 340 may provide a signal to PoE controller 360 in order to provide feedback to closet gigabit switch 210 regarding how much power to allocate and supply” to data distribution device 205. *Id.* at [0052]. PoE controller 360 may in turn “set up a signature resistance in accordance with IEEE 802.3af, to signal a class 0, 1, 2, and/or 3 power signatures.” *Id.* The closet gigabit switch 210 senses the resistance during initialization to provide the appropriate amount of power. *Id.* Process controller 340 may also “provide control signals to [PSE controller and power controller] PCPC 370 which may include instructions for providing the appropriate amount of power to VOIP telephone 215” according to the 802.3af standard. *Id.* at [0053], Fig. 3; *see also* [0063] (“the VOIP phone may include...a power controller

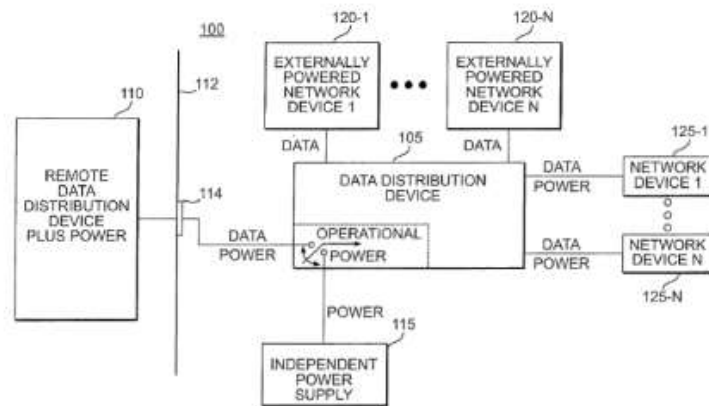


FIG. 1

43 for...designating a power signature for the VOIP phone”); [0068] (“The network device may be provided with hardware circuitry, such as the power controller 435, which designates the power signature of the VoIP phone 400 and all of the associated auxiliary devices” connected to VOIP phone 400.”). After requesting the power signature from VOIP phone 215, which may be class 0, 1, 2, or 3, the process controller may instruct the power controller in PCPC 370 to provide port 315 with the appropriate amount of power for use by VOIP telephone 215.” *Id.* The PSE controller 370

1 may also collect the classification information from the VOIP telephone to send to process controller
2 340 to report back to the closet switch 210 for powering data distribution device 205. *Id.*

3 VOIP telephone may also include a USB port for connecting peripheral devices, as shown
4 in Fig. 4. *Id.* at [0065]. The VOIP phone may include a current sensor to detect the power draw at
5 USB port 415, which is used by process controller 435 to determine the total power consumption
6 for the VOIP phone and any connected peripheral devices. *Id.* at [0065]-[0066]. Each time a
7 peripheral device is connected to or disconnected from VOIP phone 400 and each time the VOIP
8 phone is reset, the controller recalculates the total power available to the VOIP phone and the total
9 power consumption of the VOIP phone and any peripheral devices. *Id.* at [0066], [0067], Fig. 5; *see*
10 *also* [0085] (“[T]he power controller 435 may be configured to scan the auxiliary devices
11 periodically, e.g., every 3 seconds, to recognize each time an auxiliary device has been disconnected
12 from the phone.”). If the total required power is more than the total available power, the user may
13 be prompted to remove the peripheral device. *Id.* The power management process terminates when
14 the power consumption is adequately lowered—i.e., when the user removes the peripheral device.
15 *Id.*

16 **iv. Toebes**

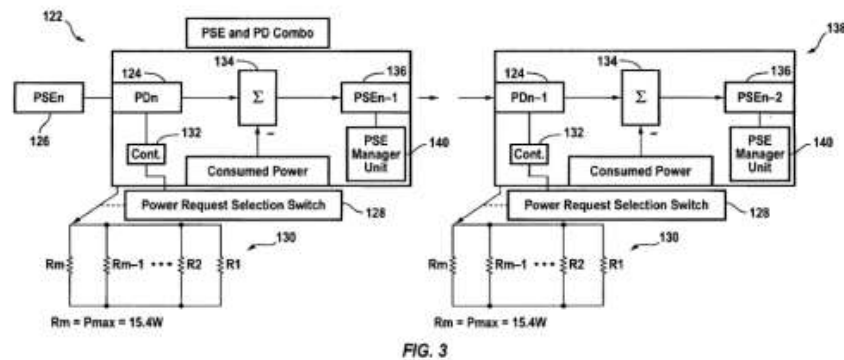
17 Toebes discloses “methods and apparatuses for providing inline power to multiple daisy
18 chained devices in a wired data telecommunications network.” Toebes at [0036]. Toebes explains
19 that “inline power,” also known as PoE, is a “technology for providing electrical power over a wired
20 telecommunications network from power source equipment (PSE) to a powered device (PD) over a
21 link section.” *Id.* at [0015]. In accordance with the IEEE 802.3af standard, Toebes teaches that two
22 processes must be accomplished in order to provide inline power: a discovery process to verify that
23 the PD can receive inline power, and a classification process to determine an amount of power to
24 provide to the PD. *Id.* at [0020].

25 The discovery process looks for an “identity network” at the PD, which “is one or more
26 electrical components which respond in certain predetermined ways when probed by a signal from
27 the PSE.” *Id.* at [0021]. A simple identity network is a resistor, such as the 25,000Ω resistor called
28 for by the IEEE 802.3af standard. *Id.* Toebes further explains that, in order to detect the resistor, the

PSE applies some reduced inline power, measures the “return currents responsive to application of the discovery signals,” and calculates the resistance. *Id.* at [0022]. If the identity network resistance is sensed, then the classification process may begin. *Id.* During classification, the PSE applies a classification-level voltage to the PD, which sends a classification current signal back to the PSE. *Id.* at [0023]. The PSE measures this current, which corresponds to a power “class” of the PD. *Id.* The discovery process prevents full inline power from being provided to “legacy” devices—which are not adapted to receive inline power—and the classification process allows power to be efficiently allocated. *Id.* at [0024]-[0025].

In a basic exemplary configuration taught by Toebe, a POE enabled switch 102 with a PSE port 104 is coupled to a “first PSE-PD combination unit 108,” which includes a first port 110 configured as a powered device (PD) and a second port 112 configured as power sourcing equipment (PSE). *Id.* at [0040], Fig. 2. Port 112 is connected to first port 116 of a second PSE-PD combination unit 18. *Id.* The second port 120 of the second unit is available for connecting to additional devices in the daisy chain. *Id.* As Toebe further explains, the three primary functional blocks of the PSE-PD device are: (1) “[t]he PD component 124 which acts as a PD power request unit to request power from a coupled PSE based on predefined current limits drawn by the PD in the power classification stage;” (2) “the summation unit 134 which sums power values from the PSE 126 with the power consumed;” and (3) the “PSE manager unit 140 which grants (or rejects) PD power requests from PDs coupled to PSE port 136.” *Id.* at [0047].

When the PSE-PD combination unit is first connected to a PSE, it presents a first identity network such as “electrical resistors with certain resistance values corresponding to certain power



1 classes” to the PSE. *Id.* at [0041]. The PD component uses the resistors to request maximum power
2 from the PSE, and the PSE can grant or reject the request. *Id.* If the request is denied, the PD
3 continues requesting less and less power, until the request is granted. *Id.* The granted power value
4 is then presented to summation unit 134 in the PSE-PD combination device, which subtracts the
5 measured or assumed value of the power consumed by the PSE-PD combination device from the
6 granted power. *Id.* at [0044]. The summation unit calculates any leftover power and provides that
7 value to the PSE component 136 of the PSE-PD combination device so that it can be made available
8 to a daisy chained PD unit, such as the second PSE-PD combination unit 138. *Id.* at [0044], Fig. 3.
9 Toebees at Fig. 3.

10 The operation continues with the second PSE-PD combination unit, which has its PD
11 component 124 coupled to PSE component 136 of the first PSE-PD unit. *Id.* at [0049]. PRSS 128
12 of the second PSE-PD combination unit is set by default to select a resistor that requests maximum
13 power from the first PSE-PD combination unit. *Id.* Once the power request is accepted (potentially
14 after several failed requests), the first PSE-PD unit provides inline power to the second PSE-PD
15 unit. *Id.* A new power classification cycle is triggered when the device is rebooted or when there is
16 an interruption in connectivity to the PSE. *Id.* at [0047].

17 **v. Robbins**

18 Robbins is directed to an “inexpensive means to power two PD’s over a single network
19 cable” which “overcome[s] a major disadvantage of conventional PoE systems.” Robbins at [0007].
20 More particularly, Robbins teaches a PoE system with an endspan PSE 21, a midspan PSE 22, a
21 mid-link PD 24, and a standard PD 25. *Id.* at [0023], Fig. 2. The mid-link PD uses power from one
22 of the PSEs and conveys power from the other PSE to another PD in the link—which may be a
23 standard PD or another mid-link PD. *Id.* at [0024]. The advantage of this arrangement is that both
24 PDs can be powered without laying a second network cable. *Id.* at [0025].

25 Rather than explicitly describing the basic components of a IEEE 802.3af compliant device,
26 Robbins explains that “the complex circuitry inside the PSE ports that handles all the functions
27 defined in the IEEE standard (detection, classification, current limiting, PD-disconnect sensing, etc.)
28 are depicted in Fig. 3 as simple voltage source symbols 37 and 41” in mid-link PD 24. *Id.* at [0028].

1 Similarly, Robbins notes that “[t]he PD controller 39 [in mid-link PD 24] handles all the PD
2 functions defined by the IEEE standard (detection, classification, in-rush current limiting, etc.).” *Id.*
3 at [0029].

4 The exemplary mid-link PD illustrated in Fig. 7 includes a first PD controller 60 that outputs
5 a signal 62 to second PD controller 61. *Id.* at [0039], Fig. 7. If the endspan PSE applies power to the
6 mid-link PD, the first PD controller 60 disables second PD controller 61, which causes the controller
7 61 to disable detection and classification functions, stop conducting current to power supply 40, and
8 appear high-impedance to the midspan PSE. *Id.* If the midspan PSE had been providing power to
9 the mid-link PD, the disabled controller 61 will appear to the midspan PSE as an open circuit, and
10 the midspan PSE will discontinue power. When voltage at controller 61 falls to a certain level, the
11 control circuitry closes switch 63—which may be a mechanical or solid-state relay—allowing
12 midspan PSE to detect and power the end-PD. *Id.* at [0039], [0036].

13 **vi. Karam ’280**

14 Karam ’280 is directed to “a method and apparatus for changing power class for a powered
15 device, before or after the device power increases.” Karam ’280 at [0006]. “During operation, a first
16 powered device, such as an IP telephone, receives power from a power source via a PoE device.”
17 *Id.* If a second powered device is connected to the first powered device, “the first powered device
18 transmits a classification signal to the power source.” *Id.* The power source then “performs a
19 powered device classification procedure to reclassify the first powered device, such as according to
20 an IEEE 802.3af standard, and provide an increase amount of power to the first powered device.”
21 *Id.* The first powered device then provides some of that power to the second powered device. *Id.*
22 This configuration is advantageous, as the second powered device “does not require additional
23 equipment in order to operate,” such as “a bulky power cube and cord.” *Id.* at [0006], [0030]. The
24 second device also does not need to be located near an external power supply, such as a wall outlet.
25 *Id.* at [0030].

26 Karam ’280 explains that an exemplary network system includes a power source 12, a first
27 powered device 14, and a second powered device 16. *Id.* at [0020], Fig. 1. The network may provide
28 power to the devices via PoE. *Id.* For example, “the power source 12 exchanges data signals with

1 the first and second powered devices 14, 16 and transmits power signals to the first powered device
2 14 and also to the second powered device 16 via the first powered device 14.” *Id.* The first powered
3 device includes classification circuitry 20 with, by way of example, an operational amplifier 30 to
4 convert voltage to current, a voltage divider, a first classification resistor RCLASS1 38, and a FET
5 gate 40. *Id.* at [0033], Fig. 3. The second powered device includes connection circuitry 24, including
6 a voltage divider, a FET gate 44, a second classification resistor RCLASS2 46, and a switch 48. *Id.*

7 When the first powered device is activated, RCLASS1 is placed in parallel with RCLASS2,
8 such that the amount of current flowing through FET 40 = $V_{ref}/RCLASS1 + V_{ref}/RCLASS2$). *Id.*
9 at [0035]. In other words, RCLASS2 in the second powered device increases the current 52 drawn
10 through gate 40 during the classification process, and this increased current is provided to power
11 source 12 as the classification signal 23. *Id.* This causes the power source to classify the first
12 powered device 14 higher than it would be classified on its own, and provide additional power. *Id.*
13 Control element 64 in the first powered device 14 controls gate 62 in response to current passing
14 through node 50, such that the gate is open when a small amount of current passes through the node
15 and remains closed when a large amount of current passes through the node. *Id.* at [0058]. When the
16 gate is closed, current flows through the node 50 and through detection resistor RDETECT 66 in
17 the second powered device. *Id.* at [0060]. The current measuring circuit 60 measures the current at
18 node 50 and transmits the current value to detection circuitry 68, which detects the presence or
19 absence of the second powered device 16. *Id.* at [0058]. The first powered device 14 can also detect
20 decoupling of the second powered device 16. *Id.* at [0063].

vii. Diab '255

Lastly, Diab '255 is directed to a PoE system for providing power to a PD with unpredictable or variable levels of power draw. Diab '255 at [0014], [0019]. As with the previous references, the system taught by Diab '255 includes a PSE that transmits power to a PD, where the PD includes a PoE module which enables the PD to communicate with the PSE according to IEEE 802.3af. *Id.* at [0014]. The system may include multiple PDs (*Id.* at [0016]), and the PD includes a power module and a power FET for producing output PoE power based on power provided by the PSE. *Id.* at [0017], Fig. 2. Diab '255 teaches that where the PD has variable power draw—as is the case with a laptop computer, for example—the PSE may indirectly provide power to a rechargeable battery within the PD, instead of directly powering the PD, because a battery has a more stable power profile. *Id.* at [0023]. Under this arrangement, the PSE does not need to account for “wide fluctuations in power draw based on changes in use.” *Id.*

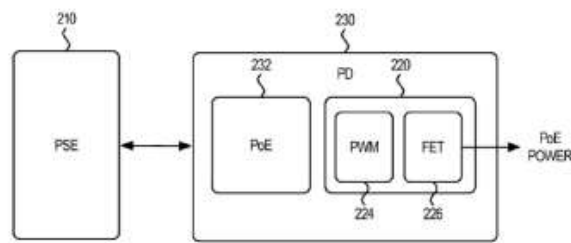


FIG. 2

Diab '255 at Fig. 2.

An exemplary PD, illustrated in Fig. 3, includes regulation circuitry 330 for guiding power from an AC outlet to either the PD's electronic circuitry 370 for use, or to the battery charging circuitry 350 to charge battery 360. *Id.* at [0025], Fig. 3. The PD further includes switch 340 for powering electronic circuitry 370 from either the AC outlet or the battery 360. *Id.* In a second example illustrated in Fig. 4, the delivery of power from AC outlet 410 to electronic circuitry 480 and battery 470 is under control of a power management unit (PMU) 450. *Id.* at [0028], Fig. 4. The PMU can monitor the current used to charge the battery using current control module 460 and adjust the battery charging if the current requirements of electronic circuitry 480 increase. PMU 450

1 includes a switch 450 to control provision of charging to the battery, which allows the device to cut-
2 off charging current if the battery is fully charged. *Id.*

3 The process begins at step 502 in Fig. 5, where the PSE detects the PD by detecting the
4 signature resistance, 25,000Ω, in the PD. *Id.* at [0034], Fig. 5. Then, the PSE identifies the class of
5 the PD by measuring current drawn when voltage is applied to the PD at a classification range. *Id.*
6 at [0035]. The resulting current measurement is used to classify the PD according to the IEEE
7 802.3af standard. *Id.* Based on the classification, the PSE provides power to the PD. *Id.* At step 508,
8 power received from the PSE is routed to the battery charging circuit of the PD, and power from the
9 battery is then used to power the PD. *Id.* at [0036].

10 **c) PoE Devices**

11 U.S. Pat. App. Pub. No. 2005/0268120 A1 to Schindler et al. (“Schindler”), U.S. Pat. App.
12 Pub. No. 2008/0235523 A1 to Hussain (“Hussain”), U.S. Pat. App. Pub. No. 2005/0044431 A1 to
13 Lang et al. (“Lang”), U.S. Pat. App. Pub. No. 2006/0218420 A1 to Camagna et al. (“Camagna”),
14 U.S. Pat. App. Pub. No. 2008/0016263 A1 to Diab et al. (“Diab ’263”), U.S. Pat. App. Pub. No.
15 2006/0168459 A1 to Dwelley et al. (“Dwelley”), U.S. Pat. App. Pub. No. 2008/0005598 A1 to
16 Landry et al. (“Landry”), U.S. Pat. App. Pub. No. 2006/0210057 A1 to Stanford (“Stanford”),
17 MAX5922, and TPS2370 are each generally directed to the provision of power via PoE. While each
18 of these references refers to PoE or the IEEE 802.3af standard, Hussain and Diab ’263 explicitly
19 incorporate IEEE 802.3af by reference.

20 **i. Schindler**

21 Schindler is directed to a method for power delivery that includes coupling an ethernet cable
22 with four wire pairs to a power delivery system and providing power to a PD on all four wire pairs.
23 Schindler at [0003]. The system allows more power to be delivered to the PD and allows the PSE
24 to provide variable power levels to a PD based on its changing power demands. *Id.* at [0006], [0016].
25 Schindler explains that one advantage of the system is “adaptability to multiport devices.” *Id.* at
26 [0025]. For example, a docking station could be coupled to an Ethernet jack, where the amount of
27 power provided by the jack could be adjusted based on the number of devices attached to the docking
28 station. *Id.*

1 Schindler teaches that the PSE 100 includes a controller 120, which controls switches 122
2 coupled to connectors 118A-D. *Id.* at [0019], Fig. 1. Schindler explains that switches 112, which
3 are used to convey power from power source 124 to the connectors, may be diodes or “any
4 components for regulating the power delivered to ports 118, such as mechanical, magnetic, or
5 electrical relays.” *Id.* at [0019]. Schindler further teaches that the PSE 100 may determine power
6 characteristics of the PD by monitoring the response of PD 102 to voltage and current values on
7 ports 118. *Id.* at [0022]. For example, after detecting the power need of PD 102, the PSE may
8 initially transmit power on all four ports 188, and reduce the number of ports after determining that
9 the PD is not using all the power. *Id.* In another embodiment, the PSE and PD may exchange power
10 information using IEEE 802.3af classification. *Id.* at [0024].

11 In operation, the PSE detects that a PD has been connected by providing power at a
12 predetermined level and monitoring the response of the PD 102. *Id.* at [0027]. The PSE then
13 determines a power level for the PD, and controller 120 applies power to the ports 118 based on the
14 power requirements of the PD. *Id.* The PSE monitors PD power usage for changes; if there is a
15 change, PSE determines whether the PD has been “powered off or disconnected from the network.”
16 *Id.* at [0028]. If the device has been powered off, the system returns to search for a PD, and the
17 process ends. *Id.* If there has been a change caused by something other than the PD disconnecting
18 or being powered off, the PSE determines a new power level for the PD and changes power
19 accordingly. *Id.* at [0029].

20 **ii. Hussain**

21 Hussain is also directed to a PoE system comprising a PSE and a PD. Hussain teaches that
22 the PSE includes a controller 218 that “detects and validates a compatible PD, determines a power
23 classification signature for the validated PD, supplies power to the PD, monitors the power, and
24 reduces or removes the power from the PD when the power is no longer requested or required.”
25 Hussain at [0026]. If the PSE determines that the PD is not compatible during the detection process,
26 “the PSE can prevent the application of power to that PD device, protecting the PD from possible
27 damage.” *Id.* Hussain explains that “[t]he IEEE has imposed standards on the detection, power
28

1 classification, and monitoring of a PD by a PSE in the IEEE 802.3af standard, which is incorporated
2 herein by reference.” Hussain at [0026].

3 Hussain further teaches that, “[i]n order to conduct its management and control of PD 106,
4 PSE 102 analyzes certain characteristics of PD 106, and the system as a whole, based on
5 measurements taken at PD 106.” *Id.* at [0032]. Example attributes determined by PSE 102 include
6 “valid device detection, power classification, AC disconnect information, short circuit detection, PD
7 load variations, various current measurements, overload conditions, and inrush conditions.” *Id.* The
8 PSE is designed to manage power based on the dynamic needs of the PD. *Id.* at [0025]. To that end,
9 the PSE measures the voltage, current, and temperature of the PD so as to characterize its power
10 requirements and implement management functions. *Id.*

11 More specifically, during initialization, the PD controller provides impedance signatures so
12 that the PSE can recognize the PD as a valid PoE device. *Id.* at [0029]. A signature resistor is used
13 to validate the PD, while a classification resistor is used to classify the PD. *Id.* During the detection
14 process, the PSE probes the current and voltage drop at the PD to calculate the resistive signature
15 of the PD. *Id.* at [0036]. If the signature is approximately 25K Ω , the PD is determined to have a
16 valid signature. If the PD is deemed non-compatible, power will not be supplied. *Id.* After detection,
17 the PSE uses power classification to determine the range of maximum power to be provided to the
18 PD. *Id.* at [0037]. To classify the device, the PSE applies a voltage at the PD and measures the
19 current through the PD’s classification resistor. *Id.* Hussain teaches that detecting a PD before a
20 normal level of power is supplied is important due to safety reasons, because legacy devices are not
21 designed to accept inline power. *Id.* at [0053].

22 **iii. Lang**

23 Lang is directed to power delivery over a data wiring system with a power source, powered
24 device, and cable for delivering both power and data. Lang at [0019]. Lang teaches that the power
25 source includes a plurality of switches, which “may be electromechanical, or alternatively,
26 configured as metal-oxide semiconductor field-effect transistors (MOSFET), bipolar junction
27 transistors, equivalent circuitry, or any combination thereof,” which form a programmable current
28 limiting system. *Id.* at [0024]. Lang further teaches that the powered device has multiple signature

1 resistors used for detection, and for signaling high and low power modes to the power source. *Id.* at
2 [0032], [0037]. In operation, the power source senses the current through the signature resistors to
3 detect a valid powered device and determine whether the device is requesting a high-powered mode.
4 *Id.*

5 **iv. Camagna**

6 Camagna is directed to “a system and method operable to provide a power feed on
7 differential cable pairs to network attached powered devices (PD).” Camagna at [0009]. Camagna
8 teaches that the system follows the detection scheme set forth in the IEEE 802.3af standard, which
9 allows the system “to be backward compatible with non-powered systems,” because “the DC
10 voltage applied [during detection] will begin at a very low voltage and only begin to deliver power
11 after confirmation that a POE device is present.” *Id.* at [0073]. The system also follows the
12 classification procedure to determine the amount of power needed by the powered device. *Id.* at
13 [0072]. Specifically, the PSE applies a voltage to the PD and “measures the current to determine the
14 power class of the device.” *Id.* at [0073].

15 **v. Diab ’263**

16 Diab ’263 similarly describes a PoE system that implements the detection and classification
17 schemes outlined in IEEE 802.3af. Diab ’263 is directed to a PoE system with a PSE that controls
18 its voltage supply based on the dynamic needs of the PD. Diab ’263 at [0027]. “More specifically,
19 the PSE controller 218 measures the voltage, current, and temperature of the outgoing and incoming
20 DC supply lines so as to characterize the power requirements of the PD 106.” *Id.* The PSE controller
21 also “detects and validates a compatible PD, determines a power classification signature for the
22 validated PD, supplies power to the PD, monitors the power, and reduces or removes the power
23 from the PD when the power is no longer requested or required.” *Id.* at [0028]. Diab ’263 explains
24 that “IEEE has imposed standards on the detection, power classification, and monitoring of a PD by
25 a PSE in the IEEE 802.3af standard and the IEEE 802.3 standard.” *Id.* at [0028].

26 **vi. Dwelley**

27 Dwelley is directed to a PoE system that implements the detection and classification schemes
28 outlined in IEEE 802.3af, and provides for a third signature that is not described in the standard for

1 communicating additional information about the PD. Specifically, Dwelley discloses a PoE system
2 where “[t]he PSE 12 may interact with each PD in accordance with the IEEE 802.3af standard.”
3 Dwelley at [0038]. This means that “the PSE 12 and the PD participate in the PD detection
4 procedure, during which the PSE 12 probes a link to detect the PD” and determine whether “the PD
5 detection signature... is valid or non-valid.” *Id.* “While the valid PD detection signature indicates
6 that the PD is in a state where it will accept power, the non-valid PD detection signature indicates
7 that the PD is in a state where it will not accept power.” *Id.* If the PD is valid, the PD may optionally
8 present “a classification signature to the PSE to indicate how much power it will draw when powered
9 up.” *Id.* at [0039]. Then, “[b]ased on the determined class of the PD, the PSE applies the required
10 power to the PD.” Dwelley at [0039]. Dwelley additionally teaches that the PD may present a *third*
11 *signature* to communicate additional information, such as “a special operating power level different
12 from the standard IEEE 802.3af levels, or [] a system serial number that uniquely identifies the PD.”
13 *Id.* at [0044]. The third signature may be provided before power is applied to the PD or after power
14 is provided. *Id.*

15 **vii. Landry**

16 Landry is directed to a PoE system with a PD having an adjustable current limiter. Landry
17 at [0016]. Landry teaches that the PD also includes PoE protocol circuitry, which incorporates a
18 PoE detection and classification circuit that follows the IEEE 802.3af standard. *Id.* at [0017]. Landry
19 further explains that, while only a single PD is shown, the PSE “may be coupled to multiple powered
20 devices and may provide power and data to each of the multiple powered devices,” which may have
21 different power requirements. *Id.* at [0018].

22 During the detection process, the PCE of Landry’s system applies a voltage to the PD and
23 “monitors a received current” or “a received voltage” to detect a resistance within the expected
24 range. *Id.* at [0003]. If a valid device is detected, the PSE may optionally classify the device by
25 applying a classification voltage to the PD and measuring the resulting current, which is associated
26 with a power class. *Id.* at [0004]-[0006].

1 **viii. Stanford**

2 Stanford is directed to a PoE system with a PSE configured to provide power to a high-
3 power PD over all four pairs of conductors in an Ethernet link. Stanford at [0003], [0011]. Stanford
4 explains that, according to the IEEE 802.3af standard, “[t]he main functions of the PSE are to search
5 the link for a PD requesting power, optionally classify the PD, supply power to the link if a PD is
6 detected, monitor the power on the link, and disconnect power when it is no longer requested or
7 required.” *Id.* at [0007]. The PD participates in the detection procedure “by presenting a PoE
8 detection signature defined by the IEEE 802.3af standard.” *Id.* Stanford further teaches that, “[i]f
9 the detection signature is valid, the PD has an option of presenting a classification signature to the
10 PSE to indicate how much power it will draw when powered up.” *Id.* at [0008]. Based on the class,
11 “the PSE applies the required power to the PD over the data pairs.” *Id.*

12 **ix. MAX5922**

13 MAX5922 is a single port network power switch for Power-Over-LAN that complies with
14 the IEEE 802.3af standard. MAX5922 at 1. The device is “specifically designed for power-sourcing
15 equipment (PSE)” and “provides power devices (PD) discovery, classification, current limit, and
16 other necessary functions for an IEEE 802.3af compliant PSE.” *Id.* The MAX5922 operates in three
17 modes: “PD detection mode, PD classification mode, and power mode.” *Id.* at 12. The MAX5922
18 performs PD detection by forcing a probe voltage and sensing the resulting current. *Id.* The
19 MAX5922 uses the current measurement to check for a valid PD resistive signature. *Id.* After
20 detection, the MAX5922 enters classification mode. *Id.* at 15. Again, the MAX5922 forces a voltage
21 and measures the current, which corresponds with the class of the PD. *Id.* The MAX5922 also has
22 a “zero-current detection function,” which “monitors the output for an undercurrent condition and
23 eventually turns off the power to the output if the PD is disconnected.” *Id.* at 16.

24 **x. TPS2370**

25 TPS2370 is an IEEE 802.3af compliant power interface switch for PDs. TPS2370 at 1. The
26 TPS2370 acts “as an interface between the power sourcing equipment (PSE) and the powered
27 device (PD)” and “performs all detection, classification, inrush current limiting, and switch FET
28 control that is necessary for compliance with the IEEE 802.3af Standard.” *Id.* at 1. The TPS2370

1 datasheet explains that “[a] powered device (PD) draws power or requests power by participating
2 in a PD detection algorithm,” which “requires the power sourcing equipment (PSE) to probe the
3 link looking for a valid PD.” *Id.* at 7. The PSE probes the link by sending out a voltage, and a
4 valid PD detects this voltage and places a resistance of between 23.75 kΩ and 26.25 kΩ across the
5 power lines. *Id.* “On detecting this current, the PSE concludes that a valid PD is connected at the
6 end of the ethernet cable and is requesting power.” *Id.* The PSE can then optionally initiate a
7 classification procedure, which “is used by the PSE to determine the maximum power required by
8 the PD during normal operation.” *Id.* To determine the PD’s power class, the PSE increases the
9 voltage across the power lines, and the amount of current drawn by the PD determines the
10 classification according to the IEEE 802.3af standard.

11 **d) Dual-Role PoE Device**

12 Biederman, discussed above along with other daisy chain PoE devices, also discloses a dual-
13 role combination PD/PSE device that can swap between PD and PSE functions depending on the
14 connected device. *See, e.g.*, Biederman at [0034], Fig. 2.

15 U.S. Patent App. Pub. No. 2008/0028237 A1 to Knight (“Knight”) is similarly directed to a
16 device “capable of communicating power and data through a single connector to another device,”
17 where the device may source or sink power. Knight at [0024], [0039]-[0040]. The device may be,
18 for example, “a dedicated network connection device..., [or] a portion of a computer, robot, [or]
19 network appliance.” *Id.* at [0031]. Knight teaches that the device may connect to multiple other
20 devices and enable communication between them according to PoE, Firewire, USB, or similar
21 communication protocols. *Id.* at [0031]-[0032], [0001], [0024].

22 Knight further explains that, when a connection is made, the device may “first attempt[] to
23 connect as a power source, then attempt[] to connect as a power sink if the power source attempt
24 fails.” *Id.* at [0048]. Alternatively, the device “may be configured to attempt to connect as a power
25 sink initially, then attempts as a power source secondarily.” *Id.* The sink/source negotiation process
26 “may be through sensing status and communicating through the power connections.” *Id.* at [0047].
27 “One example of such communication may be for a device to configure a specific resistance along
28

1 the power connections to indicate that it may sink power,” in which case “the connecting device
2 may sense the resistance and then begin supplying power to the first device.” *Id.*

3 Knight teaches that the device 102 with the power management system 124 may include
4 connector interfaces 104, 106, 108, and 110 for connecting to devices 138, 140, 142, and 144, as
5 well as a battery bank voltage source 126 which “may be used to store power during certain times
6 and discharge power during other times.” *Id.* at [0025]-[0026]. For example, in a robotic
7 application where the device 102 may be mounted in a charging base, “the battery bank 126 may
8 be charged through the outside power source 136 or through power supplied through one of the
9 connector interfaces 104, 106, 108, and 110” during a charging phase, and “[w]hen the robot is
10 mobile, the charging source may be disconnected and the battery bank 126 may supply power to
11 the device 102 and other connected devices.” *Id.* at [0025]. More particularly, “[a]ny or all of the
12 devices 138, 140, 142, or 144 may be able to supply power through the respective connector
13 interfaces to charge the battery bank 126,” and “any of the devices 138, 140, 142, and 144 may
14 draw power through the connector interfaces that would discharge the battery bank 126.” *Id.* at
15 [0029]. “In some cases, the power management system 124 may receive power from one or more
16 of the remote devices, distribute power to other remote devices, and charge or discharge the
17 battery bank 126 as appropriate . . . if the power source is greater than the total power drain for
18 external devices....If the power source is less than the total power drain, the battery bank 126 may
19 be discharged to supplement the power source.” *Id.*

20 On-The-Go Supplement to the USB 2.0 Specification Revision 1.0a (USB-OTG) is a
21 specification that enables the connectivity between USB devices. USB-OTG was implemented by
22 USB Implementers Forum, Inc. (USB-IF), first sold or offered for sale in the United States by at
23 least June 24, 2003. Various systems are equipped with the USB OTG functionality, including the
24 Samsung Yepp YP-D1 (“YP-D1”), which is an MP3 player first sold or offered for sale in the United
25 States by at least by Samsung on February 14, 2006. The YP-D1 is used to connect to other devices
26 such as computers, tablets, and cellular phones.

27 Accordingly, because each of the identified references are directed to similar devices in the
28 similar field of endeavor, a person of ordinary skill in the art would be motivated to combine the

1 teachings of two or more references together because the references disclose similar systems that
2 solve the same problems in similar ways. Thus, it would have been obvious to one of ordinary skill
3 in the art to combine any of the foregoing references and one of ordinary skill would have expected
4 such a combination to be successful.

5 To the extent that it is determined that any of the above references do not disclose a particular
6 claim element, it would have been obvious to modify the teachings of that reference to include such
7 element as taught in any other of the above references that discloses such element (as documented
8 in the claim charts attached as E-1 through E-20).

9 For example, to the extent that it is determined that any of the above references do not
10 disclose a “power delivery circuit comprising...a voltage source configured to generate a voltage,”
11 as recited in claim 1, it would have been obvious to modify the teachings of that reference to include
12 these features in view of the knowledge of a POSITA and the teachings of at least Biederman,
13 Knight, or Diab '255. Biederman teaches a combination PD/PSE unit that can swap between PD
14 and PSE functions depending on the connected device. *See, e.g.*, Biederman at [0034], Fig. 2.
15 Biederman discloses that the PSE portion of the unit contains its own 48 Volt power supply. *Id.* at
16 Fig. 5 (supply 70), Fig. 6 (supply 80), [0038]-[0039]. Power supply block 70/80 may be a
17 “conventional grid-powered or battery-powered power supply.” *Id.* at [0039]. Providing the
18 combination PD/PSE device with its own PSE power supply allows the device to power itself (in
19 PSE+PD mode) or immediately adjacent devices in a daisy chain in certain emergency situations
20 when connections to other devices in the chain that had previously been providing power are cut.
21 *Id.* at [0041], [0044]-[0046]. This would allow “the normal effects (e.g., data interruption, power
22 interruption) of a cut in the cabling coupling the devices together [to] be avoided.” *Id.* at [0044].
23 Thus, it would have been obvious to a POSITA to modify any of the PoE references to provide a
24 combination PD/PSE device with its own power supply block, in order to minimize power
25 interruptions in the event of cable cuts and provide power redundancy.

26 Knight teaches a dual-role PoE device with a battery 126 and power management system
27 124 that can be used to store energy in battery 126 during certain times and discharge power from
28 the battery during other times. Knight at [0025]-[0026]. More specifically, any of the devices 138,

1 140, 142, or 144 connected to the dual-role device 102 “may be able to supply power through the
2 respective connector interfaces to charge the battery bank 126,” and “any of the devices 138, 140,
3 142, and 144 may draw power through the connector interfaces that would discharge the battery
4 bank 126.” *Id.* at [0029]. Knight explains that this arrangement is useful for mobile robotic
5 applications, in which the device 102 may be in a charging phase when mounted in a charging base,
6 and in a power supplying phase when mobile. *Id.* at [0025]-[0026], [0029]. Accordingly, it would
7 have been obvious to a POSITA to modify any of the above references to provide for a dual-role
8 rechargeable device in certain mobile applications, where it is desirable for the device to recharge
9 when at rest and provide power to auxiliary devices when on the move. *Id.*

10 Diab ’255 similarly discloses a PoE system with a PSE that can provide power directly to a
11 PD, or indirectly to a rechargeable battery voltage source within the PD, which has a more stable
12 power use profile. Diab ’255 at [0023]. Diab ’255 explains that such an arrangement is advantageous
13 when a PSE is connected to a PD with variable and unpredictable power usage, because a
14 rechargeable battery tends to have a more stable power profile that does not need to be accounted
15 for by the PSE. *Id.* Thus, it would have been obvious to a POSITA to modify any of the PoE
16 references in view of Diab ’255 to provide for the provision of power to a PD that has variable
17 power requirements—such as a laptop—so that the PSE does not need to account for “wide
18 fluctuations in power draw based on changes in use.” *Id.* Such a combination reflects no more than
19 the use of a known technique—charging a battery—to improve similar PoE devices in the same
20 way.

21 As an additional example, to the extent that it is determined that any of the above references
22 do not disclose “a power relay switch configured to relay, when closed, the voltage generated by the
23 voltage source,” as recited in claim 1, it would have been obvious to modify the teachings of that
24 reference to include these features in view of the knowledge of a POSITA and the teachings of at
25 least Schindler, Biederman, Penning, Robbins, and Lang, which disclose a variety of switches for
26 relaying voltage from a PSE to a PD, including relay switches. *See, e.g.,* Schindler at [0019] (“In
27 one embodiment, diodes 112 may be used as a switch, and may be substituted with any components
28 for regulating the power delivered to ports 118, such as mechanical, magnetic, or electrical relays.”);

1 Biederman at [0038] (“Switches (or other equivalent Switching equipment Such as diodes,
2 transistors, relays and the like as will now be apparent to those of ordinary skill in the art) are
3 provided to enable either the PD or the PSE (or neither or both) modes at port 61.”); Penning at
4 [0032] (“The switching of power supplies for the data distribution device may be performed using
5 relays, transistors, or any other known switching devices.”); Robbins at [0036] (“In another
6 embodiment, the power switch 52 shown in FIG. 6 is a relay (either mechanical or solid-state) that
7 is controlled by circuitry.”); Lang at [0024] (“The switches 270 may be electromechanical, or
8 alternatively, configured as metal-oxide semiconductor field-effect transistors (MOSFET), bipolar
9 junction transistors, equivalent circuitry, or any combination thereof.”). Such switches are well
10 known in the art, and any suitable type of power switch could be selected by a POSITA as a matter
11 of routine design choice. At a minimum, such a combination reflects a simple substitution of one
12 known element—a relay—for another switching mechanism to obtain predictable results.

13 As an additional example, to the extent that it is determined that any of the above references
14 do not disclose “a signature resistor,” as recited in claim 1, it would have been obvious to modify
15 the teachings of that reference to include these features in view of the knowledge of a POSITA and
16 the teachings of at least IEEE 802.3af, Karam ’799, Diab ’255, Toebe, Hussain, Lang, Camagna,
17 Diab ’263, Dwelley, Landry, MAX5922, TPS2370, USB-OTG 1.0a, and Stanford, which disclose
18 the basic components of a PoE system under the IEEE 803.2af standard, including the signature
19 resistor for PD detection. Given that the above references explicitly refer to the IEEE 802.3af
20 standard, such a combination would have been obvious to a POSITA.

21 It also would have been obvious to modify the teachings of any of the above references to
22 include the “signature resistor” feature in view of the knowledge of a POSITA and the teachings of
23 at least Penning and Karam ’799. Specifically, Penning teaches a PoE device 205 with power
24 detectors 355 and 350 for determining whether power is available from connected devices 115 and
25 210. Penning at Fig. 3, [0049], [0056]. Penning teaches that the detectors may be “either voltage or
26 current detectors...of any appropriate type known to one of ordinary skill in the art.” *Id.* at [0049].
27 The detectors send signals to process controller 340, which determines which power supply to use
28 and sends a command signal to switch 380 to switch between the sources. *Id.* at [0049], [0051],

1 [0056], [0047]. Karam '799 teaches that one type of current sensor is a "current sense resistor."
2 Karam '799 at [0058], Fig. 5. It would have been obvious to a POSITA to provide such power
3 detectors in a device that may be able to receive power from multiple sources, in order to switch
4 between the sources. Such a combination would merely reflect the use of a known technique to
5 improve similar devices in the same way.

6 As an additional example, to the extent that it is determined that any of the above references
7 do not disclose "a load detector connected to the switch and configured to read a load current flowing
8 therethrough so as to detect a load in one of the connected devices, and to extract information about
9 the connected device based on the load current," as recited in claim 1 and in similar form in claim
10 7, it would have been obvious to modify the teachings of that reference to include these features in
11 view of the knowledge of a POSITA and the teachings of at least IEEE 802.3af, Karam '799, Diab
12 '255, Toebe, Hussain, Lang, Camagna, Diab '263, Dwelley, Landry, MAX5922, TPS2370, USB-
13 OTG 1.0a, and Stanford, which disclose the basic components of a PoE system under the IEEE
14 803.2af standard, including the means by which the PSE detects a valid PD and classifies its power
15 requirements using current measurements. Given that the above references explicitly refer to the
16 IEEE 802.3af standard, such a combination would have been obvious to a POSITA.

17 As an additional example, to the extent that it is determined that any of the above references
18 do not disclose "wherein the information extracted by the load detector comprises information
19 regarding whether the connected device is powered on or powered off," as recited in claim 1 and in
20 similar form in claim 7, it would have been obvious to modify the teachings of that reference to
21 include these features in view of the knowledge of a POSITA and the teachings of at least Karam
22 '799, Penning, and Schindler, which each teach a PoE system in which a first device detects whether
23 a connected device is powered off for the purpose of discontinuing power. *See, e.g.*, Karam '799 at
24 [0058] ("If the control circuitry 78 sees that power is applied and then the current in current sensor
25 92 goes to zero (device at second port 74 is off or disconnected) while current is still being used by
26 third port 76 then it forces normally closed switch 90 to open making sure that a 'hot cable' situation
27 is not created at second port 74 by removing the inline power to second port 74."); Penning at [0067]
28 ("The power management process 500 is terminated upon...powering down the VoIP phone 400.");

1 Schindler at [0028] (“If there is a change in the power usage of device 102, power delivery system
2 100 determines whether the device has been powered off or disconnected from the network at step
3 210. If device 102 has been powered off, then system 100 returns to a search for a powered device,
4 and the method is at an end.”). It would have been obvious to a POSITA to modify any of the above
5 references in view of Karam ’799, Penning, or Schindler to preserve power and avoid a “hot cable”
6 situation when a connected device is powered off. Moreover, any such combination would merely
7 reflect the use of known technique to improve similar devices or methods in the same way.

8 As an additional example, to the extent that it is determined that any of the above references
9 do not disclose “wherein the load detector is further configured to detect removal of one of the
10 plurality of devices from the network,” as recited in claim 5 and in similar form in claim 9, it would
11 have been obvious to modify the teachings of that reference to include these features in view of the
12 knowledge of a POSITA and the teachings of at least IEEE 802.3af, Karam ’799, Karam ’280,
13 Penning, MAX5922, and Schindler. As one example, Karam ’799 discloses that the power switch
14 S5 is “closed only while current [i]s being drawn from third connector 56 so that if the device were
15 unplugged from third connector 56 the power would turn off.” Karam ’799 at [0051]. The above
16 references refer to the IEEE 802.3af standard, which provides that one of the “PSE’s main functions
17 [is] to...scale power back to the detect level when power is no longer requested or required,” where
18 “an unplugged link section is one instance when power is no longer required.” IEEE 802.3AF at 29.
19 Accordingly, it would have been obvious to a POSITA that the PSE should be able to detect when
20 a device is unplugged, so that the PSE can stop providing power. This would conserve power and
21 prevent a legacy device from accidentally being powered when it is plugged in immediately after a
22 valid PD device. *See, e.g.,* Mendelsen, All You Need to Know About Power over Ethernet (PoE)
23 and the IEEE 802.3af Standard, at 18 (“When a PD is disconnected, there is a danger that it will be
24 replaced by a non-PoE-ready device while power is still on. Imagine disconnecting a powered IP
25 phone utilizing 48 Vdc, then inadvertently plugging the powered Ethernet cable into a non-PoE
26 notebook computer. What’s sure to follow is not a pretty picture. The standard defines two means
27 of disconnection, DC Disconnect and AC Disconnect, both of which provide the same functionality
28 - the PSE shutdowns power to a disconnected port within 300 to 400ms. The upper boundary is a

1 physical human limit for disconnecting one PD and reconnecting another.”). Accordingly, it would
2 have been obvious to a POSITA to modify any of the above references to detect removal of a PD in
3 order to shut down power. Such a combination would merely reflect the use of known technique to
4 improve similar PoE devices or methods in the same way.

5 As an additional example, to the extent that it is determined that any of the above references
6 do not disclose “[a] method of delivering power to one of a plurality of devices connected in a daisy
7 chain,” as recited in claim 7, it would have been obvious to modify the teachings of that reference
8 to include these features in view of the knowledge of a POSITA and the teachings of at least
9 Biederman, Karam ’799, Karam ’280, Diab ’255, Penning, Toebes, and Robbins, which each
10 disclose the provision of power via PoE to multiple devices arranged in a daisy chain. Karam ’799,
11 Karam ’280, and Robbins further explain why daisy chaining devices in a PoE system is
12 advantageous. *See, e.g.*, Karam ’799 at [0054] (“A device such as that just described would be
13 helpful to people who have a need to charge cellular phones or power other low-power equipment
14 from the inline power available on network cabling. It would also be useful in situations where low-
15 power sensors (such as IP television cameras) need to be wired in a daisy chain configuration and
16 powered from a wired network using inline power.”); Karam ’280 at [0030] (“[T]he modular
17 powered device 16 receives power directly from the first powered device 14 for operation. As a
18 result, the modular powered device 16 does not require additional equipment, such as a bulky power
19 cube and cord, in order to operate. Additionally, the modular powered device 16 does not need to
20 be located in the vicinity of an external power supply, such as a wall outlet, in order to operate.”);
21 Robbins at [0025] (“An advantage of the mid-link PD 24 is that it can be installed without laying in
22 a second network cable....No new network cable must be routed through the infrastructure of the
23 building.”). In view of the above, it would have been obvious to a POSITA to modify any of the
24 above PoE references to have daisy chain functionality, in order to provide power to devices without
25 requiring extra equipment or a local power supply.

26 A person skilled in the art would have been motivated to combine any of the above
27 references. In particular, the combinations identified herein would merely have been (a) a
28 combination of prior art elements according to known methods to yield predictable results; (b) a

1 simple substitution of one known element for another to obtain predictable results; (c) a use of
2 known technique to improve similar devices or methods in the same way; (d) application of a known
3 technique to a known device or method ready for improvement to yield predictable results; (e)
4 obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in
5 either the same field or a different one based on design incentives or other market forces since the
6 variations are predictable to one of ordinary skill in the art. Moreover, a person of ordinary skill in
7 the art had a reason to combine these references because—at a minimum—they all pertain to
8 systems and methods for delivering power to devices connected in a network via PoE, including
9 means for detecting connected devices and determining their power requirements. Several of these
10 references are specifically directed to the provision of power to devices connected in a daisy-chain
11 configuration.

12 As discussed above, the motivation to combine the teachings of the patents and other prior
13 art referenced above is found in the art as specified in the charts and in: (1) the nature of the problem
14 being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of
15 persons of ordinary skill in the art; and (4) the fact that the prior art is generally directed towards
16 systems and methods for delivering power to devices connected in a network via PoE, and (5) the
17 predictable results obtained in combining the different elements of the prior art. The Supreme Court
18 has held that a showing of a motivation to combine within the references themselves is not required
19 to prove obviousness. See *KSR*, 550 U.S. at 401 (“Any need or problem known in the field of
20 endeavor at the time of invention may provide the motivation to combine.”).

21 **e) Exemplary Combinations and Modifications**

22 As illustrated in the claim chart attached as **Exhibit E-2**, Karam ’799, alone or in combination
23 with Schindler, Biederman, Penning, Robbins, or Lang (**as shown in their respective claim charts**),
24 discloses or renders obvious all elements of the ’712 Asserted Claims.

25 Similarly, as illustrated in Exhibit E-1, Biederman, alone or in combination with (a) IEEE
26 802.3af, Karam ’799, Diab ’255, Toebes, Hussain, Lang, Camagna, Diab ’263, Dwelley, Landry,
27 MAX5922, TPS2370, or Stanford (as shown in their respective claim charts); and (b) Karam ’799,
28

1 Penning, or Schindler (as shown in their respective claim charts), discloses or renders obvious all
2 elements of the '712 Asserted Claims.

3 Furthermore, as illustrated in Exhibit E-5, Knight, alone or in combination with (a) IEEE
4 802.3af, Karam '799, Diab '255, Toebe, Hussain, Lang, Camagna, Diab '263, Dwelley, Landry,
5 MAX5922, TPS2370, or Stanford (as shown in their respective claim charts); (b) Karam '799,
6 Penning, or Schindler (as shown in their respective claim charts); and (c) Schindler, Biederman,
7 Penning, Robbins, or Lang (as shown in their respective claim charts), discloses or renders obvious
8 all elements of the '712 Asserted Claims.

9 As illustrated in Exhibit E-3, Penning, alone or in combination with (a) IEEE 802.3af, Karam
10 '799, Diab '255, Toebe, Hussain, Lang, Camagna, Diab '263, Dwelley, Landry, MAX5922,
11 TPS2370, or Stanford (as shown in their respective claim charts); and (b) Karam '799 or Schindler
12 (as shown in their respective claim charts), discloses or renders obvious all elements of the '712
13 Asserted Claims.

14 As illustrated in Exhibit E-4, Toebe, alone or in combination with (a) Karam '799, Penning,
15 or Schindler (as shown in their respective claim charts); and (b) Schindler, Biederman, Penning,
16 Robbins, or Lang (as shown in their respective claim charts), discloses or renders obvious all
17 elements of the '712 Asserted Claims.

18 As illustrated in Exhibits E-6 through E-15, E-18, E-19, and E-20 the general PoE references,
19 alone or in combination with (a) any of the daisy chained PoE references, including Karam '799,
20 Karam '280, Penning, or Toebe (as shown in their respective claim charts); and (b) Karam '799,
21 Penning, or Schindler (as shown in their respective claim charts), discloses or renders obvious all
22 elements of the '712 Asserted Claims.

23 Thus, in addition to the combinations discussed above, exemplary combinations which
24 render obvious some or all of the Asserted Claims of the '712 Patent are listed in **Appendix A**, Sec.
25 V.

26 **B. Invalidity of the '712 Patent Based on 35 U.S.C. § 112, ¶ 1**

27 Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of
28 the '712 Patent, to the extent such positions can be understood from Plaintiff's Infringement

1 Contentions, Defendant asserts that the Asserted Claims of the '712 Patent are invalid for failure to
2 provide a written description that enables the full scope of the Asserted Claims based on at least the
3 following claim terms, phrases, or limitations:

- 4 • **“a load detector connected to the switch and configured to read a load current flowing**
5 **therethrough so as to detect a load in one of the connected devices, and to extract**
6 **information about the connected device based on the load current” (claim 1):** The
7 specification does not provide sufficient written description and/or fully enable the recited
8 “load detector” limitation. For example, to the extent UCT asserts that the “load detector”
9 is configured to read a load current flowing through components other than the switch, the
10 specification lacks sufficient written description support or an enabling disclosure.
- 11 • **“a signature resistor connected to the switch and configured to detect a power source**
12 **from one or more of the connected devices;” (claim 1):** The specification does not provide
13 sufficient written description and/or fully enable the recited “signature resistor” limitation.
14 For example, the specification does not disclose or enable a person of ordinary skill in the
15 art on how a “signature resistor” is configured to detect a power source form the connected
16 devices. '712 Patent at 4:39-42.

17 Based on Defendant’s present understanding of Plaintiff’s Infringement Contentions and
18 apparent interpretation of the scope of the Asserted Claims, at least one or more of these claim terms,
19 phrases, and limitations are not described in the specification of the Asserted Patent and do not
20 enable a person of ordinary skill in the art to practice the claimed invention without undue
21 experimentation or to distinguish all operative embodiments from all nonoperative embodiments
22 without undue experimentation.

23 In addition to Defendant’s contentions regarding the specifically listed terms above,
24 Defendant contends that UCT has failed to identify specific support for each limitation of each
25 Asserted Patent in its Infringement Contentions, and instead points to the same or similar
26 information as satisfying each claim limitation. Defendant therefore contends that there is no written
27 description support for the identified, described, or explained in the specification of the Asserted
28

1 Patents to enable a person of ordinary skill in the art to practice the claimed invention under the
2 wide claim scope UCT appears to be contending applies.

3 The written description and enablement issues identified above apply to all claims that
4 include the identified limitations, either explicitly or through claim dependency, and are not limited
5 to the exemplary claims listed above.

6 **C. Invalidity of the '712 Patent Based on 35 U.S.C. § 112, ¶ 2**

7 Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of
8 the '712 Patent, to the extent such positions can be understood from Plaintiff's Infringement
9 Contentions, Defendant asserts that the Asserted Claims of the '712 Patent are invalid for reciting
10 at least the following claim terms, phrases, or limitations:

- 11 • **“a load detector connected to the switch and configured to read a load current flowing**
12 **therethrough so as to detect a load in one of the connected devices, and to extract**
13 **information about the connected device based on the load current” (claim 1):** The term
14 “load detector” is not explicitly defined in the specification, and the specification does not
15 sufficiently disclose to a person of ordinary skill in the art whether the load current is flowing
16 through the switch or separately flowing through the load detector, and where the detection
17 takes place (e.g., the load detector, the switch, or somewhere else). '712 Patent at 4:59-63
18 (describing only a load detector 450 that “detects current flow therethrough”).
- 19 • **“a signature resistor connected to the switch and configured to detect a power source**
20 **from one or more of the connected devices;” (claim 1):** The term “signature resistor” is
21 not explicitly defined in the specification, and the specification does not disclose in sufficient
22 detail to a person of ordinary skill in the art how a “signature resistor” is configured to detect
23 a power source from the connected devices.” '712 Patent at 4:39-42.

24 These claim terms, phrases, limitations, and all dependent claims thereof, as apparently
25 construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112 at least because they
26 fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

27 Based on Defendant's present understanding of Plaintiff's Infringement Contentions, at least
28 one or more of these claim terms, phrases, and limitations are indefinite because they are

1 inconsistent with and broader than the alleged invention disclosed in the specification and during
2 prosecution, and given Plaintiff's apparent constructions of the claims, a person of ordinary skill in
3 the art at the time of the invention would not understand what is claimed with reasonable certainty,
4 even when the claims are read in light of the specification and prosecution history.

5 **VIII. THE ASSERTED CLAIMS OF THE '520 PATENT ARE INVALID**

6 **A. Identification of Prior Art**

7 Defendant contends that the prior art references charted in Exhibits F-1 through F-11,
8 discussed in any incorporated IPR petition, and/or described below anticipate and/or render obvious,
9 alone or in combination, one or more of the Asserted Claims of the '520 Patent.

10 **1. The '520 Patent Claims Are Anticipated by the Prior Art**

11 Some or all of the Asserted Claims of the '520 Patent are invalid as anticipated under 35
12 U.S.C. § 102 in view of each of the prior art references identified in the claim charts included in
13 Exhibit F-1 through F-11 and/or identified in any incorporated IPR petition, which identify specific
14 examples of where each limitation of the Asserted Claims is found in the prior art references. As
15 explained above, the cited portions of prior art references identified in the attached claim charts are
16 exemplary in nature and representative of the content and teaching of the prior art references, and
17 should be understood in the context of the reference as a whole and as they would be understood by
18 a person of ordinary skill in the art.

19 In addition to references identified in any incorporated IPR petition, Defendant identifies the
20 following references as anticipating one or more of the Asserted Claims of the '520 Patent under 35
21 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an
22 admission that any reference not listed below does not also anticipate the claims of the '520 Patent.
23 Further, Defendant contends that any prior art reference in the attached charts that is charted for
24 each limitation of any given claim, anticipates that claim, regardless of whether that prior art
25 reference is listed in the following tables.

26 **a) Prior Art Patents and Applications**

27

Number	Published/Issued Date	Short Name	Exhibit Number
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1	U.S. Patent Pub. No. 2008/0084834	Filed: Oct. 9, 2006 Pub'd: April 10, 2008	Stanek	F-1
2	U.S. Patent Pub. No. 2006/0095596	Filed: Nov. 3, 2004 Pub'd: May 4, 2006	Yung	F-2
3	WIPO Patent Pub. No. 2008/117234	Filed: Mar. 25, 2007 Pub'd: Oct. 2, 2008	Van Willigen	F-3
4	U.S. Patent Pub. No. 2008/0247544	Filed: April 2, 2007 Pub'd: Oct. 9, 2008	Candelore	F-4
5	U.S. Patent Pub. No. 2006/0076977	Filed: Sep. 20, 2004 Pub'd: Apr. 23, 2006	Zhu	F-5
6	U.S. Patent No. 6,574,233	Filed: Apr. 9, 1999 Pub'd: June 3, 2003	Fuller	F-6
7	U.S. Patent No. 7,639,765	Filed: July 14, 2006 Pub'd: Dec. 29, 2009	Suzuki	F-8
8	U.S. Patent Pub. No. 2007/0200859	Filed: Jan. 31, 2007 Pub'd: Aug. 30, 2007	Banks	F-9
9	U.S. Patent No. 5,928,345	Filed: Sep. 30, 1996 Pub'd: July 27, 1999	Tetzlaff	
10	U.S. Patent Pub. No. 2005/0021892	Filed: July 22, 2004 Pub'd: Jan. 27, 2005	Kim	
11	WIPO Patent Pub. No. 2007/074611	Filed: Dec. 5, 2006 Pub'd: July 5, 2007	Takatsuji	
12	U.S. Patent Pub. No. 2006/0104396	Filed: Oct. 18, 2005 Pub'd: May 18, 2006	Soriano	
13	U.S. Patent No. 10,033,553	Filed: Nov. 22, 2007 Pub'd: July 24, 2018	Ichimura	
14	U.S. Patent No. 7,558,326	Filed: Sep. 12, 2001 Pub'd: Jul. 7, 2009	Lyle	F-10

b) Prior Art Publications

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
Philips Semiconductors	The I ² C-Bus Specification	Dec. 1998	I2C Specification	F-7
Srikanth Mujiga & Srihari Sukumaran	Modeling and Test Generation Using SAL for Interoperability Testing in Consumer Electronics	Nov. 6, 2007	Mujiga	F-9
HDMI Licensing, LLC	High-Definition Multimedia Interface Specification, Version 1.3a	Nov. 10, 2006	HDMI 1.3a Specification	
HDMI Licensing, LLC	High-Definition Multimedia Interface Specification,	Nov. 10, 2006	HDMI-CEC Supplement	

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
Raida Al-Alawi & A. J. Al-Sammak	Version 1.3a, Supplement 1 – Consumer Electronics Control (CEC) Design of a Multicode Bi-Phase Encoder for Data Transmission	February 2006	Al-Alawi	

c) Prior Art Systems

On information and belief, systems implementing the protocols identified below were in public use, on sale, or otherwise available to the public before the priority date of the '520 Patent. Defendant's further investigation and/or subsequent discovery from Plaintiff or third parties with knowledge regarding prior art systems may reveal additional relevant prior art systems and/or further information regarding the systems identified below, or other relevant prior art systems. Defendant reserves the right to supplement these Invalidity Contentions, based on subsequent investigation and discovery, including from third parties.

System	Available At Least As Of	Short Name	Exhibit Number
Devices implementing I2C bus, v. 2.0 or earlier	Dec. 1998	I2C	F-7
Devices implementing USB 2.0 or earlier and/or USB on-the-go revision 1.0a	February 2006	USB 2.0/USB-OTG	F-9
HDMI version 1.3a or earlier and the HDMI-CEC supplement	Nov. 10, 2006	HDMI 1.3a / HDMI-CEC	F-9
Silicon Image DVI audio system and protocol known as PanelLink	March 26, 2001	SIL-DVI	F-11

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the '520 Patent, Defendant contends that any

1 difference between that prior art and the corresponding patent claim would have been either inherent
2 in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically
3 denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

4 **2. The '520 Patent Claims Are Obvious Over the Prior Art**

5 To the extent Plaintiff argues that any limitation of the asserted claims of the '520 Patent are
6 not explicitly disclosed by an item of prior art identified above, in Exhibits F-1 through F-11, or
7 discussed in any incorporated IPR petition, any purported differences are such that the claimed
8 subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged
9 invention, in view of the state of the art and knowledge of those skilled in the art. The item of prior
10 art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

11 Furthermore, it would have been obvious to combine any of the prior art in Exhibits F-1
12 through F-11 with each other, at least because all of these references relate to transmission of
13 information from a transmitting device to a receiving device over a control bus, and determining
14 which device has control of the bus.

15 For example, U.S. Patent Publication No. 2008/0084834 ("Stanek") teaches "[s]ystems and
16 methods for serial data transmission having at least two different operating modes dependent on the
17 connected signaling device." Stanek, Abstract. Stanek further discloses that "[f]or HDMI
18 compatible devices, a control channel is formed of three lines (SCL, SDA and DDC/CEC ground).
19 Control signals are transmitted on this channel in accordance with the I2C bus protocol. The device
20 may be able to detect and analyze these control signals and thus conclude the presence of a HDMI
21 device when the correct signal sequence is detected." *Id.* ¶ 46.

22 U.S. Patent Publication No. 2006/0095596 ("Yung") teaches "a method and a device for a
23 host control unit to communicate over a protocol compliant bus via the introduction of an auxiliary
24 control unit that handles communications to and from the protocol compliant bus." Yung, ¶ 7. Yung
25 further teaches that "[w]hen acting as an initiator, the command control unit is adapted to receive a
26 high-level command from a host control unit, and convert and transmit the high-level command to
27 a remote command control unit via a bi-directional link in a format of frame. When acting as a
28 follower, the command control unit is adapted to receive high-level commands from the bi-

1 directional link as frames, and convert and send the frames to the host control unit as high-level
2 commands.” *Id.* ¶ 10.

3 WIPO Patent Publication No. 2008/117234 (“Van Willigen”) teaches “a method of
4 distributing audio-visual data between a first audio-visual device and a second audio-visual device
5 using a digital display interface defined by an industry standard, the interface comprising a set of
6 lines, the interface comprising a first transport channel for carrying video data in uncompressed
7 form, the method comprising, at the first audio-visual device: sending or receiving audio-visual data
8 in a compressed form using a second transport channel of the interface, wherein the second transport
9 channel uses a subset of lines of the interface which are reserved in the standard for a different use.”
10 Van Willigen, 4:8–15.

11 U.S. Patent Publication No. 2008/0247544 (“Candelore”) teaches “a method and apparatus
12 for authentication of communications in digital communication systems having multiple input
13 devices employing multiple interfaces.” Candelore, ¶ 3. Candelore further teaches that “the HDMI-
14 compatible device that is transmitting information may be referred to as a HDMI source device,
15 while the HDMI-compatible device receiving the transmitted information is referred to as a HDMI
16 sink device. It can be seen that audio, visual, control, status and CEC control information may be
17 transmitted via one cable in the system. Of course, in a bidirectional system in which information is
18 flowing both directions between various HDMI-compatible devices, such as between a TV and a
19 module, like a STB or SBB, each device will have an HDMI transmitter and HDMI receiver and
20 may be referred to as a source or sink device depending upon whether it is transmitting or receiving
21 information.” *Id.* ¶ 50.

22 U.S. Patent Publication No. 2006/0076977 (“Zhu”) teaches a “modified USB 1.1 system 200
23 including a microcontroller 205, an USB 1.1 device 201 and an USB 1.1 host 202 and the mixed
24 signal interface circuit 208 to communicate seamlessly with an USB 2.0 OTG device 209. The full
25 interface uses both software programming of the microcontroller device 205 and the hardware
26 interface 208. The USB 2.0 OTG device 209, which may be either single role (slave) or dual-role
27 (host/slave), is connected to the USB 1.1 system 200 through USB connectors 207 and 212 and USB
28 cable 210.” Zhu, ¶ 58.

1 U.S. Patent No. 6,574,233 (“Fuller”) teaches a “connection is a communications bus that has
2 a plurality of signal lines for conducting a first set of signals (a first protocol), including critical
3 control signal lines for conducting critical control signals of the first set of signals. The first device
4 transmits or receives the first set of signals on the signal lines, including transmitting and receiving
5 the control signals on the control signal lines. The first device also transmits or receives a second
6 set of signals (a second protocol) including control signals, on the signal lines other than the critical
7 control signal lines for the first protocol.” Fuller, 2:8–18. Fuller further teaches that “[a]t the
8 beginning of a bus 100 transaction cycle, a bus 100 interface circuit 110 of each device 104-105
9 checks whether its device is the bus master, at steps 300 and 350. (A device becomes bus master by
10 winning bus access contention, for example. Alternatively, the state of the system (active, standby)
11 determines who is bus master.)” Fuller, 3:35–40.

12 U.S. Patent No. 7,639,765 (“Suzuki”) teaches “an apparatus and a system which achieve
13 bidirectional communication over a single line.” Suzuki, 1:15-17. Suzuki further teaches that
14 “[s]ince CEC communication is bidirectional communication, a plurality of transmitters may
15 perform transmission simultaneously. Therefore, during transmission, bus arbitration needs to be
16 performed for a period of time defined by the standard, and the arbitration period gate pulse signal
17 S109 c indicating the arbitration period is output.” *Id.* at 9:11-17.

18 U.S. Patent No. 7,558,326 (“Lyle”) teaches “[a] communication system including a
19 transmitter, a receiver, and a TMDS-like link, in which video data is transferred between a
20 transmitter and a receiver and auxiliary data (typically including timing data associated with other
21 auxiliary data).” Lyle ‘326 at Abstract. In typical embodiments, the auxiliary data includes one or
22 more streams of audio data. *Id.* The system specifications provide various methods for sending,
23 receiving, and synchronizing auxiliary data with video data over such a link, with several proposed
24 configurations for data transmission. *Id.* at 6:25-10:5. The system further incorporates mechanisms
25 for monitoring device connectivity and includes clock recovery circuitry to synchronize data
26 transmission. *Id.* at 8:24-37, 15:44-62.

27 Philips Semiconductors, *The I2C-Bus Specification* (“I2C Specification”) teaches that “[t]wo
28 wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected

1 to the bus.” I2C Specification at 6. I2C Specification further teaches that “[t]he possibility of
2 connecting more than one microcontroller to the I²C-bus means that more than one master could try
3 to initiate a data transfer at the same time. To avoid the chaos that might ensue from such an event
4 - an arbitration procedure has been developed. This procedure relies on the wired-AND connection
5 of all I²C interfaces to the I²C-bus.” *Id.* at 7.

6 Srikanth Mujiga & Srihari Sukumaran, *Modeling and Test Generation Using SAL for*
7 *Interoperability Testing in Consumer Electronics* (“Mujiga”) teaches that “The High-Definition
8 Multimedia Interface (HDMI) [1] is used to transmit digital audio-visual signals from source devices
9 like DVD players, set-top boxes, etc., to sink devices like television sets, projectors and other
10 displays. HDMI is capable of carrying high quality multi-channel audio data and all standard and
11 high-definition consumer electronics video formats. HDMI includes three separate communication
12 channels, TMDS channel for carrying all audio and video data as well as auxiliary data, the DDC
13 channel, which is used by an HDMI source to determine the capabilities and characteristics of the
14 sink and the CEC channel which is used for high-level user functions such as automatic setup tasks
15 or tasks typically associated with infrared remote control usage.” Mujiga at 33. Mujiga further
16 teaches that ““CEC is based on a bus system and all the transactions on the CEC bus consist of an
17 initiator and one or more followers. The initiator sends the CEC frame (CEC message and data) and
18 the followers respond to the CEC message. There can be only one CEC frame at any time on the
19 CEC channel. The CEC bus arbitration ensures collisions are spotted and reliable messaging can be
20 achieved. It does this in a completely static priority-based manner based on the device’s logical
21 address.” *Id.* at 34.

22 HDMI Licensing, LLC, *High-Definition Multimedia Interface Specification, Version 1.3a*
23 (“HDMI 1.3a Specification”) and HDMI Licensing, LLC, *High-Definition Multimedia Interface*
24 *Specification, Version 1.3a, Supplement 1 – Consumer Electronics Control (CEC)* (“HDMI-CEC
25 Supplement”) together teach an interface “for transmitting digital television audiovisual signals
26 from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and
27 other video displays. HDMI can carry high quality multi-channel audio data and can carry all
28 standard and high-definition consumer electronics video formats. Content protection technology is

1 available. HDMI can also carry control and status information in both directions.” HDMI 1.3a
2 Specification at 1. The HDMI-CEC Supplement further discloses that “[t]he initiator provides bit
3 timing and bit leading edges. Only one initiator is allowed at any one time. A control signal line
4 arbitration mechanism avoids conflict when more than one initiator begins transmitting at the same
5 time.” HDMI-CEC Supplement at CEC-8.

6 U.S. Patent Publication No. 2007/0200859 (“Banks”) teaches “a system video and audio
7 source device that is coupled to a system video and audio sink through a serial link in a cable.”
8 Banks, ¶ 10. Banks further teaches that “a parallel HDMI bus transports control signals during
9 control periods 402 and 406 and transports data signals during data periods 404 and 408.” *Id.* ¶ 42.
10 Banks further teaches that “specific control and data signals can be transported over any of the ports
11 shown and during any appropriate interval.” *Id.* ¶ 44.

12 U.S. Patent No. 5,928,345 (“Tetzlaff”) teaches “a new data bus system and protocol for
13 communication between master control nodes and peripheral devices.” Tetzlaff, 1:6–7. Tetzlaff
14 further discloses that “[d]ata bus 220 also includes a single CS line coupled to the CS output of
15 master node microprocessor 200 and to the CS inputs of each of the slave nodes. The CS signal on
16 the CS data bus line is generated by one of the master nodes and indicates that the data bus is active.
17 It can be used as a delimiter between messages or to indicate which data bus is active if the master
18 node is controlling multiple data buses.” *Id.* at 4:49–55.

19 U.S. Patent Publication No. 2005/0021892 (“Kim”) teaches “a system for transferring data
20 between a mobile terminal and computer” and “[a] data transfer process between the terminal and
21 computer.” Kim, ¶¶ 5–6. Such data transfer, Kim discloses, “is accomplished when the terminal
22 transmits a control signal to the computer through a control line of a USB cable based on a value
23 stored in a terminal register unit.” *Id.* at Abstract. Kim further discloses that “[a] computer register
24 unit 31 includes a line control register 32 for receiving a control signal through the control line of
25 the USB cable, and a status register 33 for indicating a data reception status from the terminal. The
26 terminal register unit and computer register unit are connected to the control line of the USB cable.”
27 *Id.* ¶ 22.

1 WIPO Patent Publication No. 2007/074611 (“Takatsuji”) teaches that “by transmitting
2 control signals bidirectionally between TV, AV amplifier and DVD player, it is possible to operate
3 the entire home theater with one remote control.” Takatsuji, ¶ 2. Takatsuji further teaches “using a
4 CEC bus which is a bidirectional connection, in order to control by bidirectional communication
5 among the respective devices.” *Id.* ¶ 22. Takatsuji further discloses that “[a] CEC message has a
6 basic frame structure called ‘block’ and consists of one or more blocks. Each 1-bit EOM and ACK
7 field always exists every 1 block, and every block is used in the same manner.” *Id.* ¶ 13.

8 U.S. Patent Publication No. 2006/0104396 (“Soriano”) teaches that “[a] serial bus system
9 for data communication between devices according to a master-slave protocol has a data bus
10 connecting master and slave devices and a shared clock system arranged to provide a shared-clock
11 signal to the master and slave devices.” Soriano, Abstract. Soriano further teaches that “[t]he
12 described embodiments of the bus system are arranged for data exchange between electronic
13 devices, such as microprocessors, memory, I/O chips, controllers, sensors, etc. The data exchanged
14 may be control data to control the devices connected to the bus; a bus of this kind is sometimes
15 called a “control bus” (of course, a control bus may also exchange “content data”).” *Id.* ¶ 26.

16 U.S. Patent No. 10,033,553 (“Ichimura”) teaches that “[a] video signal and an audio signal
17 are TMDS transmitted from a source device to a sink device. Through a reserved line and a HPD
18 line provided separately from a TMDS transmission line, an Ethernet™ signal is bidirectionally
19 transmitted, and also, a SPDIF signal is transmitted from the sink device to the source device.”
20 Ichimura, Abstract. Ichimura further teaches that “with respect to HDMI standards, a consumer
21 electronics control (CEC) line 361, a reserved line 362, a hot plug detect (HPD) line 363, and the
22 like, are provided. The CEC line 361 is a line for a bidirectional communication of device control
23 signals. Whereas the display data channel 350 connects devices in a one-to-one manner, the CEC
24 line directly connects all devices connected to HDMI.” *Id.* at 5:51-57.

25 Raida Al-Alawi & A. J. Al-Sammak, *Design of a Multicode Bi-Phase Encoder for Data*
26 *Transmission* (“Al-Alawi”), teaches that “[a]dvances in data transmission and various digital
27 communications network architectures have resulted in an increased demand to multimedia
28 applications where data, voice, images and video signals are to be transmitted. These networks are

1 becoming very large, and often their nodes have several different connections between them
2 utilizing more than one protocol. Different protocols normally employ different line (modulation)
3 codes, and hence, it is important to develop a controller in the physical layer that can cope with
4 multiple protocols.” Al-Alawi at 2.

5 The Silicon Image PanelLink system, on information and belief, implemented at least the
6 Digital Visual Interface (DVI) 1.0 specification, which is a standard for the transmission of high-
7 speed digital video content over a display technology independent interface. DVI at 1. The interface
8 is primarily focused on, but not limited to, providing a connection between a computer and a display
9 device through a high speed serial interface. DVI at 1. DVI is based on the panelLink serial format
10 and utilizes transition minimized differential signaling (TMDS), a high speed serial linking
11 technology to send data from a digital transmitting device to a receiving device. DVI at 2.1. The
12 Silicon Image DVI audio system and protocol known as PanelLink was described in at least the
13 following documents:

- 14 • David Lieberman, “PC video interface looks to add audio capability,” EE Times,
15 (Mar. 26, 2001) (“PC audio”)
- 16 • “Silicon Image First to Couple Digital Audio and Video On the DVI Link,” Silicon
17 Image (Jan. 16, 2001) (“DVI Audio LINK”)
- 18 • “Digital Video Interface DVI revision 1.0,” (Apr. 2, 1999) (“DVI 1.0”)
- 19 • Lyle (Exhibit F-10)
- 20 • VESA Display Data Channel Standard, Version 3 (Dec.15, 1997) (“DDC”)

21 Accordingly, because each of the identified references are directed to similar devices in the
22 similar field of endeavor, a person of ordinary skill in the art would be motivated to combine the
23 teachings of two or more references together because the references disclose similar systems that
24 solve the same problems in similar ways. Thus, it would have been obvious to one of ordinary skill
25 in the art to combine any of the foregoing references and one of ordinary skill would have expected
26 such a combination to be successful.

27 To the extent that it is determined that any of the above references do not disclose a control
28 bus that is “bi-directional” and “single-line,” it would further have been obvious to modify the

1 teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Yung,
2 ¶ 27 (“The CEC bus preferably consists of a single, bi-directional line. Each node is connected via
3 the bi-directional CEC bus, thus allowing any CEC node to create a map of the network.”); Van
4 Willigen, 8:22–24 (“Line 13 is used for a Consumer Electronics Control (CEC) Channel which is
5 optional to implement, but mandatory to wire. This is a one-wire bidirectional bus which is generally
6 used for AV Link remote control signaling.”); Candelore, ¶ 50 (“FIG. 3 references an exemplary
7 HDMI System Block Diagram, said system transmitting CEC commands over a single cable.”);
8 Zhu, ¶ 59 (“USB cabling consists of D+ and D– data lines, 316 and 317 respectively, Vbus (power
9 supply) line 318, GND 319 and USB ID detect line 320.”); I2C Specification at 6 (“Two wires,
10 serial data (SDA) and serial clock (SCL), carry information between the devices connected to the
11 bus.”), 8 (“Both SDA and SCL are bi-directional lines, connected to a positive supply voltage via a
12 current-source or pull-up resistor (see Fig.3).”); Suzuki, 7:44-48 (“An N-channel MOS transistor
13 open drain terminal (TR) 113 receives and outputs the CEC signal S113 a which is connected to a
14 communication party on the other end. The CEC signal S113 a is on a single signal line where a
15 pull-up resistance is provided.”); Mujiga at 34 (“CEC is based on a bus system and all the
16 transactions on the CEC bus consist of an initiator and one or more followers. The initiator sends
17 the CEC frame (CEC message and data) and the followers respond to the CEC message.”); HDMI
18 1.3a Specification at 112 (“The CEC channel is optionally used for higher-level user functions such
19 as automatic setup tasks or tasks typically associated with infrared remote control usage.”); Tetzlaff,
20 4:49–53 (“Data bus 220 also includes a single CS line coupled to the CS output of master node
21 microprocessor 200 and to the CS inputs of each of the slave nodes. The CS signal on the CS data
22 bus line is generated by one of the master nodes and indicates that the data bus is active.”); Kim, ¶
23 19 (“The data transfer system includes a USB cable 20 having a control line, a terminal 10 provided
24 with a data port (not shown) and a terminal register unit 11, and a computer 30 provided with a USB
25 port (not shown) and a computer register unit 31.”); Takatsuji, ¶ 2 (“In addition, the HDMI standard
26 specifies a protocol CEC (Consumer Electronics Control) for bidirectionally transmitting a control
27 signal.”); Soriano, ¶ 5 (“The I2C-bus is a multi-master bus which means that the role of the master
28 may be taken by different devices. The bus has two lines, a serial data line (SDA) and a serial clock

1 line (SCL). The serial data line carries the data between the devices connected to the bus.”);
2 Ichimura, 5:51-57 (“In addition, with respect to HDMI standards, a consumer electronics control
3 (CEC) line 361, a reserved line 362, a hot plug detect (HPD) line 363, and the like, are provided.
4 The CEC line 361 is a line for a bidirectional communication of device control signals. Whereas the
5 display data channel 350 connects devices in a one-to-one manner, the CEC line directly connects
6 all devices connected to HDMI.”). Therefore, a person of ordinary skill in the art would be
7 motivated to make such a combination.

8 To the extent that it is determined that any of the above references do not disclose a process
9 for conducting “arbitration” of the control bus, it would further have been obvious to modify the
10 teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Yung,
11 ¶ 38 (“If there is any other device sending the same simultaneously, the arbitration process is
12 conducted (block 125). The arbitration process determines which device has higher priority to have
13 control of the command bus.”); Fuller, 3:35–40 (“At the beginning of a bus 100 transaction cycle, a
14 bus 100 interface circuit 110 of each device 104-105 checks whether its device is the bus master, at
15 steps 300 and 350. (A device becomes bus master by winning bus access contention, for example.
16 Alternatively, the state of the system (active, standby) determines who is bus master.”); I2C
17 Specification at 7 (“The possibility of connecting more than one microcontroller to the I²C-bus
18 means that more than one master could try to initiate a data transfer at the same time. To avoid the
19 chaos that might ensue from such an event - an arbitration procedure has been developed.”); Mujiga
20 at 34 (“The CEC bus arbitration ensures collisions are spotted and reliable messaging can be
21 achieved. It does this in a completely static priority-based manner based on the device’s logical
22 address.”); HDMI-CEC Supplement at CEC-15 (“Arbitration for the CEC line ensures collisions
23 are spotted and a reliable message layer can be achieved.”); Tetzlaff, 5:35–37 (“The above described
24 arbitration method also aids in facilitating bi-directional communications.”); Soriano, ¶ 30 (“In such
25 protocols, typically an arbitration procedure is defined which governs access to the bus in the case
26 of bus-access conflicts.”). Therefore, a person of ordinary skill in the art would be motivated to
27 make such a combination.
28

1 To the extent that it is determined that any of the above references do not disclose a
2 “transmitting device” that is a “mobile device,” it would further have been obvious to modify the
3 teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Zhu,
4 ¶ 14 (“USB On-the-Go (OTG) is a new USB communication protocol specified in the USB 2.0
5 specification. USB OTG allows peer-to-peer communications between two USB OTG devices
6 enabling, for example, a digital camera to directly communicate with a printer without the need of
7 a PC as a host.”); I2C Specification at 4 (“In consumer electronics, telecommunications and
8 industrial electronics, there are often many similarities between seemingly unrelated designs. For
9 example, nearly every system includes . . . [a]pplication-oriented circuits such as digital tuning and
10 signal processing circuits for radio and video systems, or DTMF generators for telephones with tone
11 dialling.”); HDMI 1.3a Specification at 10 (“A device’s external HDMI connection shall be
12 presented via one of the three specified HDMI connectors, Type A, Type B or Type C. . . . The
13 Type C connector carries the same signals as the Type A but is more compact and intended for
14 mobile applications.”); Tetzlaff, 1:34–38 (“Frequently, the master node in a process control
15 instrument is a Motorola or compatible microprocessor or microcontroller. For example, the
16 Motorola 68HC05 and 68HC11 microcontrollers are commonly used as the master node in process
17 control instruments.”); Kim, Fig. 2. Therefore, a person of ordinary skill in the art would be
18 motivated to make such a combination.

19 To the extent that it is determined that any of the above references do not disclose a
20 “modified protocol,” it would further have been obvious to modify the teachings of that reference
21 to include this feature in view of the following teachings: *See, e.g.*, Yung, ¶ 27 (“The optional CEC
22 protocol provides high-level control functions between all of the CEC compliant nodes in the CEC
23 network.”); Van Willigen, 8:30–32 (“In a preferred embodiment of the invention, lines 13 and 14
24 of a Type A connector are not used in the way specified by the HDMI standard (at least as defined
25 by HDMI 1.0-1.3) but are used as a bi-directional channel for carrying compressed AV content.”);
26 Candelore, ¶ 56 (“Interface 1 may be considered the normal HDMI CEC signal path that is
27 unacceptably slow while Interface 2 is the enhanced, faster data transmission path. As will be
28 described, Interface 2 may rely upon a faster signal path through the HDMI connector, as illustrated

1 in FIG. 6 or it may be based upon another protocol entirely such as USB, as shown in FIG. 7.
2 Moreover, Interface 2 may be used instead of, or in addition to, the original HDMI CEC Interface
3 1. “); Zhu, ¶ 14 (“USB On-the-Go (OTG) is a new USB communication protocol specified in the
4 USB 2.0 specification. USB OTG allows peer-to-peer communications between two USB OTG
5 devices enabling, for example, a digital camera to directly communicate with a printer without the
6 need of a PC as a host.”); Fuller, 1:45–52 (“The second device presents a first interface (e.g., uses a
7 first protocol) over the connection, while the third device presents a second interface (e.g., uses a
8 second protocol) different from the first interface over the connection. The second interface provides
9 capabilities different from (e.g., additional to, or that cannot be provided by) those provided by the
10 first interface.”); Kim, ¶ 19 (“The data transfer system includes a USB cable 20 having a control
11 line, a terminal 10 provided with a data port (not shown) and a terminal register unit 11, and a
12 computer 30 provided with a USB port (not shown) and a computer register unit 31.”); Ichimura,
13 6:35-38 (“As described above, the reserved line 362 is, a line not utilized in HDMI standards.
14 However, in the present case, the reserved line 362 is being used to detect the type of a device that
15 is connected for the sake of efficient use of a pin.”). Therefore, a person of ordinary skill in the art
16 would be motivated to make such a combination.

17 To the extent that it is determined that any of the above references do not disclose a data
18 packet followed by an “acknowledge (ACK) message,” it would further have been obvious to
19 modify the teachings of that reference to include this feature in view of the following teachings:
20 *See, e.g.,* Yung, ¶ 38 (“At block 128, each byte of the command received from the host control unit
21 is converted to a 10-bit command block by adding an “end of message” (EOM) bit, and an
22 acknowledgement (ACK) bit.”), ¶ 39 (“The follower receives each bit, combines bits into bytes and
23 sends an acknowledgement for each byte.”); I2C Specification at 10 (“If a slave can’t receive or
24 transmit another complete byte of data until it has performed some other function, for example
25 servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait
26 state. . . . Usually, a receiver which has been addressed is obliged to generate an acknowledge after
27 each byte has been received, except when the message starts with a CBUS address (see Section
28 10.1.3).”); HDMI-CEC Supplement at CEC-12 (“The ACK bit is used by follower(s) to

1 acknowledge the data or header block. It is always set to 1 by the initiator.”); Takatsuji, ¶¶ 18–19.
2 Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

3 To the extent that it is determined that any of the above references do not disclose “bi-phase
4 mark encoding,” it would further have been obvious to modify the teachings of that reference to
5 include this feature in view of the following teachings: *See, e.g.*, Yung, ¶ 38 (“The 10-bit command
6 block is converted to command signaling by converting 0s into logical 0s, and 1s into logical 1s
7 (block 128). The implementation of logical 0s and logical 1s can be defined by the designers,
8 providing the implementation is recognizable by both initiators and followers. The preferred
9 implementation is provided in the CEC protocol, which use the durations of high and low Voltages
10 to distinguish logical 0s and logical 1s.”); Soriano, ¶ 28 (“The binary data may be coded by the
11 electrical signals in various ways, e.g. by the NRZ Code, the RZ Code, the AMI Code, the
12 Manchester Code, the differential Manchester Code, etc.”); Ichimura, 2:10-15 (“Furthermore,
13 according to the first aspect, the second signal may be a signal including a clock component.
14 Thereby, an effect that the clock component is transmitted to the external device is achieved. Here,
15 as an example, the second signal may include a biphasemark modulated signal.”); Al-Alawi at 3
16 (“Several line coding techniques suitable for data transmission have been devised. Among these
17 codes are Bi-Phase-Level (Bi-Φ-L), Bi-Phase-Mark (Bi-Φ-M), Bi-Phase-Space (Bi-Φ-S),
18 Differential Manchester (DM) and Inverse Differential Manchester (IDM) codes. These widely used
19 codes belong to the Bi-Phase code family which is characterized by having at least one transition
20 per bit time.”). Therefore, a person of ordinary skill in the art would be motivated to make such a
21 combination.

22 To the extent that it is determined that any of the above references do not disclose a
23 “switchable pull-up circuit” on the control bus, it would further have been obvious to modify the
24 teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Zhu,
25 ¶ 74 (“B-device 327 detects in block 310 that bus is idle for more than 3 mS and begins (HNP) by
26 turning off pull-up on D+. This pull-up is contained within block 312. This allows the bus to
27 discharge to the session end zero SEO state.”); I2C Specification at 22 (“After each acknowledge
28 bit (A) or not-acknowledge bit (A) the active master disables its current-source pull-up circuit. This

1 enables other devices to delay the serial transfer by stretching the LOW period of the SCLH signal.
2 The active master re-enables its current-source pull-up circuit again when all devices have released
3 and the SCLH signal reaches a HIGH level, and so speeds up the last part of the SCLH signal's rise
4 time."); HDMI-CEC Supplement at 7 ("For example, this can be implemented by connecting an
5 isolating diode between the CEC input pin and the internal pull-up circuit, such that diode is reverse-
6 biased in the off state with an external device pulling-up the CEC line."); Ichimura, 9:64-10:1
7 ("Similarly, when the source device 100 is of a specific type, pull-up is performed by the resistor
8 111 and the potential of the reserved line 362 becomes 2.5V, and when the source device 100 is not
9 of a specific type, the potential becomes 0V."). Therefore, a person of ordinary skill in the art would
10 be motivated to make such a combination.

11 To the extent that it is determined that any of the above references do not disclose allowing
12 "the transmitting device to take control of the first control bus if the transmitting device and the
13 receiving device arbitrate use of the first control bus at the same time," it would further have been
14 obvious to modify the teachings of that reference to include this feature in view of the following
15 teachings: *See, e.g.*, Fuller, 3:35-40 ("At the beginning of a bus 100 transaction cycle, a bus 100
16 interface circuit 110 of each device 104-105 checks whether its device is the bus master, at steps
17 300 and 350. (A device becomes bus master by winning bus access contention, for example.
18 Alternatively, the state of the system (active, standby) determines who is bus master.)"); HDMI-
19 CEC Supplement at CEC-15 ("It should be noted that this process gives priority to the logical
20 address with the most leading zeros and, ultimately, the TV.") Therefore, a person of ordinary skill
21 in the art would be motivated to make such a combination.

22 A person skilled in the art would have been motivated to combine any of the above
23 references. In particular, the combinations identified herein would merely have been (a) a
24 combination of prior art elements according to known methods to yield predictable results; (b) a
25 simple substitution of one known element for another to obtain predictable results; (c) a use of
26 known technique to improve similar devices or methods in the same way; (d) application of a known
27 technique to a known device or method ready for improvement to yield predictable results; (e)
28 obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in

1 either the same field or a different one based on design incentives or other market forces since the
2 variations are predictable to one of ordinary skill in the art. Moreover, a person of ordinary skill in
3 the art had a reason to combine these references because—at a minimum—they all pertain to
4 transmission of information from a transmitting device to a receiving device over a control bus.

5 As discussed above, the motivation to combine the teachings of the patents and other prior
6 art referenced above is found in the art as specified in the charts and in: (1) the nature of the problem
7 being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of
8 persons of ordinary skill in the art; and (4) the fact that the prior art is generally directed towards
9 signal processing in microphone array systems, and (5) the predictable results obtained in combining
10 the different elements of the prior art. The Supreme Court has held that a showing of a motivation
11 to combine within the references themselves is not required to prove obviousness. *See KSR*, 550
12 U.S. at 401 (“Any need or problem known in the field of endeavor at the time of invention may
13 provide the motivation to combine.”).

14 For example, a person skilled in the art would have been motivated to combine Stanek with
15 Yung, Zhu, Candelore, Kim, and/or additional references discussed above and disclosed in Exhibits
16 F-1 through F-11 for the reasons provided above. Moreover, the combination of references is no
17 more than a combination of systems all directed communication between computing devices over a
18 control bus. Additionally, the combination reflects no more than a simple substitution of known
19 elements for one another to obtain predictable results. For example, a simple addition of Yung’s
20 arbitration process and bi-phase mark encoding to the system disclosed in Stanek would yield a
21 predictable result. As another example, a person of ordinary skill in the art would have been
22 motivated to implement Zhu’s switchable pull up circuit on a control bus of the HDMI connection
23 in Stanek. Indeed, Candelore discloses that the CEC control bus of the HDMI standard can be
24 modified to enhance the speed of any communications. Additionally, a skilled artisan could easily
25 incorporate Kim’s teachings that communication can occur over a control bus to make Stanek
26 compatible with mobile devices.

27 A person skilled in the art would have been motivated to combine Stanek, Yung, Van
28 Willigen, Candelore, and/or Suzuki with Mujiga, the HDMI 1.3a Specification, the HDMI-CEC

1 Supplement, Takatsuji, and/or additional references discussed above and disclosed in Exhibits F-1
2 through F-11 for the reasons provided above. Moreover, the combination of references is no more
3 than a combination of systems all directed communication between computing devices over a
4 control bus. The Stanek, Yung, Van Willigen, and Candelore references all disclose communication
5 using the HDMI standard and, specifically, the CEC line of that standard. A person of ordinary skill
6 in the art would have easily combined those references with the teachings of Mujiga, the HDMI 1.3a
7 Specification, the HDMI-CEC Supplement, Takatsuji, and other references to implement the HDMI
8 standard and the CEC bus. For example, to the extent such features are not inherent in the
9 references, a skilled artisan would be aware of and could easily incorporate the HDMI-CEC
10 Supplement's arbitration process and/or switchable pull up circuit into the system disclosed in any
11 reference incorporating the HDMI standard, due to those references' express reliance on the HDMI
12 standard.

13 A person skilled in the art would have been motivated to combine Stanek, Yung, Van
14 Willigen, Candelore, and/or Suzuki with Soriano, Ichimura, Al-Alawi and/or additional references
15 discussed above and disclosed in Exhibits F-1 through F-11 for the reasons provided above.
16 Moreover, the combination of references is no more than a combination of systems all directed to
17 communication between computing devices over a control bus. The concept of bi-phase mark
18 coding (also known as "Manchester" coding) was well-known in the art as of the time of the '520
19 patent, as demonstrated by the Soriano, Ichimura, and Al-Alawi references. Because the above
20 references all relate to communication between devices over a control bus, a skilled artisan would
21 have been capable of simply substituting bi-phase mark coding for the coding approaches used in
22 Stanek, Yung, Van Willigen, Candelore, and/or Suzuki.

23 A person skilled in the art would have been motivated to combine Yung with Van Willigen
24 and/or additional references discussed above and disclosed in Exhibits F-1 through F-11 for the
25 reasons provided above. Moreover, the combination of references is no more than a combination
26 of systems all directed communication between computing devices over a control bus. For example,
27 a person of ordinary skill in the art would have been capable of making the simple substitution of
28 Van Willigen's modified HDMI protocol for the standard HDMI protocol disclosed in Yung.

1 Thus, in addition to the combinations discussed above, exemplary combinations which
2 render obvious some or all of the Asserted Claims of the '520 Patent are listed in **Appendix A**, Sec.
3 VI.

4 **B. Invalidity of the '520 Patent Based on 35 U.S.C. § 112, ¶ 1**

5 Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of
6 the '520 Patent, to the extent such positions can be understood from Plaintiff's Infringement
7 Contentions, Defendant asserts that the Asserted Claims of the '520 Patent are invalid for failure to
8 provide a written description that enables the full scope of the Asserted Claims based on at least the
9 following claim terms, phrases, or limitations:

- 10 • **“one of a plurality of different types of control signals” (claims 1, 8):** UCT appears to
11 interpret this claim limitation as referring to a single control signal from only one possible
12 control signal. There is no support for such an interpretation in the patent.
- 13 • **“connection” (claims 12, 19):** UCT appears to interpret this claim limitation as referring to
14 a component of a single transmitting or receiving device. There is no written description
15 support for such an interpretation in the patent. The patent consistently describes the
16 connection as being between two devices. *See, e.g.*, Figs. 1, 3, 5, 2:41-53, 6:24-48, and 7:48-
17 51.
- 18 • **“plurality of different control buses” (claim 8):** There is no written description support or
19 enablement in the specification for “the plurality of different types of control signals” to be
20 transmitted over a “plurality of different control buses,” including at least because the patent
21 does not describe different control buses of a standard protocol and does not explain how
22 unidentified control signals for transmission over a single first control bus would be
23 transmitted over multiple unidentified control buses, let alone within the context of the
24 claimed method, which describes only a “first control bus.”
- 25 • **“mobile device” (claims 1, 19):** There is no written description support or enablement in
26 the specification for a “mobile device” including a laptop, monitor, or any other device
27 accused of meeting this limitation by UCT.

1 Based on Defendant's present understanding of Plaintiff's Infringement Contentions and
2 apparent interpretation of the scope of the Asserted Claims, at least one or more of these claim terms,
3 phrases, and limitations are not described in the specification of the Asserted Patent and do not
4 enable a person of ordinary skill in the art to practice the claimed invention without undue
5 experimentation or to distinguish all operative embodiments from all nonoperative embodiments
6 without undue experimentation.

7 In addition to Defendant's contentions regarding the specifically listed terms above,
8 Defendant contends that UCT has failed to identify specific support for each limitation of each
9 Asserted Patent in its Infringement Contentions, and instead points to the same or similar
10 information as satisfying each claim limitation. Defendant therefore contends that there is no written
11 description support for the identified, described, or explained in the specification of the Asserted
12 Patents to enable a person of ordinary skill in the art to practice the claimed invention under the
13 wide claim scope UCT appears to be contending applies.

14 The written description and enablement issues identified above apply to all claims that
15 include the identified limitations, either explicitly or through claim dependency, and are not limited
16 to the exemplary claims listed above.

17 **C. Invalidity of the '520 Patent Based on 35 U.S.C. § 112, ¶ 2**

18 Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of
19 the '520 Patent, to the extent such positions can be understood from Plaintiff's Infringement
20 Contentions, the Asserted Claims of the '520 Patent are invalid for reciting at least the following
21 claim terms, phrases, or limitations:

- 22 • **"the receiving device is a device utilizing the standard protocol and the transmitting**
23 **device is a mobile device utilizing a modified protocol" (claim 19):** The '520 Patent does
24 not inform, with reasonable certainty, those skilled in the art about the scope of a "standard
25 protocol" or a "modified protocol." In particular, it is not clear whether a "standard" and
26 "modified" protocol are determined based on characteristics of a device that utilizes a given
27 protocol, whether the protocols appear in the same standards specifications or are
28 promulgated by the same standards organizations, etc.

- 1 • **“the modified protocol being a modification of the standard protocol that is not**
2 **included in the standard protocol” (claims 12 and 19):** The ‘520 Patent does not inform,
3 with reasonable certainty, those skilled in the art about the scope of a “standard protocol” or
4 a “modified protocol.” In particular, it is not clear whether a “standard” and “modified”
5 protocol are determined based on characteristics of a device that utilizes a given protocol,
6 whether the protocols appear in the same standards specifications or are promulgated by the
7 same standards organizations, etc.

8 These claim terms, phrases, limitations, and all dependent claims thereof, as apparently
9 construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112 at least because they
10 fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

11 At least claims 12 and 19 (and their dependent claims) of the ‘520 Patent are invalid under
12 35 U.S.C. § 112(2) because they are mixed method-apparatus claims under the doctrine of *IPXL*
13 *Holdings L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377 (Fed. Cir. 2005). In particular, at least the
14 following claim terms and phrases improperly recite a method of using the entire claimed apparatus
15 and/or functionality not tied to the capability of any recited structural element:

- 16 • “the transmitting device is operable for coupling with a receiving device via the first
17 control bus” (claim 12)
18 • “the receiving device is a device utilizing the standard protocol and the transmitting
19 device is a mobile device utilizing a modified protocol” (claim 19)

20 Based on Defendant’s present understanding of Plaintiff’s Infringement Contentions, at least
21 one or more of these claim terms, phrases, and limitations are indefinite because they are
22 inconsistent with and broader than the alleged invention disclosed in the specification and during
23 prosecution, and given Plaintiff’s apparent constructions of the claims, a person of ordinary skill in
24 the art at the time of the invention would not understand what is claimed with reasonable certainty,
25 even when the claims are read in light of the specification and prosecution history.

26 Additionally, at least Claims 12 and 19 (and their dependent claims) of the ‘520 Patent are
27 invalid under 35 U.S.C. §§ 112(2) and (6) because the ‘520 Patent does not disclose sufficient
28

1 structure corresponding to the function recited in at least the following means-plus-function claim
2 limitations:

- 3 • “logic to convert each of one or more control signals into a data packet each of the one or
4 more control signals being one of a plurality of different types of control signals for a
5 standard protocol, each data packet including a plurality of bits to be transmitted” (claim
6 12)
- 7 • “logic to arbitrate use of the first control bus, the logic to arbitrate use being operable to:
8 determine whether the control bus is in use by the receiving device, and if the first control
9 bus is not in use by the receiving device, conduct arbitration for control of the first control
10 bus” (claim 12)
- 11 • “logic to convert each of the one or more data packets into a control signal” (claim 19)
- 12 • “logic to arbitrate use of the first control bus, the logic to arbitrate use being operable to:
13 determine whether the control bus is in use by the transmitting device, and if the first
14 control bus is not in use by the transmitting device, conduct arbitration for control of the
15 first control bus” (claim 19)

16 The indefiniteness issues identified above apply to all claims that include the identified
17 limitations, either explicitly or through claim dependency, and are not limited to the exemplary
18 claims listed above.

19 **IX. THE ASSERTED CLAIMS OF THE '231 PATENT ARE INVALID**

20 **A. Identification of Prior Art**

21 Defendant contends that the prior art references charted in Exhibits G-1 through G-11,
22 discussed in any incorporated IPR petition, and/or described below anticipate and/or render obvious,
23 alone or in combination, one or more of the Asserted Claims of the '231 Patent.

24 **1. The '231 Patent Claims Are Anticipated by the Prior Art**

25 Some or all of the Asserted Claims of the '231 Patent are invalid as anticipated under 35
26 U.S.C. § 102 in view of each of the prior art references identified in the claim charts included in
27 Exhibit G-1 through G-11 and/or identified in any incorporated IPR petition, which identify specific
28 examples of where each limitation of the Asserted Claims is found in the prior art references. As

explained above, the cited portions of prior art references identified in the attached claim charts are exemplary in nature and representative of the content and teaching of the prior art references, and should be understood in the context of the reference as a whole and as they would be understood by a person of ordinary skill in the art.

In addition to references identified in any incorporated IPR petition, Defendant identifies the following references as anticipating one or more of the Asserted Claims of the '231 Patent under 35 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an admission that any reference not listed below does not also anticipate the claims of the '231 Patent. Further, Defendant contends that any prior art reference in the attached charts that is charted for each limitation of any given claim, anticipates that claim, regardless of whether that prior art reference is listed in the following tables.

a) Prior Art Patents and Applications

Number	Published/Issued Date/Filing Date	Short Name	Exhibit Number
U.S. Patent Pub. No. 2006/0280055	Filed: June 8, 2006 Pub'd: Dec. 14, 2006	Miller '055	G-1
U.S. Patent Pub. No. 2007/0036158	Filed: Aug. 11, 2006 Pub'd: Feb. 15, 2007	Hun-Kwon	G-2
U.S. Patent No. 8,203,325	Filed: Sep. 7, 2007 Issued: June 19, 2012	Miller '325	G-3
U.S. Patent Pub. No. 2004/0010730	Filed: Mar. 6, 2003 Pub'd: Jan. 15, 2004	Saito	G-4
Japanese Patent Pub. No. 2006/248149	Filed: Mar. 15, 2005 Pub'd: Sep. 21, 2006	Ozawa	G-5
U.S. Patent Pub. No. 2003/0132941	Filed: Jan. 14, 2003 Pub'd: July 17, 2003	Echizenya	G-6
U.S. Patent Pub. No. 2006/0076977	Filed: Sep. 20, 2004 Pub'd: Apr. 13, 2006	Zhu	G-8
U.S. Patent Pub. No. 2005/0114580	Filed: Nov. 26, 2003 Pub'd: May 26, 2005	Ede	G-10
U.S. Patent Pub. No. 2007/0028127	Filed: July 6, 2006 Pub'd: Feb. 1, 2007	Kim	
U.S. Patent No. 8,670,645	Filed: Nov. 7, 2007 Pub'd: May 15, 2008	Nakajima	
U.S. Patent No. 7,558,326	Filed: Sep. 12, 2001 Pub'd: Jul. 7, 2009	Lyle	

b) Prior Art Publications

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
Video Electronics Standards Association	DisplayPort Standard, Version 1 ⁵	May 1, 2006	DisplayPort 1.0	G-7
USB Implementers Forum, Inc.	On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a	June 24, 2003	USB OTG Supplement	G-9
Adhir Upadhyay et al.	A Novel Asynchronous Wrapper Using 1-of-4 Data Encoding and Single-Track Handshaking	June 23, 2004	Upadhyay	G-10
Rick Downs	Using 1-Wire I/O for Distributed System Monitoring	Sep. 17, 1998	Downs	
PCI-SIG	PCI Express Base Specification, Revision 1.0	Apr. 29, 2002	PCIe	

c) Prior Art Systems

On information and belief, systems implementing the protocols identified below were in public use, on sale, or otherwise available to the public before the priority date of the '265 Patent. Defendant's further investigation and/or subsequent discovery from Plaintiff or third parties with knowledge regarding prior art systems may reveal additional relevant prior art systems and/or further information regarding the systems identified below, or other relevant prior art systems. Defendant reserves the right to supplement these Invalidity Contentions, based on subsequent investigation and discovery, including from third parties.

System	Available At Least As Of	Short Name	Exhibit Number
Samsung Yepp YP-D1 MP3 Player	2006	YP-D1	G-11

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed

⁵ Although the DisplayPort standards discussed herein include a tag purporting to limit their distribution to "Members Only," the versions discussed herein and/or charted in the attached exhibits are available publicly via the Internet. See, e.g., <https://glenwing.github.io/docs/DP-1.0.pdf> and <https://glenwing.github.io/docs/DP-1.2.pdf>

1 above. Defendant reserves the right to identify and rely on systems that represent different versions
2 or are otherwise related variations of the identified systems. Defendant also incorporates by
3 reference any and all other prior art systems identified in any other case brought by Plaintiff and/or
4 involving the Asserted Patents.

5 To the extent any item of prior art cited above is deemed not to disclose, explicitly or
6 inherently, any limitation of an asserted claim of the '231 Patent, Defendant contends that any
7 difference between that prior art and the corresponding patent claim would have been either inherent
8 in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically
9 denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

10 **2. The '231 Patent Claims Are Obvious Over the Prior Art**

11 To the extent Plaintiff argues that any limitation of the asserted claims of the '231 Patent are
12 not explicitly disclosed by an item of prior art identified above, in Exhibits G-1 through G-11, or
13 discussed in any incorporated IPR petition, any purported differences are such that the claimed
14 subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged
15 invention, in view of the state of the art and knowledge of those skilled in the art. The item of prior
16 art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

17 It would have been obvious to combine any of the prior art in Exhibits G-1 through G-11
18 with each other, at least because all of these references relate to serial communication between a
19 transmitting device and a receiving device using both a power bus and a control bus, and discovery
20 of devices using those buses.

21 U.S. Patent Publication No. 2006/0280055 ("Miller '055") teaches "a communication link
22 100 between a standard source (graphic/video source) 101 and a sink (display/receiver) 102.
23 Communication between the graphic/video source 101 and the display/receiver 102 enables bi-
24 directional transfer of signals that send graphic data from a source to a receiver and additional signals
25 that send and receive control information between the source and receiver." Miller '055, ¶ 5. That
26 communication occurs using the HDMI standard, which uses "control signals [that] include signals
27 related to the Data Display Channel (DDC), the Consumer Electronics Channel (CEC), and Hot
28 Plug Detect (HPD)." *Id.* ¶ 6. As Miller explains, "the signals that are transmitted between a source

1 and a sink will include, three differential channels (six wires), a clock channel (two wires), SDA,
2 SCL, CEC, DDC/CEC ground, +5V and HPD.” *Id.* ¶ 32.

3 U.S. Patent Publication No. 2007/0036158 (“Hun-Kwon”) teaches that “a media source
4 device (e.g., a STB) for reproducing predetermined media data and processing the reproduced media
5 data is connected to a Media sink device (e.g., a DTV) for receiving media data from the media
6 source device and outputting the received media data to an external part via a predetermined
7 interface cable. In this case, the media source device may be connected to the Media sink device via
8 an interface cable (e.g., a DVI or a HDMI).” Hun-Kwon, ¶ 5. Hun-Kwon further teaches that “the
9 first port 406 a includes a first power pin 407 a for receiving the voltage of +5V from the first media
10 source device 410, and a first HPD pin 408 a for generating the HPD signal.” *Id.* ¶ 62.

11 U.S. Patent No. 8,203,325 (“Miller ’325”) teaches that “[a]ctivation systems and methods
12 initiate High-Definition Multimedia Interface (HDMI) communication between an HDMI source
13 and an HDMI sink through an HDMI receptacle of the source. These systems and methods are
14 especially suited for use with mobile sources that generally operate from a battery that cannot
15 provide the +5V signal which the HDMI protocol requires sources to place on the +5V pin of their
16 HDMI receptacles. These systems and methods automatically detect the insertion of an HDMI cable
17 into the source's HDMI receptacle and subsequently generate and apply the required +5V signal to
18 the +5V pin of the source's HDMI receptacle to initiate HDMI communication.” Miller ’325,
19 Abstract. Miller ’325 further teaches that “[e]ach of the three data channels (channels 0, 1 and 2)
20 and the associated TMDS clock is formed by a signal pin (denoted as +), an inverse signal pin
21 (denoted as –), and a ground pin. These pins are located at the center and the right side of the plug
22 25. CEC, DDC data and clock, HPD, +5V, and DDC/CEC ground are each carried on respective
23 pins that are located at the left side of the plug 25.” *Id.* at 4:4–11.

24 U.S. Patent Publication No. 2004/0010730 (“Saito”) teaches that “a host is connected with
25 a peripheral by a USB cable to which a Mini-A plug and a Mini-B plug are provided on opposite
26 ends.” Saito, ¶ 108. Saito further teaches that “In the USB standard, a host can be connected with
27 a peripheral only by using VBUS (power supply), GND (ground), and two data signal lines (D+ and
28 D–). VBUS is supplied from the host. The data signal lines D+ and D– are used as differential signal

1 lines. In the OTG standard, a dual-role device to which a Mini-A plug is connected becomes an A-
2 device, as shown in FIG. 1B. The A-device operates as the host at the start of a session and is capable
3 of transferring the host function to a B-device under given conditions. A dual-role device to which
4 a Mini-B plug is connected becomes a B-device. The B-device operates as the peripheral at the start
5 of a session and is allowed to operate as the host by the A-device. The A-device supplies VBUS.”
6 *Id.* ¶¶ 109–10.

7 Japanese Patent Publication No. 2006/248149 (“Ozawa”) teaches that an “interface 200
8 communicates with an external device based on a communication method such as USB or IEEE (the
9 Institute of Electrical Engineers) 1394, sends data acquired from the external device to the CPU 203,
10 and transmits data acquired from the CPU 203 to the external device.” Ozawa, ¶ 21. Ozawa further
11 teaches that an “interrupt generation circuit 201 detects a change in the interface 200 from a state in
12 which no external device is connected to the interface 200 to a state in which the external device is
13 connected, and notifies the CPU 203 of the change. The interrupt generation circuit 201 is, for
14 example, an edge-triggered flip-flop, and detects that an external device is connected to the interface
15 200 by detecting a change in the voltage of a predetermined signal line of the interface 200. In the
16 present embodiment, when a predetermined signal line changes from a low voltage to a high voltage,
17 the interrupt generation circuit 201 detects that an external device is connected to the interface 200
18 and notifies the CPU 203 accordingly.” *Id.* ¶ 24.

19 U.S. Patent Publication No. 2003/0132941 (“Echizenya”) teaches “a controller adapted to
20 ascertain, when the host device and the monitoring device are connected with each other through
21 optical extension cables each based on DVI standard, whether these host device and monitoring
22 device have been exactly connected with each other through the optical extension cables or not as
23 well as to ascertain whether a power from an external power source or supply has been supplied to
24 attached circuits of the host device and the monitoring device or not.” Echizenya, ¶ 2. More
25 specifically, Echizenya teaches that “a video signal is digitally transmitted at high speed through the
26 optical extension cables by use of T.M.D.S. transmission system, and (DDC+5V) signal, DDC
27 clock, DDC data and HPD signal all of which are low speed signals for carrying out the plug and
28 play of a display are transmitted through the metal extension cables.” *Id.* ¶ 41.

1 Video Electronics Standards Association, *DisplayPort Standard, Version 1* (“DisplayPort
2 1.0”) teaches a link consisting of “consists of Main Link, Auxiliary Channel (AUX CH), and Hot
3 Plug Detect (HPD) signal line.” DisplayPort 1.0 at 24. DisplayPort 1.0 further teaches that
4 “DisplayPort connectors for detachable, box-to-box connections have one power pin and one return
5 current pin. The power shall be provided by Source Device only. The voltage of the power pin shall
6 be in the range of 5- to 12-V.” *Id.* at 115. DisplayPort 1.0 further discloses that “The HPD signal
7 is asserted by the DisplayPort Sink whenever the Sink is connected to its main power supply. . . .
8 The voltage level of the HPD pin is monitored by Source Device. TTL level shall be used for the
9 detection.” *Id.* at 116.

10 U.S. Patent Publication No. 2006/0076977 (“Zhu”) teaches “enabl[ing] a USB 1.1 device
11 and a USB 1.1 host to communicate seamlessly with a USB OTG device. The invention complies
12 with both USB 1.1 and OTG specifications. The invention includes the USB 1.1 host, USB 1.1
13 device and mixed signal circuits to implement USB OTG functions.” Zhu, Abstract. Zhu further
14 discloses that a “USB A-Device supplies power to the Vbus power line. It is host at the start of a
15 transaction session. It will relinquish the role of host to a dual-role B-Device to which it is connected
16 by a USB cable. This can occur only under the rules determined by the host negotiation protocol
17 (HNP).” *Id.* ¶ 17.

18 USB Implementers Forum, *On-The-Go Supplement to the USB 2.0 Specification, Revision*
19 *1.0a* (“USB OTG Supplement”) teaches that “USB has become a popular interface for exchanging
20 data between PC’s and peripherals. An increasing number of portable peripherals are using the USB
21 interface to communicate with the PC. Many of these portable devices would benefit from being
22 able to communicate to each other over the USB interface, yet certain aspects of USB make this
23 difficult to achieve.” USB OTG Supplement at 1. The USB OTG Supplement further teaches that
24 “this supplement to the USB 2.0 specification was developed that allows a portable device to take
25 on the role of a limited USB host, without the burden of supporting all the above functions of a PC.”
26 *Id.*

27 U.S. Patent Publication No. 2005/0114580 (“Ede”) teaches that “[t]he USB On-The-Go
28 (OTG) supplement to USB allows a device to be dual mode. A dual mode device has a mini A/B

1 connector that allows it to be connected to a mini A-plug as an A-device or to be connected to a
2 mini B-plug as a B-device. As a default a dual mode device when connected as an A-device operates
3 as a default host and when connected as a B-device operates as a default peripheral. However, OTG
4 will enable the role of the dual-role device to change without reversing the cable. Thus the OTG
5 device will be able to operate as a host or peripheral whether to is connected as an A-device or a B-
6 device.” Ede, ¶ 5. Ede further discloses that “[t]he A/B interface 12 of the dual-mode device 2
7 comprises a USB transceiver 14 and five pin contacts. The first pin contact 40 (Vbus) is used to
8 provide power from the A-device to the B-device. The second pin contact 42 (D+) and the third pin
9 contact 44 (D-) are used as differential data lines for transmitting data between connected devices.
10 The fourth pin contact 46 (GND) is used as an earth or ground. The fifth pin contact 48 (ID) is used
11 to detect, in the dual mode device 2, whether it is connected to a mini A-plug or a mini B-plug. A
12 mini A-plug connects, when inserted, the fourth pin contact 46 (ID) to the fifth pin contact (GND)
13 via a resistor. A mini B-plug, when inserted, leaves the fourth pin contact 46 (ID) isolated.” *Id.*
14 ¶ 24.

15 Adhir Upadhyay et al., *A Novel Asynchronous Wrapper Using 1-of-4 Data Encoding and*
16 *Single-Track Handshaking* (“Upadhyay”), teaches that “[t]he ST handshaking shown in Fig.3 needs
17 just one wire to signal both REQ and ACK. The sender pulls the ST line high to indicate a REQ.
18 The receiver pulls the ST line low to signal an ACK. Since after an REQ transmission, the ACK
19 signal returns the wire to its initial electrical state, the ST signaling essentially combines the
20 common 2-phase and 4-phase protocols-to become a 2-phase, return-to-zero handshaking scheme.”
21 Upadhyay at 206.

22 Rick Downs, *Using 1-Wire I/O for Distributed System Monitoring* (“Downs”), teaches that
23 “[o]ne popular serial bus used by integrated circuit manufacturers is the I2C bus from Philips, and
24 its compatible 2-wire bus variants from several other manufacturers. This bus scheme uses a clock
25 and a bidirectional data line, and defines 4-bit addresses for typical circuit functions.” Downs at
26 161. Downs further discloses that “The Dallas One-Wire™ (DOW) [2] bus uses only a single wire
27 to communicate data. Originally defined as a way to communicate with memory devices using a
28 minimal contact count, the DOW has been extended to several different product families. Products

1 available that use the DOW include EPROM memories, digital temperature sensors, and specialized
2 battery management devices. The use of a single data line makes routing the bus on a board much
3 simpler, or for extended systems, makes wiring simpler and less costly.” *Id.* at 162.

4 U.S. Patent Publication No. 2007/0028127 (“Kim”) teaches “a USB system comprises a host
5 device, and at least one client device connected to the host device through a USB connection, in
6 which the host interrupts a power supply to the client device through a power line when there is a
7 deadlock condition and resumes the power supply to the client device after an initialization.” Kim,
8 ¶ 11. More specifically, Kim teaches that “[t]he host device comprises a first switch connected to
9 the power line for regulating the power supply to the client device. The client device comprises a
10 pull-up resistor connected to a data line of the USB connection, the pull-up resistor being connected
11 with a second switch. The second switch disconnects the data line from the pull-up resistor when
12 the power supply through the power line is interrupted, and connects the data line with the pull-up
13 resistor when the power supply resumes.” *Id.* ¶¶ 12–14.

14 The Samsung Yepp YP-D1 (“YP-D1”) was an MP3 player released by Samsung on February
15 14, 2006. It is a device equipped with USB OTG functionality, used to connect the device to other
16 devices such as computers, tablets, and cellular phones. Aspects of YP-D1 are described in various
17 publications, including, but not limited to:

- 18 • *USB OTG Supplement*, PCI-SIG (Jun. 14, 2003);
- 19 • *Universal Serial Bus Specification, Revision 2.0*, USB-IF, (Apr. 27, 2000) (“USB 2.0
20 Specification”);
- 21 • U.S. Patent Pub. No. 2007/0028127 to Kim et al., (Feb. 1, 2007);
- 22 • *SAMSUNG YEPP YP-D1*, PCMag, (Apr. 12, 2006);
- 23 • Jasmine France, *SAMSUNG YEPP YP-D1 Review: Samsung PY-D1*, CNET (Mar. 31, 2006);
- 24 • *SAMSUNG YP-D1 Manual*, Samsung (Feb. 14, 2006)

25 Accordingly, because each of the identified references are directed to similar devices in the
26 similar field of endeavor, a person of ordinary skill in the art would be motivated to combine the
27 teachings of two or more references together because the references disclose similar systems that
28 solve the same problems in similar ways. Thus, it would have been obvious to one of ordinary skill

1 in the art to combine any of the foregoing references and one of ordinary skill would have expected
2 such a combination to be successful.

3 To the extent that it is determined that any of the above references do not disclose a “second
4 state” for a “second type of transmitting device,” it would further have been obvious to modify the
5 teachings of that reference to include this feature in view of the following teachings: *See, e.g.,* Hun-
6 Kwon, ¶ 87 (“In more detail, if the user selects the second media source device, the Media sink
7 device recognizes the power received via the second power pin, and determines whether the
8 recognized power is the voltage of +5V at step S612.”); Miller ’325, 5:9–14 (““Because the cell
9 phone 40 operates on a battery voltage in the range of 2.5 to 4.5 volts, it cannot provide a voltage
10 on the +5V line of the HDMI plug 28 that will be recognized by a sink. The activation system 50 of
11 FIG. 5, however, modifies the cell phone so that it can successfully complete HDMI
12 communications with an HDMI sink.”); Echizenya, ¶ 50 (“In the monitoring device M, it is
13 determined in a decision step 23 whether the transmitted (DDC+5V) signal is the proper (DDC+5V)
14 signal or not. In case it is the proper (DDC+5V) signal, the decision step 23 generates “Yes” signal,
15 and the process proceeds to a step 22 shown in FIG. 3. In the step 22, the HPD signal source 44
16 provided in the monitoring device M is driven to generate a HPD signal (a return signal of the
17 (DDC+5V) signal) therefrom, and the process proceeds to the next decision step 73. The decision
18 step 73 decides whether the generated HPD signal is the proper HPD signal or not. When the
19 decision step 73 decides that it is the proper HPD signal, “Yes” signal is outputted from the decision
20 step 73, and the process proceeds to a step 74.”). Therefore, a person of ordinary skill in the art
21 would be motivated to make such a combination.

22 To the extent that it is determined that any of the above references do not disclose a
23 transmitter that drives “a first signal value on the control bus periodically upon transitioning to the
24 pending state,” and a “second logic” for doing so, it would further have been obvious to modify the
25 teachings of that reference to include this feature in view of the following teachings: *See, e.g.,* USB
26 OTG Supplement at 51 (“The A-device detects the SE0 on the bus and recognizes this as a request
27 from the B-device to become Host. The A-device responds by turning on its D+ pull-up within
28 TA_BDIS_ACON max of first detecting the SE0 on the bus. . . . After waiting long enough to insure

1 that the D+ line cannot be high due to the residual effect of the B-device pull-up, (see Section 5.1.9),
2 the B-device sees that the D+ line is high and D- low, (i.e. J state). This indicates that the A-device
3 has recognized the HNP request from the B-device. At this point, the B-device becomes Host and
4 asserts bus reset to start using the bus.”); Downs at 162 (“Data transfer is initiated by the bus master,
5 which first resets the bus by pulling it low for at least 480ps. Within 60ps after the master releases
6 the line, any slave devices present on the bus will respond to the reset by pulling the bus low for at
7 least 60ps - this is known as a presence pulse. Once the master knows there is someone out there to
8 talk to, data can be communicated between the master and a slave in timeslots which are 120ps long
9 (Figure 1).”); Kim ¶ 78 (“In the USB system of FIG. 4, the data lines D+ and D- are also variable
10 in accordance with the deadlock detection. If the switch SW2 of the bus-powered high-speed USB
11 device 220 is turned off, the positive data line D+ transitions to the low level from the high level.
12 When both the data lines D+ and D- have low levels for the predetermined time T1, the USB host
13 110 detects a state of disconnection with the bus-powered high-speed USB client 220. The USB
14 host 110 turns the switch SW1 off and initializes its internal condition for the predetermined time
15 T2.”). Therefore, a person of ordinary skill in the art would be motivated to make such a
16 combination.

17 To the extent that it is determined that any of the above references do not disclose “a
18 switchable pull up circuit on the control bus” and “the transmitting device to enable the pull up
19 circuit in the discovered state,” as claimed, it would further have been obvious to modify the
20 teachings of that reference to include this feature in view of the following teachings: *See, e.g., Saito,*
21 ¶ 114 (“The dual- role device 10 includes a pull-up resistor R1 for pulling up the data signal line D+
22 and a pull-down resistor R2 for pulling down the data signal line D+ in order to operate as either the
23 host or the peripheral. The pull-up resistor R1 is connected with a power supply voltage line through
24 a switch circuit SW1 for turning the pull-up on/off. The pull-down resistor R2 is connected with a
25 ground line through a switch circuit SW2 for turning the pull-down on/off. The switch circuits SW1
26 and SW2 are controlled exclusively so that one of the switch circuits SW1 and SW2 is turned off
27 when the other is turned on.”); USB OTG Supplement at 50 (“When the B-device has finished using
28 the bus, it starts the process of returning control to the A-device simply by stopping all bus activity

1 and turning on its D+ pull-up resistor when the bus is in FS idle. The A-device will detect this lack
2 of activity and turn off its pull-up resistor. When the A-device detects the connection from the B-
3 device, it will resume bus operation as Host.”); Ede, ¶ 28 (“The B-interface 22 monitors Vbus and
4 when the voltage on the line exceeds a predetermined threshold, a pull-up resistor 24 is connected
5 to one of the data lines D+, D-. This is not described in detail as this is how a current peripheral
6 USB device responds to a host initiating a session by switching and keeping Vbus on. If the B-
7 interface 22 is a high speed interface then the pull-up resistor is connected to the data line D+ using
8 a switch. If the B-interface 22 is a low speed interface then the pull-up resistor is connected to the
9 data line D- using a switch.”); Kim, ¶¶ 13–14 (“The client device comprises a pull-up resistor
10 connected to a data line of the USB connection, the pull-up resistor being connected with a second
11 switch. The second switch disconnects the data line from the pull-up resistor when the power supply
12 through the power line is interrupted, and connects the data line with the pull-up resistor when the
13 power supply resumes.”). Therefore, a person of ordinary skill in the art would be motivated to
14 make such a combination.

15 To the extent that it is determined that any of the above references do not disclose “wherein
16 the transmitting device is a mobile device” as claimed, it would further have been obvious to modify
17 the teachings of that reference to include this feature in view of the following teachings: *See, e.g.,*
18 Miller ’325, Figs. 5A–5C, 5:9–14 (““Because the cell phone 40 operates on a battery voltage in the
19 range of 2.5 to 4.5 volts, it cannot provide a voltage on the +5V line of the HDMI plug 28 that will
20 be recognized by a sink. The activation system 50 of FIG. 5, however, modifies the cell phone so
21 that it can successfully complete HDMI communications with an HDMI sink.”); Saito, ¶¶ 305–06,
22 Fig. 1A; Ozawa, ¶¶ 7, 10, 16; USB OTG Supplement at 5, 14–16; Ede, ¶¶ 20–22; Downs at 165;
23 Kim ¶¶ 5, 85. Therefore, a person of ordinary skill in the art would be motivated to make such a
24 combination.

25 To the extent that it is determined that any of the above references do not disclose a
26 “switchable pull down circuit” on the control bus, it would further have been obvious to modify the
27 teachings of that reference to include this feature in view of the following teachings: *See, e.g.,* Saito,
28 ¶ 115 (“The dual- role device 20 includes a pull-up resistor R3 for pulling up the data signal line D+

1 and a pull-down resistor R4 for pulling down the data signal line D+. The pull-up resistor R3 is
2 connected with a power supply voltage line through a switch circuit SW3 for turning the pull-up
3 on/off. The pull-down resistor R4 is connected with a ground line through a switch circuit SW4 for
4 turning the pull-down on/off. The switch circuits SW3 and SW4 are controlled exclusively so that
5 one of the switch circuits SW3 and SW4 is turned off when the other is turned on.”); USB OTG
6 Supplement at 34 (“When an A-device is idle or acting as Host, it shall activate pull-down resistors
7 on both the D+ and D- lines. These resistors shall be within the range of 14.25 kΩ to 24.8 kΩ (RPD).
8 When an A-device is acting as a Peripheral, it shall disable the pull-down on the D+ line but shall
9 not disable the pull-down on the D- line. The A-device is allowed to disable both pull-down resistors
10 during the interval of a packet transmission, when acting as either Host or Peripheral.”); Kim, ¶ 47
11 (“The downstream port transceiver 101 is connected with a pair of data lines D+ and D−, a power
12 line Vbus, and a ground line GND. The data lines D+ and D− of the downstream port transceiver
13 101 are each connected to pull-down resistors R1 and R2. The pull-down resistors R1 and R2 have
14 values of about 15 KΩ.”). Therefore, a person of ordinary skill in the art would be motivated to
15 make such a combination.

16 To the extent that it is determined that any of the above references do not disclose “the first
17 type of device is compatible with a modified protocol” (and related limitations) as claimed, it would
18 further have been obvious to modify the teachings of that reference to include this feature in view
19 of the following teachings: *See, e.g.*, Kim, ¶ 82 (“The USB OTG system shown in FIG. 13 is set by
20 altering the functions of the host and device from the USB OTG system of FIG. 12 by means of
21 HNP. When the functions of the USB host and client are changed by HNP while the USB OTG
22 system is operating, a deadlock condition occurs to cut off connection between the two USB devices
23 and the allocation of functions is re-established as the initial configuration when the systems are
24 reconnected.”). Therefore, a person of ordinary skill in the art would be motivated to make such a
25 combination.

26 A person skilled in the art would have been motivated to combine any of the above
27 references. In particular, the combinations identified herein would merely have been (a) a
28 combination of prior art elements according to known methods to yield predictable results; (b) a

1 simple substitution of one known element for another to obtain predictable results; (c) a use of
2 known technique to improve similar devices or methods in the same way; (d) application of a known
3 technique to a known device or method ready for improvement to yield predictable results; (e)
4 obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in
5 either the same field or a different one based on design incentives or other market forces since the
6 variations are predictable to one of ordinary skill in the art. Moreover, a person of ordinary skill in
7 the art had a reason to combine these references because—at a minimum—they all pertain to serial
8 communications between a transmitting device and a receiving device that communicate via a power
9 bus and a control bus.

10 As discussed above, the motivation to combine the teachings of the patents and other prior
11 art referenced above is found in the art as specified in the charts and in: (1) the nature of the problem
12 being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of
13 persons of ordinary skill in the art; and (4) the fact that the prior art is generally directed towards
14 signal processing in microphone array systems, and (5) the predictable results obtained in combining
15 the different elements of the prior art. The Supreme Court has held that a showing of a motivation
16 to combine within the references themselves is not required to prove obviousness. *See KSR*, 550
17 U.S. at 401 (“Any need or problem known in the field of endeavor at the time of invention may
18 provide the motivation to combine.”).

19 For example, a person skilled in the art would have been motivated to combine Zhu and/or
20 the USB OTG Supplement and/or YP-D1 with Kim, Saito, Ede and/or additional references
21 discussed above and disclosed in Exhibits G-1 through G-11 for the reasons provided above.
22 Moreover, the combination of references is no more than a combination of systems all directed to
23 communication between devices using the USB 2.0 and USB On-The-Go standards. Additionally,
24 the combination reflects no more than a simple substitution of known elements for one another to
25 obtain predictable results. For example, the addition of the deadlock detection logic disclosed in
26 Kim would be a straightforward modification to the systems disclosed in Zhu and the USB OTG
27 Supplement. Additionally, Kim discloses that it is possible to modify the functions of host and
28 client devices that communicate using the USB OTG standard, and that such modifications are

1 within the level of ordinary skill in the art. Further, combining features of Zhu and the USB OTG
2 Supplement with the teachings of these references employs the use of known techniques to improve
3 similar devices in the same way. For example, Zhu with Kim would use Kim's deadlock detection
4 logic to enable seamless communication between USB devices, which is the problem disclosed in
5 Zhu.

6 Thus, in addition to the combinations discussed above, exemplary combinations which
7 render obvious some or all of the Asserted Claims of the '231 Patent are listed in **Appendix A**, Sec.
8 VII.

9 **B. Invalidity of the '231 Patent Based on 35 U.S.C. § 112, ¶ 1**

10 Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of
11 the '231 Patent, to the extent such positions can be understood from Plaintiff's Infringement
12 Contentions, Defendant asserts that the Asserted Claims of the '231 Patent are invalid for failure to
13 provide a written description that enables the full scope of the Asserted Claims based on at least the
14 following claim terms, phrases, or limitations:

- 15 • **"disabling hot plug functionality" (claims 1 and 16):** The '231 Patent does not explain
16 how hot plug functionality would be disabled or how one of skill in the art, reading the
17 specification, would understand how to do so without undue experimentation.

18 Based on Defendant's present understanding of Plaintiff's Infringement Contentions and
19 apparent interpretation of the scope of the Asserted Claims, at least one or more of these claim terms,
20 phrases, and limitations are not described in the specification of the Asserted Patent and do not
21 enable a person of ordinary skill in the art to practice the claimed invention without undue
22 experimentation or to distinguish all operative embodiments from all nonoperative embodiments
23 without undue experimentation.

24 In addition to Defendant's contentions regarding the specifically listed terms above,
25 Defendant contends that UCT has failed to identify specific support for each limitation of each
26 Asserted Patent in its Infringement Contentions, and instead points to the same or similar
27 information as satisfying each claim limitation. Defendant therefore contends that there is no written
28 description support for the identified, described, or explained in the specification of the Asserted

1 Patents to enable a person of ordinary skill in the art to practice the claimed invention under the
2 wide claim scope UCT appears to be contending applies.

3 The written description and enablement issues identified above apply to all claims that
4 include the identified limitations, either explicitly or through claim dependency, and are not limited
5 to the exemplary claims listed above.

6 **C. Invalidity of the '231 Patent Based on 35 U.S.C. § 112, ¶ 2**

7 At least claims 11, 13, and 16 (and their dependent claims) of the '231 Patent are invalid
8 under 35 U.S.C. § 112(2) because they are mixed method-apparatus claims under the doctrine of
9 *IPXL Holdings L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377 (Fed. Cir. 2005). In particular, at least
10 the following claim terms and phrases improperly recite a method of using the entire claimed
11 apparatus and/or functionality not tied to the capability of any recited structural element:

- 12 • “the transmitting device is to transition to the disconnect state when the first logic
13 determines that the voltage value on the power bus is lost” (claim 11)
- 14 • “the transmitting device is to enable the pull up circuit in the discovered state” (claim 13)
- 15 • “the receiving device to enable a voltage potential of a predetermined value on the power
16 bus and to drive a signal on the control bus at a first signal value in a disconnect state”
17 (claim 16)
- 18 • “the receiving device to discover a first type of transmitting device and transition to a first
19 state when the first signal is detected” (claim 16)
- 20 • “the receiving device to enable the switchable pull down circuit on the control bus and
21 disable hot plug functionality upon discovering the first type of transmitting device” (claim
22 16)
- 23 • “the receiving device to discover a second type of transmitting device and transition to a
24 second state when the power signal is detected” (claim 16)

25 Based on Defendant’s present understanding of Plaintiff’s Infringement Contentions, at
26 least one or more of these claim terms, phrases, and limitations are indefinite because they are
27 inconsistent with and broader than the alleged invention disclosed in the specification and during
28 prosecution, and given Plaintiff’s apparent constructions of the claims, a person of ordinary skill in

1 the art at the time of the invention would not understand what is claimed with reasonable certainty,
2 even when the claims are read in light of the specification and prosecution history.

3 Additionally, at least Claims 10 and 16 (and their dependent claims) of the '231 Patent are
4 invalid under 35 U.S.C. §§ 112(2) and (6) because the '231 Patent does not disclose sufficient
5 structure corresponding to the function recited in at least the following means-plus-function claim
6 limitations:

- 7 • “logic to detect signals on the cable interface” (claim 10)
- 8 • “a first logic to detect a voltage value on the power bus” (claim 10)
- 9 • “a second logic to detect signals on the control bus” (claim 10)
- 10 • “logic to discover a transmitting device coupled with the receiving device” (claim 16)
- 11 • “a first logic to detect a first signal on the control bus” (claim 16)
- 12 • “a second logic to detect a power signal from the receiving device” (claim 16)

13 The indefiniteness issues identified above apply to all claims that include the identified limitations,
14 either explicitly or through claim dependency, and are not limited to the exemplary claims listed
15 above.

16 **X. THE ASSERTED CLAIMS OF THE '103 PATENT ARE INVALID**

17 **A. Identification of Prior Art**

18 **1. The '103 Patent Claims Are Anticipated by the Prior Art**

19 Defendant contends that the prior art references charted in Exhibits H-1 through H-36,
20 discussed in any incorporated IPR petition, discussed or cited in the prosecution history and/or any
21 reexamination proceedings, and/or described below anticipate and/or render obvious, alone or in
22 combination, one or more of the Asserted Claims of the '103 Patent. As stated above, UCT asserts
23 claims 1, 3, 11, 17, 21, and 22 of the '103 Patent (“the '103 Asserted Claims”).

24 Some or all of the '103 Patent Asserted Claims are invalid as anticipated under 35 U.S.C. §
25 102 in view of each of the prior art references identified in the claim charts included in Exhibit H-1
26 through H-36 and/or identified in any incorporated IPR petition, which identify specific examples
27 of where each limitation of the '103 Asserted Claims is found in the prior art references. As
28 explained above, the cited portions of prior art references identified in the attached claim charts are

1 exemplary in nature and representative of the content and teaching of the prior art references, and
2 should be understood in the context of the reference as a whole and as they would be understood by
3 a person of ordinary skill in the art.

4 In addition to references identified in the incorporated IPR petition, the prosecution history,
5 and any reexamination proceedings, Defendant identifies the following references as anticipating
6 one or more of the '103 Patent Asserted Claims under 35 U.S.C. § 102. The table of anticipating
7 references below is exemplary, and it does not constitute an admission that any reference not listed
8 below does not also anticipate the claims of the '103 Patent. Further, Defendant contends that any
9 prior art reference in the attached charts that is charted for each limitation of any given claim
10 anticipates that claim, regardless of whether that prior art reference is listed in the following tables.

11 **a) Prior Art Patents and Applications**

Number	Published/Issued Date/Filing Date	Short Name	Exhibit Number
U.S. Patent No. 8,799,537	Filed: May 1, 2012 Issued: Aug. 5, 2014	Zhu 537	H-1
U.S. Patent No. 7,558,326	Filed: Sep. 12, 2001 Issued: Jul. 7, 2009	Lyle	H-2
U.S. Patent Publ. No. 2013/0080665 A1	Filed: Sept. 22, 2011 Pub'd: Mar. 28, 2013 Issued: Apr. 26, 2016	Park	H-3
U.S. Patent No. 8,090,030	Filed: Jan. 4, 2008 Pub'd: Jul. 9, 2009 Issued: Jan. 3, 2012	Kim 030	H-4
U.S. Patent Publ. No. 2007/0201492	Filed: Dec. 2, 2003 Pub'd: Aug. 30, 2007 Issued: Jun. 19, 2012	Kobayashi	H-5
U.S. Patent No. 7,746,798	Filed: Nov. 7, 2001 Pub'd: Nov. 21, 2002 Issued: Jun. 29, 2010	'798 Patent	H-6
U.S. Patent No. 8,565,337	Filed: Feb. 7, 2007 Pub'd: Aug. 7, 2008 Issued: Oct. 13, 2013	Lida 337	H-7
U.S. Patent No. 8,355,327	Filed: Aug. 17, 2008 Pub'd: Dec. 11, 2008 Issued: Jan. 15, 2013	Lida 327	H-8
U.S. Patent No. 4,486,739	Filed: Jun. 30, 1982 Issued: Dec. 4, 1984	Franaszek	H-9
U.S. Patent Publ. No. 2010/0157169	Filed: Mar. 30, 2009 Pub'd: Jun. 24, 2010 Issued: Oct. 2, 2012	Yoshida	H-10

1	U.S. Patent No. 6,738,417	Filed: Sep. 9, 1999 Issued: May 18, 2004	Kim 417	H-11
2	U.S. Patent No. 8,238,445	Filed: Mar. 14, 2007 Pub'd: Jun. 5, 2008 Issued: Aug. 7, 2012	Wang 445	H-12
3	U.S. Patent No. 6,535,505	Filed: Sep. 30, 1998 Issued: Mar. 18, 2003	Hwang	H-13
4	U.S. Patent No. 5,420,640	Filed: Dec. 3, 1993 Issued: May 30, 1995	Munich	H-14
5	U.S. Patent Publ. No. 2010/0128176	Filed: Nov. 7, 2007 Pub'd: May 27, 2010 Issued: May 14, 2013	Nakajima	H-15
6	US 2015/0280895	Prov.: Apr. 1, 2014 Filed: Apr. 1, 2015 Pub'd: Oct. 1, 2015 Issued: Jan. 1, 2015	Whitby-Strevens	H-16
7	EP 2172011 B1	Filed: Jul. 1, 2008 Issued: Oct. 2, 2013	Butcher	H-17
8	US 2014/0019653	Filed: Jul. 11, 2012 Issued: Jan. 16, 2014	Amchislavsky	H-18
9	U.S. Patent Publ. No. 2014/0004741	Filed: Jul. 18, 2013 Pub'd: Jan. 2, 2014 Issued: Mar. 17, 2015	Jol	H-19
10	U.S. Patent No. 8,332,518	Filed: Aug. 13, 2007 Pub'd: Feb. 14, 2008 Issued: Dec. 11, 2012	Bradshaw	H-20
11	U.S. Patent No. 8,019,905	Filed: Feb. 11, 2008 Pub'd: Aug. 13, 2009 Issued: Sep. 13, 2011	Wu	H-21
12	U.S. Patent No. 8,966,134	Filed: Feb. 23, 2012 Pub'd: Aug. 23, 2012 Issued: Feb. 24, 2015	Anderson 134	H-28
13	U.S. Patent Publ. No. 2013/0244491 (issued as U.S. Patent No. 9,112,327)	Filed: Sep. 7, 2012 Pub'd: Sep. 19, 2013 Issued: Aug. 18, 2015	Sarwar 491 Sarwar 327	H-28
14	U.S. Patent Publ. No. 2006/0076977	Filed: Sep. 10, 2004 Pub'd: Apr. 13, 2006 Issued: Mar. 20, 2007	Zhu 977	H-33
15	U.S. Patent No. 7,856,520	Filed: Jan. 4, 2008 Pub'd: Jul. 9, 2009 Issued: Dec. 21, 2010	Ranade	H-34
16	U.S. Patent Publ. No. 2008/0084834	Filed: Oct. 9, 2006 Issued: Apr. 10, 2008	Stanek	H-35
17	U.S. Patent No. 5,974,464	Filed: Sep. 30, 1996 Issued: Oct. 26, 1999	Shin 464	IPR2024-0148
18	U.S. Patent Publ. No. 2013/0266154	Filed: Feb. 26, 2013 Pub'd: Oct. 10, 2013 Issued: Dec. 22, 2015	McCormack	IPR2024-0148

b) Prior Art Publications

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
Video Electronics Standards Association (VESA)	DisplayPort Standard Version 1, Revision 2	Jan. 5, 2010	DisplayPort 1.2	H-23
Hitachi, Ltd. Matsushita Electric Industrial Co., Ltd. Philips Consumer Electronics, International B.V. Silicon Image, Inc. Sony Corporation Thomson Inc. Toshiba Corporation	High-Definition Multimedia Interface Specification Version 1.3a	Nov. 10, 2006	HDMI 1.3a	H-22
Digital Display Working Group	Digital Visual Interface Revision 1.0	Apr. 2, 1999	DVI 1.0	H-25
Craig Wiley	“Invited Paper: DisplayPort 1.2, Embedded DisplayPort, and Future Trends,” Society for Information Display (SID) Symposium Digest of Technical Papers: Volume 42, Issue 1 (June 2011) at 551-554	Aug. 12, 2012	Wiley	H-31
USB Implementers Forum, Inc.	Universal Serial Bus Specification, Revision 2.0	April 27, 2000	USB 2.0	H-26
USB Implementers Forum, Inc.	On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a	June 24, 2003	USB OTG 1.0a	H-29
USB Implementers Forum, Inc.	Universal Serial Bus Device Class Definition for Video Devices, Revision 1.5	Aug. 9, 2012	USB Video Class	H-32

c) Prior Art Systems

On information and belief, systems implementing the protocols identified below were in public use, on sale, or otherwise available to the public before the priority date of the '103 Patent. Defendant's further investigation and/or subsequent discovery from Plaintiff or third parties with knowledge regarding prior art systems may reveal additional relevant prior art systems and/or

further information regarding the systems identified below, or other relevant prior art systems. Defendant reserves the right to supplement these Invalidity Contentions, based on subsequent investigation and discovery, including from third parties.

System	Available At Least As Of	Short Name	Exhibit Number
Devices implementing High-Definition Multimedia Interface, Specification Version 1.3a	2006	HDMI 1.3a	H-22
Devices implementing VESA DisplayPort Standard Version 1, Revision 2, including Apple's MacBook Pro (Early 2011), Dell's UltraSharp U2414M Monitor, and HP's ZR2440w Monitor	2011	DisplayPort System	H-24
Devices implementing Digital Visual Interface DVI Revision 1.0	1999	DVI 1.0	H-25
Belkin Ethernet Adapter employing Universal Serial Bus Specification, Revision 2.0	2000	USB 2.0	H-26
Devices implementing FireWire System based on IEEE 1394	1996	Firewire	H-27
Devices implementing Thunderbolt, including Apple MacBook Pro (early 2011 and later); MacBook Air (mid 2011 and later); Mac mini (Mid 2011 and later); iMac (mid 2011 and later); Mac Pro (late 2013); and MacBook Pro (Retina, late 2013 and later)	2011	Thunderbolt	H-28
Sony Xperia with USB On-the-Go implementing USB OTG 1.0a	2012	Xperia S	H-29
Texas Instruments' DisplayPort to TMDS Translator Product TI SN75DP129	2008	TI SN75DP129	H-30
Micro-USB employing Multimedia High-definition Link (MHL)	2010	MHL	H-36

Any system that implements one or more methods and/or apparatuses described in one or more of the prior art patents and publications described and/or charted herein. As set forth above, one example prior art system that anticipates and/or renders obvious the '103 Asserted Claims includes the Sony Xperia line of smartphones (including, e.g., the Xperia S) which, on information and belief, transmitted and received USB data and video data over a USB OTG connection. See,

1 e.g., Ex. H-29. Another example of a prior art system that anticipates and/or renders obvious the
2 '103 Asserted Claims includes the Apple MacBook Pro, MacBook Air, Mac mini, iMac, and Mac
3 Pro, all of which implemented Thunderbolt. *See, e.g.*, Ex. H-28.

4 Defendant additionally identifies and relies on any system, product, or public knowledge or
5 use that embodies or otherwise incorporates any of the prior art patents and publications listed
6 above. Defendant reserves the right to identify and rely on systems that represent different versions
7 or are otherwise related variations of the identified systems. Defendant also incorporates by
8 reference any and all other prior art systems identified in any other case brought by Plaintiff and/or
9 involving the Asserted Patents.

10 To the extent any item of prior art cited above is deemed not to disclose, explicitly or
11 inherently, any limitation of an asserted claim of the '103 Patent, Defendant contends that any
12 difference between that prior art and the corresponding patent claim would have been either inherent
13 in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically
14 denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

15 **d) Other Relevant References**

16 Defendant reserves the right to rely on the prior art references identified in connection with
17 one of the other Asserted Patents in connection with the '103 patent. In addition, Defendant hereby
18 cites the following additional references as being relevant to the subject matter claimed in the '103
19 patent. Defendant is producing concurrently herewith a number of such references that are relevant
20 to the validity of the Asserted Patents, the state of the art, and as evidencing a motivation to combine
21 various references. Defendant reserves the right to rely on one or more of the references produced
22 concurrently herewith as anticipatory references under 35 U.S.C. § 102, as further evidence of
23 obviousness under 35 U.S.C. § 103, as background references demonstrating the state of the art, as
24 a limitation upon the doctrine of equivalents, or for any other purpose. Based on further
25 investigation and discovery, based on positions that Plaintiff may take regarding the scope of the
26 asserted claims, and/or based on the Court's claim construction (once issued), Defendant reserves
27 the right to revise these contentions and to rely on these references to prove the invalidity of the
28

'103 patent in a manner consistent with this Court's Rules and with the Federal Rules of Civil Procedure.

i. Prior Art Patents and Applications

Number	Published/Issued Date
EP 2023632	Filed: May 16, 2007 Issued: Oct. 2, 2013
EP 2091253	Filed: Nov. 7, 2007 Issued: Jul. 29, 2015
JP 4844230	Filed: May 16, 2006 Pub'd: Nov. 29, 1007 Issued: Dec. 28, 2011
US 8,539,628	Filed: Oct. 2, 2008 Pub'd: Apr. 9, 2009 Issued: Jan. 22, 2013
US 2009/0185637	Filed: Sep. 4, 2008 Pub'd: Jul. 23, 2009
US 8,749,285	Filed: Mar. 15, 2013 Issued: Jun. 10, 2014
U.S. Patent Publ. No. 2009/0046690	Filed: Aug. 16, 2007 Pub'd: Feb. 19, 2009 Issued: Oct. 19, 2010
US 8,429,713	Filed: Apr. 2, 2007 Pub'd: Oct. 2, 2008 Issued: Apr. 23, 2013
U.S. Patent Publ. No. 2013/0244492	Filed: Sep. 7, 2012 Pub'd: Sep. 19, 2013
Japanese Patent No. 4844230	Filed: May 16, 2006 Pub'd: Nov. 29, 2007 Issued: Dec. 28, 2011
U.S. Patent Publ. No. 2010/0066919	Filed: Nov. 7, 2007 Pub'd: Mar. 18, 2010
U.S. Patent Publ. No. 2010/0073574	Filed: Jan. 20, 2009 Pub'd: Mar. 25, 2010
U.S. Patent Publ. No. 2010/0269137	Filed: Nov. 7, 2007 Pub'd: Oct. 21, 2010
U.S. Patent Publ. No. 2010/0118188	Filed: Nov. 7, 2007 Pub'd: May 13, 2010

ii. Prior Art Publications

Author or Publisher	Title	Publication/Use Date
Daryl J. Eigen	ISDN Architecture: A Basis for New Services	1985
Garry Musgrave	An Overview of ISDN Technology	Jan. 2001
Thomas Doumas (Hewlett Packard)	Next Generation Telephony: A look at Session Initiation Protocol	Apr. 5, 1999

1 **2. The '103 Patent Claims Are Obvious Over the Prior Art**

2 To the extent Plaintiff argues that any limitation of the '103 Asserted Claims is not explicitly
3 disclosed by an item of prior art identified above, in Exhibits H-1 through H-36, or discussed in any
4 incorporated IPR petition, any purported differences are such that the claimed subject matter as a
5 whole would have been obvious to one skilled in the art at the time of the alleged invention, in view
6 of the state of the art and knowledge of those skilled in the art. The item of prior art would, therefore,
7 render the relevant claims invalid as obvious under 35 U.S.C. § 103.

8 It would have been obvious to combine any of the prior art in Exhibits H-1 through H-36
9 with each other, at least because all of these references relate to methods and apparatuses for
10 communicating both audio/visual data and other data (such as control data) between a source and a
11 sink. The charted references may further disclose transmitting audio/visual data unidirectionally,
12 while transmitting and receiving other data and/or control data bidirectionally. Moreover, the
13 references may further disclosed that audio/visual and other data are communicated on one physical
14 channel while control data is communicated on a different physical channel.

15 For example, U.S. Patent No. 8,799,537 to Zhu and Mohanty ("Zhu 537") teaches a device
16 "configured to transmit, on a DisplayPort link to [a] second device, a data flow comprising both
17 USB protocol data and uncompressed high definition media data signals." Zhu 537 at Abstract. The
18 USB protocol data and uncompressed high definition media data may be communicated between
19 the devices using a modified version of the link timing defined in the DisplayPort 1.2 specification.
20 *Id.* at 34:52-61. Zhu 537 discloses that the USB protocol data may be transmitted bidirectionally on
21 the same physical channel as the uncompressed high definition media data. *Id.* at 34:11-51. In
22 particular, Zhu 537 teaches reverse USB transmission may occur during blanking periods. *Id.* at
23 Abstract. Zhu 537 further explains that a DisplayPort link includes a separate sideband channel
24 (AUX) for bidirectional communication of control data. *Id.* at 1:42- 2:3.

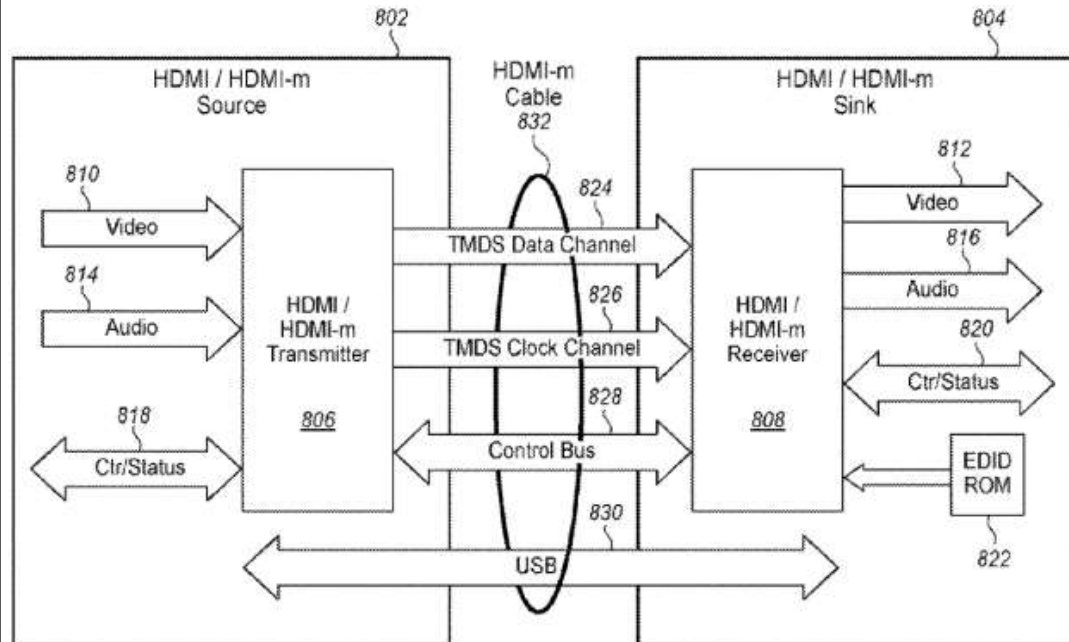
25 U.S. Patent No. 7,558,326 to Lyle et al. ("Lyle"), entitled "Method and Apparatus for
26 Sending Auxiliary Data on a TMDS-Like Link," describes a "communication system including a
27 transmitter, a receiver, and a TMDS-like link, in which video data and auxiliary data (typically
28 including timing data associated with other auxiliary data) are transmitted from the transmitter to

1 the receiver, or in which video data are transmitted over the link from the transmitter to the receiver,
2 and auxiliary data (typically including timing data associated with other auxiliary data) are
3 transmitted from the receiver to the transmitter.” Lyle at Abstract. Lyle explains that USB data is a
4 type of auxiliary data that could be transmitted. Lyle at 50:47-50. Lyle describes embodiments in
5 which “the transmitter transmits video data and auxiliary data to the receiver over a video channel
6 of the link” (*id.* at 8:46-48) and explains that auxiliary data may be sent in the opposite direction by
7 “reversing one video data transmission channel, or two or more video data transmission channels,
8 during blanking periods (to send auxiliary data from the receiver of the video data to the transmitter
9 of the video data)” (*id.* at 45:43-48). Further, embodiments include a Display Data Channel for
10 bidirectional transmission of control data. *See id.* at 28:26-45.

11 US 2013/00800665 to Park and Shamarao (“Park”) teaches a “data transmission system”
12 including “a transmission link coupling the source device and the sink device. The transmission link
13 includes a unidirectional main line having a plurality of main link channels, a bidirectional auxiliary
14 line configured to transmit data between the source device and the sink device at a first data rate,
15 and a unidirectional interrupt line. The transmission link is configured to transmit data from the
16 source device to the sink device over one of the main link lines at a second data rate and to transmit
17 data from the sink device to the source device over the auxiliary line at the second data rate. The
18 transmission link may comply with the DisplayPort standard, and the data may be transmitted in
19 accordance with the USB standard.” Park at Abstract. In particular, Park discloses at least one
20 embodiment in which USB data is transmitted bidirectionally over certain lines of the DisplayPort
21 main link, while the remaining main link lines continue to transmit AV data. *Id.* at [0030] and Fig.
22 6.

23 U.S. Patent No. 8,090,030 to Kim et al. (“Kim 030”), issued Jan. 3, 2012 and published as
24 US 2009/0178097 on July 9, 2009, discloses an “HDMI-M system architecture 800 includ[ing] a
25 source 802 and a sink 804” connected by an HDMI-M cable that carries a TMDS data channel for
26
27
28

video, audio and auxiliary data; a single-wire control bus; and a dedicated bidirectional USB connection. Kim 030 at 6:48 – 7:6. This is shown in Figure 8 of Kim 030:



Kim 030 was originally assigned to Silicon Image, Inc. and shares one or more inventors with the '103 Patent.

U.S. Patent Publ. No. 2007/0201492 to Kobayashi ("Kobayashi"), published Aug. 30, 2007, discloses a "compact packet based multimedia interface" including "a uni-directional main link having a single lane coupling the multimedia source to the multimedia sink arranged to carry a packetized multimedia data stream from the multimedia source to the multimedia display at a link rate that is independent of the native multimedia clock rate, a half duplex, bi-directional auxiliary channel connecting the multimedia source and the display that provides in concert with the uni-directional main link, a secondary communication link between the multimedia source and the display for transferring information between the multimedia source and the display, and a connector arrangement arranged to electrically connect the uni-directional main link and the half duplex, bi-directional auxiliary channel to the multimedia source and the display." Kobayashi at [0008]. Kobayashi was the basis for a rejection during prosecution of the '103 Patent. The applicant overcame that objection by arguing that "Kobayashi describes sending video data over a first

1 channel (e.g., main link 222), but only describes receiving USB data over a second, different channel
2 (e.g., auxiliary channel, such as auxiliary channel 224 or auxiliary channel 524)” and thus “does not
3 describe a single physical channel over which both video data is sent and data compliant with the
4 first standard (e.g. USB data) is sent and received.” Response to Office Action, July 12, 2017 at 8.
5 The applicant did not argue, however, that any other limitation was missing from Kobayashi. In
6 particular, the applicant did not dispute the examiner’s mapping of Kobayashi’s teachings regarding
7 “link training” and reestablishing a link from the electrical idle state, and associated signals (such
8 as training patterns and SYNC patterns), to the “synchronization signal” claim elements (see, e.g.,
9 claims 2, 3, 12, 13, and 17). Kobayashi’s disclosure of these synchronization signals is very similar
10 to the link training of the DisplayPort standards. As discussed below, a POSITA would have been
11 motivated to combine Kobayashi with any reference teaching the unidirectional transmission of AV
12 data and bidirectional transmission of USB or other data on the same physical channel.

13 U.S. Patent No. 8,565,337 to Lida et al. (“Lida 337”), published as US 2008/0187028 on
14 Aug. 7, 2008, discloses methods and apparatuses for “transmitting data for different applications
15 over a same communication network and in particular to transmitting high definition uncompressed
16 multimedia audio/video (AV) streams and networking data such as appliance control data and
17 Ethernet data over a same network.” Lida 337 at 1:6-10. In particular, Lida 337 claims a “wired
18 communication link” that includes a transceiver for transmitting a “multiplexed transmission
19 comprising a first direction of a bidirectional data channel and lossless high definition digital video
20 comprising pixel data, video clock related data, and video synchronization data” and receiving “a
21 second transmission comprising a second direction of the bidirectional data channel.” *Id.* at 13:59 –
22 14:5. The bidirectional data may comprise “Digital Video Interfacing (DVI) control signal data,
23 High Definition Multimedia Interface (HDMI) control signal data, or DisplayPort control signal
24 data, I2C, Consumer Electronics Control (CEC), Hot Plug Detection (HPD), 5V indication, or a
25 combination thereof.” *Id.* at 18:6-13. The wired communication link of Lida 337 further includes a
26 “second transceiver operative to receive the first multiplexed transmission and regenerate video
27 timing based on the video clock related data, and order in which the video pixel data and the video
28 synchronization data are received.” *Id.* at 15:14-18.

1 U.S. Patent No. 8,355,327 to Lida et al. (“Lida 327”), published as US 2008/0304433 on
2 Dec. 11, 2008, explains that “[c]urrent video, audio, or multimedia solutions transmit some or all of
3 their standby and/or low power data types over dedicated wires. For example, a High-Definition
4 Multimedia Interface (HDMI™) includes dedicated wires for DDC, HPD, and CEC controls.
5 DisplayPort™ includes two wires for transmitting the auxiliary data.” Lida 327 at 1:30-35. Lida 327
6 further discloses an apparatus and method for “transmitting in a first mode of operation bidirectional
7 data between a source device and a sink device and unidirectional uncompressed high definition
8 digital video from the source device to the sink device over at least a first subset of conductive wires
9 comprised in a cable.” *Id.* at 9:34-40; Figs. 11 and 17. In particular, Lida 327 lists several examples
10 of different “data types” that may be transmitted: “video pixel data; audio data; video
11 synchronization control data, such as horizontal and vertical video picture synchronizations; video
12 system controls, such as CEC, HPD and DDC signals; or general data transmissions, such as
13 Ethernet data, USB data, or RS232 data; or infra-red (IR) control data.” *Id.* at 4:1-7. Lida 327
14 incorporates the disclosure of Lida 337 by reference. *See id.* at 1:7-9.

15 U.S. Patent Publ. No. 2010/0157169 to Yoshida and Sato (“Yoshida”) describes a
16 modification of an HDMI protocol to allow bidirectional high-speed data transmission over an
17 HDMI connector. In particular, Yoshida describes reassigning pins 14 (Reserved) and 19 (HPD) for
18 bidirectional LAN communication. *See* Yoshida at Fig. 9 and corresponding description.

19 U.S. Patent No. 6,738,417 to Kim et al. (“Kim 417”), issued May 18, 2004, discloses and
20 claims “[a]n apparatus for bidirectional data transfer between a computer and a display connected
21 through cables having a first end at the computer and a second end at the display, the apparatus
22 comprising: a transmitter located at the computer for transmitting a pixel clock and forward data
23 aligned to the pixel clock to the receiver in a forward channel; [and] a receiver located at the display
24 for receiving the pixel clock and the forward data from the transmitter, and for transmitting
25 backward data to the transmitter in a backward channel, wherein the transmitter further comprises
26 an oversampling circuit for generating a plurality of oversampling clocks for sampling the backward
27 data received from the receiver, each clock being equally spaced in phase from its adjacent clock.”
28 Kim 417 at 5:32-47. Kim 417 further describes the use of synchronization signals. *Id.* at 5:10-23.

1 Kim 417 was originally assigned to Silicon Image, Inc. and shares one or more inventors with the
2 '103 Patent.

3 U.S. Patent Publ. No. 2010/0128176 to Nakajima et al. ("Nakajima") filed on November 7,
4 2007 and published on May 27, 2010, discloses "a receiving device that receives video and audio
5 signals from an external apparatus to perform image displaying and audio outputting, a delay-
6 information transmitting method of the receiving device, an audio output device, and a delay-control
7 method of the audio output device." Nakajima at ¶ 0001. Specifically, Nakajima describes an
8 "HDMI source [which] transmits a differential signal corresponding to pixel data of a non-
9 compressed 1-screen image unidirectionally to the HDMI sink [] through a plurality of channels in
10 an effective image period . . . i.e., a period obtained by removing a horizontal blanking period and
11 a vertical blanking period from a period between one vertical synchronizing signal and a subsequent
12 vertical synchronizing signal. The HDMI source [] further transmits differential signals
13 corresponding to the audio data and the control data which accompany at least the image, other
14 auxiliary data, etc., unidirectionally to the HDMI sink [] through a plurality of channels in the
15 horizontal blanking period or the vertical blanking period." Nakajima at ¶ 0122. The inventor of
16 Nakajima is also named on several other patents and published applications, each of which includes
17 similar disclosure, including:

- 18 • Japanese Patent No. 4844230
- 19 • U.S. Patent Publ. No. 2010/0066919
- 20 • U.S. Patent Publ. No. 2010/0073574
- 21 • U.S. Patent Publ. No. 2010/0269137
- 22 • U.S. Patent Publ. No. 2010/0118188

23 U.S. Patent No. 7,836,223 to Butcher ("Butcher") is another Silicon Image patent that
24 discusses modifying HDMI to allow bidirectional data transfer. In particular, Butcher modifies
25 HDMI so that Ethernet data can be communicated bidirectionally over the AV channels at times
26 when those channels are not used to transmit unidirectional AV data.

27 U.S. Patent Publ. No. 2014/0019653 to Amchislavsky et al. ("Amchislavsky") is yet another
28 Silicon Image patent relating to bidirectional communication of USB over an AV protocol link. In

1 particular, just like the '103 patent, Amchislavsky describes bidirectional communication of USB
2 over a Mobile High-definition Link (MHL) connection. Amchislavsky describes a link including a
3 data channel for AV data and a separate bidirectional control channel. According to Amchislavsky,
4 the MHL “specification allows for a connector to be utilized for transmission of both MHL data and
5 USB™ (Universal Serial Bus) data, where USB data may be transmitted when the connector is not
6 being utilized for the transmission of MHL data” but that “such use may be limited to only one of
7 such protocols at any time.” Amchislavsky at [0002]-[0003]. Amchislavsky thus describes methods
8 and apparatus allowing simultaneous bidirectional USB data transmission and unidirectional AV
9 data transmission over an MHL link.

10 U.S. Patent Publ. No. 2014/0004741 to Jol (“Jol”), published Jan. 2, 2014, discloses a
11 connector with “one pair of contacts for transmitting data and one pair of contacts for receiving data.
12 All data transmitted and received using the plug connector is serialized/de-serialized to enable data
13 transmission at a very high rate.” Jol at Abstract. The serialized data includes video data (such as
14 HDMI and DisplayPort data) and USB data. Jol further describes a “single wire” for control. Jol at
15 [0020].

16 U.S. Patent Publication No. 2008/0084834 to Stanek (“Stanek”), published Apr. 10, 2008,
17 discloses methods and apparatus for transmitting/receiving unidirectional HDMI video data and
18 bidirectional USB data over the same multimedia link, and sending/receiving control data over a
19 bidirectional control line (e.g. CEC line).

20 U.S. Patent No. 5,974,464 to Shin 464 (“Shin 464”), issued on Oct. 26, 1999, discloses
21 systems and method for high speed serial video signal transmission using DC-balanced coding. Shin
22 464 discloses a high-speed digital interface implemented in low-cost scalable CMOS technology.

23 U.S. Patent Publ. No. 2013/0266154 to McCormack (“McCormack”) was filed on Feb. 26,
24 2013, published on Oct. 10, 2013, and was issued on Dec. 22, 2015. McCormack discloses a
25 contactless, electromagnetic (EM) replacement for cabled Standards-based interfaces (such as USB,
26 I2S) which handles data transfer requirements associated with the Standard, and capable of
27 measuring and replicating relevant physical conditions on data lines so as to function compatibly
28 and transparently with the Standard.

1 The Video Electronics Standards Association (VESA) DisplayPort Standard Version 1,
2 Revision 2 (“DisplayPort 1.2”) “define[s] a flexible system and apparatus capable of transporting
3 video, audio and other data between a Source Device and a Sink Device over a digital
4 communications interface.” DisplayPort 1.2 at 1. A DisplayPort link as defined in DisplayPort 1.2
5 “consists of a main link, an auxiliary channel (AUX CH), and a Hot Plug Detect (HPD) signal line.”
6 *Id.* at 34. “[T]he Main Link is a unidirectional, high-bandwidth and low-latency channel used to
7 transport isochronous data streams such as uncompressed video and audio. The auxiliary channel is
8 a half-duplex bidirectional channel used for link management and device control. The HPD signal
9 also serves as an interrupt request by the Sink device.” *Id.* Moreover, DisplayPort 1.2 included a
10 Fast AUX capability, which allowed bidirectional communication of USB 2.0 data over the AUX
11 channel. *Id.* at 20.

12 Additional information about the operation of prior art systems implementing DisplayPort
13 1.2 can be found in the following documents:

- 14 • Craig Raymond Wiley, “Invited Paper: DisplayPort 1.2, Embedded DisplayPort, and
15 Future Trends,” *Society for Information Display (SID) Symposium Digest of*
16 *Technical Papers*: Volume 42, Issue 1 (June 2011) at 551-554 (Wiley) (published
17 Aug. 12, 2012) (“Wiley”);
- 18 • Mats Erik Setterberg, DisplayPort Link training optimization, Master’s Thesis,
19 Department of Computer Science and Engineering, Chalmers University of
20 Technology, University of Gothenburg (Sweden, 2017) (“Setterberg”);
- 21 • Alan Kobayashi, DisplayPort Ver. 1.2 Overview, DisplayPort Developer Conference
22 (Taipei, Dec. 6, 2010) (“DisplayPort 1.2 Overview”);
- 23 • Craig Wiley, DisplayPort Technical Overview, IEEE International Conference on
24 Consumer Electronics (ICCE) (Las Vegas, Nevada, Jan. 10, 2011) (“DisplayPort
25 Technical Overview”);
- 26 • U.S. Patent Publ. No. 2013/0244491 to Sarwar and Terlizzi (“Sarwar 491”).

27 Digital Visual Interface Revision 1.0 (“DVI 1.0”) is a protocol specification for high-speed
28 digital AV content. DVI 1.0 included a transition-minimized differential signaling (TMDS) link to

1 send graphics data to a display. See DVI 1.0 at Section 2.1. DVI 1.0 also incorporates the VESA
2 display data channel (DDC) and extended display identification data (EDID) for control signaling.
3 DVI 1.0 discloses synchronization signals.

4 IEEE 1394-1995 (“Firewire”) was a high-speed peer-to-peer serial interface standard. The
5 Firewire connector included six wires, including two signal pairs and one power pair. Firewire
6 included the use of tokens during configuration, arbitration, and data transmission. Additional
7 information about the operation of prior art systems implementing Firewire can be found in the
8 following documents:

- 9 • Michael Johas Teener, “Technical Introduction to IEEE 1394” (2004),
10 www.ieee802.org/802_tutorials/04-July/NewTechIntroTo1394.pdf
- 11 • John Canosa, “Fundamentals of Firewire™,” Questra Consulting,
12 <https://public.ostfalia.de/~bermbach/research/firewire/files/basics.pdf>

13 “High-Definition Multimedia Interface Specification Version 1.3a” (“HDMI 1.3a”),
14 published Nov. 10, 2006, by HDMI Licensing, LLC defines an interface “for transmitting digital
15 television audiovisual signals from DVD players, set-top boxes and other audiovisual sources to
16 television sets, projectors and other video displays” based on “Transition Minimized Differential
17 Signaling (TMDS).” HDMI 1.3a at 1. “HDMI can carry high quality multi-channel audio data and
18 can carry all standard and high-definition consumer electronics video formats [and] can also carry
19 control and status information in both directions.” *Id.* In particular, HDMI 1.3a describes an
20 interface between an HDMI source and HDMI sink including “four differential pairs that make up
21 the TMDS data and clock channels [that] are used to carry video, audio and auxiliary data” from
22 source to sink, a bidirectional display data channel (DDC) line “used for configuration and status
23 exchange between a single Source and a single Sink,” and an optional bidirectional consumer
24 electronics control (CEC) line that “provides high-level control functions between all of the various
25 audiovisual products in a user’s environment.” *Id.* at 8. This is shown in Figure 3-1:

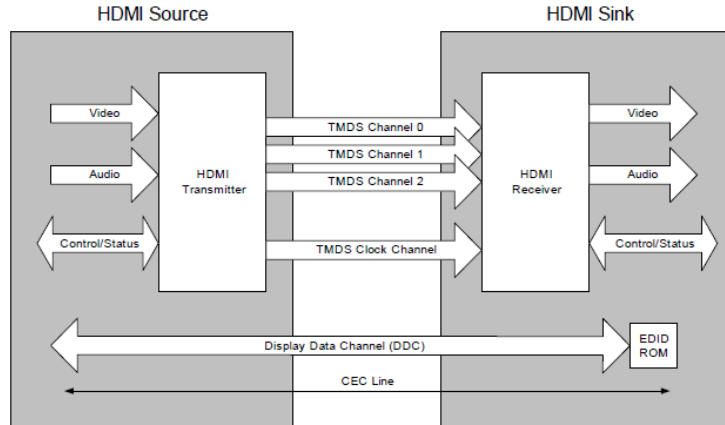
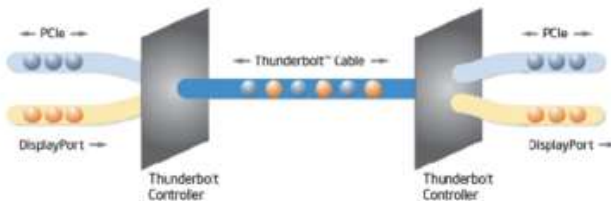


Figure 3-1 HDMI Block Diagram

Thunderbolt is a data communication protocol capable of transmitting bidirectional general data (e.g. PCI Express data) and unidirectional DisplayPort data over a single cable. The PCIe and DisplayPort data are multiplexed and transmitted over the same Thunderbolt cable, as shown below:

How Thunderbolt™ technology works

Intel Thunderbolt™ controller chips interconnect a PC and other devices, transmitting and receiving information for both PCI Express® (PCIe®) and DisplayPort® protocols. The Thunderbolt™ controller chip switches between the two protocols to support communications over a single cable. Intel is making its controller chips available to the industry, and is working with other component manufacturers to deliver the Thunderbolt™ connectors and cables.



Several Apple computer models included Thunderbolt capability before the priority date of the '103 Patent. These include at least the MacBook Pro (early 2011 and later); MacBook Air (mid 2011 and later); Mac mini (Mid 2011 and later); iMac (mid 2011 and later); Mac Pro (late 2013); and MacBook Pro (Retina, late 2013 and later). See MacBook Pro User Guide (2011); MacBook Air User Guide (2011); Mac mini User Guide (2011); iMac User Guide (2011); Mac Pro QuickStart Guide (2013); and MacBook Pro QuickStart Guide (2013) (all disclosing the inclusion of one or more Thunderbolt 1 and/or Thunderbolt 2 ports). Additional information about the operation of prior

art systems implementing Thunderbolt can be found in the following documents: Blessy C. Simon, “Thunderbolt Pinout (Thunderbolt 1, 2, 3, and 4),” <https://www.etechnophiles.com/thunderbolt-pinout-1-2-3-4/>

- Intel, “Thunderbolt Technology, The Fastest Connection to your PC” (2012), (“Intel Technology Brief”)
- Intel, “How Thunderbolt Technology Works” (2013), available at <https://web.archive.org/web/20131109071010/https://thunderbolttechnology.net/tech/how-it-works> (“How Thunderbolt Works”)
- Intel, “Thunderbolt Technology, The Fastest Connection To Your PC Experience” (2013), available at <https://web.archive.org/web/20131109071530/https://thunderbolttechnology.net/tech/PC-Experience> (“PC Experience”)
- Apple, “Introducing Thunderbolt” (2011), available at <https://web.archive.org/web/20110226054716/http://www.apple.com/thunderbolt> (“Introducing Thunderbolt”)
- Apple Insider, “Intel details Thunderbolt, says Apple has full year head start” (Feb. 24, 2011), available at https://appleinsider.com/articles/11/02/24/intel_details_thunderbolt_as_exclusive_to_apple_until_2012.html (“Apple Insider”)

U.S. Patent No. 7,746,798 to Shin et al. (“the ’798 Patent”), issued June 29, 2010 and published as US 2002/0172200 on Nov. 21, 2002, describes a “serial communications architecture for communicating between hosts and data store devices.” The ’798 Patent discloses the use of “synchronization signals” in language nearly identical to the discussion of synchronization signals in the ’103 Patent. For example, the ’798 Patent states the following:

A synchronization signal is typically used by the physical layer to help ensure correct alignment of symbols. A transmitting communications node periodically transmits synchronization primitives so that the receiving communications node can properly align with that synchronization primitive. When a communications node receives a

1 synchronization primitive, it knows that the primitive is correctly aligned on a
2 symbol boundary.

3 '798 Patent at 14:34-41; *compare* '103 Patent at claim 17 and 5:55-59. The '798 Patent was
4 originally assigned to Silicon Image, Inc. and is asserted by UCT in this litigation.

5 U.S. Patent No. 4,486,739 to Franaszek ("Franaszek") describes an 8b/10b coding scheme,
6 in which 8 bits are encoded into 10 bit code words. Franaszek discloses several special characters,
7 including "comma" codes that are used for synchronization. The 8b/10b coding scheme developed
8 by Franaszek is used in a variety of communication protocols, including DisplayPort.

9 U.S. Patent No. 8,238,445 to Wang ("Wang 445") discloses a video and audio data
10 synchronization method for HDMI. In particular, Wang describes the transmission of
11 synchronization signals and a method for determining and aligning symbol boundaries in HDMI
12 data transmission.

13 U.S. Patent No. 6,535,505 to Hwang et al. ("Hwang") discloses the use of frame
14 synchronization signals in time-division multiplex communications. U.S. Patent 5,420,640 to
15 Munich et al. ("Munich") discloses a system for multiplexed communication of video, audio, and
16 other data in which various synchronization signals are transmitted.

17 U.S. Patent No. 5,420,640 to Munich et al. ("Munich") discloses a receiver for receiving
18 digital data frames including multiple lines of data, including video, audio, and other data. Munich
19 at Abstract. Munich further discloses that the beginning of each frame of data is indicated with a
20 frame synchronization word and the beginning of each line of data is indicated with a horizontal
21 synchronization byte. *Id.*

22 U.S. Patent Publ. No. 2015/0280895 to Whitby-Strevens and Johnston ("Whitby-Strevens")
23 describes modifications to DisplayPort standards. Whitby-Strevens explicitly lists several
24 DisplayPort standards, including DisplayPort 1.2. *See* Whitby-Strevens at [0036]. It also explicitly
25 discusses USB. *Id.* at [0033] and [0042]. In particular, Whitby-Strevens discusses the use of 8b/10b
26 encoded control symbols in the DisplayPort standards, including control symbols used for
27 synchronization during normal operation and link training.

1 Universal Serial Bus Specification, Revision 2.0, April 27, 2000 (“USB 2.0”). USB 2.0
2 provides for packet-based, half-duplex bidirectional data communication over a single differential
3 pair of wires. Although USB 2.0 is intended for communicating a range of different data types, one
4 stated goal of USB 2.0 was to provide “[f]ull support for real-time data for voice, audio, and video.”
5 USB 2.0 at 11. Different classes of USB 2.0 devices are capable of different functions; one example
6 is the video class (discussed in more detail below).

7 On-The-Go Supplement to the USB 2.0 Specification (“USB OTG”) is a supplement that
8 added new functionality to the protocol specified in the Universal Serial Bus Specification, Revision
9 2.0 (“USB 2.0”). USB OTG added the capability for USB devices to communicate via the GND and
10 VBUS lines to negotiate roles. Mobile phones were one target (or anticipated) application of USB
11 OTG. For example, the Sony Xperia line of smartphones (including, e.g. the Xperia S) had USB
12 OTG capabilities. YouTube videos uploaded in 2012 show users streaming video files from USB
13 flash drives to their phones over a USB OTG connection, and documents describe bidirectional data
14 transfer to and from an Xperia 6 via USB OTG. Additional information about the operation of prior
15 art systems implementing USB OTG can be found in the following documents:

- 16 • “Sony Xperia S USB OTG demo,” YouTube video dated Mar. 8, 2012 and available
17 at <https://www.youtube.com/watch?v=xPU2gOlk2po> (“Xperia S YouTube Video
18 1”);
- 19 • “Sony Xperia S: USB OTG Increases Storage Space / Transfer Files Between
20 Smartphones,” YouTube video dated July 29, 2012 and available at
21 <https://www.youtube.com/watch?v=Gxe-nN4rmRk> (“Xperia S YouTube Video 2”);
- 22 • “Sony Xperia S UK release date announced,” Digital Spy article dated Jan. 10, 2012
23 and available at: [https://www.digitalspy.com/tech/smartphones/a359414/sony-](https://www.digitalspy.com/tech/smartphones/a359414/sony-xperia-s-uk-release-date-announced/)
24 [xperia-s-uk-release-date-announced/](https://www.digitalspy.com/tech/smartphones/a359414/sony-xperia-s-uk-release-date-announced/) (“Xperia S Digital Spy Article”);
- 25 • “Sony Xperia S (unlocked) review: Sony Xperia S (unlocked),” CNET article dated
26 July 25, 2012 and available at: [https://www.cnet.com/reviews/sony-xperia-s-](https://www.cnet.com/reviews/sony-xperia-s-unlocked-review/)
27 [unlocked-review/](https://www.cnet.com/reviews/sony-xperia-s-unlocked-review/) (“Xperia S CNET Article”);

- 1 • “Sony Xperia S review,” The Verge article dated March 5, 2012 and available at:
2 <https://www.theverge.com/2012/3/5/2841547/sony-xperia-s-review> (“Xperia S The
3 Verge Article”);
- 4 • Sony, “User Guide, Xperia S LT261” (2013) (“Xperia S User Guide”);
- 5 • Universal Serial Bus Specification, Revision 2.0, April 27, 2000 (“USB 2.0”);
- 6 • On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification,
7 Revision 1.0a, June 24, 2003 (“USB OTG 1.0a”);
- 8 • W. Ray and D. Harmon, “USB On-th-Go Solutions,” TI Developer Conference, Mar.
9 7-9, 2007 (Dallas, TX) (“USB OTG Solutions”);
- 10 • “USB On-the-Go Basics,” maxim integrated, Dec. 20, 2002 (“USB OTG Basics”).

11 Universal Serial Bus Device Class Definition for Video Devices, Revision 1.5, August 9,
12 2012 (“USB Video Class”) defines the capabilities and characteristics of a USB Video Class device.
13 It explicitly refers to USB 2.0 (as well as the later USB 3.0).

14 U.S. Patent Publ. No. 2006/0076977 to Zhu (“Zhu 977”) describes devices and methods to
15 enable a USB 1.1 device to communicate with a USB OTG device. In particular, Zhu 977 explains
16 the operation of USB OTG, including bidirectional transmission of control signals through VBUS
17 pulsing as part of session request protocol (SRP) and the transmission of video and USB data.

18 U.S. Patent No. 8,019,905 (“Wu”) discloses methods and apparatus for converting AV and
19 control data between DisplayPort and a TMDS-based protocol such as DVI, for communication
20 between one or more video sources and a video display. For example, Wu 905 describes converting
21 image data from DisplayPort format to DVI format for communication to a video display. Wu 905
22 also explicitly describes converting control signals between DisplayPort AUX channel and DVI
23 DDC lines for bidirectional communication of control information between the source and sink.

24 TI SN75DP129 is a chip for converting “a Dual-Mode DisplayPort input to Transition-
25 Minimized Differential Signaling (TMDS) output.” The TMDS output may be compliant with DVI
26 1.0 or HDMI 1.3.

27 U.S. Patent No. 8,332,518 to Bradshaw et al. (“Bradshaw”) filed on August 13, 2007 and
28 issued on December 11, 2012, discloses methods and devices involving a “bidirectional

1 communication protocol for data communication between a first device and a second device. The
2 method includes: during a first time interval, transmitting data from the first device to the second
3 device; and during a second time interval, (a) after the occurrence of a first event, (i) suspending
4 data transmission from the first device to the second device; and (ii) transmitting control data from
5 the second device to the first device; and (b) after the occurrence of a second event, transmitting
6 control data from the first device to the second device.” Bradshaw at Abst. The communication
7 protocol disclosed in Bradshaw involves the use of various synchronization signals between the first
8 and second devices. *See, e.g.*, Bradshaw at 3:64-4:16, Figs. 2-5.

9 The Mobile High-Definition Link (“MHL”) is a computing standard developed to transport
10 high-quality uncompressed audio and video. MHL was developed by the MHL Consortium,
11 consisting of Nokia, Samsung, Silicon Image, Sony, and Toshiba. MHL 1.0 was embodied in
12 connectors first sold or offered for sale in the United States no later than June 28, 2010; MHL 2.0
13 was embodied in connectors sold or offered for sale in the United States no later than April 20, 2012;
14 and MHL 3.0 was embodied in connectors sold or offered for sale in the United States no later than
15 August 22, 2013. The first connector, Micro-USB, became configured with the MHL standard no
16 later than December 1, 2010. Example devices using a port or connector conforming to the MHL
17 standard include the Samsung Galaxy S II smart phone offered for sale in the United States no later
18 than February 23, 2011; and the HTC One X smart phone offered for sale in the United States no
19 later than May 6, 2012.

20 Accordingly, because each of the identified references are directed to similar devices in the
21 similar field of endeavor, a person of ordinary skill in the art would be motivated to combine the
22 teachings of two or more references together because the references disclose similar systems that
23 solve the same problems in similar ways. Thus, it would have been obvious to one of ordinary skill
24 in the art to combine any of the foregoing references and one of ordinary skill would have expected
25 such a combination to be successful.

26 Thus, to the extent that it is determined that any of the above references do not disclose a
27 particular claim element, it would have been obvious to modify the teachings of that reference to
28

1 include such element as taught in any other of the above references that discloses such element (as
2 documented in the claim charts attached as Exhibits H-1 through H-36).

3 For example, to the extent that it is determined that any of the above references do not
4 disclose “forward data compliant with a first standard comprising a universal serial bus (USB)
5 standard and different from a standard of the video data” and/or “backward units of data comprising
6 backward data compliant with the first standard” as claimed, it would further have been obvious to
7 modify the teachings of that reference to include this feature in view of the knowledge of a POSITA
8 and the teachings of these features in at least the following references: *See, e.g.*, Zhu 537, Lyle,
9 Park, Kim 030, Kobayashi, Lida 337, Lida 327, Yoshida, Kim 417, Butcher, Amchislavsky, Stanek,
10 MHL, and Jol. Therefore, a person of ordinary skill in the art would be motivated to make such a
11 modification and/or combination.

12 As an additional example, to the extent that it is determined that any of the above references
13 do not disclose a “over a second physical channel of the multimedia link distinct from the first
14 physical channel: sending control data from the source device to the sink device” and/or “receiving
15 control data from the sink device to the source device over the second physical channel of the
16 multimedia link distinct from the first physical channel” as recited in claims 1, 11, 21, and/or 22, it
17 would further have been obvious to modify the teachings of that reference to include this feature in
18 view of the knowledge of a POSITA and the teachings of these features in at least the following
19 references: DisplayPort 1.2, DisplayPort System, DVI 1.0, HDMI 1.3a, USB OTG, Thunderbolt,
20 Zhu 537, Lyle, Park, Kim 030, Kobayashi, Lida 337, Lida 327, Yoshida, Kim 417, Butcher,
21 Amchislavsky, Stanek, MHL, and Jol. Therefore, a person of ordinary skill in the art would be
22 motivated to make such a modification and/or combination.

23 As an additional example, to the extent that it is determined that any of the above references
24 do not disclose the claimed “transmitter[s],” “receiver[s],” and “transceiver[s]” recited in claims 21
25 and 22, it would further have been obvious to modify the teachings of that reference to include this
26 feature in view of the knowledge of a POSITA and the teachings of these features in at least the
27 following references: DisplayPort 1.2, DisplayPort System, DVI 1.0, HDMI 1.3a, USB OTG,
28 Thunderbolt, Zhu 537, Lyle, Park, Kim 030, Kobayashi, Lida 337, Lida 327, Yoshida, Kim 417,

1 Butcher, Amchislavsky, Stanek, MHL, and Jol. Therefore, a person of ordinary skill in the art would
2 be motivated to make such a modification and/or combination.

3 As an additional example, to the extent that it is determined that any of the above references
4 do not disclose “sending a second synchronization signal of a second length longer than the first
5 synchronization to initialize communication over the first physical channel before sending the first
6 forward unit of data” as recited in claim 3, it would further have been obvious to modify the
7 teachings of that reference to include this feature in view of the knowledge of a POSITA and the
8 teachings of these features in at least the following references: *See, e.g.*, Zhu 537, Lyle, Kim 030,
9 Kobayashi, '798 Patent, Lida 337, Franaszek, Yoshida, Kim 417, Wang, Hwang, Munich, Whitby-
10 Strevens, DisplayPort 1.2, DisplayPort System, DVI 1.0, HDMI 1.3a, USB 2.0 (and thus USB
11 OTG), MHL, and Thunderbolt. Therefore, a person of ordinary skill in the art would be motivated
12 to make such a modification and/or combination.

13 As an additional example, to the extent that it is determined that any of the above references
14 do not disclose “aligning a boundary of a symbol in a first forward unit of data of the forward units
15 of data using the first synchronization signal.” as recited in claim 17, it would further have been
16 obvious to modify the teachings of that reference to include this feature in view of the knowledge
17 of a POSITA and the teachings of these features in at least the following references: *See, e.g.*,
18 Kobayashi, '798 Patent, Franaszek, Yoshida, Kim 417, Wang, Hwang, Munich, Whitby-Strevens,
19 DisplayPort 1.2, DisplayPort System, DVI 1.0, HDMI 1.3a, USB 2.0 (and thus USB OTG), and
20 Thunderbolt. Aligning symbol boundaries was a well-known use for synchronization signals. *See,*
21 *e.g.*, '798 patent at 15:17-21 (“The receiving communications node uses the synchronization
22 primitive encoded with packet type to align its symbol boundaries and to rapidly identify the packet
23 type. This alignment and identification can occur in the physical and link layers.”). Therefore, a
24 person of ordinary skill in the art would be motivated to make such a modification and/or
25 combination.

26 As an additional example, to the extent that it is determined that any of the above references
27 do not disclose the basic concept of the independent claims—namely, over a first physical channel,
28 communicating AV data in one direction and USB data bidirectionally and, over a second physical

1 channel, communicating control information—it would have been obvious to modify any such
2 reference in view of Zhu 537, Lyle, Park, Kim 030, Kobayashi, Lida 337, Lida 327, Yoshida, Kim
3 417, Nakajima, Butcher, Amchislavsky, Jol, DisplayPort 1.2, DisplayPort System, MHL, and USB
4 OTG system (e.g. Sony Xperia S) to include this feature. As demonstrated in the attached claim
5 charts for these references, each discloses transmitting AV data in one direction and transmitting
6 and receiving bidirectional data. Although the references differ on how the unidirectional AV data
7 and bidirectional data are assigned to various channels, collectively they demonstrated that various
8 permutations were well known in the art at the time. For example, Zhu 537, Lyle, and Park each
9 disclose communicating unidirectional AV data and bidirectional USB data on one channel (and in
10 some cases, on the same wire pair) while communicating bidirectional control data on a separate
11 channel. Lida 337 discloses communicating AV data, ethernet data, and control data in one direction
12 on a first channel, and ethernet and control data in the opposite direction on a second channel. Lida
13 327 and Kobayashi disclose transmitting AV data unidirectionally on a first channel, while
14 transmitting USB data and control signals bidirectionally on a second channel. Kim 030 discloses
15 transmitting AV data unidirectionally on a first channel, USB data bidirectionally on a second
16 channel, and control signals bidirectionally on a third channel. And Butcher describes transmitting
17 AV data and other data in one direction on a first channel, receiving other data on a second channel,
18 and communicating control signals bidirectionally on a third channel. Thus, a POSITA at the time
19 would have known that it was possible to communicate unidirectional AV data, bidirectional USB
20 data, and bidirectional control signals over a variety of channel permutations and combinations, and
21 it would have been obvious to try the specific permutation claimed in the '103 Patent—especially
22 considering that multiple prior art references taught that same permutation.

23 As an additional example, to the extent that it is determined that any of the above references
24 do not disclose “[a] non-transitory computer readable storage medium storing instructions thereon,
25 the instructions representing a digital design of a circuit” as recited in claim 22, it would further
26 have been obvious to modify the teachings of that reference to include this feature in view of the
27 knowledge of a POSITA and the teachings of these features in at least the following references: *See,*
28 *e.g.,* Zhu 537, Lyle, Kim 030, Lida 327, Butcher, MHL, and Amchislavsky.

1 A person skilled in the art would have been motivated to combine any of the above
2 references. In particular, the combinations identified herein would merely have been (a) a
3 combination of prior art elements according to known methods to yield predictable results; (b) a
4 simple substitution of one known element for another to obtain predictable results; (c) a use of
5 known technique to improve similar devices or methods in the same way; (d) application of a known
6 technique to a known device or method ready for improvement to yield predictable results; (e)
7 obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in
8 either the same field or a different one based on design incentives or other market forces since the
9 variations are predictable to one of ordinary skill in the art. Moreover, a person of ordinary skill in
10 the art had a reason to combine these references because—at a minimum—they all pertain to
11 communicating different forms of data over a multimedia link.

12 As discussed above, the motivation to combine the teachings of the patents and other prior
13 art referenced above is found in the art as specified in the charts and in: (1) the nature of the problem
14 being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of
15 persons of ordinary skill in the art; and (4) the fact that the prior art is generally directed towards
16 providing connectivity for communication of data including A/V data between, for example,
17 computers, peripherals, and/or displays, and (5) the predictable results obtained in combining the
18 different elements of the prior art. The Supreme Court has held that a showing of a motivation to
19 combine within the references themselves is not required to prove obviousness. *See KSR*, 550 U.S.
20 at 401 (“Any need or problem known in the field of endeavor at the time of invention may provide
21 the motivation to combine.”).

22 As illustrated in the claim charts attached as Exhibits H-1, H-23, H-24, and H32, Zhu 537,
23 alone or in combination with a reference describing DisplayPort, including but not limited to
24 DisplayPort 1.2, disclose or render obvious all elements of the ’103 Asserted Claims. Specifically,
25 Zhu 537 teaches methods and apparatuses for transmitting USB data and audio/visual data over a
26 DisplayPort link. Zhu 537 teaches a “mixed mode” in which USB may be multiplexed with
27 DisplayPort data for transmission in the forward direction, while USB data may also be transmitted
28 in the backward direction during a video blanking period. Zhu 537 explains that DisplayPort

1 includes one to four lanes for transmission of video data and a separate bidirectional side-band
2 channel for control information. DisplayPort 1.2 further describes the transmission, reception, and
3 use of numerous signals (including, e.g., control symbols and symbol patterns for link training) for
4 purposes of initializing communication, synchronization, and alignment of symbol boundaries. A
5 person skilled in the art would have been motivated to combine Zhu 537 with DisplayPort 1.2 for
6 the reasons provided above. Both Zhu 537 and DisplayPort 1.2 relate to communication of A/V data
7 and, in particular, data compliant with the DisplayPort 1.2 standard. Moreover, Zhu 537 explicitly
8 references DisplayPort 1.2 (and other versions of the DisplayPort standard) and discloses
9 embodiments that relate explicitly to the DisplayPort protocol. *See, e.g.*, Zhu 537 at Abstract; 1:42
10 – 2:14; 5:4-17; 17:3 – 18:20; Figs. 14-15; 33:20 – 36:24; Figs. 34-35, 41. Specifically, Zhu 537
11 describes a “system and corresponding method for selectively communicating data between a first
12 device and a second device” in which “[t]he first device may be configured to transmit, on a
13 DisplayPort link to the second device, a data flow comprising both USB protocol and uncompressed
14 high definition media data signals.” *Id.* at Abstract. Zhu 537 specifically describes embodiments
15 that are built on modifications to various aspects of DisplayPort 1.2. *See id.* at 34:52 – 36:24.
16 Moreover, Zhu 537 incorporates by reference the VESA DisplayPort standards and lists several
17 example versions. *Id.* at 1:42-47; 34:52-65. A POSITA would have been specifically motivated to
18 combine Zhu 537 with DisplayPort 1.2’s teachings about the side-band channel, including the AUX
19 and HPD lines. Zhu 537 explicitly references these concepts multiple times. *See id.* at 1:52-57; 5:6-
20 11. Moreover, a POSITA would understand that Zhu 537’s references to a “DisplayPort link” (*id.*
21 at 33:26-29), “first media port” (*id.* at 33:34-38), and “second media port” (*id.* at 33:43-46) would
22 inherently include the channels and links described in the DisplayPort standards available at the
23 time, including the side-band channel (e.g. AUX), and would also include the various control
24 symbols and symbol patterns for link training and other purposes. Additionally, the combination
25 reflects no more than a simple substitution of known elements for one another to obtain predictable
26 results. For example, Zhu 537 teaches a simple substitution of a modified MST protocol for the one
27 specified in DisplayPort 1.2.

1 Moreover, as illustrated in the claim charts attached as Exhibits H-3, H-23, and H-24, Park,
2 alone or in combination with a reference describing DisplayPort, including but not limited to
3 DisplayPort 1.2, disclose or render obvious all elements of the '103 Asserted Claims. Specifically,
4 Park teaches methods and apparatuses for transmitting USB data and audio/visual data over a
5 DisplayPort link. A person skilled in the art would have been motivated to combine Park with
6 DisplayPort 1.2 for many of the same reasons described above in connection with Zhu 537. Both
7 Park and DisplayPort 1.2 relate to communication of A/V data and, in particular, data compliant
8 with a DisplayPort standard. In fact, Park mentions DisplayPort in its title: "System and method for
9 transmitting USB data over a DisplayPort transmission link." *See also* Park at Abstract ("The
10 transmission link may comply with the DisplayPort standard"). The term "DisplayPort" appears at
11 least 40 times in Park. A POSITA would thus have been specifically motivated to combine Park
12 with DisplayPort 1.2's teachings about, for example, the side-band channel, including the AUX and
13 HPD lines, and synchronization / control signals. Additionally, the combination reflects no more
14 than a simple substitution of known elements for one another to obtain predictable results. For
15 example, Park teaches a simple substitution of a modified version of a DisplayPort link.

16 A POSITA would have been further motivated to modify Kim 030 to communicate
17 unidirectional AV data and bidirectional USB data over a single physical channel connected to a
18 single transmitter and single receiver. As discussed above, Kim 030 teaches a multimedia link
19 between source and sink for communicating unidirectional AV (HDMI) data, bidirectional USB
20 data, and bidirectional control signals. Unlike the independent claims of the '103 Patent, in Kim
21 030, AV data is communicated over one set of channels while bidirectional USB data is
22 communicated over "a dedicated USB connection differential pair." Kim 030 at 6:48 – 7:6. As
23 discussed above, however, UCT applies a broad construction in its infringement contentions such
24 that it alleges that multiple distinct differential pairs can form a single "physical channel." Thus, at
25 least under UCT's own applied construction, there is no distinction between Kim 030 and at least
26 the independent claims of the '030 Patent. Regardless, it would have been obvious to a POSITA in
27 view of the knowledge at the time (including the teaching of, for example, references such as Zhu
28 537 and Park) that Kim 030 could be modified such that unidirectional AV data and bidirectional

1 USB data would be communicated over a single physical channel (and by the same transmitter and
2 receiver) by, for example, multiplexing AV and USB data in the forward direction and using half-
3 duplex communication to send USB data in the reverse direction during available time slots (such
4 as a blanking period), as taught in Zhu 537. The teachings of Kim 030 itself would provide
5 motivation to modify Kim 030. For example, Kim 030 is directed to a mobile version of HDMI and,
6 as such, proposes to reduce the size of the HDMI connector for use with mobile devices. *See* Kim
7 030 at 4:31-37. To facilitate this, Kim 030 proposes multiplexing multiple HDMI channels to for
8 communication on a single pair of wires. *See* Kim 030 at 4:38-54 and 5:26-38. And the claims of
9 Kim 030 recite “merg[ing] multiple channels of a high-definition interface into a single channel.”
10 Kim 030 at claim 1. And at a high level, Kim 030 explicitly encourages further modification of
11 connectors for use with HDMI. *See* Kim 030 at 1:29-37. Taken together, these teachings of Kim
12 030 would have motivated a POSITA to modify Kim 030 so as to multiplex AV and USB data
13 together onto a single physical channel, as taught explicitly in Zhu 537. *See, e.g.,* Zhu 537 at 34:11-
14 24. This motivation is further supported by Zhu 537’s teaching that its principles are applicable to
15 HDMI, which is the standard that is the focus of Kim 030. *Id.* at 20:58 – 21:5.

16 For similar reasons, a POSITA would have been motivated to modify Yoshida to
17 communicate unidirectional AV data and bidirectional LAN data over a single physical channel
18 connected to a single transmitter and single receiver. Moreover, a POSITA would have been
19 motivated to modify Yoshida’s teachings to substitute bidirectional transmission of USB data for
20 bidirectional transmission of LAN data. Both LAN and USB were well-known packet-based
21 protocols and a POSITA would have understood that a link for communicating one could be
22 modified to allow communication of the other. Moreover, a POSITA would have been familiar with
23 prior art (including references such as Zhu 537, Park, Lyle, and Kim 030) that explicitly described
24 the bidirectional transmission of USB data over a multimedia link, channel, and/or cable and would
25 have been motivated and found it obvious to combine Yoshida with the teachings of any one or
26 more of those references.

27 A POSITA would also have been motivated to and found it obvious to combine Lyle with
28 (or modify Lyle in view of) the teachings of DVI 1.0. Lyle describes a “communication system

1 including a transmitter, a receiver, and a TMDS-like link, in which video data and auxiliary data
2 (typically including timing data associated with other auxiliary data) are transmitted from the
3 transmitter to the receiver, or in which video data are transmitted over the link from the transmitter
4 to the receiver, and auxiliary data (typically including timing data associated with other auxiliary
5 data) are transmitted from the receiver to the transmitter.” Lyle at Abstract. Lyle explains that USB
6 data is a type of auxiliary data that could be transmitted. Lyle at 50:47-50. Lyle describes
7 embodiments in which “the transmitter transmits video data and auxiliary data to the receiver over
8 a video channel of the link” (*id.* at 8:46-48) and explains that auxiliary data may be sent in the
9 opposite direction by “reversing one video data transmission channel, or two or more video data
10 transmission channels, during blanking periods (to send auxiliary data from the receiver of the video
11 data to the transmitter of the video data)” (*id.* at 45:43-48). Further, embodiments include a Display
12 Data Channel for bidirectional transmission of control data. *See id.* at 28:26-45. Lyle explicitly
13 describes modifications to a TMDS link according to the DVI protocol. A POSITA would therefore
14 have found it obvious that the system described in Lyle would include features, such as
15 synchronization signals, disclosed in DVI standards, such as DVI 1.0 (or at the very least, would
16 have found it obvious to combine Lyle with such teachings in DVI 1.0).

17 A POSITA would also have been motivated to and found it obvious to combine Jol with the
18 teachings of various references, including USB 2.0, DisplayPort 1.2, and HDMI 1.3a. Jol explicitly
19 discusses transmitting and receiving data according to each of these protocols over a multimedia
20 link. *See, e.g.,* Jol at Fig. 4, [0031], [0034]-[0036]. A POSITA would thus have been motivated to
21 combine Jol with (or modify Jol in view of) the teachings in these other references of, for example,
22 a dedicated bidirectional control channel and a synchronization signals. For example, Jol discusses
23 the need to communicate control signals including via “[a] single wire, serial control chip.” Jol at
24 [0020]. A POSITA would have thus recognized the utility of a dedicated control channel as
25 discussed in references such as USB 2.0, DisplayPort 1.2, and HDMI 1.3a when communicating
26 data according to such protocols. Similarly, a POSITA would have recognized that the protocols
27 described in USB 2.0, DisplayPort 1.2, and HDMI 1.3a include the synchronization symbols
28 described in those references, and would have found it obvious that the system described in Jol

1 would thus transmit such synchronization signals (or at the very least, would have found it obvious
2 to use the system described in Jol to transmit such synchronization signals).

3 A POSITA would also have been motivated to and found it obvious to combine Stanek with
4 the teachings of any HDMI specification, including HDMI 1.3a. Stanek explicitly references HDMI
5 and, in particular, incorporates by reference the HDMI 1.3 specification. Stanek at [0036]. A
6 POSITA would also have been motivated to combine Stanek with any USB standard, including USB
7 2.0, because Stanek explicitly references USB throughout its disclosure specifically cites to USB
8 2.0. Stanek at [0004]. A POSITA would also have been motivated to combine Stanek with DVI 1.0,
9 because Stanek also mentions DVI. Stanek at [0005].

10 To the extent that any of Park, Kim 030, Kobayashi, Lida 327, Lida 337, Yoshida, Kim 417,
11 Butcher, Amchislavsky, or Nakajima do not disclose sending forward units of data including video
12 data and USB data over a first physical channel during first time periods and receiving USB data
13 over the first physical channel during second time periods, a POSITA would have been motivated
14 and found it obvious to modify the teaching of such reference with, for example, the teachings in
15 Zhu 537, Lyle, Stanek, and/or Jol to include such a feature. Each of Park, Kim 030, Kobayashi, Lida
16 327, Lida 337, Yoshida, Kim 417, Butcher, Amchislavsky, Nakajima, Zhu 537, Lyle, Stanek, and
17 Jol disclose the transmission of AV data and bidirectional other data (including USB data) over one
18 or more channels of a multimedia link. At least Zhu 537, Lyle, Stanek, and Jol explicitly disclose
19 that AV data and bidirectional other data (including USB data) can be sent and received on the same
20 channel at different times. As evident in the claim charts attached as Exhibits H, these references
21 and others repeatedly emphasize that the principles of operation described in connection with one
22 protocol or standard (e.g. DisplayPort, HDMI, DVI, MHL, USB) are applicable to other protocols
23 and standards.

24 A POSITA would have been further motivated to combine Zhu 537, Park, Kim 030, Lyle,
25 Butcher, Candalore, Anchislavsky, Lida 337, Lida 327, Yoshida, Nakajima, Jol, and/or Kim 417,
26 either alone or in combination with other art, with Kobayashi. These references all disclose similar
27 systems that solve the same problems (e.g. bidirectional transmission of USB data and unidirectional
28 transmission of AV data in a multimedia link) in similar ways. Moreover, at least Zhu 537, Park,

1 and DisplayPort 1.2 all relate to the DisplayPort standards. Zhu 537, Park, and DisplayPort 1.2
2 explicitly reference the DisplayPort standard. Although Kobayashi does not reference the
3 DisplayPort standards explicitly, it was filed less than a year after the release of DisplayPort, version
4 1.0 and includes language and figures that seemingly reference DisplayPort concepts. *Compare*,
5 *e.g.*, Kobayashi at Fig. 12 (discussing bidirectional “Aux. Ch.” and unidirectional “Main Link”) to
6 DisplayPort, version 1.0 at Figure 1.2 (discussing bidirectional “AUX CH” and unidirectional
7 “Main Link”); *see also* Kobayashi at [0071] (discussing “link training”). More fundamentally,
8 Kobayashi explicitly discusses a multimedia interface for audio/visual data. And although Kim 030
9 does not reference DisplayPort, as discussed below a POSITA would have found it obvious to
10 combine a reference describing the transmission of data in connection with a HDMI standard (such
11 as Kim 030) with a reference describing the transmission of data in connection with a DisplayPort
12 standard (such as Kobayashi).

13 Moreover, as explained in further detail below, a POSITA would have been motivated and
14 found it obvious to combine any one or more AV Link Plus Data References with any one or more
15 AV Protocol and/or any one or more Sync Signal Reference.

16 The AV Link Plus Data References describe the transmission of non-AV data (including,
17 for example, USB data) over a multimedia channel, link, or cable for transmission of AV data. The
18 AV Link Plus Data References include at least the following:

- 19 • Zhu 537
- 20 • Park
- 21 • Lyle
- 22 • Kim 030
- 23 • Kim 417
- 24 • Lida 327
- 25 • Lida 337
- 26 • Kobayashi
- 27 • Yoshida
- 28 • Nakajima

- 1 • Butcher
- 2 • Amchislavsky
- 3 • Jol
- 4 • Stanek

5 Several AV link technologies were known at the time of the '103 patent. For example, at least the
6 following AV Protocols were known at the time:

- 7 • DisplayPort (including, for example, DisplayPort 1.2)
- 8 • Digital Video Interface (DVI) (including, for example, DVI 1.0)
- 9 • High-Definition Multimedia Intervace (HDMI) (including, for example, HDMI 1.3a)
- 10 • Mobile High-Definition Link (MHL) (including, for example, MHL Versions 1.0,
11 2.0, and 3.0)
- 12 • Whitby-Strevens

13 The '103 Patent describes adding bidirectional USB data transmission over an MHL
14 multimedia link (although the claims may not be limited to the MHL specification, specifically).
15 Prior to the '103 Patent, several references described adding the capability for bidirectional USB
16 data transmission over a multimedia channel of an AV link in other known protocols at the time.
17 For example, as discussed above, Zhu 537 and Park described bidirectional USB data transmission
18 over the DisplayPort 1.2 main link. Lyle described bidirectional transmission of auxiliary data
19 including, for example, USB data over a “video data transmission channel” in a DVI AV link. Kim
20 030 described bidirectional USB data transmission over a modified HDMI cable. Lida 327, Lida
21 337, Kim 417, and Kobayashi all disclose bidirectional data transmission (including, for example,
22 USB data) over generic multimedia AV links.

23 A POSITA would have been motivated and found it obvious to combine any one or more
24 AV Link Plus Data References with at least any one or more references describing the AV Protocol
25 explicitly referenced in such AV Link Plus Data Reference (and any related AV Protocol, such as
26 an earlier or later version from the same protocol family). In addition to the motivations discussed
27 above, such motivation would come from the teachings of the AV Link Plus Data Reference itself.

28

1 For example, a POSITA would have been motivated and found it obvious to make any of the
2 following exemplary combinations:

- 3 • Zhu 537 combined with DisplayPort 1.2 (or DisplayPort System)
- 4 • Zhu 537 combined with Whitby-Strevens
- 5 • Park combined with DisplayPort 1.2 (or DisplayPort System)
- 6 • Park combined with Whitby-Strevens
- 7 • Lyle combined with DVI 1.0
- 8 • Kim 030 combined with HDMI 1.3a
- 9 • Yoshida combined with HDMI 1.3a
- 10 • Nakajima combined with HDMI 1.3a
- 11 • Butcher combined with HDMI 1.3a
- 12 • Amchislavsky with MHL
- 13 • Jol with HDMI 1.3a
- 14 • Jol with DisplayPort 1.2 (or DisplayPort System)
- 15 • Stanek with HDMI 1.3a
- 16 • Stanek with DVI 1.0

17 Moreover, a POSITA would have been motivated and found it obvious to combine any one
18 or more AV Link Plus Data References with any AV Protocol. Both the '103 Patent and the prior
19 art teach that the principles relevant to the alleged invention of the '103 Patent can be applied across
20 different AV Protocols. *See, e.g.*, '103 Patent at 3:53-59 (“[T]he same principle can be applied to
21 other standards such as High-Definition Multimedia Interface (HDMI) standard, a Digital Visual
22 Interface (DVI) standard, and a DisplayPort standard.”); Zhu 537 at 20:58 – 21:5 (“Media connector
23 124 may be compatible with other media or multimedia standards besides DisplayPort such as but
24 not limited to a Digital Video Interactive (DVI) or a high definition multimedia interface (HDMI)
25 standard.”); Lida 327 at 7:38-44 (discussing DVI, HDMI, DisplayPort, and DIVA standards); Lida
26 337 at 3:1-4 (discussing HDMI, DVI, UDI, and DisplayPort); and Butcher at [0029] (discussing
27 HDMI, DisplayPort, and SCSI). For example, a POSITA would have been motivated and found it
28 obvious to make any of the following combinations:

- 1 • Zhu 537 combined with DVI 1.0 or HDMI 1.3a
2 • Park combined with DVI 1.0 or HDMI 1.3a
3 • Lyle combined with DisplayPort 1.2 (or DisplayPort System and/or Whitby-
4 Strevers) or HDMI 1.3a
5 • Kim 030 combined with DisplayPort 1.2 (or DisplayPort System and/or Whitby-
6 Strevers) or DVI 1.0
7 • Yoshida combined with DisplayPort 1.2 (or DisplayPort System and/or Whitby-
8 Strevers) or DVI 1.0
9 • Any of Lyle 327, Lyle 337, Kim 417, Nakajima, Butcher, and/or Kobayashi
10 combined with any of DVI 1.0, HDMI 1.3a, DisplayPort 1.2, Whitby-Strevers,
11 and/or DisplayPort System
12 A POSITA would also have been motivated and found it obvious to combine any one or
13 more AV Link Plus Data References with any AV Protocol, alone or in combination with any one
14 or more AV Protocol, with one or more references teaching synchronization signals (“Sync Signal
15 References”). As evident from the teachings of the Sync Signal References themselves, the use of
16 synchronization signals was a well-known feature in data communication generally (and in the
17 communication of USB data and AV data, specifically). A POSITA would therefore understand the
18 benefits and uses of synchronization signals as described in the Sync Signal References. The Sync
19 Signal References include at least the following references, which describe the transmission of one
20 or more synchronization signals over an AV and/or non-AV data link, as well as any reference the
21 claim chart for which cites disclosure from the reference in connection with, for example, claims 2,
22 3, 12, 13, and/or 17 of the ’103 patent:
23 • ’798 Patent
24 • Each of the AV Protocols (including, for example, DisplayPort 1.2, HDMI 1.3a, DVI
25 1.0)
26 • USB 2.0
27 • Kobayashi
28 • Hwang

- 1 • Munich
- 2 • Kim 417
- 3 • Franaszek
- 4 • Zhu 537
- 5 • Lyle
- 6 • Park
- 7 • Kim 030
- 8 • Lida 337
- 9 • Whitby-Strevens
- 10 • Wang 445
- 11 • Bradshaw
- 12 • The prior art to the '798 Patent identified in Section V.A above.

13 The AV Protocols and most (if not all) of the AV Link Plus Data References also discuss the need
14 for synchronization and the use of synchronization signals. Synchronization and synchronization
15 signals were well-known concepts in the relevant art of data communication going back at least 30+
16 years before the filing of the '103 patent. *See, e.g.,* Franaszek. Indeed, the predecessor to the original
17 assignee of the '103 patent, Silicon Image, described such synchronization signals in at least the
18 prior art '798 patent. A POSITA would therefore have been motivated to combine any AV Link
19 Plus Data Reference or any combination of one or more AV Link Plus Data References with one or
20 more AV Protocols (including the exemplary combinations listed above) with any one or more Sync
21 Signal References.

22 A POSITA would have been further motivated to combine any reference discussing any AV
23 Protocol with any reference discussing any other AV Protocol. Both the '103 Patent and the prior
24 art teach that the principles relevant to the alleged invention of the '103 Patent can be applied across
25 AV Protocols. *See, e.g.,* '103 Patent at 3:53-59 (“[T]he same principle can be applied to other
26 standards such as High-Definition Multimedia Interface (HDMI) standard, a Digital Visual Interface
27 (DVI) standard, and a DisplayPort standard.”); Zhu 537 at 20:58 – 21:5 (“Media connector 124 may
28 be compatible with other media or multimedia standards besides DisplayPort such as but not limited

1 to a Digital Video Interactive (DVI) or a high definition multimedia interface (HDMI) standard.”);
2 Lida 327 at 7:38-44 (discussing DVI, HDMI, DisplayPort, and DIVA standards); Lida 337 at 3:1-4
3 (discussing HDMI, DVI, UDI, and DisplayPort); and Butcher at [0029] (discussing HDMI,
4 DisplayPort, and SCSI). Thus, a POSITA would have found it obvious to, and been motivated to,
5 apply teachings regarding the communication of AV data, other data, and control signals in a
6 reference discussing one AV Protocol to any reference discussing any other AV Protocol.

7 For at least those same reasons, a POSITA would have been motivated to modify any
8 reference teaching a multimedia link, including but not limited to any AV Protocol or any patent or
9 publication related thereto, to include the capability for bidirectional communication of USB data
10 on a physical channel, link, or cable used for transmission of AV data, as taught in at least AV Link
11 Plus Data References, including by providing for a (or modifying a preexisting) transmitter,
12 receiver, and/or transceiver on the AV data channel capable of transmitting and receiving USB data.

13 A POSITA would also have been motivated to combine any reference or combination of
14 references relating to DisplayPort (or another non-TMDS video communication protocol) with an
15 adapter that converts between DisplayPort and a TMDS protocol. Such adapters are taught, for
16 example, in Wu 905 and TI SN75DP129. Motivation for such a combination can be found, for
17 example, in the teachings of Wu 905, which discusses the value of and need for such adapters. See
18 Wu 905 at 1:32 – 2:13.

19 Thus, in addition to the combinations discussed above, exemplary combinations which
20 render obvious some or all of the Asserted Claims of the ’905 Patent are listed in **Appendix A**, Sec.
21 VIII.

22 **B. Invalidity of the ’103 Patent Based on 35 U.S.C. § 112(a)**

23 Based on Defendant’s present understanding of Plaintiff’s asserted scope of the claims of
24 the ’103 Patent, to the extent such positions can be understood from Plaintiff’s Infringement
25 Contentions, Defendant asserts that one or more of the ’103 Asserted Claims are invalid for failure
26 to provide a written description that enables the full scope of the ’103 Asserted Claims based on at
27 least the following claim terms, phrases, or limitations:

- 1 • **“aligning a boundary of a symbol in a first forward unit of data of the forward units of**
2 **data using the first synchronization signal” (claim 17):** The specification does not provide
3 sufficient written description and/or fully enable the recited “aligning a boundary of a
4 symbol” limitation. For example, to the extent UCT asserts that a PDF field in packet is a
5 boundary symbol, the specification lacks sufficient written description support and/or
6 enabling disclosure for aligning such a symbol using the first synchronization signal.
- 7 • **“coupled to a . . . physical channel” (claim 22):** The specification does not provide
8 sufficient written description and/or fully enable the recited “coupled to a . . . physical
9 channel” limitation. For example, to the extent UCT asserts that components coupled
10 together over a digital circuit design are within the scope of this claim, the specification lacks
11 sufficient written description support and/or enabling disclosure for coupling components in
12 a digital circuit design.

13 Based on Defendant’s present understanding of Plaintiff’s Infringement Contentions and
14 apparent interpretation of the scope of the Asserted Claims, at least one or more of these claim terms,
15 phrases, and limitations are not described in the specification of the Asserted Patent and do not
16 enable a person of ordinary skill in the art to practice the claimed invention without undue
17 experimentation or to distinguish all operative embodiments from all nonoperative embodiments
18 without undue experimentation.

19 In addition to Defendant’s contentions regarding the specifically listed terms above,
20 Defendant contends that UCT has failed to identify specific support for each limitation of each
21 Asserted Patent in its Infringement Contentions, and instead points to the same or similar
22 information as satisfying each claim limitation. Defendant therefore contends that there is no written
23 description support for the identified, described, or explained in the specification of the Asserted
24 Patents to enable a person of ordinary skill in the art to practice the claimed invention under the
25 wide claim scope UCT appears to be contending applies.

26 The written description and enablement issues identified above apply to all claims that
27 include the identified limitations, either explicitly or through claim dependency, and are not limited
28 to the exemplary claims listed above.

1 **C. Invalidity of the '103 Patent Based on 35 U.S.C. § 112(b)**

2 Based on Defendant's present understanding of Plaintiff's asserted scope of the '103
3 Asserted Claims, to the extent such positions can be understood from Plaintiff's Infringement
4 Contentions, Defendant asserts that one or more of the '103 Asserted Claims are invalid for reciting
5 at least the following claim terms, phrases, or limitations:

- 6 • **"The method of claim 11, further comprising aligning a boundary of a symbol**
7 **in a first forward unit of data of the forward units of data using the first**
8 **synchronization signal" (claim 17):** The specification does not explicitly define "a
9 boundary of a symbol" or sufficiently inform a person of ordinary skill as to its
10 meaning in the context of claim 17. As such, claim 17 is indefinite.
11 • **"coupled to a . . . physical channel" (claim 22):** The specification does not
12 sufficiently disclose to a person of ordinary skill in the art how to couple a transmitter
13 or receiver to the physical channel to perform the claimed method in a digital circuit
14 design. Rather, the specification consistently discloses physically coupling the
15 transmitter and receiver to a physical interconnect. '103 Patent at 9:32-36.

16 These claim terms, phrases, limitations, and all dependent claims thereof, as apparently
17 construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112 at least because they
18 fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

19 Based on Defendant's present understanding of Plaintiff's Infringement Contentions, at least
20 one or more of these claim terms, phrases, and limitations are indefinite because they are
21 inconsistent with and broader than the alleged invention disclosed in the specification and during
22 prosecution, and given Plaintiff's apparent constructions of the claims, a person of ordinary skill in
23 the art at the time of the invention would not understand what is claimed with reasonable certainty,
24 even when the claims are read in light of the specification and prosecution history.

25 Additionally, Claims 21 and 22 of the '103 Patent are invalid under 35 U.S.C. §§ 112(b) and
26 (f) because the '103 Patent does not disclose sufficient structure corresponding to the function
27 recited in at least the following means-plus-function claim limitations:

- 1 • “a transmitter coupled to a first physical channel of the multimedia link and configured to
2 send forward units of data from the source device to the sink device over the first physical
3 channel during one or more first time periods, the forward units of data comprising video
4 data and forward data compliant with a first standard comprising a universal serial bus (USB)
5 standard and different from a standard of the video data” (claims 21 and 22)
- 6 • “a receiver coupled to the first physical channel and configured to receive backward units of
7 data at the source device from the sink device over the first physical channel during one or
8 more second time periods, the backward units of data comprising backward data compliant
9 with the first standard” (claims 21 and 22)
- 10 • “a control signal transceiver coupled to a second physical channel of the multimedia link
11 distinct from the first physical channel and configured to at least send control data from the
12 source device to the sink device over the second physical channel” (claims 21 and 22)

13 The indefiniteness issues identified above apply to all claims that include the identified
14 limitations, either explicitly or through claim dependency, and are not limited to the exemplary
15 claims listed above.

16 **XI. UNENFORCEABILITY**

17 Defendant reserves the right to assert, after obtaining discovery from the inventors and
18 prosecuting attorneys, that the remaining Asserted Patents are unenforceable due to inequitable
19 conduct at least on the grounds that material prior art, including but not limited to any of the
20 references identified herein, were known to the applicants or their attorney(s), material and withheld
21 with an intent to deceive the Patent Office. For example, at least the '103 Patent is unenforceable
22 for the reasons stated in Defendant's Answer. Dkt. 37, pp. 19-22.

23 Defendant also hereby incorporates by reference any allegation of unenforceability raised
24 by any other Defendant in any Answer or Counterclaim filed in any case involving an Asserted
25 Patent.

1 **XII. SUBJECT-MATTER ELIGIBILITY CONTENTIONS**

2 Pursuant to the Court’s Standing Order Regarding Subject Matter Eligibility Contentions,
3 Defendant hereby provides the bases for its contention that all Asserted Claims are patent ineligible
4 and therefore invalid under 35 U.S.C. § 101.

5 Section 101 “defines the subject matter that may be patented under the Patent Act.” *Bilski v.*
6 *Kappos*, 561 U.S. 593, 601 (2010). Under § 101, the scope of patentable subject matter encompasses
7 “any new and useful process, machine, manufacture, or composition of matter, or any new and
8 useful improvement thereof.” *Id.* (quoting 35 U.S.C. § 101). These categories are not limitless, as §
9 101 contains three important exceptions—abstract ideas, laws of nature, and natural phenomena are
10 not patentable. *Alice Corp. Pty. Ltd. v. CLS Bank Int’l*, 573 U.S. 208, 134 S. Ct. 2347, 2354 (2014).
11 The determination of whether a claim recites patent-eligible subject matter under § 101 is guided by
12 the two-step analytical framework set forth in *Alice*, *id.* at 2355. The first step requires determining
13 whether the claims are directed to one of these three exceptions. *Id.* If so, the second step requires
14 determining whether the claim elements, considered individually and as an ordered combination,
15 “amount to significantly more” than the patent-ineligible concept. *Id.*

16 The first step is to examine the fundamental concept, or the “focus” of the claim and
17 determine whether the claim as a whole is directed to an abstract idea, law of nature, and natural
18 phenomenon. *See Internet Patents Corp. v. Active Network, Inc.*, 790 F.3d 1343, 1346 (Fed. Cir.
19 2015) (“Under step one of Mayo/Alice, the claims are considered in their entirety to ascertain
20 whether their character as a whole is directed to excluded subject matter.”). While courts should be
21 careful not to oversimplify the claims at this stage of the analysis, the analysis should not focus on
22 excess verbiage or implementation details, but instead focus on the “concept embodied by the
23 majority of the limitations.” *Ultramercial, Inc. v. Hulu, LLC*, 772 F.3d 709, 715 (Fed. Cir. 2014);
24 *see also Affinity Labs of Texas, LLC v. DirecTV, LLC*, 838 F.3d 1253, 1256 (Fed. Cir. 2016)
25 (examining claim after being “stripped of excess verbiage”). Transformation into a patent-eligible
26 claim requires “more than simply ... adding the words ‘apply it.’” *Id.* (quoting *Mayo Collaborative*
27 *Servs. v. Prometheus Labs., Inc.*, 132 S. Ct. 1289, 1294 (2012)). Also, a claim is not meaningfully
28 limited if it includes only token or insignificant pre- or post-solution activity—such as merely

1 identifying a technological environment. *Mayo*, 132 S. Ct. at 1297–98, 1300–01. Finally, “simply
2 appending conventional steps, specified at a high level of generality,” to abstract ideas cannot make
3 those ideas patentable. *Mayo*, 132 S. Ct. at 1300; *see also Fort Props., Inc. v. Am. Master Lease*
4 *LLC*, 671 F.3d 1317, 1323 (Fed. Cir. 2012) (“Such a broad and general limitation does not impose
5 meaningful limits on the claim’s scope.”).

6 With respect to abstract ideas, the Federal Circuit has clarified that a relevant inquiry at step
7 one is to “ask whether the claims are directed to a specific improvement in the capabilities of
8 computing devices, or, instead, ‘a process that qualifies as an ‘abstract idea’ for which computers
9 are invoked merely as a tool.’” *Core Wireless Licensing S.A.R.L. v. LG Elecs., Inc.*, 880 F.3d 1356,
10 1361-62 (Fed. Cir. 2018) (quoting *Enfish, LLC*, 822 F.3d at 1336). In *Core Wireless Licensing*, the
11 Federal Circuit noted that in *Enfish*, “unlike claims that merely ‘add[] conventional computer
12 components to well-known business practices,’ the claimed self-referential table was ‘a specific type
13 of data structure designed to improve the way a computer stores and retrieves data in memory.’” *Id.*
14 (quoting *Enfish*, 822 F.3d at 1338–39) (underlining added). The Federal Circuit further emphasized
15 that claims directed to the improvement in the functioning of a computer must teach a specific and
16 new method that enables a computer “to do things it could not do before.” *Id.* For example, in *Finjan,*
17 *Inc. v. Blue Coat Systems, Inc.*, the Federal Circuit “held claims directed to a behavior-based virus
18 scanning method directed to patent eligible subject matter because they ‘employ[] a new kind of
19 file that enables a computer security system to do things it could not do before, ...’” *Id.* (citing *Finjan,*
20 *Inc. v. Blue Coat Sys., Inc.*, 879 F.3d 1299 (Fed. Cir. 2018)).

21 With respect to laws of nature and natural phenomenon, the Federal Circuit has held that
22 claims focused on detecting natural laws or phenomenon—even if new and useful—are patent-
23 ineligible. *See, e.g., Cleveland Clinic Found. v. True Health Diagnostics LLC*, 859 F.3d 1352, 1363
24 (Fed. Cir. 2017); *Ariosa Diagnostics, Inc. v. Sequenom, Inc.*, 788 F.3d 1371, 1378 (Fed. Cir. 2015).
25 For instance, in *Cleveland Clinic*, the claims recited a particular assay used to detect the protein
26 MPO. 859 F.3d at 1357-58. In *Ariosa*, the claims recited a technique to amplify and detect DNA.
27 788 F.3d at 1377. The Federal Circuit emphasized that “the claims at issue, as informed by the
28 specification, are generally directed to detecting the presence of a naturally occurring thing or a

1 natural phenomenon” and amounted to nothing “more than simply stat[ing] the law of nature while
2 adding the words ‘apply it.’” *Id.* at 1376-77 (internal citations omitted).

3 The Asserted Patents are not patent eligible under § 101.

4 **’905 Patent.** The Asserted Claims of the ’905 Patent are invalid under 35 U.S.C. § 101
5 because they are directed to ineligible subject matter. *See* Ex. A-7. In particular, under *Alice* Step
6 1, the ’905 Asserted Claims recite nothing more than the abstract idea of transmitting
7 and/orreceiving packets. Specifically, the claims generically recite a technique for “transmitting
8 packets,” or “receiving packets” such as the claimed “first packet” and “second packet;” transmitting
9 or receiving indicators associated with the packets, such as the “preempt indicator” and the
10 “continue indicator;” and using in-band symbols and out-of-band symbols. Such receiving and
11 transmitting fail *Alice* Step 1. *See, e.g., Prism Techs. LLC v. T-Mobile USA, Inc.*, 696 F. App’x 1014,
12 1017 (Fed. Cir. 2017) (generally finding claims to, *inter alia*, coordinating communication between
13 transmitters to “provide restricted access” as ineligible under Section 101).

14 The ’905 Asserted Claims further fail *Alice* Step 2 because they do not contain any inventive
15 concept that would transform the abstract idea into a patent-eligible invention. Rather, the claims
16 recite purely function limitations with no structural elements at all (*e.g.*, claims 1, 8, and 15) or recite
17 generic “components” combined in conventional ways to perform generic functions (*e.g.*, claim 21
18 reciting a “transmission component” for “transmitting the first packet”). *See Ultramercial, Inc. v.*
19 *Hulu, LLC*, 772 F.3d 709, 715-16 (Fed. Cir. 2014). Implementing an abstract idea using functional
20 limitations or generic computer components does not constitute a patentable improvement in
21 computer technology. *See Two-Way Media Ltd. v. Comcast Cable Commc’ns, LLC*, 874 F.3d 1329,
22 1337 (Fed. Cir. 2017). Further, the inclusion of well-known “in-band” or “out-of-band” symbols
23 fails to produce “a result that overrides the routine and conventional” use of this known
24 feature. *DDR Holdings, LLC v. Hotels.com, L.P.*, 773 F.3d 1245, 1258 (Fed. Cir. 2014). Instead, the
25 use of “in-band” and “out-of-band” symbols is a conventional, well-known process for transmitting
26 data, as shown by the accompanying prior art. Accordingly, the ’905 Asserted Claims fail *Alice* Step
27 2 because they do not contain any inventive concept that would transform the abstract idea into
28 patent-eligible subject matter.

1 **'712 Patent.** The Asserted Claims of the '712 Patent are invalid under 35 U.S.C. § 101
2 because they are directed to ineligible subject matter. In particular, under *Alice* Step 1, the '712
3 Asserted Claims recite nothing more than the abstract idea of delivering power to a device
4 communicating that it is in need of power. Specifically, claim 1 recites a power delivery circuit for
5 delivering power to a device, the circuit including a voltage source, a switch to convey voltage from
6 the voltage source when closed, a signature resistor for detection, and a load detector for extracting
7 information based on a device's current, where the information includes whether the device is on,
8 and whether it needs power. Independent claim 7 is even broader and claims a method of delivering
9 power to a device, the method including detecting a load in the device, extracting information based
10 on the load current, and relaying power based on that information, where the information includes
11 whether the device is on, and whether it needs power. Such claims are plainly directed to an abstract
12 idea and fail *Alice* step 1. *See, e.g., ChargePoint, Inc. v. SemaConnect, Inc.*, 920 F.3d 759, 770 (Fed.
13 Cir. 2019) (finding ineligible under § 101 claims directed to (a) an apparatus for charging an electric
14 vehicle that receives communications from a remote server and adjusts charging based on those
15 communications; and (b) a “network-controlled charge transfer system for electric vehicles”
16 comprising a combination of generic components, including a charge transfer device, an electrical
17 receptacle, a control device for switching the receptacle on and off, a current measuring device for
18 measuring current through the receptacle, and a controller for monitoring output of the current
19 measuring device and controlling the control device).

20 The '712 Asserted Claims also fail *Alice* step 2 because they do not contain an inventive
21 concept that would transform the abstract idea into a patent-eligible application. Instead, the claims
22 either recite routine functional limitations with no structural elements (i.e., claims 7 and 9), or recite
23 generic components combined in conventional ways (e.g., claim 1 reciting a voltage source, a power
24 relay switch, a resistor, and a load detector). *Alice*, 573 U.S. at 223 (“the mere recitation of a generic
25 computer cannot transform a patent-ineligible abstract idea into a patent-eligible invention”);
26 *WhitServe LLC v. Dropbox, Inc.*, 854 F. App'x 367, 372 (Fed. Cir. 2021) (finding claims reciting
27 “generic computer components performing routine conventional functions” such as “sending and
28 receiving information” not eligible under § 101). As the prior art cited and discussed in these

1 contentions and the attached claim charts demonstrates, the concepts and components recited in the
2 '712 Asserted Claims were all routine, conventional, and well-known at the time of invention. For
3 example, the use of a current sensor and a signature resistor to determine a connected device's power
4 requirements was well known in the art and widely used in PoE devices. Thus, at most, the '712
5 Asserted Claims merely recite an "abstract-idea-based solution implemented with generic technical
6 components in a conventional way." *ChargePoint*, 920 F.3d at 775. Accordingly, the '712 Asserted
7 Claims are invalid under § 101.

8 **'103 Patent.** The '103 Asserted Claims are directed to ineligible subject matter under 35
9 U.S.C. § 101. In particular, under *Alice* Step 1, the '103 Asserted Claims are directed to the abstract
10 idea of transmitting and receiving two different types of data on one physical channel and control
11 signals on a separate physical channel. *See, e.g., Hawk Tech. Sys., LLC v. Castle Retail, LLC*, 60
12 F.4th 1349 (Fed. Cir. 2023) (finding claims to receiving, transmitting, processing, storing, and
13 displaying image data ineligible under Section 101). The patent ineligible nature of the '103
14 Asserted Claims is even more evident under the extremely broad construction applied by UCT in
15 its infringement contentions. UCT reads the '103 Asserted Claims onto an implementation of
16 DisplayPort tunneling over USB4. Such a read necessarily assumes broad constructions. For
17 example, UCT interprets its claims so that they are not limited specifically to an audio/visual
18 "multimedia link," but would apply also to a USB link and that they do not require a single bi-
19 directional, half-duplex first physical channel with time-division multiplexing or TMDS coding.
20 The omission of these potential limitations exacerbates the fundamentally abstract nature of the '103
21 Asserted Claims.

22 The other elements of the claim do not contain any inventive concept that would transform
23 the abstract idea into a patent-eligible invention under *Alice* Step 2. For example, as demonstrated
24 in the contentions and claim charts for the '103 Patent, the limitations requiring a "multimedia link,"
25 "forward data compliant with . . . a universal serial bus (USB) standard," "video data" corresponding
26 to "a standard of the video data," the first and second "synchronization signals," and the recited
27 generic hardware (see below) are all conventional and, at most, attempt to limit the abstract idea to
28 a particular technological environment, which is insufficient to convert the abstract idea into an

1 inventive concept. *Alice Corp. v. CLS Bank Int'l*, 134 S.Ct. 2347, 2358 (2014). Further, the
2 limitations “forward data compliant with . . . a universal serial bus (USB) standard” and “video data”
3 corresponding to “a standard of the video data” recite printed matter, which is not patent-eligible
4 subject matter and thus cannot transform the abstract concept into an eligible invention. Moreover,
5 the recited hardware structures (including, for example, “source device,” “sink device,” “multimedia
6 link,” “physical channel,” “transmitter,” “receiver,” and “transceiver”) are all generic and
7 functional. As the prior art cited and discussed in these contentions and the attached claim charts
8 demonstrates, these concepts were all routine, conventional, and well-known at the time of
9 invention.

10 When these conventional elements are assembled together in the Asserted Claims, they do
11 not take on any transformative property that, considered as a whole, reflects an inventive concept.
12 Instead, the conventional elements of the claim are used in an entirely conventional manner. For
13 instance, the claims combine known data types (such as A/V data, USB data, and control signals)
14 and conventional data communication components (such as receivers, transmitters, transceivers,
15 physical channels) and concepts (such as synchronization signals and time-division multiplexing for
16 half-duplex communication) in predictable and conventional ways using known techniques. These
17 components are also used for their conventional purposes—i.e., transmitting and receiving data
18 between devices. These elements were well known in the art, and the Asserted Patents do no more
19 than use the appropriate technique for their conventionally intended purpose.

20 Moreover, the prior art cited throughout Defendant’s Invalidity Contentions (including the
21 claim charts attached as Exhibits hereto), as well as the patents themselves and the prior art cited or
22 admitted to therein, demonstrate that the claim elements are directed to well-understood, routine,
23 and conventional techniques and components. Accordingly, the ’103 Asserted Claims are invalid
24 under § 101.

25 Additionally, at least claim 22 of the ’103 Patent is directed to ineligible subject matter under
26 Section 101 for the additional reason that it is directed to the abstract idea of a “digital design of a
27 circuit.” ’103 Patent at claim 22 (preamble). The claim limitations thus recite printed matter – that
28 is, the informational content of the “instructions” that make up the “digital design.” Such limitations

are not patentable subject matter and instead are more properly the subject of other intellectual property protections such as copyright.

These Invalidity Contentions address only those claims that Plaintiff has asserted in its Infringement Contentions against Defendant. Defendant incorporates by reference any and all other subject matter eligibility contentions that have or will be served in this case or any other case brought by Plaintiff and/or involving the Asserted Patents. Defendant incorporates by reference any and all other bases for invalidity identified during prosecution, reexamination, or any other proceeding before the United States Patent and Trademark Office regarding the Asserted Patents, or any other patents in the same family as any Asserted Patent.

XIII. DOCUMENT PRODUCTION

Pursuant to Patent Local Rule 3-4, Defendant is producing with these contentions:

	Document Type	Bates
(a)	Source code, specifications, schematics, flow charts, artwork, formulas, or other documentation sufficient to show the operation of any aspects or elements of an Accused Instrumentality identified by the patent claimant in its Patent L.R. 3-1(c) chart;	HP_00000827; HP_00000828; HP_00032102; HP_00032091; HP_00032103; HP_00032152; HP_00032474; HP_00032580; HP_00032738; HP_00032473; HP_00032784; HP_00032632; HP_00032104; HP_00032153; HP_00032151; HP_00032105; HP_00032116; HP_00032122; HP_00032150; HP_00033199;
(b)	A copy or sample of the prior art identified pursuant to Patent L.R. 3-3(a) which does not appear in the file history of the patent(s) at issue. To the extent any such item is not in English, an English translation of the portion(s) relied upon shall be produced;	HP_00001650; HP_00031957; HP_00011104; HP_00018629; HP_00023544; HP_00006195; HP_00002504; HP_00029633; HP_00006773; HP_00023194; HP_00025298; HP_00024912; HP_00005846; HP_00024779; HP_00024937; HP_00003855; HP_00018816; HP_00003675; HP_00022520; HP_00022680; HP_00018951; HP_00018715; HP_00017761; HP_00006175; HP_00003751; HP_00023827; HP_00025400; HP_00005554; HP_00027025; HP_00021612; HP_00023683; HP_00024832; HP_00024272; HP_00018611; HP_00024565; HP_00014757; HP_00022963; HP_00018582; HP_00006191; HP_00022267; HP_00019267; HP_00024371; HP_00027013; HP_00002594; HP_00031636; HP_00006183; HP_00008422; HP_00018558; HP_00001256; HP_00018805; HP_00023898; HP_00024668; HP_00000829; HP_00024225; HP_00018742; HP_00031541; HP_00005927; HP_00030443; HP_00010756; HP_00024329;

1		HP_00018663; HP_00009392; HP_00029357;
2		HP_00031685; HP_00031821; HP_00025125;
3		HP_00014070; HP_00021650; HP_00024097;
4		HP_00010918; HP_00022013; HP_00009380;
5		HP_00023559; HP_00023762; HP_00024169;
6		HP_00022818; HP_00001789; HP_00030478;
7		HP_00022233; HP_00001711; HP_00021772;
8		HP_00030990; HP_00025482; HP_00025346;
9		HP_00024304; HP_00003840; HP_00031738;
10		HP_00022859; HP_00025375; HP_00023927;
11		HP_00018795; HP_00022429; HP_00024559;
12		HP_00022004; HP_00024255; HP_00001348;
13		HP_00017574; HP_00016957; HP_00021600;
14		HP_00019177; HP_00008481; HP_00022377;
15		HP_00029979; HP_00001656; HP_00031561;
16		HP_00024310; HP_00024684; HP_00006223;
17		HP_00024116; HP_00019263; HP_00031895;
18		HP_00000831; HP_00024058; HP_00031760;
19		HP_00024432; HP_00027018; HP_00021488;
20		HP_00030683; HP_00011942; HP_00024752;
21		HP_00011114; HP_00014716; HP_00011122;
22		HP_00020990; HP_00001719; HP_00029066;
23		HP_00018477; HP_00027691; HP_00006238;
24		HP_00006796; HP_00009789; HP_00031614;
25		HP_00031576; HP_00024279; HP_00030618;
26		HP_00022606; HP_00018936; HP_00022103;
27		HP_00021589; HP_00010813; HP_00021380;
28		HP_00024499; HP_00028903; HP_00022878;
		HP_00017609; HP_00022054; HP_00023240;
		HP_00010669; HP_00012036; HP_00018571;
		HP_00018962; HP_00012343; HP_00009135;
		HP_00031301; HP_00025286; HP_00021869;
		HP_00011090; HP_00012808; HP_00030429;
		HP_00031969; HP_00021785; HP_00029134;
		HP_00027037; HP_00023909; HP_00011976;
		HP_00009837; HP_00024044; HP_00029176;
		HP_00006849; HP_00002742; HP_00018499;
		HP_00012742; HP_00010498; HP_00005888;
		HP_00001698; HP_00018899; HP_00031303;
		HP_00022915; HP_00001713; HP_00012001;
		HP_00022139; HP_00022954; HP_00001758;
		HP_00002936; HP_00030532; HP_00026859;
		HP_00022748; HP_00022666; HP_00022501;
		HP_00021312; HP_00022393; HP_00018781;
		HP_00031603; HP_00025538; HP_00018344;
		HP_00029762; HP_00029752; HP_00018831;
		HP_00019306; HP_00018750; HP_00002608;
		HP_00006207; HP_00022461; HP_00024712;

1		HP_00022044; HP_00011950; HP_00031595;
2		HP_00028882; HP_00021316; HP_00021930;
3		HP_00029330; HP_00010658; HP_00012067;
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10		HP_00014470; HP_00014511; HP_00014549;
11		HP_00014570; HP_00014374; HP_00010124;
12		HP_00014176; HP_00032805; HP_00033197
13	(c)	All agreements that may be related to the accused instrumentality or may be comparable to a license that would result from a hypothetical reasonable royalty negotiation;
14		HP_00000590; HP_00000561; HP_00000518;
15		HP_00000550; HP_00000519; HP_00000535;
16		HP_00000627; HP_00000626; HP_00000726;
17		HP_00000773; HP_00000599; HP_00000758;
18		HP_00000668; HP_00000742
19	(d)	Documents sufficient to show the sales, revenue, cost, and profits for accused instrumentalities identified pursuant to Patent L.R. 3-1(b) for any period of alleged infringement; and
20		HP_00033282-286
21	(e)	All agreements that may be used to support the party denying infringement's damages case.
22		HP_00000590; HP_00000561; HP_00000518;
23		HP_00000550; HP_00000519; HP_00000535;
24		HP_00000627; HP_00000626; HP_00000726;
25		HP_00000773; HP_00000599; HP_00000758;
26		HP_00000668; HP_00000742

1 DATED: December 5, 2024

Respectfully submitted,
/s/ Lauren E. Douville
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Attorneys for Defendant HP Inc

18
19 **CERTIFICATE OF SERVICE**

20 I hereby certify that on December 5, 2024, I served a copy of the foregoing along with
21 accompanying exhibits and document production via electronic mail on all counsel of record.

22
23 /s/ Dana E. Hardy
24 On behalf of Lauren E. Douville.