

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MEDIATEK INC.,
Petitioner,

v.

DAEDALUS PRIME LLC,
Patent Owner.

IPR2024-01488
Patent 10,740,281 B2

Before WILLIAM V. SAINDON, GREGG I. ANDERSON, and
ARTHUR M. PESLAK, *Administrative Patent Judges*.

PESLAK, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

MediaTek Inc. (“Petitioner”) filed a Petition pursuant to 35 U.S.C. §§ 311–319 requesting an *inter partes* review of claims 1–21 (“the challenged claims”) of U.S. Patent No. 10,740,281 B2 (“the ’281 patent,” Ex. 1001). Paper 1. Petitioner filed a Declaration of Murali Annavaram Ph.D. in support of the Petition. Ex. 1022.

Daedalus Prime LLC (“Patent Owner”) waived the filing of a Preliminary Response. Paper 6.

We have authority, acting on the designation of the Director, to determine whether to institute an *inter partes* review under 35 U.S.C. § 314(a). *See* 37 C.F.R § 42.4(a) (2023) (“The Board institutes the trial on behalf of the Director.”). Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless the information presented in the Petition shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

Considering the Petition as well as all supporting evidence, we conclude that the information presented in the Petition establishes a reasonable likelihood that Petitioner would prevail in its challenge of at least one claim of the ’281 patent as unpatentable. Pursuant to 35 U.S.C. § 314, we hereby institute an *inter partes* review of all challenged claims of the ’281 patent on all grounds stated in the Petition.

Our factual findings, claim construction, and legal conclusions at this stage of the proceeding are based on the evidentiary record developed thus far. This decision to institute trial is not a final decision as to the unpatentability of the claims for which *inter partes* review is instituted. Our final decision will be based on the full record developed during trial.

A. Related Matters

The parties identify *Daedalus Prime LLC v. MediaTek Inc.*, 2:24-cv-00235 (E.D. Tex.) as a related matter. Pet. 92; Paper 3, 2. Patent Owner discloses that the '281 patent “is a continuation of U.S. Patent No. 10,049,080, which was/is at issue in the following USPTO proceedings: *Qualcomm Inc. v. Daedalus Prime LLC*, IPR2023-00567 (terminated-settled); and *Mercedes Benz USA LLC v. Daedalus Prime LLC*, IPR2023-01333.”¹ Paper 3, 2.

B. Real Parties in Interest

Petitioner identifies itself and no others as the real party-in-interest for this proceeding. Pet. 92.

Patent Owner identifies itself as a real party-in-interest. Paper 3, 2. Patent Owner also states that “Daedalus Prime LLC’s parent company is Daedalus Group LLC, and no publicly traded company owns ten percent (10%) or more of Daedalus Prime LLC’s stock.” *Id.*

C. The '281 Patent

The '281 patent is titled “Asymmetric Performance Multicore Architecture with Same Instruction Set Architecture.” Ex. 1001, code (54). The '281 patent relates to multi-core processors in computing systems and methods of managing power in multi-core processors. *Id.* at 1:23–26, 2:26–42.

According to the '281 patent, a power management component typically “scale[s] up the processing performance of the system as the system’s workload increases, and, scale[s] down the processing performance

¹ A Final Written Decision was entered in this case on January 8, 2025. IPR2023-01333, Paper 31.

of the system as the system's workload decreases.” Ex. 1001, 2:31–35. Scaling process performance with workload is usually accomplished by enabling or disabling entire cores and raising or lowering core supply voltages and operating frequencies in response to workload. *Id.* at 2:39–42. For example, “all cores are enabled and each core is provided with a maximum supply voltage and maximum clock frequency” under a maximum performance/power consumption state, and only one core is enabled under a minimum performance/power consumption state. *Id.* at 2:44–46; *see also id.* at Fig. 2.

The '281 patent explains that some “prior art multi core processor power management schemes have been implemented on processors whose constituent cores are identical,” while others have been implemented on processors in which the cores are radically different from each other (i.e., asymmetric). Ex. 1001, 3:42–45. For example, a processor with cores that are different from each other may have a low power core that lacks sizeable chunks of logic circuitry responsible for executing the program code instructions compared to the other cores in the processor and supports a reduced instruction set. *Id.* at 3:47–54. However, processors with cores that are different from each other can suffer from drawbacks because “it is difficult for system software to adjust switch operation between processor cores having different instruction sets.” *Id.* at 3:55–57.

The '281 patent purports to address this issue by disclosing multi-core processors “in which at least one of the cores [] is designed to be lower performance and therefore consume less power than other cores [] in the process[o]r.” Ex. 1001, 3:58–60. According to the '281 patent, the lower power cores have the same logic design as the higher power cores and

support the same instruction set, but consume less power “by having narrower drive transistor widths than the higher power core(s) and/or having other power consumption related design features.” *Id.* at 3:65–67.

The '281 patent explains that the lower power core allows the multi-processor “to entertain a power management strategy that is the same/similar to already existing power management strategies, yet, still achieve an even lower power consumption in the lower/lowest performance/power states.” Ex. 1001, 4:28–33; *see also id.* Fig. 5.

Figure 6 of the '281 patent is reproduced below and depicts an example of a power management method:

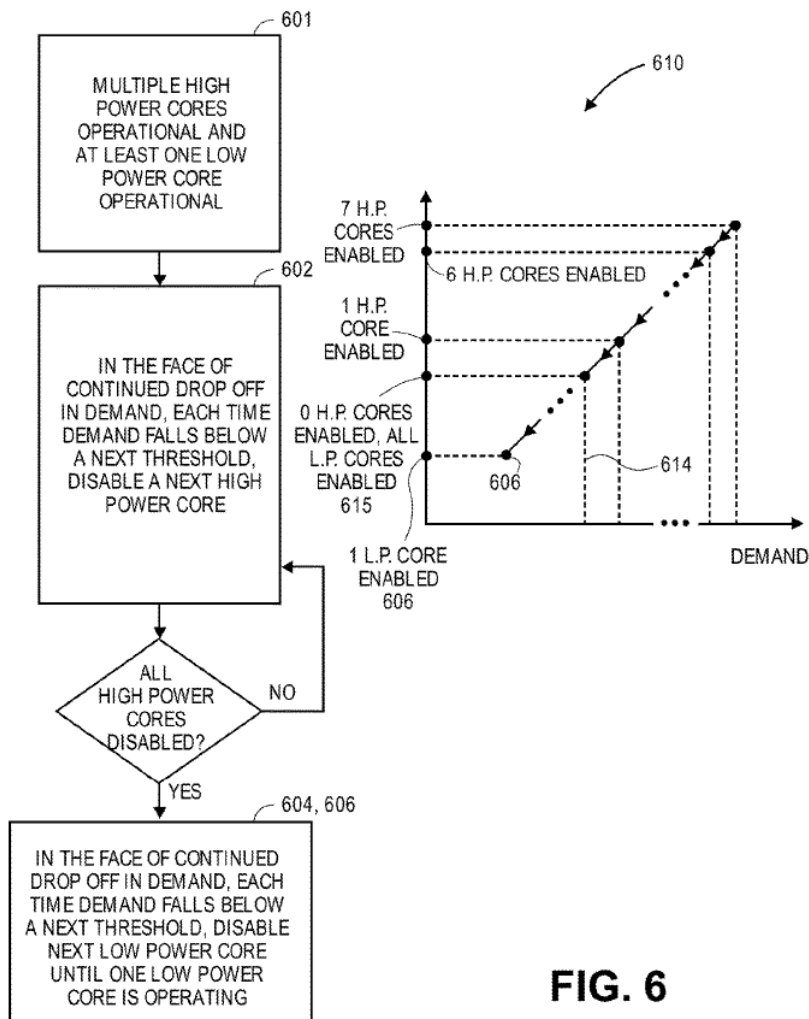


FIG. 6

Figure 6 “shows a power management process flow that can be executed, for example, with power management software that is running on the multi-processor (or another multi-processor or separate controller, etc.)” or “entirely in hardware on the multi-processor or by some combination of such hardware and software.” Ex. 1001, 4:55–61. The process begins with a multi-core processor in which multiple high-power cores and at least one low-power core are operating. *Id.* Fig. 6 (601), 4:62–65. When the demand on the processor drops below a threshold, a high-power core is disabled. *Id.* at 4:65–67. This process is repeated with the enabled high-power cores each time demand reaches a lower threshold. *Id.* at 4:62–5:14. When all of the high-power cores are disabled and the demand on the processor continues to drop, the low-power cores are disabled one by one in the same manner until only one low-power core is enabled and the lower power state is reached. *Id.* Fig. 6 (604, 606), 5:33–43.

D. Illustrative Claims

Claims 1, 8, and 15 are independent claims. Claim 1 is reproduced below:

1. A multi-core processor comprising:
 - a first plurality of cores and a second plurality of cores that support a same instruction set, wherein the first plurality of cores are higher performance and consume more power than the second plurality of cores, and each of the second plurality of cores have a maximum operating frequency that is less than a maximum operating frequency of each of the first plurality of cores;
 - a caching layer shared by the first plurality of cores and the second plurality of cores; and
 - power management hardware to enable and disable the first plurality of cores and the second plurality of cores, wherein an operating system that executes on the multi-

core processor is to monitor a demand for the multi-core processor and control a core mix of the first plurality of cores and the second plurality of cores based on the demand with the power management hardware.

Ex. 1001, 7:62–8:12.

E. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–21 would have been unpatentable on the following grounds (Pet. 1):

Claim(s) Challenged	35 U.S.C. §²	References/Basis
1, 2, 4, 6, 8, 9, 11, 13, 15, 16, 18, 20	103(a)	Sutardja, ³ Mathieson ⁴
3, 10, 17	103(a)	Sutardja, Mathieson, Patterson-1 ⁵
5, 12, 19	103(a)	Sutardja, Mathieson, Knebel ⁶
7, 14, 21	103(a)	Sutardja, Mathieson, Liu ⁷
1–4, 6, 8–11, 13, 15–18, 20	103(a)	Mathieson, Sakarda ⁸
7, 14, 21	103(a)	Mathieson, Sakarda, Liu
5, 12, 19	103(a)	Mathieson, Sakarda, and Knebel

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. Because the ’281 patent claims priority to an application filed before March 16, 2013 (the effective date of the amendments), the pre-AIA version of § 103 applies.

³ U.S. Patent Application Publication No. US 2008/0288748 A1 (filed June 30, 2008; published November 20, 2008) (Ex. 1002, “Sutardja”).

⁴ U.S. Patent Application Publication No. US 2011/0213950 A1 (filed May 25, 2010; published September 1, 2011) (Ex. 1003, “Mathieson”).

⁵ David A. Patterson & John L. Hennessy, *Memory-Hierarchy Design*, in *COMPUTER ARCHITECTURE A QUANTITATIVE APPROACH* 372–483 (2d ed., 1996) (Ex. 1004, “Patterson-1”).

⁶ U.S. Patent Application Publication No. US 2009/0106494 A1 (filed October 19, 2007; published April 23, 2009) (Ex. 1005, “Knebel”).

⁷ U.S. Patent Application Publication No. US 2006/0053258 A1 (filed September 8, 2004; published March 9, 2006) (Ex. 1006, “Liu”).

⁸ U.S. Patent No. US 9,442,758 B1 (filed January 21, 2009; issued September 13, 2016) (Ex. 1007, “Sakarda”).

II. ANALYSIS

A. Overview

A petition must show how the construed claims are unpatentable under the statutory grounds it identifies. 37 C.F.R. § 42.104(b)(4). At this stage of the proceeding, Petitioner bears the burden of demonstrating a reasonable likelihood that it would prevail with respect to at least one challenged claim for a petition to be granted. 35 U.S.C. § 314(a).

A claim is unpatentable as obvious “if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a); *see KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations).⁹ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

The Supreme Court explained that

Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

⁹ No evidence of secondary considerations has been presented at this stage of the proceeding.

KSR, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” (alteration in original))).

“Whether an ordinarily skilled artisan would have been motivated to modify the teachings of a reference is a question of fact.” *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1327 (Fed. Cir. 2016) (citations omitted). “[W]here a party argues a skilled artisan would have been motivated to combine references, it must show the artisan ‘would have had a reasonable expectation of success from doing so.’” *Arctic Cat Inc. v. Bombardier Recreational Prods. Inc.*, 876 F.3d 1350, 1360–61 (Fed. Cir. 2017) (quoting *In re Cyclobenzaprine Hydrochloride Extended-Release Capsule Patent Litig.*, 676 F.3d 1063, 1068–69 (Fed. Cir. 2012)).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art (“POSITA”) “would have had a minimum of a bachelor’s degree in electrical engineering, computer engineering, physics, or a similar field, and approximately two years of industry or academic experience in a field related to microelectronic architecture design and development, including experience with power management techniques for multicore processors.” Pet. 4 (citing Ex. 1022 ¶¶ 49–51). Petitioner further states that “[w]ork experience can substitute for formal education and additional formal education can substitute for work experience.” *Id.*

For the purposes of this Decision, we apply Petitioner’s proffered level of skill in the art because it appears consistent with the problems addressed in the ’281 patent and the prior art.

C. Claim Construction

We apply the same claim construction standard used by Article III federal courts and the International Trade Commission, both of which follow *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. 37 C.F.R. § 42.100(b) (2024). Accordingly, we construe each challenged claim of the ’281 patent to generally be “the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.*

If the specification “reveal[s] a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess[,] . . . the inventor’s lexicography governs.” *Phillips*, 415 F.3d at 1316 (citing *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002)). Another exception to the general rule that claims are given their ordinary and customary meaning is “when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Uship Intellectual Props., LLC v. United States*, 714 F.3d 1311, 1313 (Fed. Cir. 2013) (quoting *Thorner v. Sony Comput. Ent. Am., LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012)).

Petitioner states that “no terms require construction to resolve this Petition.” Pet. 4. Petitioner also states that “[r]elated litigations may involve controversies not presented here that require construction.” *Id.*

We determine that no express construction of any claim term is necessary for purposes of this Decision. *See Realtime Data, LLC v. Iancu*,

912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

The parties are free to address the construction of any claim term in subsequent authorized briefing during trial. If either party should decide to do so, the brief shall contain a specifically delineated section labelled as such.

D. Ground 1A¹⁰: Alleged Obviousness of Claims 1, 2, 4, 6, 8, 9, 11, 13, 15, 16, 18, and 20 over Sutardja and Mathieson

Petitioner contends that claims 1, 2, 4, 6, 8, 9, 11, 13, 15, 16, 18, and 20 would have been obvious over the combination of Sutardja and Mathieson. Pet. 9–34. Petitioner supports its contentions with the Declaration of Dr. Annavaram. Ex. 1022.

We begin with brief summaries of Sutardja and Mathieson, and then address Petitioner’s contentions.

1. Sutardja (Ex. 1002)

Sutardja is titled “Dynamic Core Switching.” Ex. 1002, code (54). Sutardja relates to dynamically switching cores of multi-core processing systems of mobile computing devices. *Id.* ¶ 2. Sutardja explains that processor systems in such computing devices may be asymmetric, with the processors or cores having different instruction set architectures, or symmetric with the processors or cores having identical instruction set architectures. *Id.* ¶¶ 7–8, Figs. 1A, 1B.

¹⁰ For ease of reference, we use Petitioner’s designation for this ground. Pet. 1.

Sutardja discloses obtaining increased power savings “by using a multi-core processing system with a low-speed, low-power (LP) core and a high-speed, high-power (HP) core.” Ex. 1002 ¶ 212. The “instruction set architecture (ISA) of the LP core [] may differ from the ISA of the HP core,” or alternatively, both may use the same ISAs. *Id.* ¶ 213.

Sutardja discloses using “core morphing” to optimize power consumption and improve performance. Ex. 1002 ¶ 216. Sutardja explains that:

In core morphing, cores are dynamically enabled (i.e., activated) or disabled (i.e., deactivated) based on the system load. The system load may be partly determined based on resource utilization and performance demanded by the applications. In some implementations, only one core may be active (i.e., executing applications) at a time. When one core is active, other cores may be disabled (i.e., deactivated) to save power. The other cores may be disabled in many ways. For example, the other cores may be put in a standby mode wherein the clock frequency and/or the supply voltage of the other cores may be decreased to values that are lower than when the cores are active. Alternatively, the other cores may be completely shut down by disconnecting the power supply to the cores.

Id. ¶ 218.

Sutardja discloses that “[c]ore morphing may be used in multi-core systems comprising one LP core and one HP core. When applications demand still higher performance than that provided by one HP core, multiple HP cores may be used.” Ex. 1002 ¶ 219. According to Sutardja, “[i]n the HP mode, the HP core [] is in the active state and processes threads. The LP core [] may also operate during the HP mode. In other words, the LP core [] may be in the active state during all or part of the HP mode.” *Id.* ¶ 223.

Sutardja discloses that core morphing is useful for optimizing battery life and performance of mobile devices. *Id.* ¶¶ 217, 222.

2. *Mathieson (Ex. 1003)*

Mathieson is titled “System and Method for Power Optimization.” Ex. 1003, code (54). Mathieson discloses a system and method for power optimization. *Id.* ¶ 3. Mathieson discloses a method for optimizing power in a multi-core processing complex that includes a first set of cores comprising one or more fast cores, a second set of cores comprising one or more slow cores, and a controller that determines which mode of operation is more power efficient and causes processing operations to be executed by the first set of cores or the second set of cores to achieve the lowest total power consumption. *Id.* at Abstract, ¶¶ 20, 28, 38.

Mathieson explains that a controller within the CPU switches between a first mode of operation and a second mode of operation based on workload characteristics, performance characteristics of the cores, power characteristics of the cores, and operating conditions of the processing complex. Ex. 1003 Abstract, ¶¶ 8–10, 25, 30, Fig. 2. Mathieson discloses that “[i]n the first mode of operation, the first set of cores is enabled and operable and the second set of cores is disabled” and “[i]n the second mode of operation, the second set of cores is enabled and operable and the first set of cores is disabled.” *Id.* ¶ 30 (reference numbers omitted).

For example, Mathieson’s Figure 4A (reproduced below) depicts a “flow diagram[] of method steps for switching between modes of operation of a processing complex.” Ex. 1003 ¶ 16.

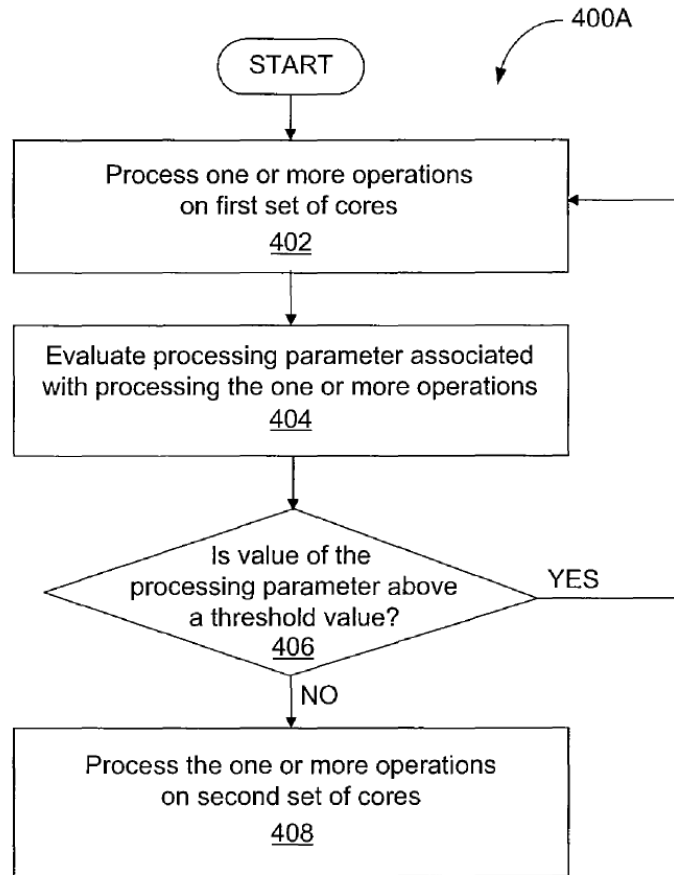


FIG. 4A

Figure 4A describes steps 402, 404, 406, and 408. The method begins when a processor's controller directs one or more operations to be executed by a first set of cores (402). Ex. 1003 ¶ 55, Fig. 4A. Next, the controller evaluates a processing parameter associated with processing the operations (404), such as a processing frequency or instruction throughput, and determines whether the parameter is above a threshold value (406). *Id.* ¶¶ 55–56. If the parameter exceeds the threshold, the processor continues processing operations using the first set of cores (402). *Id.* If the parameter is not above the threshold value, the controller directs one or more operations to be executed by a second set of cores (408). *Id.*

3. *Claims 1, 8, and 15*

Petitioner provides a limitation-by-limitation analysis of independent claims 1, 8, and 15,¹¹ mapping the prior art to the claim limitations and presenting reasons why an ordinarily skilled artisan would have been motivated to combine Sutardja and Mathieson with a reasonable expectation of success. Pet. 9–27, 31–34. Petitioner’s contentions are undisputed at this time because, as noted above, Patent Owner did not submit a preliminary response.

With this background, we analyze Petitioner’s contentions.

Independent Claim 1

Motivation to Combine/Reasonable Expectation of Success

Petitioner contends that “Sutardja discloses a multi-core processing system with a lower power (‘LP’) core and a high power (‘HP’) core.” Pet. 4 (citing Ex. 1002 ¶¶ 221–222, Figs. 3A, 3B). Petitioner further contends that “Mathieson discloses a computer system 100 with fast cores 130 and slow cores 140, where ‘cores 130 are associated with higher performance and higher leakage power than the cores 140.’” *Id.* at 6 (citing Ex. 1003 ¶ 20, Fig. 1). Petitioner further contends that “Mathieson explains that multiple ‘slow’ cores enable processing of complex operations with less power, allow simpler switching of tasks from high to low power cores, and improve parallelism and performance.” *Id.* at 10 (citing Ex. 1003 ¶¶ 29, 34, 57; Ex. 1020 ¶ 28). According to Petitioner, an ordinarily skilled artisan “would have understood that, when applied to Sutardja, following Mathieson’s teaching to use multiple, low-power cores would produce

¹¹ For ease of reference, in our analysis, we refer to Petitioner’s claim limitation identifiers. *See* Pet. vii–x, 13–27.

similar advantages, including using less power and improving parallelism.”
Id. (citing Ex. 1022 ¶¶ 59–60).

Petitioner illustrates the proposed combination of Sutardja and Mathieson with the following annotated version of Sutardja’s Figure 3A (Pet. 11):

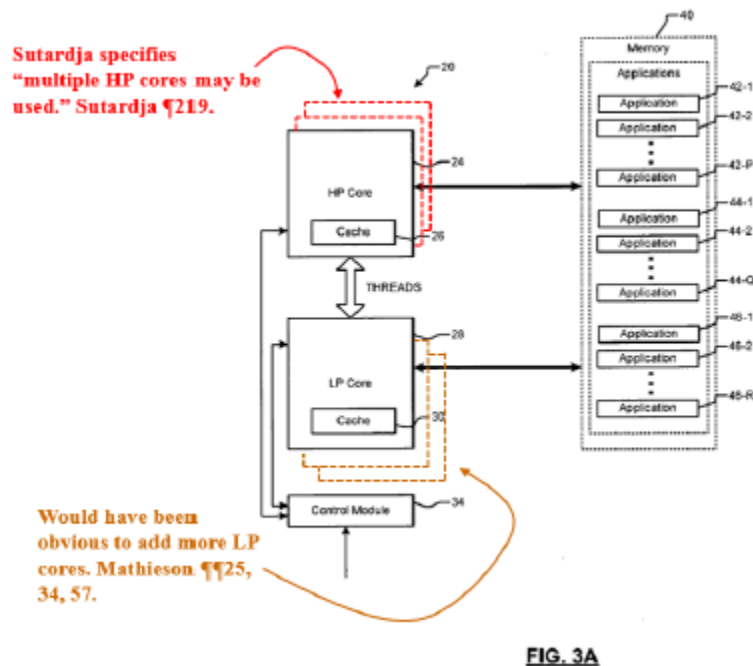


Figure 3A is a “functional block diagram[] of an exemplary processing system including a high power core.” Ex. 1002 ¶ 191. Petitioner annotates Figure 3A by adding two red broken-line rectangles behind high power core 24 with red text “Sutardja specifies ‘multiple HP cores may be used.’ Sutardja ¶ 219” and two brown broken-line rectangles behind low power core 28 with brown text “Would have been obvious to add more LP cores. Mathieson ¶¶ 25, 34, 57.” Pet. 11.

Petitioner provides the following reasons why an ordinarily skilled artisan would have been motivated to combine Sutardja and Mathieson:

1. Both address “power consumption in mobile devices.” Pet 12 (citing Ex. 1002 ¶¶ 4–5; Ex. 1003 ¶ 6–7; Ex. 1022 ¶ 63);
2. The combination “would have required nothing more than combining prior-art elements . . . according to known methods . . . to yield predictable results.” *Id.* (citing Ex. 1022 ¶ 64);
3. The use of “Mathieson’s multiple low-power cores to improve Sutardja’s basic architecture would have required nothing more than using a known technique to improve similar devices in the same way (by adding one or more low-power cores to Sutardja’s architecture).” *Id.* (citing Ex. 1022 ¶ 65);
4. “[P]rior art teachings, such as those in Mathieson and Carmack . . . would have led a [person of ordinary skill in the art] to modify Sutardja to arrive at the claimed invention.” *Id.* (citing Ex. 1022 ¶ 66);
5. An ordinarily skilled artisan would have recognized that “there may be more demand than one slow core can manage, even from applications that do not require high-speed processing” and “[b]ecause slow cores consume less power than fast cores, it would have been desirable to use an additional slow core rather than a fast core in such circumstances to consume less power.” *Id.* at 13 (citing Ex. 1022 ¶ 67);
6. There would have been a reasonable expectation of success in the combination because “[d]uplicating Sutardja’s low-power core would not have resulted in unexpected results.” *Id.* at 13 (citing Ex. 1022 ¶ 6).

We have reviewed Petitioner’s evidence and explanations, and based on the current record at this stage of the proceeding, find that Petitioner sufficiently establishes that an ordinarily skilled artisan would have been motivated to combine Sutardja and Mathieson with a reasonable expectation of success.

Claim 1

[1p]: A multi-core processor comprising:

Petitioner contends that “Sutardja-Mathieson satisfies this feature.” Pet. 13 (citing Ex. 1022 ¶ 69). In particular Petitioner contends that Sutardja discloses a multi-core processing system, i.e., “a processing system 20 with multiple cores, including at least one high-power core 24 and at least one low-power core 28.” *Id.* (citing Ex. 1002 ¶¶ 212, 219, 221–222, 225, Figs. 3A, 3B, 5). Petitioner contends that Mathieson similarly “discloses a multicore processor that has ‘fast’ and ‘slow cores.’” *Id.* at 14 (citing Ex. 1003 ¶¶ 25, 28); *see also id.* at 15 (“Mathieson discloses embodiments with **multiple** ‘slow’ cores (e.g., second set of cores 220).” (citing Ex. 1003 ¶¶ 28–29).

We have reviewed Petitioner’s evidence and explanations and, based on the current record at this stage of the proceeding, find Petitioner sufficiently establishes that the combination of Sutardja and Mathieson teaches the subject matter of the preamble regardless of whether the preamble is limiting.

[1a]: a first plurality of cores and a second plurality of cores that support a same instruction set,

Petitioner contends that the combination of Sutardja and Mathieson teaches this limitation. Pet. 15 (citing Ex. 1022 ¶ 73). As discussed above in connection with motivation to combine, Petitioner’s proposed

combination includes a first plurality of HP cores and a second plurality of LP cores. *Id.*

Petitioner specifically contends that Sutardja discloses that its “high- and low-power cores use the same instruction set architecture (ISA).”

Pet. 17 (citing Ex. 1002 ¶¶ 213, 219, 225, 249; Ex. 1022 ¶¶ 74–75).

Petitioner further contends “to the extent the ISAs may differ, Sutardja consistently teaches that the ‘first [ISA] set is a superset of the second [ISA] set,” and according to Petitioner, “even in embodiments of Sutardja where the cores *may* use different ISAs, all cores still would support at least the second ISA (because the first ISA encompasses the second ISAs).” *Id.* (citing Ex. 1002 ¶¶ 14, 45, 75, 106; Ex. 1022 ¶ 76; alterations by Petitioner).

We have reviewed Petitioner’s evidence and explanations, and based on the current record at this stage of the proceeding, Petitioner sufficiently establishes that the combination of Sutardja and Mathieson teaches this limitation.

[1b]: wherein the first plurality of cores are higher performance and consume more power than the second plurality of cores,

Petitioner contends that the combination of Sutardja and Mathieson teaches this limitation. Pet. 17. In particular, Petitioner contends that Sutardja discloses “that high-power cores 24 are high-speed and high-power while low-power core 28 is low-speed and low-power, so the high-power cores 24 are higher performance than the low-power core 28.” *Id.* (citing Ex. 1002 ¶¶ 211–213, 230; Ex. 1022 ¶ 77). Petitioner further contends that Mathieson similarly “teaches a set of multiple fast cores 210 with higher performance than a set of multiple slow cores 220.” *Id.* at 18 (citing Ex. 1003 ¶¶ 28–29). According to Petitioner, “when applying Mathieson’s teachings to Sutardja’s modified architecture, ‘the first plurality of cores are

higher performance and consume more power than the second plurality of cores.” *Id.* (citing Ex. 1022 ¶¶ 77–79).

We have reviewed Petitioner’s evidence and explanations, and based on the current record at this stage of the proceeding, find that Petitioner sufficiently establishes that the combination of Sutardja and Mathieson teaches this limitation.

[1c]: and each of the second plurality of cores have a maximum operating frequency that is less than a maximum operating frequency of each of the first plurality of cores;

Petitioner contends that the combination of Sutardja and Mathieson teaches this limitation. Pet. 18. In particular, Petitioner contends that “Sutardja teaches that its high-power cores (the first plurality of cores) can operate at frequencies greater than 1 GHz, whereas its low-power core (the second plurality of cores) operates at frequencies less than 500 MHz.” *Id.* (citing Ex. 1002 ¶¶ 44, 74, 105, 234; Ex. 1022 ¶ 80).

We have reviewed Petitioner’s evidence and explanations, and based on the current record at this stage of the proceeding, find that Petitioner sufficiently establishes that the combination of Sutardja and Mathieson teaches this limitation.

[1d]: a shared caching layer shared by the first plurality of cores and the second plurality of cores; and

Petitioner contends that the combination of Sutardja and Mathieson teaches this limitation. Pet. 20. Petitioner contends that “Sutardja’s high-power and low-power cores may share an L2 cache 206, which serves as a last-level cache (LLC) for Sutardja’s various cores.” *Id.* (citing Ex. 1002 ¶ 248; Ex. 1022 ¶ 81). Petitioner further contends that “Mathieson also teaches fast cores 210 and slow cores 220 sharing resource unit 230” which

Mathieson describes “as a shared L2 cache.” *Id.* at 22 (citing Ex. 1003 ¶¶ 25, 44–46, Fig. 2).

We have reviewed Petitioner’s evidence and explanations, and based on the current record at this stage of the proceeding, find that Petitioner sufficiently establishes that the combination of Sutardja and Mathieson teaches this limitation.

[1e]: power management hardware to enable and disable the first plurality of cores and the second plurality of cores

Petitioner contends that the combination of Sutardja and Mathieson teaches this limitation. Pet. 22. In particular, Petitioner contends that “Sutardja discloses a Power Management System (PMS) module 242 that manages power consumption” and “can trigger a core switching module 212 to enable/disable the high-power and low-power cores.” *Id.* (citing Ex. 1002 ¶¶ 218, 251, 253, 271). According to Petitioner, “[t]he term ‘module’ in Sutardja comprises ‘power management hardware,’ as claimed, to perform the functions Sutardja describes.” *Id.* at 23 (citing Ex. 1002 ¶ 209, Fig. 5; Ex. 1003 ¶ 43; Ex. 1022 ¶¶ 85–86).

We have reviewed Petitioner’s evidence and explanations, and based on the current record at this stage of the proceeding, find that Petitioner sufficiently establishes that the combination of Sutardja and Mathieson teaches this limitation.

[1f]: wherein an operating system that executes on the multi-core processor is to monitor a demand for the multi-core processor and control a core mix of the first plurality of cores and the second plurality of cores based on the demand with the power management hardware.

Petitioner contends that the combination of Sutardja and Mathieson teaches this limitation. Pet. 23. In particular, Petitioner contends that Sutardja’s “LP and HP core 200 and 204 may execute the same operating

system (OS).” *Id.* (citing Ex. 1002 ¶ 249). Petitioner further contends that Sutardja’s “kernel module 220 . . . is a component of the OS, manages system resources . . . and is coupled to resources like PMS module 242, which manages or controls power consumption, and core profile module 240, which is part of PMS module 242 and ‘may monitor system loading.’” *Id.* at 23–24 (citing Ex. 1002 ¶¶ 249, 251, Fig. 5; Ex. 1022 ¶¶ 87–88).

Petitioner next contends that Sutardja’s “Figure 9A^[12] describes ‘a power management system (PMS) 400 that optimizes power consumption of [a] mobile device using dynamic core switching.’” Pet. 24 (citing Ex. 1002 ¶ 278; second alteration by Petitioner). Petitioner argues that “Figure 9A shows a PMS module 402, which a [person of ordinary skill in the art] would have understood to be the same as . . . PMS module 242 in Figure 5” and PMS module 402 “manages power consumption based on various inputs, including ‘inputs received from the OS.’” *Id.* (citing Ex. 1002 ¶¶ 251–253, 278). Petitioner similarly argues that “kernel module 422 [shown in Figure 9A] corresponds to kernel module 220 of Figure 5.” *Id.* at 25 (citing Ex. 1002 ¶ 253; Ex. 1022 ¶ 91). According to Petitioner, an ordinarily skilled artisan would have understood that “kernel module 220 controls the core mix by enabling and disabling high power and low power cores based on demand.” *Id.* at 26 (citing Ex. 1022 ¶ 93).

We have reviewed Petitioner’s evidence and explanations, and based on the current record at this stage of the proceeding, find that Petitioner

¹² Petitioner contends that an ordinarily skilled artisan “would have understood this power management system [shown in Figure 9A] applies to the multi-core processor described in Figures 3A and 5.” Pet. 24 (citing Ex. 1022 ¶ 89).

sufficiently establishes that the combination of Sutardja and Mathieson teaches this limitation.

Summary of Claim 1

For all the foregoing reasons, Petitioner establishes a reasonable likelihood that claim 1 would have been obvious over the combination of Sutardja and Mathieson.

Independent Claim 8

For claim limitations [8a]–[8e], Petitioner relies on various contentions discussed above for claim 1. Pet. 31–32.

For the preamble of claim 8, Petitioner contends that the combination of Sutardja and Mathieson teaches “[a] method” and “switches between high-power and low-power cores.” Pet. 31 (citing Ex. 1002 ¶¶ 40, 251; Ex. 1022 ¶ 99).

We have reviewed Petitioner’s evidence and explanations and, based on the current record at this stage of the proceeding, find Petitioner sufficiently establishes that the combination of Sutardja and Mathieson teaches the subject matter of the preamble regardless of whether the preamble is limiting.

For limitation [8f], Petitioner first points to its contentions for limitations [1e] and [1f]. Pet. 32. Petitioner contends that Sutardja’s “PMS module 242 can ‘initiate or control changes in system operation based on the monitored system loading’” and “controls a core mix by (i) triggering a core switching module 212 to enable or disable the high power and low power cores and (ii) changing operating frequencies based on demand.” *Id.* (citing Ex. 1002 ¶¶ 251–253). According to Petitioner, an ordinarily skilled artisan

“would have understood Sutardja’s ‘monitored system loading’ refers to demand.” *Id.* (citing Ex. 1002 ¶ 251; Ex. 1022 ¶¶ 105–107).

We have reviewed Petitioner’s evidence and explanations, and based on the current record at this stage of the proceeding, find that Petitioner sufficiently establishes that the combination of Sutardja and Mathieson teaches limitation [8f].

Consequently, for the foregoing reasons and the reasons discussed above for claim 1, Petitioner establishes a reasonable likelihood that claim 8 would have been obvious over the combination of Sutardja and Mathieson.

Independent Claim 15

For claim limitations [15a]–[15f], Petitioner relies on various contentions discussed above for claims 1 and 8. Pet. 33–34. Consequently, for the same reasons discussed above for claim 1, Petitioner establishes a reasonable likelihood that claim 15 would have been obvious over the combination of Sutardja and Mathieson

4. Claims 2, 4, 6, 9, 11, 13, 16, 18, and 20

These claims depend directly or indirectly from claim 1, claim 8, or claim 15. Ex. 1001, 8:13–34, 8:52–9:4. Petitioner sets forth evidence and argument as to why the combination of Sutardja and Mathieson allegedly renders claims 2, 4, 6, 9, 11, 13, 16, 18, and 20 obvious. Pet. 27–31.

We reviewed the evidence cited by Petitioner, and based on the current record at this stage of the proceeding, Petitioner establishes a reasonable likelihood that these dependent claims would have been obvious over the combination of Sutardja and Mathieson.

E. Remaining Obviousness Grounds

Because we have already determined that Petitioner has shown a reasonable likelihood that it would prevail in establishing that at least one challenged claim of the '281 patent is unpatentable as discussed above and because Patent Owner has not submitted a preliminary response, we do not reach the remaining grounds at this time.

III. CONCLUSION

Based on the present record, we determine that Petitioner demonstrates a reasonable likelihood that it would prevail in establishing that at least one challenged claim of the '281 patent is unpatentable. A decision to institute under § 314 may not institute on fewer than all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 584 U.S. 357, 371 (2018). In addition, per Board practice, if the Board institutes trial, it will institute “on all of the challenged claims and on all grounds of unpatentability asserted for each claim.” *See* 37 C.F.R. § 42.108(a). We, thus, institute an *inter partes* review of all challenged claims of the '281 patent based on all grounds in the Petition. At this stage of the proceeding, we have not made a final determination under 35 U.S.C. § 318(a) with respect to the unpatentability of any challenged claim.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the '281 patent is instituted with respect to all challenged claims and grounds set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4(b), *inter partes* review of the '281 patent shall commence

IPR2024-01488
Patent 10,740,281 B2

on the entry date of this Order, and notice is hereby given of the institution
of a trial.

IPR2024-01488
Patent 10,740,281 B2

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