

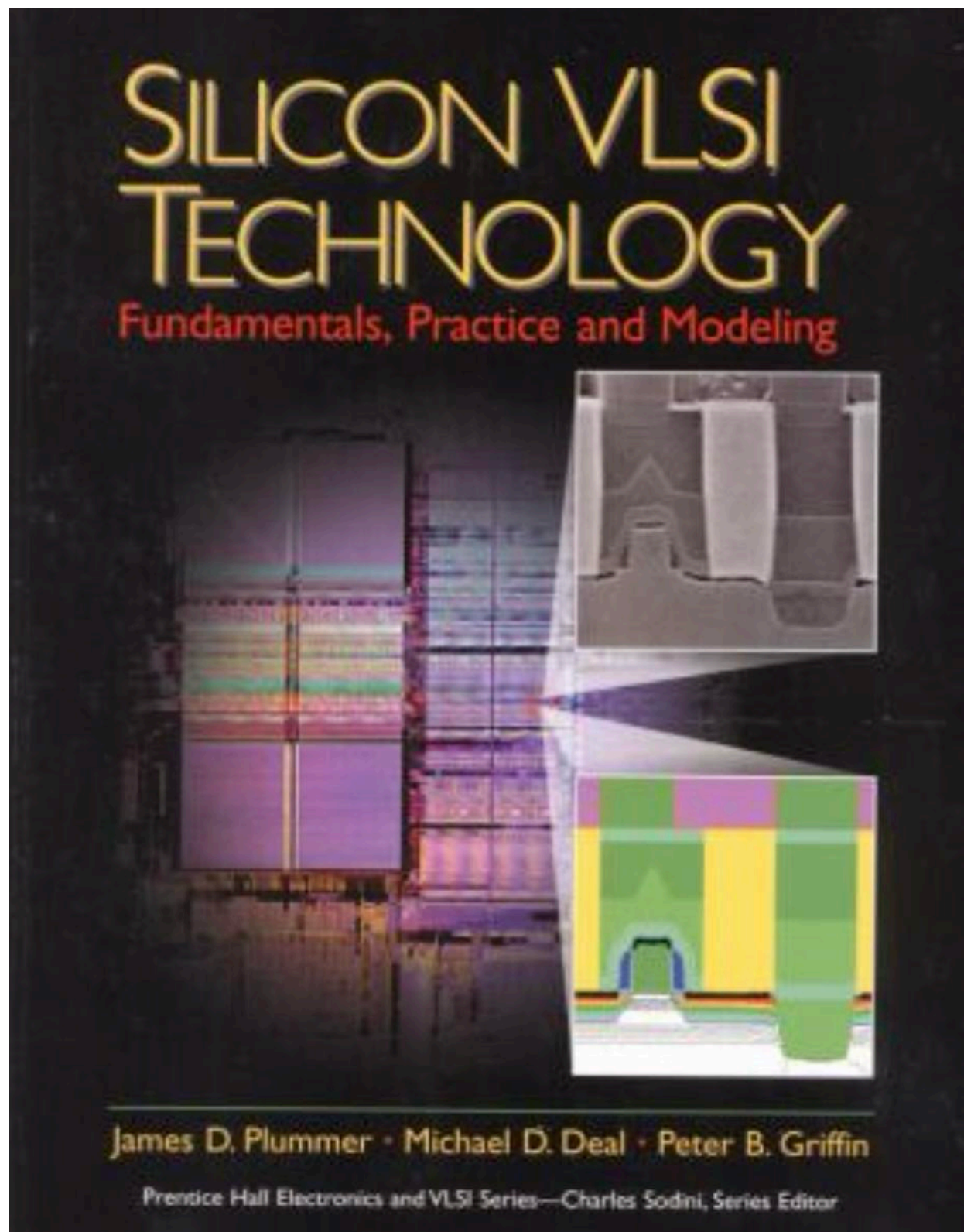


Table of Contents

Preface	i
Chapter 1: Introduction and Historical Perspective	
1.1 Introduction	1
1.2 Integrated Circuits and the Planar Process - Key Inventions That Made It All Possible	6
1.3 Semiconductors	12
1.4 Semiconductor Devices	30
1.4.1 PN Diodes	30
1.4.2 MOS Transistors	32
1.4.3 Bipolar Junction Transistors	35
1.5 Semiconductor Technology Families	37
1.6 Modern Scientific Discovery - Experiments, Theory and Computer Simulation	39
1.7 The Plan For This Book	40
1.8 Summary of Key Ideas	41
1.9 References	42
1.10 Problems	42
Chapter 2: Modern CMOS Technology	
2.1 Introduction	44
2.2 CMOS Process Flow	44
2.2.1 The Beginning - Choosing a Substrate	45
2.2.2 Active Region Formation	47
2.2.3 Process Option for Device Isolation - Shallow Trench Isolation	51
2.2.4 N and P Well Formation	53
2.2.5 Process Options for Active Region and Well Formation	57
2.2.6 Gate Formation	63
2.2.7 Tip or Extension (LDD) Formation	68
2.2.8 Source/Drain Formation	71
2.2.9 Contact and Local Interconnect Formation	73
2.2.10 Multi-Level Metal Formation	75
2.3 Summary of Key Ideas	80
2.4 Problems	81
Chapter 3: Crystal Growth, Wafer Fabrication and Basic Properties of Silicon Wafers	
3.1 Introduction	83
3.2 Historical Development and Basic Concepts	83
3.2.1 Crystal Structure	83
3.2.2 Defects in Crystals	87

3.2.3	Raw Materials and Purification	90
3.2.4	Czochralski and Float Zone Crystal Growth Methods	91
3.2.5	Wafer Preparation and Specification	94
3.3	Manufacturing Methods and Equipment	97
3.4	Measurement Methods	99
3.4.1	Electrical Measurements	99
3.4.1.1	Hot Point Probe	99
3.4.1.2	Sheet Resistance	100
3.4.1.3	Hall Effect Measurements	102
3.4.2	Physical Measurements	104
3.4.2.1	Defect Etches	105
3.4.2.2	Fourier Transform Infrared Spectroscopy	105
3.4.2.3	Electron Microscopy	106
3.5	Models and Simulation	108
3.5.1	Czochralski Crystal Growth	108
3.5.2	Dopant Incorporation During CZ Crystal Growth	112
3.5.3	Zone Refining and FZ Growth	115
3.5.4	Point Defects	118
3.5.5	Oxygen in Silicon	124
3.5.6	Carbon in Silicon	128
3.5.7	Simulation	128
3.6	Limits and Future Trends in Technologies and Models	129
3.7	Summary of Key Ideas	131
3.8	References	132
3.9	Problems	133

Chapter 4: Semiconductor Manufacturing - Clean Rooms, Wafer Cleaning and Gettering

4.1	Introduction	135
4.2	Historical Development and Basic Concepts	137
4.2.1	Level 1 Contamination Reduction: Clean Factories	140
4.2.2	Level 2 Contamination Reduction: Wafer Cleaning	142
4.2.3	Level 3 Contamination Reduction: Gettering	144
4.3	Manufacturing Methods and Equipment	147
4.3.1	Level 1 Contamination Reduction: Clean Factories	147
4.3.2	Level 2 Contamination Reduction: Wafer Cleaning	148
4.3.3	Level 3 Contamination Reduction: Gettering	150
4.4	Measurement Methods	152
4.4.1	Level 1 Contamination Reduction: Clean Factories	152
4.4.2	Level 2 Contamination Reduction: Wafer Cleaning	154
4.4.3	Level 3 Contamination Reduction: Gettering	157
4.5	Models and Simulation	160
4.5.1	Level 1 Contamination Reduction: Clean Factories	161
4.5.2	Level 2 Contamination Reduction: Wafer Cleaning	164
4.5.3	Level 3 Contamination Reduction: Gettering	166
4.5.3.1	Step 1: Making the Metal Atoms Mobile	167

4.5.3.2 Step 2: Metal Diffusion to the Gettering Site	168
4.5.3.3 Step 3: Trapping the Metal Atoms at the Gettering Site	170
4.6 Limits and Future Trends in Technologies and Models	173
4.7 Summary of Key Ideas	175
4.8 References	176
4.9 Problems	178
Chapter 5: Lithography	
5.1 Introduction	180
5.2 Historical Development and Basic Concepts	182
5.2.1 Light Sources	185
5.2.2 Wafer Exposure Systems	186
5.2.2.1 Optics Basics - Ray Tracing and Diffraction	187
5.2.2.2 Projection Systems (Fraunhofer Diffraction)	190
5.2.2.3 Contact and Proximity Systems (Fresnel Diffraction)	196
5.2.3 Photoresists	198
5.2.3.1 g-line and i-line Resists	200
5.2.3.2 Deep Ultraviolet (DUV) Resists	201
5.2.3.3 Basic Properties and Characterization of Resists	203
5.2.4 Mask Engineering - Optical Proximity Correction and Phase Shifting	207
5.3 Manufacturing Methods and Equipment	209
5.3.1 Wafer Exposure Systems	210
5.3.2 Photoresists	213
5.4 Measurement Methods	216
5.4.1 Measurement of Mask Features and Defects	217
5.4.2 Measurement of Resist Patterns	218
5.4.3 Measurement of Etched Features	219
5.5 Models and Simulation	221
5.5.1 Wafer Exposure Systems	221
5.5.2 Optical Intensity Pattern in the Photoresist	229
5.5.3 Photoresist Exposure	233
5.5.3.1 g-line and i-line DQN Resists	233
5.5.3.2 DUV Resists	237
5.5.4 Post Exposure Bake (PEB)	237
5.5.4.1 g-line and i-line DQN Resists	238
5.5.4.2 DUV Resists	239
5.5.5 Photoresist Developing	240
5.5.6 Photoresist Post Bake	243
5.5.7 Advanced Mask Engineering	244
5.6 Limits and Future Trends in Technologies and Models	245
5.6.1 Electron Beam Lithography	246
5.6.2 X-ray Lithography	248

5.6.3	Advanced Mask Engineering	250
5.6.4	New Resists	251
5.7	Summary of Key Ideas	253
5.8	References	253
5.9	Problems	255
Chapter 6: Thermal Oxidation and the Si/SiO ₂ Interface		
6.1	Introduction	258
6.2	Historical Development and Basic Concepts	261
6.3	Manufacturing Methods and Equipment	266
6.4	Measurement Methods	268
6.4.1	Physical Measurements	269
6.4.2	Optical measurements	269
6.4.3	Electrical Measurements - The MOS Capacitor	271
6.5	Models and Simulation	281
6.5.1	First Order Planar Growth Kinetics - The Linear Parabolic Model	281
6.5.2	Other Models for Planar Oxidation Kinetics	291
6.5.3	Thin Oxide SiO ₂ Growth Kinetics	294
6.5.4	Dependence of Growth Kinetics on Pressure	296
6.5.5	Dependence of Growth Kinetics on Crystal Orientation	298
6.5.6	Mixed Ambient Growth Kinetics	300
6.5.7	2D SiO ₂ Growth Kinetics	301
6.5.8	Advanced Point Defect Based Models For Oxidation	306
6.5.9	Substrate Doping Effects	309
6.5.10	Polysilicon Oxidation	312
6.5.11	Si ₃ N ₄ Growth and Oxidation Kinetics	314
6.5.12	Silicide Oxidation	317
6.5.13	Si/SiO ₂ Interface Charges	318
6.5.14	Complete Oxidation Module Simulation	323
6.6	Limits and Future Trends in Technologies and Models	325
6.7	Summary of Key Ideas	326
6.8	References	327
6.9	Problems	330
Chapter 7: Dopant Diffusion		
7.1	Introduction	335
7.2	Historical Development and Basic Concepts	338
7.2.1	Dopant Solid Solubility	339
7.2.2	Diffusion From a Macroscopic Viewpoint	340
7.2.3	Analytic Solutions of the Diffusion Equation	343
7.2.4	Gaussian Solution in an Infinite Medium	343
7.2.5	Gaussian Solution Near a Surface	345
7.2.6	Error-function Solution in an Infinite Medium	346

7.2.7	Error-function Solution Near a Surface	347
7.2.8	Intrinsic Diffusion Coefficients of Dopants in Silicon	348
7.2.9	Effect of Successive Diffusion Steps	351
7.2.10	Design and Evaluation of Diffused Layers	352
7.2.11	Summary of Basic Diffusion Concepts	355
7.3	Manufacturing Methods and Equipment	355
7.4	Measurement Methods	358
7.4.1	SIMS	358
7.4.2	Spreading Resistance	359
7.4.3	Sheet Resistance	360
7.4.4	Capacitance-Voltage	361
7.4.5	TEM Cross Section	361
7.4.6	2-D Electrical Measurements Using Scanning Probe Microscopy	362
7.4.7	Inverse Electrical Measurements	364
7.5	Models and Simulation	364
7.5.1	Numerical Solutions of the Diffusion Equation	365
7.5.2	Modifications to Fick's Laws to Account for Electric Field Effects	367
7.5.3	Modifications to Fick's Laws to Account for Concentration Dependent Diffusion	370
7.5.4	Segregation	374
7.5.5	Interfacial Dopant Pile-up	377
7.5.6	Summary of the Macroscopic Diffusion Approach	378
7.5.7	The Physical Basis for Diffusion at an Atomic Scale	379
7.5.8	Oxidation Enhanced or Retarded Diffusion	380
7.5.9	Dopant Diffusion Occurs by Both I and V	383
7.5.10	Activation Energy for Self and Dopant Diffusion	387
7.5.11	Dopant-Defect Interactions	387
7.5.12	Chemical Equilibrium Formulation for Dopant-Defect Interactions	392
7.5.13	Simplified Expression for Modeling	396
7.5.14	Charge State Effects	398
7.6	Limits and Future Trends in Technologies and Models	400
7.6.1	Doping Methods	401
7.6.2	Advanced Dopant profile Modeling - Fully-Kinetic Description of Dopant-Defect Interactions	401
7.7	Summary of Key Ideas	403
7.8	References	404
7.9	Problems	405

Chapter 8: Ion Implantation

8.1	Introduction	410
8.2	Historical Development and Basic Concepts	410
8.2.1	Implants in Real Silicon - The Role of the Crystal Structure	419

8.3	Manufacturing Methods and Equipment	423
8.3.1	High Energy Implants	425
8.3.2	Ultra Low Energy Implants	426
8.3.3	Ion Beam Heating	427
8.4	Measurement Methods	428
8.5	Models and Simulation	428
8.5.1	Nuclear Stopping	429
8.5.2	Non-local Electronic Stopping	431
8.5.3	Local Electronic Stopping	432
8.5.4	Total Stopping Powers	433
8.5.5	Damage Production	434
8.5.6	Damage Annealing	437
8.5.7	Solid Phase Epitaxy	440
8.5.8	Dopant Activation	441
8.5.9	Transient Enhanced Diffusion	444
8.5.10	Atomic Level Understanding of TED	445
8.5.11	Effects on Devices	454
8.6	Limits and Future Trends in Technologies and Models	456
8.7	Summary of Key Ideas	457
8.8	References	457
8.9	Problems	459

Chapter 9: Thin Film Deposition

9.1	Introduction	464
9.2	Historical Development and Basic Concepts	465
9.2.1	Chemical Vapor Deposition (CVD)	466
9.2.1.1	Atmospheric Pressure Chemical Vapor Deposition (APCVD)	467
9.2.1.2	Low Pressure Chemical Vapor Deposition (LPCVD)	479
9.2.1.3	Plasma Enhanced Chemical Vapor Deposition (PECVD)	481
9.2.1.4	High Density Plasma Chemical Vapor Deposition (HDPCVD)	483
9.2.2	Physical Vapor Deposition (PVD)	483
9.2.2.1	Evaporation	483
9.2.2.2	Sputter Deposition	491
	DC Sputter Deposition	492
	Reactive Sputter Deposition	498
	RF Sputter Deposition	499
	Bias-Sputtering	500
	Magnetron Sputter Deposition	502
	Collimated Sputter Deposition and Ionized Sputter Deposition	502
	High Temperature or Hot Sputter Deposition	505
9.3	Manufacturing Methods	505
9.3.1	Epitaxial Silicon Deposition	507
9.3.2	Polycrystalline Silicon Deposition	509
9.3.3	Silicon Nitride Deposition	512

9.3.4 Silicon Dioxide Deposition	513
9.3.5 Al Deposition	515
9.3.6 Ti and Ti-W Deposition	516
9.3.7 W Deposition	516
9.3.8 TiSi_2 and WSi_2 Deposition	517
9.3.9 TiN Deposition	518
9.3.10 Cu Deposition	519
9.4 Measurement Methods	521
9.5 Models and Simulation	522
9.5.1. Models for Deposition Simulations	522
9.5.1.1 Models in Physically-Based Simulators Such as SPEEDIE	523
9.5.1.2 Models for Different Types of Deposition Systems	530
9.5.1.3 Comparing CVD and PVD, and Typical Parameter Values	535
9.5.2 Simulations of Deposition using a Physically-Based Simulator, SPEEDIE	538
9.5.3 Other Deposition Simulations	545
9.6 Limits and Future Trends in Technologies and Models	547
9.7 Summary of Key Ideas	549
9.8 References	549
9.9 Problems	552
Chapter 10: Etching	
10.1 Introduction	555
10.2 Historical Development and Basic Concepts	557
10.2.1 Wet Etching	558
10.2.2 Plasma Etching	565
10.2.2.1 Plasma Etching Mechanisms	567
Chemical Etching	568
Physical Etching	570
Ion Enhanced Etching	571
10.2.2.2 Types of Plasma Etch Systems	574
Plasma Etching in Barrel Etchers	574
Plasma Etching in Parallel Plate Systems - Plasma Mode	575
Plasma Etching in Parallel Plate Systems - Reactive Ion Etching Mode	575
Etching in High Density Plasma Systems	577
Sputter Etching and Ion Milling	578
10.2.2.3 Summary of Plasma Systems and Mechanisms	580
10.3. Manufacturing Methods	581
10.3.1 Plasma Etching Conditions and Issues	582
10.3.2 Plasma Etch Methods for Various Films	586
10.3.2.1 Plasma Etching Silicon Dioxide	588
10.3.2.2 Plasma Etching Polysilicon	591
10.3.2.3 Plasma Etching Aluminum	593
10.4 Measurement Methods	594

10.5 Models and Simulation	596
10.5.1 Models for Etching Simulations	596
10.5.2 Etching Models - Linear Etch Model	599
10.5.3 Etching Models - Saturation/Adsorption Model for Ion Enhanced Etching	606
10.5.4 Etching Models - More Advanced Models	611
10.5.5 Other Etching Simulations	613
10.6 Limits and Future Trends in Technologies and Models	615
10.7 Summary of Key Ideas	617
10.8 References	618
10.9 Problems	620
Chapter 11: Backend Technology	
11.1 Introduction	622
11.2 Historical Development and Basic Concepts	627
11.2.1 Contacts	629
11.2.2 Interconnects and Vias	636
11.2.3 Dielectrics	647
11.3. Manufacturing Methods	655
11.3.1 Silicided Gates and Source/Drain Regions	656
11.3.2 First Level Dielectric Processing	657
11.3.3 Contact Formation	659
11.3.4 Global Interconnects	660
11.3.5 IMD Deposition and Planarization	662
11.3.6 Via Formation	664
11.3.7 Final Steps	664
11.4 Measurement Methods	664
11.4.1 Morphological Measurements	664
11.4.2 Electrical Measurements	665
11.4.3 Chemical and Structural Measurements	670
11.4.4 Mechanical Measurements	672
11.5 Models and Simulation	675
11.5.1 Silicide Formation	675
11.5.2 Chemical-Mechanical Polishing	681
11.5.3 Reflow	684
11.5.4 Grain Growth	690
11.5.5 Diffusion in Polycrystalline Materials	698
11.5.6 Electromigration	701
11.6 Limits and Future Trends in Technologies and Models	711
11.7 Summary of Key Ideas	715
11.8 References	716
11.9 Problems	719

Appendixes

A.1 Standard Prefixes	722
A.2 Useful Conversions	722
A.3 Physical Constants	723
A.4 Physical Properties of Silicon	724
A.5 Properties of Insulators Used in Silicon Technology	725
A.6 Color chart for deposited Si_3N_4 films	726
A.7 Color chart for thermally grown SiO_2 films	727
A.8 Irwin Curves	729
A.9 Error function	731
A.10 List of Important Symbols	736
A.11 List of Common Acronyms	737
Index	740

This chapter will focus primarily on the thermal oxidation process and the properties of the Si/SiO₂ interface. Deposited oxides and other deposited thin films are described in detail in Chapter 9.

6.2 Historical Development and Basic Concepts

A number of experiments done in the past thirty years [6.2 - 6.5], have conclusively shown that when silicon is oxidized, the oxidation process occurs at the Si/SiO₂ interface as illustrated in Fig. 6.2. Because of this, a new interface is constantly forming and moving downward into the silicon substrate. Silicon oxidation therefore occurs by the inward diffusion of the oxidant, rather than the outward diffusion of silicon. Conceptually, the simplest way to demonstrate this is to grow an SiO₂ layer with one oxygen isotope and then continue the growth with a second isotope (O¹⁶ and O¹⁸ for example). Profiling through the resulting composite oxide with a mass sensitive technique can then determine whether the second oxide grows at the top or bottom surface. This and other related experiments have consistently shown that the new oxide grows at the Si/SiO₂ interface.

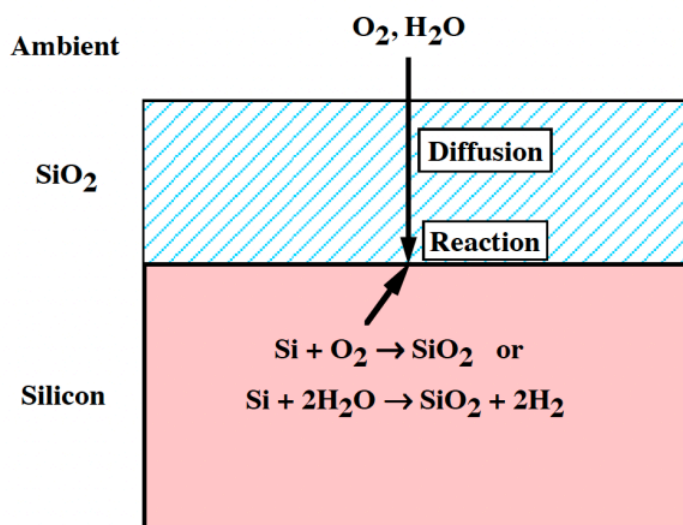


Fig. 6.2: Basic process for the oxidation of silicon. The chemical reaction takes place at the Si/SiO₂ interface.

Conceptually one can think of this process in the following way. The Si atoms in the substrate are bonded to other Si atoms. These bonds must be broken, oxygen atoms inserted between the silicon atoms, and finally Si-O bonds formed. The process involves a volume expansion because of the room needed for the oxygen atoms. As illustrated in the center of Fig. 6.3, the oxide would like to expand by 30% in all three dimensions to accommodate the oxygen atoms. However because the silicon substrate prevents expansion in the two lateral directions, the only option is for the oxide to expand upwards as shown on the right of Fig. 6.3. The volume is thus accommodated by a 2.2 times upward expansion of the oxide compared to the volume of the silicon oxidized.

Fig. 6.4 illustrates this in a real two-dimensional structure. This example is a SEM cross-section of a simple LOCOS process like the one we described in Chapter 2. On planar surfaces, most of the volume expansion is accommodated simply by the oxide growing up above the original silicon surface as in Fig. 6.3. On shaped surfaces, which are common especially in advanced

silicon device structures, the expansion may not be so easily accommodated. LOCOS results in a non-planar Si/SiO₂ interface between the nitride masked and oxidized regions and an obvious transition region between the two. This transition region takes on a characteristic “bird’s beak” shape because of lateral oxidation under the nitride mask. While Fig. 6.3 represents what happens in the real LOCOS structure away from the nitride mask, the situation is clearly much more complicated in shaped structures.

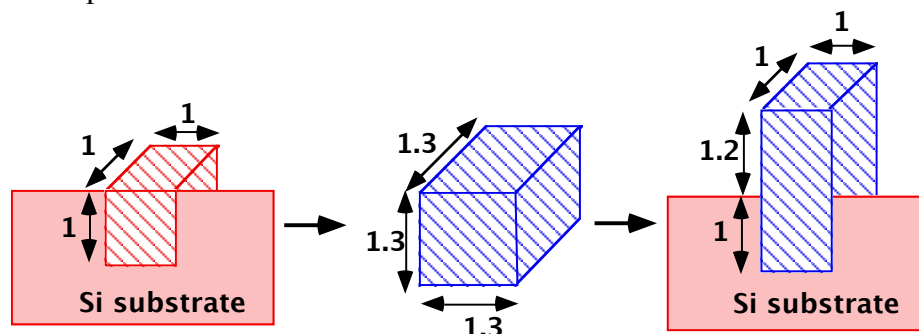


Fig. 6.3: Volume expansion that occurs during silicon oxidation. A unit volume of silicon on the left is transformed into SiO₂. In the middle the volume expansion is unconstrained; on the right the substrate restricts the expansion to one dimension.

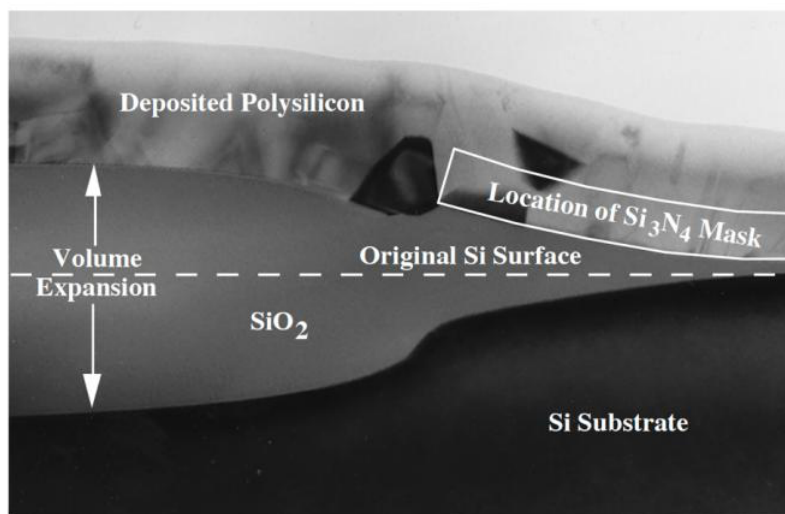


Fig. 6.4: Scanning electron micrograph of a simple LOCOS structure. The silicon oxidation was masked on the right side by a Si₃N₄ layer. A polysilicon layer has been deposited on top of the structure, after the Si₃N₄ layer was stripped, to provide contrast in the picture. Note that the grown oxide on the left side occupies approximately twice the volume of the silicon consumed in the oxidation. Courtesy of J. Bravman, Stanford University.

Oxide layers grown on silicon are amorphous. This might seem surprising initially because we are oxidizing a single crystal substrate and SiO₂ exists in both crystalline and amorphous phases. However, there are no crystalline forms of SiO₂ whose lattice size closely matches the silicon substrate. Any attempt to grow single crystal SiO₂ on silicon would therefore result in very large stresses. Such stresses could easily be large enough to generate crystallographic defects in the silicon, which would significantly degrade circuit yield and device performance. Even though

the oxide that grows is amorphous, it does have short range order, which is illustrated in Fig. 6.5. SiO_4 tetrahedra are the basic units from which SiO_2 forms. These tetrahedra bond together by sharing oxygen atoms as illustrated on the right of the figure. Such shared atoms are called bridging oxygen atoms. In the amorphous forms of SiO_2 there may also be some non-bridging oxygen atoms present. These phases are often referred to as fused silica. Crystalline forms of SiO_2 such as quartz contain only bridging oxygen bonds. The various crystalline and amorphous forms of SiO_2 arise because of the ability of the bridging oxygen bonds to rotate allowing the position of one tetrahedron to move with respect to its neighbors. This same rotation is what allows the material to lose long-range order and hence become amorphous. At normal processing temperatures, the thermodynamically stable form of SiO_2 is one of the crystalline forms. These forms are rarely observed in IC structures however, because the time required for amorphous SiO_2 to rearrange itself into a crystalline form is very long compared to normal diffusion, oxidation or anneal cycles. Occasionally fused silica furnace tubes that are used in oxidation or diffusion furnaces will crystallize (a process called devitrification) after many months or years at high temperature.

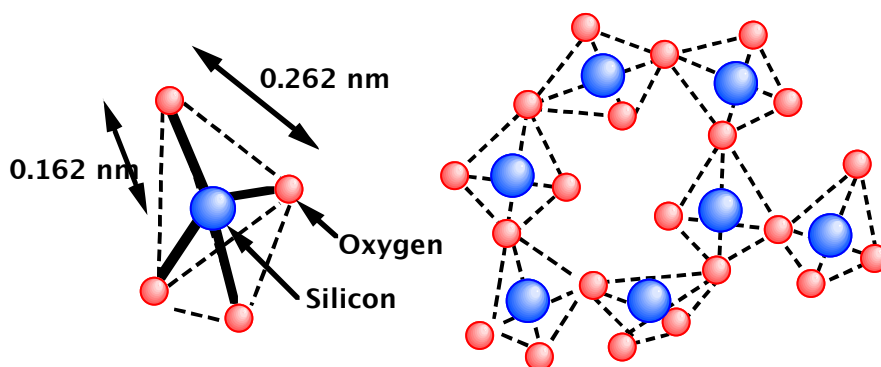


Fig. 6.5: Structure of fused silica glass. The silicon atoms are in the center of each of the tetrahedra. The O-O distance is 0.262 nm; and the Si-O distance is 0.162 nm. The Si-Si bond distance depends on the particular form of SiO_2 , but is about 0.31 nm. The six membered ring structure of SiO_2 is shown conceptually on the right.

The oxide layers that grow on Si are normally in compressive stress. At the Si/ SiO_2 interface, the growing oxide can expand only upwards, not laterally since it must attach to the silicon substrate. This results in compressive stresses that can be as large as 5×10^9 dynes cm^{-2} . At temperatures above about 1000°C , the oxide can relieve some of this stress by viscous flow; at lower temperatures, the oxide viscosity is too high to allow much relief to take place. In addition to these intrinsic stresses which can be present after an oxide is grown, there is also a large difference in the thermal expansion coefficients of Si and SiO_2 . As the wafers are cooled down after an oxide is grown, this results in an additional compressive stress in the oxide that can be as high as a few $\times 10^9$ dynes cm^{-2} . These two effects place the silicon substrate in tension; however, the substrate is many times thicker than the oxide layer and as a result, the tensile stresses are scaled down in proportion to the thickness ratio. These effects can be easily observed even on flat silicon wafers. After an oxidation, SiO_2 is normally present on both the top and back surface of the wafer and the stresses from the two oxide films therefore balance. If the oxide is chemically stripped from one surface, however, a distinct bow will be observed in the wafer because of the stresses. In fact measurement of this “wafer curvature” is one way to determine the stress levels in SiO_2 or other thin films on silicon substrates.

Fig. 3.15 showed a high-resolution transmission electron micrograph (TEM) of the Si/SiO₂ interface. The atomic resolution in this image clearly shows the silicon crystal structure, the amorphous SiO₂ layer and the abruptness of the interface. A number of recent studies using TEM and other techniques have shown that the Si/SiO₂ interface is normally characterized by a transition region which is very narrow (perhaps only one atomic distance). The interface is usually quite flat, although there are steps of one atomic distance which occur occasionally. The abruptness of the interface depends to some extent on the process conditions used to grow the oxide and the interface is a little rougher for oxides which are rapidly grown (H₂O versus O₂ oxidation or high pressure oxidation, for example). The interface is also a little rougher for oxides grown at low temperatures.

The growth kinetics of SiO₂ layers on silicon have been studied for more than three decades, and continue to be studied today. Early studies variously reported the growth rate to have a linear, parabolic, logarithmic, inverse logarithmic or power law dependence on time. The first widely accepted model of the growth kinetics was due to Deal and Grove in 1965 [6.6]. This work showed that over a wide range of conditions, the growth followed a linear parabolic law which could be explained on a solid theoretical basis. Later work has generally focused on modeling growth conditions for which the Deal Grove model is inadequate. Examples include very thin oxides, oxides grown in mixed ambients, oxides grown on 2D or 3D silicon surfaces and oxides grown on heavily doped substrates. We will discuss these and other models later in this chapter.

There has also been for many years a considerable controversy over which oxidant species diffuse through the SiO₂ to grow new layers of oxide. In the gas phase above the wafer, molecular species (O₂ or H₂O) are present. However, these species could dissociate or even ionize to form O, O⁻, O₂⁻ or many other species once they enter the SiO₂. Some early work [6.2] using an electric field suggested that a charged species was the dominant diffusant. However, later work largely discounted these results and today most workers believe that neutral O₂ and H₂O and/or OH are the dominant species involved in the oxidation process.

The electrical properties of the Si/SiO₂ interface have been studied intensively for more than 40 years. A great deal has been learned about these properties, how they depend on process conditions and how to control them. To first order, the interface is perfect. The densities of defects that are present in modern devices are on the order of 10⁹ - 10¹¹ cm⁻² compared to a silicon surface atom density of about 10¹⁵ cm⁻². Most of the defects that do exist are usually attributed to incompletely oxidized Si atoms or Si atoms with dangling or unsatisfied bonds. However, only about 1 atom in 10⁵ has such a defect.

In 1980, in an effort to unify research in this field, Deal [6.7] suggested the nomenclature shown in Fig. 6.6 to represent the various types of electrical defects that are found experimentally at the Si/SiO₂ interface and in SiO₂ layers. There are four basic types of defects or charges that exist. The first, Q_f, is known as the fixed oxide charge. Experimentally we find that a sheet of positive charge (usually 10⁹ - 10¹¹ cm⁻²) exists in the oxide, very close to the interface. It seems to be located within 2 nm of the interface (perhaps closer) and is likely associated with the transition from Si to SiO₂. Most physical explanations for Q_f suggest that it is due to incompletely oxidized Si atoms that have a net positive charge. Q_f is called the fixed oxide charge because its charge state does not change during normal device operation. It is positive and invariant under normal conditions.

The second type of charged defect present at the Si/SiO₂ interface is Q_{it}, the interface trapped charge. The physical origin of these charges is often suggested to be similar to Q_f. That is, Q_{it} is

likely due to some type of incompletely oxidized silicon atom with unsatisfied or dangling bonds located in the oxide, but very close to the interface. However there is a very important difference between Q_{it} and Q_f . The charge associated with Q_f is fixed and positive. The charge associated with Q_{it} may be positive, neutral or negative, and in fact may change during normal device operation because of the capture of holes or electrons. Hence the name trap associated with Q_{it} . These traps behave very much like the bulk deep level traps we discussed in Chapters 1 and 4 (Fig. 1.27). Energy levels associated with Q_{it} exist throughout the forbidden band, although usually there are more traps at energy levels near the conduction and valence band edges than there are in the middle of the bandgap. Oxidizing a silicon surface usually results in a density of Q_{it} on the order of $10^9 - 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, about the same density as is found for Q_f . In fact it is usually the case that a process that results in a high value of Q_f will also result in a high density of Q_{it} . This correlation is one of the experimental results that suggests a common origin for the two charges.

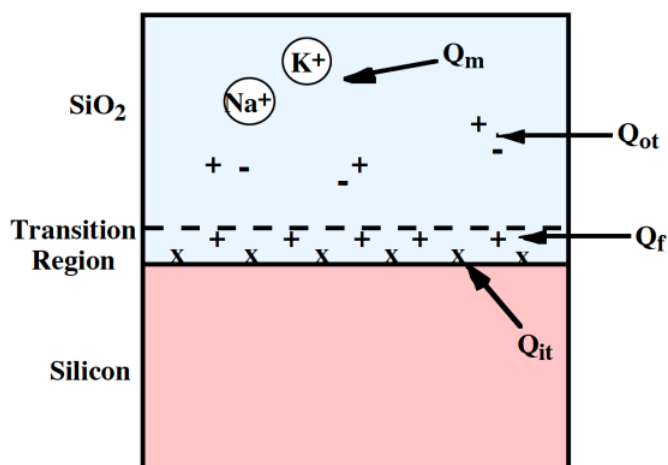


Fig. 6.6: Charges associated with the SiO_2/Si system. (After Deal [6.7]).

The other two types of charges shown in Fig. 6.6 are usually less important today. Q_m is the mobile oxide charge that may be located anywhere in the oxide, and was a serious problem in the 1960s. At that time, it was often the case that MOS structures were unstable after fabrication. We discussed this briefly in Chapter 1 and again in Chapter 4 and observed there that this instability in transistor threshold voltage was traced to the presence of mobile ions like Na^+ and K^+ in the gate oxides - Q_m . With proper attention to cleanliness in wafer fabrication facilities, this problem largely disappeared by the 1970s, although even today it occasionally becomes a problem in manufacturing facilities since ppm concentrations of these mobile ions can cause measurable instabilities. In the example we considered in Chapter 4, we saw that the shift in V_{TH} in MOS devices caused by Na^+ or K^+ is inversely proportional to C_{OX} (Eqn. 4.1). Thus as gate oxide thickness is scaled down, larger Q_m values can be tolerated.

Q_{ot} or oxide trapped charge, which also may be located anywhere in the oxide, is the final experimentally observed charge type in the Si/SiO_2 system. These defects are likely broken Si-O bonds in the bulk of the oxide, well away from the Si/SiO_2 interface. Such bonds can be broken by ionizing radiation or by some of the process steps used in manufacturing ICs today. Plasma etching, for example, exposes oxides to energetic ions, electrons and other neutral species. Ion

implantation is often done through an oxide layer. These and other processes can damage oxides resulting in traps in the bulk oxide - Q_{ot} . Such traps are normally repaired by a high temperature anneal before device fabrication is complete which allows the broken bonds to repair themselves. If they exist in the oxide because they are not fully annealed, or because the device is exposed to ionizing radiation, these traps can capture holes or electrons that may be injected into the oxide during device operation, resulting in trapped charge. Hence the name Q_{ot} .

Q_{ot} has taken on increased importance in recent years because of the high electric fields present in scaled devices. These higher fields result in more energetic or “hot” carriers that can achieve energies high enough to be injected into the gate oxides of modern MOS devices. If oxide traps are present, or if they are created by the energetic carriers themselves, charge trapping can occur. This results in device threshold shifts with time (see Eqn. 4.1) and reliability concerns. A common measure of the quality of a gate insulator is Q_{BD} or the amount of charge that can be passed through the oxide before failure (breakdown) occurs. Charge trapping in SiO_2 insulators is also a major issue in programmable devices like EPROMs in which current is purposely passed through the gate oxide as part of the write operation.

All four of the charges in Fig. 6.6 can have deleterious effects on device operation. As a result, great care is normally taken during fabrication to choose process sequences that will minimize these charges. Generally this is accomplished by high temperature inert anneals in Ar or N_2 towards the end of the process flow, and by a final moderate temperature ($\approx 400^\circ C$) anneal in H_2 or forming gas (N_2/H_2) at the end of the process. We will discuss such anneals and charges more carefully in Section 6.5.13 later in this chapter.

A final point with regard to SiO_2 layers on Si is important. One of the earliest and most important uses of SiO_2 layers was for masking against impurity diffusion. Oxides are still widely used for this purpose today and this use depends fundamentally on the fact that most impurities have much lower diffusivities in SiO_2 than they do in Si. It is reasonably simple to calculate the thickness of an oxide layer needed to successfully mask against a diffusion or ion implantation operation. However, we will defer discussion of these points until Chapters 7 and 8 where we discuss diffusion and ion implantation in detail.

The Appendix contains a number of useful and important properties of three insulators commonly used in silicon technology. SiO_xN_y is an insulator usually formed by exposing an SiO_2 layer to an NH_3 or other nitrogen containing ambient to convert the oxide into an oxynitride. The properties of both oxynitrides and Si_3N_4 vary somewhat with deposition and/or nitridation conditions and will be discussed in more detail in Section 6.5.11 and at the end of the chapter when future trends are discussed.

6.3 Manufacturing Methods and Equipment

Oxidation systems are among the simplest types of semiconductor processing equipment. Conceptually all that is needed, as illustrated in Fig. 6.7, is an oven capable of temperatures from $600 - 1200^\circ C$ and a simple gas distribution system capable of introducing O_2 or H_2O . In practice, such systems are far more complex because of the need for uniformity, reproducibility and cleanliness in the process. Modern furnaces are capable of handling up to several hundred 8" wafers, with a temperature uniformity of $\pm 0.5^\circ C$.

Most such systems in use today are horizontally oriented with the oxidant species introduced at the back end and the wafers at the front. Many recently developed furnaces are vertically