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EXHIBIT
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Correlation between Barrier Width, Barrier Height, and DC Bias Voltage Dependences on the Magnetoresistance Ratio in Ir–Mn Exchange Biased Single and Double Tunnel Junctions

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Dual spin-valve-type double tunnel junctions (DTJs) of Ir–Mn/CoFe/AlO_x/$Co_{90}Fe_{10}$/AlO_x/CoFe/Ir–Mn and spin-valve-type single tunnel junctions (STJs) of Ir–Mn/CoFe/AlO_x/CoFe/Ni–Fe were fabricated using an ultrahigh vacuum sputtering system, conventional photolithography and ion-beam milling. The STJs could be fabricated with various barrier heights by changing the oxidization conditions during deposition and changing the annealing temperature after deposition, while the AlO_x layer thickness remained unchanged. There was a correlation between barrier width, height estimated using Simmons' expressions, and dc bias voltage dependence on the MR ratio. The V_B dependence on the tunneling magnetoresistance (*TMR*) ratio was mainly related to the barrier width, and the decrease in the *TMR* ratio with increasing bias voltage is well explained, taking into account the spin-independent two-step tunneling via defect states in the barrier, as a main mechanism, at room temperature. Under optimized oxidization and annealing conditions, the maximum *TMR* ratio at a low bias voltage, and the dc bias voltage value at which the *TMR* ratio decreases in value by half ($V_{1/2}$) were 42.4% and 952 mV in DTJs, and 49.0% and 425 mV in STJs, respectively.

KEYWORDS: magnetic tunnel junctions, double tunnel junctions, barrier height, barrier width, bias voltage dependence on MR ratio

The discovery of large and reproducible tunneling magnetoresistance (*TMR*) materials[1,2] at room temperature, combined with the progress in lithographic techniques, has lead to renewed research interest in magnetic random access memory (MRAM).[3,4] The high *TMR* signal available, exceeding 40% at room temperature,[3] from single tunnel junction (STJ) devices can be utilized in a cross-point MRAM architecture[3] in which each cell consists of an STJ device connected in series with a silicon diode or field effect transistor (FET) switch. However, the *TMR* ratio decreases with increasing dc bias voltage (V_B),[5] and this decrease in the *TMR* ratio is not desirable for MRAM applications. The loss of the *TMR* ratio with increasing V_B across the junction is an important problem, because the drop in sense voltage for MRAM devices provides the large signal-to-noise ratio. From this standpoint, we have studied a double tunnel junction (DTJ)[6] which has weak V_B dependence on the *TMR* ratio.[7] Many theoretical and experimental studies[5–15] have revealed mechanisms for the loss of the *TMR* ratio with increasing V_B, and many different mechanisms have been proposed. However, experimentally, the relationships between the barrier width and barrier height and V_B dependences to the *TMR* ratio is far from clear, because in many cases, the AlO_x barriers were fabricated by the deposition of Al and subsequently oxidized in the chamber to form the tunnel barriers. In this preparation method, the fabrication of magnetic tunnel junctions (MTJs) with various barrier conditions is difficult, because changing the oxidization conditions during deposition leads to remaining Al metal or oxidization at the ferromagnetic electrode in the interfaces between the tunnel barrier and ferromagnetic electrode. The presence of the Al metal or oxidized ferromagnetic layer apparently influences the behavior of the V_B dependence on the *TMR* ratio,[16] and is not desirable for investigation of the relationship between the barrier width, barrier height and V_B dependence on the *TMR* ratio.

On the other hand, for a method of direct sputtering of the AlO_x layers and subsequent plasma oxidation in the chamber to form the tunnel barriers, Al metal remaining at the AlO_x/ferromagnetic electrode interfaces is not a concern. In STJs and DTJs prepared by the direct sputtering method of AlO_x layers, cross-sectional transmission electron microscopy images revealed the existence of uniform tunneling barriers, and a reproducible *TMR* ratio was observed. This allows us to change the various oxidization conditions.

In this paper, we present the relation between the barrier width, height estimated using Simmons' expressions,[17,18] and V_B dependences on the *TMR* ratio, and the results show a strong correlation. The decrease in the *TMR* ratio with increasing V_B is well explained, taking into account the spin-independent two-step tunneling via defect states in the barrier, as a main mechanism, at room temperature. Moreover, we first report on the spin-dependent tunneling in dual spin-valve-type DTJs. Under optimized conditions, the maximum *TMR* ratio at a low V_B and the dc bias voltage value at which the *TMR* ratio decreases in value by half ($V_{1/2}$) were 42.4% and 952 mV in the DTJs, respectively.

The DTJs of $Ni_{81}Fe_{19}$(5 nm) / Ir–Mn(12 nm) / $Co_{50}Fe_{50}$(3 nm) / AlO_x(1.8 nm) / $Co_{90}Fe_{10}$(3 nm) / AlO_x(2.1 nm) / $Co_{50}Fe_{50}$(3 nm) / Ir–Mn(12 nm) / $Ni_{81}Fe_{19}$(5 nm) were fabricated on oxidized Si substrates by an ultrahigh vacuum sputtering system. The STJs of $Ni_{81}Fe_{19}$(5 nm) / Ir–Mn(12 nm) / $Co_{50}Fe_{50}$(3 nm) / AlO_x(1.8 nm) / $Co_{50}Fe_{50}$(5 nm) / $Ni_{81}Fe_{19}$(15 nm) were also prepared in order to clarify the relation between the barrier width, barrier height, and V_B dependences on the *TMR* ratio. The base pressure was less than 5×10^{-9} Torr. The $Co_{50}Fe_{50}$/$Ni_{81}Fe_{19}$ bilayers in the STJs and the $Co_{90}Fe_{10}$ central layer in the DTJs are designed to switch their magnetic moments at a low field. The AlO_x layers were deposited by direct sputtering with an AlO_x target, and subsequently the plasma oxidized in the chamber to form the tunnel bar-

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riers. The STJs were fabricated with various barrier heights by changing the oxidization conditions (varying the oxidization time between 20 s and 80 s, and varying the RF power for oxidization between 10 W and 30 W) during deposition, and by varying the annealing temperature between 150°C and 325°C, while keeping the AlO_x layer thickness unchanged. The maximum *TMR* ratio and $V_{1/2}$ were observed under the oxidization conditions of 30 W, 80 s and after annealing at about 300°C in the STJs with 1.8 nm AlO_x layer thickness. Under the oxidization conditions of 30 W and 100 s, the presence of an oxidized ferromagnetic electrode was observed by X-ray photoelectron spectroscopy measurement. Therefore, oxidization conditions were varied between 20 s and 80 s, and between 10 W and 30 W. Thermal treatments were carried out in vacuum (less than 1×10^{-6} Torr), for 60 min. A magnetic field of 6500 Oe was applied along the easy direction of magnetization during annealing and furnace cooldown. A photolithographic patterning procedure and ion-beam milling were used to fabricate the tunnel junction devices of $4 \times 4\ \mu m^2$ junction area. A Ti(50 nm)/Au(200 nm) bilayer was used as a contact for the top electrode. The temperature dependence of the *TMR* ratio was measured in the temperature range between 3.5 K and 300 K, in order to clarify the mechanism of V_B dependence on the *TMR* ratio.

Figure 1 shows the barrier height dependence on the *TMR* ratio measured at 3.7 K and 250 K in the STJs. The *TMR* ratio increased with increasing barrier height. The solid line in Fig. 1 represents the calculation result using the free electron model, assuming Fe electrodes.[11] The tunneling currents were calculated on the basis of a Tsu-Esaki-type equation. This suggests that the result is roughly consistent with the free electron model; that is, transmission coefficients of up and down spin depend on the barrier height for the STJs.[19] However, in STJs with low barrier heights, many defects in the barrier would exist, as discussed later. Therefore, for the STJs without defects in the tunnel barrier, the *TMR* ratio with the low barrier height would have the potential to be larger than the experimental data shown in Fig. 1. The inset in Fig. 1 shows the minor hysteresis loops of the MR curves for DTJs after annealing at 325°C, and for STJs after annealing at 300°C. The maximum *TMR* ratio at room temperature was 42.4% and 49% in the DTJs with a $Co_{90}Fe_{10}$ free layer, and in the STJs with a $Co_{50}Fe_{50}/Ni_{81}Fe_{19}$ free layer, respectively. For the STJs with $Co_{50}Fe_{50}$ free and pinned layers, the *TMR* ratio was 66.7% and 49%, respectively, at 4 K and room temperature. (The spin polarization estimated using Jullier's model[20] was 0.5 and 0.44, at 4 K and room temperature, respectively.)

Figures 2(a) and 2(b) show the $V_{1/2}$ dependence on barrier height and width estimated using Simmons' expressions, respectively. There is a strong correlation between $V_{1/2}$ and the barrier width and barrier height. Increasing the applied V_B across the junction, the effective barrier height at the V_B is diminished compared with that at the low V_B. Therefore, the relationship between $V_{1/2}$ and barrier height can be explained, qualitatively, taking into account the results shown in Fig. 1. However, the calculated V_B dependence of the *TMR* ratio, assuming the free electron model, has a weak dependence.[11] Therefore, quantitatively, the V_B dependence on the *TMR* ra-

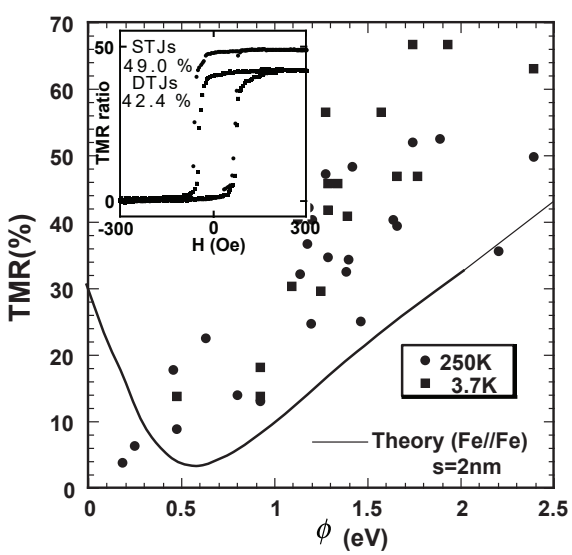

Fig. 1. Barrier height dependence on *TMR* ratio, measured at 3.7 K and 250 K, in STJs. The solid line represents the calculation result using the free electron model, assuming Fe electrodes. Inset shows minor hysteresis loops of magnetoresistance curves in the STJs and DTJs.

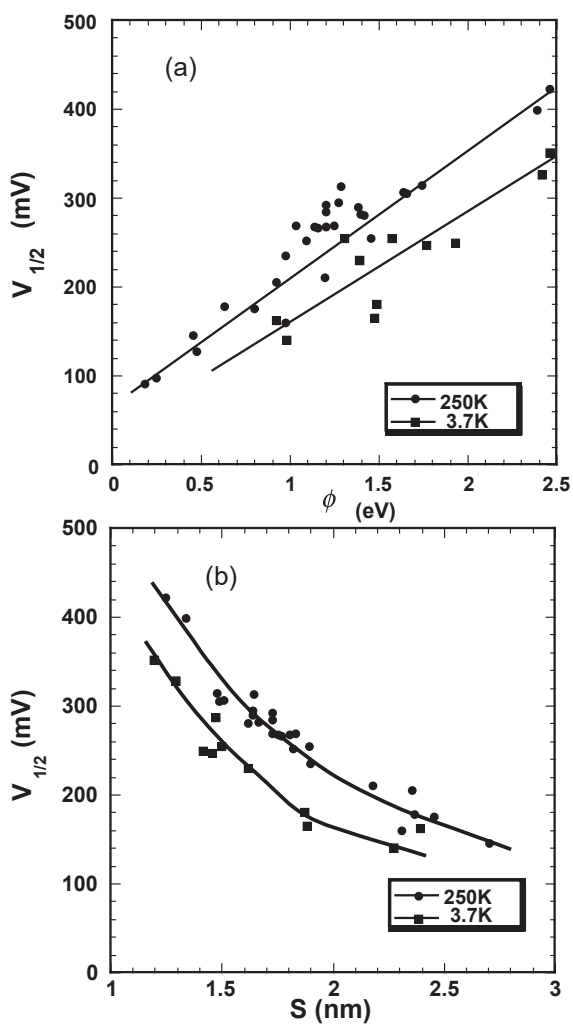

Fig. 2. (a) Barrier height and (b) Barrier width dependence on $V_{1/2}$, measured at 3.7 K and 250 K in STJs. Solid lines are to guide the eye.

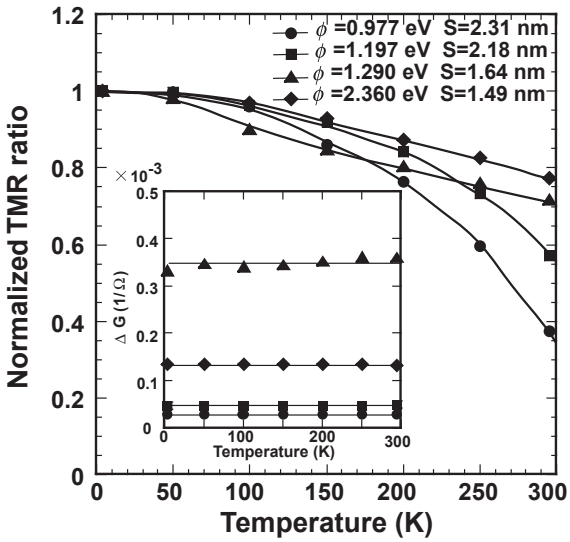

Fig. 3. Temperature dependence on *TMR* ratio. Inset shows temperature dependence on conductance change, ΔG.

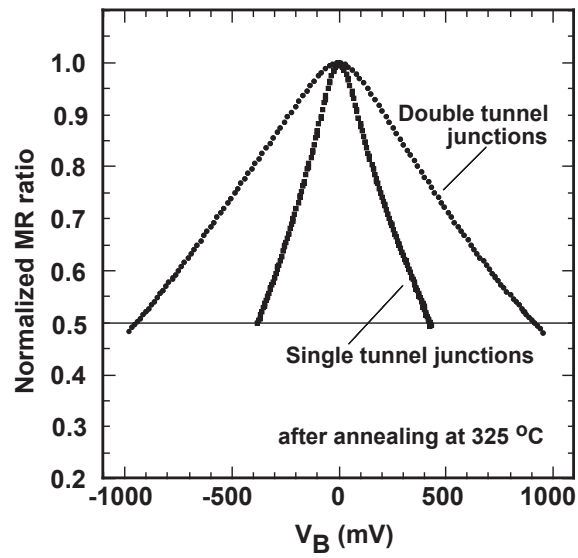

Fig. 4. DC bias voltage dependence on *TMR* ratio in STJs and DTJs fabricated under optimized oxidization and annealing conditions.

tio cannot be explained only by the change in the effective barrier height. Therefore, these results suggest that the V_B dependence of the *TMR* ratio is mainly attributed to the change in the barrier width.

In order to clarify the mechanism of V_B dependence on the *TMR* ratio, the temperature dependences of the *TMR* ratio and conductance change, ΔG, were measured as shown in Fig. 3. As shown in the inset in Fig. 3, ΔG is almost constant in a wide temperature range for the STJs fabricated under various oxidization conditions, whereas the temperature dependence of the normalized *TMR* ratio is significantly correlated with both the barrier width and barrier height.

Total conductance, $G(\theta, T)$ and $\Delta G(T)$, is expressed as[8,20]

$$G(\theta, T) = G_T(T)[1 + P_1(T)P_2(T)\cos\theta] + G_I(T),$$

$$\Delta G(T) = 2G_T(T)P_1(T)P_2(T),$$

where θ is the angle between the magnetization directions ($\theta = 0°$ for parallel and $\theta = 180°$ for antiparallel magnetization), $G_T(T)$ is an elastic tunneling due to the broadening of the Fermi distributions, $G_I(T)$ is the conductance which is independent of the relative orientation of the electrode magnetization, and $P_i(T)$ is the spin polarization with temperature dependence. The conductance change due to the broadening of the Fermi distributions increases with increasing temperature, whereas the term of the spin polarization decreases with increasing temperature. Therefore, the degree of the temperature dependence between the broadening of the Fermi surface and the spin polarization would be compatible with our junctions. The estimated degree of the temperature dependence of $G_T(T)$ using the barrier height estimated from Simmons' expression and the theory $G_T(T) = G_0 CT/\sin(CT)$ (G_0 is constant, $C = 1.387 \times 10^{-4}\,S/(\phi)^{1/2}$), is less than 3% for all STJs. Therefore, the main origin of the temperature dependence of the *TMR* ratio shown in Fig. 3 is the $G_I(T)$, i.e., hopping conductance through defect states. This result is consistent with the barrier width dependence on the *TMR* ratio, as shown in Fig. 2(b). The increase in the defect states with increasing temperature and with increasing barrier width should decrease in both the *TMR* ratio and $V_{1/2}$, taking into account the spin-independent two-step tunneling via defect states in the barrier,[10] as a main mechanism of V_B dependence of the *TMR* ratio. The increase in hopping conductance via defect states is an important mechanism for the loss of the *TMR* ratio and $V_{1/2}$.

Finally, we show the V_B dependence on the *TMR* ratio in STJs and DTJs fabricated under optimized oxidization and annealing conditions. Both STJs and DTJs were fabricated under the same oxidization (30 W, 80 s) and annealing conditions. Data were obtained at room temperature. The *TMR* ratio of STJs decreases rapidly with increasing V_B, compared with that of DTJs. The $V_{1/2}$ is slightly enhanced upon annealing in the region of $T_A < 300°C$, and has a maximum at around 320°C. As shown in Fig. 4, the maximum $V_{1/2}$ is +952 mV, −912 mV for DTJs annealed at 325°C. The maximum $V_{1/2}$ is +425 mV, −378 mV in STJs annealed at 300°C. This appears to suggest that the $V_{1/2}$ in DTJs is much larger than the twofold $V_{1/2}$ in STJs. For DTJs, more complex behavior than sequential tunneling might be considered, as reported in a previous paper.[7] Moreover, the estimated barrier heights for DTJs were about 1.5 times larger than those for STJs deposited under the same conditions, estimated using Simmons' expressions, assuming two identical STJs in series for DTJs. More detailed studies for DTJs are necessary.

In conclusion, dual spin-valve-type DTJs and spin-valve-type STJs were fabricated with various barrier heights and widths. There was a correlation between barrier width, height estimated using Simmons' expressions, and V_B dependence on the *TMR* ratio. The V_B dependence on the *TMR* ratio was mainly related to the barrier width, and the decrease in the *TMR* ratio with increasing V_B can be well explained, taking into account the spin-independent two-step tunneling via defect states in the barrier, as a main mechanism, at room temperature. With optimized oxidization and annealing conditions, the maximum *TMR* ratios at a low bias voltage and $V_{1/2}$ are 42.4% and 952 mV, respectively, in DTJs, and 49.0% and 425 mV, respectively, in STJs.

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