IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

AMAZON.COM, INC. AND AMAZON.COM SERVICES, LLC,

Petitioners,

v.

NOKIA TECHNOLOGIES OY,

Patent Owner.

Case No. IPR2024-01503

U.S. Patent 9,571,833

Declaration of Vivienne Sze

I, Vivienne Sze, declare as follows:

I. INTRODUCTION

1. I have been retained by Amazon.com, Inc. and Amazon.com Services LLC ("Petitioner") as an independent consultant in this proceeding before the United States Patent and Trademark Office ("PTO").

2. I am being compensated at my normal consulting rate of $1200/hour. My compensation is in no way contingent on the nature of my testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

3. I have been asked to provide information regarding the availability of documents uploaded on the Joint Collaborative Team on Video Coding ("JCT-VC") document management site (http://phenix.int-evry.fr/jct/) ("JCT-VC website"), membership information for JCT-VC, including committee rosters and other such information, and the presentations made to the JCT-VC around the 2011 timeframe.

II. BACKGROUND

4. My testimony set forth in this declaration is based on my own personal knowledge and experience. I understand that a copy of my current curriculum vitae, which details my education and professional and academic experience, is attached hereto as Appendix 1.

5. I have been an active member of the JCT-VC since October 2010 and attended every JCT-VC meeting starting from the 3rd HEVC meeting (October 2010 in Guangzhou) until the end of 2012.

6. I am an Associate Professor in the Electrical Engineering and Computer Science Department at the Massachusetts Institute of Technology ("MIT"), where I have taught since 2013. I teach courses on, among other subjects, hardware architecture for deep learning, analysis and design of digital integrated circuits, and digital image processing. I also lead MIT's Energy-Efficient Multimedia Systems Group, which develops and implements algorithms, architectures, circuits, and systems adapted to various applications, including video coding and processing. In 2019, I received the Edgerton Faculty Award for exceptional distinction in teaching, research, and service.

7. I received my Bachelor of Science in Electrical Engineering from the University of Toronto in 2004. I received a Master of Science and a Ph.D. in Electrical Engineering from MIT in 2006 and 2010, respectively. My doctoral thesis, titled Parallel Algorithms and Architectures for Low Power Video Decoding, was awarded the Jin-Au Kong Outstanding Doctoral Thesis Prize in Electrical Engineering at MIT.

8. After receiving my Ph.D. from MIT, I worked for nearly three years at Texas Instruments ("TI"), where I developed algorithms and architectures for

video coding, including HEVC. I was the architect of the HEVC CABAC entropy coding engine in TI's video codec. I also taught several seminars on HEVC at TI offices around the world.

9. I represented Texas Instruments at JCT-VC video coding standardization meetings to develop and standardize HEVC. I led many ad hoc breakout sessions related to entropy coding, chaired the core experiments on coefficient scanning and coding, and over twenty of my contributions were adopted into the HEVC standard.

10. I am the author or co-author of over a half dozen published papers on video coding, including "A Highly Parallel and Scalable CABAC Decoder for Next-Generation Video Coding," ISSCC Dig. Tech. Papers, pp. 126-127 (Feb. 2011); and "A 249Mpixels/s HEVC Video Decoder Chip for Quad Full HD Applications," ISSCC Dig. Tech. Papers, pp. 1533-1536 (Feb. 2013). I am also co-editor of the book "High Efficiency Video Coding (HEVC): Algorithms and Architectures," Integrated Circuits and Systems–Springer (2014). In addition to editing that book, I co-authored a chapter titled "Entropy Coding in HEVC."

11. I served as Session Chair for a special session on "Efficient Design of HEVC Video-Codec Implementations" at 2014 IEEE International Conference on Image Processing (ICIP). Furthermore, I have served as an elected member of two technical committees in the IEEE Signal Processing Society: the Design and

Implementation of Signal Processing Systems committee; and the Image, Video, and Multidimensional Signal Processing committee.

12. I am a named inventor on over two dozen issued patents in the field of video coding.

13. I am not an attorney and offer no legal opinions.

III. PUBLIC AVAILABILITY OF JCT-VC DOCUMENTS

14. Due to my involvement with video coding standardization committees, I gained personal knowledge regarding the procedures for publishing video coding standardization-related documents on the JCT-VC website. As I discuss below, during the 2011 timeframe, I recall that documents uploaded on the JCT-VC website were available for download to at least hundreds of individuals interested in the development of a video coding standard, as of the upload date of the documents on the JCT-VC website. The documents made available in that timeframe include specific JCT-VC documents that I discuss below.

15. For example, as I explain below,

- "Nakamura": Version 4 of the JCTVC-F419 proposal (including Ex-1007, Ex-1008, and Ex-1009) was publicly available for download as of its upload date of July 22, 2011 on the JCT-VC website; and
- "WD4": Version 3 of the JCTVC-F803 document (Working Draft 4) (Ex-1010) was publicly available for download as of its upload date of September 8, 2011 on the JCT-VC website.

16. I downloaded WD4 from the JCT-VC website. Specifically, I downloaded JCTVC-F803-v3.zip from the website, which included JCTVC-F803_d1.doc (Ex-1010). I believe Ex-1010 is a true and accurate copy of WD4. I also downloaded Nakamura from the JCT-VC website. Specifically, I downloaded JCTVC-F419-v4.zip from the website, which included six files: JCTVC-F419.doc (Ex-1007), JCTVC-F419_presentation.pdf (Ex-1009), JCTVC-F419_Proposal1_WD.doc (Ex-1008), JCTVC-F419_Proposal1.xls, JCTVC-F419_Proposal1and2.xls, and JCTVC-F419_Proposal2.xls. I collectively refer to these files as "Nakamura" because they were all part of the Nakamura proposal. I believe Exhibits 1007, 1008, and 1009 are true and accurate copies of the respective files from Nakamura.

17. The JCT-VC was created in the 2010 timeframe to develop the HEVC Standard (formally, ITU-T H.265 | ISO/IEC 23008-2) to replace the then-current AVC Standard (formally, ITU-T H.264 | ISO/IEC 14496-10). *See, e.g.*, Ex-1026 (copy of JCT-VC website describing the JCT-VC that is consistent with its role in the 2011 timeframe), 000001; Ex-1027 ("Purpose");[1] *see also generally* Ex-1028 (Meeting report of the sixth JCT-VC meeting in July, 2011).

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[1] Ex-1027 is a copy of a document obtained from the link "Terms of Reference for Collaborative Team on Video Coding (JCT-VC) Activities" on Ex-1026. Ex-1027 is dated January 2010, and based on my personal knowledge and recollection, describes the terms of reference (including the purpose, parent bodies, scope goals,

18. The JCT-VC included video coding experts from around the world, including people from universities and a wide range of technology companies. The JCT-VC had two parent organizations, ITU-T Study Group 16 (VCEG) and ISO/IEC JTC 1/SC 29/WG 11 (MPEG). *See,* e.g., Ex-1026, 000001; Ex-1027, 000001 ("Parent Bodies"); Ex-1028, 000002 (Section 1.1). The two parent organizations agreed to "Terms of Reference of the Joint Collaborative Team on Video Coding Standard Development" in Kyoto, Japan in January, 2010. *See,* e.g., Ex-1027, 000001.

19. Based on my knowledge and recollection, video coding personnel from the JCT-VC met quarterly for development of the new HEVC Standard, starting in April 2010. *See, e.g.*, Ex-1029 (listing JCT-VC meetings). During these meetings, the JCT-VC considered proposals ("input" documents) submitted prior to the meeting. Ex-1027, 000003 ("Working Methods"); Ex-1028, 000001 ("Approximately 254 people attended the [sixth] JCT-VC meeting, and approximately 700 input documents were discussed.").[2] Proposals in input documents that were agreed upon would be incorporated into a working draft of

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documents and contributions, etc.) of the joint collaborative team on video coding standard development for the JCT-VC that was followed in the 2011 timeframe. Based on my knowledge and recollection, Ex-1027 is a copy of the same document that was available in at least 2011.

[2] Ex-1028 is the Meeting Report of the sixth JCT-VC meeting. Similar meeting reports were prepared and published after each meeting.

the HEVC Standard specification after the meeting (e.g., an "output" document).[3] Ex-1027, 000002 ("Documents and Contributions"). For the 6th JCT-VC meeting in Torino, Italy that took place July 14-22, 2011, the output of that meeting included WD4. Ex 1028, 000001 ("The JCT-VC produced three particularly important output documents from the meeting . . . [including] the HEVC specification Working Draft 4 (WD4)").

20. I personally attended the 6th JCT-VC meeting in Torino, Italy. I personally accessed proposals and other input documents for the Torino meeting and can confirm that they were publicly available to all meeting attendees and via the JCT-VC website at least by the time the meeting took place, on July 14-22, 2011. Based on my review of WD4 and the timestamp of the JCT-VC website (*see infra* §III.A), I believe WD4 was publicly available to all meeting attendees and via the JCT-VC website by at least September 8, 2011.

21. I personally recall that people who were interested in video coding would access proposals and working drafts from the JCT-VC website, including meeting attendees and non-attendees such as graduate students that were interested in video coding.

[3] Proposals needing further consideration were assigned to "'Ad Hoc Groups' (AHGs) to progress the work on particular subject areas." Ex-1028, 000001.

A. Availability on the JCT-VC website

22. From its outset, the JCT-VC had a general policy of making JCT-VC related documents publicly available. Ex-1027, 000002 ("In order to facilitate cross-organisational communication, all input and output documents of the JCT will be public (including the drafts of the coding specification, reference software, and conformance test data)."). In at least the 2011 timeframe, each JCT-VC document was uploaded onto the JCT-VC website such that it was available for download. *Id*. ("Documents and Contributions"); Ex-1028, 000008 ("Communication practices"). Based on my knowledge and recollection, consistent with the general policy of JCT-VC, there were no restrictions for downloading documents uploaded on the JCT-VC website in the 2011 timeframe. In other words, no credentials such as a username or password were required to download documents available on the JCT-VC website in the 2011 timeframe. Moreover, based on my knowledge and recollection, given the prominence of the JCT-VC in the video coding industry, persons interested in tracking the developments of the latest video coding standard would regularly visit the JCT-VC website to ensure that products and services they were developing were consistent with the HEVC Standard under development.

23. Based on my knowledge and recollection, in at least the 2011 timeframe, the process for uploading a document to the JCT-VC website included

first registering a record for the document, the record including the Title (e.g., suggesting the underlying subject matter) and a Source (e.g., authors) of the document. Ex-1030 ("Title" and "Source" columns). As part of this registration process, two unique numbers were assigned to the document and associated with the document record – a JCT-VC number and an MPEG number. The JCT-VC number included a letter prefix that corresponded to the "Unique Serial Letter" for the respective meeting to which the document relates. Ex-1029 ("Unique Serial Letter" column); Ex-1030 ("JCT-VC number" and "MPEG number" columns).

24. Based on my knowledge and recollection, since at least 2011, the JCT-VC website was and continues to be organized in a hierarchical manner categorized by the JCT-VC meeting numbers. By navigating to any meeting, a user could view the documents related to the meeting. Once the user navigated to the meeting of interest, the list of documents relating to the meeting included information regarding the documents such as the Title and the Source. Accordingly, users could view and download a document based on the information regarding the document. For example, the document register of the 6th JCT-VC meeting in Torino could be viewed by navigating the web browser as follows: JCT-VC website → "All Meetings" → Meeting Number 6 ("Torino"). Ex-1029; Ex-1030. In fact, based on my knowledge and recollection, a list of submitted documents is included as Annex A in the JCT-VC meeting reports. *See, e.g.*, Ex-

1028, 000003 ("The documents of the JCT-VC meeting are listed in Annex A of this report. The documents can be found at [the JCT-VC website.]"), 000191-253 (Annex A).

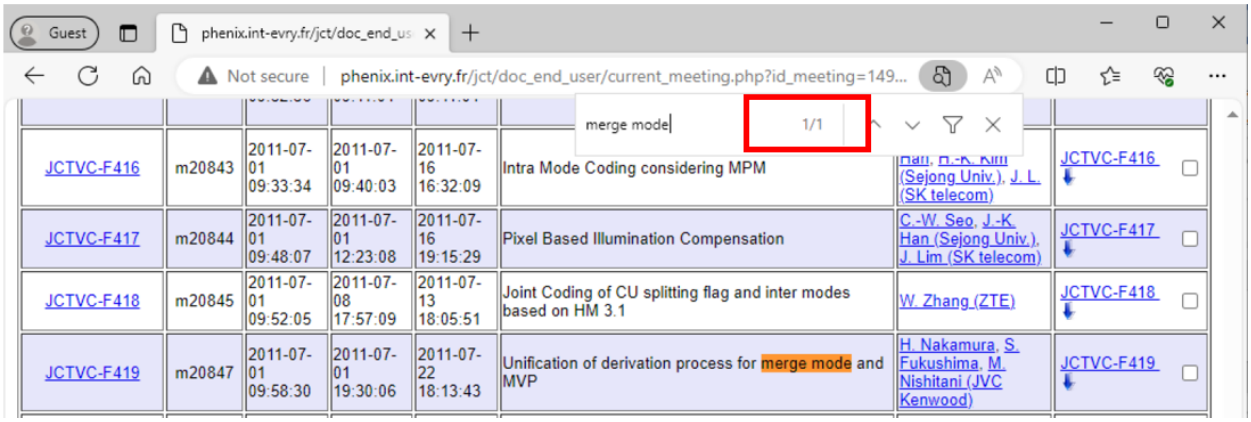
25. Moreover, the meeting page on the JCT-VC website included a search functionality with search fields including title and author. Ex-1030 (the "Search document" feature). In the case of the 6th JCT-VC meeting in Torino, there were about 780 documents listed on the Torino meeting site's document register. The user of the JCT-VC website could have performed searches based on title and author to locate documents among them. I confirmed this by accessing the Torino Meeting Document Register available on the JCT-VC website, which was also available in kind in September 2011 after the Torino meeting. Ex-1030 (document register for the Torino meeting). An interested person of ordinary skill in the art also had the ability to and could have readily located Nakamura and WD4 on the JCT-VC meeting page by using the search functionality typically provided with a web browser at that time to search the JCT-VC meeting page for the Torino meeting in September 2011.

1. Searching for Nakamura on JCT-VC website

26. Based on my knowledge and personal experience, merge mode and MVP (motion vector predictor) were common and well-known concepts in the 2011 timeframe. Because the JCT-VC website had search capability in September

2011, a person of ordinary skill interested in the common video coding concepts understood and would have expected to find, and could have found, the "JCTVC-F419" entry corresponding to Nakamura using such terms as "merge mode" and "MVP." Because of the documents that were available on the site in September 2011 (which I was aware of at that time), performing such a search at that time would have narrowed down the results to dozens of or even fewer documents. As shown in Ex-1030, as well as Ex-1031 and Ex-1032 (search screens on the document register web page), at the time, only one document on the site included the term "merge mode" in its title, while the term "MVP" appeared 20 times in document titles.

Document including the term "merge mode":



JCTVC-F416	m20843	2011-07-01 09:33:34	2011-07-01 09:40:03	2011-07-16 16:32:09	Intra Mode Coding considering MPM	Han, H.-K. Kim (Sejong Univ.), J. L. (SK telecom)	JCTVC-F416
JCTVC-F417	m20844	2011-07-01 09:48:07	2011-07-01 12:23:08	2011-07-16 19:15:29	Pixel Based Illumination Compensation	C.-W. Seo, J.-K. Han (Sejong Univ.), J. Lim (SK telecom)	JCTVC-F417
JCTVC-F418	m20845	2011-07-01 09:52:05	2011-07-08 17:57:09	2011-07-13 18:05:51	Joint Coding of CU splitting flag and inter modes based on HM 3.1	W. Zhang (ZTE)	JCTVC-F418
JCTVC-F419	m20847	2011-07-01 09:58:30	2011-07-01 19:30:06	2011-07-22 18:13:43	Unification of derivation process for merge mode and MVP	H. Nakamura, S. Fukushima, M. Nishitani (JVC Kenwood)	JCTVC-F419

Ex-1031, 000001 (annotations added).

Documents including the term "MVP":

Not secure | phenix.int-evry.fr/jct/doc_end_user/current_meeting.php?id_meeting=149...

mvp 16/20

JCTVC-F416	m20843	2011-07-01 09:33:34	2011-07-01 09:40:03	2011-07-16 16:32:09	Intra Mode Coding considering MPM	Han, H.-K. Kim (Sejong Univ.), J. L. (SK telecom)	JCTVC-F416
JCTVC-F417	m20844	2011-07-01 09:48:07	2011-07-01 12:23:08	2011-07-16 19:15:29	Pixel Based Illumination Compensation	C.-W. Seo, J.-K. Han (Sejong Univ.), J. Lim (SK telecom)	JCTVC-F417
JCTVC-F418	m20845	2011-07-01 09:52:05	2011-07-08 17:57:09	2011-07-13 18:05:51	Joint Coding of CU splitting flag and inter modes based on HM 3.1	W. Zhang (ZTE)	JCTVC-F418
JCTVC-F419	m20847	2011-07-01 09:58:30	2011-07-01 19:30:06	2011-07-22 18:13:43	Unification of derivation process for merge mode and MVP	H. Nakamura, S. Fukushima, M. Nishitani (JVC Kenwood)	JCTVC-F419

Ex-1032, 000001 (annotations added).

27. To confirm my understanding, I performed a search using the JCT-VC website's search functionality, which was the same functionality available in September 2011. Ex-1033 shows the search results for the term "merge mode" in the Title search option for the document register for the Torino meeting. As shown, only one document resulted from the search, the one document being the JCTVC-F419 document (including its version 4, i.e., Nakamura).

Search document

Title merge mode Number

Author Search Clear Search

Torino Meeting - Document Register

JCT-VC number	MPEG number	Created	First Upload	Last upload	Title	Source	Download
JCTVC-F419	m20847	2011-07-01 09:58:30	2011-07-01 19:30:06	2011-07-22 18:13:43	Unification of derivation process for merge mode and MVP	H. Nakamura, S. Fukushima, M. Nishitani (JVC Kenwood)	JCTVC-F419
							Download

Register a new document

Ex-1033, 000001.

28. Similarly, Ex-1034 shows the search results for the term "MVP" in the document register for the Torino meeting, which shows that 19 documents resulted from that search, including the JCTVC-F419 document (including its version 4, i.e., Nakamura). The same listings and search results would have been produced based on these searches had they been performed in September 2011 because the same information was available at that time, and the same search functionality was available on the JCT-VC website at that time.

29. Additionally, since all meeting documents appear on the same page, a POSITA could have easily located Nakamura using commonly-available browser search functionality (e.g., control-F) to search for terms as explained above. I performed a search using the browser search functionality, which was also available in September 2011. The results confirmed the understanding above. *See* Ex-1031; Ex-1032.

30. Therefore, this exercise confirms my recollection and understanding that in September 2011, an interested person of ordinary skill in the art also had the ability to and could have located Nakamura on the JCT-VC meeting page by reviewing the document list or using the search functionalities provided by the JCT-VC website or the web browser at that time.

2. Searching for WD4 on JCT-VC website

31. Based on my personal experience and recollection of interactions with persons skilled in the art who were interested in high efficiency video coding technologies in the 2011 timeframe, such persons knew and appreciated in 2011 (including September-November 2011) that the document best representing the current status and details of the HEVC standardization process was the working draft. Because the JCT-VC website had search capability in September 2011, such person(s) understood and would have expected to find, and could have found, the working draft for the HEVC standard at that time by using the search capabilities of the JCT-VC website, for example using common terms such as "working draft," "draft," or "High Efficiency Video Coding"/"High-Efficiency Video Coding" or variants thereof within the meeting page to locate a working draft document.

32. Because of the documents that were available on the site in September 2011 (which I was aware of at that time), performing such a search at that time would have narrowed down the results to a handful of or even fewer documents. As shown in Ex-1030, at the time, only one document on the site included terms like "working draft" or "High-Efficiency Video Coding" in its title, and only two documents included the term "video coding" in the titles. *Id.* The same listing was available on the JCT-VC website in September 2011.

Documents including the term "Working Draft":

JCTVC-F803	m21449	2011-07-28 11:38:31	2011-08-09 10:14:29	2011-11-20 18:51:47	WD4: Working Draft 4 of High-Efficiency Video Coding	B. Bross, W.-J. Han, J.-R. Ohm, G. J. Sullivan, T. Wiegand (Editors)	JCTVC-F803 ☐

Documents including the term "high-efficiency video coding":

JCTVC-F803	m21449	2011-07-28 11:38:31	2011-08-09 10:14:29	2011-11-20 18:51:47	WD4: Working Draft 4 of High-Efficiency Video Coding	B. Bross, W.-J. Han, J.-R. Ohm, G. J. Sullivan, T. Wiegand (Editors)	JCTVC-F803 ☐

Documents including the term "video coding":

JCTVC-F800	m21451	2011-08-02 10:45:19	2011-11-18 02:20:38	2011-11-18 02:20:38	Meeting report of the sixth meeting of the Joint Collaborative Team on Video Coding (JCT-VC), Torino, IT, 14-22 July 2011	G. J. Sullivan, J.-R. Ohm (JCT-VC chairs)	JCTVC-F800 ☐
JCTVC-F802	m21450	2011-07-29 20:57:51	2011-10-04 20:32:17	2011-10-04 20:32:17	HM4: HEVC Test Model 4 Encoder Description	K. McCann, S. Sekiguci, B. Bross, W.-J. Han (Editors)	JCTVC-F802 ☐

JCTVC-F803	m21449	2011-07-28 11:38:31	2011-08-09 10:14:29	2011-11-20 18:51:47	WD4: Working Draft 4 of High-Efficiency Video Coding	B. Bross, W.-J. Han, J.-R. Ohm, G. J. Sullivan, T. Wiegand (Editors)	JCTVC-F803 ☐

Ex-1030, 000048-49 (annotations added).

33. To confirm my understanding, I performed a search using the JCT-VC website's search functionality, similar to what I did for Nakamura. Ex-1035 shows the search results for the term "working draft" in the Title search option for the document register for the Torino meeting. As shown, only one document resulted from the search, the one document being Working Draft 4 (including version 3 of Working Draft 4, i.e., WD4).

Search document

Title: working draft Number:
Author: Search Clear Search

Torino Meeting - Document Register

JCT-VC number	MPEG number	Created	First Upload	Last upload	Title	Source	Download
JCTVC-F803	m21449	2011-07-28 11:38:31	2011-08-09 10:14:29	2011-11-20 18:51:47	WD4: Working Draft 4 of High-Efficiency Video Coding	B. Bross, W.-J. Han, J.-R. Ohm, G. J. Sullivan, T. Wiegand (Editors)	JCTVC-F803
							Download

Register a new document

Ex-1035, 000001.

34. Similarly, Ex-1036 shows search results for the term "high-efficiency video coding" in the document register for the Torino meeting, where only one document resulted from that search, again the one document being Working Draft 4 (including version 3 of Working Draft 4, i.e., WD4). Also, when I searched the Torino meeting document register using the term "draft," only two documents were provided in the search results, including Working Draft 4 (including version 3 of Working Draft 4, i.e., WD4). Ex-1037 (showing search results for "draft" in the document register for the Torino meeting). The same listings and search results would have been produced based on these searches had they been performed in September 2011 because the same information was available at that time, and the same search functionality was available on the JCT-VC website at that time. I also

performed searches using the search functionality provided by the web browser similar to what I did for Nakamura, which likewise located WD4 in the list of documents on the meeting page. Therefore, this exercise confirms my recollection and understanding that in September 2011, an interested person of ordinary skill in the art also had the ability to and could have located WD4 on the JCT-VC meeting page by reviewing the document list or using the search functionalities provided by the JCT-VC website or the web browser at that time.

3. Accessing Nakamura and WD4

35. As noted in the JCT-VC Terms of Reference, "[e]very contribution document to a meeting of the JCT should be registered in the document registry and uploaded to the electronic archive several days in advance of the meeting, to ensure that it is available for review by other participants." Ex-1027, 000002. Meeting notes were kept for each JCT-VC meeting as a meeting report. For the 6th JCT-VC meeting, those notes were recorded in document number JCTVC-F800. *See generally* Ex-1028.

36. Based on my knowledge and recollection, in at least 2011, to view the different versions available for a document and download one or more versions, the user would click on the JCT-VC document number. This would lead the user to the "Document information" webpage for that document. *See, e.g.*, Ex-1038, 000001 ("Document information" webpage of JCTVC-F419); Ex-1039, 000001

("Document information" webpage of JCTVC-F803 (Working Draft 4))[4]. For instance, as seen on the "Document information" web page of JCTVC-F419 attached as Ex-1038, version 4 of JCTVC-F419 (Nakamura) has an upload date of July 22, 2011.

Preview document **JCTVC-F419** for **Torino** meeting (MPEG number m20847)

Document Information

Submitted by	Hiroya Nakamura	
Title	Unification of derivation process for merge mode and MVP	**Associated Resources**
Authors	H. Nakamura S. Fukushima M. Nishitani (JVC Kenwood)	
Organizations		
Abstract		
Related Contributions		
AhG		
Sub Group	JCT-VC	
Group	MPEG-H	
Standard		
Activity		
Document	JCTVC-F419 (version 1 - date 2011-07-01 19:30:06) JCTVC-F419 (version 2 - date 2011-07-16 08:21:24) JCTVC-F419 (version 3 - date 2011-07-17 13:27:20) JCTVC-F419 (version 4 - date 2011-07-22 18:13:43) upload document	

[4] The conventional way to keep track of the different versions of a JCT-VC working draft on the JCT-VC website was to append a suffix "dx" to the document name on the top-right of the cover page, with x=0 for version 1, x=1 for version 2, and so on. However, if a particular version was rejected by a chair and thus not available online, then the value of x would continue to be incremented relative to the most recent version that was uploaded. As seen in Ex-1039, there is no version 1 for JCTVC-F803 as it was rejected. Ex-1039, 000001. Accordingly, version 2 is entitled "JCTVC_F803_d0," the subject version 3 is entitled "JCTVC_F803_d1," and version 4 is entitled "JCTVC_F803_d2."

Ex-1038, 000001 (annotations added).

37. As seen on the "Document information" web page of JCTVC-F803 attached as Ex-1039, version 3 of JCTVC-F803, i.e., WD4, has an upload date of September 8, 2011.

Preview document **JCTVC-F803** for **Torino** meeting (MPEG number m21449)

Document Information

Submitted by	Benjamin Bross	
Title	WD4: Working Draft 4 of High-Efficiency Video Coding	**Associated Resources**
Authors	B. Bross W.-J. Han J.-R. Ohm G. J. Sullivan T. Wiegand (Editors)	
Organizations		
Abstract		
Related Contributions		
AhG		
Sub Group	JCT-VC	
Group	MPEG-H	
Standard		
Activity		
Document	The document was rejected by the Chair. JCTVC-F803 (version 2 - date 2011-08-09 20:57:27) JCTVC-F803 (version 3 - date 2011-09-08 19:00:16) JCTVC-F803 (version 4 - date 2011-10-04 13:26:19) JCTVC-F803 (version 5 - date 2011-10-08 03:43:19) JCTVC-F803 (version 6 - date 2011-10-22 05:04:49) JCTVC-F803 (version 7 - date 2011-10-28 11:51:18) JCTVC-F803 (version 8 - date 2011-11-20 18:51:47) upload document	

Ex-1039, 000001 (annotations added).

IV. Conclusion

38. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true,

and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on March 21, 2024.

By:

Vivienne Sze

Vivienne Sze

APPENDIX 1: CURRICULUM VITAE OF VIVIENNE SZE

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www.rle.mit.edu/eems/

VIVIENNE SZE

EDUCATION

MASSACHUSETTS INSTITUTE OF TECHNOLOGY Cambridge, MA, United States
Ph.D. in Electrical Engineering (June 2010), ***Jin-Au Kong Outstanding Doctoral Thesis Prize at MIT***
Master of Science in Electrical Engineering (June 2006)

UNIVERSITY OF TORONTO Toronto, ON, Canada
Bachelor of Applied Science in Electrical Engineering (June 2004), ***Ranked 1st/130***

WORK EXPERIENCE

MASSACHUSETTS INSTITUTE OF TECHNOLOGY Cambridge, MA
Department of Electrical Engineering and Computer Science
Associate Professor, July 2017 – present, *Assistant Professor* (Aug. 2013 – June 2017)

- Lead the *Energy-Efficient Multimedia Systems* Group on the joint design of algorithms, architectures, circuits, and systems to enable optimal tradeoffs between power, speed, and quality of result. Applications include computer vision, autonomous navigation, machine learning, video compression, and image processing.
- ***Received the Edgerton Faculty Award for exceptional distinction in teaching, research, and service; awarded to one member of the MIT junior faculty per year:*** http://ir.mit.edu/harold-e-edgerton-faculty-achievement-award
- Teaching: 6.825 Hardware Architecture for Deep Learning; 6.374 Analysis & Design of Digital Integrated Circuits; 6.344 Digital Image Processing; 6.003 Signal Processing; 6.01 Intro to EECS I

TEXAS INSTRUMENTS INC. Dallas, TX
Systems and Applications R&D – Multimedia Signal Processing Lab / Systems Architectures Lab
Member of Technical Staff, Sept. 2010 – July 2013

- Designed low power algorithms and architectures for the High Efficiency Video Coding (HEVC) standard; evaluated and optimized trade-off between coding efficiency and hardware complexity (e.g., area, memory requirements and throughput); ***over 24 patents issued*.**
- Represented TI at the JCT-VC international video coding standardization meetings to develop HEVC; held several leadership roles (e.g., CE coordinator & ad hoc group co-chair); 100+ technical contributions and 20+ adoptions into standard. *The HEVC standard is supported on 78% of the 2 billion iPhones and 57% of the 2 billion Android phones around the world.* ***JCT-VC team received the Primetime Engineering Emmy Award for developing HEVC.***
- Recognized HEVC expert within TI; gave seminars at TI worldwide (Dallas, Bangalore, Shanghai).
- Architect for the HEVC CABAC entropy coding engine in TI's video codec.
- Supervised Ph.D. interns across multiple domains (e.g., video coding, computational imaging).

MASSACHUSETTS INSTITUTE OF TECHNOLOGY Cambridge, MA
Advisor: *Prof. Anantha Chandrakasan*
Research Assistant, Sept. 2004 – June 2010

- *Ph.D.:* Parallel Algorithms and Architectures for Low Power Video Decoding ***(Outstanding Doctoral Thesis Prize)***
  Low Power H.264/AVC Decoder ASIC: Designed and taped-out a 0.7-V H.264/AVC decoder ASIC that consumes under 2mW for HD decode at 30 fps (over 6x lower power than state-of-the-art). *Joint work with Daniel Finchelstein*
  Next Generation Video Coding Standard: Developed a highly parallel video coding algorithm, the Massively Parallel CABAC (MP-CABAC), that enables scalability between low power consumption and high performance (e.g., Ultra-HD) for the next gen. video coding standard; selected techniques adopted into HEVC; Taped-out a high-performance ASIC to demonstrate the MP-CABAC algorithm.
- *Masters:* Designed a 0.4-V 100-Mbps baseband processor for UWB communications.

AWARDS AND HONORS

- University of Toronto Engineering Mid-Career Achievement Award (2021)
- ACM-W Rising Star Award for research that had significant impact on the computing discipline (2020)
- Edgerton Faculty Award in recognition of exceptional distinction in teaching, in research, and in service (2019)
- Facebook Faculty Award (2018)
- Qualcomm Faculty Award (2017, 2018)
- Part of JCT-VC team that received the Primetime Engineering Emmy Award for the development of HEVC (2017)
- Google Faculty Research Award (2016, 2018)
- AFOSR Young Investigator Program Award (2016)

- 3M Non-Tenured Faculty Award (2016)
- DARPA Young Faculty Award (2014)
- Jonathan Allen Early Faculty Award (2013)
- Emanuel Landsman Career Development Chair (2013)
- Selected by IEEE-USA as one of the "New Faces of Engineering" which recognizes accomplishments of young engineers by highlighting their engineering contributions and impact on society (2012)

Academic Excellence

- Jin-Au Kong Outstanding Doctoral Thesis Prize for best Ph.D. thesis in EE at MIT for thesis entitled "Parallel Algorithms and Architectures for Low Power Video Decoding" (2011)
- **First Place Standing** for all four years in Electrical Engineering at the University of Toronto: Adel S. Sedra Gold Medal, W.S. Wilson Medal, and Henry G. Acres Medal (2004)

Selected Publications *(Recipients of Best Paper Awards as well as highlighted or popular papers)*

- A. Suleiman, Z. Zhang, L. Carlone, S. Karaman, V. Sze, "Navion: A Fully Integrated Energy-Efficient Visual-Inertial Odometry Accelerator for Autonomous Navigation of Nano Drones," *IEEE Symposium on VLSI Circuits (VLSI-Circuits)*, 2018. ***Best Student Paper Award and highlighted in MIT Technology Review*** https://bit.ly/2OTPo6x
- V. Sze, Y.-H. Chen, J. Emer, A. Suleiman, Z. Zhang, "Hardware for Machine Learning: Challenges and Opportunities," *IEEE Custom Integrated Circuits Conference (CICC)*, Invited Paper, May 2017. ***Outstanding Invited Paper Award***
- Y.-H. Chen, J. Emer, V. Sze, "Eyeriss: A Spatial Architecture for Energy-Efficient Dataflow for Convolutional Neural Networks," *International Symposium on Computer Architecture (ISCA),* 2016. ***Selected for IEEE Micro's Top Picks special issue on "most significant papers in computer architecture based on novelty and long-term impact" in 2016; Selected for ISCA-50 Retrospective which highlights significant and often memorable papers in 1996 - 2020***
- Y.-H. Chen, T. Krishna, J. Emer, V. Sze, "Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks," *ISSCC Dig. Tech.* 2016. ***2nd most cited ISSCC paper of all time (out of 18,000+) and highlighted in MIT Technology Review*** https://bit.ly/2OTPo6x
- Y.-H. Chen, T. Krishna, J. Emer, V. Sze, "Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks," *IEEE Journal of Solid-State Circuits,* 2017. ***5th most cited JSSC paper of all time (out of 14,000+)***
- V. Sze, Y.-H. Chen, T.-J. Yang, J. Emer, "Efficient Processing of Deep Neural Networks: A Tutorial and Survey," *Proceedings of the IEEE (PIEEE)*, December 2017. ***31st most cited PIEEE paper of all time (out of 19,000+)***
- C.-T. Huang, M. Tikekar, C. Juvekar, V. Sze, A. P. Chandrakasan, "A 249Mpixels/s HEVC Video Decoder Chip for Quad Full HD Applications," *ISSCC Dig. Tech. Papers*, pp. 1533-1536, Feb. 2013. ***World's first published H.265/HEVC chip***
- V. Sze, A. P. Chandrakasan, "A Highly Parallel and Scalable CABAC Decoder for Next-Generation Video Coding," *ISSCC Dig. Tech. Papers*, pp. 126-127, February 2011. ***Highlighted in EETimes*** https://bit.ly/2JGmirz

PROFESSIONAL SERVICES

- Systems Program Chair (2020), Program Committee (2019), Board (2020 – 2023), *MLSys Conference*
- Program Committee (Machine learning and AI), *International Solid-State Circuits Conference* (2020 – 2021)
- Technical Program Committee, *IEEE Symposium on VLSI Circuits* (2016 – 2019)
- Member at Large*, IEEE Solid-State Circuit Society (SSCS) Advisory Committee* (2018 – 2020)
- SSCS Distinguished Lecturer (2018 – 2019)
- ISSCC Challenges and Opportunities Committee (2018 – 2019)
- Program Committee, *IEEE/ACM International Symposium on Microarchitecture (MICRO)* (2017, 2018)
- Guest Editor for special issue on "Efficient HEVC Implementations" in *IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)*
- Session Chair for special session on "Efficient Design of HEVC Video-Codec Implementations" at *2014 IEEE International Conference on Image Processing (ICIP)*
- Elected Member of the *Design and Implementation of Signal Processing Systems* Technical Committee in the IEEE Signal Processing Society (2014 – 2016); Elected Member of the *Image, Video, and Multidimensional Signal Processing* Technical Committee in the IEEE Signal Processing Society (2014 – 2016)
- Invited reviewer for journals and publications from *IEEE Computer Society* (ISCA, MICRO, HPCA, CAL, TACO), *IEEE Circuits and Systems Society* (TCSVT, TCAS, TVLSI, ISCAS), *IEEE Signal Processing Society* (TIP, ICIP, ICASSP, SiPS) and *IEEE Solid-State Circuits Society* (JSSC, ISSCC, VLSI, CICC)

PUBLICATIONS

Journal Articles=29; Conference/Workshop Proceedings=64; Books/Chapters=2/3; Patents Issued=50; Keynotes/Invited Talks: 100+; Complete list of publications at https://scholar.google.com/citations?user=hNWGC5QAAAAJ&hl=en

Journal and Magazine Articles

- P. Z. X. Li, S. Karaman, **V. Sze**, "GMMap: Memory-Efficient Continuous Occupancy Map Using Gaussian Mixture Model," *IEEE Transactions on Robotics (TRO)*, Vol. 40, pp. 1339 – 1355, January 2024
- H.-Y. Lai, C. Sodini, **V. Sze**, T. Heldt, "Individualized Tracking of Neurocognitive-State-Dependent Eye-Movement Features Using Mobile Devices," *Proceedings of the ACM on Interactive, Mobile, Wearable and Ubiquitous Technologies (IMWUT)*, vol. 7, no. 1, March 2023
- S. Sudhakar, **V. Sze**, S. Karaman, "Data Centers on Wheels: Emissions from Computing Onboard Autonomous Vehicles," *IEEE Micro (Special Issue on Environmentally Sustainable Computing*, vol. 43, no. 1, pp. 29 – 39, January/February 2023
- H.-Y. Lai, G. Saavedra Peña, C. Sodini, T. Heldt, **V. Sze**, "App-based saccade latency and directional error determination across the adult age spectrum," *IEEE Transactions on Biomedical Engineering (TBME),* vol. 69, no. 2, pp. 1029-1039, February 2022
- L. Bernstein, A. Sludds, R. Hamerly, **V. Sze**, J. Emer, D. Englund, "Freely-scalable, reconfigurable optical hardware for deep learning," *Scientific Reports*, vol. 11, no. 3144, February 2021
- **V. Sze**, Y.-H. Chen, T.-Y. Yang, J. S. Emer, "How to Evaluate Deep Neural Network Processors: TOPS/W (Alone) Considered Harmful," *IEEE Solid-State Circuits Magazine*, vol. 12, no. 3, pp. 28-41, Summer 2020
- Z. Zhang, T. Henderson, S. Karaman, **V. Sze**, "FSMI: Fast computation of Shannon Mutual Information for information-theoretic mapping," *International Journal of Robotics Research (IJRR),* Vol. 39, No. 9, pp. 1155-1177, August 2020
- J. Noraky, **V. Sze**, "Low Power Depth Estimation of Rigid Objects for Time-of-Flight Imaging," *IEEE Transactions on Circuits and Systems for Video Technology (TCSVT),* Vol. 30, No. 6, pp. 1524-1534, June 2020
- H.-Y. Lai, G. Saavedra Peña, C. Sodini, **V. Sze**, T. Heldt, "Measuring Saccade Latency Using Smartphone Cameras," *IEEE Journal of Biomedical and Health Informatics (JBHI),* Vol. 24, No. 3, pp. 885-897, March 2020
- Y.-H. Chen, T.-J Yang, J. Emer, **V. Sze**, "Eyeriss v2: A Flexible Accelerator for Emerging Deep Neural Networks on Mobile Devices," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 9, No. 2, pp. 292-308, June 2019
- A. Suleiman, Z. Zhang, L. Carlone, S. Karaman, **V. Sze**, "Navion: A 2mW Fully Integrated Real-Time Visual-Inertial Odometry Accelerator for Autonomous Navigation of Nano Drones," *IEEE Journal of Solid-State Circuits VLSI Symposia Special Issue*) Vol. 54, No. 4, April 2019
- M. Tikekar, **V. Sze**, A. P. Chandrakasan, "A Fully-Integrated Energy-Efficient H.265/HEVC Decoder With eDRAM for Wearable Devices," *IEEE Journal of Solid-State Circuits (JSSC),* Vol. 53, No. 8, pp. 2368-2377, August 2018
- **V. Sze**, Y.-H. Chen, T.-J. Yang, J. Emer, "Efficient Processing of Deep Neural Networks: A Tutorial and Survey," *Proceedings of the IEEE,* vol. 105, no. 12, pp. 2295-2329, December 2017
- **V. Sze**, "Designing Hardware for Machine Learning: The Important Role Played by Circuit Designers," *IEEE Solid-State Circuits Magazine (Invited)*, vol. 9, no. 4, pp. 46-54, Fall 2017
- Y.-H. Chen, J. Emer, **V. Sze**, "Using Dataflow to Optimize Energy Efficiency of Deep Neural Network Accelerators," *IEEE Micro's Top Picks from the Computer Architecture Conferences*, May/June 2017
- A. Suleiman, Z. Zhang, **V. Sze**, "A 58.6mW 30fps Real-Time Programmable Multi-Object Detection Accelerator with Deformable Parts Models on Full HD 1920×1080 Videos," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 52, No. 3, pp. 844-855, March 2017
- Y.-H. Chen, T. Krishna, J. Emer, **V. Sze**, "Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks," *IEEE Journal of Solid-State Circuits (ISSCC Special Issue),* Vol. 52, No. 1, pp. 127-138, January 2017
- A. Suleiman, **V. Sze**, "An Energy-efficient Hardware Implementation of HOG-based Object Detection at 1080HD 60 fps with Multi-scale Support," *Journal of Signal Processing Systems (Invited – SiPS Special Issue),* December 2015
- Y.-H. Chen, **V. Sze**, "A Deeply Pipelined CABAC Decoder for HEVC Supporting Level 6.2 High-tier Applications," *IEEE Transactions on Circuits and Systems for Video Technology,* Vol. 25, No. 5, May 2015
- M. Tikekar, C. -T. Huang, C. Juvekar, **V. Sze**, A. Chandrakasan, "A 249 MPixel/s HEVC Video-Decoder Chip for 4K Ultra HD Applications," *IEEE Journal of Solid-State Circuits (ISSCC Special Issue),* Vol. 49, No. 1, pp. 61–72, January 2014
- M. E. Sinangil, **V. Sze**, M. Zhou, A. P. Chandrakasan, "Cost and Coding Efficient Motion Estimation Design Considerations for High Efficiency Video Coding (HEVC) Standard," *IEEE Journal of Selected Topics in Signal Processing*, Vol. 7, No. 6, pp. 1017 – 1028, December 2013
- M. Budagavi, A. Fuldseth, G. Bjontegaard**, V. Sze**, M. Sadafale, "Core Transform Design in the High Efficiency Video Coding (HEVC) Standard," *IEEE Journal of Selected Topics in Signal Processing*, Vol. 7, No. 6, pp. 1029–1041, December 2013
- **V. Sze**, M. Budagavi, "High Throughput CABAC Entropy Coding for HEVC," *IEEE Transactions on Circuits and Systems for Video Technology*, Vol. 22, No. 12, pp. 1778-1791, December 2012
- **V. Sze**, A. P. Chandrakasan, "Joint Algorithm-Architecture Optimization of CABAC," *Journal of Signal Processing*

Systems, Vol. 69, No. 3, pp 239-252, December 2012

- **V. Sze**, A. P. Chandrakasan, "A Highly Parallel and Scalable CABAC Decoder for Next-Generation Video Coding," *IEEE Journal of Solid-State Circuits (ISSCC Special Issue)*, Vol. 47, No. 1, pp. 8-22, January 2012
- A. P. Chandrakasan, D. C. Daly, D. F. Finchelstein, J. Kwong, Y. K. Ramadass, M. E. Sinangil, **V. Sze**, N. Verma, "Technologies for Ultra Dynamic Voltage Scaling," *Proceedings of the IEEE*, Vol. 98, No. 2, pp 191-214, February 2010
- **V. Sze**, D. F. Finchelstein, M. E. Sinangil, A. P. Chandrakasan, "A 0.7-V 1.8-mW H.264/AVC 720p Video Decoder," *IEEE Journal of Solid-State Circuits (A-SSCC Special Issue)*, Vol. 44, No. 11, pp. 2943-2956, November 2009
- D.F. Finchelstein, **V. Sze**, A.P. Chandrakasan, "Multi-Core Processing and Efficient On-Chip Caching for H.264 and Future Video Decoders," *IEEE Transactions on Circuits and Systems for Video Technology,* Vol. 19, No. 11, pp. 1704-1713, November 2009. ***Nominated for TCSVT Best Paper Award***
- A. P. Chandrakasan, F. S. Lee, D. D. Wentzloff, **V. Sze,** B. P. Ginsburg, P. P. Mercier, D. C. Daly, R. Blazquez, "Low-Power Impulse UWB Architectures and Circuits," *Proceedings of the IEEE*, Vol. 97, No. 2, pp. 332-352, February 2009

Conference and Workshop Proceedings (*Indicates authors contributed equally to this work)

- T. Andrulis, J. Emer, **V. Sze**, "CiMLoop: A Fast, Flexible, and Accurate Compute-In-Memory Modeling Framework," *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, May 2024
- V. Sivaraman, P. Karimi, V. Venkatapathy, M.Khani, S. Fouladi, M. Alizadeh, F. Durand, **V. Sze**, "Gemino: Practical and Robust Neural Compression for Video Conferencing," *USENIX Symposium on Networked Systems Design and Implementation (NDSI)*, April 2024
- F. Xue, Y. N. Wu, J. S. Emer, **V. Sze**, "Tailor Swiftiles: Accelerating Sparse Tensor Algebra by Overbooking Buffer Occupancy," *ACM/IEEE International Symposium on Microarchitecture (MICRO)*, Oct 2023
- Y. N. Wu, P.-A. Tsai, S. Muralidharan, A. Parashar, **V. Sze**, J. S. Emer, "HighLight: Efficient and Flexible DNN Acceleration with Hierarchical Structured Sparsity," *ACM/IEEE International Symposium on Microarchitecture (MICRO)*, Oct 2023
- T. Andrulis, J. Emer, **V. Sze**, "RAELLA: Reforming the Arithmetic for Efficient, Low-Resolution, and Low-Loss Analog PIM: No Retraining Required!," *International Symposium on Computer Architecture (ISCA)*, June 2023
- M. Gilbert, Y. N. Wu, A. Parashar, **V. Sze**, J. Emer, "LoopTree: Enabling Exploration of Fused-layer Dataflow Accelerators," *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS),* April 2023
- Y. Wu, P. Tsai, A. Parashar, **V. Sze**, J. Emer, "SparseLoop: An Analytical Approach to Sparse Tensor Accelerator Modeling," *ACM/IEEE International Symposium on Microarchitecture (MICRO)*, October 2022
- P. Z. X. Li, S. Karaman, **V. Sze**, "Memory-Efficient Gaussian Fitting for Depth Images in Real Time," *IEEE International Conference on Robotics and Automation (ICRA)*, May 2022
- S. Sudhakar, **V. Sze**, S. Karaman, "Uncertainty from Motion for DNN Monocular Depth Estimation," *IEEE International Conference on Robotics and Automation (ICRA)*, May 2022
- S. Sudhakar, S. Karaman, **V. Sze**, "Carbon Emissions from Computing Onboard Autonomous Vehicle," *ICRA 2022 Workshop on Robotics for Climate Change*, May 2022
- Y.-L. Liao, S. Karaman, **V. Sze**, "Searching for Efficient Multi-Stage Vision Transformers," *ICCV 2021 Workshop on Neural Architectures: Past, Present and Future,* October 2021
- K. Gupta, P. Z. X. Li, S. Karaman, **V. Sze**, "Efficient Computation of Map-scale Continuous Mutual Information on Chip in Real Time," *IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS)*, September 2021
- T.-J. Yang, Y.-L. Liao, **V. Sze**, "NetAdapt v2: Efficient Neural Architecture Search with Fast Super-Network Training and Architecture Optimization," *Conference on Computer Vision and Pattern Recognition (CVPR)*, June 2021
- F. Wang, Y. Wu, M. Woicik, **V. Sze**, J. Emer, "Architecture-Level Energy Estimation for Heterogeneous Computing Systems," *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, March 2021
- Y. Wu, P. Tsai, A. Parashar, **V. Sze**, J. Emer, "Sparseloop: An Analytical, Energy-Focused Design Space Exploration Methodology for Sparse Tensor Accelerators," *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, March 2021
- J. Ray, A. Brahmakshatriya, R. Wang, S. Kamil, A. Reuther, **V. Sze**, S. Amarasinghe, "Domain-Specific Language Abstractions for Compression," *Data Compression Conference (DCC)*, March 2021
- S. Sudhakar, S. Karaman, **V. Sze**, "Balancing Actuation and Computing Energy in Motion Planning," *International Conference on Robotics and Automation (ICRA),* May 2020
- T. Henderson, **V. Sze**, S. Karaman, "An Efficient and Continuous Approach to Information-Theoretic Exploration," *IEEE International Conference on Robotics and Automation (ICRA),* May 2020
- L. Bernstein, A. Sludds, R. Hamerly, **V. Sze**, J. Emer, D. Englund, "Digital Optical Neural Networks for Large-Scale Machine Learning," *Conference on Lasers and Electro-Optics (CLEO),* May 2020
- Y. N. Wu, V. Sze, J. S. Emer, "An Architecture-Level Energy and Area Estimator for Processing-In-Memory Accelerator Designs," *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, April 2020
- T.-J. Yang, **V. Sze**, "Design Considerations for Efficient Deep Neural Networks on Processing-in-Memory Accelerators," *IEEE International Electron Devices Meeting (IEDM)*, Invited Paper, December 2019
- Y. N. Wu, J. Emer, **V. Sze**, "Accelergy: An Architecture-Level Energy Estimation Methodology for Accelerator Designs,"

IEEE International Conference on Computer Aided Design (ICCAD), November 2019

- J. Noraky, C. Mathy, A. Cheng, **V. Sze**, "Low Power Adaptive Time-Of-Flight Imaging for Multiple Rigid Objects," *IEEE International Conference on Image Processing (ICIP),* September 2019
- P. Z. X. Li*, Z. Zhang*, S. Karaman, **V. Sze**, "High-throughput Computation of Shannon Mutual Information on Chip," *Robotics: Science and Systems (RSS)*, June 2019
- Z. Zhang, T. Henderson, **V. Sze**, S. Karaman, "FSMI: Fast computation of Shannon Mutual Information for information-theoretic mapping," *IEEE International Conference on Robotics and Automation (ICRA),* May 2019
- D. Wofk*, F. Ma*, T.-J. Yang, S. Karaman, **V. Sze**, "FastDepth: Fast Monocular Depth Estimation on Embedded Systems," *IEEE International Conference on Robotics and Automation (ICRA),* May 2019
- J. Noraky, **V. Sze**, "Depth Estimation of Non-Rigid Objects for Time-Of-Flight Imaging," *IEEE International Conference on Image Processing (ICIP)*, October 2018
- H.-Y. Lai, G. Saavedra Peña, C. Sodini, T. Heldt, **V. Sze**, "Enabling Saccade Latency Measurements with Consumer-Grade Cameras," *IEEE International Conference on Image Processing (ICIP)*, October 2018
- T.-J. Yang, A. Howard, B. Chen, X. Zhang, A. Go, V. Sze, H. Adam, "NetAdapt: Platform-Aware Neural Network Adaptation for Mobile Applications," *European Conference on Computer Vision (ECCV),* September 2018
- A. Suleiman, Z. Zhang, L. Carlone, S. Karaman, **V. Sze**, "Navion: An Energy-Efficient Visual-Inertial Odometry Accelerator for Micro Robotics and Beyond," *Hot Chips: A Symposium on High Performance Chips*, August 2018
- G. Saavedra Peña, H.-Y. Lai, **V. Sze**, T. Heldt, "Determination of saccade latency distributions using video recordings from consumer-grade devices," *IEEE International Engineering in Medicine and Biology Conference (EMBC)*, July 2018
- A. Suleiman, Z. Zhang, L. Carlone, S. Karaman, **V. Sze**, "Navion: A Fully Integrated Energy-Efficient Visual-Inertial Odometry Accelerator for Autonomous Navigation of Nano Drones," *IEEE Symposium on VLSI Circuits (VLSI-Circuits)*, June 2018. ***Best Student Paper Award***
- Y.-H. Chen*, T.-J. Yang*, J. Emer, **V. Sze**, "Understanding the Limitations of Existing Energy-Efficient Design Approaches for Deep Neural Networks," *SysML Conference*, February 2018
- T.-J. Yang, Y.-H. Chen, J. Emer, **V. Sze**, "A Method to Estimate the Energy Consumption of Deep Neural Networks," *Asilomar Conference on Signals, Systems and Computers*, Invited Paper, October 2017
- J. Noraky, **V. Sze**, "Low Power Depth Estimation for Time-of-Flight Imaging," *IEEE International Conference on Image Processing (ICIP)*, September 2017
- Z. Zhang*, A. Suleiman*, L. Carlone, **V. Sze**, S. Karaman, "Visual-Inertial Odometry on Chip: An Algorithm-and-Hardware Co-design Approach," *Robotics: Science and Systems (RSS),* July 2017
- Z. Zhang, **V. Sze**, "FAST: A Framework to Accelerate Super-Resolution Processing on Compressed Videos," *CVPR Workshop on New Trends in Image Restoration and Enhancement*, July 2017
- T.-J. Yang, Y.-H. Chen, **V. Sze**, "Designing Energy-Efficient Convolutional Neural Networks using Energy-Aware Pruning," *IEEE Conference on Computer Vision and Pattern Recognition (CVPR)*, July 2017
- M. Tikekar, **V. Sze**, A. Chandrakasan, "A Fully-Integrated Energy-Efficient H.265/HEVC Decoder with eDRAM for Wearable Devices," *Symposia on VLSI Technology and Circuits (VLSI)*, June 2017
- A. Suleiman*, Y.-H. Chen*, J. Emer, **V. Sze**, "Towards Closing the Energy Gap Between HOG and CNN Features for Embedded Vision," *IEEE International Symposium of Circuits and Systems (ISCAS)*, Invited Paper, May 2017
- **V. Sze**, Y.-H. Chen, J. Emer, A. Suleiman, Z. Zhang, "Hardware for Machine Learning: Challenges and Opportunities," *IEEE Custom Integrated Circuits Conference (CICC)*, Invited Paper, May 2017. ***Outstanding Invited Paper Award***
- Y.-H. Chen, J. Emer, **V. Sze**, "Eyeriss: A Spatial Architecture for Energy-Efficient Dataflow for Convolutional Neural Networks," *International Symposium on Computer Architecture (ISCA),* pp. 367-379, June 2016. ***Selected for IEEE Micro's Top Picks special issue on "most significant papers in computer architecture based on novelty and long-term impact" from 2016***
- A. Suleiman, Z. Zhang, **V. Sze**, "A 58.6mW Real-time Programmable Object Detection with Multi-Scale Multi-Object Support Using Deformable Parts Models on 1920×1080 Video at 30fps," *Symposia on VLSI Technology and Circuits (VLSI)*, pp. 184-185, June 2016
- Y.-H. Chen, T. Krishna, J. Emer, **V. Sze**, "Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks," *ISSCC Dig. Tech. Papers*, pp. 262-264, February 2016. ***Highlighted in EEtimes*** *(http://eyeriss.mit.edu)*
- Z. Zhang, **V. Sze**, "Rotate Intra Block Copy for Still Image Coding," *IEEE International Conference on Image Processing (ICIP)*, September 2015
- A. Suleiman, **V. Sze**, "Energy-Efficient HOG-based Object Detection at 1080HD 60 fps with Multi-Scale Support," *IEEE International Workshop on Signal Processing Systems (SiPS),* pp. 256-261, October 2014
- Y.-H. Chen, **V. Sze**, "A 2014 Mbin/s Deeply Pipelined CABAC Decoder For HEVC," *IEEE International Conference on Image Processing (ICIP)*, pp. 2110-2114, October 2014
- M. Tikekar, C.-T. Huang, **V. Sze**, A. Chandrakasan, "Energy and Area-Efficient Hardware Implementation of HEVC Inverse Transform and Dequantization," *IEEE International Conference on Image Processing (ICIP)*, pp. 2100-2104, October 2014. ***Top 10% Paper Recognition at ICIP***

- **V. Sze**, M. Budagavi, "A Comparison of CABAC Throughput for HEVC/H.265 vs. AVC/H.264," *IEEE Workshop on Signal Processing Systems (SiPS)*, pp. 165 – 170, October 2013
- C.-T. Huang, M. Tikekar, C. Juvekar, **V. Sze**, A. P. Chandrakasan, "A 249Mpixels/s HEVC Video Decoder Chip for Quad Full HD Applications," *ISSCC Dig. Tech. Papers*, pp. 1533-1536, February 2013
- M. E. Sinangil, **V. Sze,** M. Zhou, A. P. Chandrakasan, "Memory cost vs. Coding efficiency trade-offs for HEVC motion estimation engine," *IEEE International Conference on Image Processing (ICIP)*, pp. 1533-1536, September 2012
- M. E. Sinangil, **V. Sze,** M. Zhou, A. P. Chandrakasan, "Hardware-aware motion estimation search algorithm development for High-Efficiency Video Coding (HEVC) standard," *IEEE International Conference on Image Processing (ICIP)*, pp. 1529-1532, September 2012
- M. Budagavi, **V. Sze,** "Unified forward+inverse transform architecture for HEVC," *IEEE International Conference on Image Processing (ICIP)*, September 2012
- M. Zhou, **V. Sze,** M. Budagavi, "Parallel Tools in HEVC for High-Throughput Processing," *SPIE Optical Engineering + Applications, Applications of Image Processing XXXV*, August 2012
- **V. Sze,** M. Budagavi, "Parallelization of Transform Coefficient Coding for HEVC," *IEEE Picture Coding Symposium (PCS)*, pp. 509 – 512, May 2012
- M. Budagavi, **V. Sze**, M. Zhou, "HEVC ALF decode complexity analysis and reduction," *IEEE International Conference on Image Processing (ICIP)*, pp. 745-748, September 2011
- **V. Sze**, A. P. Chandrakasan, "Joint Algorithm-Architecture Optimization of CABAC to Increase Speed and Reduce Area Cost," *IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, pp. 1577–1580, May 2011
- **V. Sze**, A. P. Chandrakasan, "A Highly Parallel and Scalable CABAC Decoder for Next-Generation Video Coding," *ISSCC Dig. Tech. Papers*, pp. 126-127, February 2011. ***Highlighted in EETimes*** (https://www.eetimes.com/isscc-algorithm-paves-path-to-better-video/#)
- **V. Sze**, A. P. Chandrakasan, "A High Throughput CABAC Algorithm Using Syntax Element Partitioning," *IEEE International Conference on Image Processing (ICIP)*, pp. 773-776, November 2009
- D. F. Finchelstein, **V. Sze**, M.E. Sinangil, Y. Koken, A.P. Chandrakasan, "A Low-Power 0.7-V H.264 720p Video Decoder," *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp. 173-176, November 2008. ***Selected as one of 9 noteworthy technical papers at conference***
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- **Z. Zhang**, V. Sze, "Rotate Intra Block Copy," JVET-L0041, ITU-T/ISO/IEC JVET meeting, Macao, China, October 2018.

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- **V. Sze**, M. Budagavi, "Reduction in context coded bins for ref_idx and cu_qp_delta," JCTVC-I204, Stockholm, July 2012.
- M. Budagavi, **V. Sze**, M. Sadafale, "Hardware analysis of transform and quantization," JCTVC-G132, Geneva, November 2011.
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- **V. Sze**, M. Budagavi, "Parallel Context Processing of Coefficient Level," JCTVC-F130, Torino, July 2011.
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Pre-HEVC development -- ITU-T VCEG (Video Coding Experts Group)

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- **V. Sze**, M. U. Demircin, M. Budagavi, "CABAC throughput requirements for real-time decoding," ITU-T Q.6/SG16 VCEG, VCEG-AJ31, San Diego, October 2008.
- **V. Sze**, M. Budagavi, "Parallel CABAC," ITU-T Q.6/SG16 VCEG, COM-16-C-334-E, Geneva, April 2008.

APPENDIX 2: MATERIALS CONSIDERED

I have reviewed and considered each of the exhibits listed in the following table in drafting this Declaration.

Exhibit No.	Description
1007	Nakamura et al., "Unification of derivation process for merge mode and MVP," Joint Collaborative Team on Video Coding (JCT-VC) of ITU-T SG16 WP3 and ISO/IEC JTC1/SC29/WG11, 6th Meeting, Torino, Italy, Jul. 14-22, 2011, Document JCTVC-F419
1008	Nakamura et al., "WD description of JCTVC-F419 Proposal 1" for "Unification of derivation process for merge mode and MVP," Joint Collaborative Team on Video Coding (JCT-VC) of ITU-T SG16 WP3 and ISO/IEC JTC1/SC29/WG11, 6th Meeting, Torino, Italy, Jul. 14-22, 2011, Document JCTVC-F419
1009	Nakamura et al., "Unification of derivation process for merge mode and MVP" Presentation, Joint Collaborative Team on Video Coding (JCT-VC) of ITU-T SG16 WP3 and ISO/IEC JTC1/SC29/WG11, 6th Meeting, Torino, Italy, Jul. 14-22, 2011, Document JCTVC-F419
1010	Bross et al., "WD4: Working Draft 4 of High-Efficiency Video Coding," Joint Collaborative Team on Video Coding (JCT-VC) of ITU-T SG16 WP3 and ISO/IEC JTC1/SC29/WG11, 6th Meeting: Torino, IT, Jul. 14-22, 2011, Document JCTVC-F803 ("WD4")
1026	JCT-VC - Joint Collaborative Team on Video Coding (https://www.itu.int/en/ITU-T/studygroups/2013-2016/16/Pages/video/jctvc.aspx)
1027	Terms of Reference of the Joint Collaborative Team on Video Coding Standard Development (https://www.itu.int/dms_pub/itu-t/oth/46/01/T46010000010001PDFE.pdf)
1028	Sullivan et al., "Meeting report of the sixth meeting of the Joint Collaborative Team on Video Coding (JCT-VC), Torino, IT, 14–22 July 2011," Joint Collaborative Team on Video Coding (JCT-VC) of ITU-T SG16 WP3 and ISO/IEC JTC1/SC29/WG11, 6th Meeting, Torino, Italy, Jul. 14-22, 2011, Document JCTVC-F800

Exhibit No.	Description
1029	"All Meetings" web page (from the JCT-VC website) (http://phenix.int-evry.fr/jct/doc_end_user/all_meeting.php)
1030	"Torino Meeting - Document Register" web page (from the JCT-VC website) (http://phenix.int-evry.fr/jct/doc_end_user/current_meeting.php?id_meeting=149&search_id_group=1&search_sub_group=1)
1031	A portion of search screen for "merge mode" on the "Torino Meeting - Document Register" web page
1032	A portion of search screen for "MVP" on the "Torino Meeting - Document Register" web page
1033	Search result page for "merge mode" originated from the "Torino Meeting - Document Register" web page
1034	Search result page for "MVP" originated from the "Torino Meeting - Document Register" web page
1035	Search result page for "WD4" originated from the "Torino Meeting - Document Register" web page
1036	Search result page for "high-efficiency video coding" originated from the "Torino Meeting - Document Register" web page
1037	Search result page for "draft" originated from the "Torino Meeting - Document Register" web page
1038	"Preview document JCTVC-F419 for Torino meeting" web page (http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=2894)
1039	"Preview document JCTVC-F803 for Torino meeting" web page (http://phenix.int-evry.fr/jct/doc_end_user/current_document.php?id=3286)
	Declaration of Benjamin Bross in support of petition for *inter partes* review of U.S. Patent No. 9,113,163*, Samsung Electronics Co., Ltd. et al v. M&K Holdings Inc.*, IPR2018-00696, Exhibit 1002 (Feb. 26, 2018)
	Declaration of Dr. Anthony Vetro in support of petition for *inter partes* review of U.S. Patent No. 9,113,163*, Samsung Electronics Co., Ltd. et al v. M&K Holdings Inc.*, IPR2018-00696, Exhibit 1058 (Feb. 26, 2018)