UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR § 1.53(b))		
	Attorney Docket No.	129980-5066-US01
	First Inventor	Hyun Lee
	Title	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
	Electronically filed	November 11, 2019

APPLICATION ELEMENTS
See MPEP Chapter 600 concerning utility patent application contents.

1. ☐ Fee Transmittal Form *(with duplicate for fee processing)*
2. ☐ Applicant claims Small Entity status, see 37 C.F.R. § 1.27
3. ☒ Specification [Total Pages 23]
4. ☒ Drawing(s) *(35 USC § 113)* [Total Sheets 3]
5. ☒ Oath or Declaration [Total Pages 2]
   a. ☐ Newly executed *(original or copy)*
   b. ☒ Copy from a prior application *(37 CFR § 1.63(d))*
6. ☒ Application Data Sheet, see 37 C.F.R. § 1.76
7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
   ☐ Landscape Table on CD
8. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Form (CRF)
   b. ☐ Specification Sequence Listing on
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statement verifying identity of above copies

Address to: **Commissioner for Patents**
P.O. Box 1450
Alexandria, VA 22313-1450

ACCOMPANYING APPLICATION PARTS

9. ☐ Assignment Papers *(cover sheet & document(s))*
   Name of Assignee:
10. ☒ 37 CFR § 3.73(c) Statement
    a. ☒ Power of Attorney
11. ☐ English Translation Document *(if applicable)*
12. ☐ Information Disclosure Statement and PTO-1449
    a. ☐ Copies of citations attached
13. ☐ Preliminary Amendment
14. ☐ Return Receipt Postcard *(MPEP 503)*
15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. ☐ Non-Publication Request under 35 U.S.C. § 122 (b)(2)(B)(i)
17. ☐ Other:

Note: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **MUST** be included in an Application Data Sheet (ADS).

(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS: Customer Number 79141

Signature	/ Jamie J. Zheng /	Date	November 11, 2019
Name (Print/Type)	Jamie J. Zheng	Registration No. (Attorney/Agent)	51,167

Electronically filed November 11, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	To be assigned
Serial No.:	To be assigned	Art Unit	To be assigned
Filed:	Filed herewith	Examiner:	To be assigned
For:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES	Attorney Docket No.:	129980-5066-US01

STATEMENT UNDER 37 C.F.R. § 3.73(c)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Netlist, Inc., a corporation, states that it is the assignee of the entire right, title and interest in the patent application/patent identified above by virtue of an assignment from the inventor(s) of the parent of the patent application/patent identified above.

The assignment was recorded in the United States Patent and Trademark Office on November 15, 2017 at Reel 044140, Frame 0019, or for which a copy thereof is attached.

The undersigned is authorized to act on behalf of the assignee.

Date: November 11, 2019

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

GENERAL POWER OF ATTORNEY BY APPLICANT FOR UNITED STATES PATENT

I hereby revoke all previous powers of attorney given in the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

I hereby appoint the practitioner associated with the following Customer Number :

79141

as my/our attorney or agent, and to transact all business in the United States Patent and Trademark Office in connection with the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

Please recognize or change the **correspondence address** for the application referenced in the attached transmittal letter to the address associated with the above-mentioned **Customer Number**.

I am the Applicant:

☐ Inventor or Joint Inventor

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

■ Assignee or Person to Whom the Inventor is Under an Obligation to Assign

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is currently being filed in this document)

SIGNATURE of Applicant for Patent

Signature		Date: January 9, 2013
Name	**Gail Sasaki**	
Title	Vice President and Chief Financial Officer	
Company	Netlist, Inc.	

Note: Signature - this form must be signed by the Applicant or a person authorized to act on behalf of Applicant.

Submit multiple forms for more than one signature
Total of __ forms are submitted.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5066-US01
	Application Number	
Title of Invention	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hyun		Lee	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	State/Province	Country of Residence
Ladera Ranch	CA	US

Mailing Address of Inventor:

Address 1	175 Technology, Suite 150
Address 2	

City	State/Province	Postal Code	Country
Irvine	CA	92618	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. — Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	79141		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES		
Attorney Docket Number	129980-5066-US01	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	3	**Suggested Figure for Publication (if any)**	

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Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	79141		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	15/857553	2017-12-28

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5066-US01
	Application Number	
Title of Invention	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES	

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/857553	Continuation of	15/088115	2016-04-01	9858218	2018-01-02
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/088115	Continuation of	13/942721	2013-07-16	9311116	2016-04-12
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/942721	Continuation of	12/815339	2010-06-14	8489837	2013-07-16
Prior Application Status	Expired				Remove

Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12/815339	Claims benefit of provisional	61/186799	2009-06-12

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5066-US01
	Application Number	
Title of Invention	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES	

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5066-US01
	Application Number	
Title of Invention	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5066-US01
	Application Number	
Title of Invention	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Netlist, Inc.		
Mailing Address Information For Applicant:			
Address 1	175 Technology, Suite 150		
Address 2			
City	Irvine	**State/Province**	CA
Country	US	Postal Code	92618
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/ Jamie J. Zheng /			Date (YYYY-MM-DD)	2019-11-11
First Name	Jamie J.	Last Name	Zheng	Registration Number	51167

Additional Signature may be generated within this form by selecting the Add button. Add

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5066-US01
	Application Number	
Title of Invention	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. App. No. 15/857,553, filed December 28, 2017, which is a continuation of U.S. App. No. 15/088,115, filed April 1, 2016, now U.S. Pat. No. 9858218, which is a continuation of U.S. App. No. 13/942,721, filed July 16, 2013, now U.S. Pat. No. 9,311,116, which is a continuation of U.S. App. No. 12/815,339, filed June 14, 2010, now U.S. Pat. No. 8,489,837, which claims the benefit of priority from U.S. Provisional App. No. 61/186,799, filed June 12, 2009, each of which is incorporated in its entirety by reference herein.

FIELD OF THE DISCLOSURE

[0002] The present disclosure relates to the operation of memory modules. Specifically, the present disclosure relates to a memory module having an open drain output for parity error and for training sequences.

BACKGROUND OF THE DISCLOSURE

[0003] Memory subsystems such as memory modules are generally involved in the initialization procedure for computer systems, including servers, personal computers, and the like. For example, during system-wide initialization, the memory subsystems may undergo internal initialization procedures, or the system memory controller may otherwise interact with the memory subsystems during the initialization procedure. As part of this interaction, the system memory controller may request that the memory subsystem perform one or more requested tasks during system initialization.

SUMMARY

[0004] According to certain aspects, a memory module is coupled to a memory controller of a host computer system via an interface. The interface includes data, address and control signal pins and an output pin in addition to the data, address and control signal pins. The memory module receives a first command from the memory controller via the address and control signal pins, and enters a first mode in response to the first command. The memory module in the first mode responds to at

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least one initialization sequence, and sends a first output signal via the output pin to indicate a status of the at least one initialization sequence to the memory controller. The memory module enters a second mode in which the memory module performs memory operations including memory read/write operations according to an industry standard. During the read/write operations, the memory module communicates data with the memory controller via the data signal pins in response to second memory commands received via the address and control signal pins. The memory module may output a second output signal related to the read/write operations via the output pin.

[0005] According to certain aspects, a memory module is coupled to a memory controller of a host computer system via an interface. The interface includes data, address and control signal pins and an output pin in addition to the data, address and control signal pins. The memory module performs an internal procedure in a first mode in response to a first command from the memory controller whereby the memory controller hands off control of the internal procedure to the first memory module. The memory module sends a first output signal via the output pin to indicate a status of the internal procedure to the memory controller. The memory module enters a second mode in which the memory module performs standard operations including one or more of memory read/write, pre-charge, refresh operations according to an industry standard. The memory module may output a second output signal related to the standard operations via the output pin.

[0006] In another aspect, a memory module is operable in a first mode and in a second mode. The memory module operates according to an industry standard in the second mode by performing standard operations including memory read/write operations in response to address and control signals from a memory controller of a host computer system. The memory module comprises a standard interface including data, address and control signal pins and an output pin in addition to the data, address and control signal pins. The memory module enters the first mode in response to a first command from the memory controller, in which the memory module responds to at least one initialization sequence. The memory module further comprises a notification circuit to output a notification signal indicating a status of the at least one initialization sequence to the memory controller via the output pin.

[0007] In certain embodiments, a memory module is operable with a memory controller of a host system and comprises a printed circuit board having edge connections that fit into a corresponding

slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections. The memory module further comprises dynamic random access memory elements on the printed circuit board, and a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection. The memory module is configurable to operate in any of at least a first mode and a second mode. The memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections. The memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and is configurable to perform operations related to one or more training sequences.

[0008] In certain embodiments, the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, and the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals. The module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode. The module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figure 1 shows an example host computer system including an example memory module configured to perform handshaking with a memory controller of the host computer system according to certain embodiments described herein.

[0010] Figure 2 shows an example host computer system including example first and second

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memory modules configured to perform handshaking with a system memory controller of the host computer system according to certain embodiments described herein.

[0011] Figure 3 shows a host computer system including example first and second memory modules configured to perform handshaking with a memory controller of the host system, where the notification circuits of the first and second memory modules have another example configuration according to certain embodiments described herein.

[0012] Figure 4 and Figure 5 show example methods of using at least one memory module according to certain embodiments described herein.

DETAILED DESCRIPTION

[0013] Existing initialization schemes have certain inefficiencies which lead to wasted time and expense. Thus, there is a need to reduce the time and complexity involved in system memory controller interactions with memory subsystems during initialization. Certain embodiments described herein advantageously satisfy at least a portion of this need by providing a system and method which utilizes a feedback path from a memory subsystem such as a memory module to a system memory controller, such as a Memory Controller Hub (MCH) of a computer system during initialization.

[0014] In general, there is no existing method of handshaking between the MCH (e.g., system memory controller) and a memory subsystem (e.g., memory module) during initialization. For example, in conventional systems, the system memory controller does not monitor the error-out signal from the memory subsystem. This causes the MCH to perform blind execution. In a typical server (e.g., an Intel or AMD or other chipset based server), the lack of any handshaking between the MCH and the memory subsystem during the server initialization period has not been a serious issue since the MCH generally has complete control over the initialization procedure. However, one possible configuration for LR-DIMM (Load Reduced DIMM) includes the MCH handing over one or more parts of the initialization operation sequence to the memory subsystem. This raises an unprecedented issue not addressed in conventional systems because, in such proposed configurations, the system can benefit from the MCH handshaking with the memory subsystem controller, as described more fully below.

[0015] Such an LR-DIMM configuration may have the MCH inserting a waiting period of

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predetermined length during which the MCH is idle and the memory subsystem controller undergoes initialization. However, one shortcoming of this LR-DIMM configuration would be that it requires the MCH to be in standby (idle, or wait) while the memory subsystem controller completes its task. Under such an arrangement, since the time to complete a task can be dependent on the density, speed and configuration of the memory subsystem, and these parameters may be unknown to the MCH, the MCH may have to insert a single, predetermined standby period. In addition, if there are multiple occasions that the MCH needs to hand off control to the memory subsystem controller, the required MCH wait periods can be different from one occasion to another, and it complicates the correlation between the MCH and the memory subsystem controller. For example, the MCH according to such a scheme may give control to the local memory controller of a memory subsystem (e.g., memory module) for execution of a training sequence. The MCH may wait for a pre-determined period of time and then assume that the local memory controller has completed the training sequence. However, depending on the memory subsystem parameters (e.g., memory capacity, speed, number of ranks, etc.), the time for actually completing the training sequence may vary and may be longer or shorter than predetermined period of time.

[0016] In general, handshaking can be implemented in at least two ways; polling and notifying. In the polling method, the MCH reads a status register in the memory subsystem controller to find out if the memory subsystem controller has completed the required or requested operation. For example, a status register may be read out through a serial interface such as System Management Bus (SMBus). However, a register polling method is generally inefficient because the system memory controller does not know exactly when the memory subsystem will have completed the required or requested operation. Thus, the system memory controller may wait longer than necessary to poll the memory subsystem, thereby delaying the overall initialization process. Additionally, the problem may be compounded because multiple training sequences or other initialization sequences may be run on the memory subsystem during a particular initialization period, resulting in accumulation of such unnecessary delays. Moreover, polling generally involves scheduling polling intervals during which the system memory controller is not performing other operations, resulting in further inefficiency.

[0017] Alternatively, the notifying method is an advantageous handshaking method between the MCH and the memory subsystem controller. According to a notifying method, the memory subsystem controller sends a signal to the MCH when the memory subsystem controller completes

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the required or requested operation. This method allows the MCH to execute one or more independent commands while it is waiting for a notification signal from the memory subsystem controller.

[0018] Certain embodiments described herein provide a method of establishing a handshake mechanism based on notification signaling. In certain embodiments, this mechanism can be implemented by adding a new interface (notifying) signal between the MCH and the memory subsystem controller, or by adding an additional functionality to an existing, non-timing critical signal without altering the memory subsystem hardware. In either case, the interface between the MCH and the memory subsystem controller of certain embodiments can be an open drain signaling from the memory subsystem controller to the MCH, although a variety of other configurations are possible. As will be appreciated by persons skilled in the art, the terms MCH, system memory controller, and memory subsystem are used generally interchangeable throughout this disclosure, and the terms memory module, memory subsystem controller, and local memory controller are used generally interchangeably throughout this disclosure.

[0019] FIG. 1 illustrates an example host computer system 16 including an example memory module 10 according to certain embodiments described herein. The memory module 10 can comprise at least one output 12 configured to be operatively coupled to a system memory controller 14 of the host computer system 16. In certain embodiments, the memory module 10 is configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode. The memory module 10 may further include a controller circuit 18. In some embodiments, the controller circuit 18 is configured to cause the memory module 10 to enter the initialization mode. The memory module 10 can further include a notification circuit 20 configured to drive the at least one output 12 while the memory module 10 is in the initialization mode to provide at least one notification signal to the memory controller 14 indicating at least one status of the at least one initialization sequence.

[0020] The memory module 10 may comprise a printed-circuit board (PCB) 22. In certain embodiments, the memory module 10 has a memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, 16-GB, or higher. Other memory capacities are also compatible with certain embodiments described herein. In addition, memory modules 10 having widths of 4 bytes, 8 bytes, 16 bytes, 32

bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. The PCB 22 can have an industry-standard form factor. For example, the PCB 22 can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB 20 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB 22 has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FBDIMM), mini-DIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein. In other embodiments, certain non-DIMM form factors are possible such as, for example, single in-line memory module (SIMM), multi-media card (MMC), and small computer system interface (SCSI).

[0021] In certain embodiments, the memory module 10 is operatively coupled to (e.g., in electrical communication with) the host computer system 16. In certain other embodiments, the memory module 10 may communicate with the host computer system 16 using some other type of communication, such as, for example, optical communication. Examples of host computer systems 16 include, but are not limited to, blade servers, 1U servers, personal computers (PCs), and other applications in which space is constrained or limited. The PCB 22 can comprise an interface (not shown) that is configured to be in electrical communication with the host computer system 16. For example, the interface can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system 16. The interface of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory module 10 and the host system 16. For example, the interface can comprise a standard 240-pin DDR2 edge connector. The at least one output 12 may be routed over the interface, for example.

[0022] The memory module 10 may also comprise one or more memory elements (not shown), such as dynamic random-access memory (DRAM) elements, for example. Types of DRAM elements compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, DDR4, and synchronous DRAM (SDRAM). In addition, memory elements having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Memory elements compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP),

ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP). In certain embodiments, the memory module 10 may also include one or more non-volatile memory elements, such as one or more flash memory elements. Types of flash memory elements compatible with certain embodiments described herein include, but are not limited to, NOR flash, NAND flash, ONE-NAND flash, and multi-level cell (MLC).

[0023] The controller circuit 18 of certain embodiments generally controls the operation of the memory module 10. For example, the controller circuit 18 may control the memory elements of the memory module 10 and/or communicate with the system memory controller 14. For example, the controller circuit 18 may receive and process address and command signals (e.g., read, write commands) from the system memory controller 14 and transmit appropriate address and commands to the memory elements in response. See, e.g., U.S. Pat. Appl. Publ. Nos. 2006/0062047 A1 and 2006/0262586 A1, each of which is incorporated in its entirety by reference herein. In certain embodiments, the controller circuit 18 comprises a local memory controller. Additionally, depending on the architecture of the memory module 10, such as for an FB-DIMM, the controller circuit 18 may comprise an advanced memory buffer (AMB). The controller circuit 18 can comprise one or more of a field-programmable gate array (FPGA), a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, and a complex programmable logic device (CPLD), for example. In certain embodiments, the controller circuit 18 comprises various discrete electrical elements, while in certain other embodiments, the controller circuit 18 comprises one or more integrated circuits.

[0024] As discussed, the memory module 10 is configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode. In one embodiment, for example, the at least one initialization sequence may comprise one or more training sequences. The initialization sequence (e.g., comprising one or more training sequences) may be initiated by the system memory controller 14. In some embodiments, the controller circuit 18 is configured to cause the memory module 10 to enter the initialization mode. For example, the controller circuit 18 may be configured to execute a routine implementing the at least one initialization sequence when the appropriate signal or command is received from the memory controller 14 or is otherwise received from the host computer system 16 (e.g., upon receipt of a reset signal).

[0025] In certain embodiments, for example, the computer system 16 is coupled to a plurality of memory modules 10, 26 including the memory module 10 and at least a second memory module 26, and the memory controller 14 (e.g., MCH) trains each module 10, 26 separately, in series. In one example scenario, the memory controller 14 issues a first command to the memory module 10, and, in response, the memory module 10 executes an initialization sequence (e.g., one or more training sequences). Upon completion of the initialization sequence, the first memory module 10 advantageously issues a notification to the memory controller 14 in accordance with embodiments described herein. In response, the memory controller 14 issues a second command, this time to the memory module 26, and, in response, the memory module 26 executes an initialization sequence (e.g., one or more training sequences). Upon completion of the initialization sequence, the second memory module 26, similar to the first memory module 10, advantageously issues a notification to the memory controller 14 in accordance with embodiments described herein. In response, where there are more than two memory modules 10, 26, the memory controller 14 issues a third command to a third memory module (not shown), and so forth. One example computer system 16 capable of implementing such a scenario is configured to execute an Intel Basic Input/Output System (BIOS), and comprises a plurality of memory modules 10, 26 having an LRDIMM configuration. In such an example system, the Intel BIOS causes the system memory controller 14 to initialize the LRDIMM memory modules 10, 26 serially.

[0026] The operational mode is the normal mode of the memory module 10. For example, during the operational mode, the memory module 10 is generally accessed by the system memory controller 14 of the host computer 16 during standard computer operation not associated with initialization. For example, the system memory controller 14 may cause the memory module 10 to perform standard operations such as memory read/write, pre-charge, refresh, etc., while in operational mode, although it will be appreciated that one or more of these operations can also be performed by the memory module 10 while in initialization mode in certain embodiments.

[0027] The notification circuit 20 can be configured to drive the at least one output 12, while the memory module 10 is in the initialization mode or after the memory module 10 completes one or more initialization sequences, to provide the at least one notification signal to the memory controller 14 indicating at least one status of the at least one initialization sequence. While shown in FIGS. 1-3 as forming a part of the controller circuit 18, the notification circuit 20 may be a physically and/or logically separate circuit in certain embodiments. While a variety of

configurations are possible, the notification circuit 20 may comprise one or more transistors, one or more logic elements (e.g., AND, OR, NOR, NAND, XOR gates, and the like), or a combination thereof. In some embodiments, the notification circuit 20 may additionally or alternatively comprise one or more of an FPGA, PLD, CPLD, ASIC, custom-designed semiconductor device, discrete electrical elements, and an integrated circuit.

[0028] The at least one status of certain embodiments comprises completion of the at least one initialization sequence, such that the at least one notification signal is indicative of the completion of the at least one initialization sequence. The at least one status of certain embodiments comprises execution of the at least one initialization sequence. For example, the at least one status may indicate that the at least one initialization sequence is currently being executed. In some embodiments, the at least one status may provide an indication that a certain task has been completed by the memory module 10, such as a training task requested by the system memory controller 14. In certain embodiments, the notification circuit 20 can be configured to drive the at least one output 12 to a first state indicative of execution of the at least one initialization sequence or to a second state indicative of completion of the at least one initialization sequence. As one example, the first state may be a high or low logic level, and the second state may be a high impedance state. In another case, the first state is a high or low logic level, and the second state is the inverse logic level of the first state.

[0029] The at least one output 12 of certain embodiments is configured to be operatively coupled to at least one interrupt of the system memory controller 14, and the system memory controller 14 is responsive to the at least one notification signal indicating completion of the at least one initialization sequence. For example, the system memory controller 14 may trigger execution of an interrupt routine upon receipt of the notification signal on the output 12. The interrupt routine generally executes the appropriate operations for the at least one status indicated by the at least one notification signal. For example, if the at least one status indicates that the at least one initialization sequence is complete, execution of the interrupt routine may cause the system memory controller 14 to notify the host computer system 16 that the system initialization, or a portion thereof, is completed. In one embodiment, for example, the execution of the interrupt routine causes the system memory controller 14 to initiate a subsequent training sequence for the memory module 10 or on another memory module connected to the host system 16. For example, in one embodiment, a central processing unit (CPU) of the host system 16 (not shown) enters a

"Wait" state after issuing a command to the memory module 10 to enter the initialization mode. Receipt of the at least one notification signal on the output 12 triggers execution of the interrupt routine, which interrupts the CPU, causing the "Wait" state to be aborted and allowing the host system 16 to continue operation. In this manner, generation of the interrupt on the at least one output 12 can allow completion of the at least one initialization sequence to receive generally immediate attention from the CPU and/or memory controller 14 of the host system 16. As will be appreciated, the CPU and memory controller 14 of the host system 16 may comprise separate modules, or may alternatively comprise a single integrated module, depending on the architecture of the host system 16 chip-set.

[0030] In certain embodiments, execution of the interrupt routine causes the system memory controller 14 to cause the memory module 10 to exit the initialization mode and to enter the operational mode. In another embodiment, the memory module 10 automatically enters the operational mode upon completion of the at least one initialization sequence without intervention from the memory controller 14.

[0031] In some embodiments, the at least one output 12 is operated in conformance with a standard (e.g., an industry standard) when the memory module 10 is in the operational mode, but is not operated in conformance with the standard when the memory module 10 is in the initialization mode. An example of a standard in accordance with certain embodiments described herein is one or more of the industry standard promulgated by the Joint Electronic Devices Engineering Counsel (JEDEC). For example, the operation and behavior of the at least one output 12 may conform to an industry standard when the memory module 10 is in the operational mode, but the operation and behavior of the at least one output 12 may not conform to the industry standard when the memory module 10 is in the initialization mode. Because the at least one output 12 does not conform to the standard during initialization mode, an existing (e.g., JEDEC-specified) pin may be utilized to provide the at least one notification signal to the system memory controller 14 from the memory module 10 during the initialization mode. In one embodiment, for example, the at least one output 12 comprises an error-out pin of the memory module 10. In conventional systems, the operation of the error-out pin is undefined by the standard during initialization. However, in certain embodiments described herein, during the operational mode, the error-out pin may be used according a conventional industry standard (e.g., a JEDEC standard) to indicate a parity error has occurred in the memory module 10. During the initialization mode, the error-out pin can be used

to transmit the at least one notification signal to the system memory controller 14.

[0032] It is advantageous to use the error-out pin for initialization status notification according to certain embodiments because the error-out pin can be asserted by the memory module 10 independent from system memory controller 14 requests or commands. Also, because the error-out pin is a JEDEC-specified pin, design cost and complexity are reduced because additional pin-outs and interrupt design changes can be avoided (e.g., in cases where such changes in hardware or chipset may not be feasible to provide the at least one status to the system memory controller 14). However, in certain other embodiments, providing the at least one status may be implemented by adding one or more pins to the system memory controller 14 (e.g., MCH) and to the controller circuit 18 (e.g., local memory controller), thereby utilizing changes in hardware or the chipset.

[0033] Moreover, the error-out pin may be coupled to an interrupt of the system memory controller 14 (e.g., according to the JEDEC standard). Thus, where the error-out pin is used, from the system point of view in accordance with certain embodiments, the notification of completion of the required or requested task from the memory module 10 (e.g., by the local memory controller) generates an interrupt communicated to the system during the initialization period and indicative of completion of the required or requested task. Assertion of the same pin during normal (non-initialization) operation upon an error occurring, on the other hand, generates an interrupt communicated to the system during the normal operation indicative of the occurrence of the error condition. Thus, in certain embodiments, the error-out pin and corresponding signal memory module 10 can be used to support the notifying function and to provide the at least one status generally without changing hardware. Certain other such embodiments involve modifying the basic input/output system (BIOS) or other programming change. For example, the BIOS may be modified to indicate to the system memory controller 14 how to respond to the notification signal (e.g., to the error_out signal or the interrupt corresponding thereto).

[0034] In certain other embodiments, the at least one output 12 may include other existing (e.g., JEDEC specified) pins instead of, or in addition to, the error-out pin. In yet other configurations, at least one additional (e.g., non-JEDEC specified) pin may be employed. In general, any pin not otherwise active during the initialization mode may be used (e.g., high-order address pins, read/write pins, data pins, etc.).

[0035] The at least one output 12 can further be configured to be operatively coupled to at least

one second output 24 of a second memory module 26 in some embodiments, as schematically illustrated in FIGS. 1-3. The second memory module 26 may be generally similar in structure and function to the memory module 10, and may comprise a controller circuit 28 and a notification circuit 30, for example. The second memory module 26 may be generally identical to the first memory module 10, or may have a different memory capacity, form factor, etc., than the first memory module 10. More than two such memory modules may be present in certain embodiments. As described above, the second memory module 26 can be configured to operate in at least two modes comprising an initialization mode during which the second memory module 26 executes at least one initialization sequence, and an operational mode. For example, the initialization and operational modes may be similar to those describe above in relation to the first memory module 10.

[0036] The second memory module 26 can also be configured to drive the at least one second output 24 to a third state indicative of execution of at least one initialization sequence of the second memory module 26 or to a fourth state indicative of completion of the at least one initialization sequence of the second memory module 26. Additionally, in some embodiments, the at least one first output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are operatively coupled together by a bus 32 which is also operatively coupled to at least one input 34 of the system memory controller 14. In other embodiments (not shown), the at least one first output 12 and the at least one second output 24 are not coupled together, and are coupled to two separate inputs of the system memory controller 14.

[0037] FIG. 2 shows an example host computer system 16 including example first and second memory modules 10, 26. As shown, the notification circuits 20, 30 of the first and second memory modules 10, 26 each comprise at least one transistor 36, 38. The at least one transistor 36, 38 can be in an open-drain configuration, as shown, although other configurations are possible. In certain such embodiments, the first state of the at least one first output 12 is a first logic level, the second state of the at least one first output 12 is a high-impedance state, the third state of the at least one second output 24 is the first logic level, and the fourth state of the at least one second output 24 is the high-impedance state. In the illustrated example, while the at least one initialization sequence is in progress, the first and second memory modules 10, 26 drive the gates of the respective transistors 36, 38 high. Thus, the transistors 36, 38 are respectively low impedance while the memory modules 10, 26 are executing each section of the initialization sequence, thereby pulling

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the first and second outputs 12, 24 low. Thus, the first state and the third state are low logic levels (ground) in the example configuration. Also, because the first and second outputs 12, 24 are coupled together by the bus 32, if the at least one initialization sequence of either one of the first and second memory modules 10, 26 are in progress, the bus 32 will be pulled to a low logic level.

[0038] As each of the two memory modules 10, 26 completes its at least one initialization sequence, it can drive the corresponding at least one first and second outputs 12, 24 respectively to a high impedance state, For example, once the at least one initialization sequence on each of the first and second memory modules 10, 26 is completed, the first and second memory modules 10, 26 can drive the gates of the respective transistors 36, 38 low, resulting in a high-impedance state on the at least one first and second outputs 12, 24 causing the bus 32 to be pulled high by the system memory controller 14. Accordingly, only once the at least one initialization sequence of both the first and second memory modules 10, 26 are complete, the bus 32 will be pulled high by the internal pull-up configuration 40 of the system memory controller 14. The second state and the fourth state are therefore high-impedance values in the example embodiment. Thus, the system memory controller 14 can monitor the value on the bus 32 via the first input 34 to determine when both of the memory modules 10, 26 have completed the at least one initialization sequence. As discussed, in other configurations the at least one first and second outputs 12, 24 may be received on separate inputs of the system memory controller 14, and the status of the at least one initialization sequence of each memory module 10, 26 may be monitored independently.

[0039] As discussed above, in certain embodiments in which more than one memory module 10, 26 is connected to the system memory controller 14, each memory module 10, 26 or associated controller circuit 18 (e.g., local memory controller) causes the corresponding notification circuit 20, 30 to drive the at least one output 12, 24 to the high impedance state from the low impedance state when it completes the requested or required operation. Thus, in certain such embodiments, the system memory controller 14 (e.g., MCH) can only pull the notifying signal high when all memory modules 10, 26 or associated controller circuits (e.g., local memory controllers) have completed the required or requested operation (e.g., initialization sequence). This configuration allows the system memory controller 14 (e.g., MCH) to work with a non-homogenous memory subsystem. For example, the system memory controller 14 may be able to monitor the progress of multiple memory modules 10, 26 including a mix of DIMMs or other memory modules having differing characteristics, such as DIMM density, rank configurations, DRAM density, speed,

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DRAM configuration, etc.

[0040] Additionally, the at least one output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are configured to be operatively coupled to at least one interrupt of the system memory controller 14 in certain embodiments. In certain such embodiments, the system memory controller 14 can be responsive to the second state of the first memory module 10 and the fourth state of the second memory module 26 by triggering execution of an interrupt routine by a processor of the system memory controller 14. For example, in the example system of FIG. 2, when the bus 32 is pulled high by the pull-up configuration 40 indicating the second state of the first memory module 10 and the fourth state of the second memory module 26, the system memory controller 14 triggers execution of the interrupt routine.

[0041] In some embodiments, in which the at least one first output 12 and the at least one second output 24 are operatively coupled to separate inputs of the system memory controller 14, the at least one first output 12 and the at least out second output 24 may be operatively coupled to two separate interrupts. For example, the system memory controller 14 may be responsive to the second state of the first memory module 10 by triggering execution of a first interrupt routine associated with a first interrupt, and may be responsive to the fourth state of the second memory module 26 by triggering execution of a second interrupt routine associated with the second interrupt. In yet other embodiments, the separate inputs of the memory controller 14 are internally operatively coupled to the same interrupt, or are operatively coupled to separate interrupts which trigger the same interrupt routine.

[0042] FIG. 3 shows a host computer system 16 including an example memory module 10 where the notification circuit 20 of the memory module 10 has another example configuration in accordance with certain embodiments described herein. In the example configuration of FIG. 3, the at least one first output 12 is operatively coupled to an error-out pin of the memory module 10, and a multiplexor 42 drives the transistor 36 with either of a task_in_progress signal 44 or an error signal 46 (e.g., parity error signal). In one embodiment, for example, the multiplexor 42 may be configured to drive the transistor 36 with the task_in_progress signal 44 when the memory module 10 is in the initialization mode or is executing the at least one initialization sequence, and with the error signal 46 when the memory module 10 is in the operational mode. Thus, the memory module 10 can be advantageously configured to both perform the standard (e.g., JEDEC-specified) error

reporting functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode, as described herein. As shown in FIG. 3, a second memory module 26 including a similar configuration can also be operatively coupled to the host computer system 16. In certain embodiments, the at least one second output 24 of the second memory module 26 can be operatively coupled to the at least one first output 12 by the bus 32, as described above (e.g., with respect to FIG. 2).

[0043] FIG. 4 shows an example method 100 of using the at least one memory module 10 in accordance with certain embodiments described herein. While the description below of the method 100 refers to structure shown in FIGS. 1-3, other structures may also be used in accordance with certain embodiments described herein. At block 102, the method 100 of certain embodiments comprises providing a first memory module 10 comprising at least one first output 12 operatively coupled to a memory controller 14 of a host computer system 16. The first memory module 10 can be configured to operate in at least two modes comprising an initialization mode during which the first memory module 10 executes at least one initialization sequence, and an operational mode. For example, the at least one initialization sequence may comprise one or more steps of a series of steps associated with an initialization procedure of the host computer system 16.

[0044] At block 104, the method 100 in some embodiments comprises causing the first memory module 10 to enter the initialization mode. At block 106, the method 100 of certain embodiments comprises driving the at least one first output 12 to a first state while the memory module 10 executes the at least one initialization sequence. Upon completion of the at least one initialization sequence, the method of certain embodiments comprises driving the at least one first output 12 to a second state different than the first state. In certain embodiments, the first state is a first logic level and the second state is a high impedance state. Additionally, in certain embodiments, the at least one first output 12 is operatively coupled to at least one interrupt of the memory controller 14 such that driving the at least one output 12 to the second state triggers the memory controller to execute an interrupt routine.

[0045] In certain embodiments, the at least one output 12 is operated in conformance with JEDEC standard when the first memory module 10 is in the operational mode, but is not operated in conformance with the JEDEC standard when the first memory module 10 is in the initialization mode. The at least one first output 12 of certain embodiments include an error-out pin of the first

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memory module, for example.

[0046] The method 100 can further include providing a second memory module 26 comprising at least one second output 24 operatively coupled to the memory controller 14. The second memory module 26 can be configured to operate in one of at least two modes comprising an initialization mode, during which the second memory module 26 executes at least one initialization sequence, and an operational mode. The method 100 can further include causing the second memory module 26 to enter the initialization mode. In certain embodiments, the method 100 also includes driving the at least one second output 24 of the second memory module 26 to a third state while the second memory module 26 executes the at least one initialization sequence. Upon completion of the at least one initialization sequence, the method 100 can further include driving the at least one second output 24 of the second memory module 26 to a fourth state different from the third state.

[0047] In certain embodiments, the at least one first output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are operatively coupled together by a bus 32 which is also operatively coupled to at least one input 34 of the memory controller 14. In certain other embodiments, the at least one first output 12 of the first memory module 10 is operatively coupled to a first input 34 of the memory controller 14 and the at least one second output 24 of the second memory module 26 is operatively coupled to a second input (not shown) of the memory controller 14.

[0048] FIG. 5 shows another example method 200 of using at least one memory module 10 in accordance with certain embodiments described herein. At block 202, the method 200 may include providing a memory module 10 comprising at least one output 12 operatively coupled to a memory controller 14 of a host computer system 16. The memory module 10 may be configured to operate in at least two modes comprising an initialization mode, during which the memory module 10 executes at least one initialization sequence, and an operational mode.

[0049] The method 200 can further include causing the memory module 10 to enter the initialization mode at block 204. At block 206, the method 200 can include receiving a notification signal from the at least one output 12 of the memory module 10. The notification signal may indicate that the memory module 10 has completed the initialization sequence, for example. In certain embodiments, the method 200 further comprises executing an interrupt routine by the memory controller 14 in response to the notification signal.

TERMINOLOGY/ALTERNATIVE EMBODIMENTS

[0050] Embodiments have been described in connection with the accompanying drawings. However, it should be understood that the figures are not drawn to scale. Distances, angles, etc. are merely illustrative and do not necessarily bear an exact relationship to actual dimensions and layout of the devices illustrated. In addition, the foregoing embodiments have been described at a level of detail to allow one of ordinary skill in the art to make and use the devices, systems, etc. described herein. A wide variety of variation is possible. Components, elements, and/or steps can be altered, added, removed, or rearranged. While certain embodiments have been explicitly described, other embodiments will become apparent to those of ordinary skill in the art based on this disclosure.

[0051] Conditional language used herein, such as, among others, "can," "could," "might," "may," "e.g.," and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment.

[0052] Depending on the embodiment, certain acts, events, or functions of any of the methods described herein can be performed in a different sequence, can be added, merged, or left out all together (e.g., not all described acts or events are necessary for the practice of the method). Moreover, in certain embodiments, acts or events can be performed concurrently, e.g., through multi-threaded processing, interrupt processing, or multiple processors or processor cores, rather than sequentially.

[0053] The various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein can be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design

constraints imposed on the overall system. The described functionality can be implemented in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the disclosure.

[0054] The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein can be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor can be a microprocessor, but in the alternative, the processor can be any conventional processor, controller, microcontroller, or state machine. A processor can also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0055] The blocks of the methods and algorithms described in connection with the embodiments disclosed herein can be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module can reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, a hard disk, a removable disk, a CD-ROM, or any other form of computer-readable storage medium known in the art. An exemplary storage medium is coupled to a processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium can be integral to the processor. The processor and the storage medium can reside in an ASIC. The ASIC can reside in a user terminal. In the alternative, the processor and the storage medium can reside as discrete components in a user terminal.

[0056] Certain embodiments described herein are compatible with a memory system including memory devices with various attributes (see, e.g., FIGS. 2 and 3). For example, the memory system of certain embodiments may include various data slice sizes (e.g., two, four, eight, or 16 bit data slices) and corresponding memories (e.g., memories having two, four, eight, or 16 bit data widths).

[0057] Although certain embodiments and examples are discussed above, it is understood that the inventive subject matter extends beyond the specifically disclosed embodiments to other alternative embodiments and/or uses of the invention and obvious modifications and equivalents

thereof. It is intended that the scope of the inventions disclosed herein should not be limited by the particular disclosed embodiments. Thus, for example, in any method or process disclosed herein, the acts or operations making up the method/process may be performed in any suitable sequence and are not necessarily limited to any particular disclosed sequence.

[0058] Various aspects and advantages of the embodiments have been described where appropriate. It is to be understood that not necessarily all such aspects or advantages may be achieved in accordance with any particular embodiment. Thus, for example, it should be recognized that the various embodiments may be carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other aspects or advantages as may be taught or suggested herein.

WHAT IS CLAIMED IS:

1. A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;

dynamic random access memory elements on the printed circuit board;

a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and

wherein the memory module is configurable to operate in any of at least a first mode and a second mode;

wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;

wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;

wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection from a first state to a second state, one of the first state and the second

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state being a low logic level and the other one of the first state and the second state being a high impedance state.

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ABSTRACT OF THE DISCLOSURE

According to certain aspects, a memory module is coupled to a memory controller of a host computer system via an interface. The memory module is configurable to be trained with one or more training sequences. The memory module is also configurable to communicate data signals with the memory module during normal memory read and write operations not associated with the one or more training sequences. The memory module has an open drain output for the one or more training sequences and for any parity error during the read and write operations.

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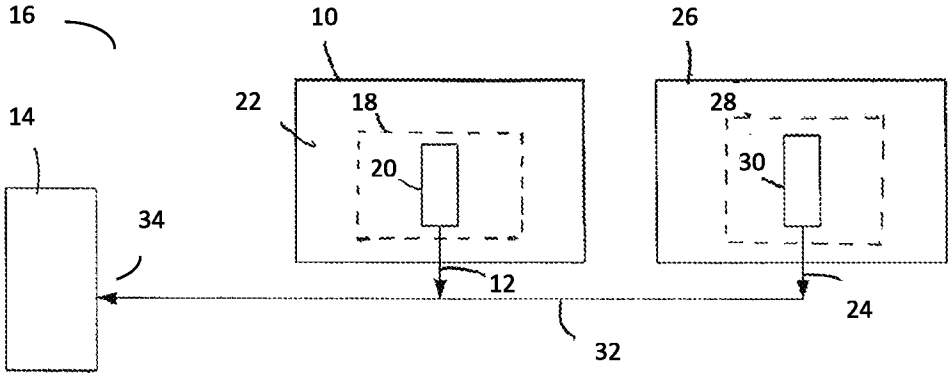


Figure 1

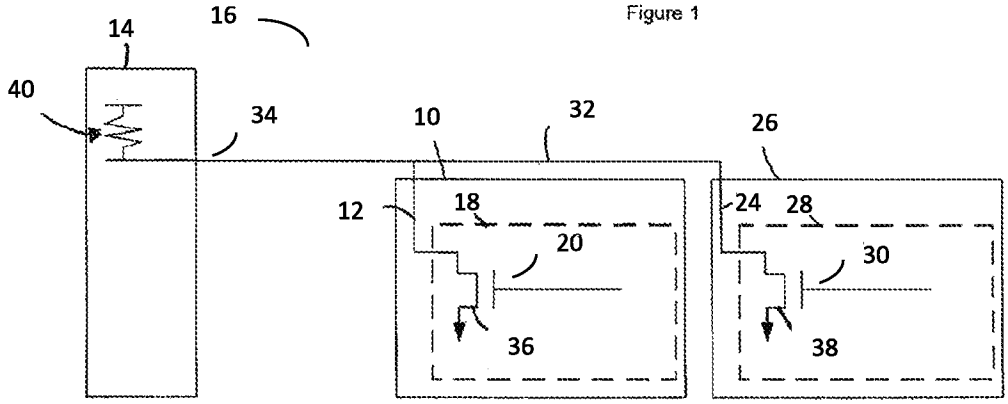


Figure 2

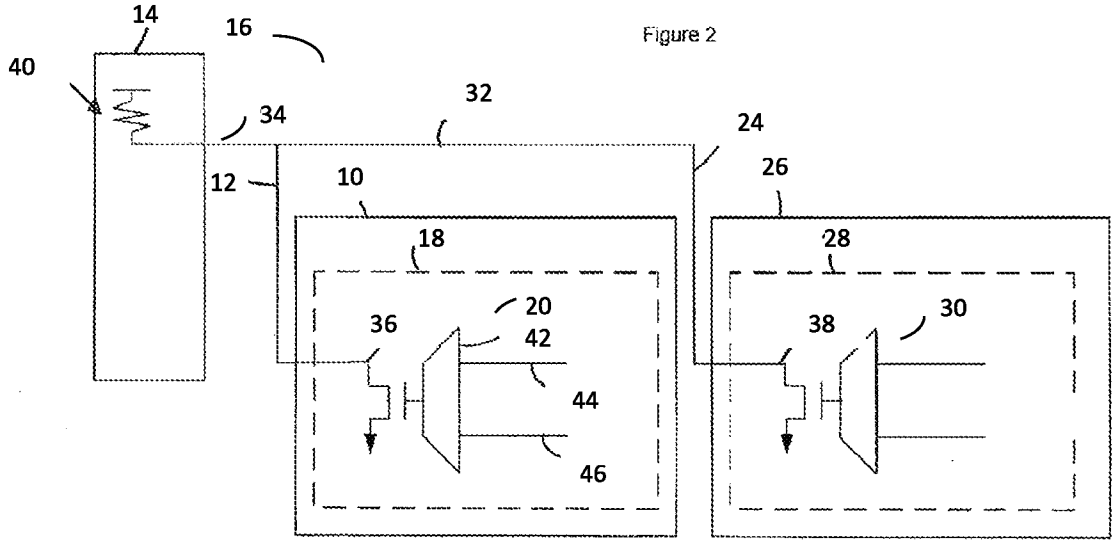


Figure 3

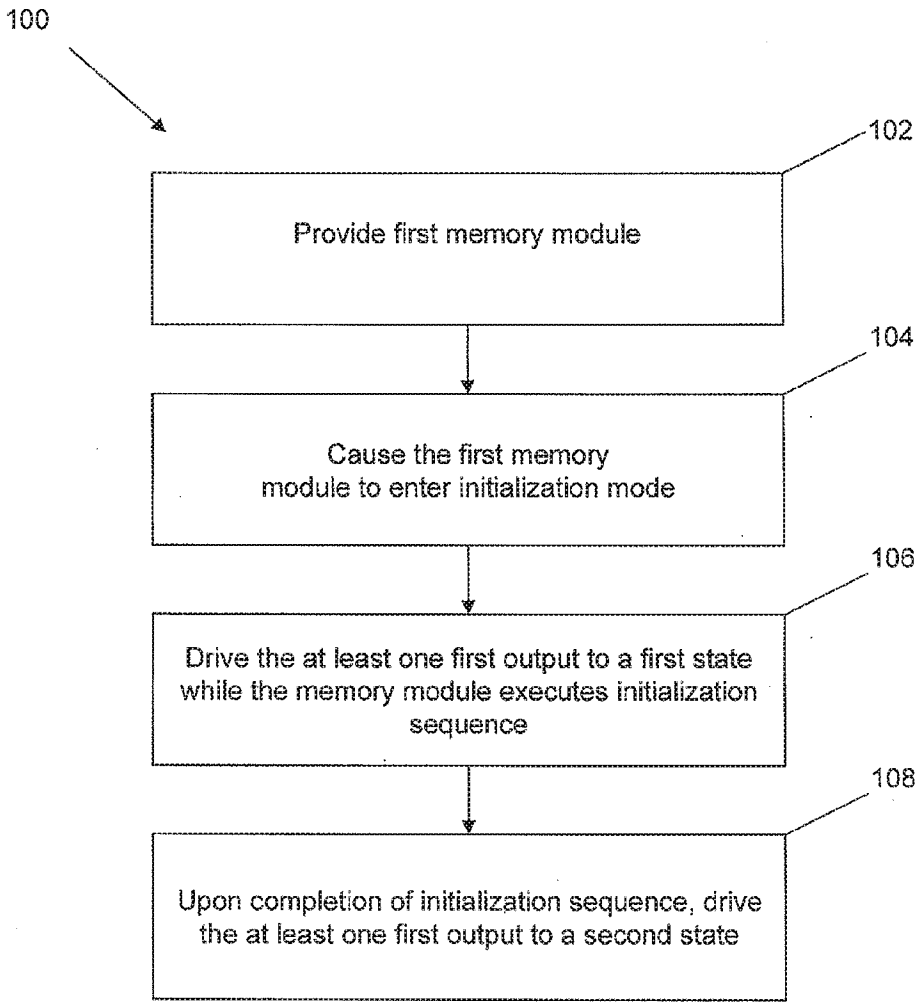

100
102
Provide first memory module
104
Cause the first memory module to enter initialization mode
106
Drive the at least one first output to a first state while the memory module executes initialization sequence
108
Upon completion of initialization sequence, drive the at least one first output to a second state

Figure 4

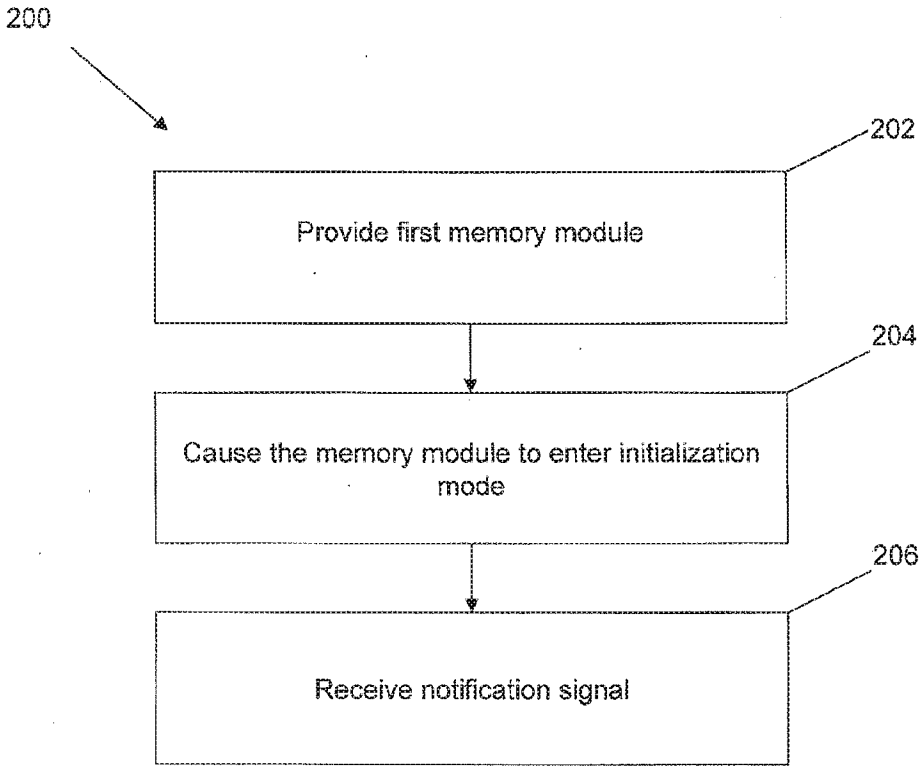

200
202
Provide first memory module
204
Cause the memory module to enter initialization mode
206
Receive notification signal

Figure 5

Electronic Acknowledgement Receipt

EFS ID:	37707345
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5066-US01
Receipt Date:	11-NOV-2019
Filing Date:	
Time Stamp:	16:51:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	129980-5066-US01_TRANSMITTAL.pdf	148650 0e3d6f958284a9b1d056b38bea53a649204fe372	no	1

Warnings:

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Information:					
2		129980-5066-US01_STMT_POA.pdf	148582 abc8df78e3f9e41e5cf6f1308be66e577c1f5168	yes	2

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Assignee showing of ownership per 37 CFR 3.73	1	1
Power of Attorney	2	2

Warnings:					
Information:					
3	Application Data Sheet	129980-5066-US01_ADS.pdf	1256465 8e094508f5efca123cabd47d725761b43fdba040	no	9
Warnings:					
Information:					
4		129980-5066US01_APPLN.pdf	217647 3b400f5ca923aed56ee701dcc9d11775e8c9b4ae	yes	23

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Specification	1	20
Claims	21	22
Abstract	23	23

Warnings:					
Information:					
5	Drawings-only black and white line drawings	129980-5066-US01-DRAWING.pdf	305870 b4bf38f2c294149f9ce60f1172ae0e9c2ca7aaa2	no	3
Warnings:					
Information:					
		Total Files Size (in bytes):	2077214		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/680,060	11/11/2019	Hyun Lee	129980-5066-US01

CONFIRMATION NO. 8269

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

FORMALITIES LETTER

OC000000112972433

Date Mailed: 12/02/2019

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

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Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Hyun Lee

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/bzewdie/

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/680,060

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE($)	FEE($)		RATE($)	FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1)		(Column 2)	(Column 3)					
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/680,060	11/11/2019	2139	0.00	129980-5066-US01	1	1

CONFIRMATION NO. 8269

FILING RECEIPT

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

OC000000112972432

Date Mailed: 12/02/2019

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Hyun Lee, Ladera Ranch, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 15/857,553 12/28/2017 PAT 10474595
which is a CON of 15/088,115 04/01/2016 PAT 9858218
which is a CON of 13/942,721 07/16/2013 PAT 9311116
which is a CON of 12/815,339 06/14/2010 PAT 8489837
which claims benefit of 61/186,799 06/12/2009

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

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Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 11/27/2019

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/680,060**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

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countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

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technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

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Electronically filed February 3, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2139
Filed:	November 11, 2019	Examiner:	TBD
For:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES	Attorney Docket No:	129980-5066-US01

RESPONSE TO THE NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

Mail Stop: MISSING PARTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice to File Missing Parts mailed December 2, 2019, enclosed is the Notice to File Missing Parts of Nonprovisional Application the above-identified application. The fee for the late oath or declaration surcharge is estimated to be $160.

Applicants note that an oath/declaration is also due. The oath/declaration will be submitted at a later date.

Also enclosed please find a Fee Transmittal Form setting forth the calculation for the statutory basic filing, search and examination fees, together with the excess claim fees due in this matter. The fees calculated for the statutory basic filing, search and examination fees together with the excess claim fees and application size fee (if applicable) are estimated to be $1720.

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The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5066-US01).

Respectfully submitted,

Date: February 3, 2020

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/680,060	11/11/2019	Hyun Lee	129980-5066-US01

CONFIRMATION NO. 8269

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

FORMALITIES LETTER

OC000000112972433

Date Mailed: 12/02/2019

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

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Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Hyun Lee

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/bzewdie/

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UTILITY PATENT APPLICATION FEE TRANSMITTAL *(Only for new nonprovisional applications under 37 CFR § 1.53(b))*	Attorney Docket No.	129980-5066-US01
	First Inventor	Hyun Lee
	Title	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
	Electronically filed	February 3, 2020

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BASIC FILING, SEARCH AND EXAMINATION FEES

Application Type	Filing Fees	Search Fees	Examination Fees	Fees Paid ($)
Utility	$ 300	$ 660	$ 760	$ 1720

EXCESS CLAIM FEES

Type	No. Filed	Less	Extra	Extra Rate ($)	Fee ($)
Total Claims	1	- 20	0	$ 100 each	0
Independent	1	- 3	0	$ 460 each	0
			Surcharge for late filing fees		160

APPLICATION SIZE FEE (Specification and Drawings)

Total Sheets	Extra Sheets	No. of each add'l 50 or fraction thereof	Fee ($)
26 x .75- 100	0 / 50	0 (round up to whole no.) x $400	0

Sub Total	$1,880
Applicant qualifies for the 50% Reduction for Independent Inventor, Nonprofit Organization or Small Business Concern minus electronic filing discount of $75	
TOTAL FILING FEE	**$1880**

Please charge the total filing fee and any other additional fees to Morgan, Lewis & Bockius LLP Deposit Account 50-0310 (order no. 129980-5066-US01).

Respectfully submitted,

Date: February 3, 2020

/Jamie J. Zheng/

Jamie J. Zheng — 51,167 (Reg. No.)

MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Electronic Patent Application Fee Transmittal

Application Number:	16680060
Filing Date:	11-Nov-2019
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng/S. Olivier
Attorney Docket Number:	129980-5066-US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				

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Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1880**

Electronic Acknowledgement Receipt

EFS ID:	38479753
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5066-US01
Receipt Date:	03-FEB-2020
Filing Date:	11-NOV-2019
Time Stamp:	20:12:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1880
RAM confirmation Number	E202023K12321254
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5066-US0RES_FEE.pdf	266554 6428a142f685b94b459721ce6b7d4442cfbd1564	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Response to Pre-Exam Formalities Notice	1	4
	Fee Worksheet (SB06)	5	5

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	37138 17cc2ef6de3287635c437a858be1b4f2aa569352	no	2

Warnings:

Information:

Total Files Size (in bytes):	303692

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed February 5, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2139
Filed:	November 11, 2019	Examiner:	TBD
For:	*Memory Module Having An Open-Drain Output For Parity Error And For Training Sequences*	Attorney Docket No.:	129980-5066-US01

MISCELLANEOUS COMMUNICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Applicant concurrently submits with this Communication the inventors' Oath/Declaration in this matter.

No additional fees are believed due at this time; however, the Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5066-US01).

Respectfully submitted,

Date: February 5, 2020

/ Jamie J. Zheng / 51,167
Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

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Customer No. 79141
Attorney Docket No.: NETL.062C1A

COMBINED DECLARATION AND ASSIGNMENT FOR UTILITY OR DESIGN APPLICATION

Title of Invention	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

DECLARATION

As a below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 13/942,721 filed on July 16, 2013 .

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) and other good and valuable consideration paid, I hereby sell and assign to

Netlist, Inc.
(Name of Assignee)

of 51 Discovery, Suite #150, Irvine, CA 92618
(Address of Assignee)

(hereinafter designated as the Assignee) my entire right, title and interest for the United States as defined in 35 USC 100, for any invention set forth in the above-identified application.

I agree to execute all papers necessary in connection with this application for patent in the USPTO for the invention, and any continuation, divisional or reissue applications thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient.

I agree to execute all papers necessary in connection with any post-grant proceeding which may occur in connection with this application or continuation, divisional or reissue thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such post-grant proceeding.

I agree to execute all papers and documents and perform any act which may be necessary in connection with claims or provisions of the International Convention for Protection of Industrial Property or similar agreements.

I agree to perform all affirmative acts which may be necessary to obtain a grant of a valid United States patent to the Assignee.

I hereby authorize and request the USPTO to issue any and all Letters Patents of the United States resulting from the application or any continuation, divisional or reissue applications thereof to the Assignee, as Assignee of my entire interest, and covenant that I have not executed, and will not execute, any agreement in conflict herewith.

First Inventor (Legal Name): Hyun Lee

Signature: _____ Date: 10/9/2013

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Electronic Acknowledgement Receipt

EFS ID:	38504770
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5066-US01
Receipt Date:	05-FEB-2020
Filing Date:	11-NOV-2019
Time Stamp:	19:18:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5066US01_MIS_COM_DECL.pdf	726122 82144bb2d2c89371064dabe1163f6706188aad40	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Oath or Declaration filed	2	3
Warnings:			
Information:			
	Total Files Size (in bytes):	726122	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/680,060	11/11/2019	2139	1880	129980-5066-US01	1	1

CONFIRMATION NO. 8269

UPDATED FILING RECEIPT

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

OC000000114474970

Date Mailed: 02/07/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Hyun Lee, Ladera Ranch, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 15/857,553 12/28/2017 PAT 10474595
which is a CON of 15/088,115 04/01/2016 PAT 9858218
which is a CON of 13/942,721 07/16/2013 PAT 9311116
which is a CON of 12/815,339 06/14/2010 PAT 8489837
which claims benefit of 61/186,799 06/12/2009

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

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Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 11/27/2019

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/680,060**

Projected Publication Date: 05/14/2020

Non-Publication Request: No

Early Publication Request: No

Title

MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

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countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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Ex. 1002, p. 66

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/680,060	11/11/2019	Hyun Lee	129980-5066-US01

CONFIRMATION NO. 8269

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

INFORMAL NOTICE

OC00000014474971

Date Mailed: 02/07/2020

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Hyun Lee

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/mnguyen/

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/680,060

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE($)	FEE($)		RATE($)	FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1)		(Column 2)	(Column 3)					
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/680,060	Filing Date 11/11/2019	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	03/05/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LDRC
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/EVA V GILLIS/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

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Electronically filed March 5, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2133
Filed:	Novemver 11, 2019	Examiner:	Rutz, Jared Ian
For:	*Memory Module Having An Open-Drain Output For Parity Error And For Training Sequences*	Attorney Docket No.:	129980-5066-US01

PRELIMINARY AMENDMENT

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Please enter the enclosed preliminary amendment.

The Commissioner is hereby authorized to charge any required fees or credit any overpayments to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5066-US01).

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Ex. 1002, p. 70

Amendments to the Specification

Please revise the specification as shown below:

Please amend the abstract as follows:

~~According to certain aspects, a memory module is coupled to a memory controller of a host computer system via an interface. The memory module is configurable to be trained with one or more training sequences. The memory module is also configurable to communicate data signals with the memory module during normal memory read and write operations not associated with the one or more training sequences. The memory module has an open drain output for the one or more training sequences and for any parity error during the read and write operations~~

According to certain embodiments, a memory module is operable with a memory controller of a host system. The memory module includes a module controller configurable to receive address and control signals from the memory controller, and dynamic random access memory elements configurable to communicate data signals with the memory controller in accordance with the address and control signals. The module controller has an open-drain output and is configurable to drive the open-drain output with a first signal to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation. The module controller is further configurable to drive the open drain output with a second signal related to one or more training sequences when the memory module performs operations associated with the one or more training sequences and not associated with any normal memory read or write operations.

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Ex. 1002, p. 71

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (New) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

a module controller on the printed circuit board and configurable to receive address and control signals associated with normal memory read or write operations via the first edge connections; and

dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and

wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

wherein the module controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation; and

wherein the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and not associated with any normal memory read or write operations.

3. (New) The memory module of claim 2, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second state

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Ex. 1002, p. 72

being a low logic level and the other one of the first state and the second state being a high impedance state.

4. (New) The memory module of claim 3, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state.

5. (New) The memory module of claim 2, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to ground, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.

6. (New) The memory module of claim 5, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.

7. (New) The memory module of claim 2, wherein the module controller comprises an integrated circuit that includes the transistor.

8. (New) The memory module of claim 2, wherein the memory module is configurable to perform the operations associated with the one or more training sequences without communicating data signals with the memory controller via the second edge connections.

9. (New) The memory module of claim 2, wherein the second edge connections are not active during the operations associated with the one or more training sequences.

10. (New) The memory module of claim 2, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configurable to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.

11. (New) A method of operation in a host system having a memory controller, comprising:

at a memory module coupled to the memory controller, the memory module including a printed circuit board, a module controller on the printed circuit board, and dynamic random

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Ex. 1002, p. 73

access memory elements on the printed circuit board, the printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections, the module controller including a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

receiving, at the module controller, address and control signals associated with one or more normal memory read or write operations from the memory controller via the first edge connections;

outputting or receiving data signals at the dynamic random access memory elements in accordance with the address and control signals, the data signals being communicated with the memory controller via the second edge connections;

applying a first signal to the gate of the transistor to indicate a parity error having occurred during one of the normal memory read or write operations;

performing training operations associated with one or more training sequences and not associated with any normal memory read or write operations; and

applying a second signal related to the one or more training sequences to the gate of the transistor while the memory module performs the training operations.

12. (New) The method of claim 11, wherein the error edge connection is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

13. (New) The method of claim 12, wherein the error edge connection is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state.

14. (New) The method of claim 11, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to ground, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.

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Ex. 1002, p. 74

15. (New) The method of claim 14, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.

16. (New) The method of claim 11, wherein the module controller comprises an integrated circuit that includes the transistor.

17. (New) The method of claim 11, wherein the memory module performs the training operations associated with the one or more training sequences without communicating data signals with the memory controller via the second edge connections.

18. (New) The method of claim 11, wherein the second edge connections are not active during the training operations associated with the one or more training sequences.

19. (New) The method of claim 11, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein applying the first signal to the gate of the transistor includes coupling the first input to the output, and applying the second signal to the gate of the transistor includes coupling the second input to the output.

20. (New) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

a module controller on the printed circuit board and configurable to receive from the memory controller via the first edge connections address and control signals associated with normal memory read or write operations; and

dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and

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Ex. 1002, p. 75

wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

wherein the module controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation;

wherein the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and not associated with any normal memory read or write operations;

wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground;

wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to ground, and drives the gate of the transistor low so as to drive the error edge connection to a high impedance state;

wherein the module controller comprises an integrated circuit that includes the transistor; and

wherein the integrated circuit further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configurable to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.

21. (New) The memory module of claim 20, wherein the second signal drives the error edge connection from the high impedance state to ground and from ground to the high impedance state.

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Ex. 1002, p. 76

REMARKS CONCERNING CLAIMS

Claim 1 is cancelled, and new claims 2-21 are added. Support for the new claims can be found throughout the specification with reference to the drawings. Therefore, no new matter is added.

CONCLUDING REMARKS

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner consider this application with a view towards allowance. **The Examiner is invited to call the undersigned attorney at (650) 843-7249, if a telephone call could help resolve any remaining items.**

Respectfully submitted,

Date: March 5, 2020

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-7278

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Ex. 1002, p. 77

Electronic Acknowledgement Receipt

EFS ID:	38785470
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5066-US01
Receipt Date:	05-MAR-2020
Filing Date:	11-NOV-2019
Time Stamp:	19:02:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5066-US01_PRE_AMD.pdf	149446 641c3f7119c1cd2700e40ef0c0dba4ef359564c2	yes	8

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	Preliminary Amendment	1	1
	Specification	2	2
	Claims	3	7
	Applicant Arguments/Remarks Made in an Amendment	8	8
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed April 13, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2133
Filed:	Novemver 11, 2019	Examiner:	Rutz, Jared Ian
For:	*Memory Module Having An Open-Drain Output For Parity Error And For Training Sequences*	Attorney Docket No.:	129980-5066-US01

SUPPLEMENTAL PRELIMINARY AMENDMENT

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Please enter the enclosed supplemental preliminary amendment.

The Commissioner is hereby authorized to charge any required fees or credit any overpayments to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5066-US01).

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Ex. 1002, p. 80

Amendments to the Specification

Please revise the specification as shown below:

Please amend Paragraph [0007] as follows:

[0007] In certain embodiments, a memory module is operable with a memory controller of a host system and comprises a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections. The memory module further comprises dynamic random access memory elements on the printed circuit board, and a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection. The memory module is configurable to operate in any of at least a first mode and a second mode. The memory module in the [[~~first~~]] second mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections. The memory module in the [[second]] first mode is not accessed by the memory controller for normal memory read or write operations, and is configurable to perform operations related to one or more training sequences.

Please amend Paragraph [0008] as follows:

[0008] In certain embodiments, the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, and the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals. The module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the [[first]] second mode. The module controller in the [[second]] first mode is further configurable to provide information related to the one or more training sequences by driving the open drain output

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Ex. 1002, p. 81

and the error edge connection from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

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Ex. 1002, p. 82

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Previously Presented) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

a module controller on the printed circuit board and configurable to receive address and control signals associated with normal memory read or write operations via the first edge connections; and

dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and

wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

wherein the module controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation; and

wherein the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and not associated with any normal memory read or write operations.

3. (Previously Presented) The memory module of claim 2, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and

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the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

4. (Previously Presented) The memory module of claim 3, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state.

5. (Currently Amended) The memory module of claim [[2]]3, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to [[ground]]the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.

6. (Previously Presented) The memory module of claim 5, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.

7. (Previously Presented) The memory module of claim 2, wherein the module controller comprises an integrated circuit that includes the transistor.

8. (Previously Presented) The memory module of claim 2, wherein the memory module is configurable to perform the operations associated with the one or more training sequences without communicating data signals with the memory controller via the second edge connections.

9. (Previously Presented) The memory module of claim 2, wherein the second edge connections are not active during the operations associated with the one or more training sequences.

10. (Previously Presented) The memory module of claim 2, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configurable to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.

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11. (Previously Presented) A method of operation in a host system having a memory controller, comprising:

at a memory module coupled to the memory controller, the memory module including a printed circuit board, a module controller on the printed circuit board, and dynamic random access memory elements on the printed circuit board, the printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections, the module controller including a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

receiving, at the module controller, address and control signals associated with one or more normal memory read or write operations from the memory controller via the first edge connections;

outputting or receiving data signals at the dynamic random access memory elements in accordance with the address and control signals, the data signals being communicated with the memory controller via the second edge connections;

applying a first signal to the gate of the transistor to indicate a parity error having occurred during one of the normal memory read or write operations;

performing training operations associated with one or more training sequences and not associated with any normal memory read or write operations; and

applying a second signal related to the one or more training sequences to the gate of the transistor while the memory module performs the training operations.

12. (Previously Presented) The method of claim 11, wherein the error edge connection is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

13. (Previously Presented) The method of claim 12, wherein the error edge connection is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state.

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14. (Currently Amended) The method of claim [[13]]12, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level [[ground]], and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.

15. (Previously Presented) The method of claim 14, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.

16. (Previously Presented) The method of claim 11, wherein the module controller comprises an integrated circuit that includes the transistor.

17. (Previously Presented) The method of claim 11, wherein the memory module performs the training operations associated with the one or more training sequences without communicating data signals with the memory controller via the second edge connections.

18. (Previously Presented) The method of claim 11, wherein the second edge connections are not active during the training operations associated with the one or more training sequences.

19. (Previously Presented) The method of claim 11, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein applying the first signal to the gate of the transistor includes coupling the first input to the output, and applying the second signal to the gate of the transistor includes coupling the second input to the output.

20. (Currently Amended) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

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a module controller on the printed circuit board and configurable to receive from the memory controller via the first edge connections address and control signals associated with normal memory read or write operations; and

dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and

wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

wherein the module controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation;

wherein the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and not associated with any normal memory read or write operations;

wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground;

wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to a low impedance state[[~~-ground~~]], and drives the gate of the transistor low so as to drive the error edge connection to a high impedance state;

wherein the module controller comprises an integrated circuit that includes the transistor; and

wherein the integrated circuit further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configurable to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.

21. (Currently Amended) The memory module of claim 20, wherein the second signal drives the error edge connection from the high impedance state to the low impedance state [[~~ground -~~]]and from the low impedance state[[~~-ground~~]] to the high impedance state.

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REMARKS

The specification and claims have been amended to address minor issues with clarity and consistency. No new matter is added.

CONCLUDING REMARKS

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner consider this application with a view towards allowance. **The Examiner is invited to call the undersigned attorney at (650) 843-7249, if a telephone call could help resolve any remaining items.**

Respectfully submitted,

Date: April 13, 2020

/Jamie J. Zheng/ 51,167

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Electronic Acknowledgement Receipt

EFS ID:	39145854
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5066US01_SUPP_PRE_AMD.pdf	134358 3c94ec7a3c79ef12e2e151627b4e66d2697af7bf	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Supplemental Response or Supplemental Amendment	1	1
	Specification	2	3
	Claims	4	8
	Applicant Arguments/Remarks Made in an Amendment	9	9
Warnings:			
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 1, 2020	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2139
				Examiner Name	To be assigned
Sheet	1	of	8	Attorney Docket Number	129980-5066US01

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				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2139
				Examiner Name	To be assigned
Sheet	2	of	8	Attorney Docket Number	129980-5066US01

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Examiner Initials	Cite No.	Foreign Patent Document Country Code[3] – Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter partes review Case No. IPR2017-00548, Petition For Inter Partes Review Of U.S. Patent No. 8,489,837, filed December 30, 2016.
		Inter partes review Case No. IPR2017-00548, Power of Attorney of Petitioners, filed December 30, 2016.
		Inter partes review Case No. IPR2017-00548, Exhibit 1002 "File History", filed December 30, 2016.
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 1, 2020	
				Application Number	16/680,060
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				First Named Inventor	Hyun Lee
				Art Unit	2139
				Examiner Name	To be assigned
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Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 1, 2020	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2139
				Examiner Name	To be assigned
Sheet	4	of	8	Attorney Docket Number	129980-5066US01

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Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 1, 2020	
				Application Number	16/680,060
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				First Named Inventor	Hyun Lee
				Art Unit	2139
				Examiner Name	To be assigned
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Examiner Signature		Date Considered	

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				First Named Inventor	Hyun Lee
				Art Unit	2139
				Examiner Name	To be assigned
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		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Petitioners Motion to Exclude, filed November 30, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Petitioners' Request for Oral Argument, filed November 30, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Patent Owner Request For Oral Argument, filed November 30, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Patent Owner Submission Of ITC Claim Construction Order, filed November 30, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Patent Owner Motion To Exclude, filed November 30, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Petitioners Opposition to Patent Owner's Motion to Exclude, filed December 14, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Patent Owner's Opposition to Petitioner's Motion to Exclude Evidence, filed December 14, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Petitioners' Reply in Support of its Motion to Exclude, filed December 21, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Patent Owner Reply To Petitioner Opposition To Motion To Exclude, filed December 21, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Patent Owner Demonstratives, filed February 4, 2019
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Petitioners' Demonstratives, filed February 4, 2019
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Notice of Accord Filing Date - Defective Petition, filed December 19, 2017
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Notice of Accepting Corrected Petition, filed December 19, 2017
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Trial Instituted Document, filed May 24, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Conduct of the Proceeding 37 C.F.R. § 42.5, filed November 30, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Order - Trial Hearing - 37 CFR 42.70, filed January 16, 2019
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Hearing Transcript, filed February 26, 2019

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 1, 2020	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2139
				Examiner Name	To be assigned
Sheet	7	of	8	Attorney Docket Number	129980-5066US01

		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 2001, 'Exhibit 2001,' filed March 19, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 2002, 'Exhibit 2002,' filed March 19, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 2003, 'Exhibit 2003,' filed March 19, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 2004, 'Exhibit 2004,' filed March 19, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 2005, 'Exhibit 2005,' filed August 10, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 2006, 'Exhibit 2006,' filed August 10, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 2007, 'Exhibit 2007,' filed August 10, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 2008, 'Exhibit 2008,' filed August 10, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 2009, 'Exhibit 2009,' filed August 10, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 2010, 'Exhibit 2010,' filed November 30, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1025, '337-TA-1023, Initial Determination (Excerpts),' filed December 14, 2017
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1026, 'Murphy Deposition Transcript in IPR2017-00548 (837 Patent),' filed December 14, 2017
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1028, 'Patent Owner's Dictionary (Exhibit 2009 in IPR2017-00548),' filed December 14, 2017
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1003, 'Declaration of Donald Alpert,' filed December 4, 2017
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1003, 'Corrected Declaration of Donald Alpert,' filed December 19, 2017
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1030, 'Declaration of Brian Nester PHV,' filed October 18, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1032, 'Annotated Page 37 of Ex. 2005,' filed November 9, 2018

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 1, 2020	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2139
				Examiner Name	To be assigned
Sheet	8	of	8	Attorney Docket Number	129980-5066US01

		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1034, 'ITC Expert Report of Robert Mr. Murphy Regarding 623 Patent (Public Version),' filed November 9, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1033, 'Annotated Page 18 of Ex. 2005,' filed November 9, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1035, 'Mr. Murphy 623 IPR Deposition Transcript (October 25, 2018),' filed November 9, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1036, 'Mr. Murphy 623 ITC Deposition Transcript (October 19, 2018),' filed November 9, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1037, 'JEDEC Standard (JESD79-3),' filed November 9, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Final Written Decision, filed March 21, 2019

Examiner Signature		Date Considered	

Electronic Acknowledgement Receipt

EFS ID:	40448547
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5066-US01
Receipt Date:	02-SEP-2020
Filing Date:	11-NOV-2019
Time Stamp:	00:50:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	129980-5066-US01_IDS_Transmittal_2020-09-01.pdf	124420 5d34f228687486a585ea310402bfdb83decba7a12	no	4

Warnings:

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Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	129980-5066-US01_IDS_List_2020_09-01.pdf	130194 d75666a560e610367b622919652af60708b9e738	no	8

Warnings:
Information:
This is not an USPTO supplied IDS fillable form

Total Files Size (in bytes):	254614

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed September 1, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2139
Filed:	November 11, 2019	Examiner:	To be assigned
For:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES	Attorney Docket No.:	129980-5066US01

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

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Ex. 1002, p. 102

2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☒ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

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Ex. 1002, p. 103

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☒ Copies of publications listed on Form PTO-1449 from prior application Serial No. 15/857,553, filed on December 28, 2017, 15/088,115, filed on April 1, 2016, 13/942,721, filed on July 16, 2013, and 12/815,339, filed on June 14, 2010, of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

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Ex. 1002, p. 104

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5066US01).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: September 1, 2020

/Jamie J. Zheng/ 51,167

Jamie Jie Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Samsung Electronics Co., Ltd.
Ex. 1002, p. 105

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 1, 2020	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2139
				Examiner Name	To be assigned
Sheet	1	of	1	Attorney Docket Number	129980-5066US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.[1]	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code[3] – Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Patent Owner Demonstratives, filed February 4, 2019
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Petitioner's Owner Demonstratives, filed February 4, 2019
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Hearing Transcript, Issued February 26, 2019

Examiner Signature		Date Considered	

Electronic Acknowledgement Receipt

EFS ID:	40448614
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5066-US01
Receipt Date:	02-SEP-2020
Filing Date:	11-NOV-2019
Time Stamp:	02:25:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	129980-5066-US01_IDS-2_Transmittal_2020-09-01.pdf	124286 350b6fa69ee06ed0ad6d000c75acceec4142387c	no	4

Warnings:

Samsung Electronics Co., Ltd.
Ex. 1002, p. 107

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	129980-5066-US01_IDS_List-2_2020_09-01.pdf	97367 5d89097dac92fc8fa354d66b440e42a8d1ca991b	no	1
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Information:					
This is not an USPTO supplied IDS fillable form					
3	Non Patent Literature	IPR2018-00303_PO_Demonstratives.pdf	2943419 1cda4157dd6b09df481d80d58ff12eb452775a50	no	35
Warnings:					
Information:					
4	Non Patent Literature	623_Petitioners_Demonstratives.pdf	14291337 ab13635df1b9269902e1fc59e301ebb232224e6a	no	70
Warnings:					
Information:					
5	Non Patent Literature	IPR2018-00303_hearing.pdf	284920 2f8dfbbf70d9a3e34fc3667de0a7a632c9a1b0e4	no	50
Warnings:					
Information:					
		Total Files Size (in bytes):	17741329		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed September 1, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2139
Filed:	November 11, 2019	Examiner:	To be assigned
For:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES	Attorney Docket No.:	129980-5066US01

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

Samsung Electronics Co., Ltd.
Ex. 1002, p. 109

2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☒ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

Samsung Electronics Co., Ltd.
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5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial No. 15/857,553, filed on December 28, 2017, 15/088,115, filed on April 1, 2016, 13/942,721, filed on July 16, 2013, and 12/815,339, filed on June 14, 2010, of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☒ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☒ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

Samsung Electronics Co., Ltd.
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8a. ☒ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on even date herewith. A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein.

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5066US01).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: September 1, 2020

/Jamie J. Zheng/ 51,167

Jamie Jie Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Samsung Electronics Co., Ltd.
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 1, 2020	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2139
				Examiner Name	To be assigned
Sheet	1	of	1	Attorney Docket Number	129980-5066US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.[1]	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code[3] – Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Commission Opinion, United States International Trade Commission, Certain Memory Modules and Components Thereof, Investigation No. 337-TA-1089, 21APR2020, 30 pgs.

Examiner Signature		Date Considered	

Electronic Acknowledgement Receipt

EFS ID:	40448684
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5066-US01
Receipt Date:	02-SEP-2020
Filing Date:	11-NOV-2019
Time Stamp:	03:37:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	ITC_Commission-Opinion-1089-Public.pdf	345044 8bf381a2419eed91806f2c37caa532bd350d0d51	no	30

Warnings:

Samsung Electronics Co., Ltd.
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Information:					
2	Transmittal Letter	129980-5066-US01_IDS-3_Transmittal_2020-09-01.pdf	124285 78ac4972546f8509d618b3e56bc9d68d0dd8cb53	no	4
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	129980-5066-US01_IDS_List-3_2020_09-01.pdf	97298 46c5bb6cddd1bb83d382bf655eddf03a650e4fd1	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
Total Files Size (in bytes):			566627		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed September 2, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2139
Filed:	November 11, 2019	Examiner:	To be assigned
For:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES	Attorney Docket No.:	129980-5066US01

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

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2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☒ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

Samsung Electronics Co., Ltd.
Ex. 1002, p. 117

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial No. 15/857,553, filed on December 28, 2017, 15/088,115, filed on April 1, 2016, 13/942,721, filed on July 16, 2013, and 12/815,339, filed on June 14, 2010, of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☒ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☒ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

Samsung Electronics Co., Ltd.
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8a. ☒ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on September 1, 2020. A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein.

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5066US01).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: September 2, 2020

/Jamie J. Zheng/ 51,167

Jamie Jie Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Samsung Electronics Co., Ltd.
Ex. 1002, p. 119

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/680,060	11/11/2019	Hyun Lee	129980-5066-US01	8269

79141 7590 09/03/2020

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2133	

NOTIFICATION DATE	DELIVERY MODE
09/03/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

padocketingdepartment@morganlewis.com
vskliba@morganlewis.com

Samsung Electronics Co., Ltd.
Ex. 1002, p. 120

Office Action Summary	Application No. 16/680,060	Applicant(s) Lee, Hyun	
	Examiner MARDOCHEE CHERY	Art Unit 2133	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 11/11/2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 2-21 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 2-21 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 11/11/2019 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP § 2146 *et seq.* for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed

determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. **A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp**.

3. Claims 1-21 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-24 of U.S. Patent No. 10,474,595; claims 1-22 of U.S. Patent No. 9,858,218. Although the claims at issue are not identical, they are not patentably distinct from each other because the claims of the issued patents make obvious the claims of the pending application.

4. "A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARDOCHEE CHERY whose telephone number is (571)272-4246. The examiner can normally be reached from 900-500.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Jared Rutz** can be reached on **(571)272-5535**. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Respectfully Submitted,
USPTO

Dated: August 30, 2020

By: /MARDOCHEE CHERY/
Primary Examiner
Art Unit 2133
Email:Mardochee.Chery@uspto.gov
Telephone: 571-272-4246
Facsimile: 571-273-4246

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/680,060	Lee, Hyun
	Examiner	Art Unit
	MARDOCHEE CHERY	2133

CPC - Searched*		
Symbol	Date	Examiner
(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2029/4402 or G11C2207/2254)	08/30/2020	MC

CPC Combination Sets - Searched*		
Symbol	Date	Examiner
(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2029/4402 or G11C2207/2254)	08/30/2020	MC

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	154	08/30/2020	MC

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST; Inventor; Assignee; CPC	08/30/2020	MC

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	08/30/2020

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Ex. 1002, p. 125

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/680,060	Lee, Hyun
	Examiner	Art Unit
	MARDOCHEE CHERY	2133

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/30/2020								
	1	-								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								
	15	✓								
	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								
	21	✓								

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	36,607	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
L2	55	L1 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
L3	25	L2 and (open$3 near2 drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
L4	13	L3 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
L5	162,327	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
L6	5,271	L5 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25

L7	31	L6 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
L8	15	L7 and (open$3 near2 drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
L9	1	L8 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
L10	0	L9 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
L11	52,734	(LEE near2 HYUN).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:26
L12	18,670	L11 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:26
L13	8	L12 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:26
L14	0	L13 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:26

L15	162,327	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2029/4402 or G11C2207/2254).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:29
L16	5,271	L15 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:32
L17	31	L16 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:32
L18	6	L17 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:34
L19	211	netlist.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:35
L20	6	L19 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:35
L21	1	L20 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:36

8/30/2020 8:37:15 PM
C:\Users\mchery\Documents\EAST\Workspaces\13942721.wsp

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 4, 2020	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
Sheet	1	of	2	Attorney Docket Number	129980-5066US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		8,407,441 B2	03-26-2013	Giovannini et al.	
		8,386,737 B2	02-26-2013	Jeon et al.	
		7,222,213 B2	05-22-2007	James	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1015, 'JEDEC COMMITTEE LETTER BALLOT, LRDIMM DDR3 Memory Initialization Chapter Proposal (Dec. 2009) ("JEDEC"),' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1003, 'Declaration of Donald Alpert,' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1039, 'Inphi Corporation, MB Initialization sequence Item 142.35, June 4, 2009,' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1026, 'JEDEC Standard, FBDIMM Advanced Memory Buffer (AMB) (March 2007)("JESD82-20A"),' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1029, 'JEDEC Standard, Low Power Double Data Rate (LPDDR) SDRAM Specification (August 2007) ("JESD209"),' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1036, 'JEDEC COMMITTEE LETTER BALLOT, DDR3 LRDIMM Design Specification Body (Dec. 2009),' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1042, '"Sequence," https://www.lexico.com/en/definition/sequence,' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1044, '"28-Bit to 56-Bit Registered Buffer with Address Parity Test One Pair to Four Pair Differential Clock PLL Driver" Texas Instruments (October 2008),' filed June 9, 2020

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 4, 2020	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
Sheet	2	of	2	Attorney Docket Number	129980-5066US01

		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1045, '"High-Speed DRAM Controller Design" Micron (2008),' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1046, '"Minutes of Meeting No. 158 JC-40 Digital Logic Committee" JEDEC (June 4, 2009),' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1050, 'Declaration of Julie Carlson,' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1054, 'Declaration of John Halbert,' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1056, 'JEDEC Stanard, DDR3 SDRAM, JESD79-3C (November 2008) ("JESD79-3C"),' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, PAPER 1, 'Petition for Inter Partes Review of U.S. Patent No. 10,474,595,' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1051, 'JEDEC, "Committee Letter Ballot, JC-40.4-09-320, Item 142.35," (Dec. 2009),' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1052, 'JEDEC, "Committee Letter Ballot, JC-45.4-09-321, Item 2192.44," (Dec. 2009),' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1055, 'Declaration of Roland Knaack,' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1025, 'JEDEC Standard, FBDIMM: Architecture and Protocol (January 2007) ("JESD206"),' filed June 9, 2020
		Inter Partes Review No. 2020-01044 of US Patent No. 9858218, Case No. IPR2020-01044, EXHIBITS 1003, 'Declaration of Donald Alpert,' filed June 9, 2020
		Inter Partes Review No. 2020-01044 of US Patent No. 9858218, Case No. IPR2020-01044, PAPER 1, 'Petition for Inter Partes Review of U.S. Patent No. 9,858,218,' filed June 9, 2020

Examiner Signature		Date Considered	

Electronic Acknowledgement Receipt

EFS ID:	40483519
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5066-US01
Receipt Date:	04-SEP-2020
Filing Date:	11-NOV-2019
Time Stamp:	21:31:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	129980_5066US_01_IDS4_Transmittal.pdf	175348 0cf36a582d048d33c4e0ea9e38a3a87aaf65af92	no	4

Warnings:

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Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	129980_5066US_01_IDS4_List.pdf	161802 bffd6fd7e3bf60c19828d4fb4a60bea158928941	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Non Patent Literature	Ex-1015-Proposal.pdf	359179 a89ab9ee867505c796eedf4b2f08d5e22c32d2f0	no	9
Warnings:					
Information:					
4	Non Patent Literature	Ex-1003-Declaration.pdf	2042976 ed0ca145600a0b1ecf0db0bd301213ebdc7e2815	no	185
Warnings:					
Information:					
5	Non Patent Literature	Ex-1039-Inphi.pdf	396300 1875305a4e93c0d2e0e273e9790139661b7efa14	no	11
Warnings:					
Information:					
6	Non Patent Literature	Ex-1026-JESD82-20A.pdf	16311220 30e78c3729ef9b4ea29870d47b0c91daa06dae55	no	198
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7	Non Patent Literature	Ex-1029-JESD209-LPDDR.pdf	5579665 91e69c036a7cf5017a9515a9c4e0970d4ee29497	no	68
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8	Non Patent Literature	Ex1036-JEDEC-Proposal.pdf	1074616 7b7a37228d383b716c7dbfc76649a2399721a425	no	45
Warnings:					
Information:					

9	Non Patent Literature	Ex1042-Sequence.pdf	349673 e19d77f5b2998467cc643ccf12c1f7b550f98491	no	5
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Information:					
10	Non Patent Literature	Ex1044-TI-DDR3-buffer.pdf	1160170 612c583d43c4c554e7731f7273b1889b35f31e37	no	10
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11	Non Patent Literature	Ex1045-Micron.pdf	485253 24f2c8e41acb15829e0d9ad1c550abb85e4a03cf	no	25
Warnings:					
Information:					
12	Non Patent Literature	Ex1046-JEDEC-Meeting.pdf	224181 a96ae35ee85c1ea7c2230e4d2aa443d8be9de966	no	33
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13	Non Patent Literature	Ex1050-JEDEC-declaration.pdf	8629024 6869721e0ffebe85c1e8ca5847ead587eda37b8b	no	250
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Information:					
14	Non Patent Literature	Ex1054-Halbert-declaration.pdf	299650 0d305e8c320355f58520ccf01da2a346772e60a8	no	10
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Information:					
15	Non Patent Literature	Ex1056-JESD-79-3C-DDR3.pdf	11705296 cd9f69f7e4565a33fbba8e7bcadd24abac5d5472	no	211
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Information:					

16	Non Patent Literature	Ex1051-Letter-Ballot.pdf	89379 2f4d775d3a199ac38c963c0b6dee586d09882cd8	no	1
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17	Non Patent Literature	Ex1052-Letter-Ballot.pdf	87563 3d77693332a41c45de15b46e718861a736e81b14	no	1
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Information:					
18	Non Patent Literature	Ex1055-Declaration-Knaack.pdf	7535010 84c6717a027f22169eae33cbd9417ee46f010898	no	95
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Information:					
19	Non Patent Literature	Ex1025-JESD206_fbdimm_arch.pdf	2304038 658563047fdfe7172d1634f4f2b829e9ee9ced96	no	128
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Information:					
20	Non Patent Literature	2020-06-09-Petition.pdf	886956 21df882c3000a6fc0ee042796a624c24059b229f	no	99
Warnings:					
Information:					
21	Non Patent Literature	Ex1003-Alpert-Decl-2020-01044.pdf	1769717 bf47316148692398be5223584230811fb6b6d67a	no	156
Warnings:					
Information:					
22	Non Patent Literature	2020-06-08-Petition-2020-01044.pdf	1261788 90f25e84b80ec4b2229f3a92010f02f7e5bfcc0e	no	93
Warnings:					
Information:					
			Total Files Size (in bytes):	62888804	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed September 4, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee et al	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2133
Filed:	November 11, 2019	Examiner:	Chery, Mardochee
For:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES	Attorney Docket No.:	129980-5066US01

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☒ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

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2. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☒ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

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5. ☒ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☒ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☐ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial No. , filed on , of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f)

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supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5066US01).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: September 4, 2020

/ Jamie J. Zheng / 51,167
Jamie J. Zheng (Reg. No.)
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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/680,060	Filing Date 11/11/2019	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	11/09/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/BRENDA L TURNER/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronically filed November 9, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2133
Filed:	November 11, 2019	Examiner:	Chery, Mardochee
For:	*Memory Module Having An Open-Drain Output For Parity Error And For Training Sequences*	Attorney Docket No.:	129980-5066-US01

RESPONSE TO NON-FINAL OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Office Action dated September 3, 2020 for the above identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5066-US01).

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Electronic Patent Application Fee Transmittal

Application Number:	16680060
Filing Date:	11-Nov-2019
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	129980-5066-US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	170	170
		Total in USD ($)		**170**

Electronic Acknowledgement Receipt

EFS ID:	41077450
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5066-US01
Receipt Date:	09-NOV-2020
Filing Date:	11-NOV-2019
Time Stamp:	21:51:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$170
RAM confirmation Number	E2020A9L52016422
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer Filed	129980-5066-US01_TD.pdf	33477 aa679edaa3085567e38ed468538ee6ba159c9942	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	129980-5066-US01_TD-Fee.pdf	20781 215efb189d469fa53caab22daf9844dfa54e1a7a	no	2
Warnings:					
Information:					
3		129980-5066-US01_Amendment_NFOA.pdf	150426 108ccffea82e4fbeebf1e5bde368ac5e112b6663	yes	8

Multipart Description/PDF files in .zip description

Document Description	Start	End
Applicant Arguments/Remarks Made in an Amendment	7	8
Claims	2	6
Amendment/Req. Reconsideration-After Non-Final Reject	1	1

Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30402 1ea51db4e37c3cbd5b83ab82af5eb2a05b1cdd40	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	235086		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: DIST.E.FILE Document Description: Electronic Terminal Disclaimer - Filed	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	16680060
Filing Date	11-Nov-2019
First Named Inventor	Hyun Lee
Attorney Docket Number	129980-5066-US01
Title of Invention	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
Netlist, Inc.	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

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as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

- (●) Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.
- ( ) I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

- ( ) Small Entity
- ( ) Micro Entity
- (●) Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

- (●) An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

  Registration Number 51167

- ( ) A sole inventor
- ( ) A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application
- ( ) A joint inventor; all of whom are signing this request

Signature	/Jamie J. Zheng/
Name	Jamie J. Zheng

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	16680060
Filing Date:	11-Nov-2019
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	129980-5066-US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	170	170
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**170**

REMARKS

This amendment responds to the office action mailed September 3, 2020. In the office action, the Examiner:

- rejected claims 1-21 on the ground of nonstatutory double patenting as being unpatentable over claims 1-24 of U.S. Patent No. 10,474,595 and claims 1-22 of U.S. 9,858,218.

REMARKS CONCERNING CLAIMS

Claims 8 and 17 have been amended for clarity, and claim 21 has been amended to correspond with claims 8 and 17.

No new matter has been added.

With respect to all amendments, Applicant has not dedicated or abandoned any unclaimed subject matter. Moreover, Applicant has not acquiesced to any characterizations of the invention, nor any rejections or objections of the claims, made by the Examiner. Moreover, the Applicant hereby rescinds any prior disclaimer of claim scope, to the extent they exist, made during the prosecution of this application or made during the prosecution of any patent or other related patents/applications, and advises the Examiner that any such previous disclaimers and the cited references that they were made to avoid may need to be revisited.

After entry of this amendment, the pending claims are: claims 2-21.

REMARKS CONCERNING DOUBLE PATENTING REJECTIONS

I. **REJECTION OF CLAIMS 1-21 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING AS BEING UNPATENTABLE OVER CLAIMS 1-24 OF U.S. PATENT NO. 10,474,595 AND CLAIMS 1-22 OF U.S. 9,858,218**

Applicant submits herewith a terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d), which should overcome any actual or provisional rejection of claims 2-21 based on the nonstatutory obviousness-type double patenting ground over:

claims 1-24 of U.S. Patent No. 10,474,595; and/or

claims 1-22 of U.S. Patent No. 9,858,218.

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Applicant's filing of the terminal disclaimer is for the sole purpose of advancing prosecution. It should not be understood as implying that Applicant agrees with the rejection of claims 2-21 on the ground of nonstatutory double patenting made in the Office Action.

CONCLUDING REMARKS

By responding in the foregoing remarks only to particular positions asserted by the examiner, the Applicant does not necessarily acquiesce in other positions that have not been explicitly addressed. In addition, the Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: November 9, 2020

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-7278

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Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Previously Presented) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

a module controller on the printed circuit board and configurable to receive address and control signals associated with normal memory read or write operations via the first edge connections; and

dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and

wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

wherein the module controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation; and

wherein the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and not associated with any normal memory read or write operations.

3. (Previously Presented) The memory module of claim 2, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

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4. (Previously Presented) The memory module of claim 3, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state.

5. (Previously Presented) The memory module of claim 3, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.

6. (Previously Presented) The memory module of claim 5, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.

7. (Previously Presented) The memory module of claim 2, wherein the module controller comprises an integrated circuit that includes the transistor.

8. (Currently Amended) The memory module of claim 2, wherein ~~the memory module is configurable to perform~~ the operations associated with the one or more training sequences ~~without~~ are performed when the memory module is not communicating data signals associated with any normal memory read or write operations between the dynamic random access memory elements and ~~with~~ the memory controller via the second edge connections.

9. (Previously Presented) The memory module of claim 2, wherein the second edge connections are not active during the operations associated with the one or more training sequences.

10. (Previously Presented) The memory module of claim 2, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configurable to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.

11. (Previously Presented) A method of operation in a host system having a memory controller, comprising:

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at a memory module coupled to the memory controller, the memory module including a printed circuit board, a module controller on the printed circuit board, and dynamic random access memory elements on the printed circuit board, the printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections, the module controller including a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

receiving, at the module controller, address and control signals associated with one or more normal memory read or write operations from the memory controller via the first edge connections;

outputting or receiving data signals at the dynamic random access memory elements in accordance with the address and control signals, the data signals being communicated with the memory controller via the second edge connections;

applying a first signal to the gate of the transistor to indicate a parity error having occurred during one of the normal memory read or write operations;

performing training operations associated with one or more training sequences and not associated with any normal memory read or write operations; and

applying a second signal related to the one or more training sequences to the gate of the transistor while the memory module performs the training operations.

12. (Previously Presented) The method of claim 11, wherein the error edge connection is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

13. (Previously Presented) The method of claim 12, wherein the error edge connection is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state.

14. (Previously Presented) The method of claim 12, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.

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15. (Previously Presented) The method of claim 14, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.

16. (Previously Presented) The method of claim 11, wherein the module controller comprises an integrated circuit that includes the transistor.

17. (Currently Amended) The method of claim 11, wherein ~~the memory module performs~~ the training operations associated with the one or more training sequences ~~without~~ are performed when the memory module is not communicating data signals associated with any normal memory read or write operations between the dynamic random access memory elements and ~~with~~ the memory controller via the second edge connections.

18. (Previously Presented) The method of claim 11, wherein the second edge connections are not active during the training operations associated with the one or more training sequences.

19. (Previously Presented) The method of claim 11, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein applying the first signal to the gate of the transistor includes coupling the first input to the output, and applying the second signal to the gate of the transistor includes coupling the second input to the output.

20. (Previously Presented) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

a module controller on the printed circuit board and configurable to receive from the memory controller via the first edge connections address and control signals associated with normal memory read or write operations; and

dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and

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wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

wherein the module controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation;

wherein the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and not associated with any normal memory read or write operations;

wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground;

wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to a low impedance state, and drives the gate of the transistor low so as to drive the error edge connection to a high impedance state;

wherein the module controller comprises an integrated circuit that includes the transistor; and

wherein the integrated circuit further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configurable to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.

21. (Currently Amended) The memory module of claim 20, wherein the operations associated with the one or more training sequences are performed when the memory module is not communicating data signals associated with any normal memory read or write operations between the dynamic random access memory elements and the memory controller via the second edge connections ~~the second signal drives the error edge connection from the high impedance state to the low impedance state and from the low impedance state to the high impedance state~~.

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Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
* 16/680,060 *	16/680,060	Lee, Hyun	
	Examiner	**Art Unit**	
	CHERY, MARDOCHEE	2133	

Document Code - DISQ	**Internal Document - DO NOT MAIL**

TERMINAL DISCLAIMER	☑ APPROVED	☐ DISAPPROVED
Date Filed: **09 November 2020**	**This patent is subject to a Terminal Disclaimer**	

Approved/Disapproved by:

/PAMELA A YOUNG/

Technology Center: OPLC

Telephone: (571)272-3622

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed November 26, 2020	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
Sheet	1	of	3	Attorney Docket Number	129980-5066US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Patent Owner's Preliminary Response, filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Petitioners' Reply To Patent Owner's Preliminary Response, filed October 8, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Patent Owner's Sur-Reply to Petitioner's Reply to Patent Owner's Preliminary Response, filed October 15, 2020
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, Patent Owner's Preliminary Response, filed September 18, 2020
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, Petitioners' Reply To Patent's Owner Preliminary Response, filed October 8, 2020
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, Patent Owner's Sur-Reply to Petitioner's Reply to Patent Owner's Preliminary Response, filed October 15, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 1069, 'Netlist, Inc. Complaint for Patent Infringement, Netlist, Inc. v. SK hynix Inc. et al, 6:20-cv-00194 (March 17, 2020),' filed October 8, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 1071, 'SK hynix Inc. et al v. Netlist, Inc., IPR2018-00303, Paper No. 42, PTAB March 21, 2018 Final Written Decision,' filed October 8, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2001, 'Scheduling Order, Netlist, Inc. v. SK hyinx Inc. and SK hynix America Inc., Civil No. 6:20-cv-00194-ADA (W.D. Tex, Jul. 8, 2020), ECF No. 046,' filed September 18, 2020

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed November 26, 2020	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
Sheet	2	of	3	Attorney Docket Number	129980-5066US01

		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2005, 'Claim Construction Order, STC.UNM v. Apple Inc., Civil No. 1:20-cv-00351-ADA (W.D. Tex. Jun8, 2020),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2006, 'Claim Construction Order, Uniloc 2017 LLC v. Apple Inc., Civil No. 6:19-cv-00532-ADA (W.D. Tex. Jun 8, 2020),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2007, 'Claim Construction Order, MV3 Partners LLC v. Roku Inc., Civil No. 6:18-cv-00308-ADA (W.D.Tex. Oct.19,2019),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2009, 'Exhibit A1 of SK hynix's Invalidity Contentions, dated Aug. 7, 2020,' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2010, 'Exhibit A21 of SK hynix's Invalidity Contentions, dated Aug. 7, 2020,' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2011, 'Exhibit A19 of SK hynix's Invalidity Contentions, dated Aug. 7, 2020,' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2012, 'Exhibit A36 of SK hynix's Invalidity Contentions, dated Aug. 7, 2020,' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2013, 'SK hynix's Invalidity Contentions, dated Aug. 7, 2020,' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2014, 'Petition Fo r IPR of U.S. Patent No. 8,489,837, Sk Hynix, et al v. Netlist Inc., IPR2017-00548, Paper No. 1 (PTAB Dec. 30, 2016),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2015, 'Petition For IPR of U.S. Patent No. 9,535,623, Sk Hynix, et al v. Netlist Inc., IPR2018-00303, Paper No. 1 (PTAB Dec. 14, 2017),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2016, 'Final Written Decision, Sk Hynix, et al v. Netlist Inc., IPR2018-00303, Paper No. 42 (PTAB Mar. 21, 2019),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2017, 'Decl. of Dr. Alpert Regarding U.S. Patent No. 9,535,623, Sk Hynix, et al v. Netlist Inc., IPR2018-00303, Ex. 1003 (PTAB Dec. 13, 2017),' filed September 18, 2020

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				**Electronically filed November 26, 2020**	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
Sheet	3	of	3	Attorney Docket Number	129980-5066US01

Examiner Signature		Date Considered	

Electronic Acknowledgement Receipt

EFS ID:	41234609
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5066-US01
Receipt Date:	26-NOV-2020
Filing Date:	11-NOV-2019
Time Stamp:	23:23:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	129980-5066US01_IDSTransmittal_11-26-2020.pdf	127979 9014f607ca518cf4cd9fae1807ba1ea9d1c3cbec	no	4

Warnings:

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Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	129980-5066US01_Form1449_11-26-2020.pdf	219610 537e4948419c2a50418ca4a80e80dbfdf8f26eb1	no	3
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Information:					
This is not an USPTO supplied IDS fillable form					
3	Non Patent Literature	PAPER6_IPR2020-01042.pdf	882071 2e545223b65ccd70b9c1559c7ec787307236d8a7	no	46
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4	Non Patent Literature	PAPER8_IPR2020-01042.pdf	282858 4e5ea76ee57282238bdafe437601897589f9d939	no	20
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5	Non Patent Literature	PAPER9_IPR2020-01042.pdf	447666 9a8eb4b452235ec1cd30e006fd557884daca956e	no	12
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6	Non Patent Literature	PAPER6_IPR2020-01044.pdf	820805 73df39d361439b98fbb653aaad7bb3906921af63	no	35
Warnings:					
Information:					
7	Non Patent Literature	PAPER8_IPR2020-01044.pdf	279436 d0da3ffd6fe117164f03575c6a4bae6161871f84	no	20
Warnings:					
Information:					
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Information:					

9	Non Patent Literature	EX1069.pdf	467532 449cfc58018f906ee0141296f6bb844b46974a0f	no	16
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Information:					
11	Non Patent Literature	EX2001.pdf	176661 6a29bf0283c645f67de102d11bb6578243fff2b2	no	4
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Information:					
12	Non Patent Literature	EX2005.pdf	479062 c439f6d96dc0e259d84077e9d2d658d2f1eb9165	no	1
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Information:					
13	Non Patent Literature	EX2006.pdf	1157527 4bb9ce50ea32158bb9423f2a9e8a4573c96f077e	no	1
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Information:					
14	Non Patent Literature	EX2007.pdf	641244 4fc4a01cc966f0aaa689dc70d72fb183522da6ad	no	15
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Information:					
15	Non Patent Literature	EX2009.pdf	3685382 2c8fe7591031b90bdff7e1dbe37b598040adc369	no	143
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Information:					

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Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
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20	Non Patent Literature	EX2014.pdf	647342 da35c2531254d88bdb034ac906841b40fc0085d4	no	55
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21	Non Patent Literature	EX2015.pdf	1098827 68fe865b0e44f61f8fbcb913269c189396f5b866	no	79
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Information:					
23	Non Patent Literature	EX2017.pdf	2005153 ec6e3dea06dc3dcddeec2993a819f09a74ca9cc8	no	168
Warnings:					
Information:					
			Total Files Size (in bytes):	19698558	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed November 26, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee, et al.	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2133
Filed:	November 11, 2019	Examiner:	Chery, Mardochee
For:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES	Attorney Docket No.:	129980-5066US01

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☒ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

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2. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☒ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

5. ☒ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☒ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☐ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial No. , filed on , of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f)

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supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5066US01).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: November 26, 2020

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed February 3, 2021	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	LEE, Hyun
				Art Unit	2133
				Examiner Name	MARDOCHEE, Chery
Sheet	1	of	2	Attorney Docket Number	129980-5066US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Patent Owner's Preliminary Response, filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Petitioners' Reply To Patent Owner's Preliminary Response, filed October 8, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Patent Owner's Sur-Reply to Petitioner's Reply to Patent Owner's Preliminary Response, filed October 15, 2020
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, Patent Owner's Preliminary Response, filed September 18, 2020
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, Petitioners' Reply To Patent's Owner Preliminary Response, filed October 8, 2020
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, Patent Owner's Sur-Reply to Petitioner's Reply to Patent Owner's Preliminary Response, filed October 15, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 1069, 'Netlist, Inc. Complaint for Patent Infringement, Netlist, Inc. v. SK hynix Inc. et al, 6:20-cv-00194 (March 17, 2020),' filed October 8, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 1071, 'SK hynix Inc. et al v. Netlist, Inc., IPR2018-00303, Paper No. 42, PTAB March 21, 2018 Final Written Decision,' filed October 8, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2001, 'Scheduling Order, Netlist, Inc. v. SK hyinx Inc. and SK hynix America Inc., Civil No. 6:20-cv-00194-ADA (W.D. Tex, Jul. 8, 2020), ECF No. 046,' filed September 18, 2020

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed February 3, 2021	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	LEE, Hyun
				Art Unit	2133
				Examiner Name	MARDOCHEE, Chery
Sheet	2	of	2	Attorney Docket Number	129980-5066US01

		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, EXHIBIT 2005, "Claim Construction Order: STC.UNM v. Apple Inc., Civil No. A-20-CV-00351-ADA (USDC W.D. Tex. 08JUN2020)," filed September 18, 2020, 1 pg.
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, EXHIBIT 2006, "Claim Construction Order: Uniloc 2017 LLC v. Apple Inc., Civil No. W-19-CV-00532-ADA (USDC W.D. Tex. 08JUN2020)," filed September 18, 2020, 1 pg.
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, EXHIBIT 2007, "Claim Construction Order: MV3 Partners LLC v. Roku, Inc., Civil No. 6:18-CV-00308-ADA (USDC W.D.Tex. 02OCT2019)," filed September 18, 2020, 15 pgs.
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, EXHIBIT 2009, "Exhibit A1 of SK hynix's Invalidity Contentions, US Patent No. 9,858,218 v. Hazelzet," filed September 18, 2020, 143 pgs.
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, EXHIBIT 2010, "Exhibit A21 of SK hynix's Invalidity Contentions, US Patent No. 9,858,218 v. JEDEC Initialization Ballot," filed September 18, 2020, 36 pgs.
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, EXHIBIT 2011, "Exhibit A19 of SK hynix's Invalidity Contentions, US Patent No. 9,858,218 v. Buchmann," filed September 18, 2020, 57 pgs.
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, EXHIBIT 2012, "Exhibit A36 of SK hynix's Invalidity Contentions, US Patent No. 9,858,218 v. Kim," filed September 18, 2020, 68 pgs.
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2014, 'Petition For IPR of U.S. Patent No. 8,489,837, Sk Hynix, et al v. Netlist Inc., IPR2017-00548, Paper No. 1 (PTAB Dec. 30, 2016),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2015, 'Petition For IPR of U.S. Patent No. 9,535,623, Sk Hynix, et al v. Netlist Inc., IPR2018-00303, Paper No. 1 (PTAB Dec. 14, 2017),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2016, 'Final Written Decision, Sk Hynix, et al v. Netlist Inc., IPR2018-00303, Paper No. 42 (PTAB Mar. 21, 2019),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2017, 'Decl. of Dr. Alpert Regarding U.S. Patent No. 9,535,623, Sk Hynix, et al v. Netlist Inc., IPR2018-00303, Ex. 1003 (PTAB Dec. 13, 2017),' filed September 18, 2020

Examiner Signature		Date Considered	

Electronic Acknowledgement Receipt

EFS ID:	41831955
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5066-US01
Receipt Date:	03-FEB-2021
Filing Date:	11-NOV-2019
Time Stamp:	23:46:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Letter specifying the conditions for filing under 37CFR1.97	129980-5066US01_Supplemental-IDSTransmittal_03FEB2021.pdf	103691 b09656f1034f036daf9a01affe74ea1a069632aa	no	1

Warnings:

Samsung Electronics Co., Ltd.
Ex. 1002, p. 175

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	129980-5066US01_Supplemental-Form1449_03FEB2021.pdf	212109 e423a238f508aec172b6cba0e9f3b04625b4170c	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
			Total Files Size (in bytes):	315800	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed February 3, 2021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee, et al.	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2133
Filed:	November 11, 2019	Examiner:	Chery Mardochee
For:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES	Attorney Docket No.:	129980-5066-US01

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on November 26, 2020. A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on November 26, 2020.

Enclosures accompanying this Information Disclosure Statement are a list of all patents, publications, applications, or other information submitted for consideration by the office. **Copies of publications listed have been previously submitted on November 26, 2020, and are therefore not being submitted herewith.**

The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5066-US01).

No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: February 3, 2021

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)
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1400 Page Mill Road
Palo Alto, CA 94304
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Ex. 1002, p. 177

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed February 3, 2021	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	LEE, Hyun
				Art Unit	2133
				Examiner Name	MARDOCHEE, Chery
Sheet	1	of	2	Attorney Docket Number	129980-5066US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Exhibit 1058, "Order Governing Proceedings -- Patent Case, Netlist v. SK hynix et al., Case No. WA:20-CV-00194-ADA, USDC, Western District of Texas, Waco Division (May 27, 2020)," filed October 8, 2020, 9 pgs.
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Exhibit 2004, "Order Denying Motion to Stay Pending Inter Partes Review of US Patent Numbers 8,799,468 and 9,465,925," filed September 18, 2020, 7 pgs.
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Exhibit 2007, "Claim Construction Order: MV3 Partners v. Roku," filed September 18, 2020, 15 pgs.
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Exhibit 2009, "Exhibit B1, SK hynix's Preliminary Invalidity Contentions: US Patent No. 10,474,595 v. Hazelzet," filed September 18, 2020, 159 pgs.
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Exhibit 2010, "Exhibit B21, SK hynix's Preliminary Invalidity Contentions: US Patent No. 10,474,595 v. JEDEC Initialization Ballot," filed September 18, 2020, 54 pgs.
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Exhibit 2011, "Exhibit B19, SK hynix's Preliminary Invalidity Contentions: US Patent No. 10,474,595 v. Buchmann," filed September 18, 2020, 109 pgs.
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Exhibit 2012, "Exhibit B36, SK hynix's Preliminary Invalidity Contentions: US Patent No. 10,474,595 v. Kim," filed September 18, 2020, 92 pgs.
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Paper 6, "IPR2020-01042, US Patent No. 10,474,595: Patent Owner's Preliminary Response," filed September 18, 2020, 46 pgs.

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed February 3, 2021	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	LEE, Hyun
				Art Unit	2133
				Examiner Name	MARDOCHEE, Chery
Sheet	2	of	2	Attorney Docket Number	129980-5066US01

		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Paper 10, "IPR2020-01042, US Patent No. 10,474,595: Patent Owner's Updated Exhibit List," filed October 15, 2020, 4 pgs.
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Paper 11, "IPR2020-01042, US Patent No. 10,474,595: Petitioners' Updated Exhibit List," filed November 6, 2020, 9 pgs.
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Paper 14, "IPR2020-01042, US Patent No. 10,474,595: Decision Granting Institution of Inter Partes Review, SK hynix et al. v. Netlist," filed December 17, 2020, 47 pgs.
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, Paper 8, "IPR2020-01044, US Patent No. 9,858,218: Petitioners' Reply To Patent Owner's Preliminary Response," filed October 8, 2020, 20 pgs.
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, Paper 13, "IPR2020-01044, US Patent No. 9,858,218 B1: Decision Granting Institution of Inter Partes Review, SK hynix et al. v. Netlist," filed December 17, 2020, 55 pgs.

Examiner Signature		Date Considered	

Electronic Patent Application Fee Transmittal

Application Number:	16680060
Filing Date:	11-Nov-2019
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	129980-5066-US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
		Total in USD ($)		**260**

Electronic Acknowledgement Receipt

EFS ID:	41832034
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5066-US01
Receipt Date:	04-FEB-2021
Filing Date:	11-NOV-2019
Time Stamp:	01:19:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$260
RAM confirmation Number	E202124220192612
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	129980-5066US01_IDSTransmittal_03FEB2021.pdf	128044 9da1e3137ae6e3275d0166c220df7039b38021cd	no	4
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6	Non Patent Literature	IPR2020-01042_EXHIBIT2009.pdf	3855570 f7602e1f175ab7d0d9548b3c709711b67d1bc602	no	159
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Warnings:					
Information:					
11	Non Patent Literature	IPR2020-01042_PAPER10.pdf	336615 774d03ece9ee65ec34f9d6efc27e6956290e4c53	no	4
Warnings:					
Information:					
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Information:					

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15	Non Patent Literature	IPR2020-01044_PAPER13.pdf	480313 d245960e31251ad53678dd1b2f82d6d21edbf854	no	55
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Information:					
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Warnings:					
Information:					
			Total Files Size (in bytes):	14553218	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed February 3, 2021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee, et al.	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2133
Filed:	November 11, 2019	Examiner:	Chery Mardochee
For:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES	Attorney Docket No.:	129980-5066-US01

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☒ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

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Ex. 1002, p. 186

2. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☒ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5066-US01).

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4d. ☐ The $65 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☐ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial No. , filed on , of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f)

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supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5066-US01).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: February 3, 2021

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)
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UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/680,060	11/11/2019	Hyun Lee	129980-5066-US01	8269

79141 7590 02/24/2021

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2133	

NOTIFICATION DATE	DELIVERY MODE
02/24/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jzheng@uschlaw.com
padocketingdepartment@morganlewis.com

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Office Action Summary	Application No. 16/680,060	Applicant(s) Lee, Hyun	
	Examiner MARDOCHEE CHERY	Art Unit 2133	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 11/9/20.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 2-21 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 2-21 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 9/2/20; 2/4/21; 2/3/21; 11/26/21.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

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DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 103

2. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 2-24 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Hazelzet (20080098277 cited in IDS of 09/02/2020) and JEDEC (cited in IDS of 09/02/2020).

Regarding claim 1, Hazelzet discloses a memory module operable with a memory controller of a host system [FIG. 2], comprising: a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections [FIG. 2:

a DIMM with ECC/Parity buffer chip coupled to a memory interface chip which in turn coupled to a memory controller or processor; memory interface chip sends and receives data from the DIMM via data line and sends address and commands via a line; the memory interface chip then sends and receives data via the line to the DRAMs and sends address and command information to the register chip via the line; the memory interface chip further sends check bits for error correction purposes to the ECC/Parity register chip via another line]; a module controller on the printed circuit board and configurable to receive address and control signals associated with normal memory read or write operations via the first edge connections [FIG. 2: *memory controller receiving address and control signals through DATA line, CMD/CHK BITS line*]; and dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals [FIG.2: *SDRAMs communicate data signals with memory controller via DATA, CMD/CHK BITS signals*]; and wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate [FIGs. 4A, 4B; ¶0062, 0067, 0072, 0109: *ECC mode signal source coupled to selection input of multiplexers and to error logic circuit, the multiplexers having their selection inputs coupled to a source; two open-drain outputs available for reporting an error are driven low*]; wherein the module controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation [¶0072, 0076, 0109: *UE indicates that a parity error occurred*].

Although Hazelzet discloses a test mode in which the controller apply a signal to training sequences [¶0082], Hazelzet does not explicitly disclose applying a signal to training sequences when performing operations associated with the one or more training sequences and not associated with any normal memory read or write operations.

JEDEC, however, discloses wherein the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and not associated

with any normal memory read or write operations [See JEDEC's Figures 3-4, 3-7, 3-6, 3-9, 3-11, 3-13, 3-14; Pages 14-54: *during the training sequences, JEDEC's memory controller communicates no data with the module and performs no operations to read or write to the memory devices, and that the training is carried out by memory buffer (module controller) itself; additionally Hazelzet's memory module can be placed into a training mode to implement JEDEC's training sequences*].

It would have been obvious to a POSITA to combine Hazelzet and JEDEC in order to perform multiple functions during multiple operations/modes including initialization/training because such was well known to improve memory module reliability (Pages 14-54).

Regarding claim 3, Hazelzet discloses the memory module of claim 2, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state [¶0018-0020].

Regarding claim 4, Hazelzet discloses the memory module of claim 3, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state [¶0018-0020].

Regarding claim 5, Hazelzet discloses the memory module of claim 2, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to ground, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state [¶0018-0020, 0022, 0067].

Regarding claim 6, Hazelzet discloses the memory module of claim 5, wherein the first signal

drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground [¶0098-0099].

Regarding claim 7, Hazelzet discloses the memory module of claim 2, wherein the module controller comprises an integrated circuit that includes the transistor [¶0072].

Regarding claim 8, JEDEC discloses the memory module of claim 2, wherein the memory module is configurable to perform the operations associated with the one or more training sequences without communicating data signals with the memory controller via the second edge connections [Page 66: all DIMMs can be accessed from a single command one bit per DIMM].

Regarding claim 9, Hazelzet discloses the memory module of claim 2, wherein the second edge connections are not active during the operations associated with the one or more training sequences [¶0066].

Regarding claim 10, Hazelzet discloses the memory module of claim 2, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configurable to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences [FIGs. 4A, 4B].

Regarding claim 11, the rationale in the rejection of claim 2 is herein incorporated.

Regarding claim 12, the rationale in the rejection of claim 3 is herein incorporated.

Regarding claim 13, the rationale in the rejection of claim 4 is herein incorporated.

Regarding claim 14, the rationale in the rejection of claim 5 is herein incorporated.

Regarding claim 15, the rationale in the rejection of claim 6 is herein incorporated.

Regarding claim 16, the rationale in the rejection of claim 7 is herein incorporated.

Regarding claim 17, the rationale in the rejection of claim 8 is herein incorporated.

Regarding claim 18, the rationale in the rejection of claim 9 is herein incorporated.

Regarding claim 19, the rationale in the rejection of claim 10 is herein incorporated.

Regarding claim 20, the rationale in the rejection of claims 2-10 is herein incorporated.

Regarding claim 21, the rationale in the rejection of claim 4 is herein incorporated.

Conclusion

4. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 02/04/2021 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609.04(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARDOCHEE CHERY whose telephone number is (571)272-4246. The examiner can normally be reached from 900-500.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Jared Rutz** can be reached on **(571)272-5535**. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Respectfully Submitted,
USPTO

Dated: February 20, 2021

By: /MARDOCHEE CHERY/
Primary Examiner
Art Unit 2133
Email:Mardochee.Chery@uspto.gov
Telephone: 571-272-4246
Facsimile: 571-273-4246

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/680,060	Lee, Hyun
	Examiner	Art Unit
	MARDOCHEE CHERY	2133

CPC - Searched*		
Symbol	Date	Examiner
(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2029/4402 or G11C2207/2254)	08/30/2020	MC

CPC Combination Sets - Searched*		
Symbol	Date	Examiner
(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2029/4402 or G11C2207/2254)	08/30/2020	MC

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	154	08/30/2020	MC

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST; Inventor; Assignee; CPC	08/30/2020	MC

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	08/30/2020

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/680,060	Lee, Hyun
	Examiner	Art Unit
	MARDOCHEE CHERY	2133

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/30/2020	02/20/2021							
	1	-	-							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							
	10	✓	✓							
	11	✓	✓							
	12	✓	✓							
	13	✓	✓							
	14	✓	✓							
	15	✓	✓							
	16	✓	✓							
	17	✓	✓							
	18	✓	✓							
	19	✓	✓							
	20	✓	✓							
	21	✓	✓							

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed November 26, 2020	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
Sheet	1	of	3	Attorney Docket Number	129980-5066US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Patent Owner's Preliminary Response, filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Petitioners' Reply To Patent Owner's Preliminary Response, filed October 8, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Patent Owner's Sur-Reply to Petitioner's Reply to Patent Owner's Preliminary Response, filed October 15, 2020
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, Patent Owner's Preliminary Response, filed September 18, 2020
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, Petitioners' Reply To Patent's Owner Preliminary Response, filed October 8, 2020
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, Patent Owner's Sur-Reply to Petitioner's Reply to Patent Owner's Preliminary Response, filed October 15, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 1069, 'Netlist, Inc. Complaint for Patent Infringement, Netlist, Inc. v. SK hynix Inc. et al, 6:20-cv-00194 (March 17, 2020),' filed October 8, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 1071, 'SK hynix Inc. et al v. Netlist, Inc., IPR2018-00303, Paper No. 42, PTAB March 21, 2018 Final Written Decision,' filed October 8, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2001, 'Scheduling Order, Netlist, Inc. v. SK hyinx Inc. and SK hynix America Inc., Civil No. 6:20-cv-00194-ADA (W.D. Tex, Jul. 8, 2020), ECF No. 046,' filed September 18, 2020

Examiner Signature	/MARDOCHEE CHERY/	Date Considered	02/20/2021

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /MC/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed November 26, 2020	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
Sheet	2	of	3	Attorney Docket Number	129980-5066US01

		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2005, 'Claim Construction Order, STC.UNM v. Apple Inc., Civil No. 1:20-cv-00351-ADA (W.D. Tex. Jun8, 2020),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2006, 'Claim Construction Order, Uniloc 2017 LLC v. Apple Inc., Civil No. 6:19-cv-00532-ADA (W.D. Tex. Jun 8, 2020),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2007, 'Claim Construction Order, MV3 Partners LLC v. Roku Inc., Civil No. 6:18-cv-00308-ADA (W.D.Tex. Oct.19,2019),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2009, 'Exhibit A1 of SK hynix's Invalidity Contentions, dated Aug. 7, 2020,' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2010, 'Exhibit A21 of SK hynix's Invalidity Contentions, dated Aug. 7, 2020,' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2011, 'Exhibit A19 of SK hynix's Invalidity Contentions, dated Aug. 7, 2020,' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2012, 'Exhibit A36 of SK hynix's Invalidity Contentions, dated Aug. 7, 2020,' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2013, 'SK hynix's Invalidity Contentions, dated Aug. 7, 2020,' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2014, 'Petition Fo r IPR of U.S. Patent No. 8,489,837, Sk Hynix, et al v. Netlist Inc., IPR2017-00548, Paper No. 1 (PTAB Dec. 30, 2016),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2015, 'Petition For IPR of U.S. Patent No. 9,535,623, Sk Hynix, et al v. Netlist Inc., IPR2018-00303, Paper No. 1 (PTAB Dec. 14, 2017),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2016, 'Final Written Decision, Sk Hynix, et al v. Netlist Inc., IPR2018-00303, Paper No. 42 (PTAB Mar. 21, 2019),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2017, 'Decl. of Dr. Alpert Regarding U.S. Patent No. 9,535,623, Sk Hynix, et al v. Netlist Inc., IPR2018-00303, Ex. 1003 (PTAB Dec. 13, 2017),' filed September 18, 2020

Examiner Signature	/MARDOCHEE CHERY/	Date Considered	02/20/2021

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /MC/

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				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
Sheet	3	of	3	Attorney Docket Number	129980-5066US01

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				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	LEE, Hyun
				Art Unit	2133
				Examiner Name	MARDOCHEE, Chery
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				First Named Inventor	LEE, Hyun
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				Examiner Name	MARDOCHEE, Chery
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				First Named Inventor	LEE, Hyun
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				Examiner Name	MARDOCHEE, Chery
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				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2139
				Examiner Name	To be assigned
Sheet	1	of	1	Attorney Docket Number	129980-5066US01

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				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
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Examiner Initials	Cite No.	Foreign Patent Document Country Code[3] – Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter partes review Case No. IPR2017-00548, Petition For Inter Partes Review Of U.S. Patent No. 8,489,837, filed December 30, 2016.
		Inter partes review Case No. IPR2017-00548, Power of Attorney of Petitioners, filed December 30, 2016.
		Inter partes review Case No. IPR2017-00548, Exhibit 1002 "File History", filed December 30, 2016.
		Inter partes review Case No. IPR2017-00548, Exhibit 1003 "Declaration of Donald Alpert", filed December 30, 2016.
		Inter partes review Case No. IPR2017-00548, Exhibit 1004 "Camelback Computer Architecture", filed December 30, 2016.

Examiner Signature	/MARDOCHEE CHERY/	Date Considered	02/20/2021

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.C./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 1, 2020	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2139
				Examiner Name	To be assigned
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Examiner Signature	/MARDOCHEE CHERY/	Date Considered	02/20/2021

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Examiner Signature	/MARDOCHEE CHERY/	Date Considered	02/20/2021

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 1, 2020	
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Examiner Signature	/MARDOCHEE CHERY/	Date Considered	02/20/2021

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				Art Unit	2139
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		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Petitioners Motion to Exclude, filed November 30, 2018
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		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Patent Owner Request For Oral Argument, filed November 30, 2018
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		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Petitioners' Reply in Support of its Motion to Exclude, filed December 21, 2018
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Examiner Signature	/MARDOCHEE CHERY/	Date Considered	02/20/2021

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.C./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 1, 2020	
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				Art Unit	2139
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		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1025, '337-TA-1023, Initial Determination (Excerpts),' filed December 14, 2017
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		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1003, 'Declaration of Donald Alpert,' filed December 4, 2017
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1003, 'Corrected Declaration of Donald Alpert,' filed December 19, 2017
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1030, 'Declaration of Brian Nester PHV,' filed October 18, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1032, 'Annotated Page 37 of Ex. 2005,' filed November 9, 2018

Examiner Signature	/MARDOCHEE CHERY/	Date Considered	02/20/2021

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				Art Unit	2139
				Examiner Name	To be assigned
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		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1034, 'ITC Expert Report of Robert Mr. Murphy Regarding 623 Patent (Public Version),' filed November 9, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1033, 'Annotated Page 18 of Ex. 2005,' filed November 9, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1035, 'Mr. Murphy 623 IPR Deposition Transcript (October 25, 2018),' filed November 9, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1036, 'Mr. Murphy 623 ITC Deposition Transcript (October 19, 2018),' filed November 9, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1037, 'JEDEC Standard (JESD79-3),' filed November 9, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Final Written Decision, filed March 21, 2019

Examiner Signature	/MARDOCHEE CHERY/	Date Considered	02/20/2021

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.C./

Doc Code: A.NE.AFCP
Document Description: After Final Consideration Pilot Program Request

PTO/SB/434 (05-13)

CERTIFICATION AND REQUEST FOR CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0

Practitioner Docket No.:	Application No.:	Filing Date:
129980-5066-US01	16/680,060	November 11, 2019
First Named Inventor:	**Title:**	
Hyun Lee	Memory Module Having an Open-Drain Output for Parity Error and for Training Sequences	

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0 (AFCP 2.0) OF THE ACCOMPANYING RESPONSE UNDER 37 CFR 1.116.

1. The above-identified application is (i) an original utility, plant, or design nonprovisional application filed under 35 U.S.C. 111(a) [a continuing application (*e.g.*, a continuation or divisional application) is filed under 35 U.S.C. 111(a) and is eligible under (i)], or (ii) an international application that has entered the national stage in compliance with 35 U.S.C. 371(c).
2. The above-identified application contains an outstanding final rejection.
3. Submitted herewith is a response under 37 CFR 1.116 to the outstanding final rejection. The response includes an amendment to at least one independent claim, and the amendment does not broaden the scope of the independent claim in any aspect.
4. This certification and request for consideration under AFCP 2.0 is the only AFCP 2.0 certification and request filed in response to the outstanding final rejection.
5. Applicant is willing and available to participate in any interview requested by the examiner concerning the present response.
6. This certification and request is being filed electronically using the Office's electronic filing system (EFS-Web).
7. Any fees that would be necessary consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, extension of time fees, are being concurrently filed herewith. [There is no additional fee required to request consideration under AFCP 2.0.]
8. By filing this certification and request, applicant acknowledges the following:
    - Reissue applications and reexamination proceedings are not eligible to participate in AFCP 2.0.
    - The examiner will verify that the AFCP 2.0 submission is compliant, *i.e.*, that the requirements of the program have been met (see items 1 to 7 above). For compliant submissions:
        - The examiner will review the response under 37 CFR 1.116 to determine if additional search and/or consideration (i) is necessitated by the amendment and (ii) could be completed within the time allotted under AFCP 2.0. If additional search and/or consideration is required but cannot be completed within the allotted time, the examiner will process the submission consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, by mailing an advisory action.
        - If the examiner determines that the amendment does not necessitate additional search and/or consideration, or if the examiner determines that additional search and/or consideration is required and could be completed within the allotted time, then the examiner will consider whether the amendment places the application in condition for allowance (after completing the additional search and/or consideration, if required). If the examiner determines that the amendment does not place the application in condition for allowance, then the examiner will contact the applicant and request an interview.
            - The interview will be conducted by the examiner, and if the examiner does not have negotiation authority, a primary examiner and/or supervisory patent examiner will also participate.
            - If the applicant declines the interview, or if the interview cannot be scheduled within ten (10) calendar days from the date that the examiner first contacts the applicant, then the examiner will proceed consistent with current practice concerning responses after final rejection under 37 CFR 1.116.

Signature	Date
/Jamie J. Zheng/	April 24, 2021
Name (Print/Typed)	**Practitioner Registration No.**
Jamie J. Zheng	51167

***Note**: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.*

☐ * Total of _____ forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

REMARKS

This amendment responds to the final office action dated February 24, 2021. In the final office action, the Examiner:

- rejected claims 2-21 under 35 U.S.C. 103(a) as being unpatentable over Hazelzet (US 20080098277 cited in IDS of 09/02/2020, hereafter "Hazelzet") in view of JEDEC (cited in IDS of 09/02/2020).

REMARKS CONCERNING CLAIMS

Claims 2, 11, and 20 have been amended.

No new matter has been added. The amendments are for clarity and should not necessitate additional search or examination.

After entry of this amendment, the pending claims are: claims 2-21.

REMARKS CONCERNING REJECTIONS UNDER 35 U.S.C. 103(A)

It is unclear what the final office action refers to by "JEDEC (cited in IDS of 09/02/2000)." The file history of the present application shows that, among the references listed in the three IDS's filed on 09/02/2020, JEDEC Standard (JESD79-3) is the only document titled with "JEDEC," but JEDEC Standard (JESD79-3) does not seem to have the content that matches the statements made on page 4 of the final office action. Based on these statements, and upon checking the references titled with "JEDEC" in the IDS's filed in September 2020, Applicant believes that, by "JEDEC (cited in IDS of 09/02/2000)," the final office action is referring to JEDEC Standard, FBDIMM: Architecture and Protocol (January 2007) ("JESD206"), which is listed in the IDS filed on September 4, 2020. The remarks below are based on this understanding. A supplemental office action with the exact identification of the JEDEC reference cited by the final office action is hereby requested if the Applicant's understanding is incorrect. For consistency with the final office action, JESD206 is referred to hereafter as "JEDEC."

In KSR, the Supreme Court reaffirmed the doctrine that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR,* 550 U.S. at 416, 82 USPQ2d at 1395. The rationale to support a conclusion that the claim would have been obvious is that **all** of the claimed elements were

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known in the prior art, and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, if the combination yielded nothing more than predictable results to one of ordinary skill in the art. *Id.*; *Sakraida v. AG Pro, Inc.,* 425 U.S. 273, 282, 189 USPQ 449, 453 (1976); *Anderson's-Black Rock, Inc. v. Pavement Salvage Co.,* 396 U.S. 57, 62-63, 163 USPQ 673, 675 (1969); *Great Atl. & P. Tea Co. v. Supermarket Equip. Corp.,* 340 U.S. 147, 152, 87 USPQ 303, 306 (1950). "[I]t can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does." *KSR,* 550 U.S. at 418, 82 USPQ2d at 1396. If any of these findings cannot be made, then this rationale cannot be used to support a conclusion that the claim would have been obvious to one of ordinary skill in the art.

Accordingly, claims 2-21 are improperly rejected under 35 U.S.C. 103(a) as being unpatentable over Hazelzet in view of JEDEC because neither Hazelzet nor JEDEC teaches or suggests, among other things, "to apply (or applying) a first signal to the gate of the transistor (having an open drain coupled to the error edge connection) to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation," **and** "to apply (or applying) a second signal related to one or more training sequences to the gate of the transistor when the memory module performs training operations associated with the one or more training sequences." In other words, neither references teaches or suggests outputting a signal to indicate a parity error during normal memory operation and outputting a signal related to one or more training sequences during a training operation using the **same** open-drain output by applying different signals to the **same** gate of the **same** transistor.

Hazelzet uses **two** open drain outputs 120, 121 for reporting **two** different errors, a correctable error (e.g., error corrected by the ECC logic) and an uncorrectable error (e.g., uncorrectable ECC error or parity error), **respectively** (Hazelzet, [0072]), both during normal memory operations. Hazelzet never mentions outputting any signal related to training sequences, let alone teaching or suggesting using the **same** open-drain output for reporting parity errors to output any signal related to training sequences. Therefore, Hazelzet does not teach or suggest "to apply a first signal … to indicate a parity error" and "to apply a second signal related to one or more training sequences" to the **same** gate of the **same** transistor in **different** operations.

JEDEC does not make up for the deficiencies of Hazelzet. Although JEDEC discusses training sequences, it does not teach or suggest outputting any signal related to the training

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sequences through an open-drain output, let alone an open drain output of a transistor with a gate that also receives first signal "to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation." Instead, JEDEC uses polling to deal with the situation that the training is carried out by the memory buffer without participation from the host. With polling, the host continues to send TS2 patters until it receives at least 4 TS2 patterns on its northbound receivers (JEDEC, p. 32-34 and Table 3-16). As discussed in the specification of present application, polling is one of the techniques the claimed invention is improving upon (Specification, [0016]).

Furthermore, persons of ordinary skill in the art would not be motivated to combine JEDEC's training sequences with the ECC solution in Hazelzet, because Hazelzet's solution using ECC and JEDEC memory buffer training are distinct solutions to distinct problems. ECC is an effective way to reduce and eliminate soft and hard errors in memory systems in order to improve the reliability of data being communicated, while JEDEC's training seeks to pre-emptively optimize the performance of memory modules with memory buffers by resolving the timing issues associated with the memory buffers. Persons of ordinary skill in the art would not be motivated to add the training discussed in JEDEC to Hazelzet, or replace Hazelzet's ECC solution with JEDEC's trainings, to arrive at the claimed invention, because, first of all, Hazelzet does not use any memory buffers that would present the timing issues faced by JEDEC to begin with.

Moreover, there is no teaching or suggestion in either Hazelzet or JEDEC why it would be advantageous to use either of the outputs 120, 121 in Hazelzet to output a signal related to any training sequences. Thus, without the hindsight of the claimed invention, combining Hazelzet's ECC solution and JEDEC's training would not even arrive at the claimed invention.

Therefore, claims 2-21 are not combinations of know elements found in Hazelzet and JEDEC, and are thus patentable over Hazelzet in view of JEDEC.

CONCLUDING REMARKS

By responding in the foregoing remarks only to particular positions asserted by the examiner, the Applicant does not necessarily acquiesce in other positions that have not been explicitly addressed. In addition, the Applicant's arguments for the patentability of a claim

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should not be understood as implying that no other reasons for the patentability of that claim exist.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: April 24, 2021

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)
Customer No. 79141

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Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Currently Amended) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

a module controller on the printed circuit board and configurable to receive address and control signals associated with normal memory read or write operations via the first edge connections; and

dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and

wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

wherein the module controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation; and

wherein the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs training operations associated with the one or more training sequences, wherein the training operations are not ~~and not associated with any~~ normal memory read or write operations.

3. (Previously Presented) The memory module of claim 2, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

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4. (Previously Presented) The memory module of claim 3, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state.

5. (Previously Presented) The memory module of claim 3, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.

6. (Previously Presented) The memory module of claim 5, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.

7. (Previously Presented) The memory module of claim 2, wherein the module controller comprises an integrated circuit that includes the transistor.

8. (Previously Presented) The memory module of claim 2, wherein the operations associated with the one or more training sequences are performed when the memory module is not communicating data signals associated with any normal memory read or write operations between the dynamic random access memory elements and-the memory controller via the second edge connections.

9. (Previously Presented) The memory module of claim 2, wherein the second edge connections are not active during the operations associated with the one or more training sequences.

10. (Previously Presented) The memory module of claim 2, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configurable to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.

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11. (Currently Amended) A method of operation in a host system having a memory controller, comprising:

at a memory module coupled to the memory controller, the memory module including a printed circuit board, a module controller on the printed circuit board, and dynamic random access memory elements on the printed circuit board, the printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections, the module controller including a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

receiving, at the module controller, address and control signals associated with one or more normal memory read or write operations from the memory controller via the first edge connections;

outputting or receiving data signals at the dynamic random access memory elements in accordance with the address and control signals, the data signals being communicated with the memory controller via the second edge connections;

applying a first signal to the gate of the transistor to indicate a parity error having occurred during one of the normal memory read or write operations;

performing training operations associated with one or more training sequences, wherein the training operations are not ~~and not associated with any~~ normal memory read or write operations; and

applying a second signal related to the one or more training sequences to the gate of the transistor while the memory module performs the training operations.

12. (Previously Presented) The method of claim 11, wherein the error edge connection is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

13. (Previously Presented) The method of claim 12, wherein the error edge connection is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state.

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14. (Previously Presented) The method of claim 12, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.

15. (Previously Presented) The method of claim 14, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.

16. (Previously Presented) The method of claim 11, wherein the module controller comprises an integrated circuit that includes the transistor.

17. (Previously Presented) The method of claim 11, wherein the training operations associated with the one or more training sequences are performed when the memory module is not communicating data signals associated with any normal memory read or write operations between the dynamic random access memory elements and the memory controller via the second edge connections.

18. (Previously Presented) The method of claim 11, wherein the second edge connections are not active during the training operations associated with the one or more training sequences.

19. (Previously Presented) The method of claim 11, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein applying the first signal to the gate of the transistor includes coupling the first input to the output, and applying the second signal to the gate of the transistor includes coupling the second input to the output.

20. (Currently Amended) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge

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connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

a module controller on the printed circuit board and configurable to receive from the memory controller via the first edge connections address and control signals associated with normal memory read or write operations; and

dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and

wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

wherein the module controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation;

wherein the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs training operations associated with the one or more training sequences, wherein the training operations are not ~~and not associated with any~~ normal memory read or write operations;

wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground;

wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to a low impedance state, and drives the gate of the transistor low so as to drive the error edge connection to a high impedance state;

wherein the module controller comprises an integrated circuit that includes the transistor; and

wherein the integrated circuit further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configurable to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.

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21. (Previously Presented) The memory module of claim 20, wherein the operations associated with the one or more training sequences are performed when the memory module is not communicating data signals associated with any normal memory read or write operations between the dynamic random access memory elements and the memory controller via the second edge connections.

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Electronically filed April 24, 2021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2133
Filed:	November 11, 2019	Examiner:	Chery, Mardochee
For:	*Memory Module Having an Open-Drain Output for Parity Error and for Training Sequences*	Attorney Docket No.:	129980-5066-US01

CERTIFICATE OF EFS-WEB TRANSMISSION
I hereby certify that this correspondence is being transmitted to the United States Patent and Trademark Office (USPTO) via the USPTO's Electronic Filing System (EFS-Web) on:
APRIL 24, 2021 (DATE).
By: Jamie J. Zheng
Signature: /Jamie J. Zheng/
Registration Number: 51167

RESPONSE TO FINAL OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment and Remarks are in response to the Final Office Action dated February 24, 2021 for the above identified patent application, and is filed under the After Final Consideration Pilot (AFCP) 2.0.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. 129980-5066-US01).

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Electronic Acknowledgement Receipt

EFS ID:	42544161
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5066-US01
Receipt Date:	25-APR-2021
Filing Date:	11-NOV-2019
Time Stamp:	02:58:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	After Final Consideration Program Request	129980-5066US01_AFCP.pdf	226166 4a62270866cc211395e32db61e5d46a9520c403a	no	2

Warnings:

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Information:					
2		129980-5066-US01_Amendment_FOA.pdf	250271 6146c6f13e0706134cd281d253d6422e5bb73fc1	yes	11

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Applicant Arguments/Remarks Made in an Amendment	8	11
Claims	2	7
Response After Final Action	1	1

Warnings:	
Information:	
Total Files Size (in bytes):	476437

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/680,060	Filing Date 11/11/2019	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	04/25/2021	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/VIKKI GRAY/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed April 26, 2021	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	LEE, Hyun
				Art Unit	2133
				Examiner Name	MARDOCHEE, Chery
Sheet	1	of	1	Attorney Docket Number	129980-5066-US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

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Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2024, "Declaration of Matthew S. Galica," filed 08MAR2021, 4 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2025, "Declaration of Andrew H. DeVoogd," filed 08MAR2021, 4 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2026, "Remote Deposition Under Oral Examination of Dr. Donald Alpert, March 10, 2021," filed 11MAR2021, 493 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2027, "DDR3 SDRAM LRDIMM," filed 11MAR2021, 18 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2028, "Join JEDEC Membership Details," filed 11MAR2021, 2 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2029, "DRAM Circuit Design: Fundamental and High-Speed Topics," filed 11MAR2021, 4 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2030, "Semiconductor Memories: A Handbook and Design, Manufacture, and Application Second Edition," filed 11MAR2021, 6 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2031, "Deposition of Donald Alpert, Ph.D.," filed 11MAR2021, 218 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2032, "Declaration of Robert J. Murphy," filed 11MAR2021, 65 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Paper 21, "Patent Owner's Response Under 37 C.F.R. Section 42.120," 11MAR2021, 68 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Paper 22, "Patent Owner's Request for Rehearing of Institution Decision," 30MAR2021, 12 pgs.
		Inter Partes Review of US Patent No. 9,858,218, Case No. IPR2020-01044, Exhibit 2032, "Declaration of Robert J. Murphy," filed 12MAR2021, 63 pgs.

Examiner Signature		Date Considered	

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Electronic Patent Application Fee Transmittal

Application Number:	16680060
Filing Date:	11-Nov-2019
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng/Marya Li
Attorney Docket Number:	129980-5066-US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
		Total in USD ($)		**260**

Electronic Acknowledgement Receipt

EFS ID:	42559192
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/Marya Li
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5066-US01
Receipt Date:	26-APR-2021
Filing Date:	11-NOV-2019
Time Stamp:	22:03:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$260
RAM confirmation Number	E20214PM06253805
Deposit Account	
Authorized User	

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	129980-5066-US01_IDS_Transmittal_2021-04-26.pdf	96409 b5ad9eabf8e9094b43896e969e218d729c2ba45e	no	2
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	129980-5066-US01_IDS_Form1449_2021-04-26.pdf	184994 649d328515a3e757c09bc78c23f3482d7081bc46	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Non Patent Literature	IPR2020-01042_EX-2024.pdf	221706 18452b7e6bcefde0613051e4759edd91a26dec80	no	4
Warnings:					
Information:					
4	Non Patent Literature	IPR2020-01042_EX-2025.pdf	290011 080aeb606b5af7e425c9eea88a8f905130fb69b4	no	4
Warnings:					
Information:					
5	Non Patent Literature	IPR2020-01042_EX-2026.pdf	16284979 4d9bc7ad87cb153ab7f8b0095f4d02869c5d7743	no	493
Warnings:					
Information:					
6	Non Patent Literature	IPR2020-01042_EX-2027.pdf	718730 3f3af9e184ed1388233ae99092beaae6c0f5e0a4	no	18
Warnings:					

Information:					
7	Non Patent Literature	IPR2020-01042_EX-2028.pdf	293321 9ba92ca788d6bc4643fae3a72bb2794bf249ef91	no	2
Warnings:					
Information:					
8	Non Patent Literature	IPR2020-01042_EX-2029.pdf	1843046 d1034b7acd58e063f46e27a5c1d5858d05b0419c	no	4
Warnings:					
Information:					
9	Non Patent Literature	IPR2020-01042_EX-2030.pdf	1992377 6f6f2fff43d02302445a363feb1c5c6ef5e18e92	no	6
Warnings:					
Information:					
10	Non Patent Literature	IPR2020-01042_EX-2031.pdf	1177771 a91b64ca94bdc565f80f91f130c559e297930a00	no	218
Warnings:					
Information:					
11	Non Patent Literature	IPR2020-01042_EX-2032.pdf	2349135 4a5ead957b57f8ccedd05fa2a4d6bdfd9ed4167b	no	65
Warnings:					
Information:					
12	Non Patent Literature	IPR2020-01042_PAPER-21.pdf	1242332 7ebe56d43dc0b9cf17183c155146f30f217b4084	no	68
Warnings:					
Information:					
13	Non Patent Literature	IPR2020-01042_PAPER-22.pdf	411537 3356a5c36804b455aabda03e0072b4358a38c9b8	no	12
Warnings:					
Information:					

14	Non Patent Literature	IPR2020-01044_EX-2032.pdf	1992071 1091746fd1d49666d6465da3b5439998654 34d15	no	63
Warnings:					
Information:					
15	Fee Worksheet (SB06)	fee-info.pdf	30609 7ef3bbd98f24e8e05ed8209769f6aa7752fe 83db	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	29129028		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	LEE, Hyun	Confirmation No.:	8269
Serial No.:	16/680,060	Group Art Unit:	2133
Filed:	November 11, 2019	Examiner:	MARDOCHEE, Chery
For:	*MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES*	Attorney Docket No.:	129980-5066-US01

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

Enclosures accompanying this Information Disclosure Statement are: 1) A list of all patents, publications, applications, or other information submitted for consideration by the office; 2) A legible copy of each publication or that portion which caused it to be listed on the PTO-1449.

Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee. In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is paid herewith. However, the Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Deposit Account No. 60-3916 (order no. 129980-5066-US01).

No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of

Samsung Electronics Co., Ltd.
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a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: April 26, 2021

/Jamie J. Zheng/ 51,167

Jamie Zheng (Reg. No.)
3790 El Camino Real #1147
Palo Alto, CA 94306
(650) 521-4828

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/680,060	11/11/2019	Hyun Lee	129980-5066-US01	8269

79141 7590 05/05/2021

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2133	

NOTIFICATION DATE	DELIVERY MODE
05/05/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com

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Advisory Action Before the Filing of an Appeal Brief	**Application No.** 16/680,060	**Applicant(s)** Lee, Hyun	
	Examiner MARDOCHEE CHERY	**Art Unit** 2133	**AIA (FITF) Status** No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 25 April 2021 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☑ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:
   a) ☑ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection.The current period for reply expires ____ months from the mailing date of *the prior Advisory Action* or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.
   Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANTS FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37CFR 41.37(a).

AMENDMENTS

3. ☑ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   a) ☑ They raise new issues that would require further consideration and/or search (see NOTE below);
   b) ☑ They raise the issue of new matter (see NOTE below);
   c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____ (See 37CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicants reply has overcome the following rejection(s): _____
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s):(a) ☐ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____
9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☑ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
13. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
14. ☐ Other: _____.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:
    Claim(s) allowed:_____.
    Claim(s) objected to:_____.
    Claim(s) rejected:2-21.
    Claim(s) withdrawn from consideration:_____.

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	04/30/2021

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Continuation of REQUEST FOR RECONSIDERATION/OTHER 12. The request for reconsideration has been considered but does NOT place the application in condition for allowance because: The new amendment to the claims, "the training operations are not normal read and write," is not supported by the original disclosure, is considered new matter, and requires further search and consideration. The proposed amendment of 4/25/21 and ids of 4/26/21 cannot be considered within the time permitted under AFCP 2.0.

AFCP 2.0 Decision

Application No.	Applicant(s)	
16/680,060	Lee, Hyun	
Examiner	**Art Unit**	**AIA (FITF) Status**
MARDOCHEE CHERY	2133	No

This is in response to the After Final Consideration Pilot request filed 25 April 2021.

1. **Improper Request** – The AFCP 2.0 request is improper for the following reason(s) and the after final amendment submitted with the request will be treated under pre-pilot procedure.

   ☐ An AFCP 2.0 request form PTO/SB/434 (or equivalent document) was not submitted.

   ☐ A non-broadening amendment to at least one independent claim was not submitted.

   ☐ The request is not the first proper AFCP 2.0 request submitted in response to the most recent final rejection.

   ☐ Other: _____

2. **Proper Request**

   A. After final amendment submitted with the request will not be treated under AFCP 2.0.
   The after final amendment cannot be reviewed and a search conducted within the guidelines of the pilot program.

   ☑ The after final amendment will be treated under pre-pilot procedure.

   B. Updated search and/or completed additional consideration.
   The examiner performed an updated search and/or completed additional consideration of the after final amendment within the time authorized for the pilot program. The result(s) of the updated search and/or completed additional consideration are:

   ☐ 1. All of the rejections in the most recent final Office action are overcome and a Notice of Allowance is issued herewith.

   ☐ 2. The after final amendment would not overcome all of the rejections in the most recent final Office action . See attached interview summary for further details.

   ☐ 3. The after final amendment was reviewed, and it raises a new issue(s). See attached interview summary for further details.

   ☐ 4. The after final amendment raises new issues, but would overcome all of the rejections in the most recent final Office action. A decision on determining allowability could not be made within the guidelines of the pilot. See attached interview summary for further details, including any newly discovered prior art.

   ☐ 5. Other: _____

   Examiner Note: Please attach an interview summary when necessary as described above.

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DO NOT ENTER: /M.C/

04/30/2021

Electronically filed April 24, 2021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2133
Filed:	November 11, 2019	Examiner:	Chery, Mardochee
For:	*Memory Module Having an Open-Drain Output for Parity Error and for Training Sequences*	Attorney Docket No.:	129980-5066-US01

CERTIFICATE OF EFS-WEB TRANSMISSION
I hereby certify that this correspondence is being transmitted to the United States Patent and Trademark Office (USPTO) via the USPTO's Electronic Filing System (EFS-Web) on:
APRIL 24, 2021 (DATE).
By: Jamie J. Zheng
Signature: /Jamie J. Zheng/
Registration Number: 51167

RESPONSE TO FINAL OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment and Remarks are in response to the Final Office Action dated February 24, 2021 for the above identified patent application, and is filed under the After Final Consideration Pilot (AFCP) 2.0.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. 129980-5066-US01).

Samsung Electronics Co., Ltd.
Ex. 1002, p. 249

Electronically filed May 24, 2021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2133
Filed:	November 11, 2019	Examiner:	Chery, Mardochee
For:	*Memory Module Having an Open-Drain Output for Parity Error and for Training Sequences*	Attorney Docket No.:	129980-5066-US01

RESPONSE TO FINAL OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment and Remarks are in response to the Final Office Action dated February 24, 2021 and the Advisory Action dated May 5, 2021 for the above identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. 129980-5066-US01).

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Ex. 1002, p. 250

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/680,060	Filing Date 11/11/2019	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	05/24/2021	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/VIKKI GRAY/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronically filed May 24, 2021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2133
Filed:	November 11, 2019	Examiner:	Chery, Mardochee
For:	*Memory Module Having an Open-Drain Output for Parity Error and for Training Sequences*	Attorney Docket No.:	129980-5066-US01

RESPONSE TO FINAL OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment and Remarks are in response to the Final Office Action dated February 24, 2021 and the Advisory Action dated May 5, 2021 for the above identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. 129980-5066-US01).

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Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Previously Presented) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

a module controller on the printed circuit board and configurable to receive address and control signals associated with normal memory read or write operations via the first edge connections; and

dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and

wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

wherein the module controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation; and

wherein the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and not associated with any normal memory read or write operations.

3. (Previously Presented) The memory module of claim 2, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

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4. (Previously Presented) The memory module of claim 3, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state.

5. (Previously Presented) The memory module of claim 3, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.

6. (Previously Presented) The memory module of claim 5, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.

7. (Previously Presented) The memory module of claim 2, wherein the module controller comprises an integrated circuit that includes the transistor.

8. (Previously Presented) The memory module of claim 2, wherein the operations associated with the one or more training sequences are performed when the memory module is not communicating data signals associated with any normal memory read or write operations between the dynamic random access memory elements and the memory controller via the second edge connections.

9. (Previously Presented) The memory module of claim 2, wherein the second edge connections are not active during the operations associated with the one or more training sequences.

10. (Previously Presented) The memory module of claim 2, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configurable to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.

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Ex. 1002, p. 254

11. (Previously Presented) A method of operation in a host system having a memory controller, comprising:

at a memory module coupled to the memory controller, the memory module including a printed circuit board, a module controller on the printed circuit board, and dynamic random access memory elements on the printed circuit board, the printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections, the module controller including a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

receiving, at the module controller, address and control signals associated with one or more normal memory read or write operations from the memory controller via the first edge connections;

outputting or receiving data signals at the dynamic random access memory elements in accordance with the address and control signals, the data signals being communicated with the memory controller via the second edge connections;

applying a first signal to the gate of the transistor to indicate a parity error having occurred during one of the normal memory read or write operations;

performing training operations associated with one or more training sequences and not associated with any normal memory read or write operations; and

applying a second signal related to the one or more training sequences to the gate of the transistor while the memory module performs the training operations.

12. (Previously Presented) The method of claim 11, wherein the error edge connection is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

13. (Previously Presented) The method of claim 12, wherein the error edge connection is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state.

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14. (Previously Presented) The method of claim 12, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.

15. (Previously Presented) The method of claim 14, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.

16. (Previously Presented) The method of claim 11, wherein the module controller comprises an integrated circuit that includes the transistor.

17. (Previously Presented) The method of claim 11, wherein the training operations associated with the one or more training sequences are performed when the memory module is not communicating data signals associated with any normal memory read or write operations between the dynamic random access memory elements and the memory controller via the second edge connections.

18. (Previously Presented) The method of claim 11, wherein the second edge connections are not active during the training operations associated with the one or more training sequences.

19. (Previously Presented) The method of claim 11, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein applying the first signal to the gate of the transistor includes coupling the first input to the output, and applying the second signal to the gate of the transistor includes coupling the second input to the output.

20. (Previously Presented) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge

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connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

a module controller on the printed circuit board and configurable to receive from the memory controller via the first edge connections address and control signals associated with normal memory read or write operations; and

dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and

wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

wherein the module controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation;

wherein the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and not associated with any normal memory read or write operations;

wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground;

wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to a low impedance state, and drives the gate of the transistor low so as to drive the error edge connection to a high impedance state;

wherein the module controller comprises an integrated circuit that includes the transistor; and

wherein the integrated circuit further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configurable to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.

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21. (Previously Presented) The memory module of claim 20, wherein the operations associated with the one or more training sequences are performed when the memory module is not communicating data signals associated with any normal memory read or write operations between the dynamic random access memory elements and the memory controller via the second edge connections.

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REMARKS

This amendment responds to the final office action dated February 24, 2021 and the Advisory Action dated May 5, 202. In the final office action, the Examiner:

- rejected claims 2-21 under 35 U.S.C. 103(a) as being unpatentable over Hazelzet (US 20080098277 cited in IDS of 09/02/2020, hereafter "Hazelzet") in view of JEDEC (cited in IDS of 09/02/2020).

REMARKS CONCERNING CLAIMS

In the response to the Final Office Action submitted on April 24, 2021, claims 2, 11, and 20 were amended for clarity. According to the Advisory Action, the amendment has not been entered. To advance prosecution, Applicant has withdrawn the amendments to claims 2, 11 and 20, and claims 1-21 are as previously presented before the Final Office Action.

REMARKS CONCERNING REJECTIONS UNDER 35 U.S.C. 103(A)

It is unclear what the final office action refers to by "JEDEC (cited in IDS of 09/02/2000)." The file history of the present application shows that, among the references listed in the three IDS's filed on 09/02/2020, JEDEC Standard (JESD79-3) is the only document titled with "JEDEC," but JEDEC Standard (JESD79-3) does not seem to have the content that matches the statements made on page 4 of the final office action. Based on these statements, and upon checking the references titled with "JEDEC" in the IDS's filed in September 2020, Applicant believes that, by "JEDEC (cited in IDS of 09/02/2000)," the final office action is referring to JEDEC Standard, FBDIMM: Architecture and Protocol (January 2007) ("JESD206"), which is listed in the IDS filed on September 4, 2020. The remarks below are based on this understanding. A supplemental office action with the exact identification of the JEDEC reference cited by the final office action is hereby requested if the Applicant's understanding is incorrect. For consistency with the final office action, JESD206 is referred to hereafter as "JEDEC."

In KSR, the Supreme Court reaffirmed the doctrine that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR,* 550 U.S. at 416, 82 USPQ2d at 1395. The rationale to support a conclusion that the claim would have been obvious is that **all** of the claimed elements were

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known in the prior art, and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, if the combination yielded nothing more than predictable results to one of ordinary skill in the art. *Id.*; *Sakraida v. AG Pro, Inc.*, 425 U.S. 273, 282, 189 USPQ 449, 453 (1976); *Anderson's-Black Rock, Inc. v. Pavement Salvage Co.*, 396 U.S. 57, 62-63, 163 USPQ 673, 675 (1969); *Great Atl. & P. Tea Co. v. Supermarket Equip. Corp.*, 340 U.S. 147, 152, 87 USPQ 303, 306 (1950). "[I]t can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does." *KSR*, 550 U.S. at 418, 82 USPQ2d at 1396. If any of these findings cannot be made, then this rationale cannot be used to support a conclusion that the claim would have been obvious to one of ordinary skill in the art.

Accordingly, claims 2-21 are improperly rejected under 35 U.S.C. 103(a) as being unpatentable over Hazelzet in view of JEDEC because neither Hazelzet nor JEDEC teaches or suggests, among other things, "to apply (or applying) a first signal to the gate of the transistor (having an open drain coupled to the error edge connection) to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation," **and** "to apply (or applying) a second signal related to one or more training sequences to the gate of the transistor when the memory module performs training operations associated with the one or more training sequences." In other words, neither references teaches or suggests outputting a signal to indicate a parity error during normal memory operation and outputting a signal related to one or more training sequences during a training operation using the **same** open-drain output by applying different signals to the **same** gate of the **same** transistor.

Hazelzet uses **two** open drain outputs 120, 121 for reporting **two** different errors, a correctable error (e.g., error corrected by the ECC logic) and an uncorrectable error (e.g., uncorrectable ECC error or parity error), **respectively** (Hazelzet, [0072]), both during normal memory operations. Hazelzet never mentions outputting any signal related to training sequences, let alone teaching or suggesting outputting any signal related to training sequences using the **same** open-drain output for reporting parity errors. Therefore, Hazelzet does not teach or suggest "to apply a first signal … to indicate a parity error" and "to apply a second signal related to one or more training sequences" to the **same** gate of the **same** transistor in **different** operations.

JEDEC does not make up for the deficiencies of Hazelzet. Although JEDEC discusses training sequences, it does not teach or suggest outputting any signal related to the training

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sequences through an open-drain output, let alone an open drain output of a transistor with a gate that also receives first signal "to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation." Instead, JEDEC uses polling to deal with the situation that the training is carried out by the memory buffer without participation from the host. With polling, the host continues to send TS2 patters until it receives at least 4 TS2 patterns on its northbound receivers (JEDEC, p. 32-34 and Table 3-16). As discussed in the specification of present application, polling is one of the techniques the claimed invention is improving upon (Specification, [0016]). The claimed invention eliminates the need for polling by outputting a signal related to the training sequences through an open-drain output. To make the memory module backward compatible, the open-drain output is not just any open-drain output, it is the **same** open-drain output for reporting parity errors, a feature taught by none of the cited references, individually or in combination.

Furthermore, persons of ordinary skill in the art would not be motivated to combine JEDEC's training sequences with the ECC solution in Hazelzet, because Hazelzet's solution using ECC and JEDEC memory buffer training are distinct solutions to distinct problems. ECC is an effective way to reduce and eliminate soft and hard errors in memory systems in order to improve the reliability of data being communicated, while JEDEC's training seeks to pre-emptively optimize the performance of memory modules with memory buffers by resolving the timing issues associated with the memory buffers. Persons of ordinary skill in the art would not be motivated to add the training discussed in JEDEC to Hazelzet, or replace Hazelzet's ECC solution with JEDEC's trainings, to arrive at the claimed invention, because, first of all, Hazelzet does not use any memory buffers that would present the timing issues faced by JEDEC to begin with.

Moreover, there is no teaching or suggestion in either Hazelzet or JEDEC why it would be advantageous to use either of the outputs 120, 121 in Hazelzet to output a signal related to any training sequences. Thus, without the hindsight of the claimed invention, combining Hazelzet's ECC solution and JEDEC's training would not even arrive at the claimed invention.

Therefore, claims 2-21 are not combinations of know elements found in Hazelzet and JEDEC, and are thus patentable over Hazelzet in view of JEDEC.

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CONCLUDING REMARKS

By responding in the foregoing remarks only to particular positions asserted by the examiner, the Applicant does not necessarily acquiesce in other positions that have not been explicitly addressed. In addition, the Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: May 24, 2021

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

Customer No. 79141

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Electronic Acknowledgement Receipt

EFS ID:	42808380
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5066-US01
Receipt Date:	24-MAY-2021
Filing Date:	11-NOV-2019
Time Stamp:	23:41:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5066-US01_Response_FOA_AA.pdf	201163 9a4867b3afb1fe8d0a86cd88013d655bc21bff11	yes	11

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Response After Final Action	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	11
Warnings:			
Information:			
	Total Files Size (in bytes):	201163	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/680,060	11/11/2019	Hyun Lee	129980-5066-US01	8269

79141 7590 06/03/2021

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER
CHERY, MARDOCHEE

ART UNIT	PAPER NUMBER
2133	

NOTIFICATION DATE	DELIVERY MODE
06/03/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com

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Advisory Action Before the Filing of an Appeal Brief	**Application No.** 16/680,060	**Applicant(s)** Lee, Hyun	
	Examiner MARDOCHEE CHERY	**Art Unit** 2133	**AIA (FITF) Status** No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 24 May 2021 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☑ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:
   a) ☑ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection.The current period for reply expires ____ months from the mailing date of *the prior Advisory Action* or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.
   Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANTS FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37CFR 41.37(a).

AMENDMENTS

3. ☑ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   a) ☑ They raise new issues that would require further consideration and/or search (see NOTE below);
   b) ☑ They raise the issue of new matter (see NOTE below);
   c) ☑ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____ (See 37CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicants reply has overcome the following rejection(s): _____
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☑ For purposes of appeal, the proposed amendment(s):(a) ☑ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____
9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☑ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
13. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
14. ☐ Other: _____.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:
    Claim(s) allowed:_____.
    Claim(s) objected to:_____.
    Claim(s) rejected:2-21.
    Claim(s) withdrawn from consideration:_____.

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	05/28/2021

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Continuation of REQUEST FOR RECONSIDERATION/OTHER 12. The request for reconsideration has been considered but does NOT place the application in condition for allowance because: The After Final amendment filed on 5/24/2021 is a second amendment after final presented in the case and thus, has not been entered. Note that any second or subsequent amendment after final will be considered only to the extent that it removes issues for appeal or puts a claim in obvious patentable condition. See MPEP 2272(II).

DO NOT ENTER: /M.C/

05/28/2021

Electronically filed May 24, 2021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2133
Filed:	November 11, 2019	Examiner:	Chery, Mardochee
For:	*Memory Module Having an Open-Drain Output for Parity Error and for Training Sequences*	Attorney Docket No.:	129980-5066-US01

RESPONSE TO FINAL OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment and Remarks are in response to the Final Office Action dated February 24, 2021 and the Advisory Action dated May 5, 2021 for the above identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. 129980-5066-US01).

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Ex. 1002, p. 268

Doc Code: ECOMM.AUTH/ECOMM.WTDW
Doc Description: Internet Communications Authorized/Internet Communications Authorization Withdrawn

PTO/SB/439 (11-15)

AUTHORIZATION FOR INTERNET COMMUNICATIONS IN A PATENT APPLICATION OR REQUEST TO WITHDRAW AUTHORIZATION FOR INTERNET COMMUNICATIONS		
	Application No.	16/680,060
	Filing Date	2019-11-11
	First Named Inventor	Hyun LEE
	Art Unit	2133
	Examiner Name	Mardochee CHERY
	Practitioner Docket No.	129980-5066-US01

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. To authorize permission for Internet Communications.

☑ Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via video conferencing, instant messaging, or electronic mail. I understand that a copy of these communications will be made of record in the application file. (MPEP 502.03)

II. To withdraw authorization for Internet Communications.

☐ The authorization given on _____, to the USPTO to communicate with the undersigned and any practitioner in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via Internet communications such as video conferencing, instant messaging, or electronic mail is hereby withdrawn. I understand that the withdrawal is effective when approved rather than when received.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 51167.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Jamie J. Zheng/ — Signature

June 24, 2021 — Date

Jamie J. Zheng — Typed or printed name

650-521-4828 — Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Juristic entities must be represented by a patent practitioner (see 37 CFR 1.31, which is applicable to any paper filed on or after September 16, 2012, that is presented on behalf of a juristic entity, regardless of application filing date). Submit multiple forms if more than one signature is required, see below*.

☐ * Total of _____ forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	43080911
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5066-US01
Receipt Date:	24-JUN-2021
Filing Date:	11-NOV-2019
Time Stamp:	14:53:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Internet Communications Authorized	129980-5066__01_USPTO_SB439.pdf	103777 bc0799c9604909887d521bd1a8804a7fdf8f7751	no	2

Warnings:

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Information:	
Total Files Size (in bytes):	103777

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/680,060	11/11/2019	Hyun Lee	129980-5066-US01	8269

79141 7590 06/30/2021

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2133	

NOTIFICATION DATE	DELIVERY MODE
06/30/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com

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Applicant-Initiated Interview Summary	**Application No.** 16/680,060	**Applicant(s)** Lee, Hyun		
	Examiner MARDOCHEE CHERY	**Art Unit** 2133	**AIA (First Inventor to File) Status** No	**Page** 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	**Title**	**Type**
MARDOCHEE CHERY	Primary Examiner	Telephonic
Jamie Zheng (Reg. No. 51,167)	Attorney of Record	

Date of Interview: 25 June 2021

Issues Discussed:

Other

The Applicant's Representative and the Examiner discussed the Advisory action of 6/3/21 in view of the remarks filed 5/24/21 and 4/25/21. However, no agreement was reached.

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	6/25/21

Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04
Please further see:
MPEP 713.04
Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)
37 CFR § 1.2 Business to be transacted in writing

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2133
Filed:	November 11, 2019	Examiner:	Chery, Mardochee
For:	*Memory Module Having an Open-Drain Output for Parity Error and for Training Sequences*	Attorney Docket No.:	129980-5066-US01

INTERVIEW SUMMARY

Applicant's attorney thanks Examiner Chery for the opportunity to discuss the above-referenced patent application during a telephone interview on June 25, 2021, with Jamie Zheng. In the interview, consideration of the Remarks made in response to the Final Office Action, submitted on April 24, 2021, and again on May 24, 2021, was requested. No agreement was reached.

Respectfully submitted,

Date: July 2, 2021

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

Customer No. 79141

Electronic Acknowledgement Receipt

EFS ID:	43156150
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5066-US01
Receipt Date:	02-JUL-2021
Filing Date:	11-NOV-2019
Time Stamp:	03:03:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant summary of interview with examiner	129980-5066-US01_Interview_Summary.pdf	99445 a213d91efffe8bcc8086a4d510d85178f652d734	no	1

Warnings:

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Information:	
Total Files Size (in bytes):	99445

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/680,060	Filing Date 11/11/2019	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	07/26/2021	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/PAULA D MCCRAY STANLEY/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (02-18)
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	16/680,060	Filing Date	2019-11-11	Docket Number (if applicable)	NL066-13US01	Art Unit	2133
First Named Inventor	Hyun LEE			Examiner Name	Mardochee CHERY		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 603916

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

Applicant Signature

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Jamie J. Zheng/	Date (YYYY-MM-DD)	2021-07-26
Name	Jamie J. Zheng	Registration Number	51167

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Electronically filed July 26, 2021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2133
Filed:	November 11, 2019	Examiner:	Chery, Mardochee
For:	*Memory Module Having an Open-Drain Output for Parity Error and for Training Sequences*	Attorney Docket No.:	NL066-13US01

RESPONSE TO FINAL OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment and Remarks are in response to the Final Office Action dated February 24, 2021 and the Advisory Action dated May 5, 2021 for the above identified patent application, and are filed with a Request for Continued Examination (RCE).

Applicant petitions for a two-month extension of time to respond to the Final Office Action, which extends the period for responding to the Final Office Action from May 24, 2021 to July 26, 2021 (July 24-25, 2021, being on a weekend).

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. NL066-13US01).

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Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Currently Amended) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

a module controller on the printed circuit board and configurable to receive address and control signals associated with normal memory read or write operations via the first edge connections; and

dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and

wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

wherein the module controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation; and

wherein the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and ~~not associated with~~ when the dynamic random access memory elements are not accessed for any normal memory read or write operations.

3. (Previously Presented) The memory module of claim 2, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second

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state being a low logic level and the other one of the first state and the second state being a high impedance state.

4. (Previously Presented) The memory module of claim 3, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state.

5. (Previously Presented) The memory module of claim 3, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.

6. (Previously Presented) The memory module of claim 5, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.

7. (Previously Presented) The memory module of claim 2, wherein the module controller comprises an integrated circuit that includes the transistor.

8. (Currently Amended) The memory module of claim 2, wherein the operations associated with the one or more training sequences are performed when the ~~memory module is~~ dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations ~~between the dynamic random access memory elements and~~ with the memory controller via the second edge connections.

9. (Previously Presented) The memory module of claim 2, wherein the second edge connections are not active during the operations associated with the one or more training sequences.

10. (Previously Presented) The memory module of claim 2, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configurable to couple the first input to the output during

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the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.

11. (Currently Amended) A method of operation in a host system having a memory controller, comprising:

at a memory module coupled to the memory controller, the memory module including a printed circuit board, a module controller on the printed circuit board, and dynamic random access memory elements on the printed circuit board, the printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections, the module controller including a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

receiving, at the module controller, address and control signals associated with one or more normal memory read or write operations from the memory controller via the first edge connections;

outputting or receiving data signals at the dynamic random access memory elements in accordance with the address and control signals, the data signals being associated with the one or more normal memory read or write operations and communicated with the memory controller via the second edge connections;

applying a first signal to the gate of the transistor to indicate a parity error having occurred during one of the one or more normal memory read or write operations;

performing training operations associated with one or more training sequences ~~and not associated with~~ when the dynamic random access memory elements are not accessed for any normal memory read or write operations; and

applying a second signal related to the one or more training sequences to the gate of the transistor while the memory module performs the training operations.

12. (Previously Presented) The method of claim 11, wherein the error edge connection is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

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13. (Previously Presented) The method of claim 12, wherein the error edge connection is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state.

14. (Previously Presented) The method of claim 12, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.

15. (Previously Presented) The method of claim 14, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.

16. (Previously Presented) The method of claim 11, wherein the module controller comprises an integrated circuit that includes the transistor.

17. (Currently Amended) The method of claim 11, wherein the training operations associated with the one or more training sequences are performed when the ~~memory module is~~ dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations ~~between the dynamic random access memory elements and~~ with the memory controller via the second edge connections.

18. (Previously Presented) The method of claim 11, wherein the second edge connections are not active during the training operations associated with the one or more training sequences.

19. (Previously Presented) The method of claim 11, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein applying the first signal to the gate of the transistor includes coupling the first input to the output, and applying the second signal to the gate of the transistor includes coupling the second input to the output.

20. (Currently Amended) A memory module operable with a memory controller of a host system, comprising:

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a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

a module controller on the printed circuit board and configurable to receive from the memory controller via the first edge connections address and control signals associated with normal memory read or write operations; and

dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and

wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

wherein the module controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation;

wherein the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and ~~not associated with~~ when the dynamic random access memory elements are not accessed for any normal memory read or write operations;

wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground;

wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to a low impedance state, and drives the gate of the transistor low so as to drive the error edge connection to a high impedance state;

wherein the module controller comprises an integrated circuit that includes the transistor; and

wherein the integrated circuit further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configurable to couple the first input to the output during the normal memory read or write operation, and to couple the

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second input to the output during the operations associated with the one or more training sequences.

21. (Currently Amended) The memory module of claim 20, wherein the operations associated with the one or more training sequences are performed when the ~~memory module is~~ dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations ~~between the dynamic random access memory elements and~~ with the memory controller via the second edge connections.

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REMARKS

This amendment responds to the final office action dated February 24, 2021. In the final office action, the Examiner:

- rejected claims 2-21 under 35 U.S.C. 103(a) as being unpatentable over Hazelzet (US 20080098277 cited in IDS of 09/02/2020, hereafter "Hazelzet") in view of JEDEC (cited in IDS of 09/02/2020).

REMARKS CONCERNING CLAIMS

Claims 2, 8, 11, 17 and 20-21 have been amended for clarity.

No new matter has been added.

After entry of this amendment, the pending claims are: claims 2-21.

REMARKS CONCERNING REJECTIONS UNDER 35 U.S.C. 103(A)

It is unclear what the final office action refers to by "JEDEC (cited in IDS of 09/02/2000)." The file history of the present application shows that, among the references listed in the three IDS's filed on 09/02/2020, JEDEC Standard (JESD79-3) is the only document titled with "JEDEC," but JEDEC Standard (JESD79-3) does not seem to have the content that matches the statements made on page 4 of the final office action. Based on these statements, and upon checking the references titled with "JEDEC" in the IDS's filed in September 2020, Applicant believes that, by "JEDEC (cited in IDS of 09/02/2000)," the final office action is referring to JEDEC Standard, FBDIMM: Architecture and Protocol (January 2007) ("JESD206"), which is listed in the IDS filed on September 4, 2020. The remarks below are based on this understanding. A supplemental office action with the exact identification of the JEDEC reference cited by the final office action is hereby requested if the Applicant's understanding is incorrect. For consistency with the final office action, JESD206 is referred to hereafter as "JEDEC."

In KSR, the Supreme Court reaffirmed the doctrine that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR,* 550 U.S. at 416, 82 USPQ2d at 1395. The rationale to support a conclusion that the claim would have been obvious is that **all** of the claimed elements were known in the prior art, and one skilled in the art could have combined the elements as claimed by

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known methods with no change in their respective functions, if the combination yielded nothing more than predictable results to one of ordinary skill in the art. *Id.*; *Sakraida v. AG Pro, Inc.*, 425 U.S. 273, 282, 189 USPQ 449, 453 (1976); *Anderson's-Black Rock, Inc. v. Pavement Salvage Co.*, 396 U.S. 57, 62-63, 163 USPQ 673, 675 (1969); *Great Atl. & P. Tea Co. v. Supermarket Equip. Corp.*, 340 U.S. 147, 152, 87 USPQ 303, 306 (1950). "[I]t can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does." *KSR*, 550 U.S. at 418, 82 USPQ2d at 1396. If any of these findings cannot be made, then this rationale cannot be used to support a conclusion that the claim would have been obvious to one of ordinary skill in the art.

Accordingly, claims 2-21 are improperly rejected under 35 U.S.C. 103(a) as being unpatentable over Hazelzet in view of JEDEC because neither Hazelzet nor JEDEC teaches or suggests, among other things, "to apply (or applying) a first signal to the gate of the transistor (having an open drain coupled to the error edge connection) to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation," **and** "to apply (or applying) a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences." In other words, neither references teaches or suggests outputting a signal to indicate a parity error during normal memory operation and outputting a signal related to one or more training sequences during a training operation using the **same** open-drain output by applying different signals to the **same** gate of the **same** transistor.

Hazelzet uses **two** open drain outputs 120, 121 to report **two** different errors, a correctable error (e.g., error corrected by the ECC logic) and an uncorrectable error (e.g., uncorrectable ECC error or parity error), **respectively** (Hazelzet, [0072]), both during normal memory operations. Hazelzet never mentions outputting any signal related to training sequences, let alone teaching or suggesting outputting a signal related to training sequences using the **same** open-drain output for reporting parity errors. Therefore, Hazelzet does not teach or suggest "to apply a first signal … to indicate a parity error" and "to apply a second signal related to one or more training sequences" to the **same** gate of the **same** transistor in **different** operations.

JEDEC does not make up for the deficiencies of Hazelzet. Although JEDEC discusses training sequences, it does not teach or suggest outputting any signal related to the training sequences through an open-drain output, let alone an open drain output of a transistor with a gate

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that also receives first signal "to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation." Instead, JEDEC uses polling to deal with the situation that the training is carried out by the memory buffer without participation from the host. With polling, the host continues to send TS2 patters until it receives at least 4 TS2 patterns on its northbound receivers (JEDEC, p. 32-34 and Table 3-16). As discussed in the specification of present application, polling is one of the techniques the claimed invention attempts to avoid or is improving upon (Specification, [0016]). With the claimed invention, in which a signal related to training sequences is output through an open-drain output, the need for polling can be reduced or eliminated. To make the memory module backward compatible, the open-drain output is not just any open-drain output, it is the **same** open-drain output for reporting parity errors. This feature is taught by none of the cited references, individually or in combination.

Furthermore, persons of ordinary skill in the art would not be motivated to combine JEDEC's training sequences with the ECC solution in Hazelzet, because Hazelzet's ECC solution and JEDEC memory buffer training are distinct solutions to distinct problems. ECC is an effective way to reduce and eliminate soft and hard errors in memory systems in order to improve the reliability of data being communicated, while JEDEC's training seeks to pre-emptively optimize the performance of memory modules with memory buffers by resolving the timing issues associated with the memory buffers. Persons of ordinary skill in the art would not be motivated to add the training discussed in JEDEC to Hazelzet, or replace Hazelzet's ECC solution with JEDEC's trainings. Even if they do, they would not arrive at the claimed invention without impermissible hindsight because Hazelzet specifically teaches using two separate open drain outputs for parity error and ECC signals, respectively (Hazelzet, [0072]).

Moreover, there is no teaching or suggestion in either Hazelzet or JEDEC why it would be advantageous to use either of the outputs 120, 121 in Hazelzet to output a signal related to any training sequences. Thus, any such combination is based not on the teachings or suggestions of the references but on the hindsight gleaned from the claimed invention.

Therefore, claims 2-21 are not combinations of know elements found in Hazelzet and JEDEC, and are thus patentable over Hazelzet in view of JEDEC.

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CONCLUDING REMARKS

By responding in the foregoing remarks only to particular positions asserted by the examiner, the Applicant does not necessarily acquiesce in other positions that have not been explicitly addressed. In addition, the Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: July 26, 2021

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

Customer No. 79141

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Electronic Patent Application Fee Transmittal

Application Number:	16680060
Filing Date:	11-Nov-2019
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NL066-13US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 2 months with $0 paid	1252	1	640	640
Miscellaneous:				
RCE- 1ST REQUEST	1801	1	1360	1360
		Total in USD ($)		**2000**

Electronic Acknowledgement Receipt

EFS ID:	43348371
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NL066-13US01
Receipt Date:	26-JUL-2021
Filing Date:	11-NOV-2019
Time Stamp:	21:10:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$2000
RAM confirmation Number	E20217PL10463470
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	NL066-13US01_RCE_SB30.pdf	1364279 ec97a5759230d6ea46b29be94314408fa3dd30fb	no	3
Warnings:					
Information:					
2		NL066-13US01_Amendment_RCE.pdf	203611 bafa176fe805c48ab66e64cf290feec5716aacb8	yes	11

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment Submitted/Entered with Filing of CPA/RCE	1	1
Claims	2	7
Applicant Arguments/Remarks Made in an Amendment	8	11

Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	40647 dba0a6b25aef4afb0008b407e9c95c2b724e55b5	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1608537		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/680,060	11/11/2019	Hyun Lee	NL066-13US01	8269

79141 7590 09/15/2021

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2133	

NOTIFICATION DATE	DELIVERY MODE
09/15/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com

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Office Action Summary	Application No. 16/680,060	Applicant(s) Lee, Hyun	
	Examiner MARDOCHEE CHERY	Art Unit 2133	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 07/26/2021.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 2-21 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 2-21 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 4/26/2021.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

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DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/26/2021 has been entered.

Response to Arguments

3. Applicant's arguments filed 07/26/2021 have been fully considered but they are not persuasive.

a. Applicant's Representative argues on page 8 of the remarks of 07/26/2021 that "it is unclear what the final Office action refers to by "JEDEC (cited in IDS of 09/02/20)."

The Examiner respectfully disagrees. Sheet 8 of the IDS filed by applicant's Representative on 09/02/20 lists a document titled "JEDEC Standard (JESD79-3). However, it is noted that that document has a date-stamp of 09/04/20.

b. Applicant's Representative argues on page 9 of the remarks of 07/26/2021 that neither Hazelnet nor JEDEC teaches or suggests "to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation, and to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences."

The Examiner respectfully disagrees and would to point out that the alleged features are not positively recited in the claims and the alleged features are a statement of purpose or use

which do not add any patentable weight to the claims. As the language of the claims states, "the module controller is **to apply** a first signal to the gate of the transistor **to indicate** a parity error having occurred when the memory module is being accessed for a normal memory read or write operation, and **to apply** a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences." The claims do not positively recite "applying a first signal to the gate of the transistor **indicating** a parity error having occurred".

Thus, the limitations "**to apply** a first signal to the gate of the transistor **to indicate** a parity error having occurred…and **to apply** a second signal related to one or more training sequences to the gate of the transistor…" are intended use language, functional recitation, and statement of purpose and use which do not add any patentability weight to the claims. See, e.g., In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963) (The claims were directed to a core member for hair curlers and a process of making a core member for hair curlers. Court held that the intended use of hair curling was of no significance to the structure and process of making.); In re Sinex, 309 F.2d 488, 492, 135 USPQ 302, 305 (CCPA 1962) (statement of intended use in an apparatus claim did not distinguish over the prior art apparatus). If a prior art structure is capable of performing the intended use as recited in the preamble, then it meets the claim. See, e.g., In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997). See also MPEP § 2112 - § 2112.02. MPEP 2114.

c. Applicant's representative further argues on pages 9-10 of the remarks that neither references teaches or suggests "outputting a signal to indicate a parity error during normal memory operation and outputting a signal related to one or more training sequences during a training operation using the same open-drain output by applying different signals to the same gate of the same transistor."

The Examiner respectfully disagrees. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., outputting a signal to indicate a parity error during normal memory operation and outputting a signal related to one or more training sequences during a training operation using the same open-drain output by applying different signals to the same gate of the same transistor) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

d. Applicant's representative argues on page 10 of the remarks that "persons of ordinary skill in the art would not be motivated to combine JEDEC's training sequences with the ECC solution inHazelzet, because Hazelzet's ECC solution and JEDEC memory buffer training are distinct solutions to distinct problems."

The Examiner respectfully disagrees. In response to applicant's argument that "persons of ordinary skill in the art would not be motivated to combine JEDEC's training sequences with the ECC solution inHazelzet," the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

The Courts have made clear that the teaching, suggestion, or motivation test is flexible and an explicit suggestion to combine the prior art is not necessary. The motivation to combine may be implicit and may be found in the knowledge of one of ordinary skill in the art, or, in some cases, from the nature of the problem to be solved. Id. at 1366, 80 USPQ2d at 1649. "An implicit motivation to combine exists not only when a suggestion may be gleaned from the prior art as a whole, but when the improvement' is technology-independent and the combination of references results in a product or

process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient. Because the desire to enhance commercial opportunities by improving a product or process is universal-and even common-sensical-we have held that there exists in these situations a motivation to combine prior art references even absent any hint of suggestion in the references themselves. In such situations, the proper question is whether the ordinary artisan possesses knowledge and skills rendering him capable of combining the prior art references." Id. at 1368, 80 USPQ2d at 1651.< In re Sernaker, 702 F.2d 989, 994-95, 217 USPQ 1, 5-6 (Fed. Cir. 1983). >See also Dystar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick, 464 F.3d 1356, 1368, 80 USPQ2d 1641, 1651 (Fed. Cir. 2006).

The ultimate inference as to the existence of a motivation to combine references may boil down to a question of "common sense." *Philip W. Wyers v. Master Lock Company*, 95 USPQ2d 1525, 1532 (Fed. Cir. 2010) (internal citations omitted).

In view of the Supreme Court decision in KSR International Co. v. Teleflex Inc., the Examiner would like to point out that, in determining obviousness under 35 U.S.C 103, the Supreme Court stated that the Federal Circuit had erred in four ways: (1) "By holding that courts and patent examiners should look only to the problem the patentee was trying to solve;" (2) by assuming "that a person of ordinary skill attempting to solve a problem will be led only to those elements of prior art designed to solve the same problem;" (3) by concluding "that a patent claim cannot be proved obvious merely by showing that the combination of elements was obvious to try;" and (4) by overemphasizing "the risk of courts and patent examiners falling prey to hindsight bias" and as a result applying "rigid preventative rules that deny fact finders recourse to common sense."

Furthermore, the Supreme Court stated that: "When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill".

Still further, the court states that "the focus when making a determination of obviousness should be on what a person of ordinary skill in the pertinent art would have known at the time of the invention…and this is regardless of whether the source of that knowledge and ability was documentary prior art, general knowledge in the art, or common sense".

Finally, for purposes of 35 U.S.C 103, prior art can be either in the field of applicant's endeavor or be reasonably pertinent to the particular problem with which the applicant was concerned. Furthermore, prior art that is in a field of endeavor other than that of the applicant, or solves a problem which is different from that which the applicant was trying to solve, may also be considered for the purposes of 35 U.S.C 103. See, e.g., In re *KSR International Co. v. Teleflex Inc.,* 550 U.S. at,82 USPQ2d at 1396 (2007).

Claim Rejections - 35 USC § 103

4. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 2-24 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Hazelzet (20080098277 cited in IDS of 09/02/2020) and JEDEC (cited in IDS of 09/02/2020).

Regarding claim 1, Hazelzet discloses a memory module operable with a memory controller of a host system [FIG. 2], comprising: a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections [FIG. 2: *a DIMM with ECC/Parity buffer chip coupled to a memory interface chip which in turn coupled to a memory controller or processor; memory interface chip sends and receives data from the DIMM via data line and sends address and commands via a line; the memory interface chip then sends and receives data via the line to the DRAMs and sends address and command information to the register chip via the line; the memory interface chip further sends check bits for error correction purposes to the ECC/Parity register chip via another line*]; a module controller on the printed circuit board and configurable to receive address and control signals associated with normal memory read or write operations via the first edge connections [FIG. 2: *memory controller receiving address and control signals through DATA line, CMD/CHK BITS line*]; and dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals [FIG.2: *SDRAMs communicate data signals with memory controller via DATA, CMD/CHK BITS signals*]; and wherein the module controller includes a transistor having an open drain coupled to the error edge

connection, a source coupled to ground, and a gate [FIGs. 4A, 4B; ¶0062, 0067, 0072, 0109: *ECC mode signal source coupled to selection input of multiplexers and to error logic circuit, the multiplexers having their selection inputs coupled to a source; two open-drain outputs available for reporting an error are driven low*]; wherein the module controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation [¶0072, 0076, 0109: *UE indicates that a parity error occurred*].

Although Hazelzet discloses a test mode in which the controller apply a signal to training sequences [¶0082], Hazelzet does not explicitly disclose applying a signal to training sequences when performing operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations.

JEDEC, however, discloses wherein the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations [See JEDEC's Figures 3-4, 3-7, 3-6, 3-9, 3-11, 3-13, 3-14; Pages 14-54: *during the training sequences, JEDEC's memory controller communicates no data with the module and performs no operations to read or write to the memory devices, and that the training is carried out by memory buffer (module controller) itself; additionally Hazelzet's memory module can be placed into a training mode to implement JEDEC's training sequences*].

It would have been obvious to a POSITA to combine Hazelzet and JEDEC in order to perform multiple functions during multiple operations/modes including initialization/training because such was well known to improve memory module reliability (Pages 14-54).

Regarding claim 3, Hazelzet discloses the memory module of claim 2, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the

second state being a low logic level and the other one of the first state and the second state being a high impedance state [¶0018-0020].

Regarding claim 4, Hazelzet discloses the memory module of claim 3, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state [¶0018-0020].

Regarding claim 5, Hazelzet discloses the memory module of claim 2, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to ground, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state [¶0018-0020, 0022, 0067].

Regarding claim 6, Hazelzet discloses the memory module of claim 5, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground [¶0098-0099].

Regarding claim 7, Hazelzet discloses the memory module of claim 2, wherein the module controller comprises an integrated circuit that includes the transistor [¶0072].

Regarding claim 8, JEDEC discloses the memory module of claim 2, wherein the operations are associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections [Page 66: all DIMMs can be accessed from a single command one bit per DIMM].

Regarding claim 9, Hazelzet discloses the memory module of claim 2, wherein the second edge connections are not active during the operations associated with the one or more training sequences [¶0066].

Regarding claim 10, Hazelzet discloses the memory module of claim 2, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configurable to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences [FIGs. 4A, 4B].

Regarding claim 11, the rationale in the rejection of claim 2 is herein incorporated.

Regarding claim 12, the rationale in the rejection of claim 3 is herein incorporated.

Regarding claim 13, the rationale in the rejection of claim 4 is herein incorporated.

Regarding claim 14, the rationale in the rejection of claim 5 is herein incorporated.

Regarding claim 15, the rationale in the rejection of claim 6 is herein incorporated.

Regarding claim 16, the rationale in the rejection of claim 7 is herein incorporated.

Regarding claim 17, the rationale in the rejection of claim 8 is herein incorporated.

Regarding claim 18, the rationale in the rejection of claim 9 is herein incorporated.

Regarding claim 19, the rationale in the rejection of claim 10 is herein incorporated.

Regarding claim 20, the rationale in the rejection of claims 2-10 is herein incorporated.

Regarding claim 21, the rationale in the rejection of claim 4 is herein incorporated.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Emma et al. (9389876) discloses a memory array accessible by a plurality of word lines and bit lines; each memory cell comprises a transistor wherein the transistor has a gate, a source and a drain.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARDOCHEE CHERY whose telephone number is (571)272-4246. The examiner can normally be reached from 900-500.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Jared Rutz** can be reached on **(571)272-5535**. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Respectfully Submitted,
USPTO

Dated: September 10, 2021

By: /MARDOCHEE CHERY/
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Facsimile: 571-273-4246

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/680,060	Lee, Hyun
	Examiner	Art Unit
	MARDOCHEE CHERY	2133

CPC - Searched*		
Symbol	Date	Examiner
(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2029/4402 or G11C2207/2254)	08/30/2020	MC

CPC Combination Sets - Searched*		
Symbol	Date	Examiner
(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2029/4402 or G11C2207/2254)	08/30/2020	MC

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	154	08/30/2020	MC

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST; Inventor; Assignee; CPC	08/30/2020	MC
EAST; GOOGLE NPL	09/10/2021	MC

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	08/30/2020

Samsung Electronics Co., Ltd.
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/680,060	Lee, Hyun
	Examiner	Art Unit
	MARDOCHEE CHERY	2133

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	08/30/2020

Samsung Electronics Co., Ltd.
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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/680,060	Lee, Hyun
	Examiner	Art Unit
	MARDOCHEE CHERY	2133

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/30/2020	02/20/2021	09/10/2021						
	1	-	-	-						
	2	✓	✓	✓						
	3	✓	✓	✓						
	4	✓	✓	✓						
	5	✓	✓	✓						
	6	✓	✓	✓						
	7	✓	✓	✓						
	8	✓	✓	✓						
	9	✓	✓	✓						
	10	✓	✓	✓						
	11	✓	✓	✓						
	12	✓	✓	✓						
	13	✓	✓	✓						
	14	✓	✓	✓						
	15	✓	✓	✓						
	16	✓	✓	✓						
	17	✓	✓	✓						
	18	✓	✓	✓						
	19	✓	✓	✓						
	20	✓	✓	✓						
	21	✓	✓	✓						

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	9	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/18 14:54
S2	2	S1 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/18 14:55
S3	50	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/18 14:57
S4	3	S3 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/18 14:57
S6	4	"8621170".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/19 18:18
S7	2	("8489837" "8489837").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/03 18:03

S9	54	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/03/02 17:33
S10	3	S9 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/03/02 17:33
S11	1	S10 and (manufactur$3 industry) near3 standard	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/03/02 17:33
S12	1	S10 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/03/02 17:35
S13	9	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/03/02 17:36
S14	5	S13 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/03/02 17:36
S15	51	controller near5 (open near2 drain near2 (I/O output))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/25 14:55

S16	0	S15 and (parity near3 (error signal bit check)) with (host computer CPU node)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/25 14:57
S17	0	S15 and (parity near3 (error signal bit check)) same (host computer CPU node)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/25 14:57
S18	2	S15 and (parity near3 (error signal bit check))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/25 14:57
S19	2	S15 and ((parity error) near5 (signal bit check))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/25 14:57
S20	41	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 00:53
S21	0	S20 and (drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 00:55
S22	2,094,169	(FET MOSFET transistor p-junction n-junction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 00:56

S23	1	S20 and (FET MOSFET transistor p-junction n-junction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 00:56
S24	0	controller near3 (open near2 drain) with (parity ECC) with controller near5 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:17
S25	0	controller near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:18
S26	0	(controller hub switch channel) near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:19
S27	0	(controller hub switch channel) with (open near2 drain) with (parity ECC) with controller with (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:19
S28	0	(controller hub switch channel) with (open near2 drain) with (parity ECC redundancy (correct$3 near2 code)) with controller with (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:20
S29	47	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:20

S30	0	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) same (parity ECC redundancy (correct$3 near2 code))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:21
S31	2	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:21
S32	31	S29 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:23
S33	3	S32 and (parity ECC redundancy error (correct$3 near2 code))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:24
S34	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/14 11:55
S35	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/14 11:57
S36	3	mardochee and filter near3 snoop	US-PGPUB; USPAT;	SAME	ON	2016/11/14 11:59

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S37	71	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:00
S38	3	S37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:06
S39	3	S37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate pin)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:08
S40	2	S37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) near5 ($3RAM DIM DIMM SODIMM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:09
S41	3	S37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:12
S42	2	S41 and (error fault ECC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:13

S43	2	S41 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:13
S44	2	S43 and (transistor $3FET drain$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:14
S45	2	S43 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:15
S46	2	S45 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:31
S47	4	("20100202240" "20080256281").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:32
S48	2	S47 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:32
S49	1	S47 and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:35

S50	4	("20100202240" "20080256281").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/24 14:13
S51	3	"20060062047".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/24 14:41
S52	27,512	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:09
S53	44	S52 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:11
S54	0	S53 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:12
S55	0	S53 and (controller hub switch channel) same (open$3 near2 drain) same controller with (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:13
S56	23	S53 and (open$3 near2 drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:13

S57	14	S56 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:14
S58	11	S56 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:19
S60	5	("20060262586" "20060062047").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/29 00:37
S61	14	("9858218" "9311116" "8489837").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:23
S62	0	S61 and edge near3 connect$3 near5 ("not" "don't" "doesn't") near2 (active activat$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:31
S63	14	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:32
S64	78	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:32

S65	66	controller near5 (open near2 drain near2 (I/O output))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:32
S66	6	S65 and ((parity error) near5 (signal bit check))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:32
S67	53	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:33
S68	4	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:33
S69	29,963	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:34
S70	48	S69 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:34
S71	24	S70 and (open$3 near2 drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:34

S72	12	S71 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:34
S74	142	("3414781" "3560935" "4672570" "5388074" "5438536" "5511152" "5450576" "5606662" "5684979" "5835733" "6693840" "6754787" "6763437" "6886109" "7024518" "7065688" "7093115" "7155579" "7221699" "7266633" "7489163" "7525860" "7539909" "7568130" "7586350" "7647467" "7757101" "8074034" "8139430" "8359521" "8429493" "20030115427" "20050071580" "20050193161" "200600062047" "20060262586" "20070091702" "20070136523" "20070214347" "20080098277" "20080147897" "20080155378" "20080256281" "20090119464" "20100005218" "20100042778" "20100142383" "20100202240" "20110022789").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/15 13:19
S75	7	S74 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/15 13:19
S76	714	"2" and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/15 13:20
S77	4	S74 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/15 13:20
S78	6	S75 and (open$3 near2 drain)	US-PGPUB; USPAT; USOCR;	OR	ON	2019/03/15 13:20

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S79	138,210	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:42
S80	4,275	S79 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:42
S81	30	S80 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:44
S82	15	S81 and (open$3 near2 drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:45
S83	1	S82 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:45
S84	0	S83 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:46

S85	1	S82 and (handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:46
S86	4	S82 and (FET MOSFET transistor p-junction n-junction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:47
S87	2	S86 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:48
S88	2	S87 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:52
S89	48,967	(LEE near2 HYUN).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:54
S90	18,643	S89 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:54
S91	8	S90 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:55

S92	0	S91 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:56
S95	2	"6798891".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/11 12:39
S96	36,607	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
S97	55	S96 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
S98	25	S97 and (open$3 near2 drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
S99	13	S98 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
S100	162,327	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25

		G11C16/26 or G11C29/78 or G11C2207/2254).cpc.				
S101	5,271	S100 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
S102	31	S101 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
S103	15	S102 and (open$3 near2 drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
S104	1	S103 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
S105	0	S104 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
S106	52,734	(LEE near2 HYUN).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:26
S107	18,670	S106 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/08/30 20:26

			DERWENT; IBM_TDB			
S108	8	S107 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:26
S109	0	S108 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:26
S110	162,327	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2029/4402 or G11C2207/2254).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:29
S111	5,271	S110 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:32
S112	31	S111 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:32
S113	6	S112 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:34
S114	211	netlist.as.	US-PGPUB; USPAT; USOCR;	OR	ON	2020/08/30 20:35

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S115	6	S114 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:35
S116	1	S115 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:36
S117	3	"20080098277".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 21:06
S118	2	S117 and (transistor mosfet fet (discrete near2 element) source drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 21:53
S119	0	S117 and (transistor mosfet fet (discrete near2 element) source drain gate) with (controller) with (parity error)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 21:55
S120	1	S117 and (train$3 test$3 diagnosys sampl$3) near5 (signal input$4 output$4 sequence series operation command read$3 writ$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 22:23
S121	1	S117 and (train$3 test$3 diagnosys sampl$3) near5 (mode signal input$4 output$4 sequence series operation command read$3 writ$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2021/02/20 22:26

		with (transistor mosfet fet (discrete near2 element) source drain gate memory)	JPO; DERWENT; IBM_TDB			
S122	0	S117 and (low near5 state)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 23:05
S123	1	S117 and (low high) near5 (pull$3 state level impedance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 23:06
S124	1	S117 and edge	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 23:21
S125	0	S117 and (edge pin connector) near5 (first primary second$3) near5 (active inactive enabl$3 disabl$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 23:23
S126	0	S117 and (edge pin connector) near5 (first primary second$3) with (active inactive enabl$3 disabl$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 23:23
S127	1	S117 and (edge pin connector) near5 (first primary second$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 23:23
S128	1	S117 and (edge pin connector contact) with (active inactive enabl$3 disabl$3 off on)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2021/02/20 23:26

			DERWENT; IBM_TDB			

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed April 26, 2021	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	LEE, Hyun
				Art Unit	2133
				Examiner Name	MARDOCHEE, Chery
Sheet	1	of	1	Attorney Docket Number	129980-5066-US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

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		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2024, "Declaration of Matthew S. Galica," filed 08MAR2021, 4 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2025, "Declaration of Andrew H. DeVoogd," filed 08MAR2021, 4 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2026, "Remote Deposition Under Oral Examination of Dr. Donald Alpert, March 10, 2021," filed 11MAR2021, 493 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2027, "DDR3 SDRAM LRDIMM," filed 11MAR2021, 18 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2028, "Join JEDEC Membership Details," filed 11MAR2021, 2 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2029, "DRAM Circuit Design: Fundamental and High-Speed Topics," filed 11MAR2021, 4 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2030, "Semiconductor Memories: A Handbook and Design, Manufacture, and Application Second Edition," filed 11MAR2021, 6 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2031, "Deposition of Donald Alpert, Ph.D.," filed 11MAR2021, 218 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2032, "Declaration of Robert J. Murphy," filed 11MAR2021, 65 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Paper 21, "Patent Owner's Response Under 37 C.F.R. Section 42.120," 11MAR2021, 68 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Paper 22, "Patent Owner's Request for Rehearing of Institution Decision," 30MAR2021, 12 pgs.
		Inter Partes Review of US Patent No. 9,858,218, Case No. IPR2020-01044, Exhibit 2032, "Declaration of Robert J. Murphy," filed 12MAR2021, 63 pgs.

Examiner Signature	/MARDOCHEE CHERY/	Date Considered	09/10/2021

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Ex. 1002, p. 333

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.C./

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Three-dimensional processing system having independent ...

Grant · Filed Jan 13, 2014 · Issued Jul 12, 2016 · Philip G. Emma · International Business Machines Corporation

In other words, to obtain the same power consumption or power density profile, ...

wherein the access transistor 222 has a gate terminal connected to a word ...

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/680,060	Filing Date 11/11/2019	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	12/15/2021	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/KIM R WATSON/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

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PATENT AND TRADEMARK OFFICE

Little, Kevin

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Sent: Wednesday, December 15, 2021 11:55 PM
To: PatentApp15DEC21
Subject: US Patent Application No. 16/680,060 filed November 11, 2019 - Response to Office Action dated September 15, 2021
Attachments: NL066-13US01_Amendment_NFOA_After_RCE.pdf; JESD_79-3.pdf

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Sir:

The enclosed Amendment and Remarks are in response to the Non-Final Office Action dated September 15, 2021, in the above identified patent application.

Thanks,

/Jamie J. Zheng/
Jamie J. Zheng
Customer No. 79141

Jamie Zheng, Ph.D, Esq.
USCH Law, PC
(650) 521-4828

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OPAP AKUMA-13
DEC 15 2021
PATENT & TRADEMARK OFFICE

Electronically filed December 15, 2021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2133
Filed:	November 11, 2019	Examiner:	Chery, Mardochee
For:	*Memory Module Having an Open-Drain Output for Parity Error and for Training Sequences*	Attorney Docket No.:	NL066-13US01

RESPONSE TO NON-FINAL OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment and Remarks are in response to the Non-Final Office Action dated September 15, 2021, in the above identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. NL066-13US01).

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Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Previously Presented) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

a module controller on the printed circuit board and configurable to receive address and control signals associated with normal memory read or write operations via the first edge connections; and

dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and

wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

wherein the module controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation; and

wherein the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations.

3. (Previously Presented) The memory module of claim 2, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

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4. (Previously Presented) The memory module of claim 3, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state.

5. (Previously Presented) The memory module of claim 3, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.

6. (Previously Presented) The memory module of claim 5, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.

7. (Previously Presented) The memory module of claim 2, wherein the module controller comprises an integrated circuit that includes the transistor.

8. (Previously Presented) The memory module of claim 2, wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.

9. (Previously Presented) The memory module of claim 2, wherein the second edge connections are not active during the operations associated with the one or more training sequences.

10. (Previously Presented) The memory module of claim 2, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configurable to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.

11. (Previously Presented) A method of operation in a host system having a memory controller, comprising:

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at a memory module coupled to the memory controller, the memory module including a printed circuit board, a module controller on the printed circuit board, and dynamic random access memory elements on the printed circuit board, the printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections, the module controller including a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

receiving, at the module controller, address and control signals associated with one or more normal memory read or write operations from the memory controller via the first edge connections;

outputting or receiving data signals at the dynamic random access memory elements in accordance with the address and control signals, the data signals being associated with the one or more normal memory read or write operations and communicated with the memory controller via the second edge connections;

applying a first signal to the gate of the transistor to indicate a parity error having occurred during one of the one or more normal memory read or write operations;

performing training operations associated with one or more training sequences when the dynamic random access memory elements are not accessed for any normal memory read or write operations; and

applying a second signal related to the one or more training sequences to the gate of the transistor while the memory module performs the training operations.

12. (Previously Presented) The method of claim 11, wherein the error edge connection is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

13. (Previously Presented) The method of claim 12, wherein the error edge connection is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state.

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14. (Previously Presented) The method of claim 12, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.

15. (Previously Presented) The method of claim 14, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.

16. (Previously Presented) The method of claim 11, wherein the module controller comprises an integrated circuit that includes the transistor.

17. (Previously Presented) The method of claim 11, wherein the training operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.

18. (Previously Presented) The method of claim 11, wherein the second edge connections are not active during the training operations associated with the one or more training sequences.

19. (Previously Presented) The method of claim 11, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein applying the first signal to the gate of the transistor includes coupling the first input to the output, and applying the second signal to the gate of the transistor includes coupling the second input to the output.

20. (Previously Presented) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

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a module controller on the printed circuit board and configurable to receive from the memory controller via the first edge connections address and control signals associated with normal memory read or write operations; and

dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and

wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

wherein the module controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation;

wherein the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations;

wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground;

wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to a low impedance state, and drives the gate of the transistor low so as to drive the error edge connection to a high impedance state;

wherein the module controller comprises an integrated circuit that includes the transistor; and

wherein the integrated circuit further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configurable to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.

21. (Previously Presented) The memory module of claim 20, wherein the operations associated with the one or more training sequences are performed when the dynamic random

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access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.

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REMARKS

This amendment responds to the Office Action dated September 15, 2021. In the Office Action, the Examiner:

- rejected claims 2-21 under 35 U.S.C. 103(a) as being unpatentable over Hazelzet (US 20080098277 cited in IDS of 09/02/2020, hereafter "Hazelzet") in view of JEDEC (cited in IDS of 09/02/2020).

REMARKS CONCERNING RESPONSE TO ARGUMENTS

Applicant appreciates the Examiner identifying JESD79-3 as "JEDEC (cited in IDS of 09/02/2000)." There were three IDS's submitted on 09/02/2020 and multiple JEDEC references listed in the three IDS's. Thus, without the identification, Applicant was at lost trying to guess the exact JEDEC reference referred to in the previous office actions.

The Examiner responded to Applicant's arguments submitted on July 26, 2021 by stating:

> As the language of the claims states, "the module controller is to apply a first signal to the gate of the transistor to indicate a parity error having occurred ... , and to apply a second signal related to one or more training sequences to the gate of the transistor ...." The claims do not positively recite "applying a first signal to the gate of the transistor indicating a parity error having occurred."
>
> Thus, the limitations "to apply a first signal to the gate of the transistor to indicate a parity error having occurred ... and to and to apply a second signal related to one or more training sequences to the gate of the transistor ...." are intended use language, functional recitation, and statement of purpose and use which do not add any patentability weight to the claims.

Applicant respectfully disagrees. First, the claims do not just recite "to apply a first signal the gate of the transistor to indicate a parity error having occurred ... and to and to apply a second signal related to one or more training sequences to the gate of the transistor ...." The claims recite, among other things, "the module controller **is configurable to** apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation" and "wherein the module controller **is further configurable to** apply a second signal related to one or more training

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sequences to the gate of the transistor when ..." (emphasis added). Thus, the claims are partially defined by the functions that the module controller is configurable to carry out, and Applicant made the arguments that the circuits in the cited references were not configurable to perform the functions recited in the claims, because no such functions were even taught or suggested in either of the cited references.

There is nothing inherently wrong with defining some part of an invention in functional terms. Functional language does not, in and of itself, render a claim improper. Id. In fact, 35 U.S.C. 112(f) and pre-AIA 35 U.S.C. 112, sixth paragraph, expressly authorize a form of functional claiming (means- (or step-) plus- function claim limitations discussed in MPEP § 2181et seq.). Functional language may also be employed to limit the claims without using the means-plus-function format. See, e.g., K-2 Corp. v. Salomon S.A., 191 F.3d 1356, 1363, 52 USPQ2d 1001, 1005 (Fed. Cir. 1999). Unlike means-plus-function claim language that applies only to purely functional limitations, Phillips v. AWH Corp., 415 F.3d 1303, 1311, 75 USPQ2d 1321, 1324 (Fed. Cir. 2005) (en banc) ("Means-plus-function claiming applies only to purely functional limitations that do not provide the structure that performs the recited function."), functional claiming often involves the recitation of some structure followed by its function. For example, in In re Schreiber, the claims were directed to a conical spout (the structure) that "allow[ed] several kernels of popped popcorn to pass through at the same time" (the function). In re Schreiber, 128 F.3d 1473, 1478, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997). As noted by the court in Schreiber, "[a] patent applicant is free to recite features of an apparatus either structurally or functionally." Id. See also MPEP § 2173.05(g).

Functional claim language that is not limited to a specific structure covers all devices that are **capable** of performing the recited function. Therefore, if the prior art discloses a device that can inherently perform the claimed function, a rejection under 35 U.S.C. 102 and/or 35 U.S.C. 103 may be appropriate. See *In re Translogic Technology, Inc.,* 504 F.3d 1249, 1258, 84 USPQ2d 1929, 1935-1936 (Fed. Cir. 2007).

REMARKS CONCERNING REJECTIONS UNDER 35 U.S.C. 103(A)

In rejecting claim 2 under 35 U.S.C. 103(a) as being unpatentable over Hazelzet in view of JEDEC, the Office Action alleges:

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> JEDEC, however discloses wherein the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations [See JEDEC's Figures 3-4, 3-7, 3-6, 3-9, 3-11, 3-13, 3-14; pages 14-54 during the training sequences, JEDEC's memory controller communicates no data with the module and performs no operations to read or write to the memory devices, and that the training is carried out by memory buffer (module controller) itself; additionally Hazelzet's memory module can be placed into a training mode to implement JEDEC's training sequences.

Applicant respectfully disagrees. First, there are no Figures 3-4, 3-7, 3-6, 3-9, 3-11, 3-13, 3-14 in JESD79-3, which is identified as "JEDEC (cited in IDS of 09/02/2000)" and which is attached as Exhibit I for easy reference. As shown in Exhibit I, the figures in JESD79-3 are labeled as Figure1, Figure 2, Figure 3, ..., so Applicant is at lost again trying to find Figures 3-4, 3-7, 3-6, 3-9, 3-11, 3-13, 3-14 in JESD79-3, as referred to in the Office Action.

Second, the Office Action cites these figures in JEDEC as disclosing "during the training sequences, JEDEC's memory controller communicates no data with the module and performs no operations to read or write to the memory devices." The Office Action fails show, however, where in JEDEC it is taught or suggested that "the module controller is further configurable to apply a second signal related to one or more training sequences to the gate of the transistor," the same gate upon which the module controller is also configurable to apply the first signal to indicate a parity error having occurred.

In other words, without showing any teaching or suggestion in either Hazelzet or JEDEC of a module controller configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred during normal memory read or write operations, and then a second signal related to one or more training sequences to the **same** gate of the transistor, the Office Action fails to establish a prima facie case of obviousness of claim 2 over Hazelzet in view of JEDEC.

Therefore, claim 2 is not a combination of of know elements found in Hazelzet and JEDEC, and is thus patentable over Hazelzet in view of JEDEC.

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Claims 3-10 depend from claim 2 and include further limitations in addition to the limitations in claim 2. Therefore, claims 3-10 are patentable for at least similar reasons claim 2 is patentable.

Furthermore, regarding claims 3-5, the Office Action alleges that "Hazelzet discloses wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state." Applicant respectfully disagrees. The Office Action has not established that Hazelzet discloses applying a signal related to training sequences to the gate of a transistor having an open drain output, let alone how such a signal would the error edge connection.

Regarding claim 10, the Office Action cites Hazelzet's FIGS. 4A, 4B as disclosing "wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configurable to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences." Applicant respectfully disagrees.

Hazelzet's FIGS. 4A and 4B show many multiplexors (e.g., MUX 60a, 60e, 61, 62a, 62n in FIG. 4A and MUX 102a, ..., 102n, 103, 104, 105a, 105b, 106a, 106b), as multiplexors are common in electronic circuits. It is unclear which multiplexor the Office Action is referring to, but none of the multiplexors in Hazelzet's FIGS. 4A and 4B has an output coupled to the gate of a transistor having an open drain output, a first input to receive the first signal for indicating a parity error, and a second input to receive the second signal related to one or more training sequences. Here again, the Office Action fails to establish a prima facie case of obviousness.

The arguments related to claim 2 apply to claim 11. Claim 11 recites, among other things, "applying a first signal to the gate of the transistor to indicate a parity error having occurred during one of the one or more normal memory read or write operations," "performing training operations ...," and "applying a second signal related to the one or more training sequences to the gate of the transistor while the memory module performs the training operations," which, as discussed above, are not found in either Hazelzet, or JEDEC, or their combination. Therefore, claim 11 is also patentable.

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Claims 12-19 depend from claim 11 and include further limitations in addition to the limitations in claim 11. Therefore, claims 12-19 are patentable for at least similar reasons claim 11 is patentable.

Furthermore, regarding claims 12-14, Hazelzet does not teach or suggest applying a signal related to training sequences to the gate of a transistor having an open drain output, let alone how such a signal would drive the error edge connection.

Regarding claim 19, none of the many multiplexors in Hazelzet's FIGS. 4A and 4B is "a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal," where the first signal is for indicating parity error and the second signal is related to one or more training sequences, as recited in claim 19.

The above arguments apply to claim 20. For example, Hazelzet, or JEDEC, or their combination does not teach or suggest, among other things, "wherein the module controller comprises an integrated circuit that includes" "a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate" and "further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal," where the first signal is for indicating a parity error and the second signal is related to one or more training sequences, as recited in claim 20.

Therefore claim 20 is patentable over Hazelzet in view of JEDEC.

Claim 21 depends from claim 20 and includes further limitations in addition to the limitations in claim 20. Therefore, claim 21 is patentable for at least similar reasons claim 20 is patentable.

Withdrawal of the rejections is therefore respectfully requested.

CONCLUDING REMARKS

By responding in the foregoing remarks only to particular positions asserted by the examiner, the Applicant does not necessarily acquiesce in other positions that have not been explicitly addressed. In addition, the Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

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Ex. 1002, p. 348

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: December 15, 2021

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

Customer No. 79141

Samsung Electronics Co., Ltd.
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OPAP AKIMA-13
DEC 15 2021
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Exhibit I

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/680,060	11/11/2019	Hyun Lee	NL066-13US01	8269

79141 7590 12/21/2021

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2133	

NOTIFICATION DATE	DELIVERY MODE
12/21/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com

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Applicant-Initiated Interview Summary	**Application No.** 16/680,060	**Applicant(s)** Lee, Hyun		
	Examiner MARDOCHEE CHERY	**Art Unit** 2133	**AIA (First Inventor to File) Status** No	**Page** 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	**Title**	**Type**
MARDOCHEE CHERY	Primary Examiner	Telephonic
Jamie Zheng (Reg. No. 51167)	Attorney	

Date of Interview: 16 December 2021

Issues Discussed:

35 U.S.C. 103

Applicant's Representative and the Examiner discussed the outstanding rejection over Hazelzet (20080098277) and JEDEC (both cited in the IDS of 9/2/20) as well as further amendment. However, no agreement was reached.

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	12/16/21

Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04
Please further see:
MPEP 713.04
Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)
37 CFR § 1.2 Business to be transacted in writing

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

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Electronically filed January 7, 2022

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2133
Filed:	November 11, 2019	Examiner:	Chery, Mardochee
For:	*Memory Module Having an Open-Drain Output for Parity Error and for Training Sequences*	Attorney Docket No.:	NL066-13US01

SUPPLEMENTAL RESPONSE TO NON-FINAL OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This submission supplements the Response to the Non-Final Office Action dated September 15, 2021, filed on December 15, 2021, in the above identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. NL066-13US01).

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Ex. 1002, p. 353

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Currently Amended) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

a module controller on the printed circuit board and ~~configurable~~ configured to receive address and control signals associated with normal memory read or write operations via the first edge connections; and

dynamic random access memory elements on the printed circuit board and ~~configurable~~ configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and

wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

wherein the module controller is ~~configurable~~ configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation; and

wherein the module controller is further ~~configurable~~ configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations.

3. (Previously Presented) The memory module of claim 2, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second

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state being a low logic level and the other one of the first state and the second state being a high impedance state.

4. (Previously Presented) The memory module of claim 3, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state.

5. (Previously Presented) The memory module of claim 3, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.

6. (Previously Presented) The memory module of claim 5, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.

7. (Previously Presented) The memory module of claim 2, wherein the module controller comprises an integrated circuit that includes the transistor.

8. (Previously Presented) The memory module of claim 2, wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.

9. (Previously Presented) The memory module of claim 2, wherein the second edge connections are not active during the operations associated with the one or more training sequences.

10. (Currently Amended) The memory module of claim 2, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input configured to receive the first signal, and a second input configured to receive the second signal, and wherein the module controller is ~~configurable~~ configured to couple the first input to the output during the normal memory read or write operation, and to

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couple the second input to the output during the operations associated with the one or more training sequences.

11. (Previously Presented) A method of operation in a host system having a memory controller, comprising:

at a memory module coupled to the memory controller, the memory module including a printed circuit board, a module controller on the printed circuit board, and dynamic random access memory elements on the printed circuit board, the printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections, the module controller including a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

receiving, at the module controller, address and control signals associated with one or more normal memory read or write operations from the memory controller via the first edge connections;

outputting or receiving data signals at the dynamic random access memory elements in accordance with the address and control signals, the data signals being associated with the one or more normal memory read or write operations and communicated with the memory controller via the second edge connections;

applying a first signal to the gate of the transistor to indicate a parity error having occurred during one of the one or more normal memory read or write operations;

performing training operations associated with one or more training sequences when the dynamic random access memory elements are not accessed for any normal memory read or write operations; and

applying a second signal related to the one or more training sequences to the gate of the transistor while the memory module performs the training operations.

12. (Previously Presented) The method of claim 11, wherein the error edge connection is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

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13. (Previously Presented) The method of claim 12, wherein the error edge connection is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state.

14. (Previously Presented) The method of claim 12, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.

15. (Previously Presented) The method of claim 14, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.

16. (Previously Presented) The method of claim 11, wherein the module controller comprises an integrated circuit that includes the transistor.

17. (Previously Presented) The method of claim 11, wherein the training operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.

18. (Previously Presented) The method of claim 11, wherein the second edge connections are not active during the training operations associated with the one or more training sequences.

19. (Previously Presented) The method of claim 11, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein applying the first signal to the gate of the transistor includes coupling the first input to the output, and applying the second signal to the gate of the transistor includes coupling the second input to the output.

20. (Currently Amended) A memory module operable with a memory controller of a host system, comprising:

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a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

a module controller on the printed circuit board and ~~configurable~~ configured to receive from the memory controller via the first edge connections address and control signals associated with normal memory read or write operations; and

dynamic random access memory elements on the printed circuit board and ~~configurable~~ configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and

wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

wherein the module controller is ~~configurable~~ configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation;

wherein the module controller is further ~~configurable~~ configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations;

wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground;

wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to a low impedance state, and drives the gate of the transistor low so as to drive the error edge connection to a high impedance state;

wherein the module controller comprises an integrated circuit that includes the transistor; and

wherein the integrated circuit further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is ~~configurable~~ configured to couple the first input to the output during the normal memory read or write operation, and to

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couple the second input to the output during the operations associated with the one or more training sequences.

21. (Previously Presented) The memory module of claim 20, wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.

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REMARKS

This submission supplements the response to the Office Action dated September 15, 2021, which was submitted on December 15, 2021.

INTERVIEW SUMMARY

Applicant's attorney thanks Examiner Chery for the opportunity to discuss the above-referenced patent application during a telephone interview on December 16, 2021, with Jamie Zheng. In the interview, the outstanding rejection over the cited references were discussed, as well as the Examiner's interpretation of the word "configurable" in the claims. The Examiner suggested that all recitations of the word "configurable" be replaced with the word "configured." Applicant's attorney agreed to make the changes in a supplemental amendment, as submitted herewith.

REMARKS CONCERNING CLAIM AMENDMENT

Claims 2, 10 and 20 have been amended as suggested by the Examiner during the Examiner's Interview on December 16, 2021.

No new matter has been added.

After entry of this amendment, the pending claims are: claims 2-21.

Reconsideration of the pending claims in light of the amendments made herein and the remarks made in the Response to Office Action submitted on December 15, 2021, is respectfully requested.

With respect to all amendments, Applicant has not dedicated or abandoned any unclaimed subject matter. Moreover, Applicant has not acquiesced to any characterizations of the invention, nor any rejections or objections of the claims, made by the Examiner. Moreover, the Applicant hereby rescinds any prior disclaimer of claim scope, to the extent they exist, made during the prosecution of this application or made during the prosecution of any patent or other related patents/applications, and advises the Examiner that any such previous disclaimers and the cited references that they were made to avoid may need to be revisited.

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The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: January 7, 2022

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

Customer No. 79141

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 7, 2022	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
Sheet	1	of	1	Attorney Docket Number	129980-5066US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		7,411,862 B2	08-12-2008	Hein et al.	
		20060277355 A1	12-07-2006	Ellsberry et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, EXHIBITS 1067, Samsung Electronics Co. LTD., et al. v. Netlist Inc., In the United States District Court for the District of Delaware, 'Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract,' filed October 15, 2021
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, EXHIBITS 1061, Netlist, Inc. vs. SK Hynix Inc., et al., In the United States District Court for the Western District of Texas Waco Division, 'Claim Construction Order,' issued March 12, 2021, filed October 15, 2021
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, EXHIBITS 1055, 'Declaration of Sung Joo Park,' filed October 15, 2021
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, EXHIBITS 1003, 'Declaration of Donald Alpert,' filed October 15, 2021
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, PAPER 1, 'Petition for Inter Partes Review of U.S. Patent No. 9,858,218,' October 15, 2021
		Inter Partes Review No. 2022-00064 of US Patent No. 10474595, EXHIBITS 1003, 'Declaration of Donald Alpert,' filed October 15, 2021
		Inter Partes Review No. 2022-00064 of US Patent No. 10474595, PAPER 1, 'Petition for Inter Partes Review of U.S. Patent No. 10,474,595,' October 15, 2021

Examiner Signature		Date Considered	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	LEE, Hyun	Confirmation No.:	8269
Serial No.:	16/680,060	Group Art Unit:	2133
Filed:	November 11, 2019	Examiner:	MARDOCHEE, Chery
For:	*MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES*	Attorney Docket No.:	NL066-13US01

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☒ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☐ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

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☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

3d. ☐ The $120 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

4d. ☐ The $120 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

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5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial Nos. _____, filed on _____, of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

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9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Deposit Account No. 60-3916 (order no. NL066-13US01).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: January 7, 2022

/Jamie J. Zheng/ 51,167

Jamie Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828

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Electronic Patent Application Fee Transmittal

Application Number:	16680060
Filing Date:	11-Nov-2019
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NL066-13US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
		Total in USD ($)		**260**

Electronic Acknowledgement Receipt

EFS ID:	44699861
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NL066-13US01
Receipt Date:	07-JAN-2022
Filing Date:	11-NOV-2019
Time Stamp:	21:42:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$260
RAM confirmation Number	E202217L43134658
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		NL066-13US01_Supplemental_Amendment_NFOA_After_RCE.pdf	178589 6b993d471cec49b1eccbe8d4f8d4beb99e5f8c5c	yes	9

Multipart Description/PDF files in .zip description

Document Description	Start	End
Supplemental Response or Supplemental Amendment	1	1
Claims	2	7
Applicant Arguments/Remarks Made in an Amendment	8	9

Warnings:

Information:

2	Information Disclosure Statement (IDS) Form (SB08)	NL066-12US01_IDS_List_2021-01-07.pdf	186185 d4fc895668817ab5dbaadace0197046f5b6d1e1a	no	1

Warnings:

Information:

This is not an USPTO supplied IDS fillable form

3	Non Patent Literature	Samsung_DJ_Complaint.pdf	1300992 acc58326c49d1e1321f227d74ac735258705c9cf	no	82

Warnings:

Information:

4	Non Patent Literature	Claim_Construction_Order_218-595-523.pdf	302312 c0d2c5345ed42266ad8cf978b9f679f1bbde74a6	no	5

Warnings:

Information:

5	Non Patent Literature	IPR2022-00062_SJ-Park_Declaration.pdf	13566570 67e5afe71732ad23a55ae975fa6deb237b6d2ea6	no	95
Warnings:					
Information:					
6	Non Patent Literature	IPR2022-00062_Alpert_Declaration.pdf	2345915 a48185a14f491bfa8fc983d413b0f0547f14cb6e	no	168
Warnings:					
Information:					
7	Non Patent Literature	IPR2022-00062_Petition.pdf	2603739 788aa7606af3ab3233a2cad194136c35a5fb053b	no	102
Warnings:					
Information:					
8	Non Patent Literature	IPR2022-00064_Alpert_Declaration.pdf	2126444 c4f54a3f7c7460d1f845992beab5a9283643e13f	no	197
Warnings:					
Information:					
9	Non Patent Literature	IPR2022-00064_Petition.pdf	2835434 40764a8b7e7b60b9d5bea71c6ada961aab12431f	no	108
Warnings:					
Information:					
10	Transmittal Letter	NL066-12US01_IDS_Transmittal_2021-01-07.pdf	126067 679bcf7230763c94d618d4eebcfa651a960036af	no	4
Warnings:					
Information:					
11	Fee Worksheet (SB06)	fee-info.pdf	38101 de75958bf43a1abac299132f8c9488d944925866	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	25610348	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

OK TO ENTER: /M.C/

02/17/2022

Electronically filed January 7, 2022

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	8269
Serial No.:	16/680,060	Art Unit:	2133
Filed:	November 11, 2019	Examiner:	Chery, Mardochee
For:	*Memory Module Having an Open-Drain Output for Parity Error and for Training Sequences*	Attorney Docket No.:	NL066-13US01

SUPPLEMENTAL RESPONSE TO NON-FINAL OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This submission supplements the Response to the Non-Final Office Action dated September 15, 2021, filed on December 15, 2021, in the above identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. NL066-13US01).

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Google "parity" error "normal operation" "training" "training operation" "same" "gate" "tran

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www.google.com/patents/US9389876

Three-dimensional processing system having independent ...

Grant · Filed Jan 13, 2014 · Issued Jul 12, 2016 · Philip G. Emma · International Business Machines Corporation

In other words, to obtain the same power consumption or power density profile, ...

wherein the access transistor 222 has a gate terminal connected to a word ...

Overview · Related · Discuss

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UNITED STATES PATENT AND TRADEMARK OFFICE

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Alexandria, Virginia 22313-1450
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NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 02/23/2022

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER
CHERY, MARDOCHEE

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 02/23/2022

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/680,060	11/11/2019	Hyun Lee	NL066-13US01	8269

TITLE OF INVENTION: MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	05/23/2022

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

Samsung Electronics Co., Ltd.
Ex. 1002, p. 375

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 02/23/2022

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/680,060	11/11/2019	Hyun Lee	NL066-13US01	8269

TITLE OF INVENTION: MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	05/23/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHERY, MARDOCHEE	2133	711-154000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Samsung Electronics Co., Ltd.
Ex. 1002, p. 376

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/680,060	11/11/2019	Hyun Lee	NL066-13US01	8269

79141 7590 02/23/2022

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER	
CHERY, MARDOCHEE	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 02/23/2022

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Samsung Electronics Co., Ltd.
EX1002, p. 378

Notice of Allowability	Application No. 16/680,060	Applicant(s) Lee, Hyun	
	Examiner MARDOCHEE CHERY	Art Unit 2133	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to reply filed 01/07/2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 2-21 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 1/7/22.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	2/12/21

Samsung Electronics Co., Ltd.
Ex. 1002, p. 379

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/680,060	Lee, Hyun
	Examiner	Art Unit
	MARDOCHEE CHERY	2133

CPC - Searched*		
Symbol	Date	Examiner
(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2029/4402 or G11C2207/2254)	08/30/2020	MC

CPC Combination Sets - Searched*		
Symbol	Date	Examiner
(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2029/4402 or G11C2207/2254)	08/30/2020	MC

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	154	08/30/2020	MC

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST; Inventor; Assignee; CPC	08/30/2020	MC
EAST; GOOGLE NPL	09/10/2021	MC
EAST Updated	02/12/2022	MC

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	08/30/2020

Samsung Electronics Co., Ltd.
Ex. 1002, p. 380

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/680,060	Lee, Hyun
	Examiner	Art Unit
	MARDOCHEE CHERY	2133

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	See Attached	02/12/2022	MC

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	08/30/2020

Samsung Electronics Co., Ltd.
Ex. 1002, p. 381

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/680,060	Lee, Hyun
	Examiner	**Art Unit**
	MARDOCHEE CHERY	2133

CPC								
Symbol							**Type**	**Version**
G06F	/	13	/	1694			F	2013-01-01
G11C	/	5	/	04			I	2013-01-01
G11C	/	7	/	1063			I	2013-01-01
G06F	/	13	/	1668			I	2013-01-01
G06F	/	9	/	445			I	2013-01-01
G06F	/	13	/	24			I	2013-01-01
G06F	/	3	/	0619			I	2013-01-01
G06F	/	3	/	0632			I	2013-01-01
G06F	/	3	/	0659			I	2013-01-01
G06F	/	3	/	0673			I	2013-01-01
G06F	/	11	/	1068			I	2013-01-01
G11C	/	29	/	52			I	2013-01-01
G06F	/	12	/	0646			I	2013-01-01
G11C	/	2207	/	2254			A	2013-01-01
G11C	/	5	/	00			A	2013-01-01
G11C	/	7	/	1066			A	2013-01-01
G11C	/	16	/	26			A	2013-01-01
G11C	/	29	/	78			A	2013-01-01
G11C	/	2029	/	4402			A	2013-01-01

CPC Combination Sets									
Symbol							**Type**	**Set**	**Ranking**	**Version**
	/		/							

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	12 February 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office

Part of Paper No.: 20220211

Samsung Electronics Co., Ltd.
Ex. 1002, p. 382

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/680,060	Lee, Hyun
	Examiner	**Art Unit**
	MARDOCHEE CHERY	2133

INTERNATIONAL CLASSIFICATION					
CLAIMED					
G06F	/	12	/	00	
NON-CLAIMED					
	/		/		

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
711	154

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE (Assistant Examiner) (Date)	**Total Claims Allowed:** 20	
/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133 (Primary Examiner) 12 February 2022 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Samsung Electronics Co., Ltd.
Ex. 1002, p. 383

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/680,060	Lee, Hyun
	Examiner	**Art Unit**
	MARDOCHEE CHERY	2133

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
-	1	9	10	18	19										
1	2	10	11	19	20										
2	3	11	12	20	21										
3	4	12	13												
4	5	13	14												
5	6	14	15												
6	7	15	16												
7	8	16	17												
8	9	17	18												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	12 February 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office

Part of Paper No.: 20220211

Samsung Electronics Co., Ltd.
Ex. 1002, p. 384

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 8269

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
16/680,060	11/11/2019	711	2133	NL066-13US01

APPLICANTS
Netlist, Inc., Irvine, CA;

INVENTORS
Hyun Lee, Ladera Ranch, CA;

**** CONTINUING DATA ***************************
This application is a CON of 15/857,553 12/28/2017 PAT 10474595
which is a CON of 15/088,115 04/01/2016 PAT 9858218
which is a CON of 13/942,721 07/16/2013 PAT 9311116
which is a CON of 12/815,339 06/14/2010 PAT 8489837
which claims benefit of 61/186,799 06/12/2009

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
11/27/2019

Foreign Priority claimed	❑ Yes ☑ No	❑ Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	❑ Yes ☑ No					
Verified and Acknowledged	/MARDOCHEE CHERY/ Examiner's Signature	Initials	CA	3	1	1

ADDRESS
USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304
UNITED STATES

TITLE
MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES

FILING FEE RECEIVED		
1880	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other _____ ❑ Credit

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed January 7, 2022	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
Sheet	1	of	1	Attorney Docket Number	129980-5066US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		7,411,862 B2	08-12-2008	Hein et al.	
		20060277355 A1	12-07-2006	Ellsberry et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, EXHIBITS 1067, Samsung Electronics Co. LTD., et al. v. Netlist Inc., In the United States District Court for the District of Delaware, 'Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract,' filed October 15, 2021
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, EXHIBITS 1061, Netlist, Inc. vs. SK Hynix Inc., et al., In the United States District Court for the Western District of Texas Waco Division, 'Claim Construction Order,' issued March 12, 2021, filed October 15, 2021
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, EXHIBITS 1055, 'Declaration of Sung Joo Park,' filed October 15, 2021
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, EXHIBITS 1003, 'Declaration of Donald Alpert,' filed October 15, 2021
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, PAPER 1, 'Petition for Inter Partes Review of U.S. Patent No. 9,858,218,' October 15, 2021
		Inter Partes Review No. 2022-00064 of US Patent No. 10474595, EXHIBITS 1003, 'Declaration of Donald Alpert,' filed October 15, 2021
		Inter Partes Review No. 2022-00064 of US Patent No. 10474595, PAPER 1, 'Petition for Inter Partes Review of U.S. Patent No. 10,474,595,' October 15, 2021

Examiner Signature	/MARDOCHEE CHERY/	Date Considered	02/12/2022

All References Considered Except Where Lined Through. /M.C/

EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S8	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.	USPAT	SAME	ON	2016/02/18 00:10
S59	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.	USPAT	SAME	ON	2017/09/28 16:08
S73	3	("9858218" "9311116" "8489837").pn.	USPAT	OR	ON	2018/08/22 17:23
S93	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.	USPAT	SAME	ON	2019/08/05 14:40
S94	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification	USPAT	SAME	ON	2019/08/05 14:40

		signal indicat$3 status initialization mode memory controller via least output$4)).clm.				
S129	0	"20080098277".pn.	USPAT	OR	ON	2021/02/20 21:05
S130	1	(output$4 issu$3 broadcast$3) near5 (parity near3 error) with (output$4 issu$3 broadcast$3) near5 (train$3) with (open near3 (drain gate source transistor))	USPAT	OR	ON	2021/09/10 20:58
S131	1	(output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) same (output$4 issu$3 broadcast$3) near5 (train$3 test$3) near4 (signal operation code instruction) same ((open$3 clos$3 shun$4) near3 (drain gate source transistor))	USPAT	OR	ON	2021/09/10 21:03
S132	148	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) and (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) and ((open$3 clos$3 shun$4) near3 (drain gate source transistor))	USPAT	OR	ON	2021/09/10 21:10
S133	145	S132 and @ad<"20090612"	USPAT	OR	ON	2021/09/10 21:13
S134	4	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) and (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) and ("same") near3 ((open$3 clos$3 shun$4) near3 (drain gate source transistor))	USPAT	OR	ON	2021/09/10 21:14
S135	4	S134 and @ad<"20090612"	USPAT	OR	ON	2021/09/10 21:15
S136	124	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) and (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) and ("same") near3 ((drain gate source transistor))	USPAT	OR	ON	2021/09/10 21:15
S137	121	S136 and @ad<"20090612"	USPAT	OR	ON	2021/09/10 21:17
S138	0	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) same (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3)	USPAT	OR	ON	2021/09/10 21:20

		near4 (signal operation code instruction) same ("same") near3 ((drain gate source transistor))				
S149	0	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) same (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) same ("same") near3 ((drain gate source transistor))	USPAT	OR	ON	2022/02/12 14:59

2/12/2022 5:53:38 PM
C:\Users\mchery\Documents\EAST\Workspaces\13942721.wsp

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
		("3414781" "3560935" "4672570" "5388074" "5438536" "5511152" "5450576" "5606662" "5684979" "5835733" "6693840" "6754787" "6763437" "6886109" "7024518" "7065688" "7093115" "7155579" "7221699" "7266633" "7489163" "7525860" "7539909" "7568130" "7586350" "7647467" "7757101" "8074034" "8139430" "8359521" "8429493" "20030115427" "20050071580"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/15 13:16
		S53 and (controller hub switch channel) same (open$4 near2 drain) same controller with (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:12
S1	9	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/18 14:54
S2	2	S1 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/18 14:55
S3	50	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/18 14:57
S4	3	S3 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2015/05/18 14:57

			JPO; DERWENT; IBM_TDB			
S6	4	"8621170".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/19 18:18
S7	2	("8489837" "8489837").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/09/03 18:03
S9	54	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/03/02 17:33
S10	3	S9 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/03/02 17:33
S11	1	S10 and (manufactur$3 industry) near3 standard	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/03/02 17:33
S12	1	S10 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/03/02 17:35
S13	9	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2016/03/02 17:36

			DERWENT; IBM_TDB			
S14	5	S13 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/03/02 17:36
S15	51	controller near5 (open near2 drain near2 (I/O output))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/25 14:55
S16	0	S15 and (parity near3 (error signal bit check)) with (host computer CPU node)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/25 14:57
S17	0	S15 and (parity near3 (error signal bit check)) same (host computer CPU node)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/25 14:57
S18	2	S15 and (parity near3 (error signal bit check))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/25 14:57
S19	2	S15 and ((parity error) near5 (signal bit check))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/25 14:57
S20	41	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2016/09/24 00:53

			DERWENT; IBM_TDB			
S21	0	S20 and (drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 00:55
S22	2,094,169	(FET MOSFET transistor p-junction n-junction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 00:56
S23	1	S20 and (FET MOSFET transistor p-junction n-junction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 00:56
S24	0	controller near3 (open near2 drain) with (parity ECC) with controller near5 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:17
S25	0	controller near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:18
S26	0	(controller hub switch channel) near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:19
S27	0	(controller hub switch channel) with (open near2 drain) with (parity ECC) with controller with (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2016/09/24 01:19

			DERWENT; IBM_TDB			
S28	0	(controller hub switch channel) with (open near2 drain) with (parity ECC redundancy (correct$3 near2 code)) with controller with (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:20
S29	47	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:20
S30	0	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) same (parity ECC redundancy (correct$3 near2 code))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:21
S31	2	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:21
S32	31	S29 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:23
S33	3	S32 and (parity ECC redundancy error (correct$3 near2 code))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/24 01:24
S34	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	SAME	ON	2016/11/14 11:55

		"7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	DERWENT; IBM_TDB			
S35	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/14 11:57
S36	3	mardochee and filter near3 snoop	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2016/11/14 11:59
S37	71	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:00
S38	3	S37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:06
S39	3	S37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate pin)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:08
S40	2	S37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) near5 ($3RAM DIM DIMM SODIMM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2016/11/14 12:09

			DERWENT; IBM_TDB			
S41	3	S37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:12
S42	2	S41 and (error fault ECC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:13
S43	2	S41 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:13
S44	2	S43 and (transistor $3FET drain$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:14
S45	2	S43 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:15
S46	2	S45 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:31
S47	4	("20100202240" "20080256281").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2016/11/14 12:32

			DERWENT; IBM_TDB			
S48	2	S47 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:32
S49	1	S47 and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/11/14 12:35
S50	4	("20100202240" "20080256281").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/24 14:13
S51	3	"20060062047".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/24 14:41
S52	27,512	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:09
S53	44	S52 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:11
S54	0	S53 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2017/09/28 16:12

			DERWENT; IBM_TDB			
S55	0	S53 and (controller hub switch channel) same (open$3 near2 drain) same controller with (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:13
S56	23	S53 and (open$3 near2 drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:13
S57	14	S56 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:14
S58	11	S56 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:19
S60	5	("20060262586" "20060062047").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/29 00:37
S61	14	("9858218" "9311116" "8489837").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:23
S62	0	S61 and edge near3 connect$3 near5 ("not" "don't" "doesn't") near2 (active activat$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2018/08/22 17:31

			DERWENT; IBM_TDB			
S63	14	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:32
S64	78	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:32
S65	66	controller near5 (open near2 drain near2 (I/O output))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:32
S66	6	S65 and ((parity error) near5 (signal bit check))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:32
S67	53	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:33
S68	4	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:33
S69	29,963	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2018/08/22 17:34

		(controller device microcontroller micro-controller) and drain$3	DERWENT; IBM_TDB			
S70	48	S69 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:34
S71	24	S70 and (open$3 near2 drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:34
S72	12	S71 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/08/22 17:34
S74	142	("3414781" "3560935" "4672570" "5388074" "5438536" "5511152" "5450576" "5606662" "5684979" "5835733" "6693840" "6754787" "6763437" "6886109" "7024518" "7065688" "7093115" "7155579" "7221699" "7266633" "7489163" "7525860" "7539909" "7568130" "7586350" "7647467" "7757101" "8074034" "8139430" "8359521" "8429493" "20030115427" "20050071580" "20050193161" "200600062047" "20060262586" "20070091702" "20070136523" "20070214347" "20080098277" "20080147897" "20080155378" "20080256281" "20090119464" "20100005218" "20100042778" "20100142383" "20100202240" "20110022789").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/15 13:19
S75	7	S74 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/15 13:19

S76	714	"2" and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/15 13:20
S77	4	S74 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/15 13:20
S78	6	S75 and (open$3 near2 drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/15 13:20
S79	138,210	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:42
S80	4,275	S79 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:42
S81	30	S80 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:44
S82	15	S81 and (open$3 near2 drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/08/05 14:45

			DERWENT; IBM_TDB			
S83	1	S82 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:45
S84	0	S83 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:46
S85	1	S82 and (handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:46
S86	4	S82 and (FET MOSFET transistor p-junction n-junction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:47
S87	2	S86 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:48
S88	2	S87 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:52
S89	48,967	(LEE near2 HYUN).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/08/05 14:54

			DERWENT; IBM_TDB			
S90	18,643	S89 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:54
S91	8	S90 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:55
S92	0	S91 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/05 14:56
S95	2	"6798891".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/08/11 12:39
S96	36,607	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
S97	55	S96 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
S98	25	S97 and (open$3 near2 drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/08/30 20:25

			DERWENT; IBM_TDB			
S99	13	S98 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
S100	162,327	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
S101	5,271	S100 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
S102	31	S101 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
S103	15	S102 and (open$3 near2 drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
S104	1	S103 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:25
S105	0	S104 and @ad<"20090612"	US-PGPUB; USPAT; USOCR;	OR	ON	2020/08/30 20:25

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S106	52,734	(LEE near2 HYUN).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:26
S107	18,670	S106 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:26
S108	8	S107 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:26
S109	0	S108 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:26
S110	162,327	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2029/4402 or G11C2207/2254).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:29
S111	5,271	S110 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:32

S112	31	S111 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:32
S113	6	S112 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:34
S114	211	netlist.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:35
S115	6	S114 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:35
S116	1	S115 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/30 20:36
S117	3	"20080098277".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 21:06
S118	2	S117 and (transistor mosfet fet (discrete near2 element) source drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 21:53

S119	0	S117 and (transistor mosfet fet (discrete near2 element) source drain gate) with (controller) with (parity error)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 21:55
S120	1	S117 and (train$3 test$3 diagnosys sampl$3) near5 (signal input$4 output$4 sequence series operation command read$3 writ$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 22:23
S121	1	S117 and (train$3 test$3 diagnosys sampl$3) near5 (mode signal input$4 output$4 sequence series operation command read$3 writ$4) with (transistor mosfet fet (discrete near2 element) source drain gate memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 22:26
S122	0	S117 and (low near5 state)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 23:05
S123	1	S117 and (low high) near5 (pull$3 state level impedance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 23:06
S124	1	S117 and edge	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 23:21
S125	0	S117 and (edge pin connector) near5 (first primary second$3) near5 (active inactive enabl$3 disabl$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 23:23

S126	0	S117 and (edge pin connector) near5 (first primary second$3) with (active inactive enabl$3 disabl$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 23:23
S127	1	S117 and (edge pin connector) near5 (first primary second$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 23:23
S128	1	S117 and (edge pin connector contact) with (active inactive enabl$3 disabl$3 off on)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/20 23:26
S139	35	("20060277355" | "7411862" | "20030115427" | "20050071580" | "3414781" | "3560935" | "4672570" | "5388074" | "5438536" | "5450576" | "5511152" | "5606662" | "5684979" | "5835733" | "6693840" | "6754787" | "6763437" | "6886109" | "7024518" | "7065688" | "7093115" | "7155579" | "7221699" | "7266633" | "7489163" | "7525860" | "7539909" | "7568130" | "7586350" | "7647467" | "7757101" | "8074034" | "8139430" | "8359521" | "8429493").PN.	US-PGPUB; USPAT	OR	ON	2022/02/12 14:59
S140	2	S139 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/02/12 15:00
S141	0	S140 and controller near5 (open near2 drain near2 (I/O output))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/02/12 15:01

S142	101	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/02/12 15:18
S143	13	S142 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/02/12 15:18
S144	12	S143 and ((parity error) near5 (signal bit check))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/02/12 15:19
S145	4	S144 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/02/12 15:20
S146	4	S145 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/02/12 15:21
S147	4	S146 and (open$3 near2 drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/02/12 15:21
S148	1	S147 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2022/02/12 15:26

2/12/2022 5:54:01 PM
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed April 3, 2022	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
Sheet	1	of	2	Attorney Docket Number	129980-5066US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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		8,402,208	2013-03-19	Berke	
		8,452,917	2013-05-28	Amer et al.	
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		2011/0007585	2011-01-13	Shan et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, PAPER 7, PATENT OWNERS PRELIMINARY RESPONSE, filed February 18, 2022
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, EXHIBIT 2001, Declaration of Robert J. Murphy, filed February 18, 2022
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, EXHIBIT 2019, Redline comparison of 2022IPR-00064 to IPR2020-01042, filed February 18, 2022
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, EXHIBIT 3001, Emails regarding Petitioner's request for authorization to file pre-institution replies, filed March 10, 2022
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, PAPER No. 11. Petitioner's Authorized Reply to Patent Owner's Preliminary Response, filed March 18, 2022
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, PAPER NO. 12, PATENT OWNERS AUTHORIZED SUR-REPLY IN SUPPORT OF ITS PRELIMINARY RESPONSE, filed March 25, 2022
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, PAPER No. 8, ORDER Conduct of the Proceeding 37 C.F.R. sec 42.5, issued March 11, 2022
		Inter Partes Review No. 2020-00064 of US Patent No.10474595, Paper No. 7, NETLIST, INC.S PATENT OWNERS PRELIMINARY RESPONSE, filed February 18, 2022

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed April 3, 2022	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
Sheet	2	of	2	Attorney Docket Number	129980-5066US01

		Inter Partes Review No. 2020-00064 of US Patent No.10474595, EXHIBIT 2001, Declaration of Robert J. Murphy, filed February 18, 2022
		Inter Partes Review No. 2020-00064 of US Patent No.10474595, EXHIBIT 2019, Redline comparison of 2022IPR-00064 to IPR2020-01042, filed February 18, 2022
		Inter Partes Review No. 2020-00064 of US Patent No.10474595, Paper No. 11, Petitioner's Authorized Reply to Patent Owner's Preliminary Response, filed March 18, 2022
		Inter Partes Review No. 2020-00064 of US Patent No.10474595, Paper No. 12, PATENT OWNERS AUTHORIZED SUR-REPLY IN SUPPORT OF ITS PRELIMINARY RESPONSE, filed March 25, 2022
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Examiner Signature		Date Considered	

Electronic Patent Application Fee Transmittal

Application Number:	16680060
Filing Date:	11-Nov-2019
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NL066-13US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
		Total in USD ($)		**260**

Electronic Acknowledgement Receipt

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Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NL066-13US01
Receipt Date:	04-APR-2022
Filing Date:	11-NOV-2019
Time Stamp:	01:50:32
Application Type:	Utility under 35 USC 111(a)

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RAM confirmation Number	E202244257173436
Deposit Account	
Authorized User	

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	NL066-12US01_IDS_Transmittal_2022-04-03.pdf	125105 e57a644d19d2d0549adf0f3b32bec8abe35e7374	no	4
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	NL066-12US01_IDS_List_2022-04-03.pdf	207763 4fe302ea39d4d45a40b8299a85447a92710e8fd7	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Non Patent Literature	IPR2022-00062_POPR.pdf	610417 386f04478650cdeb6e27a1cfdf94811db4d8d28f	no	74
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4	Non Patent Literature	IPR2022-00062_PO_Reply_Paper-12.pdf	216277 c84d666e5e7c8c03d34dfbfbd85d7ebd67734979	no	11
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5	Non Patent Literature	IPR2022-00062_Order_Paper-8.pdf	140797 57250f5b261c484aa6080508a32847ffad0f2983	no	5
Warnings:					
Information:					
6	Non Patent Literature	IPR2022-00064_POPR.pdf	619730 cd79cea5656d502649f8023893ca62850b8f3a9d	no	78
Warnings:					

Information:					
7	Non Patent Literature	IPR2022-00062_Ex-2001.pdf	1521273 c78342a6c071ff3070c2c8581f102a8d35da0b83	no	88
Warnings:					
Information:					
8	Non Patent Literature	IPR2022-00064_Ex-2001.pdf	1525244 8db51e4fb6eb61afe9fc85319533b0155310dc2c	no	90
Warnings:					
Information:					
9	Non Patent Literature	IPR2022-00064_Ex-2006.pdf	2407413 1619e5386b6472ca19b0c44324286589c725d273	no	5
Warnings:					
Information:					
10	Non Patent Literature	IPR2022-00062_Ex-2013.pdf	523746 ee9ad81c4c4e3bc6340d1dff3c3cc9aa7f327e2e	no	2
Warnings:					
Information:					
11	Non Patent Literature	IPR2022-00064_Ex-2017.pdf	237036 558b15b3563f42777c6e4e8f6a92803cbfd4b609	no	7
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Information:					
12	Non Patent Literature	IPR2022-00062_Ex-2019.pdf	985073 38f85a10123013eaea3fd35cb1c7f7beda7de53d	no	96
Warnings:					
Information:					
13	Non Patent Literature	IPR2022-00062_Ex-3001.pdf	330479 cb8b163e3c47b33e821ba0ec4e93964642ffcce7	no	5
Warnings:					
Information:					

14	Non Patent Literature	IPR2022-00062_Petitioner_Reply_POPR.pdf	314112 b95d42af0d96e3f416818de76ff5ad70e6e7596c	no	16
Warnings:					
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15	Non Patent Literature	IPR2022-00064_Ex-2019.pdf	739468 38f0483431c9cda339ffb9361ac10c73530c4584	no	118
Warnings:					
Information:					
16	Non Patent Literature	IPR2022-00064_Petitioner_Reply_POPR.pdf	312923 14bde1afd3bb7a077bb34f1c3720bab5427ebf9d	no	16
Warnings:					
Information:					
17	Non Patent Literature	IPR2022-00064_PO_Reply_Paper-12.pdf	213039 a73192e09bc7fbc431803f2f24fe7a9f4d8ba237	no	11
Warnings:					
Information:					
18	Non Patent Literature	IPR2022-00062_Ex-2011.pdf	505512 3bb0ceeec756b2e30faffe9aa90e2de5ec44abb5	no	4
Warnings:					
Information:					
19	Non Patent Literature	IPR2022-00062_Ex-2012.pdf	614959 35f7d088bbd0a8c52ff6b31a3c46f6a838db256f	no	6
Warnings:					
Information:					
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Information:					

21	Fee Worksheet (SB06)	fee-info.pdf	38101 646a9b512da34467fef6dfcff61b821e14847fe5	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	16799325

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	LEE, Hyun	Confirmation No.:	8269
Serial No.:	16/680,060	Group Art Unit:	2133
Filed:	November 11, 2019	Examiner:	MARDOCHEE, Chery
For:	*MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES*	Attorney Docket No.:	NL066-13US01

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☒ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☐ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

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Ex. 1002, p. 420

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

3d. ☐ The $120 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☒ The Certification Statement in Item 5 below is applicable.

4b. ☒ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

4d. ☐ The $120 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

5. ☒ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

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Ex. 1002, p. 421

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☒ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial Nos. _____, filed on _____, of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

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Ex. 1002, p. 422

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Deposit Account No. 60-3916 (order no. NL066-13US01).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: April 3, 2022

/Jamie J. Zheng/ 51,167

Jamie Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828

Samsung Electronics Co., Ltd.
Ex. 1002, p. 423

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed April 3, 2022	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
Sheet	1	of	2	Attorney Docket Number	129980-5066US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		8,054,664	2011-11-08	Harashima et al	
		8,402,208	2013-03-19	Berke	
		8,452,917	2013-05-28	Amer et al.	
		2005/0138267	2005-06-23	Bains et al.	
		2005/0138302	2005-06-23	Lusk et al.	
		2009/0103373	2009-04-23	Shau	
		2011/0007585	2011-01-13	Shan et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, PAPER 7, PATENT OWNERS PRELIMINARY RESPONSE, filed February 18, 2022
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, EXHIBIT 2001, Declaration of Robert J. Murphy, filed February 18, 2022
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, EXHIBIT 2019, Redline comparison of 2022IPR-00064 to IPR2020-01042, filed February 18, 2022
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, EXHIBIT 3001, Emails regarding Petitioner's request for authorization to file pre-institution replies, filed March 10, 2022
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, PAPER No. 11. Petitioner's Authorized Reply to Patent Owner's Preliminary Response, filed March 18, 2022
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, PAPER NO. 12, PATENT OWNERS AUTHORIZED SUR-REPLY IN SUPPORT OF ITS PRELIMINARY RESPONSE, filed March 25, 2022
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, PAPER No. 8, ORDER Conduct of the Proceeding 37 C.F.R. sec 42.5, issued March 11, 2022
		Inter Partes Review No. 2020-00064 of US Patent No.10474595, Paper No. 7, NETLIST, INC.S PATENT OWNERS PRELIMINARY RESPONSE, filed February 18, 2022

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed April 3, 2022	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
Sheet	2	of	2	Attorney Docket Number	129980-5066US01

		Inter Partes Review No. 2020-00064 of US Patent No.10474595, EXHIBIT 2001, Declaration of Robert J. Murphy, filed February 18, 2022
		Inter Partes Review No. 2020-00064 of US Patent No.10474595, EXHIBIT 2019, Redline comparison of 2022IPR-00064 to IPR2020-01042, filed February 18, 2022
		Inter Partes Review No. 2020-00064 of US Patent No.10474595, Paper No. 11, Petitioner's Authorized Reply to Patent Owner's Preliminary Response, filed March 18, 2022
		Inter Partes Review No. 2020-00064 of US Patent No.10474595, Paper No. 12, PATENT OWNERS AUTHORIZED SUR-REPLY IN SUPPORT OF ITS PRELIMINARY RESPONSE, filed March 25, 2022
		Inter Partes Review No. 2020-00062/64 of US Patent No. 9858218/10474595, EXHIBIT 2006, IT Solution Architects, Server Memory: RDIMM vs LRDIMM and When to Use Them (Aug. 16, 2017), https://medium.com/@ITsolutions/server-memory-rdimm-vslrdimm-and-when-to-use-them-a550f4b7cf39, filed February 18, 2022
		Inter Partes Review No. 2020-00062/64 of US Patent No. 9858218/10474595, EXHIBIT 2011, Excerpt of DRAM Circuit Design, Fundamental and HighSpeed Topics (2008), filed February 18, 2022
		Inter Partes Review No. 2020-00062/64 of US Patent No. 9858218/10474595, EXHIBIT 2012, Excerpt of Semiconductor Memories, A Handbook of Design, Manufacture, and Application Second Edition (1997), filed February 18, 2022
		Inter Partes Review No. 2020-00062/64 of US Patent No. 9858218/10474595, EXHIBIT, 2013, JEDEC, Member Online Services, https://www.jedec.org/service_members/, filed February 18, 2022
		Inter Partes Review No. 2020-00062/64 of US Patent No. 9858218/10474595, EXHIBIT 2016, Intel, Fully Buffered DIMM (FB-DIMM) Design Considerations (Feb 18, 2004), http://www.csit-sun.pub.ro/~cpop/Documentatie_SMP/Intel_Microprocessor_Systems/PC_Memory/OSA-S009.pdf, filed February 18, 2022
		Inter Partes Review No. 2020-00062/64 of US Patent No. 9858218/10474595, Microway, DDR4 RDIMM and LRDIMM Performance Comparison (July 10, 2015), https://www.microway.com/hpctech-tips/ddr4-rdimm-lrdimm-performance-comparison/, filed February 18, 2022

Examiner Signature		Date Considered	

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				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
Sheet	1	of	1	Attorney Docket Number	129980-5066US01

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FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, PAPER 14, "DECISION - Granting Institution of Inter Partes Review," issued May 16, 2022
		Inter Partes Review No. 2020-00064 of US Patent No.10474595, PAPER 14, "DECISION - Granting Institution of Inter Partes Review," issued May 16, 2022

Examiner Signature		Date Considered	

Electronic Patent Application Fee Transmittal

Application Number:	16680060
Filing Date:	11-Nov-2019
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NL066-13US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
		Total in USD ($)		**260**

Electronic Acknowledgement Receipt

EFS ID:	45770814
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NL066-13US01
Receipt Date:	20-MAY-2022
Filing Date:	11-NOV-2019
Time Stamp:	22:06:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$260
RAM confirmation Number	E20225JM07074486
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	IPR2020-00062_Institution_Decision.pdf	671146 e359e4dccb0298675b3b591d90992ac195b3f01d	no	58
Warnings:					
Information:					
2	Non Patent Literature	IPR2020-00064_Institution_Decision.pdf	637753 3bcfeff76b03fe77c47b1572cdf49c1946652aed	no	56
Warnings:					
Information:					
3	Transmittal Letter	NL066-12US01_IDS_Transmittal_2022-05-20.pdf	118999 496d82881c3f2218a36a993a626bf604d3bc13d7	no	4
Warnings:					
Information:					
4	Information Disclosure Statement (IDS) Form (SB08)	NL066-12US01_IDS_List_2022-05-20.pdf	179459 764bf5bb00a7dfc3a819f3c740b61fbf5e38ce7c	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
5	Fee Worksheet (SB06)	fee-info.pdf	38101 c692992444d8d8fd8c95b654e1ed39b14feddece	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1645458		

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	LEE, Hyun	Confirmation No.:	8269
Serial No.:	16/680,060	Group Art Unit:	2133
Filed:	November 11, 2019	Examiner:	MARDOCHEE, Chery
For:	*MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES*	Attorney Docket No.:	NL066-13US01

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

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1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☒ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☐ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English

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language abstracts of the non-English language publications.

2. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

3d. ☐ The $120 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☒ The Certification Statement in Item 5 below is applicable.

4b. ☒ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916

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(order no. NL066-13US01).

4d. ☐ The $120 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

5. ☒ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☒ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☐ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial Nos. _____, filed on _____, of which this application claims

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priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Deposit Account No. 60-3916 (order no. NL066-13US01).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: May 20, 2022

/Jamie J. Zheng/ 51,167

Jamie Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828

Samsung Electronics Co., Ltd.
Ex. 1002, p. 435

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 02/23/2022
USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/680,060	11/11/2019	Hyun Lee	NL066-13US01	8269

TITLE OF INVENTION: MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	05/23/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHERY, MARDOCHEE	2133	711-154000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 **USCH Law, PC**
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: **Netlist, Inc.**

(B) RESIDENCE: (CITY and STATE OR COUNTRY): **Irvine, CA**

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ☒ Corporation or other private group entity ❑ Government

4a. Fees submitted: ☒ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. **60-3916**

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature **/Jamie J. Zheng/** Date **May 23, 2022**

Typed or printed name **Jamie J. Zheng** Registration No. **51167**

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 02/23/2022

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER
CHERY, MARDOCHEE

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 02/23/2022

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/680,060	11/11/2019	Hyun Lee	NL066-13US01	8269

TITLE OF INVENTION: MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	05/23/2022

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

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Notice of Allowability	Application No. 16/680,060	Applicant(s) Lee, Hyun	
	Examiner MARDOCHEE CHERY	Art Unit 2133	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to reply filed 01/07/2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 2-21 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 1/7/22.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	2/12/21

Samsung Electronics Co., Ltd.
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Electronic Patent Application Fee Transmittal

Application Number:	16680060
Filing Date:	11-Nov-2019
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NL066-13US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1200**

Electronic Acknowledgement Receipt

EFS ID:	45772349
Application Number:	16680060
International Application Number:	
Confirmation Number:	8269
Title of Invention:	MEMORY MODULE HAVING AN OPEN-DRAIN OUTPUT FOR PARITY ERROR AND FOR TRAINING SEQUENCES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NL066-13US01
Receipt Date:	23-MAY-2022
Filing Date:	11-NOV-2019
Time Stamp:	01:56:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1200
RAM confirmation Number	E20225M257151758
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	NL066-13US01_Issue_Fee_2022-02-23.pdf	393152 80203f3c929759e0fb8d3f84ed140c1b93d4258e	no	3
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	37958 e130274efbe57478605b90dabac294681d42da3d	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	431110		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed May 20, 2022	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
Sheet	1	of	1	Attorney Docket Number	129980-5066US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review No. 2020-00062 of US Patent No. 9858218, PAPER 14, "DECISION - Granting Institution of Inter Partes Review," issued May 16, 2022
		Inter Partes Review No. 2020-00064 of US Patent No.10474595, PAPER 14, "DECISION - Granting Institution of Inter Partes Review," issued May 16, 2022

Examiner Signature	/MARDOCHEE CHERY/	Date Considered	06/07/2022

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed September 1, 2020	
				Application Number	16/680,060
				Filing Date	November 11, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2139
				Examiner Name	To be assigned
Sheet	1	of	8	Attorney Docket Number	129980-5066US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.[1]	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		3,414,781	12-03-1968	Dill	
		3,560,935	02-02-1971	Beers	
		4,672,570	06-09-1987	Benken	
		5,388,074	02-07-1995	Buckenmaier	
		5,438,536	08-01-1995	Salzman	
		5,511,152	04-23-1996	Lai et al.	
		5,450,576	09-12-1995	Kennedy	
		5,606,662	02-25-1997	Wisor	
		5,684,979	11-04-1997	Grimes	
		5,835,733	11-10-1998	Walsh, et al.	
		6,693,840 B2	02-17-2004	Shimada et al.	
		6,754,787 B2	06-22-2004	Miller, et al.	
Change(s) applied		6,763,437 B1	07-13-2004	Nguyen et al.	
to document,		6,886,109 B2	~~04-26-1997~~	Olarig et al. 04/2005	
/A.C./		7,024,518 B2	04-04-2006	Halbert et al.	
2/28/2022		7,065,688 B1	06-20-2006	Moyes et al.	
		7,093,115 B2	08-15-2006	Poisner et al.	
		7,155,579 B1	12-26-2006	Neils, et al.	
		7,221,699 B1	05-22-2007	Lindskog	
		7,266,633 B2	09-04-2007	James	
		7,489,163 B2	02-10-2009	Goodnow et al.	
		7,525,860 B2	04-28-2009	Hokenmaier	
		7,539,909 B2	05-26-2009	LeClerg et al.	
		7,568,130 B2	07-28-2009	Smith et al.	
		7,586,350 B2	09-08-2009	Chung et al.	
		7,647,467 B1	01-12-2010	Hutsell et al.	
		7,757,101 B2	01-13-2010	Nonaka, et al.	
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				Application Number	16/680,060
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				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	Chery, Mardochee
Sheet	1	of	2	Attorney Docket Number	129980-5066US01

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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

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