UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

Case IPR2025-00001
Patent 11,386,024 B2

DECLARATION OF DR. DONALD ALPERT REGARDING U.S. PATENT NO. 11,386,024

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Samsung Electronics Co., Ltd.
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I. INTRODUCTION

A. Engagement

1. I have been retained by counsel for Samsung Electronics Co., Ltd. ("Samsung") as an expert witness in the above-captioned proceeding. I have been asked to provide my opinion about the state of the art of the technology described in U.S. Patent No. 11,386,024 ("the 024 Patent") (EX1001) and on the patentability of the claims of this patent. The following is my written declaration on these topics.

B. Background and Qualifications

2. I am an independent consultant with Camelback Computer Architecture, LLC. My residence and place of business is at 7 Farm Road, Los Altos CA, 94024. I am over the age of eighteen, and I am a citizen of the United States.

3. I have over 45 years of academic and industrial experience in applying, designing, studying, teaching, and writing about microprocessors and computer systems. I received an Electrical Engineering Ph.D. degree in 1984 from Stanford University. I earlier received an Electrical Engineering B.S. degree from MIT in 1973 and an Electrical Engineering M.S. degree from Stanford University in 1978. I have taught classes in computer architecture at Stanford, Tel Aviv, and Arizona State Universities.

4. From 1976 to 1977, I worked at Burroughs Corporation, where I designed peripheral interface controllers, including those for serial data communications based on Intel 8080 microprocessor components. From 1980 to 1989, I was the lead architect for the design of three high-performance microprocessors at Zilog and National Semiconductor. Later, at Intel, I was the lead architect of the Pentium® Processor from 1989 to 1992 and of the 815 chipset from 1999 to 2000, both of which became the most widely used PC components of their time. The 815 chipset comprised two components: (1) a memory controller hub (MCH) that included a graphics controller and memory controller with interfaces to the CPU, 133 MHz SDRAM system memory modules, an optional, external graphics controller and (2) an I/O controller hub (ICH) that included various I/O controllers (e.g., network, hard drive, USB) for system peripheral devices. Additionally, I served as co-manager for the Itanium processor design from 1993-1997.

5. I am a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE), and served as the chair of the IEEE Technical Committee on Microprocessors and Microcomputers from 1999 to 2000. I was the keynote speaker at the first Cool Chips conference, dedicated to the study of low-power microprocessors and systems. I have given invited lectures at several universities, and published ten papers in various professional journals and conference

proceedings. My paper entitled "Architecture of the Pentium Processor," was selected as best paper in IEEE Micro for 1993. I am a named inventor on over 30 U.S. patents that pertain to microprocessors, computer systems, and related technology.

6. I have reviewed the 024 Patent, and I am familiar with the patent's subject matter, which is within the scope of my education and professional experience. Based at least on my background in academia, industry, and consulting, I am familiar with the issues and technology relating to processors, chipsets, memory, and peripheral devices for computer systems. I have personally analyzed, developed, and tested such computer components and systems. More specifically, the Pentium® Processor and 815 chipset for which I was the lead architect at Intel implemented various features for initializing, calibrating, and testing the memory system, which comprised cache memory, a memory controller, and standard SDRAM modules.

7. My Curriculum Vitae, including my publications and patents, is submitted herewith as EX1004.

C. Compensation and Prior Testimony

8. I am being compensated at a rate of $600.00 per hour for my study and testimony in this matter. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this investigation.

My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

9. I have previously submitted declarations in several IPR proceedings, including IPR2014-00970 and IPR2014-00971, IPR2015-00148, IPR2015-00191, IPR2016-01106, IPR2017-00548, IPR2018-00303, IPR2020-01042 and IPR2020-01044, IPR2021-01567, IPR2022-00062 and IPR2022-00064, and IPR2022-00236. Additionally, I have testified as an expert witness in Federal Court and the ITC, as summarized in Exhibit 1004 at 6-7.

D. Information Considered

10. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this report and those listed in the Exhibit List at the end of this declaration.

11. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions — including documents that may not yet have been provided to me.

12. My analysis of the materials produced in this investigation is ongoing and I will continue to review any new material as it is provided. This report represents only those opinions I have formed to date. I reserve the right to revise,

supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

II. LEGAL STANDARDS FOR PATENTABILITY

13. In expressing my opinions and considering the subject matter of the claims of the 024 Patent, I am relying upon certain basic legal principles that have been explained to me.

14. First, I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious in view of what was known before the invention was made.

15. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as "prior art" and generally includes patents and printed publications (e.g., books, journal publications, articles on websites, product manuals, etc.).

16. I understand that in this proceeding the Petitioner has the burden of proving that the claims of the 024 Patent are anticipated by or obvious in view of the prior art by a preponderance of the evidence. I understand that "a preponderance of the evidence" is evidence sufficient to show that a fact is more likely true than it is not.

17. I understand that in this proceeding the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art

in view of the patent and its file history. The claims after being construed in this manner are then to be compared to the information in the prior art.

18. I understand that in this proceeding the information that may be evaluated is limited to patents and printed publications. My analysis below compares the claims to patents and printed publications that are prior art to the claims.

19. I understand that there are two ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to "anticipate" the claim. Second, the prior art can be shown to have made the claim "obvious" to a person of ordinary skill in the art. In this declaration I focus on "obviousness." My understanding of the legal standard for "obviousness" is set forth below.

20. I understand that a claimed invention is not patentable if it would have been obvious to a person of ordinary skill in the field of the invention at the time the invention was made.

21. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)) as follows:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my evaluation of whether the claims of the 024 Patent would have been considered obvious as of the priority date of the patent.

23. I understand that to find a claim in a patent obvious, one must make certain findings regarding the claimed invention and the prior art. Specifically, I understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

24. In addition, I understand that the obviousness inquiry should not be done in hindsight, but must be done using the perspective of a person of ordinary skill in the relevant art as of the effective filing date of the patent claim.

25. I understand the objective factors indicating obviousness or non-obviousness may include the following: (1) commercial success of products covered by the patent claims; (2) a long-felt need for the invention; (3) failed attempts by others to make the invention; (4) copying of the invention by others in the field; (5) unexpected results achieved by the invention; (6) praise of the

invention by those in the field; (7) the taking of licenses under the patent by others; (8) expressions of surprise by experts and those skilled in the art at the making of the invention; and (9) the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this evidence must be specifically connected to the invention rather than being associated with the prior art or with marketing or other efforts to promote an invention. I am not presently aware of any evidence of "objective factors" suggesting the claims are not obvious, and I reserve my right to address any such evidence if it is identified in the future.

26. I understand the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market demands or design considerations may prompt variations of a prior art system or process, either in the same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art.

27. I also understand that if a person of ordinary skill can implement a predictable variation, that variation would have been considered obvious. I understand that for similar reasons, if a technique has been used to improve one device, and a Skilled Artisan would recognize that it would improve similar

devices in the same way, using that technique to improve the other device would have been obvious unless its actual application yields unexpected results or challenges in implementation.

28. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can take account of the "ordinary innovation" and experimentation that does no more than yield predictable results, which are inferences and creative steps that a Skilled Artisan would employ.

29. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

30. I understand that the obviousness analysis cannot be confined by a formalistic conception of the words "teaching, suggestion, and motivation." I understand that in 2007, the Supreme Court issued its decision in *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), where the Court rejected the previous requirement of a "teaching, suggestion, or motivation to combine" known elements of prior art for purposes of an obviousness analysis as a precondition for finding

obviousness. It is my understanding that *KSR* confirms that any motivation that would have been known to a person of skill in the art, including common sense, or any motivation derived from the nature of the problem to be solved, is sufficient to explain why references would have been combined.

31. I understand that a person of ordinary skill in the art attempting to solve a problem will not be led only to those elements of prior art designed to solve the same problem. I understand that under the *KSR* standard, steps suggested by common sense are important and should be considered. Common sense teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. As such, the prior art considered can be directed to any need or problem known in the field of endeavor as of the priority date of the patent and can provide a reason for combining the elements of the prior art in the manner claimed. In other words, the prior art does not need to be directed towards solving the same problem that is addressed in the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem.

32. I understand that obviousness does not require that the features of a secondary reference be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of those references

would have suggested to a Skilled Artisan. The disclosures of the prior art references need not be physically combinable. Combining the teachings of the references should be the focus of the analysis.

33. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or more prior art references discourages or lead away from the line of inquiry disclosed in the reference(s). A reference does not "teach away" from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (*e.g.*, because it would not work or explicit statements saying the combination should not be made).

34. I understand that a person of ordinary skill is also a person of ordinary creativity.

35. I further understand that in many fields, there may be little discussion of obvious techniques or combination, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive design trends. When there is such a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of

ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious. The fact that a particular combination of prior art elements was "obvious to try" may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than innovation.

III. RELEVANT INFORMATION CONCERNING THE CONTESTED PATENT

36. The 024 Patent "relates to the operation of memory modules. Specifically, … to a memory module having an open-drain output for parity error and for training sequences." EX1001, 1:20-25. As explained below in detail, memory modules and open-drain outputs were well known long before the 024 Patent.

A. Background Technology

1. JEDEC standards

37. The 024 Patent discloses that a "memory module performs memory operations including memory read/write operations according to an industry standard." EX1001, 1:54-56. "An example of a standard in accordance with certain embodiments described herein is one or more of the industry standard

promulgated by the Joint Electronic Devices Engineering Counsel (JEDEC)." *Id*., 8:46-57.

38. JEDEC was a well-known organization at the time of the 024 Patent for developing industry standards related to memory devices, including the JESD79 standard for DDR SDRAM devices (EX1024), the JESD209 standard for Low Power DDR SDRAM devices (EX1029), the JESD79-2B standard for DDR2 SDRAM devices (EX1084), and the JESD79-3C standard for DDR3 SDRAM devices (EX1056). These standards defined certain features and procedures for the memory devices, including initialization sequences for specifying how the memory devices would operate in a given memory system. *See, e.g.*, EX1024 (JESD79), 8-12; EX1029 (JESD209), 9-17; EX1084 (JESD79-2B), 9-20; EX1056 (JESD79-3C), 19-32. For example, these standards defined mode registers of the memory devices and a corresponding procedure to set operating parameters (e.g., burst length, latencies, etc.) in those mode registers. *Id*. To help setting the proper timing in the memory system as the speed of the memories increased, the DDR3 standard also defined a "write leveling" feature which provided feedback to a controller during initialization so that it can properly adjust the data strobe (DQS) and clock (CK) relationship for write operations. EX1056, pp.42-45. The DDR3 standard also had a multi-purpose register that may be used to provide a predefined bit sequence for timing calibration of read operations. *Id*., pp.48-54.

39. JEDEC also developed industry standards related to memory modules that include one or more standardized memory devices and optional buffer devices to interface with a system memory controller. For example, the JEDEC 21-C standard described the architecture and protocol for a Registered DIMM (RDIMM standard, EX1083), the JESD206 standard described the architecture and protocol for fully buffered DIMMs (FBDIMM standard, EX1025), and the JESD82-20A standard described an Advanced Memory Buffer (AMB) for FBDIMMs (EX1026). In the FBDIMM, the AMB buffers address, control, and data signals between the system controller and the memory devices. EX1025, p.5. The FBDIMM standards also specify initialization procedures that include training, testing, and polling states of the AMB. EX1025, pp.15-54. The FBDIMM standard further discloses a "Hot Add Sequence" during which "the host may interrupt the system firmware indicating that the FBD channel is now up or wait for the system firmware to poll its status register." *Id.*, p.114 (step e). Thus, the FBDIMM standard teaches, as it was well known at the time, that indicating the completion of initialization or similar tasks is not limited to polling and, where available, an interrupt signal can also be used.

40. According to the FBDIMM standards, the AMB can perform calibration of the DDR memory devices, including DRAM power-up initialization, mode register setting, and DDR bus calibration. EX1026, pp.23-25. After a mode

register setting command, for example, the AMB can be polled to see if it "has completed the selected operation." *Id.*, p.24. The "DDR bus calibration functions … must be executed before read data can be captured reliably. These functions issue a series of write and read transactions on the DRAM bus, analyze the read data captured, and program a set of calibration results configuration registers. During subsequent operations, these configuration registers control the DDR I/O circuits and ensure proper data capture." *Id.*, p.24. For example, the "Advanced Memory Buffer automatically finds the end of the preamble of each of the 18 DQS pairs on the DDR bus … and stores this information for use during read transaction," and a "DQS delay calibration adjusts the Advanced Memory Buffer's on-chip delay circuits that align DQS signals to the center of their associated DQ/CB data eyes at the capture flops in the DDR I/O cluster." *Id.*, p.25. Furthermore, the "AMB supports memory self test for memory initialization during system boot up." *Id.*

41. In 2009, JEDEC was developing a standard for DDR3 LRDIMMs. *See, e.g.*, EX1036 (JEDEC committee proposal for DDR3 LRDIMM Design Specification); EX1039 (Inphi's JEDEC proposal for the Memory Buffer (MB) initialization sequence, including MB-DRAM interface training and Host-MB training); EX1015 (JEDEC committee proposal for LRDIMM DDR3 Memory Initialization). A Skilled Artisan would have known about the development of the

DDR3 LRDIMM standard and the content of JEDEC proposals by different companies at the time, including those related to the initialization of the Load Reduced DIMM. EX1008, p.22 (the provisional describing "the recent proposal in JEDEC for … Load Reduced DIMM… the LR-DIMM proposal requires … the current LR-DIMM proposal"). I understand that Netlist's expert "agree[d] that a POSITA would have understood certain steps and requirements of LR-DIMM initialization, as they existed at the time of the Provisional." EX1078, pp.25-26; EX1105 (EX2027 in IPR2022-00062), ¶¶32-33; EX1106 (EX2027 in IPR2022-00064), ¶¶40-41.

2. Shared pins

42. By the effective filing date of the 024 Patent, a Skilled Artisan would have known that it was common to design the pins of a memory device and, accordingly in a memory module, such that a single pin is shared for various types of signals for different purposes due to the limited number of pins. A Skilled Artisan would have also understood, e.g., from Prof. Jacob's textbook, that DRAMs had a small number of input/output (I/O) pins because, initially, their manufacturing cost was dominated by the number of I/O pins. EX1070 (Jacob), p.322. "This desire to limit I/O pins has had a long-term effect on DRAM architecture; the address pins for most DRAMs are still multiplexed, meaning that two different portions of a data address[, i.e., row and column address] are sent

over the same pins at different times, as opposed to using more address pins and sending the entire address at once." *Id*.; *see also* EX1024 (DDR standard), p.7 (A0-A11 Address Inputs to carry row address for Activate command and column address for Read and Write commands). Similarly, the A10 address line, which was not used for column address (*id*., p.3, Address Assignment Table showing column address using only A0-A9), was used to convey auto-precharge commands (*id.* p.7, address line A10 also used for auto-precharge command). The address lines were also used to convey mode register settings. *Id*., pp.7-8. The later versions of the DDR standard kept sharing pins by multiple functions. *See, e.g.*, EX1056 (DDR3 standard), p.33 (Command Truth Table, below, showing the address lines carrying both row and column address, mode register setting, A10 still carrying auto-precharge commands, A12 carrying on-the-fly burst length command, and A13-A15 marked as reserved for future use (RFU) when not carrying row address); EX1084 (DDR2 standard), pp.46-47 (similar).

Table 6 — Command Truth Table

Function	Abbreviation	CKE		CS#	RAS#	CAS#	WE#	BA0-BA2	A13-A15	A12-BC#	A10-AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9, 12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

43. Professor Jacob also explains that pin cost remained a major concern. EX1070, p.351 ("The obvious conclusion is that in the future, DRAM design will be far more concerned about pin count than transistor count."). Thus, a Skilled Artisan would have understood at the time the benefits of sharing the same pin by multiple functions. Indeed, JEDEC standards often added functions by sharing existing pins. For example, JEDEC eight-bit wide (x8) DDR3 memories could be programmed to use their data mask (DM) pin as operating either as a data mask

(DM) or a termination data strobe (TDQS). EX1056 (DDR3 standard), pp. 13-14; *see also* EX1084 (DDR2 standard), p.6 (similar). Similarly, JEDEC Advanced Memory Buffer (AMB) could also use some pins either as a data mask or as a data strobe, depending on the configuration implemented on the memory module. EX1026 (JESD82-20A), pp.18-19 ("Data mask is supported for non-ECC (64-bit) DIMMs only. …The data mask signals share pins with the DQS[16:9] pins. ... The following table shows the mapping between DQS pins and data mask pins.").

44. Similarly, a Skilled Artisan would have understood at the time that a parity-error pin which reports parity error in command/address signals can also be used for other functions. EX1017 (Kim) at FIG. 5 (showing that the pins related to the open drain transistor (on the right) is shared between the "parity check" circuitry and the "CRC check" circuitry (on the left)).

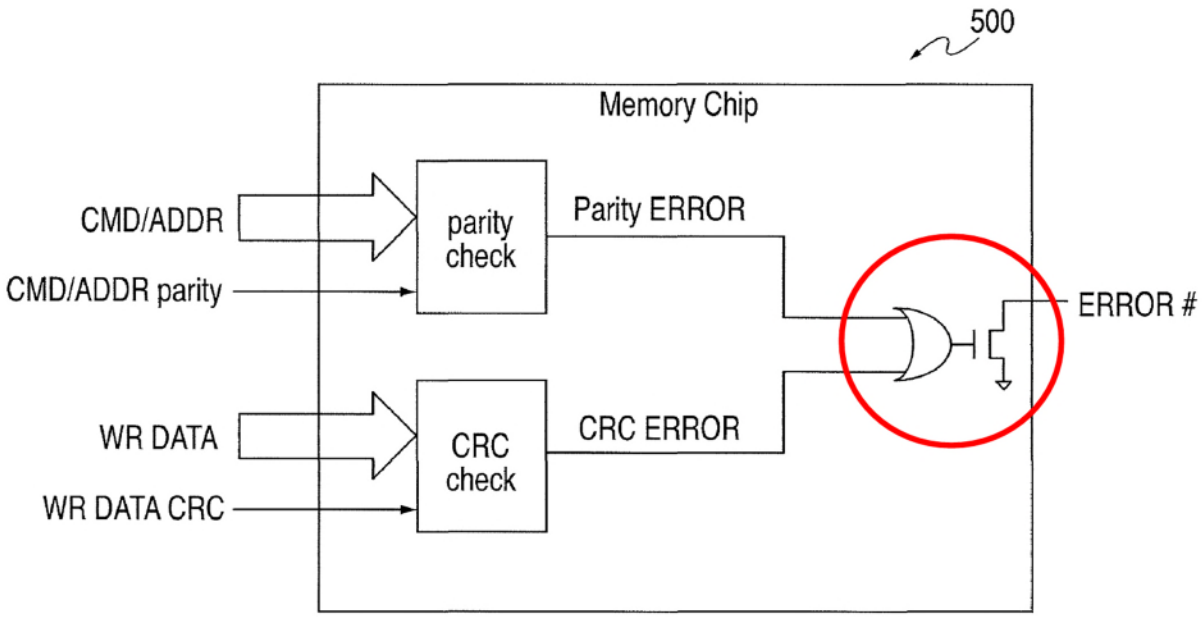


FIG. 5

Kim explains that its "pin... for reporting CRC errors ... could also be merged with an existing error pin available on many industry standard modules for the reporting of address/command errors." EX1017 (Kim) at 5:49-55; *see also id.*, 6:13-18 ("In alternate exemplary embodiments, other functions also share the error feedback pin (e.g., parity or CRC error(s) on command and address information).").

45. A Skilled Artisan also knew that it was customary to use a logic OR circuit as shown in FIG. 5 of Kim, or a similar logic circuit, to couple the signals corresponding to the different functions to the shared pin. *See, e.g.*, EX1017 (Kim) at FIG. 5 (showing a logic OR circuit coupled to the gate of the open drain transistor), 6:13-16 ("FIG. 5 is a block diagram of a memory device 500 that shares an error feedback pin between data CRC and address parity in accordance with an

exemplary embodiment of the present invention."); *see also* EX1023, US 20080155378 (Amidi) at ¶[0018] ("An output device 120 functioning as a logic OR ties the output ends of the error detection module 158 and the transmission memory 156 together such that the error detection module 158 and the transmission memory 156 share the output terminal error-out 168 to transmit signals to the memory controller 110. The output device 120 can be implemented as an OR gate, a wired-OR gate, an open collector, or other device functioning as a logic OR."); *see also id*., FIG. 2 (showing that the "error out" signal is output from a "logic OR" element).

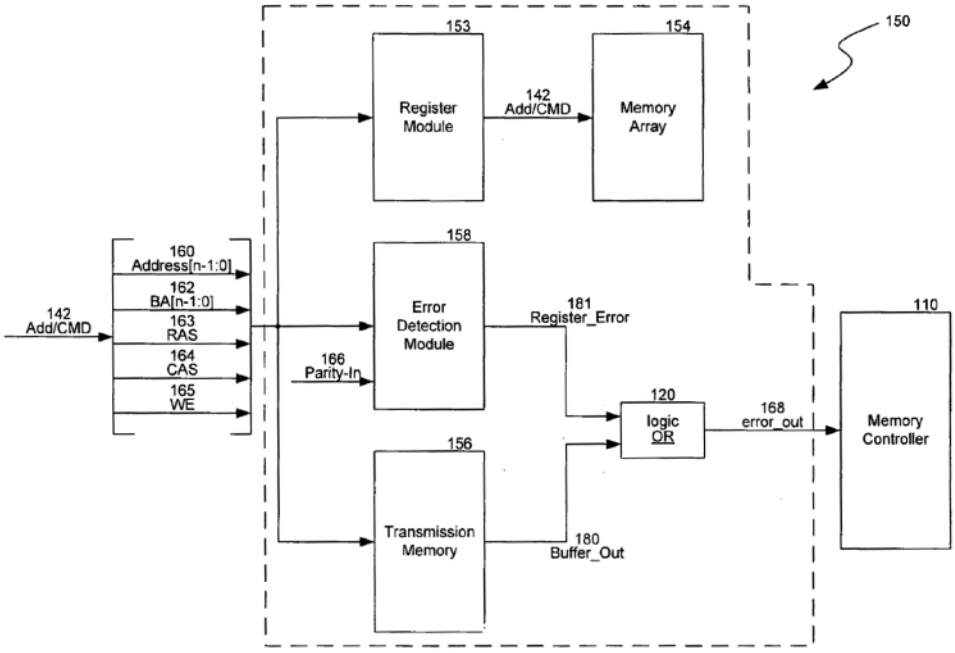


FIG. 2

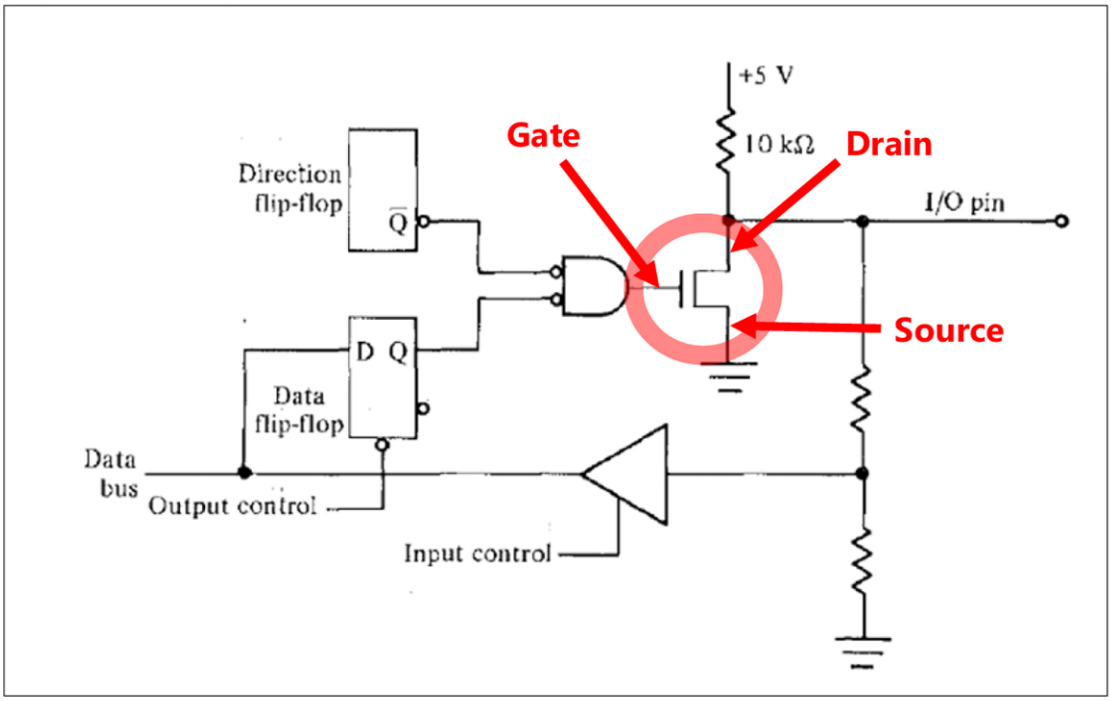
3. Open-drain output

46. An open-drain output is an example of the general concept commonly known as an "open-circuit output." EX1088 (JESD99A.01),[1] 50-51. For example, an output connected to the collector of a bipolar transistor whose emitter is connected to ground is called an open-collector output. *Id*. Similarly, an output connected to the drain of a field-effect transistor whose source is connected to ground is called an open-drain output. *Id*. In both cases, when the transistor is in its "on" state, corresponding to a low impedance (conductive) path through the transistor, the output voltage is driven to ground by the turned-on transistor; when the transistor is in its "off" state, corresponding to a high impedance (non-conductive) path through the transistor, the output voltage is determined by other circuitry coupled to the output. *Id*., 50.

47. The concepts of open-collector and open-drain output were known for decades and explained to students in textbooks, such as Prof. Stone's Microcomputer Interfacing from 1982. *See*, *e.g.*, EX1089, pp.207-208. For

[1] JESD99A.01 (EX1088) is the JEDEC Standard for "Terms, Definitions, and Letter Symbols for Microelectronic Devices (May 2003). *See* EX1086, 41, 64, 110, 111 (JEDEC Catalogue as of July 27, 2004); EX1087 (download page for JESD99A.01 as of November 26, 2003).

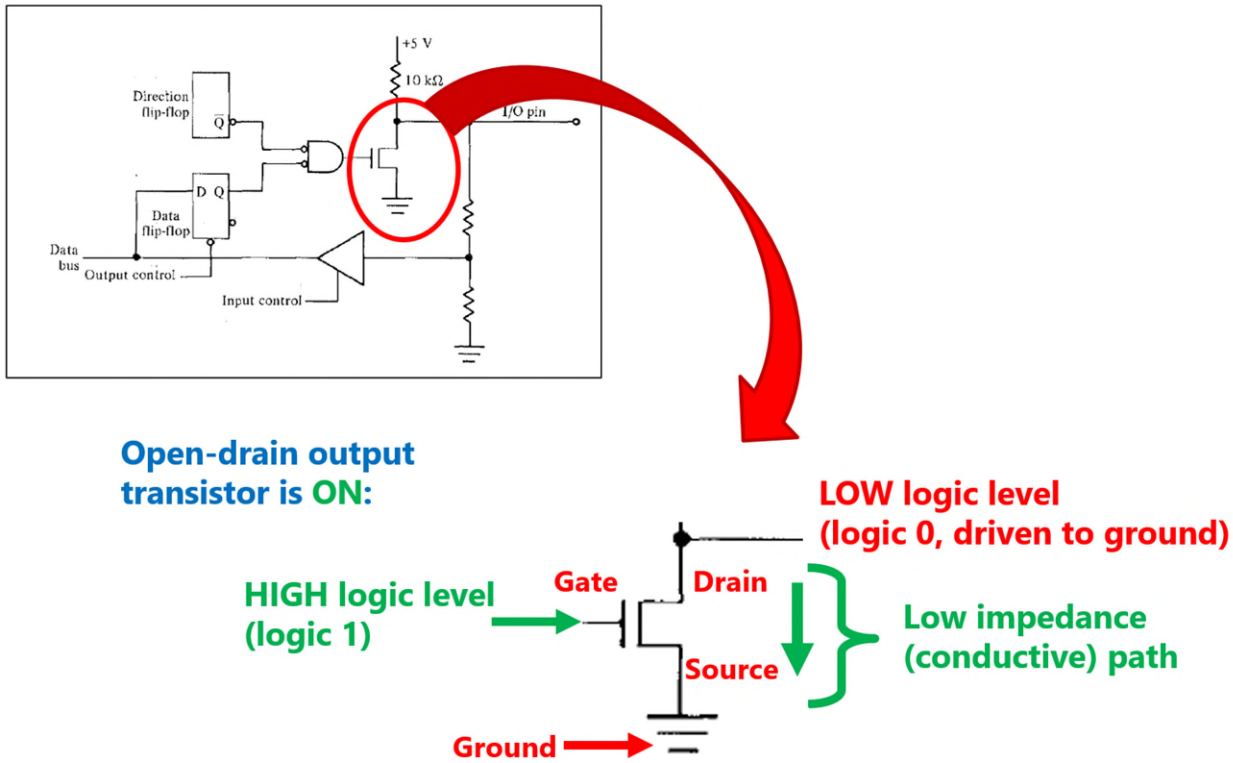
example, Fig. 6.2 of Professor Stone's textbook (reproduced below, annotated) shows "an open-drain circuit of a field effect transistor" (in red circle) in "an electrical model of one open-collector circuit." *Id.*



Here, the output (I/O pin) is connected to the drain of the field-effect transistor (in the red circle), thus it is an open-drain output. EX1088, p.50 ("Outputs of this generic class [(open-circuit output)] are usually classified according to the name of the element [(here: drain)] of the active device [(here: transistor)] to which they are connected…, e.g., … open-drain output.").

48. Professor Stone explains that the open-drain output (labeled I/O pin in Figure 6.2) has two states, depending on the voltage applied to the gate of the field-effect transistor. EX1089, pp.207-208. When the transistor is turned "on," the

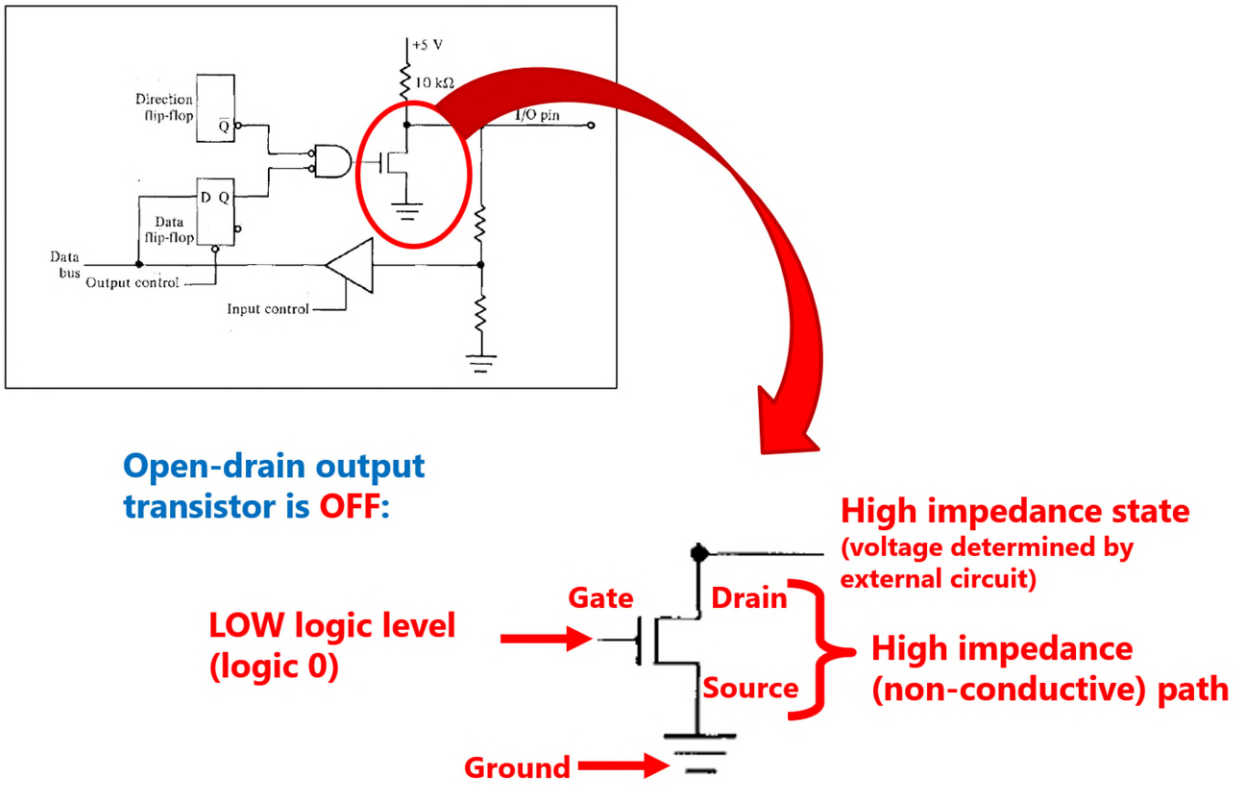
output (I/O pin) is driven close to ground, outputting a low logic level, as illustrated below:



Here, the transistor is in an "on" state because its gate receives a "high" voltage representing a logic 1 so that "the transistor conducts and there is a low impedance path from the I/O pin to ground through the transistor." *Id*. That low impedance path through the turned-on transistor between the output (I/O pin) and the ground drives the output voltage on the I/O pin to approach ground, corresponding to a "low" logic level that represents a logic 0. EX1088, p.50 ("When the active device [(here: the transistor)] is in its on state, the output voltage approaches the voltage

of the supply [(here: ground)] to which it is connected (through the active device).")

49. When the transistor is turned "off," the output (I/O pin) is in a high impedance state and the output voltage is determined by external circuitry as illustrated below:



Professor Stone explains that the transistor is in this "off" state when "the transistor gate-voltage drops below threshold to logic 0, the transistor opens[, i.e., becomes off and non-conductive]. Now the path from the I/O pin to ground is open [i.e., non-conductive]." EX1089, pp.207-208. That is, the path through the turned-off transistor has such a high impedance that it can be considered non-conducting for

any practical purposes. EX1088, p.50 ("when the device [(here: the transistor)] is in its off state, the output impedance to any other terminal … is high"). In this high impedance state of the I/O pin, "the output voltage is determined by the external circuit to which the output is connected." *Id*. In other words, this one transistor being turned off, by itself, does not determine the voltage at the output. That is because the output is typically connected to other circuit elements (within or outside of the IC and/or the module), such as one or more pull-up resistors and one or more other open-drain transistors, so that the output voltage can be either high or low, depending on these other circuit elements. *See, e.g.*, EX1017 (Kim) at FIG. 4 (reproduced below). In the example of Professor Stone's Figure 6.2 (above), "provided that no other open-collector output attached to the same pin is also active," then "the I/O pin is pulled high to 5 V by the 10 kΩ resistor." EX1089, pp.207-208.

50. By the effective filing date of the 024 Patent, a Skilled Artisan would have understood that it was common to use an "open drain output" in a memory module to send signals, such as error signals, from the memory modules to the host memory controller. *See, e.g.*, EX1017 (Kim) at FIG. 4 (reproduced below), 4:40-48 ("a single pin is used, dotted via an open drain or related method across memory devices in a memory subsystem, to report write data errors"); 6:1-16 (similar); EX1014 (Hazelzet) at ¶¶[0072] ("Two open-drain outputs are available

to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command…"), [0109] (similar).

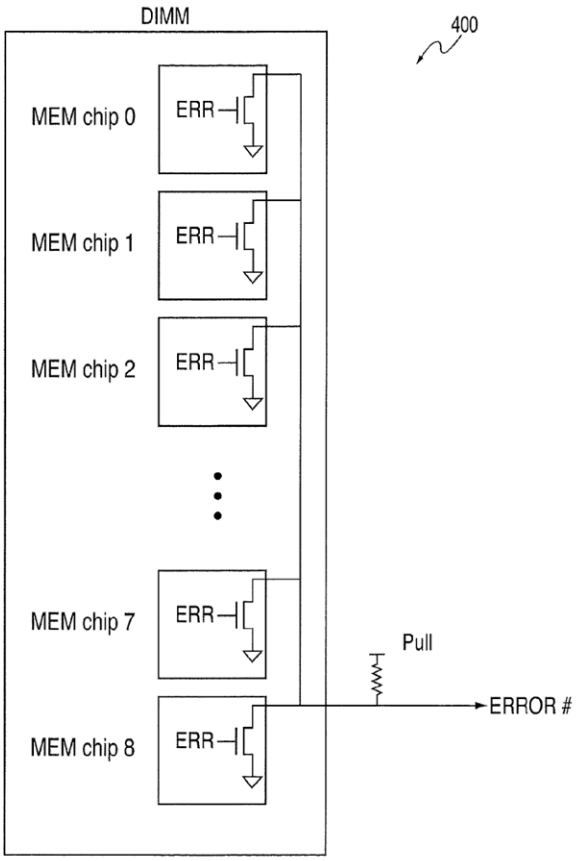


FIG. 4

51. In Kim's Fig. 4 example, each memory chip has an output pin coupled to the drain of a field-effect transistor, which includes three ports (i.e., a gate, source, and a drain). *See, e.g.*, EX1017 (Kim) at FIG. 4 (reproduced above). Kim shows that the open drain outputs of the memory chips are connected together and coupled to a pull-up resistor (i.e., connected to a high voltage via a resistor). FIG. 4 of Kim also shows that the source of each transistor is coupled to ground.

Because the source of the transistor is coupled to ground (as opposed to Vdd), a positive voltage at the gate (i.e., a high value of the "ERR" signal in FIG. 4 of Kim) would turn on the transistor, creating a low impedance path between ground and the output. Based on this bias condition, a Skilled Artisan would have understood that Kim's transistor is an NMOS (i.e., n-channel Metal Oxide Semiconductor) transistor, as opposed to a PMOS (i.e., p-channel Metal Oxide Semiconductor). *See, e.g.*, EX1017 (Kim) at FIG. 4. This is also clear from the symbol. A PMOS transistor would use a symbol with a bubble at the gate. *Id*. Thus, a Skilled Artisan would have understood that, when *any* of the transistors in Kim's Fig. 4 is "on," i.e., has a low impedance path through the transistor, the output ERROR# would be pulled closer to ground by that low impedance path, corresponding to a "low" logic level that represents a logic 0.

52. A Skilled Artisan would have also understood that, when the gates of all the transistors are low, thus all the transistors are "off," i.e., in a high impedance state, the common output ("ERROR#" in FIG. 4 of Kim) would also be in a high impedance state and its voltage would be pulled to a high logic level (i.e., to the supply voltage connected to the resistor) through the resistor. EX1017 (Kim) at FIG. 4. In other words, when the open-drain output of each memory is in a high-impedance state, then the voltage on the common output is determined by an external circuit, such as a high voltage through the pull-up resistor. *Id*.; *see also*

EX1014 (Hazelzet) at ¶[0099]. On the other hand, if any of the transistors is turned on because the gate of the corresponding transistor is high, the open drain outputs would switch to a low level because the low impedance path of the turned-on transistor would drive its output to a low logic level (e.g., close to ground). *Id.* Once the output is driven low by any of the transistors, turning on other transistors would not change the low logic level of the output, thereby implementing an OR function. I understand that Netlist's expert has agreed that this was known for decades. *See* EX1077, pp.178:21-179:4 ("Q. In your opinion would a person of ordinary skill in the art have known that an open drain output in combination with a pull-up or pull-down resistor would result in a wired-or function? . . . THE WITNESS: Yes. One of ordinary skill in the art would have known this. It's probably 40 years old.").

53. A Skilled Artisan would have understood that this OR functionality of an open-drain or open-collector output is particularly useful in certain situations. Professor Stone explains that "[m]any designers use open-collectors for signals asserted in the low state, in which case the open-collector performs an OR function of the active low signals. … For example, an interrupt request signal is often implemented as an active low signal … [so that it] is low if any device asserts its active low output." EX1089, p.208. Professor Stone further explains that such an interrupt request signal can be used "for detecting when an I/O port has completed

an operation. … For interrupt-driven I/O, the port generates a signal to the processor, called an *interrupt request*, at the completion of an operation … Thus there is no need to interrogate the port to find if the port is ready. The interrupt request conveys the ready information." EX1089, pp.15-16. For example, the IEEE-488 bus uses an "open-collector bus to perform an OR function when two or more signals are asserted simultaneously." *Id*., pp.218-219. In the IEEE-488 bus, a line called "NOT READY FOR DATA" (NRFD) "is an open-collector control line so that NRFD rises only when all slaves are ready." *Id*. p.220. As another example, "[s]ome disk systems take advantage of the open-collector drivers to do 'wired-Or' logic of status signals from multiple drives." *Id*., p.281.

54. In short, a Skilled Artisan would have been very familiar with open-drain and open-collector outputs and their use for signaling status of a device, such as completion of an operation or being ready, thereby avoiding the need for the system controller to interrogate the device about its status.

B. Person of Ordinary Skill in the Art ("POSITA" or "Skilled Artisan")

55. Based on my experience and the prior art I discuss herein, I believe a person of ordinary skill in the art in the field of the 024 Patent would be someone who was familiar with computer memory systems and basic CPU architecture documented in the computer/memory architecture literature and generally available in commercial systems as of 2009-10. Such literature and commercial systems

would have included techniques related to how computer components access a computer's memory, including the role of a memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory devices to the other components of the computer system. They would also include schemes for initialization of computer systems, including initialization/training of memory components. Such a person would also have been familiar with the standards that govern the operation of memory devices. The person of ordinary skill in the art would have had a bachelor's degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems. Alternatively, such a person could have had equivalent combinations with more or less education and less or more experience. EX1102, 11-12; EX1103, 11-12; EX1034, 8-9.

C. The 024 Patent

1. Overview of the 024 Patent

56. The 024 Patent states that it describes "a method of establishing a handshake mechanism based on notification signaling." EX1001 (024 Patent) at 4:48-50. The 024 Patent discloses that "this [handshake] mechanism can be implemented by adding a new interface (notifying) signal between the MCH [i.e., system memory controller] and the memory subsystem controller, or by adding an additional functionality to an existing, non-timing critical signal without altering

the memory subsystem hardware." EX1001 (024 Patent) at 4:50-55. The 024 Patent further discloses that this interface "can be an open drain signaling from the memory subsystem controller to the MCH [system memory controller]." EX1001 (024 Patent) at 4:55-59.

57. According to the 024 Patent, before the patent "[i]n general, there [was] *no existing method of handshaking* between the MCH (e.g., system memory controller) and a memory subsystem (e.g., memory module) during initialization." EX1001 (024 Patent) at 3:40-43 (emphasis added). "For example, in conventional systems, the system memory controller does not monitor the error-out signal from the memory subsystem." *Id*., 3:43-45. The 024 Patent states that the MCH in "typical" servers of the prior art would have "complete control over the initialization procedure" so the lack of handshaking "has not been a serious issue." Id., 3:46-51. For the LR-DIMM (Load Reduced DIMM), however, the MCH hands over parts of the initialization operations to a memory module, and simply waits a predetermined amount of time, assuming that the memory module had completed those initialization operations. EX1001 (024 Patent) at 3:51-62. In particular, the provisional application, incorporated by reference in its entirety into the 024 Patent, EX1001, 1:15-18, admits that a prior art "LR-DIMM proposal [in JEDEC] requires the MCH to insert a waiting period." EX1008, 22.

58. The 024 Patent suggests that use of "handshaking" between memory controller and memory module (i.e., exchanging information about the completion of the initialization procedure) would be a better idea. EX1001 (024 Patent) at 3:34-43. It states that, generally, "handshaking can be implemented in at least two ways; polling and notifying." EX1001 (024 Patent) at 4:18-19. The 024 Patent claims that polling is "generally inefficient because the system memory controller does not know exactly when the memory subsystem will have completed the required or requested operation," thus causing the controller to "wait longer than necessary to poll the memory subsystem, thereby delaying the overall initialization process." EX1001 (024 Patent) at 4:24-30. It further states that "the notifying method is an advantageous handshaking method between the MCH and the memory subsystem controller." EX1001 (024 Patent) at 4:39-41.

59. Figure 3 of the 024 Patent illustrates an exemplary memory module 10 with a notification circuit 20 whose output 12 is coupled to an error-pin of the memory module, and a multiplexor 42 drives the transistor 36 with either of a task_in_progress signal 44 or an error signal 46 (e.g., parity error signal). EX1001, Fig. 3, 11:57-65. "Thus, the memory module 10 can be advantageously configured to both perform the standard (e.g., JEDEC-specified) error reporting functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode." *Id*. 12:4-9.

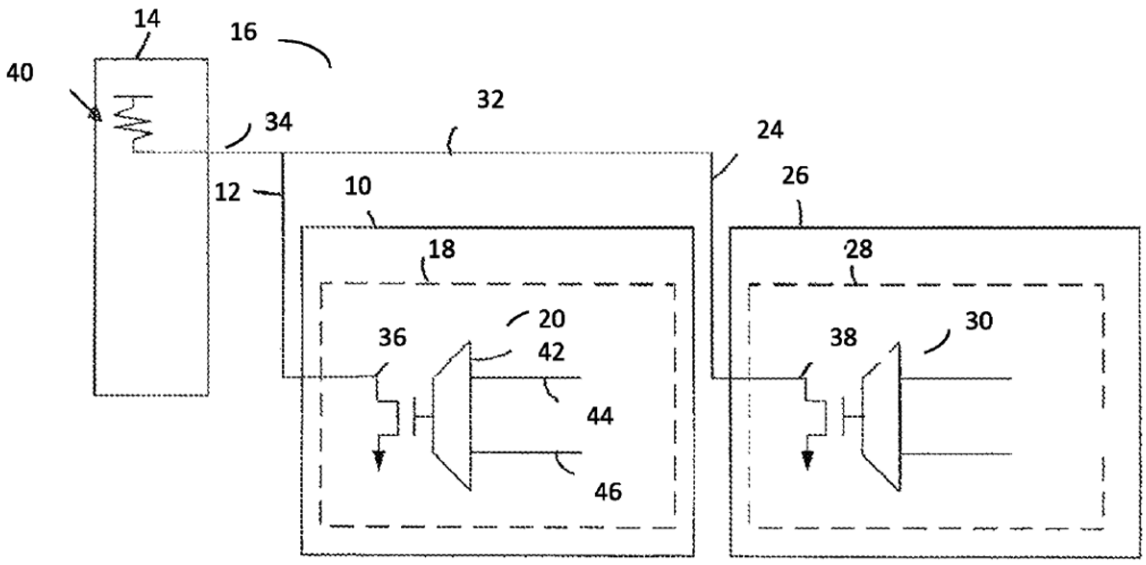


Figure 3

2. Effective filing date of the 024 Patent: No earlier than June 14, 2010

60. The 024 Patent is a continuation of various applications including a utility application filed June 14, 2010, and also claims priority to U.S. Provisional Application No. 61/186,799 (EX1008, "the provisional" or "the provisional application"), filed June 12, 2009. EX1001, pp.1-2. I have been asked to give my opinion as to whether, from the perspective of a Skilled Artisan, the provisional application shows that the inventor actually invented what is claimed in each of the claims of the 024 Patent, and possessed the claimed subject matter, as of the provisional's filing date. When considering that question, I have considered whether the provisional explicitly or inherently discloses the elements of the claims. To determine whether the provisional inherently discloses an element, I

considered whether any element not explicitly disclosed would be necessarily comprehended in the description provided by a Skilled Artisan. I conclude that certain elements of the claims are not adequately disclosed in the provisional. I understand that in IPR2020-01042 and -01044, and IPR2022-00062 and -00064, the Board's Institution Decisions agreed that limitations similar to those discussed below are not adequately disclosed in the provisional. EX1059, 21-27; EX1062, 21-31; EX1108, 18-25; EX1109, 16-24. As such, the Board agreed that the challenged claims were not adequately disclosed in the provisional, and as such, those claims were not entitled to the provisional filing date. *Id.* I understand that the Board also noted that the petition in these IPRs successfully showed that the JEDEC proposal qualified as prior art. *Id.*

a) **Negative limitation in independent claims 1, 10, and 19: *"when the dynamic random access memory elements are not accessed for any normal memory read or write operations"***

61. Independent claims 1, 10, and 19 (i.e., all of the independent claims) of the 024 Patent recite the negative limitation of "*when the dynamic random access memory elements are* ***not accessed*** *for any normal memory read or write operations.*" EX1001, 15:46-49 (claim 1), 16:55-57 (claim 10), 18:16-19 (claim 19). The provisional application provides no support for this negative limitation. *See* EX1008.

62. The provisional application does not mention any "*normal memory read or write operations*." EX1008. Actually, the provisional does not mention any "*write operations*" at all. EX1008. The provisional mentions a read operation only when "the MCH [(i.e., Memory Controller Hub)] reads a status register in the memory subsystem controller." EX1008, 22. According to the provisional, "since the standard DDR2/3 specification does not provide a way ***to read any registers*** in the memory subsystem controller, this ***is not an implementable method***." *Id*. As the provisional took the position that status register read operations cannot be implemented, they cannot provide support for a "*normal memory read*" in the 024 claims. Since the provisional lacks any disclosure about "*normal memory read or write operations*," it cannot support the limitation of "*when the dynamic random access memory elements are not accessed for any normal memory read or write operations*."

63. The provisional mentions "normal operation." EX1008, 24-25. I understand that Patent Owner's expert took the position in the past that "*normal* memory read or write operations" refer *only* to memory read or write operations that occur *during* the "operational mode" or "normal mode." *See* EX1106 (EX2027 in IPR2022-00064), ¶¶27-29. According to this interpretation, the disclosure of "normal operation" alone discloses that no "normal memory read or write operations" happen outside of such "normal mode." *Id*., ¶¶35-37. I disagree

with this circular logic. Indeed, even Patent Owner's expert admitted under cross examination with respect to a parent of the 024 Patent that, "in some cases computer designers … can actually do *initialization sequences and normal operations…at the same time*, and that *is well known* in the industry." EX1021, 17:15-19.

64. A Skilled Artisan would have understood that the plain and ordinary meaning of "*normal memory read or write operations*" refers to the standard (or "normal") memory read or write operations when the memory is written and read in the "normal way" which, in the case of DDR SDRAMs, includes providing an Activate command (with row address) and subsequently a Write or Read command (with column address) to write data to or read data from the addressed part of the memory. *See, e.g.*, EX1056 (JESD79-3C), pp.33, 55-76. Such standard read or write operations can be performed independent of what "mode" the system or the memory module is in. Thus, a Skilled Artisan would have understood that "*normal memory read or write operations*" can be performed not only during an operational mode, but also in other modes, e.g., during initialization. As the 024 Patent itself explains, "the system memory controller 14 may cause the memory module 10 to perform standard operations such as ***memory read/write***, pre-charge, refresh, etc., ***while in operational mode***, although it will be appreciated that one or more of

these operations can also be performed by the memory module 10 ***while in initialization mode*** in certain embodiments." EX1001, 7:21-32.

65. The contemporaneous LRDIMM DDR3 Memory Initialization Chapter Proposal in JEDEC confirms that "*normal memory read or write operations*" can also be performed for training purposes, such as DQ/DQS margining: "host performs ***normal writes*** to DRAM for write DQ/DQS margining, … [and] read DQ/DQS margining by using ***normal reads*** from DRAM or by using the DRAM multi purpose register (MPR)." EX1015, p.9. A Skilled Artisan would have understood that DQ/DQS margining refers to varying the Vref or Vdd voltages and monitoring the noise immunity and sensitivity of the data (DQ) and strobe (DQS) to widen the range of operating conditions. EX1069 (Tektronix Application Note), p.11. Thus, a Skilled Artisan would have understood that the provisional's mentioning of "normal operation" does not say anything about "*when the dynamic random access memory elements are not accessed for any normal memory read or write operations*."

66. Similarly, the provisional discloses that "an error occurrence generates an interrupt to the system during normal operation," and that an Error-Out pin is "High during normal operation unless a parity error occurs." EX1008, 24-25. A Skilled Artisan would have understood that those statements refer to the well-known operation of the Error-Out pin during normal operation and say

nothing about "*when the dynamic random access memory elements are **not accessed** for any normal memory read or write operations*." Thus, to the extent one might try to argue that "*normal memory read or write operations*" are ***not the same*** operations performed during initialization because the provisional discloses that the Error-Out pin operates differently during initialization, I disagree. The provisional merely describes the operation of the Error-out pin "during MB training" and "during normal operation," but the Error-out pin's operation does not change what a Skilled Artisan would have understood as "*normal memory read or write operations*." Indeed, JEDEC DDR, DDR2, and DDR3 memories do not have Error-out pins, but they can perform "*normal memory read or write operations.*" EX1024 (JESD79), p.7 (no Error_out or similar pin), pp.9-10 ("Normal operation" set in Mode Register); EX1084 (JESD79-2B), p.6-7 (no Error_out or similar pin), p.11 ("Normal operation" set in Mode Register); EX1056 (JESD79-3C), 13-14 (no Error_out or similar pin), 23&25 ("Normal operating mode" selected by Mode Register Set command). Similarly, the standard Registered DIMM also lacked any Error_out pins, but was understood to perform "*normal memory read or write operations*." EX1083 (JESD21-C), 6-7 (no Error_out or similar pin).

67. Furthermore, independent claims 1 and 19 require the module controller to be configured "*to apply a second signal related to one or more training sequences … **when** the memory module performs operations associated*

with the one or more training sequences and when the dynamic random access memory elements are ***not accessed*** *for any normal memory read or write operations*." EX1001, 15:42-49, 18:12-19. A Skilled Artisan would have understood from this claim language that the limitation of "*when the dynamic random access memory elements are not accessed for any normal memory read or write operations*" is a condition "*to apply a second signal related to one or more training sequences.*" But the provisional has no express or implicit disclosure about not accessing the memories for normal read or write operations as a condition to apply the "*second signal related to one or more training sequences.*"

68. Indeed, nothing in the provisional excludes normal memory read or write operations from the claimed "*operations associated with one or more training sequences*." The provisional references "training" in a single sentence fragment in the caption of Figure 3 (reproduced below). EX1008, 25.

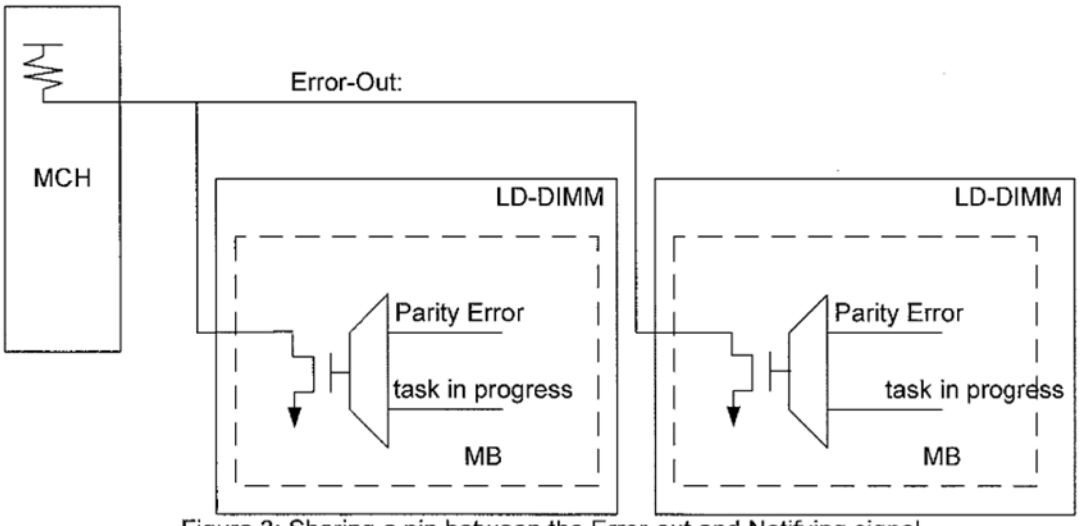
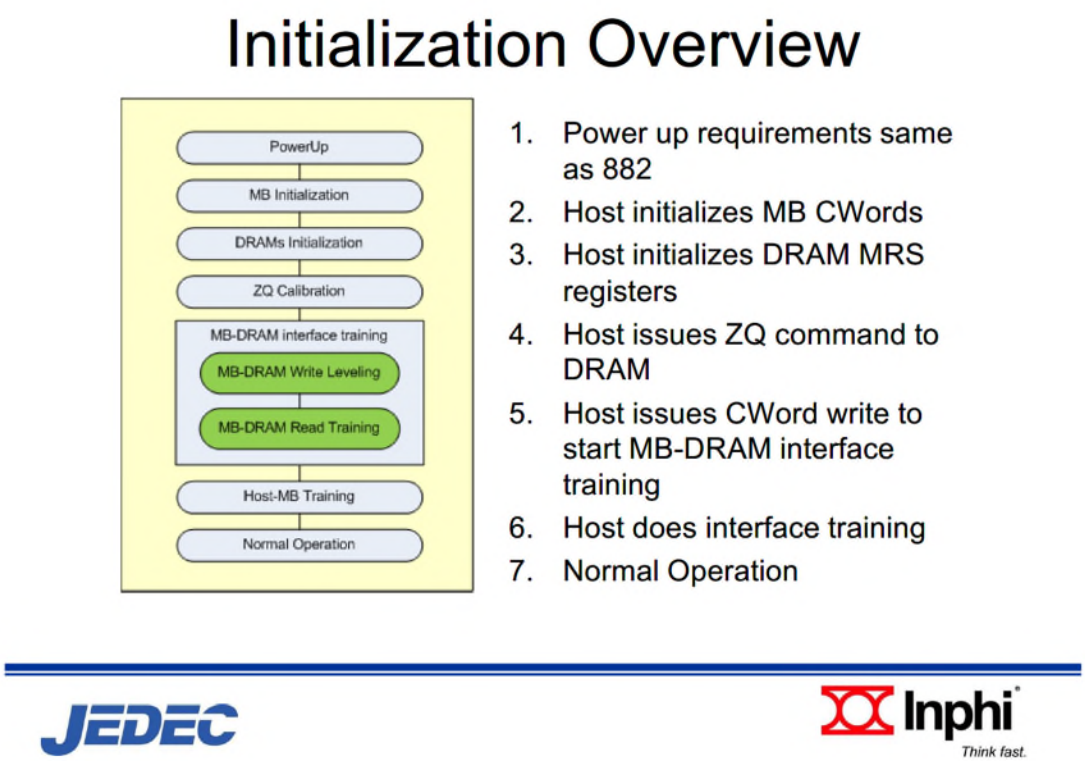


Figure 3: Sharing a pin between the Error-out and Notifying signal

Error-Out pin: Low during MB training (high signal indicates that training is done)
High during normal operation unless a parity error occurs

A Skilled Artisan would have understood that, in the context of JEDEC's proposals for load reduced DIMMs (denoted as both LD-DIMM and LR-DIMM in the provisional, EX1008, 22), "MB training" can refer to memory buffer training in general. *See, e.g.*, EX1039, 2 (reproduced below).



As shown by Inphi's JEDEC presentation above, a Skilled Artisan would have also understood that there were different types of "MB training," including MB-DRAM interface training and Host-MB training. *Id*. The provisional, however, does not specify which, if any, of these MB-training it is referring to, much less how the different training types relate to accessing or not the memory devices for normal memory read or write operations.

69. In any event, a Skilled Artisan would have understood that the memory devices can be accessed for normal read or write operations in association with any such MB training, for example, the host can make normal writes and reads and corresponding adjustments to ensure that the memory devices can be properly read or written in a wide range of operating conditions. EX1015, 9 ("The

host performs ***normal writes*** to DRAM for write DQ/DQS margining… The host performs read DQ/DQS margining by using ***normal reads*** from DRAM…"); *see also* EX1030 (US2007/0008791 by Butt, titled "DQS Strobe Centering (Data Eye Training) Method"), [0044] ("Verifying that valid DDR data may be read with the delay offset values set to zero. For example, a routine may be executed that writes to, reads from, and compares a selected data pattern to a selected range of the DDR memory 106.").

70. To be clear, a Skilled Artisan would have understood that the use of "normal writes" and "normal reads" was just one option, and training sequences can be performed without them. Indeed, the JEDEC proposal expressly excludes any DRAM commands to the Memory Buffer, including commands for normal read and write operations, during the MB-DRAM training. EX1015, 8 ("***No DRAM commands*** … can be issued to the MB ***until the MB-DRAM Interface training is complete***."). A Skilled Artisan would have also understood that techniques, such as JEDEC's standardized Write leveling, can be used for training proper write timing without any "normal writes," EX1056 (JESD79-3C), pp.42-45 (Write leveling), and reading a pre-determined pattern from the standardized Multi Purpose Register can be used for training proper read timing without any "normal reads," for example, for "Read Enable Training," EX1015 at 8 ("MB-DRAM Training" including "'Read Enable Training' to ensure it can capture read data

from the DRAMs correctly, as part of the DRAM interface training"), 8-9 (Host-MB Training" including the "host perform[ing] read DQ/DQS margining by using ***normal reads from DRAM or by using the DRAM multi purpose register (MPR)***"); EX1056 (JESD79-3C), pp.48-54 ("The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence…Memory controller repeats these calibration reads until read data capture at memory controller is optimized."). While using any of these known techniques would have been obvious to a Skilled Artisan, the provisional does not disclose whether and when its "MB training" uses any normal reads and writes, or whether it uses the standard Write leveling and MPR features instead. Therefore, a Skilled Artisan would have understood that the provisional lacks any disclosure of the claimed negative limitations about "*normal memory read or write operations*."

71. Independent, claim 10 similarly requires "*performing training operations associated with one or more training sequences when the dynamic random access memory elements are* ***not accessed*** *for any normal memory read or write operations; and applying a second signal related to the one or more training sequences … while the memory module performs the training operations*." EX1001, 16:54-60. As discussed immediately above, the provisional does not disclose how accessing the memory devices or not "*for any normal read or write operations*" relate to the only mentioning of MB-training, and a Skilled Artisan

would have understood that MB-training in general can include "normal writes to DRAM" and "normal reads from DRAM." EX1015, 9. Thus, the provisional also fails to support claim 10.

b) **Negative limitation in dependent claims 7 and 16: *"when the dynamic random access memory elements are <u>not communicating data</u> signals … <u>via the second edge connections</u>"***

72. Dependent claims 7 and 16 of the 024 Patent recite the negative limitation of "*the [training] operations associated with the one or more training sequences are performed when the dynamic random access memory elements are* ***not communicating data*** *signals associated with any normal memory read or write operations with the memory controller* ***via the second edge connections.***" EX1001, 16:4-9, 17:14-19. The provisional also lacks any disclosure of these limitations.

73. As discussed above with reference to independent claims 1 and 10, from which claims 7 and 16 respectively depend, the provisional does not disclose that the memory devices are not accessed for any normal memory read or write operations as part of the training. *Supra*, ¶¶61-71. For similar reasons, the provisional does not disclose that the training operations are performed when the memories are not communicating data associated with the normal memory read or write operations with the memory controller via the second edge connections. Indeed, a Skilled Artisan would have understood that normal read and write

operations can be performed as part of the training, for example, for DQ/DQS margining when the host communicates data signals through the edge connections of a DIMM. EX1015, 9 ("The host performs ***normal writes*** to DRAM for write DQ/DQS margining… The host performs read DQ/DQS margining by using ***normal reads*** from DRAM…").

c) **Negative limitation in dependent claims 8 and 17: *"the second edge connections are <u>not active</u> during the operations associated with the one or more training sequences"***

74. Dependent claims 8 and 17 of the 024 Patent recite the negative limitation of "***the second edge connections are not active*** *during the operations associated with the one or more training sequences.*" EX1001, 16:10-12, 17:20-22. The provisional also lacks any disclosure of these limitations.

75. As discussed above with reference to independent claims 1 and 10, from which claims 8 and 17 respectively depend, the provisional does not disclose that the memory devices are not accessed for any normal memory read or write operations as part of the training. *Supra*, ¶¶61-71. For similar reasons, the provisional does not disclose that ***the second edge connections are not active*** *during the operations associated with the one or more training sequences.*" Indeed, a Skilled Artisan would have understood that normal read and write operations can be performed as part of the training, for example, for DQ/DQS margining when the host communicates data signals through the edge connections

of a DIMM. EX1015, 9 ("The host performs ***normal writes*** to DRAM for write DQ/DQS margining… The host performs read DQ/DQS margining by using ***normal reads*** from DRAM…").

d) Independent claims 1, 10, and 19: *"one or more training sequences"*

76. Each of the independent claims 1, 10, and 19 recites "*one or more training sequences*." EX1001, 15:42-49 (claim 1), 16:54-60 (claim 10), 18:12-19 & 18:36-38 (claim 19). Claims 1 and 10 also recite applying "*a second signal related to one or more training sequences to the gate of the transistor*" and claim 19 recites coupling "*the second input to the output during the operations associated with the one or more training sequences.*" The provisional fails to disclose these limitations. Instead of the claimed "*one or more training sequences*" and the "*associated*" operations, the provisional merely discloses that the Error-Out pin is "Low during MB training (high signal indicates that training is done)." EX1008, p.25.

77. A Skilled Artisan would have understood the term "MB training" as a generic disclosure of "training" a memory buffer in some way. "MB training," by itself, does not disclose any specific training "*sequences*," and particularly not "*one or more*" training sequences, much less applying signals related to such specific "*training sequences*." Indeed, the phrases "training sequence" and "training sequences" are completely absent from the provisional. Instead of the specifically

claimed "*one or more training sequences*," the provisional associates the Low and High value of the error-out signal with the generic term "MB training." EX1008, 25.

78. The provisional application also mentions "initialization operation sequences," *id*., 22, but that does not disclose "*training sequences*" either. A Skilled Artisan would have understood that the term "initialization operation sequences" refers to a generic description of initialization, and is not limited to any specific "*training sequences*." *See, e.g.*, EX1056 (JESD79-C), pp.19-20 (explaining that "The following sequence is required for POWER UP and Initialization" including steps 1-11, such as applying power and issuing Mode Register Set commands, until step 12 when "The DDDR3 SDRAM is now ready for normal operation," without any reference to "*training sequences*.").

79. A Skilled Artisan would not "necessarily comprehend" the term "*one or more training sequences*" and its relation with the value of the error-out signal from the bare disclosure of "MB training" as of June 12, 2009, the filing date of the provisional application.

D. The Prosecution History of the 024 Patent

80. The prosecution histories of the 024 Patent and the other patent applications in the family of the 024 Patent are discussed below, starting with the earliest filed application, the 799 Provisional Application.

1. Provisional Application No. 61/186,799 (filed June 12, 2009) [EX1008]

81. The applicants filed U.S. Provisional Application No. 61/186,799 on June 12, 2009. EX1008,1. This application was titled "Method of Providing Handshaking Between a Memory Controller Hub and a Memory Subsystem" and consisted of an approximately two-and-a-half page written description and three figures. *Id.*, 22-25. This application acknowledged that "[i]n general, handshaking can be implemented in two methods; polling and notifying[,]"noted that "[i]n the notifying method, the memory subsystem controller sends a signal to the [Memory Controller Hub (MCH)] when it completes the required or requested operation" (*id.*,22) and claimed to "provide a method of establishing a handshake mechanism based on the notification signaling[]" (*id.*, 23). Specifically, this application proposed adding an "interface (notifying) signal between the MCH and the memory subsystem controller or by adding an additional functionality to an exi[s]ting, non-timing critical, signal without altering the memory subsystem hardware…." *Id.*,23.

2. Application No. 12/815,339 (filed June 14, 2010) [EX1007] resulting in U.S. Patent No. 8,489,837 (issued July 16, 2013) [EX1019], later found invalid by the Board [EX1035]

82. The applicants filed U.S. Patent Application No. 12/815,339 on June 14, 2010, claiming priority to U.S. Provisional Application No. 61/186,799 (discussed above). EX1007, 36.

83. On September 14, 2012, the examiner rejected several of the applicants' original claims as obvious over U.S. Patent Application Publication No. 2010/0042778 to Tanguay et al. ("Tanguay") and U.S. Patent Application Publication No. 2004/0115427 to Roohparvar et al. ("Roohparvar"). *Id.*, 61-67.

84. The applicants filed a response on February 14, 2013, amending the independent claims to overcome the examiner's rejection and include a limitation that required "trigger[ing] the memory controller to execute an interrupt routine." *Id.*, 85-88; *see also id.*, 91-92 (noting the addition of this limitation and arguing that the amended claims were unpatentable over Tanguay and Roohparvar).

85. The examiner thereafter allowed the claims without explanation (*id.*,103-104), resulting in the issuance of U.S. Patent No. 8,489,837 (the "'837 Patent") on July 16, 2013 (*id.*, 134).

86. On May 15, 2017, the PTAB instituted *inter partes* review proceedings to consider the patentability of Claims 1-3, 5, and 6 of the '837 Patent. *See* EX1035, 2. The PTAB entered a Final Written Decision on May 3, 2018, cancelling all of the challenged claims as unpatentable. *Id.*, 16-17. Cancelled Claims 1-3, 5, and 6 are reproduced below:

> 1. A memory module comprising:
>
> at least one output configured to be operatively coupled to a memory controller of a host computer system, the memory module configured to operate in at least two modes comprising an initialization mode during

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which the memory module executes at least one initialization sequence and an operational mode;

a controller circuit configured to cause the memory module to enter the initialization mode; and

a notification circuit configured to drive the at least one output while the memory module is in the initialization mode to provide at least one notification signal to the memory controller indicating at least one status of the at least one initialization sequence; and

wherein the at least one notification signal triggers the memory controller to execute an interrupt routine.

2. The memory module of claim 1, wherein the at least one status comprises completion of the at least one initialization sequence.

3. The memory module of claim 1, wherein the at least one status comprises execution of the at least one initialization sequence.

5. The memory module of claim 1, wherein the at least one output comprises an error-out pin of the memory module.

6. The memory module of claim 1, wherein the notification circuit is configured to drive the at least one output to a first state indicative of execution of the at least one initialization sequence or to a second state indicative of completion of the at least one initialization sequence.

87. Specifically, the PTAB (1) cancelled Claims 1-3 and 6 as unpatentable because they were obvious in view of U.S. Patent Application Publication No. 2005/0071580 to LeClerg ("LeClerg") and U.S. Patent Application Publication No. 2005/0193161 to Lee ("Lee") and (2) cancelled Claims 1-3, 5, and 6 as unpatentable because they were obvious in view of LeClerg, Lee, and U.S. Patent No. 8,359,521 to Kim ("Kim"). EX1035, 16-17; EX1019, 13-14.

3. Application No. 13/942,721 (filed July 16, 2013) [EX1006] resulting in U.S. Patent No. 9,311,116 (issued Apr. 12, 2016) [EX1094]

88. On July 16, 2013, before the aforementioned ’837 Patent issued, the applicants filed U.S. Patent Application No. 13/942,721, claiming priority back to U.S. Provisional Application No. 61/186,799 (discussed above). EX1006, 39.

89. On August 5, 2014, the applicants filed a preliminary amendment, amending and cancelling some of the originally filed claims, and adding new claims. *Id.*, 55-59.

90. On May 22, 2015, the examiner issued a nonstatutory double patenting rejection against the claims, finding that they were “not patentably distinct” from the claims of the ’837 Patent (discussed above). *Id.*, 66-68.

91. On August 24, 2015, the applicants filed a terminal disclaimer (*id.*, 86), arguing that this overcame the examiner’s rejection (*id.*, 80).

92. On November 16, 2015, the examiner again rejected the claims based on nonstatutory double patenting, finding that the terminal disclaimer was signed by an individual who “ha[d] not been established as being authorized to act on behalf of the assignee.” *Id.*, 92.

93. On January 21, 2016, the applicants filed a second terminal disclaimer (*id.*, 97), amended the claims (*id.*, 100-03), and argued that the second terminal disclaimer overcame the examiner’s rejection (*id.*, 104).

94. The examiner thereafter allowed the claims without explanation (*id.*,115-16), resulting in the issuance of U.S. Patent No. 9,311,116 (the "'116 Patent") on April 12, 2016 (*id.*, 132).

4. Application No. 15/088,115 (filed Apr. 1, 2016) [EX1005] resulting in U.S. Patent No. 9,858,218 (issued Jan. 2, 2018) [EX1095], later found invalid by the Board [EX1102]

95. On April 1, 2016, before the aforementioned '116 Patent issued, the applicants filed U.S. Patent Application No. 15/088,115, claiming priority back to U.S. Provisional Application No. 61/186,799 (discussed above). EX1005, 46.

96. On May 20, 2016, the examiner issued a nonstatutory double patenting rejection against the claims, finding that they were "not patentably distinct" from the claims of the '116 and '837 Patents (discussed above). *Id.*, 51-52. The examiner also rejected the claims as obvious over the same references that had originally been used to reject the claims of the '837 Patent during prosecution: Tanguay and Roohparvar. *Id.*, 53-56.

97. On August 10, 2016, the applicants filed a terminal disclaimer (*id.*, 61), arguing that this overcame the examiner's nonstatutory double patenting rejection (*id.*, 75). The applicants also cancelled the originally filed claims, introducing a new claim set. *Id.*, 70-74. The applicants argued that neither Tanguay nor Roohparvar disclosed "any signal output by a module controller to the memory controller, … let alone any signal output from a module controller via

an open drain output to indicate a parity error having occurred in the memory module during a read, write, refresh, or precharge operation, or a notification signal associated with one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation output from the module controller via the same open drain output…." *Id.*, 75-80.

98. On November 11, 2016, the examiner rejected the claims as obvious over U.S. Patent Application Publication No. 2010/0202240 to Moshayedi ("Moshayedi") and U.S. Patent Application Publication No. 2008/0256281 to Fahr ("Fahr"). *Id.*, 103-105.

99. The applicants filed a response on April 25, 2017, arguing that neither Moshayedi nor Fahr disclosed "wherein the module controller is further configured to process one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation, and wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the memory controller via the open drain output of the module controller and the edge and the error edge connection[.]" *Id.*, 138-44.

100. On May 25, 2017, the applicants filed another response, further amending the claims (*id.*, 168-72) and repeating the same arguments against Moshayedi and Fahr (*id.*, 173-79).

101. On June 16, 2017, the examiner rejected the claims as obvious in view of Moshayedi, Fahr, and U.S. Patent Application Publication No. 2010/0142383 to Goishi ("Goishi"). *Id.*, 187-90.

102. On September 18, 2017, the applicants filed a response, further amending the claims (*id.*, 204-09) and arguing that Moshayedi, Fahr, and Goishi all failed to disclose "'an open drain output coupled to the error edge connection' and the module controller being configured to output to the error edge connection 'a signal indicating a parity error having occurred' while the memory module is configured to perform one or more memory read or write operations[]" (*id.*, 210-16).

103. The examiner thereafter allowed the claims without explanation (*id.*, 228-29), resulting in the issuance of U.S. Patent No. 9,858,218 (the "'218 Patent") on January 2, 2018 (EX1095).

104. Thereafter, on June 8, 2020, SK hynix Inc. and SK hynix America Inc. filed with the PTAB a petition for *inter partes* review of all claims (Claims 1-22). EX1062, 8, 10. I filed a declaration in support of this petition. *See id.*, 8.

105. On December 17, 2020, the PTAB instituted *inter partes* review proceedings to consider the patentability of all the issued claims of the '218 Patent (Claims 1-22). EX1062, 8, 54. Claims 1-22 (which were ultimately cancelled as unpatentable, as discussed below) are reproduced below:

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1. A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

dynamic random access memory elements on the printed circuit board;

a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and

wherein the memory module is operable in at least a first mode and a second mode, wherein the memory module in the first mode is configured to be trained with one or more training sequences; wherein the memory module in the second mode is configured to perform one or more memory read or write operations not associated with the one or more training sequences by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections;

wherein the module controller is configured to receive via the second edge connections the address and command signals associated with the one or more memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals, and wherein the module controller is further configured to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the second mode;

wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output while the memory module is in the first mode.

2. The memory module of claim 1, wherein the module controller comprises an integrated circuit.

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3. The memory module of claim 1, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.

4. The memory module of claim 3, wherein the notification circuit is configured to drive the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.

5. The memory module of claim 4, wherein the notification circuit is configured to drive the parity error signal by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.

6. The memory module of claim 4, wherein the notification circuit is configured to drive the notification signal using one or more OR logic elements.

7. The memory module of claim 1, wherein the first edge connections are not active when the memory module is in the first mode and configured to be trained with the one or more training sequences.

8. The memory module of claim 1, wherein the module controller is configured to drive the notification signal to indicate a status of the one or more training sequences.

9. A method performed by a memory module operating with a memory controller of the host system, the memory module including dynamic random access memory elements on a printed circuit board, the printed circuit board having edge connections that fit into a corresponding slot of a host system, the edge connections including first edge connections via which the dynamic random access memory devices communicate data with the memory controller, second edge connections via which the memory module receives address and command signals from the memory controller, and an error edge connection in addition to the first edge connections and the second edge connections, the method comprising:

receiving from the memory controller address and command signals associated with one or more memory read or write operations;

controlling the dynamic random access memory elements in accordance with the address and command signals;

outputting to the memory controller via an open-drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module; and

training with one or more training sequences while the first edge connections are not active, and driving a notification signal associated with the one or more training sequences to the memory controller via the open drain output and the error edge connection.

10. The method of claim 9, wherein driving the notification signal comprises driving a gate of each of one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground, the one or more transistors each having an open drain coupled to the open drain output.

11. The method of claim 10, wherein driving the signal indicating the parity error comprises driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground.

12. The method of claim 10, wherein driving the notification signal comprises using one or more OR logic elements.

13. The method of claim 9, wherein the memory module is configured to be trained with the one or more training sequences in response to a request by the memory controller.

14. The method of claim 9, wherein the notification signal indicates a status of the one or more training sequences.

15. A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and command signals, and an error edge connection in addition to the first edge connections and the second edge connections;

dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the first edge connections; and

a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection;

wherein the memory module is configurable to perform at least a first operation and a second operation;

wherein the module controller in the first operation is configured to receive via the second edge connections address and command signals associated with one or more memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals, wherein the module controller in the first operation is further configured to output to the memory controller a signal indicating a parity error having occurred in the memory module; and

wherein the memory module in the second operation is configured to be trained with one or more training sequences while the first edge connections are not active, and wherein the module controller in the second operation is configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output of the module controller.

16. The memory module of claim 15, wherein the module controller comprises an integrated circuit.

17. The memory module of claim 15, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.

18. The memory module of claim 17, wherein the notification circuit is configured to generate the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.

19. The memory module of claim 18, wherein the notification circuit is configured to drive the signal indicating the parity error by driving the gate

of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.

20. The memory module of claim 18, wherein the notification circuit is configured to drive the notification signal using one or more OR logic elements.

21. The memory module of claim 15, wherein the memory module is configured to perform the second operation in response to a command from the memory controller.

22. The memory module of claim 15, wherein the module controller is configured to drive the notification signal to indicate a status of the one or more training sequences.

106. As part of its institution decision, the PTAB determined that U.S. Provisional Application No. 61/186,799 (filed June 12, 2009) did not provide written description support for the challenged claims. EX1062, 31. Accordingly, the PTAB determined that there was a sufficient showing that JEDEC COMMITTEE LETTER BALLOT, LRDIMM DDR Memory Initialization Chapter Proposal (Dec. 2009) ("JEDEC") [EX1015] was prior art to the '218 Patent. *Id.*

107. On May 6, 2021, the PTAB dismissed the *inter partes* review proceedings petitioned for by SK hynix Inc. and SK hynix America Inc. due to settlement after institution of trial. EX1060.

108. On October 15, 2021, Samsung Electronics Co., Ltd. filed with the PTAB a petition for *inter partes* review of the '218 Patent. EX1098. I filed a declaration in support of this petition. EX1099.

109. The PTAB entered a Final Written Decision on May 8, 2023, cancelling all of the challenged claims as unpatentable. EX1102, 77-78. Specifically, the PTAB (1) cancelled Claims 1-22 as unpatentable because they were obvious over U.S. Patent Application Publication No. 2008/0098277 to Hazelzet ("Hazelzet") and U.S. Patent No. 8,139,430 to Buchmann ("Buchmann") and (2) cancelled Claims 3-6, 10-12, and 17-20 as unpatentable because they were obvious over Hazelzet, Buchmann, and Kim (which, as discussed above, was also used in an *inter partes* review proceeding against the '837 Patent). *Id.*, 77-78. The PTAB declined to consider whether the challenged claims were unpatentable because they were obvious over Hazelzet and JEDEC. *Id.*, 78 & n.13.

110. The PTAB found that a person of ordinary skill in the art "'would have had a [B]achelor's degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems. She would have been familiar with computer memory systems and basic CPU architecture documented in the literature, including standards, and generally available in commercial systems, including how computer components access a computer's memory, the role of a memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory devices to the other components of the computer system.'" *Id.*, 11-12 (quoting EX1099, ¶56). The PTAB gave the claim terms "memory read and write operations,"

"training sequence," "notification signal" and related terms their plain and ordinary meaning. *Id.*, 12-15.

111. On October 19, 2023, the Federal Circuit dismissed Netlist's appeal of the PTAB's final written decision. EX1104; EX1095, 15-16.

5. Application No. 15/169,745 (filed June 1, 2016) [EX1038] resulting in U.S. Patent No. 9,535,623 (issued Jan. 3, 2017) [EX1031], later found invalid by the Board [EX1034]

112. On June 1, 2016, before the aforementioned '218 Patent issued, the applicants filed U.S. Patent Application No. 15/169,745, claiming priority back to U.S. Provisional Application No. 61/186,799 (discussed above). EX1038, 50.

113. On July 29, 2016, the examiner issued a nonstatutory double patenting rejection against the claims, finding that they were "not patentably distinct" from the claims of the '116 Patent (discussed above). *Id.*, 56-58.

114. On August 3, 2016, the applicants filed a terminal disclaimer (*id.*, 79-81), amended the claims (*id.*, 64-70), and argued that the second terminal disclaimer overcame the examiner's rejection (*id.*, 71).

115. The examiner thereafter allowed the claims without explanation (*id.*,100-01), resulting in the issuance of U.S. Patent No. 9,535,623 (the "'623 Patent") on January 3, 2017 (*id.*, 124).

116. Thereafter, on December 14, 2017, SK hynix Inc., SK hynix America Inc., and SK hynix memory solutions, Inc. filed with the PTAB a petition for *inter*

partes review of all claims (Claims 1-29) of the '623 Patent. EX1032. I provided a declaration in support of this petition. EX1033.

117. The PTAB then instituted *inter partes* review of all challenged claims. EX1034, 2. On March 21, 2019, the PTAB entered a Final Written Decision cancelling all of the challenged claims as unpatentable. *Id.*, 20-22. Cancelled claims 1-29 are reproduced below:

> 1. A memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system, the memory module comprising:
>
> a module controller having an open drain output, the module controller generating a parity error signal and driving the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode, the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode, wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system, the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode and outputting the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode; and
>
> a printed circuit board having a first set of edge connections for communicating address and control signals from the memory controller of the host system, a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module controller, the memory module communicating to the memory controller of the host system via the error edge connection the parity error signal while the memory

module operates in the first mode and the notification signal while the memory module is in the second mode.

2. The memory module of claim 1, further comprising:

a plurality of synchronous dynamic random access memory elements, wherein, while the memory module is in the first mode, the module controller receives and processes address and control signals corresponding to read or write commands from the memory controller of the host system and transmits processed address and control signals to the plurality of synchronous dynamic random access memory elements.

3. The memory module of claim 1, wherein, while the memory module is in the second mode, the module controller drives the notification signal to a logic low level via the open drain output to indicate a status of the one or more training sequences.

4. The memory module of claim 1, wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module.

5. The memory module of claim 1, wherein the one or more training sequences are executed by the module controller in response to a command or a signal received from the memory controller of the host system.

6. The memory module of claim 1, wherein the module controller comprises one or more integrated circuit.

7. The memory module of claim 1, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.

8. The memory module of claim 7, wherein the notification circuit generates the notification signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.

9. The memory module of claim 7, wherein the notification circuit generates the parity error signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.

10. The memory module of claim 7, wherein the notification circuit generates the notification signal using one or more OR logic elements.

11. The memory module of claim 1, wherein the module controller implements the one or more training sequences in response to a signal or a command received from the memory controller of the host system.

12. A memory module to be coupled to a memory controller of a host system, the memory module comprising:

a plurality of synchronous dynamic random access memory elements;

a printed circuit board (PCB) having a first set of edge connections for communicating address and control signals from the memory controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in a first mode, the PCB further including an error edge connection in addition to the first set of edge connections and the second set of edge connections;

a module circuit controlling the plurality of synchronous dynamic random access memory elements in response to read and write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode, the module circuit generating a parity error signal indicative of a parity error having occurred in the memory module while the memory module operates in the first mode, the module circuit causing the memory module to enter a second mode in response to a command from the memory controller of the host system, the module circuit generating a notification signal in response to one or more training sequences while the memory module is in the second mode, the notification signal indicating a status of the one or more training sequences; and

a notification circuit having an open drain output coupled to the error edge connection of the PCB, the notification circuit driving the parity error signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module operates in the first mode, the notification circuit driving the notification signal to the memory controller of the host system via the

open drain output and the error edge connection while the memory module is in the second mode.

13. The memory module of claim 12, wherein the memory module executes the one or more training sequences in response to a signal or a command from the memory controller of the host system.

14. The memory module of claim 12, wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module.

15. The memory module of claim 12, wherein the notification circuit generates the notification signal using one or more OR logic elements.

16. The memory module of claim 12, wherein the notification circuit is a physically separate circuit from the module circuit.

17. The memory module of claim 12, wherein the module circuit includes the notification circuit.

18. The memory module of claim 12, wherein the notification circuit includes one or more transistors each having an open drain coupled to the open drain output.

19. The memory module of claim 18, wherein the notification circuit generates the notification signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.

20. The memory module of claim 18, wherein the notification circuit generates the parity error signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.

21. A memory module operable in at least a first mode and a second mode, the memory module comprising:

a plurality of synchronous dynamic random access memory elements;

a printed circuit board (PCB) having a first set of edge connections for communicating address and control signals from the memory controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the

memory controller of the host system while the memory module operates in the first mode, the PCB further including an error edge connection in addition to the first set of edge connections and the second set of edge connections, wherein the PCB is configured to fit into a corresponding slot connector of the host system; and

a module controller having an open drain output coupled to the error edge connection, the module controller being configured to transmit address and control signals to the plurality of synchronous dynamic random access memory elements in response to read or write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode, to generate a parity error signal indicating a parity error having occurred in the memory module while the memory module is in the first mode, and to transmit the parity error signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the first mode, the module controller being further configured to cause the memory module to enter the second mode in response to a command from the memory controller of the host system, to generate a notification signal indicating a status of one or more training sequences while the memory module is in the second mode, and to transmit the notification signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the second mode.

22. The memory module of claim 21, wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module.

23. The memory module of claim 21, wherein the memory module executes the one or more training sequences in response to a command or a signal received from the memory controller of the host system.

24. The memory module of claim 21, wherein the module controller includes a notification circuit comprising one or more transistors, each of the one or more transistors having an open drain coupled to the open drain output.

25. The memory module of claim 24, wherein the notification circuit is configured to generate the notification signal by driving a gate of each of the

one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.

26. The memory module of claim 24, wherein the notification circuit is configured to generate the parity error signal by by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.

27. The memory module of claim 24, wherein the notification circuit is configured to generate the notification signal using one or more OR logic elements.

28. The memory module of claim 24, wherein the module controller comprises one or more integrated circuits.

29. The memory module of claim 21, wherein the module controller is further configured to implement the one or more training sequences in response to a signal or a command received from the memory controller of the host system.

118. Specifically, the PTAB (1) cancelled Claims 1-29 as unpatentable because they were obvious in view of Hazelzet (discussed above) and any one of Buchmann (discussed above) and U.S. Patent Application Publication No. 2008/0147897 to Talbot ("Talbot"), (2) cancelled Claims 8, 9, 19, 20, 25, and 26 as unpatentable because they were obvious in view of Hazelzet, U.S. Patent No. 7,525,860 to Hokenmaier ("Hokenmaier") and any one of Buchmann or Talbot, and (3) cancelled Claims 10, 15, and 27 as unpatentable because they were obvious in view of Hazelzet, Kim (discussed above), and any one of Buchmann or Talbot. EX1034, 20-22; EX1031, 15-16. The PTAB did not issue a decision as to grounds

that also included U.S. Patent Application Pub. 2008/0155378 to Amidi ("Amidi"). *See* EX1034, 6, 20, 22.

119. The PTAB found that a person of ordinary skill in the art "would be someone who was familiar with computer memory systems and basic CPU architecture, which includes knowledge of techniques related to how computer components access a computer's memory, including the role of a memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory, as well as applicable standards]" and "would have had a bachelor's degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems." *Id.*, 8 (citing EX1032, 4-5; EX1033, ¶43).

6. Application No. 15/857,553 (filed Dec. 28, 2017) [EX1096], resulting in U.S. Patent No. 10,474,595 (issued Nov. 12, 2019) [EX1097], later found invalid by the Board [EX1103]

120. On December 28, 2017, before the aforementioned '218 Patent issued, the applicants filed U.S. Patent Application No. 15/857,553, claiming priority back to U.S. Provisional Application No. 61/186,799 (discussed above). EX1096, 43.

121. On August 28, 2018, the examiner issued a nonstatutory double patenting rejection against the claims, finding that they were "not patentably distinct" from the claims of the '837, '116, and '218 Patents (discussed above). *Id.*, 82-83.

122. On November 28, 2018, the applicants filed a terminal disclaimer (*id.*, 106-07), amended the claims (*id.*, 99-103), and argued that the terminal disclaimer overcame the examiner's rejection (*id.*, 104-05).

123. On February 6, 2019, the examiner issued a notice of allowance without explanation. *Id.*, 121-22.

124. On March 1, 2019, the applicants filed a request for continued examination (*id.*, 145), amended the specification's title and abstract (*id.*, 147), and amended the claims (*id.*, 148-53).

125. On March 29, 2019, the examiner issued a notice of allowance without explanation. *Id.*, 182-83.

126. On July 1, 2019, the applicants filed a request for continued examination (*id.*, 222), amended the specification's title and abstract (*id.*, 239-40), and amended the claims (*id.*, 224-32).

127. The examiner thereafter allowed the claims without explanation (*id.*, 243-44), resulting in the issuance of U.S. Patent No. 10,474,595 (the "'595 Patent") on November 12, 2019 (*id.*, 266).

128. Thereafter, on June 8, 2020, SK hynix Inc. and SK hynix America Inc. filed with the PTAB a petition for *inter partes* review of all claims (Claims 1-24). EX1058. I filed a declaration in support of this petition. *See id.*, 80.

129. On December 17, 2020, the PTAB instituted *inter partes* review of all challenged claims. EX1059, 45. Claims 1-24 (which were ultimately cancelled as unpatentable, as discussed below) are reproduced below:

> 1. A memory module operable with a memory controller of a host system, comprising:
>
> a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;
>
> dynamic random access memory elements on the printed circuit board;
>
> a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and
>
> wherein the memory module is configurable to operate in any of at least a first mode and a second mode;
>
> wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;
>
> wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the dynamic random access memory elements are configurable to

communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;

wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

2. The memory module of claim 1, wherein the module controller comprises an integrated circuit.

3. The memory module of claim 1, wherein the module controller includes a notification circuit comprising a transistor having an open drain coupled to the open drain output and source coupled to the ground.

4. The memory module of claim 3, wherein the module controller is configurable to drive a gate of the transistor high so as to drive open drain output and the error edge connection to ground, or to drive the gate of the transistor low so as to drive the open drain output and the error edge connection to the high impedance state.

5. The memory module of claim 4, wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and the ground.

6. The memory module of claim 3, wherein the notification circuit further includes a multiplexor or a logic circuit having a output coupled to a gate of the transistor and configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.

7. The memory module of claim 3, wherein the module controller is configurable to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal so as to

drive the open drain output from the high impedance state to ground or from ground to the high impedance state.

8. The memory module of claim 1, wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode.

9. The memory module of claim 1, wherein the memory module in the second mode is configurable to perform the operations related to the one or more training sequences without communicating data signals via the first edge connections while the memory module is in the second mode.

10. A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;

dynamic random access memory elements on the printed circuit board;

a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and

wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or

more training sequences without communicating data signals via the first edge connections;

wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;

wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode.

11. The memory module of claim 10, wherein the module controller comprises an integrated circuit.

12. The memory module of claim 10, wherein the module controller includes a notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to the ground, wherein the module controller is configurable to output to the memory controller the open-drain signals related to the one or more training sequences by driving a gate of the transistor high so as to drive the open drain output and the error edge connection to ground, and by driving the gate of the transistor low as to drive the open drain output and the error edge connection to the high impedance state, and wherein the notification circuit is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and ground.

13. The memory module of claim 12, wherein the notification circuit further includes a multiplexor or a logic circuit having an output coupled to the gate of the transistor and configurable to drive the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.

14. The memory module of claim 10, wherein the module controller is configurable to output the open-drain signals related to the one or more training sequences by driving the open drain output from the high impedance state to the low logic level or from the low logic level to the high impedance state.

15. The memory module of claim 10, wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode.

16. The memory module of claim 10, wherein the second edge connections include one or more high-order address pins that are not active while the memory module is in the second mode.

17. A method, comprising:

at a memory module coupled with a memory controller of a host system, the memory module including a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections, the memory module further including dynamic random access memory elements on the printed circuit board;

receiving via the second edge connections address and control signals associated with one or more memory read or write operations;

controlling the dynamic random access memory elements to communicate data signals corresponding to the one or more memory read or write operations via the first edge connections in response to the address and control signals;

outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is being accessed by the memory controller for a memory read or write operation;

performing operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations; and

outputting to the memory controller via the open drain output and the error edge connection open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation.

18. The method of claim 17, wherein the second edge connections include one or more pins that are not active while the memory module is trained with the one or more training sequences.

19. The method of claim 18, wherein the second edge connections include one or more high-order address pins that are not active while the memory module is trained with the one or more training sequences.

20. The method of claim 17, wherein the memory module includes a notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to ground, wherein outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module comprises driving a gate of the transistor high to provide a low impedance path between the open drain output and ground, and wherein outputting the open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation comprises driving the gate of the transistor to drive the open drain output from a high impedance state to ground and from ground to the high impedance state.

21. A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

dynamic random access memory elements on the printed circuit board; and

a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller including a transistor having a gate and an open drain output coupled to the error edge connection;

wherein the module controller is configurable to drive the gate of the transistor so as to drive the open drain output to a first state or a second state, the first state being a low logic level and the second state being a high impedance state;

wherein the module controller is configurable to receive via the second edge connections memory commands associated with normal memory read or write operations and to output a set of address and control signals for each of the normal memory read or write operations;

wherein the dynamic random access memory elements are configurable to communicate one or more N-bit-wide data signals with the memory controller via the first edge connections in response to the set of address and control signals, where N is at least 32;

wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred during any of the memory read or write operations by driving the open drain output and the error edge connection to the first state;

wherein the memory module is configurable to perform operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations; and

wherein the module controller is configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection from one of the first state and the second state to the other one of the first state and the second state.

22. The memory module of claim 21, wherein the module controller further includes a multiplexor or a logic circuit having an output coupled to the gate of the transistor, and wherein the module controller is configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.

> 23. The memory module of claim 22, wherein the transistor has a source coupled to ground, wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and ground, and wherein the module controller is configurable to provide the information related to the one or more training sequences by driving the open drain output from a high impedance state to ground or from ground to the high impedance state.
>
> 24. The memory module of claim 21, wherein the memory module is configurable to perform the operations related to the one or more training sequences while the memory module is not communicating signals via the first edge connections.

130. As part of its institution decision, the PTAB determined that U.S. Provisional Application No. 61/186,799 (filed June 12, 2009) did not provide written description support for the challenged claims. EX1059, 27. Accordingly, the PTAB determined that there was a sufficient showing that JEDEC [EX1015] (discussed above) was prior art to the '595 Patent. *Id.* The PTAB also noted that the terms "memory read or write operations" and "normal memory read and write operations" have their "ordinary and customary meanings." *Id.*, 29-30.

131. On May 6, 2021, the PTAB dismissed the *inter partes* review proceedings petitioned for by SK hynix Inc. and SK hynix America Inc. due to settlement after institution of trial. EX1060.

132. On October 15, 2021, Samsung Electronics Co., Ltd. filed with the PTAB a petition for *inter partes* review of all claims (Claims 1-24) of the '595 Patent. EX1100. I provided a declaration in support of this petition. EX1101.

133. The PTAB entered a Final Written Decision on May 9, 2023, cancelling all of the challenged claims as unpatentable. EX1103, 84-85. Specifically, the PTAB (1) cancelled Claims 1-24 as unpatentable because they were obvious in view of Hazelzet and Buchmann (which, as discussed above, were also used in an *inter partes* review proceeding against the '218 Patent) and (2) cancelled Claims 3-7, 12-14, 20, 22, and 23 as unpatentable because they were obvious over Hazelzet, Buchmann, and Kim (which, as discussed above, was also used in an *inter partes* review proceeding against the '837 and '218 Patents). *Id.* The PTAB declined to consider whether the challenged claims were unpatentable because they were obvious over Hazelzet and JEDEC. *Id.*, 85&n.13.

134. The PTAB found that a person of ordinary skill in the art "would have had a [B]achelor's degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems. She would have been familiar with computer memory systems and basic CPU architecture documented in the literature, including standards, and generally available in commercial systems, including how computer components access a computer's memory, the role of a memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory devices to the other components of the computer system" *Id.*, 11-12 (quoting EX1100, 10).

135. The PTAB gave the claim terms "memory read and write operations," "normal memory read or write operations," "mode," "training sequence," "notification signal" and related terms their plain and ordinary meaning. *Id.*, 12-15.

136. On October 19, 2023, the Federal Circuit dismissed Netlist's appeal of the PTAB's final written decision. EX1104; EX1097, 18-19.

7. Application No. 16/680,060 (filed Nov. 11, 2019) [EX1002] resulting in U.S. Patent No. 11,386,024 (issued July 12, 2022) [EX1001]

137. On November 11, 2019, before the aforementioned '595 Patent issued, the applicants filed U.S. Patent Application No. 16/680,060, claiming priority back to U.S. Provisional Application No. 61/186,799 (discussed above). EX1002, 45.

138. On March 5, 2020, the applicants filed a preliminary amendment that replaced the abstract (*id.*, 71) and cancelled the original claim set, replacing it with a new claim set (*id.*, 72-76).

139. On April 13, 2020, the applicants filed a supplemental preliminary amendment that amended two paragraphs of the specification (*id.*, 81-82) and amended the claims (*id.*, 83-87).

140. On September 3, 2020, the examiner issued a nonstatutory double patenting rejection against the claims, finding that they were "not patentably

distinct" from the claims of the '595 and 218 Patents (discussed above). *Id.*, 122-23.

141. On November 9, 2020, the applicants filed a terminal disclaimer (*id.*, 149-50), amended three dependent claims (*id.*, 155-59), and argued that the terminal disclaimer overcame the examiner's rejection (*id.*, 153-54).

142. On February 24, 2021, the examiner rejected the claims as obvious over Hazelzet and what the examiner referred to as "JEDEC," with citations to figures and pages that correspond to the JEDEC standard JESD206 (FBDIMM: Architecture and Protocol (January 2007) (EX1025). EX1002, 192-96, 222 (applicant confirming "JEDEC" refers to "JESD206").

143. On April 25, 2021, the applicants proposed amendments to the claims (*id.*, 226-31) and argued that "neither Hazelzet nor [JESD206] teaches or suggests, among other things, 'to apply (or applying) a first signal to the gate of the transistor (having an open drain coupled to the error edge connection) to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation," **and** "to apply (or applying) a second signal related to one or more training sequences to the gate of the transistor when the memory module performs training_operations [sic] associated with the one or more training sequences.'" *Id.*, 222-24. The applicants also argued that "persons of ordinary skill in the art would not be motivated to combine [JESD206]'s training

sequences with the ECC Solution in Hazelzet, because Hazelzet's solution using ECC and [JESD206] memory buffer training are distinct solutions to distinct problems." *Id.*, 224. The applicants also argued that "there is no teaching or suggestion in either Hazelzet or [JESD206] why it would be advantageous to use either of the outputs 120, 121 in Hazelzet to output a signal related to any training sequences." *Id.*

144. On May 5, 2021, the examiner issued an advisory action stating that the amendment of "the training operations are not normal read and write" into the claims was not supported by the original disclosure and was considered new matter. *Id.*, 247. The examiner stated that the proposed amendment of April 25, 2021, could not be considered. *Id.*

145. On May 24, 2021, the applicants filed a response without the amendments that had been proposed on April 25, 2021, repeating their arguments regarding the alleged lack of disclosure by Hazelzet and JESD206. *Id.*, 259-61.

146. On June 3, 2021, the examiner issued an advisory action saying that the "amendment filed on 5/24/2021 is a second amendment after final presented in the case and thus, has not been entered." *Id.*, 267.

147. On July 26, 2021, the applicants amended the claims (*id.*, 283-88) and argued that "neither Hazelzet nor [JESD206] teaches or suggests, among other things, 'to apply (or applying) a first signal to the gate of the transistor (having an

open drain coupled to the error edge connection) to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation,' **and** 'to apply (or applying) a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences.'" *Id.*, 289-91. The applicants also argued that "persons of ordinary skill in the art would not be motivated to combine [JESD206]'s training sequences with the ECC Solution in Hazelzet, because Hazelzet's solution using ECC and [JESD206] memory buffer training are distinct solutions to distinct problems." *Id.*, 291. The applicants also argued that "there is no teaching or suggestion in either Hazelzet or [JESD206] why it would be advantageous to use either of the outputs 120, 121 in Hazelzet to output a signal related to any training sequences." *Id.*

148. On September 15, 2021, the examiner again rejected the claims as obvious in view of Hazelzet and "JEDEC." *Id.*, 300. The Examiner initially suggested that "JEDEC" referred to JESD79-3 [EX1085], *id.*, but then the Examiner again cited to Figures (such as "3-4, 3-7," etc.) which exist in JESD206 [EX1025] and not JESD79-3 [EX1085], *id.*, 306, 346, so it appears the Examiner was continuing to rely on JESD206 [EX1025] as the applicant had understood, *id.*, 289. The Examiner wrote that "the alleged features [which applicant argues are not taught or suggested by Hazelzet or JESD206] are not positively recited in the

claims and that the alleged features are a statement of purpose or use which do not add patentable weight to the claims." *Id.*, 300-01. The examiner also rejected the applicants' argument regarding a lack of a motivation to combine because "the features upon which the applicant relies…are not recited in the rejected claim(s)." *Id.*, 301-02. The examiner also noted various other problems with the applicants' arguments regarding an alleged lack of a motivation to combine. *Id.*, 302-04. The examiner then again rejected the claims as obvious in view of Hazelzet and JESD206. *Id.*, 305-09.

149. On December 15, 2021, the applicants filed a response. The applicants noted it was ambiguous whether the Examiner's reference to "JEDEC" was to JESD79-3 [EX1085], as suggested by the Examiner, or to JESD206 [EX1025], given that the cited figures only appeared in JESD206. *Id.*, 344, 346. The applicants also argued that "the claims are partially defined by the functions that the module controller is configured to carry out[]" because the claims recite "'the module controller is **configurable to** apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation' and 'wherein the module controller is **further configurable to** apply a second signal related to one or more training sequences to the gate of the transistor when ...'" *Id.*, 344-45. The applicants also argued that neither Hazelzet nor JESD79-3 disclosed "a module

controller configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred during normal memory read or write operations, and then a second signal related to one or more training sequences to the **same** gate of the transistor." *Id.*, 346. The applicants also identified alleged deficiencies in the prior art for other specific claims. *Id.*, 347-48.

150. On January 7, 2022, the applicants amended the claims to replace "configurable" with "configured" (*id.*, 354-59) and asked the examiner to reconsider the rejection (*id.*, 360).

151. The examiner thereafter allowed the claims without explanation (*id.*, 375-79), resulting in the issuance of U.S. Patent No. 11,386,024 (the "'024 Patent") on July 12, 2022 (*id.*, 447).

E. Comparison of the claims of the 024 Patent to claims previously found invalid

152. I have reviewed the Final Written Decisions issued by the PTAB cancelling the claims of the '623, '218, and '595 Patents (discussed above). The claims already cancelled by the PTAB contain limitations identical or substantially similar to the limitations of the '024 Patent. I have provided a mapping of the limitations below.

153. The table below compares the claim limitations of the 024 Patent (reprinted below starting on page 321) to those in the '623 Patent (reprinted below starting on page 327).

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('623 Patent, EX1031, EX1034)**
1.[a] A memory module operable with a memory controller of a host system, comprising:	**1.[a] A memory module** configured to fit into a corresponding slot of a host system **to operate with a memory controller of the host system**, the memory module comprising:
[1.b.1] a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,	**[1.d] a printed circuit board having** a first set of **edge connections for communicating address and control signals from the memory controller** of the host system, a second set of **edge connections for communicating data signals between the memory module and the memory controller** of the host system while the memory module operates in the first mode… **1.[a] A memory module configured to fit into a corresponding slot of a host system** to operate with a memory controller of the host system
[1.b.2] the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;	**[1.d]** a printed circuit board having **a first set of edge connections** for communicating address and control signals from the memory controller of the host system, **a second set of edge connections** for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, **and an error edge connection** coupled to the open drain output of the module controller.

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('623 Patent, EX1031, EX1034)**
[1.c.1] a module controller on the printed circuit board and	**1.[a] A memory module** … comprising: … **[1.b] a module controller**… … **[1.d] a printed circuit board** …
[1.c.2] configured to receive address and control signals associated with normal memory read or write operations via the first edge connections; and	**2.** …while the memory module is in the first mode, **the module controller receives** and processes **address and control signals corresponding to read or write commands** from the memory controller of the host system …. **[1.d]** a printed circuit board having **a first set of edge connections for communicating address and control signals** from the memory controller of the host system
[1.d.1] dynamic random access memory elements on the printed circuit board and	**2.** The memory module of claim 1, further comprising: a plurality of synchronous **dynamic random access memory elements**… **1.[a] A memory module** … comprising: … **[1.d] a printed circuit board** …

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('623 Patent, EX1031, EX1034)**
[1.d.2] configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and	**2.** … the module controller receives and processes **address and control signals corresponding to read or write commands** from the memory controller of the host system and **transmits processed address and control signals to the plurality** of synchronous **dynamic random access memory elements** **[1.d]** a printed circuit board having … **a second set of edge connections for communicating data signals between the memory module and the memory controller** of the host system while the memory module operates in the first mode....

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('623 Patent, EX1031, EX1034)
[1.e.1] wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;	**7.** … wherein **the module controller includes** a notification circuit comprising one or more **transistors each having an open drain coupled to the open drain output**. **8.** The memory module of claim 7, wherein the notification circuit generates the notification signal by driving a **gate** of each of the one or more transistors to a logic high level such that the open drain of each of the one or more **transistors provides a low impedance path to ground**[2] . **[1.d]** … **an error edge connection coupled to the open drain output** of the module controller.

[2] As explained above, *supra*, ¶¶46-54, a Skilled Artisan would have understood at the time that, in an open drain circuit, the field effect transistor's drain is coupled to the output, its source is coupled to ground, and its gate is used to control the state of the output.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('623 Patent, EX1031, EX1034)
[1.e.2] wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation; and	**7.** … wherein **the module controller includes** a notification circuit **9.** … wherein the notification circuit **generates the parity error signal by driving a gate of each of the one or more transistors** .... **[1.b]** … the parity error signal **indicating a parity error having occurred** in the memory module **while the memory module operates in the first mode** **2.** … **while the memory module is in the first mode**, the module controller **receives and processes** address and control signals corresponding to **read or write commands** from the memory controller of the host system

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('623 Patent, EX1031, EX1034)
[1.e.3] wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations.[3]	**[1.c]** … **the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode** … **8.** … wherein the notification circuit generates **the notification signal by driving a gate of each of the one or more transistors** … **2.** … **while the memory module is in the first mode**, the module controller **receives and processes** address and control signals corresponding to **read or write commands** from the memory controller of the host system

[3] As explained above, *supra* ¶¶61-71, the provisional does not provide § 112 support for this negative limitation, but a Skilled Artisan would have understood at the time that one obvious option was to initialize the memory module and memory elements during a training mode that does ***not*** use any normal read or write operations, *supra* ¶70.

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('623 Patent, EX1031, EX1034)**
2. The memory module of claim 1, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.	**8.** … wherein the notification circuit generates **the notification signal by driving a gate of each of the one or more transistors to a logic high level** such that **the open drain of each of the one or more transistors provides a low impedance path to ground**.[4]

[4] As explained above, *supra*, ¶¶46-54, a Skilled Artisan would have understood at the time that, when the field effect transistor in an open drain circuit is turned on by a "high" logic level at its gate, there is a low impedance (conductive) path to ground through the transistor which drives the open drain output to approach ground, corresponding to a low logic level; and when the field effect transistor is turned off by a "low" logic level at its gate, the path through the transistor has a high impedance (i.e., is non-conductive), so the open drain output is in a high impedance state.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('623 Patent, EX1031, EX1034)
3. The memory module of claim 2, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state.	**8.** … wherein the notification circuit **generates the notification signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground**.[5]
4. The memory module of claim 2, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.	**8.** … wherein the notification circuit generates **the notification signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground**.[6]
5. The memory module of claim 4, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.	**9.** … wherein the notification circuit generates **the parity error signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground**.

[5] See footnote 4 directly above.

[6] See footnote 4 above.

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('623 Patent, EX1031, EX1034)**
6. The memory module of claim 1, wherein the module controller comprises an integrated circuit that includes the transistor.	**6.** … wherein **the module controller comprises one or more integrated circuit**. **7.** … wherein **the module controller includes** a notification circuit comprising **one or more transistors** each having an open drain coupled to the open drain output.
7. The memory module of claim 1, wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.	**[1.c]** … the module controller generating a notification signal indicating at least one status of **one or more training sequences while the memory module is in the second mode** … **2.** … **while the memory module is in the first mode**, the module controller **receives** and processes address and control signals corresponding to **read or write commands from the memory controller** of the host system and transmits processed address and control signals **to the plurality of synchronous dynamic random access memory elements**. **[1.d]** a printed circuit board having **… a second set of edge connections for communicating data signals between the memory module and the memory controller** of the host system **while the memory module operates in the first mode**

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('623 Patent, EX1031, EX1034)**
8. The memory module of claim 1, wherein the second edge connections are not active during the operations associated with the one or more training sequences.	**[1.c]** … the module controller generating a notification signal indicating at least one status of **one or more training sequences while the memory module is in the second mode** … **2.** … **while the memory module is in the first mode**, the module controller **receives** and processes address and control signals corresponding to **read or write commands from the memory controller** of the host system and transmits processed address and control signals **to the plurality of synchronous dynamic random access memory elements**. **[1.d]** a printed circuit board having **… a second set of edge connections for communicating data signals between the memory module and the memory controller** of the host system **while the memory module operates in the first mode**

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('623 Patent, EX1031, EX1034)**
9. The memory module of claim 1, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input configured to receive the first signal, and a second input configured to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.	**10.** … wherein the **notification circuit** generates the notification signal **using one or more OR logic elements**. **9.** … wherein **the notification circuit generates the parity error signal by driving a gate of each of the one or more transistors** to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground. **8.** … wherein **the notification circuit generates the notification signal by driving a gate of each of the one or more transistors** to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.
10.[a] A method of operation in a host system having a memory controller, comprising:	*See* 024 claim element **1.[a]** above.
[10.b.1] at a memory module coupled to the memory controller,	*See* 024 claim element **1.[a]** above.
[10.b.2] the memory module including a printed circuit board,	*See* 024 claim element **[1.b.1]** above.
[10.c] a module controller on the printed circuit board, and	*See* 024 claim element **[1.c.1]** above.
[10.d] dynamic random access memory elements on the printed circuit board,	*See* 024 claim element **[1.d.1]** above.

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('623 Patent, EX1031, EX1034)**
[10.e.1] the printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,	*See* 024 claim element **[1.b.1]** above.
[10.e.2] the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections,	*See* 024 claim element **[1.b.2]** above.
[10.f] the module controller including a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;	*See* 024 claim element **[1.e.1]** above.
[10.g] receiving, at the module controller, address and control signals associated with one or more normal memory read or write operations from the memory controller via the first edge connections;	*See* 024 claim element **[1.c.2]** above.
[10.h] outputting or receiving data signals at the dynamic random access memory elements in accordance with the address and control signals, the data signals being associated with the one or more normal memory read or write operations and communicated with the memory controller via the second edge connections;	*See* 024 claim elements **[1.d.2] and [1.c.2]** above.
[10.i] applying a first signal to the gate of the transistor to indicate a parity error having occurred during one of the one or more normal memory read or write operations;	*See* 024 claim element **[1.e.2]** above.

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('623 Patent, EX1031, EX1034)**
[10.j] performing training operations associated with one or more training sequences when the dynamic random access memory elements are not accessed for any normal memory read or write operations; and	*See* 024 claim element **[1.e.3]** above.
[10.k] applying a second signal related to the one or more training sequences to the gate of the transistor while the memory module performs the training operations.	*See* 024 claim element **[1.e.3]** above.
11. The method of claim 10, wherein the error edge connection is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.	*See* 024 claim **2** above.
12. The method of claim 11, wherein the error edge connection is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state.	*See* 024 claim **3** above.
13. The method of claim 11, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.	*See* 024 claim **4** above.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('623 Patent, EX1031, EX1034)
14. The method of claim 13, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.	*See* 024 claim **5** above.
15. The method of claim 10, wherein the module controller comprises an integrated circuit that includes the transistor.	*See* 024 claim **6** above.
16. The method of claim 10, wherein the training operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.	*See* 024 claim **7** above.
17. The method of claim 10, wherein the second edge connections are not active during the training operations associated with the one or more training sequences.	*See* 024 claim **8** above.
18. The method of claim 10, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein applying the first signal to the gate of the transistor includes coupling the first input to the output, and applying the second signal to the gate of the transistor includes coupling the second input to the output.	*See* 024 claim **9** above.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('623 Patent, EX1031, EX1034)
19.[a] A memory module operable with a memory controller of a host system, comprising:	*See* 024 claim element **1.[a]** above.
[19.b.1] a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,	*See* 024 claim element **[1.b.1]** above.
[19.b.2] the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;	*See* 024 claim element **[1.b.2]** above.
[19.c.1] a module controller on the printed circuit board and	*See* 024 claim element **[1.c.1]** above.
[19.c.2] configured to receive from the memory controller via the first edge connections address and control signals associated with normal memory read or write operations; and	*See* 024 claim elements **[1.b.1]** and **[1.c.2]** above.
[19.d.1] dynamic random access memory elements on the printed circuit board and	*See* 024 claim element **[1.d.1]** above.
[19.d.2] configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and	*See* 024 claim element **[1.d.2]** above.
[19.e.1] wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;	*See* 024 claim element **[1.e.1]** above.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('623 Patent, EX1031, EX1034)
[19.e.2] wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation;	*See* 024 claim element **[1.e.2]** above.
[19.e.3] wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations;	*See* 024 claim element **[1.e.3]** above.
[19.f] wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground;	*See* 024 claim **5** above.
[19.g] wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to a low impedance state, and drives the gate of the transistor low so as to drive the error edge connection to a high impedance state;	*See* 024 claim **4** above.[7]

[7] While claim 4 refers to driving the output to "the low logic level," and claim element [19.g] instead refers to driving the output to a "low impedance state," both are describing the same operation. As explained above in detail, *supra* ¶¶46-54,

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('623 Patent, EX1031, EX1034)
[19.h] wherein the module controller comprises an integrated circuit that includes the transistor; and	*See* 024 claim **6** above.
[19.i] wherein the integrated circuit further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.	*See* 024 claim **9** above.
20. The memory module of claim 19, wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.	*See* 024 claim **7** above.

when the transistor of an open-drain circuit is in a "low impedance state," it is conducting so that the open drain output is driven to approach ground, corresponding to "the low logic level." *See, e.g.*, EX1089, pp.207-208 ("the transistor conducts and there is a low impedance path from the I/O pin to ground through the transistor").

154. The table below compares the claim limitations of the 024 Patent (reprinted below starting on page 321) to those in the ’218 Patent (reprinted below starting on page 333).

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims (’218 Patent, EX1095, EX1102)
1.[a] A memory module operable with a memory controller of a host system, comprising:	**1.[a]** A **memory module operable with a memory controller of a host system**, comprising:
[1.b.1] a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,	**[1.b] printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller**…
[1.b.2] the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;	**[1.b]** …**the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections**
[1.c.1] a module controller on the printed circuit board and	**[1.d] a module controller on the printed circuit board**…
[1.c.2] configured to receive address and control signals associated with normal memory read or write operations via the first edge connections; and	**[1.g.i]** wherein the module controller is **configured to receive via the second edge[8] connections the address and command signals associated with one or more memory read or write operations**…

[8] The “second edge” connections in the ’218 Patent (e.g., for address and command) correspond to the “first edge” connections in the 024 Patent, and the

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('218 Patent, EX1095, EX1102)
[1.d.1] dynamic random access memory elements on the printed circuit board and	**[1.c] dynamic random access memory elements on the printed circuit board**
[1.d.2] configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and	**[1.f]** wherein the memory module in the second mode is **configured to** perform one or more memory read or write operations not associated with the one or more training sequences by **communicating data signals via the first edge connections in response to address and command signals** received via the second edge connections

"first edge" connections in the '218 Patent (e.g., for data) correspond to the "second edge" connections in the 024 Patent.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('218 Patent, EX1095, EX1102)
[1.e.1] wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;	**[1.d]** … **the module controller having an open drain output coupled to the error edge connection** **3. …** the module controller **includes** a notification circuit comprising **one or more transistors each having an open drain coupled to the open drain output**. **4.** The memory module of claim 3, wherein the notification circuit is configured to drive the notification signal by driving a **gate** of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to **ground**[9].

[9] See footnote 2 above.

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('218 Patent, EX1095, EX1102)**
[1.e.2] wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation; and	**5.** … wherein the notification circuit is **configured to drive the parity error signal by driving the gate of each of the one or more transistors** ... **[1.h]** … **a signal indicating a parity error having occurred while the memory module is in the second mode** **[1.f]** wherein the memory module **in the second mode is configured to perform one or more memory read or write operations** not associated with the one or more training sequences …

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('218 Patent, EX1095, EX1102)
[1.e.3] wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations.[10]	**4.** … wherein the notification circuit is **configured to drive the notification signal by driving a gate of each of the one or more transistors** … **[1.i]** wherein the module controller is further configured to drive **a notification signal associated with the one or more training sequences** to the error edge connection via the open drain output **while the memory module is in the first mode.** **[1.e.ii]** wherein the memory module **in the first mode is configured to be trained with one or more training sequences**; **[1.f]** wherein the memory module **in the second mode is configured to perform one or more memory read or write operations** not associated with the one or more training sequences … **7**. The memory module of claim 1, wherein **the first edge connections are not active when the memory module is in the first mode and configured to be trained** with the one or more training sequences.

[10] See footnote 3 above.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('218 Patent, EX1095, EX1102)
2. The memory module of claim 1, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.	**4.** … wherein the notification circuit is configured to **drive the notification signal by driving** a gate of each of the one or more transistors **to a logic high level to provide a low impedance path between the open drain output to ground.**[11]
3. The memory module of claim 2, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state.	**4.** … wherein the notification circuit is configured **to drive the notification signal by driving** a gate of each of the one or more transistors **to a logic high level to provide a low impedance path between the open drain output to ground.**[12]

[11] As explained above, *supra*, ¶¶46-54, a Skilled Artisan would have understood at the time that, when the field effect transistor in an open drain circuit is turned on by a "high" logic level at its gate, there is a low impedance (conductive) path to ground through the transistor which drives the open drain output to approach ground, corresponding to a low logic level; and when the field effect transistor is turned off by a "low" logic level at its gate, the path through the transistor has a high impedance (i.e., is non-conductive), so the open drain output is in a high impedance state..

[12] See footnote 11 directly above.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('218 Patent, EX1095, EX1102)
4. The memory module of claim 2, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.	**4.** … wherein the notification circuit is configured **to drive the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.**[13]
5. The memory module of claim 4, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.	**5.** … wherein the notification circuit is configured **to drive the parity error signal by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.**
6. The memory module of claim 1, wherein the module controller comprises an integrated circuit that includes the transistor.	**2.** … wherein **the module controller comprises an integrated circuit**. **3.** … wherein **the module controller includes** a notification circuit comprising **one or more transistors** each having an open drain coupled to the open drain output.

[13] See footnote 11 above.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('218 Patent, EX1095, EX1102)
7. The memory module of claim 1, wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.	**[1.e.ii]** wherein the memory module **in the first mode is configured to be trained with one or more training sequences**; **[1.f]** wherein the memory module **in the second mode is configured to perform one or more memory read or write operations not associated with the one or more training sequences by communicating data signals via the first edge connections** in response to address and command signals received via the second edge connections; **7**. The memory module of claim 1, wherein **the first edge connections are not active when the memory module is in the first mode and configured to be trained** with the one or more training sequences.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('218 Patent, EX1095, EX1102)
8. The memory module of claim 1, wherein the second edge connections are not active during the operations associated with the one or more training sequences.	**[1.e.ii]** wherein the memory module **in the first mode is configured to be trained with one or more training sequences**; **[1.f]** wherein the memory module **in the second mode is configured to perform one or more memory read or write operations not associated with the one or more training sequences by communicating data signals via the first edge connections** in response to address and command signals received via the second edge connections; **7**. The memory module of claim 1, wherein **the first edge connections are not active when the memory module is in the first mode and configured to be trained** with the one or more training sequences.

9. The memory module of claim 1, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input configured to receive the first signal, and a second input configured to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.	**6.** … wherein the notification circuit is configured **to drive the notification signal using one or more OR logic elements.** **5.** … wherein the notification circuit is configured **to drive the parity error signal by driving the gate of each of the one or more transistors** to a logic high level to provide a low impedance path between the open drain output to ground. **[1.h]** wherein the module controller is further configured to output via the open drain output and the error edge connection **a signal indicating a parity error** having occurred while the memory module is **in the second mode;** **[1.f]** wherein the memory module **in the second mode is configured to perform one or more memory read or write operations** not associated with the one or more training sequences … **4.** … wherein the notification circuit is configured **to drive the notification signal by driving a gate of each of the one or more transistors** to a logic high level to provide a low impedance path between the open drain output to ground. **[1.i]** wherein the module controller is further configured to drive **a**

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('218 Patent, EX1095, EX1102)
	notification signal associated with the one or more training sequences to the error edge connection via the open drain output while the memory module is in the first mode.
10.[a] A method of operation in a host system having a memory controller, comprising:	**9.[a]** A **method** performed by a memory module **operating with a memory controller of the host system**
[10.b.1] at a memory module coupled to the memory controller,	**9.[a]** A method **performed by a memory module operating with a memory controller** of the host system
[10.b.2] the memory module including a printed circuit board,	**[9.b] the memory module including** dynamic random access memory elements on **a printed circuit board**
[10.c] a module controller on the printed circuit board, and	**[1.d]** a module controller on the printed circuit board …
[10.d] dynamic random access memory elements on the printed circuit board,	**[9.b]** the memory module including **dynamic random access memory elements on a printed circuit board**
[10.e.1] the printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,	**[9.c] the printed circuit board having edge connections that fit into a corresponding slot of a host system**, the edge connections including first edge connections via which the dynamic random access memory devices **communicate data with the memory controller**, second edge connections via which the memory module **receives address and command signals from the memory controller**…

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('218 Patent, EX1095, EX1102)**
[10.e.2] the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections,	**[9.c]** … **the edge connections including first edge connections**…, **second edge connections…, and an error edge connection in addition to the first edge connections and the second edge connections**…
[10.f] the module controller including a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;	*See* 024 claim element **[1.e.1]** above.
[10.g] receiving, at the module controller, address and control signals associated with one or more normal memory read or write operations from the memory controller via the first edge connections;	**[9.d] receiving from the memory controller address and command signals associated with one or more memory read or write operations**; **[9.c] … second edge connections** via which the memory module **receives address and command signals from the memory controller**…

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('218 Patent, EX1095, EX1102)**
[10.h] outputting or receiving data signals at the dynamic random access memory elements in accordance with the address and control signals, the data signals being associated with the one or more normal memory read or write operations and communicated with the memory controller via the second edge connections;	**[9.c]** … the edge connections including **first edge connections via which the dynamic random access memory devices communicate data with the memory controller**… **[9.d]** receiving from the memory controller **address and command signals associated with one or more memory read or write operations**; **[9.e] controlling the dynamic random access memory elements in accordance with the address and command signals**;
[10.i] applying a first signal to the gate of the transistor to indicate a parity error having occurred during one of the one or more normal memory read or write operations;	**[9.f] outputting** to the memory controller **via an open-drain output** coupled to the error edge connection **a signal indicating a parity error having occurred** in the memory module; and **11.** The method of claim 10, wherein **driving the signal indicating the parity error comprises driving the gate of each of the one or more transistors** to a logic high level to provide a low impedance path from the open drain output to ground.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('218 Patent, EX1095, EX1102)
[10.j] performing training operations associated with one or more training sequences when the dynamic random access memory elements are not accessed for any normal memory read or write operations; and	**[9.g] training with one or more training sequences while the first edge connections are not active** **[9.c]** … the edge connections including **first edge connections via which the dynamic random access memory devices communicate data with the memory controller**…
[10.k] applying a second signal related to the one or more training sequences to the gate of the transistor while the memory module performs the training operations.	**[9.h] driving a notification signal associated with the one or more training sequences** to the memory controller via the open drain output and the error edge connection **14.** … wherein **the notification signal indicates a status of the one or more training sequences**.
11. The method of claim 10, wherein the error edge connection is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.	**10.** … **driving the notification signal comprises driving a gate of each of one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground,**[14] **the one or more transistors each having an open drain coupled to the open drain output.**

[14] See footnote 11 above.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('218 Patent, EX1095, EX1102)
12. The method of claim 11, wherein the error edge connection is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state.	**10.** … **driving the notification signal comprises driving a gate of each of one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground,**[15] **the one or more transistors each having an open drain coupled to the open drain output.**
13. The method of claim 11, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.	**10.** … **driving the notification signal comprises driving a gate of each of one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground,**[16] **the one or more transistors each having an open drain coupled to the open drain output.**
14. The method of claim 13, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.	**11.** … wherein **driving the signal indicating the parity error comprises driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground**.
15. The method of claim 10, wherein the module controller comprises an integrated circuit that includes the transistor.	*See* 024 claim **6** above.

[15] See footnote 11 above.

[16] See footnote 11 above.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('218 Patent, EX1095, EX1102)
16. The method of claim 10, wherein the training operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.	**[9.g] training with one or more training sequences while the first edge connections are not active** **[9.c]** … the edge connections including **first edge connections via which the dynamic random access memory devices communicate data with the memory controller**…
17. The method of claim 10, wherein the second edge connections are not active during the training operations associated with the one or more training sequences.	**[9.g] training with one or more training sequences while the first edge connections are not active** **[9.c]** … the edge connections including **first edge connections via which the dynamic random access memory devices communicate data with the memory controller**…
18. The method of claim 10, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein applying the first signal to the gate of the transistor includes coupling the first input to the output, and applying the second signal to the gate of the transistor includes coupling the second input to the output.	*See* 024 claim **9** above.
19.[a] A memory module operable with a memory controller of a host system, comprising:	*See* 024 claim element **1.[a]** above.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('218 Patent, EX1095, EX1102)
[19.b.1] a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,	*See* 024 claim element **[1.b.1]** above.
[19.b.2] the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;	*See* 024 claim element **[1.b.2]** above.
[19.c.1] a module controller on the printed circuit board and	*See* 024 claim element **[1.c.1]** above.
[19.c.2] configured to receive from the memory controller via the first edge connections address and control signals associated with normal memory read or write operations; and	*See* 024 claim elements **[1.b.1]** and **[1.c.2]** above.
[19.d.1] dynamic random access memory elements on the printed circuit board and	*See* 024 claim element **[1.d.1]** above.
[19.d.2] configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and	*See* 024 claim element **[1.d.2]** above.
[19.e.1] wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;	*See* 024 claim element **[1.e.1]** above.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('218 Patent, EX1095, EX1102)
[19.e.2] wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation;	*See* 024 claim element **[1.e.2]** above.
[19.e.3] wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations;	*See* 024 claim element **[1.e.3]** above.
[19.f] wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground;	*See* 024 claim **5** above.
[19.g] wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to a low impedance state, and drives the gate of the transistor low so as to drive the error edge connection to a high impedance state;	*See* 024 claim **4** above.[17]

[17] While claim 4 refers to driving the output to "the low logic level," and claim element [19.g] instead refers to driving the output to a "low impedance state," both are describing the same operation. As explained above in detail, *supra* ¶¶46-54,

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('218 Patent, EX1095, EX1102)
[19.h] wherein the module controller comprises an integrated circuit that includes the transistor; and	*See* 024 claim **6** above.
[19.i] wherein the integrated circuit further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.	*See* 024 claim **9** above.
20. The memory module of claim 19, wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.	*See* 024 claim **7** above.

when the transistor of an open-drain circuit is in a "low impedance state" (conductive), the open drain output is driven to approach ground, corresponding to "the low logic level." *See, e.g.*, EX1089, pp.207-208 ("the transistor conducts and there is a low impedance path from the I/O pin to ground through the transistor").

155. The table below compares the claim limitations of the 024 Patent (reprinted below starting on page 321) to those in the '595 Patent (reprinted below starting on page 338).

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)**
1.[a] A memory module operable with a memory controller of a host system, comprising:	**1.[a] A memory module operable with a memory controller of a host system**, comprising:
[1.b.1] a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,	**[1.b] a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller**…
[1.b.2] the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;	**[1.b]** … **the edge connections including first edge connections…, second edge connections…, and an error edge connection in addition to the first edge connections and the second edge connections**;
[1.c.1] a module controller on the printed circuit board and	**[1.d] a module controller on the printed circuit board**…
[1.c.2] configured to receive address and control signals associated with normal memory read or write operations via the first edge connections; and	**[1.f.i]** wherein **the module controller is configurable to receive via the second edge[18] connections the address and control signals associated with the one or more normal memory read or write operations,**…

[18] The "second edge" connections in the '595 Patent (e.g., for address and control) correspond to the "first edge" connections in the 024 Patent, and the "first

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)**
[1.d.1] dynamic random access memory elements on the printed circuit board and	**[1.c] dynamic random access memory elements on the printed circuit board**;
[1.d.2] configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and	**[1.f.ii]** wherein the dynamic random access memory elements are **configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals**,
[1.e.1] wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;	**3.** The memory module of claim 1, **wherein the module controller includes** a notification circuit comprising **a transistor having an open drain coupled to the open drain output and source coupled to the ground**. **4.** The memory module of claim 3, wherein the module controller is configurable to drive a **gate** of the transistor high so as to drive open drain output and the error edge connection to **ground**, or to drive the **gate** of the transistor low so as to drive the open drain output and the error edge connection to the high impedance state. **[1.d]** … the module controller having **an open drain output coupled to the error edge connection**

edge" connections in the '595 Patent (e.g., for data) correspond to the "second edge" connections in the 024 Patent.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)
[1.e.2] wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation; and	**5.** … **wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor** high to provide a low impedance path between the open drain output and the ground. **[1.f.iii] wherein the module controller is** further **configurable to output** via the open drain output and the error edge connection **a signal indicating a parity error having occurred** while the memory module is **in the first mode**; **[1.e.ii]** wherein the memory module **in the first mode** is configurable **to perform one or more normal memory read or write operations** …
[1.e.3] wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations[19].	**7.** … **wherein the module controller is configurable to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal** … **[1.e.iii]** wherein **the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations**, and

[19] See footnote 3 above.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)
2. The memory module of claim 1, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.	**7.** The memory module of claim 3, wherein the module controller is configurable to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal so as **to drive the open drain output from the high impedance state to ground or from ground to the high impedance state.** **[1.g]** wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences **by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state**.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)
3. The memory module of claim 2, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state.	**7.** The memory module of claim 3, wherein the module controller is configurable to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal so as **to drive the open drain output from the high impedance state to ground or from ground to the high impedance state.** **[1.g]** wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences **by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state**.

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)**
4. The memory module of claim 2, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.	**7.** The memory module of claim 3, wherein the module controller is configurable to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal so as **to drive the open drain output from the high impedance state to ground or from ground to the high impedance state.** **[1.g]** wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences **by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state**.
5. The memory module of claim 4, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.	**5.** … wherein the module controller is configurable **to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and the ground**.

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)**
6. The memory module of claim 1, wherein the module controller comprises an integrated circuit that includes the transistor.	**2.** … **wherein the module controller comprises an integrated circuit**. **3.** … **wherein the module controller includes** a notification circuit comprising **a transistor** having an open drain coupled to the open drain output and source coupled to the ground.
7. The memory module of claim 1, wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.	**9.** The memory module of claim 1, wherein the memory module in the second mode is **configurable to perform the operations related to the one or more training sequences without communicating data signals via the first edge connections while the memory module is in the second mode**. **[1.e.iii]** wherein the memory module **in the second mode is not accessed by the memory controller for normal memory read or write operations…**
8. The memory module of claim 1, wherein the second edge connections are not active during the operations associated with the one or more training sequences.	**8.** … wherein **the second edge connections** include one or more pins that **are not active while the memory module is in the second mode.** **[1.e.iv]** wherein the memory module **in the second mode** is configurable **to perform operations related to one or more training sequences**

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)**
9. The memory module of claim 1, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input configured to receive the first signal, and a second input configured to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.	**6.** … wherein the notification circuit further **includes a multiplexor or a logic circuit having a output coupled to a gate of the transistor and configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences** **[1.e.ii]** wherein the memory module **in the first mode is configurable to perform one or more normal memory read or write operations** …
10.[a] A method of operation in a host system having a memory controller, comprising:	**17.[a] A method**, comprising: **[17.b]** at a memory module coupled with **a memory controller of a host system**…
[10.b.1] at a memory module coupled to the memory controller,	**[17.b]** at a memory module coupled with **a memory controller of a host system**…
[10.b.2] the memory module including a printed circuit board,	**[17.b]** …**the memory module including a printed circuit board**…
[10.c] a module controller on the printed circuit board, and	**[20.a]** … wherein **the memory module includes a notification circuit …** **3.** … wherein **the module controller includes a notification circuit** …
[10.d] dynamic random access memory elements on the printed circuit board,	**[17.b]** …, the memory module further including **dynamic random access memory elements on the printed circuit board**;

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)**
[10.e.1] the printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,	**[17.b]** …a **printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller**…
[10.e.2] the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections,	**[17.b]**…**the edge connections including first edge connections**…, **second edge connections**…, **and an error edge connection in addition to the first edge connections and the second edge connections**…
[10.f] the module controller including a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;	**20.[a]** … wherein the memory module includes a **notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to ground**, **20.[b]** … wherein outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module comprises driving a **gate** of the transistor high to provide a low impedance path between the open drain output and **ground**, **[17.c]** …**an open drain output coupled to the error edge connection**…

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)
[10.g] receiving, at the module controller, address and control signals associated with one or more normal memory read or write operations from the memory controller via the first edge connections;	**[17.c] receiving via the second edge connections address and control signals associated with one or more memory read or write operations**;… **[1.f.i]** … wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the **one or more normal memory read or write operations**
[10.h] outputting or receiving data signals at the dynamic random access memory elements in accordance with the address and control signals, the data signals being associated with the one or more normal memory read or write operations and communicated with the memory controller via the second edge connections;	**[17.c]** …**controlling the dynamic random access memory elements to communicate data signals corresponding to the one or more memory read or write operations via the first edge connections in response to the address and control signals**;… **[1.f.i]** … wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the **one or more normal memory read or write operations**

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)**
[10.i] applying a first signal to the gate of the transistor to indicate a parity error having occurred during one of the one or more normal memory read or write operations;	**[17.c]** …**outputting via an open drain output** coupled to the error edge connection **a signal indicating a parity error having occurred in the memory module while the memory module is being accessed by the memory controller for a memory read or write operation**; **[20.b]** … wherein **outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module comprises driving a gate of the transistor high** to provide a low impedance path between the open drain output and ground, **[1.f.i]** … wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the **one or more normal memory read or write operations**
[10.j] performing training operations associated with one or more training sequences when the dynamic random access memory elements are not accessed for any normal memory read or write operations; and	**[17.d] performing operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations**… **[1.e.iii]** … wherein the memory module in the second mode is **not accessed by the memory controller for normal memory read or write operations**

Listing of Challenged Claims (024 Patent)	**Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)**
[10.k] applying a second signal related to the one or more training sequences to the gate of the transistor while the memory module performs the training operations.	**[17.d] performing operations related to one or more training sequences** … and **outputting** to the memory controller **via the open drain output** and the error edge connection **open drain signals related to the one or more training sequences and unrelated to any memory read or write operation** **[20.c]** wherein **outputting the open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation comprises** driving the gate of the transistor **to drive the open drain output from a high impedance state to ground and from ground to the high impedance state**.
11. The method of claim 10, wherein the error edge connection is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.	**[20.c]** wherein **outputting the open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation comprises** driving the gate of the transistor **to drive the open drain output from a high impedance state to ground and from ground to the high impedance state**.
12. The method of claim 11, wherein the error edge connection is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state.	**[20.c]** wherein **outputting the open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation comprises** driving the gate of the transistor **to drive the open drain output from a high impedance state to ground and from ground to the high impedance state**.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)
13. The method of claim 11, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.	**[20.c]** wherein **outputting the open-drain signals related to the one or more training sequences** and unrelated to any memory read or write operation **comprises driving the gate of the transistor to drive the open drain output from a high impedance state to ground and from ground to the high impedance state**.
14. The method of claim 13, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.	**[20.c]** wherein **outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module comprises driving a gate of the transistor high to provide a low impedance path between the open drain output and ground**
15. The method of claim 10, wherein the module controller comprises an integrated circuit that includes the transistor.	**2.** … **wherein the module controller comprises an integrated circuit**. **20.[a]** … wherein **the memory module includes a notification circuit having a transistor …**

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)
16. The method of claim 10, wherein the training operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.	**[17.d] performing operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations…** **[1.e.iii]** … wherein the memory module in the second mode is **not accessed by the memory controller for normal memory read or write operations**
17. The method of claim 10, wherein the second edge connections are not active during the training operations associated with the one or more training sequences.	**18.** The method of claim 17, **wherein the second edge connections** include one or more **pins that are not active while the memory module is trained with the one or more training sequences**.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)
18. The method of claim 10, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein applying the first signal to the gate of the transistor includes coupling the first input to the output, and applying the second signal to the gate of the transistor includes coupling the second input to the output.	**13.** The memory module of claim 12, wherein **the notification circuit further includes a multiplexor or a logic circuit having an output coupled to the gate of the transistor and configurable to drive the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences**
19.[a] A memory module operable with a memory controller of a host system, comprising:	*See* 024 claim element **1.[a]** above.
[19.b.1] a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,	*See* 024 claim element **[1.b.1]** above.
[19.b.2] the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;	*See* 024 claim element **[1.b.2]** above.
[19.c.1] a module controller on the printed circuit board and	*See* 024 claim element **[1.c.1]** above.
[19.c.2] configured to receive from the memory controller via the first edge connections address and control signals associated with normal memory read or write operations; and	*See* 024 claim elements **[1.b.1] and [1.c.2]** above.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)
[19.d.1] dynamic random access memory elements on the printed circuit board and	*See* 024 claim element **[1.d.1]** above.
[19.d.2] configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and	*See* 024 claim element **[1.d.2]** above.
[19.e.1] wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;	*See* 024 claim element **[1.e.1]** above.
[19.e.2] wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation;	*See* 024 claim element **[1.e.2]** above.
[19.e.3] wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations;	*See* 024 claim element **[1.e.3]** above.

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)
[19.f] wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground;	*See* 024 claim **5** above.
[19.g] wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to a low impedance state, and drives the gate of the transistor low so as to drive the error edge connection to a high impedance state;	*See* 024 claim **4** above.[20]
[19.h] wherein the module controller comprises an integrated circuit that includes the transistor; and	*See* 024 claim **6** above.

[20] While claim 4 refers to driving the output to "the low logic level," and claim element [19.g] instead refers to driving the output to a "low impedance state," both are describing the same operation. As explained above in detail, *supra* ¶¶46-54, when the transistor of an open-drain circuit is in a "low impedance state" (conductive), the output is driven to approach ground, corresponding to "the low logic level." *See*, *e.g.*, EX1089, pp.207-208 ("the transistor conducts and there is a low impedance path from the I/O pin to ground through the transistor").

Listing of Challenged Claims (024 Patent)	Listing of Invalidated Claims ('595 Patent, EX1097, EX1103)
[19.i] wherein the integrated circuit further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.	*See* 024 claim **9** above.
20. The memory module of claim 19, wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.	*See* 024 claim **7** above.

F. Construction of terms used in the 024 Patent claims

156. I understand that in an *inter partes* review proceeding the claims of the patent are to be given their ordinary and customary meaning in view of the specification and file history (i.e., the meaning that the term in question would have to a Skilled Artisan).

157. I also understand that where a patent application provides an explicit definition of a claim term in the specification, that definition may control the interpretation of that term in the claim.

158. I also understand that if no explicit definition is given to a term in the patent specification, the claim terms must be evaluated using the ordinary meaning of the words being used in those claims, evaluated from the perspective of a Skilled Artisan.

159. I understand that in its Final Written Decision for the '218 Patent, the PTAB declined to construe Samsung's proposed terms, which included "*memory read or write operations*," "*mode*," and "*training sequence*," giving these terms their plain and ordinary meaning. EX1102,12-15. I also understand that in its Final Written Decision for the '595 Patent, the PTAB declined to construe Samsung's proposed terms, which included "*memory read or write operations*," "*mode*," "*training sequence*," and "*notification signal associated with the [one or more training sequences]*" / "*information related to the [one or more training sequences]*" / "*open-drain signals related to the [one or more training sequences]*," giving these terms their plain and ordinary meaning. EX1103,12-15. I also understand that in the related district court case, Case No. 6:20-CV-00194, in the Western District of Texas, the Court construed certain terms in the '218 and '595 Patents:

Claim Term in '218 and '595 Patents	**District Court's Construction**
"mode" / "first mode" / "second mode"	Plain and ordinary meaning
"one or more training sequences"	"Training sequences" means "operations in a particular order for preparing a memory system to perform its intended functions"
"notification signal associated with the [one or more training sequences]"	See above for construction of "one or more training sequences." The rest of the phrase has its plain and ordinary meaning, which does not encompass polling.
"information related to the [one or more training sequences]"	See above for construction of "one or more training sequences." The rest of the phrase has its plain and ordinary meaning, which does not encompass polling.
"open-drain signals related to the [one or more training sequences]"	See above for construction of "one or more training sequences." The rest of the phrase has its plain and ordinary meaning, which does not encompass polling.

EX1061, 2-3. I have applied the PTAB's conclusion in my analysis of the challenged claims below, giving these terms their plain and ordinary meaning. However, even if I applied the constructions issued by the Western District of Texas, my analysis and conclusions would remain the same.

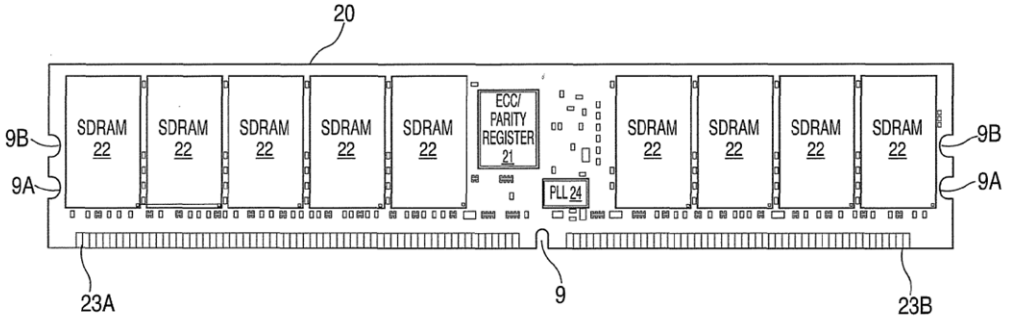
IV. OVERVIEW OF THE PRIOR ART

160. Below is an overview of the primary prior art references that I considered when analyzing the validity of the claims of the 024 Patent.

A. U.S. Patent Publication No. 2008/0098277 to Hazelzet (EX1014)

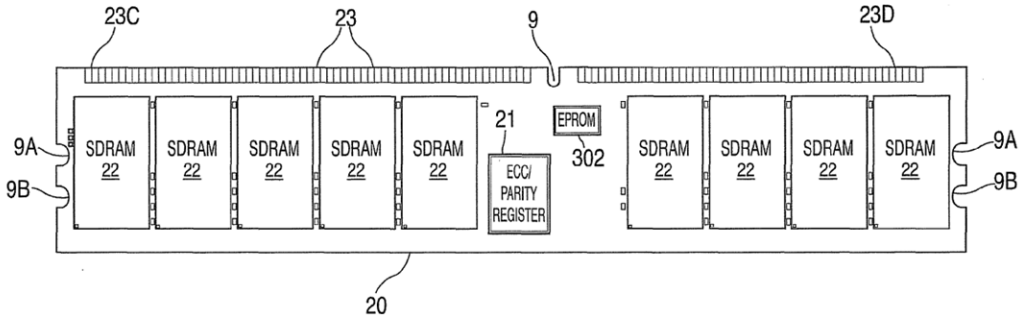
161. U.S. Patent Publication No. 2008/0098277 to Hazelzet ("Hazelzet") (EX1014) was filed on October 23, 2006 and published on April 24, 2008. I understand that Hazelzet is prior art to the 024 Patent. Hazelzet is entitled "High Density High Reliability Memory Module With Power Gating and a Fault Tolerant Address and Command Bus" and discloses such functionality. EX1014 (Hazelzet) at Title. Therefore, Hazelzet is directed to memory modules that have high density, high reliability, and can save power. *Id*., Abstract.

162. Hazelzet discloses memory modules that can include up to four ranks of memory devices arranged in a registered DIMM format that is consistent with JEDEC standards. EX1014, [0039-40], [0044], FIGS. 3A-3D (FIG. 3C-3D reproduced below, showing stacked arrangement of memory devices), [0008], [0014], [0016]. Hazelzet discloses that its modules can be initialized in a number of different ways, including those described in related JEDEC standards. EX1014, [0123]-[0125].



FRONT SIDE OF DIMM - 4 HIGH STACK

FIG. 3C



BACK SIDE OF DIMM - 4 HIGH STACK

FIG. 3D

163. Hazelzet's modules can operate in an "ECC mode" or a "parity mode." EX1014 (Hazelzet) at ¶¶[0064],[0069]-[0070]; *see also id*. at FIG. 8 (reproduced below), ¶¶[0020], [0022], [0049], [0059]-[0062], [0072], [0075], [0081], [0101]-[0103], [0106]-[0107], [0109].

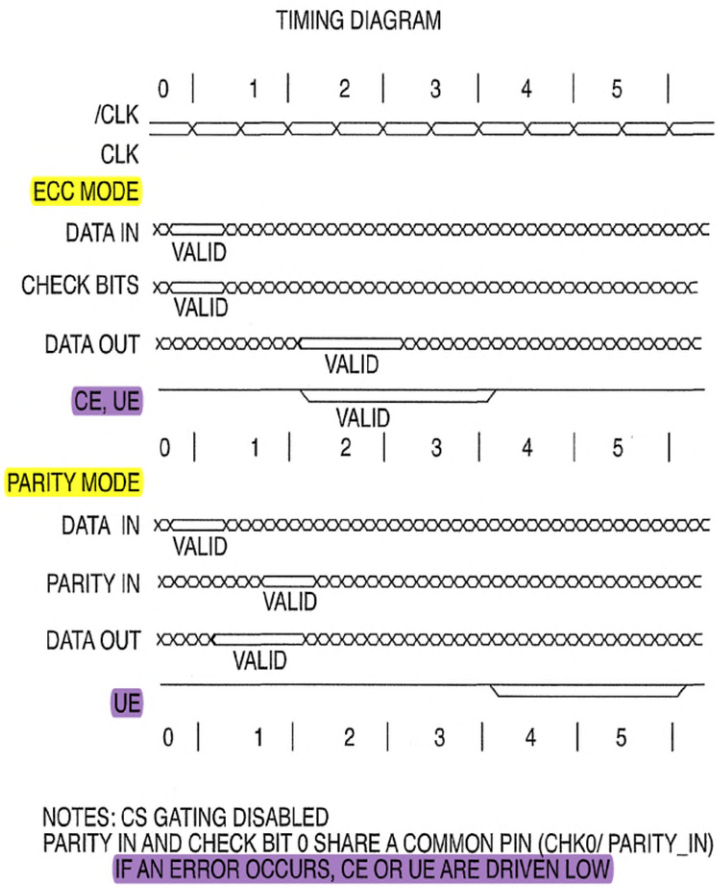


FIG. 8

164. Hazelzet explains that the "ECC mode" is a mode that allows the host system to detect and/or correct "correctable errors" or "uncorrectable errors" (e.g., "double bit error"). EX1014 (Hazelzet) at ¶[0069] ("This ECC logic will ... correct all single bit errors and detect all double bit errors present on the twenty-two chip select gated data inputs."). In the "ECC mode," the detected correctable errors would be output through an "/Error (CE)" output pin and any uncorrectable errors (e.g., double bit errors) would be reported through an "/Error (UE)" output pin.

EX1014 (Hazelzet) at ¶[0069]. Hazelzet explains that these two outputs (i.e., CE and UE) are "open-drain outputs." EX1014 (Hazelzet) at ¶¶[0072], [0109].

165. Hazelzet further explains that the "parity operating mode" is a mode that allows the host system to "interrogate the device to determine the error condition" of the memory module. EX1014 (Hazelzet) at ¶[0064] ("A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition."). Hazelzet further explains that such "error condition" in the "parity mode" is also reported to the host "via the Uncorrectable Error (UE) line" when the memory module is in the "parity mode," EX1014 (Hazelzet) at ¶[0070], which is the open-drain output that is used to report the uncorrectable errors in the "ECC mode." EX1014 (Hazelzet) at ¶¶[0072], [0109].

166. Hazelzet further explains that its memory module is in the "ECC mode" when the "/ECC Mode" signal becomes "low," EX1014 (Hazelzet) at ¶[0069], and that the memory module switches to the "parity mode" when the "/ECC Mode" signal becomes "high." EX1014 (Hazelzet) at ¶[0070].

B. JEDEC LRDIMM Proposal (EX1015)

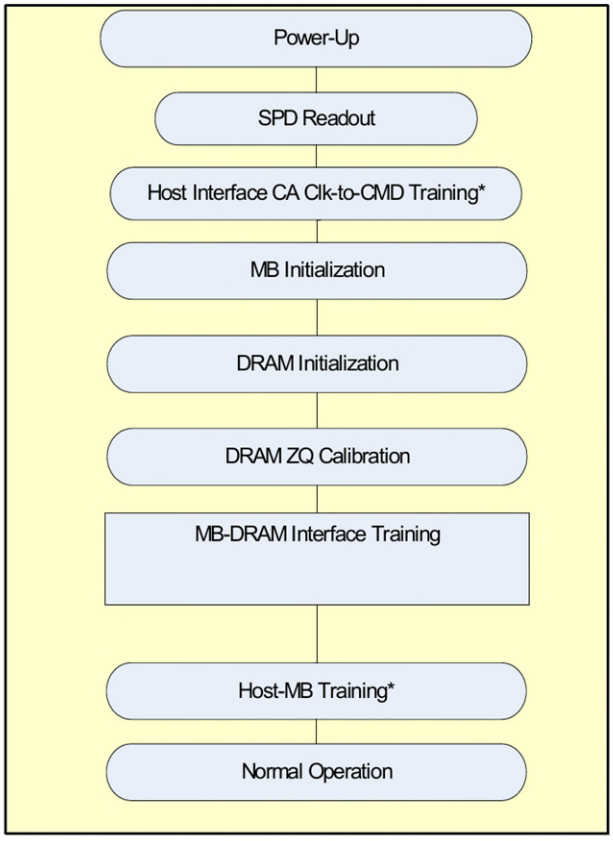
167. The JEDEC reference (EX1015) is a proposal disclosing modifications to the Memory Buffer ("module controller") functionality of a DDR3 LRDIMM memory module (Load Reduced DIMM) standards which were

under development at the time of the alleged invention by the standard developing organization called JEDEC.

168. I understand that Netlist disputed whether JEDEC proposals, like the DDR3 LRDIMM proposal were publicly available as printed publications. However, as I explained above, *supra*, ¶¶38-41, a Skilled Artisan would have been familiar with the content of the JEDEC proposals at the time. *See, e.g.,* EX1008, p.22 (the provisional describing "the recent proposal in JEDEC for … Load Reduced DIMM… the LR-DIMM proposal requires … the current LR-DIMM proposal"). Netlist's expert agreed. EX1077 (Murphy Dep.), 55:8-56:11 ("Q. In your opinion would a person of ordinary skill in the art have known about the contents of presentations and proposals to JEDEC relevant to memory modules and memory devices … THE WITNESS: Yes, I believe that would have been the case …"). I understand that Netlist's expert also agreed that a Skilled Artisan would have known about the content of presentations and proposals specifically relevant to the LRDIMM standards. *Id.* 57:7-25 ("In your opinion would a person of ordinary skill in the art have known about the contents of presentations and proposals to JEDEC relevant to LR-DIMM memory modules … THE WITNESS: As I said previously, yes, I believe they would…"). Thus, there seems to be no dispute that the content of the JEDEC LRDIMM proposal (EX1015) was known to a Skilled Artisan.

169. In particular, JEDEC proposed to add an initialization mode to train the Memory Buffer of the LR-DIMM module that included training sequences and corresponding handshaking methods, including the ability to output notification signals providing the status of those sequences. EX1015, pp.1, 3, 8. The proposed training in the initialization mode specifically included Host-MB Training and MB-DRAM Training using training sequences such as Write Leveling, Read Enable Training, and Read/Write DQ/DQS training the interface between the Memory Buffer and the DRAMs of the module. EX1015, pp.3-4, Fig. 1 (reproduced below).

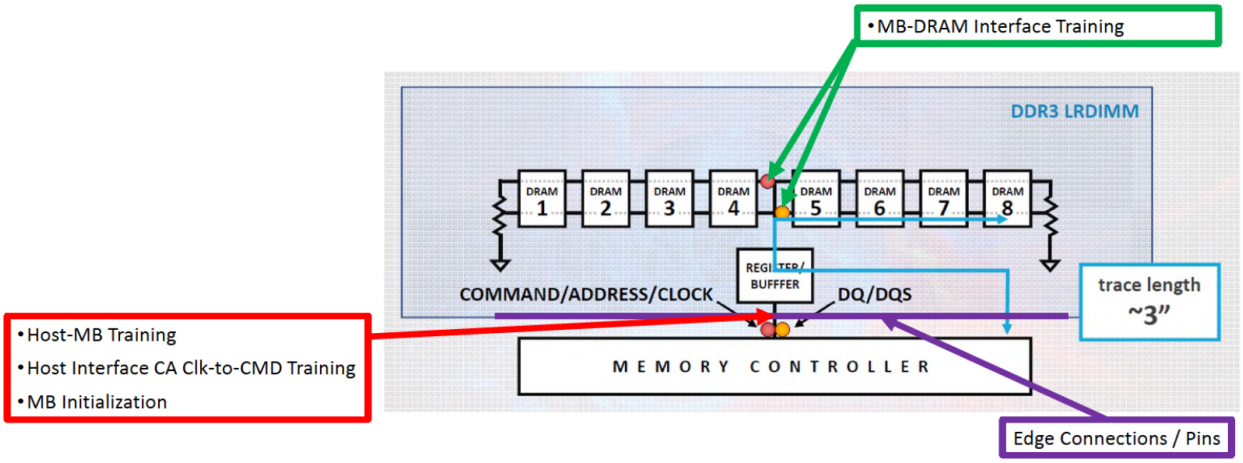
Figure 1 — Initialization Overview



* This step is optional for the MB but may be done by some platforms

Samsung Electronics Co., Ltd.
Ex. 1003, p. 147

I understand that Netlist's expert has agreed that the following demonstrative illustrates the components involved in the different types of training:



EX1081 (annotating EX1079, 10); EX1077, 131:4-133:3. JEDEC also states that "[n]o DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete...." EX1015, 8.

170. With respect to the MB-DRAM Training, JEDEC discloses that it is done by the buffer and the "Host can wait … or periodically poll the buffer … or wait for ERROUT#. *Id.*, 3, 8 ("training completion can be signaled by the assertion of ERROUT#"). A Skilled Artisan would have understood that "ERROUT#" refers to the parity error out pin on the proposed JEDEC standard LRDIMM module of the time. Specifically, a Skilled Artisan would have understood other aspects of the DDR3 LRDIMM standard development at the time, including those described in the proposed "DDR3 LRDIMM Design

Specification." EX1036, 2. Much like Hazelzet's registered memory modules (RDIMM), the DDR3 LRDIMM memory modules at the time of the alleged invention included a PCB with DRAMs and various edge connections for data signals, address and command signals, and an ErrOut_n pin that, during normal operation, was used to notify the memory controller of parity errors on the Address and Command bus through the use of an open-drain output. EX1036, 5-10, *see, e.g.*, at 9 (reproduced below).

ErrOut_n	OUT (open drain)		Parity error detected on the Address and Command bus. A resistor may be connected from ErrOut_n bus line to V_{DD} on the system planar to act as a pull up.

A Skilled Artisan would have understood that the LRDIMM Design Specification's ErrOut_n and the JEDEC proposal's ERROUT# referred to the same output/pin on the DDR3 LRDIMMs of the time. *See also* EX1044, 1 (October 2008 TI DDR3 buffer datasheet that discloses ERROROUT# open drain parity error signal).

171. The JEDEC proposal therefore discloses an initialization mode that includes one or more training sequences for a memory module that buffers address, command and data signals, such as a DDR3 LRDIMM. During initialization, the module can be made to perform operations related to various training sequences and outputs a notification signal indicating status (e.g., completion) of the training

sequences over the same open drain output used to report parity errors in a normal mode of operation.

C. U.S. Patent No. 8,139,430 to Buchmann (EX1016)

172. U.S. Patent No. 8,139,430 to Buchmann et al. ("Buchmann"), the application for which was filed on July 1, 2008, issued on March 20, 2012. I understand that Buchmann is prior art to the 024 Patent. Buchmann is entitled "Power-On Initialization and Test for a Cascade Interconnect Memory System." EX1016 (Buchmann) at Title.

173. Buchmann discloses power-on initialization of exemplary memory modules (110) where each memory module has a memory buffer (MB, 106) for buffering data, command, and address to and from the memory devices (108). EX1016, FIGS. 1-2, 4:5-50.

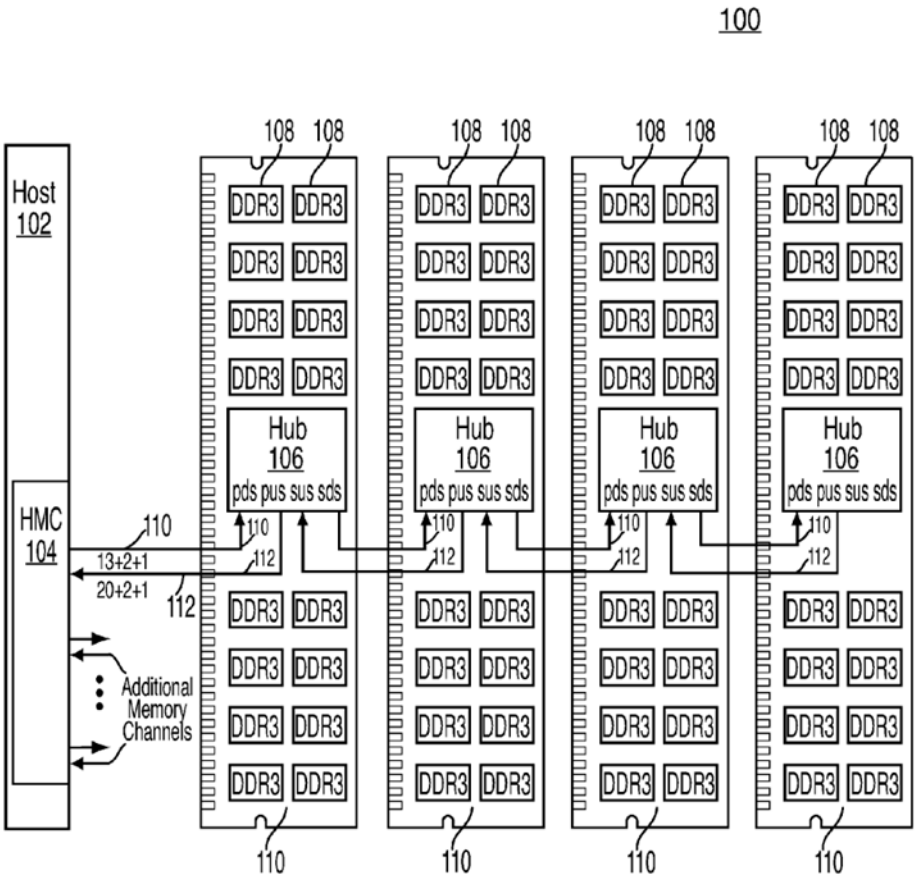


FIG. 1

174. Buchmann discloses two modes of operation (i.e., "SBC mode" and "high-speed mode"), EX1016 (Buchmann) at Abstract, 1:39-44. The "high-speed mode" is a mode of operation "at a high nominal speed." EX1016 (Buchmann) at 14:67-15:2. On the other hand, the "SBC mode" is a mode of operation "at a reduced rate" of communication. EX1016 (Buchmann) at 14:65-67. According to Buchmann, before the high-speed bus between the memory controller and the memory module (e.g., downstream bus 110 and upstream bus 112 in FIG. 1) can be used reliably to communicate with the memory modules, the memory module

operates in the SBC mode to train the high-speed bus. EX1016 (Buchmann) at 14:5-8, 3:52-54, 3:64-67; *see also id*. at FIG. 1, 4:11-14.

175. In particular, Buchmann discloses executing training and/or initialization sequences in its "SBC mode," which is also referred to as an "error correcting code protected quasi-static bit communication" mode. EX1016 (Buchmann) at 14:1-15:15; *see also id*. at 3:52-54, 5:6-22, 4:51-12:59. For example, the training and/or initialization sequences taught by Buchmann include "TS0-clock detection, test and repair; TS1-static configuration and calibration; TS2-downstream lane training and repair; TS3-upstream lane training and repair; TS4 packet training; TS5-initiate valid packets; TS6-frame lock; and TS7-read data latency calculation and inter-channel de-skew," EX1016 (Buchmann) at 5:40-46, FIG. 3.

176. As an example, training sequence TS0 involves "clock detection and repair," EX1016 (Buchmann) at 5:51-53, which is a training of the clock signal in the SBC mode. EX1016 (Buchmann) at 5:66-6:22. In particular, the memory buffer MB ("a module controller") enters the TS0 state and initiates the training sequence TS0 of Buchmann (an example of a "training sequence") after receiving the SBC command "TS0_pdsck" from the host. EX1016 (Buchmann) at 6:1-50 (Table 1 and Table 2, explaining that the "TS0_pdsck" command "causes the downstream receiver logic to enter the TS0 state, reset its memory channel PLLs

and select the PDSCK clock as the MB reference clock" and that the "Host/MB drives downstream bus clock on SDSCK lane and issues TS0_pdsck SBC."). Further, during the TS0 training sequence, the memory module generates and outputs various notification signals providing information about the training sequence to the memory controller of the host system, including the status of the TS0 training sequence (e.g., "TS_done," which notifies the host that the TS0 training is "done."). EX1016 (Buchmann) at FIG. 4, 5:51-7:2 & Tables 1-2.

177. As another example, training sequence TS3 involves "upstream lane training" and is "used to perform upstream data lane training," EX1016 (Buchmann) at 8:24-26, in the SBC mode, EX1016 (Buchmann) at 8:27-47 (showing the SBC commands used during TS3 in Table 5). In particular, the memory buffer MB ("a module controller") initiates the "upstream lane training" TS3 of Buchmann (another example of a "training sequence") after correction/forwarding of the SBC command "TS3_annc" (*i.e.*, "TS3a announcement SBC") from the host. EX1016 (Buchmann) at 8:24-27 ("TS3 ... immediately follows TS2 with the host responsible for sending the TS3a announcement SBC."), Table 5 ("TS3_annc: This command announces the beginning of TS3a. This SBC is corrected and forwarded by MBs in the memory channel."). Further, during the "upstream lane training" sequence TS3, the memory module generates and outputs various notification signals providing

information about the training schemes to the memory controller of the host system, including the status of the TS3 training sequence, such as "TS3_ack," which indicates that all downstream MBs have returned the TS3a_ack SBC, and "TS_done," which notifies the host that the TS3 training sequence is "done." EX1016, FIG. 6, 8:24-9:18 & Tables 5-6.

178. Buchmann discloses that his training operations may be initiated by power on, reset or initial program load operations, and "may be entered at different states," which a person of ordinary skill would understand to mean that this system was configurable to carry out some or all of the disclosed training. EX1016, 3:67-4:4, 4:51-5:12, FIG. 3. Moreover, Buchmann does not disclose the use of memory read and write operations during his TS0 and TS3 sequences during initialization/power-on. Buchmann therefore discloses a training mode in which the memory module can be made to perform operations related to various training sequences and which does not include any memory read and write operations in response to memory controller commands.

179. Buchmann's implementation involves a daisy chain arrangement among the various modules of his system, resulting in signals from the memory module to the host indicating completion of a training sequence reaching the host only after all modules had completed the sequence. *See, e.g.*, EX1016 (Buchmann) at 3:49-52, 14:41-43, 16:47-50, 28:23-26. However, Buchmann also explains that

"one or more other bus structure(s) or a combination of bus structures" may be used, including "point-to-point bus(es)," "multi-drop bus(es)," and/or "other shared or parallel bus(es)." *Id*. at 28:26-31.

D. U.S. Patent No. 8,386,722 to Wang et al. (EX1090)

180. United States Patent No. 8,386,722 to Wang et al. ("Wang") was filed on June 23, 2008, EX1110, and the patent issued February 26, 2013, EX1090. I understand that Wang is prior art to the 024 Patent. Wang is entitled "Stacked DIMM Memory Interface." EX1090 (Wang) at Title; *see also* EX1110, 29.

181. Wang discloses interface circuits (e.g., 550) coupled between the memory devices (542) and the system's memory controller (524) to overcome "command scheduling constraints that limit command scheduling and command issue rates in memory systems: inter-device command scheduling constraints, and intra-device command scheduling constraints." EX1090, 1:19-40, 2:16-18, Fig. 5B, 5E (reproduced below).

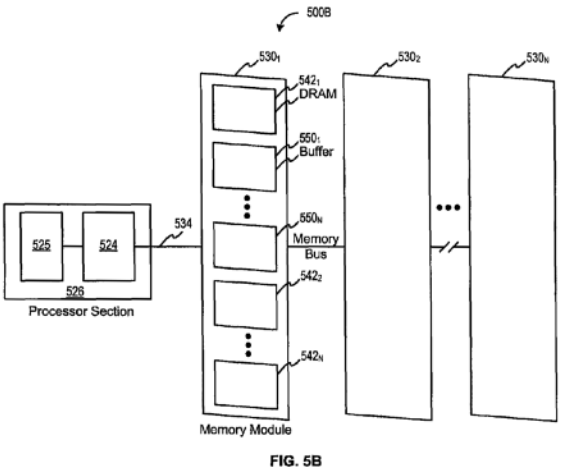


FIG. 5B

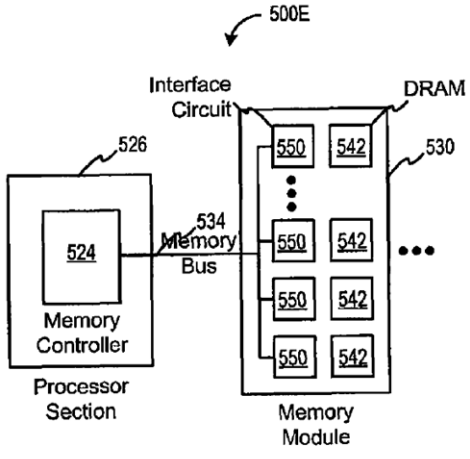


FIG. 5E

182. Wang explains that "[o]ne advantage of the disclosed interface circuit is that it can provide higher memory performance by not requiring idle bus cycles to turnaround the data bus when switching from reading from one memory device to reading from another memory device, or from writing to one memory device to writing to another memory device." EX1090, 2:40-45. For example, Wang explains that, as the operating speed increases, the prior art needed idle cycles for "switching from one memory device driving the data bus to another memory device driving the data bus," and such idle cycles can be advantageously reduced or eliminated by Wang's interface circuit, thereby providing higher communication speed. EX1090, 6:18-60, Figs. 3A-3C (illustrating idle cycles between different memories driving the data bus), 8:15-62, Figs. 4A-4B (illustrating Wang's solution to eliminate idle data-bus cycles using its interface circuit).

183. Wang also discloses "how the interface circuit can optionally make use of a training or clock-to-data phase calibration sequence to independently track the clock-to-data phase relationship between the memory components and the interface circuit." EX1090, 3:17-22, Fig. 4C.

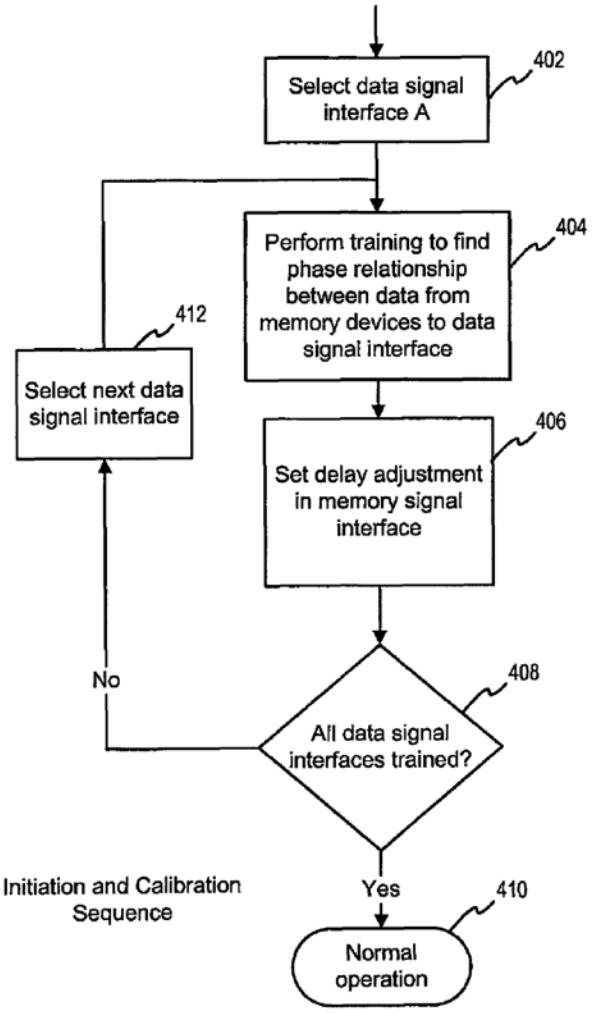


FIG. 4C

E. U.S. Patent No. 8,359, 521 to Kim et al. (EX1017)

184. United States Patent No. 8,359,521 to Kim et al. ("Kim") was filed on January 22, 2008, the underlying application was published July 23, 2009, and the patent issued January 22, 2013. I understand that Kim is prior art to the 024 Patent. Kim is entitled "Providing a Memory Device Having a Shared Error Feedback Pin." EX1017 (Kim) at Title.

185. Kim discloses a "system and method for providing a memory device having a shared error feedback pin." EX1017 (Kim) at Abstract, Fig. 5 (below, showing shared ERROR# pin to indicate Parity error in command/address signals or CRC error in write data).

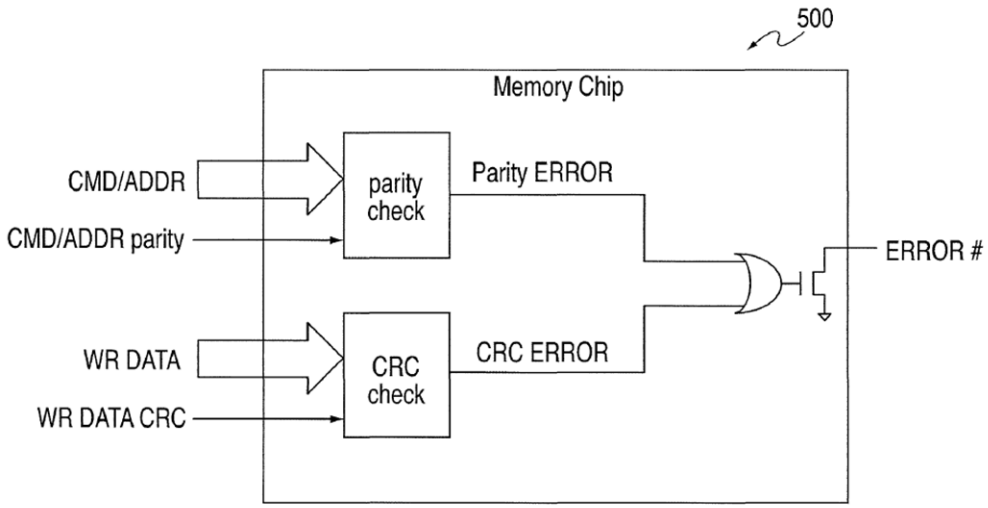


FIG. 5

Kim discloses that sharing functionality with an error pin is desirable in order to maximize use of available bandwidth, simplify the memory controller, EX1017 (Kim) at 4:40-49, "mak[e] use of unused circuits within the subsystem," EX1017 (Kim) at 11:31-34, and enable compatibility with standard memory modules, EX1017 (Kim) at 5:49-57. Kim also teaches that information passing from a memory subsystem, such as the error conditions passed from a memory module through the shared error feedback pin, can also include status reporting and information related to completing initialization. EX1017 (Kim) at 12:18-26. Kim further teaches how this shared error pin can be implemented using an open drain

configuration and/or an OR-gate. EX1017 (Kim) at 5:49-57; *see also id*. at 4:40-48; 6:1-16; FIGS. 4 and 5.

V. COMPARISON OF THE PRIOR ART TO THE CLAIMS OF THE 024 PATENT

186. My analysis below is based on my understanding of the law and the other information discussed above.

A. The Combinations Relied on Here

187. The combinations analyzed here – Hazelzet/Buchmann, Hazelzet/JEDEC, and Hazelzet/Wang (Ground 1-3, respectively) optionally with Kim (Ground 4-6, respectively) – are straightforward. In each, Hazelzet's memory module would be modified to add the functionality of buffering the data signals to the Memory Buffer, similar to that in JEDEC's DDR3 LRDIMM or in Wang, and implementing corresponding training during initialization which includes training sequences and which reports completion of those training sequences by a notification/status signal output over an open-drain output (e.g., UE 121) of Hazelzet.

188. The Board has repeatedly found a motivation to combine Hazelzet and Buchmann, and disagreed with Netlist's arguments to the contrary. *See* EX1034 ('623 FWD), pp.7-20; EX1102 ('218 FWD), pp.15-44; EX1103 ('595 FWD), pp.16-44. In the Hazelzet/Buchmann combination, the training sequences would be like those described as TS0, EX1016 (Buchmann) at FIG. 4, 5:51-7:2 & Tables 1-

2, or alternatively, like those described as TS3, EX1016 (Buchmann) at FIG. 6, 8:24-9:18 & Tables 5-6. The open-drain output signals would be conveying the TS0_done information in the former case, EX1016 (Buchmann) at FIG. 4, 5:51-7:2 & Tables 1-2, and TS3_ack or the TS3_done information in the latter case, EX1016 (Buchmann) at FIG. 6, 8:24-9:18 & Tables 5-6. Furthermore, Buchmann does not disclose the memory controller communicating any data with the module or performing any normal memory read or write operations during initialization/power-on. As discussed above, a Skilled Artisan would have understood that training can be performed without any "*normal memory read or write operations*." *See* ¶70 (explaining the use of standardized write leveling for training write timing and the use of MPR for training read timing, e.g., Read Enable training). Therefore, there is no reason to access the memory devices for any normal read or write operations when the training sequences similar to those of Buchmann are performed.

189. In the Hazelzet/JEDEC combination, the training sequences would be like those described as MB-DRAM Training in the JEDEC proposal (e.g., Write Leveling, Read Enable Training, or Read/Write DQ/DQS training), EX1015 at 3, 8, and the open drain output would be used to signal completion of the MB-DRAM training similar to the signal output on the ERROUT# pin as described in JEDEC, *id*. at 3, 8; *see also* EX1036, 8 (penultimate entry in table on page re ErrOut_n – is

an open drain output for parity errors during normal operation). During those training sequences, the memory controller communicates no data with the module and the memory devices are not accessed for any normal memory read or write operations; the MB-DRAM training is carried out by the memory buffer and the module controller on the module. EX1015, 8 ("No DRAM commands…over the Command/Address and Control buses…can be issued to the MB until the MB-DRAM Interface training is complete…"). As discussed above, a Skilled Artisan would have understood that the DRAM interface training can be performed using standardized features (Write leveling, MPR) without any "*normal memory read or write operations*." *See* ¶70 (explaining the use of standardized write leveling for training write timing and the use of MPR for training read timing, e.g., Read Enable training).

190. In the Hazelzet/Wang combination, the training sequences would be like those described as "training or clock-to-data phase calibration sequence" between the interface circuits and the memory devices in Wang. EX1090, 3:17-22, 8:63-9:67, Fig. 4C. "The goal of the training or calibration sequence is to establish the clock-to-data phase relationship between the data from a given memory device among the memory components 210 and a given memory data signal interface 278." *Id*. 9:12-15. The open-drain output signals would indicate when all data signal interfaces are trained, *id*. at 9:47-52, 9:58-67, Fig. 4C (step 408), so that

normal operation can be performed subsequently, *id*. (step 410). Furthermore, Wang does not disclose the memory controller communicating any data with the module or access the memory devices for any normal read or write operations during the training. As discussed above, a Skilled Artisan would have understood that DRAM interface training can be performed using standardized features (Write leveling, MPR) without any "*normal memory read or write operations*." *See* ¶70 (explaining the use of standardized write leveling for training write timing and the use of MPR for training read timing, e.g., Read Enable training). Indeed, Wang discloses that normal operation happens after training. *Id*.

191. In these combinations, the circuitry of Hazelzet's module would be modified to implement the training as part of initialization with Hazelzet's other disclosed initialization operations, and to use an open drain output of Hazelzet to communicate the new notification signals about the status of the training. EX1014 (Hazelzet) at ¶[0123] (initialization operations); EX1015, 3 (training occurs during initialization); EX1016 (Buchmann) at 3:49-60 (same). As explained in more detail below, Hazelzet already uses his UE 121 open-drain output for two different signals in two different modes. Thus, this ECC/Parity register necessarily includes circuitry for receiving inputs for each of those signals, and selecting which one to drive on the UE 121 output depending on the mode of the module. Therefore, it was well within the level of ordinary skill to modify such circuitry such that it

accepted three different inputs for three different modes and would select among them depending on the mode, and a Skilled Artisan had the skill to make that modification without undue experimentation and with a reasonable expectation of success.

192. Finally, these combinations would employ the well-known open-drain signaling circuitry, which included a transistor having its source coupled to ground and its drain as the output. That is what a Skilled Artisan would have understood the phrase "open drain" to mean, as explained above. *Supra*, ¶¶46-54. A Skilled Artisan would have also known that, in order to use open-drain signaling to indicate training completion among multiple modules, the open-drain output would have to be configured such that the transistor output is driven to logic low (ground) while training is still occurring and driven to logic high upon training completion. This is because, with an open-drain configuration shared by multiple modules, any module can individually drive the output to logic low, but it takes the collective action of all connected modules (and an external pull-up resistor) to drive the output to logic high. Moreover, a Skilled Artisan would have also understood that to drive the output to logic low (which would have a low impedance (conductive) state of the transistor), the gate of the transistor must be logic high, causing the transistor to conduct and connect the drain to ground. Conversely, to drive the output to logic high (which would have a high impedance (non-conductive) state of

the transistor and requires an external pull-up resistor), the gate of the transistor must be logic low, turning the transistor off. As explained above, this is how an open-drain output works. *Supra*, ¶¶46-54; EX1014, ¶[0099]; EX1017, FIGS. 4-5, 5:65-6:18.

B. Reasons to Combine

193. All of the prior art relied on in this declaration, including Hazelzet, JEDEC, Buchmann, Wang, or Kim are analogous art to the 024 Patent because all are in the same field of invention: memory module design, including improving memory module operation to achieve improved capacity, speed, reliability, and efficiency by techniques such as data buffering, error detection and correction, initialization, training, and the use of pins/paths for multiple purposes during different operations/modes. EX1001 (024 Patent) at Abstract, 1:22-38 ("The present invention relates to the operation of memory modules. Specifically, the present disclosure relates to a memory module having an open drain output for parity error and for training sequences. … Memory subsystems such as memory modules are generally involved in the initialization procedure…"), 3:30-39 ("Existing initialization schemes have certain inefficiencies which lead to wasted time and expense…."); EX1014 (Hazelzet) at Abstract ("A high density high reliability memory module with power gating and a fault tolerant address and command bus."), ¶¶[0007] (similar), [0069]-[0070] (explaining two operating

modes, ECC mode and parity mode, in which the two modes share a signal pin for notifying the memory controller of errors), [0123] ("Initialization…based on the available interface busses, the desired initialization speed, available space, cost/complexity objectives, subsystem interconnect structures…"); EX1015 (JEDEC proposal), 1, 3, 8 (noting document is JEDEC ballot for "LRDIMM DDR3 Memory Initialization Chapter Proposal" that includes various training during initialization, including utilizing the parity ERROUT# pin for multiple purposes for training notifications of status); EX1016 (Buchmann), 1:7-9, 3:49-60, 4:51-5:50, 12:60-13:41, 14:1-63, 20:20-21:19, 33:45-67 (explaining that its invention relates to memory modules, with, among other things, an SBC mode and a "high-speed" or "functional" mode, wherein the SBC mode combines initialization/training and ECC that runs at power-on initialization and can also be entered from normal (i.e., "high-speed" or "functional") operation for ECC without full re-initialization/training); EX1090 (Wang) at 1:5-8 ("Embodiments of the present invention generally relate to memory subsystems and, more specifically, to improvements to such memory subsystems."), 2:16-18 ("…what is needed in the art is a memory subsystem and method to overcome the shortcomings of prior art systems."), 9:9-15 ("The training or calibration sequence is typically performed after the initialization and configuration logic 282 receives either an interface circuit initialization or calibration request…"); EX1017 (Kim) at 1:16-22, 5:49-57,

6:8-18, 11:20-34, 12:36-53 (explaining that invention relates to memory modules, with, among other things, two operating modes — ECC mode and parity mode — in which the two modes share a signal pin for notifying the memory controller of errors, and initialization operations/modes that includes "completing a training process to establish reliable communication," and further teaching that "initialization circuitry" "may reside local to the" memory module and that, by doing so, "added performance may be obtained as related to the specific function, often while making use of unused circuits within the subsystem," and further teaching that, in addition to sharing ECC and parity on the error out pin, "[i]n alternate exemplary embodiments, other functions also share the error feedback pin").

194. Furthermore, each of Hazelzet, JEDEC, Buchmann, Wang, and Kim is reasonably pertinent to the problem addressed by the 024 Patent: increasing memory module capacity, speed, performance, efficiency, and/or reliability by techniques such as data buffering and corresponding training and sharing an output pin/path to perform multiple functions during multiple operations/modes, including initialization/training. EX1001 (024 Patent) at Abstract, 6:41-56, 8:46-9:23; EX1014 (Hazelzet) at Abstract, ¶¶[0007], [0069]-[0070], [0123]; EX1015, 1, 3, 8; EX1016 (Buchmann) at 1:7-9, 3:49-60, 4:51-5:50, 12:60-13:41, 14:1-63, 20:20-21:19, 33:45-67; EX1090 (Wang) at Abstract (accurate timing reference,

eliminating the cost of idle cycles, increasing memory system bandwidth), 2:40-45 ("One advantage of the disclosed interface circuit is that it can provide higher memory performance by not requiring idle bus cycles to turnaround the data bus…"), 8:1-10 ("The advantage of the … interface circuit 250 … is that it can provide the higher capacity, higher parallelism that the memory controller desires while retaining the use of the DQS signal in an infrastructure-compatible system to provide the accurate timing reference for data transmission that is critical for modern memory systems, without the cost of the idle cycles"); EX1017 (Kim) at 1:16-22, 5:49-57, 6:8-18, 11:20-34, 12:36-53.

195. The prior art relied on to illustrate the knowledge of a Skilled Artisan is also analogous art. *See*, *e.g.*, EX1022 (Talbot), ¶¶[0004]-[0005], [0032-33], [0052] (explaining that invention relates to memory modules, with, among other things, two modes — "a normal operation mode and a configuration and test mode," part of which is called "training mode" — and, during "training mode," the "CRC signal path" (normally used for "error detection" and "correct[ion]") is used to "loop back" "training patterns" sent on the "BCMD signal path" (a command signal) to train the BCMD signal path); EX1025 (JESD206), 15-18 (JEDEC memory module standard for FBDIMM, specifying, in addition to various operating modes, initialization sequences that "must sequence the AMB devices through the Disable, Calibrate, (back to Disable), Training, Testing, and Polling

states in order to transition the AMBs into the active channel L0 state" (e.g., operating modes)); EX1027 (Hein), 1:61-2:19, 6:24-25, 10:24-45 (discussing importance of training, including for memory modules, and disclosing, in addition to a "standard operating mode," a "training mode" that occurs before "standard operating mode").

196. Also, one skilled in the art would have considered each of the combinations analyzed here to be merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement. Each of Hazelzet, JEDEC, Buchmann, Wang, and Kim, for example, is a prior art disclosure employing known data buffering, signaling and/or training techniques. Many prior art systems had similarly included such techniques. Combining them as described here would therefore have been well within the level of ordinary skill in the art, would not have resulted in any unpredictable results, and could have been readily accomplished without undue experimentation and with a reasonable expectation of success.

197. A Skilled Artisan would have been motivated to make these combinations for at least the following reasons.

1. Motivation to add data buffering and corresponding training

198. A Skilled Artisan would have been motivated to add data buffering and corresponding training to the memory module of Hazelzet. Indeed, Hazelzet emphasizes the need for a "high density high reliability memory module" and "improved overall system reliability." EX1014 (Hazelzet) at Abstract ("A high density high reliability memory module with power gating and a fault tolerant address and command bus."), ¶[0001-0002] ("This invention relates generally to a high-density, high-reliability memory module with a fault tolerant address and command bus for use as a main memory that will achieve the degree of fault-tolerance and self-healing necessary for autonomic computing systems."), ¶[0004] ("The present invention provides such a comprehensive system solution that includes the capability of high memory density and a high degree of fault tolerance and the overall differentiated system reliability long desired in the server market."), ¶[0007] ("The present invention is directed to a high density high reliability memory controller/interface module, provided with a high degree of compatibility with industry standard solutions, capable of meeting the desired density, performance and reliability requirements and interfacing with the presently available memory modules, as well as with existing or enhanced support devices. The present invention accomplishes all these ends, resulting in a high density and enhanced reliability memory solution at low cost."), ¶[0003] ("Thus the emphasis

and need for improved overall system reliability is increasing dramatically and requires a comprehensive system solution that includes both a high degree of fault tolerance and overall reliability."); *see also id*. at ¶[0042] ("The ECC/Parity buffer chips 21 on DIMM 20 include unique error correction code (ECC) circuitry that is coupled to the memory interface chip 18 via line 25 to provide even greater significant reliability enhancement to such servers. The inclusion of this new, improved error correction code (ECC) circuitry results in a significant reduction in interconnect failure."), ¶[0044] ("The novel ECC/ Parity buffer 21 on DIMM 20 thus provides leading-edge performance and reliability and key operational features different from and unavailable from the prior art while retaining timing requirements generally consistent with devices such as the JEDEC 14 bit 1:2 DDR II register.").

199. Hazelzet discloses a Registered DIMM (RDIMM) which buffers address and command signals, but not data signals. EX1014 (Hazelzet), e.g., at Fig. 1, [0036]. In accordance with its emphasis on the need for a "high density…memory module," Hazelzet discloses that its RDIMM can support up to 4 ranks of memory. *Id*., at Abstract ("A high density high reliability memory module with…up to four ranks of memory devices mounted on the first side and second side of the circuit board"). A Skilled Artisan would have understood at the time that increasing the number of ranks without data buffering creates more

electrical load on the data bus that limits the speed of the memory module. *See, e.g.*, EX1028 (Ellsberry) at [0031] ("signal drivers to drive data signals to and from the memory banks and to and from the DIMM interface 202...reduces resistive and/or capacitive loading of the data bus coupled to the DIMM interface and the bus…"). Thus, a Skilled Artisan would have been motivated to lower that load on the data bus by updating Hazelzet's RDIMM to a module that also buffers data signals. Indeed, data buffering was well known at the time and had been already used in the LR-DIMM of the JEDEC proposal, in the fully-buffered DIMM as shown in Buchmann, in the module with Wang's data interface circuits, as well as in the modules of Ellsberry.

200. A Skilled Artisan would have also known, as the provisional admits, about the DDR3 LR-DIMMs and the corresponding initialization and training of LR-DIMMs at the time. EX1008, 22 (describing "recent proposal in JEDEC for L[R]-DIMM (load Reduced DIMM) requires the MCH to hand over one or more parts of the initialization operation sequences to the memory subsystem controller"). Further, the JEDEC proposal includes a portion of the draft standard for DDR3 LRDIMMs being voted upon by JEDEC members that specifically addresses "power-up initialization," requires various training including "MB-DRAM Training" and explains that, during that training, "[t]he MB performs 'Write Leveling' to the DRAMs ***to ensure successful writes***, and 'Read Enable

Training' ***to ensure it can capture read data from the DRAMs correctly***, as part of the DRAM interface training," and further teaches that "MB DRAM interface training must be completed before any MB host interface read or write training ***to ensure that the MB DRAM interface is configured optimally for DRAM reads and writes***." EX1015, 3, 8-9 (emphasis added). These statements about ensuring successful and optimally configured read and write operations by training would have motivated a person of ordinary skill to add a data buffer and corresponding training to other systems, such as that of Hazelzet.

201. A Skilled Artisan would have also known about Wang's interface circuit and its corresponding training, and that "it can provide higher memory performance by not requiring idle bus cycles to turnaround the data bus" and it "might be advantageously applied to reduce or eliminate idle time…between the data transfers" therefore "it can provide the higher capacity, higher parallelism that the memory controller desires while retaining the use of the DQS signal in an infrastructure-compatible system to provide the accurate timing reference for data transmission that is critical for modern memory systems." EX1090, 2:40-45, 6:52-60, 8:1-10. Wang also explains that "in the case of higher speed memory systems, where data bus cycles times are comparable in duration to, or shorter than, one-nanosecond, a one-nanosecond uncertainty in skew or jitter between signal timing from different devices means that memory controllers can no longer reliably

capture data from different devices without accounting for the inter-device skew and jitter characteristics." EX1090, 7:44-51. To address those issues, Wang teaches a "training or calibration sequence" whose "goal … is to establish the clock-to-data phase relationship between the data from a given memory device … and a given memory data signal interface." *Id*., 9:9-15.

202. As discussed above, Hazelzet discloses a memory module that can include up to four ranks of memory devices and buffers address and command signals, but the data lines are not buffered—an arrangement known at the time as a Registered DIMM. *Supra* ¶¶161-166; *see also* EX1079, pp.8-10 (illustrating RDIMM, FBDIMM, and LRDIMM arrangements). In the DDR3 Load Reduced DIMM (LRDIMM), however, the Memory Buffer (MB) also buffers data signals. EX1036, 5 ("Product Description"). The LRDIMM Design Specification explained in detail the advantages of adding the LRDIMM's data buffering functionality to a Registered DIMM (RDIMM), like Hazelzet's module, which buffers only address and command signals. *Id*. In particular, the LRDIMM Design Specification explained that "LRDIMM differs from RDIMMs in that the SDRAMs do not connect directly to the edge connector … The Memory Buffer (MB) buffers both address and data. Increased performance is achieved based on the LRDIMM presenting only one load to the system. Increased capacity is achieved since the MB drives only the SDRAMs on the module and therefore a

well defined topology and load. The maximum number of SDRAM die is 144. The LRDIMM is intended to function in all RDIMM platforms with appropriate BIOS changes. Systems designed to function with LRDIMMs will be better able to take advantage of LRDIMM features." *Id*.

203. Similarly, a Skilled Artisan would have understood that Wang's interface circuits also buffer the data signals and provide advantages over an RDIMM design similar to those discussed above with reference to the LRDIMM. In addition, Wang explains the advantages of its specific data buffering design over other data buffering techniques, such as those used in FBDIMM modules, including that its "invention may be used with previously existing memory controllers, without modification to their logic or interfacing requirements." EX1090, 1:41-2:15.

204. Thus, a Skilled Artisan would have understood at the time that Hazelzet's RDIMM can be upgraded with JEDEC's LRDIMM functionality or the functionality of Wang's interface circuit to buffer the data lines, not just the address and command lines. A Skilled Artisan would have been motivated to make such an upgrade because the LRDIMM's and Wang's data buffering increased performance by presenting a single load to the system instead of the multiple loads on the data pins of Hazelzet's RDIMM module which had multiple ranks coupled to those data pins. The Skilled Artisan would have been further

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Ex. 1003, p. 174

motivated to make such an upgrade because the LRDIMM and Wang's interface circuit would have worked even in RDIMM platforms (with appropriate BIOS changes), thus it was possible to achieve these advantages in existing, RDIMM based systems, like in Hazelzet. These advantages of buffering the data lines in addition to buffering the address and command lines of a DIMM, thus isolating the memory devices from the system bus, were well known to a Skilled Artisan at the time. *See, e.g.*, EX1028 (Ellsberry), [0031] ("Additionally, each memory bank switch 206 and 208 includes signal drivers to drive data signals to and from the memory banks and to and from the DIMM interface 202. This reduces resistive and/or capacitive loading of the data bus coupled to the DIMM interface and the bus…"). Thus, a Skilled Artisan would have understood that buffering the data lines on Hazelzet's module, like in the LRDIMM format or as taught by Wang, would advantageously reduce the load of the four memory ranks on the module to a single load. I understand that Netlist's expert has agreed that a Skilled Artisan would have understood this. EX1077, 86:12-21 ("Q. So if I understand correctly, as a benefit of reducing electrical load, that it can permit the signaling on the memory module to be faster? … THE WITNESS: Yes."), 104:6-24 ("Q. In what situations would an LR-DIMM memory module be more advantageous than a memory module without a data buffer? … THE WITNESS: ….[I]f you need

something that needed large capacity, you would pick the LR-DIMMs or anything that had a data buffer on it.").

205. Furthermore, given Hazelzet's emphasis on the need for a "high reliability memory module" and "improved overall system reliability," one skilled in the art would have been motivated to add training to Hazelzet because it was known that training improved the reliability of a memory module's operations. EX1027 (Hein), 1:35-2:12 (discussing importance of training, including for DIMMs, given advent of DDR memory devices and increasing frequencies, and stating "During a training stage, such a memory controller may write certain data to and read certain data from a memory device, for example a DRAM, and shift the data signal in respect to the clock signal within the time domain, such that the data signal arrives at the memory device with a well-defined synchronization to the clock signal. The memory controller may vary this time shift until a written value corresponds to a read value, which indicates that timing is correct. *In this way, a reliable, fast, and efficient exchange of information is enabled*." (emphasis added)); EX1025 (JESD206), 15-18 ("FBDIMM Architecture and Protocol" standard, specifying initialization sequences that "must sequence the AMB devices through the Disable, Calibrate, (back to Disable), Training, Testing, and Polling states in order to transition the AMBs into the active channel L0 state" and, for training, noting that, "[b]efore the channel is initialized the bit lanes are not aligned

to a frame boundary, thus preventing Channel and DRAM commands from being communicated to the AMBs" such that training is required). This is particularly true given the emerging DDR3 applications in the 2009-10 time frame and their increased speeds. EX1045, 22-24 (2008 Micron technical note explaining need for training for reads and writes); EX1090 (Wang), 6:33-37 ("As the speed of the clock increases, the inter- and intra-device delays comprise successively more and more of a clock cycle (as a ratio). At some point, the inter- and intra-device delays are sufficiently large (relative to a clock cycle) that the multiple devices on a shared bus must be managed."), 7:44-51 ("However, in the case of higher speed memory systems, where data bus cycles times are comparable in duration to, or shorter than, one-nanosecond, a one-nanosecond uncertainty in skew or jitter between signal timing from different devices means that memory controllers can no longer reliably capture data from different devices without accounting for the inter-device skew and jitter characteristics."). Indeed, Hazelzet also discloses that "[i]nitialization of the memory subsystem" should occur, it just does not expressly address training as part of that initialization or provide further details regarding how to go about that aspect of initialization. EX1014, ¶[0123]; EX1017, 12:36-53.

206. Accordingly, a Skilled Artisan would have been motivated to upgrade Hazelzet's RDIMM with the functionality of buffering the data lines like in JEDEC's LRDIMM or as in Wang's interface circuits because it would have

increased the performance and allowed higher capacity by decreasing the load on the data lines. The Skilled Artisan would have been also motivated to use the initialization techniques of JEDEC for the upgraded LRDIMM, including MB-DRAM Training, because it ensured that the different interfaces, including the MB-DRAM interface, are optimally configured for reading and writing the memory devices. EX1015, 8-9 ("MB DRAM interface training must be completed before any MB host interface read or write training to ensure that the MB DRAM interface is configured optimally for DRAM reads and writes."). Similarly, a Skilled Artisan would have been motivated to use the training of Wang's interface circuit in the upgraded module of Hazelzet in order to "reliably capture data from different devices" by "accounting for the inter-device skew and jitter characteristics." EX1090, 7:44-51. Such a combination would have been well within the level of skill at the time and provided nothing more than expected from the combination: a load reduced DIMM with a memory buffer (MB) or Wang's interface circuit functionality that buffered data, address and command signals and implemented training to ensure a reliable and optimal configuration for reading and writing the memory devices during normal operation.

207. Also, Buchmann's "SBC mode" is a mode of operation where "error correcting code" is provided, EX1016 (Buchmann) at 14:25-32, as well as a "training phase that allows more flexibility and improved control data exchange

during start-up," *id*., 3:64-67, to establish "reliable communication" on the bus, *id*. at 14:28-35 ("Quasi-static bit communication, also referred to as 'static bit communication' or 'SBC', can be used to control the sequence of link initialization and training phases to establish reliable communication on the high-speed bus. When error correction of an SBC sample is performed prior to checking for a static pattern, the error correction may be able to repair errors that would otherwise prevent the pattern from being static over a period of time."); *see also id*. at 14:5-8. Thus, one skilled in the art would have been motivated by Hazelzet's desire to improve reliability to look to systems such as JEDEC's, Wang's, and Buchman's that were designed to do just that.

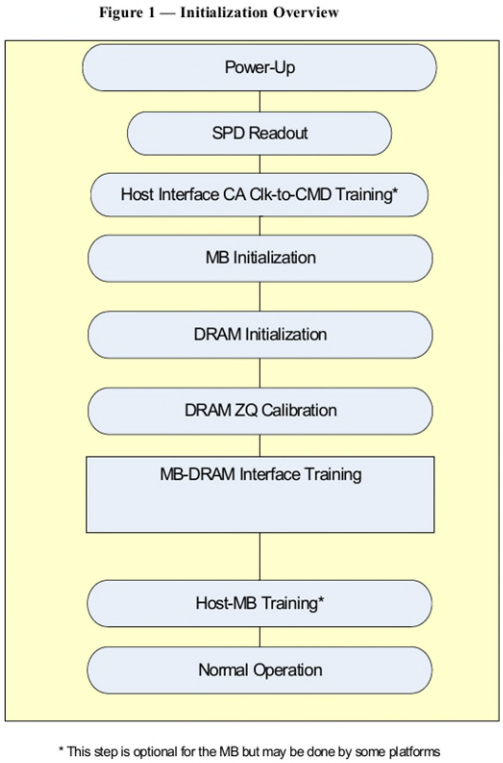
208. Furthermore, Buchmann also discloses a buffer/register that buffers data signals in addition to address and command signals. As discussed above with reference to JEDEC and Wang, a Skilled Artisan would have been motivated to add the functionality of buffering the data signals to Hazelzet's Registered DIMM, for example, because Hazelzet's module can have up to four ranks of memory devices, each presenting its corresponding load on the data lines, and the Skilled Artisan would have understood that buffering the data lines lowers the load of the module to a single one (that of the buffer), allowing improved performance, higher frequencies of operation, and higher capacity, as discussed above. *Supra*, ¶¶198-206. The Skilled Artisan would have been also motivated to use Buchmann's

initialization techniques for the upgraded Hazelzet module, including Buchmann's training and corresponding notifications, because those initialization techniques provided a known, reliable way for efficiently initializing the upgraded module. Accordingly, making the combination of Hazelzet and Buchmann was well within the level of skill at the time and provided nothing more than expected at the time, a DIMM with a buffer to buffer data, address and command signals and efficient training of that buffer during initialization to ensure optimal read and write performance during normal operation.

2. Motivation to use training without normal memory read or write operations

209. One skilled in the art would also have been motivated to combine Hazelzet and JEDEC or Buchmann or Wang by performing training separate from normal memory operations, such as normal memory read or write operations, because she would have known that training the memory systems helps to ensure that the subsequent normal memory operations occur in a most-efficient and reliable way. As discussed above, a Skilled Artisan would have understood that training can be performed without any "*normal memory read or write operations*." *See* ¶70 (explaining the use of standardized write leveling for training write timing and the use of MPR for training read timing, e.g., Read Enable training). For example, it was well known that training during initialization of a memory module before normal operations was necessary to minimize errors, by "ensur[ing]

successful writes," and "ensur[ing] [the Memory Buffer (MB) on the DIMM] can capture read data from the DRAMs correctly." EX1015, 8. Training can also be performed after initialization, whenever data "can no longer reliably capture[d]." EX1090, 7:44-51 ("However, in the case of higher speed memory systems…memory controllers can no longer reliably capture data from different devices without accounting for the inter-device skew and jitter characteristics."). Accordingly, training is taught to be completed as part of "power-up initialization," before moving to "Normal Operation," EX1015 (JEDEC), 3 (listing eight steps, including various training steps, as part of initialization before listing "Normal Operation" as step 9), Fig. 1 at p.4 (similar, reproduced below, left), or any other time when the system controller requests it, EX1090 (Wang), Fig. 4C (reproduced below, right), Fig. 4D (showing "Calibration command" issued during "Normal Operation,"). Either way, the system returns to "normal operation" after the training, which was designed to improve such a subsequent "normal operation." EX1090, 9:9-52 ("The training or calibration sequence is typically performed after the initialization and configuration logic 282 receives either an interface circuit initialization or calibration request… In step 408, the initialization and configuration logic 282 determines whether all memory data signal interfaces 278 within the interface circuit 250 have been calibrated. If so, the method ends in step 410 with the interface circuit 250 entering normal operation regime.").



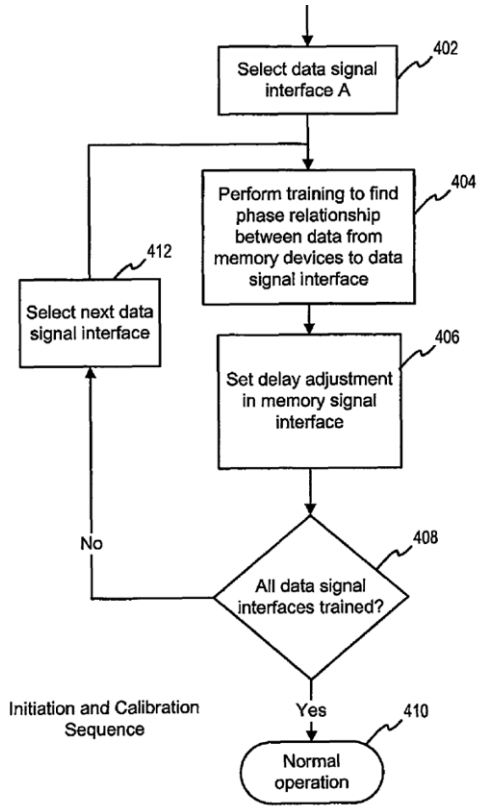


FIG. 4C

See also EX1025, 15-18 ("FBDIMM Architecture and Protocol" standard, specifying initialization sequences that "must sequence the AMB devices through the Disable, Calibrate, (back to Disable), Training, Testing, and Polling states in order to transition the AMBs into the active channel L0 state" and, for training, noting that, "[b]efore the channel is initialized the bit lanes are not aligned to a frame boundary, thus preventing Channel and DRAM commands from being communicated to the AMBs" such that training sequences are required); EX1022, Fig. 4, ¶¶[0032], [0052], [0088-89]; EX1056, 18, 22, 25-26, 42-44; EX1057, Fig. 5, Abstract, 2:13-34, 2:60-3:3, 9:11-10:44. Likewise, Buchmann's invention is an

"initialization training sequence" completed at "power-on," EX1016 (Buchmann) at Abstract (explaining that its "memory buffer includes logic for executing a power-on and initialization training sequence initiated by the memory controller."), which would also suggest to a Skilled Artisan that training before normal operations is important.

210. The memory system in Hazelzet would be initialized upon power-on. *See, e.g.*, EX1014 (Hazelzet) at ¶[0123] ("Initialization of the memory subsystem may be completed via one or more methods, based on the available interface busses, the desired initialization speed, available space, cost/complexity objectives, subsystem interconnect structures, the use of alternate processors (such as a service processor) which may be used for this and other purposes, etc."); *see also* EX1025, 15-18 (JEDEC memory module standard for FBDIMM, specifying initialization sequences that "must sequence the AMB devices through the Disable, Calibrate, (back to Disable), Training, Testing, and Polling states in order to transition the AMBs into the active channel L0 state" (e.g., operating modes)); EX1027, 1:61-2:19; 6:24-25; 10:24-45 (discussing importance of training, including for memory modules, and disclosing, in addition to a "standard operating mode," a "training mode" that occurs before "standard operating mode"). Thus, JEDEC's, Buchmann's, and Wang's training (each of which can occur during initialization) would have complemented that power-up process as part of Hazelzet's

initialization, and one skilled in the art would have therefore been motivated to combine Hazelzet and JEDEC or Buchmann or Wang to perform training without normal memory operations, such as normal memory read or write operations, in order to make sure that, after the training, the subsequent normal memory read and write operations can be reliable and efficiently performed.

3. Motivation to use Hazelzet's open drain signaling for training notifications

211. In the obvious combination of Hazelzet and JEDEC or Buchmann or Wang analyzed here it would have been further obvious to a Skilled Artisan to employ the open-drain parity and ECC signal connections and techniques of Hazelzet to communicate the status of the JEDEC or Buchmann or Wang training sequences, respectively, in order to indicate to the system memory controller that the modules are performing training operations and cannot be accessed for any normal read or write operations during that training. Based on the status indication of the open-drain output, the system memory controller can return to "Normal Operation" after the completion of the training. Therefore, as explained below in detail, any combination of Hazelzet with JEDEC or Buchmann or Wang renders obvious the claimed limitation of "*apply[ing] a second signal related to one or more training sequences … when the memory module performs operations associated with the one or more training sequences*" in claim 1 and corresponding limitations in independent claims 10 and 19.

212. To be clear: as to the JEDEC combination, it is my opinion that a Skilled Artisan would have found it obvious to communicate that the MB-DRAM training was completed using the open drain output (e.g., UE 121) of Hazelzet; as to the Buchmann combination, it is my opinion that a Skilled Artisan would have found it obvious to communicate the TS_done signal of Buchmann for TS0 training, and also obvious to communicate the TS3_ack and/or TS_done signals of Buchmann for TS3 training, using the open drain output (e.g., UE 121) of Hazelzet; and as to the Wang combination, it is my opinion that a Skilled Artisan would have found it obvious to communicate that the phase-relationship training of Wang was completed using the open drain output (e.g., UE 121) of Hazelzet. The reasons to make such combinations are set forth below.

213. As discussed above, open-drain outputs were well known at the time. *Supra*, ¶¶46-54. Using open-drain outputs for handshaking was also well known. For example, Professor Stone explained more than 25 years before the 024 Patent that one of the strategies to communicate to a processor that an input/output port is busy with an operation and cannot receive other instructions is that the port itself sends a signal to the processor, sometimes called an interrupt request, to indicate when the port has completed the pending operation and can receive further instructions without the processor interrogating the port about its status. EX1089 (Stone), 15-16 ("For interrupt-driven I/O, the port generates a signal to the

processor, called *interrupt request*, at the completion of an operation. The processor…recognizes that the device is no longer busy, and initiates a new transaction. Thus, there is no need to interrogate the port to find out if the port is ready. The interrupt request conveys the ready information."). Thus, a Skilled Artisan would have understood that, and been motivated to, advantageously use handshaking similar to that of the well-known interrupt technique between memory modules and their memory controller in the proposed combinations without the need to interrogate the modules to find out whether the modules are ready (e.g., done with their training). Thus, a Skilled Artisan would have found it obvious to add an interrupt-like handshake techniques to Hazelzet's module to inform the memory controller (in "a role analogous to traffic lights on a roadway") whether their training is still ongoing or completed, so the memory controller would know when the training is complete and when it can initiate data transactions corresponding to normal memory read and write operations with the memory modules. EX1089 (Stone), 14-15, 89 ("The handshake lines have a role analogous to traffic lights on a roadway.").

214. Professor Stone also explains that open-drain outputs (and the similarly operating "open-collector" outputs, *supra* ¶¶46-54) were known and advantageously used in a "wired-OR" configuration to indicate the status of one or more devices coupled to a controller. EX1089 (Stone), 281 ("Some disk systems

take advantage of the open-collector drivers to do 'wired-OR' logic of status signals from multiple drivers."). Thus, a Skilled Artisan would have understood that the wired-OR logic of open-drain outputs, like Hazelzet's UE pin, is particularly useful to indicate when all slave devices coupled to a master device are ready for data. *Id*. 219-220 ("In fact, these two control signals are asserted as active low signals in order to use the open-collector bus to perform an OR function when two or more signals are asserted simultaneously. … NRFD [Not Ready For Data] is an open-collector control line so that NRFD rises only when all slaves are ready.").

215. For example, Hazelzet's "ECC mode" is a mode where a notification signal indicating an "uncorrectable error" (*i.e.*, "UE") can be output to the memory controller through the open-drain output line and 121 (*i.e.*, output for uncorrectable error "UE"). EX1014 (Hazelzet) at FIG. 4B, ¶¶[0044], [0049], [0059], [0064], [0069], [0072], [0109]. The open-drain output line 121 (or "/Error (UE)" 121) is the same open drain output that is also used for the parity error signal. EX1014 (Hazelzet) at FIG. 4B, ¶¶[0044], [0049], [0059], [0064], [0070], [0109]. The open-drain output line 121 is coupled to the memory controller of the host system using error edge connection number 142. EX1014 (Hazelzet) at FIG. 7A (indicating "UE" is pin 142). As such, Hazelzet's implementation involves using the same open-drain output ("/Error (UE)" 121), in two different modes, to output both a

parity error notification signal and an ECC notification signal, depending on which mode the memory module is in. EX1014 (Hazelzet) at FIG. 4B, ¶¶[0044], [0049], [0059], [0064], [0069-70], [0072], [0109]. Hazelzet's use of the same output in two different modes would have suggested to, and motivated, a person of ordinary skill in the art to use that same output during training, e.g., in a training mode, particularly when the training was implemented separate from, e.g., before, the parity and ECC modes of Hazelzet, as here. In such a system, those ECC and Parity modes, which include normal memory operations, would therefore not be using the open drain outputs while the training mode was running during initialization.

216. Similarly, the JEDEC proposal employs this same technique, using the same open-drain output to communicate parity error and training completion in different modes. EX1015, pp.3, 8. Thus, a Skilled Artisan would have viewed the JEDEC proposal's open-drain notification technique as a natural fit in the system of Hazelzet (with its updated data buffering memory modules), and the content of JEDEC's disclosure would have motivated the use of that open-drain signaling technique even when Hazelzet is combined with Buchmann or Wang, disclosing status notifications of the memory module to the memory controller. *See*, *e.g.*, EX1016 (Buchmann), 6:19-20 ("TS_done"), 8:43-44 ("TS_done"); EX1090 (Wang), 4:55-62 ("In various embodiments, the emulation and command

translation logic 280 may respond to signals from the system-facing interfaces by responding back to the system 220 by presenting signals to the system 220…").

217. Further, a person of ordinary skill in the art would have been motivated to use the same output pin to notify both error and training status in different modes of operation because such multiple use of a pin was known, and would have been considered an efficient use of the limited number of output pins on integrated circuits. For instance, Kim, EX1017, is a patent assigned to IBM that shares with Hazelzet a substantial overlap in their disclosures, particularly in the disclosures of open-drain shared outputs and in the latter halves of their specifications. Kim was filed approximately a year and a half after Hazelzet and discloses additional details regarding the use of an open-drain output on a memory module to notify the memory controller of errors during a parity normal operating mode and during an ECC normal operating mode. EX1017 (Kim) at 1:16-22; 5:49-57; 6:8-16. Kim further teaches initialization operations (initialization/training modes) that include "completing a training process to establish reliable communication," *id*. at 12:36-53, teaches that "initialization circuitry" "may reside local to the" memory module and that, by doing so, "added performance may be obtained as related to the specific function, often while making use of unused circuits within the subsystem," *id*. at 11:20-34, and further teaches that, in addition to sharing ECC and parity on the error out pin, "[i]n

alternate exemplary embodiments, other functions also share the error feedback pin," *id*. at 6:16-18. Such disclosures would have motivated a Skilled Artisan to use Hazelzet's "/Error (UE)" 121 open-drain output (corresponding to Kim's "error feedback pin") to notify the memory controller that the training was in progress or done.

218. As another example, Talbot discloses memory modules, with, among other things, two modes: "a normal operation mode and a configuration and test mode" (a part of which is called "training mode"). EX1022 (Talbot) at ¶¶[0004]-[0005], [0032]-[0033], [0052]. Talbot further discloses that, during the "training mode," the "CRC signal path" (normally used for "error detection" and "correct[ion]", *id*. at [0033]) is used to "loop[] back" "training patterns" sent on the "BCMD signal path" (a command signal) to train the BCMD signal path, *id*. at [0052]. Thus, Talbot discloses using a CRC (a type of ECC) signal path to return signals relating to training during the training mode when the CRC functionality is off. *Id*. at [0033], [0052]. Such disclosures would have motivated a Skilled Artisan to use Hazelzet's "/Error (UE)" 121 open-drain output (corresponding to Talbot's "CRC signal path") to notify the memory controller that the training was in progress or done.

219. Moreover, a Skilled Artisan would have been motivated to arrange the updated Hazelzet modules to communicate a signal indicating completion of

training to the memory controller only when all memory modules have completed that training, in order to ensure that the entire memory system had been trained before proceeding to normal operations. This would permit training to be completed in an orderly and systematic manner, thereby limiting the complexity of the control circuitry needed to implement the training. EX1043, 7:30-51. Use of an open drain signal in this manner was a known, efficient way to communicate information about multiple circuits because it effectively OR'd the inputs into a single output. EX1017 (Kim) at FIG. 4, 5:65-6:12 (illustrating and describing just such a system); *see also* EX1014 (Hazelzet) at [0018] ("After holding the error line low for only 2 clock cycles, the driver can be disabled and the output permitted to return to an un-driven state (high impedance) thus allowing this line to be shared by multiple modules."), [0109] ("The error reporting circuitry, of the present invention is included to permit external monitoring of device operation. Two open-drain outputs are available to permit multiple modules to share a common signal pin for reporting an error that occurred during a valid command (any /CS low) cycle (consistent with the re-driven signals).").

220. In addition, a Skilled Artisan would have been further motivated to modify Hazelzet as described above, because Hazelzet's memory system includes multiple memory modules in need of training. In other words, there would be a motivation to delay transitioning to a normal mode of operations until all memory

modules had signaled the completion of training. EX1014 (Hazelzet) at [0018] ("After holding the error line low for only 2 clock cycles, the driver can be disabled and the output permitted to return to an un-driven state (high impedance) thus allowing this line to be shared by multiple modules."), [0109] ("The error reporting circuitry, of the present invention is included to permit external monitoring of device operation. Two open-drain outputs are available to permit multiple modules to share a common signal pin for reporting an error that occurred during a valid command (any /CS low) cycle (consistent with the re-driven signals)."); *see also* EX1017 (Kim) at FIG. 4, 5:65-6:12; EX1043, 7:30-51; EX1090 (Wang) 9:58-67 ("The process is then repeated until all of the memory data signal interfaces 278 have been trained and respective delays are set."). In particular, a Skilled Artisan would have been motivated to use Hazelzet's open-drain output to notify the host of training status because that technique allows any module in the system to pull the open drain pin to "low" (to ground) if it is still executing its training sequence, regardless of whether other modules in the system have completed training and are no longer pulling that pin low. *Id*. As demonstrated above, an open-drain output was a known way to signal when multiple circuits were, or were not all, finished performing some operation. *See* ¶¶46-54.

C. Claims 1-20 are obvious in light of Hazelzet in combination with either JEDEC, Buchmann, or Wang, with or without Kim for certain claims

221. My analysis is based on my understanding of the law as set forth above and the ordinary and accustomed meaning of the claim terms as understood by one of ordinary skill in the art in view of the 024 Patent and its file history. *See* ¶¶156-159. Furthermore, in light of the similarity of the disclosures of the ’024 Patent and the prior art references considered here, the same analysis applies under any reasonable construction of the claims.

1. Claim 1 is Unpatentable

222. In my opinion, Claim 1 is unpatentable because it is obvious in view of Grounds 1-6. As discussed above, *supra at* ¶¶153-155, the limitations of claim 1 of the 024 Patent correspond to claim limitations of the ’623, ’218, and ’595 patents, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 (’623 FWD), pp.9-20; EX1102 (’218 FWD), pp.15-53; EX1103 (’595 FWD), pp.16-53.

a) [1.a] Preamble

223. The preamble of Claim 1 requires “*[a] memory module operable with a memory controller of a host system, comprising*.” As discussed above, *supra at* ¶¶153-155, the limitations of claim element [1.a] of the 024 Patent correspond to claim element [1.a] of the ’623 patent, and claim element [1.a] of the ’218 and ’595 patents, which the Board already found obvious over the combination of

Hazelzet and Buchmann. EX1034 ('623 FWD), p.9; EX1102 ('218 FWD), p.44; EX1103 ('595 FWD), p.44.

224. Hazelzet discloses dual inline memory modules 20 ("DIMMs") that are configured to operate with the "memory controller" 19 of the host system. EX1014 (Hazelzet) at FIGs. 2, 3A-3D, ¶¶[0037], [0038], [0039]; *see also* EX1014 (Hazelzet) at ¶[0036] (referring to DIMMs as "dual inline memory modules").

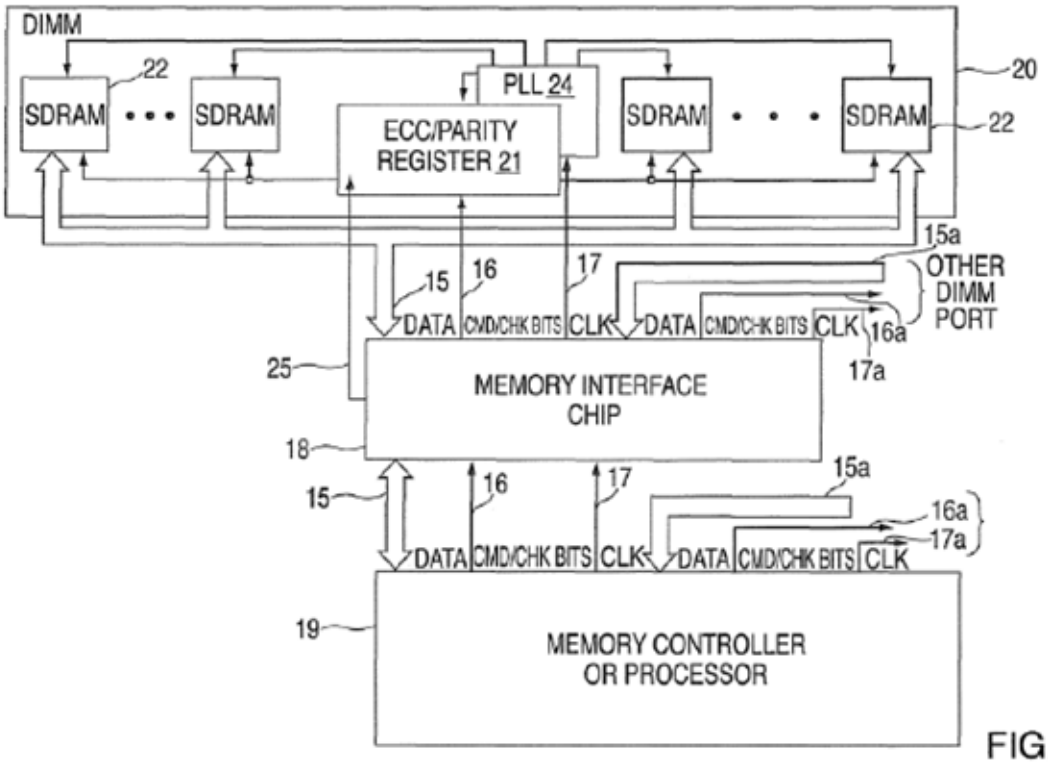


FIG. 2

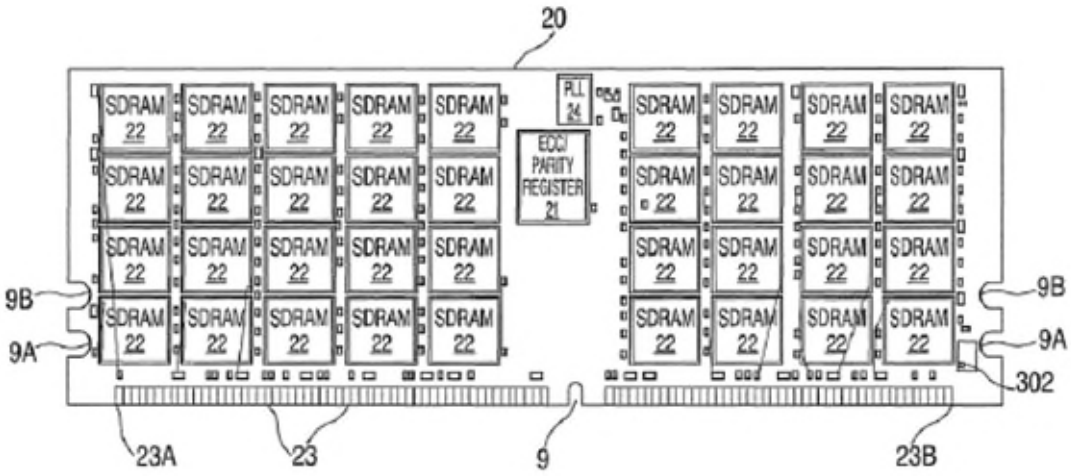
225. Accordingly, to the extent the preamble of claim 1 is limiting, Hazelzet discloses "*[a] memory module operable with a memory controller of a host system.*"

b) [1.b.1] Printed Circuit Board

226. The preamble of claim 1 requires that the memory module is "*a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [1.b.1] of the 024 Patent correspond to claim elements [1.a] and [1.d] of the '623 patent, and claim element [1.b] of the '218 and '595 patents, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-20; EX1102 ('218 FWD), pp.44-46; EX1103 ('595 FWD), pp.44-45.

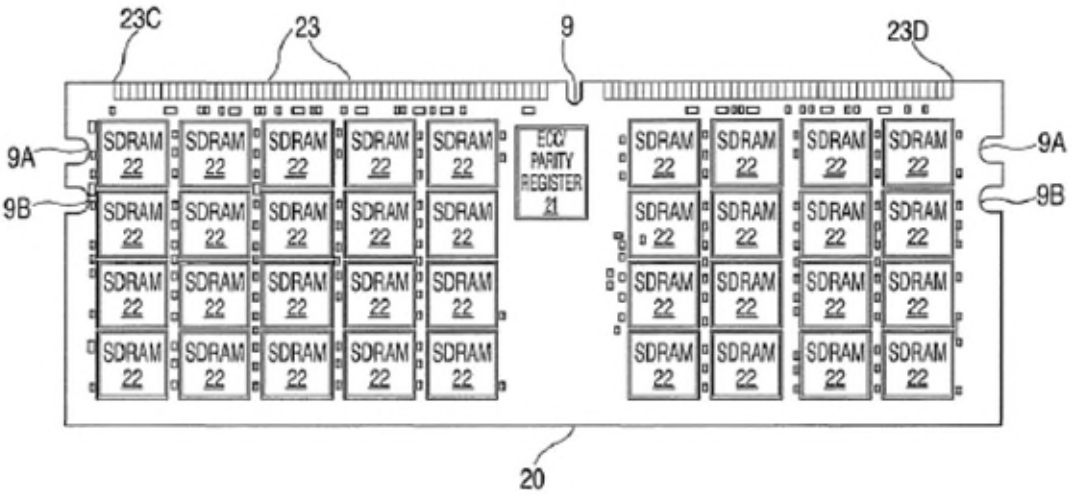
227. Hazelzet explains that the "DIMM of the present invention is comprised of a printed circuit board having a front side and a back side and a plurality of double data rate (DDR) DRAMs or synchronous dynamic random access memories (SDRAMs) affixed to both the front surface and the back surface," EX1014, ¶[0015], examples of which are shown in FIGS. 2, 3A, 3B, 3C, and 3D. *See* EX1014, FIGS. 2, 3A-3D; *see also id*. at ¶[0037] ("Turning now to FIGS. 2, 3A, 3B, 3C, 3D, 4A, 4B, 5, 8, 9, 10 and 11, the enhanced server memory arrangement of the present invention will be described."), ¶[0039], Abstract ("The memory module includes a rectangular printed circuit board having a first side and

a second side, a length of between 149 and 153 millimeters and first and second ends having a width smaller than said length.").



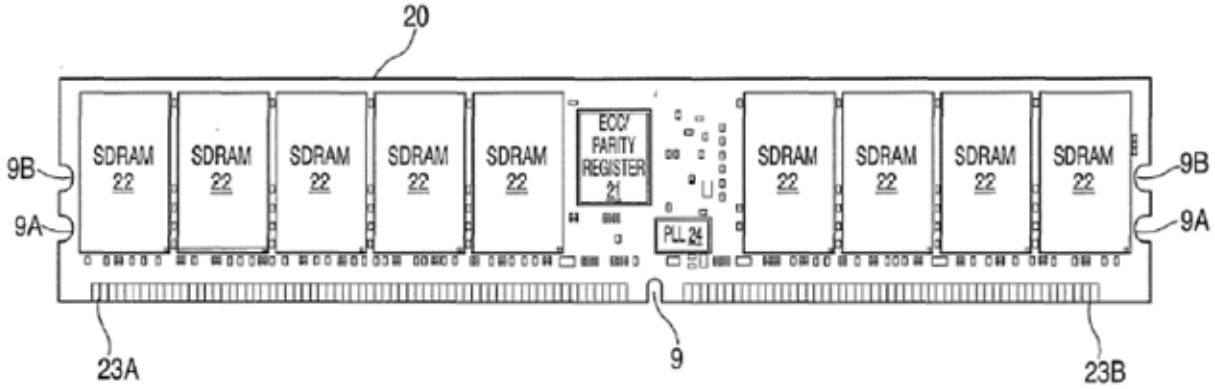
FRONT SIDE OF DIMM - 72 PLANAR

FIG. 3A



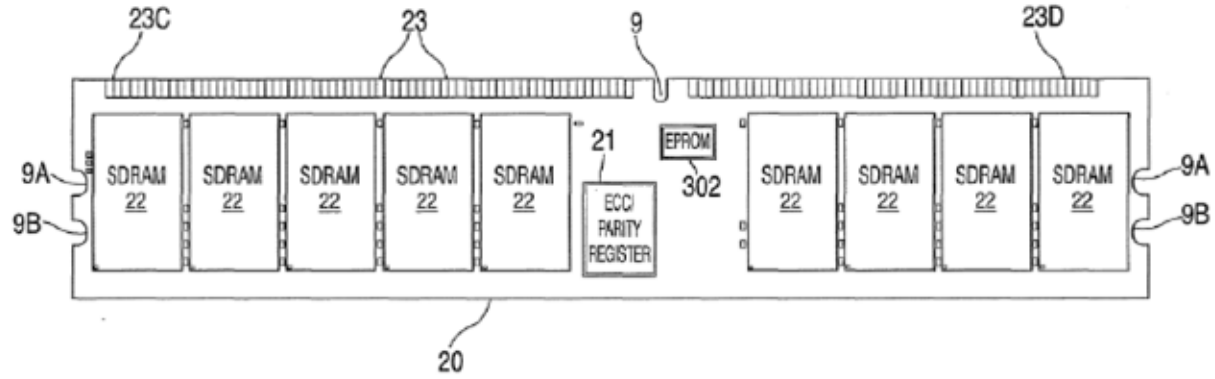
BACK SIDE OF DIMM - 72 PLANAR

FIG. 3B



FRONT SIDE OF DIMM - 4 HIGH STACK

FIG. 3C



BACK SIDE OF DIMM - 4 HIGH STACK

FIG. 3D

228. Hazelzet further explains that its memory modules include "connectors 23 along the edge of both the back and front sides" of the printed circuit board, EX1014 (Hazelzet) at ¶[0039] ("Generally speaking DIMMs are printed circuit cards designed to carry a plurality of DRAMs 22 thereon and the DRAM output pins (not shown) are connected via the printed circuit to selected connectors 23 along the edge of both the back and front sides of the card and are often provided with a single indexing key or notch 9 on the connector edge."),

which are provided to form connections to the memory controller of the host system when the memory module is inserted into a corresponding "slot" of the host system. EX1014 (Hazelzet) at ¶[0097] ("Referring to FIG. 11, column 1102 is the slot in the memory system being occupied by the memory module. ... For memory modules having one buffer chip 21, the IIC address correlates to the slot being occupied by the memory module as shown in column 1106"); *see also id.* at ¶[0032], FIG. 11, FIG. 9 (showing the maximum number of "DIMM slots" for "1, 2, and 4 rank DIMMs.").

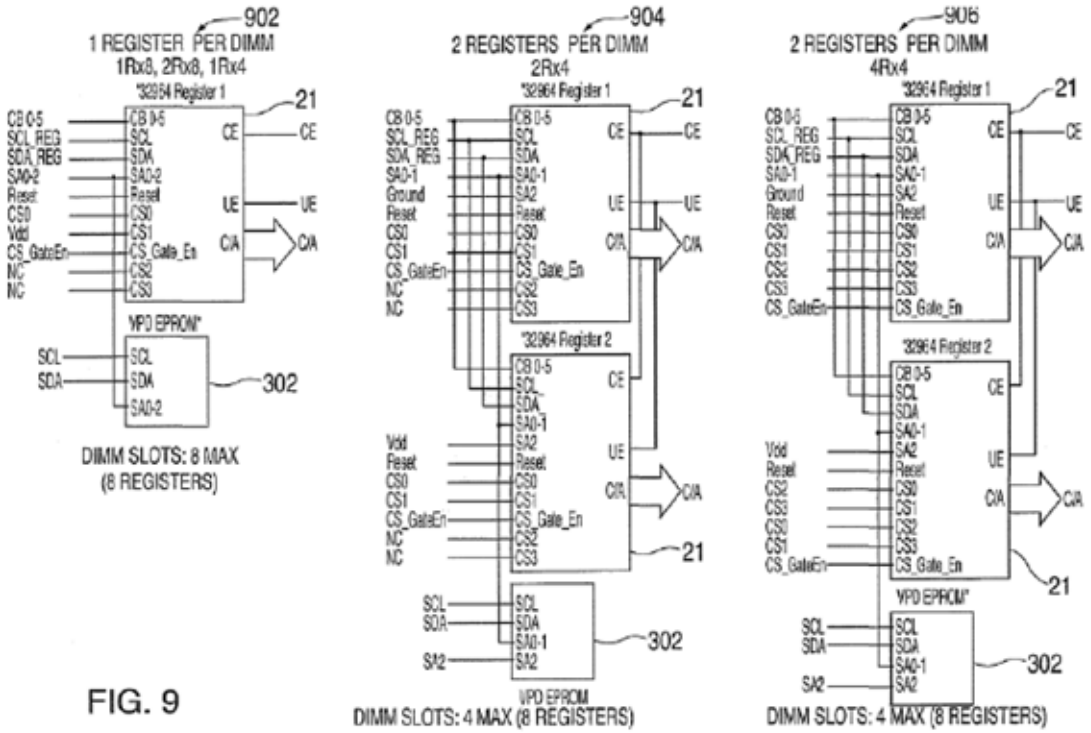


FIG. 9

229. Hazelzet therefore discloses "*a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller.*"

c) [1.b.2] First, Second, and Error Edge Connections

230. The claim requires "*the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [1.b.2] of the 024 Patent correspond to claim element [1.d] of the '623 patent, and claim element [1.b] of the '218 and '595 patents, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-20; EX1102 ('218 FWD), pp.44-46; EX1103 ('595 FWD), pp.44-45.

231. Hazelzet discloses that the printed circuit board has "*first edge connections*" for communicating address and control signals from the memory controller of the host system. EX1014 (Hazelzet) at FIGS. 7A-7C (FIGS. 7A-B reproduced below showing exemplary edge connections for address and control signals annotated green), ¶[0072] (referring to "/CS" as commands), ¶[0068] (listing various address and control signals including "chip select (CS), address (Addr), row address strobe (RAS), column address strobe (CAS) and write enable (WE)" signals); *see also* EX1014 (Hazelzet) at ¶[0038] ("The memory interface chip 18 then sends and receives data, via line 15, to the memory devices or DRAMs 22 and sends address and command information to the register chip 21 via add/cmd line 16 and check bits for error correction purposes to the ECC/ Parity

register chip 21 via line 25."), FIG. 2 (showing address and command line 16), ¶¶[0015], [0035], [0041].

SERVER DIMM PIN NUMBER	PIN NAME
1	Vref
2	SCL
3	SDA
4	UE
5	CE
6	VDD
7	ECCMODE
8	DLY CKE/ODT
9	CS GATE EN
10	GND
11	DQ0
12	DQ1
13	GND
14	DQS0*
15	DQS0
16	GND
17	DQ2
18	DQ3
19	GND
20	VDD
21	GND
22	DQ8
23	DQ9
24	GND
25	DQS1*
26	DQS1
27	GND
28	DQ10
29	DQ11
30	GND
31	DQ16
32	DQ17
33	GND
34	DQS2*
35	DQS2
36	GND
37	DQ18
38	DQ19
39	GND
40	RESET
41	VDD
42	GND
43	DQ24
44	DQ25
45	GND
46	DQS3*
47	DQS3
48	GND
49	DQ26
50	DQ27
51	GND
52	CB0

SERVER DIMM PIN NUMBER	PIN NAME
139	Vref
140	SCL
141	SDA
142	UE
143	CE
144	VDD
145	ECCMODE
146	DLY CKE/ODT
147	CS GATE EN
148	GND
149	DQ4
150	DQ5
151	GND
152	DQS9
153	DQS9*
154	GND
155	DQ6
156	DQ7
157	GND
158	VDD
159	GND
160	DQ12
161	DQ13
162	GND
163	DQS10
164	DQS10*
165	GND
166	DQ14
167	DQ15
168	GND
169	DQ20
170	DQ21
171	GND
172	DQS11
173	DQS11*
174	GND
175	DQ22
176	DQ23
177	GND
178	RESET
179	VDD
180	GND
181	DQ28
182	DQ29
183	GND
184	DQS12
185	DQS12*
186	GND
187	DQ30
188	DQ31
189	GND
190	CB4

FIG. 7A

53	CB1
54	GND
55	DQS8*
56	DQS8
57	GND
58	CB2
59	CB3
60	GND
61	VDD
62	CKE1
63	CHKBT4
64	CHKBT5
65	CKE0
66	VDD
67	A15
68	BA2
69	CHKBT0/PTY
70	A11
71	VDD
72	A7
73	A5
74	A4
75	A2
76	VDD
77	CK0
78	CK0B
79	VDD
80	GND
81	VDD
82	A10
83	BA0
84	WE
85	VDD
86	CS0
87	CAS
88	0DT0
89	CS3
90	VDD
91	CS1
92	ODT1
93	CS2
94	VDD
95	GND
96	DQ32
97	DQ33
98	GND
99	DQS4*
100	DQS4
101	GND
102	DQ34

191	CB5
192	GND
193	DQS17
194	DQS17*
195	GND
196	CB6
197	CB7
198	GND
199	VDD
200	CKE1
201	CHKBT1
202	CHKBT3
203	CKE0
204	VDD
205	A14
206	A12
207	A9
208	CHKBT2
209	VDD
210	A8
211	A6
212	A3
213	A1
214	VDD
215	CK0
216	CK0B
217	VDD
218	GND
219	VDD
220	A0
221	BA1
222	RAS
223	VDD
224	CS0
225	CS3
226	0DT0
227	A13
228	VDD
229	CS1
230	0DT1
231	CS2
232	VDD
233	GND
234	DQ36
235	DQ37
236	GND
237	DQS13
238	DQS13*
239	GND
240	DQ38

FIG. 7B

232. Hazelzet further discloses that the printed circuit board has "*second edge connections*" for communicating data signals between the memory module and the memory controller of the host system. EX1014 (Hazelzet) at FIGS. 7A-7C (FIGS. 7A-B reproduced above showing exemplary data, DQ, edge connections annotated blue). Hazelzet's "*second edge connections*" (DQ) are used for data communication while the memory module is in either the "parity mode" or the

"ECC mode." *Id*. at Fig. 2 (showing data connections 15 to SDRAMs 22 separate from the ECC/Parity register 21), ¶¶[0015], [0035], [0038], [0041].

233. Hazelzet further explains that the printed circuit board has "*an error edge connection in addition to the first edge connections and the second edge connections*," the "*error edge connection*" coupled to the open-drain output of the module controller. EX1014 (Hazelzet) at FIG. 7A (reproduced above showing error edge connections annotated red, including an uncorrectable error pin UE (4, 142) of the memory module that is coupled to the open drain output "/Error (UE)" 121); *see also id*. at FIG. 4B, ¶¶[0072], [0109].

234. Accordingly, Hazelzet discloses "*the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections*."

d) [1.c.1] Module Controller

235. The claim requires "*a module controller on the printed circuit board*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [1.c.1] of the 024 Patent correspond to claim elements [1.a], [1.b], and [1.d] of the '623 patent, and claim element [1.d] of the '218 and '595 patents, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-20; EX1102 ('218 FWD), pp.46-47; EX1103 ('595 FWD), pp.45-46.

Samsung Electronics Co., Ltd.
Ex. 1003, p. 201

236. Hazelzet discloses "*a module controller on the printed circuit board,*" the "*module controller*" including one or more "ECC/Parity register" 21 on the DIMM's printed circuit board. EX1014 (Hazelzet) at FIG. 2 (reproduced below, showing an ECC/Parity register on a DIMM), FIGS. 3A-3D (reproduced below, showing an ECC/Parity register on each side of a DIMM), FIGS. 4A-4B (showing details of the ECC/Parity register), ¶¶[0041], [0044], FIG. 9, [0032] ("FIG. 9 shows the buffer connections and total number of buffers used in a system when the buffer of the present invention is used on 1, 2 and 4 rank DIMMs;"). As shown in FIGS. 2, 3A, 3B, 3C, and 3D, the "ECC/Parity register" is "*on the printed circuit board*." EX1014 (Hazelzet) at FIGS. 3A-3D, ¶[0039] ("Further, as shown in FIG. 3A on the front of each DIMM 20, in addition to the DRAMs, there is positioned a phase locked loop (PLL) chip 24 and the novel ECC/Parity Buffer chip 21 of the present invention."), ¶[0042].

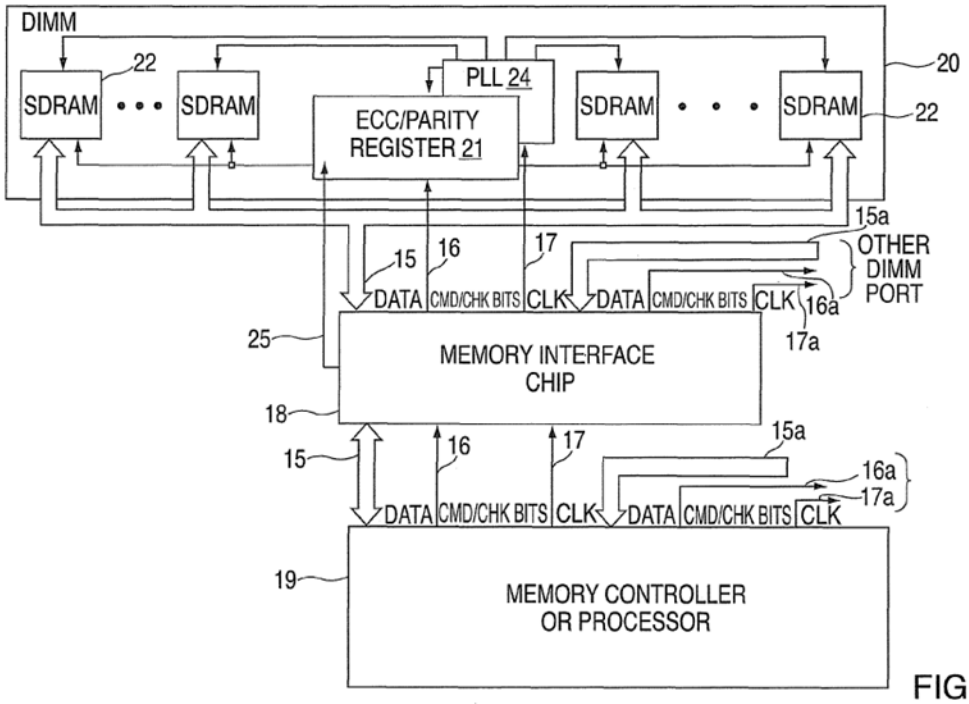
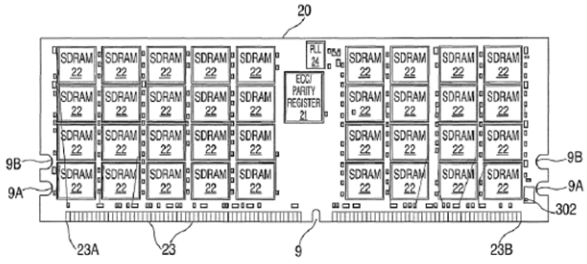
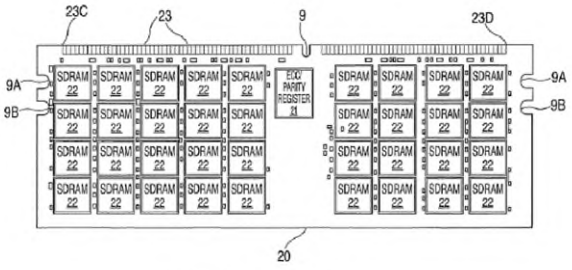


FIG. 2



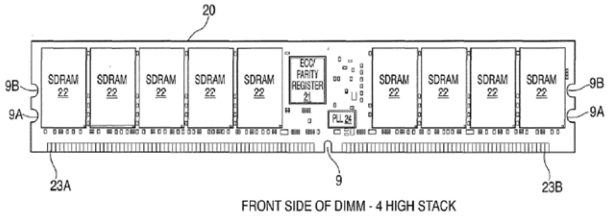
FRONT SIDE OF DIMM - 72 PLANAR

FIG. 3A



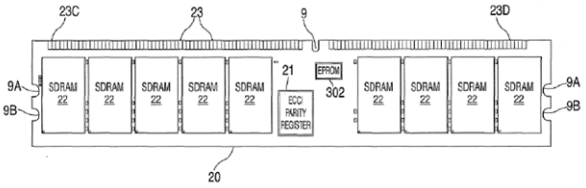
BACK SIDE OF DIMM - 72 PLANAR

FIG. 3B



FRONT SIDE OF DIMM - 4 HIGH STACK

FIG. 3C



BACK SIDE OF DIMM - 4 HIGH STACK

FIG. 3D

237. Accordingly, Hazelzet discloses "*a module controller on the printed circuit board*."

e) [1.c.2] Receive Address and Control Signals

238. The claim requires the "*module controller … configured to receive address and control signals associated with normal memory read or write operations via the first edge connections*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [1.c.2] of the 024 Patent correspond to claim element [1.d] and claim 2 of the '623 patent, and claim element [1.g.i] of the '218 patent and [1.f.i] of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), pp.50-51; EX1103 ('595 FWD), pp.48-49.

239. Hazelzet discloses that "as shown in this FIG. 2, the memory interface chip 18 sends and receives data from the DIMMs via the data line 15 and sends address and commands via line 16." EX1014, ¶[0038], FIG. 2 (reproduced below).

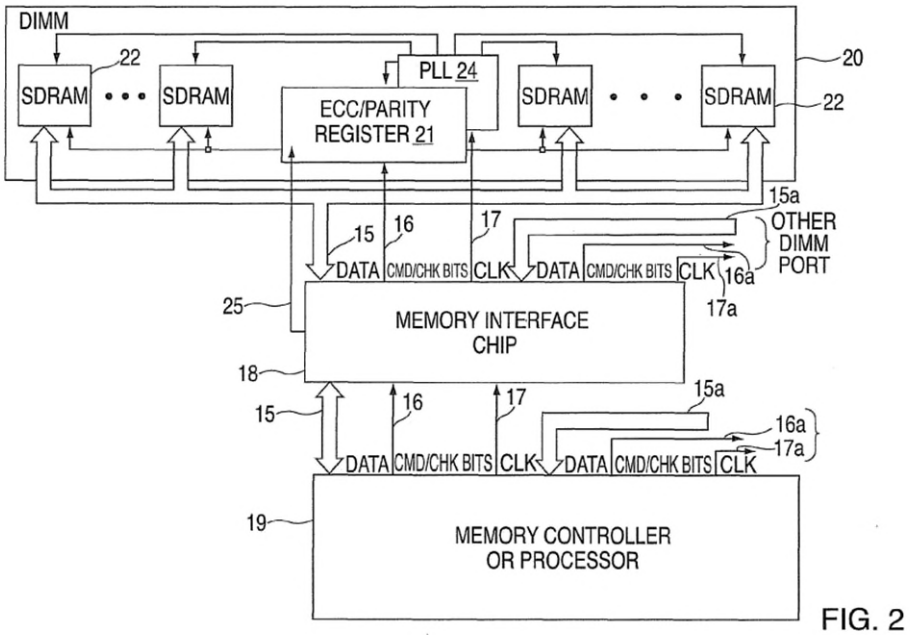


FIG. 2

Fig. 2 of Hazelzet shows line 15 coupling the memory controller 19 and the SDRAMs 22, and line 16 coupling the memory controller 19 and the register 21. *Id*. A Skilled Artisan would have understood from Figure 2 that lines 15 and 16 are coupled to edge connectors for data and address/control, respectively, since those lines couple the DIMM to the memory controller. Indeed, Hazelzet shows that its module receives "*address and control signals*" (green) "*via the first edge connections*," EX1014 at FIG. 7B (reproduced below left, annotated), and those "*address and control signals*" are subsequently received by the "*module controller*," including ECC/Parity register, *id*. at Fig. 4A (reproduced below right, annotated). Indeed, Hazelzet's Figs. 4A and 4B illustrate the ECC/Parity register 21, which buffers the address and command signals on line 16, as shown in Fig. 2 of Hazelzet. *Id*. at Fig. 2 and 4A-4B, [0027] and [0044]. Thus, a Skilled Artisan would have readily understood that, in addition to the CS, CKE, ODT and RST control lines expressly enumerated in Fig. 4A, the "twenty two data lines 32a through 32n" illustrated in Fig. 4A as D0-D21 are also part of the address and command line 16. *Id*. at [0048]; *see also* id. at Fig. 7 (showing 16 address lines A0-A15, three bank address lines BA0-BA2, and command signals RAS, CAS, and WE, adding up to twenty two address and command lines).

53	CB1	191	CB5
54	GND	192	GND
55	DQS8*	193	DQS17
56	DQS8	194	DQS17*
57	GND	195	GND
58	CB2	196	CB6
59	CB3	197	CB7
60	GND	198	GND
61	VDD	199	VDD
62	CKE1	200	CKE1
63	CHKBT4	201	CHKBT1
64	CHKBT5	202	CHKBT3
65	CKE0	203	CKE0
66	VDD	204	VDD
67	A15	205	A14
68	BA2	206	A12
69	CHKBT0/PTY	207	A9
70	A11	208	CHKBT2
71	VDD	209	VDD
72	A7	210	A8
73	A5	211	A6
74	A4	212	A3
75	A2	213	A1
76	VDD	214	VDD
77	CK0	215	CK0
78	CK0B	216	CK0B
79	VDD	217	VDD
80	GND	218	GND
81	VDD	219	VDD
82	A10	220	A0
83	BA0	221	BA1
84	WE	222	RAS
85	VDD	223	VDD
86	CS0	224	CS0
87	CAS	225	CS3
88	ODT0	226	ODT0
89	CS3	227	A13
90	VDD	228	VDD
91	CS1	229	CS1
92	ODT1	230	ODT1
93	CS2	231	CS2
94	VDD	232	VDD
95	GND	233	GND
96	DQ32	234	DQ36
97	DQ33	235	DQ37
98	GND	236	GND
99	DQS4*	237	DQS13
100	DQS4	238	DQS13*
101	GND	239	GND
102	DQ34	240	DQ38

FIG. 7B

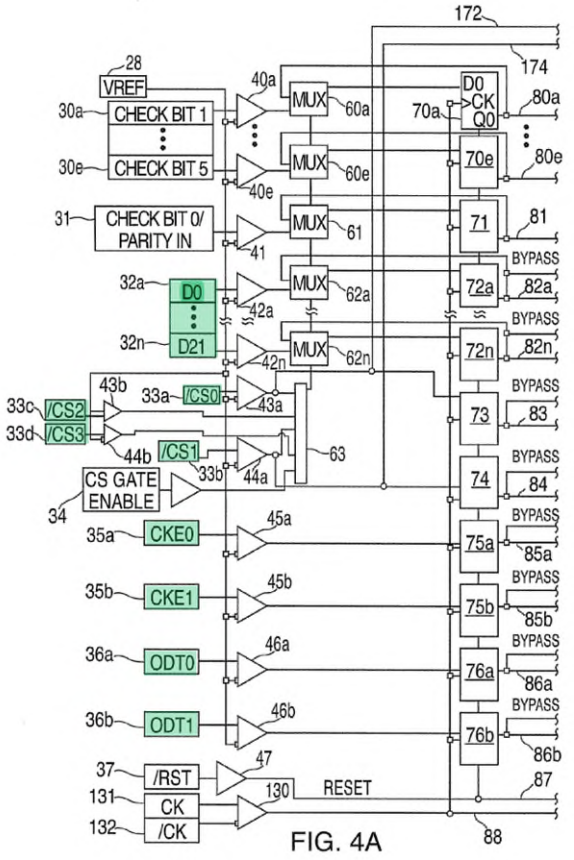


FIG. 4A

Hazelzet further explains that the ECC/Parity register receives the address and control signals and includes buffer circuits to drive those signals to the memory devices. *Id.* ¶[0024] ("FIGS. 4A and 4B are schematic views of the ECC/ Parity register, shown in FIG. 3A;"), ¶[0044] ("FIG. 4A shows the input portion of the … buffer/register segment 21a of the present invention… As depicted in FIGS. 4A and 4B, the buffer chip (also referred to herein as the buffer device) includes a plurality of buffer circuits (e.g., receivers, multiplexers, latches, etc.) for driving the address and command data."). *See also* ¶¶[0015], [0035], [0038], [0041].

Hazelzet therefore discloses that the "*module controller … configured to receive address and control signals … via the first edge connections*."

240. A Skilled Artisan would have also understood that, during normal operations of Hazelzet's module, those "*address and control signals [are] associated with normal memory read or write operations"* in order to write data into and read data from the memory devices of the module SDRAMs (22). For example, Hazelzet expressly discloses address and control signals, including address signals A0-A15 and BA0-BA and control signals RAS, CAS, WE, and CS, which a Skilled Artisan would have understood were used to transmit read and write commands to the memories during normal memory operations in accordance with the well-known JEDEC standards. EX1014, [0068] ("… the inputs … chip select (CS), address (Addr), row address strobe (RAS), column address strobe (CAS) and write enable (WE) …"), [0073] ("signals received by the register (address/command, control signals…)"), [0084] (similar), Fig. 2 (reproduced below, illustrating the address and command lines, green).

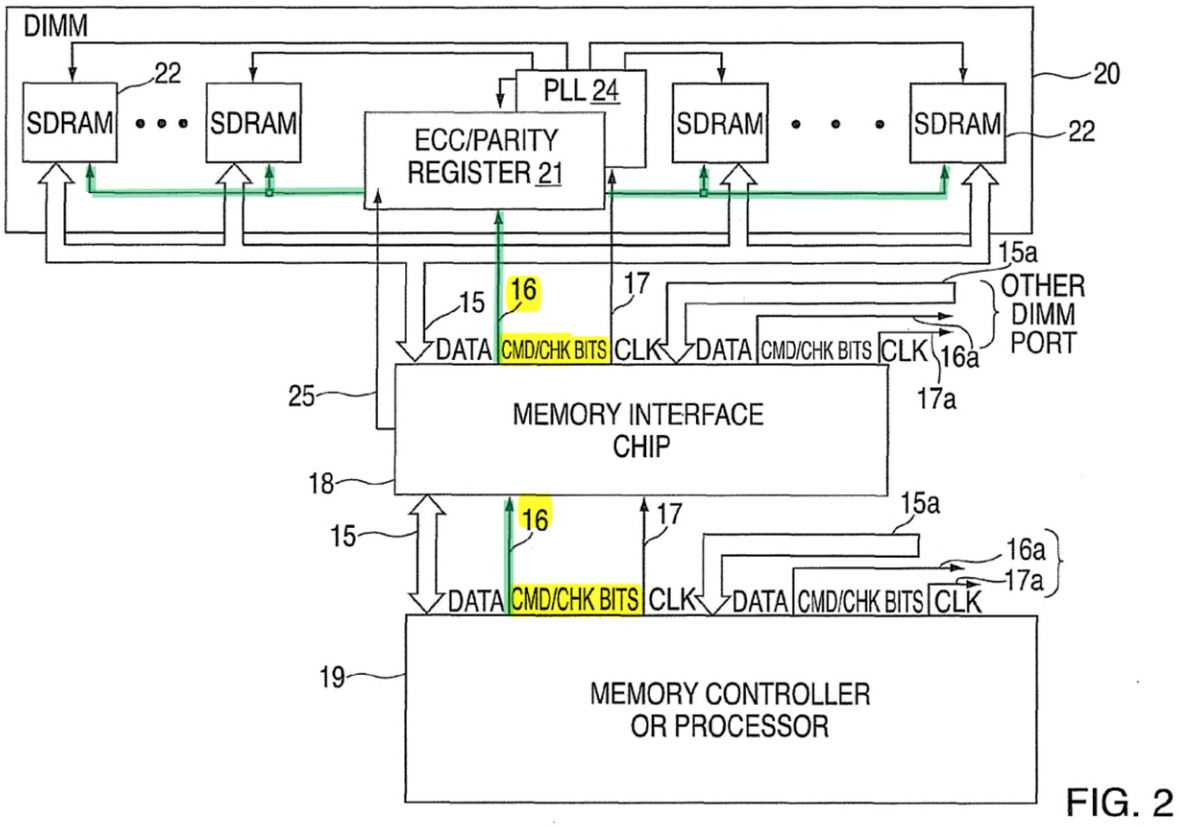


FIG. 2

See also EX1056 (JESD79-3C), p.33 (Command Truth Table, reproduced below, annotated, showing Read and Write commands being conveyed by CS#, RAS#, CAS#, WE# and address signals A0-A15, BA0-BA2); EX1084 (JESD79-2B), 46-47 (Command Truth Table, similar); EX1024 (JESD79), 13 (Truth Table for Commands, similar).

Table 6 — Command Truth Table

Function	Abbreviation	CKE		CS#	RAS#	CAS#	WE#	BA0-BA2	A13-A15	A12-BC#	A10-AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9, 12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11

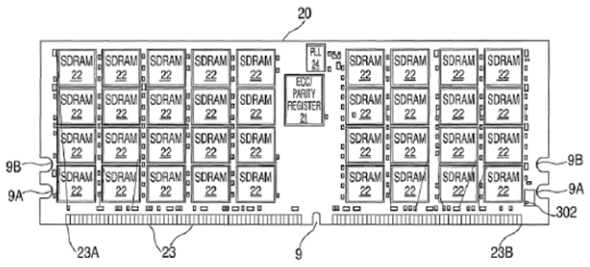
241. Hazelzet therefore discloses that the address and control signals received by the module over the address/control edge connections are associated with "*normal memory read or write operations.*"

242. Accordingly, Hazelzet discloses the memory controller being "*configured to receive address and control signals associated with normal memory read or write operations via the first edge connections.*"

f) [1.d.1] DRAM

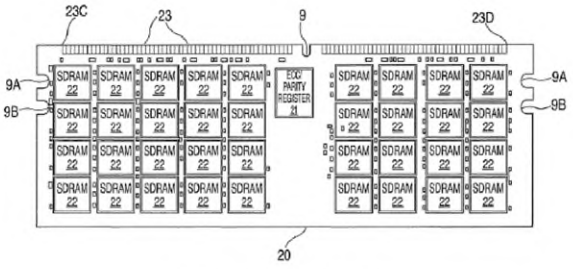
243. The claim requires "*dynamic random access memory elements on the printed circuit board*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [1.d.1] of the 024 Patent correspond to claim elements [1.d], and [1.a] and claim 2 of the '623 patent, and claim element [1.c] of the '218 and '595 patents, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), p.46; EX1103 ('595 FWD), p.45.

244. Hazelzet explains that its memory module (DIMM) includes a plurality of "synchronous dynamic random access memories (SDRAMs)" / "DRAMs" on the "printed circuit board," EX1014 (Hazelzet) at ¶[0015] ("The DIMM of the present invention is comprised of a printed circuit board having a front side and a back side and a plurality of double data rate (DDR) DRAMs or synchronous dynamic random access memories (SDRAMs) affixed to both the front surface and the back surface."), examples of which are shown in FIGS. 2, 3A, 3B, 3C, and 3D. *See* EX1014 (Hazelzet) at FIGs. 2, 3A-3D (reproduced below); *see also id*. at ¶[0037], ¶[0039].



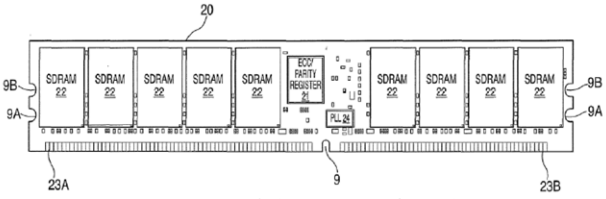
FRONT SIDE OF DIMM - 72 PLANAR

FIG. 3A



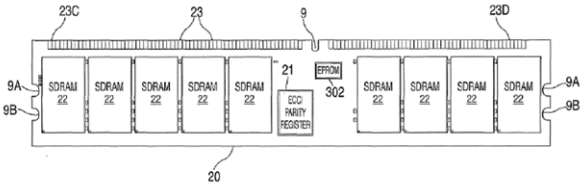
BACK SIDE OF DIMM - 72 PLANAR

FIG. 3B



FRONT SIDE OF DIMM - 4 HIGH STACK

FIG. 3C



BACK SIDE OF DIMM - 4 HIGH STACK

FIG. 3D

245. Accordingly, Hazelzet discloses "*dynamic random access memory elements on the printed circuit board.*"

g) [1.d.2] Communicate Data Signals

246. The claim requires the "*dynamic random access memory elements …configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [1.d.2] of the 024 Patent correspond to claim element [1.d] and claim 2 of the '623 patent, and claim elements [1.f] of the '218 patent and [1.f.ii] of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), pp.47-50; EX1103 ('595 FWD), p.49.

247. Hazelzet discloses that, "as shown in this FIG. 2, the memory interface chip 18 sends and receives data from the DIMMs via the data line 15 and sends address and commands via line 16. The memory interface chip 18 then sends and receives data, via line 15, to the memory devices, or DRAMs 22 and sends address and command information to the register chip 21 via add/cmd line 16." EX1014, ¶[0038]; FIG. 2 (reproduced below).

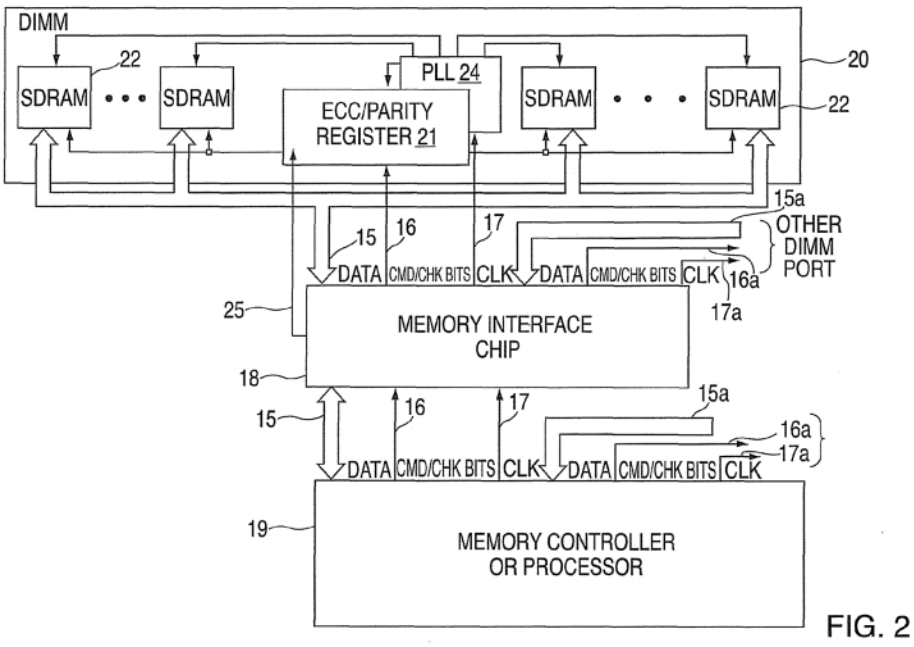


FIG. 2

Hazelzet's Figure 2 shows the SDRAMs 22 using line 15 for communicating data signals with the memory controller for normal memory read and write operations, and line 16 for receiving the address and control signals corresponding to those normal memory read and write operations. *Id*. As discussed above, a Skilled Artisan would have understood, for example from the relevant JEDEC standards, that the SDRAM memories on Hazelzet's module communicate the data signals in

accordance with the address and control signals of the corresponding read or write operations. EX1024, pp.14, 17-45 (explaining communicating data signals for DDR SDAMs in accordance with the address and control signals of the corresponding read and write operations); EX1084, pp.21-38 (similar for DDR2 SDRAMs); EX1056, pp.56-76 (similar for DDR3 SDRAMs).

248. A Skilled Artisan would have also understood that the memory devices in Hazelzet's module communicate the data signals "*via the second edge connections*" (blue) as discussed above. EX1014, FIGS. 2, 7A-7C (7A-B reproduced below, annotated), ¶¶[0015], [0035], [0038], [0041].

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Ex. 1003, p. 213

SERVER DIMM PIN NUMBER	PIN NAME
1	Vref
2	SCL
3	SDA
4	UE
5	CE
6	VDD
7	ECCMODE
8	DLY CKE/ODT
9	CS GATE EN
10	GND
11	DQ0
12	DQ1
13	GND
14	DQS0*
15	DQS0
16	GND
17	DQ2
18	DQ3
19	GND
20	VDD
21	GND
22	DQ8
23	DQ9
24	GND
25	DQS1*
26	DQS1
27	GND
28	DQ10
29	DQ11
30	GND
31	DQ16
32	DQ17
33	GND
34	DQS2*
35	DQS2
36	GND
37	DQ18
38	DQ19
39	GND
40	RESET
41	VDD
42	GND
43	DQ24
44	DQ25
45	GND
46	DQS3*
47	DQS3
48	GND
49	DQ26
50	DQ27
51	GND
52	CB0

SERVER DIMM PIN NUMBER	PIN NAME
139	Vref
140	SCL
141	SDA
142	UE
143	CE
144	VDD
145	ECCMODE
146	DLY CKE/ODT
147	CS GATE EN
148	GND
149	DQ4
150	DQ5
151	GND
152	DQS9
153	DQS9*
154	GND
155	DQ6
156	DQ7
157	GND
158	VDD
159	GND
160	DQ12
161	DQ13
162	GND
163	DQS10
164	DQS10*
165	GND
166	DQ14
167	DQ15
168	GND
169	DQ20
170	DQ21
171	GND
172	DQS11
173	DQS11*
174	GND
175	DQ22
176	DQ23
177	GND
178	RESET
179	VDD
180	GND
181	DQ28
182	DQ29
183	GND
184	DQS12
185	DQS12*
186	GND
187	DQ30
188	DQ31
189	GND
190	CB4

FIG. 7A

53	CB1
54	GND
55	DQS8*
56	DQS8
57	GND
58	CB2
59	CB3
60	GND
61	VDD
62	CKE1
63	CHKBT4
64	CHKBT5
65	CKE0
66	VDD
67	A15
68	BA2
69	CHKBT0/PTY
70	A11
71	VDD
72	A7
73	A5
74	A4
75	A2
76	VDD
77	CK0
78	CK0B
79	VDD
80	GND
81	VDD
82	A10
83	BA0
84	WE
85	VDD
86	CS0
87	CAS
88	0DT0
89	CS3
90	VDD
91	CS1
92	ODT1
93	CS2
94	VDD
95	GND
96	DQ32
97	DQ33
98	GND
99	DQS4*
100	DQS4
101	GND
102	DQ34

191	CB5
192	GND
193	DQS17
194	DQS17*
195	GND
196	CB6
197	CB7
198	GND
199	VDD
200	CKE1
201	CHKBT1
202	CHKBT3
203	CKE0
204	VDD
205	A14
206	A12
207	A9
208	CHKBT2
209	VDD
210	A8
211	A6
212	A3
213	A1
214	VDD
215	CK0
216	CK0B
217	VDD
218	GND
219	VDD
220	A0
221	BA1
222	RAS
223	VDD
224	CS0
225	CS3
226	0DT0
227	A13
228	VDD
229	CS1
230	0DT1
231	CS2
232	VDD
233	GND
234	DQ36
235	DQ37
236	GND
237	DQS13
238	DQS13*
239	GND
240	DQ38

FIG. 7B

249. Furthermore, as discussed above, the JEDEC proposal, Buchmann, and Wang disclose improvements to Hazelzet's data communication, including buffering the data signals. *Supra* ¶¶198-208. In each of those combinations, the data buffering circuitry is implemented on Hazelzet's memory module between the "*second edge connections*" and the SDRAMs on the module in order for the memory devices to communicate data with the memory controller according to the address and control signals of the normal read and write operations. *Id*.

250. For example, Wang explains in detail how the memory devices communicate data signals with the memory controller through Wang's interface circuit using the system data signal interface 274 on one hand (blue, coupled to the memory controller at the bottom of FIG. 2C), and the memory data signal interface 278 on the other hand (blue, coupled to one or more memory devices at the top of FIG. 2C), in accordance with the address and control signals corresponding to normal memory read and write operations (green):

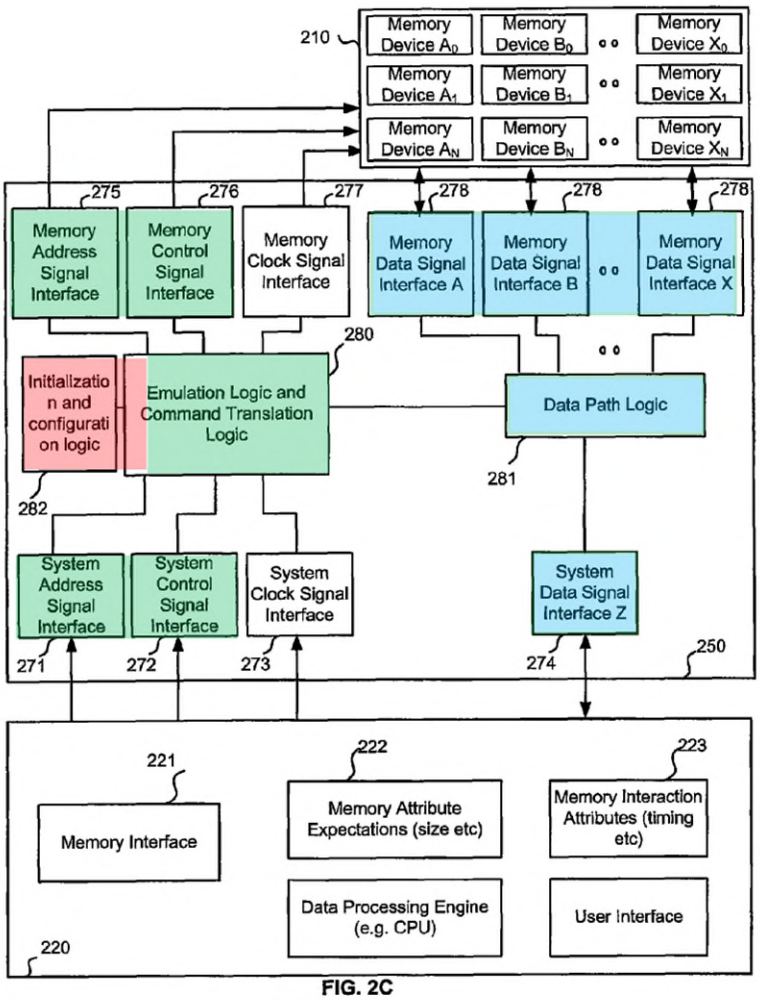


FIG. 2C

EX1090, FIG. 2C (reproduced above showing interfaces, including data signal interfaces 278 to memory devices and system data signal interface 274, and the address and control signal interfaces 275 and 276 to the memory devices and system address and control signal interfaces 271 and 272 from the system).

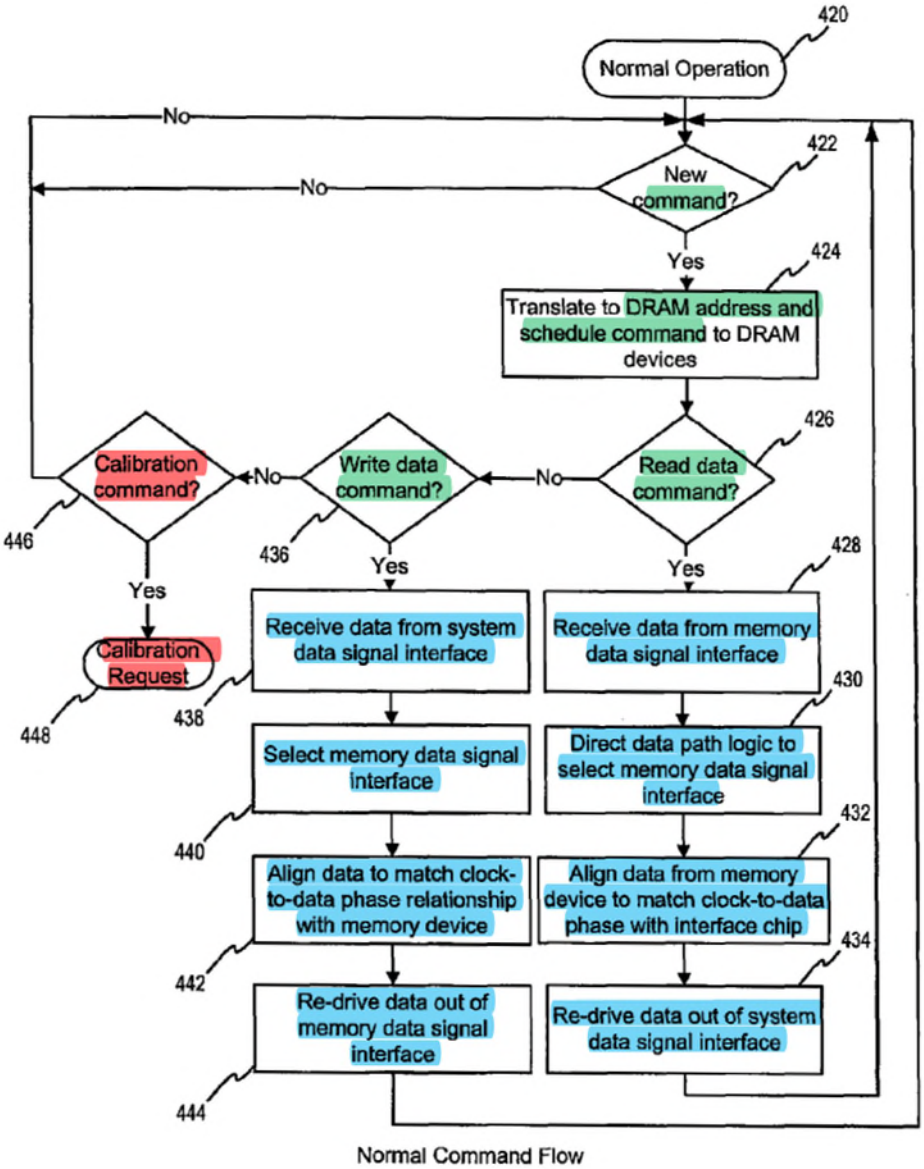


FIG. 4D

EX1090, FIG. 4D (reproduced above explaining processing data (blue) and address and command (green) signals for normal read and write operations through the interface). Wang also explains that its interface is "infrastructure compatible," which would have further motivated to use the functionality of Wang's interface circuit in Hazelzet's system. *Id*. 8:1-10 ("The advantage of the infrastructure-compatible burst merging interface circuit 250 illustrated in FIGS. 2B and 2C and described in greater detail below is that it can provide the higher capacity, higher parallelism that the memory controller desires while retaining the use of the DQS signal in an infrastructure-compatible system to provide the accurate timing reference for data transmission that is critical for modern memory systems, without the cost of the idle cycles required for the multiple bus masters (DRAM devices) to switch from one DRAM device to another.").

251. Similarly, a Skilled Artisan would have understood that, in the JEDEC combination, the "LRDIMM … Memory Buffer (MB) buffers both address and data…[and] is intended to function in all RDIMM platforms with appropriate BIOS changes," therefore motivating her to upgrade Hazelzet's RDIMM to an LRDIMM, since the upgraded module would "function in all RDIMM platforms with appropriate BIOS changes." EX1036, p.5. Buchmann also explains in detail that its memory devices are communicating data signals with the memory controller through Buchmann's memory buffer using the buffer's Memory Device

Data Interface (blue) in accordance address and control signals provided by the buffer's Memory Hub Control (green). EX1016, FIG. 16, 21:20-60.

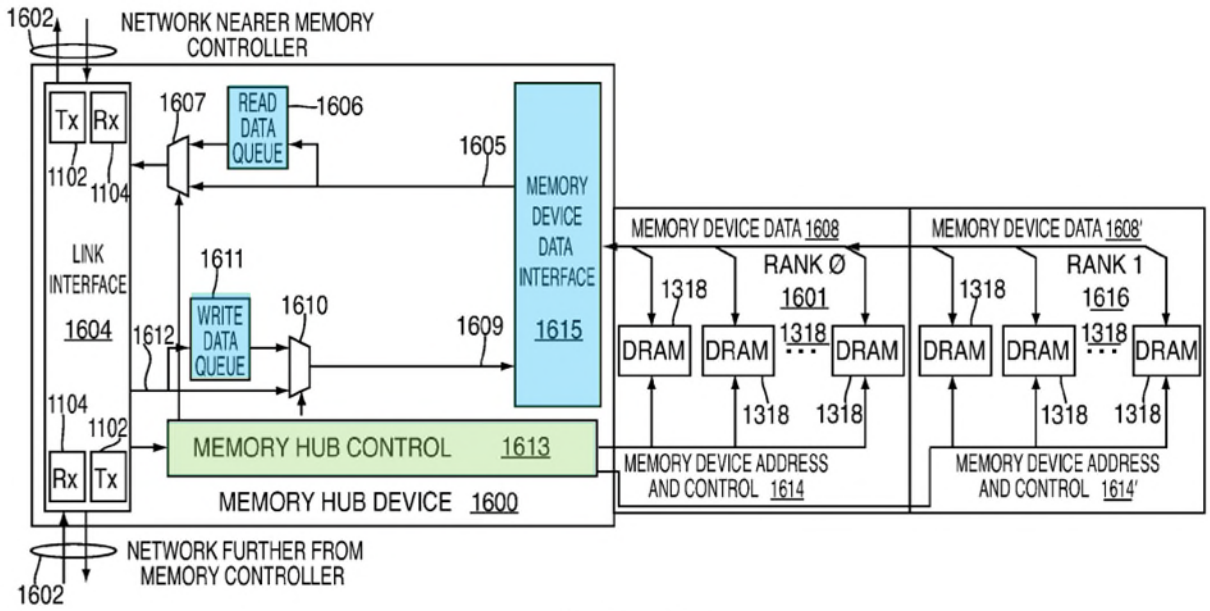


FIG. 16

252. Accordingly, Hazelzet alone or in combination with JEDEC, Buchmann, or Wang discloses the dynamic random access memory elements being "*configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals*."

h) [1.e.1] Transistor

253. The claim requires "*wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [1.e.1] of the 024 Patent correspond to claim element [1.d] and claims 7-8 of the '623 patent, claim element [1.d] and claims 3-4 of the

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’218 patent, and claim element [1.d] and claims 3-4 of the ’595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 (’623 FWD), pp.9-21; EX1102 (’218 FWD), pp.46-47, 62-64; EX1103 (’595 FWD), pp.45-46, 66-69.

254. As explained in claim element [1.b.2], Hazelzet discloses that the “ECC/Parity register” (in the “*module controller*”) has an open-drain output (UE). As discussed above, a Skilled Artisan would have understood that such an open-drain output includes “*a transistor having an open drain…, a source coupled to ground and a gate*.” *Supra* ¶¶46-54. Hazelzet also discloses that its open-drain output is coupled to the error edge connection. *See, e.g.*, EX1014 (Hazelzet), FIGS. 4B, 7A (reproduced below).

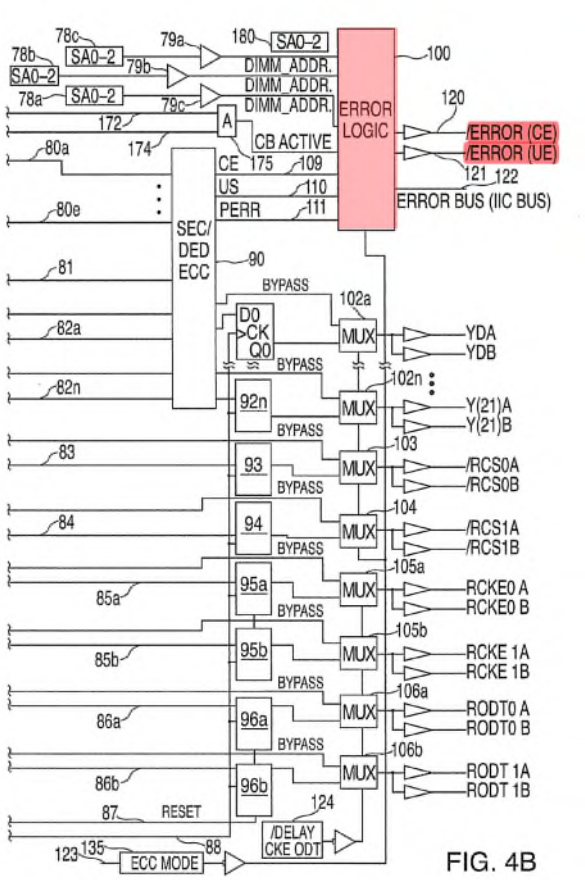


FIG. 4B

SERVER DIMM PIN NUMBER	PIN NAME
1	Vref
2	SCL
3	SDA
4	UE
5	CE
6	VDD
7	ECCMODE
8	DLY CKE/ODT
9	CS GATE EN
10	GND
11	DQ0
12	DQ1
13	GND
14	DQS0*
15	DQS0
16	GND
17	DQ2
18	DQ3
19	GND
20	VDD
21	GND
22	DQ8
23	DQ9
24	GND
25	DQS1*
26	DQS1
27	GND
28	DQ10
29	DQ11
30	GND
31	DQ16
32	DQ17
33	GND
34	DQS2*
35	DQS2
36	GND
37	DQ18
38	DQ19
39	GND
40	RESET
41	VDD
42	GND
43	DQ24
44	DQ25
45	GND
46	DQS3*
47	DQS3
48	GND
49	DQ26
50	DQ27
51	GND
52	CB0

SERVER DIMM PIN NUMBER	PIN NAME
139	Vref
140	SCL
141	SDA
142	UE
143	CE
144	VDD
145	ECCMODE
146	DLY CKE/ODT
147	CS GATE EN
148	GND
149	DQ4
150	DQ5
151	GND
152	DQS9
153	DQS9*
154	GND
155	DQ6
156	DQ7
157	GND
158	VDD
159	GND
160	DQ12
161	DQ13
162	GND
163	DQS10
164	DQS10*
165	GND
166	DQ14
167	DQ15
168	GND
169	DQ20
170	DQ21
171	GND
172	DQS11
173	DQS11*
174	GND
175	DQ22
176	DQ23
177	GND
178	RESET
179	VDD
180	GND
181	DQ28
182	DQ29
183	GND
184	DQS12
185	DQS12*
186	GND
187	DQ30
188	DQ31
189	GND
190	CB4

FIG. 7A

255. In particular, Hazelzet explains that the "ECC/Parity register" has an "error correction code circuit ECC segment 21b" which outputs signals notifying the system memory controller of correctable, uncorrectable, and parity errors. EX1014 (Hazelzet) at ¶[0044] (explaining that the "error correction code circuit ECC segment 21b" is within the "ECC/Parity buffer chip 21," i.e., "ECC/Parity register"). Such "error correction code circuit ECC segment 21b" (within the "ECC/Parity register") includes the circuitry for determining whether the errors occurred, SEC/DED ECC circuit 90, and error logic circuit 100 that receives error signals from SEC/DED ECC circuit 90, such as UE 110 and PERR 111, and

provides the above-mentioned "open-drain output(s)," such as UE 121. EX1014 (Hazelzet) at FIG 4B, ¶¶[0059], [0072] ("Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals). These two outputs are driven low for two clocks to allow the memory controller time to sense the error. /Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic, /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error. Note that the timing of /Error (UE) is different in parity mode vs. ECC mode.").

256. Hazelzet discloses that those "open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error," and further discloses that the "outputs are driven low for two clocks to allow the memory controller time to sense the error. ... /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error."). EX1014, ¶[0072]. Further, Hazelzet explains that its open-drain output is driven "low" (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage), and further explains that the open-drain "output [is] permitted to return to an un-driven state (high impedance)" when the "driver [is] disabled" (i.e., gate receives a low/ground voltage). EX1014

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(Hazelzet) at ¶[0099] ("Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., '0' two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.").

257. As noted above, the combinations analyzed here include a field effect transistor. Indeed, a Skilled Artisan would have understood the phrase "open drain" in the context of Hazelzet's disclosures to necessarily mean the output is driven by a field effect transistor (as opposed to an open collector configuration), and that field effect transistors have three terminals, *i.e.*, gate, source, and drain, that the drain would be connected to the output, the source to ground and the gate to a logic element that performed a selection, e.g., a logical OR operation, of the UE 110 and PERR 111 error signals to drive the gate, as depicted in Figure 5 of Kim. EX1017, FIGS. 4-5, 5:65-6:18; *see also generally* EX1020, U.S. Patent No. 3,414,781 to Dill ("Dill"), entitled "Field Effect Transistor Having Interdigitated Source And Drain And Overlying, Insulated Gate." A Skilled Artisan would have thus understood that the disclosed "open drain" output is the output of "*a transistor having an open drain*" while the "*source*" of that transistor is "*coupled to the*

ground." *See* ¶¶46-54; *see also* EX1017 (Kim) at FIG. 4, 5:49-57, 4:40-48; 6:1-16. Furthermore, even if not inherently disclosed, it would have been obvious to a Skilled Artisan to implement in this fashion given the knowledge of a Skilled Artisan regarding open-drain outputs. *See* ¶¶46-54.

258. The obvious combinations of Hazelzet and JEDEC or Buchmann or Wang therefore satisfy the limitation of "*the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate.*"

259. To the extent one might argue otherwise, this claim limitation would have been obvious in view of Hazelzet, JEDEC or Buchmann or Wang in further view of Kim. Kim discloses an "open drain output" that is an output pin coupled to the drain of a transistor, which includes three ports (*i.e.*, a gate, source, and a drain). *See, e.g.*, EX1017 (Kim) at FIG. 4. In particular, FIG. 4 of Kim shows an open-drain output that is coupled to a pull-up resistor (*i.e.*, connected to a high voltage via a pull-up resistor). FIG. 4 of Kim also shows that the source of the transistor is coupled to ground and that the gate of the transistor is coupled to "ERR."

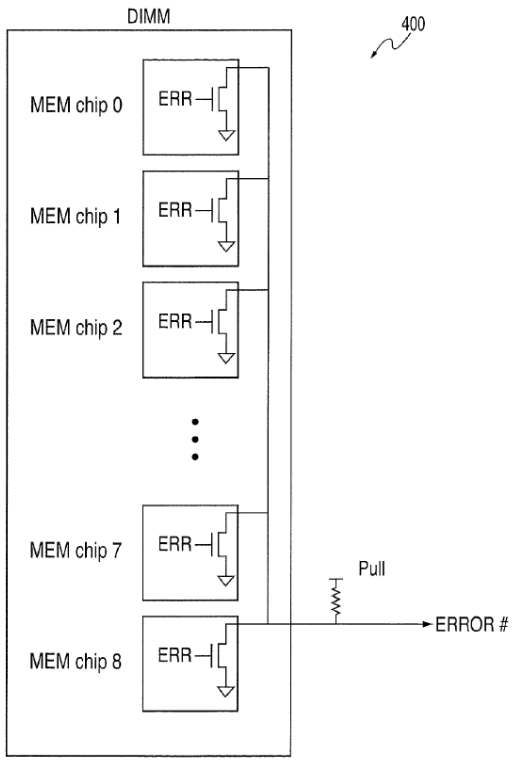


FIG. 4

260. Kim further discloses in Figure 5 the use of a logic element (an OR gate) such that multiple error signals could drive the gate of the open-drain transistor. EX1017, FIG. 5, 6:13-6:18.

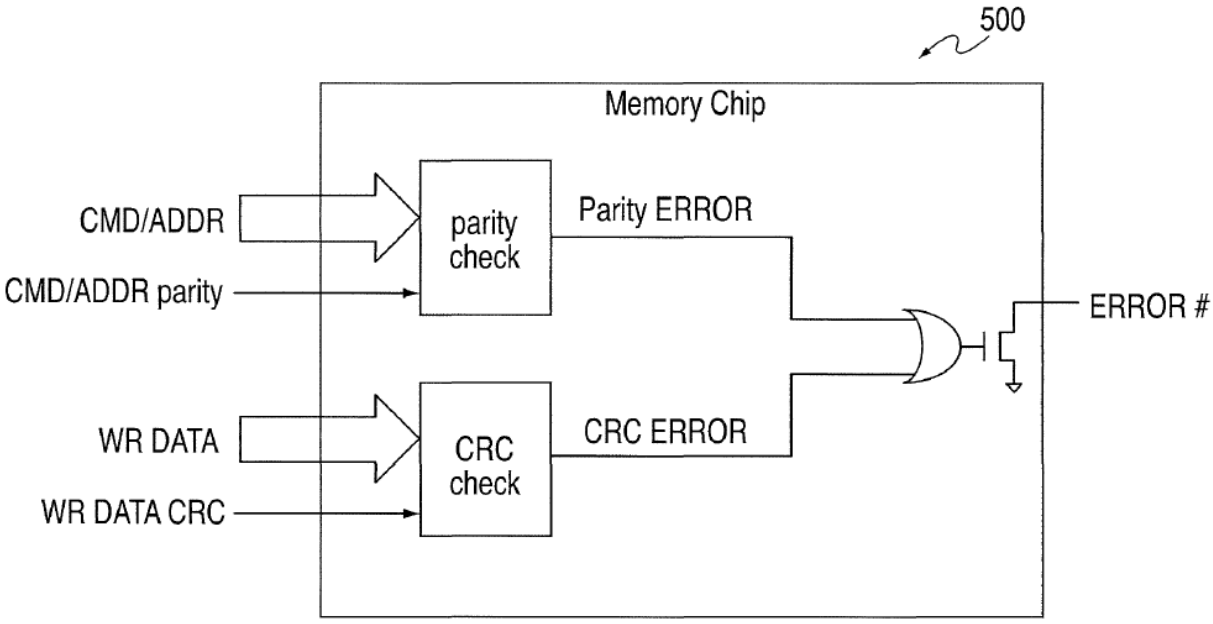
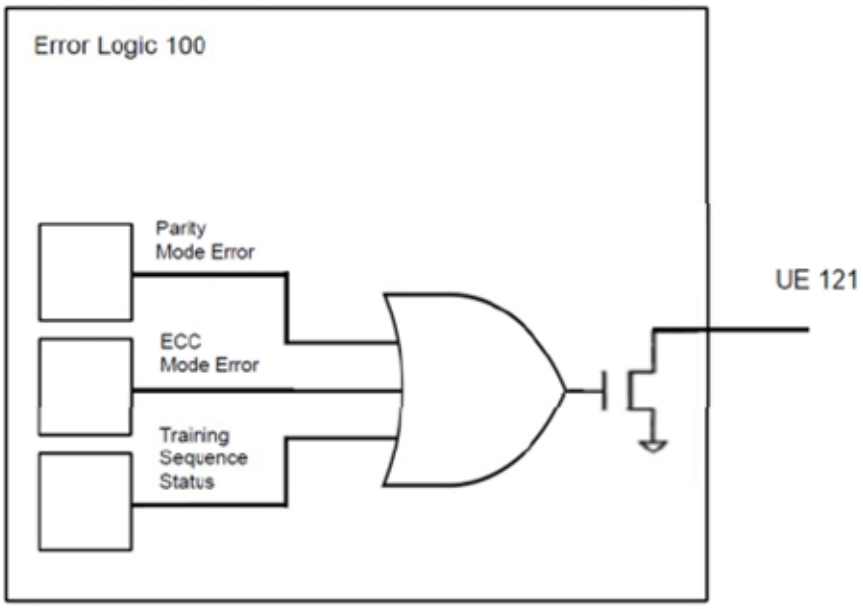


FIG. 5

261. In the combinations analyzed here, Kim's open-drain transistor configuration would be included within Hazelzet's error logic 100 such that signals indicating parity mode error, ECC mode error, and training status would be provided to a logic gate, such as an OR gate, as in Kim, which would select among them based on the mode of the module, as in Hazelzet. The output of the OR gate would be coupled to, and would drive, the gate of an open drain transistor, which itself drives UE 121, as shown in the annotation below:



262. As in Hazelzet, UE 121 is coupled to an error edge connector.

263. As I note above, Hazelzet discloses that UE 121 is used in both Parity Mode and ECC Mode, so there is necessarily logic circuitry within Error Logic 100 for selecting which signal to use to drive the open drain output. Kim uses an OR gate for that function, as in this combination, but a multiplexor would have also worked. It would have been obvious and common sense to use a three input OR gate here, since there are three modes in the modified version of Hazelzet.

264. A Skilled Artisan would understand that, in this combination, each signal input of the OR gate would remain low when the module was not in its associated mode, and the signal whose mode was active could be high to indicate the occurrence of the event to be signaled (error in Parity Mode or ECC Mode; ongoing training in Training Mode), or low to indicate that the event is not

occurring (Parity/ECC) or acknowledge/completed (training). The signal whose mode was active would then be passed through the OR gate to drive the gate of the transistor.

265. I note this is how both Hazelzet and JEDEC employ open drain signaling. For example, Hazelzet discloses that the "ECC/Parity register" (*i.e.*, "*module controller*," as claimed) has "open drain output[s]." EX1014 (Hazelzet) at ¶[0072]. Hazelzet further explains that the "ECC/Parity register" has an "error correction code circuit ECC segment 21b," whose outputs signals notify the system memory controller of correctable, uncorrectable, and parity errors. EX1014 (Hazelzet) at ¶[0044]. Such "error correction code circuit ECC segment 21b" (within the "ECC/Parity register") includes the circuitry for determining whether the errors occurred, SEC/DED ECC circuit 90, and error logic circuit 100 that receives error signals from SEC/DED ECC circuit 90, such as UE 110 and PERR 111, and provides the above-mentioned "open-drain output(s)," such as UE 121. EX1014 (Hazelzet) at FIG 4B, ¶¶[0059],[0072]. Hazelzet discloses that those "open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error," and further discloses that the "outputs are driven low for two clocks to allow the memory controller time to sense the error. ... /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error."). Further, Hazelzet

explains that its open-drain output is driven "low" (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage), and further explains that the open-drain "output [is] permitted to return to an un-driven state (high impedance)" when the "driver [is] disabled" (i.e., gate receives a low/ground voltage). EX1014 (Hazelzet) at ¶[0099] ("Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., '0' two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.").

266. Based upon these disclosures, a Skilled Artisan would have understood Hazelzet's open-drain outputs to be driven by a field effect transistor (as opposed to a bipolar transistor in an open collector configuration), that field effect transistors have three terminals, *i.e.*, gate, source, and drain, that the drain would be connected to the output, the source to ground and the gate to an OR logic element that OR'ed the UE 110 and PERR 111 error signals to drive the gate, as depicted in Figure 5 of Kim. EX1017, FIGs. 4-5, 5:65-6:18.

267. Also, as explained above, *see* ¶¶46-54, a Skilled Artisan would have understood that an open-drain output as set forth in the figure above, *supra*, ¶261,

would be in a high-impedance state when the gate of the transistor is at a logic low level, because the transistor would be off. *See, e.g.*, EX1017 (Kim) at FIG. 4. If all the outputs are in a high impedance state, its voltage would be determined by external circuitry, for example, pulled to a high logic level by the pull-up resistor. EX1014 (Hazelzet) at ¶[0099]. On the other hand, the open drain output would switch to a low logic level (*e.g.*, ground) due to the low impedance path through the transistor when the gate of the transistor is at a logic high level, since the transistor would be on. *Id*.

268. In this combination, as shown in the annotated figure above, the module controller would therefore include "*a transistor having an open drain coupled to the error edge connection, a source coupled to the ground, and a gate*."

269. A Skilled Artisan would have been motivated to combine Kim into the obviousness combination of Hazelzet and JEDEC or Buchmann or Wang for various reasons. Kim was filed approximately a year and a half after Hazelzet and includes some of the same disclosures. It discloses additional details regarding the use of an open-drain output on a memory module to notify the memory controller of errors during a parity normal operating mode and during an ECC normal operating mode. EX1017(Kim) at 1:16-22, 5:49-57, 6:8-16. To use the output-pin scheme of Kim in the system of Hazelzet would therefore have been only the use of known techniques for their known purposes to achieve predictable results, *i.e.*,

using an open-drain output to provide error or status information from multiple components.

270. Kim, Hazelzet, JEDEC, Buchmann, and Wang are analogous art to the 024 Patent because each is directed to the field of memory module design, including error detection and correction, initialization, training and the use of pins/paths for multiple purposes during different operations/modes, EX1001, Abstract, 6:41-56, 8:46-9:23; EX1014, Abstract, ¶¶[0007], [0069]-[0070], [0123]; EX1015, 1, 3, 8; EX1016, 1:7-9, 3:49-60, 4:51-5:50, 12:60-13:41, 14:1-63, 20:20-21:19, 33:45-67; EX1017, 1:16-22, 5:49-57, 6:8-18, 11:20-34, 12:36-53; EX1090 1:5-8, 2:16-18, 9:9-15, and also because Kim, Hazelzet, JEDEC, Buchmann, and Wang are reasonably pertinent to the particular problem the inventor of the 024 Patent was trying to solve, increasing memory module capacity, performance, and/or reliability by sharing an output pin/path to perform multiple functions during multiple operations/modes, including initialization/training, EX1001, Abstract, 6:41-56, 8:46-9:23; EX1014, Abstract, ¶¶[0007], [0069]-[0070], [0123]; EX1015, 1, 3, 8; EX1016, 1:7-9, 3:49-60, 4:51-5:50, 12:60-13:41, 14:1-63, 20:20-21:19, 33:45-67; EX1017, 1:16-22, 5:49-57, 6:8-18, 11:20-34, 12:36-53; EX1090 1:5-8, 2:16-18, 9:9-15.

271. Moreover, a person of ordinary skill in the art would have been motivated to use the open-drain output pin reporting technique of Kim in the

combined scheme of Hazelzet and JEDEC or Buchmann or Wang because it represented a well-known (and therefore reliable) and simple technique to provide error and/or status information from a number of memory components. *See, e.g.*, EX1014 (Hazelzet) at ¶[0072], ¶[0122]; EX1017, FIGs. 4-5, 5:65-6:18, 12:18-23. The open-drain interrupt reporting technique of Kim permitted a single signal line with an OR logic element to indicate error or status information, thus simplifying the design of the system and saving pins on the various integrated circuits connected to the bus, which necessarily can have only a finite number of pins. Thus, a person of ordinary skill in the art could readily have modified Hazelzet's open-drain output with the teachings of Kim and would have been motivated to do so.

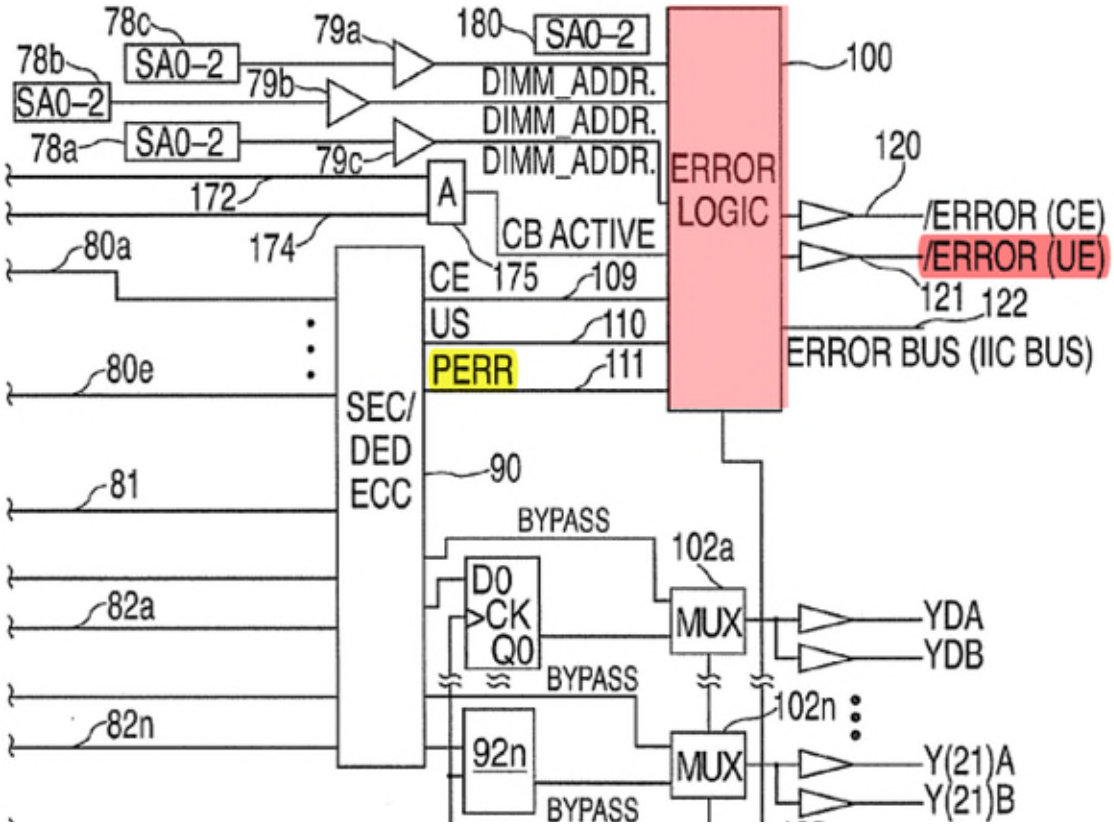
272. Accordingly, Hazelzet alone or in combination with JEDEC or Buchmann or Wang with or without Kim disclose "*wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate*."

i) [1.e.2] Indicate Parity Error

273. Claim 1 requires "*wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation*." As discussed above, *supra at* ¶¶153-155, the limitations of claim

element [1.e.2] of the 024 Patent correspond to claim element [1.b] and claims 2, 7, and 9 of the ’623 patent, claim elements [1.f] and [1.h] and claim 5 of the ’218 patent, and claim elements [1.e.ii] and [1.f.iii] and claim 5 of the ’595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 (’623 FWD), pp.9-21; EX1102 (’218 FWD), pp.47-52, 62-63; EX1103 (’595 FWD), pp.46-47, 50, 69-71.

274. As discussed above, *see* ¶¶253-272, Hazelzet explains that its “ECC/Parity register” (included in the “*module controller*”) has open-drain output, such as Uncorrectable Error (UE) lines capable of utilizing parity error signals (PERR) to output signal UE 121 to the host indicating a parity error. EX1014, ¶¶[0059], [0070], [0072], [0076]. As further discussed above, when the memory module is in the “parity mode,” the “parity generator/checker circuit 231” (within SEC/DED ECC circuit 90) generates and sends the “parity error signal (PERR)” to the “error logic circuit” 100. EX1014 (Hazelzet) at FIG. 4B, FIG. 5 (both reproduced below), ¶¶[0059], [0070], [0072], [0076] (“FIG. 5 is a block diagram of the SEC/DED ECC circuit of FIG. 4B. ... The parity generator/checker circuit 231 further has a second input coupled to the parity in signal source 31 via primary latch 71 and output line 81 and depending on the state of the parity input signal on input 31 sends a parity error signal (PERR) on output line 111 to the error logic circuit 100.”).


78c
SA0-2
78b
SA0-2
78a
SA0-2
79a
79b
79c
180
SA0-2
DIMM_ADDR.
DIMM_ADDR.
DIMM_ADDR.
100
ERROR LOGIC
120
/ERROR (CE)
/ERROR (UE)
121 122
ERROR BUS (IIC BUS)
172
A
CB ACTIVE
174
80a
80e
81
82a
82n
SEC/ DED ECC
CE 175
109
US
110
PERR
111
90
BYPASS
102a
D0
CK
Q0
MUX
YDA
YDB
BYPASS
102n
92n
MUX
Y(21)A
Y(21)B
BYPASS

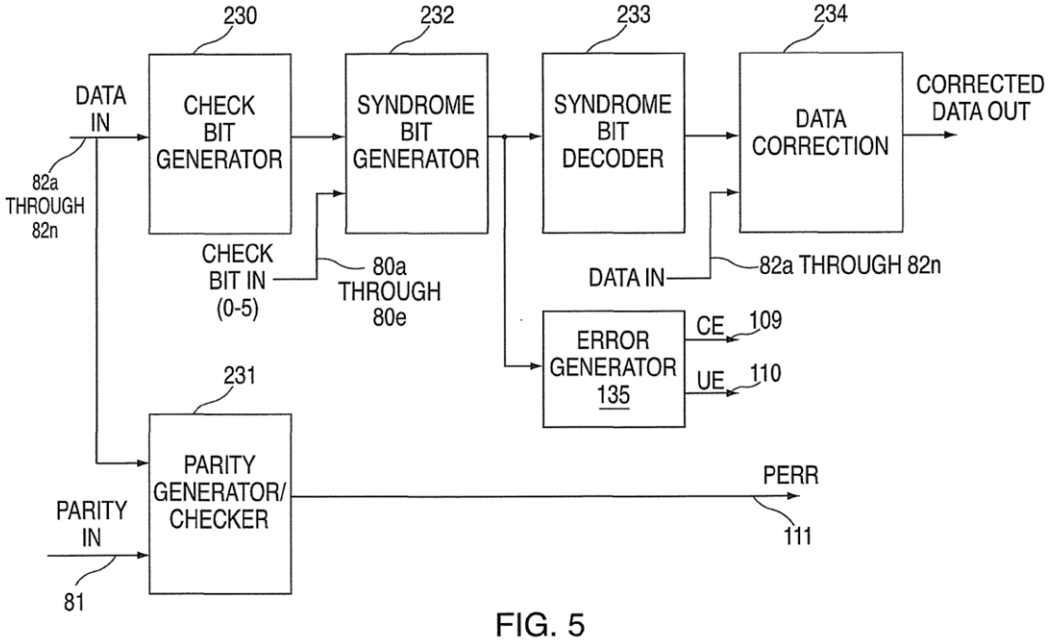

230
232
233
234
DATA IN
82a THROUGH 82n
CHECK BIT GENERATOR
SYNDROME BIT GENERATOR
SYNDROME BIT DECODER
DATA CORRECTION
CORRECTED DATA OUT
CHECK BIT IN (0-5)
80a THROUGH 80e
DATA IN
82a THROUGH 82n
ERROR GENERATOR 135
CE 109
UE 110
231
PARITY GENERATOR/ CHECKER
PARITY IN
81
PERR
111

FIG. 5

275. In particular, Hazelzet explains that in the "parity mode," the parity error "will be reported two clock pulses later via the Uncorrectable Error (UE) line (driven low for two clock pulses)." EX1014 (Hazelzet) at Fig. 8 (reproduced below in part), ¶[0070]; *see also id.* at [0018] ("After holding the error line low for only 2 clock cycles, the driver can be disabled and the output permitted to return to an un-driven state (high impedance) thus allowing this line to be shared by multiple modules.").

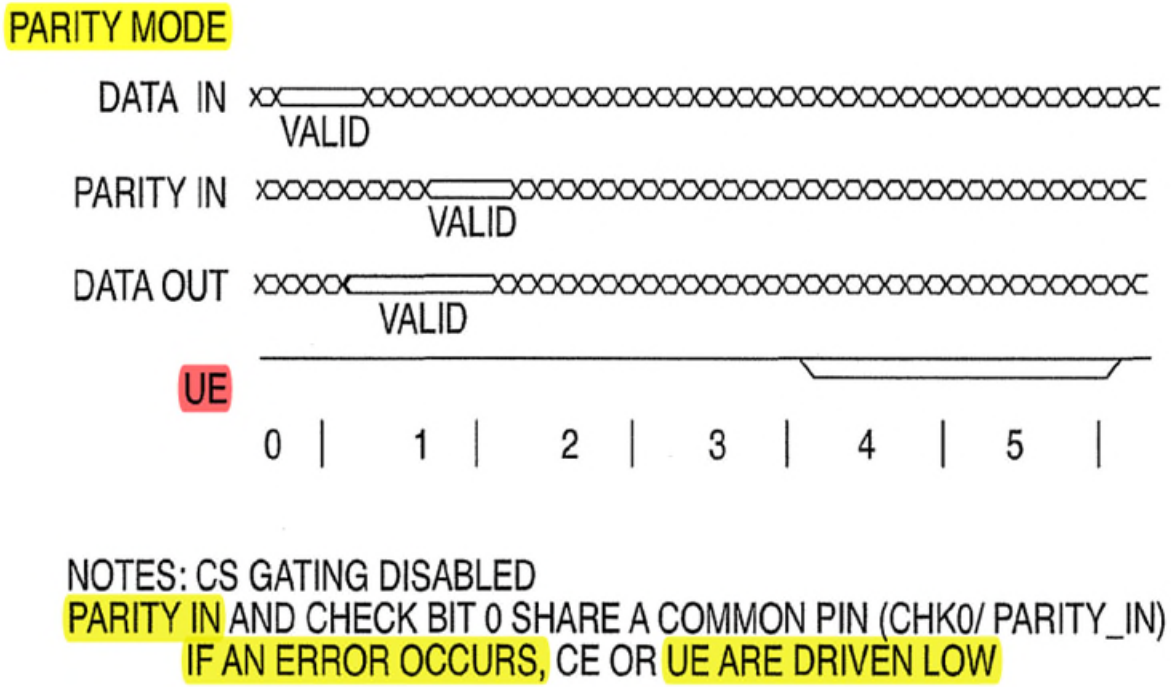


FIG. 8

276. Further, as explained above, *see* ¶¶253-272, Hazelzet discloses that its open-drain output is driven "low" (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage), and further explains that the open-drain "output [is]

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permitted to return to an un-driven state (high impedance)" when the "driver [is] disabled" (i.e., gate receives a low/ground voltage). EX1014 (Hazelzet) at ¶[0099] ("Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., '0' two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules."). Accordingly, a high voltage applied to the gate of the open-drain output's transistor drives the open-drain output low, indicating a parity error in the "parity" mode. *See, e.g.*, ¶¶267, 46-54. Therefore, Hazelzet discloses that "*the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error*."

277. Hazelzet further explains that its "parity" mode is a mode that allows the host system to "determine the error condition" of the memory module. EX1014 (Hazelzet) at ¶[0064] ("A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition."). In Hazelzet, such "error condition" is reported to the host "via the Uncorrectable Error (UE) line" when the memory module is in the "parity mode." EX1014 (Hazelzet) at ¶[0070] ("In addition to the

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above ECC mode, the same twenty two chip select gated data signals can be operated in 'parity mode (/ECC Mode high), whereby the signal received on CHK0/Parity in line is received as parity to the register one clock pulse later than the chip select gated data inputs. The received parity bit is then compared to the parity calculated across these same inputs by the register parity logic to verify that the information has not been corrupted. The twenty two chip select gated data signals will be latched and re-driven on the first clock pulse and any error will be reported two clock pulses later via the Uncorrectable Error (UE) line (driven low for two clock pulses) and in the Error Bus Registers. No correction of errors will be completed in this mode. The convention of parity, in this application, is odd parity (odd numbers of 1s [sic] across data and parity inputs equals valid parity).").

Hazelzet also explains that the error line is driven "low, i.e., '0'," when "an error is detected." EX1014 (Hazelzet) at ¶[0099] ("Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., '0' two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules."), ¶[0018] ("Still another object of the invention is to provide for Parity

error reporting in which the parity signal is delivered one cycle after the address and command to which it applies, and the error line be driven low two clocks after the address and command bits are driven to the DRAMs from the register on the DIMM."), FIG. 8 (explaining that UE is driven low "if an error occurs" in the "parity mode").

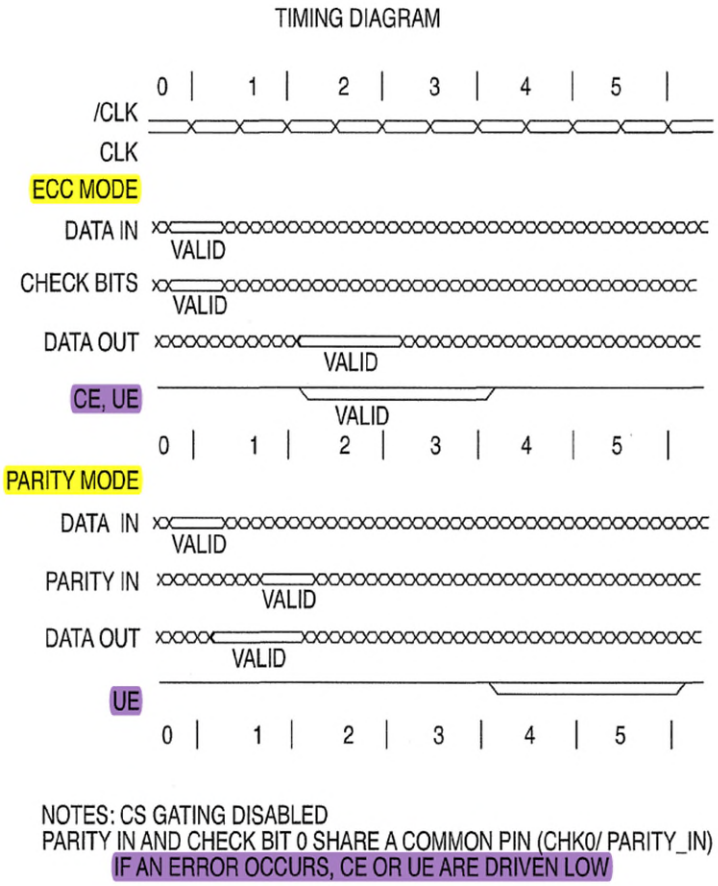


FIG. 8

278. Hazelzet also explains that the generated parity error signal is related to the received address and command signals. EX1014 (Hazelzet) at ¶¶ [0018] ("Still another object of the invention is to provide for Parity error reporting in

which the parity signal is delivered one cycle after the address and command to which it applies…"), [0099] ("Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies…"), [0072] ("Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals)."). Indeed, the inputs to Hazelzet's ECC/Parity register include the address and command signals on line 16 and the corresponding check bits on line 25. EX1014 (Hazelzet) at Fig. 2 (reproduced below), ¶[0038] ("The memory interface chip 18 then … sends address and command information to the register chip 21 via add/cmd line 16 and check bits for error correction purposes to the ECC/ Parity register chip 21 via line 25.").

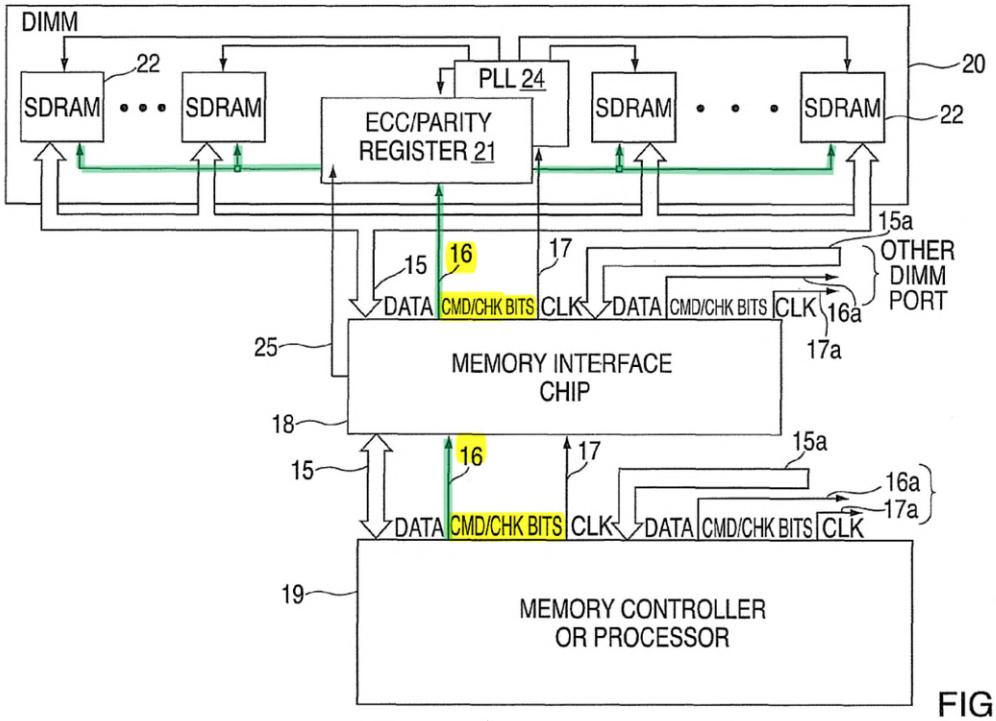


FIG. 2

A Skilled Artisan would have understood that normal memory read and write operations are initiated by a valid command (with a low chip select signal) using such address and command signals. *See*, *e.g.*, EX1056, p.33; *see also* EX1014 (Hazelzet) at ¶[0109] ("Two open-drain outputs are available to permit multiple modules to share a common signal pin for reporting an error that occurred during a valid command (any /CS=low) cycle (consistent with the re-driven signals)"). Therefore, a Skilled Artisan would have also understood that Hazelzet's parity reporting based on the address and command signals of a valid command indicates a parity error "*having occurred when the memory module is being accessed for a normal memory read or write operation.*"

279. Accordingly, Hazelzet alone or in combination discloses "*wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation.*"

j) [1.e.3] Training Sequences

280. Claim 1 requires "*wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [1.e.3] of the 024 Patent correspond to claim element [1.c] and claims 2 and 8 of the '623 patent, claim elements [1.e.ii], [1.f] and [1.i] and claims 4 and 7 of the '218 patent, and claim element [1.e.iii] and claim 7 of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), pp.47-50, 63-64, 67-68; EX1103 ('595 FWD), pp.47-48, 73-74.

281. As demonstrated above, in the combinations analyzed here the open drain output is configured such that the transistor output is driven low (to ground) while training is still occurring and driven high upon completion (by the pull-up

Samsung Electronics Co., Ltd.
Ex. 1003, p. 240

resistor). Moreover, to drive the output low (i.e., to ground), the signal at the gate of the transistor ("*a second signal*" when the module performs operations related to training) must be high, causing the transistor to conduct and connect the drain to ground. On the other hand, the output would be in a high impedance state to allow the output to be driven high (e.g., by a pull-up resistor) when the gate of the transistor is low, turning the transistor off. *See* ¶¶211-220.

282. As also explained above, in any of the obvious combinations of Hazelzet and JEDEC or Buchmann or Wang, the open-drain output would be at a low logic level (i.e., the open-drain output driven low, because the gate would be driven high) to indicate the training operations (e.g., MB-DRAM, TS0 or TS3, Wang's interface training) were in progress, and the open-drain output would be in a high impedance state (because the gate would be driven low) so that the logic level of the open-drain output can be pulled high by a pull-up resistor when those operations completed in each memory module. *See* ¶¶46-54, 211-220. Therefore, Hazelzet alone or in combination with JEDEC or Buchmann or Wang renders obvious that "*the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences.*"

283. As discussed above, each of the combinations also renders obvious that, while the module performs operations related to training, "*the dynamic random access memory elements are not accessed for any normal memory read or write operations.*" *Supra* ¶¶209-210. For example, JEDEC teaches that, during the MB-DRAM training (the training that is added to Hazelzet in the JEDEC combination), "[n]o DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete." EX1015, 8. A Skilled Artisan would have understood from this disclosure that, during such training that is performed by the memory module to train the memory device interface on the memory module, the memory devices are not accessed for any normal memory read or write operations since "[n]o DRAM commands…. over the Command/Address and Control buses … can be issued to the MB until the MB-DRAM Interface training is complete." *Id*.; *see also supra* ¶240 (discussing JEDEC standard for commands); EX1056 (JESD79-3C), pp.33-34 (Command Truth Table), pp.56-76 (examples of normal Read and Write operations); EX1024 (JESD79), p.13 (Truth Table for Commands), pp.17-45 (examples of normal Read and Write operations). Furthermore, a Skilled Artisan would have understood that each of the MB-Training steps, such as Write Leveling, Read Enable training, and Read/Write DQ/DQS training, can be performed using standardized write leveling

mode and a preset data pattern in the Multi-Purpose Register (MPR) of DDR3 memories without any normal memory read or write operations. EX1056, 42-45 (Write leveling), 48-51 (MPR for read calibration).

284. Similarly, Buchmann teaches performing its training during power-on initialization, before any normal operations, such as normal memory read and write operations. *Supra* ¶¶209-210, *see, e.g.*, EX1016 at Abstract ("the memory buffer includes logic for executing a power-on and initialization training sequence initiated by the memory controller"), 5:51-6:50 (describing TS0 training during initialization), 8:24-9:18 (describing TS3 training during initialization). The TS0 and TS3 training does not use any normal operations, such as normal memory read and write operations. *Id*., 6:25-:50 (TABLE 2 listing Clock Detection and Repair Training States without any normal memory operations), 8:50-9:15 (TABLE 6 listing US Lane Training and Repair Training States without any normal memory operations).

285. Wang also teaches that the module returns to normal operations only after all the memory interfaces have been trained. FIG. 4C (reproduced below), 9:58-67 ("The flow diagram of FIG. 4C shows that the memory data signal interfaces 278 are trained sequentially, and after memory data interface A has been trained, memory data interface B is similarly trained, and respective delays set for data interface B. The process is then repeated until all of the memory data signal

interfaces 278 have been trained and respective delays are set. In other embodiments, the respective memory data signal interfaces 278 may be trained in parallel. After the calibration sequence is complete, control returns to the normal flow diagram as illustrated in FIG. 4D.")

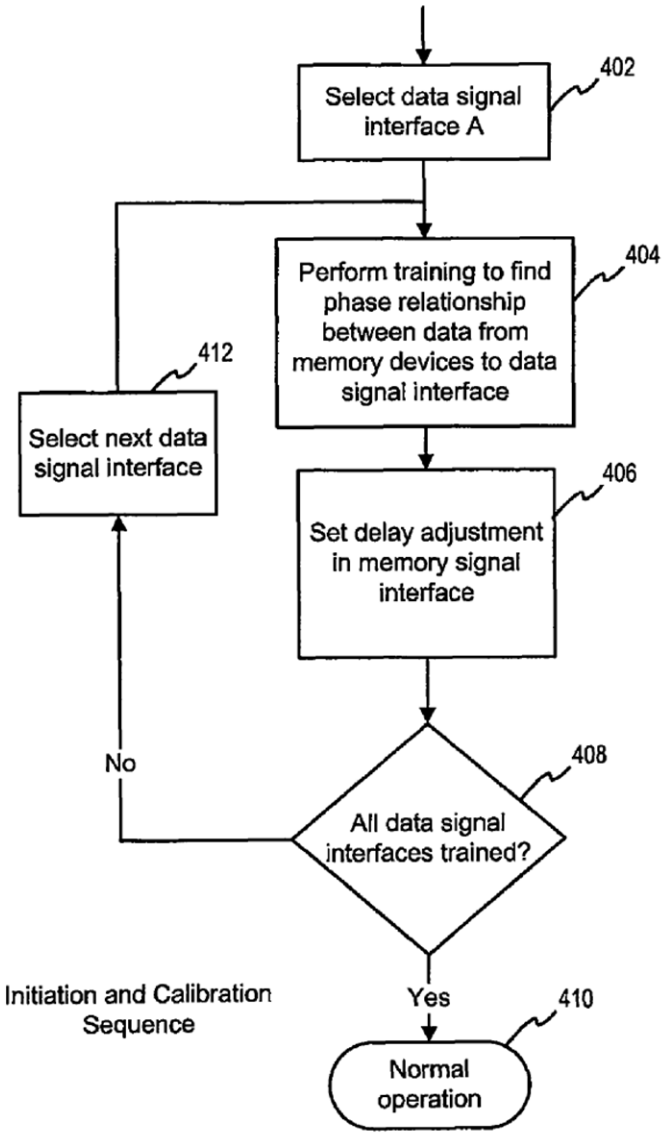


FIG. 4C

As indicated by Wang's Fig. 4C, after completing the training of all the interfaces, the module returns to normal operations, that include normal memory read and write operations, as shown in Wang's FIG. 4D (reproduced below, annotated).

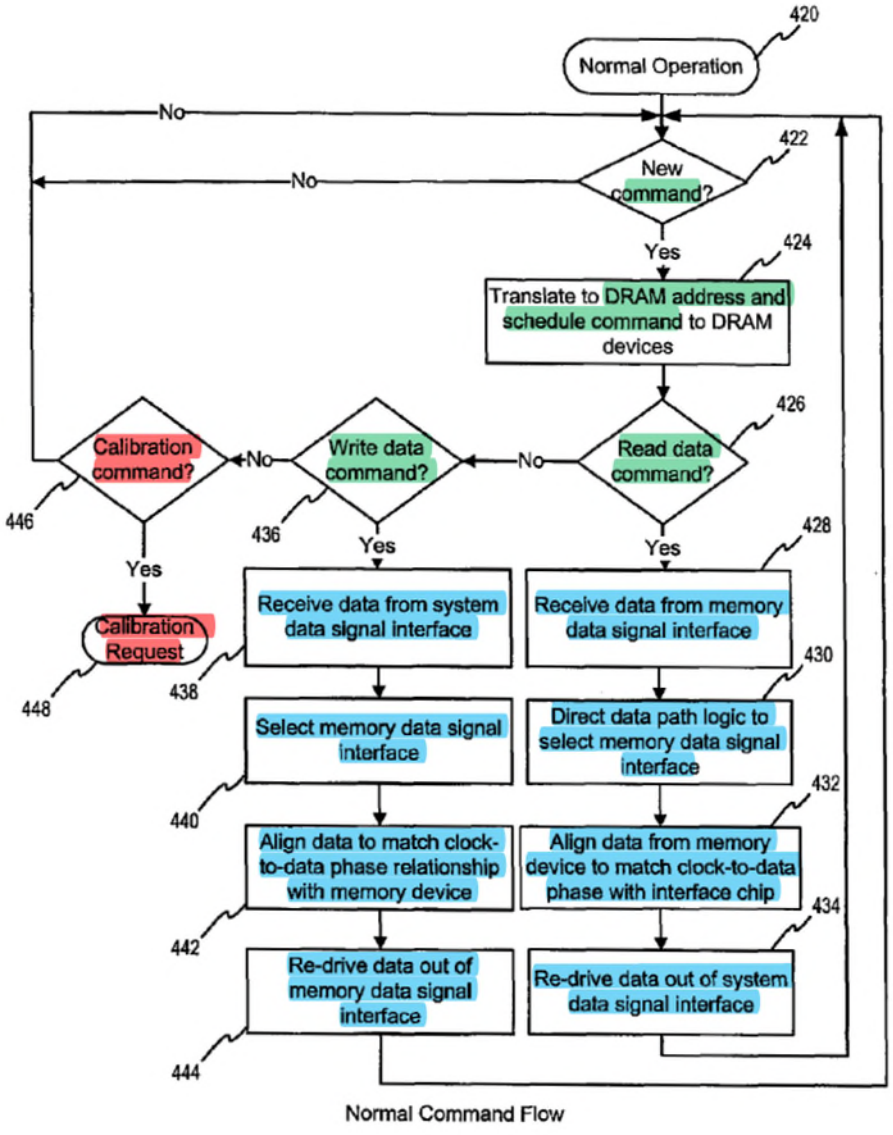


FIG. 4D

As illustrated in this flowchart, Wang teaches to a Skilled Artisan that the normal memory read and write operations are separate from the training which is performed in response to a calibration command (red). EX1090, 11:1-9 ("… the

method then proceeds to step 446, where the emulation and command translation logic determines whether the new command is a CALIBRATION command. If so, then the method ends at step 448, where the emulation and command translation logic 280 issues a calibration request to the initialization and configuration logic 282. The calibration sequence has been described in FIG. 4C."). In particular, Wang discloses that its training is performed by initialization and configuration logic 282 (red) in the interface circuit 250 in response to a "Calibrate" command from the memory controller. EX1090 (Wang), Figs. 2C.

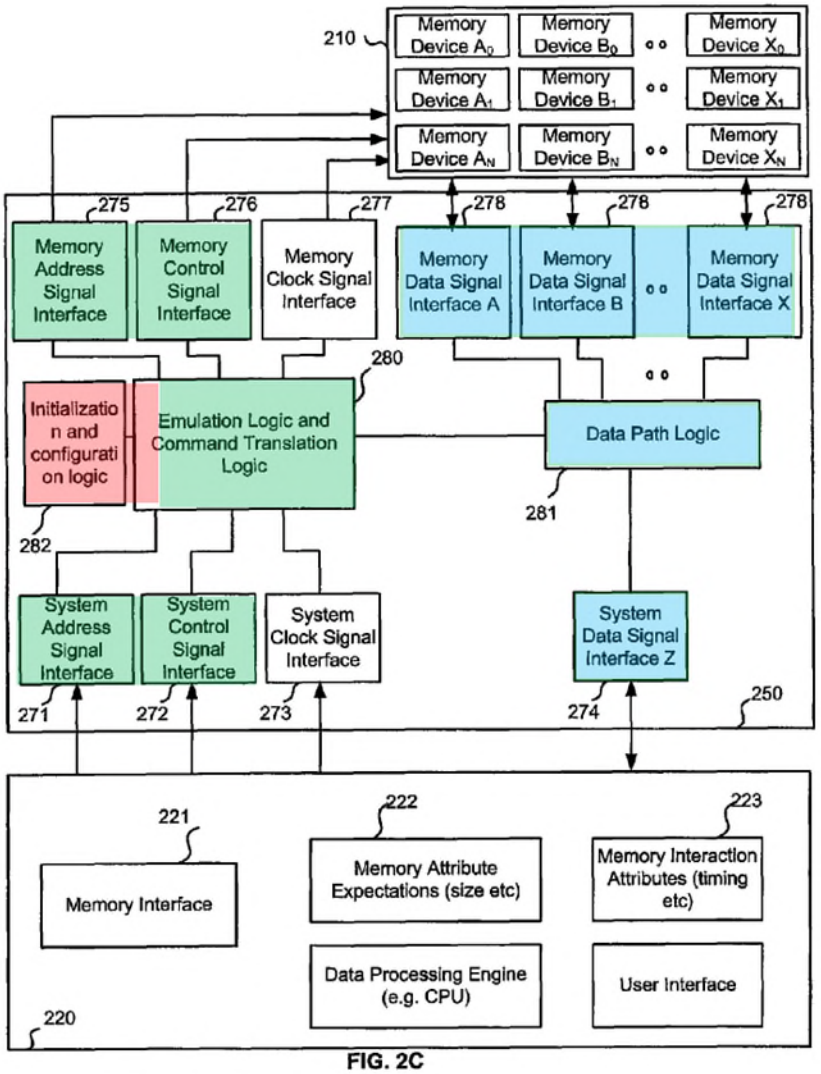


FIG. 2C

For example, Wang discloses that it can use DDR3 SDRAMs. EX1090 (Wang), 4:1-9, 5:37-43. As discussed above, a Skilled Artisan would have understood that training the memory interface for DDR3 memory devices can be performed using standard write leveling and MPR modes without any normal operations, such as normal memory read or write operations. *Supra*, ¶¶70, 190. A Skilled Artisan would have been motivated to use standard write leveling and MPR modes because

they were standard, well-known techniques, specifically developed for training DDR3 memory devices. EX1056 (JESD79-3C), pp.40-45, 48-54.

286. As discussed above, a Skilled Artisan would have been motivated to use Hazelzet's open-drain output to indicate completion of the training and the return to the normal operations to the controller so that it can perform normal memory read and write operations. *Supra* ¶¶211-220. For example, Hazelzet teaches that the open-drain output (e.g., UE) can be used to inform the system controller about the status of the memory module. EX1014, [0122]. Thus, a Skilled Artisan would have understood that the UE pin of Hazelzet is available to indicate the status of Wang's training of the memory device data interface, because the memory module cannot be accessed for normal read or write operations during the training, so there is no need for the UE pin to indicate parity or ECC errors in the received commands like in normal mode. Accordingly, the UE pin can be used, and a Skilled Artisan would have been motivated to use it, for other purposes, such as reporting status information to the controller about the training being under way and/or completed. Indeed, a Skilled Artisan would have known about the JEDEC proposal which expressly teaches using the ERROUT# pin to signal completion of the MB-DRAM training. EX1015, pp.3, 8; *see also* ¶¶170, 189, 193, 216.

287. Similarly, in a Buchmann combination analyzed here, it would have been obvious to use Hazelzet's open drain output to convey the TS_done signal to indicate completion of training. *Supra*, ¶¶187-192. For example, when the TS0 training operations are being carried out, the address/control and data signals would not be used for normal memory read and write operations because TS0 training involves training of the "clock" itself, and no address/control or data signals are transmitted between the host and the memory module during such training. EX1016 (Buchmann) at 5:51-7:2. Thus, a Skilled Artisan would have been motivated to use Hazelzet's open drain output, which is not otherwise used during training, to indicate to the memory controller when the training is complete, so that the controller can perform the next training steps or return to the normal memory operations, including normal memory read and write operations.

288. To the extent Patent Owner argues otherwise, a Skilled Artisan would have found it obvious at least not to perform normal memory read and write operations using any data, control or address signals while the clock or clock-to-data relationships are being trained for the same reasons set forth above. For example, a Skilled Artisan would have been motivated not to use the address, control and data signals for normal memory read and write operations before the training is complete in order to avoid unreliable operation during periods when the clock may be unstable or the clock-to-data phase relationship is not established.

289. Accordingly, the combinations discussed above at least render obvious the limitation of "*wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations.*"

2. Claim 2 is Unpatentable

290. Claim 2 requires "*The memory module of claim 1, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state*." As discussed above, *supra at* ¶¶153-155, the limitations of claim 2 of the 024 Patent correspond to claim 8 of the '623 patent, claim 4 of the '218 patent, and claim element [1.g] and claim 7 of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.20-21; EX1102 ('218 FWD), pp.63-64; EX1103 ('595 FWD), pp.50-52, 73-74.

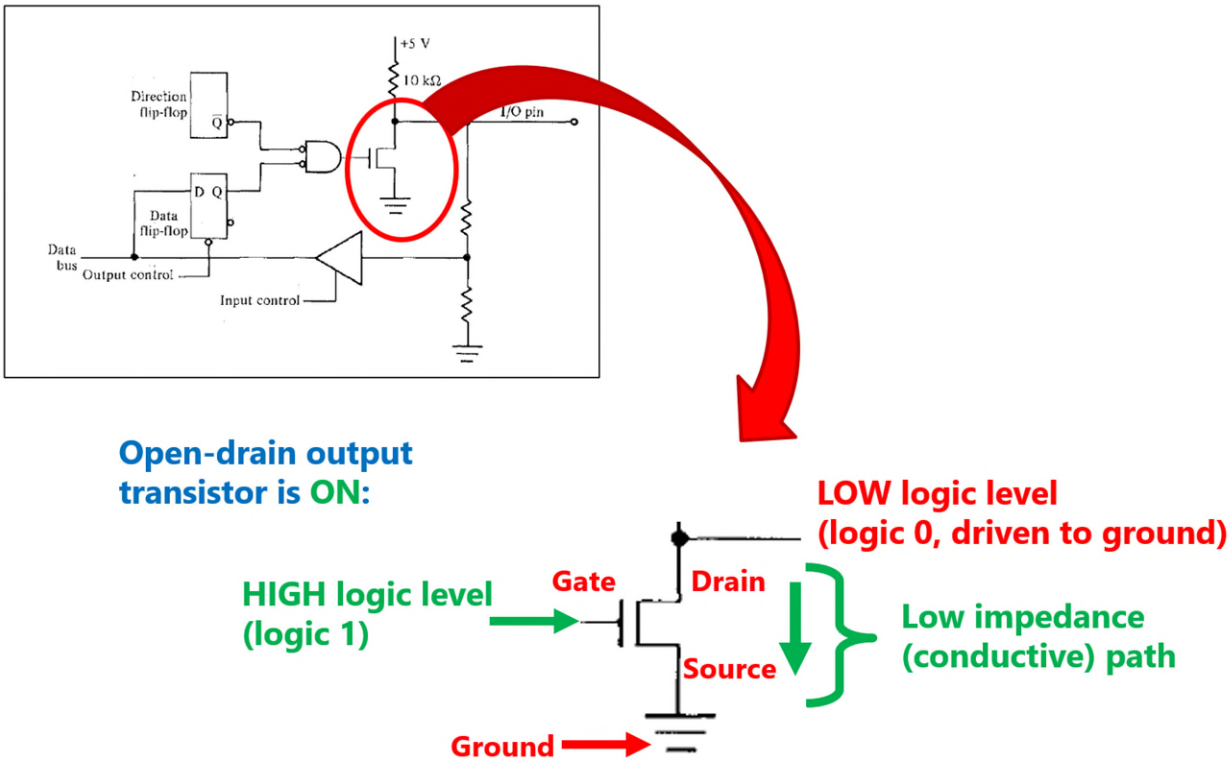
291. As demonstrated above, in the combinations analyzed here the open drain output is configured such that the transistor output is driven low (ground) while training is still occurring and is in a high-impedance state upon completion (so that it can be pulled high by a pull-up resistor). Moreover, to drive the output

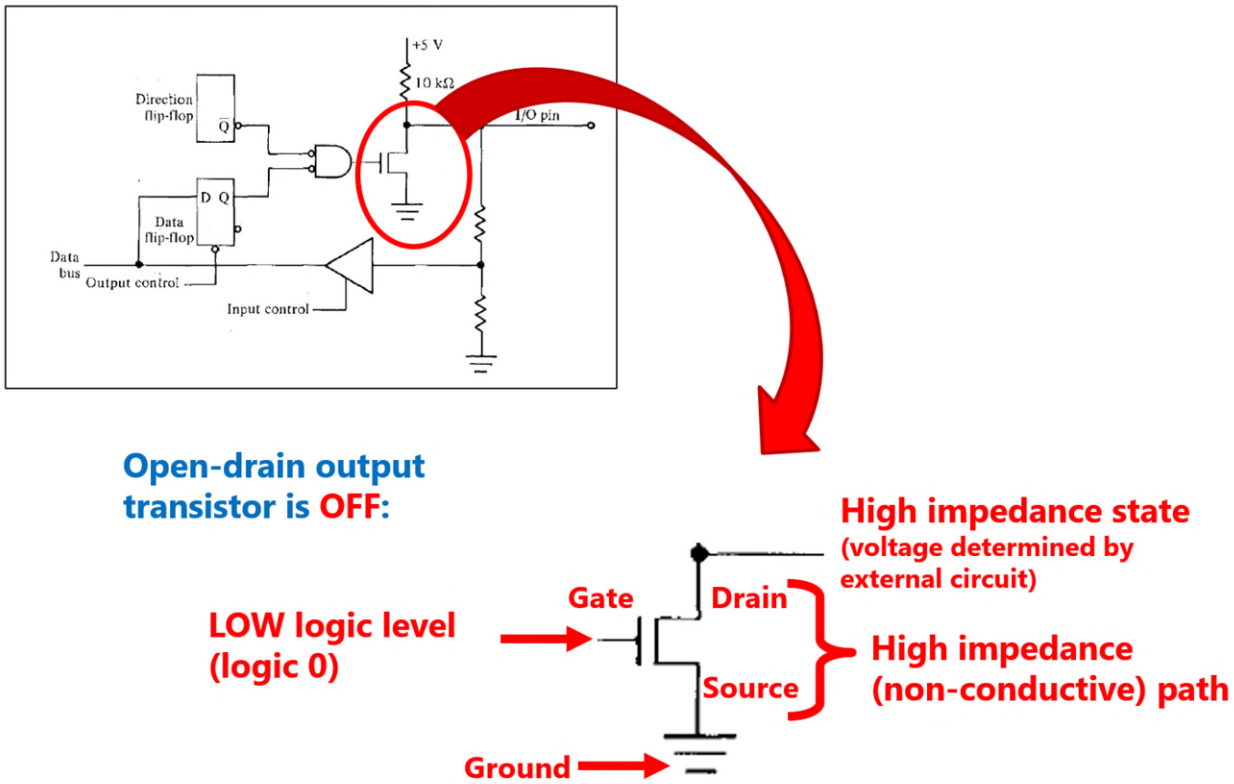
low (i.e., ground), the gate of the transistor must be high, causing the transistor to conduct and connect the drain to ground. Conversely, to allow the output to be pulled high (which would be a high impedance state), the gate of the transistor must be low, turning the transistor off. *See* ¶¶46-54.

292. Similarly, Hazelzet explains that its open-drain output is driven "low" (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage), and further explains that the open-drain "output [is] permitted to return to an un-driven state (high impedance)" when the "driver [is] disabled." EX1014 (Hazelzet) at ¶[0099] ("Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., '0' two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules."). Accordingly, a Skilled Artisan would have understood that the known open-drain output for such a system, such as disclosed in Kim, was used in Hazelzet, *see* ¶¶46-54, *above,* and that Hazelzet's open-drain output would not be driven by the transistor (*i.e.*, high impedance state) when the gate of the transistor is low, because the transistor would be off. EX1014 (Hazelzet) at ¶[0099]; *see* ¶¶46-54, *above*; EX1017 (Kim)

at FIG. 4. On the other hand, Hazelzet's open-drain output would switch to a low logic level (to ground) when the gate of the transistor is high, because the transistor would be on. *Id*.

293. Accordingly, one skilled in the art would have known that the open-drain output, thus the edge connection connected to it, would be driven to ground when the transistor's gate is driven high. *See* ¶¶46-54; EX1014 (Hazelzet) at ¶[0099]; EX1017 (Kim) at FIGs. 4-5, 5:65-6:18. Likewise, one skilled in the art would have known that the open-drain output, thus the edge connection connected to it, would be in a high impedance state when the transistor's gate is driven low. *Id*. As discussed above, this was decades old technology at the time. *See, e.g.*, EX1089 (Stone) at 207-208 ("When the gate of the transistor (the input driven by the NAND) has a voltage above threshold, which represents a logic 1, the transistor conducts and there is a low impedance path from the I/O pin to ground through the transistor. When the transistor gate-voltage drops below threshold to logic 0, the transistor opens. Now the path from the I/O pin to ground through the transistor is open [i.e., off and non-conductive], and the I/O pin is pulled high to 5 V by the 10 kΩ resistor.").


+5 V
10 kΩ
I/O pin
Direction flip-flop
Q
D Q
Data flip-flop
Data bus
Output control
Input control
Open-drain output transistor is ON:
LOW logic level (logic 0, driven to ground)
HIGH logic level (logic 1)
Gate
Drain
Source
Low impedance (conductive) path
Ground



294. Accordingly, the combinations discussed above disclose the limitation of "*wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.*"

3. Claim 3 is Unpatentable

295. Claim 3 requires "*[t]he memory module of claim 2, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state.*" As discussed above, *supra at* ¶¶153-155, the limitations of claim 3 of the 024 Patent

correspond to claim 8 of the ’623 patent, claim 4 of the ’218 patent, and claim element [1.g] and claim 7 of the ’595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 (’623 FWD), pp.20-21; EX1102 (’218 FWD), pp.63-64; EX1103 (’595 FWD), pp.50-52, 73-74.

296. As demonstrated above, in the combinations analyzed here the open-drain output is configured such that the transistor output coupled to the error edge connection is driven to the low logic level (to ground) while training is still occurring and driven to the high impedance state upon completion. Moreover, to drive the output to the low logic level (i.e., to ground), the gate of the transistor must be high, causing the transistor to conduct and connect the drain to ground. Conversely, to drive the output to the high impedance state, the gate of the transistor must be low, turning the transistor off. *See* ¶¶46-54.

297. Similarly, Hazelzet explains that its open-drain output is driven “low” (i.e., to ground) when the driver is enabled (i.e., the gate receives a high voltage), and further explains that the open-drain “output [is] permitted to return to an un-driven state (high impedance)” when the “driver [is] disabled.” EX1014 (Hazelzet) at ¶[0099] (“Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., ‘0’ two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is

detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules."). Accordingly, a Skilled Artisan would have understood that the known open-drain output for such a system, such as disclosed in Kim, was used in Hazelzet, *see* ¶¶46-54, *above*, and that Hazelzet's open-drain output would be in the high impedance state when the gate of the transistor is low, because the transistor would be off. EX1014 (Hazelzet) at ¶[0099]; *see* ¶¶46-54, *above*; EX1017 (Kim) at FIG. 4. On the other hand, Hazelzet's open-drain output would switch to a low logic level (*e.g.*, to ground) when the gate of the transistor is high, because the transistor would be on. *Id*. *See* ¶¶46-54.

298. Accordingly, one skilled in the art would have known that the open-drain output, thus the edge connection connected to it, would be driven to ground ("*the low logic level*") when the transistor's gate is driven high. *See* ¶¶46-54; *see also* EX1017 (Kim) at FIGS. 4-5, 5:65-6:18. Likewise, one skilled in the art would have known that the open-drain output, thus the edge connection connected to it, would be in a high impedance state when the transistor's gate is driven low. *Id*.

299. The obvious combinations of Hazelzet and JEDEC or Buchmann or Wang with or without Kim therefore satisfy the limitation of "*wherein the second*

signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state."

4. Claim 4 is Unpatentable

300. Claim 4 requires "*[t]he memory module of claim 2, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state*." As discussed above, *supra at* ¶¶153-155, the limitations of claim 4 of the 024 Patent correspond to claim 8 of the '623 patent, claim 4 of the '218 patent, and claim element [1.g] and claim 7 of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.20-21; EX1102 ('218 FWD), pp.63-64; EX1103 ('595 FWD), pp.50-52, 73-74.

301. As demonstrated above with reference to claim 3, in the combinations analyzed here, the open-drain output is configured such that the transistor output connected to the error edge connection is driven to the low logic level (ground) when the second signal drives the gate of the transistor high, causing the transistor to conduct and connect the drain to ground. Conversely, to have the output and the connected error edge connection in the high impedance state, the second signal drives the gate of the transistor low, turning the transistor off. *See* ¶¶295-299.

302. Accordingly, the combinations discussed here disclose the "*wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state*" limitation.

5. Claim 5 is Unpatentable

303. Claim 5 requires "*[t]he memory module of claim 4, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground*." As discussed above, *supra at* ¶¶153-155, the limitations of claim 5 of the 024 Patent correspond to claim 9 of the '623 patent, and claim 5 of the '218 and '595 patents, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.20-21; EX1102 ('218 FWD), pp.64-66; EX1103 ('595 FWD), pp.69-71.

304. As discussed above, *see* ¶¶253-272, Hazelzet explains that its "ECC/Parity register" ("*a module controller*") has "open-drain output[s]" (e.g., Uncorrectable Error (UE) line[s]") capable of utilizing "parity error signals" (PERR) to output signal UE 121 to the host indicating a parity error. *See, e.g.*, EX1014, ¶¶[0059], [0070], [0072], [0076]. When the memory module is in the "parity mode," the "parity generator/checker circuit 231" (within SEC/DED ECC circuit 90) generates and sends the "parity error signal (PERR)" to the "error logic circuit" 100. EX1014 (Hazelzet) at FIGS. 4B-5, ¶¶[0059], [0070], [0072], [0076]

("FIG. 5 is a block diagram of the SEC/DED ECC circuit of FIG. 4B. ... The parity generator/checker circuit 231 further has a second input coupled to the parity in signal source 31 via primary latch 71 and output line 81 and depending on the state of the parity input signal on input 31 sends a parity error signal (PERR) on output line 111 to the error logic circuit 100.").

305. In particular, Hazelzet explains that in the "parity mode," the parity error "will be reported two clock pulses later via the Uncorrectable Error (UE) line (driven low for two clock pulses)." EX1014 (Hazelzet) at ¶[0070]; *see also id.* at [0018] ("After holding the error line low for only 2 clock cycles, the driver can be disabled and the output permitted to return to an un-driven state (high impedance) thus allowing this line to be shared by multiple modules.").

306. Further, as explained in claim 4, *see* ¶¶300-302, *above*, Hazelzet discloses to a Skilled Artisan that its open-drain output is driven to the low logic level, i.e., to ground, when the transistor's gate receives a high voltage and therefore the transistor turns "on" and provides a low impedance path between the error edge connection and ground, as was known for decades, *see* ¶¶46-54, *above*. The same principles apply here, when "*the first signal drives the gate of the transistor high*" to indicate a parity error. EX1014 (Hazelzet) at ¶[0099] ("Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error

line low, i.e., '0' two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.").

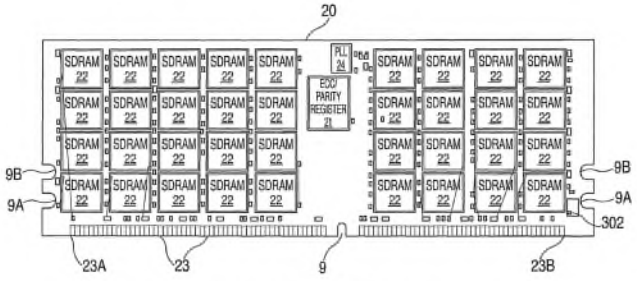
307. Accordingly, the obvious combinations of Hazelzet and JEDEC or Buchmann or Wang with or without Kim therefore satisfy the limitation of "*wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.*"

6. Claim 6 is Unpatentable

308. Claim 6 requires "*[t]he memory module of claim 1, wherein the module controller comprises an integrated circuit that includes the transistor*." As discussed above, *supra at* ¶¶153-155, the limitations of claim 6 of the 024 Patent correspond to claims 6-7 of the '623 patent, claims 2 and 3 of the '218 and '595 patents, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.20-21; EX1102 ('218 FWD), pp.61-63; EX1103 ('595 FWD), pp.66-68.

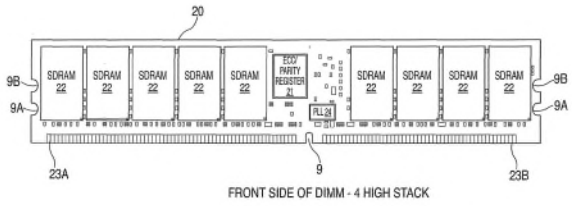
309. As discussed above, the claimed "*transistor*" is in Hazelzet's "ECC/Parity register" (in the "*module controller*") which is also referred to as a "buffer device" or a "buffer chip." EX1014 (Hazelzet) at ¶[0038]. Hazelzet

further explains that the module support devices — including "buffers" (in the "*module controller*"), "registers," and "PLL" — may be comprised of "multiple separate chips" or may be "combined onto a single package or even integrated onto a single device." EX1014 (Hazelzet) at ¶[0115]; *see also id*. at FIG. 3A-3D (FIGS. 3A and 3C reproduced below illustrating ECC/Parity integrated circuits), ¶[0039] ("It should be understood that the PLL chip 24 can be eliminated if its circuitry is provided on the buffer chip 21 or within the same package as the buffer chip 21."), ¶[0042].



FRONT SIDE OF DIMM - 72 PLANAR

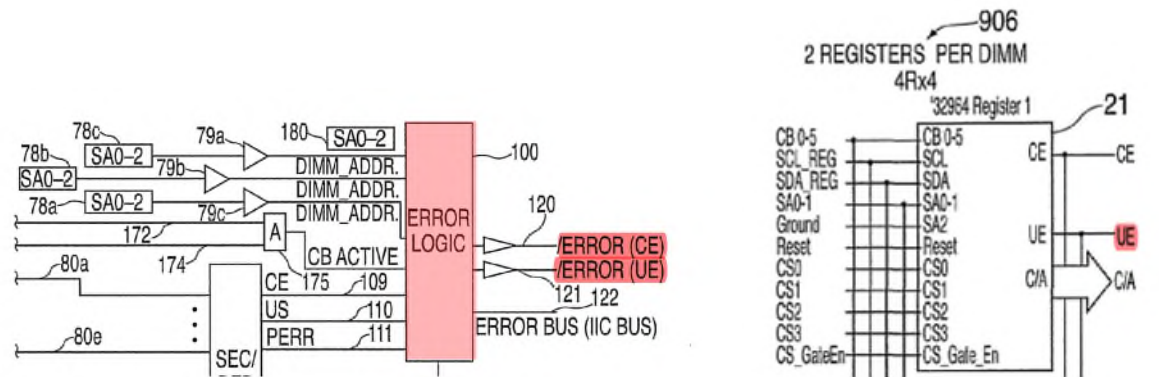
FIG. 3A



FRONT SIDE OF DIMM - 4 HIGH STACK

FIG. 3C

In particular, Hazelzet teaches that its ECC/Parity buffer chip 21 includes error logic circuit 100 which generates the open-drain output UE. EX1014, [0044], [0059], Fig. 4B (reproduced below in part, on the left), Fig. 9 (showing integrated circuits with respective UE output pins, reproduced below in part, on the right).



A Skilled Artisan would have understood from this disclosure that the module controller includes an integrated circuit, such as ECC/Parity buffer chip which, in turn includes the transistor with the open drain output UE.

310. Accordingly, the combinations disclose the limitation of "*wherein the module controller comprises and integrated circuit that includes the transistor*."

7. Claim 7 is Unpatentable

311. Claim 7 requires "*[t]he memory module of claim 1, wherein the operation associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections*." As discussed above, *supra at* ¶¶153-155, the limitations of claim 7 of the 024 Patent correspond to claim elements [1.c] and [1.d] and claim 2 of the '623 patent, claim elements [1.e.ii] and [1.f] and claim 7 of the '218 patent, and claim element [1.e.iii] and claim 9 of the '595 patent, which the Board already found obvious over the combination of Hazelzet and

Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), pp.47-50, 67-68; EX1103 ('595 FWD), pp.47-48, 74-75.

312. As discussed above with reference to claim [1.e.3], the combinations proposed here render obvious the requirement of claim 7 that "*the operation associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations.*" *See supra*, ¶¶280-289. For reasons discussed above with reference to claim element [1.e.3], it would have been obvious that no data signals are communicated with the memory controller via the second edge connections when the operations associated with the training sequences are performed. *See id.*

313. For example, in the JEDEC combination analyzed here, JEDEC discloses that during the MB-DRAM training (i.e., the training that is added to Hazelzet here), "[n]o DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete and the DODTn inputs must be kept low." EX1015, 8. A Skilled Artisan would have understood from this that during such training the address/control pins (including the high order address/control pins) would remain inactive as those are pins used to provide "DRAM commands

or control word writes," and no data signals would be communicated on the data pins. *Id*.

314. Similarly, in the obvious combination of Hazelzet and Buchmann, the memory module can execute a training sequence (e.g., TS0 training, which involves training of the "clock") in the SBC mode. EX1016 (Buchmann) at 5:51-7:2; *see also* ¶¶280-289 (claim element [1.e.3]). Because this training involves training of the "clock" itself, a Skilled Artisan would have understood that there are no "data" signals being transmitted between the host and the memory module during the TS0 training.

315. Similarly, in the combination of Hazelzet and Wang, a Skilled Artisan would have understood that the operations associated with the one or more "*training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections*" for the reasons discussed above with reference to claim element [1.e.3], *supra*, ¶¶280-289, including that Wang's training uses the memory devices data signal lines, thus rendering obvious that the memory devices are not accessed by the memory controller for normal read or write operations, thus no data associated with such normal memory read or write operations is communicated through the "*second edge connections*."

316. Accordingly, the combinations discussed here disclose the limitation of "*wherein the operation associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.*"

8. Claim 8 is Unpatentable

317. Claim 8 requires "*[t]he memory module of claim 1, wherein the second edge connections are not active during the operations associated with the one or more training sequences*." As discussed above, *supra at* ¶¶153-155, the limitations of claim 8 of the 024 Patent correspond to claim elements [1.c] and [1.d] and claim 2 of the '623 patent, claim elements [1.e.ii] and [1.f] and claim 7 of the '218 patent, and claim element [1.e.iv] and claim 8 of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), pp.47-50, 67-68; EX1103 ('595 FWD), pp.48, 74-75.

318. As discussed above with reference to claim 7, it would have been obvious to a Skilled Artisan that no data signals are communicated through the "*second edge connections*" when the operations associated with training are performed. *Supra*, ¶¶311-316. For the same reasons, it would have been obvious

that those "*second edge connections*" are not active when no data signals are communicated through the "*second edge connections.*"

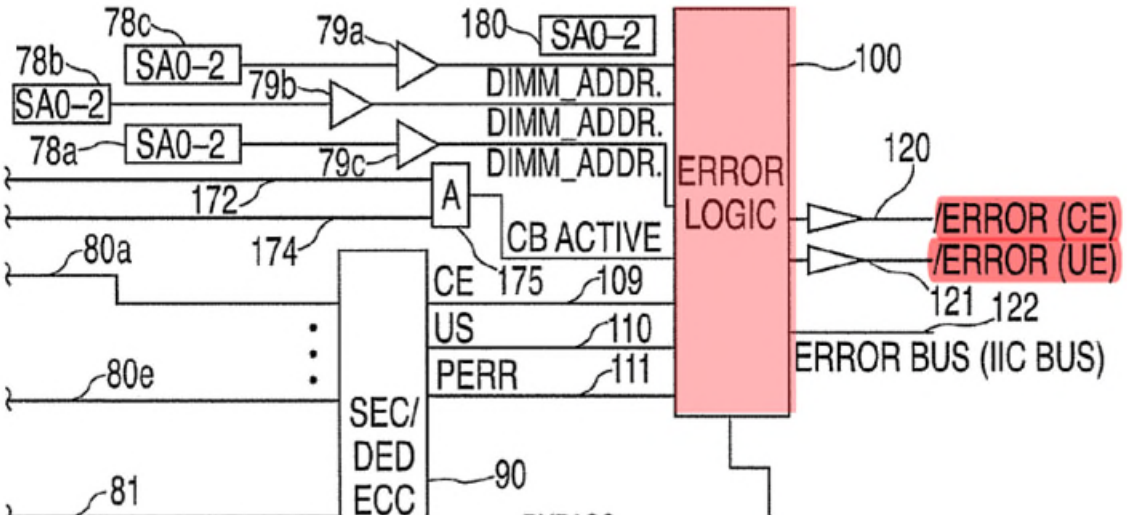
319. Accordingly, the combinations disclose the limitations of "*wherein the second edge connections are not active during the operations associated with the one or more training sequences.*"

9. Claim 9 is Unpatentable

320. Claim 9 requires "*[t]he memory module of claim 1, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input configured to receive the first signal, and a second input configured to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences*." As discussed above, *supra at* ¶¶153-155, the limitations of claim 9 of the 024 Patent correspond to claims 8-10 of the '623 patent, claim elements [1.f], [1.h], and [1.i] and claims 4-6 of the '218 patent, and claim element [1.e.ii] and claim 6 of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.20-21; EX1102 ('218 FWD), pp.47-53, 63-67; EX1103 ('595 FWD), pp.46-47, 71-73.

321. Hazelzet in combination with JEDEC, or Buchmann, or Wang with or without Kim renders obvious these limitations for the reasons discussed above with reference to claim element [1.e.3]. *Supra*, ¶¶280-289.

322. For example, FIG. 4B of Hazelzet shows the "error correction code circuit including "Error Logic 100" (red). EX1014 (Hazelzet) at ¶[0044], [0059], FIG. 4B (reproduced below, in part, annotated).



Hazelzet discloses that Error Logic 100 receives the "US [sic: UE] 110" signal and the "PERR 111" signal, one of these signals determining the value to the same "/ERROR (UE)" pin depending on which mode the memory module is in. *See* EX1014 (Hazelzet) at FIG. 4B (showing an open-drain output "/ERROR (UE) 121" for uncorrectable error or parity error, depending on the mode of operation), ¶¶[0072] (explaining that "/Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a

parity error."), ¶¶[0044], [0059], [0069-71], FIG. 8 (reproduced below, annotated, showing the same UE pin being used in "ECC mode" and "Parity mode."

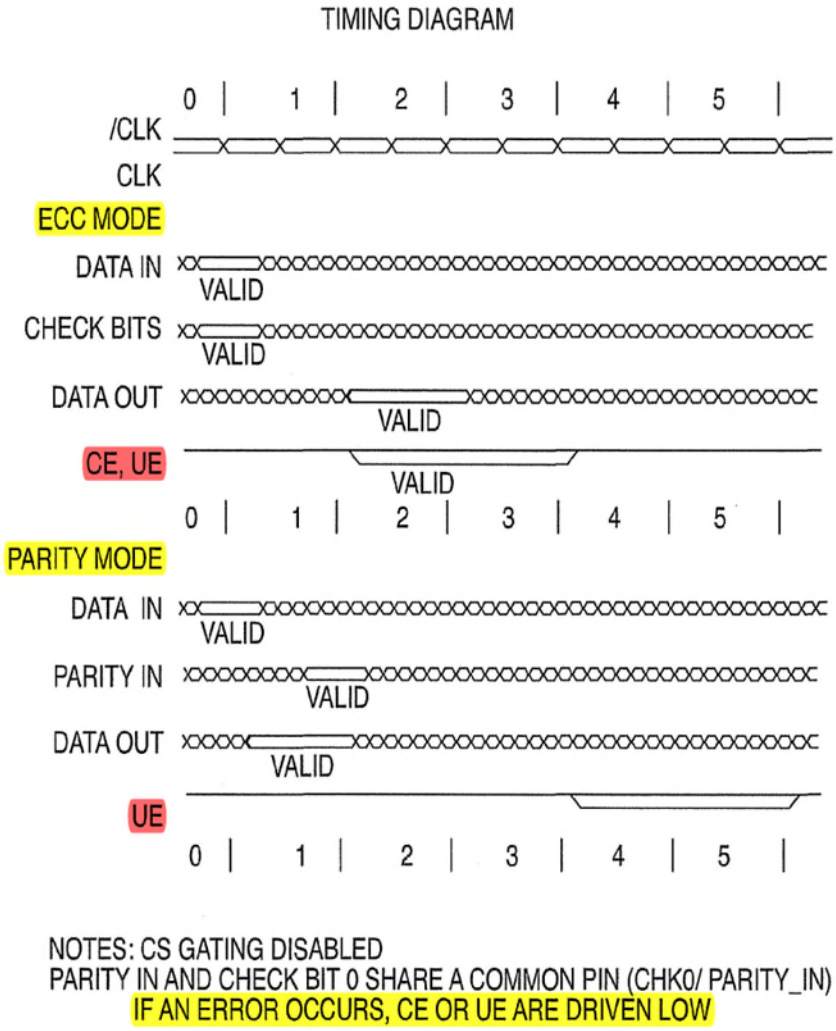


FIG. 8

As set forth above, *see* ¶¶211-220, in the combinations analyzed here, that circuitry would be modified to implement notifications about the additional training, in which the UE 121 open-drain output would, when the module is performing

operations related to training, be used to send the notification/status signals identified above.

323. Hazelzet also discloses that UE 121 is an open-drain output, EX1014, [0072], which a Skilled Artisan would understand is driven by a transistor in an open-drain configuration. EX1017, FIGS. 4-5, 5:65-6:18 (depicting in FIG. 5 OR logic gate used for such purpose); *see* ¶¶46-54, *above*. A Skilled Artisan would have understood that such a transistor has "*a gate*" that can be driven to assert the open-drain output. *Id*.

324. Because in the combinations analyzed here, Error Logic 100 receives both "US [sic: UE] 110" signal and the "PERR 111" signal and the training mode notification signals, but uses only one such signal to drive the UE 121 output, depending on mode, a Skilled Artisan would have understood that Error Logic 100 would necessarily include logic circuitry (in addition to the open drain transistor) to determine which signal should be used to drive the transistor. EX1017, FIGS. 4-5, 5:65-6:18 (FIG. 5, reproduced below, including OR logic coupled to the transistor's gate used for such purpose).

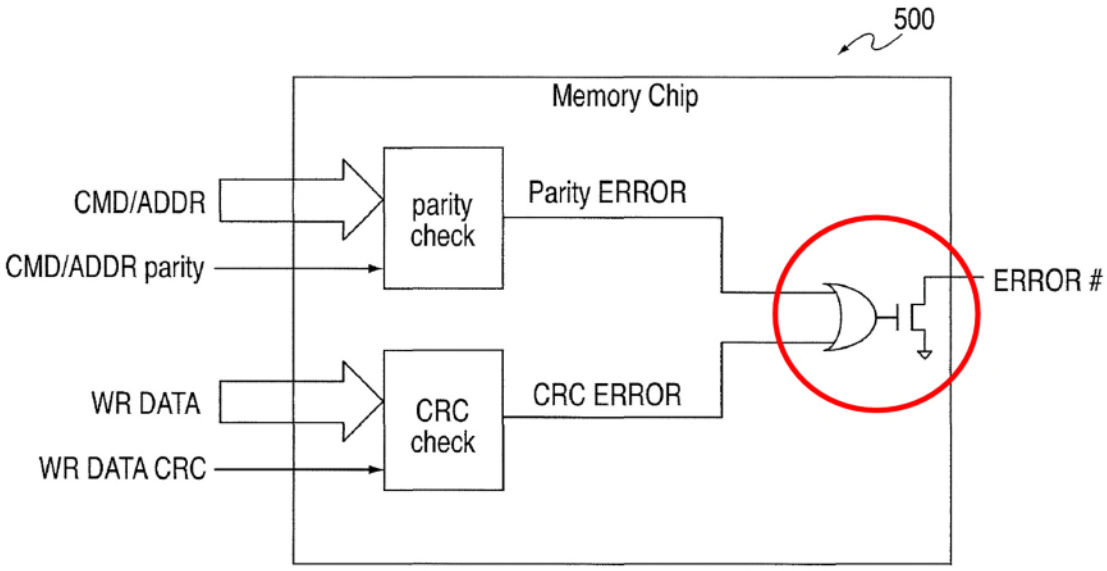
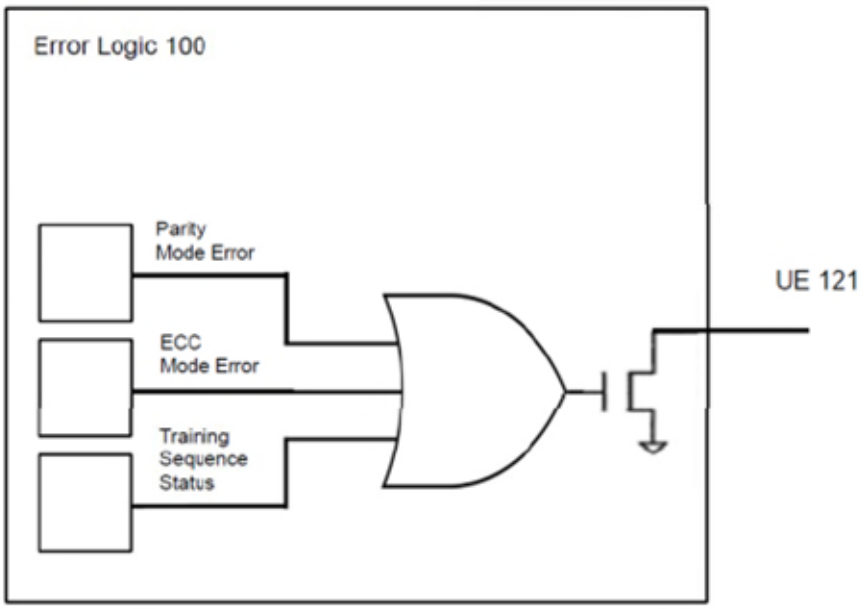


FIG. 5

A Skilled Artisan would have understood that adding the training notification functionality would be straightforward and could use a three-input OR circuit or a multiplexer, as discussed above with reference to claim element [1.e.1]. *See* ¶¶253-272.



That additional logic circuitry is a "*logic circuit*," and necessarily has "*an output coupled to a gate of the transistor*" because that is how a transistor in an open drain configuration is driven (by a signal driving the gate), *see* EX1017, FIGS. 4-5, 5:65-6:18; *see* ¶¶46-54, *above*. Moreover, the signal driving that gate is necessarily related to one of the signals input to Error Logic 100 (*e.g.*, "PERR 111" ("*first signal*") or the training notification signals ("*second signal*"), depending on mode, so the additional logic circuitry has "*a first input configured to receive the first signal, and a second input configured to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.*"

325. The obvious combinations of Hazelzet and JEDEC or Buchmann or Wang with or without Kim therefore satisfy the limitation of "*wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input configured to receive the first signal, and a second input configured to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.*"

10. Claim 10 is Unpatentable

326. In my opinion, Claim 10 is unpatentable because it is obvious in view of Grounds 1-6.

a) [10.a]-[10.b.1]

327. Claim 10 requires "*[a] method of operation in the host system having a memory controller, comprising: at a memory module coupled to the memory controller*." As discussed above, *supra at* ¶¶153-155, the limitations of claim elements [10.a]-[10.b.1] of the 024 Patent correspond to claim element [1.a] of the '623 patent, claim element [9.a] of the '218 patent, and claim elements [17.a]-[17.b] of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), p.9; EX1102 ('218 FWD), pp.53-54; EX1103 ('595 FWD), p.57.

328. As shown in the table below, claim elements [10.a] and [10.b.1] are very similar to claim element 1.a:

Claim 1	**Claim 10**
[1.a] A memory module operable with a memory controller of a host system, comprising:	[10.a] A method of operation in a host system having a memory controller, comprising: [10.b.1] at a memory module coupled to the memory controller,

329. For the same reasons discussed above with reference to claim limitation [1.a], the prior art references in Grounds 1-6 satisfy "*[a] method of*

operation in a host system having a memory controller, comprising: at a memory module coupled to the memory controller." *See supra* ¶¶223-225.

b) [10.b.2]

330. Claim 10 requires "*the memory module including a printed circuit board*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [10.b.2] of the 024 Patent correspond to claim elements [1.a] and [1.d] of the '623 patent, claim element [9.b] of the '218 patent, and claim element [17.b] of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), p.54; EX1103 ('595 FWD), p.57.

331. As shown in the table below, claim element [10.b.2] is very similar to claim elements [1.a] and [1.b.1]:

Claim 1	**Claim 10**
[1.a] A memory module operable with a memory controller of a host system, comprising: [1.b.1] a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,	[10.b.2] the memory module including a printed circuit board,

332. For the same reasons discussed above with reference to claim limitations [1.a] and [1.b.1], the prior art references in Grounds 1-6 satisfy "*the memory module including a printed circuit board*." *See supra* ¶¶223-229.

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c) [10.c]

333. Claim 10 requires "*a module controller on the printed circuit board*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [10.c] of the 024 Patent correspond to claim elements [1.a], [1.b], and [1.d] of the '623 patent, claim element [1.d] of the '218 patent, and claim element [20.a] and claim 3 of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-20; EX1102 ('218 FWD), pp.46-47; EX1103 ('595 FWD), pp.66-68, 75-77.

334. As shown in the table below, claim element [10.c] is very similar to claim element [1.c.1]:

Claim 1	**Claim 10**
[1.c.1] a module controller on the printed circuit board and	[10.c] a module controller on the printed circuit board, and

335. For the same reasons discussed above with reference to claim limitation [1.c.1], the prior art references in Grounds 1-6 satisfy "*a module controller on the printed circuit board*." *See supra* ¶¶235-237.

d) [10.d]

336. Claim 10 requires "*dynamic random access memory elements on the printed circuit board*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [10.d] of the 024 Patent correspond to claim elements [1.a] and [1.d] and claim 2 of the '623 patent, claim element [9.b] of the '218 patent, and claim

element [17.b] of the ’595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 (’623 FWD), pp.9-20; EX1102 (’218 FWD), p.54; EX1103 (’595 FWD), p.57.

337. As shown in the table below, claim element [10.d] is very similar to claim element [1.d.1]:

Claim 1	**Claim 10**
[1.d.1] dynamic random access memory elements on the printed circuit board and	[10.d] dynamic random access memory elements on the printed circuit board,

338. For the same reasons discussed above with reference to claim limitation [1.d.1], the prior art references in Grounds 1-6 satisfy “*dynamic random access memory elements on the printed circuit board*.” *See supra* ¶¶243-245.

e) [10.e.1]

339. Claim 10 requires “*the printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller*.” As discussed above, *supra at* ¶¶153-155, the limitations of claim element [10.e.1] of the 024 Patent correspond to claim elements [1.a] and [1.d] of the ’623 patent, claim element [9.c] of the ’218 patent, and claim element [17.b] of the ’595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 (’623 FWD), pp.9-20; EX1102 (’218 FWD), pp.54-55; EX1103 (’595 FWD), p.57.

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340. As shown in the table below, claim element [10.e.1] is very similar to claim element [1.b.1]:

Claim 1	**Claim 10**
[1.b.1] a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,	[10.e.1] the printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,

341. For the same reasons discussed above with reference to claim limitation [1.b.1], the prior art references in Grounds 1-6 satisfy "*the printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller*." *See supra* ¶¶226-229.

f) [10.e.2]

342. Claim 10 requires "*the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [10.e.2] of the 024 Patent correspond to claim element [1.d] of the '623 patent, claim element [9.c] of the '218 patent, and claim element [17.b] of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-20; EX1102 ('218 FWD), pp.54-55; EX1103 ('595 FWD), p.57.

343. As shown in the table below, claim element [10.e.2] is very similar to claim element [1.b.2]:

Claim 1	**Claim 10**
[1.b.2] the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;	[10.e.2] the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections,

344. For the same reasons discussed above with reference to claim limitation [1.b.2], the prior art references in Grounds 1-6 satisfy "*the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections*." *See supra* ¶¶230-234.

g) [10.f]

345. Claim 10 requires "*the module controller including a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [10.f] of the 024 Patent correspond to claim element [1.d] and claims 7-8 of the '623 patent, claim element [1.d] and claims 3-4 of the '218 patent, and claim elements [17.c] and [20.a]-[20.b] of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann.

EX1034 (’623 FWD), pp.9-21; EX1102 (’218 FWD), pp.46-47, 62-63; EX1103 (’595 FWD), pp.57-58, 75-77.

346. As shown in the table below, claim element [10.f] is very similar to claim element [1.e.1]:

Claim 1	**Claim 10**
[1.e.1] wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;	[10.f] the module controller including a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

347. For the same reasons discussed above with reference to claim limitation [1.e.1], the prior art references in Grounds 1-6 satisfy “*the module controller including a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate*.” *See supra* ¶¶253-272.

h) [10.g]

348. Claim 10 requires “*receiving, at the module controller, address and control signals associated with one or more normal memory read or write operations from the memory controller via the first edge connections*.” As discussed above, *supra at* ¶¶153-155, the limitations of claim element [10.g] of the 024 Patent correspond to claim element [1.d] and claim 2 of the ’623 patent, claim elements [9.c] and [9.d] of the ’218 patent, and claim elements [1.f.i] and [17.c] of the ’595 patent, which the Board already found obvious over the combination of

Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), pp.54-55; EX1103 ('595 FWD), pp.48-49, 57-58.

349. As shown in the table below, claim element [10.g] is very similar to claim elements [1.b.1] and [1.c.2]:

Claim 1	**Claim 10**
[1.b.1] a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, [1.c.2] configured to receive address and control signals associated with normal memory read or write operations via the first edge connections; and	[10.g] receiving, at the module controller, address and control signals associated with one or more normal memory read or write operations from the memory controller via the first edge connections;

350. For the same reasons discussed above with reference to claim limitations [1.b.1] and [1.c.2], the prior art references in Grounds 1-6 satisfy "*receiving, at the module controller, address and control signals associated with one or more normal memory read or write operations from the memory controller via the first edge connections*." *See supra* ¶¶226-229, 238-242.

i) [10.h]

351. Claim 10 requires "*outputting or receiving data signals at the dynamic random access memory elements in accordance with the address and control signals, the data signals being associated with the one or more normal*

memory read or write operations and communicated with the memory controller via the second edge connections." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [10.h] of the 024 Patent correspond to claim element [1.d] and claim 2 of the '623 patent, claim elements [9.c]-[9.e] of the '218 patent, and claim elements [1.f.i] and [17.c] of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), pp.54-55; EX1103 ('595 FWD), pp.48-49, 57-58.

352. As shown in the table below, claim element [10.h] is very similar to claim elements [1.c.2] and [1.d.2]:

Claim 1	**Claim 10**
[1.c.2] configured to receive address and control signals associated with normal memory read or write operations via the first edge connections; and [1.d.2] configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and	[10.h] outputting or receiving data signals at the dynamic random access memory elements in accordance with the address and control signals, the data signals being associated with the one or more normal memory read or write operations and communicated with the memory controller via the second edge connections;

353. For the same reasons discussed above with reference to claim limitations [1.c.2] and [1.d.2], the prior art references in Grounds 1-6 satisfy "*outputting or receiving data signals at the dynamic random access memory*

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elements in accordance with the address and control signals, the data signals being associated with the one or more normal memory read or write operations and communicated with the memory controller via the second edge connections." *See supra* ¶¶238-242, 246-252.

j) [10.i]

354. Claim 10 requires "*applying a first signal to the gate of the transistor to indicate a parity error having occurred during one of the one or more normal memory read or write operations*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [10.i] of the 024 Patent correspond to claim element [1.b] and claims 2, 7, and 9 of the '623 patent, claim element [9.f] and claim 11 of the '218 patent, and claim elements [1.f.i], [17.c], and [20.b] of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), pp.55-56, 64-66; EX1103 ('595 FWD), pp.48-49, 57-58, 75-77.

355. As shown in the table below, claim element [10.i] is very similar to claim element [1.e.2]:

Claim 1	**Claim 10**
[1.e.2] wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation; and	[10.i] applying a first signal to the gate of the transistor to indicate a parity error having occurred during one of the one or more normal memory read or write operations;

356. For the same reasons discussed above with reference to claim limitation [1.e.2], the prior art references in Grounds 1-6 satisfy "*applying a first signal to the gate of the transistor to indicate a parity error having occurred during one of the one or more normal memory read or write operations*." *See supra* ¶¶273-279.

k) [10.j]

357. Claim 10 requires "*performing training operations associated with one or more training sequences when the dynamic random access memory elements are not accessed for any normal memory read or write operations*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [10.j] of the 024 Patent correspond to claim element [1.c] and claims 2 and 8 of the '623 patent, claim elements [9.c] and [9.g] of the '218 patent, and claim elements [1.e.iii] and [17.d] of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), pp.54-56, 64-66; EX1103 ('595 FWD), pp.47-48,58-59.

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358. As shown in the table below, claim element [10.j] is very similar to claim element [1.e.3]:

Claim 1	**Claim 10**
[1.e.3] wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations.	[10.j] performing training operations associated with one or more training sequences when the dynamic random access memory elements are not accessed for any normal memory read or write operations; and

359. For the same reasons discussed above with reference to claim limitation [1.e.3], the prior art references in Grounds 1-6 satisfy "*performing training operations associated with one or more training sequences when the dynamic random access memory elements are not accessed for any normal memory read or write operations*." *See supra* ¶¶280-289.

l) [10.k]

360. Claim 10 requires "*applying a second signal related to the one or more training sequences to the gate of the transistor while the memory module performs the training operations*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [10.k] of the 024 Patent correspond to claim element [1.c] and claims 2 and 8 of the '623 patent, claim element [9.h] and claim 14 of the

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’218 patent, and claim elements [17.d] and [20.c] of the ’595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 (’623 FWD), pp.9-21; EX1102 (’218 FWD), pp.56-57, 68-69; EX1103 (’595 FWD), pp.58-59, 75-77.

361. As shown in the table below, claim element [10.k] is very similar to claim element [1.e.3]:

Claim 1	**Claim 10**
[1.e.3] wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations.	[10.k] applying a second signal related to the one or more training sequences to the gate of the transistor while the memory module performs the training operations.

362. For the same reasons discussed above with reference to claim limitation [1.e.3], the prior art reference in Grounds 1-6 satisfy “*applying a second signal related to the one or more training sequences to the gate of the transistor while the memory module performs the training operations*.” *See supra* ¶¶280-289.

11. Claim 11

363. Claim 11 requires “*The method of claim 10, wherein the error edge connection is driven by the second signal from a first state to a second state, one of*

the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state." As discussed above, *supra at* ¶¶153-155, the limitations of claim 11 of the 024 Patent correspond to claim 8 of the '623 patent, claim 10 of the '218 patent, and claim element [20.c] of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.20-21; EX1102 ('218 FWD), pp.69-70; EX1103 ('595 FWD), pp.75-77.

364. As shown in the table below, Claim 11 is very similar to Claim 2:

Claim 2	**Claim 11**
[2] The memory module of claim 1, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.	[11] The method of claim 10, wherein the error edge connection is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

365. For the same reasons discussed above with reference to Claim 2, the prior art references in Grounds 1-6 satisfy "*wherein the error edge connection is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state*." *See supra* ¶¶290-294.

12. Claim 12

366. Claim 12 requires "*The method of claim 11, wherein the error edge connection is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state*." As discussed above, *supra at* ¶¶153-155, the limitations of claim 12 of the 024 Patent correspond to claim 8 of the '623 patent, claim 10 of the '218 patent, and claim element [20.c] of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.20-21; EX1102 ('218 FWD), pp.69-70; EX1103 ('595 FWD), pp.75-77.

367. As shown in the table below, Claim 12 is very similar to Claim 3:

Claim 3	**Claim 12**
[3] The memory module of claim 2, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state.	[12] The method of claim 11, wherein the error edge connection is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state.

368. For the same reasons discussed above with reference to Claim 3, the prior art references in Grounds 1-6 satisfy "*wherein the error edge connection is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state*." *See supra* ¶¶295-299.

13. Claim 13

369. Claim 13 requires "*The method of claim 11, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state*." As discussed above, *supra at* ¶¶153-155, the limitations of claim 13 of the 024 Patent correspond to claim 8 of the '623 patent, claim 10 of the '218 patent, and claim element [20.c] of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.20-21; EX1102 ('218 FWD), pp.69-70; EX1103 ('595 FWD), pp.75-77.

370. As shown in the table below, Claim 13 is very similar to Claim 4:

Claim 4	**Claim 13**
[4] The memory module of claim 2, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.	[13] The method of claim 11, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.

371. For the same reasons discussed above with reference to Claim 4, the prior art references in Grounds 1-6 satisfy "*wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic*

level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state." *See supra* ¶¶300-302.

14. Claim 14

372. Claim 14 requires "*The method of claim 13, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground*." As discussed above, *supra at* ¶¶153-155, the limitations of claim 14 of the 024 Patent correspond to claim 9 of the '623 patent, claim 11 of the '218 patent, and claim element [20.c] of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.20-21; EX1102 ('218 FWD), pp.64-66; EX1103 ('595 FWD), pp.75-77.

373. As shown in the table below, Claim 14 is very similar to Claim 5:

Claim 5	**Claim 14**
[5] The memory module of claim 4, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.	[14] The method of claim 13, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.

374. For the same reasons discussed above with reference to Claim 5, the prior art references in Grounds 1-6 satisfy "*wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground*." *See supra* ¶¶303-307.

15. Claim 15

375. Claim 15 requires "*The method of claim 10, wherein the module controller comprises an integrated circuit that includes the transistor*." As discussed above, *supra at* ¶¶153-155, the limitations of claim 15 of the 024 Patent correspond to claims 6 and 7 of the '623 patent, claims 2 and 3 of the '218 patent, and claim 2 and claim element [20.a] of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.20-21; EX1102 ('218 FWD), pp.61-63; EX1103 ('595 FWD), pp.66, 75-77.

376. As shown in the table below, Claim 15 is very similar to Claim 6:

Claim 6	**Claim 15**
[6] The memory module of claim 1, wherein the module controller comprises an integrated circuit that includes the transistor.	[15] The method of claim 10, wherein the module controller comprises an integrated circuit that includes the transistor.

377. For the same reasons discussed above with reference to Claim 6, the prior art references in Grounds 1-6 satisfy "*wherein the module controller comprises an integrated circuit that includes the transistor*." *See supra* ¶¶308-310.

16. Claim 16

378. Claim 16 requires "*The method of claim 10, wherein the training operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data*

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signals associated with any normal memory read or write operations with the memory controller via the second edge connections." As discussed above, *supra at* ¶¶153-155, the limitations of claim 16 of the 024 Patent correspond to claim elements [1.c] and [1.d] and claim 2 of the '623 patent, claim elements [9.c] and [9.g] of the '218 patent, and claim elements [1.e.iii] and [17.d] of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), pp.54-56; EX1103 ('595 FWD), pp.47-48, 58-59.

379. As shown in the table below, Claim 16 is very similar to Claim 7:

Claim 7	**Claim 16**
[7] The memory module of claim 1, wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.	[16] The method of claim 10, wherein the training operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.

380. For the same reasons discussed above with reference to Claim 7, the prior art references in Grounds 1-6 satisfy "*wherein the training operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals*

associated with any normal memory read or write operations with the memory controller via the second edge connections." *See supra* ¶¶311-316.

17. Claim 17

381. Claim 17 requires "*The method of claim 10, wherein the second edge connections are not active during the training operations associated with the one or more training sequences*." As discussed above, *supra at* ¶¶153-155, the limitations of claim 17 of the 024 Patent correspond to claim elements [1.c] and [1.d] and claim 2 of the '623 patent, claim elements [9.c] and [9.g] of the '218 patent, and claim 18 of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), pp.74-77; EX1103 ('595 FWD), pp.58-59.

382. As shown in the table below, Claim 17 is very similar to Claim 8:

Claim 8	**Claim 17**
[8] The memory module of claim 1, wherein the second edge connections are not active during the operations associated with the one or more training sequences.	[17] The method of claim 10, wherein the second edge connections are not active during the training operations associated with the one or more training sequences.

383. For the same reasons discussed above with reference to Claim 8, the prior art references in Grounds 1-6 satisfy "*wherein the second edge connections are not active during the training operations associated with the one or more training sequences*." *See supra* ¶¶317-319.

18. Claim 18

384. Claim 18 requires "*The method of claim 10, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein applying the first signal to the gate of the transistor includes coupling the first input to the output, and applying the second signal to the gate of the transistor includes coupling the second input to the output*." As discussed above, *supra at* ¶¶153-155, the limitations of claim 18 of the 024 Patent correspond to claims 8-10 of the '623 patent, claim elements [1.f], [1.h], and [1.i] and claims 4-6 of the '218 patent, and claim 13 of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.20-21; EX1102 ('218 FWD), pp.47-53, 63-67; EX1103 ('595 FWD), pp.71-73.

385. As shown in the table below, Claim 18 is very similar to Claim 9:

Claim 9	**Claim 18**
[9] The memory module of claim 1, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input configured to receive the first signal, and a second input configured to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.	[18] The method of claim 10, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein applying the first signal to the gate of the transistor includes coupling the first input to the output, and applying the second signal to the gate of the transistor includes coupling the second input to the output.

386. For the same reasons discussed above with reference to Claim 9, the prior art references in Grounds 1-6 satisfy "*wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein applying the first signal to the gate of the transistor includes coupling the first input to the output, and applying the second signal to the gate of the transistor includes coupling the second input to the output*." *See supra* ¶¶320-325.

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19. Claim 19

a) [19.a]

387. Claim 19 requires "*[a] memory module operable with a memory controller of a host system, comprising*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [19.a] of the 024 Patent correspond to claim element [1.a] of the '623 patent, and claim element [1.a] of the '218 and '595 patents, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), p.9; EX1102 ('218 FWD), p.44; EX1103 ('595 FWD), p.44.

388. As shown in the table below, claim element [19.a] is very similar to claim element [1.a]:

Claim 1	**Claim 19**
[1.a] A memory module operable with a memory controller of a host system, comprising:	[19.a] A memory module operable with a memory controller of a host system, comprising:

389. For the same reasons discussed above with reference to claim limitation [1.a], the prior art references in Grounds 1-6 satisfy "*[a] memory module operable with a memory controller of a host system, comprising*." *See supra* ¶¶223-225.

b) [19.b.1]

390. Claim 19 requires "*a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical*

communication with the memory controller." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [19.b.1] of the 024 Patent correspond to claim elements [1.a] and [1.d] of the '623 patent, and claim element [1.b] of the '218 and '595 patents, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp. 9-20; EX1102 ('218 FWD), pp.44-46; EX1103 ('595 FWD), pp.44-45.

391. As shown in the table below, claim element [19.b.1] is very similar to claim element [1.b.1]:

Claim 1	**Claim 19**
[1.b.1] a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,	[19.b.1] a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,

392. For the same reasons discussed above with reference to claim limitation [1.b.1], the prior art references in Grounds 1-6 satisfy "*a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller*." *See supra* ¶¶226-229.

c) [19.b.2]

393. Claim 19 requires "*the edge connections including first edge connections, second edge connections, and an error edge connection in addition to*

the first edge connections and the second edge connections." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [19.b.1] of the 024 Patent correspond to claim element [1.d] of the '623 patent, and claim element [1.b] of the '218 and '595 patents, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-20; EX1102 ('218 FWD), pp.44-46; EX1103 ('595 FWD), pp.44-45.

394. As shown in the table below, claim element [19.b.2] is very similar to claim element [1.b.2]:

Claim 1	**Claim 19**
[1.b.2] the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;	[19.b.2] the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

395. For the same reasons discussed above with reference to claim limitation [1.b.2], the prior art references in Grounds 1-6 satisfy "*the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections*." *See supra* ¶¶230-234.

d) [19.c.1]

396. Claim 19 requires "*a module controller on the printed circuit board*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [19.c.1]

of the 024 Patent correspond to claim elements [1.a], [1.b], and [1.d] of the '623 patent, and claim element [1.d] of the '218 and '595 patents, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-20; EX1102 ('218 FWD), pp.46-47; EX1103 ('595 FWD), pp.45-46.

397. As shown in the table below, claim element [19.c.1] is very similar to claim element [1.c.1]:

Claim 1	**Claim 19**
[1.c.1] a module controller on the printed circuit board and	[19.c.1] a module controller on the printed circuit board and

398. For the same reasons discussed above with reference to claim limitation [1.c.1], the prior art references in Grounds 1-6 satisfy "*a module controller on the printed circuit board*." *See supra* ¶¶235-237.

e) [19.c.2]

399. Claim 19 requires "*configured to receive from the memory controller via the first edge connections address and control signals associated with normal memory read or write operations*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [19.c.2] of the 024 Patent correspond to claim elements [1.a] and [1.d] and claim 2 of the '623 patent, claim elements [1.b] and [1.g.i] of the '218 patent, and claim elements [1.b] and [1.f.i] of the '595 patent, which the Board already found obvious over the combination of Hazelzet and

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Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), pp.74-77; EX1103 ('595 FWD), pp.58-59.

400. As shown in the table below, claim element [19.c.2] is very similar to claim elements [1.b.1] and [1.c.2]:

Claim 1	**Claim 19**
[1.b.1] a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, [1.c.2] configured to receive address and control signals associated with normal memory read or write operations via the first edge connections; and	[19.c.2] configured to receive from the memory controller via the first edge connections address and control signals associated with normal memory read or write operations; and

401. For the same reasons discussed above with reference to claim limitations [1.b.1] and [1.c.2], the prior art references in Grounds 1-6 satisfy "*configured to receive from the memory controller via the first edge connections address and control signals associated with normal memory read or write operations*." *See supra* ¶¶226-229, 238-242.

f) [19.d.1]

402. Claim 19 requires "*dynamic random access memory elements on the printed circuit board*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [19.d.1] of the 024 Patent correspond to claim elements [1.a] and

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[1.d] and claim 2 of the ’623 patent, and claim element [1.c] of the ’218 and ’595 patents, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 (’623 FWD), pp.9-21; EX1102 (’218 FWD), pp.74-77; EX1103 (’595 FWD), pp.58-59.

403. As shown in the table below, claim element [19.d.1] is very similar to claim element [1.d.1]:

Claim 1	**Claim 19**
[1.d.1] dynamic random access memory elements on the printed circuit board and	[19.d.1] dynamic random access memory elements on the printed circuit board and

404. For the same reasons discussed above with reference to claim limitation [1.d.1], the prior art references in Grounds 1-6 satisfy “*dynamic random access memory elements on the printed circuit board*.” *See supra* ¶¶243-245.

g) [19.d.2]

405. Claim 19 requires “*configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals*.” As discussed above, *supra at* ¶¶153-155, the limitations of claim element [19.d.2] of the 024 Patent correspond to claim element [1.d] and claim 2 of the ’623 patent, claim element [1.f] of the ’218 patent, and claim element [1.f.ii] of the ’595 patents, which the Board already found obvious over

the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), pp.74-77; EX1103 ('595 FWD), pp.58-59.

406. As shown in the table below, claim element [19.d.2] is very similar to claim element [1.d.2]:

Claim 1	**Claim 19**
[1.d.2] configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and	[19.d.2] configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and

407. For the same reasons discussed above with reference to claim limitation [1.d.2], the prior art references in Grounds 1-6 satisfy "*configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals*." *See supra* ¶¶246-252.

h) [19.e.1]

408. Claim 19 requires "*wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [19.e.1] of the 024 Patent correspond to claim element [1.d] and claims 7-8 of the '623 patent, and claim element [1.d] and claims 3-4 of the '218 and '595 patents, which the Board already found obvious over the

combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), pp.74-77; EX1103 ('595 FWD), pp.58-59.

409. As shown in the table below, claim element [19.e.1] is very similar to claim element [1.e.1]:

Claim 1	**Claim 19**
[1.e.1] wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;	[19.e.1] wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;

410. For the same reasons discussed above with reference to claim limitation [1.e.1], the prior art references in Grounds 1-6 satisfy "*wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate*." *See supra* ¶¶253-272.

i) [19.e.2]

411. Claim 19 requires "*wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [19.e.2] of the 024 Patent correspond to claim element [1.b] and claims 2, 7, and 9 of the '623 patent, claim elements [1.f] and [1.h] and claim 5 of the '218 patent, and claim elements [1.e.ii] and [1.f.iii] and claim 5 of the '595 patent,

which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), pp.74-77; EX1103 ('595 FWD), pp.58-59.

412. As shown in the table below, claim element [19.e.2] is very similar to claim element [1.e.2]:

Claim 1	**Claim 19**
[1.e.2] wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation; and	[19.e.2] wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation;

413. For the same reasons discussed above with reference to claim limitation [1.e.2], the prior art references in Grounds 1-6 satisfy "*wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation*." *See supra* ¶¶273-279.

j) [19.e.3]

414. Claim 19 requires "*wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access*

memory elements are not accessed for any normal memory read or write operations." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [19.e.3] of the 024 Patent correspond to claim element [1.c] and claims 2 and 8 of the '623 patent, claim elements [1.e.ii], [1.f] and [1.i] and claims 4 and 7 of the '218 patent, and claim element [1.e.iii] and claim 7 of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), pp.47-50, 63-64, 67-68; EX1103 ('595 FWD), pp.47-48, 73-74.

415. As shown in the table below, claim element [19.e.3] is very similar to claim element [1.e.3]:

Claim 1	**Claim 19**
[1.e.3] wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations.	[19.e.3] wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations;

416. For the same reasons discussed above with reference to claim limitation [1.e.3], the prior art references in Grounds 1-6 satisfy "*wherein the module controller is further configured to apply a second signal related to one or*

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more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations." *See supra* ¶¶280-289.

k) [19.f]

417. Claim 19 requires "*wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [19.f] of the 024 Patent correspond to claim 9 of the '623 patent, and claim 5 of the '218 and '595 patents, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.20-21; EX1102 ('218 FWD), pp.64-66; EX1103 ('595 FWD), pp.69-71.

418. As shown in the table below, claim element [19.f] is very similar to Claim 5:

Claim 5	**Claim 19**
[5] The memory module of claim 4, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.	[19.f] wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground;

419. For the same reasons discussed above with reference to Claim 5, the prior art references in Grounds 1-6 satisfy "*wherein the first signal drives the gate*

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of the transistor high to provide a low impedance path between the error edge connection and ground." *See supra* ¶¶303-307.

l) [19.g]

420. Claim 19 requires "*wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to a low impedance state, and drives the gate of the transistor low so as to drive the error edge connection to a high impedance state*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [19.g] of the 024 Patent correspond to claim 8 of the '623 patent, claim 4 of the '218 patent, and claim element [1.g] and claim 7 of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.20-21; EX1102 ('218 FWD), pp.63-64; EX1103 ('595 FWD), pp.50-52, 73-74.

421. As shown in the table below, claim element [19.g] is very similar to Claim 4:

Claim 4	**Claim 19**
[4] The memory module of claim 2, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.	[19.g] wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to a low impedance state, and drives the gate of the transistor low so as to drive the error edge connection to a high impedance state;

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422. While claim 4 refers to driving the output to "the low logic level," and claim element [19.g] instead refers to driving the output to a "low impedance state," both are describing the same operation. As explained above in detail, *supra* ¶¶46-54, when the transistor of an open-drain output is in a "low impedance state," the output is driven to ground, i.e., "the low logic level." *See*, *e.g.*, EX1089, pp.207-208 ("the transistor conducts and there is a low impedance path from the I/O pin to ground through the transistor"). Thus, for the same reasons discussed above with reference to Claim 4, the prior art references in Grounds 1-6 satisfy "*wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to a low impedance state, and drives the gate of the transistor low so as to drive the error edge connection to a high impedance state*." *See supra* ¶¶300-302.

m) [19.h]

423. Claim 19 requires "*wherein the module controller comprises an integrated circuit that includes the transistor*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [19.h] of the 024 Patent correspond to claims 6 and 7 of the '623 patent, claims 2 and 3 of the '218 and '595 patents, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.20-21; EX1102 ('218 FWD), pp.61-63; EX1103 ('595 FWD), pp.66-68.

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424. As shown in the table below, claim element [19.h] is very similar to Claim 6:

Claim 6	**Claim 19**
[6] The memory module of claim 1, wherein the module controller comprises an integrated circuit that includes the transistor.	[19.h] wherein the module controller comprises an integrated circuit that includes the transistor; and

425. For the same reasons discussed above with reference to Claim 6, the prior art references in Grounds 1-6 satisfy "*wherein the module controller comprises an integrated circuit that includes the transistor*." *See supra* ¶¶308-310.

n) [19.i]

426. Claim 19 requires "*wherein the integrated circuit further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences*." As discussed above, *supra at* ¶¶153-155, the limitations of claim element [19.i] of the 024 Patent correspond to claims 8-10 of the '623 patent, claim elements [1.f], [1.h], and [1.i] and claims 4-6 of the '218 patent, and claim element [1.e.ii] and claim 6 of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD),

pp.20-21; EX1102 (’218 FWD), pp.47-53, 63-67; EX1103 (’595 FWD), pp.46-47, 71-73.

427. As shown in the table below, claim element [19.i] is very similar to Claim 9:

Claim 9	**Claim 19**
[9] The memory module of claim 1, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input configured to receive the first signal, and a second input configured to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.	[19.i] wherein the integrated circuit further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.

428. For the same reasons discussed above with reference to Claim 9, the prior art references in Grounds 1-6 satisfy “*wherein the integrated circuit further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to*

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couple the second input to the output during the operations associated with the one or more training sequences." *See supra* ¶¶320-325.

20. Claim 20

429. Claim 20 requires "*The memory module of claim 19, wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections*." As discussed above, *supra at* ¶¶153-155, the limitations of claim 7 of the 024 Patent correspond to claim elements [1.c] and [1.d] and claim 2 of the '623 patent, claim elements [1.e.ii] and [1.f] and claim 7 of the '218 patent, and claim element [1.e.iii] and claim 9 of the '595 patent, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-21; EX1102 ('218 FWD), pp.47-50, 67-68; EX1103 ('595 FWD), pp.47-48, 74-75.

430. As shown in the table below, Claim 20 is very similar to Claim 7:

Claim 7	**Claim 20**
[7] The memory module of claim 1, wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.	[20] The memory module of claim 19, wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.

431. For the same reasons discussed above with reference to Claim 7, the prior art references in Grounds 1-6 satisfy "*wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections*." *See supra* ¶¶311-316.

D. <u>Secondary Considerations</u>

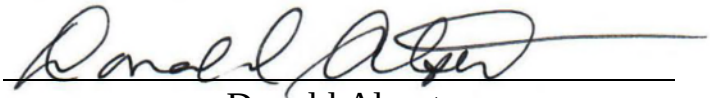
432. As noted above, I am not presently aware of any evidence of "objective factors" suggesting the claims are not obvious, and I reserve my right to address any such evidence if it is identified in the future.

* * *

I, Donald Alpert, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the

knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: October 3, 2024



Donald Alpert

Samsung Electronics Co., Ltd.
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EXHIBIT LIST

Exhibit #	Description
1001	U.S. Patent No. 11,386,024
1002	File History of U.S. Patent No. 11,386,024
1003	Declaration of Donald Alpert
1004	Curriculum Vitae of Donald Alpert
1005	File History of U.S. Patent Application No. 15/088,115 (i.e., U.S. Patent No. 9,858,218)
1006	File History of U.S. Patent Application No. 13/942,721 (i.e., U.S. Patent No. 9,311,116)
1007	File History of U.S. Patent Application No. 12/815,339 (i.e., U.S. Patent No. 8,489,837)
1008	U.S. Provisional App. No. 61/186,799
1009	U.S. Patent Publication No. 2010/0042778 to Tanguay et al.
1010	U.S. Patent Publication No. 2003/0115427 to Roohparvar
1011	U.S. Patent Publication No. 2010/0202240 to Moshayedi et al.
1012	U.S. Patent Publication No. 2008/0256281 to Fahr et al.
1013	U.S. Patent Publication No. 2010/0142383 to Goishi et al.
1014	U.S. Patent Publication No. 2008/0098277 to Hazelzet
1015	JEDEC COMMITTEE LETTER BALLOT, LRDIMM DDR3 Memory Initialization Chapter Proposal (Dec. 2009) (“JEDEC”)
1016	U.S. Patent No. 8,139,430 to Buchmann et al.
1017	U.S. Patent No. 8,359,521 to Kim et al.
1018	U.S. Patent No. 8,407,441 to Giovannini et al.

Exhibit #	Description
1019	U.S. Patent No. 8,489,837 to Lee
1020	U.S. Patent No. 3,414,781 to Dill
1021	*SK hynix Inc. et al. v. Netlist, Inc*., IPR2017-00548, Exhibit 1021, (PTAB December 11, 2017) (Deposition of Robert J. Murphy in 837 Patent IPR)
1022	U.S. Patent Application Pub. 2008/0147897 to Talbot
1023	U.S. Patent Application Pub. 2008/0155378 to Amidi
1024	JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000) ("JESD79")
1025	JEDEC Standard, FBDIMM: Architecture and Protocol (January 2007) ("JESD206")
1026	JEDEC Standard, FBDIMM Advanced Memory Buffer (AMB) (March 2009) ("JESD82-20A")
1027	U.S. Patent No. 7,411,862 to Hein et al.
1028	US Patent App. Publication No. 2006/0277355 by Ellsberry et al.
1029	JEDEC Standard, Low Power Double Data Rate (LPDDR) SDRAM Specification (August 2007) ("JESD209")
1030	U.S. Patent Pub. No. 2007/0008791 to Butt
1031	U.S. Patent No. 9,535,623 (623 Patent)
1032	*SK hynix, Inc. et al. v. Netlist, Inc*., IPR2018-00303, Paper No. 1 (PTAB December 14, 2017) (623 Patent IPR Petition)
1033	*SK hynix, Inc. et al. v. Netlist, Inc*., IPR2018-00303, Exhibit 1003 (PTAB December 14, 2017) (Alpert Declaration in 623 Patent IPR)
1034	*SK hynix, Inc. et al. v. Netlist, Inc*., IPR2018-00303, Paper No. 42 (PTAB March 21, 2019) (623 Patent Final Written Decision)

Exhibit #	Description
1035	*SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00548, Paper No. 25 (PTAB May 3, 2018) (837 Patent Final Written Decision)
1036	JEDEC COMMITTEE LETTER BALLOT, DDR3 LRDIMM Design Specification Body (Dec. 2009)
1037	JEDEC, Compilation of Tallies for JC-40 CMOS Digital Logic and point committees (Dec. 4, 2009)
1038	File History of U.S. Patent Application No. 15/169,745 (i.e., U.S. Patent No. 9,535,623)
1039	Inphi Corporation, "MB Initialization sequence Item 142.35," June 4, 2009
1040	U.S. Patent No. 8,386,737 to Jeon et al.
1041	Petitioner's Reply, *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00548, Paper 14 (PTAB December 11, 2017).
1042	"Sequence," https://www.lexico.com/en/definition/sequence
1043	U.S. Patent No. 7,222,213 to James
1044	Texas Instruments, "*28-Bit to 56-Bit Registered Buffer with Address Parity Test One Pair to Four Pair Differential Clock PLL Driver*" (October 2008)
1045	Micron, "*High-Speed DRAM Controller Design*" (2008)
1046	JEDEC, "*Minutes of Meeting No. 158 JC-40 Digital Logic Committee*" (June 4, 2009)
1047	*SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00548, Exhibit 2009, (PTAB September 6, 2017)
1048	JEDEC, JEDEC Manual of Organization and Procedure, JM21P (Rev. of JM21N, May 2008) (May 2010)

Exhibit #	Description
1049	JEDEC, JEDEC Manual of Organization and Procedure, JM21N (Rev. of JM21M, December 2006) (May 2008)
1050	Declaration of Julie Carlson
1051	JEDEC, "Committee Letter Ballot, JC-40.4-09-320, Item 142.35," (Dec. 2009)
1052	JEDEC, "Committee Letter Ballot, JC-45.4-09-321, Item 2192.44," (Dec. 2009)
1053	JEDEC, "Tally of Votes, Committee Letter Ballot, JC-45.4-09-321, 2192.44" (Dec. 9, 2009)
1054	Declaration of John Halbert
1055	Declaration of Sung Joo Park
1056	JEDEC Standard, DDR3 SDRAM, JESD79-3C (November 2008) ("JESD79-3C")
1057	U.S. Patent No. 7,647,467 to Hutsell et al.
1058	*SK hynix Inc. et al. v. Netlist, Inc*., IPR2020-1042, Paper No. 1 (PTAB June 8, 2020) (595 Patent Petition)
1059	*SK hynix Inc. et al. v. Netlist, Inc*., IPR2020-1042, Paper No. 14 (PTAB December 17, 2020) (595 Patent Institution Decision)
1060	*SK hynix Inc. et al. v. Netlist, Inc*., IPR2020-1042, Paper No. 25 (PTAB May 6, 2021) (595 Patent Termination Order)
1061	*Netlist, Inc. v. SK hynix Inc. et al*., 6-20-cv-00194-ADA (W.D. Tex. March 12, 2021) (Claim Construction Order)
1062	*SK hynix Inc. et al. v. Netlist, Inc*., IPR2020-1044, Paper No. 1 (PTAB June 8, 2020) (218 Patent Institution Decision)
1063	Netlist's 8-K announcing patent cross license with Samsung on November 12, 2015

Exhibit #	Description
1064	Defendant Samsung's Motion for Judgment on the Pleadings in *Netlist Inc. v. Samsung Electronics Co., Ltd.*, No. 8:20-cv-00993, ECF No. 60 (C.D. Cal. June 22, 2021)
1065	Order denying Samsung's Motion for Judgment on the Pleadings in *Netlist Inc. v. Samsung Electronics Co., Ltd.*, No. 8:20-cv-00993, ECF No. 120 (C.D. Cal. Aug. 5, 2021)
1066	Plaintiff Netlist's Motion for Partial Summary Judgment in *Netlist Inc. v. Samsung Electronics Co., Ltd.*, No. 8:20-cv-00993, ECF No. 145 (C.D. Cal. Aug. 16, 2021)
1067	Complaint for Declaratory Judgment of Non-Infringement in *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)
1068	First Amended Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Jan. 18, 2022)
1069	Tektronix Application Note, *Electrical Verification of DDR Memory* (2009)
1070	Bruce Jacob et al., *Memory Systems: Cache, DRAM, Disk* (2008)
1071	JEDEC's 2009 Meeting Schedule (Apr. 6, 2009), https://web.archive.org/web/20090406143859/ http://www.jedec.org/service_members/ Meetings/09Sch.cfm
1072	JEDEC's Catalogue (Apr. 21, 2009), http://web.archive.org/web/20090421000459/ http://www.jedec.org/Catalog/display.cfm
1073	Join JEDEC (Apr. 10, 2009), https://web.archive.org/web/20090410060243/ http:/www.jedec.org/join_jedec/default.cfm

Exhibit #	Description
1074	JEDEC Member Companies (May 5, 2009), https://web.archive.org/web/20090505225114/ http://www.jedec.org/service_members/ New_Members/memberco.cfm
1075	JEDEC Benefits (Apr. 13, 2009), https://web.archive.org/web/20090413045324/ http:/www.jedec.org/join_jedec/benefits.cfm
1076	Declaration by the Internet Archive for Exhibits 1071–75 (Aug. 5, 2022)
1077	Transcript of Deposition of Robert J. Murphy (Oct. 27, 2022)
1078	Redline comparing Declaration of Robert J. Murphy in IPR2022-00064 (595 Patent) [Ex. 1106] to Declaration of Robert J. Murphy in IPR2022-00062 (218 Patent) [Ex. 1105]
1079	Netlist's Technology Tutorial
1080	[Replaced by Exhibit 1081] Annotation of DDR3 LRDIMM showing location of (1) Host Interface CA Clk-to-CMD Training, (2) MB Initialization, (3) MB-DRAM Training, and (4) Host-MB Training
1081	Corrected annotation of DDR3 LRDIMM showing location of (1) Host Interface CA Clk-to-CMD Training, (2) MB Initialization, (3) MB-DRAM Training, and (4) Host-MB Training
1082	Petitioner's Demonstratives for Oral Argument on February 15, 2023
1083	JEDEC 21-C Standard, DDR SDRAM Registered DIMM (Jan. 2002)
1084	JESD79-2B, JEDEC DDR2 SDRAM Standard (Jan. 2005)
1085	JESD79-3, JEDEC DDR3 SDRAM Standard (June 2007) (Exhibit 1037 in IPR2018-00303)
1086	JEDEC's Catalogue (July 27, 2004), https://web.archive.org/web/20040727032111/ http://www.jedec.org/Catalog/display.cfm

Exhibit #	Description
1087	JEDEC download page for JESD99A.01 (Nov. 26, 2003), https://web.archive.org/web/20031126173530/ http://www.jedec.org/download/search/jesd99a01.pdf
1088	JEDEC Standard JESD99A.01, *Terms, Definitions, and Letter Symbols for Microelectronics Devices* (May 2003)
1089	Harold S. Stone, *Microcomputer Interfacing* (1982)
1090	U.S. Patent No. 8,386,722 to Wang et al.
1091	Deposition of John Bentley Halbert, III (July 22, 2022) [Exhibit 2022 in IPR2022-00062 and -00064]
1092	Deposition of Julie Carlson (July 22, 2022) [Exhibit 2024 in IPR2022-00062 and -00064]
1093	Deposition of Sung Joo Park (July 28, 2022) [Exhibit 2025 in IPR2022-00062 and -00064]
1094	U.S. Patent No. 9,311,116 (issued Apr. 12, 2016)
1095	U.S. Patent No. 9,858,218 (issued Jan. 2, 2018)
1096	File History of U.S. Patent No. 10,474,595
1097	U.S. Patent No. 10,474,595
1098	Petition of *Inter Partes* Review of U.S. Patent No. 9,858,218, IPR2022-00062, Paper No. 1 (PTAB Oct. 15, 2021)
1099	Declaration of Dr. Donald Alpert Regarding U.S. Patent No. 9,858,218, IPR2022-00062, Exhibit 1003 (PTAB Oct. 15, 2021)
1100	Petition of *Inter Partes* Review of U.S. Patent No. 10,474,595, IPR2022-00064, Paper No. 1 (PTAB Oct. 15, 2021)
1101	Declaration of Dr. Donald Alpert Regarding U.S. Patent No. 10,474,595, IPR2022-00064, Exhibit 1003 (PTAB Oct. 15, 2021)

Exhibit #	Description
1102	Final Written Decision, IPR2022-00062, Paper No. 54 (PTAB May 8, 2023) (U.S. Patent No. 9,858,218)
1103	Final Written Decision, IPR2022-00064, Paper No. 54 (PTAB May 9, 2023) (U.S. Patent No. 10,474,595)
1104	Order dismissing appeals of IPR2022-00062 and -00064, *Netlist, Inc. v. Samsung Electronics Co., Ltd.*, No. 23-2182 (Fed. Cir. Oct. 19, 2023)
1105	Declaration of Robert J. Murphy, Ex. 2027 in IPR2022-00062 (218 Patent)
1106	Declaration of Robert J. Murphy, Ex. 2027 in IPR2022-00064 (595 Patent)
1107	Deposition of Steven Przybylski (Feb. 15–16, 2024)
1108	Institution Decision, IPR2022-00062, Paper No. 14 (PTAB May 16, 2022) (U.S. Patent No. 9,858,218)
1109	Final Written Decision, IPR2022-00064, Paper No. 14 (PTAB May 16, 2022) (U.S. Patent No. 10,474,595)
1110	U.S. Patent Application No. 12/144,396 to Wang (filed June 23, 2008)
1111	[intentionally omitted]
1112	[intentionally omitted]
1113	*Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation* (June 21, 2022)
1114	Complaint for Declaratory Judgment of Non-Infringement in *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:23-cv-01122 (D. Del. filed Oct. 9, 2023) (U.S. Patent No. 11,386,024)

Exhibit #	Description
1115	Complaint for Declaratory Judgment of Non-Infringement in *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:24-cv-00614 (D. Del. filed May 22, 2024) (U.S. Patent No. 11,880,319)

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CLAIM LISTING

Ref. #	Listing of Challenged Claims in the 024 Patent
1.a	A memory module operable with a memory controller of a host system, comprising:
1.b.1	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,
1.b.2	the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;
1.c.1	a module controller on the printed circuit board and
1.c.2	configured to receive address and control signals associated with normal memory read or write operations via the first edge connections; and
1.d.1	dynamic random access memory elements on the printed circuit board and
1.d.2	configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and
1.e.1	wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;
1.e.2	wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation; and
1.e.3	wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations.
2	The memory module of claim 1, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

Ref. #	Listing of Challenged Claims in the 024 Patent
3	The memory module of claim 2, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state.
4	The memory module of claim 2, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.
5	The memory module of claim 4, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.
6	The memory module of claim 1, wherein the module controller comprises an integrated circuit that includes the transistor.
7	The memory module of claim 1, wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.
8	The memory module of claim 1, wherein the second edge connections are not active during the operations associated with the one or more training sequences.
9	The memory module of claim 1, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input configured to receive the first signal, and a second input configured to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.
10.a	A method of operation in a host system having a memory controller, comprising:
10.b.1	at a memory module coupled to the memory controller,
10.b.2	the memory module including a printed circuit board,
10.c	a module controller on the printed circuit board, and
10.d	dynamic random access memory elements on the printed circuit board,

Ref. #	Listing of Challenged Claims in the 024 Patent
10.e.1	the printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,
10.e.2	the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections,
10.f	the module controller including a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;
10.g	receiving, at the module controller, address and control signals associated with one or more normal memory read or write operations from the memory controller via the first edge connections;
10.h	outputting or receiving data signals at the dynamic random access memory elements in accordance with the address and control signals, the data signals being associated with the one or more normal memory read or write operations and communicated with the memory controller via the second edge connections;
10.i	applying a first signal to the gate of the transistor to indicate a parity error having occurred during one of the one or more normal memory read or write operations;
10.j	performing training operations associated with one or more training sequences when the dynamic random access memory elements are not accessed for any normal memory read or write operations; and
10.k	applying a second signal related to the one or more training sequences to the gate of the transistor while the memory module performs the training operations.
11	The method of claim 10, wherein the error edge connection is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.
12	The method of claim 11, wherein the error edge connection is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state.

Ref. #	Listing of Challenged Claims in the 024 Patent
13	The method of claim 11, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.
14	The method of claim 13, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground1.
15	The method of claim 10, wherein the module controller comprises an integrated circuit that includes the transistor.
16	The method of claim 10, wherein the training operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.
17	The method of claim 10, wherein the second edge connections are not active during the training operations associated with the one or more training sequences.
18	The method of claim 10, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein applying the first signal to the gate of the transistor includes coupling the first input to the output, and applying the second signal to the gate of the transistor includes coupling the second input to the output.
19.a	A memory module operable with a memory controller of a host system, comprising:
19.b.1	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,
19.b.2	the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;
19.c.1	a module controller on the printed circuit board and

Ref. #	Listing of Challenged Claims in the 024 Patent
19.c.2	configured to receive from the memory controller via the first edge connections address and control signals associated with normal memory read or write operations; and
19.d.1	dynamic random access memory elements on the printed circuit board and
19.d.2	configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and
19.e.1	wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;
19.e.2	wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation;
19.e.3	wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations;
19.f	wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground;
19.g	wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to a low impedance state, and drives the gate of the transistor low so as to drive the error edge connection to a high impedance state;
19.h	wherein the module controller comprises an integrated circuit that includes the transistor; and

Ref. #	Listing of Challenged Claims in the 024 Patent
19.i	wherein the integrated circuit further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.
20	The memory module of claim 19, wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.

Ref. #	Listing of Invalidated Claims in the '623 Patent [EX1031, EX1034]
1.a	A memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system, the memory module comprising:
1.b	a module controller having an open drain output, the module controller generating a parity error signal and driving the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode, the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode, wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system,
1.c	the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode and outputting the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode; and
1.d	a printed circuit board having a first set of edge connections for communicating address and control signals from the memory controller of the host system, a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module controller,
1.e	the memory module communicating to the memory controller of the host system via the error edge connection the parity error signal while the memory module operates in the first mode and the notification signal while the memory module is in the second mode.
2	The memory module of claim 1, further comprising: a plurality of synchronous dynamic random access memory elements, wherein, while the memory module is in the first mode, the module controller receives and processes address and control signals corresponding to read or write commands from the memory controller of the host system and transmits processed address and control signals to the plurality of synchronous dynamic random access memory elements.

Ref. #	Listing of Invalidated Claims in the ’623 Patent [EX1031, EX1034]
3	The memory module of claim 1, wherein, while the memory module is in the second mode, the module controller drives the notification signal to a logic low level via the open drain output to indicate a status of the one or more training sequences.
4	The memory module of claim 1, wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module.
5	The memory module of claim 1, wherein the one or more training sequences are executed by the module controller in response to a command or a signal received from the memory controller of the host system.
6	The memory module of claim 1, wherein the module controller comprises one or more integrated circuit.
7	The memory module of claim 1, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.
8	The memory module of claim 7, wherein the notification circuit generates the notification signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.
9	The memory module of claim 7, wherein the notification circuit generates the parity error signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.
10	The memory module of claim 7, wherein the notification circuit generates the notification signal using one or more OR logic elements.
11	The memory module of claim 1, wherein the module controller implements the one or more training sequences in response to a signal or a command received from the memory controller of the host system.
12.a	A memory module to be coupled to a memory controller of a host system, the memory module comprising:

Ref. #	Listing of Invalidated Claims in the '623 Patent [EX1031, EX1034]
12.b	a plurality of synchronous dynamic random access memory elements;
12.c	a printed circuit board (PCB) having a first set of edge connections for communicating address and control signals from the memory controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in a first mode, the PCB further including an error edge connection in addition to the first set of edge connections and the second set of edge connections;
12.d	a module circuit controlling the plurality of synchronous dynamic random access memory elements in response to read and write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode,
12.e	the module circuit generating a parity error signal indicative of a parity error having occurred in the memory module while the memory module operates in the first mode,
12.f	the module circuit causing the memory module to enter a second mode in response to a command from the memory controller of the host system, the module circuit generating a notification signal in response to one or more training sequences while the memory module is in the second mode, the notification signal indicating a status of the one or more training sequences; and
12.g	a notification circuit having an open drain output coupled to the error edge connection of the PCB, the notification circuit driving the parity error signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module operates in the first mode, the notification circuit driving the notification signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the second mode.
13	The memory module of claim 12, wherein the memory module executes the one or more training sequences in response to a signal or a command from the memory controller of the host system.

Ref. #	Listing of Invalidated Claims in the '623 Patent [EX1031, EX1034]
14	The memory module of claim 12, wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module.
15	The memory module of claim 12, wherein the notification circuit generates the notification signal using one or more OR logic elements.
16	The memory module of claim 12, wherein the notification circuit is a physically separate circuit from the module circuit.
17	The memory module of claim 12, wherein the module circuit includes the notification circuit.
18	The memory module of claim 12, wherein the notification circuit includes one or more transistors each having an open drain coupled to the open drain output.
19	The memory module of claim 18, wherein the notification circuit generates the notification signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.
20	The memory module of claim 18, wherein the notification circuit generates the parity error signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.
21.a	A memory module operable in at least a first mode and a second mode, the memory module comprising:
21.b	a plurality of synchronous dynamic random access memory elements;
21.c	a printed circuit board (PCB) having a first set of edge connections for communicating address and control signals from the memory controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, the PCB further including an error edge connection in addition to the first set of edge connections and the second set of edge connections,

Ref. #	Listing of Invalidated Claims in the '623 Patent [EX1031, EX1034]
21.d	wherein the PCB is configured to fit into a corresponding slot connector of the host system; and
21.e	a module controller having an open drain output coupled to the error edge connection, the module controller being configured to transmit address and control signals to the plurality of synchronous dynamic random access memory elements in response to read or write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode, to generate a parity error signal indicating a parity error having occurred in the memory module while the memory module is in the first mode, and to transmit the parity error signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the first mode,
21.f	the module controller being further configured to cause the memory module to enter the second mode in response to a command from the memory controller of the host system, to generate a notification signal indicating a status of one or more training sequences while the memory module is in the second mode, and to transmit the notification signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the second mode.
22	The memory module of claim 21, wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module.
23	The memory module of claim 21, wherein the memory module executes the one or more training sequences in response to a command or a signal received from the memory controller of the host system.
24	The memory module of claim 21, wherein the module controller includes a notification circuit comprising one or more transistors, each of the one or more transistors having an open drain coupled to the open drain output.

Ref. #	Listing of Invalidated Claims in the ’623 Patent [EX1031, EX1034]
25	The memory module of claim 24, wherein the notification circuit is configured to generate the notification signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.
26	The memory module of claim 24, wherein the notification circuit is configured to generate the parity error signal by by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.
27	The memory module of claim 24, wherein the notification circuit is configured to generate the notification signal using one or more OR logic elements.
28	The memory module of claim 24, wherein the module controller comprises one or more integrated circuits.
29	The memory module of claim 21, wherein the module controller is further configured to implement the one or more training sequences in response to a signal or a command received from the memory controller of the host system.

Ref. #	Listing of Invalidated Claims in the ’218 Patent [EX1095, EX1102]
1.a	A memory module operable with a memory controller of a host system, comprising:
1.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;
1.c	dynamic random access memory elements on the printed circuit board;
1.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and
1.e	[i] wherein the memory module is operable in at least a first mode and a second mode, [ii] wherein the memory module in the first mode is configured to be trained with one or more training sequences;
1.f	wherein the memory module in the second mode is configured to perform one or more memory read or write operations not associated with the one or more training sequences by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections;
1.g	[i] wherein the module controller is configured to receive via the second edge connections the address and command signals associated with the one or more memory read or write operations and [ii] to control the dynamic random access memory elements in accordance with the address and command signals, and
1.h	wherein the module controller is further configured to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the second mode;

Ref. #	Listing of Invalidated Claims in the ’218 Patent [EX1095, EX1102]
1.i	wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output while the memory module is in the first mode.
2	The memory module of claim 1, wherein the module controller comprises an integrated circuit.
3	The memory module of claim 1, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.
4	The memory module of claim 3, wherein the notification circuit is configured to drive the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
5	The memory module of claim 4, wherein the notification circuit is configured to drive the parity error signal by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
6	The memory module of claim 4, wherein the notification circuit is configured to drive the notification signal using one or more OR logic elements.
7	The memory module of claim 1, wherein the first edge connections are not active when the memory module is in the first mode and configured to be trained with the one or more training sequences.
8	The memory module of claim 1, wherein the module controller is configured to drive the notification signal to indicate a status of the one or more training sequences.
9.a	A method performed by a memory module operating with a memory controller of the host system,
9.b	the memory module including dynamic random access memory elements on a printed circuit board,

Ref. #	Listing of Invalidated Claims in the ’218 Patent [EX1095, EX1102]
9.c	the printed circuit board having edge connections that fit into a corresponding slot of a host system, the edge connections including first edge connections via which the dynamic random access memory devices communicate data with the memory controller, second edge connections via which the memory module receives address and command signals from the memory controller, and an error edge connection in addition to the first edge connections and the second edge connections, the method comprising:
9.d	receiving from the memory controller address and command signals associated with one or more memory read or write operations;
9.e	controlling the dynamic random access memory elements in accordance with the address and command signals;
9.f	outputting to the memory controller via an open-drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module; and
9.g	training with one or more training sequences while the first edge connections are not active, and
9.h	driving a notification signal associated with the one or more training sequences to the memory controller via the open drain output and the error edge connection.
10	The method of claim 9, wherein driving the notification signal comprises driving a gate of each of one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground, the one or more transistors each having an open drain coupled to the open drain output.
11	The method of claim 10, wherein driving the signal indicating the parity error comprises driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground.
12	The method of claim 10, wherein driving the notification signal comprises using one or more OR logic elements.
13	The method of claim 9, wherein the memory module is configured to be trained with the one or more training sequences in response to a request by the memory controller.

Ref. #	Listing of Invalidated Claims in the ’218 Patent [EX1095, EX1102]
14	The method of claim 9, wherein the notification signal indicates a status of the one or more training sequences.
15.a	A memory module operable with a memory controller of a host system, comprising:
15.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and command signals, and an error edge connection in addition to the first edge connections and the second edge connections;
15.c	dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the first edge connections; and
15.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection;
15.e	wherein the memory module is configurable to perform at least a first operation and a second operation;
15.f	[i] wherein the module controller in the first operation is configured to receive via the second edge connections address and command signals associated with one or more memory read or write operations and [ii] to control the dynamic random access memory elements in accordance with the address and command signals,
15.g	wherein the module controller in the first operation is further configured to output to the memory controller a signal indicating a parity error having occurred in the memory module; and
15.h	wherein the memory module in the second operation is configured to be trained with one or more training sequences while the first edge connections are not active, and
15.i	wherein the module controller in the second operation is configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output of the module controller.

Ref. #	Listing of Invalidated Claims in the ’218 Patent [EX1095, EX1102]
16	The memory module of claim 15, wherein the module controller comprises an integrated circuit.
17	The memory module of claim 15, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.
18	The memory module of claim 17, wherein the notification circuit is configured to generate the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
19	The memory module of claim 18, wherein the notification circuit is configured to drive the signal indicating the parity error by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
20	The memory module of claim 18, wherein the notification circuit is configured to drive the notification signal using one or more OR logic elements.
21	The memory module of claim 15, wherein the memory module is configured to perform the second operation in response to a command from the memory controller.
22	The memory module of claim 15, wherein the module controller is configured to drive the notification signal to indicate a status of the one or more training sequences.

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Ref. #	Listing of Invalidated Claims in the ’595 Patent [EX1097, EX1103]
1.a	A memory module operable with a memory controller of a host system, comprising:
1.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;
1.c	dynamic random access memory elements on the printed circuit board;
1.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and
1.e	[i] wherein the memory module is configurable to operate in any of at least a first mode and a second mode; [ii] wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, [iii] wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and [iv] wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;

Ref. #	Listing of Invalidated Claims in the ’595 Patent [EX1097, EX1103]
1.f	[i] wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, [ii] wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and [iii] wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;
1.g	wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.
2	The memory module of claim 1, wherein the module controller comprises an integrated circuit.
3	The memory module of claim 1, wherein the module controller includes a notification circuit comprising a transistor having an open drain coupled to the open drain output and source coupled to the ground.
4	The memory module of claim 3, wherein the module controller is configurable to drive a gate of the transistor high so as to drive open drain output and the error edge connection to ground, or to drive the gate of the transistor low so as to drive the open drain output and the error edge connection to the high impedance state.
5	The memory module of claim 4, wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and the ground.

Ref. #	Listing of Invalidated Claims in the '595 Patent [EX1097, EX1103]
6	The memory module of claim 3, wherein the notification circuit further includes a multiplexor or a logic circuit having a output coupled to a gate of the transistor and configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.
7	The memory module of claim 3, wherein the module controller is configurable to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal so as to drive the open drain output from the high impedance state to ground or from ground to the high impedance state.
8	The memory module of claim 1, wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode.
9	The memory module of claim 1, wherein the memory module in the second mode is configurable to perform the operations related to the one or more training sequences without communicating data signals via the first edge connections while the memory module is in the second mode.
10.a	A memory module operable with a memory controller of a host system, comprising:
10.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;
10.c	dynamic random access memory elements on the printed circuit board;

Ref. #	Listing of Invalidated Claims in the '595 Patent [EX1097, EX1103]
10.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and
10.e	wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections;
10.f	wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;
10.g	wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode.
11	The memory module of claim 10, wherein the module controller comprises an integrated circuit.

Ref. #	Listing of Invalidated Claims in the ’595 Patent [EX1097, EX1103]
12.a	The memory module of claim 10, wherein the module controller includes a notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to the ground,
12.b	wherein the module controller is configurable to output to the memory controller the open-drain signals related to the one or more training sequences by driving a gate of the transistor high so as to drive the open drain output and the error edge connection to ground, and by driving the gate of the transistor low as to drive the open drain output and the error edge connection to the high impedance state,
12.c	and wherein the notification circuit is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and ground.
13	The memory module of claim 12, wherein the notification circuit further includes a multiplexor or a logic circuit having an output coupled to the gate of the transistor and configurable to drive the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.
14	The memory module of claim 10, wherein the module controller is configurable to output the open-drain signals related to the one or more training sequences by driving the open drain output from the high impedance state to the low logic level or from the low logic level to the high impedance state.
15	The memory module of claim 10, wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode.
16	The memory module of claim 10, wherein the second edge connections include one or more high-order address pins that are not active while the memory module is in the second mode.
17.a	A method, comprising:

Ref. #	Listing of Invalidated Claims in the '595 Patent [EX1097, EX1103]
17.b	at a memory module coupled with a memory controller of a host system, the memory module including a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections, the memory module further including dynamic random access memory elements on the printed circuit board;
17.c	receiving via the second edge connections address and control signals associated with one or more memory read or write operations; controlling the dynamic random access memory elements to communicate data signals corresponding to the one or more memory read or write operations via the first edge connections in response to the address and control signals; outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is being accessed by the memory controller for a memory read or write operation;
17.d	performing operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations; and outputting to the memory controller via the open drain output and the error edge connection open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation.
18	The method of claim 17, wherein the second edge connections include one or more pins that are not active while the memory module is trained with the one or more training sequences.
19	The method of claim 18, wherein the second edge connections include one or more high-order address pins that are not active while the memory module is trained with the one or more training sequences.
20.a	The method of claim 17, wherein the memory module includes a notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to ground,

Ref. #	Listing of Invalidated Claims in the ’595 Patent [EX1097, EX1103]
20.b	wherein outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module comprises driving a gate of the transistor high to provide a low impedance path between the open drain output and ground, and
20.c	wherein outputting the open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation comprises driving the gate of the transistor to drive the open drain output from a high impedance state to ground and from ground to the high impedance state.
21.a	A memory module operable with a memory controller of a host system, comprising:
21.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;
21.c	dynamic random access memory elements on the printed circuit board; and
21.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller including a transistor having a gate and an open drain output coupled to the error edge connection; wherein the module controller is configurable to drive the gate of the transistor so as to drive the open drain output to a first state or a second state, the first state being a low logic level and the second state being a high impedance state;

Ref. #	Listing of Invalidated Claims in the ’595 Patent [EX1097, EX1103]
21.e	[i] wherein the module controller is configurable to receive via the second edge connections memory commands associated with normal memory read or write operations and to output a set of address and control signals for each of the normal memory read or write operations; [ii] wherein the dynamic random access memory elements are configurable to communicate one or more N-bit-wide data signals with the memory controller via the first edge connections in response to the set of address and control signals, where N is at least 32; [iii] wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred during any of the memory read or write operations by driving the open drain output and the error edge connection to the first state;
21.f	wherein the memory module is configurable to perform operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations; and wherein the module controller is configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection from one of the first state and the second state to the other one of the first state and the second state.
22	The memory module of claim 21, wherein the module controller further includes a multiplexor or a logic circuit having an output coupled to the gate of the transistor, and wherein the module controller is configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.
23.a	The memory module of claim 22, wherein the transistor has a source coupled to ground,
23.b	wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and ground, and

Ref. #	Listing of Invalidated Claims in the ’595 Patent [EX1097, EX1103]
23.c	wherein the module controller is configurable to provide the information related to the one or more training sequences by driving the open drain output from a high impedance state to ground or from ground to the high impedance state.
24	The memory module of claim 21, wherein the memory module is configurable to perform the operations related to the one or more training sequences while the memory module is not communicating signals via the first edge connections.