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Application Number	Filed herewith
Filing Date	03/31/2016
First Named Inventor	HYUN LEE
Title	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	NETL.062C2

SIGNATURE of Applicant or Patent Practitioner

Signature	/Jamie J. Zheng/	Date	March 31, 2016
Name	Jamie J. Zheng	Telephone	650-521-4828
Registration Number	51,167		

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Ex. 1005, p. 2

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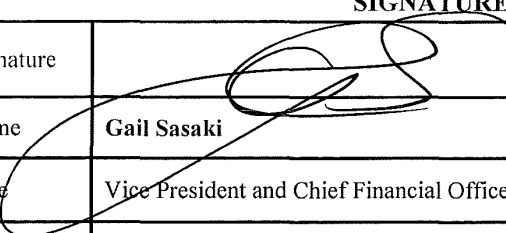
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SIGNATURE of Applicant for Patent

Signature		Date: January 9, 2013
Name	Gail Sasaki	
Title	Vice President and Chief Financial Officer	
Company	Netlist, Inc.	

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.062C2
		Application Number	
Title of Invention	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

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Title of the Invention	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		
Attorney Docket Number	NETL.062C2	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	3	Suggested Figure for Publication (if any)	4

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.062C2
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Title of Invention	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		

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Prior Application Status	Pending	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
	Continuation of	13942721	2013-07-16		
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13942721	Continuation of	12815339	2010-06-14	8489837	2013-07-16
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
12815339	non provisional of	61186799	2009-06-12		
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.062C2
		Application Number	
Title of Invention	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		

			Remove
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Clear		
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		Application Number	
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Name of the Deceased or Legally Incapacitated Inventor :			
If the Applicant is an Organization check here. ☒			
Organization Name	Netlist, Inc.		
Mailing Address Information:			
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Address 2			
City	Irvine	State/Province	CA
Country	US	Postal Code	92618
Phone Number	949-435-0025	Fax Number	
Email Address	gsasaki@netlist.com		
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SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. App. No. 13/942,721, filed July 16, 2013, to be issued as U.S. Pat. No. 9,311,116 on April 12, 2016, which is a continuation of U.S. App. No. 12/815,339, filed June 14, 2010, now U.S. Pat. No. 8,489,837, which claims the benefit of priority from U.S. Provisional App. No. 61/186,799, filed June 12, 2009, each of which is incorporated in its entirety by reference herein.

FIELD OF THE DISCLOSURE

[0002] The present disclosure relates to the operation of memory modules. Specifically, the present disclosure relates to systems and methods for handshaking with a memory module during or upon completion of initialization.

BACKGROUND OF THE DISCLOSURE

[0003] Memory subsystems such as memory modules are generally involved in the initialization procedure for computer systems, including servers, personal computers, and the like. For example, during system-wide initialization, the memory subsystems may undergo internal initialization procedures, or the system memory controller may otherwise interact with the memory subsystems during the initialization procedure. As part of this interaction, the system memory controller may request that the memory subsystem perform one or more requested tasks during system initialization.

SUMMARY

[0004] According to certain aspects, a memory module is coupled to a memory controller of a host computer system via an interface. The interface includes data, address and control signal pins and an output pin in addition to the data, address and control signal pins. The memory module receives a first command from the memory controller via the address and control signal pins, and enters a first mode in response to the first command. The memory module in the first mode responds to at least one initialization sequence, and sends a first output signal via the output pin to indicate a status of the at least one initialization sequence to the memory controller.

The memory module enters a second mode in which the memory module performs memory operations including memory read/write operations according to an industry standard. During the read/write operations, the memory module communicates data with the memory controller via the data signal pins in response to second memory commands received via the address and control signal pins. The memory module may output a second output signal related to the read/write operations via the output pin.

[0005] According to certain aspects, a memory module is coupled to a memory controller of a host computer system via an interface. The interface includes data, address and control signal pins and an output pin in addition to the data, address and control signal pins. The memory module performs an internal procedure in a first mode in response to a first command from the memory controller whereby the memory controller hands off control of the internal procedure to the first memory module. The memory module sends a first output signal via the output pin to indicate a status of the internal procedure to the memory controller. The memory module enters a second mode in which the memory module performs standard operations including one or more of memory read/write, pre-charge, refresh operations according to an industry standard. The memory module may output a second output signal related to the standard operations via the output pin.

[0006] In another aspect, a memory module is operable in a first mode and in a second mode. The memory module operates according to an industry standard in the second mode by performing standard operations including memory read/write operations in response to address and control signals from a memory controller of a host computer system. The memory module comprises a standard interface including data, address and control signal pins and an output pin in addition to the data, address and control signal pins. The memory module enters the first mode in response to a first command from the memory controller, in which the memory module responds to at least one initialization sequence. The memory module further comprises a notification circuit to output a notification signal indicating a status of the at least one initialization sequence to the memory controller via the output pin.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Figure 1 shows an example host computer system including an example memory

module configured to perform handshaking with a memory controller of the host computer system according to certain embodiments described herein.

[0008] Figure 2 shows an example host computer system including example first and second memory modules configured to perform handshaking with a system memory controller of the host computer system according to certain embodiments described herein.

[0009] Figure 3 shows a host computer system including example first and second memory modules configured to perform handshaking with a memory controller of the host system, where the notification circuits of the first and second memory modules have another example configuration according to certain embodiments described herein.

[0010] Figure 4 and Figure 5 show example methods of using at least one memory module according to certain embodiments described herein.

DETAILED DESCRIPTION

[0011] Existing initialization schemes have certain inefficiencies which lead to wasted time and expense. Thus, there is a need to reduce the time and complexity involved in system memory controller interactions with memory subsystems during initialization. Certain embodiments described herein advantageously satisfy at least a portion of this need by providing a system and method which utilizes a feedback path from a memory subsystem such as a memory module to a system memory controller, such as a Memory Controller Hub (MCH) of a computer system during initialization.

[0012] In general, there is no existing method of handshaking between the MCH (e.g., system memory controller) and a memory subsystem (e.g., memory module) during initialization. For example, in conventional systems, the system memory controller does not monitor the error-out signal from the memory subsystem. This causes the MCH to perform blind execution. In a typical server (e.g., an Intel or AMD or other chipset based server), the lack of any handshaking between the MCH and the memory subsystem during the server initialization period has not been a serious issue since the MCH generally has complete control over the initialization procedure. However, one possible configuration for LR-DIMM (Load Reduced DIMM) includes the MCH handing over one or more parts of the initialization operation sequence to the memory subsystem. This raises an unprecedented issue not addressed in

conventional systems because, in such proposed configurations, the system can benefit from the MCH handshaking with the memory subsystem controller, as described more fully below.

[0013] Such an LR-DIMM configuration may have the MCH inserting a waiting period of predetermined length during which the MCH is idle and the memory subsystem controller undergoes initialization. However, one shortcoming of this LR-DIMM configuration would be that it requires the MCH to be in standby (idle, or wait) while the memory subsystem controller completes its task. Under such an arrangement, since the time to complete a task can be dependent on the density, speed and configuration of the memory subsystem, and these parameters may be unknown to the MCH, the MCH may have to insert a single, predetermined standby period. In addition, if there are multiple occasions that the MCH needs to hand off control to the memory subsystem controller, the required MCH wait periods can be different from one occasion to another, and it complicates the correlation between the MCH and the memory subsystem controller. For example, the MCH according to such a scheme may give control to the local memory controller of a memory subsystem (e.g., memory module) for execution of a training sequence. The MCH may wait for a pre-determined period of time and then assume that the local memory controller has completed the training sequence. However, depending on the memory subsystem parameters (e.g., memory capacity, speed, number of ranks, etc.), the time for actually completing the training sequence may vary and may be longer or shorter than predetermined period of time.

[0014] In general, handshaking can be implemented in at least two ways; polling and notifying. In the polling method, the MCH reads a status register in the memory subsystem controller to find out if the memory subsystem controller has completed the required or requested operation. For example, a status register may be read out through a serial interface such as System Management Bus (SMBus). However, a register polling method is generally inefficient because the system memory controller does not know exactly when the memory subsystem will have completed the required or requested operation. Thus, the system memory controller may wait longer than necessary to poll the memory subsystem, thereby delaying the overall initialization process. Additionally, the problem may be compounded because multiple training sequences or other initialization sequences may be run on the memory subsystem during a particular initialization period, resulting in accumulation of such unnecessary delays. Moreover, polling generally involves scheduling polling intervals during which the system memory

controller is not performing other operations, resulting in further inefficiency.

[0015] Alternatively, the notifying method is an advantageous handshaking method between the MCH and the memory subsystem controller. According to a notifying method, the memory subsystem controller sends a signal to the MCH when the memory subsystem controller completes the required or requested operation. This method allows the MCH to execute one or more independent commands while it is waiting for a notification signal from the memory subsystem controller.

[0016] Certain embodiments described herein provide a method of establishing a handshake mechanism based on notification signaling. In certain embodiments, this mechanism can be implemented by adding a new interface (notifying) signal between the MCH and the memory subsystem controller, or by adding an additional functionality to an existing, non-timing critical signal without altering the memory subsystem hardware. In either case, the interface between the MCH and the memory subsystem controller of certain embodiments can be an open drain signaling from the memory subsystem controller to the MCH, although a variety of other configurations are possible. As will be appreciated by persons skilled in the art, the terms MCH, system memory controller, and memory subsystem are used generally interchangeable throughout this disclosure, and the terms memory module, memory subsystem controller, and local memory controller are used generally interchangeably throughout this disclosure.

[0017] FIG. 1 illustrates an example host computer system 16 including an example memory module 10 according to certain embodiments described herein. The memory module 10 can comprise at least one output 12 configured to be operatively coupled to a system memory controller 14 of the host computer system 16. In certain embodiments, the memory module 10 is configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode. The memory module 10 may further include a controller circuit 18. In some embodiments, the controller circuit 18 is configured to cause the memory module 10 to enter the initialization mode. The memory module 10 can further include a notification circuit 20 configured to drive the at least one output 12 while the memory module 10 is in the initialization mode to provide at least one notification signal to the memory controller 14 indicating at least one status of the at least one initialization sequence.

[0018] The memory module 10 may comprise a printed-circuit board (PCB) 22. In certain embodiments, the memory module 10 has a memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, 16-GB, or higher. Other memory capacities are also compatible with certain embodiments described herein. In addition, memory modules 10 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. The PCB 22 can have an industry-standard form factor. For example, the PCB 22 can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB 20 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB 22 has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FBDIMM), mini-DIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein. In other embodiments, certain non-DIMM form factors are possible such as, for example, single in-line memory module (SIMM), multi-media card (MMC), and small computer system interface (SCSI).

[0019] In certain embodiments, the memory module 10 is operatively coupled to (e.g., in electrical communication with) the host computer system 16. In certain other embodiments, the memory module 10 may communicate with the host computer system 16 using some other type of communication, such as, for example, optical communication. Examples of host computer systems 16 include, but are not limited to, blade servers, 1U servers, personal computers (PCs), and other applications in which space is constrained or limited. The PCB 22 can comprise an interface (not shown) that is configured to be in electrical communication with the host computer system 16. For example, the interface can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system 16. The interface of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory module 10 and the host system 16. For example, the interface can comprise a standard 240-pin DDR2 edge connector. The at least one output 12 may be routed over the interface, for example.

[0020] The memory module 10 may also comprise one or more memory elements (not shown), such as dynamic random-access memory (DRAM) elements, for example. Types of

DRAM elements compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, DDR4, and synchronous DRAM (SDRAM). In addition, memory elements having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Memory elements compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μ BGA), mini-BGA (mBGA), and chip-scale packaging (CSP). In certain embodiments, the memory module 10 may also include one or more non-volatile memory elements, such as one or more flash memory elements. Types of flash memory elements compatible with certain embodiments described herein include, but are not limited to, NOR flash, NAND flash, ONE-NAND flash, and multi-level cell (MLC).

[0021] The controller circuit 18 of certain embodiments generally controls the operation of the memory module 10. For example, the controller circuit 18 may control the memory elements of the memory module 10 and/or communicate with the system memory controller 14. For example, the controller circuit 18 may receive and process address and command signals (e.g., read, write commands) from the system memory controller 14 and transmit appropriate address and commands to the memory elements in response. See, e.g., U.S. Pat. Appl. Publ. Nos. 2006/0062047 A1 and 2006/0262586 A1, each of which is incorporated in its entirety by reference herein. In certain embodiments, the controller circuit 18 comprises a local memory controller. Additionally, depending on the architecture of the memory module 10, such as for an FB-DIMM, the controller circuit 18 may comprise an advanced memory buffer (AMB). The controller circuit 18 can comprise one or more of a field-programmable gate array (FPGA), a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, and a complex programmable logic device (CPLD), for example. In certain embodiments, the controller circuit 18 comprises various discrete electrical elements, while in certain other embodiments, the controller circuit 18 comprises one or more integrated circuits.

[0022] As discussed, the memory module 10 is configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode. In one embodiment, for example, the at least one initialization sequence may comprise one or more training sequences. The initialization

sequence (e.g., comprising one or more training sequences) may be initiated by the system memory controller 14. In some embodiments, the controller circuit 18 is configured to cause the memory module 10 to enter the initialization mode. For example, the controller circuit 18 may be configured to execute a routine implementing the at least one initialization sequence when the appropriate signal or command is received from the memory controller 14 or is otherwise received from the host computer system 16 (e.g., upon receipt of a reset signal).

[0023] In certain embodiments, for example, the computer system 16 is coupled to a plurality of memory modules 10, 26 including the memory module 10 and at least a second memory module 26, and the memory controller 14 (e.g., MCH) trains each module 10, 26 separately, in series. In one example scenario, the memory controller 14 issues a first command to the memory module 10, and, in response, the memory module 10 executes an initialization sequence (e.g., one or more training sequences). Upon completion of the initialization sequence, the first memory module 10 advantageously issues a notification to the memory controller 14 in accordance with embodiments described herein. In response, the memory controller 14 issues a second command, this time to the memory module 26, and, in response, the memory module 26 executes an initialization sequence (e.g., one or more training sequences). Upon completion of the initialization sequence, the second memory module 26, similar to the first memory module 10, advantageously issues a notification to the memory controller 14 in accordance with embodiments described herein. In response, where there are more than two memory modules 10, 26, the memory controller 14 issues a third command to a third memory module (not shown), and so forth. One example computer system 16 capable of implementing such a scenario is configured to execute an Intel Basic Input/Output System (BIOS), and comprises a plurality of memory modules 10, 26 having an LRDIMM configuration. In such an example system, the Intel BIOS causes the system memory controller 14 to initialize the LRDIMM memory modules 10, 26 serially.

[0024] The operational mode is the normal mode of the memory module 10. For example, during the operational mode, the memory module 10 is generally accessed by the system memory controller 14 of the host computer 16 during standard computer operation not associated with initialization. For example, the system memory controller 14 may cause the memory module 10 to perform standard operations such as memory read/write, pre-charge, refresh, etc., while in operational mode, although it will be appreciated that one or more of these

operations can also be performed by the memory module 10 while in initialization mode in certain embodiments.

[0025] The notification circuit 20 can be configured to drive the at least one output 12, while the memory module 10 is in the initialization mode or after the memory module 10 completes one or more initialization sequences, to provide the at least one notification signal to the memory controller 14 indicating at least one status of the at least one initialization sequence. While shown in FIGS. 1-3 as forming a part of the controller circuit 18, the notification circuit 20 may be a physically and/or logically separate circuit in certain embodiments. While a variety of configurations are possible, the notification circuit 20 may comprise one or more transistors, one or more logic elements (e.g., AND, OR, NOR, NAND, XOR gates, and the like), or a combination thereof. In some embodiments, the notification circuit 20 may additionally or alternatively comprise one or more of an FPGA, PLD, CPLD, ASIC, custom-designed semiconductor device, discrete electrical elements, and an integrated circuit.

[0026] The at least one status of certain embodiments comprises completion of the at least one initialization sequence, such that the at least one notification signal is indicative of the completion of the at least one initialization sequence. The at least one status of certain embodiments comprises execution of the at least one initialization sequence. For example, the at least one status may indicate that the at least one initialization sequence is currently being executed. In some embodiments, the at least one status may provide an indication that a certain task has been completed by the memory module 10, such as a training task requested by the system memory controller 14. In certain embodiments, the notification circuit 20 can be configured to drive the at least one output 12 to a first state indicative of execution of the at least one initialization sequence or to a second state indicative of completion of the at least one initialization sequence. As one example, the first state may be a high or low logic level, and the second state may be a high impedance state. In another case, the first state is a high or low logic level, and the second state is the inverse logic level of the first state.

[0027] The at least one output 12 of certain embodiments is configured to be operatively coupled to at least one interrupt of the system memory controller 14, and the system memory controller 14 is responsive to the at least one notification signal indicating completion of the at least one initialization sequence. For example, the system memory controller 14 may trigger

execution of an interrupt routine upon receipt of the notification signal on the output 12. The interrupt routine generally executes the appropriate operations for the at least one status indicated by the at least one notification signal. For example, if the at least one status indicates that the at least one initialization sequence is complete, execution of the interrupt routine may cause the system memory controller 14 to notify the host computer system 16 that the system initialization, or a portion thereof, is completed. In one embodiment, for example, the execution of the interrupt routine causes the system memory controller 14 to initiate a subsequent training sequence for the memory module 10 or on another memory module connected to the host system 16. For example, in one embodiment, a central processing unit (CPU) of the host system 16 (not shown) enters a “Wait” state after issuing a command to the memory module 10 to enter the initialization mode. Receipt of the at least one notification signal on the output 12 triggers execution of the interrupt routine, which interrupts the CPU, causing the “Wait” state to be aborted and allowing the host system 16 to continue operation. In this manner, generation of the interrupt on the at least one output 12 can allow completion of the at least one initialization sequence to receive generally immediate attention from the CPU and/or memory controller 14 of the host system 16. As will be appreciated, the CPU and memory controller 14 of the host system 16 may comprise separate modules, or may alternatively comprise a single integrated module, depending on the architecture of the host system 16 chip-set.

[0028] In certain embodiments, execution of the interrupt routine causes the system memory controller 14 to cause the memory module 10 to exit the initialization mode and to enter the operational mode. In another embodiment, the memory module 10 automatically enters the operational mode upon completion of the at least one initialization sequence without intervention from the memory controller 14.

[0029] In some embodiments, the at least one output 12 is operated in conformance with a standard (e.g., an industry standard) when the memory module 10 is in the operational mode, but is not operated in conformance with the standard when the memory module 10 is in the initialization mode. An example of a standard in accordance with certain embodiments described herein is one or more of the industry standard promulgated by the Joint Electronic Devices Engineering Counsel (JEDEC). For example, the operation and behavior of the at least one output 12 may conform to an industry standard when the memory module 10 is in the operational mode, but the operation and behavior of the at least one output 12 may not conform to the

industry standard when the memory module 10 is in the initialization mode. Because the at least one output 12 does not conform to the standard during initialization mode, an existing (e.g., JEDEC-specified) pin may be utilized to provide the at least one notification signal to the system memory controller 14 from the memory module 10 during the initialization mode. In one embodiment, for example, the at least one output 12 comprises an error-out pin of the memory module 10. In conventional systems, the operation of the error-out pin is undefined by the standard during initialization. However, in certain embodiments described herein, during the operational mode, the error-out pin may be used according a conventional industry standard (e.g., a JEDEC standard) to indicate a parity error has occurred in the memory module 10. During the initialization mode, the error-out pin can be used to transmit the at least one notification signal to the system memory controller 14.

[0030] It is advantageous to use the error-out pin for initialization status notification according to certain embodiments because the error-out pin can be asserted by the memory module 10 independent from system memory controller 14 requests or commands. Also, because the error-out pin is a JEDEC-specified pin, design cost and complexity are reduced because additional pin-outs and interrupt design changes can be avoided (e.g., in cases where such changes in hardware or chipset may not be feasible to provide the at least one status to the system memory controller 14). However, in certain other embodiments, providing the at least one status may be implemented by adding one or more pins to the system memory controller 14 (e.g., MCH) and to the controller circuit 18 (e.g., local memory controller), thereby utilizing changes in hardware or the chipset.

[0031] Moreover, the error-out pin may be coupled to an interrupt of the system memory controller 14 (e.g., according to the JEDEC standard). Thus, where the error-out pin is used, from the system point of view in accordance with certain embodiments, the notification of completion of the required or requested task from the memory module 10 (e.g., by the local memory controller) generates an interrupt communicated to the system during the initialization period and indicative of completion of the required or requested task. Assertion of the same pin during normal (non-initialization) operation upon an error occurring, on the other hand, generates an interrupt communicated to the system during the normal operation indicative of the occurrence of the error condition. Thus, in certain embodiments, the error-out pin and corresponding signal memory module 10 can be used to support the notifying function and to provide the at least one

status generally without changing hardware. Certain other such embodiments involve modifying the basic input/output system (BIOS) or other programming change. For example, the BIOS may be modified to indicate to the system memory controller 14 how to respond to the notification signal (e.g., to the error_out signal or the interrupt corresponding thereto).

[0032] In certain other embodiments, the at least one output 12 may include other existing (e.g., JEDEC specified) pins instead of, or in addition to, the error-out pin. In yet other configurations, at least one additional (e.g., non-JEDEC specified) pin may be employed. In general, any pin not otherwise active during the initialization mode may be used (e.g., high-order address pins, read/write pins, data pins, etc.).

[0033] The at least one output 12 can further be configured to be operatively coupled to at least one second output 24 of a second memory module 26 in some embodiments, as schematically illustrated in FIGS. 1-3. The second memory module 26 may be generally similar in structure and function to the memory module 10, and may comprise a controller circuit 28 and a notification circuit 30, for example. The second memory module 26 may be generally identical to the first memory module 10, or may have a different memory capacity, form factor, etc., than the first memory module 10. More than two such memory modules may be present in certain embodiments. As described above, the second memory module 26 can be configured to operate in at least two modes comprising an initialization mode during which the second memory module 26 executes at least one initialization sequence, and an operational mode. For example, the initialization and operational modes may be similar to those describe above in relation to the first memory module 10.

[0034] The second memory module 26 can also be configured to drive the at least one second output 24 to a third state indicative of execution of at least one initialization sequence of the second memory module 26 or to a fourth state indicative of completion of the at least one initialization sequence of the second memory module 26. Additionally, in some embodiments, the at least one first output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are operatively coupled together by a bus 32 which is also operatively coupled to at least one input 34 of the system memory controller 14. In other embodiments (not shown), the at least one first output 12 and the at least one second output 24 are not coupled together, and are coupled to two separate inputs of the system memory controller

14.

[0035] FIG. 2 shows an example host computer system 16 including example first and second memory modules 10, 26. As shown, the notification circuits 20, 30 of the first and second memory modules 10, 26 each comprise at least one transistor 36, 38. The at least one transistor 36, 38 can be in an open-drain configuration, as shown, although other configurations are possible. In certain such embodiments, the first state of the at least one first output 12 is a first logic level, the second state of the at least one first output 12 is a high-impedance state, the third state of the at least one second output 24 is the first logic level, and the fourth state of the at least one second output 24 is the high-impedance state. In the illustrated example, while the at least one initialization sequence is in progress, the first and second memory modules 10, 26 drive the gates of the respective transistors 36, 38 high. Thus, the transistors 36, 38 are respectively low impedance while the memory modules 10, 26 are executing each section of the initialization sequence, thereby pulling the first and second outputs 12, 24 low. Thus, the first state and the third state are low logic levels (ground) in the example configuration. Also, because the first and second outputs 12, 24 are coupled together by the bus 32, if the at least one initialization sequence of either one of the first and second memory modules 10, 26 are in progress, the bus 32 will be pulled to a low logic level.

[0036] As each of the two memory modules 10, 26 completes its at least one initialization sequence, it can drive the corresponding at least one first and second outputs 12, 24 respectively to a high impedance state. For example, once the at least one initialization sequence on each of the first and second memory modules 10, 26 is completed, the first and second memory modules 10, 26 can drive the gates of the respective transistors 36, 38 low, resulting in a high-impedance state on the at least one first and second outputs 12, 24 causing the bus 32 to be pulled high by the system memory controller 14. Accordingly, only once the at least one initialization sequence of both the first and second memory modules 10, 26 are complete, the bus 32 will be pulled high by the internal pull-up configuration 40 of the system memory controller 14. The second state and the fourth state are therefore high-impedance values in the example embodiment. Thus, the system memory controller 14 can monitor the value on the bus 32 via the first input 34 to determine when both of the memory modules 10, 26 have completed the at least one initialization sequence. As discussed, in other configurations the at least one first and second outputs 12, 24 may be received on separate inputs of the system memory controller 14, and the

status of the at least one initialization sequence of each memory module 10, 26 may be monitored independently.

[0037] As discussed above, in certain embodiments in which more than one memory module 10, 26 is connected to the system memory controller 14, each memory module 10, 26 or associated controller circuit 18 (e.g., local memory controller) causes the corresponding notification circuit 20, 30 to drive the at least one output 12, 24 to the high impedance state from the low impedance state when it completes the requested or required operation. Thus, in certain such embodiments, the system memory controller 14 (e.g., MCH) can only pull the notifying signal high when all memory modules 10, 26 or associated controller circuits (e.g., local memory controllers) have completed the required or requested operation (e.g., initialization sequence). This configuration allows the system memory controller 14 (e.g., MCH) to work with a non-homogenous memory subsystem. For example, the system memory controller 14 may be able to monitor the progress of multiple memory modules 10, 26 including a mix of DIMMs or other memory modules having differing characteristics, such as DIMM density, rank configurations, DRAM density, speed, DRAM configuration, etc.

[0038] Additionally, the at least one output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are configured to be operatively coupled to at least one interrupt of the system memory controller 14 in certain embodiments. In certain such embodiments, the system memory controller 14 can be responsive to the second state of the first memory module 10 and the fourth state of the second memory module 26 by triggering execution of an interrupt routine by a processor of the system memory controller 14. For example, in the example system of FIG. 2, when the bus 32 is pulled high by the pull-up configuration 40 indicating the second state of the first memory module 10 and the fourth state of the second memory module 26, the system memory controller 14 triggers execution of the interrupt routine.

[0039] In some embodiments, in which the at least one first output 12 and the at least one second output 24 are operatively coupled to separate inputs of the system memory controller 14, the at least one first output 12 and the at least one second output 24 may be operatively coupled to two separate interrupts. For example, the system memory controller 14 may be responsive to the second state of the first memory module 10 by triggering execution of a first interrupt routine

associated with a first interrupt, and may be responsive to the fourth state of the second memory module 26 by triggering execution of a second interrupt routine associated with the second interrupt. In yet other embodiments, the separate inputs of the memory controller 14 are internally operatively coupled to the same interrupt, or are operatively coupled to separate interrupts which trigger the same interrupt routine.

[0040] FIG. 3 shows a host computer system 16 including an example memory module 10 where the notification circuit 20 of the memory module 10 has another example configuration in accordance with certain embodiments described herein. In the example configuration of FIG. 3, the at least one first output 12 is operatively coupled to an error-out pin of the memory module 10, and a multiplexor 42 drives the transistor 36 with either of a task_in_progress signal 44 or an error signal 46 (e.g., parity error signal). In one embodiment, for example, the multiplexor 42 may be configured to drive the transistor 36 with the task_in_progress signal 44 when the memory module 10 is in the initialization mode or is executing the at least one initialization sequence, and with the error signal 46 when the memory module 10 is in the operational mode. Thus, the memory module 10 can be advantageously configured to both perform the standard (e.g., JEDEC-specified) error reporting functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode, as described herein. As shown in FIG. 3, a second memory module 26 including a similar configuration can also be operatively coupled to the host computer system 16. In certain embodiments, the at least one second output 24 of the second memory module 26 can be operatively coupled to the at least one first output 12 by the bus 32, as described above (e.g., with respect to FIG. 2).

[0041] FIG. 4 shows an example method 100 of using the at least one memory module 10 in accordance with certain embodiments described herein. While the description below of the method 100 refers to structure shown in FIGS. 1-3, other structures may also be used in accordance with certain embodiments described herein. At block 102, the method 100 of certain embodiments comprises providing a first memory module 10 comprising at least one first output 12 operatively coupled to a memory controller 14 of a host computer system 16. The first memory module 10 can be configured to operate in at least two modes comprising an initialization mode during which the first memory module 10 executes at least one initialization sequence, and an operational mode. For example, the at least one initialization sequence may

comprise one or more steps of a series of steps associated with an initialization procedure of the host computer system 16.

[0042] At block 104, the method 100 in some embodiments comprises causing the first memory module 10 to enter the initialization mode. At block 106, the method 100 of certain embodiments comprises driving the at least one first output 12 to a first state while the memory module 10 executes the at least one initialization sequence. Upon completion of the at least one initialization sequence, the method of certain embodiments comprises driving the at least one first output 12 to a second state different than the first state. In certain embodiments, the first state is a first logic level and the second state is a high impedance state. Additionally, in certain embodiments, the at least one first output 12 is operatively coupled to at least one interrupt of the memory controller 14 such that driving the at least one output 12 to the second state triggers the memory controller to execute an interrupt routine.

[0043] In certain embodiments, the at least one output 12 is operated in conformance with JEDEC standard when the first memory module 10 is in the operational mode, but is not operated in conformance with the JEDEC standard when the first memory module 10 is in the initialization mode. The at least one first output 12 of certain embodiments include an error-out pin of the first memory module, for example.

[0044] The method 100 can further include providing a second memory module 26 comprising at least one second output 24 operatively coupled to the memory controller 14. The second memory module 26 can be configured to operate in one of at least two modes comprising an initialization mode, during which the second memory module 26 executes at least one initialization sequence, and an operational mode. The method 100 can further include causing the second memory module 26 to enter the initialization mode. In certain embodiments, the method 100 also includes driving the at least one second output 24 of the second memory module 26 to a third state while the second memory module 26 executes the at least one initialization sequence. Upon completion of the at least one initialization sequence, the method 100 can further include driving the at least one second output 24 of the second memory module 26 to a fourth state different from the third state.

[0045] In certain embodiments, the at least one first output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are

operatively coupled together by a bus 32 which is also operatively coupled to at least one input 34 of the memory controller 14. In certain other embodiments, the at least one first output 12 of the first memory module 10 is operatively coupled to a first input 34 of the memory controller 14 and the at least one second output 24 of the second memory module 26 is operatively coupled to a second input (not shown) of the memory controller 14.

[0046] FIG. 5 shows another example method 200 of using at least one memory module 10 in accordance with certain embodiments described herein. At block 202, the method 200 may include providing a memory module 10 comprising at least one output 12 operatively coupled to a memory controller 14 of a host computer system 16. The memory module 10 may be configured to operate in at least two modes comprising an initialization mode, during which the memory module 10 executes at least one initialization sequence, and an operational mode.

[0047] The method 200 can further include causing the memory module 10 to enter the initialization mode at block 204. At block 206, the method 200 can include receiving a notification signal from the at least one output 12 of the memory module 10. The notification signal may indicate that the memory module 10 has completed the initialization sequence, for example. In certain embodiments, the method 200 further comprises executing an interrupt routine by the memory controller 14 in response to the notification signal.

TERMINOLOGY/ALTERNATIVE EMBODIMENTS

[0048] Embodiments have been described in connection with the accompanying drawings. However, it should be understood that the figures are not drawn to scale. Distances, angles, etc. are merely illustrative and do not necessarily bear an exact relationship to actual dimensions and layout of the devices illustrated. In addition, the foregoing embodiments have been described at a level of detail to allow one of ordinary skill in the art to make and use the devices, systems, etc. described herein. A wide variety of variation is possible. Components, elements, and/or steps can be altered, added, removed, or rearranged. While certain embodiments have been explicitly described, other embodiments will become apparent to those of ordinary skill in the art based on this disclosure.

[0049] Conditional language used herein, such as, among others, “can,” “could,” “might,” “may,” “e.g.,” and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments

include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment.

[0050] Depending on the embodiment, certain acts, events, or functions of any of the methods described herein can be performed in a different sequence, can be added, merged, or left out all together (e.g., not all described acts or events are necessary for the practice of the method). Moreover, in certain embodiments, acts or events can be performed concurrently, e.g., through multi-threaded processing, interrupt processing, or multiple processors or processor cores, rather than sequentially.

[0051] The various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein can be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. The described functionality can be implemented in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the disclosure.

[0052] The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein can be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor can be a microprocessor, but in the alternative, the processor can be any conventional processor, controller, microcontroller, or state machine. A processor can also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a

plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0053] The blocks of the methods and algorithms described in connection with the embodiments disclosed herein can be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module can reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, a hard disk, a removable disk, a CD-ROM, or any other form of computer-readable storage medium known in the art. An exemplary storage medium is coupled to a processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium can be integral to the processor. The processor and the storage medium can reside in an ASIC. The ASIC can reside in a user terminal. In the alternative, the processor and the storage medium can reside as discrete components in a user terminal.

[0054] Certain embodiments described herein are compatible with a memory system including memory devices with various attributes (see, e.g., FIGS. 2 and 3). For example, the memory system of certain embodiments may include various data slice sizes (e.g., two, four, eight, or 16 bit data slices) and corresponding memories (e.g., memories having two, four, eight, or 16 bit data widths).

[0055] Although certain embodiments and examples are discussed above, it is understood that the inventive subject matter extends beyond the specifically disclosed embodiments to other alternative embodiments and/or uses of the invention and obvious modifications and equivalents thereof. It is intended that the scope of the inventions disclosed herein should not be limited by the particular disclosed embodiments. Thus, for example, in any method or process disclosed herein, the acts or operations making up the method/process may be performed in any suitable sequence and are not necessarily limited to any particular disclosed sequence.

[0056] Various aspects and advantages of the embodiments have been described where appropriate. It is to be understood that not necessarily all such aspects or advantages may be achieved in accordance with any particular embodiment. Thus, for example, it should be recognized that the various embodiments may be carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other aspects or advantages as may be taught or suggested herein.

WHAT IS CLAIMED IS:

1. A method performed by a memory module coupled to a memory controller of a host computer system via an interface, the interface including data, address and control signal pins and an output pin in addition to the data, address and control signal pins, the method comprising:
 - receiving a first command from the memory controller via the address and control signal pins;
 - entering a first mode in response to the first command, wherein the memory module in the first mode responds to at least one initialization sequence;
 - sending a first output signal via the output pin to indicate a status of the at least one initialization sequence to the memory controller;
 - entering a second mode in which the memory module performs memory operations including memory read/write operations according to an industry standard, wherein, during the read/write operations, the memory module communicates data with the memory controller via the data signal pins in response to second memory commands received via the address and control signal pins; and
 - outputting a second output signal related to the read/write operations via the output pin.
2. The method of claim 1, wherein the signal indicating a status of the at least one initialization sequence causes the memory controller to execute an interrupt routine.
3. The method of claim 1, further comprising receiving a second command from the memory controller, the second command causing the memory module to exit the first mode.
4. The method of claim 1, wherein the second output signal indicates an error having occurred in the memory module.
5. The method of claim 1, wherein the memory module comprises a transistor having a drain terminal coupled to the output pin, and wherein the first output signal is an open-drain signal.
6. The method of claim 5, wherein sending the first output signal comprises driving the output pin to a high impedance state, and wherein the output pin is kept at a low-impedance state before the memory module completes the internal procedure in the first mode.

7. A method performed by a memory module coupled to a memory controller of a host computer system via an interface, the interface including data, address and control signal pins and an output pin in addition to the data, address and control signal pins, the method comprising:
- receiving a first command from the memory controller via the address and control signal pins;
 - entering a first mode in response to the first command in which the memory module performs an internal procedure;
 - sending a first output signal via the output pin to indicate a status of the internal procedure to the memory controller;
 - entering a second mode in which the memory module performs memory operations including memory read/write operations according to an industry standard, wherein, during the read/write operations, the memory module communicates data with the memory controller via the data signal pins in response to second memory commands received via the address and control signal pins; and
 - outputting a second output signal related to the standard operations via the output pin.
8. The method of claim 7, wherein the signal indicating a status of the internal procedure causes the memory controller to execute an interrupt routine.
9. The method of claim 7, further comprising receiving a second command from the memory controller, the second command causing the memory module to exit the first mode.
10. The method of claim 7, wherein the second output signal indicates an error having occurred in the memory module.
11. The method of claim 7, wherein the memory module comprises a transistor having a drain terminal coupled to the output pin, and wherein the first output signal is an open-drain signal.
12. The method of claim 11, wherein sending the first output signal comprises driving the output pin to a high impedance state, and wherein the output pin is kept at a low-impedance state before the memory module completes the internal procedure in the first mode..

13. The method of claim 7, wherein the first output signal indicates completion of the internal procedure.
14. The method of claim 7, wherein the internal procedure includes at least one initialization sequence.
15. A memory module operable in a first mode and in a second mode, the memory module operating according to an industry standard in the second mode by performing standard operations including memory read/write operations in response to address and control signals from a memory controller of a host computer system, the memory module comprising:
- a standard interface including data, address and control signal pins and an output pin in addition to the data, address and control signal pins;
 - a controller circuit to receive a first command from the memory controller, the first command causing the memory module to enter the first mode in which the memory module responds to at least one initialization sequence; and
 - a notification circuit to output a notification signal indicating a status of the initialization sequence to the memory controller via the output pin.
16. The memory module of claim 15, wherein the signal indicating a status of the initialization sequence causes the memory controller to execute an interrupt routine.
17. The memory module of claim 15, wherein the output pin is used to output an error reporting signal during the second mode that indicates an error having occurred in the memory module during the read/write operations.
18. The memory module of claim 15, wherein the output pin is coupled to an interrupt of the memory controller.
19. The memory module of claim 15, wherein the notification circuit comprises a transistor having a drain terminal coupled to the output pin, and wherein the notification signal is an open-drain signal.
20. The memory module of claim 16, wherein the notification circuit comprises a first input corresponding to the first mode, a second input corresponding to the second mode, and a

multiplexor selecting between the first input and the second input to couple to a gate of the transistor based on whether the memory module is in the first mode or the second mode.

SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

ABSTRACT OF THE DISCLOSURE

According to certain aspects, a memory module is coupled to a memory controller of a host computer system via an interface. The interface includes data, address and control signal pins and an output pin in addition to the data, address and control signal pins. The memory module receives a first command from the memory controller via the address and control signal pins, and enters a first mode in response to the first command. The memory module in the first mode responds to at least one initialization sequence, and sends a first output signal via the output pin to indicate a status of the at least one initialization sequence to the memory controller. The memory module enters a second mode in which the memory module performs memory operations including memory read/write operations according to an industry standard. During the read/write operations, the memory module communicates data with the memory controller via the data signal pins in response to second memory commands received via the address and control signal pins. The memory module may output a second output signal related to the read/write operations via the output pin.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		
First Named Inventor/Applicant Name:		Hyun Lee		
Filer:		Jamie Jie Zheng		
Attorney Docket Number:		NETL.062C2		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

Electronic Acknowledgement Receipt	
EFS ID:	25368212
Application Number:	15088115
International Application Number:	
Confirmation Number:	7163
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062C2
Receipt Date:	01-APR-2016
Filing Date:	
Time Stamp:	00:50:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1600
RAM confirmation Number	7304
Deposit Account	
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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Drawings-only black and white line drawings	2016-03-31_Drawings_NETL062C2.pdf	315345 2c98f39e9915747c0e51480c91f3023d4534c727	no	3
Warnings:					
Information:					
2	Oath or Declaration filed	2013-10-09_Declaration_NETL062C1.pdf	286314 ac827f939d7ed2eef5ec73035d1f3c9f0f8509d	no	2
Warnings:					
Information:					
3	Power of Attorney	2016-03-31_POA_Transmittal_NETL062C2.pdf	195891 f3a39f72def1d8d04c85d0d54828a1674b1099ce	no	3
Warnings:					
Information:					
4	Power of Attorney	AIA_General_POA_Netlist.pdf	133545 f8258889ee9edc63b1cc17705b3158faed49e9e	no	1
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
5	Application Data Sheet	2016-03-31_ApplicationDataSheet_NETL062C2.pdf	1437421 82ab8d1bc5c7d1bfff3223841a577bed3e6bb326e	no	6
Warnings:					
Information:					
6		2016-03-31_Spec_NETL062C2.pdf	21752195 8f27135247cca256ba56124c4b3f62c2dd2a9432	yes	24
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	19	
	Claims		20	23	

	Abstract	24	24				
Warnings:							
Information:							
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Warnings:							
Information:							
Total Files Size (in bytes):		24155743					
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.							

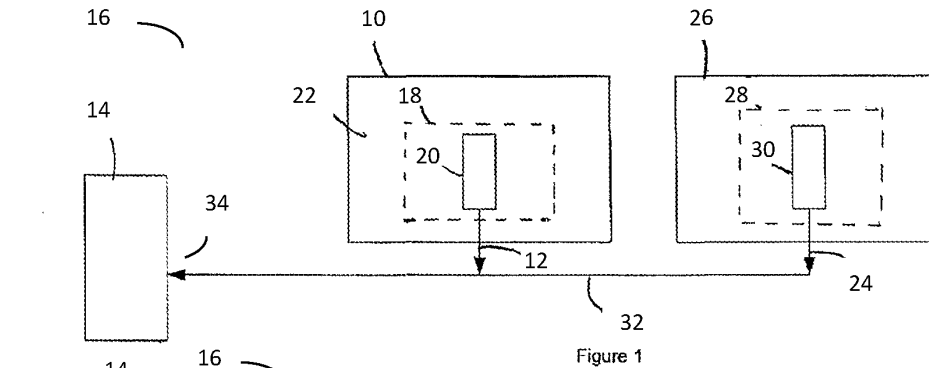


Figure 1

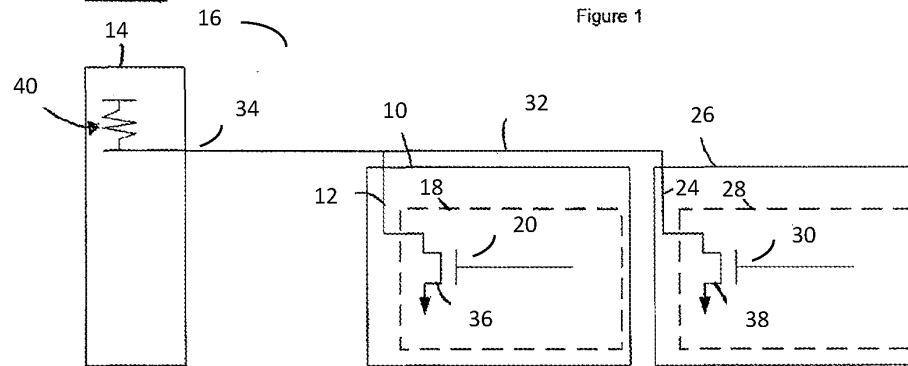


Figure 2

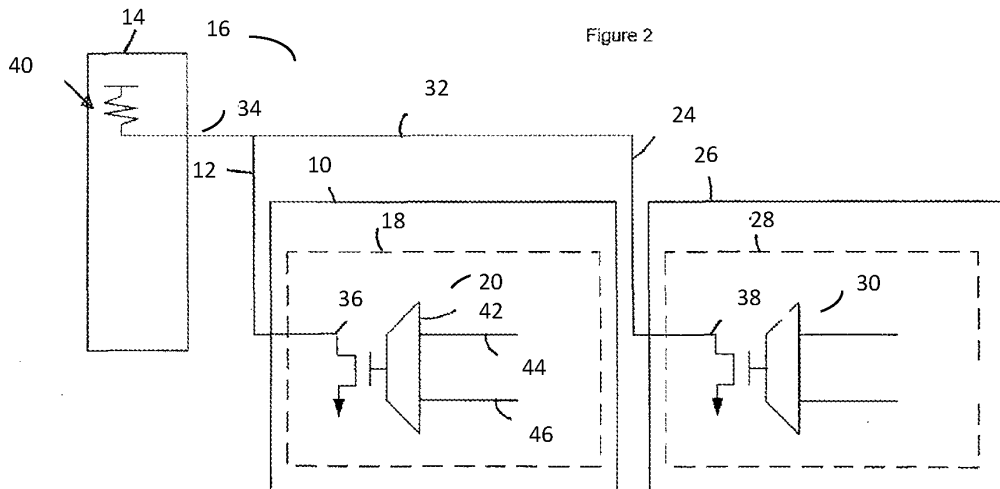


Figure 3

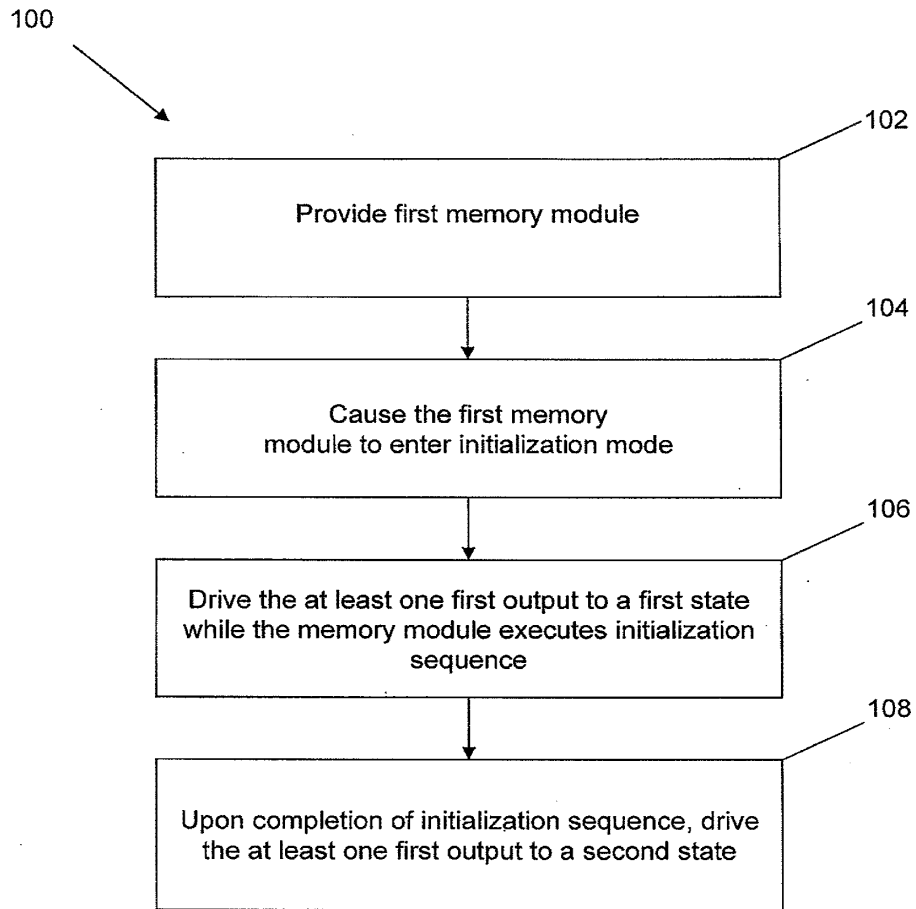


Figure 4

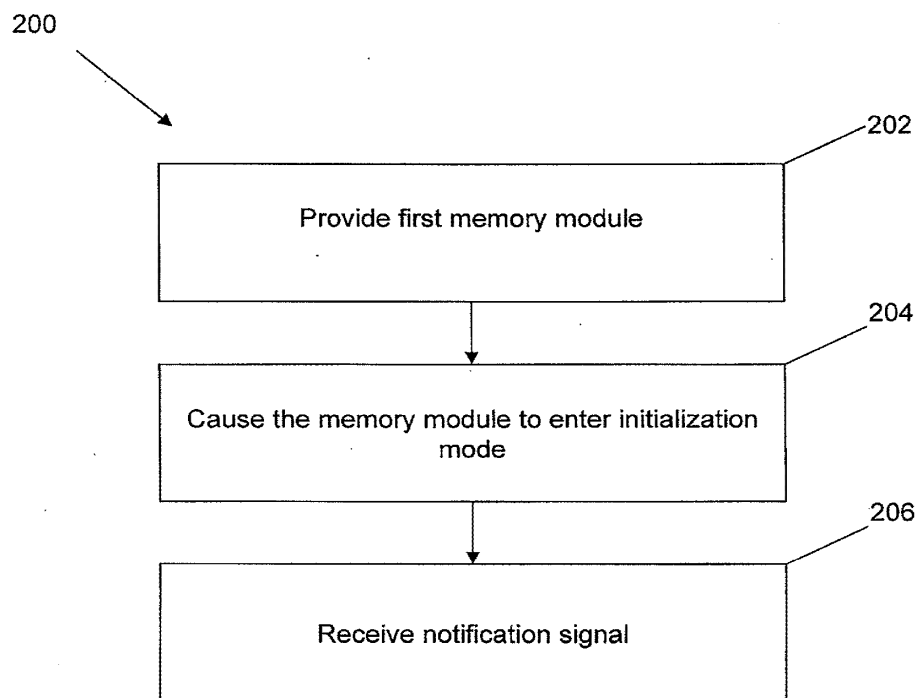


Figure 5

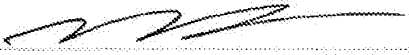
COMBINED DECLARATION AND ASSIGNMENT FOR UTILITY OR DESIGN APPLICATION	
Title of Invention	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
DECLARATION	
As a below named inventor, I hereby declare that:	
This declaration is directed to:	
☐ The attached application, or	
☒ United States application or PCT international application number 13/942,721 filed on July 16, 2013	
The above-identified application was made or authorized to be made by me.	
I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.	
I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.	
Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."	
ASSIGNMENT	
In consideration of the sum of One Dollar (\$1.00) and other good and valuable consideration paid, I hereby sell and assign to	
Netlist, Inc. (Name of Assignee)	
of 51 Discovery, Suite #150, Irvine, CA 92618 (Address of Assignee)	
(hereinafter designated as the Assignee) my entire right, title and interest for the United States as defined in 35 USC 100, for any invention set forth in the above-identified application.	
I agree to execute all papers necessary in connection with this application for patent in the USPTO for the invention, and any continuation, divisional or reissue applications thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient.	
I agree to execute all papers necessary in connection with any post-grant proceeding which may occur in connection with this application or continuation, divisional or reissue thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such post-grant proceeding.	

I agree to execute all papers and documents and perform any act which may be necessary in connection with claims or provisions of the International Convention for Protection of Industrial Property or similar agreements.

I agree to perform all affirmative acts which may be necessary to obtain a grant of a valid United States patent to the Assignee.

I hereby authorize and request the USPTO to issue any and all Letters Patents of the United States resulting from the application or any continuation, divisional or reissue applications thereof to the Assignee, as Assignee of my entire interest, and covenant that I have not executed, and will not execute, any agreement in conflict herewith.

First Inventor (Legal Name): Hyun Lee

Signature: 

Date: 10/9/2013

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 15/088,115				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280			
SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A			N/A	600			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720			
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 = *			OR	x 80 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 420 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	1600			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
TOTAL ADD'L FEE								OR	TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
TOTAL ADD'L FEE								OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
15/088,115	04/01/2016	2139	1600	NETL.062C2	20	3

CONFIRMATION NO. 7163

FILING RECEIPT



0000000082284236

79141

Jamie J. Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

Date Mailed: 04/19/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Hyun Lee, Ladera Ranch, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 13/942,721 07/16/2013 PAT 9311116
which is a CON of 12/815,339 06/14/2010 PAT 8489837
which claims benefit of 61/186,799 06/12/2009

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 04/18/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/088,115**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No
Title

SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/088,115	04/01/2016	Hyun Lee	NEIL.062C2	7163
79141	7590	05/20/2016	EXAMINER	
Jamie J. Zheng, Ph.D Esq. P.O. Box 60573 Palo Alto, CA 94306			CHERY, MARDOCHEE	
			ART UNIT	PAPER NUMBER
			2133	
			NOTIFICATION DATE	DELIVERY MODE
			05/20/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jz@jzpatent.com
eofficeaction@appcoll.com
infohub.j@gmail.com

Office Action Summary	Application No. 15/088,115	Applicant(s) LEE, HYUN	
	Examiner Mardochee CHERY	Art Unit 2133	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 4/1/16.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-20 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-20 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☒ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 4/1/16 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 4) ☐ Other: ____.

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to

be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit <http://www.uspto.gov/forms/>. The filing date of the application will determine what form should be used. **A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to <http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp>.**

4. Claims 1-20 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 9311116 and 1-18 of **U.S. Patent #8489837**. Although the claims at issue are not identical, they are not patentably distinct from each other because claims 1-20 of U.S. Patent No. 9311116 and 1-18 of **U.S. Patent #8489837** anticipate and/or make obvious claims 1-20 of the current application.

5. “A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). “ ELI LILLY AND

COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim Rejections - 35 USC § 103

6. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-21 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Tanguay et al. (US 2010/0042778) and Roohparvar (2003/0115427).

As per claim 1, Tanguay discloses a method performed by a memory module coupled to a memory controller of a host computer system via an interface, the interface including data, address and control signal pins and an output pin in addition to the data, address and control signal pins [Fig. 2: DDR2 SDRAM array 260 connected to SDRAM controller 116 through connectors 140 pins BA [1:0], ADDR [13:0], RAS#, CAS#, WE#, etc...], the method comprising: receiving a first command from the memory controller via the address and control signal pins [Fig. 2: first command is sent to array 260 ADDR 14 and RAS#, CAS# 4 pins]; entering a first mode in response to the first command, wherein the memory module in the first mode responds to at least one initialization sequence [¶0026, 0028: before accessing the memory device, initializing the memory device]; sending a first output signal via the output pin to indicate a status of the at least one initialization sequence to the memory controller [¶0024, 0025: perform initialization procedure appropriate for the type of memory and initializing the mode registers]; entering a second mode in which the memory module performs memory operations including memory read/write operations according to an industry standard, wherein, during the read/write operations, the memory module communicates data with the memory controller via the data signal pins in response to second memory commands received via the address and control signal pins [¶0016, 0024: initializing the DIMM as specified by the JEDEC DDR standard and then access the DIMM]; and outputting a second output signal related to the read/write operations via the output pin [¶0016, 0025: accessing the DIMM by performing read and write commands].

Tanguay does explicitly detail what is the status of the initialization sequence. Roohparvar, however, at paragraph ¶0030 discloses a notification circuit configured to drive at least one output while the memory module is in the initialization mode to provide at least one notification signal to the memory controller indicating at least one status of the at least initialization sequence.

At the time of invention, it would have been obvious to one of ordinary skill in the art, to have circuitry determining the status of a notification signal in order to provide a memory that is able to initialize itself without requiring the memory controller to wait unnecessarily for the initialization to be performed (Roohparvar @ ¶0028-0030).

As per claim 2, Roohparvar discloses the method of claim 1, wherein the signal indicating a status of the at least one initialization sequence causes the memory controller to execute an interrupt routine [¶0030].

As per claim 3, Roohparvar discloses the method of claim 1, further comprising receiving a second command from the memory controller, the second command causing the memory module to exit the first mode [¶0012, 24, 27].

As per claim 4, Roohparvar discloses the method of claim 1, wherein the second output signal indicates an error having occurred in the memory module [¶0031].

As per claim 5, the cited art discloses the method of claim 1, wherein the memory module comprises a transistor having a drain terminal coupled to the output pin, and wherein the first output signal is an open-drain signal [Roohparvar @ ¶0027-28].

As per claim 6, Roohparvar discloses the method of claim 5, wherein sending the first output signal comprises driving the output pin to a high impedance state, and wherein the output pin is kept at a low-impedance state before the memory module completes the internal procedure in the first mode [¶0023-0024].

As per claims 7-20, the rationale in the rejection of claims 1-6 is herein incorporated.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee CHERY whose telephone number is (571)272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jared Ian Rutz can be reached on (571)272-5535. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

May 16, 2016

/Mardochee CHERY/
Primary Examiner, Art Unit 2133

Notice of References Cited	Application/Control No. 15/088,115	Applicant(s)/Patent Under Reexamination LEE, HYUN	
	Examiner Mardochee CHERY	Art Unit 2133	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2010/0042778 A1	02-2010	Tanguay; Kevin B.	G06F13/1694	711/105
*	B	US-2003/0115427 A1	06-2003	Roohparvar, Frankie F.	G11C7/02	711/154
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. Patent and Trademark Office
PTO-892 (Rev. 01-2001)
20160516

Notice of References Cited

Part of Paper No.

Samsung Electronics Co., Ltd.
Ex. 1005, p. 58

<i>Index of Claims</i>	Application/Control No.	Applicant(s)/Patent Under Reexamination
	Examiner	Art Unit

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original								

Search Notes 	Application/Control No. 15088115	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
711	116	5/16/16	MC
713	1	5/16/16	MC

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Search	5/16/16	MC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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Doc Code: DIST.E.FILE Document Description: Electronic Terminal Disclaimer - Filed		PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce	
Electronic Petition Request	TERMINAL DISCLAIMER TO OBTAIN A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT		
Application Number	15088115		
Filing Date	01-Apr-2016		
First Named Inventor	Hyun Lee		
Attorney Docket Number	NETL.062C2		
Title of Invention	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		
☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action ☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.			
Owner		Percent Interest	
Netlist, Inc.		100%	
The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s) 8489837 9311116 as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns. In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later: - expires for failure to pay a maintenance fee; - is held unenforceable; - is found invalid by a court of competent jurisdiction; - is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321; - has all claims canceled by a reexamination certificate; - is reissued; or - is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.			

- ☒ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.
- ☐ I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

- ☐ Small Entity
- ☐ Micro Entity
- ☒ Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

- ☒ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application
- Registration Number 51167
- ☐ A sole inventor
- ☐ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application
- ☐ A joint inventor; all of whom are signing this request

Signature	/Jamie J. Zheng/
Name	Jamie J. Zheng

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal				
Application Number:		15088115		
Filing Date:		01-Apr-2016		
Title of Invention:		SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		
First Named Inventor/Applicant Name:		Hyun Lee		
Filer:		Jamie Jie Zheng		
Attorney Docket Number:		NETL.062C2		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Statutory or Terminal Disclaimer	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				160

Doc Code: DISQ.E.FILE

Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 15088115

Filing Date: 01-Apr-2016

Applicant/Patent under Reexamination: Lee et al.

Electronic Terminal Disclaimer filed on August 10, 2016

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt	
EFS ID:	26609660
Application Number:	15088115
International Application Number:	
Confirmation Number:	7163
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062C2
Receipt Date:	10-AUG-2016
Filing Date:	01-APR-2016
Time Stamp:	23:50:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$160
RAM confirmation Number	6770
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Electronic Terminal Disclaimer-Filed	eTerminal-Disclaimer.pdf	33614	no	2
			9f8f6db6301ae44aa2a85fdbbe8bd46a88dc2c916		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30378	no	2
			53dd4eacb1d04af2925449207d1dd85017c7b70f		
Warnings:					
Information:					
Total Files Size (in bytes):			63992		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Netlist, Inc.
App. No. : 15/088,115
Filed : April 1, 2016
For : SYSTEMS AND METHODS
FOR HANDSHAKING WITH A
MEMORY MODULE
Examiner : CHERY, MARDOCHEE
Art Unit : 2133
Conf. No. : 7163
Docket No. : NETL.062C2

CERTIFICATE OF EFS WEB
TRANSMISSION

I hereby certify that this correspondence and any other attachment noted on the Automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web Server on:

August 10, 2016

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

RESPONSE TO NON-FINAL OFFICE ACTION DATED MAY 20, 2016

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Non-Final Office Action dated May 20, 2016 for the above-identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

AMENDMENTS to the SPECIFICATION begin on Page 2 of this paper.

AMENDMENTS to the CLAIMS begin on Page 3 of this paper.

REMARKS begin on Page 8 of this paper.

IN THE SPECIFICATION:

Please replace the Title with the following:

MEMORY MODULE SYSTEMS AND METHODS FOR HANDSHAKING WITH A
MEMORY CONTROLLER MODULE

Please replace Paragraph [0001] with the following:

[0001] This application is a continuation of U.S. App. No. 13/942,721, filed July 16, 2013, ~~to be issued as~~ now U.S. Pat. No. 9,311,116 ~~on April 12, 2016~~, which is a continuation of U.S. App. No. 12/815,339, filed June 14, 2010, now U.S. Pat. No. 8,489,837, which claims the benefit of priority from U.S. Provisional App. No. 61/186,799, filed June 12, 2009, each of which is incorporated in its entirety by reference herein.

IN THE CLAIMS:

Claims 1-20. (Cancelled)

21. (New) A memory module, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of a host system, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

dynamic random access memory elements configured to communicate data signals with the memory controller via the first edge connections;

a module controller coupled to the dynamic random access memory elements, wherein the module controller is configured to receive from the memory controller via the second edge connections address and command signals associated with one or more memory read, write, pre-charge, or refresh operations and to control the memory elements in accordance with the address and command signals, the module controller having an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations;

wherein the module controller is further configured to process one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation, and wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection.

22. (New) The memory module of claim 21, wherein the module controller comprises one or more integrated circuit.

23. (New) The memory module of claim 21, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.

24. (New) The memory module of claim 23, wherein the notification circuit drives the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
25. (New) The memory module of claim 24, wherein the notification circuit drives the signal indicating the parity error by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
26. (New) The memory module of claim 24, wherein the notification circuit drives the notification signal using one or more OR logic elements.
27. (New) The memory module of claim 21, wherein the one or more training sequences are initiated by the memory controller.
28. (New) The memory module of claim 21, wherein the module controller processes the one or more training sequences in response to a command received from the memory controller.
29. (New) A method performed by a memory module operating with a memory controller of the host system, the memory module including dynamic random access memory elements on a printed circuit board, the printed circuit board having edge connections that fit into a corresponding slot of a host system, the edge connections including first edge connections via which the dynamic random access memory devices communicate data with the memory controller, second edge connections via which the memory module receives address and command signals from the memory controller, and an error edge connection in addition to the first edge connections and the second edge connections, the method comprising:
- receiving from the memory controller address and command signals associated with one or more memory read, write, pre-charge, or refresh operations;
 - controlling the dynamic random access memory elements to perform the one or more memory read, write, pre-charge, or refresh operations in accordance with the address and command signals;

outputting to the memory controller via an open-drain output coupled to the error edge connection a signal indicating a parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations;

processing one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation; and

driving a notification signal associated with the one or more training sequences to the memory controller via the open drain output and the error edge connection.

30. (New) The method of claim 29, wherein driving the notification signal comprises driving a gate of each of one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground, the one or more transistors each having an open drain coupled to the open drain output.

31. (New) The method of claim 30, wherein driving the signal indicating the parity error comprises driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground.

32. (New) The method of claim 30, wherein driving the notification signal comprises using one or more OR logic elements.

33. (New) The method of claim 29, wherein the one or more training sequences are initiated by the memory controller.

34. (New) The method of claim 29, wherein the one or more training sequences are processed in response to a command received from the memory controller of the host system via the second edge connections.

35. (New) A memory module, comprising:
a printed circuit board having edge connections that fit into a corresponding slot of a host system, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;
dynamic random access memory elements configured to communicate data signals with the memory controller via the first edge connections; and

a module controller coupled to the dynamic random access memory elements, wherein the module controller is configured to receive from the memory controller via the second edge connections address and command signals associated with one or more memory read, write, pre-charge, or refresh operations and to control the memory elements in accordance with the address and command signals, the module controller having an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations;

wherein the module controller is further configured to process one or more training sequences while the memory module is not performing any memory read, write, pre-charge, or refresh operation, and wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection.

36. (New) The memory module of claim 35, wherein the module controller comprises one or more integrated circuit.

37. (New) The memory module of claim 35, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.

38. (New) The memory module of claim 37, wherein the notification circuit generates the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.

39. (New) The memory module of claim 38, wherein the notification circuit drives the signal indicating the parity error by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.

40. (New) The memory module of claim 38, wherein the notification circuit drives the notification signal using one or more OR logic elements.

41. (New) The memory module of claim 35, wherein the one or more training sequences are initiated by the memory controller.
42. (New) The memory module of claim 35, wherein the module controller processes the one or more training sequences in response to a command received from the memory controller of the host system via the second edge connections.

REMARKS

This amendment responds to the Non-Final Office Action dated May 20, 2016. In the Office Action, the Examiner:

- rejected claims 1-20 on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 9311116 and claims 1-18 of U.S. Patent No. 8489837; and
- rejected claims 1-20 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Tanguay US 2010/0042778 (hereafter “Tanguay”) in view of Roohparvar US 20030115427 (hereafter “Roohparvar”).

Claims 1-20 are cancelled without prejudice. New claims 21-42 are presented. Support for the new claims is presented below. Thus, no new matter is added.

Applicant files herewith a terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) to overcome any nonstatutory double patenting rejections over U.S. Patent No. 9311116 and U.S. Patent No. 8489837.

New claim 21 recites a memory module, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of a host system, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections (See for example Paragraphs [0019] and [0029] of the Specification for support);

dynamic random access memory elements configured to communicate data signals with the memory controller via the first edge connections (See for example Paragraphs [0019] and [0020] of the Specification for support);

a module controller coupled to the dynamic random access memory elements, wherein the module controller is configured to receive from the memory controller via the second edge connections address and command signals associated with one or more memory read, write, pre-charge, or refresh operations and to control the memory elements in accordance with the address and command signals (See for example Paragraphs [0021] and [0024] of the Specification for support), the module controller having an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error having occurred during the one

or more memory read, write, pre-charge, or refresh operations (See for example FIGS. 2-3, and Paragraph [0040] and the last five lines of Paragraph [0029] of the Specification for support);

wherein the module controller is further configured to process one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation (See for example Paragraphs [0022], [0024], and [0041] of the Specification for support), and wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection (See for example FIGS. 1-3, and Paragraphs [0025] and [0029] and the last four lines of Paragraph [0017] of the Specification for support).

Thus, new claim 21 requires, among other things, a module controller that receives address and command signals associated with one or more memory read, write, pre-charge, or refresh operations and that controls dynamic random access memory elements in accordance with the address and command signals. New claim 21 further requires such a module controller to have an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations. New claim 21 further requires that the module controller be further configured to drive a notification signal associated with one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation to the memory controller via the open drain output of the module controller. These features are not found in Tanguay and Roohparvar, either individually or in combination.

As shown in FIGS. 2-3 of Tanguay, Tanguay's bus switch 284, the only component in Tanguay's memory module that receives address and command signals from the DDR1 SDRAM controller 116, does not output any signals to the DDR1 SDRAM controller 116. As also shown in FIG. 2 in Tanguay and discussed in paragraph [0024] and [0025] of Tanguay, which the Examiner cites in the Office Action, the only output signals Tanguay's memory module 250 sends to its memory controller 116 are the DQ and DQS signals, which are data and data strobe signals communicated between the DDR1 SDRAM Controller 116 and the DDR2 SDRAMs 260. Thus, Tanguay does not disclose or teach any signal output by a module controller to the memory controller, as required by new claim 21, let alone any signal output from a module controller via an

open drain output to indicate a parity error having occurred in the memory module during a read, write, refresh or precharge operation, or a notification signal associated with one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation output from the module controller via the same open drain output, as also required by new claim 21.

Roohparvar does not make up for the deficiencies of Tanguay. First of all, Roohparvar describes a synchronous memory device 100, which is different from a memory module and which does not comprise a printed circuit board having edge connections that fit into a corresponding slot of a host system, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections, and dynamic random access memory elements configured to communicate data signals with the memory controller via the first edge connections.

Secondly, Roohparvar does not disclose or teach the module controller recited in claim 1. As shown in FIG. 1 of Roohparvar, the functional block in Roohparvar's memory device 100 that receives address and command signals and that controls the memory array 104 via the state machine 132 is the Command Execution Logic. Yet, the Command Execution Logic does not output any signal indicating a parity error having occurred in the memory device 100 during a read, write, refresh or precharge operation, as required by new claim 21. The Command Execution Logic also does not output a notification signal associated with one or more training sequences to the memory controller, as also required by new claim 21.

The Examiner cites paragraph [0030] in Roohparvar in the Office Action, where the memory 104 in Roohparvar's memory device 100 is described as being "designed to notify the external processor 200 when initialization has been completed." But, the memory 104 is part of an array of non-volatile flash memory cells 102 (*See Roohparvar, paragraph [0020], lines 2-6*). The memory 104 is thus not a module controller that receives address and command signals from a memory controller via a set of edge connections and that controls dynamic random access memory elements accordingly, as

required by new claim 21. The memory 104 also does not include an open drain output by which it outputs a signal indicating a parity error having occurred in the memory module during a read, write, refresh or precharge operation, or a notification signal associated with one or more training sequences, as also required by new claim 21.

Instead, Roohparvar describes providing “an output signal on its DQ lines 143 that indicates the completion of initialization for the external processor 200 to read” (*See Roohparvar, paragraph [0030] lines 5-8*). This is in direct contradiction to new claim 21, which requires the notification signal be output via an error edge connection other than any of the first edge connections (via which the dynamic random access memory elements communicate data signals with the memory controller) or the second edge connections (via which the module controller receives from the memory controller address and command signals associated with one or more memory read, write, pre-charge, or refresh operations).

Therefore, new claim 21 is patentable over Tanguay in view of Roohparvar.

New claims 22-28 depend from new claim 21. Therefore, new claims 22-28 are patentable for at least the same reasons new claim 21 is patentable.

Support for new claim 22 can be found at least in the last two lines of Paragraph [0021] of the Specification.

Support for new claim 23 can be found at least in Paragraph [0035] of the Specification with reference to FIG. 2 of the Drawings.

Support for new claim 24 can be found at least in Paragraph [0035], lines 8-16 and Paragraph [0036] of the Specification.

Support for new claim 25 can be found at least in Paragraph [0040] of the Specification.

Support for new claim 26 can be found at least in Paragraph [0025] of the Specification.

Support for new claim 27 can be found at least in lines 3-6 of Paragraph [0022] of the Specification.

Support for new claim 28 can be found at least in lines 7-10 of Paragraph [0022] of the Specification.

New claim 29 recites a method performed by a memory module operating with a memory controller of the host system, the memory module including dynamic random access memory elements on a printed circuit board (See for example Paragraphs [0019] and [0020] of the Specification for support), the printed circuit board having edge connections that fit into a corresponding slot of a host system, the edge connections including first edge connections via which the dynamic random access memory devices communicate data with the memory controller, second edge connections via which the memory module receives address and command signals from the memory controller, and an error edge connection in addition to the first edge connections and the second edge connections (See for example Paragraphs [0019] and [0029] of the Specification for support), the method comprising:

- receiving from the memory controller address and command signals associated with one or more memory read, write, pre-charge, or refresh operations (See for example Paragraphs [0021] and [0024] of the Specification for support);

- controlling the dynamic random access memory elements to perform the one or more memory read, write, pre-charge, or refresh operations in accordance with the address and command signals (See for example Paragraphs [0021] and [0024] of the Specification for support);
- and

- outputting to the memory controller via an open-drain output coupled to the error edge connection a signal indicating a parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations (See for example Paragraph [0040] and the last five lines of Paragraph [0029] of the Specification for support);

- processing one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation (See for example Paragraphs [0022], [0024], and [0041] of the Specification for support);
- and

- driving a notification signal associated with the one or more training sequences to the memory controller via the open drain output and the error edge connection (See for example Paragraphs [0025] and [0029]

and the last four lines of Paragraph [0017] of the Specification for support).

New claim 29 is patentable over Tanguay in view of Roohparvar because, as discussed above, neither Tanguay nor Roohparvar discloses or teaches, among other things, “outputting to the memory controller via an open-drain output coupled to the error edge connection a signal indicating a parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations” and “driving a notification signal associated with the one or more training sequences (that are unrelated to any memory read, write, pre-charge, or refresh operation) to the memory controller via the open drain output coupled to the error edge connection.”

New claims 30-34 depend from new claim 29. Therefore, new claims 30-34 are patentable for at least the same reasons new claim 29 is patentable.

Support for new claim 30 can be found at least in Paragraphs [0035] and [0036] of the Specification with reference to FIG. 2 of the Drawings.

Support for new claim 31 can be found at least in Paragraph [0040] of the Specification.

Support for new claim 32 can be found at least in Paragraph [0025] of the Specification.

Support for new claim 33 can be found at least in lines 3-6 of Paragraph [0022] of the Specification.

Support for new claim 34 can be found at least in lines 7-10 of Paragraph [0022] of the Specification.

The above arguments related to new claims 21-28 apply to new claims 35-42, respectively. Therefore new claims 35-42 are also patentable.

Applicant submits that claims 21-42 are in condition for allowance and respectfully requests such action. The Examiner is invited to call the undersigned at (650) 521-4828 to discuss any remaining issues.

Respectfully submitted,

Date: August 10, 2016

/Jamie J. Zheng/

51167

Jamie J. Zheng

(Reg. No.)

Customer No. 79141

INFORMATION DISCLOSURE STATEMENT

Applicant	: Netlist, Inc.
App. No.	: 15/088,115
Filed	: April 1, 2016
For	: SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
Examiner	: CHERY, MARDOCHEE
Art Unit	: 2133
Conf. No.	: 7163
Docket No.	: NETL.062C2

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 24 references. Copies of foreign documents and/or their translation and non-patent literature are submitted herewith.

The applicant would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

Application No.: 15/088,115
Filing Date: April 1, 2016

The Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to
Deposit Account No. 50-5963.

Respectfully submitted,

Dated: August 10, 2016

/Jamie J. Zheng/

Jamie J. Zheng
Customer No. 79141
(650) 521-4828

51167
(Reg. No.)

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	15/088,115
				Filing Date	April 1, 2016
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	CHERY, MARDOCHEE
Sheet	1	of	2	Attorney Docket Number	NETL.062C2

US PATENT DOCUMENTS					
Examiner Initials *	Cite No. ¹	Document Number	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	1.	US 7266633	09-04-2007	Micron Technology, Inc.	
	2.	US 7539909	05-26-2009	Intel Corporation	
	3.	US 7065688	06-20-2006	Advanced Micro Devices, Inc.	
	4.	US 5450576	09-12-1995	Ast Research, Inc.	
	5.	US 5684979	11-04-1997	IBM Corporation	
	6.	US 6886109	04-26-2005	Hewlett-Packard Development Company, L.P.	
	7.	US 7024518	04-04-2006	Intel Corporation	
	8.	US 7093115	08-15-2006	Intel Corporation	
	9.	US 7489163	02-10-2009	IBM Corporation	
	10.	US 8429493	04-23-2013	Apple Inc.	
	11.	US 20050071580	03-31-2005	Intel Corporation	
	12.	US 2007/0214347	09-13-2007	Rothman et al.	
	13.	US 20100005218	01-07-2010	IBM Corporation	
	14.	US 4672570	06-09-1987	The United States Of America As Represented By The Secretary Of The Air Force	
	15.	US 5511152	04-23-1996	Digital Equipment Corporation	
	16.	US 6763437	07-13-2004	Maxtor Corporation	

EXAMINER

DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	15/088,115
				Filing Date	April 1, 2016
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	CHERY, MARDOCHEE
Sheet	2	of	2	Attorney Docket Number	NETL.062C2

US PATENT DOCUMENTS					
Examiner Initials *	Cite No. ¹	Document Number	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	17.	US 7586350	09-08-2009	Hynix Semiconductor Inc.	
	18.	US 20030115427	06-19-2003	Micron Technology, Inc	
	19.	US 20070091702	04-26-2007	Andrey Nikitin	
	20.	US 20080256281	10-16-2008	IBM Corporation	
	21.	US 20090119464	05-07-2009	Grundy Kevin P	
	22.	US 20100042778	02-18-2010	Advanced Micro Devices, Inc.	
	23.	US 20100202240	08-12-2010	Stec, Inc.	
	24.	US 20110022789	01-27-2011	Kabushiki Kaisha Toshiba	

EXAMINER**DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Electronic Patent Application Fee Transmittal				
Application Number:		15088115		
Filing Date:		01-Apr-2016		
Title of Invention:		SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		
First Named Inventor/Applicant Name:		Hyun Lee		
Filer:		Jamie Jie Zheng		
Attorney Docket Number:		NETL.062C2		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
Total in USD (\$)				180

Electronic Acknowledgement Receipt	
EFS ID:	26609646
Application Number:	15088115
International Application Number:	
Confirmation Number:	7163
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062C2
Receipt Date:	10-AUG-2016
Filing Date:	01-APR-2016
Time Stamp:	23:41:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$180
RAM confirmation Number	6747
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2016-08-10_Amendment_NETL062C2.pdf	147629	yes	14
			8dab9b0b2403799d713c6d7d46ca16f5763896b3		
	Multipart Description/PDF files in .zip description				
	Document Description		Start		End
	Amendment/Req. Reconsideration-After Non-Final Reject		1		1
	Specification		2		2
	Claims		3		7
	Applicant Arguments/Remarks Made in an Amendment		8		14
Warnings:					
Information:					
2	Transmittal Letter	2016-08-10_IDS_Cover_NETL062C2.pdf	51965	no	2
			f5025f6e98633589597eae77c0fbd95be0064		
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	2016-08-10_IDS_NETL062C2.pdf	87604	no	2
			be84708a571b416c936a3d1c2e1a8e024315b968		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
4	Fee Worksheet (SB06)	fee-info.pdf	30504	no	2
			8edb0d4af731f5808332b27110ac3661bfcbabe1		
Warnings:					
Information:					
Total Files Size (in bytes):			317702		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 15/088,115		Filing Date 04/01/2016		☐ To be Mailed						
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO														
APPLICATION AS FILED – PART I														
(Column 1)		(Column 2)												
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)						
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A								
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A		N/A		N/A								
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A								
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		X \$		=						
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		X \$		=						
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).												
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))														
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL								
APPLICATION AS AMENDED – PART II														
(Column 1)		(Column 2)		(Column 3)										
AMENDMENT	08/10/2016		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)			
	Total (37 CFR 1.16(i))		* 22		Minus ** 20		= 2		X \$80 =		160			
	Independent (37 CFR 1.16(h))		* 3		Minus *** 3		= 0		X \$420 =		0			
	☐ Application Size Fee (37 CFR 1.16(s))													
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))													
						TOTAL ADD'L FEE		160						
(Column 1)		(Column 2)		(Column 3)										
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)			
	Total (37 CFR 1.16(i))		*		Minus **		=		X \$		=			
	Independent (37 CFR 1.16(h))		*		Minus ***		=		X \$		=			
	☐ Application Size Fee (37 CFR 1.16(s))													
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))													
						TOTAL ADD'L FEE								
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										LIE LYNNELL JOHNSON				

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 08/18/2016

LJOHNSO1	SALE	#00000002	Mailroom Dt:	08/10/2016	505963	15088115
		01	FC : 1202	160.00	DA	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist, Inc.
App. No.	:	15/088,115
Filed	:	April 1, 2016
For	:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
Examiner	:	CHERY, MARDOCHEE
Art Unit	:	2133
Conf. No.	:	7163
Docket No.	:	NETL.062C2

AUTHORIZATION TO COMMUNICATE VIA EMAIL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application by video conferencing, instant messaging, or electronic mail. I understand that a copy of these communications will be made of record in the application file.

The undersigned can be reached at (650) 521-4828 or jz@jzpatent.com for any questions regarding the above-reference patent application.

Respectfully submitted,

Date: August 10, 2016

/Jamie J. Zheng/

Jamie J. Zheng
Customer No. 79141

51167

(Reg. No.)

Electronic Acknowledgement Receipt	
EFS ID:	26609769
Application Number:	15088115
International Application Number:	
Confirmation Number:	7163
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062C2
Receipt Date:	11-AUG-2016
Filing Date:	01-APR-2016
Time Stamp:	02:23:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2016-08-10_Email_Authorization_NETL062C2.pdf	58524 1b64e83e96fdb37e3ec7c93f7aecbdf24fb699	no	1

Warnings:

Information:	
Total Files Size (in bytes):	58524
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist, Inc.
App. No.	:	15/169,745
Filed	:	June 1, 2016
For	:	MEMORY MODULE CAPABLE OF HANDSHAKING WITH A MEMORY CONTROLLER OF A HOST SYSTEM
Examiner	:	CHERY, MARDOCHEE
Art Unit	:	2133
Conf. No.	:	6558
Docket No.	:	NETL.062C3

AUTHORIZATION TO COMMUNICATE VIA EMAIL

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Alexandria, VA 22313-1450

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The undersigned can be reached at (650) 521-4828 or jz@jzpatent.com for any questions regarding the above-reference patent application.

Respectfully submitted,

Date: August 10, 2016

/Jamie J. Zheng/
Jamie J. Zheng
Customer No. 79141

51167
(Reg. No.)

Electronic Acknowledgement Receipt	
EFS ID:	26609770
Application Number:	15088115
International Application Number:	
Confirmation Number:	7163
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062C2
Receipt Date:	11-AUG-2016
Filing Date:	01-APR-2016
Time Stamp:	02:24:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2016-08-10_Email_Authorization_NETL062C3.pdf	65304 51d5ff97e52cca2748d9e222f8e477dd7acc86d6	no	2

Warnings:

Information:	
Total Files Size (in bytes):	65304
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/088,115	04/01/2016	Hyun Lee	NETL.062C2	7163
79141	7590	11/25/2016	EXAMINER	
Jamie J. Zheng, Ph.D Esq. P.O. Box 60573 Palo Alto, CA 94306			CHERY, MARDOCHEE	
			ART UNIT	PAPER NUMBER
			2133	
			NOTIFICATION DATE	DELIVERY MODE
			11/25/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jz@jzpatent.com
eofficeaction@appcoll.com
infohub.j@gmail.com

Office Action Summary	Application No. 15/088,115	Applicant(s) LEE, HYUN	
	Examiner Mardochee CHERY	Art Unit 2133	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 8/10/16.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 21-42 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 21-42 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date 8/10/16.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 4) ☐ Other: ____.

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 103

2. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

3. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 21-42 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Moshayedi (US 20100202240 A1) and Fahr (US 20080256281 A1).

As per claim 21, Moshayedi discloses a memory module, comprising: a printed circuit board having edge connections that fit into a corresponding slot of a host system, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections [¶0026, 0027, 0060]; dynamic random access memory elements configured to communicate data signals with the memory controller via the first edge connections [¶0027]; a module controller coupled to the dynamic random access memory elements, wherein the module controller is configured to receive from the memory controller via the second edge connections address and command signals associated with one or more memory read, write, pre-charge, or refresh operations and to control the memory elements in accordance with the address and command signals [¶0032, 0055], the module controller having an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations [¶0027, 0033, 0047, 0059, 0060, 0066]; wherein the module controller is further configured to process one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation, and wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection [¶0066, 0084, 0027, 0033, 0047].

Fahr discloses two open-drain outputs are available to permit multiple modules to share a common signal line [¶0067].

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant to drive a notification signal via an open drain output in order to permit external monitoring of the memory operation.

As per claim 22, Moshayedi discloses the memory module of claim 21, wherein the module controller comprises one or more integrated circuit [Figs. 6A-6B].

As per claim 23, Fahr discloses the memory module of claim 21, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output [¶0067].

As per claim 24, Moshayedi discloses the memory module of claim 23, wherein the notification circuit drives the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground [Figs. 7A-7B].

As per claim 25, Moshayedi discloses the memory module of claim 24, wherein the notification circuit drives the signal indicating the parity error by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground [Figs. 7A-7B].

As per claim 26, Moshayedi discloses the memory module of claim 24, wherein the notification circuit drives the notification signal using one or more OR logic elements [Figs. 7A-7B].

As per claim 27, Moshayedi discloses the memory module of claim 21, wherein the one or more training sequences are initiated by the memory controller [Fig. 5].

As per claim 28, Moshayedi discloses the memory module of claim 21, wherein the module controller processes the one or more training sequences in response to a command received from the memory controller [Fig. 5].

As per claims 29-42, the rationale in the rejection of claims 21-28 is herein incorporated.

Conclusion

6. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 8/10/16 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609.04(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee CHERY whose telephone number is (571)272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jared Ian Rutz can be reached on (571)272-5535. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

November 14, 2016

/Mardochee CHERY/
Primary Examiner, Art Unit 2133

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.C./

PTO/SB/08a/b(07-09)

Approved for use through 7/31/2012. OMB 0651-0031

US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	15/088,115
				Filing Date	April 1, 2016
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	CHERY, MARDOCHEE
Sheet	1	of	2	Attorney Docket Number	NETL.062C2

US PATENT DOCUMENTS					
Examiner Initials *	Cite No. ¹	Document Number	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	1.	US 7266633	09-04-2007	Micron Technology, Inc.	
	2.	US 7539909	05-26-2009	Intel Corporation	
	3.	US 7065688	06-20-2006	Advanced Micro Devices, Inc.	
	4.	US 5450576	09-12-1995	Ast Research, Inc.	
	5.	US 5684979	11-04-1997	IBM Corporation	
	6.	US 6886109	04-26-2005	Hewlett-Packard Development Company, L.P.	
	7.	US 7024518	04-04-2006	Intel Corporation	
	8.	US 7093115	08-15-2006	Intel Corporation	
	9.	US 7489163	02-10-2009	IBM Corporation	
	10.	US 8429493	04-23-2013	Apple Inc.	
	11.	US 20050071580	03-31-2005	Intel Corporation	
	12.	US 2007/0214347	09-13-2007	Rothman et al.	
	13.	US 20100005218	01-07-2010	IBM Corporation	
	14.	US 4672570	06-09-1987	The United States Of America As Represented By The Secretary Of The Air Force	
	15.	US 5511152	04-23-1996	Digital Equipment Corporation	
	16.	US 6763437	07-13-2004	Maxtor Corporation	

EXAMINER

/Mardochee Chery/

DATE CONSIDERED

11/20/2016

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Samsung Electronics Co., Ltd.

Ex. 1005, p. 108

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.C./

PTO/SB/08a/b(07-09)

Approved for use through 7/31/2012. OMB 0651-0031

US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	15/088,115
				Filing Date	April 1, 2016
				First Named Inventor	Hyun Lee
				Art Unit	2133
				Examiner Name	CHERY, MARDOCHEE
Sheet	2	of	2	Attorney Docket Number	NETL.062C2

US PATENT DOCUMENTS					
Examiner Initials *	Cite No. ¹	Document Number	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	17.	US 7586350	09-08-2009	Hynix Semiconductor Inc.	
	18.	US 20030115427	06-19-2003	Micron Technology, Inc	
	19.	US 20070091702	04-26-2007	Andrey Nikitin	
	20.	US 20080256281	10-16-2008	IBM Corporation	
	21.	US 20090119464	05-07-2009	Grundy Kevin P	
	22.	US 20100042778	02-18-2010	Advanced Micro Devices, Inc.	
	23.	US 20100202240	08-12-2010	Stec, Inc.	
	24.	US 20110022789	01-27-2011	Kabushiki Kaisha Toshiba	

EXAMINER

/Mardochee Chery/

DATE CONSIDERED

11/20/2016

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Samsung Electronics Co., Ltd.

Ex. 1005, p. 109

<i>Index of Claims</i> 	Application/Control No. 15088115	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant			☐ CPA			☐ T.D.			☐ R.1.47		
CLAIM		DATE									
Final	Original	11/14/2016									
	1	-									
	2	-									
	3	-									
	4	-									
	5	-									
	6	-									
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	28	✓									
	29	✓									
	30	✓									
	31	✓									
	32	✓									
	33	✓									
	34	✓									
	35	✓									
	36	✓									

<i>Index of Claims</i> 	Application/Control No. 15088115	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

✓	Rejected
=	Allowed

-	Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	11/14/2016								
	37	✓								
	38	✓								
	39	✓								
	40	✓								
	41	✓								
	42	✓								

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5	("20100042778" "20030115427").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/16 14:07
L2	4	1 and (initializ\$7 near5 (memory device array))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/16 14:18
L3	1	1 and (read\$3 writ\$4 access\$3) same (JDEC JEDEC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/16 14:22
L4	0	1 and (second\$3 another other) near3 (mode status state) with (memory DIMM \$3RAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/16 14:41
L5	0	1 and (second\$3 another other) near5 (mode status state) with (memory DIMM \$3RAM device controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/16 14:41
L6	0	1 and (second\$3 another other different) near5 (mode status state) with (memory DIMM \$3RAM device controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/16 14:41
L7	3	1 and (mode status state) with (memory DIMM \$3RAM device controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/16 14:42
L8	0	1 and (mode status state) with (memory DIMM \$3RAM device controller) same (exit\$3 branch\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/16 14:42
L9	0	1 and (error) with (memory DIMM \$3RAM device controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/16 14:45
L10	0	1 and (error fault) with (memory DIMM \$3RAM device controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/16 14:45

EAST Search History

L11	1	1 and (error fault\$3 fail\$4) with (memory DI MM \$3RAM device controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/16: 14:45
L12	2	1 and (transistor gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/16: 14:46
L13	1	1 and (high\$3 low\$3) near3 (impedance power resistance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/16: 14:48

5/ 16/ 2016 2:55:26 PM**C:\ Users\ mchery\ Documents\ EAST\ Workspaces\ 13942721.wsp**

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	40	(page near2 mov\$3) with (main near2 (memory storage)) with (cach\$3 "L2" "L3" "L4")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 09:15
S2	32	S1 and @ad<"20131203"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 09:24
S3	14	(page near2 mov\$3) with (main near2 (memory storage)) with (cach\$3 "L2" "L3" "L4") same (multipl\$7 several plural\$3) near3 (processor CPU core)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 09:48
S4	11	S3 and @ad<"20131203"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 09:49
S5	5	(page near2 mov\$3) with (main near2 (memory storage)) with (cach\$3 "L2" "L3" "L4") same (multipl\$7 several plural\$3) near3 (processor CPU core) same (fetch\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 10:01
S6	2	S5 and @ad<"20131203"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 10:02
S7	5	(page near2 mov\$3) with (main near2 (memory storage)) with (cach\$3 "L2" "L3" "L4") same (multipl\$7 several plural\$3) near3 (processor CPU core) same (fetch\$3 aggregat\$3 filter\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 10:06
S8	8	(page near2 mov\$3) with (main near2	US-PGPUB;	OR	ON	2016/05/23

		(memory storage)) with (cach\$3 "L2" "L3" "L4") same (multipl\$7 several plural\$3) near3 (processor CPU core) and (fetch\$3 aggregat\$3 filter\$3)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			10:07
S9	5	S8 and @ad< "20131203"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 10:08
S10	12	(page near2 mov\$3) near5 (main near2 (memory storage)) with (cach\$3 "L2" "L3" "L4") same (multipl\$7 several plural\$3) near3 (processor CPU core)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 10:37
S11	9	S10 and @ad< "20131203"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 10:39
S12	8	S8 and (accumulat\$3 stor\$3 aggregat\$3 filter\$3) near3 (data instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 11:38
S13	40	(page near2 mov\$3) with (main near2 (memory storage)) with (cach\$3 "L2" "L3" "L4")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 14:02
S14	32	S13 and @ad< "20131203"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 14:02
S15	0	S14 and (filter\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 14:02
S16	86	(page near2 mov\$3) same (main near2 (memory storage)) same (cach\$3 "L2" "L3" "L4")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2016/05/23 14:03

			IBM_TDB			
S17	10	S16 and (filter\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 14:03
S18	7	S17 and @ad<"20131203"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 14:03
S19	87	(pag\$3 near2 mov\$3) same (main near2 (memory storage)) same (cach\$3 "L2" "L3" "L4")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 14:07
S20	10	S19 and (filter\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 14:08
S21	5	(filter\$3 near3 engine) same (compar\$3 comparison match\$3 equal\$3) same fetch\$3 same (cach\$3 (main near3 (storage memory)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 14:23
S22	5	(filter\$3 near3 engine) same (compar\$3 comparison match\$3 equal\$3) same fetch\$3 same (cach\$3 "L1" "L2" "L3" (main near3 (storage memory)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 14:23
S23	2	(filter\$3 near3 engine) same (compar\$3 comparison match\$3 equal\$3) same fetch\$3 same (cach\$3 "L1" "L2" "L3" (main near3 (storage memory))) same (mask\$3 bitmask\$3 bit-mask\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 14:24
S24	0	S23 and @ad<"20131203"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 14:24
S25	2	(filter\$3 near3 engine) same (compar\$3 comparison match\$3 equal\$3) same fetch\$3 same (cach\$3 "L1" "L2" "L3" (main near3 (storage memory))) and	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2016/05/23 14:26

		(mask\$3 bitmask\$3 bit-mask\$3)	JPO; DERWENT; IBM_TDB			
S26	26	(filter\$3 near\$3 engine) and (compar\$3 comparison match\$3 equal\$3) same fetch\$3 same (cach\$3 "L1" "L2" "L3" (main near\$3 (storage memory))) and (mask\$3 bitmask\$3 bit-mask\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 14:28
S27	24	S26 and @ad<"20131203"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 14:28
S28	14	(filter\$3 near\$3 engine) and (compar\$3 comparison match\$3 equal\$3) same fetch\$3 same (cach\$3 "L1" "L2" "L3" (main near\$3 (storage memory))) and (compar\$3 comparison match\$3 equal\$3) same (mask\$3 bitmask\$3 bit-mask\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 14:29
S29	12	S28 and @ad<"20131203"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 14:29
S30	8	("20020083299" "6738872" "20140108742").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 14:46
S31	1	S30 and filter\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 14:46
S32	18	(filter\$3) and (compar\$3 comparison match\$3 equal\$3) same fetch\$3 same (cach\$3 "L1" "L2" "L3" (main near\$3 (storage memory))) and (compar\$3 comparison match\$3 equal\$3) same (mask\$3 bitmask\$3 bit-mask\$3) same (buffer\$3 queue\$3 enqueue\$3) same (processor cpu core)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 15:03
S33	0	S30 and (filter\$3) and (compar\$3 comparison match\$3 equal\$3) same fetch\$3 same (cach\$3 "L1" "L2" "L3" (main near\$3 (storage memory))) and (compar\$3 comparison match\$3 equal\$3) same (mask\$3 bitmask\$3 bit-mask\$3) same (buffer\$3 queue\$3 enqueue\$3) same (processor cpu core)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 15:03

S34	1	S30 and (filter\$3) and (compar\$3 comparison match\$3 equal\$3) same fetch\$3 same (cach\$3 "L1" "L2" "L3" (main near3 (storage memory))) and (compar\$3 comparison match\$3 equal\$3) same (mask\$3 bitmask\$3 bit-mask\$3) same (buffer\$3 queue\$3 enqueue\$3) and (processor cpu core)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 15:03
S35	0	S30 and (line-wise)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 15:16
S36	0	S34 and (cach\$3 near3 line)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 15:16
S37	1	S34 and (line)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 15:17
S38	3	S30 and (line)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 15:17
S39	2	S30 and (cach\$3 near3 line) same (compar\$3 comparison match\$3 equal\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 15:18
S40	0	S30 and (boolean "XOR" "OR" arithmetic) near3 (operation instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 15:21
S41	0	S30 and (boolean "XOR" "OR" arithmetic) near3 (operation instruction operator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/05/23 15:21
S42	1	S30 and (boolean "XOR" "OR" arithmetic)	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2016/05/23 15:21

			JPO; DERWENT; IBM_TDB			
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5/ 29/ 2016 5:11:06 PM
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Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	15088115
	Filing Date	2016-04-01
	First Named Inventor	Hyun Lee
	Art Unit	2133
	Examiner Name	CHERY, MARDOCHEE
	Attorney Docket Number	N3044.10014US04

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	8359521		2013-01-22	Kim et al.	
	2	7155579		2006-12-26	Neils, et al.	
	3	6754787		2004-06-22	Miller, et al.	
	4	5835733		1998-11-10	Walsh, et al.	
	5	3560935		1971-02-02	Beers	
	6	7757101		2010-07-13	Nonaka, et al.	
	7	5388074		1995-02-07	Buckenmaier	
	8	5438536		1995-08-01	Salzman	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	15088115
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	Art Unit	2133
	Examiner Name	CHERY, MARDOCHEE
	Attorney Docket Number	N3044.10014US04

9	6693840	2004-02-17	Shimada, et al.
10	8074034	2011-12-06	Sartore

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	1	20050193161		2005-09-01	Lee, et al.	
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	1	Inter partes review Case No. IPR2017-00548, Petition For Inter Partes Review Of U.S. Patent No. 8,489,837, filed December 30, 2016.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	15088115
	Filing Date	2016-04-01
	First Named Inventor	Hyun Lee
	Art Unit	2133
	Examiner Name	CHERY, MARDOCHEE
	Attorney Docket Number	N3044.10014US04

2	inter partes review Case No. IPR2017-00548, Exhibit 1003 "Declaration of Donald Alpert", filed December 30, 2016.
3	inter partes review Case No. IPR2017-00548, Exhibit 1010 "5400 MCH Datasheet", filed December 30, 2016.
4	inter partes review Case No. IPR2017-00548, Exhibit 1011 "Microsoft Computer Dictionary (5th Ed. 2002)", filed December 30, 2016.

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¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

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	Filing Date	2016-04-01
	First Named Inventor	Hyun Lee
	Art Unit	2133
	Examiner Name	CHERY, MARDOCHEE
	Attorney Docket Number	N3044.10014US04

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JAMIE J. ZHENG/	Date (YYYY-MM-DD)	2017-03-28
Name/Print	Jamie J. Zheng	Registration Number	51167

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Electronic Patent Application Fee Transmittal				
Application Number:		15088115		
Filing Date:		01-Apr-2016		
Title of Invention:		SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		
First Named Inventor/Applicant Name:		Hyun Lee		
Filer:		Jamie Jie Zheng/Brian GONzalez		
Attorney Docket Number:		N3044.10014US04		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
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Patent-Appeals-and-Interference:				
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Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
Total in USD (\$)				180

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EFS ID:	28765725
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	Intel5400_MCH_.pdf	6350995	no	472
			f72b15f0e219c0b93ca7d615934afbb55a718161		
Warnings:					
Information:					
2	Non Patent Literature	2017-12-30_Declaration-Alpert_IPR2017-00548_.pdf	1253091	no	71
			8ccd07987580b86c03d6c789b0b7d7be2d651d62		
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3	Non Patent Literature	2017-12-30_IPR2017-00548_Petition_.pdf	877567	no	55
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4	Non Patent Literature	Microsoft_Computer-Dictionary_.pdf	17706684	no	648
			61d7cc53d39cd3faca40e1d401e1f1a10f9540de		
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5	Information Disclosure Statement (IDS) Form (SB08)	2017-03-28_IDS_N3044-10014 US04.pdf	1035855	no	5
			c56013f49b5a55f7f0a11a30d1939684f2ed75fb		
Warnings:					
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6	Fee Worksheet (SB06)	fee-info.pdf	30804	no	2
			84876c8f18fea5b0e1b69a6d9d9a8b3bbb814b19		
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: A.NE.AFCP

Document Description: After Final Consideration Pilot Program Request

PTO/SB/434 (05-13)

CERTIFICATION AND REQUEST FOR CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0		
Practitioner Docket No.: N3044.10014US04	Application No.: 15/088,115	Filing Date: 04-01-2016
First Named Inventor: Hyun Lee	Title: SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE	
APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0 (AFCP 2.0) OF THE ACCOMPANYING RESPONSE UNDER 37 CFR 1.116. - The above-identified application is (i) an original utility, plant, or design nonprovisional application filed under 35 U.S.C. 111(a) [a continuing application (<i>e.g.</i>, a continuation or divisional application) is filed under 35 U.S.C. 111(a) and is eligible under (i)], or (ii) an international application that has entered the national stage in compliance with 35 U.S.C. 371(c). - The above-identified application contains an outstanding final rejection. - Submitted herewith is a response under 37 CFR 1.116 to the outstanding final rejection. The response includes an amendment to at least one independent claim, and the amendment does not broaden the scope of the independent claim in any aspect. - This certification and request for consideration under AFCP 2.0 is the only AFCP 2.0 certification and request filed in response to the outstanding final rejection. - Applicant is willing and available to participate in any interview requested by the examiner concerning the present response. - This certification and request is being filed electronically using the Office's electronic filing system (EFS-Web). - Any fees that would be necessary consistent with current practice concerning responses after final rejection under 37 CFR 1.116, <i>e.g.</i>, extension of time fees, are being concurrently filed herewith. [There is no additional fee required to request consideration under AFCP 2.0.] - By filing this certification and request, applicant acknowledges the following: - Reissue applications and reexamination proceedings are not eligible to participate in AFCP 2.0. - The examiner will verify that the AFCP 2.0 submission is compliant, <i>i.e.</i>, that the requirements of the program have been met (see items 1 to 7 above). For compliant submissions: - The examiner will review the response under 37 CFR 1.116 to determine if additional search and/or consideration (i) is necessitated by the amendment and (ii) could be completed within the time allotted under AFCP 2.0. If additional search and/or consideration is required but cannot be completed within the allotted time, the examiner will process the submission consistent with current practice concerning responses after final rejection under 37 CFR 1.116, <i>e.g.</i>, by mailing an advisory action. - If the examiner determines that the amendment does not necessitate additional search and/or consideration, or if the examiner determines that additional search and/or consideration is required and could be completed within the allotted time, then the examiner will consider whether the amendment places the application in condition for allowance (after completing the additional search and/or consideration, if required). If the examiner determines that the amendment does not place the application in condition for allowance, then the examiner will contact the applicant and request an interview. - The interview will be conducted by the examiner, and if the examiner does not have negotiation authority, a primary examiner and/or supervisory patent examiner will also participate. - If the applicant declines the interview, or if the interview cannot be scheduled within ten (10) calendar days from the date that the examiner first contacts the applicant, then the examiner will proceed consistent with current practice concerning responses after final rejection under 37 CFR 1.116.		
Signature /JAMIE J. ZHENG/		Date April 25, 2017
Name (Print/Typed) Jamie J. Zheng		Practitioner Registration No. 51167
Note: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.		
☒ * Total of <u>1</u> forms are submitted.		

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Netlist, Inc.
App. No. : 15/088,115
Filed : April 1, 2016
For : SYSTEMS AND METHODS
FOR HANDSHAKING WITH A
MEMORY MODULE
Examiner : CHERY, MARDOCHEE
Art Unit : 2133
Conf. No. : 7163
Docket No. : N3044.10014US04

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April 25, 2017

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

RESPONSE TO FINAL OFFICE ACTION DATED NOVEMBER 25, 2016

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Final Office Action dated November 25, 2016 for the above-identified patent application.

Submitted herewith is a Request for Consideration under the After Final Consideration Pilot 2.0 (AFCP 2.0) (Form PTO/SB/434).

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

AMENDMENTS to the CLAIMS begin on Page 2 of this paper.

REMARKS begin on Page 7 of this paper.

IN THE CLAIMS:

Claims 1-20. (Cancelled)

21. (Currently Amended) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of ~~the~~ a host system, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

dynamic random access memory elements configured to communicate data signals with the memory controller via the first edge connections;

a module controller coupled to the dynamic random access memory elements, wherein the module controller is configured to receive from the memory controller via the second edge connections address and command signals associated with one or more memory read, write, pre-charge, or refresh operations and to control the memory elements in accordance with the address and command signals, the module controller having an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error in response to the parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations;

wherein the module controller is further configured to process one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation, and wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection.

22. (Previously Presented) The memory module of claim 21, wherein the module controller comprises one or more integrated circuit.

23. (Previously Presented) The memory module of claim 21, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.
24. (Previously Presented) The memory module of claim 23, wherein the notification circuit drives the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
25. (Previously Presented) The memory module of claim 24, wherein the notification circuit drives the parity error signal by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
26. (Previously Presented) The memory module of claim 24, wherein the notification circuit drives the notification signal using one or more OR logic elements.
27. (Previously Presented) The memory module of claim 21, wherein the one or more training sequences are initiated by the memory controller.
28. (Previously Presented) The memory module of claim 21, wherein the module controller processes the one or more training sequences in response to a command received from the memory controller.
29. (Previously Presented) A method performed by a memory module operating with a memory controller of the host system, the memory module including dynamic random access memory elements on a printed circuit board, the printed circuit board having edge connections that fit into a corresponding slot of a host system, the edge connections including first edge connections via which the dynamic random access memory devices communicate data with the memory controller, second edge connections via which the memory module receives address and command signals from the memory controller, and an error edge connection in addition to the first edge connections and the second edge connections, the method comprising:

receiving from the memory controller address and command signals associated with one or more memory read, write, pre-charge, or refresh operations;

controlling the dynamic random access memory elements to perform the one or more memory read, write, pre-charge, or refresh operations in accordance with the address and command signals;

outputting to the memory controller via an open-drain output coupled to the error edge connection a signal indicating a parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations;

processing one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation; and

driving a notification signal associated with the one or more training sequences to the memory controller via the open drain output and the error edge connection.

30. (Previously Presented) The method of claim 29, wherein driving the notification signal comprises driving a gate of each of one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground, the one or more transistors each having an open drain coupled to the open drain output.

31. (Previously Presented) The method of claim 30, wherein driving the signal indicating the parity error comprises driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground.

32. (Previously Presented) The method of claim 30, wherein driving the notification signal comprises using one or more OR logic elements.

33. (Previously Presented) The method of claim 29, wherein the one or more training sequences are initiated by the memory controller.

34. (Previously Presented) The method of claim 29, wherein the one or more training sequences are processed in response to a command received from the memory controller of the host system via the second edge connections.

35. (Currently Amended) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the a-host system, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

dynamic random access memory elements configured to communicate data signals with the memory controller via the first edge connections; and

a module controller coupled to the dynamic random access memory elements, wherein the module controller is configured to receive from the memory controller via the second edge connections address and command signals associated with one or more memory read, write, pre-charge, or refresh operations and to control the memory elements in accordance with the address and command signals, the module controller having an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error in response to the parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations;

wherein the module controller is further configured to process one or more training sequences while the memory module is not performing any memory read, write, pre-charge, or refresh operation, and wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection.

36. (Previously Presented) The memory module of claim 35, wherein the module controller comprises one or more integrated circuit.

37. (Previously Presented) The memory module of claim 35, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.

38. (Previously Presented) The memory module of claim 37, wherein the notification circuit generates the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.

39. (Previously Presented) The memory module of claim 38, wherein the notification circuit drives the signal indicating the parity error by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.

40. (Previously Presented) The memory module of claim 38, wherein the notification circuit drives the notification signal using one or more OR logic elements.

41. (Previously Presented) The memory module of claim 35, wherein the one or more training sequences are initiated by the memory controller.

42. (Previously Presented) The memory module of claim 35, wherein the module controller processes the one or more training sequences in response to a command received from the memory controller of the host system via the second edge connections.

REMARKS

This amendment responds to the Final Office Action dated November 25, 2016.

In the Office Action, the Examiner:

- rejected claims 21-42 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Moshayedⁱ US 20100202240 (hereafter “Moshayedⁱ”) in view of Fahr US 20080256281 (hereafter “Fahr”).

Claims 21 and 35 are amended. The amendments made in claims 21 and 35 are to address issues with antecedent basis and for better clarity, and thus should not necessitate any additional search and/or consideration. Support for the amendments can be found throughout the Specification (e.g., ¶0011-0012). Thus, no new matter is added.

Claim 21 as amended recites a memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

dynamic random access memory elements configured to communicate data signals with the memory controller via the first edge connections;

a module controller coupled to the dynamic random access memory elements, wherein the module controller is configured to receive from the memory controller via the second edge connections address and command signals associated with one or more memory read, write, pre-charge, or refresh operations and to control the memory elements in accordance with the address and command signals, the module controller having an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error in response to the parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations;

wherein the module controller is further configured to process one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation, and wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection.

In rejecting claim 21, the Examiner simply lumps multiple paragraphs in Moshayedi together, and states that these paragraphs disclose the various elements in claim 21 without any explanation or reasoning. For example, the Examiner cites Moshayedi [¶0027, 0033, 0047, 0059, 0060, 0066] as disclosing “the module controller having an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error in response to the parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations,” without pointing out where the open drain output is in Moshayedi and which signal in Moshayedi corresponds to the “signal indicating a parity error.”

Thus, the Applicant is left to guess what the Examiner’s rationale is in rejecting claim 21 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Moshayedi in view of Fahr. The Examiner seems to consider the non-volatile controller 110 in Moshayedi as corresponding to the module controller in claim 21. As shown in Moshayedi FIG. 1, the non-volatile controller 110 is shown to have several outputs: CACHE_DIRTY, DRAM_AVAILABLE, NVDIMM_READY, TEST_TX, and VBACK_RESET. The question is, which of these outputs the Examiner considers to correspond to the “open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error in response to the parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations?”

As described in Moshayedi ¶0037, the “CACHE_DIRTY signal indicates that flash memory 130 contains a data image of DRAM 120.” “During the BACKUP state, the CACHE_DIRTY signal **indicates the start of the backup process**. During POWER UP state, the CACHE_DIRTY **indicates that flash memory 130 contains a backup image.**” (*Emphasis added*) Therefore, the CACHE_DIRTY output cannot be “an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller **a signal indicating a parity error** in response to the parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations.”

As described in Mosheyedi ¶0038, the “DRAM_AVAILABLE signal **indicates when the system can access DRAM 120.**” (*Emphasis added*) “When DRAM_AVAILABLE is low, controller 110 has control of DRAM 120. When the signal is high, the system can take the DRAM devices (e.g., 121-122) out of self-refresh and access the data.” Therefore, the DRAM_AVAILABLE output cannot be “an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal **indicating a parity error** in response to the parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations.”

As described in Mosheyedi ¶0039, the “NVDIMM_READY signal **indicates that module 100 is capable of handling a power-loss event.**” (*Emphasis added*) “During normal system operation (idle state), the system cannot assert NVCACHE_ENABLE until NVDIMM_READY is asserted. During backup operation, NVDIMM_READY is deasserted. During restore operation, NVDIMM_READY is deasserted. If controller 110 determines at any time that a power loss event cannot be handled correctly, for example, if the EDL capacitor bank failed a self-test operation, controller 110 deasserts the NVDIMM_READY to notify the system to move any cache data from the DIMM memory (e.g., to move the data to permanent storage such as a hard drive of the system).” Therefore, the NVDIMM_READY output cannot be “an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller **a signal indicating a parity error** in response to the parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations.”

As described in Mosheyedi ¶0044, “Signals TEST_RX and TEST_TX **make up a production test interface** that is a 57.6Kbaud serial link.” “During normal system operation, the test signals are tristated and floating.” Therefore, the TEST_TX output cannot be “an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller **a signal indicating a parity error** in response to the parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations.”

As described in Mosheyedi ¶0043, “Module 100 also includes a third I2C interface that is located between controller 110 and backup power source 200 (the “backup power supply I2C interface”).” “The backup power supply I2C interface allows controller 110 **to communicate with the external backup power supply module using VBACK_SDA and VBACK_SCL**... The backup power supply reset (VBACK_RESET) allows controller 110 to reset the external backup power supply module.”).” (*Emphasis added*) Therefore, the VBACK_RESET output cannot be “an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller **a signal indicating a parity error** in response to the parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations.”

Furthermore, Moshayedi ¶0027 cited by the Examiner does not describe any output to the memory controller either. Also, Moshayedi ¶0033 cited by the Examiner describes the functions of NVDIMM_PG and NVCACHE_ENABLE, which are inputs, instead of outputs to the non-volatile control 110. Therefore, neither NVDIMM_PG nor NVCACHE_ENABLE can be “an open drain output” recited in claim 21.

Careful readings of the other paragraphs cited by the Examiner (i.e., ¶0047, 0059, 0060, 0066) with regard to this claim element also do not shed any light as to where in Moshayedi it is disclosed “an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error in response to the parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations.”

In fact, Moshayedi is about a flash-backed dual in-line memory module (DIMM) 100 including a nonvolatile memory 130, a volatile memory 120, and a nonvolatile memory control 110 whose main function is to control the data flow between the non-volatile memory and the volatile memory during data backup and restore in case of power failure. (See Moshayedi ¶0004, 0005, 0016) As described in Moshayedi ¶0027, which is cited by the Examiner, when “controller 110 controls DRAM 120, **the register is isolated from the edge connector using FET bus switches 163 and controller 110 can**

directly drive the register inputs.” (*Emphasis added*) This is because, the DIMM transfers data from the volatile memory to the non-volatile memory under the control of the controller 110 and does not need to respond to command from the system.

Furthermore, as described in Moshayedi ¶0027, when “**the system controls the DRAM array, the FET bus switches 163 are on and the FPGA (i.e., the controller 110) tristates its outputs.”** (*Emphasis added*) Therefore, the controller 110 in Moshayedi is decoupled from the DRAM array 120 when the DRAM array is performing read/write operations in accordance with the address and command signals from the system. Thus, the controller 110 in Moshayedi cannot possibly “control the memory elements in accordance with the address and command signals” received from the system, as required by claim 21, or act on any parity error that occurs during memory read, write, pre-charge, or refresh operations.

Therefore, unlike what is claimed in claim 21, the controller 110 in Moshayedi is not “configured to receive from the memory controller via the second edge connections address and command signals associated with one or more memory read, write, pre-charge, or refresh operations and to control the memory elements in accordance with the address and command signals.”

The Examiner further cites Moshayedi [¶0066, 0084, 0027, 0033, 0047] as disclosing “wherein the module controller is further configured to process one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation, and wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection,” without stating what the Examiner considers as the training sequences and what signal can be regarded as the “notification signal associated with the one or more training sequences.”

Moshayedi ¶0066 is about power transistors “responsible for moving the DRAM devices to the backup power and isolating the backup power from the system VDD and V3P_AUX.” Moshayedi ¶0084 discusses variations of different components in the system shown in FIG. 1 of Moshayedi. Moshayedi ¶0027 discusses the flash-backed dual

in-line memory module (DIMM) 100 in general. Moshayedi ¶0033 describes NVDIMM_PG signal, which “reports the state of the power in the user system.” Moshayedi ¶0047 describes transitions to and from GLITCH state, which “signifies a case in which the system temporarily lost power, but power has returned before the backup operation completed thus allowing the user to retrieve the DRAM contents without using the flash data.” (See Moshayedi ¶0049)

Therefore, these paragraphs cited by the Examiner do not even come close to disclosing or teaching “wherein the module controller is further configured to process one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation, and wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection.”

Fahr does not make up for the deficiency of Moshayedi. The Examiner cites Fahr ¶0067 as disclosing two open-drain outputs to permit multiple modules to share a common signal line. But, claim 21 does not just recite an open drain output, it recites a memory module including, among other things, a module controller having an open-drain output. It further includes the limitations that the module controller “outputs to the memory controller a signal indicating a parity error” AND “is further configured to drive a notification signal associated with the one or more training sequences to the memory controller” **via the same open-drain output**.

Fahr, on the other, describes an ECC/Parity register on a DIMM using two open-drain outputs for two different error signals, /Error (CE) 120 and /Error (UE) 121, respectively (Fahr [0067]. Neither of these open drain output is use to output to the memory controller “a signal indicating a parity error” AND “a notification signal associated with the one or more training sequences to the memory controller.”

Therefore, claim 21 as amended is patentable over Moshayedi in view of Fahr.

Claims 22-28 depend from claim 21 as amended. Therefore, claims 22-28 are patentable for at least the same reasons claim 21 as amended is patentable.

The arguments regarding claim 21 as amended apply to claim 29. Therefore, claim 29 is also patentable.

Claims 30-34 depend from claim 29. Therefore, claims 30-34 are patentable for at least the same reasons claim 29 is patentable.

The arguments regarding claim 21 as amended apply to claim 35 as amended. Therefore, claim 35 as amended is also patentable.

Claims 36-42 depend from claim 35 as amended. Therefore, claims 36-42 are patentable for at least the same reasons claim 35 as amended is patentable.

Applicant submits that claims 21-42 are in condition for allowance and respectfully requests such action. The Examiner is invited to call the undersigned at (650) 521-4828 to set up a telephone interview under the After Final Consideration Pilot 2.0 (AFCP 2.0) (Form PTO/SB/434) to discuss any remaining issues.

Respectfully submitted,

Date: April 25, 2017

/Jamie J. Zheng/

51167

Jamie J. Zheng
Customer No. 79141

(Reg. No.)

Electronic Patent Application Fee Transmittal				
Application Number:		15088115		
Filing Date:		01-Apr-2016		
Title of Invention:		SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		
First Named Inventor/Applicant Name:		Hyun Lee		
Filer:		Jamie Jie Zheng		
Attorney Docket Number:		N3044.10014US04		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension - 2 months with \$0 paid	1252	1	600	600
Miscellaneous:				
Total in USD (\$)				600

Electronic Acknowledgement Receipt	
EFS ID:	29025969
Application Number:	15088115
International Application Number:	
Confirmation Number:	7163
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	N3044.10014US04
Receipt Date:	25-APR-2017
Filing Date:	01-APR-2016
Time Stamp:	23:47:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 600
RAM confirmation Number	042617INTEFSW23514400
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	After Final Consideration Program Request	2017-04-25_AFCP_N3044-10014US04.pdf	226701	no	2
			a887acfe276ac604d90faf5cb500086efa6a499e		
Warnings:					
Information:					
2	Response After Final Action	2017-04-25_Amendment_NETL062C2.pdf	525830	no	13
			ff8e4ba635e6dbbbf07885027c090cbbaf188b9		
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30698	no	2
			970b908bd287a44911585406be75d3cddb3d7acb		
Warnings:					
Information:					
Total Files Size (in bytes):			783229		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 15/088,115	Filing Date 04/01/2016	☐ To be Mailed
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO							
APPLICATION AS FILED – PART I							
(Column 1)		(Column 2)					
FOR	NUMBER FILED	NUMBER EXTRA			RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A			N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A			N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A			N/A		
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*			X \$ =		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*			X \$ =		
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL		
APPLICATION AS AMENDED – PART II							
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT	04/25/2017	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 22	Minus	** 22	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.							

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/088,115	04/01/2016	Hyun Lee	N3044.10014US04	7163
79141	7590	05/16/2017	EXAMINER	
Jamie J. Zheng, Ph.D Esq. MASCHOFF BRENNAN 1389 Center Drive Suite 300 Park City, UT 84098			CHERY, MARDOCHEE	
			ART UNIT	PAPER NUMBER
			2133	
			NOTIFICATION DATE	DELIVERY MODE
			05/16/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

d@mabr.com

Advisory Action Before the Filing of an Appeal Brief	Application No. 15/088,115	Applicant(s) LEE, HYUN	
	Examiner Mardochee CHERY	Art Unit 2133	AIA (First Inventor to File) Status No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 25 April 2017 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.
NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance;
 (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires _____ months from the mailing date of the prior Advisory Action or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.

Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because

a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);

b) ☒ They raise the issue of new matter (see NOTE below);

c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☒ For purposes of appeal, the proposed amendment(s): (a) ☒ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:
See Continuation Sheet.

13. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____

14. ☐ Other: _____.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____

Claim(s) objected to: _____

Claim(s) rejected: 21-42.

Claim(s) withdrawn from consideration: _____

5/3/2017	/Mardochee CHERY/ Primary Examiner, Art Unit 2133
----------	--

Continuation of 12. does NOT place the application in condition for allowance because: The after final amendment filed 04/25/2017, under AFCP 2.0, cannot be reviewed and a search conducted under the guidelines of the pilot program and the amendment potentially raises the issue of new matter and require further search and consideration.

AFCP 2.0 Decision

Application No.

15/088,115

Applicant(s)

LEE, HYUN

Examiner

Mardochee CHERY

Art Unit

2133

This is in response to the After Final Consideration Pilot request filed 04/25/2017.

1. **Improper Request** – The AFCP 2.0 request is improper for the following reason(s) and the after final amendment submitted with the request will be treated under pre-pilot procedure.

- ☐ An AFCP 2.0 request form PTO/SB/434 (or equivalent document) was not submitted.
- ☐ A non-broadening amendment to at least one independent claim was not submitted.
- ☐ A proper AFCP 2.0 request was submitted in response to the most recent final rejection.
- ☐ Other:

2. Proper Request

- A. After final amendment submitted with the request will not be treated under AFCP 2.0.

The after final amendment cannot be reviewed and a search conducted within the guidelines of the pilot program.

- ☒ The after final amendment will be treated under pre-pilot procedure.

- B. Updated search and/or completed additional consideration.

The examiner performed an updated search and/or completed additional consideration of the after final amendment within the time authorized for the pilot program. The result(s) of the updated search and/or completed additional consideration are:

- ☐ 1. All of the rejections in the most recent final Office action are overcome and a Notice of Allowance is issued herewith.
- ☐ 2. The after final amendment would not overcome all of the rejections in the most recent final Office action. See attached interview summary for further details.
- ☐ 3. The after final amendment was reviewed, and it raises a new issue(s). See attached interview summary for further details.
- ☐ 4. The after final amendment raises new issues, but would overcome all of the rejections in the most recent final Office action. A decision on determining allowability could not be made within the guidelines of the pilot. See attached interview summary for further details, including any newly discovered prior art.
- ☐ 5. Other:

Examiner Note: Please attach an interview summary when necessary as described above.

PATENT

"DO NOT ENTER"
05/03/2017
MC

Customer No. 79141

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Netlist, Inc.
App. No. : 15/088,115
Filed : April 1, 2016
For : SYSTEMS AND METHODS
FOR HANDSHAKING WITH A
MEMORY MODULE
Examiner : CHERY, MARDOCHEE
Art Unit : 2133
Conf. No. : 7163
Docket No. : N3044.10014US04

CERTIFICATE OF EFS WEB
TRANSMISSION

I hereby certify that this correspondence and
any other attachment noted on the Automated
Acknowledgement Receipt, is being
transmitted from within the Pacific Time zone
to the Commissioner for Patents via the EFS
Web Server on:

April 25, 2017

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

RESPONSE TO FINAL OFFICE ACTION DATED NOVEMBER 25, 2016

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Final Office Action dated November 25, 2016 for the above-identified patent application.

Submitted herewith is a Request for Consideration under the After Final Consideration Pilot 2.0 (AFCP 2.0) (Form PTO/SB/434).

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

AMENDMENTS to the CLAIMS begin on Page 2 of this paper.

REMARKS begin on Page 7 of this paper.

Doc code: RCEX

PTO/SB/30EFS (07-14)

Doc description: Request for Continued Examination (RCE)

Approved for use through 07/31/2016. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL **(Submitted Only via EFS-Web)**

Application Number	15088115	Filing Date	2016-04-01	Docket Number (if applicable)	N3044.10014US04	Art Unit	2133
First Named Inventor	Hyun Lee			Examiner Name	CHERY, MARDOCHEE		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, to any international application that does not comply with the requirements of 35 U.S.C. 371, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV.

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☒ Amendment/Reply

☒ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
 (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to
 Deposit Account No. 505394

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

Applicant Signature

Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-14)

Approved for use through 07/31/2016. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	JAMIE J. ZHENG/	Date (YYYY-MM-DD)	2017-05-25
Name	Jamie J. Zheng	Registration Number	51167

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		15088115		
Filing Date:		01-Apr-2016		
Title of Invention:		SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		
First Named Inventor/Applicant Name:		Hyun Lee		
Filer:		Jamie Jie Zheng/Brian Gonzalez		
Attorney Docket Number:		N3044.10014US04		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension - 3 months with \$600 paid	1253	1	800	800
Miscellaneous:				
RCE- 1st Request	1801	1	1200	1200
Total in USD (\$)				2000

Electronic Acknowledgement Receipt	
EFS ID:	29318311
Application Number:	15088115
International Application Number:	
Confirmation Number:	7163
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/Brian Gonzalez
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10014US04
Receipt Date:	25-MAY-2017
Filing Date:	01-APR-2016
Time Stamp:	20:14:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$2000
RAM confirmation Number	052617INTEFSW20242000
Deposit Account	505394
Authorized User	Brian Gonzalez
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.21 (Miscellaneous fees and charges)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	2017-05-25_IDS_N3044-10014 US04.pdf	1035213	no	4
			4eb301a8ae598c032179b1c4b4006b12916eb3fe		
Warnings:					
Information:					
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2	Non Patent Literature	IPR2017-00548_2017-04-09_Patent-Owners-Preliminary-Response.pdf	1662735	no	25
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3	Non Patent Literature	IPR2017-00548_2017-04-09_Trial-Instituted.pdf	5388837	no	16
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4		2017-05-25_Amendment_RCE_N3044-10014US04.pdf	557424	yes	13
			31877427aa27100d5b0f503597f2f9b35d645a8b		
	Multipart Description/PDF files in .zip description				
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	Claims	2	6		
	Applicant Arguments/Remarks Made in an Amendment	7	13		
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5	Request for Continued Examination (RCE)	2017-05-25_RCE_N3044-10014 US04.pdf	1349896	no	3
			9c6fe855b400edd94d9c260984514fbc0ab d177d		
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6	Fee Worksheet (SB06)	fee-info.pdf	32584	no	2
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	15088115
	Filing Date	2016-04-01
	First Named Inventor	Hyun Lee
	Art Unit	2133
	Examiner Name	CHERY, MARDOCHEE
	Attorney Docket Number	N3044.10014US04

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	15088115
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	Art Unit	2133
	Examiner Name	CHERY, MARDOCHEE
	Attorney Docket Number	N3044.10014US04

1	Inter partes review Case No. IPR2017-00548, Patent Owner's Preliminary Response filed April 9, 2017.
2	Inter partes review Case No. IPR2017-00548, Trial Instituted document dated May 15, 2017.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	15088115
	Filing Date	2016-04-01
	First Named Inventor	Hyun Lee
	Art Unit	2133
	Examiner Name	CHERY, MARDOCHEE
	Attorney Docket Number	N3044.10014US04

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JAMIE J. ZHENG/	Date (YYYY-MM-DD)	2017-05-25
Name/Print	Jamie J. Zheng	Registration Number	51167

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Netlist, Inc.
App. No. : 15/088,115
Filed : April 1, 2016
For : SYSTEMS AND METHODS
FOR HANDSHAKING WITH A
MEMORY MODULE
Examiner : CHERY, MARDOCHEE
Art Unit : 2133
Conf. No. : 7163
Docket No. : N3044.10014US04

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Jamie J. Zheng, Reg. No. 51167

AMENDMENT AND REQUEST FOR CONTINUED EXAMINATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits the following Amendment and Request for Continued Examination in response to the Final Office Action dated November 25, 2016 for the above-identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5394.

AMENDMENTS to the CLAIMS begin on Page 2 of this paper.

REMARKS begin on Page 7 of this paper.

IN THE CLAIMS:

Claims 1-20. (Cancelled)

21. (Currently Amended) A memory module ~~operable with a memory controller of a host system~~, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of ~~the~~ a host system, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

dynamic random access memory elements configured to communicate data signals with the memory controller via the first edge connections;

a module controller coupled to the dynamic random access memory elements, wherein the module controller is configured to receive from the memory controller via the second edge connections address and command signals associated with one or more memory ~~read or write read, write, pre-charge, or refresh~~ operations and to control the memory elements in accordance with the address and command signals, the module controller having an open drain output coupled to the error edge connection whereby the module controller ~~is configured to output outputs~~ to the memory controller a signal indicating a parity error having occurred during the one or more memory ~~read or write read, write, pre-charge, or refresh~~ operations;

wherein the module controller is further configured to ~~process one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation;~~ and wherein the module controller is further configured to drive a notification signal associated with ~~the~~ one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection, ~~wherein the one or more training sequences are not associated with any memory read or write operation.~~

22. (Currently Amended) The memory module of claim 21, wherein the module controller comprises ~~an one or more~~ integrated circuit.

23. (Previously Presented) The memory module of claim 21, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.
24. (Previously Presented) The memory module of claim 23, wherein the notification circuit drives the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
25. (Previously Presented) The memory module of claim 24, wherein the notification circuit drives the parity error signal by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
26. (Previously Presented) The memory module of claim 24, wherein the notification circuit drives the notification signal using one or more OR logic elements.
27. (Previously Presented) The memory module of claim 21, wherein the one or more training sequences are initiated by the memory controller.
28. (Currently Amended) The memory module of claim 21, wherein the module controller ~~is configured to drive the notification signal to indicate a status of processes~~ the one or more training sequences ~~in response to a command received from to~~ the memory controller.
29. (Currently Amended) A method performed by a memory module operating with a memory controller of the host system, the memory module including dynamic random access memory elements on a printed circuit board, the printed circuit board having edge connections that fit into a corresponding slot of a host system, the edge connections including first edge connections via which the dynamic random access memory devices communicate data with the memory controller, second edge connections via which the memory module receives address and command signals from the memory controller, and an error edge connection in addition to the first edge connections and the second edge connections, the method comprising:

receiving from the memory controller address and command signals associated with one or more memory ~~read or write read, write, pre-charge, or refresh~~ operations;
controlling the dynamic random access memory elements to perform the one or more memory ~~read or write read, write, pre-charge, or refresh~~ operations in accordance with the address and command signals;
outputting to the memory controller via an open-drain output coupled to the error edge connection a signal indicating a parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations; ~~and~~
~~processing one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation; and~~
~~while the memory module is not performing any memory read or write operation,~~
driving a notification signal associated with the one or more training sequences to the memory controller via the open drain output and the error edge connection.

30. (Previously Presented) The method of claim 29, wherein driving the notification signal comprises driving a gate of each of one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground, the one or more transistors each having an open drain coupled to the open drain output.

31. (Previously Presented) The method of claim 30, wherein driving the signal indicating the parity error comprises driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground.

32. (Previously Presented) The method of claim 30, wherein driving the notification signal comprises using one or more OR logic elements.

33. (Previously Presented) The method of claim 29, wherein the one or more training sequences are initiated by the memory controller.

34. (Currently Amended) The method of claim 29, wherein ~~the notification signal indicates a status of~~ the one or more training sequences ~~are processed in response to a~~

~~command received from to~~ the memory controller of the host system ~~via the second edge connections.~~

35. (Currently Amended) A memory module ~~operable with a memory controller of a host system,~~ comprising:

a printed circuit board having edge connections that fit into a corresponding slot of ~~the a~~ host system, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

dynamic random access memory elements configured to communicate data signals with the memory controller via the first edge connections; and

a module controller coupled to the dynamic random access memory elements, wherein the module controller is configured to receive from the memory controller via the second edge connections address and command signals associated with one or more memory ~~read or write read, write, pre-charge, or refresh~~ operations and to control the memory elements in accordance with the address and command signals, the module controller having an open drain output coupled to the error edge connection whereby the module controller ~~is configured to output outputs~~ to the memory controller a signal indicating a parity error having occurred during the one or more memory ~~read or write read, write, pre-charge, or refresh~~ operations;

wherein the module controller is further configured to ~~process one or more training sequences while the memory module is not performing any memory read, write, pre-charge, or refresh operation, and wherein the module controller is further configured to drive~~ a notification signal associated with ~~the one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection while the memory module is not performing any memory read or write operation.~~

36. (Currently Amended) The memory module of claim 35, wherein the module controller comprises ~~an one or more~~ integrated circuit.

37. (Previously Presented) The memory module of claim 35, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.

38. (Previously Presented) The memory module of claim 37, wherein the notification circuit generates the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.

39. (Previously Presented) The memory module of claim 38, wherein the notification circuit drives the signal indicating the parity error by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.

40. (Previously Presented) The memory module of claim 38, wherein the notification circuit drives the notification signal using one or more OR logic elements.

41. (Previously Presented) The memory module of claim 35, wherein the one or more training sequences are initiated by the memory controller.

42. (Currently Amended) The memory module of claim 35, wherein the module controller ~~is configured to drive the notification signal to indicate a status of processes~~ the one or more training sequences ~~to in response to a command received from the memory controller of the host system via the second edge connections.~~

REMARKS

This amendment responds to the Final Office Action dated November 25, 2016.

In the Office Action, the Examiner:

- rejected claims 21-42 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Moshayedi US 20100202240 (hereafter “Moshayedi”) in view of Fahr US 20080256281 (hereafter “Fahr”).

Claims 21-22, 28-29, 34-36, and 42 are amended. Support for the amendments can be found throughout the Specification (e.g., paragraphs [0011], [0012], [0021], and [0025]). Thus, no new matter is added.

Claim 21 as amended recites a memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

dynamic random access memory elements configured to communicate data signals with the memory controller via the first edge connections;

a module controller coupled to the dynamic random access memory elements, wherein the module controller is configured to receive from the memory controller via the second edge connections address and command signals associated with one or more memory read or write operations and to control the memory elements in accordance with the address and command signals, the module controller having an open drain output coupled to the error edge connection whereby the module controller is configured to output to the memory controller a signal indicating a parity error having occurred during the one or more memory read or write operations;

wherein the module controller is further configured to drive a notification signal associated with one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection, wherein the one or more training sequences are not associated with any memory read or write operation.

As recited, the memory module in claim 21 as amended comprises a module controller configured to control the memory elements during one or more memory read or write operations in accordance with address and command signals associated with the

one or more read or write operations from a memory controller of a host system. The module controller has an open drain output whereby the module controller is configured to output to the memory controller a signal indicating a parity error having occurred during one or more memory read or write operations. The module controller is then further configured to drive a notification signal associated with one or more training sequences that are not associated with any memory read or write operation to the memory controller via the *same* open drain output.

In rejecting claim 21, the Examiner refers to multiple paragraphs in Moshayedi as disclosing the various elements in claim 21 without any explanation or reasoning. For example, the Examiner cites Moshayedi [¶0027, 0033, 0047, 0059, 0060, 0066] as disclosing “the module controller having an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error having occurred during the one or more memory read or write operations,” without pointing out where the open drain output is in Moshayedi and which signal in Moshayedi corresponds to the “signal indicating a parity error.”

Thus, the Applicant is left to guess what the Examiner’s rationale is in rejecting claim 21 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Moshayedi in view of Fahr. The Examiner seems to consider the non-volatile controller 110 in Moshayedi as corresponding to the module controller in claim 21. As shown in Moshayedi FIG. 1, the non-volatile controller 110 is shown to have several outputs: CACHE_DIRTY, DRAM_AVAILABLE, NVDIMM_READY, TEST_TX, and VBACK_RESET. So, the question is, which of these outputs the Examiner considers to correspond to the “open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error having occurred during the one or more memory read, write, pre-charge, or refresh operations?”

As described in Moshayedi ¶0037, the “CACHE_DIRTY signal indicates that flash memory 130 contains a data image of DRAM 120.” “During the BACKUP state, the CACHE_DIRTY signal indicates the start of the backup process. During POWER UP state, the CACHE_DIRTY indicates that flash memory 130 contains a backup

image.” Therefore, the CACHE_DIRTY output cannot be “an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error having occurred during the one or more memory operations.”

As described in Mosheyedi ¶0038, the “DRAM_AVAILABLE signal indicates when the system can access DRAM 120.” “When DRAM_AVAILABLE is low, controller 110 has control of DRAM 120. When the signal is high, the system can take the DRAM devices (e.g., 121-122) out of self-refresh and access the data.” Therefore, the DRAM_AVAILABLE output cannot be “an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error having occurred during the one or more memory operations.”

As described in Mosheyedi ¶0039, the “NVDIMM_READY signal indicates that module 100 is capable of handling a power-loss event.” “During normal system operation (idle state), the system cannot assert NVCACHE_ENABLE until NVDIMM_READY is asserted. During backup operation, NVDIMM_READY is deasserted. During restore operation, NVDIMM_READY is deasserted. If controller 110 determines at any time that a power loss event cannot be handled correctly, for example, if the EDL capacitor bank failed a self-test operation, controller 110 deasserts the NVDIMM_READY to notify the system to move any cache data from the DIMM memory (e.g., to move the data to permanent storage such as a hard drive of the system).” Therefore, the NVDIMM_READY output cannot be “an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error having occurred during the one or more memory operations.”

As described in Mosheyedi ¶0044, “Signals TEST_RX and TEST_TX make up a production test interface that is a 57.6Kbaud serial link.” “During normal system operation, the test signals are tristated and floating.” Therefore, the TEST_TX output cannot be “an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error having occurred during the one or more memory operations.”

As described in Mosheyedi ¶0043, “Module 100 also includes a third I2C interface that is located between controller 110 and backup power source 200 (the “backup power supply I2C interface”).” “The backup power supply I2C interface allows controller 110 to communicate with the external backup power supply module using VBACK_SDA and VBACK_SCL... The backup power supply reset (VBACK_RESET) allows controller 110 to reset the external backup power supply module.”).” Therefore, the VBACK_RESET output cannot be “an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error having occurred during the one or more memory operations.”

Furthermore, Moshayedi ¶0027 cited by the Examiner does not describe any output to the memory controller either. Also, Moshayedi ¶0033 cited by the Examiner describes the functions of NVDIMM_PG and NVCACHE_ENABLE, which are inputs, instead of outputs to the non-volatile control 110. Therefore, neither NVDIMM_PG nor NVCACHE_ENABLE can be “an open drain output” recited in claim 21.

Careful reading of the other paragraphs cited by the Examiner (i.e., ¶0047, 0059, 0060, 0066) with regard to this claim element also does not shed any light as to where in Moshayedi it is disclosed “an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error having occurred during the one or more memory operations.”

In fact, Moshayedi is about a flash-backed dual in-line memory module (DIMM) 100 including a nonvolatile memory 130, a volatile memory 120, and a nonvolatile memory control 110 whose main function is to control the data flow between the non-volatile memory and the volatile memory during data backup and restore in case of power failure. (See Moshayedi ¶0004, 0005, 0016) As described in Moshayedi ¶0027 cited by the Examiner, when “controller 110 controls DRAM 120, **the register is isolated from the edge connector using FET bus switches 163 and controller 110 can directly drive the register inputs.**” (*Emphasis added*) Therefore, unlike what is claimed in claim 21, the controller 110 in Moshayedi is not “configured to receive from the memory controller

via the second edge connections address and command signals associated with one or more memory operations and to control the memory elements in accordance with the address and command signals.”

Furthermore, as described in Moshayedi ¶0027, when “**the system controls the DRAM array, the FET bus switches 163 are on and the FPGA (i.e., the controller 110) tristates its outputs.**” (*Emphasis added*) Therefore, the controller 110 in Moshayedi is decoupled from the DRAM array 120 when the DRAM array is performing read/write operations in accordance with the address and command signals from the system. Thus, the controller 110 in Moshayedi cannot possibly “control the memory elements in accordance with the address and command signals” received from the system, as required by claim 21, or act on any parity error that occurs during memory operations.

The Examiner further cites Moshayedi [¶0066, 0084, 0027, 0033, 0047] as disclosing “wherein the module controller is further configured to process one or more training sequences unrelated to any memory operation, and wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection,” without stating what the Examiner considers as the training sequences and what signal can be regarded as the “notification signal associated with the one or more training sequences.”

Moshayedi ¶0066 is about power transistors “responsible for moving the DRAM devices to the backup power and isolating the backup power from the system VDD and V3P_AUX.” Moshayedi ¶0084 discusses variations of different components in the system shown in FIG. 1 of Moshayedi. Moshayedi ¶0027 discusses the flash-backed dual in-line memory module (DIMM) 100 in general. Moshayedi ¶0033 describes NVDIMM_PG signal, which “reports the state of the power in the user system.” Moshayedi ¶0047 describes transitions to and from GLITCH state, which “signifies a case in which the system temporarily lost power, but power has returned before the backup operation completed thus allowing the user to retrieve the DRAM contents without using the flash data.” (See Moshayedi ¶0049)

Therefore, these paragraphs cited by the Examiner do not even come close to disclosing or teaching “wherein the module controller is further configured to process one or more training sequences unrelated to any memory operation, and wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection.”

Fahr does not make up for the deficiency of Moshayedi. The Examiner cites Fahr ¶0067 as disclosing two open-drain outputs to permit multiple modules to share a common signal line. But, claim 21 does not just recite an open drain output, it recites a memory module including, among other things, a module controller having an open-drain output. It further includes the limitations that the module controller “outputs to the memory controller a signal indicating a parity error” AND “is further configured to drive a notification signal associated with the one or more training sequences to the memory controller” *via the same open-drain output*.

Fahr, on the other, describes an ECC/Parity register on a DIMM using two open-drain outputs for two different error signals, /Error (CE) 120 and /Error (UE) 121, respectively (Fahr [0067]. Neither of these open drain output is used to output to the memory controller “a signal indicating a parity error” AND “a notification signal associated with the one or more training sequences to the memory controller.”

Therefore, claim 21 as amended is patentable over Moshayedi in view of Fahr.

Claim 22 as amended, claims 23-27, and claim 28 as amended depend from claim 21 as amended. Therefore, claim 22 as amended, claims 23-27, and claim 28 are patentable for at least the same reasons claim 21 as amended is patentable.

The arguments regarding claim 21 as amended apply to claim 29 as amended. Therefore, claim 29 as amended is also patentable.

Claims 30-33 and claim 34 as amended depend from claim 29 as amended. Therefore, claims 30-33 and claim 34 as amended are patentable for at least the same reasons claim 29 as amended is patentable.

The arguments regarding claim 21 as amended apply to claim 35 as amended. Therefore, claim 35 as amended is also patentable.

Claim 36 as amended, claims 37-41, and claim 42 as amended depend from claim 35 as amended. Therefore, claim 36 as amended, claims 37-41, and claim 42 as amended are patentable for at least the same reasons claim 35 as amended is patentable.

Applicant submits that claims 21-42 are in condition for allowance and respectfully requests such action. The Examiner is invited to call the undersigned at (650) 521-4828 to discuss any remaining issues.

Respectfully submitted,

Date: May 25, 2017

/Jamie J. Zheng/

51167

Jamie J. Zheng
Customer No. 79141

(Reg. No.)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 15/088,115		Filing Date 04/01/2016		☐ To be Mailed		
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO											
APPLICATION AS FILED – PART I											
(Column 1)			(Column 2)								
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A		N/A		N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A					
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		X \$ =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		X \$ =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))											
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL					
APPLICATION AS AMENDED – PART II											
(Column 1)			(Column 2)			(Column 3)					
AMENDMENT	05/25/2017		CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))		* 22		Minus	** 22	= 0		X \$80 =		0
	Independent (37 CFR 1.16(h))		* 3		Minus	***3	= 0		X \$420 =		0
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE		0			
(Column 1)			(Column 2)			(Column 3)					
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))		*		Minus	**	=		X \$ =		
	Independent (37 CFR 1.16(h))		*		Minus	***	=		X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE					
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.											

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/088,115	04/01/2016	Hyun Lee	N3044.10014US04	7163
79141	7590	05/31/2017	EXAMINER	
Jamie J. Zheng, Ph.D Esq. MASCHOFF BRENNAN 1389 Center Drive Suite 300 Park City, UT 84098			CHERY, MARDOCHEE	
			ART UNIT	PAPER NUMBER
			2133	
			NOTIFICATION DATE	DELIVERY MODE
			05/31/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

d@mabr.com

<i>Applicant-Initiated Interview Summary</i>	Application No.	Applicant(s)	
	15/088,115	LEE, HYUN	
	Examiner	Art Unit	
	Mardochee CHERY	2133	

All participants (applicant, applicant's representative, PTO personnel):

(1) Mardochee CHERY. (3) ____.

(2) Jamie J. Zheng (Reg. No. 51167). (4) ____.

Date of Interview: 24 May 2017.

Type: ☒ Telephonic ☐ Video Conference
 ☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
 If Yes, brief description: ____.

Issues Discussed ☐101 ☐112 ☐102 ☒103 ☐Others
 (For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 21.

Identification of prior art discussed: Moshayedi (20100202240); Fahr (20080256281).

Substance of Interview
 (For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Applicant's representative and the examiner discussed the AFCP 2.0 filed 04/25/17 and potential claim amendments to overcome the art of record.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/Mardochee CHERY/ Primary Examiner, Art Unit 2133	5/24/17
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Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record

A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews

Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.

All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:

- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

- 1) A brief description of the nature of any exhibit shown or any demonstration conducted,
- 2) an identification of the claims discussed,
- 3) an identification of the specific prior art discussed,
- 4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
- 5) a brief identification of the general thrust of the principal arguments presented to the examiner,
(The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
- 6) a general indication of any other pertinent matters discussed, and
- 7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/088,115	04/01/2016	Hyun Lee	N3044.10014US04	7163
79141	7590	06/16/2017	EXAMINER	
Jamie J. Zheng, Ph.D Esq. MASCHOFF BRENNAN 1389 Center Drive Suite 300 Park City, UT 84098			CHERY, MARDOCHEE	
			ART UNIT	PAPER NUMBER
			2133	
			NOTIFICATION DATE	DELIVERY MODE
			06/16/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

d@mabr.com

Office Action Summary	Application No. 15/088,115	Applicant(s) LEE, HYUN	
	Examiner Mardochee CHERY	Art Unit 2133	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 5/25/17.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 21-42 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 21-42 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 4) ☐ Other: ____.

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

(a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 21-42 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention. In particular, the newly added limitations to claims 21, 29, and 35, “wherein the one or more training sequences are not associated with any memory read or write operation”, “while the memory module is not performing any memory read or write operation”, “while the memory module is not performing any memory read or write operation”, respectively, are not supported by the original

disclosure and constitute new matter. Consequently, these limitations are not entitled to the earliest filing date of the parent application.

Claim Rejections - 35 USC § 103

4. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

5. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 21-42 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Moshayedi (US 20100202240 A1) and Fahr (US 20080256281 A1) and Goishi (US 20100142383 A1).

As per claim 21, Moshayedi discloses a memory module operable with a memory controller of a host system, comprising: a printed circuit board having edge connections that fit into a corresponding slot of a host system, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections [¶0026, 0027, 0060]; dynamic random access memory elements configured to communicate data signals with the memory controller via the first edge connections [¶0027]; a module controller coupled to the dynamic random access memory elements, wherein the module controller is configured to receive from the memory controller via the second edge connections address and command signals associated with one or more memory read or write operations and to control the memory elements in accordance with the address and command signals [¶0032, 0055], the module controller having an open drain output coupled to the error edge connection whereby the module controller is configured to output to the memory controller a signal indicating a parity error having occurred during the one or more memory read or write operations [¶0027, 0033, 0047, 0059, 0060, 0066]; wherein the module controller is further configured to drive a notification signal associated with one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection [¶0066, 0084, 0027, 0033, 0047].

Fahr discloses two open-drain outputs are available to permit multiple modules to share a common signal line [¶0067].

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant to drive a notification signal via an open drain output in order to permit external monitoring of the memory operation.

Goishi discloses wherein the one or more training sequences are not associated with any memory read or write operation [¶0039: *data storing section storing predetermined individual data that is unrelated to the executed test program*].

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant, to have one or more training sequences being not associated with any memory read or write operation in order to provide a test apparatus and method capable of overcoming generation of complicated test pattern that includes redundant data.

As per claim 22, Moshayedi discloses the memory module of claim 21, wherein the module controller comprises an integrated circuit [Figs. 6A-6B].

As per claim 23, Fahr discloses the memory module of claim 21, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output [¶0067].

As per claim 24, Moshayedi discloses the memory module of claim 23, wherein the notification circuit drives the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground [Figs. 7A-7B].

As per claim 25, Moshayedi discloses the memory module of claim 24, wherein the notification circuit drives the signal indicating the parity error by driving the gate of each of the

one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground [Figs. 7A-7B].

As per claim 26, Moshayedi discloses the memory module of claim 24, wherein the notification circuit drives the notification signal using one or more OR logic elements [Figs. 7A-7B].

As per claim 27, Moshayedi discloses the memory module of claim 21, wherein the one or more training sequences are initiated by the memory controller [Fig. 5].

As per claim 28, Moshayedi discloses the memory module of claim 21, wherein the module controller is configured to drive the notification signal to indicate a status of the one or more training sequences to the memory controller [Fig. 5].

As per claims 29-42, the rationale in the rejection of claims 21-28 is herein incorporated.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee CHERY whose telephone number is (571)272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jared Ian Rutz can be reached on (571)272-5535. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

June 12, 2017

/Mardochee CHERY/
Primary Examiner, Art Unit 2133

Notice of References Cited	Application/Control No. 15/088,115	Applicant(s)/Patent Under Reexamination LEE, HYUN	
	Examiner Mardochee CHERY	Art Unit 2133	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2010/0142383 A1	06-2010	GOISHI; MASARU	H04L43/50	370/250
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 15088115	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	11/14/2016	06/12/2017						
	1	-	-						
	2	-	-						
	3	-	-						
	4	-	-						
	5	-	-						
	6	-	-						
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	18	-	-						
	19	-	-						
	20	-	-						
	21	✓	✓						
	22	✓	✓						
	23	✓	✓						
	24	✓	✓						
	25	✓	✓						
	26	✓	✓						
	27	✓	✓						
	28	✓	✓						
	29	✓	✓						
	30	✓	✓						
	31	✓	✓						
	32	✓	✓						
	33	✓	✓						
	34	✓	✓						
	35	✓	✓						
	36	✓	✓						

<i>Index of Claims</i> 	Application/Control No. 15088115	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA				☐ T.D.				☐ R.1.47			
CLAIM		DATE													
Final	Original	11/14/2016	06/12/2017												
	37	✓	✓												
	38	✓	✓												
	39	✓	✓												
	40	✓	✓												
	41	✓	✓												
	42	✓	✓												

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	9	(train\$3 test\$3 initializ\$5 calibrat\$3 manufactur\$3 fabricat\$3) near7 (pattern sequence code data metadata input value parameter) with (("not") near3 (associat\$3 relat\$3) unrelat\$3 un-relat\$3 unassociat\$3 un-associat\$3) near5 (read\$3 writ\$4 access\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 16:55
L2	19	(train\$3 test\$3 initializ\$5 calibrat\$3 manufactur\$3 fabricat\$3) near7 (pattern sequence code data metadata input value parameter) with (("not") near3 (associat\$3 relat\$3) unrelat\$3 un-relat\$3 unassociat\$3 un-associat\$3) near7 (read\$3 writ\$4 access\$3 stored storing stores ((memory storage) near3 (operation)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 16:55
L3	10	L2 not L1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 16:55
L4	6	L3 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 16:55
L5	0	L4 and (memory storage) near2 (module volume device) near3 ("not") near3 (read\$3 writ\$4 access\$3 perform\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 16:55
L6	0	L2 and (memory storage) near2 (module volume device) near3 ("not") near3 (read\$3 writ\$4 access\$3 perform\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 16:57
L7	50	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 16:58

L8	31	L7 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 16:58
L9	4	(train\$3 test\$3 initializ\$5) near5 (pattern sequence code data) near5 (("not") near3 (associat\$3 relat\$3) unrelat\$3 un-relat\$3 unassociat\$3 un-associat\$3) near5 (read\$3 writ\$4 access\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 16:58
L10	4	L9 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 16:58
L11	8	(train\$3 test\$3 initializ\$5 calibrat\$3 manufactur\$3 fabricat\$3) near7 (pattern sequence code data) with (("not") near3 (associat\$3 relat\$3) unrelat\$3 un-relat\$3 unassociat\$3 un-associat\$3) near5 (read\$3 writ\$4 access\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 16:58
L12	4	L11 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 16:58
L13	35	L8 L10 L12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 16:58
L14	0	L13 and (memory storage) near2 (module volume device) near3 ("not") near3 (read\$3 writ\$4 access\$3 perform\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 17:02
L15	0	(memory storage) near2 (module volume device) near3 ("not") near3 (read\$3 writ\$4 access\$3 perform\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 17:05
L16	0	(memory storage) near2 (module volume device) near3 ("not") near3 (read\$3 writ\$4 access\$3 (perform\$3 near3 (read\$3 writ\$4)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2017/06/12 17:07

			DERWENT; IBM_TDB			
L17	4	(memory storage) near2 (apparatus module volume device) near5 ("not") near3 (read\$3 writ\$4 access\$3 stor\$3 (perform\$3 near3 (read\$3 writ\$4)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 17:07
L18	3	L17 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 17:08
L19	112	(memory storage) near3 (apparatus module volume device) near5 ("not" "don't") near3 (read\$3 writ\$4 access\$3 stor\$3 (perform\$3 near3 (read\$3 writ\$4)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 17:15
L20	0	(memory storage) near3 (apparatus module volume device) near5 ("not" "don't") near3 (read\$3 writ\$4 access\$3 stor\$3 (perform\$3 near3 (read\$3 writ\$4))) with (memory storage) near2 controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 17:31
L21	0	(memory storage) near3 (apparatus module volume device) near5 ("not" "don't") near3 (read\$3 writ\$4 access\$3 stor\$3 (perform\$3 near3 (read\$3 writ\$4))) same (memory storage) near2 controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 17:31
L22	2	(memory storage) near3 (apparatus module volume device) near5 ("not" "don't") near3 (read\$3 writ\$4 access\$3 stor\$3 (perform\$3 near3 (read\$3 writ\$4))) same (memory storage) near3 controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 17:32
L23	2	(train\$3 test\$3 initializ\$5 calibrat\$3 manufactur\$3 fabricat\$3) near7 (pattern sequence code data metadata input value parameter) with (memory storage) near3 (apparatus module volume device) near5 ("not" "don't") near3 (read\$3 writ\$4 access\$3 stor\$3 (perform\$3 near3 (read\$3 writ\$4)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 17:36
L24	2	(memory storage) near3 (apparatus module volume device) near5 ("not" "don't") near3 (read\$3 writ\$4 access\$3 stor\$3 (perform\$3 near3 (read\$3 writ\$4 access\$3))) same (memory storage) near3 controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 17:56
L25	2	(memory storage module) near3 (apparatus module volume device) near5	US-PGPUB; USPAT;	OR	ON	2017/06/12 18:06

		("not" "don't") near3 (read\$3 writ\$4 access\$3 stor\$3 (perform\$3 near3 (read\$3 writ\$4 access\$3))) same (memory storage) near3 controller	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L26	5	(memory storage module) near5 (apparatus module volume device) near5 ("not" "don't") near5 (read\$3 writ\$4 access\$3 stor\$3 (perform\$3 near3 (read\$3 writ\$4 access\$3))) same (memory storage) near3 controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 18:07
L27	5	(memory storage module) near5 (apparatus module volume device) near5 ("not" "don't") near5 (read\$3 writ\$4 access\$3 stor\$3 (perform\$3 near3 (read\$3 writ\$4 access\$3))) same (memory storage module volume device) near3 controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 18:08
L28	2	L27 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/12 18:09

6/12/2017 7:08:29 PM

C:\Users\mchery\Documents\EAST\Workspaces\13942721.wsp

Search Notes 	Application/Control No. 15088115	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
711	116	5/16/16	MC
713	1	5/16/16	MC

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Search	5/16/16	MC
EAST Updated Search	6/12/17	MC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/088,115	04/01/2016	Hyun Lee	N3044.10014US04	7163
79141	7590	07/19/2017	EXAMINER	
Jamie J. Zheng, Ph.D Esq. MASCHOFF BRENNAN 1389 Center Drive Suite 300 Park City, UT 84098			CHERY, MARDOCHEE	
			ART UNIT	PAPER NUMBER
			2133	
			NOTIFICATION DATE	DELIVERY MODE
			07/19/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

d@mabr.com

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record

A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews

Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.

All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:

- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

- 1) A brief description of the nature of any exhibit shown or any demonstration conducted,
- 2) an identification of the claims discussed,
- 3) an identification of the specific prior art discussed,
- 4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
- 5) a brief identification of the general thrust of the principal arguments presented to the examiner,
(The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
- 6) a general indication of any other pertinent matters discussed, and
- 7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Netlist, Inc.
App. No. : 15/088,115
Filed : April 1, 2016
For : SYSTEMS AND METHODS
FOR HANDSHAKING WITH A
MEMORY MODULE
Examiner : CHERY, MARDOCHEE
Art Unit : 2133
Conf. No. : 7163
Docket No. : N3044.10014US04

CERTIFICATE OF EFS WEB
TRANSMISSION

I hereby certify that this correspondence and
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transmitted from within the Pacific Time zone
to the Commissioner for Patents via the EFS
Web Server on:

September 18, 2017

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits the following Amendment and remarks in response to the Non-Final Office Action dated June 16, 2017 for the above-identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5394.

AMENDMENTS to the CLAIMS begin on Page 2 of this paper.

REMARKS begin on Page 8 of this paper.

IN THE CLAIMS:

Claims 1-20. (Cancelled)

21. (Currently Amended) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

dynamic random access memory elements on the printed circuit board configured to communicate data signals with the memory controller via the first edge connections;

a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and

wherein the memory module is operable in at least a first mode and a second mode, wherein the memory module in the first mode is configured to be trained with one or more training sequences; wherein the memory module in the second mode is configured to perform one or more memory read or write operations not associated with the one or more training sequences by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections;

wherein the module controller is configured to receive ~~from the memory controller~~ via the second edge connections the address and command signals associated with the one or more memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals, ~~the module controller having an open drain output coupled to the error edge connection whereby and wherein the module controller is further configured to output to the memory controller via the open drain output and the error edge connection~~ a signal indicating a

parity error having occurred while the memory module is in the second mode ~~during the one or more memory read or write operations;~~

wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the error edge connection ~~memory controller~~ via the open drain output while the memory module is in the first mode ~~of the module controller and the error edge connection, wherein the one or more training sequences are not associated with any memory read or write operation.~~

22. (Previously Presented) The memory module of claim 21, wherein the module controller comprises an integrated circuit.

23. (Previously Presented) The memory module of claim 21, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.

24. (Previously Presented) The memory module of claim 23, wherein the notification circuit drives the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.

25. (Previously Presented) The memory module of claim 24, wherein the notification circuit drives the parity error signal by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.

26. (Previously Presented) The memory module of claim 24, wherein the notification circuit drives the notification signal using one or more OR logic elements.

27. (Currently Amended) The memory module of claim 21, wherein the first edge connections are not active while the memory module is trained with the one or more training sequences ~~one or more training sequences are initiated by the memory controller.~~

28. (Currently Amended) The memory module of claim 21, wherein the module controller is configured to drive the notification signal to indicate a status of the one or more training sequences ~~to the memory controller.~~

29. (Currently Amended) A method performed by a memory module operating with a memory controller of the host system, the memory module including dynamic random access memory elements on a printed circuit board, the printed circuit board having edge connections that fit into a corresponding slot of a host system, the edge connections including first edge connections via which the dynamic random access memory devices communicate data with the memory controller, second edge connections via which the memory module receives address and command signals from the memory controller, and an error edge connection in addition to the first edge connections and the second edge connections, the method comprising:

receiving from the memory controller address and command signals associated with one or more memory read or write operations;

controlling the dynamic random access memory elements ~~to perform the one or more memory read or write operations~~ in accordance with the address and command signals;

outputting to the memory controller via an open-drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module ~~during the one or more memory read, write, pre-charge, or refresh operations~~; and

training with one or more training sequences while the first edge connections are not active ~~memory module is not performing any memory read or write operation, and~~ driving a notification signal associated with the one or more training sequences to the memory controller via the open drain output and the error edge connection.

30. (Previously Presented) The method of claim 29, wherein driving the notification signal comprises driving a gate of each of one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground, the one or more transistors each having an open drain coupled to the open drain output.

31. (Previously Presented) The method of claim 30, wherein driving the signal indicating the parity error comprises driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground.

32. (Previously Presented) The method of claim 30, wherein driving the notification signal comprises using one or more OR logic elements.

33. (Currently Amended) The method of claim 29, wherein the memory module is configured to be trained with the one or more training sequences~~are initiated by in response to a request by~~ the memory controller.

34. (Currently Amended) The method of claim 29, wherein the notification signal indicates a status of the one or more training sequences~~to the memory controller of the host system~~.

35. (Currently Amended) A memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and command signals, and an error edge connection in addition to the first edge connections and the second edge connections;

dynamic random access memory elements on the printed circuit board and configurable~~configured~~ to communicate data signals with the memory controller via the first edge connections; and

a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection;

wherein the memory module is configurable to perform at least a first operation and a second operation;

wherein the module controller in the first operation is configured to receive ~~from the memory controller~~ via the second edge connections address and command signals associated with one or more memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals, ~~the module controller having an open drain output coupled to the error edge connection whereby~~ wherein the module controller in the first operation is further configured to output to the memory controller a signal indicating a parity error having occurred in the memory module during the one or more memory read or write operations; and

wherein the memory module in the second operation is configured to be trained with one or more training sequences while the first edge connections are not active, and wherein the module controller in the second operation is ~~further~~ configured to drive a notification signal associated with the one or more training sequences to the error edge connection ~~memory controller via the open drain output of the module controller and the error edge connection while the memory module is not performing any memory read or write operation.~~

36. (Previously Presented) The memory module of claim 35, wherein the module controller comprises an integrated circuit.

37. (Previously Presented) The memory module of claim 35, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.

38. (Previously Presented) The memory module of claim 37, wherein the notification circuit generates the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.

39. (Previously Presented) The memory module of claim 38, wherein the notification circuit drives the signal indicating the parity error by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.

40. (Previously Presented) The memory module of claim 38, wherein the notification circuit drives the notification signal using one or more OR logic elements.

41. (Currently Amended) The memory module of claim 35, wherein the memory module is configured to perform the second operation in response to a command from
~~one or more training sequences are initiated by the memory controller.~~

42. (Currently Amended) The memory module of claim 35, wherein the module controller is configured to drive the notification signal to indicate a status of the one or more training sequences ~~to the memory controller of the host system.~~

REMARKS

This amendment responds to the Non-Final Office Action dated June 16, 2017. In the Office Action, the Examiner:

- rejected claims 21-42 under 35 U.S.C. 112(a) or pre-AIA 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirements;
- rejected claims 21-42 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Moshayedi US 20100202240 (hereafter “Moshayedi”) and Fahr US 20080256281 (hereafter “Fahr”) and Goishi (US 20100142383 A1).

Claim Amendment

Claims 21, 27-29, 33-35, and 41-42 are amended. Support for the amendments can be found throughout the Specification (e.g., paragraphs [0019], [0021]-[0026], and [0032]). Thus, no new matter is added.

Rejection of Claims 21-42 under 35 U.S.C. 112(a) or Pre-AIA 35 U.S.C. 112, First Paragraph

The amendments to the claims address the issues raised by the Examiner. Therefore, the rejection of claims 21-42 under 35 U.S.C. 112(a) or pre-AIA 35 U.S.C. 112, first paragraph, should be withdrawn.

Rejection of Claims 21-42 under Pre-AIA 35 U.S.C. 103(a) as Being Unpatentable over Moshayedi and Fahr and Goishi

Claim 21 as amended recites a memory module operable with a memory controller of a host system, comprising:

a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;

dynamic random access memory elements on the printed circuit board;

a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and

wherein the memory module is operable in at least a first mode and a second mode, wherein the memory module in the first mode is configured to be trained with one or more training sequences; wherein the memory module in the second mode is configured to perform one or more memory read or write operations not associated with the one or more training sequences by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections;

wherein the module controller is configured to receive via the second edge connections the address and command signals associated with the one or more memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals, and wherein the module controller is further configured to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the second mode;

wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output while the memory module is in the first mode.

In rejecting claim 21, the Examiner refers to multiple paragraphs in Moshayedi as disclosing the various elements in claim 21 without any explanation or reasoning. For example, the Examiner cites Moshayedi [¶0027, 0033, 0047, 0059, 0060, 0066] as disclosing “the module controller having an open drain output coupled to the error edge connection” and the module controller being configured to output “a signal indicating a parity error having occurred,” without pointing out where the open drain output is in Moshayedi and which signal in Moshayedi corresponds to the “signal indicating a parity error.”

Thus, the Applicant is left to guess what the Examiner’s rationale is in rejecting claim 21 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Moshayedi in view of Fahr. The Examiner seems to consider the non-volatile controller 110 in Moshayedi as corresponding to the module controller in claim 21. As shown in Moshayedi’s FIG. 1, the non-volatile controller 110 is shown to have several outputs: CACHE_DIRTY,

DRAM_AVAILABLE, NVDIMM_READY, TEST_TX, and VBACK_RESET. So, the question is, which of these outputs the Examiner considers to correspond to the “open drain output,” via which the module controller outputs to the error edge connection “a parity error signal indicating a parity error having occurred” while the memory module is configured to perform one or more memory read or write operations.

As described in Mosheyedi ¶0037, the “CACHE_DIRTY signal indicates that flash memory 130 contains a data image of DRAM 120.” “During the BACKUP state, the CACHE_DIRTY signal indicates the start of the backup process. During POWER UP state, the CACHE_DIRTY indicates that flash memory 130 contains a backup image.” Therefore, the CACHE_DIRTY output cannot be “an open drain output,” via which the module controller outputs to the error edge connection “a parity error signal indicating a parity error having occurred” while the memory module is configured to perform one or more memory read or write operations.

As described in Mosheyedi ¶0038, the “DRAM_AVAILABLE signal indicates when the system can access DRAM 120.” “When DRAM_AVAILABLE is low, controller 110 has control of DRAM 120. When the signal is high, the system can take the DRAM devices (e.g., 121-122) out of self-refresh and access the data.” Therefore, the DRAM_AVAILABLE output cannot be “an open drain output,” via which the module controller outputs to the error edge connection “a parity error signal indicating a parity error having occurred” while the memory module is configured to perform one or more memory read or write operations.

As described in Mosheyedi ¶0039, the “NVDIMM_READY signal indicates that module 100 is capable of handling a power-loss event.” “During normal system operation (idle state), the system cannot assert NVCACHE_ENABLE until NVDIMM_READY is asserted. During backup operation, NVDIMM_READY is deasserted. During restore operation, NDIMM_READY is deasserted. If controller 110 determines at any time that a power loss event cannot be handled correctly, for example, if the EDL capacitor bank failed a self-test operation, controller 110 deasserts the NVDIMM_READY to notify the system to move any cache data from the DIMM memory (e.g., to move the data to

permanent storage such as a hard drive of the system).” Therefore, the NVDIMM_READY output cannot be “an open drain output,” via which the module controller outputs to the error edge connection “a parity error signal indicating a parity error having occurred” while the memory module is configured to perform one or more memory read or write operations.

As described in Mosheyedi ¶0044, “Signals TEST_RX and TEST_TX make up a production test interface that is a 57.6Kbaud serial link.” “During normal system operation, the test signals are tristated and floating.” Therefore, the TEST_TX output cannot be “an open drain output,” via which the module controller outputs to the error edge connection “a parity error signal indicating a parity error having occurred” while the memory module is configured to perform one or more memory read or write operations.

As described in Mosheyedi ¶0043, “Module 100 also includes a third I2C interface that is located between controller 110 and backup power source 200 (the “backup power supply I2C interface”).” “The backup power supply I2C interface allows controller 110 to communicate with the external backup power supply module using VBACK_SDA and VBACK_SCL... The backup power supply reset (VBACK_RESET) allows controller 110 to reset the external backup power supply module.”).” Therefore, the VBACK_RESET output cannot be “an open drain output coupled to the error edge connection whereby the module controller outputs to the memory controller a signal indicating a parity error having occurred” while the memory module is configured to perform one or more memory read or write operations.

Furthermore, Moshayedi ¶0027 cited by the Examiner does not describe any open drain output coupled to an error edge connection. Moshayedi ¶0033 cited by the Examiner describes the functions of NVDIMM_PG and NVCACHE_ENABLE, which are inputs, instead of outputs to the non-volatile control 110. Therefore, neither NVDIMM_PG nor NVCACHE_ENABLE can be “an open drain output” recited in claim 21.

Careful reading of the other paragraphs cited by the Examiner (i.e., ¶0047, 0059, 0060, 0066) with regard to this claim element also does not shed any light as to where in Moshayedi it is disclosed “an open drain output coupled to the error edge connection” and the module controller being configured to output to the error edge connection “a signal indicating a parity error having occurred” while the memory module is configured to perform one or more memory read or write operations.

In fact, Moshayedi is about a flash-backed dual in-line memory module (DIMM) 100 including a nonvolatile memory 130, a volatile memory 120, and a nonvolatile memory control 110 whose main function is to control the data flow between the non-volatile memory and the volatile memory during data backup and restore in case of power failure. (See Moshayedi ¶0004, 0005, 0016) As described in Moshayedi ¶0027 cited by the Examiner, when “controller 110 controls DRAM 120, **the register is isolated from the edge connector using FET bus switches 163 and controller 110 can directly drive the register inputs.**” (*Emphasis added*) Therefore, unlike what is claimed in claim 21, the controller 110 in Moshayedi is not “configured to receive via the second edge connections address and command signals associated with one or more memory operations and to control the memory elements in accordance with the address and command signals.”

Furthermore, as described in Moshayedi ¶0027, when “**the system controls the DRAM array, the FET bus switches 163 are on and the FPGA (i.e., the controller 110) tristates its outputs.**” (*Emphasis added*) Therefore, the controller 110 in Moshayedi is decoupled from the DRAM array 120 when the DRAM array is performing read/write operations in accordance with the address and command signals from the system. Thus, the controller 110 in Moshayedi cannot possibly “control the memory elements in accordance with the address and command signals” received via the second edge connections, as required by claim 21, or act on any parity error that occurs while the memory module is in the second mode.

The Examiner further cites Moshayedi [¶0066, 0084, 0027, 0033, 0047] as disclosing “wherein the module controller is further configured to drive a notification

signal associated with the one or more training sequences” without stating what the Examiner considers as the training sequences and what signal can be regarded as the “notification signal associated with the one or more training sequences.”

Moshayedi ¶0066 is about power transistors “responsible for moving the DRAM devices to the backup power and isolating the backup power from the system VDD and V3P_AUX.” Moshayedi ¶0084 discusses variations of different components in the system shown in FIG. 1 of Moshayedi. Moshayedi ¶0027 discusses the flash-backed dual in-line memory module (DIMM) 100 in general. Moshayedi ¶0033 describes NVDIMM_PG signal, which “reports the state of the power in the user system.” Moshayedi ¶0047 describes transitions to and from GLITCH state, which “signifies a case in which the system temporarily lost power, but power has returned before the backup operation completed thus allowing the user to retrieve the DRAM contents without using the flash data.” (See Moshayedi ¶0049)

Therefore, these paragraphs cited by the Examiner do not even come close to disclosing or teaching “wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences.”

Fahr does not make up for the deficiency of Moshayedi. The Examiner cites Fahr ¶0067 as disclosing two open-drain outputs to permit multiple modules to share a common signal line. But, claim 21 does not just recite an open drain output, it recites a memory module including, among other things, a module controller having an open-drain output. It further includes the limitations that the module controller is configured to output “a signal indicating a parity error having occurred” while the memory module is configured to perform one or more memory read or write operations, AND “to drive a notification signal associated with the one or more training sequences” *via the same open-drain output*.

Fahr, on the other hand, describes an ECC/Parity register on a DIMM using two open-drain outputs for two different error signals, /Error (CE) 120 and /Error (UE) 121, respectively (Fahr [0067]). Neither of these open drain outputs is used to output “a signal

indicating a parity error” AND “a notification signal associated with the one or more training sequences.”

Goishi does not make up for the deficiencies of Moshayedi and Fahr.

Therefore, claim 21 as amended is patentable over Moshayedi and Fahr and Goishi.

Claims 22-26 and claims 27-28 as amended depend from claim 21 as amended. Therefore, claims 22-26 and claims 27-28 as amended are patentable for at least the same reasons claim 21 as amended is patentable.

The arguments regarding claim 21 as amended apply to claim 29 as amended. Therefore, claim 29 as amended is also patentable.

Claims 30-32 and claims 33-34 as amended depend from claim 29 as amended. Therefore, claims 30-32 and claims 33-34 as amended are patentable for at least the same reasons claim 29 as amended is patentable.

The arguments regarding claim 21 as amended apply to claim 35 as amended. Therefore, claim 35 as amended is also patentable.

Claims 36 -40 and claims 41-42 as amended depend from claim 35 as amended. Therefore, claims 36 -40 and claims 41-42 as amended are patentable for at least the same reasons claim 35 as amended is patentable.

Applicant submits that claims 21-42 are in condition for allowance and respectfully requests such action. The Examiner is invited to call the undersigned at (650) 521-4828 to discuss any remaining issues.

Respectfully submitted,

Date: September 18, 2017

/Jamie J. Zheng/

51167

Jamie J. Zheng
Customer No. 79141

(Reg. No.)

Electronic Acknowledgement Receipt	
EFS ID:	30399154
Application Number:	15088115
International Application Number:	
Confirmation Number:	7163
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/Brian Gonzalez
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10014US04
Receipt Date:	18-SEP-2017
Filing Date:	01-APR-2016
Time Stamp:	18:12:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2017-09-18_OA- Response_N3044-10014US04. pdf	563283	yes	14
			a34e337d427e85e757ca27a4a627c312aa8 82570		

	Multipart Description/PDF files in .zip description		
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 15/088,115		Filing Date 04/01/2016		☐ To be Mailed			
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO												
APPLICATION AS FILED – PART I												
(Column 1)			(Column 2)									
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)				
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A						
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))		N/A		N/A		N/A						
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A						
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		X \$ =						
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		X \$ =						
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).										
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))												
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL						
APPLICATION AS AMENDED – PART II												
(Column 1)			(Column 2)			(Column 3)						
AMENDMENT	09/18/2017		CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))		* 22		Minus	** 22	= 0		X \$80 =		0	
	Independent (37 CFR 1.16(h))		* 3		Minus	***3	= 0		X \$420 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))											
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
						TOTAL ADD'L FEE				0		
(Column 1)			(Column 2)			(Column 3)						
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))		*		Minus	**	=		X \$ =			
	Independent (37 CFR 1.16(h))		*		Minus	***	=		X \$ =			
	☐ Application Size Fee (37 CFR 1.16(s))											
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	15088115
	Filing Date	2016-04-01
	First Named Inventor	Hyun Lee
	Art Unit	2133
	Examiner Name	CHERY, MARDOCHEE
	Attorney Docket Number	N3044.10014US04

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		15088115
	Filing Date		2016-04-01
	First Named Inventor	Hyun Lee	
	Art Unit	2133	
	Examiner Name	CHERY, MARDOCHEE	
	Attorney Docket Number	N3044.10014US04	

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2001 – Declaration Of Robert J. Murphy, filed September 6, 2017.	
	2	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2002 – DEPOSITION OF DONALD ALPERT, Ph.D. filed September 6, 2017.	
	3	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2003 – Defendants' Opening Claim Construction Brief filed September 6, 2017.	
	4	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2004 – PLAINTIFF NETLIST, INC.'S OPENING CLAIM CONSTRUCTION BRIEF filed September 6, 2017.	
	5	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2005 – PLAINTIFF NETLIST, INC.'S AMENDED OPENING CLAIM CONSTRUCTION BRIEF filed September 6, 2017.	
	6	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2006 – DEFENDANTS' REPLY CLAIM CONSTRUCTION BRIEF filed September 6, 2017.	
	7	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2006 – DEFENDANTS' REPLY CLAIM CONSTRUCTION BRIEF filed September 6, 2017.	
	8	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2007 – PLAINTIFF NETLIST, INC.'S RESPONSIVE CLAIM CONSTRUCTION BRIEF filed September 6, 2017.	
	9	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2008 – UNITED STATES INTERNATIONAL TRADE COMMISSION Open Sessions filed September 6, 2017.	
	10	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2009 – Computer Desktop Encyclopedia September 6, 2017.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	15088115
	Filing Date	2016-04-01
	First Named Inventor	Hyun Lee
	Art Unit	2133
	Examiner Name	CHERY, MARDOCHEE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	15088115
	Filing Date	2016-04-01
	First Named Inventor	Hyun Lee
	Art Unit	2133
	Examiner Name	CHERY, MARDOCHEE
	Attorney Docket Number	N3044.10014US04

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JAMIE J. ZHENG/	Date (YYYY-MM-DD)	2017-09-25
Name/Print	Jamie J. Zheng	Registration Number	51167

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	30467310
Application Number:	15088115
International Application Number:	
Confirmation Number:	7163
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/Brian Gonzalez
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10014US04
Receipt Date:	25-SEP-2017
Filing Date:	01-APR-2016
Time Stamp:	17:55:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	2017-09-25_IDS_N3044-10014 US04.pdf	1043371 6f954caffc473ae9db7aebaf0cb5578e29e9fdd7	no	5

Warnings:

Information:					
2	Non Patent Literature	IPR2017-00548_Exhibit-2004.pdf	1039719	no	31
			387ddc90da03f67fd24d48f37d345b5f16a5b3e9		
Warnings:					
Information:					
3	Non Patent Literature	IPR2017-00548_Exhibit-2009.PDF	860735	no	3
			c3ba8c6b84c3efc8235165fd7329fb46964798a5		
Warnings:					
Information:					
4	Non Patent Literature	IPR2017-00548_Exhibit-2001.pdf	10647383	no	63
			6c373f0ff90fe401ca63f753ff11a7d8544715e3		
Warnings:					
Information:					
5	Non Patent Literature	IPR2017-00548_Exhibit-2003.pdf	13782885	no	30
			b31420e38d818c9d31a4ac96537d88429d77ba5a		
Warnings:					
Information:					
6	Non Patent Literature	IPR2017-00548_Exhibit-2005.pdf	14995705	no	32
			0ac2925c45fb97fa1843fd1c70b8d9d49d67160c		
Warnings:					
Information:					
7	Non Patent Literature	IPR2017-00548_Exhibit-2006.pdf	14119812	no	31
			bd9a9288de1698f4056f21d2e5329ea647241e40		
Warnings:					
Information:					
8	Non Patent Literature	IPR2017-00548_Exhibit-2007.pdf	332384	no	30
			fdf6341d3c8de4af59900505afb81d42c988c770		
Warnings:					
Information:					

9	Non Patent Literature	IPR2017-00548_Exhibit-2008.pdf	445901 6ab21b96f8f191b906f8c53686489d793683b7a1	no	144
Warnings:					
Information:					
10	Non Patent Literature	IPR2017-00548_Exhibit-2002A.pdf	1495873 37f9ebdc67301d9956cbeeca46d86b1296db9766	no	195
Warnings:					
Information:					
Total Files Size (in bytes):			58763768		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 10/12/2017
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

EXAMINER

CHERY, MARDOCHEE

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 10/12/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/088,115	04/01/2016	Hyun Lee	N3044.10014US04	7163

TITLE OF INVENTION: SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	01/12/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 10/12/2017
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/088,115	04/01/2016	Hyun Lee	N3044.10014US04	7163

TITLE OF INVENTION: SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	01/12/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHERY, MARDOCHEE	2133	711-170000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/088,115	04/01/2016	Hyun Lee	N3044.10014US04	7163
79141 7590 10/12/2017 Jamie J. Zheng, Ph.D Esq. MASCHOFF BRENNAN 1389 Center Drive Suite 300 Park City, UT 84098			EXAMINER CHERY, MARDOCHEE	
			ART UNIT 2133	PAPER NUMBER

DATE MAILED: 10/12/2017

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/088,115	Applicant(s) LEE, HYUN	
	Examiner Mardochee CHERY	Art Unit 2133	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the reply filed 09/18/2017.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 21-42. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>9/25/2017</u>	6. ☐ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	

/Mardochee CHERY/ Primary Examiner, Art Unit 2133	9/28/2017
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Issue Classification 	Application/Control No. 15088115	Applicant(s)/Patent Under Reexamination LEE, HYUN	
	Examiner MARDOCHEE CHERY	Art Unit 2133	

CPC					
Symbol				Type	Version
G06F	13	1694		F	2013-01-01
G06F	13	24		I	2013-01-01
G06F	12	0646		I	2013-01-01
G06F	9	445		I	2013-01-01
G11C	16	26		A	2013-01-01
G11C	5	00		A	2013-01-01
G11C	2029	4402		A	2013-01-01
G11C	29	78		A	2013-01-01
G11C	7	1066		A	2013-01-01

CPC Combination Sets					
Symbol	Type	Set	Ranking	Version	

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	22	
/MARDOCHEE CHERY/ Primary Examiner.Art Unit 2133	9/28/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

Issue Classification 	Application/Control No. 15088115	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION														
CLASS			SUBCLASS			CLAIMED					NON-CLAIMED									
711			170			G	0	6	F	12 / 00 (2006.0)										
CROSS REFERENCE(S)																				
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																			
																</				

NONE		Total Claims Allowed:	
		22	
(Assistant Examiner)	(Date)		
/MARDOCHEE CHERY/ Primary Examiner.Art Unit 2133	9/28/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

Issue Classification 	Application/Control No. 15088115	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
-	1		17	13	33										
-	2	-	18	14	34										
-	3	-	19	15	35										
-	4	-	20	16	36										
-	5	1	21	17	37										
-	6	2	22	18	38										
-	7	3	23	19	39										
-	8	4	24	20	40										
-	9	5	25	21	41										
-	10	6	26	22	42										
-	11	7	27												
-	12	8	28												
-	13	9	29												
-	14	10	30												
-	15	11	31												
-	16	12	32												

NONE		Total Claims Allowed:	
(Assistant Examiner)		22	
(Date)			
/MARDOCHEE CHERY/ Primary Examiner.Art Unit 2133	9/28/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

Search Notes 	Application/Control No. 15088115	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

CPC- SEARCHED		
Symbol	Date	Examiner
G11C5/00; G11C16/26; G11C2029/4402; G11C29/78; G11C7/1066	9/28/2017	MC

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner
G11C5/00; G11C16/26; G11C2029/4402; G11C29/78; G11C7/1066	9/28/2017	MC

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
711	116	5/16/16	MC
713	1	5/16/16	MC

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Search	5/16/16	MC
EAST Updated Search	6/12/17	MC
EAST Updated Search	9/28/17	MC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	See attached	9/28/2017	MC

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Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	15088115
	Filing Date	2016-04-01
	First Named Inventor	Hyun Lee
	Art Unit	2133
	Examiner Name	CHERY, MARDOCHEE
	Attorney Docket Number	N3044.10014US04

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	1	20060262586	A1	2006-11-23	Solomon et al.			
	2	20060062047	A1	2006-03-23	Bhakta et al.			
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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²ⁱ	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T ⁵
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2001 – Declaration Of Robert J. Murphy, filed September 6, 2017.	
	2	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2002 – DEPOSITION OF DONALD ALPERT, Ph.D. filed September 6, 2017.	
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	8	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2007 – PLAINTIFF NETLIST, INC.'S RESPONSIVE CLAIM CONSTRUCTION BRIEF filed September 6, 2017.	
	9	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2008 – UNITED STATES INTERNATIONAL TRADE COMMISSION Open Sessions filed September 6, 2017.	
	10	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2009 – Computer Desktop Encyclopedia September 6, 2017.	

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Application Number	15088115
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Examiner Signature	/MARDOCHEE CHERY/	Date Considered	09/29/2017
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¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

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	Attorney Docket Number	N3044.10014US04

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JAMIE J. ZHENG/	Date (YYYY-MM-DD)	2017-09-25
Name/Print	Jamie J. Zheng	Registration Number	51167

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
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EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	((controller circuit configured cause memory module enter\$3 initialization mode in response command host computer system memory module execut\$3 at least one initialization sequence during initialization mode) and (at least one output\$3 defin\$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output\$3 notification signal indicat\$3 status initialization mode memory controller via least output\$4)).clm.	USPAT	SAME	ON	2017/09/28 16:08

9/ 28/ 2017 4:26:36 PM
C:\ Users\ mchery\ Documents\ EAST\ Workspaces\ 13942721.wsp

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	27512	(controller microcontroller micro-controller) same (memory \$3RAM) with (read write pre-charge\$3 precharge\$3 refresh\$3) and (transistor \$3FET drain\$3) same (controller device microcontroller micro-controller) and drain\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:09
L3	44	2 and edge\$3 near5 (wire port connect\$3 attach\$5 bond\$3 drain source gate pin) same (\$3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:11
L4	0	3 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:12
L5	0	3 and (controller hub switch channel) same (open\$3 near2 drain) same controller with (host computer node engine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:13
L6	23	3 and (open\$3 near2 drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:13
L7	14	6 and @ad<"20090612"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:14
L8	11	6 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/09/28 16:19

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BIB DATA SHEET

CONFIRMATION NO. 7163

SERIAL NUMBER 15/088,115	FILING or 371(c) DATE 04/01/2016 RULE	CLASS 711	GROUP ART UNIT 2133	ATTORNEY DOCKET NO. N3044.10014US04		
APPLICANTS Netlist, Inc., Irvine, CA; INVENTORS Hyun Lee, Ladera Ranch, CA; ** CONTINUING DATA ***** This application is a CON of 13/942,721 07/16/2013 PAT 9311116 which is a CON of 12/815,339 06/14/2010 PAT 8489837 which claims benefit of 61/186,799 06/12/2009 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 04/18/2016						
Foreign Priority claimed ☐ Yes ☒ No	35 USC 119(a-d) conditions met ☐ Yes ☒ No	☐ Met after Allowance	STATE OR COUNTRY CA	SHEETS DRAWINGS 3	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
Verified and /MARDOCHEE CHERY/ Acknowledged Examiner's Signature	Initials					
ADDRESS Jamie J. Zheng, Ph.D Esq. MASCHOFF BRENNAN 1389 Center Drive Suite 300 Park City, UT 84098 UNITED STATES						
TITLE SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE						
FILING FEE RECEIVED 1760	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
15/088,115	04/01/2016	2133	1760	N3044.10014US04	20	3

CONFIRMATION NO. 7163
CORRECTED FILING RECEIPT



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79141

Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

Date Mailed: 10/25/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Hyun Lee, Ladera Ranch, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 13/942,721 07/16/2013 PAT 9311116
which is a CON of 12/815,339 06/14/2010 PAT 8489837
which claims benefit of 61/186,799 06/12/2009

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 04/18/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/088,115**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No
Title

MEMORY MODULE AND METHODS FOR HANDSHAKING WITH A MEMORY CONTROLLER

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)

Approved for use through 07/31/2016. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2001 – Declaration Of Robert J. Murphy, filed September 6, 2017.	
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	15088115
Filing Date	2016-04-01
First Named Inventor	Hyun Lee
Art Unit	2133
Examiner Name	CHERY, MARDOCHEE
Attorney Docket Number	N3044.10014US04

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Examiner Signature	/MARDOCHEE CHERY/	Date Considered	09/29/2017
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See attached certification statement.

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A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JAMIE J. ZHENG/	Date (YYYY-MM-DD)	2017-09-25
Name/Print	Jamie J. Zheng	Registration Number	51167

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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	1	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2001 – Declaration Of Robert J. Murphy, filed September 6, 2017.	
	2	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2002 – DEPOSITION OF DONALD ALPERT, Ph.D. filed September 6, 2017.	
	3	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2003 – Defendants' Opening Claim Construction Brief filed September 6, 2017.	
	4	Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2004 – PLAINTIFF NETLIST, INC.'S OPENING CLAIM CONSTRUCTION BRIEF filed September 6, 2017.	
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Signature	/JAMIE J. ZHENG/	Date (YYYY-MM-DD)	2017-09-25
Name/Print	Jamie J. Zheng	Registration Number	51167

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