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Giovannini et al.

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(54) **METHOD AND APPARATUS FOR CALIBRATING WRITE TIMING IN A MEMORY SYSTEM**

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(51) **Int. Cl.**
G06F 12/00 (2006.01)

(52) **U.S. Cl.** **711/167**; 711/100; 711/154; 711/170

(58) **Field of Classification Search** 711/100, 711/154, 167, 170
See application file for complete search history.

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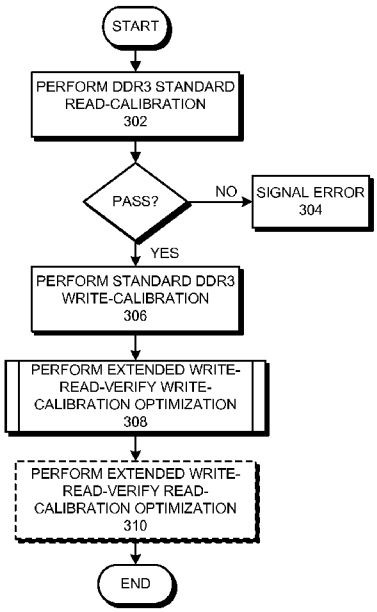
Primary Examiner — Midys Rojas

(57) **ABSTRACT**

A system that calibrates timing relationships between signals involved in performing write operations is described. This system includes a memory controller which is coupled to a set of memory chips, wherein each memory chip includes a phase detector configured to calibrate a phase relationship between a data-strobe signal and a clock signal received at the memory chip from the memory controller during a write operation. Furthermore, the memory controller is configured to perform one or more write-read-validate operations to calibrate a clock-cycle relationship between the data-strobe signal and the clock signal, wherein the write-read-validate operations involve varying a delay on the data-strobe signal relative to the clock signal by a multiple of a clock period.

22 Claims, 12 Drawing Sheets



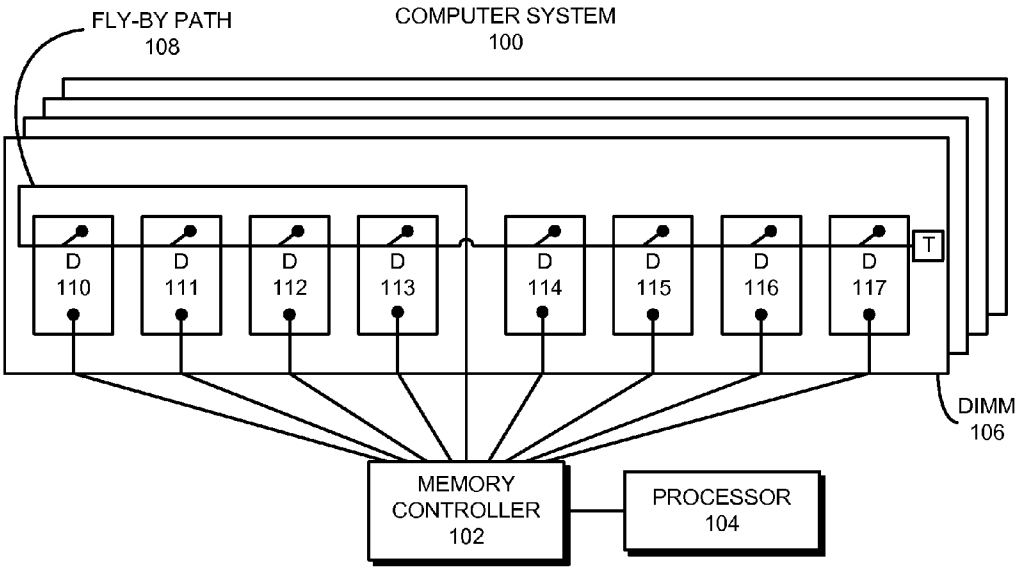

FLY-BY PATH
108
COMPUTER SYSTEM
100
D
110
D
111
D
112
D
113
D
114
D
115
D
116
D
117
T
DIMM
106
MEMORY
CONTROLLER
102
PROCESSOR
104

FIG. 1

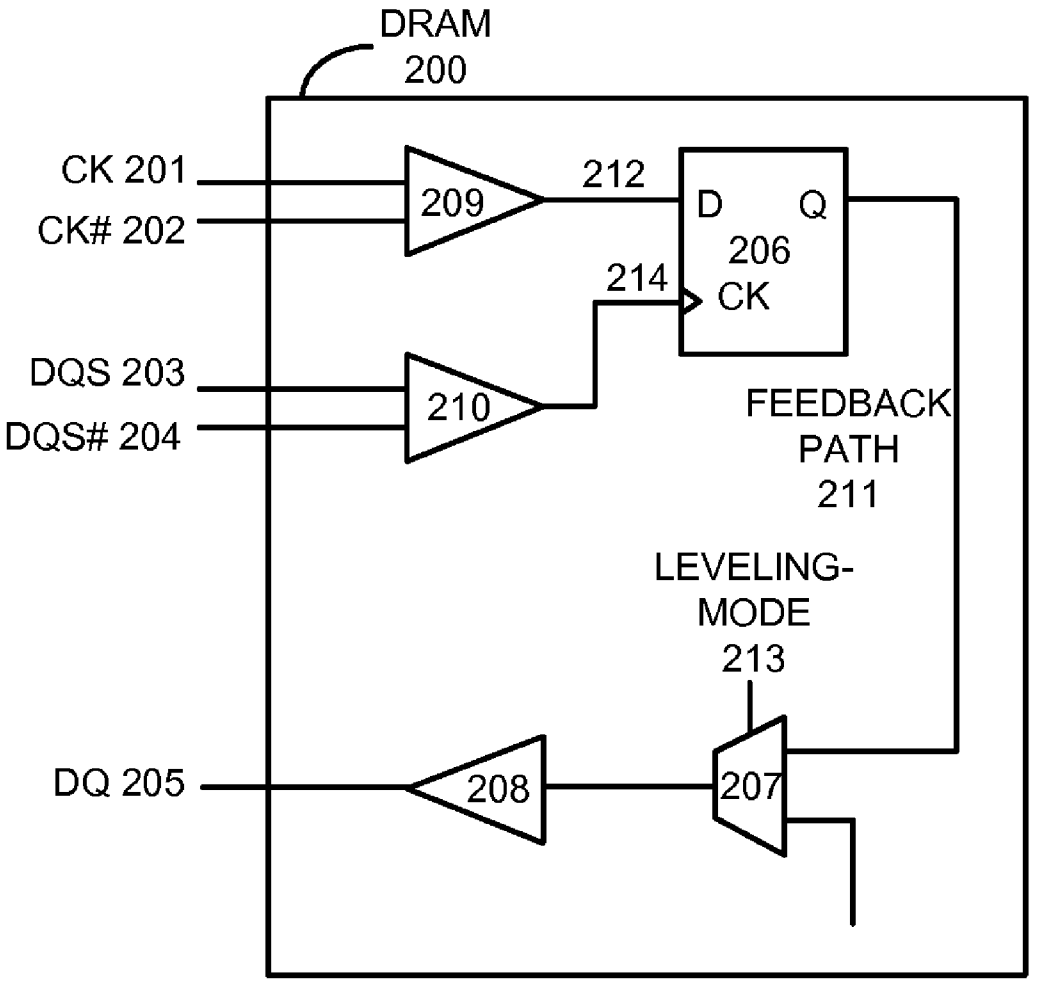

DRAM
200
CK 201
CK# 202
209
212
D
Q
206
214
CK
DQS 203
DQS# 204
210
FEEDBACK
PATH
211
LEVELING-
MODE
213
DQ 205
208
207

FIG. 2

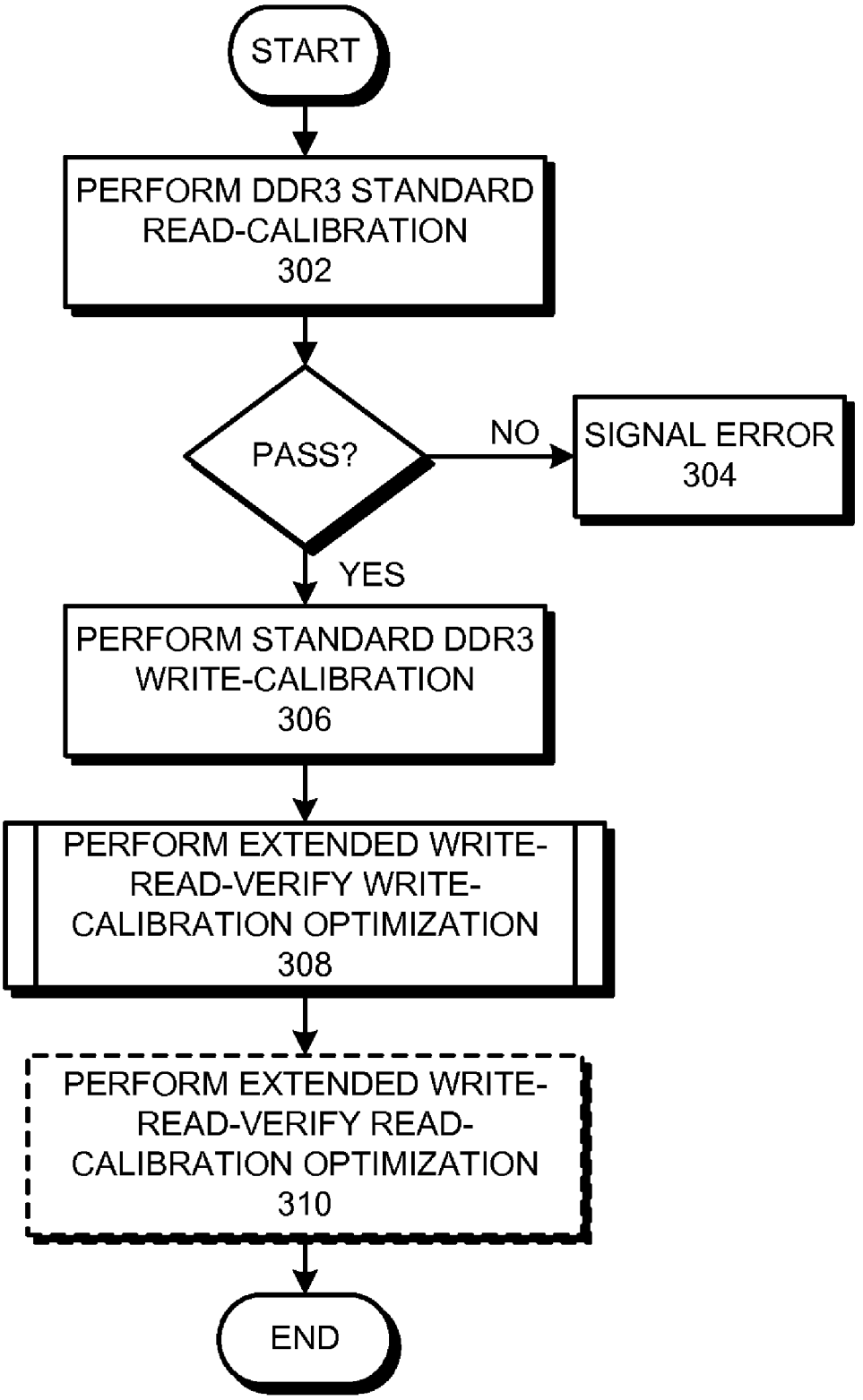

START
PERFORM DDR3 STANDARD READ-CALIBRATION 302
PASS?
NO
SIGNAL ERROR 304
YES
PERFORM STANDARD DDR3 WRITE-CALIBRATION 306
PERFORM EXTENDED WRITE-READ-VERIFY WRITE-CALIBRATION OPTIMIZATION 308
PERFORM EXTENDED WRITE-READ-VERIFY READ-CALIBRATION OPTIMIZATION 310
END

FIG. 3

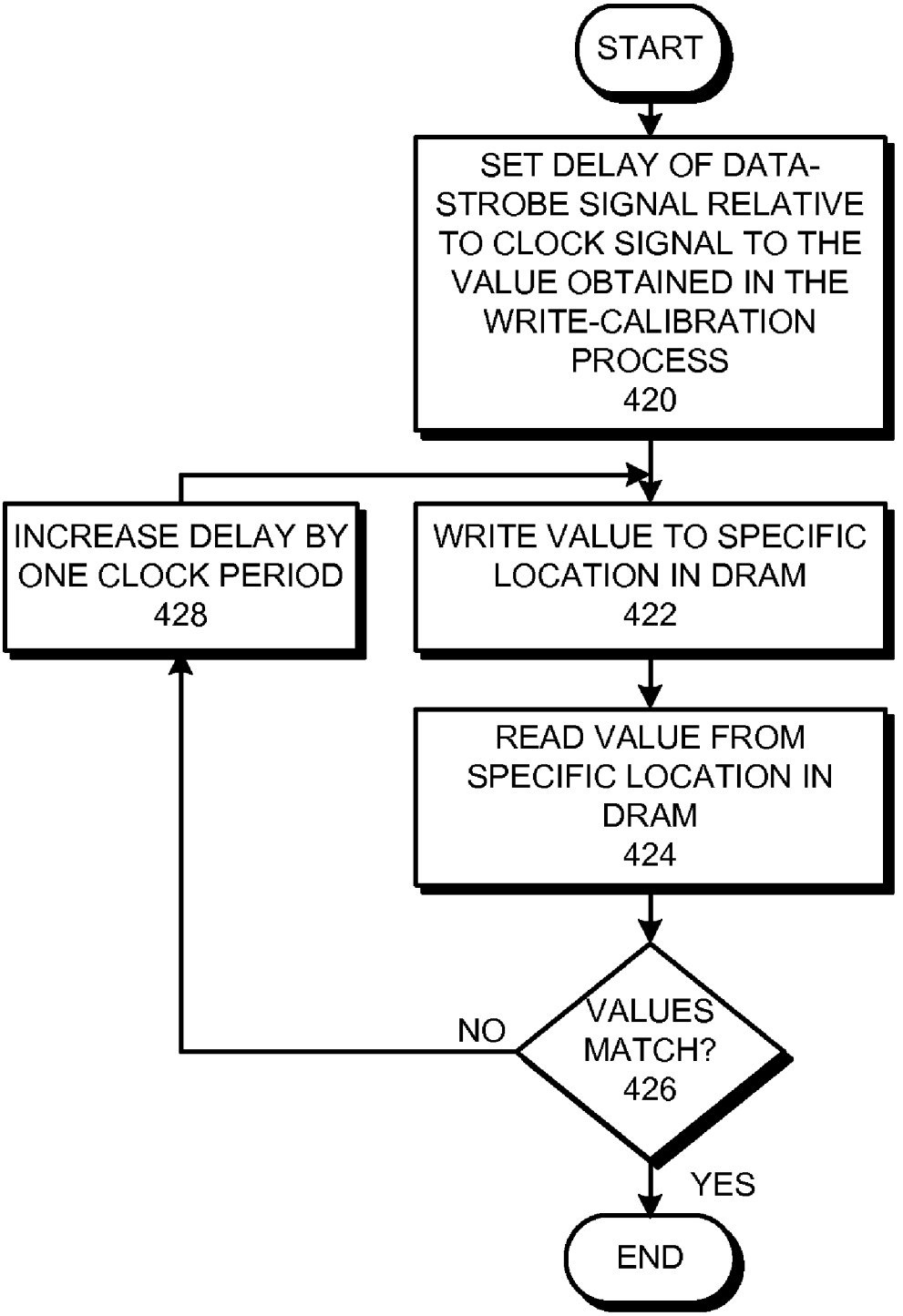

START
SET DELAY OF DATA-STROBE SIGNAL RELATIVE TO CLOCK SIGNAL TO THE VALUE OBTAINED IN THE WRITE-CALIBRATION PROCESS
420
INCREASE DELAY BY ONE CLOCK PERIOD
428
WRITE VALUE TO SPECIFIC LOCATION IN DRAM
422
READ VALUE FROM SPECIFIC LOCATION IN DRAM
424
VALUES MATCH?
426
NO
YES
END

FIG. 4

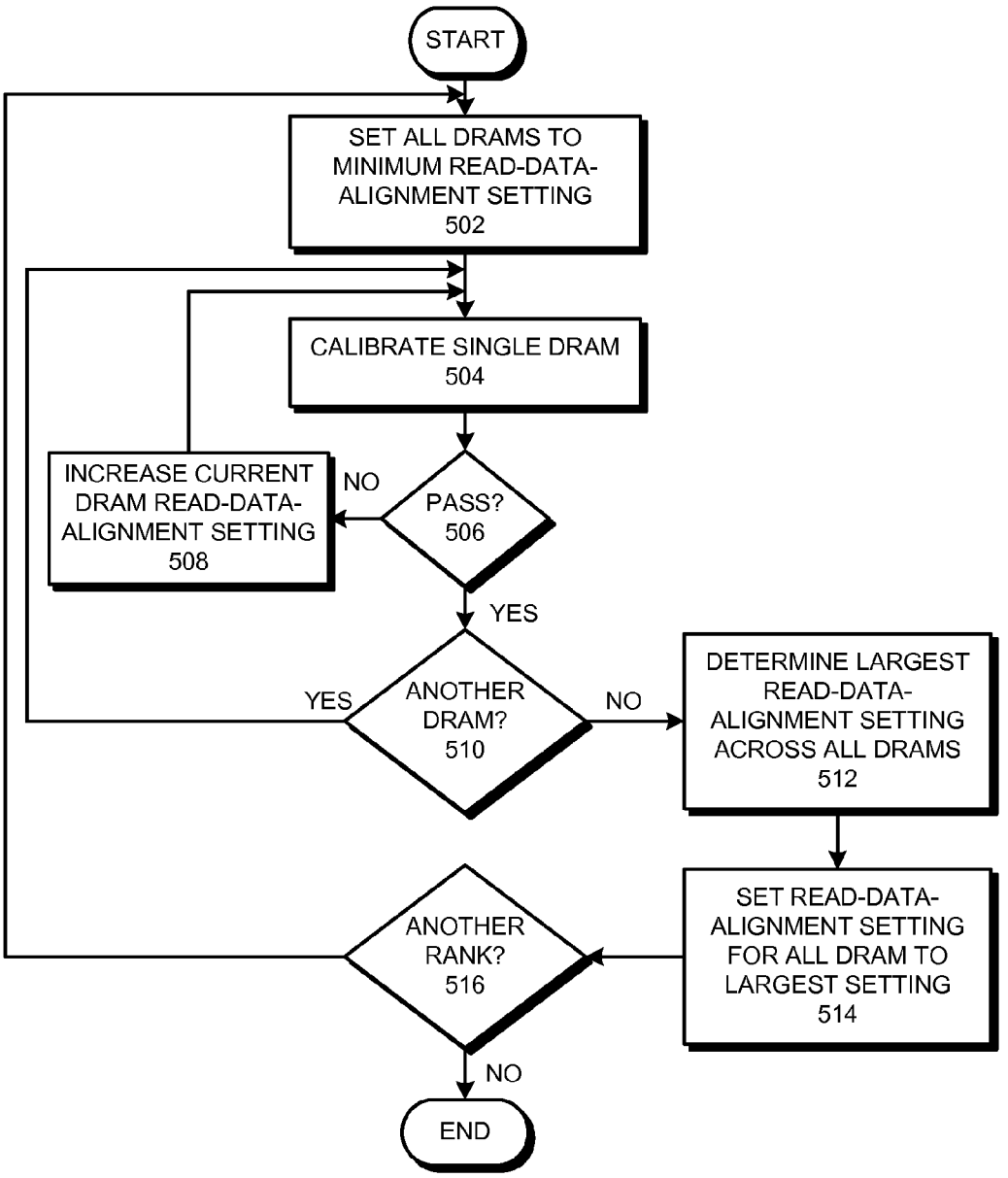

START
SET ALL DRAMS TO MINIMUM READ-DATA-ALIGNMENT SETTING 502
CALIBRATE SINGLE DRAM 504
PASS? 506
NO
INCREASE CURRENT DRAM READ-DATA-ALIGNMENT SETTING 508
YES
ANOTHER DRAM? 510
YES
NO
DETERMINE LARGEST READ-DATA-ALIGNMENT SETTING ACROSS ALL DRAMS 512
SET READ-DATA-ALIGNMENT SETTING FOR ALL DRAM TO LARGEST SETTING 514
ANOTHER RANK? 516
NO
END

FIG. 5

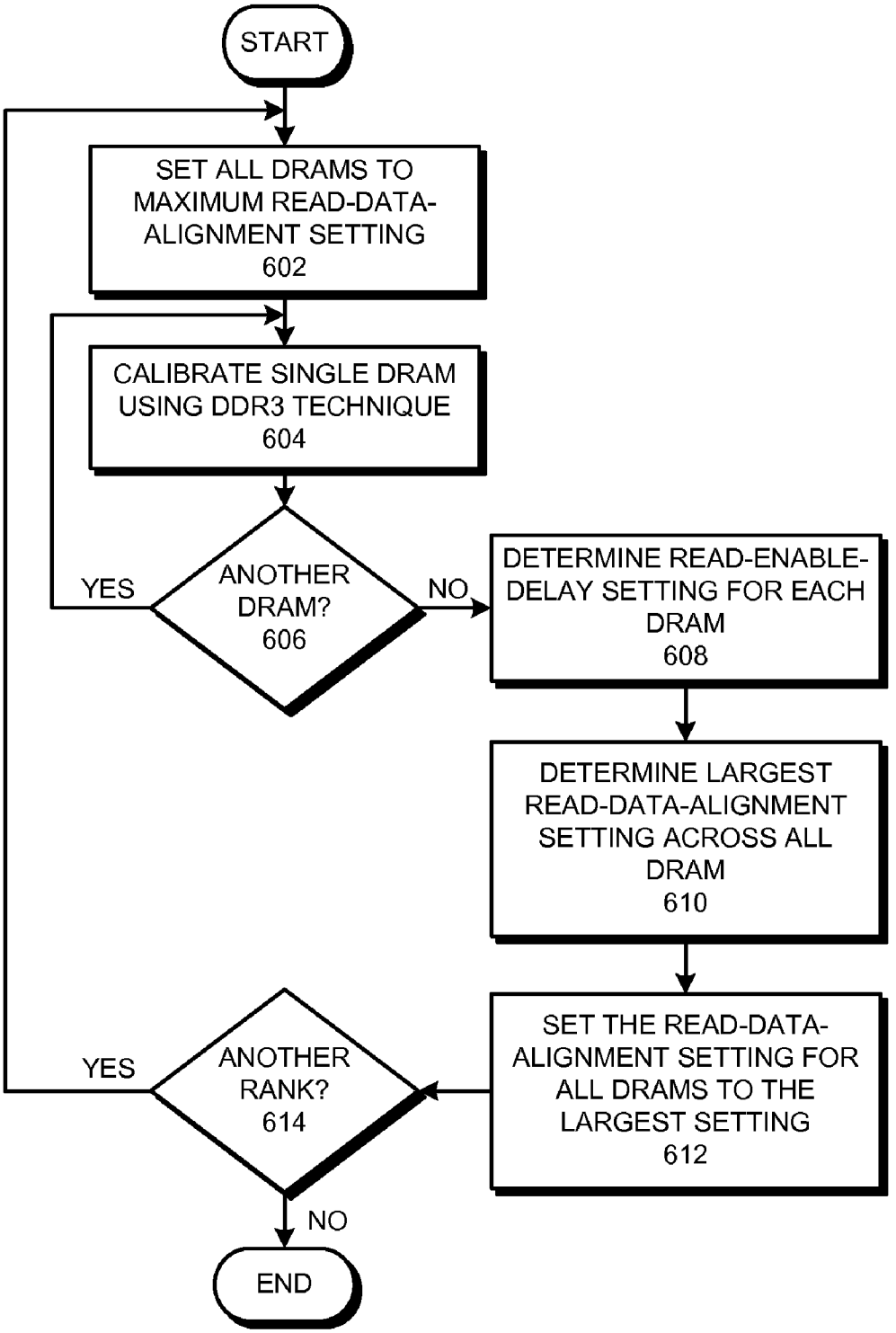

START
SET ALL DRAMS TO MAXIMUM READ-DATA-ALIGNMENT SETTING 602
CALIBRATE SINGLE DRAM USING DDR3 TECHNIQUE 604
ANOTHER DRAM? 606
YES
NO
DETERMINE READ-ENABLE-DELAY SETTING FOR EACH DRAM 608
DETERMINE LARGEST READ-DATA-ALIGNMENT SETTING ACROSS ALL DRAM 610
SET THE READ-DATA-ALIGNMENT SETTING FOR ALL DRAMS TO THE LARGEST SETTING 612
ANOTHER RANK? 614
YES
NO
END

FIG. 6

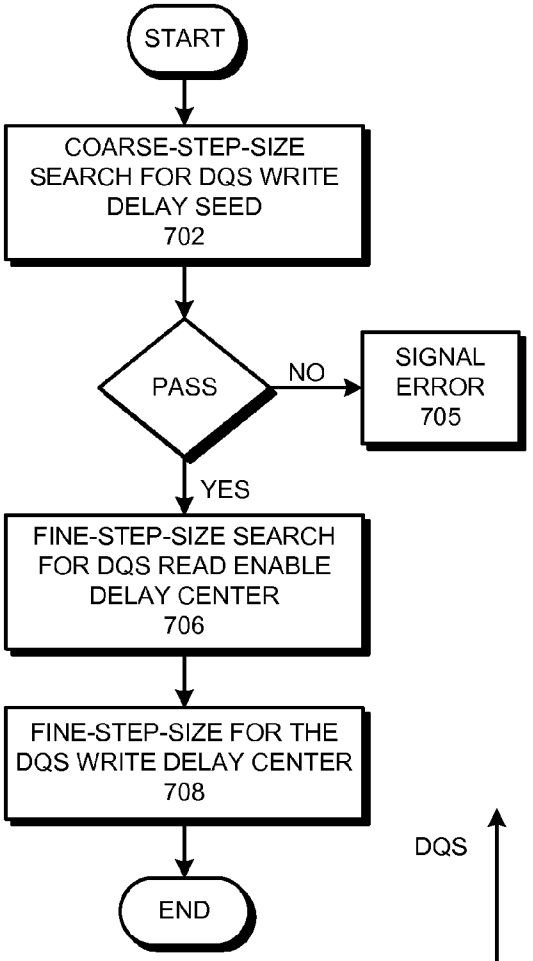

START
COARSE-STEP-SIZE SEARCH FOR DQS WRITE DELAY SEED
702
PASS
NO
SIGNAL ERROR
705
YES
FINE-STEP-SIZE SEARCH FOR DQS READ ENABLE DELAY CENTER
706
FINE-STEP-SIZE FOR THE DQS WRITE DELAY CENTER
708
END

FIG. 7

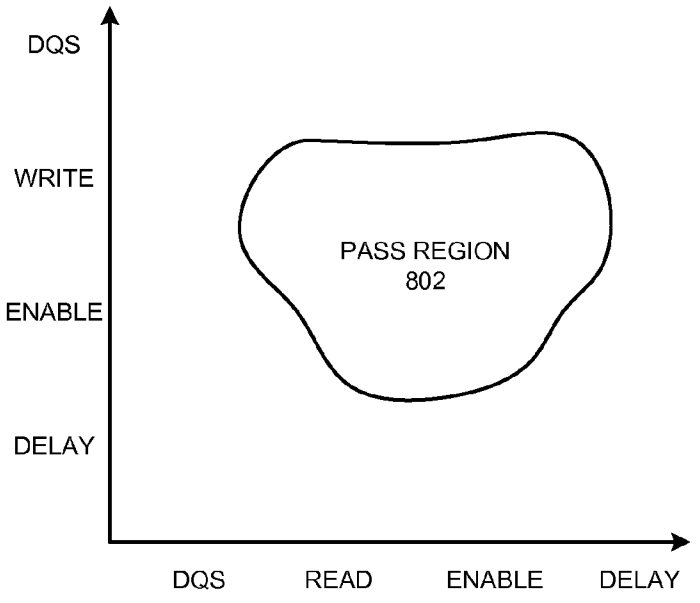

DQS
WRITE
ENABLE
DELAY
PASS REGION
802
DQS
READ
ENABLE
DELAY

FIG. 8

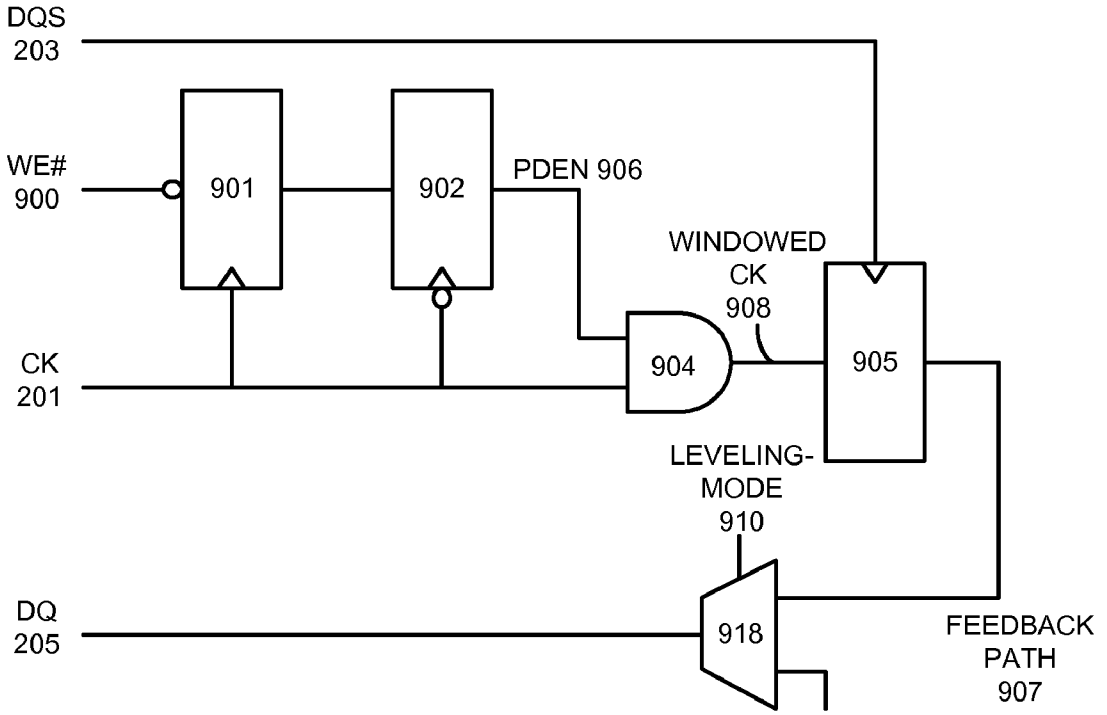

DQS
203
WE#
900
901
902
PDEN 906
WINDOWED
CK
908
CK
201
904
905
LEVELING-
MODE
910
DQ
205
918
FEEDBACK
PATH
907

FIG. 9

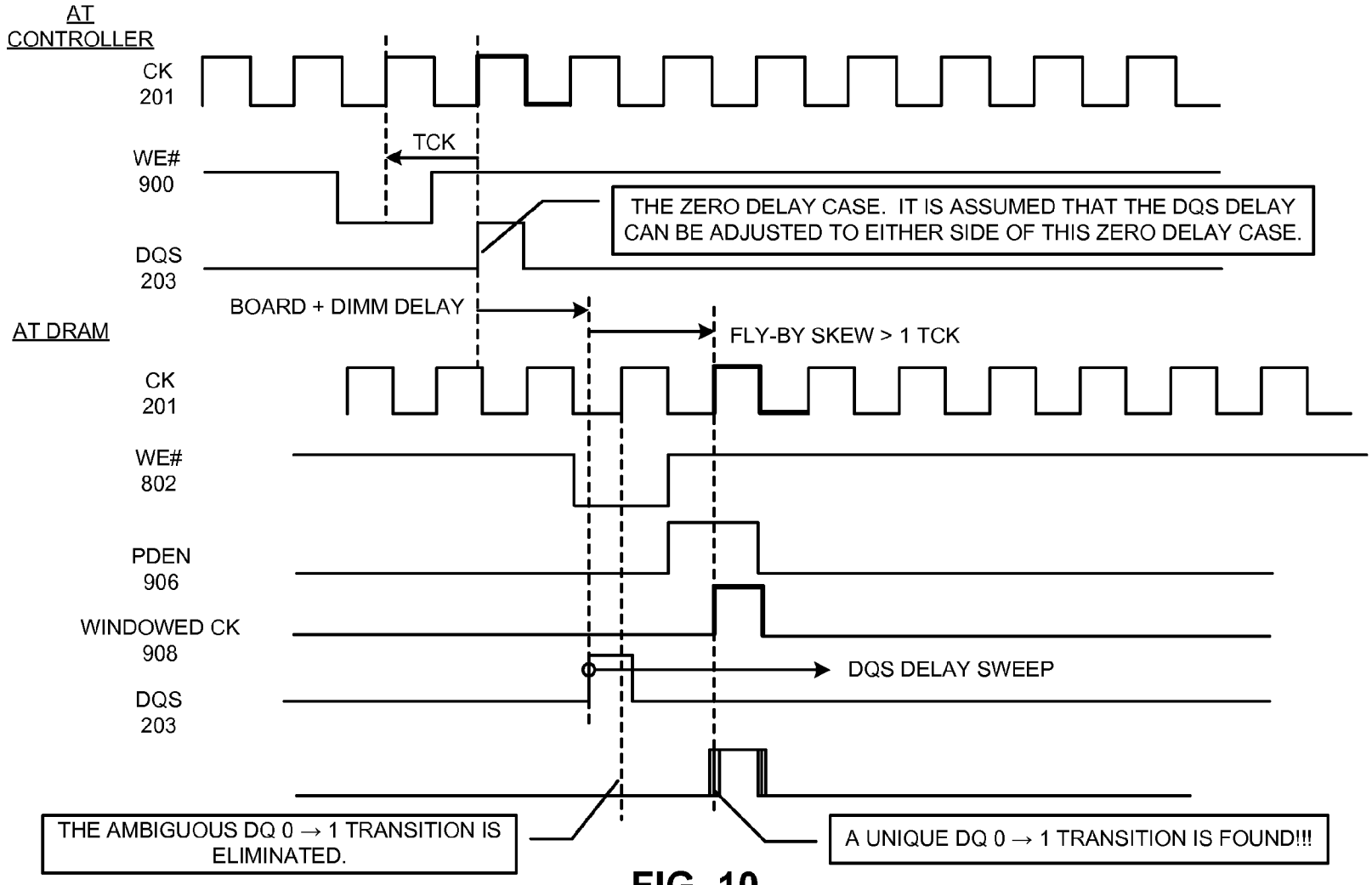

AT CONTROLLER
CK 201
TCK
WE# 900
THE ZERO DELAY CASE. IT IS ASSUMED THAT THE DQS DELAY CAN BE ADJUSTED TO EITHER SIDE OF THIS ZERO DELAY CASE.
DQS 203
BOARD + DIMM DELAY
AT DRAM
FLY-BY SKEW > 1 TCK
CK 201
WE# 802
PDEN 906
WINDOWED CK 908
DQS DELAY SWEEP
DQS 203
THE AMBIGUOUS DQ 0 → 1 TRANSITION IS ELIMINATED.
A UNIQUE DQ 0 → 1 TRANSITION IS FOUND!!!

FIG. 10

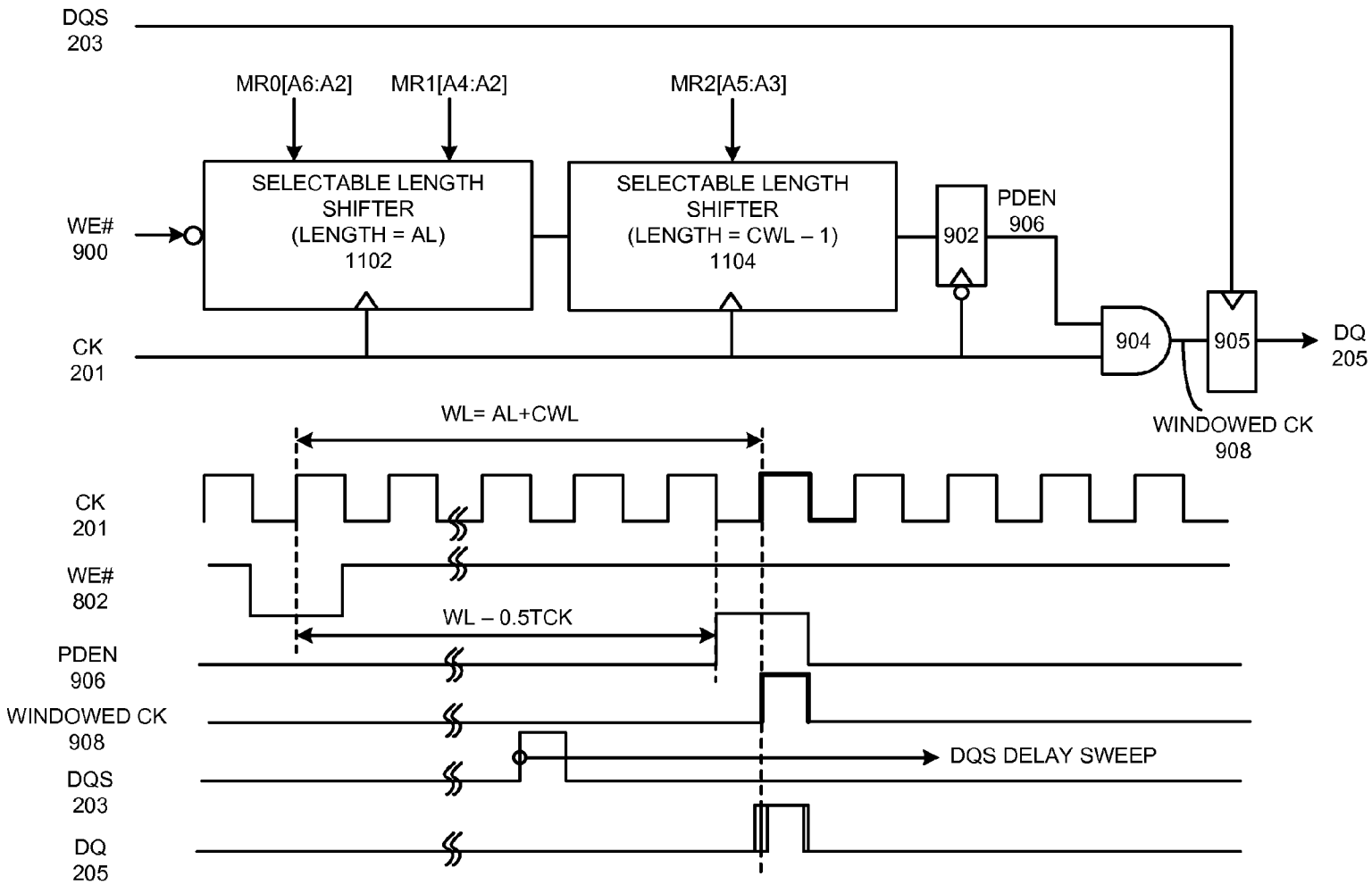

DQS
203
MR0[A6:A2]
MR1[A4:A2]
MR2[A5:A3]
SELECTABLE LENGTH SHIFTER (LENGTH = AL) 1102
SELECTABLE LENGTH SHIFTER (LENGTH = CWL – 1) 1104
WE#
900
CK
201
902
PDEN
906
904
905
DQ
205
WINDOWED CK
908
WL= AL+CWL
CK
201
WE#
802
WL – 0.5TCK
PDEN
906
WINDOWED CK
908
DQS
203
DQS DELAY SWEEP
DQ
205

FIG. 11

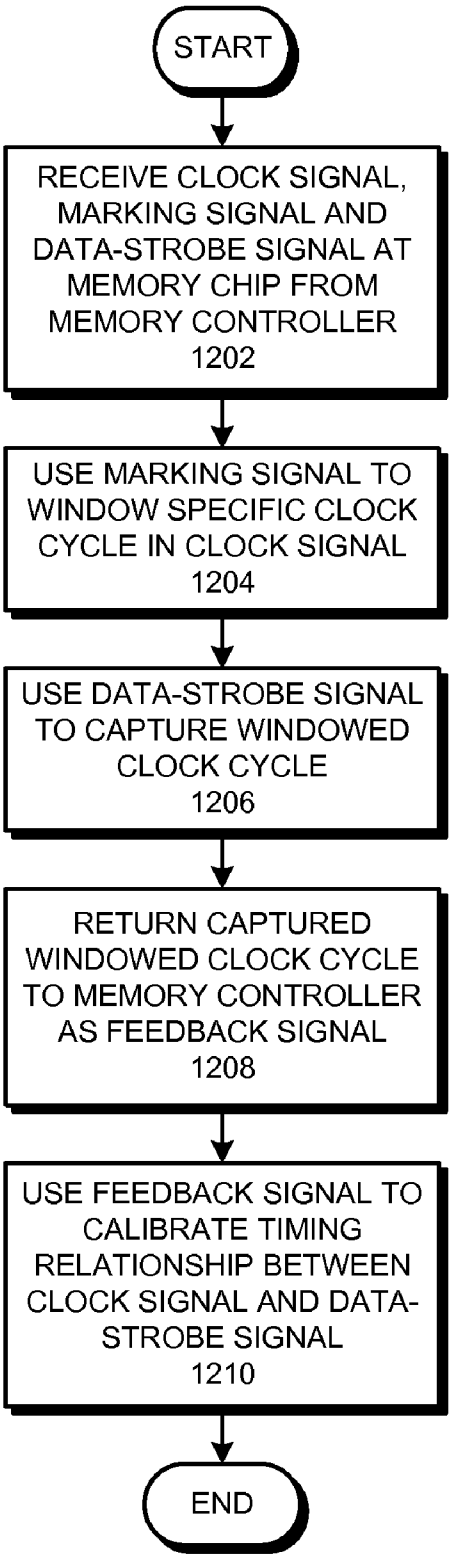

START
RECEIVE CLOCK SIGNAL, MARKING SIGNAL AND DATA-STROBE SIGNAL AT MEMORY CHIP FROM MEMORY CONTROLLER
1202
USE MARKING SIGNAL TO WINDOW SPECIFIC CLOCK CYCLE IN CLOCK SIGNAL
1204
USE DATA-STROBE SIGNAL TO CAPTURE WINDOWED CLOCK CYCLE
1206
RETURN CAPTURED WINDOWED CLOCK CYCLE TO MEMORY CONTROLLER AS FEEDBACK SIGNAL
1208
USE FEEDBACK SIGNAL TO CALIBRATE TIMING RELATIONSHIP BETWEEN CLOCK SIGNAL AND DATA-STROBE SIGNAL
1210
END

FIG. 12

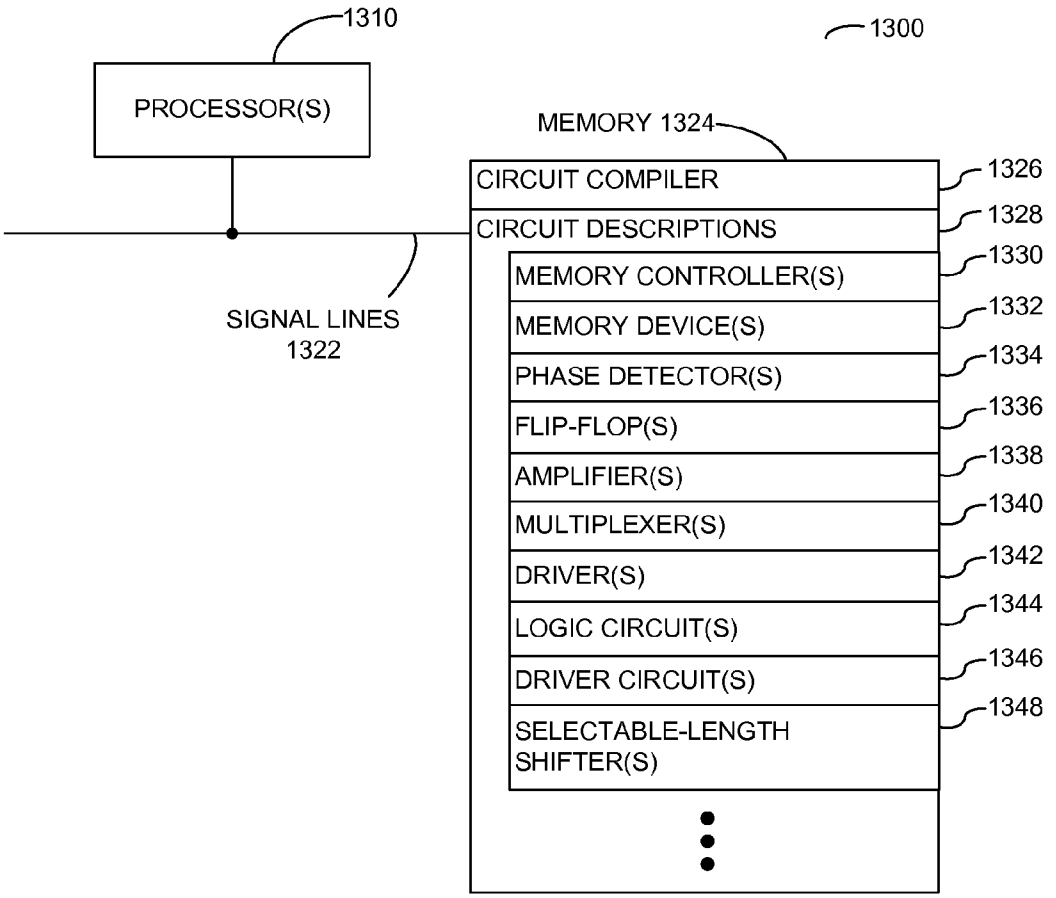

1310
1300
PROCESSOR(S)
MEMORY 1324
CIRCUIT COMPILER
CIRCUIT DESCRIPTIONS
MEMORY CONTROLLER(S)
MEMORY DEVICE(S)
PHASE DETECTOR(S)
FLIP-FLOP(S)
AMPLIFIER(S)
MULTIPLEXER(S)
DRIVER(S)
LOGIC CIRCUIT(S)
DRIVER CIRCUIT(S)
SELECTABLE-LENGTH SHIFTER(S)
SIGNAL LINES 1322
1326
1328
1330
1332
1334
1336
1338
1340
1342
1344
1346
1348

FIG. 13

METHOD AND APPARATUS FOR CALIBRATING WRITE TIMING IN A MEMORY SYSTEM

RELATED APPLICATIONS

This application is a divisional application of, and hereby claims priority under 35 U.S.C. §120 to, pending U.S. patent application Ser. No. 12/049,928, entitled "Method and Apparatus for Calibrating Write Timing in a Memory System," filed on Mar. 17, 2008, by Thomas J. Giovannini, Alok Gupta, Ian Shaeffer and Steven C. Woo. The present application further claims priority under 35 U.S.C. §119 to U.S. Provisional Patent Application No. 61/016,317, filed Dec. 21, 2007, to which the Ser. No. 12/049,928 parent application also claims priority.

BACKGROUND

Field

The present embodiments generally relate to techniques for calibrating the timing of signals involved in performing write operations to a memory for a computer system.

BRIEF DESCRIPTION OF THE FIGURES

FIG. **1** illustrates an embodiment of a computer system.

FIG. **2** illustrates an embodiment of a phase detector.

FIG. **3** presents a flow chart illustrating an embodiment of a memory-timing calibration process.

FIG. **4** presents a flow chart illustrating an embodiment of a write-read-verify process to calibrate memory timing.

FIG. **5** presents a flow chart illustrating an example of a process for calibrating a read-data-alignment setting.

FIG. **6** presents a flow chart illustrating another example of a process for calibrating a read-data-alignment setting.

FIG. **7** presents a flow chart illustrating another example of a memory-timing calibration process.

FIG. **8** presents a graph illustrating pass-fail regions.

FIG. **9** illustrates an embodiment of a modified phase-detector circuit.

FIG. **10** presents a timing diagram illustrating an example of a calibration process.

FIG. **11** illustrates a variation of a calibration phase-detector circuit along with an associated timing diagram.

FIG. **12** presents a flow chart illustrating an example of a write-timing calibration process.

FIG. **13** is a block diagram illustrating an embodiment of a system.

DETAILED DESCRIPTION

The following description is presented to enable any person skilled in the art to make and use the disclosed embodiments, and is provided in the context of a particular application and its requirements. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the present description. Thus, the present description is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

Embodiments of an apparatus that calibrates timing relationships between signals involved in performing write

operations are described. These embodiments include a memory controller which is coupled to a set of memory chips. Each of these memory chips includes a phase detector configured to enable calibration of a phase relationship between a data-strobe signal and a clock signal received at the memory chip from the memory controller. Furthermore, the memory controller is configured to perform one or more write-read-validate operations to calibrate a clock-cycle relationship between the data-strobe signal and the clock signal, wherein the write-read-validate operations involve varying a delay on the data-strobe signal relative to the clock signal by a multiple of a clock period.

In some embodiments, the set of memory chips are coupled to the memory controller through a fly-by topology, wherein the clock signal is routed from the memory controller to the set of memory chips in a multi-drop fashion along a "fly-by path," and wherein data signals and the data-strobe signal are routed from the memory controller to the set of memory chips through direct connections. Note that a "fly-by delay separation" which results from a difference in delay between the clock signal on the fly-by path and the data-strobe signal on a direct path can exceed one clock period. In some embodiments, the memory chips are calibrated in order of increasing delay along the fly-by path.

In some embodiments, while calibrating the phase relationship between the data-strobe signal and the clock signal, the memory controller is configured to assert a pulse on the data-strobe signal at varying delays relative to the clock signal and to look for a transition at the output of the phase detector, wherein the transition indicates that the data-strobe signal is aligned with the clock signal.

In some embodiments, while calibrating the clock-cycle relationship, the memory controller is configured to successively: vary a delay on the data-strobe signal relative to the clock signal by a multiple of a clock period; write a value to a specific location in the memory chip; read a value from the specific location in the memory chip; and determine whether the data-strobe signal and the clock signal are calibrated by validating that the value read from the specific location matches the value written to the specific location.

In some embodiments, the apparatus is configured to sequentially calibrate all memory chips in the set of memory chips.

In some embodiments, the calibration is performed at full memory speed using robust data patterns.

In some embodiments, the memory controller is additionally configured to adjust a timing relationship between the data-strobe signal and the data-strobe enable signal during a read operation.

Some embodiments provide another system for calibrating timing relationships between signals involved in performing write operations in a memory system. During a calibration mode, this system receives signals at a memory chip in a set of memory chips, wherein the signals include a clock signal, a marking signal and a data-strobe signal from a memory controller, and wherein the marking signal includes a pulse which marks a specific clock cycle in the clock signal. Next, the system facilitates calibration of a timing relationship between the data-strobe signal and the clock signal by using the marking signal to window the specific clock cycle in the clock signal, thereby generating a windowed clock signal. Next, the system uses the data-strobe signal to capture the windowed clock signal at a phase detector on the memory chip. Finally, the system returns the captured windowed clock signal to the memory controller so that the memory controller can calibrate the timing relationship.

In some embodiments, the marking signal is communicated from the memory controller to the memory through a selected signal line on the fly-by path, wherein the selected signal line carries another signal when the memory system is not in the calibration mode.

In some embodiments, the selected signal line carries a write-enable signal when the memory system is not in the calibration mode.

In some embodiments, using the data-strobe signal to capture the windowed clock signal involves using the data strobe signal to clock the windowed clock signal into a flip-flop.

In some embodiments, a semiconductor memory device that facilitates calibrating timing relationships between signals involved in performing write operations is disclosed. The memory device includes a clock input to receive a clock signal. In addition, the memory device includes a first input to receive a marking signal from a memory controller. The marking signal includes a pulse which marks a specific clock cycle in the clock signal. The memory device also includes: a second input to receive a data-strobe signal from the memory controller; and a phase detector, which uses the marking signal to window the specific clock cycle in the clock signal, the phase detector also uses the data-strobe signal to capture the windowed clock cycle. The memory device includes an output which provides the captured windowed clock cycle as a feedback signal to the memory controller.

In some embodiments a memory controller is coupled to a memory chip that receives a clock signal, and includes a calibration mode to calibrate a clock-cycle relationship between the data-strobe signal and a clock signal by iteratively: varying a delay on the data-strobe signal relative to the clock signal by a multiple of a clock period; writing a first value to a specific location in the memory chip; reading a second value from the specific location in the memory chip; and determining whether the data-strobe signal and the clock signal are calibrated by validating that the value read from the specific location matches the value written to the specific location.

In some embodiments, the system generates the windowed clock signal by using the rising edge of the clock signal to clock the marking signal through a cascade of flip-flops whose overall latency represents the DRAM write latency. The output of this cascade is then registered on the falling edge of the clock to create the phase-detector enable signal. Next, the system generates the windowed clock signal by logically ANDing the phase-detector enable signal with the clock signal.

Computer System

As memory systems begin to operate at extremely high data rates (for example, greater than 1000 Mega transfers per second ("MT/s")), a "fly-by" memory topology may be used to achieve the required level of signaling performance. For example, see computer system **100** illustrated in FIG. **1**, which includes a processor **104** that communicates with a Dual Inline Memory Module ("DIMM") **106** through a memory controller **102**. This computer system has a fly-by layout topology, in which control signals, including one or more request (RQ) signal(s) and a clock (CK) signal, are routed from memory controller **102** to multiple synchronous dynamic random access memory ("SDRAM" or "DRAM") chips **110-117**. In this embodiment, the control signals and clock signal within DIMM **106** are coupled, in a multi-drop fashion, to each of the DRAM chips **110-117** using a fly-by path **108**. Request signals may include address signals and are propagated over signal lines which are, in an embodiment, trace-length matched relative to one-another and the clock signal line. The request signals and the clock signal propagate along the fly-by path **108** and are received by each of the DRAM chips **110-117** in sequence. At the same time, the data-strobe (DQS) and data (DQ) signals are routed directly to each of the DRAM chips **110-117** in DIMM **106**, and hence do not incur the delay through the fly-by path.

For each DRAM chip, the data-strobe (DQS) and data (DQ) signals, in one embodiment are routed point-to-point between a dedicated DQ interface port on the memory controller **102** and a DQ interface. In a system that supports multiple ranks, the direct connection may involve routing data-strobe (DQS) and data (DQ) signals between the dedicated DQ interface port on the memory controller **102** and connection points of each DQ interface for corresponding DRAM chips in each rank. A "rank" is a grouping of DRAM chips that contribute to a memory transfer that occurs in response to a memory access command given to the DRAM chips in a rank. In a system that supports multiple DIMM modules (each having either with a single or dual ranks), the direct connection may involve routing between the data-strobe (DQS) and data (DQ) signals between each dedicated DQ interface port on the memory controller and connection points of each DQ interface for corresponding DRAM chips in each DIMM module. (Note that, throughout this specification, a "DRAM chip" may be referred to as "DRAM".)

In an embodiment, the data strobe signal (DQS) may be routed alongside the data signals (DQ) and is used at the receiver of the integrated circuit (i.e., memory controller or DRAM) to receive the data. For example, in a write operation, when the memory controller is transmitting data to a DRAM, the controller sends a DQS signal alongside the data and the DQS signal is used at the DRAM to receive that data. In a read operation, when a DRAM is transmitting data to the memory controller, the DRAM will send a DQS signal alongside the data being transmitted to the controller. The DQS signal, when received by the controller is then used to strobe in the data which accompanied that DQS signal. DQS signals may be transmitted over a single bi-directional signal line for read and write operations, or separate unidirectional signal lines may be provided for respective read/write operations.

In an embodiment featuring a memory system configured with a fly-by layout topology, the RQ/CK propagation delay increases to each DRAM that receives RQ and CK signals from the fly-by signal path. This causes an increasing skew between RQ/CK and DQ/DQS signals received at each successive DRAM. To compensate for this effect during write transactions, memory controller **102** introduces increasing DQ/DQS transmit delay relative to when RQ/CK is transmitted for each successive DRAM. Similarly, during read transactions memory controller **102** introduces increasing DQS read-enable receive sample delays for each successive DRAM. These write and read delays, which are introduced by memory controller **102**, are referred to as "write-levelization" and "read-levelization" delays, respectively.

Also, during read transactions, the optimum read-data-alignment setting may increase for each successive DRAM that receives RQ and CK signals from the fly-by signal path, with the DRAM at the end of fly-by signal path requiring the largest read-data-alignment setting. Once this largest read-data-alignment setting is determined, it can be used to calculate settings for all the DQ/DQS groups in order to align the read data received at each of the DQ blocks at memory controller **102**.

In an embodiment, DRAM chips which are designed according to the DDR3 standard (JESD79-3 as published by JEDEC Solid State Technology Association) may be provided with built-in circuitry to facilitate timing adjustment. For example, FIG. **2** illustrates a phase-detector circuit within

a DRAM chip **200** that facilitates phase adjustments between a clock signal on the fly-by path and a data-strobe signal on a direct path. In this phase-detector circuit, operational amplifier **209** converts a differential clock signal comprised of CK signal **201** and CK# signal **202** into a non-differential clock signal **212**. Similarly, operational amplifier **210** converts a differential strobe signal comprised of DQS signal **203** and DQS# signal **204** into a non-differential data-strobe signal **214**. The non-differential data-strobe signal **214** is then used to clock the non-differential clock signal **212** into a flip-flop **206**. The output of flip-flop **206** feeds through a feedback path **211** and then through a multiplexer **207** and a driver **208** onto a data line DQ **205**. Note that multiplexer **207** selectively feeds the output of flip-flop **206** onto data line DQ **205** based on a value of a leveling-mode signal **213**. This allows memory controller **102** to determine whether the clock signal **212** and data-strobe signal **214** are phase-aligned, which in turn, enables memory controller **102** (FIG. **1**) to calibrate the phase relationship between the data-strobe signal **214** and the clock signal **212** by asserting a pulse on data-strobe signal **214** at varying delays relative to clock signal **212** and looking for a transition at the output of the phase detector which appears on data line DQ **205**.

In the embodiment described above in reference to FIG. **2**, situations may exist where the resulting timing adjustment provided by the above-described phase-detector circuit may not be correct because write/read data integrity is not verified during the adjustment process. In particular, if the fly-by delay separation between the clock signal and the data-strobe signal exceeds one clock period, the above-described timing adjustment process will adjust the phase relationship properly, but the timing adjustment may be off by a multiple of a clock period.

To account for such situations, embodiments are presented below that verify write/read data integrity during the timing-adjustment process. In doing so, they write and read robust data patterns to and from the DRAM of interest, as well as simultaneously communicating data patterns to the other DRAMs in the topology, so that realistic switching noise effects may be accounted for during the timing-adjustment process.

DRAM Calibration Process

FIG. **3** presents a flow chart illustrating an embodiment of a memory timing calibration process. In this embodiment, there are a few assumptions for this calibration process: (1) It is assumed that the timing relationship between request (RQ) and clock (CK) signals has been set to compensate for the estimated average skew between RQ and CK; (2) It is assumed that the timing relationship between data signals (DQ) and data-strobe signal (DQS) for each DQ/DQS group has been set to compensate for the estimated average skew between DQ and DQS; (3) It is also assumed that DRAMs will be processed in successive order of increasing RQ/CK delay; and (4) It is additionally assumed that the skew between any two DQ/DQS groups is much less than one CK cycle.

Referring to FIG. **3**, the process starts by performing a read-calibration (read-leveling) process (operation **302**) in which a register or other storage on each DRAM (of a set of DRAMS coupled to the flyby RQ and direct DQ topology as shown in FIG. **1**) provides a predefined data pattern to the controller. The DRAM situated closest to the controller on the fly-by RQ bus and (thus having the shortest RQ/CK flight time delay) transmits the predefined data pattern before the DRAM situated furthest to the controller on the fly-by RQ bus (thus having the longest RQ/CK flight time delay). The controller can then determine the receive timing offset for each receive DQ block in the controller by, for example, adjusting its read data strobe enable delay to be properly aligned with the received read data strobe whose arrival time results from the propagation delay of a read command being received at the corresponding DRAM.

If the system does not pass the calibration process in operation **302**, the system signals an error (operation **304**). Otherwise, the system performs a write-calibration (write-leveling) process (operation **306**). (Note that this write-calibration process, in an embodiment, may make use of the phase-detector circuit located in each DRAM as is illustrated in FIG. **2**.) In an embodiment the write calibration process involves providing a DQS strobe signal that each DRAM (of a set of DRAMS coupled to the flyby RQ and direct DQ topology as shown in FIG. **1**) uses to sample the clock signal CK and outputs the result over the direct DQ lines back to the controller. In the write—calibration process, the controller can then determine transmit timing offsets for each transmit DQ block on the controller to, for example, levelize write data skew that results from the propagation delay of a corresponding write command being received in succession at each DRAM.

After the write calibration process (operation **306**), the clock and data-strobe signals should be phase-aligned, but the timing of these signals may still be misaligned by a multiple of a clock period. In order to remedy this problem, in an embodiment, the system performs an extended write-read-verify write-calibration optimization (operation **308**). (This process is described in more detail below with reference to FIG. **4**.) The system can additionally perform an extended write-read-verify read-calibration optimization (operation **310**).

FIG. **4** presents a flow chart illustrating an example of a write-read-verify process to calibrate write timing. At the start of this process, the system sets the delay of the data-strobe signal relative to the clock signal to the value obtained in the write calibration process (operation **420**). This assumes that the write calibration process began its DQS delay search with the minimum delay setting. Next, the system writes a value to a specific location in the DRAM (operation **422**) and then reads a value from the same location (operation **424**). Then, the system determines if the value written to the memory location and the value read from the memory location match (operation **426**). If not, the system increases the delay by one clock period (operation **428**) and returns to operation **422**. On the other hand, if the values match, the write operation was successful, which indicates that the system is calibrated and hence the calibration process is complete.

Read-Data-Alignment Calibration

In an embodiment, the system additionally has to be calibrated to compensate for misalignment of read data from different DRAM devices. Read data from successive DRAM devices, configured in a system that uses the fly-by topology, arrive at the memory controller with successively increasing delay. In an embodiment, a read alignment process involves queuing read data within successive DQ receiver blocks at the controller.

After read data from different DRAM devices arrives at the memory controller with successively increasing delay, it is received by a circuit on the controller that temporary stores the read data before the read data is internally aligned to the controller clock and then processed further. "Read-alignment" (also referred to as "read-data-alignment") involves synchronizing the read data to the same clock signal as the read data comes out of, for example a first in, first out buffer ("FIFO") in the memory controller and is provided to the core of the memory controller. This clock signal is not the same as

the read data strobe enable signal which is different for each slice of data and enables data to be written into the FIFO. A buffer circuit and/or flip-flop circuit elements may be used in place of or in conjunction with the FIFO.

More specifically, FIG. **5** presents a flow chart illustrating an embodiment of a process for calibrating a read-data-alignment setting. The system starts by setting all DRAMs to a minimum possible read-data-alignment setting (operation **502**). Next, the system calibrates a single DRAM using the technique described previously in FIG. **3** (operation **504**) and then determines whether the DRAM passes the calibration process (operation **506**). If the DRAM does not pass the calibration process, the system increases the current read-data-alignment setting (operation **508**) and returns to operation **504**. Otherwise, if the DRAM passes the calibration process, the system determines if there exists another DRAM to calibrate (operation **510**). If so, the system returns to operation **504** to calibrate the next DRAM. Otherwise, the system determines the largest read-data-alignment setting across all DRAMs (operation **512**) and sets to read-data-alignment setting for all DRAMs to this largest setting (operation **514**).

Next, the system determines if there exists another rank of DRAMs to calibrate (operation **516**). If so, the system returns to operation **502** to calibrate the next rank of DRAMs. Otherwise, if there are no additional ranks of DRAMs, the process is complete.

In an alternative embodiment, which is illustrated in FIG. **6**, the read-alignment setting is initialized to a maximum possible setting and is then decreased. More specifically, in this alternative embodiment, the system starts by setting all DRAMs to a maximum possible read-data-alignment setting (operation **602**). Next, the system calibrates a single DRAM using the technique described previously in FIG. **3** (operation **604**) and determines if there exists another DRAM to calibrate (operation **606**). If so, the system returns to operation **604** to calibrate the next DRAM. Otherwise, the system determines the read-enable-delay setting for each DRAM (operation **608**) and then determines a largest read-data-alignment setting across all DRAMs (operation **610**). The system then sets the read-data-alignment setting for all DRAMs to this largest setting (operation **612**).

Next, the system determines if there exists another rank of DRAMs to calibrate (operation **614**). If so, the system returns to operation **602** to calibrate the next rank of DRAMs. Otherwise, if there are no additional ranks of DRAMs, the process is complete.

2D Write-Read-Verify Calibration Technique for a Single DRAM

FIG. **7** presents a flow chart illustrating an alternative embodiment for a memory-timing calibration process which uses a two-dimensional ("2D") Write-Read-Verify calibration technique. This 2D search technique uses a two-pass approach. The first pass uses coarse-step-sizes for transmit and receive phase settings (write and read levelization delays, respectively) (operation **702**). Starting from the origin of the 2D search region, the system first incrementally steps the transmit phase. For each transmit phase, the system attempts to find a "coarse-pass" region by incrementally stepping the receive phase. The system continues to step through the transmit phase until a sufficiently large coarse-pass region is found. When this occurs, the first pass is terminated and the latest transmit phase is used as a seed for the second pass of the technique.

If the system does not find a coarse-pass region and hence does not pass the first phase, the system signals an error (operation **705**).

Otherwise, if the system successfully finds a coarse-pass region, the system performs a fine-step-size search for the DQS read-enable-delay center (operation **706**), and then performs a fine-step-size search for the DQ/DQS write-delay center (operation **708**). More specifically, starting with the seed generated during the first-pass transmit phase, the second pass uses a fine step size for the receive phase setting to find the entire pass region around the first-pass transmit phase. It then finds the center of this region, and uses the center receive phase as the optimum receive phase setting. Starting at the center receive phase, the second pass then uses a fine step size for the transmit phase setting to find the entire pass region around the center receive phase setting. The system then finds the center of this region, and uses the center transmit phase as the transmit phase setting.

Note that the above-described 2D calibration technique can for example be used with DDR2 SDRAM chips or other types of memory devices. Hence, the flow diagram of FIG. **5** can be used by substituting the 2D technique into operation **504**. Alternatively, the flow diagram of FIG. **6** can be used by substituting the 2D technique into operation **604**.

FIG. **8** presents a graph illustrating pass-fail regions. Note that the above-described 2D search will identify a 2D pass region **802** for all possible combinations of read-enable delays and write-enable delays.

Phase-Detector Circuit **1**

FIG. **9** illustrates an embodiment of a phase-detector circuit which, for example, may facilitate write timing calibration for DRAM fly-by delay separations greater than one clock cycle. In this phase-detector circuit, a marking pulse is received on, for example, a write enable ("WE#") signal line **900**, and this marking pulse is fed through two D-flops **901** and **902**, which are clocked on alternate rising and falling edges of the clock signal **201**. This generates a phase-detector enable signal (PDEN) **906** with a window for the desired time slot. PDEN signal **906** is then ANDed with clock signal **904** to generate a windowed clock signal **908**. In an embodiment WE# is routed and propagates alongside CK along the fly-by path.

Data-strobe signal (DQS) **203** is then used to clock the windowed clock signal **908** into a flip-flop **905**. The output of flip-flop **905** feeds through a feedback path **905** and then through a multiplexer **918** onto a data line DQ **205**. Note that multiplexer **918** selectively feeds the output of flip-flop **206** onto data line DQ **205** based on a value of a leveling-mode signal **910**.

This feedback signal enables the memory controller to determine whether the clock signal **201** and DQS **203** are aligned, which in turn, enables the memory controller to calibrate the timing relationship between the DQS **203** and the clock signal **201** by asserting a pulse on DQS **203** at varying delays relative to clock signal **201** and looking for a transition at the output of the phase detector which appears on data line DQ **205**.

Note that any command or control line on the fly-by path can be used to communicate this marking pulse. Hence, it is not necessary to use the specific command line WE#, because another command or control line can be used in place of the WE# command line for this purpose (for example, command lines such as RAS#, CAS#, or control lines such as chip select (CS#) or clock enable (CKE#) may be used in place of WE# in various embodiments). In this embodiment, the WE# command line is used since it is associated with a memory write function in normal operation (i.e., non calibration mode operation).

After windowed clock signal **908** is generated, DQS signal **203** is used to clock windowed clock signal **908** into a flip-

flop **905**. In similar fashion to the circuit illustrated in FIG. **2**, the output of flip-flop **905** feeds through a feedback path **907**, in through a multiplexer **918**, and onto a data line DQ **205**. During this process, multiplexer **918** selectively feeds the output of flip-flop **905** onto data line DQ **205** based on a value of a leveling-mode signal **910**. Hence, during a leveling mode of operation, the memory controller is able to determine whether the windowed clock signal **908** and data-strobe signal DQS **203** are phase-aligned. This enables the memory controller to calibrate the timing relationship between the DQS signal **203** and the windowed clock signal **908** by asserting a pulse on DQS signal **203** at varying delays relative to windowed clock signal **908** and by looking for a transition at the output of the phase detector which appears on data line DQ **205**.

However, in the case where the DRAM fly-by delay separation exceeds one clock cycle, the circuit illustrated in FIG. **9** will only generate a zero-to-one transition if DQS signal **203** and clock signal **201** are phase aligned and are additionally aligned on the proper clock cycle. This is unlike the circuit illustrated in FIG. **2** which generates a zero-to-one transition in cases where DQS signal **203** and clock signal **201** are phase aligned but are not aligned on the proper clock cycle.

Calibration Process

FIG. **10** presents a timing diagram illustrating an example of a calibration process which uses the circuitry illustrated in FIG. **9**. The top portion of FIG. **10** illustrates the timing of signals at the memory controller and the bottom portion of FIG. **10** illustrates the timing of signals at the memory chip (DRAM). In FIG. **10**, the controller sends a clock signal (CK **201**) and a data-strobe signal (DQS **203**) to the DRAM.

As is illustrated in FIG. **10**, a DQS pulse is asserted by the controller. In this embodiment, CK and all DQS signals to the DIMM containing the DRAM are routed with equal length traces on the circuit board. After the time of flight on the circuit board, CK and DQS propagate to each DRAM in the DIMM. During this process, the DQS signals are routed with equal length to each DRAM within the DIMM. However, the CK is routed to each DRAM successively along a fly-by path. This results in successively increasing skew between CK and DQS at each DRAM along the fly-by path. As memory clock speeds continue to increase, these DRAM fly-by delay separations begin to exceed one clock cycle. This causes CK-versus-DQS skews which are greater than one clock cycle. In an embodiment, at least one command signal (e.g., WE#) is routed and propagates alongside CK along the fly-by path.

As is illustrated by the arrow attached to the DQS pulse at the DRAM in FIG. **10**, the calibration process sweeps the DQS pulse delay relative to CK to find a zero-to-one transition at the output of the standard phase detector. Detection of a zero-to-one transition is an indicator of correct CK vs. DQS phase alignment.

Note that the memory controller asserts the WE# signal **900** one clock cycle before the DQS pulse is asserted. After signal propagation between the memory controller and the DRAM, more than one clock cycle of skew exists between CK signal **201** and DQS signal **203**. As shown in the circuitry illustrated in FIG. **9**, the WE# signal **900** is staged and inverted to window the desired CK time slot. The resulting window signal, PDEN, is then used to prevent detections of false transitions as illustrated at the bottom of FIG. **10**.

Phase Detector Circuit II

FIG. **11** illustrates an embodiment of a phase-detector circuit that may be utilized in a DRAM, along with an associated timing diagram. This embodiment is similar to the embodiment illustrated in FIG. **9**, except that WE# signal **900** is staged through staging circuitry for the WE# signal **900** on the DRAM (instead of through flip-flop **901**).

More specifically, WE# signal **900** is staged through a first selectable-length shifter **1102** for additive latency (AL) with a delay programmed to be AL, and a second selectable-length shift register **1104** for CAS write latency (CWL) with a delay programmed to be=CWL-1, wherein the "1" represents the delay through flip-flop **902**. Additive latency is a programmable delay between receipt of a column command (e.g., a read or write command) at the DRAM and the internal application or posting of that command that signifies when execution of that command is commenced internally. Write latency is the programmable delay between the internal application or posting of the write command and when data associated with that write command is sampled by the DRAM. By using this staging circuitry, the memory controller can perform the write-calibration process using the same write latency that results during normal operation.

Calibration Process

FIG. **12** presents a flow chart illustrating an embodiment of a write timing calibration process. During this process, a clock signal, a marking signal and a data-strobe signal are sent to a memory chip from a memory controller (operation **1202**). Next, the marking signal is used to "window" a specific clock cycle in the clock signal (operation **1204**). This generates a windowed clock signal.

Next, a pulse on the data-strobe signal is used to capture the windowed clock signal in a memory element (operation **1206**). This captured windowed clock signal is then returned to the memory controller as a feedback signal (operation **1208**).

The memory controller then uses the feedback signal to calibrate a timing relationship between the clock signal and the data-strobe signal (operation **1210**). For example, this calibration process can involve asserting a pulse on the data-strobe signal at varying delays relative to the clock signal and look for a transition at the output of the phase detector, wherein the transition indicates that the data-strobe signal is aligned with the clock signal.

Note that the FIGS. **1-12** may include fewer components or operations, or additional components or operations. Moreover, two or more components or operations can be combined into a single component or operations, and/or the position of one or more components or operations can be changed.

Additionally, components and/or functionality illustrated in FIGS. **1-12** may be implemented using analog circuits and/or digital circuits. Furthermore, components and/or functionality in FIGS. **1-12** may be implemented using hardware and/or software.

Devices and circuits described herein may be implemented using computer-aided design tools available in the art, and embodied by computer-readable files containing software descriptions of such circuits. These software descriptions may be: behavioral, register transfer, logic component, transistor and layout geometry-level descriptions. Moreover, the software descriptions may be stored on storage media or communicated by carrier waves.

Data formats in which such descriptions may be implemented include, but are not limited to: formats supporting behavioral languages like C, formats supporting register transfer level (RTL) languages like Verilog and VHDL, formats supporting geometry description languages (such as GDSII, GDSIII, GDSIV, CIF, and MEBES), and other suitable formats and languages. Moreover, data transfers of such files on machine-readable media may be done electronically over the diverse media on the Internet or, for example, via email. Note that physical files may be implemented on

machine-readable media such as: 4 mm magnetic tape, 8 mm magnetic tape, 3½ inch floppy media, CDs, DVDs, and so on.

FIG. **13** presents a block diagram illustrating an embodiment of a system **1300** that stores such computer-readable files. This system may include at least one data processor or central processing unit (CPU) **1310**, memory **1324** and one or more signal lines or communication busses **1322** for coupling these components to one another. Memory **1324** may include random access memory and/or non-volatile memory, such as: ROM, RAM, EPROM, EEPROM, flash, one or more smart cards, one or more magnetic disc storage devices, and/or one or more optical storage devices.

Memory **1324** may store a circuit compiler **1326** and circuit descriptions **1328**. Circuit descriptions **1328** may include descriptions of the circuits, or a subset of the circuits discussed above. In particular, circuit descriptions **1328** may include circuit descriptions of: one or more memory controllers **1330**, one or more memory devices **1332**, one or more phase detectors **1334**, one or more flip-flops **1336**, one or more amplifiers **1338**, one or more multiplexers **1340**, one or more drivers **1342**, one or more logic circuits **1344**, one or more driver circuits **1346**, and/or one or more selectable-length shifters **1348**.

Note that the system **1300** may include fewer components or additional components. Moreover, two or more components can be combined into a single component and/or the position of one or more components can be changed.

The foregoing descriptions of embodiments have been presented for purposes of illustration and description only. They are not intended to be exhaustive or to limit the present description to the forms disclosed. Accordingly, many modifications and variations will be apparent to practitioners skilled in the art. Additionally, the above disclosure is not intended to limit the present description. The scope of the present description is defined by the appended claims.

What is claimed is:

1. A method of operation in a memory system comprising:

during a calibration mode, sending signals including a clock signal, a marking signal and a data-strobe signal from a memory controller to a memory chip in a set of memory chips, wherein the marking signal includes a pulse which marks a specific clock cycle of the clock signal; and

receiving a feedback signal from the memory chip, the feedback signal having been produced at the memory chip by using the marking signal to window the specific clock cycle of the clock signal, thereby generating a windowed clock signal, and using the data-strobe signal to capture the windowed clock signal; and

calibrating, based on the feedback signal, timing relationships between signals involved in performing write operations that occur between the memory controller and the memory chip.

2. The method of claim **1**, wherein calibrating, based on the feedback signal, the timing relationships between signals involved in performing write operations, includes calibrating a timing relationship between the data-strobe signal and the clock signal.

3. The method of claim **1**,

wherein the data-strobe signal and associated data signals are sent to the memory chip through a first path; and

wherein the clock signal and the marking signal are sent to the memory controller through a second path; and

wherein a difference in delay between the first path and the second path can exceed one clock period of the clock signal.

4. The method of claim **1**,

wherein the data-strobe signal and associated data signals are sent to the memory chip through a direct path; and

wherein the clock signal and the marking signal are sent to the memory controller through a multi-drop path, which passes through the set of memory chips in a multi-drop fashion; and

wherein a difference in delay between the clock signal and the data-strobe signal can exceed one clock period of the clock signal.

5. The method of claim **1**, wherein calibrating the timing relationship between the data-strobe signal and the clock signal involves asserting a pulse on the data-strobe signal at varying delays relative to the clock signal and looking for a transition in the feedback signal, wherein the transition indicates that the data-strobe signal is aligned with the clock signal.

6. The method of claim **1**, wherein the marking signal is communicated to the memory through a selected signal line on the multi-drop path, wherein the selected signal line carries another signal when the memory system is not in the calibration mode.

7. The method of claim **6**, wherein the selected signal line carries a write-enable signal when the memory system is not in the calibration mode.

8. The method of claim **1**, wherein the method is repeated for all memory chips in the set of memory chips.

9. The method of claim **1**, further comprising adjusting a timing relationship between the data-strobe signal and the clock signal during read operations.

10. A memory controller to couple to a memory chip that receives a clock signal, the memory controller comprising:

an interface to output, during a calibration mode, a marking signal and a data-strobe signal to the memory chip, wherein the marking signal identifies a specific clock cycle in the clock signal; and

a feedback input to receive a feedback signal from the memory chip, the feedback signal having been generated at the memory chip by using the marking signal to window the specific clock cycle in the clock signal to generate a windowed clock cycle, and using the data-strobe signal to capture the windowed clock cycle to produce the feedback signal; and

a calibration mechanism which analyzes the feedback signal to calibrate a timing relationship between the data-strobe signal and the clock signal.

11. The memory controller of claim **10**,

wherein the data-strobe signal and associated data signals are sent to the memory chip through a first path; and

wherein the clock signal and the marking signal are sent to the memory controller through a second path; and

wherein a difference in delay between the first path and the second path can exceed one clock period.

12. The memory controller of claim **10**,

wherein the data-strobe signal and associated data signals are sent to the memory chip through a direct path; and

wherein the clock signal and the marking signal are sent to the memory controller through a multi-drop path, which passes through the set of memory chips in a multi-drop fashion; and

wherein a difference in delay between the clock signal and the data-strobe signal can exceed one clock period.

13. The memory controller of claim **10**, wherein the calibration mechanism asserts a pulse on the data-strobe signal at varying delays relative to the clock signal and looks for a

transition in the feedback signal, wherein the transition indicates that the data-strobe signal is aligned with the clock signal.

14. The memory controller of claim **10**, wherein the marking signal is communicated to the memory through a selected signal line on the multi-drop path, wherein the selected signal line carries another signal when the memory system is not in the calibration mode.

15. The memory controller of claim **14**, wherein the selected signal line carries a write-enable signal when the memory controller is not in the calibration mode.

16. The memory controller of claim **10**, wherein the calibration mechanism additionally calibrates a timing relationship between the data-strobe signal and the data-strobe enable signal during read operations.

17. A method for calibrating timing relationships between signals involved in performing write operations in a memory system, comprising:

during a calibration mode, receiving signals from a memory controller at a memory chip in a set of memory chips, wherein the signals include,

a clock signal which is used as a reference clock by the memory chip,

a marking signal which includes a pulse that identifies a specific clock cycle in the clock signal, and

a data-strobe signal that accompanies data signals and is used to strobe the data signals into memory elements at the memory chip; and

facilitating calibration of a timing relationship between the data-strobe signal and the clock signal by,

the marking signal windowing the specific clock cycle in the clock signal to generate a windowed clock signal,

the data-strobe signal capturing the windowed clock signal at a phase detector on the memory chip, and

returning the captured windowed clock signal to the memory controller.

18. A semiconductor memory device that facilitates calibrating timing relationships between signals involved in performing write operations, the semiconductor memory device comprising:

a clock input to receive a clock signal;

a first input to receive a marking signal from a memory controller, wherein the marking signal includes a pulse which identifies a specific clock cycle of the clock signal;

a second input to receive a data-strobe signal from the memory controller;

a phase detector that uses the marking signal to window the specific clock cycle of the clock signal, wherein the phase detector uses the data-strobe signal to capture the windowed clock cycle; and

an output which provides the captured windowed clock cycle as a feedback signal to the memory controller.

19. The semiconductor memory device of claim **18**, wherein the phase detector circuit comprises:

a windowing circuit which uses the marking signal to window the specific clock cycle in the clock signal; and

a memory element that uses the data-strobe signal to capture the windowed clock cycle.

20. The semiconductor memory device of claim **19**, wherein the memory element is a flip-flop circuit which uses the data-strobe signal to capture the windowed clock cycle.

21. The semiconductor memory device of claim **19**, wherein the windowing circuit includes:

a series of flip-flops to clock the marking signal and generate a phase-detector enable signal, the series of flip-flops including:

a cascade of flip-flops having a latency time which represents a write latency time of the semiconductor memory device, wherein the cascade of flip-flops uses a first edge transition of the clock signal to clock the marking signal; and

an additional flip-flop which captures the output of the cascade of flip-flops on a second edge transition of the clock signal to create a phase-detector enable signal; and

a logic gate to receive the phase-detector enable signal and the clock signal, the logic gate to generate the windowed clock cycle based on a predetermined logic function of the logic gate.

22. The semiconductor memory device of claim **18**,

wherein the data-strobe signal and associated data signals are received from the memory controller through a first path; and

wherein the clock signal and the marking signal are received from the memory controller through a second path; and

wherein a difference in delay between signals received from the first path and associated data signals received from the second path can exceed one clock period of the clock signal.

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