

1 UNITED STATES PATENT AND TRADEMARK OFFICE

2 BEFORE THE PATENT TRIAL AND APPEAL BOARD

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4 SK HYNIX, INC., SK HYNIX : Inter Partes
5 AMERICA, INC., and SK HYNIX : Review No.
6 MEMORY SOLUTIONS, INC., : IPR2017-00548
7 Petitioner, :
8 v. : Patent No.
9 Netlist, Inc., : 8,489,837
10 Patent Owner. :
11 - - - - - X

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15 Deposition of ROBERT J. MURPHY

16 Los Angeles, California

17 Thursday, November 16, 2017

18 9:02 a.m.
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25 Reported by: Lisa Moskowitz, CSR 10816, RPR, CRR, CLR

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2 Deposition of ROBERT J. MURPHY, held at the offices
3 of:

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14 Systems Administrator.
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1 ALSO PRESENT:

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P R O C E E D I N G S

THE VIDEOGRAPHER: Here begins media
number 1 in the videotaped deposition of Robert J.
Murphy in the matter of SK Hynix, et al., v Netlist,
Inc., (PTAB) in the United States Patent and
Trademark Office before the Patent Trial and Appeal
Board, case numbers IPR2017-00548 and IPR2017-00549.

Today's date is November 16, 2017. The
time on the video monitor is 9:02 a.m. The
videographer today is David Kim, representing Planet
Depos. This video deposition is taking place at
555 West Fifth Street, Los Angeles, California.

Would counsel please voice identify
themselves and state whom they represent.

MR. MICALLEF: Joe Micallef, Sidley Austin,
for the petitioners.

MR. SUH: Wonjoo Suh, Sidley Austin, for
the petitioners.

MR. ARJOMAND: Mehran Arjomand, Morrison &
Foerster, for the patent owner.

MR. KIM: David S. Kim for the patent
owner.

MR. DUCKER: Philip Ducker from Mintz Levin
for the patent owner.

Transcript of Robert J. Murphy
Conducted on November 16, 2017

7

1 THE VIDEOGRAPHER: The court reporter today
2 is Lisa Moskowitz, representing Planet Depos.

3 Would the reporter please swear in the
4 witness.

5
6 Whereupon,

7 ROBERT J. MURPHY,
8 having been first duly sworn or affirmed to testify to
9 the truth, the whole truth, and nothing but the truth,
10 was examined and testified as follows:

11 EXAMINATION BY COUNSEL FOR THE PETITIONERS
12 BY MR. MICALLEF:

13 Q Good morning, Mr. Murphy.

14 A Good morning.

15 Q Please state your full name and address for
16 the record.

17 A Robert J. Murphy, 72 Fairview Plaza, Los
18 Gatos, California, 92530.

19 Q What do you do for a living?

20 A I run a design consulting business for my
21 living.

22 Q What kind of design?

23 A I generally design subsections of
24 integrated circuits commonly known as IP or
25 intellectual property for sale to people who are

09:03:02

09:03:03

09:03:07

09:03:09

09:03:18

09:03:18

09:03:19

09:03:22

09:03:22

09:03:28

09:03:31

09:03:32

09:03:39

09:03:40

09:03:41

09:03:45

09:03:48

1 making the integrated circuits themselves.

09:03:51

2 Generally, the specialty is memory, but I've done
3 things other than memory.

09:03:55

09:03:58

4 Q Have you been deposed before?

09:03:59

5 A I have.

09:04:01

6 Q So you understand the rules here?

09:04:02

7 A I do.

09:04:03

8 Q You'll let me know if you don't understand
9 anything about my questions.

09:04:04

09:04:06

10 A I will try my best.

09:04:07

11 Q Is there any reason you cannot give
12 accurate testimony today?

09:04:09

09:04:11

13 A I don't believe so.

09:04:12

14 Q Thanks. I'm going to hand you a copy of
15 what has been previously marked as Exhibit 1001 in
16 these proceedings. It's United States
17 Patent 8489837, and I would ask you to take a look
18 at that.

09:04:14

09:04:18

09:04:21

09:04:24

09:04:29

19 (Murphy Exhibit Number 1001 was marked for
20 identification.)

09:04:30

09:04:49

21 THE WITNESS: I have.

09:04:49

22 BY MR. MICALLEF:

09:04:49

23 Q Can we agree to refer to that as the '837
24 patent?

09:04:50

09:04:54

25 A Yes, we can.

09:04:54

1	Q	You have seen it before?	09:04:55
2	A	I have.	09:04:56
3	Q	You have read the whole thing?	09:04:56
4	A	I have.	09:04:58
5	Q	Did you read the whole thing in preparation	09:04:59
6		for this deposition today?	09:05:00
7	A	Yes.	09:05:02
8	Q	Okay. You will agree that the patent uses	09:05:02
9		the term "mode."	09:05:06
10	A	Yes, the patent does use the term "mode."	09:05:11
11	Q	Do you agree it uses the term "mode" in its	09:05:14
12		ordinary sense?	09:05:17
13		MR. ARJOMAND: Objection to form.	09:05:19
14		THE WITNESS: I have stated in my expert	09:05:20
15		report that it uses -- I believe it uses the term	09:05:23
16		"mode" given the claims construction I've provided.	09:05:26
17		So if you understand the quote ordinary sense to	09:05:31
18		mean that mode indicates different states of	09:05:35
19		behavior, then I would agree with you. And I think	09:05:40
20		that is what an ordinary person of skill in the art	09:05:44
21		would understand mode to be.	09:05:48
22		BY MR. MICALLEF:	09:05:49
23	Q	Do you think the patent uses the term	09:05:50
24		"mode" in a way that differs at all from what a	09:05:52
25		person of ordinary skill in the art would understand	09:05:55

1	the word "mode" to mean?	09:05:59
2	A No, I don't think so.	09:06:01
3	Q Okay. Thank you.	09:06:02
4	You agree that the '837 patent does not use	09:06:04
5	the phrase "behavioral state"?	09:06:06
6	A I believe that's accurate. My recollection	09:06:12
7	is that it is accurate, although it does use the	09:06:18
8	word "behavior."	09:06:21
9	Q Would you agree the '837 patent does not	09:06:21
10	explain how to tell one behavioral state from	09:06:26
11	another?	09:06:29
12	A No, I don't think that's true. I think	09:06:32
13	that the -- as I've said, the person of ordinary	09:06:39
14	skill in the art would understand that different	09:06:46
15	modes have different behavioral states, and it's	09:06:49
16	very well identified in the patent that the behavior	09:06:54
17	is different in, for instance, the initialization	09:06:57
18	mode or the operational mode. And, therefore, one	09:07:04
19	of a POSITA reading this document would understand	09:07:09
20	that that means there's different behavior in those	09:07:16
21	two different states.	09:07:19
22	Q My question was different than that. My	09:07:20
23	question was just would you agree the '837 patent	09:07:23
24	does not explain how to tell one behavioral state	09:07:25
25	from another?	09:07:28

1 A Maybe you need to be more clear to me on
2 what you mean by "explain." The patent definitely
3 talks about two different modes. It talks about
4 those modes having different behaviors. And the
5 operation that we see the part do in the different
6 modes is decidedly different. In fact, some of the
7 pins, for example, respond differently in one of the
8 modes versus another mode. And because of that, I
9 think a POSITA would definitely see that it does, in
10 effect, describe the behavioral state of those two
11 states that are shown as embodiments or in the
12 embodiments.

13 Q I'm not asking whether it describes the
14 behavioral state. I'm asking if the patent explains
15 how one can tell the difference between one
16 behavioral state and another?

17 MR. ARJOMAND: Objection. Asked and
18 answered.

19 THE WITNESS: Yeah, I think it does do
20 that. Let me see if I can find the best example of
21 that for you.

22 So in column 2 at the top in the middle
23 starting at column 1 at the bottom it says "In
24 certain embodiments, the memory module is configured
25 to operate in at least two modes comprising an

1 initialization mode during which the memory module
2 executes at least one initialization sequence and an
3 operational mode." And then the method may
4 compromise causing the memory module to enter the
5 initialization mode.

6 So it's pretty clear here, I think, that
7 the modes are entered into, and, therefore, they're
8 exited from their effective state, and the -- it's
9 well identified that the operational mode does not
10 include an initialization sequence.

11 BY MR. MICALLEF:

12 Q Where do you see in column 1, line 67
13 through column 2, line 10 where it says "The
14 operational mode does not include an initialization
15 sequence"?

16 A Well, it's stated in the fourth -- third
17 and fourth line of that column 2. The way the
18 language is written, a POSITA would read this and
19 say that the memory -- it says, for instance, in
20 line 3, "The memory module executes at least one
21 initialization sequence." And that's described as
22 when in the initialization mode in that sentence.
23 And then later it just says "an operational mode."

24 So by leaving out the information about the
25 initialization sequence, the document would explain

1 to a person of ordinary skill in the art that the 09:11:35
2 initialization sequence is in the initialization 09:11:37
3 mode, and there isn't an initialization sequence in 09:11:40
4 the operational mode. It's just not stated there. 09:11:43

5 Q It's not stated; so, therefore, you're 09:11:48
6 concluding it cannot be part of the operational 09:11:52
7 mode? 09:11:55

8 MR. ARJOMAND: Objection. Form. 09:11:57

9 THE WITNESS: No, I'm concluding that the 09:11:57
10 patentee described the initialization sequence as 09:12:00
11 being in the initialization mode, and he didn't 09:12:02
12 describe another initialization sequence being in 09:12:05
13 the operational mode. 09:12:09

14 BY MR. MICALLEF: 09:12:09

15 Q And so if I understand -- I mean, we 09:12:09
16 started this with my question about whether the 09:12:12
17 patent explains how to tell one behavioral state 09:12:15
18 from another, and you're pointing me to this 09:12:18
19 sentence which carries over from column 1 to 09:12:21
20 column 2 -- correct? -- as an example of that? 09:12:24

21 A As an example, yes. 09:12:29

22 Q Okay. So if I understand your position, 09:12:31
23 it's that this sentence explains how one would tell 09:12:33
24 the difference between these two particular 09:12:43
25 behavioral states which, I guess, you are 09:12:46

1 associating with operational mode and initialization
2 mode?

3 MR. ARJOMAND: Objection to form.

4 THE WITNESS: Yes, and you asked -- at
5 least my understanding of your question is that you
6 asked how or where the document describes two
7 different behavioral states, and I gave an
8 example -- I haven't picked it out of the document
9 yet, but there's an example of where the pins do
10 different things based on which mode it is in, and
11 I've given this from -- this piece of information
12 from the bottom of column 1 and the top of column 2.

13 BY MR. MICALLEF:

14 Q And so in that passage, column 1 to 2, what
15 you're really focusing on, I understand, is part of
16 the larger sentence, but the phrase you're focusing
17 on is this initialization mode during which the
18 memory module executes at least one initialization
19 sequence, and you're suggesting that a person of
20 ordinary skill in the art would understand that that
21 distinguishes the behavioral state of the
22 initialization mode from other behavioral states?

23 MR. ARJOMAND: Objection.

24 BY MR. MICALLEF:

25 Q Is that fair?

1	MR. ARJOMAND: Objection to form.	09:13:55
2	THE WITNESS: I don't know whether that's a	09:13:57
3	great characterization of what I said, but the --	09:13:58
4	the document here clearly shows that a certain type	09:14:03
5	of sequence is exercised and executed in one mode,	09:14:11
6	and the patentee had a choice to describe whether	09:14:17
7	that same sequence was available in the operational	09:14:20
8	mode and did not include it there.	09:14:25
9	So a POSITA would read this and assume that	09:14:28
10	the initialization sequence is only in the	09:14:34
11	initialization mode, and the fact that the two words	09:14:36
12	are both based on initialization, that would be a	09:14:39
13	reasonable conclusion for a POSITA to come to.	09:14:42
14	BY MR. MICALLEF:	09:14:44
15	Q But regardless of where the sequence	09:14:45
16	occurs, my point is distinguishing between	09:14:47
17	behavioral states, and so what I'm asking you is are	09:14:50
18	you saying that this is a passage from the patent	09:14:55
19	that explains how to distinguish one behavioral	09:14:57
20	state from another?	09:15:00
21	A Yeah, I think this passage is one of many	09:15:02
22	things that could be looked at to help describe how	09:15:07
23	a POSITA would understand the differences between	09:15:09
24	two behavioral states.	09:15:13
25	Q Okay. Now, that passage uses the term	09:15:15

1 "operational mode." What's your understanding of 09:15:23
2 the meaning of that? 09:15:26

3 A I generally think that the operational mode 09:15:27
4 is a mode -- sorry, I was going to say a mode of 09:15:36
5 operation. That's not a very good way to explain 09:15:41
6 it. A mode where the device is operating for its 09:15:43
7 primary intention. 09:15:50

8 Q What would the primary intention be in the 09:15:55
9 context of the '837 patent? 09:15:58

10 A Well, the primary intention is for the 09:16:01
11 memory modules to store information; right? And so 09:16:06
12 they store information given to them by the 09:16:09
13 computer, and then they retrieve that information 09:16:11
14 based on commands that they get from the CPU, for 09:16:16
15 example. 09:16:19

16 Q So are you -- we're talking about, let's 09:16:20
17 say -- let's put some adjectives on it. Standard 09:16:25
18 computer operations. Is that fair? 09:16:44

19 MR. ARJOMAND: Objection to form. 09:16:32

20 THE WITNESS: Standard computer operation. 09:16:33
21 At this point, I don't see anything objectionable 09:16:46
22 about that. I mean, in standard computer operation, 09:16:48
23 the CPU writes information to the memory devices, 09:16:51
24 and it reads information from the memory devices, 09:16:57
25 and that happens as a matter of course when the 09:17:00

1	computer is operating in its normal mode. So it	09:17:05
2	seems like that would match. I mean, we haven't	09:17:12
3	defined standard here so . . .	09:17:16
4	BY MR. MICALLEF:	09:17:18
5	Q Unfortunately, we haven't defined normal	09:17:19
6	either.	09:17:21
7	A Correct.	09:17:22
8	Q Let's see if we can caveat it a little.	09:17:23
9	Would you agree that the operational mode would not	09:17:27
10	be when the computer is booting up or powering down?	09:17:29
11	A Well, I would definitely agree that	09:17:34
12	operational mode would not be generally present when	09:17:42
13	you're booting up because there are certain	09:17:50
14	sequences at boot-up time that you do go through.	09:17:59
15	However, in some cases computer designers and	09:18:04
16	systems designers are very inventive. They can	09:18:09
17	actually do initialization sequences and normal	09:18:14
18	operations of some sort at the same time, and that	09:18:19
19	is well known in the industry that that can occur.	09:18:26
20	So I think you have to be careful about sort of what	09:18:33
21	you say about boot-up.	09:18:37
22	And then as far as booting a system down, I	09:18:42
23	think the same actually -- the same type of thing	09:18:49
24	applies when you turn a machine off. You may, for	09:18:54
25	instance, as part of a boot-down sequence simply	09:18:59

1 tell the machine, for instance, what's ever stored
2 in the cache before we turn the machine off, store
3 that somewhere so I can retrieve it later in which
4 case you're just going through normal reads and
5 writes to save the data that's in the cache maybe
6 out to the disk so that when you boot up next time
7 it's readily available and you can reload it into
8 the cache. So literally that group of normal reads
9 and writes would occur during -- or under the banner
10 of somebody saying, "Well, you're in boot-down mode
11 now. We're going to boot you down."

12 But before we do all of that, there are
13 certain pieces we're going to do, and one of those
14 pieces might be to just do normal reads and writes
15 as if you were still operating in a standard or
16 normal fashion.

17 Q Can I get you to turn to column 5 of the
18 '837 patent. At about line 46 there's a sentence,
19 46 through 48, that reads, "In one embodiment, for
20 example, at least one initialization sequence may
21 comprise one or more training sequences."

22 A I see it.

23 Q What's your understanding of a "training
24 sequence"?

25 A A training sequence, as an example, can be

1 a sequence in which you, in a special mode, you 09:20:45
2 operate the devices in a fashion -- the memory 09:20:54
3 devices in a fashion that lets you ascertain what 09:20:58
4 particular values to set parameters to -- the 09:21:05
5 example I'm thinking of is timing -- so that the 09:21:10
6 memory devices operate in the most optimum way. 09:21:15

7 Q Would such a sequence include the normal 09:21:23
8 reads and writes you referred to when you testified 09:21:27
9 about boot-down? 09:21:29

10 MR. ARJOMAND: Objection. Form. 09:21:34

11 THE WITNESS: No, I don't believe that it 09:21:38
12 would. 09:21:40

13 BY MR. MICALLEF: 09:21:40

14 Q What did you mean by normal read and write? 09:21:41

15 A In boot-down or in that sentence? 09:21:46

16 Q Let's start with boot-down. 09:21:50

17 A Well, in boot-down I thought I previously 09:21:53
18 described that before we turn the machine off, there 09:21:56
19 might be information that you want to save. So, for 09:21:59
20 instance, you might have programmed your laptop that 09:22:06
21 when you close the lid -- right? -- the laptop 09:22:10
22 actually boots down. It turns off, doesn't use any 09:22:15
23 power. 09:22:20

24 Q Okay. 09:22:23

25 A In an effort to make the boot-up process 09:22:25

1 quicker when you come back from that, some machines
2 will take all of the state that's in the CPU. Every
3 value stored in a register on a whole chip and store
4 it somewhere. And then when you tell the machine --
5 when you press the button to turn the machine on
6 again, it reloads all of that state, all the stored
7 values back into every one of those registers so
8 that the machine effectively comes up in the same
9 identical position it was in when you shut the
10 laptop.

09:22:29
09:22:33
09:22:37
09:22:40
09:22:44
09:22:46
09:22:51
09:22:54
09:22:58
09:23:01

11 So in doing that, there are a group of
12 commands which would be considered normal reads and
13 writes to go get that information and store it out
14 into a memory somewhere or on the disk.

09:23:02
09:23:05
09:23:07
09:23:11

15 Q What are the commands?

09:23:14

16 A What are the commands?

09:23:16

17 Q Yes.

09:23:17

18 A That do the storing?

09:23:18

19 Q The group of commands which would be
20 considered normal reads and writes is what you said.
21 What commands are you referring to?

09:23:21
09:23:23
09:23:28

22 A So you have to move the data from the CPU
23 because you're going to power the CPU down to some
24 non-volatile storage methodology. It could be a
25 flash. It could be a disk, a portion of the disk.

09:23:29
09:23:33
09:23:37
09:23:39

1	And so you have to do normal reads and writes to get	09:23:43
2	the data out of the CPU and into either the flash or	09:23:47
3	the disk.	09:23:52
4	Q Okay. Go ahead.	09:23:53
5	A Those normal reads and writes wouldn't look	09:23:57
6	any different from a normal read and write when you	09:24:00
7	sent memory -- you know, sent memory information to	09:24:04
8	the disk or sent memory information to the flash.	09:24:08
9	Q And in a training sequence, is there data	09:24:10
10	written to memory or read from memory?	09:24:14
11	A In general, the data written is not written	09:24:18
12	to the same piece of memory that the normal reads	09:24:24
13	and writes are writing to.	09:24:28
14	Q Tell me what the piece of memory that the	09:24:31
15	normal reads and writes are writing to is.	09:24:34
16	A As I just explained, the piece of memory	09:24:37
17	that the normal reads and writes are writing to, for	09:24:40
18	example, in the boot-down procedure would be the	09:24:44
19	disk drive or the -- or a flash if it has flash on	09:24:48
20	board. Obviously, normal reads and writes also	09:24:54
21	occur out to the DRAM memory that would be in a	09:24:57
22	system.	09:25:02
23	The reads and writes of information	09:25:02
24	occurring from the training procedure or the	09:25:06
25	training sequences, those pieces of information	09:25:16

1 would be stored in specialized areas, for instance,
2 in the memory controller or in the memory controller
3 portion of a processor if the memory controller is
4 integrated into the processor.

5 Q So you're saying training sequences never
6 write data into, for example, the DRAMs, the main
7 memory?

8 A They never write data into -- now you have
9 to help me understand what you mean by "data."
10 There are many types of data. Which type of data
11 are you talking about?

12 Q Let's just go broad. Write bits into main
13 memory. Would you agree that -- well, is it your
14 view that a training sequence would never write bits
15 in the main memory?

16 A Well, the training sequence never -- it
17 writes -- for instance, it would write specialized
18 bits in the memory devices, but they are not bits
19 that are used for normal reads and writes. For
20 instance, a configuration bit gets written.

21 Q Now, you're talking about the sequence of
22 bits that gets written are special?

23 MR. ARJOMAND: Objection. Form.

24 THE WITNESS: The sequence of bits that
25 gets written is special.

1 BY MR. MICALLEF:

09:27:03

2 Q You said "specialized bits." Bits are
3 usually 1s and 0s represented by voltages, and so
4 I'm kind of wondering what's special about your bits
5 that you're referring to.

09:27:04

09:27:06

09:27:06

09:27:10

6 A Well, in a standardized training sequence
7 for DRAM, it is a special mode. And to get into
8 that mode you have to literally tell the device, the
9 memory device, that I want you to go into that mode.
10 You have to enter this mode. In this case, I'm
11 thinking of the right leveling mode.

09:27:12

09:27:14

09:27:20

09:27:25

09:27:29

09:27:32

12 So to do that, somebody has to write a
13 different bit piece of data into an MR register
14 position in the memory device.

09:27:34

09:27:41

09:27:46

15 Now, standard or normal data that the
16 memory devices hold and give back to the computer --
17 right? -- are not the data that's stored in the MR
18 registers. The configuration bits are not normal
19 data that memory devices store for the user and then
20 give back.

09:27:50

09:27:55

09:28:01

09:28:06

09:28:11

09:28:16

21 Q Would a training sequence ever store bits
22 in the memory array of a memory device?

09:28:16

09:28:19

23 A At this point when you say "memory array,"
24 are you limiting yourself to the dynamic cells like
25 in a DRAM memory array?

09:28:25

09:28:41

09:28:45

1	Q	Let's start with that.	09:28:47
2	A	I don't believe it would do -- I don't	09:28:50
3		think I would necessarily say never, but I don't --	09:28:53
4		I can't think of a case when it does that.	09:28:57
5	Q	Okay. I want to direct your attention to a	09:28:59
6		different part of the '837 patent.	09:29:06
7	A	Okay.	09:29:08
8	Q	In column 6 beginning at line 27 through 33	09:29:09
9		it says, "For example, the system memory controller	09:29:18
10		14 may cause the memory module 10 to perform	09:29:22
11		standard operations such as memory read/write,	09:29:24
12		pre-charge, refresh, et cetera, while in operational	09:29:29
13		mode, although it will be appreciated that one or	09:29:32
14		more of these operations can also be performed by	09:29:35
15		the memory module 10 while in initialization mode in	09:29:38
16		certain embodiments."	09:29:42
17		Do you see that?	09:29:45
18	A	I do.	09:29:45
19	Q	Would you agree that a person -- at the	09:29:45
20		time of this patent, a person of ordinary skill in	09:29:49
21		the art would have understood this to be an accurate	09:29:52
22		statement?	09:29:55
23	A	Yes, I think they would.	09:30:04
24	Q	And would you understand memory read/write	09:30:14
25		to refer to the kind of commands that are used to	09:30:19

1	read to -- I'm sorry, read from or write data to,	09:30:25
2	say, the memory -- the array of the memory devices?	09:30:31
3	MR. ARJOMAND: Objection. Form.	09:30:35
4	THE WITNESS: I believe that this sentence	09:30:38
5	talks about operation -- standard operations that	09:30:40
6	are to the main memory array of a dynamic RAM. For	09:30:53
7	instance, pre-charge, refresh, memory read and	09:31:02
8	write, all occur in the main dynamic cells which we	09:31:04
9	call the main memory array, yes.	09:31:09
10	BY MR. MICALLEF:	09:31:12
11	Q And so the memory read and write here, what	09:31:12
12	one might call sort of the normal memory commands	09:31:15
13	that a memory controller or processor would issue to	09:31:19
14	read and write data out into main memory under	09:31:22
15	standard or regular use of a computer?	09:31:26
16	MR. ARJOMAND: Objection. Form.	09:31:31
17	THE WITNESS: I believe that to be the	09:31:32
18	case, yes.	09:31:33
19	BY MR. MICALLEF:	09:31:33
20	Q And the patent here says that those same	09:31:34
21	commands can be used in the initialization mode.	09:31:36
22	Agree with that?	09:31:38
23	A Yes.	09:31:40
24	Q Okay. And would you agree that the	09:31:41
25	interpretation, the proper interpretation on	09:31:45

1 initialization mode must be consistent with this
2 passage here at column 6, lines 27 through 33?

3 MR. ARJOMAND: Objection to form.

4 THE WITNESS: Well, if we're going to
5 determine what initialization mode means for use
6 within the document -- right? -- then it is the
7 normal occurrence that the definition is applied
8 equally in every place of its location.

9 BY MR. MICALLEF:

10 Q That wasn't my question.

11 A I'm sorry.

12 Q My question was wouldn't you agree that the
13 proper interpretation of initialization mode for
14 purposes of the '837 patent must be consistent with
15 this passage in column 6?

16 MR. ARJOMAND: Objection to form.

17 THE WITNESS: Well, I thought I answered
18 your question in that if you're looking for the
19 proper understanding of what initialization mode is
20 and you pick a construction for that term, what I
21 understand about how the law for patents is done is
22 that that construction must apply anywhere where the
23 term is used in the patent. And if it doesn't, then
24 it certainly raises a flag about whether that
25 construction's appropriate or not.

1 BY MR. MICALLEF:

09:33:57

2 Q You agree that the phrase "initialization
3 mode" is a claim term at issue or included in the
4 claims at issue in this proceeding?

09:33:58

09:34:01

09:34:04

5 MR. ARJOMAND: Objection to form.

09:34:06

6 THE WITNESS: It's certainly included in
7 the claims. I don't believe -- I believe Hynix has
8 included it as a construction --

09:34:08

09:34:09

09:34:21

9 BY MR. MICALLEF:

09:34:23

10 Q I just asked if it's in the claims?

09:34:23

11 MR. ARJOMAND: Counsel, he wasn't finished
12 with his question -- or the answer.

09:34:26

09:34:27

13 THE WITNESS: I'm sorry, could I hear the
14 question back again.

09:34:30

09:34:31

15 (Record read by the reporter as follows:

09:34:45

16 "QUESTION: You agree that the
17 phrase "initialization mode" is a
18 claim term at issue or included in
19 the claims at issue in this
20 proceeding?")

21 THE WITNESS: So I believe you asked about
22 two things there, not just in the claims but whether
23 it's a claim term.

09:34:46

09:34:47

09:34:52

24 BY MR. MICALLEF:

09:34:53

25 Q Well, let's make sure the record is clear.

09:34:53

1	It's a claim term; right? Initialization mode?	09:34:56
2	A I believe Hynix has offered it up as a	09:34:59
3	claim term. I don't believe Netlist has.	09:35:04
4	Q It is included in the claims at issue here;	09:35:06
5	correct?	09:35:11
6	A That I agree with.	09:35:11
7	Q Okay. And the interpretation of that	09:35:13
8	phrase, initialization mode, may be at issue between	09:35:16
9	the parties in this proceeding. Do you agree with	09:35:20
10	that?	09:35:23
11	A I do.	09:35:23
12	Q And in order -- what's your understanding	09:35:24
13	of how to interpret a claim term in a proceeding	09:35:27
14	such as this?	09:35:30
15	A My understanding is that it follows the	09:35:31
16	broadest reasonable interpretation from one of	09:35:34
17	ordinary skill in the art or from the Phillips	09:35:42
18	criteria which is the intrinsic data.	09:35:44
19	Q Those are two different standards, are they	09:35:49
20	not?	09:35:51
21	A Yes, they are.	09:35:52
22	Q Which one is at issue here?	09:35:52
23	A I believe the first one is at issue here.	09:35:54
24	Q And what's your understanding of what that	09:35:57
25	legal principle requires?	09:35:59

1	MR. ARJOMAND: Objection. Asked and	09:36:01
2	answered.	09:36:01
3	THE WITNESS: It requires the broadest	09:36:02
4	reasonable interpretation of one of ordinary skill	09:36:04
5	in the art.	09:36:12
6	BY MR. MICALLEF:	09:36:13
7	Q It requires the broadest reasonable	09:36:14
8	interpretation consistent with the specification of	09:36:17
9	the patent, doesn't it?	09:36:19
10	A I'm sorry. I forgot that part.	09:36:20
11	Q So that interpretation must be consistent	09:36:22
12	with the passage in column 6, lines 27 to 33 under	09:36:25
13	the law?	09:36:31
14	MR. ARJOMAND: Objection.	09:36:32
15	BY MR. MICALLEF:	09:36:33
16	Q Under the law. Do you agree with that?	09:36:33
17	MR. ARJOMAND: Objection to form.	09:36:35
18	THE WITNESS: I thought I answered this	09:36:36
19	already. I said that if the construction of the	09:36:37
20	claim -- if the construction of the claim term	09:36:45
21	"initialization mode," for example, is not usable as	09:36:50
22	a description in every occurrence of the term	09:36:58
23	"initialization mode" in the patent, then it's	09:37:05
24	probably suspect as a claims construction	09:37:09
25	definition.	09:37:14

1 BY MR. MICALLEF:

09:37:17

2 Q I'm going to place in front of you what's
3 been previously marked in this proceeding as
4 Exhibit 1005. It's the published -- the United
5 States patent application publication U.S.
6 2005/00715830 to LeClerc, et al., and ask you to
7 take a look at that.

09:37:32

09:37:34

09:37:37

09:37:41

09:37:47

09:37:53

8 (Murphy Exhibit Number 1005 was marked for
9 identification.)

09:37:53

09:37:53

10 THE WITNESS: I have it.

09:38:20

11 BY MR. MICALLEF:

09:38:21

12 Q Before we get to that, let me ask you a
13 question about your understanding of a little bit
14 more about patent law.

09:38:21

09:38:25

09:38:27

15 You referenced the Phillips claim
16 construction standard. Do you recall that?

09:38:29

09:38:31

17 A Yes.

09:38:33

18 Q Would you agree that under the Phillips
19 claim construction standard the interpretation of
20 initialization mode must also be consistent with the
21 passage in the '837 patent at column 6, lines 27 to
22 33?

09:38:33

09:38:36

09:38:38

09:38:41

09:38:46

23 A Well, I think, again, what I said for the
24 other question applies here, that any claims
25 construction proposition that doesn't fit inside of

09:38:49

09:38:55

09:38:59

1 the document, doesn't match up the intrinsic
2 information inside the document and for Phillips
3 it's only -- my understanding is it's only inside
4 intrinsic information -- if it doesn't match the
5 usage by the patent -- I mean, by the patentee in
6 those situations, then that claims construction
7 definition must be suspect.

8 Q So let's look at LeClerc. You've seen --
9 can we agree to refer to Exhibit 1005 as LeClerc?

10 A Yes.

11 Q You've seen this before?

12 A I have.

13 Q And you've read the whole thing?

14 A I have.

15 Q Did you read the whole thing in preparation
16 for your testimony today?

17 A I have.

18 Q Okay. I want to direct your attention
19 to -- I guess it would be paragraph 20. Just let me
20 know when you have that in front of you. Are you
21 ready for my question?

22 A I am.

23 Q Specifically I'd like to direct your
24 attention to the last sentence in paragraph 20 which
25 states, "In response to read commands, processor 102

1	receives data from memory controller 104."	09:41:01
2	Do you see that?	09:41:06
3	A I do.	09:41:06
4	Q So would you agree that this passage that I	09:41:07
5	just read into the record is not limited to the	09:41:14
6	actual data that is stored or retrieved in the	09:41:18
7	memory system, stored to or retrieved from the	09:41:24
8	memory system, I guess?	09:41:29
9	MR. ARJOMAND: Objection to form.	09:41:32
10	THE WITNESS: So from what I can see	09:41:56
11	literally here in paragraph 20, it doesn't -- it	09:41:58
12	doesn't specifically say what type of read or write	09:42:10
13	commands occur. They're just read or write	09:42:15
14	commands, and so at least in this -- just in this	09:42:20
15	passage it could be any type of read or write	09:42:25
16	command. Elsewhere in the document it may define	09:42:29
17	something else, but right here it only defines that.	09:42:36
18	BY MR. MICALLEF:	09:42:38
19	Q Okay. Would you agree that that could	09:42:38
20	refer to -- I mean, when I say that -- strike that.	09:42:42
21	Let me ask a more precise question.	09:42:49
22	In that sentence that I read, it uses the	09:42:51
23	word "data." So would you agree that that data	09:42:55
24	could include information that came from, for	09:42:58
25	example, registers in a memory system?	09:43:01

1 A In LeClerc's description of his patent
2 invention, yes, it could.

3 Q Okay. So I'd like to direct your attention
4 to paragraph 35, and the sentence in particular --
5 I'll give you a chance to read it if you want, but
6 just to focus this. The sentence I'd like to ask
7 you about is in the middle and it states, "Buffer
8 module 202 communicates with the memory controller
9 (e.g., controller 105) and/or upstream memory
10 modules (if any) via an upstream portion 210 of the
11 memory module channel (referred to herein as the
12 upstream channel)."

13 Do you see that sentence?

14 A I do.

15 Q There's no question that in LeClerc, the
16 buffer module communicates with the memory
17 controller over this upstream channel 210. Agreed?

18 MR. ARJOMAND: Objection.

19 THE WITNESS: This passage that you've
20 pointed me to and the specific sentence clearly lays
21 out the communications that go on between the buffer
22 module 202 and the memory controller 104.

23 BY MR. MICALLEF:

24 Q And those communications occur over this
25 upstream portion 210 which that passage refers to as

1	an upstream channel; correct?	09:45:34
2	A In general, I would say that's correct.	09:45:39
3	However, if you include the additional -- if you	09:45:52
4	include the additional fact that there could be	09:46:04
5	multiple memory modules, and we look specifically at	09:46:07
6	Figure 2, so if this is one memory module, and	09:46:10
7	there's another memory module -- right? -- so this	09:46:17
8	is labeled as -- sorry. I'm pointing to the	09:46:21
9	right-most side of Figure 2 at the top, the arrow	09:46:27
10	labeled 212. In the section we're talking about,	09:46:30
11	that's listed as the downstream channel.	09:46:34
12	Q Okay.	09:46:36
13	A My only point here is recognize that the	09:46:37
14	downstream channel at this module location becomes	09:46:40
15	the upstream channel when you look at the next-door	09:46:43
16	neighbors. So it will actually use both downstream	09:46:50
17	and upstream depending upon where in the module	09:46:55
18	hierarchy you're at.	09:47:00
19	Q But the downstream module would still be	09:47:01
20	communicating with the memory controller via its	09:47:04
21	upstream channel; correct?	09:47:06
22	A Yes. My point is it would be its upstream	09:47:07
23	channel and the next-door neighbor's downstream then	09:47:11
24	upstream channel.	09:47:18
25	Q I think I understand. Thank you.	09:47:19

1 Would you agree that those communications
2 could include an initialization status message?

3 MR. ARJOMAND: Objection to form.
4 BY MR. MICALLEF:

5 Q Just to be clear, let me strike that. I
6 want to make sure you understand my question.

7 Would you agree that the communication sent
8 from the buffer module 202 on the upstream channel
9 to the memory controller could include
10 initialization status messages?

11 A Based on what I've read in LeClerc, yes.

12 Q Okay. If I could direct your attention now
13 to paragraph -- well, paragraph 45 through 52, and
14 in particular, I want to ask you a question about
15 paragraph 46, but why don't you just take a look at
16 those passages and familiarize yourself with them
17 and let me know when you're ready for a question.

18 A And you specifically are going to ask about
19 46?

20 Q Correct.

21 A Okay. I'm ready.

22 Q And so in this patent -- well, in this set
23 of paragraphs, 45 through 52, it's talking --
24 LeClerc is discussing or describing the storage of
25 certain information in registers in the memory

1	system. Is that fair?	09:50:01
2	A That's correct.	09:50:03
3	Q Okay. And in 46 it states that there's a	09:50:04
4	certain start initialization register which	09:50:12
5	indicates to the quote, "initialization test	09:50:15
6	controller 304 that it should begin the process of	09:50:19
7	initializing its associated storage units."	09:50:23
8	Do you see that?	09:50:27
9	A I do.	09:50:28
10	Q And so this discloses that it is this	09:50:28
11	controller 304 that begins this process, what	09:50:33
12	LeClerc calls the process of initializing; correct?	09:50:37
13	A Well, the process actually got started at	09:50:42
14	the memory controller, and when the -- as I recall	09:50:51
15	from LeClerc when a particular memory module reads	09:51:02
16	information that is sent along the channel that is	09:51:07
17	directed to that memory module and decoded as being	09:51:12
18	a message for, for instance, for me -- right? --	09:51:15
19	then it will receive that, decode the message, and	09:51:21
20	then start the process of initialization on that	09:51:32
21	module.	09:51:37
22	Q Let's --	09:51:39
23	A So my only difference sort of from what you	09:51:40
24	asked is it doesn't all start within the memory	09:51:47
25	module itself. It's got to have a command from the	09:51:50

1	memory controller first to get this going.	09:51:53
2	Q Okay. Let's see if we can take it in	09:51:55
3	smaller parts.	09:51:58
4	A Sure.	09:51:58
5	Q This passage, this paragraph 46, refers to	09:51:59
6	this process of initializing?	09:52:02
7	A Yes.	09:52:04
8	Q Okay. Can we agree that's an	09:52:05
9	initialization sequence?	09:52:07
10	A Yes.	09:52:10
11	Q Okay. Can we agree that at least an	09:52:10
12	example of it is described with respect to Figure 5	09:52:15
13	of LeClerc?	09:52:19
14	MR. ARJOMAND: Objection to form.	09:52:20
15	THE WITNESS: I don't think -- well, this	09:53:00
16	section doesn't specifically call out Figure 5, and	09:53:09
17	when I read -- when I read the boldened numbers in	09:53:12
18	these paragraphs, I see 304, 306, and when I look at	09:53:21
19	Figure 5, I see them listed as 502, 504, 506, 508.	09:53:27
20	And I don't see -- if I scan up from 45, I don't see	09:53:41
21	a reference to Figure 5 here anywhere. So the	09:53:49
22	Figure 5 that you talked about is actually	09:54:21
23	referenced in paragraph 77.	09:54:25
24	BY MR. MICALLEF:	09:54:36
25	Q Okay. But are you telling me that you	09:54:36

1 think -- well, let me ask you this: Does Figure 5
2 describe a process of initializing associated memory
3 storage units?

4 MR. ARJOMAND: Objection to form.

5 BY MR. MICALLEF:

6 Q In your opinion.

7 A Well, in paragraph 77 it says, "Figure 5
8 illustrates a flow chart of a method for a memory
9 module to initialize memory." So, I mean, that
10 part's right there. It's just that in your question
11 you were associating paragraph 45 through 52,
12 paragraphs 45 through 52, with Figure 5, and I
13 couldn't see -- first of all, the numbering schemes
14 don't match. One set is 304 through 306 and the
15 other set is 502 through 508. And then secondly,
16 the names that are in parentheses in paragraph, for
17 instance, 46, 47, 48, and 49, they are start
18 initialization, start test, initialization complete,
19 and test complete. Those names don't match what we
20 see in Figure 5.

21 Q That may be so, but isn't the sort of
22 natural reading of LeClerg that the method of
23 initializing in Figure 5 is an example of the
24 process of initializing that's referred to in
25 paragraph 46?

1	MR. ARJOMAND: Objection to form.	09:56:13
2	THE WITNESS: I don't see that laid out	09:56:16
3	here for a person reading this patent at all.	09:56:18
4	BY MR. MICALLEF:	09:56:22
5	Q Okay. Well, let me ask it the other way.	09:56:22
6	You think they are not the same thing or one is not	09:56:27
7	the example of the other?	09:56:29
8	MR. ARJOMAND: Objection to form.	09:56:32
9	THE WITNESS: No, I didn't say that. You	09:56:32
10	asked me a question about 46 -- paragraphs 46	09:56:35
11	through 52 relating to Figure 5, and in the document	09:56:41
12	Figure 5 is specifically related to by paragraphs,	09:56:48
13	as I said, 77 through 84.	09:56:50
14	BY MR. MICALLEF:	09:56:54
15	Q I hear you. I just want to know -- you	09:56:55
16	know, you told me that you don't think Figure 5 is	09:56:57
17	an example of the process of initializing 46, but	09:57:00
18	then I thought I heard you say you're not going to	09:57:06
19	say it's not an example either. So does that mean	09:57:08
20	you don't have an opinion on it?	09:57:11
21	MR. ARJOMAND: Objection to form. Asked	09:57:13
22	and answered.	09:57:14
23	THE WITNESS: So the thing that's unclear	09:57:17
24	from how you've posed the question is whether or not	09:57:21
25	these two pieces -- sections of the document, so	09:57:26

1 paragraphs 45 through 52 or the one I picked out,
2 paragraphs 77 to 84, are actually related to the
3 same thing.

4 BY MR. MICALLEF:

5 Q That's what I'm asking you, for your
6 opinion.

7 A Right. And so in looking at the document,
8 I looked for what any standard POSITA would look
9 for. Are the numbers the same? The answer is no.
10 Are the names the same? The answer is no. Does
11 that mean I can conclude that they're not about the
12 same thing? Well, the answer is no. I can't
13 conclude that without a proper analysis.

14 Q So as you sit here today, you cannot tell
15 me one way or the other whether Figure 5 is an
16 example of the process of initializing referred to
17 in paragraph 46; correct?

18 MR. ARJOMAND: Objection to form. Asked
19 and answered.

20 THE WITNESS: Well, 45 isn't -- isn't
21 describing a process. See, that's part of the
22 problem.

23 BY MR. MICALLEF:

24 Q I said 46, sir.

25 A Okay. But 45 is the prelude to 46 through

1	52; correct?	09:58:58
2	Q Sir, can you answer my question? Would you	09:58:59
3	like it read back?	09:59:02
4	A Sure.	09:59:03
5	(Record read by the reporter as follows:	09:59:18
6	"QUESTION: So as you sit here	
7	today, you cannot tell me one way or	
8	the other whether Figure 5 is an	
9	example of the process of	
10	initializing referred to in	
11	paragraph 46; correct?")	09:59:18
12	MR. ARJOMAND: Same objections for the	09:59:19
13	record.	09:59:20
14	THE WITNESS: I think the reason that	09:59:43
15	there's confusion about this is that what's	09:59:45
16	described in 46 through 52 is identified in the	09:59:47
17	paragraph above, 45. In paragraph 45 at the end it	09:59:52
18	says, "In one embodiment, the registers 306 include	10:00:00
19	at least the following information." So 46 through	10:00:03
20	52 is not telling you about the process. It's	10:00:08
21	telling you about where information in that process	10:00:12
22	is stored. And Figure 5 specifically talks about in	10:00:15
23	column 77 through 84 the actual process or method	10:00:21
24	that's being done to initialize, and I think that's	10:00:27
25	the difference.	10:00:30

1	BY MR. MICALLEF:	10:00:35
2	Q So you can't say one way or the other, can	10:00:35
3	you?	10:00:38
4	MR. ARJOMAND: Objection to form. Asked	10:00:38
5	and answered.	10:00:39
6	THE WITNESS: I'm sorry. I can't say one	10:00:40
7	way or another what?	10:00:43
8	BY MR. MICALLEF:	10:00:43
9	Q Whether Figure 5 is an example of the	10:00:44
10	process of initializing referred to in paragraph 46.	10:00:47
11	MR. ARJOMAND: Objection to form. Asked	10:00:54
12	and answered.	10:00:57
13	THE WITNESS: So 46 does not describe a	10:01:06
14	process of initializing. 46 describes a piece of	10:01:09
15	information that is in a register.	10:01:13
16	BY MR. MICALLEF:	10:01:15
17	Q Sir, I didn't say describes. I said it	10:01:16
18	refers to a process of initializing.	10:01:18
19	A Refers to -- 46 still does not refer to a	10:01:20
20	process of initializing. It refers to a piece of	10:01:28
21	data stored in a register.	10:01:32
22	Q Okay. Your reading of 46 is that it does	10:01:36
23	not refer to the process of initializing its	10:01:43
24	associated storage units; is that right?	10:01:45
25	A It just says that the bit indicates that	10:02:01

1 the initialization test controller should begin the 10:02:06
2 process. It doesn't define the process. 10:02:08

3 Q So I can tell the board at the oral hearing 10:02:11
4 that Mr. Murphy said paragraph 46 does not refer to 10:02:14
5 quote, the process of initializing its associated 10:02:20
6 storage units, end quote. Correct? 10:02:22

7 MR. ARJOMAND: Objection to form. Asked 10:02:26
8 and answered. 10:02:27

9 THE WITNESS: No. That's not correct. 10:02:27

10 BY MR. MICALLEF: 10:02:29

11 Q So I can tell the board that you agree it 10:02:29
12 refers to a process of initializing; right? 10:02:32

13 A The problem with the question you've asked 10:02:34
14 is you've specifically pointed me to Figure 5 which 10:02:37
15 is not listed here. 10:02:41

16 Q Sir, your counsel is here to make 10:02:43
17 objections. I just want answers to my questions. 10:02:46

18 A Okay. 10:02:48

19 Q And you do agree it refers to a process of 10:02:51
20 initializing, but you're not going to tell me 10:02:54
21 whether Figure 5 is an example of that or not. Is 10:02:56
22 that fair? 10:03:02

23 MR. ARJOMAND: Objection to form. Asked 10:03:02
24 and answered. 10:03:05

25 THE WITNESS: So the question I understand 10:03:15

1 is really compound. A, you want to know if 46 10:03:18
2 refers to a process of initialization, and clearly, 10:03:23
3 the words are right there. Right? Then the second 10:03:29
4 part of the compound question is is Figure 5 an 10:03:34
5 explanation of an initialization process. Do I 10:03:41
6 understand you correctly? Did your question have 10:03:51
7 those two pieces to it? 10:03:54

8 BY MR. MICALLEF: 10:03:56

9 Q Let's answer those two. 10:03:56

10 A Okay. 10:03:58

11 Q Let's take them apart with the second one 10:03:59
12 first. Is Figure 5 an example of the process of 10:04:02
13 initializing that's referred to in paragraph 46? 10:04:06

14 MR. ARJOMAND: Objection. Asked and 10:04:13
15 answered. 10:04:15

16 THE WITNESS: So the process that is shown 10:05:00
17 in Figure 5 and is described through paragraph 77 10:05:01
18 through 84 is a process and method for initializing 10:05:07
19 a memory as detailed in paragraph 77. And down in 10:05:18
20 paragraph 82, inside of that process -- number 4 10:05:26
21 states that "Inside of that process, the embodiment 10:05:40
22 it is describing includes initializing a start 10:05:48
23 initialization register to include a value that 10:05:54
24 indicates to the initialization test controller 10:05:56
25 (example module 304) that it should begin the 10:06:02

1 initialization process."

10:06:05

2 And figure -- sorry, paragraph 46 talks

10:06:09

3 about "The data that is stored in a start

10:06:14

4 initialization register which indicates to the

10:06:18

5 initialization test/controller 304 that it should

10:06:20

6 begin the process of initializing its associated

10:06:23

7 storage units." So they are connected in that

10:06:27

8 fashion.

10:06:30

9 BY MR. MICALLEF:

10:06:31

10 Q So do you think the initialization process

10:06:33

11 referred to in paragraph 82 is the process of

10:06:36

12 initialization -- excuse me, initializing referred

10:06:40

13 to in paragraph 46?

10:06:44

14 THE WITNESS: Could you read that back to

10:06:52

15 me.

10:06:54

16 (Record read by the reporter as follows:

10:07:09

17 "QUESTION: So do you think the

18 initialization process referred to in

19 paragraph 82 is the process of

20 initialization -- excuse me,

21 initializing referred to in

22 paragraph 46?")

23 THE WITNESS: I think what's shown in 4 is

10:07:20

24 a --

10:07:27

25 BY MR. MICALLEF:

10:07:27

1	Q	In 4?	10:07:27
2	A	I'm sorry, what's listed as number 4 in	10:07:30
3		paragraph 82.	10:07:32
4	Q	Okay.	10:07:33
5	A	Is a subsection of the process of	10:07:34
6		initializing that's talked about in paragraph 46.	10:07:38
7	Q	Can you tell me what else would be part of	10:07:52
8		that process of initializing referred to in	10:07:55
9		paragraph 46?	10:07:58
10	A	Well, I think that's pretty clearly laid	10:07:58
11		out in paragraph 77 through 84 where it details a	10:08:00
12		method for memory module to initialize memory.	10:08:07
13	Q	Okay. Would you agree that the	10:08:09
14		initialization process referred to in paragraph 82	10:08:18
15		is an initialization sequence for purposes of the	10:08:22
16		claims of the '837 patent?	10:08:26
17	MR. ARJOMAND:	Objection to form.	10:08:30
18	THE WITNESS:	Well, paragraph 82 only	10:08:37
19		details a single item, and in my mind, and I think	10:08:56
20		in a POSITA's mind, a sequence is a group of things	10:09:01
21		that happen. So the way you phrased the question,	10:09:05
22		at least how I understood it, 82 doesn't describe a	10:09:10
23		sequence. It describes a portion of a sequence	10:09:14
24		because it's -- it is only describing initializing a	10:09:19
25		start initialization register.	10:09:26

1	BY MR. MICALLEF:	10:09:28
2	Q I was referring to the phrase	10:09:28
3	"initialization process," though. That's what my	10:09:30
4	question asked about. Would you agree that that's	10:09:32
5	an initialization sequence?	10:09:37
6	MR. ARJOMAND: Objection to form.	10:09:38
7	THE WITNESS: Oh, that the initialization	10:09:39
8	process is an initialization sequence?	10:09:40
9	BY MR. MICALLEF:	10:09:42
10	Q Yes, sir.	10:09:43
11	A I think that's a reasonable understanding	10:09:44
12	for one of ordinary skill in the art, yes.	10:09:52
13	MR. MICALLEF: I think we've been going for	10:09:58
14	an hour and ten minutes. Would you like to take a	10:09:59
15	break?	10:10:02
16	THE WITNESS: No, I'm good. Thank you.	10:10:06
17	MR. MICALLEF: I have to look at your	10:10:09
18	counsel in case any of them have their legs crossed.	10:10:11
19	BY MR. MICALLEF:	10:10:36
20	Q So in paragraph 86, if I could direct your	10:10:36
21	attention there.	10:10:39
22	A I see 86.	10:10:43
23	Q Okay. And it refers to writing the	10:10:44
24	initialization data value to the first address	10:10:49
25	incrementing the address register to the next	10:10:52

1 location and repeating the process until the 10:10:54
2 initialization data value has been written to the 10:10:57
3 last address. 10:10:59

4 Would you agree that that would be part of 10:11:02
5 the initialization process referred to in 10:11:07
6 paragraph 82? 10:11:11

7 A And by "in paragraph 82," you're only 10:11:18
8 referring to the last three words, "the 10:11:21
9 initialization process"? 10:11:25

10 Q Yes. I'm focusing on that and not the 10:11:26
11 initialization of that register. 10:11:29

12 A Okay. Yes, the sentence you described 10:11:30
13 would be part of the initialization process. 10:11:46

14 Q And so given this description in 10:11:48
15 paragraph 86, would it be fair to assume that the -- 10:11:56
16 excuse me, the initialization process includes 10:12:02
17 writing data, initialization data, to certain memory 10:12:05
18 locations and then reading it back from those memory 10:12:10
19 locations? 10:12:15

20 MR. ARJOMAND: Objection to form. 10:12:16

21 THE WITNESS: The sentence that you pointed 10:12:18
22 to describes writing the initialization data value 10:12:19
23 to the first address, incrementing it, and it 10:12:27
24 doesn't talk about reading it back because the 10:12:32
25 initialization is -- the initialization, at least in 10:12:35

1	LeClerc, is only the writing to.	10:12:43
2	BY MR. MICALLEF:	10:12:46
3	Q Okay. Is that because LeClerc describes	10:12:47
4	the reading back as the test?	10:12:50
5	A Yes.	10:12:53
6	Q Okay. So it's not just writing to that's	10:12:53
7	described here. It's sort of writing to sequential	10:12:59
8	memory locations; correct?	10:13:05
9	MR. ARJOMAND: Objection.	10:13:06
10	THE WITNESS: I don't see the word	10:13:07
11	"sequential" anywhere in here, so -- and I believe I	10:13:09
12	don't remember the particular paragraph. But I	10:13:12
13	believe it's stated somewhere here that it can be	10:13:15
14	non-sequential and in certain -- in certain memory	10:13:19
15	test programs, for example, writing to the memory is	10:13:26
16	not done sequentially.	10:13:31
17	BY MR. MICALLEF:	10:13:32
18	Q Well, perhaps so, but in paragraph 86 it	10:13:33
19	refers to incrementing the address register to the	10:13:37
20	next location and repeating the process.	10:13:38
21	Do you see that?	10:13:40
22	A I understand that that is what is said.	10:13:41
23	But I also understand that because you have a	10:13:47
24	separate chip that's driving this initialization and	10:13:50
25	because one understands from reading the document	10:13:56

1 that there will be tests afterwards, and then 10:14:01
2 knowing that memory devices have certain patterns 10:14:05
3 that make them fail worse than other patterns, the 10:14:09
4 next location may be not necessarily the next 10:14:14
5 sequential location. You could, for instance, write 10:14:20
6 all the bits on a single column on a single row, and 10:14:24
7 the next location address-wise is just not the next 10:14:30
8 digital increment. 10:14:34

9 Q I see. Well, would you agree that even 10:14:35
10 with that explanation, this kind of writing to a 10:14:39
11 memory location, then incrementing the address 10:14:44
12 register to the next location, and then repeating 10:14:48
13 the process until you get to whatever last address 10:14:50
14 you're looking for, that's not the kind of thing 10:14:54
15 that the system would do in the operational mode? 10:14:59

16 MR. ARJOMAND: Objection to form. 10:15:02

17 THE WITNESS: Well, LeClerc only has two 10:15:17
18 modes; so it has sleep mode and normal mode. So in 10:15:19
19 LeClerc it actually does initialization and, 10:15:27
20 quote/unquote, normal operations in the same mode, 10:15:31
21 in the normal mode. 10:15:34

22 BY MR. MICALLEF: 10:15:35

23 Q Would you agree that what I read there in 10:15:37
24 paragraph 86 is not the kind of thing a computer 10:15:39
25 would do during standard operating while it's being 10:15:42

1	operated by a user for its normal purposes?	10:15:51
2	MR. ARJOMAND: Objection to form.	10:15:54
3	THE WITNESS: I don't believe that's true	10:16:03
4	based on what LeClerc has said in other places in	10:16:05
5	the document. He specifically talks about doing	10:16:08
6	initialization when a memory module comes out of	10:16:16
7	sleep mode. And it's well known that memory modules	10:16:20
8	get turned off and on based on their potential usage	10:16:24
9	to save power. So the machine could be working with	10:16:28
10	modules 2 through 8 in a normal mode, and module 1	10:16:33
11	could have been put into a sleep mode and then woken	10:16:42
12	up and be going through initialization while the	10:16:48
13	other modules are operating in normal fashion. So I	10:16:51
14	don't think I agree with you.	10:16:55
15	BY MR. MICALLEF:	10:16:57
16	Q I'd like to direct your attention to	10:16:58
17	paragraph 73 of LeClerc and, in particular, the	10:17:05
18	second sentence which states, "In an alternate	10:17:09
19	embodiment, the processor instead sends a start	10:17:13
20	initialization and a start test command to the	10:17:17
21	memory controller, and the memory controller	10:17:19
22	generates and sends the module initialization and	10:17:21
23	memory test commands to the memory modules."	10:17:24
24	Do you see that?	10:17:27
25	A I do.	10:17:27

1	Q	So would you agree that in that sentence	10:17:27
2		the processor is not sending commands directly to	10:17:31
3		the memory module?	10:17:35
4	A	Well, it says that the processor is sending	10:17:38
5		commands to the memory controller; so the answer is	10:17:44
6		yes.	10:17:47
7	Q	Would you also agree that what gets sent to	10:17:47
8		the memory controller from the processor is	10:17:52
9		something different from what the memory controller	10:17:54
10		sends to the memory module in that sentence?	10:17:56
11	A	I don't think that sentence necessarily	10:18:00
12		implies that. You're, I think, reading the word	10:18:16
13		"generates" to mean that it has changed the commands	10:18:25
14		given to the memory controller from the processor in	10:18:29
15		some fashion and then shipped them off to the	10:18:32
16		modules. But generates can easily just mean pass	10:18:35
17		through. I got the commands from the memory	10:18:41
18		controller, and I'm passing them through to the	10:18:43
19		module.	10:18:46
20	Q	But what I was really looking at was the	10:18:46
21		fact that the things that get sent from the	10:18:50
22		processor to the memory controller have certain	10:18:52
23		names, and the things that get passed from the	10:18:54
24		memory controller to the memory module have	10:18:56
25		different names. Wouldn't that suggest they are	10:18:58

1	different things?	10:19:01
2	MR. ARJOMAND: Objection to form.	10:19:02
3	THE WITNESS: From an engineering sense,	10:19:20
4	not necessarily so. The names may just indicate	10:19:21
5	where the signals are coming from, for example. So	10:19:24
6	the -- sometimes names are given different --	10:19:27
7	sometimes names are given different words so that	10:19:37
8	they identify where you're talking about the signal	10:19:41
9	being. So, for instance, we see start	10:19:44
10	initialization, and we see module initialization.	10:19:46
11	It could be that those words just mean the start --	10:19:53
12	an engineer looking at this would know, for example,	10:19:58
13	that any time he sees a start initialization	10:20:01
14	command, he knows it's coming from the processor,	10:20:04
15	and the memory -- the module initialization words	10:20:08
16	basically knows he's dealing with the same -- could	10:20:10
17	be the same signal coming from the memory	10:20:13
18	controller, and that's an example of a pretty common	10:20:17
19	engineering usage. So I don't think it's definitive	10:20:19
20	one way or the other.	10:20:23
21	BY MR. MICALLEF:	10:20:23
22	Q And that, of course, could not be the	10:20:24
23	example here, though, because the sentence before	10:20:26
24	what I read you says that the module initialization	10:20:29
25	and module test commands come from the processor;	10:20:33

1	correct?	10:20:44
2	MR. ARJOMAND: Objection to form.	10:20:44
3	THE WITNESS: No, I don't believe so	10:20:45
4	because in the alternate embodiment, it's describing	10:20:47
5	the processor sending the commands to a memory	10:20:51
6	controller and the memory controller sending them to	10:20:56
7	the -- to the module.	10:21:02
8	BY MR. MICALLEF:	10:21:04
9	Q But it is certainly the case that the name	10:21:04
10	module initialization command does not differentiate	10:21:06
11	between whether it came from the processor or the	10:21:11
12	memory controller like you were suggesting could be	10:21:14
13	the case. Isn't that right, sir?	10:21:17
14	A That's not right because each of those	10:21:19
15	sentences are prescribed as being in specific	10:21:23
16	embodiments. So understanding what the embodiment	10:21:29
17	is lets you interpret what the words mean; right?	10:21:31
18	In the first embodiment described, it's the	10:21:38
19	processor that sends the commands directly to the	10:21:41
20	memory module, and they are, therefore, called	10:21:45
21	module initialization and module test. And in that	10:21:48
22	embodiment since it's described as not having a	10:21:53
23	memory controller, and it's described as the	10:21:56
24	processor sending those things, then it's known in	10:21:58
25	that embodiment that those names come from the	10:22:01

1	processor.	10:22:04
2	Q I'm sorry. Are you suggesting that the	10:22:04
3	embodiment of the first sentence of paragraph 73 is	10:22:06
4	described as not having a memory controller?	10:22:10
5	A No, I said the processor sends the commands	10:22:15
6	to the memory module.	10:22:19
7	Q You said "in that embodiment since it's	10:22:20
8	described as not having a memory controller." That	10:22:24
9	wasn't right, was it?	10:22:28
10	A So in 73 in the first sentence it	10:23:06
11	specifically says "The processor sends module	10:23:14
12	initialization and module test commands to each	10:23:16
13	memory module."	10:23:20
14	Q It never says that it is described as not	10:23:21
15	having a memory controller. In fact, it says -- it	10:23:25
16	describes exactly the opposite of that. Isn't that	10:23:27
17	right?	10:23:31
18	MR. ARJOMAND: Objection to form. Asked	10:23:32
19	and answered.	10:23:34
20	THE WITNESS: I'm sorry. I don't see	10:23:46
21	memory controller in the paragraphs above at all.	10:23:48
22	Let me take a look.	10:23:57
23	No, I believe I'm reading it the right way.	10:24:52
24	I don't see memory controller described in 72,	10:24:56
25	paragraph 72, or 71 or paragraph 70 or paragraph 69.	10:25:01

1	And 73 starts with "in an above-described	10:25:15
2	embodiment." How many paragraphs do I have to go	10:25:22
3	back till I find that particular embodiment that has	10:25:25
4	a memory controller in it?	10:25:29
5	BY MR. MICALLEF:	10:25:30
6	Q How about none? Let's talk about	10:25:30
7	paragraph 73, which actually says, "In an	10:25:32
8	above-described embodiment, the processor, e.g.,	10:25:35
9	processor 102, (Figure 1), which is a system	10:25:38
10	(Figure 1), that has a memory controller."	10:25:41
11	Isn't that right?	10:25:44
12	A It does have a memory controller, but this	10:25:45
13	sentence says that the processor sends the commands	10:25:48
14	to the module.	10:25:51
15	Q And so you want the board to believe that	10:25:52
16	this sentence that refers to the processor of	10:25:54
17	Figure 1 doesn't actually refer to the system of	10:25:57
18	Figure 1 that has a memory controller. That's your	10:25:59
19	testimony, sir; right?	10:26:03
20	MR. ARJOMAND: Objection to form.	10:26:04
21	THE WITNESS: Unless you're trying to tell	10:26:06
22	me that this sentence is lying because it literally	10:26:07
23	says the processor sends module initialization and	10:26:11
24	module test commands to each memory module.	10:26:16
25	///	

1	BY MR. MICALLEF:	10:26:18
2	Q And there's no reason that a processor	10:26:18
3	can't do that through a memory controller; correct?	10:26:21
4	A But if that's the case, in the alternate	10:26:37
5	embodiment below, why does it specifically state	10:26:40
6	that it sends the commands to the memory controller?	10:26:43
7	Q Well, I'm not here to answer your	10:26:45
8	questions. You're here to answer mine. So here's	10:26:49
9	one: You don't have any understanding of why it	10:26:52
10	does that. You don't have any reasonable	10:26:55
11	explanation because you don't understand this	10:26:57
12	paragraph; correct?	10:26:59
13	MR. ARJOMAND: Objection to form.	10:26:59
14	THE WITNESS: I don't believe that's	10:27:03
15	correct. I believe I understand the paragraph.	10:27:04
16	BY MR. MICALLEF:	10:27:05
17	Q Then give me a reasonable explanation.	10:27:05
18	MR. ARJOMAND: Objection to form.	10:27:10
19	THE WITNESS: I did give you a reasonable	10:27:10
20	explanation.	10:27:12
21	BY MR. MICALLEF:	10:27:15
22	Q Your question, sir, but if that's the case	10:27:15
23	in the alternate embodiment below, why does it	10:27:21
24	specifically state that it sends the commands to the	10:27:24
25	memory controller. Answer your own question. Why?	10:27:27

1	A	Because it's trying to differentiate itself	10:27:30
2		from the sentence above.	10:27:32
3	Q	And so you want the board to believe the	10:27:34
4		sentence above which refers to Figure 1 doesn't	10:27:36
5		include a memory controller even though Figure 1 has	10:27:40
6		a memory controller and Figure 1 is an embodiment	10:27:44
7		described above and this patent plainly states --	10:27:47
8		plainly states that the memory controller can take	10:27:51
9		commands, initialization commands, from the	10:27:54
10		processor and send them -- pass them through to the	10:27:56
11		memory module. That's what you want the board --	10:28:01
12		you want the board to read all that out of there; is	10:28:03
13		that right?	10:28:07
14	A	No.	10:28:07
15		MR. ARJOMAND: Objection to form.	10:28:09
16		THE WITNESS: One of the other things that	10:28:09
17		the patent talks about is the memory controller is	10:28:10
18		subsumed inside the processor itself.	10:28:13
19		BY MR. MICALLEF:	10:28:15
20	Q	Sir, agreed that this patent says the	10:28:16
21		memory controller can just pass commands from the	10:28:18
22		processor through the memory module?	10:28:20
23	A	I just don't see -- I don't see that here	10:28:22
24		in this paragraph.	10:28:26
25	Q	I'm asking you, wouldn't you agree that	10:28:26

1	elsewhere in this patent it says exactly that?	10:28:28
2	MR. ARJOMAND: Objection to form.	10:28:32
3	THE WITNESS: Elsewhere in the patent it	10:28:32
4	says that that can be done, but in this paragraph it	10:28:35
5	doesn't say that.	10:28:37
6	BY MR. MICALLEF:	10:28:38
7	Q But in an above-described embodiment from	10:28:38
8	this paragraph, it does say that, doesn't it?	10:28:41
9	MR. ARJOMAND: Objection to form.	10:28:46
10	THE WITNESS: Well, it says both things	10:28:50
11	that we've talked about.	10:28:52
12	BY MR. MICALLEF:	10:28:53
13	Q My question is just about one. We're	10:28:53
14	looking at paragraph 73 in an above-described	10:28:56
15	embodiment. There is an embodiment above that	10:29:00
16	paragraph that has the processor sending commands to	10:29:03
17	a memory module through the memory controller;	10:29:06
18	correct?	10:29:11
19	MR. ARJOMAND: Objection to form. Asked	10:29:11
20	and answered.	10:29:12
21	THE WITNESS: There is one of those, but	10:29:16
22	that doesn't mean it's the only one.	10:29:18
23	BY MR. MICALLEF:	10:29:19
24	Q And it's the one of Figure 1. It's the	10:29:19
25	embodiment of Figure 1, isn't it?	10:29:22

1	MR. ARJOMAND: Objection to form.	10:29:24
2	THE WITNESS: It certainly references you	10:29:34
3	to Figure 1, but I don't think your reading includes	10:29:37
4	all of the possible information there.	10:29:40
5	BY MR. MICALLEF:	10:29:41
6	Q Okay. Let's take a break.	10:29:42
7	THE VIDEOGRAPHER: We are now going off the	10:29:45
8	record, and the time is 10:30 a.m.	10:29:47
9	(Recess taken from 10:29 a.m. to	10:29:51
10	10:43 a.m.)	10:43:41
11	THE VIDEOGRAPHER: We are now going back on	10:43:42
12	the record, and the time is 10:44 a.m.	10:43:44
13	BY MR. MICALLEF:	10:43:48
14	Q Mr. Murphy, I'm going to hand you a	10:43:49
15	document that has been previously marked as	10:43:51
16	Exhibit 2001 in this proceeding entitled	10:43:55
17	"Declaration of Robert J. Murphy," and I will ask	10:43:59
18	you to take a look at that.	10:44:04
19	A Thank you.	10:44:06
20	(Murphy Exhibit Number 2001 was marked for	10:44:42
21	identification.)	10:45:05
22	THE WITNESS: I have it.	10:45:05
23	BY MR. MICALLEF:	10:45:06
24	Q Okay. And you've seen that document	10:45:06
25	before?	10:45:07

1	A	I have.	10:45:08
2	Q	It is your declaration?	10:45:08
3	A	It is.	10:45:10
4	Q	And your signature is on the back? Close	10:45:10
5		to the back I should say, page 54?	10:45:18
6	A	Yes.	10:45:20
7	Q	And you have been retained by Netlist to	10:45:21
8		submit or put this declaration together and submit	10:45:27
9		it in this proceeding?	10:45:30
10	A	Yes.	10:45:31
11	Q	Part of that retention, is it fair to say,	10:45:33
12		was to come here today and testify about it?	10:45:38
13	A	Yes.	10:45:40
14	Q	And you've been paid to -- for your time in	10:45:41
15		drafting the declaration. Agreed?	10:45:46
16	A	Yes.	10:45:48
17	Q	And you're being paid for your time to	10:45:48
18		testify today?	10:45:51
19	A	Yes.	10:45:51
20	Q	At what rate or what's your compensation	10:45:51
21		for these activities?	10:45:54
22	A	\$475 an hour.	10:45:55
23	Q	Can you estimate how much time you've spent	10:45:58
24		before today on this project?	10:46:05
25	A	No, not really. I don't know exactly.	10:46:15

1	Q	Over a hundred hours?	10:46:17
2	A	I don't think so, but that's just my best	10:46:21
3		guess.	10:46:33
4	Q	Over 50?	10:46:34
5	A	Yes.	10:46:38
6	Q	Okay. And your declaration, you have	10:46:38
7		reviewed it recently?	10:46:42
8	A	I have.	10:46:44
9	Q	What was the last time you read it?	10:46:44
10	A	Last night.	10:46:46
11	Q	Okay. Did you notice any mistakes?	10:46:47
12	A	No, but I wasn't really looking for	10:46:54
13		mistakes so . . .	10:46:58
14	Q	Okay. What were you looking for?	10:46:58
15	A	Just to refresh my memory of what was in	10:47:03
16		the document.	10:47:06
17	Q	Okay. I'd like to direct your attention to	10:47:07
18		paragraph 22, which is on page 11 of your	10:47:16
19		declaration. Do you have that in front of you?	10:47:19
20	A	I do.	10:47:29
21	Q	The first sentence of that paragraph says,	10:47:30
22		"The inventor rejected the use of polling to	10:47:34
23		determine the end of the initialization process, and	10:47:38
24		instead, advocated the use of notifying."	10:47:41
25		Do you see that sentence?	10:47:44

1	A	I do.	10:47:45
2	Q	Is it fair to say that in that sentence you	10:47:46
3		are offering the opinion that the invention of the	10:47:54
4		'837 patent could not properly be considered to	10:47:56
5		cover polling?	10:48:00
6	MR. ARJOMAND:	Objection to form.	10:48:03
7	THE WITNESS:	I don't think I was offering	10:48:08
8		that opinion here. I think what is stated here is	10:48:10
9		simply a recounting of what is in the document.	10:48:17
10	BY MR. MICALLEF:		10:48:20
11	Q	Okay. So you were not advancing a	10:48:20
12		particular interpretation of any claim language in	10:48:28
13		your statement about the inventor rejecting polling?	10:48:31
14	A	No. In fact, if you'll look on the prior	10:48:36
15		page, you'll see this is in a section called the	10:48:39
16		overview of the '837 patent.	10:48:43
17	Q	Okay. So I take it then that you have not	10:48:46
18		offered an opinion in this proceeding that the	10:48:49
19		claims of the '837 patent should be construed in a	10:48:52
20		manner to exclude polling?	10:48:57
21	A	That's correct.	10:48:58
22	Q	Okay. Would you agree, or is it -- would	10:48:59
23		you agree that the ordinary meaning of the claims of	10:49:06
24		the '837 patent could read on polling?	10:49:12
25	MR. ARJOMAND:	Objection to form.	10:49:16

1 THE WITNESS: I certainly don't feel like I 10:49:21
2 could agree to that here today. I haven't studied 10:49:23
3 that at all. 10:49:26

4 BY MR. MICALLEF: 10:49:27

5 Q Okay. So let me ask it a little different 10:49:27
6 way and maybe we can come to a meeting of the minds. 10:49:31

7 Are you aware of any words in, for example, 10:49:36
8 claim 1 of the '837 patent that would, if given 10:49:38
9 their ordinary meaning to a person of ordinary skill 10:49:42
10 in the art, would exclude polling? 10:49:45

11 A In any of the claims? 10:49:50

12 Q Claim 1, sir. 10:49:57

13 A Oh, sorry. 10:49:58

14 Well, as I said, I haven't been asked to or 10:50:20
15 done any analysis with respect to polling at all. 10:50:23
16 The thing that I would say about briefly looking at 10:50:27
17 claim 1 here today is that I would want to -- I 10:50:34
18 would want to make that analysis and understand 10:50:41
19 whether notification circuit would necessarily 10:50:47
20 exclude polling, but I haven't done the analysis 10:50:58
21 so . . . 10:51:04

22 Q Okay. Can you tell me what you understand 10:51:04
23 polling to be? 10:51:11

24 A My understanding, in general, is that 10:51:13
25 polling is a process via which one device requests 10:51:17

1 information from another or from multiple devices 10:51:27
2 and then expects to hear back an answer from them. 10:51:34

3 Q So in that kind of process, the information 10:51:38
4 or signal, whatever it may be, coming back from the 10:51:43
5 requestee, if I may say that, would be part of the 10:51:50
6 polling? Or actually part of the polling process. 10:51:55
7 Strike that. Let me ask a better question. 10:52:03

8 What I really mean is if you're going to do 10:52:05
9 polling, you're going to get something back from 10:52:08
10 somebody. Is that fair? 10:52:13

11 A Yeah, on first blush thinking of it, that 10:52:16
12 seems to be the normal way. Again, I haven't spent 10:52:19
13 any time on polling at all. 10:52:22

14 Q The point of polling, though, is to receive 10:52:25
15 some information back from whatever it is being 10:52:28
16 polled? 10:52:33

17 A Yes, basically a question asked and a 10:52:33
18 question answered. 10:52:37

19 Q Okay. So back to paragraph 22 of your 10:52:38
20 declaration. In the second sentence you state, "The 10:52:57
21 technique of notifying as described in the '837 10:53:03
22 patent involves sending a signal from the memory 10:53:06
23 system to the host computer which indicates the 10:53:08
24 memory module has completed initialization." 10:53:12

25 Do you see that? 10:53:16

1	A	Yes.	10:53:17
2	Q	So would it be fair to say that's your	10:53:18
3		definition of notifying?	10:53:22
4	A	No, it's not my definition of notifying.	10:53:23
5		It's an exact quote from the patentee.	10:53:27
6	Q	Okay. So you're saying you think this is	10:53:30
7		the definition of the '837 patent of notifying?	10:53:35
8	A	That's not what I said either. I said that	10:53:39
9		it's a direct quote from what the patentee wrote in	10:53:42
10		the '837 about the technique of notifying.	10:53:49
11	Q	Okay. Well, let me just ask you this then:	10:53:52
12		Wouldn't you agree that in the '837 patent polling	10:53:57
13		also involves sending a signal from the memory	10:54:02
14		system to the host computer system which indicates	10:54:06
15		the memory module has completed initialization?	10:54:10
16	A	I would say, in general, that's correct. I	10:54:14
17		mean, as I talked about before a question asked and	10:54:39
18		a question answered involves sending information	10:54:43
19		back to the memory system -- or from the memory	10:54:47
20		system to the host computer. And so if you ignore	10:54:50
21		all other things, that section of description is the	10:54:55
22		same.	10:55:02
23	Q	Okay. Well, then can you explain to me --	10:55:05
24		strike that.	10:55:05
25		Let me put it to you this way: When I read	10:55:17

1 this, I thought you were trying to make a
2 distinction between polling and notifying, but I
3 didn't see it. So I'm just going to ask you what's
4 the distinction between polling and notifying?

5 A Okay. So this was written to give the
6 reader an overview of the '837 patent as shown on
7 page 10, specific item number 2. These are direct
8 quotes from the patent. They are not my
9 interpretation of the patent or my opinion of what
10 the patent does or doesn't say.

11 So with respect to your question about the
12 difference between notifying and polling which is
13 what I believe your question was, the difference is
14 not in the -- whether a piece of information is sent
15 back to the computer system from the memory module
16 or memory subsystem. As you said, those happen in
17 both cases.

18 The difference relates to when those things
19 happen or when that thing happens. And the process
20 for sending a signal back to the computer system in
21 a polling environment is only initiated when the
22 computer itself asks for that information, and
23 notifying does not have that feature.

24 Q Let me jump back to something. You said
25 these are direct quotes from the patent, but are you

10:55:20
10:55:23
10:55:24
10:55:27
10:55:28
10:55:34
10:55:43
10:55:48
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10:55:56
10:55:59
10:56:03
10:56:08
10:56:16
10:56:22
10:56:25
10:56:29
10:56:30
10:56:36
10:56:48
10:56:54
10:57:01
10:57:07
10:57:09
10:57:14

1 sure of that testimony since in paragraph 22 you 10:57:17
2 cite column 3, lines 24 to 52, and I'm pretty sure 10:57:21
3 the preceding sentence -- that that citation is 10:57:28
4 different from the preceding sentence. 10:57:32

5 A I'm sorry. That citation is supposed to be 10:57:34
6 that. Let me check. 10:57:37

7 So I believe you're correct. They're not 10:58:16
8 direct quotes. Instead they are my concise 10:58:31
9 compression of the actual patent cite that's there. 10:58:41

10 Q Okay. In fact, that cite you have on that 10:58:46
11 second sentence at paragraph 22, column 3, lines 24 10:58:50
12 to 52, that actually includes a description of 10:58:54
13 polling as well, doesn't it? 10:58:58

14 A It does. 10:58:59

15 Q Okay. Now, in paragraph 23 on that on that 10:59:00
16 same page 11 you state, "Alternatively, the 10:59:11
17 notifying method," et cetera. What do you mean by 10:59:14
18 "alternatively"? What is this paragraph alternative 10:59:17
19 to? 10:59:21

20 A It's alternative -- sorry. It's probably 10:59:28
21 my bad writing analysis. It's alternatively, 10:59:35
22 meaning alternately to the polling method, the 10:59:41
23 notifying method. I should have written this 10:59:47
24 sentence better. Is an advantageous handshaking 10:59:50
25 method. 10:59:54

1 Q So the paragraph 23 should have said the
2 notifying -- as an alternative to the polling
3 method, the notifying method is, et cetera,
4 et cetera?

5 A Right.

6 Q Would you agree that Mr. Lee, the inventor
7 of the '837 patent, did not invent the notifying
8 method?

9 MR. ARJOMAND: Objection to form.
10 Objection to foundation.

11 THE WITNESS: In general, the notifying
12 method, yes, I would agree. He didn't invent that.

13 BY MR. MICALLEF:

14 Q I also wanted to ask you some questions
15 about your views on the level of ordinary skill in
16 the art. For example, if you could turn to page 14
17 of your declaration, if I understand correctly in
18 paragraph 30, for example, you seem to be
19 disagreeing with Dr. Alpert's use of this word
20 "familiar." I say that because it's emphasized in
21 your report. Is that fair?

22 A Yes.

23 Q Can you tell me what your disagreement is?

24 A My disagreement revolves around the exact
25 definition of what familiar means. Do they actually

1 know about the computer memory systems, or do they 11:01:43
2 understand the actual ways in which they work, or 11:01:50
3 are they familiar because they know that's a 11:01:54
4 computer system? 11:01:57

5 Q So would it be fair to say that what you 11:01:58
6 think is that person of skill would have the more 11:02:06
7 in-depth familiarity that you just referred to 11:02:11
8 rather than the mere facial familiarity? 11:02:14

9 A Well, I wouldn't use the word "familiar" at 11:02:16
10 all. 11:02:22

11 Q Okay. What word would you use? 11:02:22

12 A Well, I think that a person of ordinary 11:02:25
13 skill in the art here is not a person who's just 11:02:34
14 simply familiar in some fashion with either the 11:02:42
15 techniques or computer memory systems. 11:02:47

16 The -- I think the better phrase is 11:02:58
17 knowledgeable about those systems or those things. 11:03:05
18 Familiar to me just leaves the user wondering 11:03:09
19 what -- I mean, not the user, the reader wondering 11:03:16
20 what skill do you actually have when you're reading 11:03:20
21 this patent. Because the degree or the definition 11:03:24
22 of "familiar" it seems to be too loosey-goosey. 11:03:27

23 Q Let's tighten it up a little bit and get 11:03:42
24 some meat on the bones of your opinion here. Let's 11:03:46
25 take an example. So on page 14 about near the end 11:03:50

1 there you quote Dr. Alpert's declaration at 43 where
2 he say quote, "a person" -- he says, "A person of
3 ordinary skill in the art would be, quote, familiar
4 with techniques used for the initialization of
5 computer systems including initialization of memory
6 components, end quote.

11:03:53

11:03:58

11:04:01

11:04:02

11:04:06

11:04:09

7 Do you see that?

11:04:10

8 A Yes.

11:04:11

9 Q So let's use that subject, okay? The
10 techniques used for the initialization of computer
11 systems including initialization of memory
12 components.

11:04:11

11:04:16

11:04:19

11:04:21

13 What kind of knowledge do you think a
14 person of ordinary skill in the art in 2009, 2010
15 would have had about that subject matter?

11:04:22

11:04:26

11:04:31

16 A Well, I think they would have had more
17 knowledge than just the word "familiar" -- or the
18 words "familiar with" imports.

11:04:34

11:04:40

11:04:46

19 Q I've garnered that aspect of your opinion.

11:04:49

20 A Right.

11:04:53

21 Q I was hoping you would give me more.

11:04:53

22 A Well, I mean, in my definition of -- in my
23 definition, which is found in paragraph 27 -- right?
24 -- the person of ordinary skill in the art has at
25 least one year of work experience relating to memory

11:04:56

11:05:05

11:05:12

11:05:15

1 systems, and it's that work experience that tells 11:05:20
2 you what the word "familiar" in the next part of the 11:05:27
3 sentence is to be understood as. 11:05:31

4 If you actually worked in memory systems, 11:05:35
5 for example, you can get a good idea of what they 11:05:40
6 would be familiar with if they had done that. 11:05:43

7 Q So when you use the word "familiar," it's 11:05:46
8 not loosey-goosey? 11:05:50

9 A No, the -- it's not in the way I just 11:05:52
10 explained it. Here in Dr. Alpert's proposed and the 11:05:58
11 petitioner's proposed person of ordinary skill in 11:06:05
12 the art, we see familiar with computer systems and 11:06:11
13 basic CPU, familiar with techniques related to how 11:06:14
14 components access memory. It just seems to me that 11:06:19
15 that's -- it just seems to me that that's not 11:06:40
16 appropriate, especially when you look later on in 11:06:43
17 his description of that, and you see that he's 11:06:47
18 several years of additional experience working with 11:06:52
19 computer memory systems, and yet, they're only 11:06:55
20 familiar with these things here? How does that -- 11:06:59
21 it seems to be a disconnect in addition to being 11:07:02
22 poorly defined, I guess, is the best way I can say 11:07:12
23 it. 11:07:16

24 Q Just so I understand your testimony, when 11:07:16
25 you say a person of ordinary skill would be familiar 11:07:20

1 with the design of memory devices and modules as in 11:07:21
2 paragraph 27, you further explain that by noting 11:07:25
3 that this person would have had one year of work 11:07:29
4 experience relating to memory systems? 11:07:32

5 A Right. 11:07:34

6 Q And that makes it no longer loosey-goosey? 11:07:35

7 A I think it helps define what one would 11:07:38
8 understand would be the level of expertise of that 11:07:43
9 person, yes. 11:07:45

10 Q And when Dr. Alpert says that such a person 11:07:46
11 would be familiar with various specific subject 11:07:49
12 matter or techniques as you quote in paragraph 30 11:07:53
13 and then that such a person would have several years 11:07:58
14 of experience, you say that doesn't make it 11:08:01
15 something better than loosey-goosey? 11:08:05

16 A No, I think it's inconsistent. When I read 11:08:07
17 his description in paragraph 30, I get the sense 11:08:13
18 that this person is just familiar with these things, 11:08:20
19 and then later on I read that, well, they have 11:08:27
20 several years of experience. I would expect them, 11:08:30
21 given that they have several years of experience, to 11:08:32
22 be much more than just familiar with them. 11:08:35

23 Q Okay. So let's see if we can give the 11:08:36
24 board a little bit of help here. Would you agree 11:08:39
25 that a person of ordinary skill in the art in this 11:08:43

1	particular -- related to this particular patent, the	11:08:46
2	'837 patent, would be knowledgeable of memory	11:08:50
3	modules?	11:08:54
4	A Yes.	11:08:54
5	Q Would you agree that such a person would be	11:08:59
6	knowledgeable of how a memory controller reads and	11:09:01
7	writes to memory modules?	11:09:04
8	A Yes.	11:09:07
9	Q Would you agree that such a person would be	11:09:09
10	knowledgeable about initialization sequences used in	11:09:14
11	memory modules?	11:09:21
12	A As it pertains to the operation of a memory	11:09:21
13	module, yes.	11:09:24
14	Q Would you agree that such a person would be	11:09:25
15	knowledgeable about the interactions between a	11:09:31
16	memory controller and a memory module as they	11:09:38
17	pertain to initialization?	11:09:40
18	A Yes, I believe they would.	11:09:43
19	Q Okay. Would you agree that a person of	11:09:44
20	ordinary skill in the art would be knowledgeable	11:09:51
21	about how to signal information back and forth	11:09:52
22	between a memory controller and a memory module?	11:09:58
23	A Signaling, in general, would be known by a	11:10:00
24	person of ordinary skill in the art, yes.	11:10:04
25	Q And would you agree that such a person	11:10:05

1	would know there were various ways to pass	11:10:08
2	information back between a memory controller and a	11:10:11
3	memory module?	11:10:13
4	A Yes.	11:10:14
5	Q Okay. Agree a person of ordinary skill in	11:10:15
6	the art would have been knowledgeable about the	11:10:19
7	notifying method as you have described it?	11:10:21
8	MR. ARJOMAND: Objection to form.	11:10:25
9	THE WITNESS: I think so, yes. And if not	11:10:31
10	knowledgeable beforehand, it's certainly laid out	11:10:37
11	well enough in the patent to understand what	11:10:41
12	notifying means.	11:10:43
13	BY MR. MICALLEF:	11:10:44
14	Q Would you agree that a person of ordinary	11:10:45
15	skill in the art would have been knowledgeable of	11:10:47
16	polling?	11:10:48
17	A With respect to computer systems and memory	11:10:50
18	design, yes. Memory systems, yeah.	11:10:55
19	Q If I used the phrase "open drain	11:10:58
20	signaling," do you have an understanding of what I	11:11:05
21	mean?	11:11:06
22	A I do.	11:11:07
23	Q What do you think it means?	11:11:07
24	A It means the type of circuitry that allows	11:11:08
25	one to create a wired or to send information across	11:11:14

1	a single wire.	11:11:21
2	Q You agree that a person of ordinary skill	11:11:22
3	in the art would have been knowledgeable about open	11:11:24
4	drain signaling?	11:11:27
5	A I do.	11:11:27
6	Q Okay. You agree that a person of ordinary	11:11:28
7	skill in the art would have been knowledgeable about	11:11:38
8	technical standards that were applicable to memory	11:11:40
9	modules?	11:11:45
10	A I'm sure that they would be aware that	11:11:45
11	there are technical standards. Whether they knew	11:11:49
12	them all, for instance, for every type of memory	11:11:53
13	module out there, I don't know about that. But they	11:11:55
14	would certainly be aware that there are technical	11:11:59
15	standards with respect to memory modules and other	11:12:02
16	portions of a computer system.	11:12:05
17	Q Do you think a person of ordinary skill in	11:12:08
18	the art would have been aware of the details of,	11:12:12
19	say, JEDEC DDR standards?	11:12:18
20	A If as I said they worked in the design	11:12:22
21	relating to memory systems and familiar with the	11:12:27
22	design of memory devices and modules, then yes, they	11:12:31
23	would know what the JEDEC standards are.	11:12:35
24	Q Do you agree a person of ordinary skill in	11:12:37
25	the art would have understood that compliance with a	11:12:40

1 standard could be an advantage in the market? 11:12:42

2 MR. ARJOMAND: Objection to form. 11:12:46

3 THE WITNESS: Yes, I think in this field 11:12:50
4 they would have learned that relatively quickly once 11:12:52
5 they were on the job. 11:12:56

6 BY MR. MICALLEF: 11:12:57

7 Q Okay. Let me see here. I would like to 11:12:57
8 ask you some questions about your interpretation of 11:13:09
9 the word "mode." And I believe that section of your 11:13:12
10 report begins on page 17. Could you turn to that. 11:13:17

11 A I have it. 11:13:28

12 Q Now, you use the phrase -- well, let me 11:13:29
13 just ask you -- strike that. 11:13:34

14 Is it your view that the interpretation 11:13:43
15 you're proposing here is just the ordinary meaning 11:13:46
16 of the word "mode" to a person of ordinary skill in 11:13:51
17 the art reading the '837 patent? 11:13:57

18 MR. ARJOMAND: Objection to form. 11:14:02

19 THE WITNESS: No, I don't think it's the 11:14:11
20 necessary -- is necessarily the ordinary meaning. 11:14:12
21 Clearly, that's what Hynix has proposed here, the 11:14:17
22 plain and ordinary meaning. And in the table that's 11:14:22
23 listed in page 17, I haven't listed that as being 11:14:28
24 what I believe to be the correct construction. So 11:14:34
25 no, it's not the normal and ordinary meaning. 11:14:38

1	BY MR. MICALLEF:	11:14:43
2	Q Okay. Can you tell me what is a behavioral	11:14:43
3	state?	11:14:50
4	A It's a state of operation in which the	11:14:53
5	device or subsection of a device that you're talking	11:14:58
6	about is different than a different behavioral	11:15:04
7	state.	11:15:09
8	Q I'm just wondering what you mean by a	11:15:10
9	subsection of a device that you're talking about.	11:15:28
10	A So if I have a block on a chip that I make	11:15:30
11	dual purpose, and I have signals that come in and	11:15:40
12	those signals tell it which purpose, functionality,	11:15:48
13	behavior to be, then that subsection of the chip	11:15:55
14	changes its behavior and, therefore, is in a	11:15:59
15	different mode. And as is consistent with the	11:16:03
16	description here, that section or the whole chip in	11:16:09
17	those cases may be switched into that mode.	11:16:12
18	Q So let me simplify. You gave me a	11:16:17
19	hypothetical. Let me give you a much simpler	11:16:21
20	hypothetical along the lines. Let's just take two	11:16:25
21	RAM cells, just two.	11:16:28
22	A Okay.	11:16:30
23	Q If I'm reading from one and writing to the	11:16:30
24	other, are they in two different behavioral states?	11:16:33
25	A I don't know if I would classify them as in	11:16:49

1	two different behavioral states because the behavior	11:16:59
2	of a RAM cell is -- the behavior of a RAM cell is --	11:17:07
3	I can't see where you would say that the behavior of	11:17:35
4	the cell is, quote/unquote, different in a read	11:17:38
5	versus a write.	11:17:44
6	Q Well, surely the behavior of a cell is	11:17:46
7	different between a read and a write.	11:17:48
8	A Well, it depends upon how well you	11:17:52
9	understand cells, I guess. The behavior of the	11:17:55
10	circuitry around the cell in a read and write is	11:18:09
11	definitely very different, but the cell itself,	11:18:13
12	given your hypothetical -- right? -- is -- I don't	11:18:20
13	see that as being two different behavioral states.	11:18:37
14	It is -- the transistors are connected in a very	11:18:42
15	specific fashion and they -- they operate based on	11:18:54
16	what the external world gives them.	11:19:03
17	Q And so the circuitry -- you mentioned the	11:19:05
18	circuitry around the cell. What circuitry are you	11:19:10
19	referring to?	11:19:14
20	A So, for instance, the sense amplifiers	11:19:15
21	versus the write circuits.	11:19:18
22	Q So if we include those circuits with the	11:19:20
23	cell during a read and a write, there's different	11:19:23
24	behavior?	11:19:27
25	MR. ARJOMAND: Objection to form.	11:19:28

1 THE WITNESS: If you include those circuits 11:19:32
2 along with the cell -- yes, there is different 11:19:34
3 behavior. 11:19:40

4 BY MR. MICALLEF: 11:19:40

5 Q So they would be that collection of 11:19:40
6 transistors, if you will, the first cell in its 11:19:43
7 write circuitry, sense amp circuitry as opposed to 11:19:50
8 the second cell, and its related circuitry, they 11:19:55
9 would be in different behavioral states when one is 11:19:58
10 performing a read and one is performing a write? 11:20:02

11 MR. ARJOMAND: Objection to form. 11:20:06

12 THE WITNESS: I've certainly never thought 11:20:06
13 about it as being in different behavioral states. I 11:20:08
14 think that's something I would have to analyze more 11:20:22
15 to understand whether I really believe they were 11:20:25
16 different -- in different behavioral states, per se. 11:20:28

17 BY MR. MICALLEF: 11:20:34

18 Q Okay. But you would say if those same two 11:20:34
19 cells and their related circuitry were both being 11:20:41
20 written to, they would be in the same behavioral 11:20:46
21 state? 11:20:48

22 A Well, that's -- my point is that I'm not 11:20:49
23 sure it's a state. I would say they have the same 11:20:54
24 behavior, but whether that behavior is a state or 11:20:57
25 not, I don't know whether that -- I would ascribe 11:21:01

1	that term to the hypothetical you've given.	11:21:05
2	Q So can things have different behavior and	11:21:12
3	be in the same state, behavioral state?	11:21:15
4	MR. ARJOMAND: Objection to form.	11:21:19
5	MR. MICALLEF: Strike that. Let me ask a	11:21:23
6	different question.	11:21:24
7	BY MR. MICALLEF:	11:21:24
8	Q Just tell me how I know if two different	11:21:25
9	components have different behavior that they're in	11:21:28
10	different behavioral states.	11:21:31
11	MR. ARJOMAND: Objection to form.	11:21:33
12	THE WITNESS: Well, if we take the	11:21:40
13	hypothetical and move it up the hierarchy, a good	11:21:42
14	example of a chip, for example, that has two	11:21:48
15	behavioral states. So you have a chip, and it's a	11:21:53
16	memory chip, and like all other memory chips, it	11:22:00
17	operates in a standard, normal operational mode.	11:22:05
18	And that's one of the behavioral states. You can	11:22:11
19	apply signals to it, and you see how it behaves, and	11:22:15
20	it has certain functionality there.	11:22:22
21	So it's very common in the memory	11:22:26
22	manufacturing areas to add other modes which they	11:22:29
23	used, for example, to test to do internal, internal	11:22:34
24	to the manufacturer, special testing. And one of	11:22:40
25	the ways that's been used in the past, certainly in	11:22:44

1 the time frame of 2009, to get the part into this 11:22:47
2 unique functional behavioral state is to take one of 11:22:53
3 the input pins voltage levels and raise it up above 11:23:00
4 the power supply level of the part. And the reason 11:23:04
5 that this changes the behavioral state is that 11:23:07
6 there's a what we call an overvoltage detector, and 11:23:10
7 it detects that this pin has been raised up above a 11:23:16
8 certain power supply level, and it effectively 11:23:20
9 repurposes the functionality inside the chip so that 11:23:23
10 the manufacturer can do specialized testing. 11:23:28

11 BY MR. MICALLEF: 11:23:31

12 Q Repurposes the same functionality that's 11:23:37
13 used in a different behavioral state for a new 11:23:40
14 behavioral state? 11:23:42

15 A No, actually you have to build both pieces 11:23:43
16 of functionality in the device, and you switch one 11:23:46
17 off and you switch the other one on. 11:23:50

18 Q So let me ask you this: On page 17 of your 11:23:52
19 declaration in paragraph 36, you say -- you're 11:23:59
20 saying that the initialization mode and the 11:24:06
21 operational mode are separate and distinct modes 11:24:09
22 during which different distinct behavior and 11:24:11
23 operations occur. What's the difference between 11:24:14
24 behavior and operations? 11:24:17

25 A Well, operations, for example, in this 11:24:24

1	particular sentence could define what particular	11:24:27
2	sequence of events happen in what order, for	11:24:36
3	example. Other operations could be operations which	11:24:40
4	include specialized functionality, for example,	11:24:55
5	initialization.	11:25:04
6	Q Let's start with the first one. The	11:25:05
7	operations referred to in that sentence are -- I'm	11:25:08
8	sorry, a particular sequence of operations? Is that	11:25:14
9	what you said?	11:25:17
10	A No, I said they could include a particular	11:25:17
11	sequence of operations.	11:25:20
12	Q Okay. What about that, if anything, would	11:25:22
13	be called behavior?	11:25:23
14	A Well, how the signals get applied to the	11:25:26
15	part is one part of it. How the part understands	11:25:33
16	what those signals tell it to do is another. And	11:25:38
17	then the last part of it, the behavior of what	11:25:41
18	signals the part decides in this particular mode	11:25:45
19	it's going to send out on its output pins.	11:25:49
20	Q I didn't understand the last part. You	11:26:02
21	said, "And then the last part of it, the behavior of	11:26:05
22	what signals the part decides in this particular	11:26:09
23	mode it's going to send out on its output pins."	11:26:12
24	A Yes.	11:26:18
25	Q The behavior of signals are you referring	11:26:19

1	to?	11:26:20
2	A The behavior of picking which signal would	11:26:21
3	be sent off the chip or off the module.	11:26:27
4	Q So how the signals get applied to the part,	11:26:34
5	how the part understands what those signals tell it	11:26:37
6	to do, and the behavior of the part, I guess, after	11:26:41
7	it gets the signals?	11:26:46
8	A Yes.	11:26:47
9	Q This is all part of a particular --	11:26:47
10	defining the behavioral state?	11:26:50
11	A Yes.	11:26:52
12	Q Okay. So in the context of the '837	11:26:53
13	patent -- well, strike that. Let me ask you a	11:27:06
14	different question.	11:27:08
15	I don't see anything in the proposed	11:27:16
16	interpretation here on page 17 of your declaration	11:27:19
17	about power levels. Would you agree that that	11:27:23
18	interpretation -- first of all, you agree it doesn't	11:27:30
19	say anything about power levels?	11:27:31
20	A I agree with that, yes.	11:27:32
21	Q Would you agree that behavioral state is	11:27:35
22	not necessarily defined by power levels?	11:27:43
23	MR. ARJOMAND: Objection to form.	11:27:47
24	THE WITNESS: Sitting here today having	11:27:51
25	done no analysis, I would say generally yes. And if	11:27:53

1	I can help clear up the issue a little bit, I only	11:27:56
2	gave a hypothetical example where a power -- a power	11:28:00
3	or a voltage level on a pin would change the mode	11:28:08
4	that a chip operates in in support of this	11:28:17
5	definition the "may be switched to" part. So that	11:28:24
6	was my only.	11:28:36
7	BY MR. MICALLEF:	11:28:37
8	Q You would agree that the '837 patent	11:28:37
9	doesn't say anything about power levels?	11:28:39
10	MR. ARJOMAND: Objection to form.	11:28:42
11	THE WITNESS: It does not say anything	11:28:42
12	about power levels, but it does talk about going	11:28:43
13	into and out of different modes somehow.	11:28:46
14	BY MR. MICALLEF:	11:28:49
15	Q Right. But that description of going in	11:28:49
16	and out of modes is never tied to any particular	11:28:51
17	power level or transition between power levels; is	11:28:55
18	that right?	11:28:58
19	MR. ARJOMAND: Objection to form.	11:28:58
20	THE WITNESS: That's correct. I only gave	11:28:59
21	it as an example.	11:29:01
22	BY MR. MICALLEF:	11:29:02
23	Q Whether this interpretation on page 17 of	11:29:03
24	mode is correct or not, can we agree that the proper	11:29:05
25	interpretation really shouldn't turn on power	11:29:10

1	levels?	11:29:13
2	MR. ARJOMAND: Objection to form.	11:29:13
3	THE WITNESS: Yeah, I think that would be	11:29:15
4	an accurate assessment.	11:29:17
5	BY MR. MICALLEF:	11:29:18
6	Q Okay. I want to ask you about another word	11:29:20
7	in this interpretation. The word "system." So	11:29:22
8	that's one of those words that can mean almost	11:29:28
9	anything. So what do you mean by it?	11:29:31
10	A Well, we are looking for broadest	11:29:36
11	reasonable interpretation. We are talking about	11:29:44
12	modes of a thing; right? In reality based on the	11:29:49
13	patent, we're talking about an electrical piece of	11:29:57
14	gear.	11:30:01
15	Generally, in the engineering world	11:30:04
16	independent of whether it's big or small, it's	11:30:08
17	generally called "system." You know, we talk here	11:30:10
18	and you see in the patents and in the prior art, the	11:30:13
19	patent and the prior art, memory subsystem, and you	11:30:16
20	haven't seem -- you have not seemed to have a	11:30:24
21	problem with that word in that it's a subsystem. It	11:30:28
22	is a very -- it is a very broad word, and it helps	11:30:32
23	in this definition because it tells you what the	11:30:39
24	behavioral state is part of.	11:30:48
25	Q So let's go back to my simple hypothetical	11:30:53

1	of two RAM cells, but let's include the associated	11:30:56
2	write circuitry and sense amp circuitry --	11:30:56
3	(Clarification from the reporter.)	11:30:56
4	BY MR. MICALLEF:	11:30:56
5	Q -- let's include the associated write	11:31:12
6	circuitry and sense amp circuitry with each. Let's	11:31:15
7	call that the system.	11:31:19
8	A Yes.	11:31:25
9	Q Now, if I'm writing to just one of those	11:31:26
10	cells, I think you would agree that the behavior of	11:31:28
11	that cell and its associated circuitry is different	11:31:30
12	from the behavior of the other one and its	11:31:32
13	associated circuitry?	11:31:35
14	MR. ARJOMAND: Objection to form.	11:31:36
15	BY MR. MICALLEF:	11:31:37
16	Q Correct?	11:31:37
17	A Yeah, that's correct.	11:31:39
18	Q So would it be fair to say that system is	11:31:42
19	in the -- let's call it the write mode?	11:31:44
20	A Well, given the way you just described it,	11:31:49
21	you've described two systems.	11:31:52
22	Q Well --	11:31:54
23	A Because now you're trying to label one as	11:31:58
24	being in a write mode and the other as being in the	11:32:02
25	read mode. So did you want to make the hypothetical	11:32:04

1	where there are two systems, one has one memory cell	11:32:05
2	and sense amp and write circuit and the other has	11:32:07
3	another memory cell and a sense amp and a write	11:32:12
4	circuit?	11:32:14
5	Q Well, it's kind of -- no, it's kind of what	11:32:14
6	I'm getting at. The system is, it's just line	11:32:16
7	drawing; right? Is the computer over there one	11:32:18
8	system, or is it multiple systems? Would you agree	11:32:21
9	that it would be either way you could say accurately	11:32:24
10	that, say, a modern system is a system just as it	11:32:29
11	includes various systems?	11:32:34
12	MR. ARJOMAND: Objection to form.	11:32:35
13	THE WITNESS: Yes, the term can be used	11:32:40
14	that way.	11:32:42
15	BY MR. MICALLEF:	11:32:42
16	Q And so I'm trying to get -- and the reason	11:32:42
17	I'm spending so much time on it is because you have	11:32:43
18	included it in this proposed interpretation. So I'm	11:32:46
19	trying to get where the contours of it. In my	11:32:49
20	hypothetical, the system is both cells and their	11:32:53
21	associated circuitry.	11:32:55
22	A Okay.	11:32:56
23	Q Now, my question is would you agree it's in	11:32:57
24	the write mode or write behavioral state, if you	11:33:01
25	will?	11:33:05

1	MR. ARJOMAND: Objection to form.	11:33:05
2	THE WITNESS: Well, as I've talked about	11:33:06
3	before, I haven't thought of just a simple two-cell	11:33:07
4	system, if you will, to be able to tell you whether	11:33:14
5	my opinion is that they each have different distinct	11:33:17
6	behavioral states.	11:33:21
7	The one thing that I will say about the	11:33:26
8	construction is if you remove the words "data	11:33:31
9	system" out of this construction, then you have no	11:33:35
10	object for the distinct behavioral state to be acted	11:33:38
11	on or part of or a definition of.	11:33:44
12	BY MR. MICALLEF:	11:33:47
13	Q Fair enough. But do you understand that	11:33:47
14	claim construction -- a claim construction is	11:33:50
15	supposed to capture the objective meaning of a claim	11:33:52
16	term; right?	11:33:55
17	MR. ARJOMAND: Objection.	11:33:56
18	THE WITNESS: I understand that.	11:33:57
19	BY MR. MICALLEF:	11:33:58
20	Q So I should be able to take those words and	11:33:58
21	read that on prior art, for example, and say that's	11:34:00
22	a mode. That thing over there is not a mode.	11:34:04
23	That's a mode. At least under your interpretation;	11:34:09
24	right?	11:34:12
25	A Yes.	11:34:12

1 Q And so you've used the word "system," and
2 so I'm saying I'm taking your interpretation,
3 reading it on my two RAM cells with their associated
4 circuitry as a single system, one of them is being
5 written to, one is not, and I say that is a
6 particular distinct behavioral state, that system of
7 two RAM cells because one of them is being written
8 to and the other is not. Would you agree that I'm
9 right about that?

10 MR. ARJOMAND: Objection to form.

11 THE WITNESS: As I said, I'm just hearing
12 about this hypothetical today, and I haven't had any
13 time to think about whether it is what you
14 described. And so, I mean, I can give other
15 examples that very clearly show that people of
16 ordinary skill in the art understand that this is a
17 good definition for what a mode is.

18 You will find, for example, the word "mode"
19 used in the JEDEC specs, and it's used specifically
20 around write leveling. And the behavior that
21 happens in the part when in a write leveling mode,
22 as it is literally called in the JEDEC spec is very
23 distinct and behaviorally different from when the
24 part is running in its normal standard operation.

25 ///

1 BY MR. MICALLEF:

11:35:40

2 Q Here's my question. If I define a system,
3 does the behavior of everything in the system have
4 to be uniform in order to say it's in a particular
5 behavioral state?

11:35:41

11:35:43

11:35:46

11:36:14

6 A I don't think that's the case given how
7 little time I've had to think about this. The
8 example that I've given with respect to a chip and
9 functionality on a chip and the fact that I've told
10 you that both pieces of functionality that support
11 the two behavioral states must be built into the
12 chip. That dictates that when you're in one mode,
13 circuitry A drives the conditions and the behavior
14 of the chip in that mode. When you're in another
15 mode, different circuitry drives the behavior and
16 the conditions of the chip separately.

11:36:16

11:36:19

11:36:33

11:36:37

11:36:41

11:36:45

11:36:48

11:37:02

11:37:06

11:37:12

11:37:15

17 Q So referring back to that same page, 17 and
18 that paragraph 36, there is a sentence that goes
19 from 17 over to page 18. It starts with a quote.
20 It doesn't end with a quote. There's no end
21 quotation, but that is a quotation from the '837
22 patent; correct?

11:37:20

11:37:48

11:37:52

11:37:59

11:38:01

11:38:06

23 A I believe it is. I'll double-check if you
24 want me to.

11:38:09

11:38:11

25 Yes, it is a quote and it should have

11:38:27

1	quotes before the "id" on page 18.	11:38:30
2	Q Right. So you were citing that	11:38:32
3	statement -- that quote, excuse me, from the patent	11:38:36
4	as an example of this distinct behavior and	11:38:40
5	operations that you say defines different modes;	11:38:42
6	correct?	11:38:45
7	MR. ARJOMAND: Objection to form.	11:38:45
8	THE WITNESS: That's correct.	11:38:50
9	BY MR. MICALLEF:	11:38:50
10	Q And the quoted sentence says that this	11:38:51
11	output 12 may conform to an industry standard or may	11:38:53
12	not conform to an industry standard; correct?	11:38:58
13	A Yes.	11:39:01
14	Q So explain to me why conformance or	11:39:02
15	compliance with an industry standard would indicate	11:39:08
16	different modes.	11:39:14
17	A It indicates different behavior. As I've	11:39:18
18	already talked about before, when you're in one	11:39:30
19	mode, the part operates in a certain fashion, a	11:39:35
20	certain behavior. Part of that behavior, for	11:39:38
21	instance, may be one output listed here is	11:39:42
22	number 12, and that output may have a specification	11:39:48
23	from an industry standard that it operates to in	11:39:53
24	that behavioral mode. In that mode.	11:39:57
25	Q But if the standard requires, for example,	11:40:00

1 writing to a DRAM chip in the standard ordinary way 11:40:03
2 to the memory array and the system can do that when 11:40:10
3 it's not complying with the standard, those aren't 11:40:16
4 different behaviors; right? 11:40:19

5 MR. ARJOMAND: Objection to form. 11:40:20

6 THE WITNESS: Well, that's not what this is 11:40:22
7 talking about. 11:40:23

8 BY MR. MICALLEF: 11:40:24

9 Q I'm trying to get at why you think -- why 11:40:24
10 you think these distinctions between complying or 11:40:27
11 conformance with a standard is associated with 11:40:30
12 modes. 11:40:34

13 A Okay. The way the patentee has described 11:40:35
14 this, he has described two modes: initialization 11:40:43
15 mode and operational mode. And my definition is 11:40:46
16 distinct behavioral state that the system may be 11:40:51
17 switched to. Okay? So if this particular output 11:40:54
18 pin operated in the same fashion during operational 11:41:00
19 mode -- I'm sorry, during initialization mode that 11:41:08
20 it did when it was in operational mode, meaning it 11:41:15
21 conformed to the industry standard in both 11:41:19
22 situations, then it would not be an indicator of 11:41:22
23 whether the part was in two different states, two 11:41:28
24 different modes. But because the functionality of 11:41:31
25 the pin has been redefined and that functionality of 11:41:37

1 that output pin no longer conforms to some industry 11:41:44
2 standard, we know by definition that the part at 11:41:51
3 least in some fashion is in a different mode because 11:41:54
4 its behavior at the output pin has been changed. 11:41:58

5 Q So you would agree it's not really the 11:42:16
6 standard we're talking about. It's the behavior of 11:42:19
7 the pin? 11:42:21

8 A That's correct. This just happens to be an 11:42:21
9 example that the patentee used to show -- I mean, in 11:42:24
10 this section he tells you there are two modes of 11:42:31
11 operation, and then he also goes on to say, you 11:42:34
12 know, one of the -- one of the things that changes 11:42:38
13 in the behavior between the two operations happens 11:42:41
14 to be this particular output pin. And in one mode, 11:42:44
15 that output pin happens to conform to some standard. 11:42:48
16 But in the other mode when the behavior gets 11:42:52
17 changed, it doesn't conform to that standard. It's 11:42:54
18 used for something else. 11:42:57

19 Q Okay. Just let me get my bearings here. 11:42:58
20 I wanted to ask you something about 11:43:52
21 LeClerc, if you could grab that again. 11:43:56

22 A Which -- 11:44:02

23 Q Back to the description of Figure 5, which 11:44:03
24 I guess begins at paragraph 77. 11:44:09

25 A I have it. 11:44:26

1 Q Okay. These, for lack of a better word,
2 subparagraphs or paragraphs 79 through 84, those
3 operations -- well, what is described there is six
4 different operations that initialize registers;
5 correct? Different registers?

6 MR. ARJOMAND: Objection to form.

7 THE WITNESS: Yes.

8 BY MR. MICALLEF:

9 Q In this context, would you agree it's fair
10 to say that a person of ordinary skill in the art
11 would understand the registers referred to here as
12 essentially just storage devices?

13 A Well, in general, a register is a storage
14 device, yes.

15 Q There's no intelligence to them, to the
16 registers that are referred to here in these
17 paragraphs in the sense that a CPU would have
18 intelligence?

19 A Well, I'm not positive I would agree with
20 that. Some intelligence is given to them by how the
21 registers are grouped. So, for example, in 79
22 you're initializing an address register. So not
23 only does the storage element hold data, but because
24 of its nomenclature, we know what data it holds;
25 right?

1	Q	But that register isn't going to process	11:46:01
2		that data that it's holding in any manner?	11:46:04
3	A	Well, it could be part of a circuitry that	11:46:08
4		processes the data.	11:46:15
5	Q	Just the register I'm talking about.	11:46:16
6	A	Just the register process the data. Yeah,	11:46:18
7		if that's the only place you drew the circle is just	11:46:26
8		around the register, then it's just going to hold	11:46:29
9		data, right.	11:46:32
10	Q	And would a conventional implementation of	11:46:32
11		that kind of register be like a series of	11:46:38
12		flip-flops?	11:46:41
13	A	It could be.	11:46:42
14	Q	Okay.	11:46:42
15	A	There are many conventional ways to make	11:46:43
16		registers.	11:46:47
17	Q	Okay. When LeClerg says "initializing the	11:46:47
18		register," would you agree that's referring to	11:46:52
19		writing some data into the register?	11:46:56
20		MR. ARJOMAND: Objection to form.	11:46:58
21		THE WITNESS: Generally, yes.	11:47:01
22		BY MR. MICALLEF:	11:47:02
23	Q	Okay. Would you also agree that what's	11:47:02
24		going -- what's described here in these six	11:47:08
25		paragraphs, 79 through 84, that's not what you would	11:47:11

1	call the sort of normal memory commands that the	11:47:17
2	system would use to read and write to DRAMs. Is	11:47:21
3	that fair?	11:47:27
4	A Well, I certainly don't see that	11:47:27
5	description in LeClerc, and it's certainly possible	11:47:32
6	that it is a normal writing to a location, if you	11:47:42
7	will. I think the one thing that you can say about	11:47:50
8	it is that the location address is an address that	11:47:55
9	would not be found in the main memory of the memory	11:47:59
10	devices.	11:48:02
11	Q Because that address, the main memory	11:48:02
12	addresses, would be addresses that point to the --	11:48:06
13	what we were calling earlier the memory array?	11:48:09
14	A Yeah, the core cells, yes.	11:48:12
15	Q The core cells. And these registers would	11:48:14
16	be separate from that array?	11:48:17
17	A Yes.	11:48:19
18	Q So I'd like to direct your attention to	11:48:37
19	paragraph 46 of your report. Do you have that in	11:48:41
20	front of you?	11:48:55
21	A I do.	11:48:55
22	Q You are discussing Dr. Alpert's analysis	11:48:56
23	here, and you write, "The expression during which	11:49:06
24	merely connotes some time period, but a POSITA would	11:49:12
25	understand that a mode must be more than simply a	11:49:16

1	label for a time period."	11:49:19
2	A I see that.	11:49:24
3	Q So would you agree that Dr. Alpert says	11:49:25
4	more than simply that a mode is simply more than a	11:49:33
5	time period? He identifies -- specifically, he	11:49:37
6	identifies some operations that occur within the	11:49:41
7	mode. Agree?	11:49:45
8	MR. ARJOMAND: Objection to form.	11:49:47
9	THE WITNESS: Well, there are -- there are	11:49:52
10	only two modes defined in LeClerc, first of all.	11:50:10
11	There's the sleep mode and normal. So there are	11:50:15
12	initialization procedures, and there are normal	11:50:26
13	operation procedures effectively.	11:50:31
14	BY MR. MICALLEF:	11:50:36
15	Q I'm asking you about this notion of	11:50:36
16	characterizing a mode as a time period during which	11:50:42
17	certain operations occur.	11:50:45
18	A Okay.	11:50:47
19	Q I'm not talking about LeClerc. I'm talking	11:50:48
20	about the '837 patent. Would you agree that that's	11:50:52
21	a reasonable way to define a mode in this particular	11:50:57
22	field of technology?	11:51:00
23	MR. ARJOMAND: Objection to form.	11:51:01
24	THE WITNESS: So first I'll note that you	11:51:04
25	pointed me to 46, which is in my report talking	11:51:06

1	about what Dr. Alpert said, and 45 talks about, you	11:51:13
2	know, his relation to -- in relation to his	11:51:25
3	application of his constructions to LeClerc.	11:51:27
4	So the --	11:51:30
5	BY MR. MICALLEF:	11:51:47
6	Q Would you like my question read back?	11:51:48
7	A Yeah, probably.	11:51:50
8	MR. MICALLEF: There's two of them. Why	11:51:52
9	don't I do it. Strike that. Why don't I just ask	11:51:53
10	it again.	11:51:56
11	BY MR. MICALLEF:	11:51:57
12	Q I'm asking you about this notion of	11:51:57
13	characterizing a mode at a time period which certain	11:51:59
14	operations occur. Would you agree that that is a	11:52:04
15	reasonable way to define a mode in this particular	11:52:07
16	field of technology?	11:52:10
17	A Well, I don't agree that that's a	11:52:11
18	reasonable way to define it. The -- you can't	11:52:15
19	simply say that because the time -- some timestamp	11:52:25
20	said it's after this time point and before that time	11:52:34
21	that means you're in this mode of operation. So the	11:52:37
22	modes of operation or a mode of operation is	11:52:44
23	actually entered into because of certain signals	11:52:48
24	that are given to the device, whether it's a memory	11:52:55
25	device or a module device, and then the mode is	11:52:59

1 exited by another set of signals telling it what -- 11:53:03
2 you know, how to change its behavior. If you simply 11:53:09
3 say that based on some point in time, you lose the 11:53:13
4 concept of what was it that told the thing to have 11:53:19
5 the behavior you now want it to have in this new 11:53:23
6 mode? It can't be just time, and that's my point 11:53:27
7 here. 11:53:31

8 Q But if you talk about time period during 11:53:32
9 which certain operations occur, it's not just time, 11:53:47
10 is it? It's time and operations; right? 11:53:50

11 MR. ARJOMAND: Objection to form. 11:53:53

12 THE WITNESS: So in that case what 11:53:59
13 difference -- if it's really based on the 11:54:04
14 operations, what difference does it make if time is 11:54:06
15 involved or not? 11:54:09

16 BY MR. MICALLEF: 11:54:12

17 Q Well, why don't you answer my question. If 11:54:13
18 you define it that way as a time period during which 11:54:16
19 certain operations occur, it's not just time. It's 11:54:21
20 time and operations that are the variables; right? 11:54:24

21 A The way that definition is, but my point 11:54:26
22 here in 46 is that a POSITA wouldn't understand that 11:54:29
23 that's what mode means. 11:54:33

24 Q Well, a person of ordinary skill in the art 11:54:34
25 reading the '837 patent would be able to understand 11:54:36

1	that verbal formula what is meant by a time period	11:54:41
2	during which certain operations occur, wouldn't he?	11:54:46
3	MR. ARJOMAND: Objection to form.	11:54:50
4	THE WITNESS: There's no description of	11:54:50
5	time related to mode in the '837 that I saw at all.	11:54:52
6	Now, if you want to say that the time is limited to	11:54:58
7	when you first received some sort of a signal that	11:55:04
8	told you to go into a particular mode and then the	11:55:07
9	time when a second signal was received telling to	11:55:12
10	you leave that mode and you want to relate time	11:55:15
11	somehow that way, then maybe they could understand	11:55:19
12	that. But it's not just -- and in addition to that	11:55:23
13	I don't think it's just the -- sorry, you said time	11:55:31
14	and --	11:55:39
15	BY MR. MICALLEF:	11:55:39
16	Q Operations.	11:55:40
17	A Operations. It's not just the operations.	11:55:40
18	You've left out behavior.	11:55:44
19	Q So if you could open up the -- or get the	11:55:46
20	'837 patent in front of you, I'd like to direct your	11:55:53
21	attention to the abstract.	11:55:57
22	In the second sentence of the abstract says	11:56:04
23	"The memory module can be configured to operate in	11:56:06
24	at least two modes comprising an initialization mode	11:56:10
25	during which the memory module executes at least one	11:56:14

1	initialization sequence in an operational mode."	11:56:18
2	And so this is an example of the '837	11:56:22
3	patent relating mode to time period that you did not	11:56:25
4	see in the patent. Isn't that right, sir?	11:56:28
5	A No, that's not true. I believe you've	11:56:31
6	misread the sentence. What this sentence is talking	11:56:33
7	about is that it comprises two -- it has at least	11:56:38
8	two modes, and one is the initialization mode. And	11:56:42
9	after you've entered that mode -- another way to	11:56:48
10	think of it is after you've entered that mode, then	11:56:58
11	the memory module executes at least one	11:57:01
12	initialization sequence.	11:57:05
13	Q It's the same verbal formula that	11:57:05
14	Dr. Alpert used. It's during which, the time	11:57:09
15	language that you objected to, and operations and	11:57:12
16	initialization sequence that you're not giving any	11:57:16
17	credit to. Isn't that right, sir?	11:57:18
18	MR. ARJOMAND: Objection to form. Lacks	11:57:20
19	foundation.	11:57:21
20	THE WITNESS: That's not correct.	11:57:22
21	BY MR. MICALLEF:	11:57:22
22	Q You can't say that this way of describing	11:57:23
23	an initialization mode in the abstract of the '837	11:57:26
24	patent is an unreasonable description that a person	11:57:29
25	of ordinary skill in the art would not understand.	11:57:33

1	Isn't that right, sir?	11:57:34
2	A No, that's not correct.	11:57:36
3	Q You think a person of skill would not	11:57:37
4	understand this phrase in the abstract. Is that	11:57:39
5	your testimony?	11:57:41
6	A No, my testimony is that a person of	11:57:42
7	ordinary skill in the art reading this would	11:57:47
8	understand that once you entered the initialization	11:57:48
9	mode, once you're inside of that mode, you could	11:57:51
10	perform or the memory module executes at least one	11:57:57
11	initialization sequence.	11:58:03
12	Q So during the time in which you're in that	11:58:03
13	mode, it executes an initialization sequence; right?	11:58:06
14	A You still have to first enter the mode.	11:58:08
15	Q And this is a description of time related	11:58:11
16	to mode in the '837 patent?	11:58:14
17	MR. ARJOMAND: Objection to form.	11:58:16
18	THE WITNESS: I do not believe that. I	11:58:17
19	believe it's a description of functionality based on	11:58:18
20	a set of signals that forces the part to go into a	11:58:23
21	particular mode of operation.	11:58:28
22	BY MR. MICALLEF:	11:58:30
23	Q Well, isn't it true, sir, that the phrase	11:58:31
24	"during which merely connotes some time period"?	11:58:33
25	A No. It can also -- and I think in this	11:58:36

1	case it connotes the actions that occur when you're	11:58:40
2	in the mode that's selected.	11:58:45
3	Q Why, sir, in paragraph 46 of your	11:58:47
4	declaration did you write "The expression during	11:58:49
5	which merely connotes some time period"?	11:58:52
6	A In Dr. Alpert's -- in Dr. Alpert's thing.	11:58:54
7	The way it's written and the way he used various	11:59:00
8	pieces to support what he said.	11:59:03
9	Q So you want the board to believe that when	11:59:04
10	Dr. Alpert was opining on the '837 patent, he used	11:59:06
11	the phrase during which, those two ordinary English	11:59:11
12	words, in a way that was wholly different from the	11:59:15
13	way the '837 patent uses it. Isn't that right?	11:59:19
14	MR. ARJOMAND: Objection to form.	11:59:22
15	THE WITNESS: You cannot derive what	11:59:25
16	"during which" means without reading the rest of the	11:59:28
17	sentence.	11:59:30
18	BY MR. MICALLEF:	11:59:31
19	Q And he didn't either. He said it was the	11:59:31
20	time period during which the initialization	11:59:34
21	operation --	11:59:37
22	A So he's prefaced it --	11:59:37
23	Q Excuse me. Isn't that what he said, sir?	11:59:39
24	A That is what he said.	11:59:42
25	Q Thank you. In fact, the '837 patent uses	11:59:43

1	that same phraseology over and over and over again.	11:59:45
2	Isn't that right?	11:59:49
3	MR. ARJOMAND: Objection to form.	11:59:50
4	THE WITNESS: No, it doesn't.	11:59:51
5	BY MR. MICALLEF:	11:59:52
6	Q You didn't see that in that patent over and	11:59:53
7	over again?	11:59:55
8	A I did not.	11:59:55
9	Q Well, sir, let's go take a little look.	11:59:56
10	I'd like to direct your attention to	11:59:59
11	column 1 in the summary portion of the patent at	12:00:03
12	lines 38 to 39 where I quote "The patent states an	12:00:08
13	initialization mode during which the memory mode	12:00:14
14	executes at least one initialization sequence."	12:00:18
15	There's the patent using that same phraseology	12:00:19
16	again, isn't it?	12:00:23
17	A No, of course, not.	12:00:23
18	Q You're saying that's different -- you want	12:00:24
19	the board to believe that's different than what's in	12:00:26
20	the abstract?	12:00:28
21	A Of course.	12:00:29
22	Q Okay. How about --	12:00:29
23	A You have, sir --	12:00:31
24	Q Excuse me. Excuse me. Let me ask the	12:00:32
25	questions.	12:00:34

1	MR. ARJOMAND: No, he was answering your	12:00:35
2	question, sir.	12:00:37
3	MR. MICALLEF: No, he wasn't.	12:00:38
4	MR. ARJOMAND: Let him finish his answer.	12:00:42
5	MR. MICALLEF: I have his answer. You can	12:00:44
6	ask him on redirect. And I do not appreciate this	12:00:45
7	interruption. This is cross-examination, not a	12:00:49
8	deposition.	12:00:52
9	MR. ARJOMAND: Counsel, you're raising your	12:00:52
10	voice. There's no need for you to raise your voice.	12:00:52
11	You didn't let him finish his answer.	12:00:52
12	MR. MICALLEF: You can ask him what he	12:00:55
13	meant to say on redirect.	12:00:56
14	BY MR. MICALLEF:	12:00:57
15	Q I'd like to direct your attention to	12:00:57
16	column 4 of the '837 patent. Lines 10 to 11 where	12:01:02
17	it again refers to "An initialization mode during	12:01:10
18	which the memory module executes at least one	12:01:12
19	initialization sequence."	12:01:17
20	Do you see that?	12:01:18
21	A I do.	12:01:18
22	Q And that is also a description of time	12:01:18
23	related to mode in the '837 patent?	12:01:21
24	A I do not believe that's the case. I	12:01:24
25	believe that's a description of the mode that the	12:01:26

1	device is in. While in the mode, during that mode,	12:01:31
2	then those operations occur.	12:01:39
3	Q And you did not consider those passages I	12:01:41
4	just pointed to you in developing your proposed	12:01:43
5	interpretation of mode, did you?	12:01:47
6	A I did.	12:01:48
7	Q Oh, you did?	12:01:50
8	A I don't see the occurrence of time in any	12:01:51
9	of the passages that you've pointed me to.	12:01:56
10	Q Well, you were the one who said "during	12:01:58
11	which merely connotes some time period," didn't you?	12:02:01
12	MR. ARJOMAND: Objection to form.	12:02:05
13	THE WITNESS: I said that with respect to	12:02:06
14	what Dr. Alpert has proposed as his construction.	12:02:09
15	BY MR. MICALLEF:	12:02:13
16	Q Let's just be clear so the board	12:02:13
17	understands. Your statement in paragraph 46 of your	12:02:16
18	declaration, "The expression during which merely	12:02:19
19	connotes some time period," in your testimony today	12:02:22
20	is flat out wrong. Is that right?	12:02:25
21	MR. ARJOMAND: Objection --	12:02:29
22	BY MR. MICALLEF:	12:02:29
23	Q Did I get that right?	12:02:29
24	MR. ARJOMAND: Objection to form. Asked	12:02:31
25	and answered.	12:02:32

1	THE WITNESS: My paragraph 46 relates to	12:02:37
2	how Dr. Alpert used "during which" in his	12:02:39
3	construction.	12:02:42
4	BY MR. MICALLEF:	12:02:42
5	Q And up want the board to believe that that	12:02:42
6	was somehow -- that analysis of Dr. Alpert of the	12:02:45
7	'837 patent was somehow a totally different use of	12:02:49
8	the two words "during which" than the '837 patent	12:02:52
9	used. Is that your testimony?	12:02:54
10	MR. ARJOMAND: Objection to form. Asked	12:02:57
11	and answered.	12:02:59
12	THE WITNESS: I believe Dr. Alpert uses the	12:02:59
13	definition of "during which" totally different than	12:03:02
14	what the '837 patent uses "during which."	12:03:05
15	BY MR. MICALLEF:	12:03:10
16	Q Why didn't your paragraph 46 even mention	12:03:10
17	Dr. Alpert?	12:03:14
18	A This whole section is all about Dr. Alpert.	12:03:16
19	If you go 44, 45, 46 doesn't, but 47 does.	12:03:23
20	Q The first sentence of 46 is just about "the	12:03:29
21	expression during which," which you say the	12:03:33
22	expression itself merely connotes some time period.	12:03:36
23	A And the part that you're extracting --	12:03:39
24	Q Is that a yes or no, sir?	12:03:42
25	A You have ignored the fact that it's an	12:03:43

1	analysis of what Dr. Alpert said, and you're trying	12:03:48
2	to turn it into something different.	12:03:51
3	Q I'd like to direct your attention to	12:03:55
4	page 25 of your declaration. In paragraph 48, you	12:04:04
5	say in the middle of the page you say, "There is no	12:04:13
6	difference between the reads and writes used for the	12:04:16
7	initialization procedure and the reads and writes	12:04:20
8	used for regular memory access."	12:04:24
9	Do you see that?	12:04:27
10	A Yes.	12:04:29
11	Q And what do you mean by that?	12:04:30
12	A During the initialization procedure,	12:04:33
13	various -- well, sorry. I have --	12:04:39
14	Q Strike it. Let me ask a different	12:04:44
15	question.	12:04:46
16	The same is true, isn't it, in the '837	12:04:46
17	patent that memory reads and writes that are used	12:04:53
18	for regular memory access are also used during the	12:04:56
19	initialization procedure?	12:05:00
20	MR. ARJOMAND: Objection to form.	12:05:00
21	THE WITNESS: As far as the DRAMs are	12:05:31
22	concerned, yes, they're regular reads and writes.	12:05:33
23	BY MR. MICALLEF:	12:05:35
24	Q So this is not a distinction between the	12:05:35
25	'837 patent and LeClerc like you were suggesting it	12:05:37

1	was. Is that fair?	12:05:42
2	MR. ARJOMAND: Objection to form.	12:05:43
3	THE WITNESS: Well, the -- there is no	12:05:48
4	difference between the reads and the writes in	12:05:56
5	LeClerg used for the initialization procedure and	12:06:03
6	the reads and writes used for regular memory access	12:06:06
7	because in LeClerg, there are only two modes:	12:06:09
8	There's a sleep mode, and there's normal mode.	12:06:12
9	However, the regular reads and writes that occur in	12:06:16
10	the '837 can occur in both the initialization mode	12:06:21
11	and in the normal mode.	12:06:25
12	BY MR. MICALLEF:	12:06:27
13	Q That's right. So if you use your regular	12:06:27
14	reads and writes for both initialization and regular	12:06:29
15	memory access, that's not a distinction between '837	12:06:32
16	and the prior art because the '837 says you can do	12:06:36
17	that; right?	12:06:40
18	MR. ARJOMAND: Objection to form.	12:06:43
19	THE WITNESS: The difference is that the	12:06:43
20	'837 does that in two different modes and	12:06:45
21	specifically states it that way.	12:06:49
22	BY MR. MICALLEF:	12:06:50
23	Q But you were using this sentence in	12:06:50
24	paragraph 48 as evidence of the difference in modes,	12:06:52
25	weren't you?	12:06:56

1	MR. ARJOMAND: Objection to form. Asked	12:06:57
2	and answered.	12:06:58
3	THE WITNESS: No, I was using this	12:06:58
4	statement as that in LeClerc in the one mode that	12:07:00
5	LeClerc has that has reads and writes in it, the	12:07:07
6	reads and writes used in what he calls the	12:07:11
7	initialization procedure are the same kinds of reads	12:07:14
8	and writes that are used in regular memory access.	12:07:20
9	BY MR. MICALLEF:	12:07:24
10	Q And you're saying that because you're	12:07:25
11	trying to argue that because of that, the same reads	12:07:25
12	and writes used in initialization procedure and	12:07:27
13	regular memory access, there's only one mode; right?	12:07:30
14	That was your point.	12:07:33
15	MR. ARJOMAND: Objection to form. Asked	12:07:35
16	and answered.	12:07:36
17	THE WITNESS: It was my point, and that's	12:07:37
18	exactly what LeClerc teaches.	12:07:39
19	BY MR. MICALLEF:	12:07:41
20	Q But it's not what the '837 patent teaches,	12:07:41
21	is it? The '837 patent says you can use the same	12:07:45
22	memory read and writes in both modes; right?	12:07:49
23	MR. ARJOMAND: Objection to form.	12:07:52
24	THE WITNESS: Yes. Why do you see that	12:08:01
25	that's a problem? I don't understand the -- the	12:08:04

1	mode issue here is that the part's behavior is	12:08:13
2	different when it's in a different mode.	12:08:18
3	BY MR. MICALLEF:	12:08:19
4	Q Let's just agree. You can use the exact	12:08:19
5	same memory reads and write commands in operational	12:08:22
6	mode as you do in an initialization mode in the	12:08:25
7	context of the '837 patent; right?	12:08:28
8	MR. ARJOMAND: Objection to form.	12:08:30
9	THE WITNESS: Only insofar as what signals	12:08:32
10	the memory devices see.	12:08:35
11	BY MR. MICALLEF:	12:08:38
12	Q The '837 patent never puts that caveat on	12:08:40
13	it, does it?	12:08:43
14	A The '837 tells us specifically that the two	12:08:44
15	modes are different.	12:08:52
16	Q You didn't say in your paragraph 48 only	12:08:53
17	insofar as what signals the memory devices see, did	12:08:56
18	you?	12:09:02
19	A Well, I was talking about LeClerc, and	12:09:02
20	LeClerc only has one operational mode, and inside of	12:09:04
21	that there are initialization procedures, and there	12:09:08
22	are normal operation procedures.	12:09:10
23	Q So now you want the board to read that into	12:09:11
24	your direct testimony only insofar as what signals	12:09:14
25	the memory devices see; isn't that right?	12:09:17

1	A	Well, you asked me whether or not -- you	12:09:20
2		asked me whether or not reads and writes are doable	12:09:26
3		in both modes in the '837. And so it's not	12:09:37
4		inconceivable in two different modes that some	12:09:45
5		portions of those two modes actually have things	12:09:49
6		that do the same thing. But it's still possible	12:09:51
7		that those two modes have completely different	12:09:55
8		behavior when viewed as a whole.	12:09:58
9	Q	So the fact that there's no difference	12:10:00
10		between reads and writes used for initialization and	12:10:04
11		reads and writes used for regular memory access is	12:10:07
12		not evidence of the same mode being used? It could	12:10:10
13		be two wholly different modes?	12:10:17
14	MR. ARJOMAND:	Objection to form.	12:10:21
15	THE WITNESS:	In the '837 that's true, but	12:10:22
16		it's not true in LeClerc. There's only one	12:10:24
17		operational mode in LeClerc.	12:10:27
18	BY MR. MICALLEF:		12:10:29
19	Q	It's ten after noon. Why don't we take a	12:10:36
20		break and get some lunch.	12:10:46
21	MR. SUH:	We have lunch here.	12:10:48
22	THE VIDEOGRAPHER:	We are now going off the	12:10:49
23		record, and the time is 12:11 p.m.	12:10:51
24		(Lunch recess taken from 12:11 p.m. to	12:11:04
25		12:53 p.m.)	12:53:11

1	THE VIDEOGRAPHER: We are now going back on	12:53:13
2	the record, and the time is 12:53 p.m.	12:53:15
3	BY MR. MICALLEF:	12:53:18
4	Q Mr. Murphy, I'd like to direct your	12:53:19
5	attention to paragraph 52 of your report -- of your	12:53:22
6	declaration, excuse me. Just let me know when	12:53:26
7	you've had a chance to read that.	12:53:47
8	A I've read it.	12:53:52
9	Q So in this paragraph you are saying that	12:53:57
10	because you believe Dr. Alpert had some	12:54:01
11	unfamiliarity with basic aspects of low power mode,	12:54:05
12	that the board should find him to be lacking in	12:54:12
13	credibility when it comes to opinions on other	12:54:18
14	aspects of a memory module. Is that a fair	12:54:22
15	characterization?	12:54:25
16	A I would say so, yes.	12:54:25
17	Q Just so we're all clear, you would agree	12:54:27
18	that you should also be held to the same standard?	12:54:30
19	MR. ARJOMAND: Objection to form.	12:54:36
20	THE WITNESS: Because I don't have a basic	12:54:37
21	aspect of a low power mode?	12:54:40
22	BY MR. MICALLEF:	12:54:42
23	Q No, you would agree, wouldn't you, that if	12:54:42
24	the board were to find that your familiarity with	12:54:45
25	some aspect of memory modules is shown to be	12:54:47

1	wanting, that they should consider you to be lacking	12:54:50
2	in credibility as to the functionality of other	12:54:56
3	aspects of the memory module. Isn't that fair?	12:54:59
4	A It might depend upon what aspect of memory	12:55:03
5	modules, but, in general, I would say that's	12:55:07
6	probably fair.	12:55:09
7	Q Okay. I'd like to direct your attention to	12:55:10
8	paragraph 61 of your declaration.	12:55:26
9	A I see that.	12:55:40
10	Q Now, in this paragraph, you note that	12:55:41
11	Dr. Alpert has identified a plurality of controller	12:55:45
12	circuits, and you say that he appears to contend	12:55:49
13	that they are all part of his analysis but that the	12:55:51
14	claim element requires a single controller circuit.	12:55:55
15	Do you see that? Well, did I characterize it	12:55:58
16	correctly?	12:56:01
17	A Yes, I think so.	12:56:02
18	Q And so is it your opinion that the claim is	12:56:05
19	not satisfied by a module that includes more than	12:56:10
20	one controller circuit?	12:56:13
21	A It's my opinion that the claim requires	12:56:16
22	just a single circuit based on the language that's	12:56:20
23	in the claim.	12:56:23
24	Q A single circuit and no more. That's your	12:56:23
25	opinion?	12:56:26

1	A	Yes.	12:56:27
2	Q	Why?	12:56:28
3	A	Because of exactly how the claim's language	12:56:28
4		reads.	12:56:33
5	Q	What language are you referring to?	12:56:34
6	A	So in the '837 which is Exhibit 1001,	12:56:39
7		column 14, we see the language that says down around	12:56:48
8		line 14 in column 14, "To drive the at least one	12:57:03
9		output while the memory module is in the	12:57:10
10		initialization mode."	12:57:12
11		So based on that and also in line 17 where	12:57:15
12		it says "memory controller indicating at least one	12:57:25
13		status of the at least one initialization sequence	12:57:29
14		and wherein the at least one notification signal,"	12:57:35
15		it's my opinion that those types of languages	12:57:43
16		describe very succinctly when the patentee intended	12:57:49
17		to identify one or more that the patentee used the	12:57:52
18		language "at least one."	12:57:58
19		In the other one we're looking at here in	12:57:59
20		paragraph 61, a controller circuit which is line 12	12:58:02
21		in column 14 in claim 1, "a controller circuit	12:58:11
22		configured to cause the memory module to enter the	12:58:16
23		initialization mode," the "at least one" language	12:58:18
24		doesn't appear.	12:58:22
25	Q	I see. So you're saying because it	12:58:23

1	sometimes uses "at least one" where it doesn't use	12:58:31
2	"at least one," it means one and one only?	12:58:33
3	A Yes.	12:58:36
4	MR. ARJOMAND: Objection to form.	12:58:37
5	BY MR. MICALLEF:	12:58:37
6	Q I note you did not propose that as an	12:58:37
7	interpretation, did you?	12:58:39
8	A As an interpretation where?	12:58:45
9	Q As an interpretation to the claim language,	12:58:47
10	in your claim construction section. Isn't that	12:58:52
11	right?	12:58:56
12	A It's not in claims construction, but my	12:58:58
13	understanding is that the phrase "a" followed by a	12:59:05
14	particular element in the claim can be viewed as one	12:59:10
15	or more based on the reading inside the claim and	12:59:13
16	inside the knowledge that's in the four corners of	12:59:17
17	the document.	12:59:21
18	Q So let me ask you this: The last phrase in	12:59:21
19	this claim 1 of the '837 patent is wherein the "at	12:59:31
20	least one notification signal triggers the memory	12:59:39
21	controller to execute an interrupt routine."	12:59:42
22	Do you see that?	12:59:45
23	A I do.	12:59:46
24	Q So under your theory, a system that had a	12:59:46
25	notification signal trigger the memory controller to	12:59:50

1	execute two interrupt routines would not satisfy	12:59:53
2	this claim. Is that fair?	12:59:59
3	MR. ARJOMAND: Objection. Outside the	13:00:02
4	scope of his direct testimony.	13:00:04
5	THE WITNESS: Well, first of all, you used	13:00:08
6	the word "system," and I see the claim is drawn to a	13:00:09
7	memory module. And I think it's pretty well	13:00:14
8	understood that an interrupt routine, because it is	13:00:24
9	a routine, could have many pieces to it. But as a	13:00:33
10	global thing it would just be called a single	13:00:43
11	interrupt routine. But I think given the same	13:00:46
12	identification that I've pointed to, that that --	13:00:52
13	that the "at least one notification" signal triggers	13:01:02
14	the memory controller to execute an interrupt	13:01:15
15	routine would be understood to be a single routine	13:01:19
16	insofar as it's dealing with just one of the "at	13:01:28
17	least one notification."	13:01:34
18	So, for instance, if there was two	13:01:35
19	notification signals, because it's at least one,	13:01:38
20	then I could easily see that one executes one	13:01:43
21	routine and another one executes a different	13:01:47
22	routine.	13:01:49
23	BY MR. MICALLEF:	13:01:49
24	Q I see.	13:01:49
25	A But I think that is how I would	13:01:50

1	characterize it sitting here today.	13:01:52
2	Q Okay. And so similarly claim 5 of the '837	13:01:53
3	patent which requires an error-out pin under your	13:02:03
4	interpretation would not be satisfied by a memory	13:02:09
5	module that had two error-out pins; correct?	13:02:11
6	MR. ARJOMAND: Objection. Outside the	13:02:17
7	scope of his direct testimony.	13:02:19
8	THE WITNESS: Well, I think this one is	13:02:24
9	slightly different because of how the language is	13:02:29
10	applied here. So right before the "error-out pin"	13:02:32
11	wording, we see wherein the at least one output	13:02:40
12	comprises an error-out pin.	13:02:43
13	So based on the at least one output, there	13:03:01
14	could be more than one output; right? Each of them	13:03:03
15	could comprise an error-out pin. There could be	13:03:07
16	more than one error-out pin effectively because the	13:03:11
17	way the language is written.	13:03:14
18	BY MR. MICALLEF:	13:03:16
19	Q But only one error-out pin per output.	13:03:16
20	A Correct.	13:03:22
21	Q And you have not offered a construction of	13:03:23
22	the word "output"?	13:03:26
23	A I have not.	13:03:26
24	Q So that term should be given under the law	13:03:27
25	its broadest reasonable interpretation consistent	13:03:30

1	with the patent specification?	13:03:33
2	MR. ARJOMAND: Objection. Outside of his	13:03:35
3	direct testimony.	13:03:36
4	THE WITNESS: Yes.	13:03:38
5	BY MR. MICALLEF:	13:03:46
6	Q So I'd like to direct your attention to	13:03:47
7	paragraph 63 of your report which, I believe, goes	13:03:50
8	from page 31 over to page 32, and in particular, the	13:03:53
9	first full sentence on page 32.	13:04:01
10	A I see that sentence.	13:04:11
11	Q By the way, Mr. Murphy, I forgot to ask you	13:04:12
12	did you have any conversations with your counsel at	13:04:15
13	lunch or during any of the breaks about the subject	13:04:17
14	matter of your testimony today?	13:04:20
15	A No.	13:04:21
16	Q Thank you.	13:04:22
17	Okay. So you see that sentence in	13:04:23
18	paragraph 63. So are you suggesting in that	13:04:25
19	sentence that you think that Dr. Alpert testified	13:04:30
20	that the upstream channel is a signal?	13:04:36
21	A Well, under my -- in my understanding,	13:05:16
22	Dr. Alpert is required to show how LeClerc teaches a	13:05:20
23	notification signal, and from what I read in his	13:05:26
24	report, he only talked about the channel which is a	13:05:32
25	plurality of wires running together. And he didn't	13:05:39

1	point to a specific signal on the channel.	13:05:42
2	Q You would agree that the upstream channel	13:05:45
3	210 is a plurality of wires that carries signals.	13:05:50
4	Is that fair?	13:05:55
5	A I think that's fair.	13:05:55
6	Q Okay. But your reading of Dr. Alpert was	13:05:56
7	that he was not of that understanding?	13:05:59
8	A No, my reading of Dr. Alpert's was I	13:06:02
9	expected him to point out the signal which is the	13:06:07
10	notification signal that is on the upstream channel,	13:06:12
11	and he didn't do that.	13:06:18
12	Q Did you understand Dr. Alpert to be opining	13:06:20
13	that the initialization status messages that were	13:06:31
14	sent from the module to the memory controller were	13:06:42
15	signals that were carried on that upstream channel?	13:06:46
16	A I don't recall that right away. Do you	13:06:50
17	have a copy of his declaration, and can you point me	13:06:54
18	to where you're talking about?	13:06:58
19	Q We do have a copy of that. I'm not sure I	13:07:00
20	can point you quickly.	13:07:13
21	Before you look, I want to make sure -- I'm	13:07:15
22	asking about what you understood before you open	13:07:18
23	that document right now.	13:07:21
24	A Sure.	13:07:22
25	Q Yeah, so did you understand Dr. Alpert to	13:07:22

1	be pointing to the initialization status messages as	13:07:27
2	the notification signal?	13:07:33
3	A I would say at this point my best	13:07:36
4	recollection is no, but I'd rather review what he	13:07:44
5	said, and then answer more accurately. That's why I	13:07:47
6	asked for the document.	13:07:53
7	Q Yeah, so before you look at the document --	13:07:54
8	A Sure.	13:07:57
9	Q -- your recollection is you did not have	13:08:01
10	that understanding before you came in here today as	13:08:03
11	far as you know?	13:08:07
12	MR. ARJOMAND: Objection to form. Asked	13:08:08
13	and answered.	13:08:09
14	THE WITNESS: Well, my understanding is	13:08:27
15	that he has to identify a notification signal, and a	13:08:31
16	parallel group of things isn't a notification	13:08:39
17	signal. It's a group of signals.	13:08:42
18	BY MR. MICALLEF:	13:08:44
19	Q I see. And so does that mean before you	13:08:44
20	came here --	13:08:54
21	A I just can't remember exactly what he said.	13:08:55
22	That's all.	13:08:58
23	Q So as you sit here today, you can't	13:08:58
24	remember one way or the other whether you thought	13:09:00
25	Dr. Alpert identified the initialization status	13:09:03

1	message as a notification signal?	13:09:05
2	MR. ARJOMAND: Objection. Asked and	13:09:09
3	answered.	13:09:10
4	THE WITNESS: Yeah, I just can't remember	13:09:16
5	the details right this second. That's why I have to	13:09:18
6	look at the document.	13:09:20
7	BY MR. MICALLEF:	13:09:21
8	Q Did you read the petition?	13:09:22
9	A Yes.	13:09:23
10	Q Let me ask you a different question then.	13:09:24
11	In fact, let me ask you a question about your	13:09:37
12	opinions on page 44 of your declaration. So there's	13:09:48
13	a sentence -- just to point you specifically, there	13:09:58
14	is a sentence at the very top of page 44 that I'd	13:10:01
15	like to direct your attention to.	13:10:04
16	A I'm on 44.	13:10:12
17	Q And I notice that sentence refers to an	13:10:14
18	"initialization complete" message that identified	13:10:22
19	the module or memory device that has completed	13:10:26
20	initialization.	13:10:29
21	Do you see that?	13:10:30
22	A I do.	13:10:30
23	Q Just give me one second, please.	13:10:31
24	And the initialization complete message	13:10:57
25	that you're referring to here, that is the	13:11:02

1 initialization or one version of the initialization 13:11:05
2 status message of LeClerg. Is that fair? 13:11:07
3 A I thought LeClerg separated them out into 13:11:15
4 statuses being not complete and -- well, or complete 13:11:21
5 as being a subset of status maybe. There's not 13:11:26
6 complete and complete. 13:11:29
7 Q That's why I said one version. 13:11:31
8 A One version. Yes, I think that's correct. 13:11:34
9 Q Okay. Right. And the status of this one 13:11:36
10 would be complete? 13:11:38
11 A Yes. 13:11:39
12 Q Okay. And the status that we're talking 13:11:40
13 about is called out in the claim; correct? 13:11:43
14 MR. ARJOMAND: Objection to form. 13:11:47
15 THE WITNESS: In which claim? 13:11:47
16 BY MR. MICALLEF: 13:11:49
17 Q Claim 1. 13:11:49
18 A Of '837? 13:11:50
19 Q Yes. Let me strike that. I'll ask it a 13:11:54
20 different way. 13:11:58
21 Claim 1 requires that the notification 13:11:59
22 signal indicates at least one status; correct? 13:12:05
23 A Yes. That's what the claim requires. 13:12:10
24 Q Okay. And this analysis on page 44 relates 13:12:13
25 to claim 3 which is a dependent claim that just says 13:12:17

1	the status comprises execution of the at least one	13:12:21
2	initialization sequence; correct?	13:12:25
3	A Well, that's what claim 3 says, yes.	13:12:33
4	Q Right. So claim 3 is sort of directed to a	13:12:37
5	version or a flavor of the notification signal. Is	13:12:42
6	that fair?	13:12:47
7	MR. ARJOMAND: Objection to form.	13:12:47
8	THE WITNESS: I don't see how you get	13:13:15
9	execution out of one notification signal.	13:13:17
10	BY MR. MICALLEF:	13:13:26
11	Q My question was just claim 3 is directed to	13:13:26
12	a particular type of notification signal, one that	13:13:31
13	comprises -- where the status that gets indicated	13:13:34
14	comprises execution of the at least one	13:13:38
15	initialization sequence. That's what claim 3 is	13:13:40
16	about; correct?	13:13:43
17	MR. ARJOMAND: Objection to form.	13:13:45
18	THE WITNESS: Yes, that is what claim 3 is	13:13:48
19	about.	13:13:50
20	BY MR. MICALLEF:	13:13:50
21	Q Okay. So when you draft -- put together	13:13:50
22	your analysis of claim 3, for example, here on	13:13:53
23	page 44, you were discussing Dr. Alpert's treatment	13:13:56
24	of the initialization status message of LeClerc.	13:14:02
25	Isn't that fair?	13:14:08

1	A	Yes.	13:14:15
2	Q	So you must have understood that he was	13:14:15
3		identifying that initialization status message of	13:14:18
4		LeClerg as the notification signal; correct?	13:14:21
5	MR. ARJOMAND:	Objection. Form.	13:14:26
6	THE WITNESS:	Well, with respect to his	13:14:47
7		reading of LeClerg in view of Kim?	13:14:49
8	BY MR. MICALLEF:		13:14:56
9	Q	The analysis with respect to claim 3 that	13:14:56
10		you've included in pages 43 through 45 of your	13:14:59
11		report. That's the analysis I'm talking about.	13:15:03
12	A	Yes, so on page 44, five lines down, it	13:15:05
13		says, "Consequently, LeClerg, through its integrated	13:15:11
14		message passing system, is teaching away from the	13:15:15
15		type of solution proposed by Kim based on dedicated	13:15:20
16		wires from the memory modules to the memory	13:15:21
17		controller. It's also true that Kim proposes a	13:15:23
18		single-wire system which we've talked about as a	13:15:26
19		wired or configuration."	13:15:30
20		And the status information that is talked	13:15:36
21		to about in claim 3 which refers back to claim 1	13:15:50
22		talks to at least one notification signal to the	13:15:56
23		memory controller. But Kim only has a single.	13:16:01
24	Q	So let me --	13:16:10
25	A	So how --	13:16:11

1	Q	Oh, I'm sorry.	13:16:12
2	A	How do you put multiple statuses on a	13:16:13
3		single line?	13:16:16
4	Q	Well, okay. Let me go at this a little	13:16:24
5		different way then. I don't think we're	13:16:27
6		communicating.	13:16:30
7	A	Okay.	13:16:30
8	Q	Back to that first sentence at the top of	13:16:30
9		page 44, it refers to -- you say, "LeClerg discloses	13:16:33
10		the sending of an initialization complete message	13:16:37
11		that identified the module or memory device that has	13:16:40
12		completed the initialization."	13:16:44
13		Do you see that?	13:16:46
14	A	I do.	13:16:47
15	Q	I note you don't have a cite at the end of	13:16:48
16		that sentence. Was there some reason for that?	13:16:50
17	A	No. I just think it was obvious that	13:16:53
18		LeClerg disclosed that.	13:16:57
19	Q	Did you have anywhere in mind where LeClerg	13:16:59
20		disclosed that the "initialization complete" message	13:17:03
21		identified the module or memory device that had	13:17:05
22		completed initialization?	13:17:10
23	A	So specifically in LeClerg, which is	13:17:23
24		Exhibit 1005, at paragraph 33, the last sentence, it	13:18:18
25		says, "In another embodiment each memory module	13:18:26

1	12 -- 112, 114 passes a received command to the	13:18:29
2	downstream direction only if it is not the	13:18:34
3	destination of the command."	13:18:38
4	So that tells one of ordinary skill in the	13:18:40
5	art that the commands that are sent across the	13:18:45
6	downstream channels from the memory controller or	13:18:47
7	the processor have addressing information in them.	13:18:50
8	And then there's the section of the	13:18:56
9	claim -- I'm sorry, section of LeClerc that talks	13:19:05
10	about the use of the information sent across the	13:19:21
11	channel, for instance, to do memory replacement.	13:19:24
12	I'll have to find the paragraph for you. I don't	13:19:29
13	know it off the top of my head.	13:19:32
14	And, therefore, to do memory replacement,	13:19:33
15	you have to know not only which module you're	13:19:36
16	talking about but also potentially which device on	13:19:39
17	the module. So the LeClerc definitely talks about	13:19:42
18	that information being in the system and being used	13:19:47
19	by the system to perform certain functions.	13:19:53
20	Q But would you agree LeClerc does not talk	13:19:55
21	about that information being included in the	13:19:59
22	initialization status message that gets sent from	13:20:01
23	the module back up to the memory controller?	13:20:04
24	MR. ARJOMAND: Objection. Form.	13:20:08
25	THE WITNESS: I don't think I agree with	13:20:26

1	that. I just have to find the support for it.	13:20:27
2	So in paragraph 91, the status message is	13:20:59
3	talked about as having the possibility of including	13:21:30
4	success or failure. It also has the possibility of	13:21:36
5	being a single or group of messages, one or more	13:21:40
6	separate messages in various embodiments --	13:21:44
7	BY MR. MICALLEF:	13:21:48
8	Q I'm sorry. Where are you reading, sir?	13:21:48
9	A I'm sorry. 91. There's no column --	13:21:51
10	there's no line numbers in 91. Roughly 91 in the	13:21:54
11	middle.	13:21:58
12	Q Okay.	13:21:58
13	A "The success or failure indicator and the	13:21:59
14	error information can be sent as part of the	13:22:02
15	completed message or as one or more separate	13:22:04
16	messages in various embodiments."	13:22:09
17	So the completed message is an example of	13:22:13
18	what you talked about is one of the particular	13:22:19
19	status messages; correct?	13:22:22
20	Q I'm sorry?	13:22:24
21	A We've talked about this before.	13:22:25
22	Q So you think this paragraph 91 discloses	13:22:26
23	the identification of the module or memory device	13:22:30
24	that has completed initialization within the	13:22:35
25	initialization status message?	13:22:38

1	A	Yes. The status message -- so the status	13:22:42
2		message here is talked about in paragraph 90.	13:22:46
3	Q	90? I'm sorry. 90?	13:22:51
4	A	90.	13:22:53
5	Q	Now 90. I thought you said 91 earlier.	13:22:54
6	A	The part I was reading originally was 91	13:22:58
7		but 91 is a continuation of what's described in 90.	13:23:04
8		"The process begins in block 602 when buffer module	13:23:05
9		receives an initialization status query. In	13:23:06
10		response to the message, the buffer module	13:23:11
11		determines whether the initialization process is	13:23:14
12		completed."	13:23:15
13	Q	So that would all be on the module;	13:23:17
14		correct?	13:23:20
15	A	That's all on the module, correct.	13:23:20
16	Q	All right.	13:23:23
17	A	And if the initialization process is not	13:23:24
18		completed, then the buffer module returns a not	13:23:29
19		completed message as its status.	13:23:32
20	Q	Okay. And where --	13:23:35
21	A	And then in the next sentence it says:	13:23:37
22		"If the process has completed, the buffer	13:23:41
23		module returns a completed message to the	13:23:43
24		processor as its status. In one embodiment,	13:23:46
25		the buffer module also returns the success or	13:23:50

1 failure indicator and error information. If 13:23:54
2 any is indicated in the error registers, the 13:23:57
3 success or failure indicator and the error 13:24:01
4 information can be sent as part of the 13:24:03
5 completed message, which is the status message, 13:24:06
6 or as one or more separate messages in various 13:24:08
7 embodiments. The error information can include 13:24:11
8 the number of locations for which a failure was 13:24:14
9 detected and/or the error types and/or the 13:24:18
10 actual addresses of the failed locations. That 13:24:20
11 information can be used, for example, to 13:24:24
12 perform online sparing or other error-recovery 13:24:26
13 operations to take place." 13:24:30

14 So to have that information to be 13:24:36
15 functional to the system, it has to know which 13:24:39
16 module it came from and potentially which device it 13:24:41
17 came from. 13:24:44

18 Q Whether or not that's so, sir, I don't see 13:24:44
19 anywhere in all those words that you read that said 13:24:47
20 the identification information must be in the 13:24:50
21 initialization status message as opposed to being 13:24:53
22 obtained by the memory controller in some other 13:24:57
23 manner. Would you agree with that? 13:25:00

24 A No. The language here is very clear. 13:25:05

25 Q Okay. 13:25:07

1	A	It's describing -- it's describing the	13:25:07
2		process being completed and the buffer module	13:25:10
3		returning a completed message.	13:25:13
4	Q	Okay.	13:25:15
5	A	Which is a status message.	13:25:16
6	Q	Would you agree that the claims of the '837	13:25:17
7		patent do not require a notification signal to	13:25:20
8		identify the module or memory device that has	13:25:23
9		completed its initialization?	13:25:29
10	A	As far as my reading of the claims, I do	13:25:32
11		not believe that it requires that. That's correct.	13:25:39
12	Q	Okay. So you also state here that -- or	13:25:40
13		you at least imply that Kim discloses the use of	13:25:49
14		dedicated wires. You agree that Kim never calls any	13:25:53
15		of its connections dedicated wires?	13:26:00
16	MR. ARJOMAND:	Objection. Form.	13:26:04
17	THE WITNESS:	That may be true from a	13:26:09
18		language point of view, but from the pictures in	13:26:11
19		Kim, there is clearly a dedicated wire for the wired	13:26:15
20		or configuration.	13:26:25
21	BY MR. MICALLEF:		13:26:26
22	Q	Doesn't Kim explain in one portion that its	13:26:26
23		open drain output reporting configuration can be	13:26:29
24		used on a pin that's designated by an industry	13:26:32
25		standard for some other purpose?	13:26:36

1 A As far as the pin is concerned, that's
2 true. But there's a dedicated -- from the picture,
3 there's a dedicated wire that creates the open drain
4 configuration. It has to be dedicated to that. It
5 might also have other things that it -- a
6 different -- like a different wire -- different
7 dedicated wire for some other usage that meet at the
8 pin, but at least from the picture of Kim, there is
9 a dedicated wire for the wire or of Kim's example.

13:26:39
13:26:44
13:26:46
13:26:52
13:26:55
13:26:59
13:27:03
13:27:08
13:27:11

10 Q And you think that wire is not also used
11 for the industry standard functionality that Kim
12 refers to?

13:27:18
13:27:21
13:27:25

13 MR. ARJOMAND: Objection. Form.

13:27:27

14 THE WITNESS: Yeah, I think it's not used
15 or at least the section that Kim shows is not used
16 for a wire for the industry standard configuration
17 because -- I don't have Kim in front of me. Sorry.
18 BY MR. MICALLEF:

13:27:39
13:27:41
13:27:44
13:27:50
13:28:00

19 Q I note you also refer to -- in the next
20 sentence in that same paragraph 82 on page 44, you
21 seem to suggest that LeClerg includes unrestricted
22 expandability and flexibility.

13:28:02
13:28:09
13:28:13
13:28:20

23 Do you see that?

13:28:23

24 A Yes.

13:28:23

25 Q Agree that LeClerg never mentions that

13:28:28

1	phrase?	13:28:31
2	A It never mentions that phrase except as	13:28:31
3	shown in the pictures, the architectural	13:28:34
4	configuration that LeClerc discloses is well known	13:28:42
5	to have unrestricted -- basically unrestricted	13:28:44
6	expandability and flexibility.	13:28:45
7	Q Do you think a person of skill in the art	13:28:47
8	would read LeClerc as having unrestricted	13:28:49
9	flexibility as in unlimited flexibility?	13:28:53
10	A Not from the point of view to infinity, but	13:28:56
11	to the point that the expandability and the	13:29:00
12	flexibility can be modified at next to no cost.	13:29:03
13	Q What do you think the intended purpose of	13:29:10
14	LeClerc is?	13:29:12
15	MR. ARJOMAND: Objection. Form.	13:29:15
16	THE WITNESS: Well, the intended purpose of	13:29:18
17	LeClerc is to provide a more flexible -- one of the	13:29:22
18	purposes is given the architecture he displays is to	13:29:28
19	provide a more flexible way to put many modules on a	13:29:34
20	set of wires that go back to the processor. And	13:29:39
21	that's why we see the hierarchical messaging system	13:29:42
22	that's detailed pretty well in LeClerc.	13:29:48
23	BY MR. MICALLEF:	13:29:50
24	Q And your view is that adding the open drain	13:29:50
25	connection of Kim -- let me strike that. Let me ask	13:29:53

1	a different question.	13:29:56
2	Are you under the understanding that in the	13:29:57
3	combination of LeClerc and Kim, something from	13:29:59
4	LeClerc is taken out?	13:30:02
5	A The -- not necessarily from a hardware	13:30:04
6	point of view. What is taken out is a capability	13:30:14
7	point of view. So, for instance, it's well known	13:30:20
8	that open drain wire configurations can only be	13:30:24
9	extended a certain amount of distance or to a	13:30:30
10	certain number of things without getting very slow	13:30:34
11	in response time.	13:30:36
12	Q So let's just -- point of procedure here.	13:30:37
13	You do know we're talking about the combination of	13:30:42
14	LeClerc and Kim that our side put into the petition	13:30:45
15	and supporting documents; right?	13:30:48
16	A I do.	13:30:51
17	Q So that's not any other combination of	13:30:51
18	LeClerc and Kim that you might think makes sense.	13:30:55
19	Agree with that?	13:30:57
20	A Yes. Only yours.	13:30:58
21	Q Okay. So did you see somewhere in the	13:31:00
22	petition where it said something would be taken out	13:31:04
23	of LeClerc?	13:31:06
24	A From your point of view I saw nothing.	13:31:09
25	Q Okay.	13:31:12

1	A	From --	13:31:14
2	Q	Go ahead.	13:31:15
3	A	From what one of ordinary skill in the art	13:31:16
4		would understand when you try to add the features	13:31:19
5		that you found in Kim to LeClerc, they would	13:31:21
6		understand that some of the capability to have	13:31:26
7		expandability and flexibility that's described in	13:31:32
8		LeClerc would disappear based on the implementation	13:31:36
9		as Dr. Alpert talks about of Kim's technique,	13:31:40
10		especially when he talks about Kim's technique over	13:31:47
11		multiple memory modules that Kim never even talks	13:31:50
12		about. Kim talks about the technique used on a	13:31:53
13		single memory module.	13:31:56
14	Q	And so that's the basis of your analysis,	13:31:57
15		this reading of our combination and then concluding	13:32:00
16		that something would necessarily have to be taken	13:32:06
17		out. Is that fair?	13:32:12
18	MR. ARJOMAND:	Objection to form.	13:32:14
19	THE WITNESS:	I think the -- I think, as I	13:32:16
20		said, the capability would be reduced. If you want	13:32:19
21		to call that taken out, then I'll use your words	13:32:26
22		"taken out." But the capability certainly gets	13:32:29
23		reduced.	13:32:32
24		The second thing is that the protocol that	13:32:32
25		LeClerc has built up for his hierarchical-based	13:32:36

1 message processing arrangement that connects all 13:32:40
2 these things, all the signals would follow a 13:32:42
3 standard protocol and format, that's all known -- 13:32:47
4 well-known technology. 13:32:52

5 Now you're adding, based on Kim, a signal 13:32:54
6 that's handled completely differently than what's in 13:32:58
7 existence for LeClerg. And I don't see, especially 13:33:01
8 because -- and I've said this in the report -- 13:33:05
9 especially because LeClerg already has an 13:33:08
10 error-handling system. I don't see any reason why a 13:33:11
11 POSITA would be drawn to combine the two to add this 13:33:15
12 open drain configuration you happen to see on Kim. 13:33:19

13 BY MR. MICALLEF: 13:33:23

14 Q So would you agree that this identification 13:33:23
15 of memory modules or memory devices that had 13:33:25
16 completed initialization would be information that 13:33:31
17 is reflected in the registers of LeClerg at least at 13:33:34
18 some point? 13:33:40

19 A Well, the -- yeah, the registers are put 13:33:40
20 there to, as we've read today, identify the starting 13:33:54
21 address, the ending address, the value to be 13:33:58
22 written, and then completed or not completed. And 13:34:02
23 maybe I don't have the whole set, but that's a bunch 13:34:05
24 of them. All that information is stored in the 13:34:08
25 registers. 13:34:11

1 LeClerc very clearly defines that it can be
2 a partial or complete initialization; right? So the
3 registers have that data, and when the -- and
4 LeClerc definitely talks about the fact that when
5 the procedure is over, that that information can be
6 shipped back to the memory device to enable it to
7 have certain -- I'm sorry, to the memory controller
8 so that the memory controller can have information
9 to do its work and decide if it needs to do other
10 things to the module itself.

11 Q And you're of the opinion that that
12 information would include an identification of the
13 memory module or memory device that has completed
14 initialization. Is that fair?

15 A Well, I don't think it's just my opinion.
16 I think a person of ordinary skill in the art would
17 understand that if you collect all this information
18 about errors, even completion, or things like that,
19 and you don't know which memory module it relates
20 to, you don't have much information, do you?

21 Q So -- but there would be no reason why if
22 you used the open-drain technique, signaling
23 technique of Kim, in the system of LeClerc, why you
24 would have to alter the data that is stored in those
25 registers. Isn't that right?

1	MR. ARJOMAND: Objection. Form.	13:35:43
2	THE WITNESS: Well, I guess the answer to	13:35:45
3	that depends upon what information you're sending	13:35:46
4	across the line that you're using from LeClerc.	13:35:50
5	BY MR. MICALLEF:	13:35:54
6	Q My question was just if you're using Kim's	13:35:54
7	open-drain technique, you can leave the registers	13:35:57
8	and information in them. That gets put in them the	13:36:00
9	same. Isn't that right?	13:36:04
10	MR. ARJOMAND: Objection. Form.	13:36:05
11	THE WITNESS: It is possible to leave them	13:36:11
12	the same. However, if you do that, why are you	13:36:12
13	adding this other line in a completely different	13:36:15
14	format? It goes to the motivation to combine. I	13:36:19
15	have a system that handles this stuff that's	13:36:23
16	described by LeClerc. Why would I add what Kim	13:36:26
17	says? And especially considering the fact that Kim	13:36:30
18	only applies that technique on a single module.	13:36:32
19	Within a single module it applies that technique.	13:36:38
20	It doesn't -- he doesn't say anything about	13:36:40
21	stitching that wire through all the modules; right?	13:36:42
22	And, in fact, when you look at LeClerc, the modules	13:36:46
23	don't get stitched together in any way, shape, or	13:36:50
24	form. The modules get connected to the individual	13:36:54
25	controller on the module, and then those get	13:36:57

1	connected through the upstream and downstream	13:37:01
2	channels.	13:37:04
3	BY MR. MICALLEF:	13:37:05
4	Q Do you understand that you don't need a	13:37:06
5	motivation to combine to find obviousness?	13:37:08
6	A I don't think that's the case. To find	13:37:16
7	obviousness, you have to have some idea as to why	13:37:27
8	you would add part A to part B.	13:37:31
9	Q So your understanding of the law of	13:37:34
10	obviousness is that one must show, without question,	13:37:37
11	must show a motivation to combine?	13:37:43
12	MR. ARJOMAND: Objection.	13:37:45
13	THE WITNESS: At this point today, I can't	13:37:46
14	remember if there is another -- another way to do it	13:37:47
15	other than showing a motivation to combine.	13:37:51
16	BY MR. MICALLEF:	13:37:58
17	Q Just give me one minute.	13:38:05
18	I might be done, but I'd like to take a	13:38:22
19	break and chat with my colleague here; so why don't	13:38:25
20	we take five minutes?	13:38:28
21	MR. ARJOMAND: Okay.	13:38:30
22	THE VIDEOGRAPHER: We are now going off the	13:38:31
23	record, and the time is 1:38 p.m.	13:38:32
24	(Recess taken from 1:38 p.m. to 1:48 p.m.)	13:38:35
25	THE VIDEOGRAPHER: We are now going back on	13:48:02

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Conducted on November 16, 2017

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1	the record, and the time is 1:48 p.m.	13:48:04
2	MR. MICALLEF: I pass the witness.	13:48:07
3	MR. ARJOMAND: Thank you. Can we just take	13:48:09
4	a quick five-minute break?	13:48:11
5	MR. MICALLEF: You can.	13:48:15
6	MR. ARJOMAND: Thank you.	13:48:16
7	THE VIDEOGRAPHER: We are now going off the	13:48:16
8	record, and the time is 1:48 p.m.	13:48:18
9	(Recess taken from 1:48 p.m. to 1:52 p.m.)	13:48:20
10	THE VIDEOGRAPHER: We are now going back on	13:52:41
11	the record, and the time is 1:53 p.m.	13:52:42
12	MR. ARJOMAND: Thank you, Counsel. We have	13:52:45
13	no further questions.	13:52:46
14	MR. MICALLEF: Okay. Then I think the	13:52:48
15	videographer would like to make a modification.	13:52:50
16	THE VIDEOGRAPHER: Yes. On the read-on, I	13:52:53
17	stated that we were here for both 548 and 549, but	13:52:56
18	this deposition was only for 00548.	13:53:02
19	And this concludes the deposition of	13:53:06
20	Robert J. Murphy, consisting of three DVDs. We are	13:53:09
21	now going off the record, and the time is 1:53 p.m.	13:53:14
22	THE REPORTER: Counsel, would you both like	13:53:22
23	to get the rough draft tonight?	13:53:24
24	MR. MICALLEF: Yes, please.	13:53:27
25	MR. ARJOMAND: No, I don't think we need	13:53:28

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it.

(Off the record at 1:53 p.m.)

13:53:30

1 ACKNOWLEDGMENT OF DEPONENT

2
3 I, ROBERT J. MURPHY, do hereby acknowledge
4 that I have read and examined the foregoing testimony,
5 and the same is a true, correct, and complete
6 transcription of the testimony given by me, and any
7 corrections appear on the attached errata sheet signed
8 by me.
9
10

11 _____
12 (DATE)

11 _____
12 (SIGNATURE)

1 CERTIFICATE OF SHORTHAND REPORTER

2
3 I, Lisa Moskowitz, Certified Reporter within
4 and for the State of California, do hereby certify:

5
6 That ROBERT J. MURPHY, the witness whose
7 deposition is hereinbefore set forth, was duly sworn
8 by me before the commencement of such deposition and
9 that such deposition was taken before me and is a true
10 record of the testimony given by such witness.

11 I further certify that the adverse party,
12 Netlist, was represented by counsel at the deposition.

13 I further certify that the deposition of
14 ROBERT J. MURPHY occurred at the offices of Sidley
15 Austin, LLP, 555 West Fifth Street, Suite 4000, Los
16 Angeles, California 90013 on Thursday, November 16,
17 2017, commencing at 9:02 a.m. to 1:53 p.m.

18 I further certify that I am not related to
19 any of the parties to this action by blood or
20 marriage, that I am not employed by or an attorney to
21 any of the parties to this action, and that I am in no
22 way interested, financially or otherwise, in the
23 outcome of this matter.
24
25

1 IN WITNESS WHEREOF, I have hereunto set my
2 hand this 20th day of November, 2017.

3
4
5 
6

7 _____
8 LISA MOSKOWITZ
9 CSR 10816, RPR, CRR, CLR
10 NCRA Realtime Systems Administrator
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Conducted on November 16, 2017

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A			
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