

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

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Case IPR2025-00001

Patent 11,386,024 B2

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**PETITION FOR *INTER PARTES* REVIEW OF  
U.S. PATENT NO. 11,386,024**

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**EXHIBIT LIST**

| <b>Exhibit #</b> | <b>Description</b>                                                                                      |
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| 1001             | U.S. Patent No. 11,386,024                                                                              |
| 1002             | File History of U.S. Patent No. 11,386,024                                                              |
| 1003             | Declaration of Donald Alpert                                                                            |
| 1004             | Curriculum Vitae of Donald Alpert                                                                       |
| 1005             | File History of U.S. Patent Application No. 15/088,115 (i.e., U.S. Patent No. 9,858,218)                |
| 1006             | File History of U.S. Patent Application No. 13/942,721 (i.e., U.S. Patent No. 9,311,116)                |
| 1007             | File History of U.S. Patent Application No. 12/815,339 (i.e., U.S. Patent No. 8,489,837)                |
| 1008             | U.S. Provisional App. No. 61/186,799                                                                    |
| 1009             | U.S. Patent Publication No. 2010/0042778 to Tanguay et al.                                              |
| 1010             | U.S. Patent Publication No. 2003/0115427 to Roohparvar                                                  |
| 1011             | U.S. Patent Publication No. 2010/0202240 to Moshayedi et al.                                            |
| 1012             | U.S. Patent Publication No. 2008/0256281 to Fahr et al.                                                 |
| 1013             | U.S. Patent Publication No. 2010/0142383 to Goishi et al.                                               |
| 1014             | U.S. Patent Publication No. 2008/0098277 to Hazelzet                                                    |
| 1015             | JEDEC COMMITTEE LETTER BALLOT, LRDIMM DDR3 Memory Initialization Chapter Proposal (Dec. 2009) (“JEDEC”) |
| 1016             | U.S. Patent No. 8,139,430 to Buchmann et al.                                                            |
| 1017             | U.S. Patent No. 8,359,521 to Kim et al.                                                                 |
| 1018             | U.S. Patent No. 8,407,441 to Giovannini et al.                                                          |

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| Exhibit # | Description                                                                                                                                             |
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| 1019      | U.S. Patent No. 8,489,837 to Lee                                                                                                                        |
| 1020      | U.S. Patent No. 3,414,781 to Dill                                                                                                                       |
| 1021      | <i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00548, Exhibit 1021, (PTAB December 11, 2017) (Deposition of Robert J. Murphy in 837 Patent IPR) |
| 1022      | U.S. Patent Application Pub. 2008/0147897 to Talbot                                                                                                     |
| 1023      | U.S. Patent Application Pub. 2008/0155378 to Amidi                                                                                                      |
| 1024      | JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000) (“JESD79”)                                                               |
| 1025      | JEDEC Standard, FBDIMM: Architecture and Protocol (January 2007) (“JESD206”)                                                                            |
| 1026      | JEDEC Standard, FBDIMM Advanced Memory Buffer (AMB) (March 2009) (“JESD82-20A”)                                                                         |
| 1027      | U.S. Patent No. 7,411,862 to Hein et al.                                                                                                                |
| 1028      | US Patent App. Publication No. 2006/0277355 by <u>Ellsberry</u> et al.                                                                                  |
| 1029      | JEDEC Standard, Low Power Double Data Rate (LPDDR) SDRAM Specification (August 2007) (“JESD209”)                                                        |
| 1030      | U.S. Patent Pub. No. 2007/0008791 to Butt                                                                                                               |
| 1031      | U.S. Patent No. 9,535,623 (623 Patent)                                                                                                                  |
| 1032      | <i>SK hynix, Inc. et al. v. Netlist, Inc.</i> , IPR2018-00303, Paper No. 1 (PTAB December 14, 2017) (623 Patent IPR Petition)                           |
| 1033      | <i>SK hynix, Inc. et al. v. Netlist, Inc.</i> , IPR2018-00303, Exhibit 1003 (PTAB December 14, 2017) (Alpert Declaration in 623 Patent IPR)             |
| 1034      | <i>SK hynix, Inc. et al. v. Netlist, Inc.</i> , IPR2018-00303, Paper No. 42 (PTAB March 21, 2019) (623 Patent Final Written Decision)                   |

| Exhibit # | Description                                                                                                                                         |
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| 1035      | <i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00548, Paper No. 25 (PTAB May 3, 2018) (837 Patent Final Written Decision)                   |
| 1036      | JEDEC COMMITTEE LETTER BALLOT, DDR3 LRDIMM Design Specification Body (Dec. 2009)                                                                    |
| 1037      | JEDEC, Compilation of Tallies for JC-40 CMOS Digital Logic and point committees (Dec. 4, 2009)                                                      |
| 1038      | File History of U.S. Patent Application No. 15/169,745 (i.e., U.S. Patent No. 9,535,623)                                                            |
| 1039      | Inphi Corporation, “MB Initialization sequence Item 142.35,” June 4, 2009                                                                           |
| 1040      | U.S. Patent No. 8,386,737 to Jeon et al.                                                                                                            |
| 1041      | Petitioner’s Reply, <i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00548, Paper 14 (PTAB December 11, 2017).                                |
| 1042      | “Sequence,” <a href="https://www.lexico.com/en/definition/sequence">https://www.lexico.com/en/definition/sequence</a>                               |
| 1043      | U.S. Patent No. 7,222,213 to James                                                                                                                  |
| 1044      | Texas Instruments, “28-Bit to 56-Bit Registered Buffer with Address Parity Test One Pair to Four Pair Differential Clock PLL Driver” (October 2008) |
| 1045      | Micron, “ <i>High-Speed DRAM Controller Design</i> ” (2008)                                                                                         |
| 1046      | JEDEC, “ <i>Minutes of Meeting No. 158 JC-40 Digital Logic Committee</i> ” (June 4, 2009)                                                           |
| 1047      | <i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00548, Exhibit 2009, (PTAB September 6, 2017)                                                |
| 1048      | JEDEC, JEDEC Manual of Organization and Procedure, JM21P (Rev. of JM21N, May 2008) (May 2010)                                                       |

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| 1049      | JEDEC, JEDEC Manual of Organization and Procedure, JM21N (Rev. of JM21M, December 2006) (May 2008)                                   |
| 1050      | Declaration of Julie Carlson                                                                                                         |
| 1051      | JEDEC, “Committee Letter Ballot, JC-40.4-09-320, Item 142.35,” (Dec. 2009)                                                           |
| 1052      | JEDEC, “Committee Letter Ballot, JC-45.4-09-321, Item 2192.44,” (Dec. 2009)                                                          |
| 1053      | JEDEC, “Tally of Votes, Committee Letter Ballot, JC-45.4-09-321, 2192.44” (Dec. 9, 2009)                                             |
| 1054      | Declaration of John Halbert                                                                                                          |
| 1055      | Declaration of Sung Joo Park                                                                                                         |
| 1056      | JEDEC Standard, DDR3 SDRAM, JESD79-3C (November 2008) (“JESD79-3C”)                                                                  |
| 1057      | U.S. Patent No. 7,647,467 to Hutsell et al.                                                                                          |
| 1058      | <i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2020-1042, Paper No. 1 (PTAB June 8, 2020) (595 Patent Petition)                   |
| 1059      | <i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2020-1042, Paper No. 14 (PTAB December 17, 2020) (595 Patent Institution Decision) |
| 1060      | <i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2020-1042, Paper No. 25 (PTAB May 6, 2021) (595 Patent Termination Order)          |
| 1061      | <i>Netlist, Inc. v. SK hynix Inc. et al.</i> , 6-20-cv-00194-ADA (W.D. Tex. March 12, 2021) (Claim Construction Order)               |
| 1062      | <i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2020-1044, Paper No. 1 (PTAB June 8, 2020) (218 Patent Institution Decision)       |
| 1063      | Netlist’s 8-K announcing patent cross license with Samsung on November 12, 2015                                                      |

| Exhibit # | Description                                                                                                                                                                                                                                                          |
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| 1064      | Defendant Samsung’s Motion for Judgment on the Pleadings in <i>Netlist Inc. v. Samsung Electronics Co., Ltd.</i> , No. 8:20-cv-00993, ECF No. 60 (C.D. Cal. June 22, 2021)                                                                                           |
| 1065      | Order denying Samsung’s Motion for Judgment on the Pleadings in <i>Netlist Inc. v. Samsung Electronics Co., Ltd.</i> , No. 8:20-cv-00993, ECF No. 120 (C.D. Cal. Aug. 5, 2021)                                                                                       |
| 1066      | Plaintiff Netlist’s Motion for Partial Summary Judgment in <i>Netlist Inc. v. Samsung Electronics Co., Ltd.</i> , No. 8:20-cv-00993, ECF No. 145 (C.D. Cal. Aug. 16, 2021)                                                                                           |
| 1067      | Complaint for Declaratory Judgment of Non-Infringement in <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)                                                                                             |
| 1068      | First Amended Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:21-cv-01453 (D. Del. filed Jan. 18, 2022)                                        |
| 1069      | Tektronix Application Note, <i>Electrical Verification of DDR Memory</i> (2009)                                                                                                                                                                                      |
| 1070      | Bruce Jacob et al., <i>Memory Systems: Cache, DRAM, Disk</i> (2008)                                                                                                                                                                                                  |
| 1071      | JEDEC’s 2009 Meeting Schedule (Apr. 6, 2009),<br><a href="https://web.archive.org/web/20090406143859/http://www.jedec.org/service_members/Meetings/09Sch.cfm">https://web.archive.org/web/20090406143859/http://www.jedec.org/service_members/Meetings/09Sch.cfm</a> |
| 1072      | JEDEC’s Catalogue (Apr. 21, 2009),<br><a href="http://web.archive.org/web/20090421000459/http://www.jedec.org/Catalog/display.cfm">http://web.archive.org/web/20090421000459/http://www.jedec.org/Catalog/display.cfm</a>                                            |
| 1073      | Join JEDEC (Apr. 10, 2009),<br><a href="https://web.archive.org/web/20090410060243/http://www.jedec.org/join_jedec/default.cfm">https://web.archive.org/web/20090410060243/http://www.jedec.org/join_jedec/default.cfm</a>                                           |

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| 1074      | JEDEC Member Companies (May 5, 2009),<br><a href="https://web.archive.org/web/20090505225114/http://www.jedec.org/service_members/New_Members/memberco.cfm">https://web.archive.org/web/20090505225114/http://www.jedec.org/service_members/New_Members/memberco.cfm</a> |
| 1075      | JEDEC Benefits (Apr. 13, 2009),<br><a href="https://web.archive.org/web/20090413045324/http://www.jedec.org/join_jedec/benefits.cfm">https://web.archive.org/web/20090413045324/http://www.jedec.org/join_jedec/benefits.cfm</a>                                         |
| 1076      | Declaration by the Internet Archive for Exhibits 1071–75 (Aug. 5, 2022)                                                                                                                                                                                                  |
| 1077      | Transcript of Deposition of Robert J. Murphy (Oct. 27, 2022)                                                                                                                                                                                                             |
| 1078      | Redline comparing Declaration of Robert J. Murphy in IPR2022-00064 (595 Patent) [Ex. 1106] to Declaration of Robert J. Murphy in IPR2022-00062 (218 Patent) [Ex. 1105]                                                                                                   |
| 1079      | Netlist’s Technology Tutorial                                                                                                                                                                                                                                            |
| 1080      | [Replaced by Exhibit 1081] Annotation of DDR3 LRDIMM showing location of (1) Host Interface CA Clk-to-CMD Training, (2) MB Initialization, (3) MB-DRAM Training, and (4) Host-MB Training                                                                                |
| 1081      | <u>Corrected</u> annotation of DDR3 LRDIMM showing location of (1) Host Interface CA Clk-to-CMD Training, (2) MB Initialization, (3) MB-DRAM Training, and (4) Host-MB Training                                                                                          |
| 1082      | Petitioner’s Demonstratives for Oral Argument on February 15, 2023                                                                                                                                                                                                       |
| 1083      | JEDEC 21-C Standard, DDR SDRAM Registered DIMM (Jan. 2002)                                                                                                                                                                                                               |
| 1084      | JESD79-2B, JEDEC DDR2 SDRAM Standard (Jan. 2005)                                                                                                                                                                                                                         |
| 1085      | JESD79-3, JEDEC DDR3 SDRAM Standard (June 2007) (Exhibit 1037 in IPR2018-00303)                                                                                                                                                                                          |
| 1086      | JEDEC’s Catalogue (July 27, 2004),<br><a href="https://web.archive.org/web/20040727032111/http://www.jedec.org/Catalog/display.cfm">https://web.archive.org/web/20040727032111/http://www.jedec.org/Catalog/display.cfm</a>                                              |

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| 1087      | JEDEC download page for JESD99A.01 (Nov. 26, 2003),<br><a href="https://web.archive.org/web/20031126173530/http://www.jedec.org/download/search/jesd99a01.pdf">https://web.archive.org/web/20031126173530/<br/>http://www.jedec.org/download/search/jesd99a01.pdf</a> |
| 1088      | JEDEC Standard JESD99A.01, <i>Terms, Definitions, and Letter Symbols for Microelectronics Devices</i> (May 2003)                                                                                                                                                      |
| 1089      | Harold S. Stone, <i>Microcomputer Interfacing</i> (1982)                                                                                                                                                                                                              |
| 1090      | U.S. Patent No. 8,386,722 to Wang et al.                                                                                                                                                                                                                              |
| 1091      | Deposition of John Bentley Halbert, III (July 22, 2022) [Exhibit 2022 in IPR2022-00062 and -00064]                                                                                                                                                                    |
| 1092      | Deposition of Julie Carlson (July 22, 2022) [Exhibit 2024 in IPR2022-00062 and -00064]                                                                                                                                                                                |
| 1093      | Deposition of Sung Joo Park (July 28, 2022) [Exhibit 2025 in IPR2022-00062 and -00064]                                                                                                                                                                                |
| 1094      | U.S. Patent No. 9,311,116 (issued Apr. 12, 2016)                                                                                                                                                                                                                      |
| 1095      | U.S. Patent No. 9,858,218 (issued Jan. 2, 2018)                                                                                                                                                                                                                       |
| 1096      | File History of U.S. Patent No. 10,474,595                                                                                                                                                                                                                            |
| 1097      | U.S. Patent No. 10,474,595                                                                                                                                                                                                                                            |
| 1098      | Petition of <i>Inter Partes</i> Review of U.S. Patent No. 9,858,218, IPR2022-00062, Paper No. 1 (PTAB Oct. 15, 2021)                                                                                                                                                  |
| 1099      | Declaration of Dr. Donald Alpert Regarding U.S. Patent No. 9,858,218, IPR2022-00062, Exhibit 1003 (PTAB Oct. 15, 2021)                                                                                                                                                |
| 1100      | Petition of <i>Inter Partes</i> Review of U.S. Patent No. 10,474,595, IPR2022-00064, Paper No. 1 (PTAB Oct. 15, 2021)                                                                                                                                                 |
| 1101      | Declaration of Dr. Donald Alpert Regarding U.S. Patent No. 10,474,595, IPR2022-00064, Exhibit 1003 (PTAB Oct. 15, 2021)                                                                                                                                               |

Petition for *Inter Partes* Review of U.S. Patent No. 11,386,024

| Exhibit # | Description                                                                                                                                                                                          |
|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1102      | Final Written Decision, IPR2022-00062, Paper No. 54 (PTAB May 8, 2023) (U.S. Patent No. 9,858,218)                                                                                                   |
| 1103      | Final Written Decision, IPR2022-00064, Paper No. 54 (PTAB May 9, 2023) (U.S. Patent No. 10,474,595)                                                                                                  |
| 1104      | Order dismissing appeals of IPR2022-00062 and -00064, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd.</i> , No. 23-2182 (Fed. Cir. Oct. 19, 2023)                                                  |
| 1105      | Declaration of Robert J. Murphy, Ex. 2027 in IPR2022-00062 (218 Patent)                                                                                                                              |
| 1106      | Declaration of Robert J. Murphy, Ex. 2027 in IPR2022-00064 (595 Patent)                                                                                                                              |
| 1107      | Deposition of Steven Przybylski (Feb. 15–16, 2024)                                                                                                                                                   |
| 1108      | Institution Decision, IPR2022-00062, Paper No. 14 (PTAB May 16, 2022) (U.S. Patent No. 9,858,218)                                                                                                    |
| 1109      | Institution Decision, IPR2022-00064, Paper No. 14 (PTAB May 16, 2022) (U.S. Patent No. 10,474,595)                                                                                                   |
| 1110      | U.S. Patent Application No. 12/144,396 to Wang (filed June 23, 2008)                                                                                                                                 |
| 1111      | [intentionally omitted]                                                                                                                                                                              |
| 1112      | [intentionally omitted]                                                                                                                                                                              |
| 1113      | <i>Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation</i> (June 21, 2022)                                                             |
| 1114      | Complaint for Declaratory Judgment of Non-Infringement in <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:23-cv-01122 (D. Del. filed Oct. 9, 2023) (U.S. Patent No. 11,386,024) |

Petition for *Inter Partes* Review of U.S. Patent No. 11,386,024

| Exhibit # | Description                                                                                                                                                                                          |
|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1115      | Complaint for Declaratory Judgment of Non-Infringement in <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:24-cv-00614 (D. Del. filed May 22, 2024) (U.S. Patent No. 11,880,319) |

**CLAIM LISTING**

| <b>Ref. #</b> | <b>Listing of Challenged Claims in the 024 Patent</b>                                                                                                                                                                                                                                                                                                                  |
|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>1.a</b>    | A memory module operable with a memory controller of a host system, comprising:                                                                                                                                                                                                                                                                                        |
| <b>1.b.1</b>  | a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,                                                                                                                                                                                              |
| <b>1.b.2</b>  | the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;                                                                                                                                                                                |
| <b>1.c.1</b>  | a module controller on the printed circuit board and                                                                                                                                                                                                                                                                                                                   |
| <b>1.c.2</b>  | configured to receive address and control signals associated with normal memory read or write operations via the first edge connections; and                                                                                                                                                                                                                           |
| <b>1.d.1</b>  | dynamic random access memory elements on the printed circuit board and                                                                                                                                                                                                                                                                                                 |
| <b>1.d.2</b>  | configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and                                                                                                                                                                                                              |
| <b>1.e.1</b>  | wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;                                                                                                                                                                                                                 |
| <b>1.e.2</b>  | wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation; and                                                                                                                                 |
| <b>1.e.3</b>  | wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations. |
| <b>2</b>      | The memory module of claim 1, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.                                                                             |

| Ref. # | Listing of Challenged Claims in the 024 Patent                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3      | The memory module of claim 2, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state.                                                                                                                                                                                                                                                                                                                                                |
| 4      | The memory module of claim 2, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.                                                                                                                                                                                                                                                                        |
| 5      | The memory module of claim 4, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.                                                                                                                                                                                                                                                                                                                                                                            |
| 6      | The memory module of claim 1, wherein the module controller comprises an integrated circuit that includes the transistor.                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7      | The memory module of claim 1, wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.                                                                                                                                                                                                                         |
| 8      | The memory module of claim 1, wherein the second edge connections are not active during the operations associated with the one or more training sequences.                                                                                                                                                                                                                                                                                                                                                                                             |
| 9      | The memory module of claim 1, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input configured to receive the first signal, and a second input configured to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences. |
| 10.a   | A method of operation in a host system having a memory controller, comprising:                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 10.b.1 | at a memory module coupled to the memory controller,                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 10.b.2 | the memory module including a printed circuit board,                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 10.c   | a module controller on the printed circuit board, and                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 10.d   | dynamic random access memory elements on the printed circuit board,                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

| Ref. #        | Listing of Challenged Claims in the 024 Patent                                                                                                                                                                                                                                                                   |
|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>10.e.1</b> | the printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,                                                                                                                                      |
| <b>10.e.2</b> | the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections,                                                                                                                          |
| <b>10.f</b>   | the module controller including a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;                                                                                                                                                                  |
| <b>10.g</b>   | receiving, at the module controller, address and control signals associated with one or more normal memory read or write operations from the memory controller via the first edge connections;                                                                                                                   |
| <b>10.h</b>   | outputting or receiving data signals at the dynamic random access memory elements in accordance with the address and control signals, the data signals being associated with the one or more normal memory read or write operations and communicated with the memory controller via the second edge connections; |
| <b>10.i</b>   | applying a first signal to the gate of the transistor to indicate a parity error having occurred during one of the one or more normal memory read or write operations;                                                                                                                                           |
| <b>10.j</b>   | performing training operations associated with one or more training sequences when the dynamic random access memory elements are not accessed for any normal memory read or write operations; and                                                                                                                |
| <b>10.k</b>   | applying a second signal related to the one or more training sequences to the gate of the transistor while the memory module performs the training operations.                                                                                                                                                   |
| <b>11</b>     | The method of claim 10, wherein the error edge connection is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.                       |
| <b>12</b>     | The method of claim 11, wherein the error edge connection is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state.                                                                                                          |

| Ref. #        | Listing of Challenged Claims in the 024 Patent                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>13</b>     | The method of claim 11, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level, and drives the gate of the transistor low so as to drive the error edge connection to the high impedance state.                                                                                                                                                                                                                     |
| <b>14</b>     | The method of claim 13, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.                                                                                                                                                                                                                                                                                                                         |
| <b>15</b>     | The method of claim 10, wherein the module controller comprises an integrated circuit that includes the transistor.                                                                                                                                                                                                                                                                                                                                                                           |
| <b>16</b>     | The method of claim 10, wherein the training operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.                                                                                                                                                             |
| <b>17</b>     | The method of claim 10, wherein the second edge connections are not active during the training operations associated with the one or more training sequences.                                                                                                                                                                                                                                                                                                                                 |
| <b>18</b>     | The method of claim 10, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein applying the first signal to the gate of the transistor includes coupling the first input to the output, and applying the second signal to the gate of the transistor includes coupling the second input to the output. |
| <b>19.a</b>   | A memory module operable with a memory controller of a host system, comprising:                                                                                                                                                                                                                                                                                                                                                                                                               |
| <b>19.b.1</b> | a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller,                                                                                                                                                                                                                                                                                                                     |
| <b>19.b.2</b> | the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;                                                                                                                                                                                                                                                                                                       |
| <b>19.c.1</b> | a module controller on the printed circuit board and                                                                                                                                                                                                                                                                                                                                                                                                                                          |

| Ref. #        | Listing of Challenged Claims in the 024 Patent                                                                                                                                                                                                                                                                                                                         |
|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>19.c.2</b> | configured to receive from the memory controller via the first edge connections address and control signals associated with normal memory read or write operations; and                                                                                                                                                                                                |
| <b>19.d.1</b> | dynamic random access memory elements on the printed circuit board and                                                                                                                                                                                                                                                                                                 |
| <b>19.d.2</b> | configured to communicate data signals with the memory controller via the second edge connections in accordance with the address and control signals; and                                                                                                                                                                                                              |
| <b>19.e.1</b> | wherein the module controller includes a transistor having an open drain coupled to the error edge connection, a source coupled to ground, and a gate;                                                                                                                                                                                                                 |
| <b>19.e.2</b> | wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation;                                                                                                                                     |
| <b>19.e.3</b> | wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations; |
| <b>19.f</b>   | wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground;                                                                                                                                                                                                                          |
| <b>19.g</b>   | wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to a low impedance state, and drives the gate of the transistor low so as to drive the error edge connection to a high impedance state;                                                                                                                      |
| <b>19.h</b>   | wherein the module controller comprises an integrated circuit that includes the transistor; and                                                                                                                                                                                                                                                                        |

| Ref. #      | Listing of Challenged Claims in the 024 Patent                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
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| <b>19.i</b> | wherein the integrated circuit further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences. |
| <b>20</b>   | The memory module of claim 19, wherein the operations associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations with the memory controller via the second edge connections.                                                                                                                                                                     |

| Ref. #     | Listing of Invalidated Claims in the '623 Patent [EX1031, EX1034]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>1.a</b> | A memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system, the memory module comprising:                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <b>1.b</b> | a module controller having an open drain output, the module controller generating a parity error signal and driving the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode, the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode, wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system, |
| <b>1.c</b> | the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode and outputting the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode; and                                                                                                                                                                                                                                                |
| <b>1.d</b> | a printed circuit board having a first set of edge connections for communicating address and control signals from the memory controller of the host system, a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module controller,                                                                                                                                       |
| <b>1.e</b> | the memory module communicating to the memory controller of the host system via the error edge connection the parity error signal while the memory module operates in the first mode and the notification signal while the memory module is in the second mode.                                                                                                                                                                                                                                                                                                                      |
| <b>2</b>   | The memory module of claim 1, further comprising: a plurality of synchronous dynamic random access memory elements, wherein, while the memory module is in the first mode, the module controller receives and processes address and control signals corresponding to read or write commands from the memory controller of the host system and transmits processed address and control signals to the plurality of synchronous dynamic random access memory elements.                                                                                                                 |

| <b>Ref. #</b> | <b>Listing of Invalidated Claims in the '623 Patent [EX1031, EX1034]</b>                                                                                                                                                                                                                 |
|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>3</b>      | The memory module of claim 1, wherein, while the memory module is in the second mode, the module controller drives the notification signal to a logic low level via the open drain output to indicate a status of the one or more training sequences.                                    |
| <b>4</b>      | The memory module of claim 1, wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module.                                                                                                                           |
| <b>5</b>      | The memory module of claim 1, wherein the one or more training sequences are executed by the module controller in response to a command or a signal received from the memory controller of the host system.                                                                              |
| <b>6</b>      | The memory module of claim 1, wherein the module controller comprises one or more integrated circuit.                                                                                                                                                                                    |
| <b>7</b>      | The memory module of claim 1, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.                                                                                               |
| <b>8</b>      | The memory module of claim 7, wherein the notification circuit generates the notification signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground. |
| <b>9</b>      | The memory module of claim 7, wherein the notification circuit generates the parity error signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground. |
| <b>10</b>     | The memory module of claim 7, wherein the notification circuit generates the notification signal using one or more OR logic elements.                                                                                                                                                    |
| <b>11</b>     | The memory module of claim 1, wherein the module controller implements the one or more training sequences in response to a signal or a command received from the memory controller of the host system.                                                                                   |
| <b>12.a</b>   | A memory module to be coupled to a memory controller of a host system, the memory module comprising:                                                                                                                                                                                     |

| Ref. #      | Listing of Invalidated Claims in the '623 Patent [EX1031, EX1034]                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>12.b</b> | a plurality of synchronous dynamic random access memory elements;                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <b>12.c</b> | a printed circuit board (PCB) having a first set of edge connections for communicating address and control signals from the memory controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in a first mode, the PCB further including an error edge connection in addition to the first set of edge connections and the second set of edge connections;                       |
| <b>12.d</b> | a module circuit controlling the plurality of synchronous dynamic random access memory elements in response to read and write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode,                                                                                                                                                                                                                                          |
| <b>12.e</b> | the module circuit generating a parity error signal indicative of a parity error having occurred in the memory module while the memory module operates in the first mode,                                                                                                                                                                                                                                                                                                                                                        |
| <b>12.f</b> | the module circuit causing the memory module to enter a second mode in response to a command from the memory controller of the host system, the module circuit generating a notification signal in response to one or more training sequences while the memory module is in the second mode, the notification signal indicating a status of the one or more training sequences; and                                                                                                                                              |
| <b>12.g</b> | a notification circuit having an open drain output coupled to the error edge connection of the PCB, the notification circuit driving the parity error signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module operates in the first mode, the notification circuit driving the notification signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the second mode. |
| <b>13</b>   | The memory module of claim 12, wherein the memory module executes the one or more training sequences in response to a signal or a command from the memory controller of the host system.                                                                                                                                                                                                                                                                                                                                         |

| <b>Ref. #</b> | <b>Listing of Invalidated Claims in the '623 Patent [EX1031, EX1034]</b>                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>14</b>     | The memory module of claim 12, wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module.                                                                                                                                                                                                                                                                                                                                              |
| <b>15</b>     | The memory module of claim 12, wherein the notification circuit generates the notification signal using one or more OR logic elements.                                                                                                                                                                                                                                                                                                                                                                       |
| <b>16</b>     | The memory module of claim 12, wherein the notification circuit is a physically separate circuit from the module circuit.                                                                                                                                                                                                                                                                                                                                                                                    |
| <b>17</b>     | The memory module of claim 12, wherein the module circuit includes the notification circuit.                                                                                                                                                                                                                                                                                                                                                                                                                 |
| <b>18</b>     | The memory module of claim 12, wherein the notification circuit includes one or more transistors each having an open drain coupled to the open drain output.                                                                                                                                                                                                                                                                                                                                                 |
| <b>19</b>     | The memory module of claim 18, wherein the notification circuit generates the notification signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.                                                                                                                                                                                                                    |
| <b>20</b>     | The memory module of claim 18, wherein the notification circuit generates the parity error signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.                                                                                                                                                                                                                    |
| <b>21.a</b>   | A memory module operable in at least a first mode and a second mode, the memory module comprising:                                                                                                                                                                                                                                                                                                                                                                                                           |
| <b>21.b</b>   | a plurality of synchronous dynamic random access memory elements;                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>21.c</b>   | a printed circuit board (PCB) having a first set of edge connections for communicating address and control signals from the memory controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, the PCB further including an error edge connection in addition to the first set of edge connections and the second set of edge connections, |

| Ref. #      | Listing of Invalidated Claims in the '623 Patent [EX1031, EX1034]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
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| <b>21.d</b> | wherein the PCB is configured to fit into a corresponding slot connector of the host system; and                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| <b>21.e</b> | a module controller having an open drain output coupled to the error edge connection, the module controller being configured to transmit address and control signals to the plurality of synchronous dynamic random access memory elements in response to read or write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode, to generate a parity error signal indicating a parity error having occurred in the memory module while the memory module is in the first mode, and to transmit the parity error signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the first mode, |
| <b>21.f</b> | the module controller being further configured to cause the memory module to enter the second mode in response to a command from the memory controller of the host system, to generate a notification signal indicating a status of one or more training sequences while the memory module is in the second mode, and to transmit the notification signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the second mode.                                                                                                                                                                                                                                                               |
| <b>22</b>   | The memory module of claim 21, wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>23</b>   | The memory module of claim 21, wherein the memory module executes the one or more training sequences in response to a command or a signal received from the memory controller of the host system.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| <b>24</b>   | The memory module of claim 21, wherein the module controller includes a notification circuit comprising one or more transistors, each of the one or more transistors having an open drain coupled to the open drain output.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

| <b>Ref. #</b> | <b>Listing of Invalidated Claims in the '623 Patent [EX1031, EX1034]</b>                                                                                                                                                                                                                                     |
|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>25</b>     | The memory module of claim 24, wherein the notification circuit is configured to generate the notification signal by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.    |
| <b>26</b>     | The memory module of claim 24, wherein the notification circuit is configured to generate the parity error signal by by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground. |
| <b>27</b>     | The memory module of claim 24, wherein the notification circuit is configured to generate the notification signal using one or more OR logic elements.                                                                                                                                                       |
| <b>28</b>     | The memory module of claim 24, wherein the module controller comprises one or more integrated circuits.                                                                                                                                                                                                      |
| <b>29</b>     | The memory module of claim 21, wherein the module controller is further configured to implement the one or more training sequences in response to a signal or a command received from the memory controller of the host system.                                                                              |

| Ref. #     | Listing of Invalidated Claims in the '218 Patent [EX1095, EX1102]                                                                                                                                                                                                                                                                                                 |
|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>1.a</b> | A memory module operable with a memory controller of a host system, comprising:                                                                                                                                                                                                                                                                                   |
| <b>1.b</b> | a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections; |
| <b>1.c</b> | dynamic random access memory elements on the printed circuit board;                                                                                                                                                                                                                                                                                               |
| <b>1.d</b> | a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and                                                                                                                                                            |
| <b>1.e</b> | [i] wherein the memory module is operable in at least a first mode and a second mode,<br>[ii] wherein the memory module in the first mode is configured to be trained with one or more training sequences;                                                                                                                                                        |
| <b>1.f</b> | wherein the memory module in the second mode is configured to perform one or more memory read or write operations not associated with the one or more training sequences by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections;                                        |
| <b>1.g</b> | [i] wherein the module controller is configured to receive via the second edge connections the address and command signals associated with the one or more memory read or write operations and<br>[ii] to control the dynamic random access memory elements in accordance with the address and command signals, and                                               |
| <b>1.h</b> | wherein the module controller is further configured to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the second mode;                                                                                                                                           |

| Ref. #     | Listing of Invalidated Claims in the '218 Patent [EX1095, EX1102]                                                                                                                                                                                                       |
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| <b>1.i</b> | wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output while the memory module is in the first mode.                              |
| <b>2</b>   | The memory module of claim 1, wherein the module controller comprises an integrated circuit.                                                                                                                                                                            |
| <b>3</b>   | The memory module of claim 1, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.                                                                              |
| <b>4</b>   | The memory module of claim 3, wherein the notification circuit is configured to drive the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.   |
| <b>5</b>   | The memory module of claim 4, wherein the notification circuit is configured to drive the parity error signal by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground. |
| <b>6</b>   | The memory module of claim 4, wherein the notification circuit is configured to drive the notification signal using one or more OR logic elements.                                                                                                                      |
| <b>7</b>   | The memory module of claim 1, wherein the first edge connections are not active when the memory module is in the first mode and configured to be trained with the one or more training sequences.                                                                       |
| <b>8</b>   | The memory module of claim 1, wherein the module controller is configured to drive the notification signal to indicate a status of the one or more training sequences.                                                                                                  |
| <b>9.a</b> | A method performed by a memory module operating with a memory controller of the host system,                                                                                                                                                                            |
| <b>9.b</b> | the memory module including dynamic random access memory elements on a printed circuit board,                                                                                                                                                                           |

| Ref. #     | Listing of Invalidated Claims in the '218 Patent [EX1095, EX1102]                                                                                                                                                                                                                                                                                                                                                                                                                                                |
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| <b>9.c</b> | the printed circuit board having edge connections that fit into a corresponding slot of a host system, the edge connections including first edge connections via which the dynamic random access memory devices communicate data with the memory controller, second edge connections via which the memory module receives address and command signals from the memory controller, and an error edge connection in addition to the first edge connections and the second edge connections, the method comprising: |
| <b>9.d</b> | receiving from the memory controller address and command signals associated with one or more memory read or write operations;                                                                                                                                                                                                                                                                                                                                                                                    |
| <b>9.e</b> | controlling the dynamic random access memory elements in accordance with the address and command signals;                                                                                                                                                                                                                                                                                                                                                                                                        |
| <b>9.f</b> | outputting to the memory controller via an open-drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module; and                                                                                                                                                                                                                                                                                                                                   |
| <b>9.g</b> | training with one or more training sequences while the first edge connections are not active, and                                                                                                                                                                                                                                                                                                                                                                                                                |
| <b>9.h</b> | driving a notification signal associated with the one or more training sequences to the memory controller via the open drain output and the error edge connection.                                                                                                                                                                                                                                                                                                                                               |
| <b>10</b>  | The method of claim 9, wherein driving the notification signal comprises driving a gate of each of one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground, the one or more transistors each having an open drain coupled to the open drain output.                                                                                                                                                                                                   |
| <b>11</b>  | The method of claim 10, wherein driving the signal indicating the parity error comprises driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground.                                                                                                                                                                                                                                                                     |
| <b>12</b>  | The method of claim 10, wherein driving the notification signal comprises using one or more OR logic elements.                                                                                                                                                                                                                                                                                                                                                                                                   |
| <b>13</b>  | The method of claim 9, wherein the memory module is configured to be trained with the one or more training sequences in response to a request by the memory controller.                                                                                                                                                                                                                                                                                                                                          |

| <b>Ref. #</b> | <b>Listing of Invalidated Claims in the '218 Patent [EX1095, EX1102]</b>                                                                                                                                                                                                                                                                                                                                                                                                                        |
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| <b>14</b>     | The method of claim 9, wherein the notification signal indicates a status of the one or more training sequences.                                                                                                                                                                                                                                                                                                                                                                                |
| <b>15.a</b>   | A memory module operable with a memory controller of a host system, comprising:                                                                                                                                                                                                                                                                                                                                                                                                                 |
| <b>15.b</b>   | a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and command signals, and an error edge connection in addition to the first edge connections and the second edge connections; |
| <b>15.c</b>   | dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the first edge connections; and                                                                                                                                                                                                                                                                                                                  |
| <b>15.d</b>   | a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection;                                                                                                                                                                                                                                                                                              |
| <b>15.e</b>   | wherein the memory module is configurable to perform at least a first operation and a second operation;                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>15.f</b>   | [i] wherein the module controller in the first operation is configured to receive via the second edge connections address and command signals associated with one or more memory read or write operations and<br>[ii] to control the dynamic random access memory elements in accordance with the address and command signals,                                                                                                                                                                  |
| <b>15.g</b>   | wherein the module controller in the first operation is further configured to output to the memory controller a signal indicating a parity error having occurred in the memory module; and                                                                                                                                                                                                                                                                                                      |
| <b>15.h</b>   | wherein the memory module in the second operation is configured to be trained with one or more training sequences while the first edge connections are not active, and                                                                                                                                                                                                                                                                                                                          |
| <b>15.i</b>   | wherein the module controller in the second operation is configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output of the module controller.                                                                                                                                                                                                                                                          |

| <b>Ref. #</b> | <b>Listing of Invalidated Claims in the '218 Patent [EX1095, EX1102]</b>                                                                                                                                                                                                                |
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| <b>16</b>     | The memory module of claim 15, wherein the module controller comprises an integrated circuit.                                                                                                                                                                                           |
| <b>17</b>     | The memory module of claim 15, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.                                                                                             |
| <b>18</b>     | The memory module of claim 17, wherein the notification circuit is configured to generate the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.               |
| <b>19</b>     | The memory module of claim 18, wherein the notification circuit is configured to drive the signal indicating the parity error by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground. |
| <b>20</b>     | The memory module of claim 18, wherein the notification circuit is configured to drive the notification signal using one or more OR logic elements.                                                                                                                                     |
| <b>21</b>     | The memory module of claim 15, wherein the memory module is configured to perform the second operation in response to a command from the memory controller.                                                                                                                             |
| <b>22</b>     | The memory module of claim 15, wherein the module controller is configured to drive the notification signal to indicate a status of the one or more training sequences.                                                                                                                 |

| Ref. #     | Listing of Invalidated Claims in the '595 Patent [EX1097, EX1103]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
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| <b>1.a</b> | A memory module operable with a memory controller of a host system, comprising:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>1.b</b> | a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;                                                                                                                                                                                                         |
| <b>1.c</b> | dynamic random access memory elements on the printed circuit board;                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <b>1.d</b> | a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| <b>1.e</b> | <p>[i] wherein the memory module is configurable to operate in any of at least a first mode and a second mode;</p> <p>[ii] wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections,</p> <p>[iii] wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and</p> <p>[iv] wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;</p> |

| Ref. #     | Listing of Invalidated Claims in the '595 Patent [EX1097, EX1103]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
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| <b>1.f</b> | <p>[i] wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations,</p> <p>[ii] wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and</p> <p>[iii] wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;</p> |
| <b>1.g</b> | <p>wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.</p>                                                                                                                                                                                                                                                         |
| <b>2</b>   | <p>The memory module of claim 1, wherein the module controller comprises an integrated circuit.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>3</b>   | <p>The memory module of claim 1, wherein the module controller includes a notification circuit comprising a transistor having an open drain coupled to the open drain output and source coupled to the ground.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| <b>4</b>   | <p>The memory module of claim 3, wherein the module controller is configurable to drive a gate of the transistor high so as to drive open drain output and the error edge connection to ground, or to drive the gate of the transistor low so as to drive the open drain output and the error edge connection to the high impedance state.</p>                                                                                                                                                                                                                                                                                                                                 |
| <b>5</b>   | <p>The memory module of claim 4, wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and the ground.</p>                                                                                                                                                                                                                                                                                                                                                                                                     |

| <b>Ref. #</b> | <b>Listing of Invalidated Claims in the '595 Patent [EX1097, EX1103]</b>                                                                                                                                                                                                                                                                                                                                                                                                                        |
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| <b>6</b>      | The memory module of claim 3, wherein the notification circuit further includes a multiplexor or a logic circuit having a output coupled to a gate of the transistor and configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.                                                                                                                                              |
| <b>7</b>      | The memory module of claim 3, wherein the module controller is configurable to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal so as to drive the open drain output from the high impedance state to ground or from ground to the high impedance state.                                                                                                                                                        |
| <b>8</b>      | The memory module of claim 1, wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode.                                                                                                                                                                                                                                                                                                                                   |
| <b>9</b>      | The memory module of claim 1, wherein the memory module in the second mode is configurable to perform the operations related to the one or more training sequences without communicating data signals via the first edge connections while the memory module is in the second mode.                                                                                                                                                                                                             |
| <b>10.a</b>   | A memory module operable with a memory controller of a host system, comprising:                                                                                                                                                                                                                                                                                                                                                                                                                 |
| <b>10.b</b>   | a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections; |
| <b>10.c</b>   | dynamic random access memory elements on the printed circuit board;                                                                                                                                                                                                                                                                                                                                                                                                                             |

| Ref. #      | Listing of Invalidated Claims in the '595 Patent [EX1097, EX1103]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
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| <b>10.d</b> | a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and                                                                                                                                                                                        |
| <b>10.e</b> | wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections;                                            |
| <b>10.f</b> | wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode; |
| <b>10.g</b> | wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode.                                                                                                                                                                                                                                                                                                                                                                                                          |
| <b>11</b>   | The memory module of claim 10, wherein the module controller comprises an integrated circuit.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

| Ref. #      | Listing of Invalidated Claims in the '595 Patent [EX1097, EX1103]                                                                                                                                                                                                                                                                                                                                                       |
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| <b>12.a</b> | The memory module of claim 10, wherein the module controller includes a notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to the ground,                                                                                                                                                                                                                |
| <b>12.b</b> | wherein the module controller is configurable to output to the memory controller the open-drain signals related to the one or more training sequences by driving a gate of the transistor high so as to drive the open drain output and the error edge connection to ground, and by driving the gate of the transistor low as to drive the open drain output and the error edge connection to the high impedance state, |
| <b>12.c</b> | and wherein the notification circuit is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and ground.                                                                                                                                                                                |
| <b>13</b>   | The memory module of claim 12, wherein the notification circuit further includes a multiplexor or a logic circuit having an output coupled to the gate of the transistor and configurable to drive the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.                                                                              |
| <b>14</b>   | The memory module of claim 10, wherein the module controller is configurable to output the open-drain signals related to the one or more training sequences by driving the open drain output from the high impedance state to the low logic level or from the low logic level to the high impedance state.                                                                                                              |
| <b>15</b>   | The memory module of claim 10, wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode.                                                                                                                                                                                                                                                          |
| <b>16</b>   | The memory module of claim 10, wherein the second edge connections include one or more high-order address pins that are not active while the memory module is in the second mode.                                                                                                                                                                                                                                       |
| <b>17.a</b> | A method, comprising:                                                                                                                                                                                                                                                                                                                                                                                                   |

| Ref. #      | Listing of Invalidated Claims in the '595 Patent [EX1097, EX1103]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
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| <b>17.b</b> | at a memory module coupled with a memory controller of a host system, the memory module including a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections, the memory module further including dynamic random access memory elements on the printed circuit board; |
| <b>17.c</b> | receiving via the second edge connections address and control signals associated with one or more memory read or write operations; controlling the dynamic random access memory elements to communicate data signals corresponding to the one or more memory read or write operations via the first edge connections in response to the address and control signals; outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is being accessed by the memory controller for a memory read or write operation;                                                                            |
| <b>17.d</b> | performing operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations; and outputting to the memory controller via the open drain output and the error edge connection open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation.                                                                                                                                                                                                                                                                                                               |
| <b>18</b>   | The method of claim 17, wherein the second edge connections include one or more pins that are not active while the memory module is trained with the one or more training sequences.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <b>19</b>   | The method of claim 18, wherein the second edge connections include one or more high-order address pins that are not active while the memory module is trained with the one or more training sequences.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <b>20.a</b> | The method of claim 17, wherein the memory module includes a notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to ground,                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

| Ref. #      | Listing of Invalidated Claims in the '595 Patent [EX1097, EX1103]                                                                                                                                                                                                                                                                                                                                                                                                                          |
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| <b>20.b</b> | wherein outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module comprises driving a gate of the transistor high to provide a low impedance path between the open drain output and ground, and                                                                                                                                                                                                     |
| <b>20.c</b> | wherein outputting the open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation comprises driving the gate of the transistor to drive the open drain output from a high impedance state to ground and from ground to the high impedance state.                                                                                                                                                                                 |
| <b>21.a</b> | A memory module operable with a memory controller of a host system, comprising:                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>21.b</b> | a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;                                                                                                                          |
| <b>21.c</b> | dynamic random access memory elements on the printed circuit board; and                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <b>21.d</b> | a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller including a transistor having a gate and an open drain output coupled to the error edge connection; wherein the module controller is configurable to drive the gate of the transistor so as to drive the open drain output to a first state or a second state, the first state being a low logic level and the second state being a high impedance state; |

| Ref. #      | Listing of Invalidated Claims in the '595 Patent [EX1097, EX1103]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
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| <b>21.e</b> | <p>[i] wherein the module controller is configurable to receive via the second edge connections memory commands associated with normal memory read or write operations and to output a set of address and control signals for each of the normal memory read or write operations;</p> <p>[ii] wherein the dynamic random access memory elements are configurable to communicate one or more N-bit-wide data signals with the memory controller via the first edge connections in response to the set of address and control signals, where N is at least 32;</p> <p>[iii] wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred during any of the memory read or write operations by driving the open drain output and the error edge connection to the first state;</p> |
| <b>21.f</b> | <p>wherein the memory module is configurable to perform operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations; and wherein the module controller is configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection from one of the first state and the second state to the other one of the first state and the second state.</p>                                                                                                                                                                                                                                                                                                                                                                       |
| <b>22</b>   | <p>The memory module of claim 21, wherein the module controller further includes a multiplexor or a logic circuit having an output coupled to the gate of the transistor, and wherein the module controller is configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| <b>23.a</b> | <p>The memory module of claim 22, wherein the transistor has a source coupled to ground,</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| <b>23.b</b> | <p>wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and ground, and</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

| <b>Ref. #</b> | <b>Listing of Invalidated Claims in the '595 Patent [EX1097, EX1103]</b>                                                                                                                                                                  |
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| <b>23.c</b>   | wherein the module controller is configurable to provide the information related to the one or more training sequences by driving the open drain output from a high impedance state to ground or from ground to the high impedance state. |
| <b>24</b>     | The memory module of claim 21, wherein the memory module is configurable to perform the operations related to the one or more training sequences while the memory module is not communicating signals via the first edge connections.     |

**I. PETITIONER’S MANDATORY NOTICES**

**A. Real Parties-in-Interest (37 C.F.R. §42.8(b)(1))**

The real parties-in-interest are the Petitioner, Samsung Electronics Co., Ltd., and Samsung Semiconductor, Inc.

**B. Related Matters (37 C.F.R. §42.8(b)(2))**

The following judicial or administrative matters would affect, or be affected by, a decision in this proceeding concerning U.S. Patent No. 11,386,024.

The following proceedings are currently pending:

- *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.*, IPR2025-00002 (U.S. Patent No. 11,880,319)
- *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021) (U.S. Patent Nos. 9,858,218 and 10,474,595)
- *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.*, No. 1:23-cv-01122-RGA (D. Del. filed Oct. 9, 2023) (U.S. Patent No. 11,386,024)
- *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.*, No. 1:24-cv-00614 (D. Del. filed May 22, 2024) (U.S. Patent No. 11,880,319)
- U.S. Application No. 18/413,017

The following proceedings have concluded:

Petition for *Inter Partes* Review of U.S. Patent No. 11,386,024

- *Netlist, Inc. v. SK hynix Inc., et al.*, Nos. 8:16-cv-01605 (C.D. Cal. filed Aug. 31, 2016) (U.S. Patent No. 8,489,837)
- *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (USITC filed Sept. 1, 2016) (U.S. Patent No. 8,489,837)
- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00548 (U.S. Patent No. 8,489,837)
- *Netlist, Inc. v. SK hynix Inc. et al.*, No. 8:17-cv-01030 (C.D. Cal. filed June 14, 2017) (U.S. Patent No. 9,535,623)
- *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1089 (USITC filed Oct. 31, 2017) (U.S. Patent No. 9,535,623)
- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2018-00303 (U.S. Patent No. 9,535,623)
- *Netlist, Inc. v. SK hynix Inc. et al.*, No. 6:20-cv-00194 (W.D. Tex. filed Mar. 17, 2020) (U.S. Patent Nos. 9,858,218 and 10,474,595)
- *SK hynix Inc., et al. v. Netlist, Inc.*, IPR2020-01042 (U.S. Patent No. 10,474,595)
- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2020-01044 (U.S. Patent No. 9,858,218)

- *Samsung Electronics Co., Ltd. v Netlist, Inc.*, IPR2022-00062 (U.S. Patent No. 9,858,218)
- *Samsung Electronics Co., Ltd. v Netlist, Inc.*, IPR2022-00064 (U.S. Patent No. 10,474,595)

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**D. Service Information (37 C.F.R. §42.8(b)(4))**

Service information is provided in the designation of counsel above.

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## II. INTRODUCTION

Petitioner respectfully requests trial on claims 1-20 of U.S. Patent No. 11,386,024 (“’024 Patent”) (EX1001).

## III. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

### A. Standing (§42.104(a))

The ’024 Patent is available for IPR and Petitioner is not barred or estopped from requesting IPR on the below-identified grounds.

### B. Identification of Challenge (§42.104(b))

Petitioner challenges claims 1-20:

| Ground | Claims Challenged | 35 U.S.C. | References               |
|--------|-------------------|-----------|--------------------------|
| 1      | 1-20              | §103(a)   | <u>Hazelzet+JEDEC</u>    |
| 2      |                   |           | <u>Hazelzet+Buchmann</u> |
| 3      |                   |           | <u>Hazelzet+Wang</u>     |
| 4      |                   |           | Ground 1+ <u>Kim</u>     |
| 5      |                   |           | Ground 2+ <u>Kim</u>     |
| 6      |                   |           | Ground 3+ <u>Kim</u>     |

Petitioner provides below its proposed claim constructions and the precise reasons why the claims are unpatentable. The evidence relied upon is listed above, beginning on page viii.

#### **IV. RELEVANT INFORMATION CONCERNING THE CONTESTED PATENT**

##### **A. Estoppel from prior Final Written Decisions against Netlist**

Estoppel precludes Netlist from relitigating virtually every issue presented by this Petition, because the Board, applying the same art as Grounds 2 and 5 here, previously invalidated substantially similar claims in Netlist’s related ’623 (p.xxiii, EX1034), ’218 (p.xxix, EX1102), and ’595 (p.xxxiv, EX1103) Patents. All of those claims have since been canceled by IPR Certificates. EX1031, 16; EX1095, 16; EX1097, 19.

“[C]ollateral estoppel applies to IPR proceedings[]” when (1) “the issue is identical to one decided in the [previous] action,” (2) the issue was “actually litigated,” (3) the issue was “essential” to the previous judgment, and (4) the estopped party “had a full and fair opportunity to litigate the issue.” *Google LLC v. Hammond Dev. Int’l, Inc.*, 54 F.4th 1377, 1381 (Fed. Cir. 2022). In addition, Netlist “is precluded from taking action inconsistent with the adverse judgment[s].” 37 C.F.R. §42.73(d)(3).

With respect to Factor (1), Netlist is “bound...by any subsidiary factual determinations that were actually litigated and essential to the judgment[s].” *Mobile Tech, Inc. v. InVue Security Prods. Inc.*, IPR2018-00481, Paper 29, at 18 (PTAB July 16, 2019); *see also, e.g., VirnetX Inc. v. Apple, Inc.*, 909 F.3d 1375, 1378 (Fed. Cir. 2018) (estopping patentee from relitigating whether reference was

“a printed publication”). As to invalidity of entire patent claims, “collateral estoppel may apply even if the patent claims ‘use slightly different language to describe substantially the same invention,’ so long as ‘the differences between the unadjudicated patent claims and adjudicated patent claims do not materially alter the question of invalidity.’” *Google*, 54 F.4th at 1381; *see also Mobile Tech*, IPR2018-00481, Paper 29, at 22-29. In addition, with respect to at least the ’623 Final Written Decision (dated March 21, 2019), EX1034, resulting in cancellation of those claims on July 13, 2021, EX1031, and with respect to a Final Written Decision against an even earlier patent in the family, EX1035; EX1019, 14, Netlist should have been precluded during prosecution of the ’024 Patent (which started November 11, 2019 and concluded July 12, 2022, *see* EX1002) from “obtaining...any...claim that is not patentably distinct from a finally refused or canceled claim.” 37 C.F.R. §42.73(d)(3)(i); *SoftView LLC v. Apple Inc.*, 108 F.4th 1366 (Fed. Cir. 2024) (applying §42.73(d)(3)(i)).

As discussed below in more detail (pp.55-107), each of the ’024 Patent claims is substantially identical to the claims of the ’623 (p.xxiii), ’218 (p.xxix), and ’595 (p.xxxiv) Patents that the Board found obvious in view of Ground 2 (Hazelzet+Buchmann) and/or Ground 5 (Hazelzet+Buchmann+Kim), EX1003, ¶¶152-155, meaning Netlist is estopped from relitigating those issues here, including the obviousness of the ’024 Patent claims. Indeed, the Examiner

concluded during prosecution that the '024 Patent claims were “not patentably distinct” from the claims of the '595 and '218 Patents. EX1002, 123. Similarly, because the Board previously found motivations to combine Hazelzet+Buchmann (EX1034, 9-20; EX1102, 18-44; EX1103, 19-44) and Hazelzet+Buchmann+Kim (EX1034, 20-21; EX1102, 71-75; EX1103, 78-82), Netlist is also estopped from arguing against the motivations to combine for Grounds 2 and 5 here.

Factors (2), (3), and (4) are satisfied because the obviousness of the '623, '218, and '595 claims over Ground 2 (Hazelzet+Buchmann) and Ground 5 (Hazelzet+Buchmann+Kim) was actually litigated and essential to the Final Written Decisions, and Netlist had full and fair opportunities to litigate all the issues before the Board in each of the three IPRs. *See* EX1034; EX1102; EX1103; EX1031, 16; EX1097, 19; EX1095, 16.

In sum, Netlist has already had three bites at the apple, which is far too many.

**B. Effective filing date: No earlier than June 14, 2010**

The '024 Patent is a continuation of, *inter alia*, an application filed **June 14, 2010**, and also claims priority to Provisional Application No. 61/186,799 (EX1008, “the provisional”), filed **June 12, 2009**. EX1001, Face. The priority date for the claims of the '024 Patent does not matter for Grounds 2-3 and 5-6, but it matters

for Grounds 1 and 4 based on the JEDEC reference (EX1015), which is dated no later than November 11, 2009.

Netlist cannot show §112 support in the provisional for multiple claim limitations, discussed below, and thus JEDEC (EX1015) is prior art to the claims of the '024 Patent. See 35 U.S.C. §119(e)(1); *id.* §112, ¶1; *Parus Holdings, Inc. v. Google LLC*, 70 F.4th 1365, 1371-72 (Fed. Cir. 2023); *Novartis Pharms. Corp. v. Accord Healthcare, Inc.*, 38 F.4th 1013, 1016-17 (Fed. Cir. 2022) (discussing written description for negative claim limitations); *Rivera v. ITC*, 857 F.3d 1315, 1322 (Fed. Cir. 2017) (distinguishing written description from obviousness). The Board has previously recognized in four related Institution Decisions that limitations similar to those identified below lack §112 support in the provisional. See EX1059, 21-27; EX1062, 21-31; EX1108, 18-25; EX1109, 16-24.

**1. Unsupported negative limitation (claims 1, 10, 19)**

All of the independent claims (1, 10, 19) include the negative limitation “when the dynamic random access memory elements are **not accessed** for any normal memory read or write operations,”<sup>1</sup> which is not supported by the provisional. EX1001, 15:46-:49, 16:55-:57, 18:16-:19; EX1003, ¶¶61-71. Indeed,

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<sup>1</sup> All emphasis in quotes, and color highlighting in figures, has been added unless otherwise noted.

the provisional does not mention “*normal memory read or write operations*” at all. EX1008; EX1003, ¶62.

The provisional refers to “normal operation,” but says nothing about the “memory” being “**not accessed** for any normal memory read or write operations”:

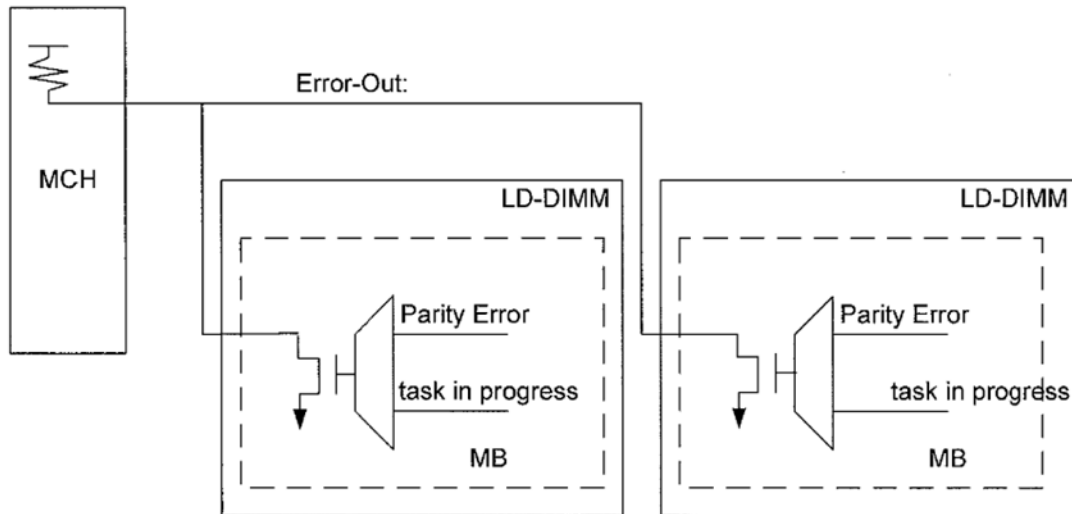


Figure 3: Sharing a pin between the Error-out and Notifying signal

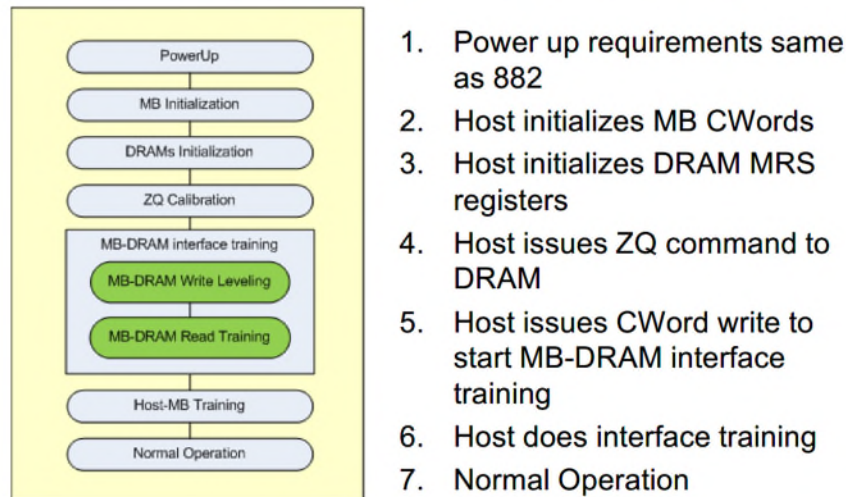
Error-Out pin: Low during MB training (high signal indicates that training is done)  
High during normal operation unless a parity error occurs

EX1008, 25, Fig.3; EX1003, ¶¶63-66. Instead, the provisional describes the Error-Out pin’s “normal operation.” *Id.* The “*normal memory read or write operations*,” however, are ***the same*** even if performed during initialization, and regardless of the Error-out pin’s operation. *Id.* Indeed, JEDEC memories and modules without Error-out pins still perform “*normal memory read or write operations*.” EX1024, p.7 (no Error\_out pin), pp.9-10 (“Normal operation” set in Mode Register); *see also* EX1084, pp.6-7, p.11; EX1056, 13-14, 23-25; EX1083, 6-7.

Netlist has previously made the circular argument that only read/write operations during “normal” or “operational” mode (as opposed to during initialization) are “*normal memory read or write operations*,” but the provisional has no such disclosure. EX1106, ¶¶27-29, 35-37. As the ’024 Patent and even Netlist’s expert admits, normal read/write operations were known to occur during initialization (not just in “normal” mode). EX1001, 7:21-:32 (“standard...memory read/write...in operational mode...can also be performed...while in initialization mode”); EX1015, p.9 (“normal [writes/reads]” during DQ/DQS training); EX1021, 17:15-:19 (“initialization sequences and normal operations...at the same time...is well known in the industry”); *see also* EX1069, p.11; EX1056, pp.33, 55-76 (DDR3 normal read/write operations); EX1003, ¶¶63-66.

In context, the claim recites the memories being “***not accessed*** for any normal...operations” as a condition “to apply a...signal related to...training sequences,” but the provisional has no such disclosure. EX1003, ¶¶67-71. The provisional refers generally to “MB [(memory buffer)] training,” EX1008, 25, which a POSITA understood can include MB-DRAM and/or Host-MB training, each of which can be performed with or without “*normal memory read or write operations*”:

## Initialization Overview



EX1039, 2 (June 4, 2009); EX1008, 22 (referring on June 12, 2009, to the “recent” “L[R]-DIMM” proposal, which included the above and resulted in EX1015); EX1003, ¶68. Thus, the provisional’s mentioning of “MB training,” by itself, does not exclude “*normal*” read/write operations. EX1003, ¶¶69-70; EX1015, pp.8-9 (“No DRAM commands”; “Read Enable Training”; “normal reads...*or* by using the...MPR”); EX1030, [0044] (training with normal “writes” and “reads”); EX1056, pp.42-45 (write leveling without normal writes), 48-54 (MPR for read training without normal reads).

### 2. Unsupported negative limitation (claims 7 and 16)

Claims 7 and 16 require “*training...performed when the dynamic random access memory elements are not communicating data signals associated with any*

*normal memory read or write operations with the memory controller via the second edge connections,”* which is not supported by the provisional. EX1001, 16:4-:9, 17:14-:19; EX1003, ¶¶72-73. As discussed above (pp.8-11), the provisional is silent on these limitations, and it was known that “normal” read/write operations could be performed as part of training, e.g., for DQ/DQS margining when the host communicates data signals through a DIMM’s edge connections. EX1003, ¶¶72-73; EX1015, 9.

**3. Unsupported negative limitation (claims 8 and 17)**

Claims 8 and 17 require that “*the second edge connections are not active during the operations associated with the one or more training sequences.*” EX1001, 16:10-12, 17:20-22. As discussed above (pp.8-12), the provisional is silent on these limitations, and it was known that edge connections could be active during training. EX1003, ¶¶74-75.

**4. Unsupported limitation (claims 1, 10, 19)**

Each independent claim also requires “*a second signal related to **one or more training sequences***” or “*operations associated with **one or more training sequences.***” EX1001, 15:42-:49, 16:54-:60, 18:12-:19, 18:36-:38. The provisional fails to disclose these limitations. EX1003, ¶¶76-79. The provisional simply teaches that the Error-Out pin is “Low during MB training (high signal indicates that training is done),” EX1008, 25, which does not disclose “*one or more training*

*sequences.*” EX1003, ¶¶76-77. The provisional also refers to “initialization operation sequences,” EX1008, 22, but that is just a generic reference to initialization, *see, e.g.*, EX1056, pp.19-20, not “*one or more training sequences.*” EX1003, ¶¶78-79.

**C. Person of Ordinary Skill in the Art (“POSITA”)**

A POSITA in 2009-10 would have had a Bachelor’s degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems. She would have been familiar with computer memory systems and basic CPU architecture documented in the literature, including standards, and generally available in commercial systems, including how computer components access a computer’s memory, the role of a memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory devices to the other components of the computer system. EX1003, ¶55; EX1102, 11-12; EX1103, 11-12; EX1034, 8-9.

**D. Background Technology**

**1. JEDEC standards**

The ’024 Patent expressly refers to “industry standard[s] promulgated by...JEDEC.” EX1001, 1:54-:56, 8:46-:54. A POSITA would have been familiar with the JEDEC standards, including those for the initialization and operation of memory devices and modules. EX1024, pp.8-12 (DDR initialization, mode register); EX1029, pp.9-17 (similar, LPDDR); EX1084, pp.9-20 (similar, DDR2);

EX1056, pp.19-32 (similar, DDR3), 42-45 (write leveling), 48-54 (MPR for read training); EX1025, pp.5, 15-54 (FBDIMM initialization, training, testing, polling), 114 (“interrupt” indicating “Hot Add” completion); EX1026, pp.23-25 (AMB calibrating DDR bus, polled for completion, “supports memory self test”); EX1003, ¶¶37-41.

In 2009, JEDEC was developing a standard for DDR3 “Load Reduced DIMM”s (LRDIMMs), as the provisional admits, EX1008, 22. *See, e.g.*, EX1015; EX1036; EX1039. A POSITA would have been familiar with that development and the content of the various JEDEC proposals, including those related to initialization. EX1003, ¶41; EX1078, pp.25-26 (Netlist’s expert agreeing); EX1105, ¶¶32-33; EX1106, ¶¶40-41.

## **2. Shared pins**

A POSITA would have understood, e.g., from textbooks, that memory devices and memory modules had a limited number of pins due to their manufacturing cost, making it obvious and common to share pins for different functions. EX1003, ¶¶42-45; EX1070, pp.322 (“desire to limit I/O pins”), 351 (“[p]in cost is becoming a major concern”). For example, JEDEC standards shared address pins (e.g., A0 to A15) for different functionalities, including “OP Code,” “Precharge” (A10), Burst Length (A12), “Row Address (RA),” and Column Address (“CA”):

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[BA=Bank Address, RA=Row Address, CA=Column Address, BC#=Burst Chop, X=Don't Care, V=Valid]

**Table 6 — Command Truth Table**

| Function                                     | Abbrevia<br>tion | CKE               |                  | CS# | RAS# | CAS# | WE# | BA0-<br>BA2 | A13-<br>A15      | A12-<br>BC# | A10-<br>AP | A0-<br>A9, A11 | Notes        |
|----------------------------------------------|------------------|-------------------|------------------|-----|------|------|-----|-------------|------------------|-------------|------------|----------------|--------------|
|                                              |                  | Previous<br>Cycle | Current<br>Cycle |     |      |      |     |             |                  |             |            |                |              |
| Mode Register Set                            | MRS              | H                 | H                | L   | L    | L    | L   | BA          | OP Code          |             |            |                |              |
| Refresh                                      | REF              | H                 | H                | L   | L    | L    | H   | V           | V                | V           | V          | V              |              |
| Self Refresh Entry                           | SRE              | H                 | L                | L   | L    | L    | H   | V           | V                | V           | V          | V              | 7,9,12       |
| Self Refresh Exit                            | SRX              | L                 | H                | H   | X    | X    | X   | X           | X                | X           | X          | X              | 7,8,9,<br>12 |
|                                              |                  |                   |                  | L   | H    | H    | H   | V           | V                | V           | V          | V              |              |
| Single Bank Precharge                        | PRE              | H                 | H                | L   | L    | H    | L   | BA          | V                | V           | L          | V              |              |
| Precharge all Banks                          | PREA             | H                 | H                | L   | L    | H    | L   | V           | V                | V           | H          | V              |              |
| Bank Activate                                | ACT              | H                 | H                | L   | L    | H    | H   | BA          | Row Address (RA) |             |            |                |              |
| Write (Fixed BL8 or BC4)                     | WR               | H                 | H                | L   | H    | L    | L   | BA          | RFU              | V           | L          | CA             |              |
| Write (BC4, on the Fly)                      | WRS4             | H                 | H                | L   | H    | L    | L   | BA          | RFU              | L           | L          | CA             |              |
| Write (BL8, on the Fly)                      | WRS8             | H                 | H                | L   | H    | L    | L   | BA          | RFU              | H           | L          | CA             |              |
| Write with Auto Precharge (Fixed BL8 or BC4) | WRA              | H                 | H                | L   | H    | L    | L   | BA          | RFU              | V           | H          | CA             |              |
| Write with Auto Precharge (BC4, on the Fly)  | WRAS4            | H                 | H                | L   | H    | L    | L   | BA          | RFU              | L           | H          | CA             |              |
| Write with Auto Precharge (BL8, on the Fly)  | WRAS8            | H                 | H                | L   | H    | L    | L   | BA          | RFU              | H           | H          | CA             |              |

EX1056, p.33; *see also* EX1084, pp.46-47; EX1024, pp.3, 7-8, 13 (similar).

Similarly, new functions were regularly added to memories by sharing existing pins. *See, e.g.*, EX1056, pp.13-14 (data mask (DM) pin used as DM or TDQS); EX1084, p.6; EX1026, pp.18-19 (similar).

A POSITA also understood that a pin for reporting (CMD/ADDR) parity error could also be used to report other functions, e.g., (DATA) CRC error:

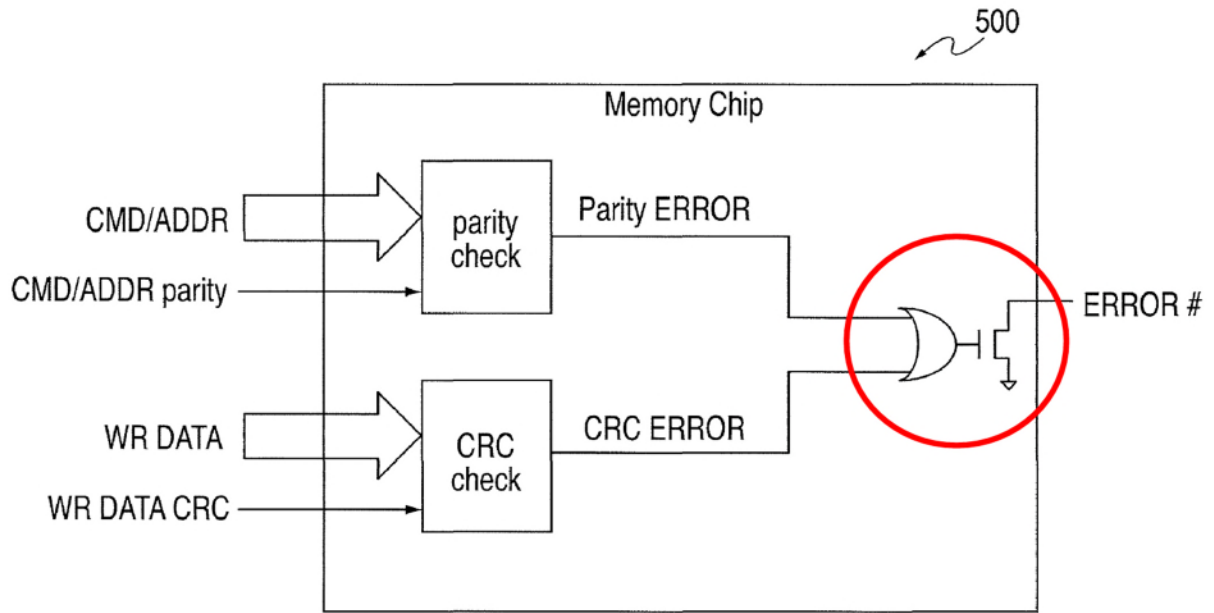


FIG. 5

EX1017, Fig.5 (above), 5:49-:55, 6:13-:18 (“other functions also share the error feedback pin”); EX1003, ¶44.

Furthermore, a POSITA understood how to use logic circuits (*e.g.*, OR) to couple the different functionalities to the shared pin. *Id.* (Fig.5 above); EX1023, ¶[0018], Fig.2 (below); EX1003, ¶45.

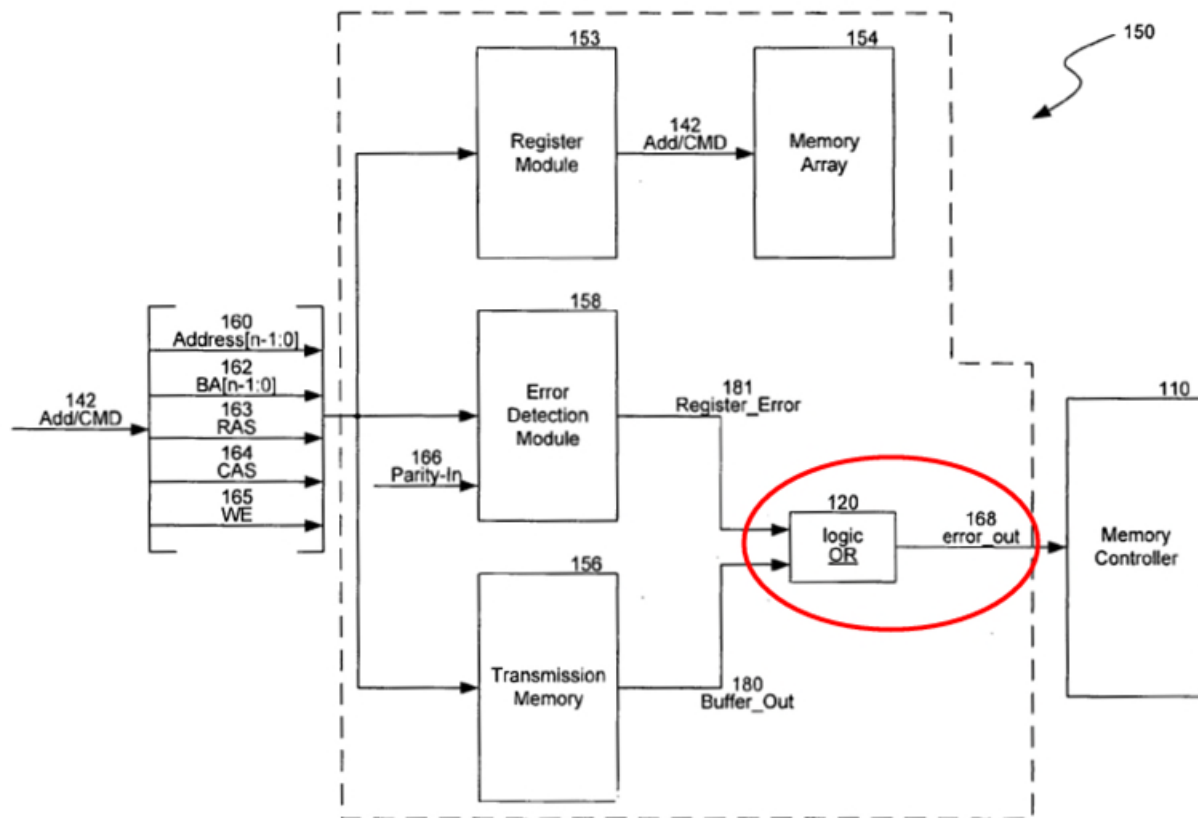


**FIG. 2**

Thus, a POSITA would have been motivated to use existing pins, like error\_out above, to implement new reporting functionalities. EX1003, ¶¶42-45.

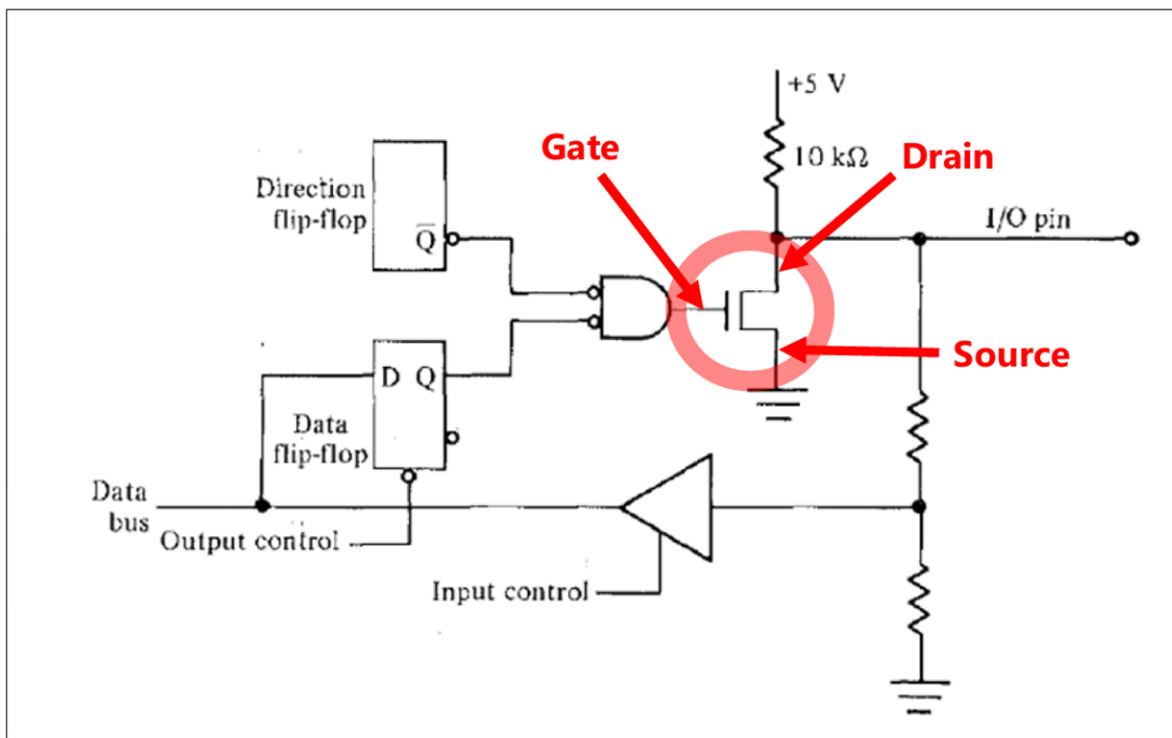
### 3. Open-drain output

An “open-drain output” was a well-known technique for implementing a wired “OR” functionality: “Q. In your opinion would a [POSITA] have known that an open drain output...would result in a wired-or function?...THE

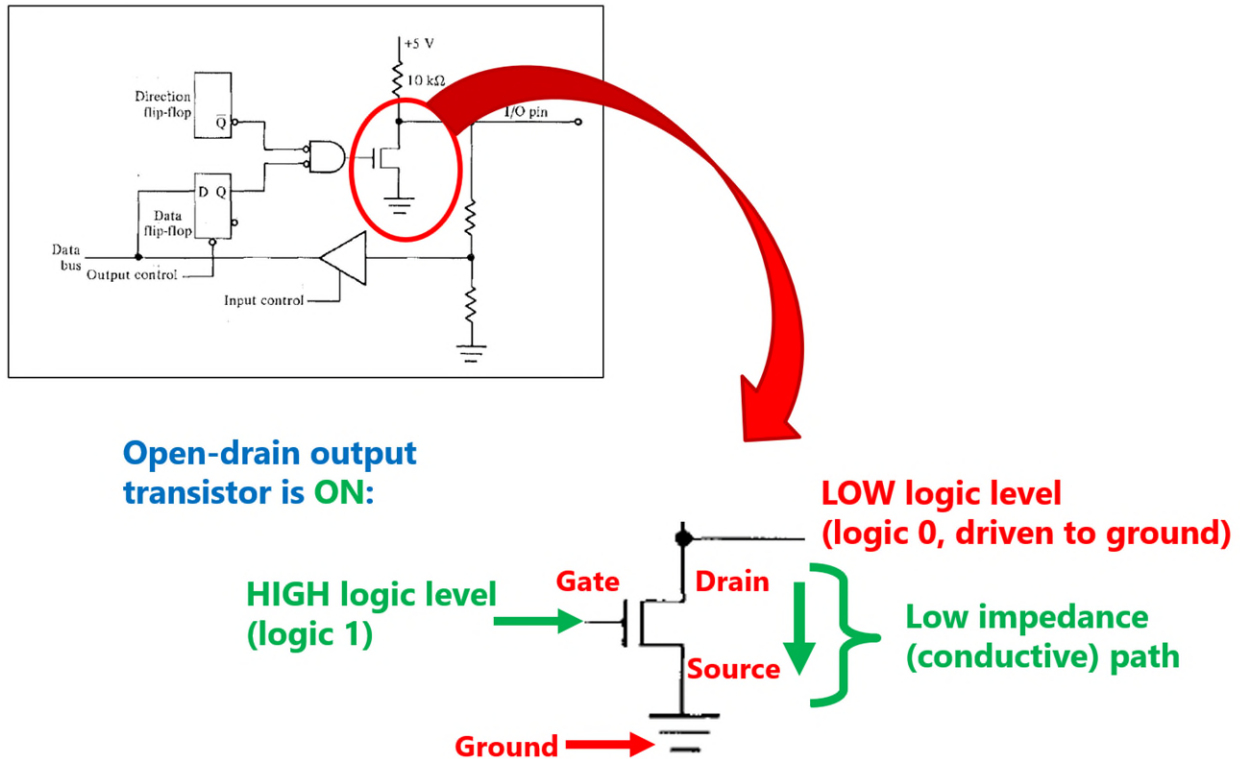
WITNESS: Yes.....It’s probably 40 years old.” EX1077, pp.178:21-179:4;

EX1089, pp.207-09; EX1088, pp.50-51; EX1003, ¶¶46-54.

As illustrated below, an “open-drain output” (e.g., I/O pin) is connected to the drain of a field-effect transistor (FET, in red circle) whose source is connected to ground. EX1003, ¶¶46-47; EX1089, pp.207-208 (Fig. 6.2, below); EX1088, pp.50-51. This concept of an “open-drain output” (called “open-collector output” when a bipolar transistor is used instead of a FET) was taught in textbooks for decades. *Id.*

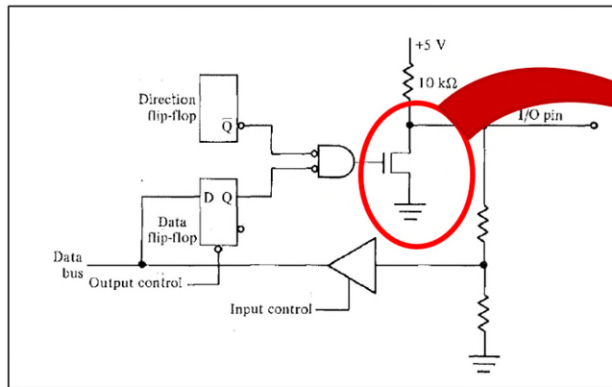


The transistor is “on” when its gate receives a “high” voltage (logic 1), driving the output (I/O) pin towards ground via a low impedance (conductive) path, thus outputting a low logic level:

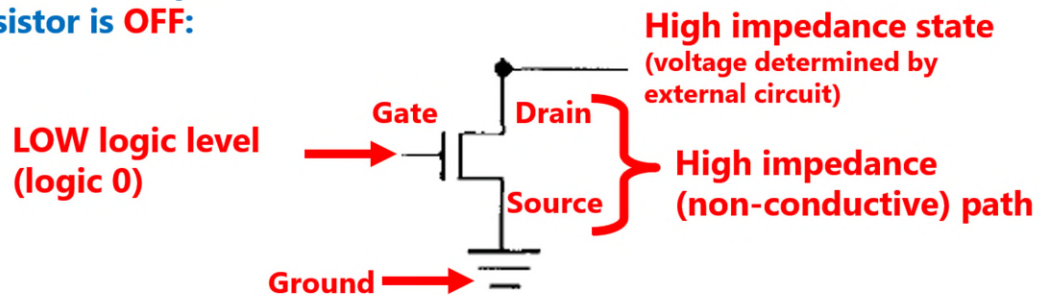


EX1003, ¶48; EX1089, pp.207-08; EX1088, p.50.

The transistor is “off” when its gate receives a “low” voltage (logic zero), causing the transistor to become open (i.e., non-conductive), and the I/O pin and the path to ground to be in a high impedance state:



**Open-drain output  
transistor is OFF:**



EX1003, ¶49; EX1089, pp.207-208, EX1088, p.50. In this high impedance state, the voltage at the output is determined by other circuitry connected to the same output, such as a pull-up resistor (above: 10 kΩ, pulling to 5V) or other open-drain transistors potentially pulling to ground, thus creating the wired “OR” functionality. *Id.*; EX1077, pp.178:21-179:4.

Open-drain outputs were commonly used by multiple devices, such as memory modules, to send status (e.g., error) reports to the memory controller:

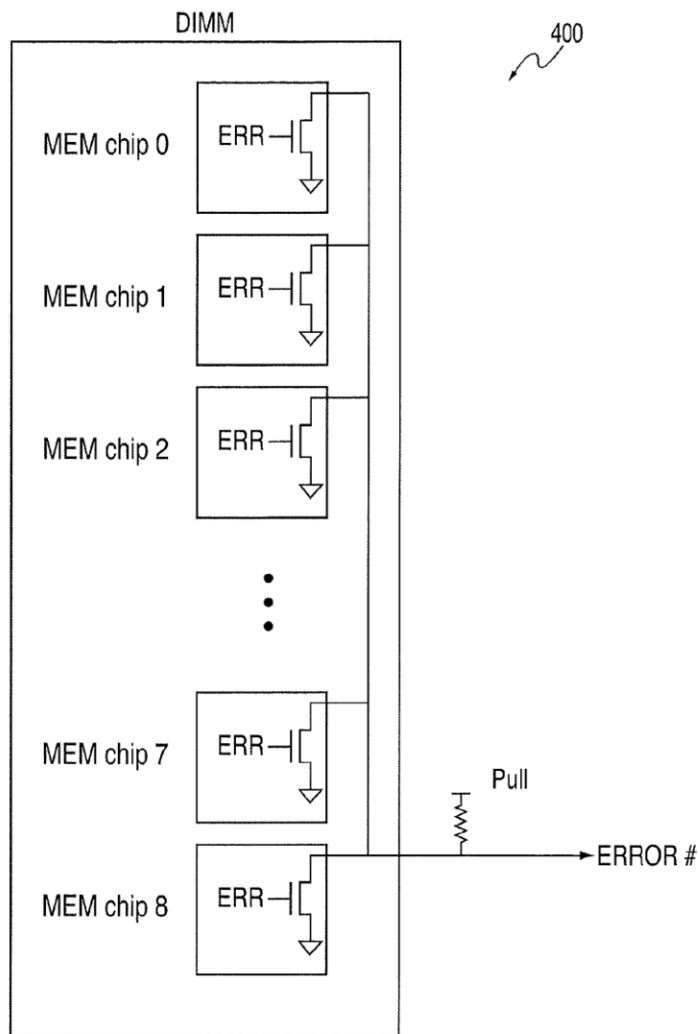


FIG. 4

EX1017, Fig.4 (above), 4:40-:48 (“single pin...via an open drain...across memory devices...to report...errors”), 6:1-:16 (similar); EX1014, ¶¶[0072] (“open-drain outputs...to permit multiple modules...for reporting an error”), [0109] (similar); EX1003, ¶50.

In Kim’s Figure 4 (above), when *any* of the transistors is “on,” thus creating a low impedance path to ground, the common output (ERROR#) would have a low

voltage (logic 0) regardless of the states of the other transistors. EX1003, ¶¶51-52. Only when *all* of the transistors are “off” (high impedance state) would the common output (ERROR#) be pulled up to a high logic level through the “Pull” resistor. *Id.*; EX1014, ¶[0099]. This wired “OR” functionality of an open-drain output was known for decades. EX1077, pp.178:21-179:4; EX1003, ¶52.

Open-drain and open-collector outputs, with their “OR” functionality, were commonly used for interrupt requests and to report completion of (or being ready for) an operation, thus avoiding the need to interrogate a device to determine its status. EX1089, pp.15-16, 208, 218-20 (NOT-READY-FOR-DATA open-collector line “rises only when all slaves are ready”), 281 (“open-collector...status signals from multiple drives”); EX1003, ¶¶53-54.

## **E. The ’024 Patent**

### **1. Overview of the ’024 Patent**

The ’024 Patent describes “establishing a handshake mechanism” “by adding a new interface (notifying) signal .... [which] can be an open drain signaling from the memory [module] controller to the MCH [system memory controller].” EX1001, 4:48-:59; EX1003, ¶56. According to the ’024 Patent, “there [was] no existing method of handshaking between the MCH...and a ... memory module...during initialization...[e.g.,] the system memory controller does not monitor the error-out signal from the memory [module],” and “typical” prior

art servers would instead simply wait a predetermined amount of time, assuming that initialization had completed. EX1001, 3:40-:62; EX1008, 22 (“waiting period”); EX1003, ¶57. The ’024 Patent suggests implementing “handshaking” between the memory controller and memory module by a “notifying method,” because the alternative polling method is “generally inefficient.” EX1001, 4:18-:41; EX1003, ¶58.

Figure 3 illustrates an exemplary memory module (10) with an open-drain output (12) whose transistor (36) is controlled by a multiplexor (42) driving the transistor’s gate with either (i) a task\_in\_progress signal (44) “when the memory module 10 is in the initialization mode or is executing the at least one initialization sequence,” or (ii) an error signal (46) to report parity errors during operational mode. EX1001, Fig.3 (below), 11:57-12:9; EX1003, ¶59.

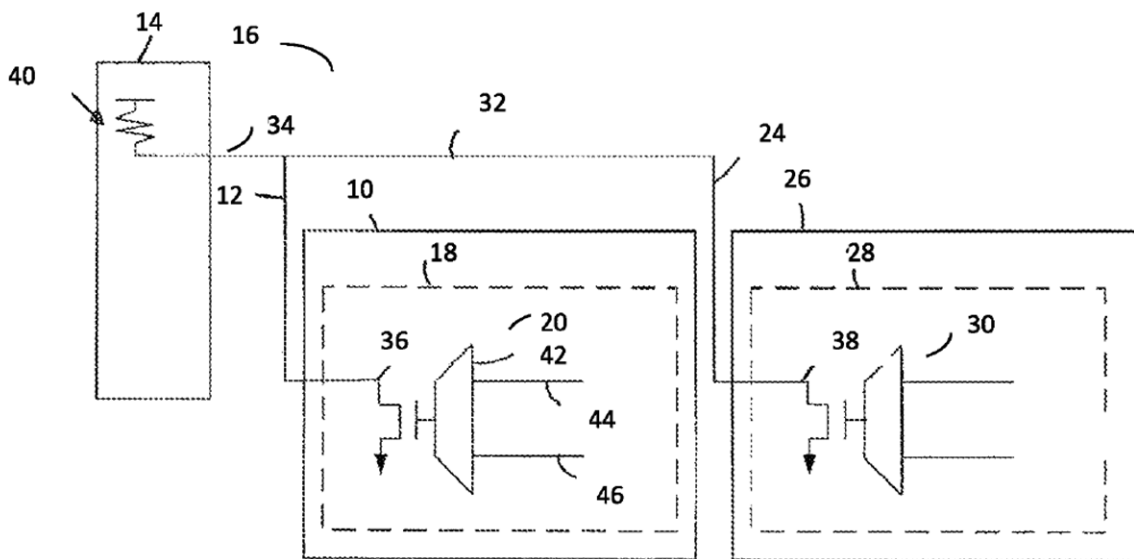


Figure 3

## 2. **Prosecution History**

The '024 Patent claims priority back to U.S. Provisional Application No. 61/186,799 (filed June 12, 2009) (EX1008). EX1002, 45; EX1003, ¶¶80-155. As discussed above (pp.5-7), the Board has invalidated numerous claims in the same family as the '024 Patent in light of Grounds 2 and 5, including:

- '595 Patent, Claims 1-24 (EX1103, pp.84-85);
- '218 Patent, Claims 1-22 (EX1102, pp.77-78); and
- U.S. Patent No. 9,424,623 (“'623 Patent”) (EX1031),<sup>2</sup> Claims 1-29 (EX1034, p.22).

EX1003, ¶¶95-155. Further, in its Institution Decisions for the '218 and '595 Patents, the Board found a sufficient showing that JEDEC (part of Grounds 1 and 4) was prior art. EX1059, 21-27; EX1062, 21-31; EX1108, 18-25, 29-32; EX1109, 16-24, 27-30.

The '024 Patent claims are substantially similar to those already invalidated by the Board, *see* EX1003, ¶¶152-155, as discussed below in more detail for each limitation of the '024 Patent claims (pp.55-107), and as evidenced by terminal disclaimers that were filed to overcome double patenting rejections, including:

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<sup>2</sup> The '623 Patent claimed priority to the '218 Patent. EX1031, Face (citing Application No. 15/088,115).

- '024 Patent, in view of the '595 and '218 Patents (EX1002, pp.122-23, 149-50; EX1003, ¶¶137-151); and
- '595 Patent, in view of, e.g., the '218 Patent (EX1096, pp.82-83, 106-07; EX1003, ¶¶120-136).

## **V. CLAIM CONSTRUCTION**

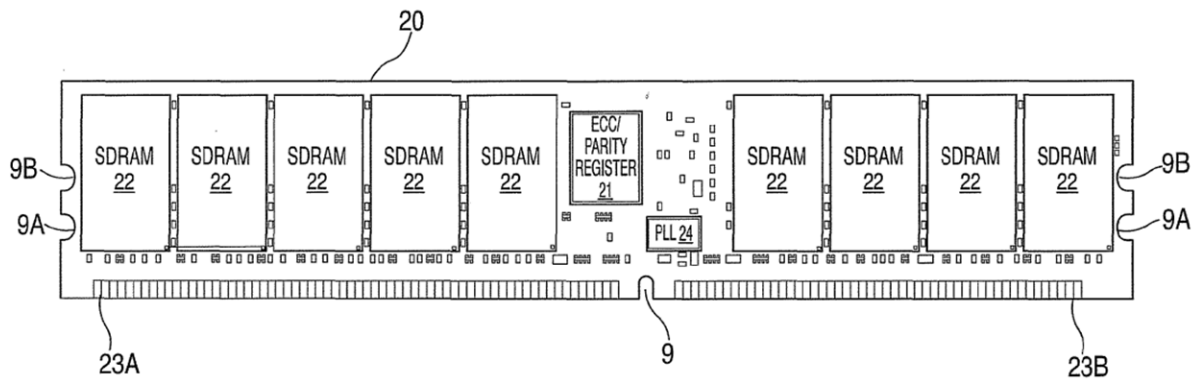
No claim construction is needed because the claims are obvious under any reasonable interpretation. EX1003, ¶¶156-159. For example, in the previous IPRs against the 218 and 595 Patents, the Board did not adopt any express claim constructions “and instead g[a]ve the claim terms their plain and ordinary meanings.” EX1102, 12-15; EX1103, 12-15; EX1061, 2-3.

## **VI. OVERVIEW OF THE PRIOR ART**

### **A. Hazelzet (EX1014)**

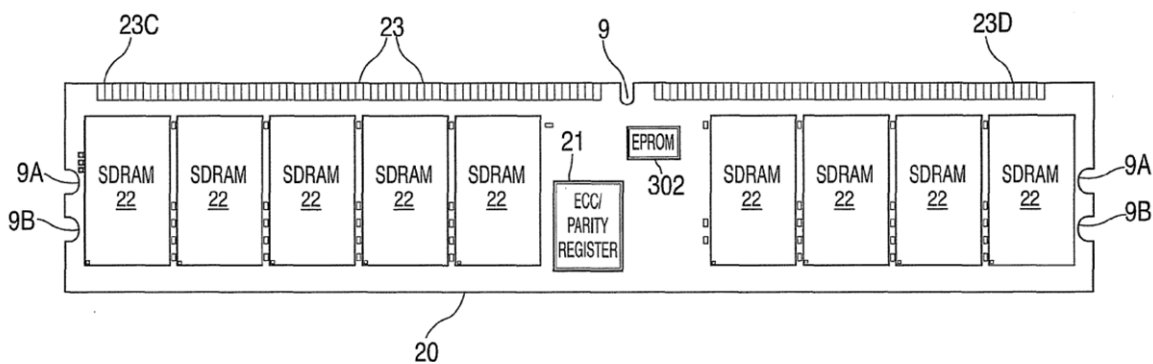
U.S. Patent Publication No. 2008/0098277 to Hazelzet (“Hazelzet”) (EX1014) was filed on October 23, 2006, and published on April 24, 2008. Hazelzet is prior art under pre-AIA 35 U.S.C. §§102(a), (b), and (e).

Hazelzet discloses memory modules, each including up to four ranks of (stacked) memory devices which can be initialized in a number of ways. EX1014, ¶¶[0008], [0014], [0016], [0039-40], [0044], [0123-25], Figs. 3A-3D (Figs. 3C-3D below); EX1003, ¶162.



FRONT SIDE OF DIMM - 4 HIGH STACK

FIG. 3C



BACK SIDE OF DIMM - 4 HIGH STACK

FIG. 3D

Hazelzet's module can operate in an "ECC mode" or a "parity mode." EX1014,

¶¶[0064], [0069-70], Fig. 8 (below); EX1003, ¶¶163, 166.



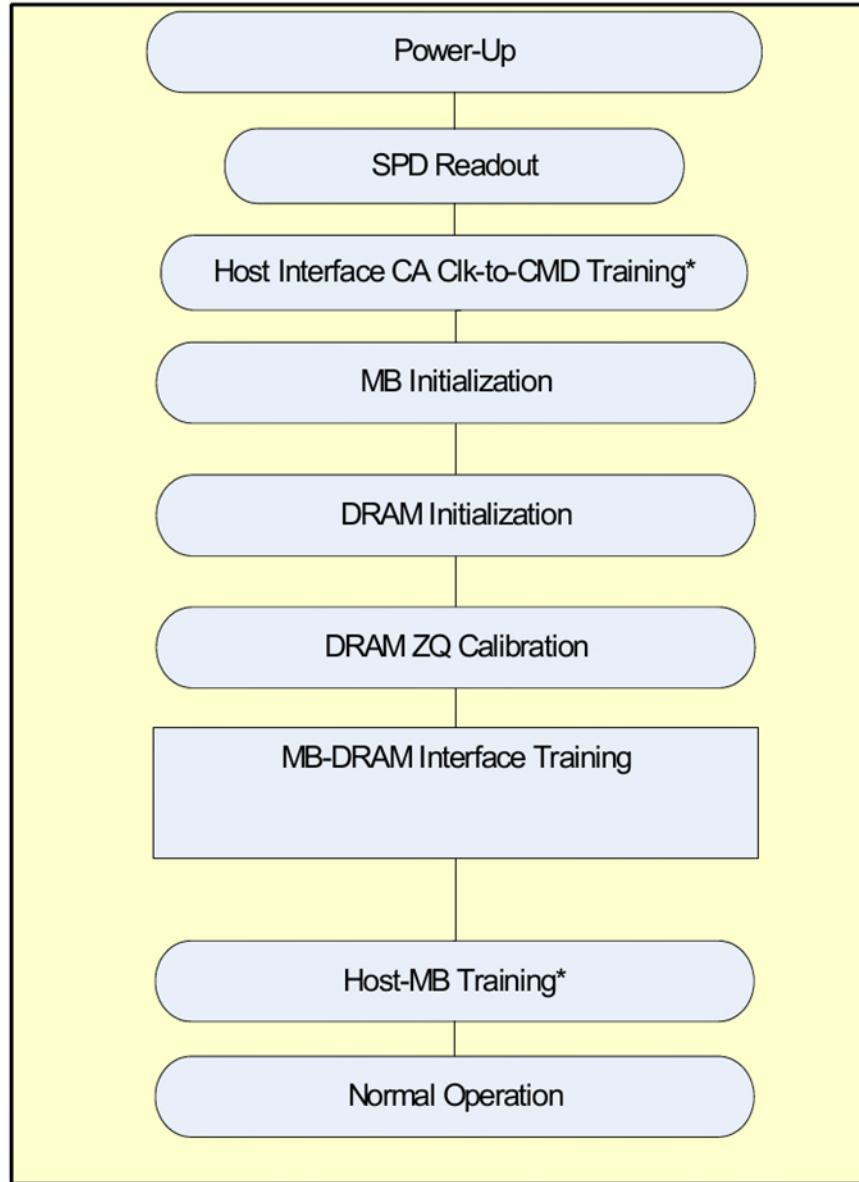
FIG. 8

In ECC mode, the module detects “correctable” and “uncorrectable” errors and reports them to the host through respective “/Error (CE)” and “/Error (UE)” open-drain outputs. EX1014, ¶¶[0069], [0072], [0109]; EX1003, ¶¶163-164. In parity mode, the module reports a parity “error condition” to the host “via the Uncorrectable Error (UE) line,” the same UE output also used in ECC mode. EX1014, ¶¶[0064], [0070], [0072], [0109]; EX1003, ¶¶165-166.

**B. JEDEC (EX1015)**

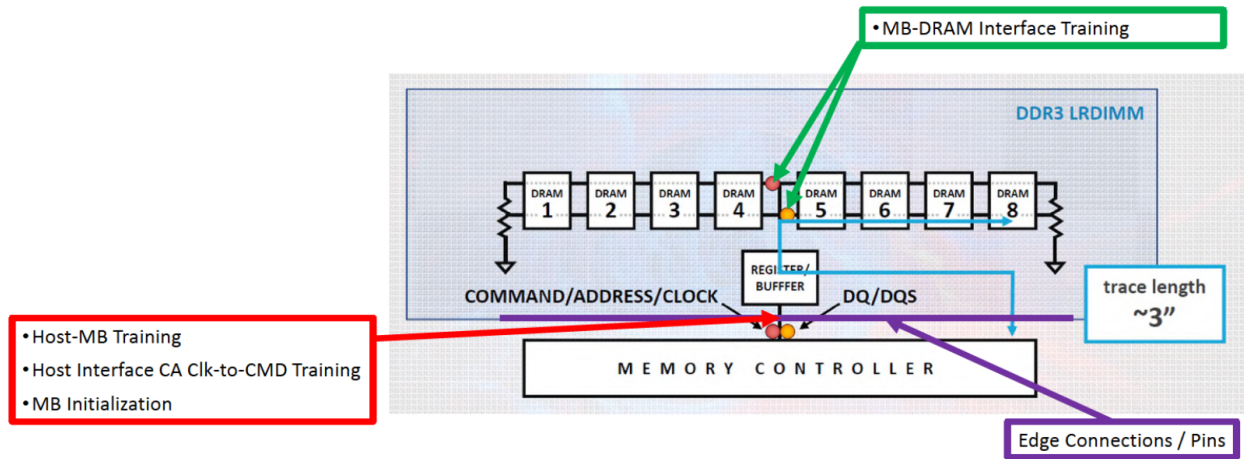
JEDEC (EX1015) is a proposal to JEDEC. It is prior art as discussed below (pp.36-43) and was known to a POSITA as admitted by the provisional, EX1008, 22 (“recent proposal in JEDEC”), and Netlist’s expert, EX1077, 55:8-57:25 (“[POSITAs] would understand about the content...in the JEDEC proposals”). JEDEC concerns the Memory Buffer (“MB” or “module controller”) on a DDR3 LRDIMM memory module, including an initialization mode with training sequences and corresponding handshaking methods to report their status. EX1015, 1, 3, 8; EX1003, ¶¶167-171. This training includes Host-MB Training and MB-DRAM Training using sequences such as Write Leveling, Read Enable Training, and Read/Write DQ/DQS training. EX1015, 3-4, Fig.1 (below).

**Figure 1 — Initialization Overview**



\* This step is optional for the MB but may be done by some platforms

The following demonstrative illustrates the components involved in the different types of training:



EX1081 (annotating EX1079, 10); EX1077, 131:4-133:3; EX1003, ¶169. JEDEC teaches that “No DRAM commands or control word writes...can be issued to the MB until the MB-DRAM Interface training is complete” and “training completion can be signaled by the assertion of ERRROUT#,” which is an open-drain output also used for reporting parity errors during normal operation. EX1015, 3, 8; EX1036, 2, 5-10 (p.9 below); EX1044, 1 (“open drain output ERRROUT”); EX1003, ¶¶169-171.

|          |                        |                                                                                                                                                                       |
|----------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ErrOut_n | OUT<br>(open<br>drain) | Parity error detected on the Address and Command bus. A resistor may be connected from ErrOut_n bus line to V <sub>DD</sub> on the system planar to act as a pull up. |
|----------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|

### C. **Buchmann** (EX1016)

U.S. Patent No. 8,139,430 to Buchmann (“Buchmann”) was filed on July 1, 2008, and is prior art under pre-AIA §102(e).

Buchmann is directed to power-on initialization and testing of memory modules, each including a memory buffer (MB 106) for buffering data, address,

and command signals. EX1016, 4:5-:50, Fig.1 (below), Fig.2; EX1003, ¶¶173-179.

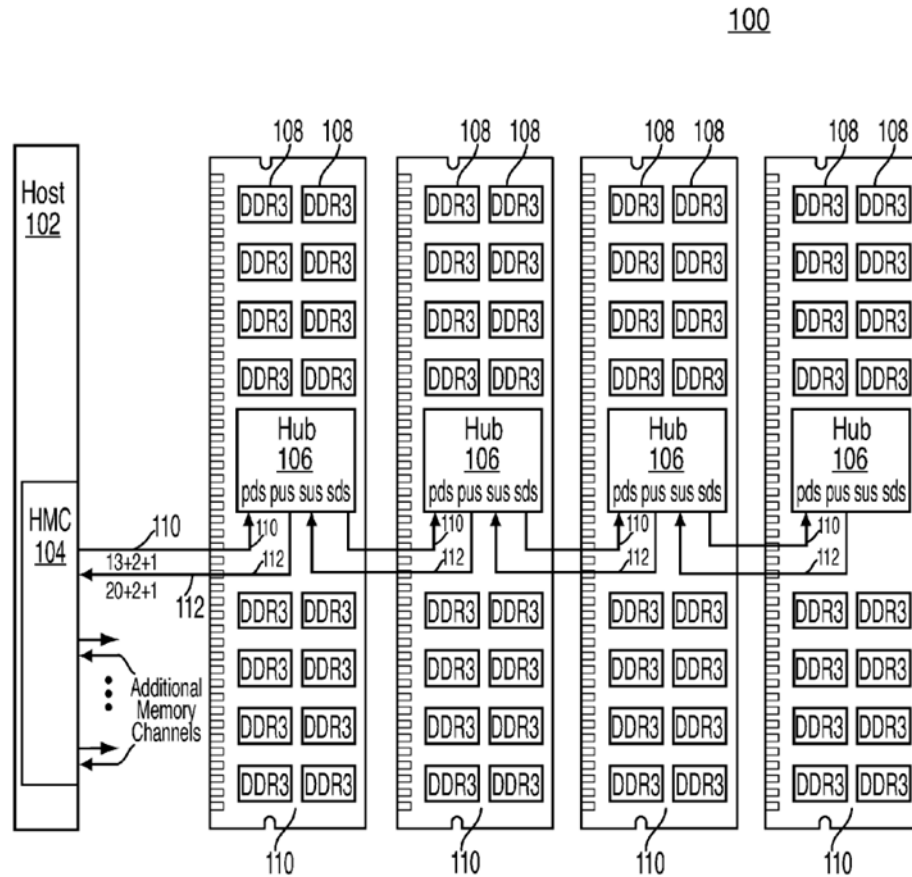


FIG. 1

Buchmann discloses “SBC” and “high-speed” modes of operation, EX1016, Abstract, 1:39-:44, 14:65-15:2, and executing training sequences in the SBC mode so that the modules can be reliably used in the high-speed mode, EX1016, 4:51-12:59; EX1003, ¶¶174-175.

For example, during training sequences TS0 (“clock detection and repair”) and TS3 (“upstream data lane training”), Buchmann’s memory module generates

various notification signals, including “TS\_done,” notifying the host that TS0/TS3 training is “done.” EX1016, Figs.4, 6, 5:51-7:2, 8:24-9:18; EX1003, ¶¶176-177.

Buchmann’s training operations may be initiated by power on, reset, or initial program load, and do not use memory read/write operations during TS0 and TS3. EX1016, 3:67-4:4, 4:51-5:12, Fig.3; EX1003, ¶178.

Buchmann discloses a daisy-chain arrangement of the modules, as well as other types of “bus structures.” EX1016, 3:49-:52, 14:41-:43, 16:47-:50, 28:23-:31; EX1003, ¶179.

**D. Wang (EX1090)**

U.S. Patent No. 8,386,722 to Wang (“Wang”) (EX1090) was filed on June 23, 2008, EX1110, and is prior art under pre-AIA §102(e).

Wang teaches interface circuits (e.g., 550) coupled between memory devices 542 and the system’s memory controller 524 to overcome “command scheduling constraints,” EX1090, 1:19-:40, 2:16-:18, Figs.5B, 5E (below); EX1003, ¶181, and to eliminate “idle bus cycles,” EX1090, 2:40-:45, 6:18-:60, Figs.3A-3C, 8:15-:62, Figs.4A-4B; EX1003, ¶182.

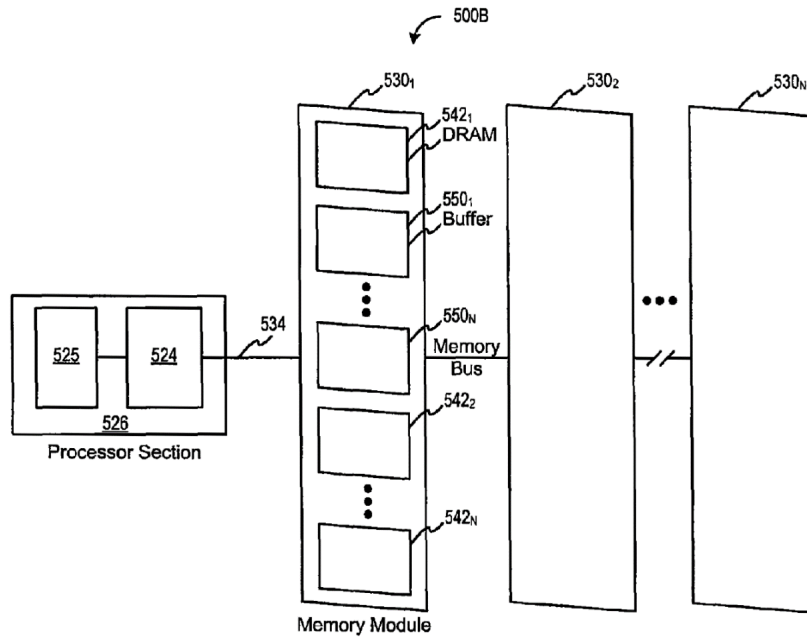


FIG. 5B

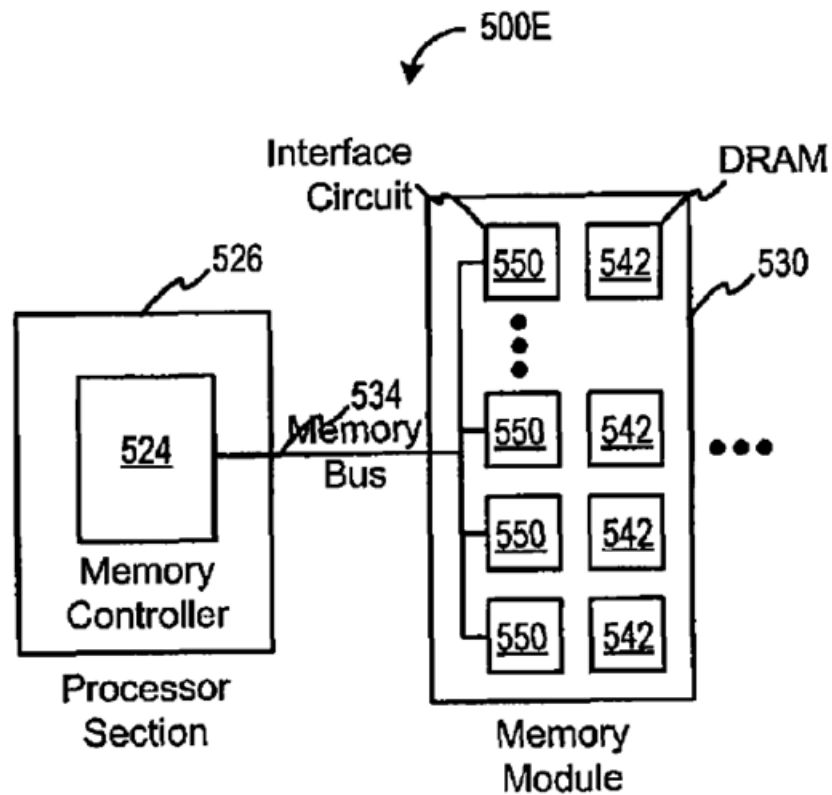


FIG. 5E

Wang also teaches that its interface circuit can be trained to provide higher memory performance. EX1090, 3:17-:22, Fig.4C (below); EX1003, ¶183.

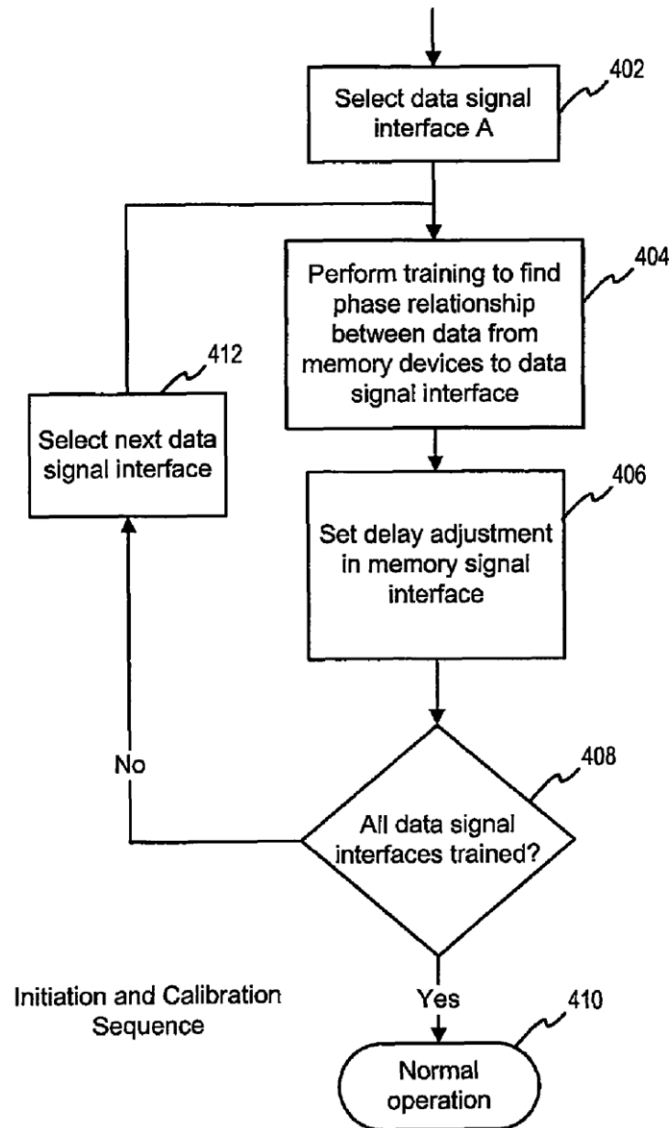


**FIG. 4C**

**E. Kim (EX1017)**

U.S. Patent No. 8,359,521 to Kim ("Kim") (EX1017) was filed on January 22, 2008, and is prior art under pre-AIA §102(e).

Kim describes a “memory device having a shared error feedback pin.”

EX1017, Abstract, Fig.5 (below, showing shared ERROR# pin to report Parity or CRC errors); EX1003, ¶185.

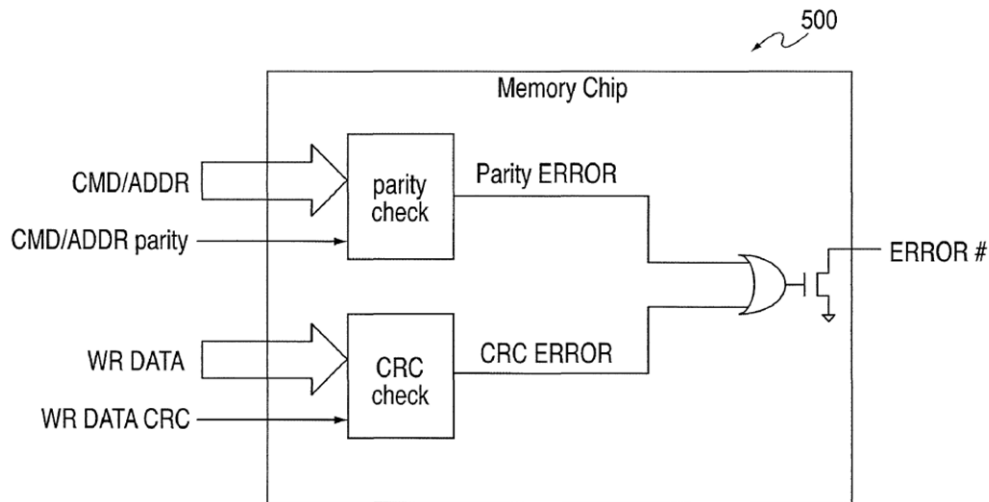


FIG. 5

Kim teaches that multiple functionalities sharing an error pin “maximizes use of available bandwidth, simplifies the memory controller,” EX1017, 4:40-:49, “mak[es] use of unused circuits within the subsystem,” *id.* 11:31-:34, and enables compatibility with standard memory modules, *id.* 5:49-:57. Kim also discloses that a memory module can report status and initialization-completion information, *id.* 12:18-:26, and the shared error pin can be implemented using an open-drain configuration and/or an OR-gate. EX1017, 5:49-:57; *see also id.* 4:40-:48; 6:1-16; Figs.4-5; EX1003, ¶185.

## VII. ARGUMENT

### A. **JEDEC (EX1015) in Ground 1 is a “printed publication” and admitted prior art**

JEDEC (EX1015) is a proposal to the JEDEC standard setting organization which was publicly accessible by November 11, 2009, and at least before June 13, 2010. *See* EX1055<sup>3</sup> & EX1093, 27:20-37:8, 42:16-44:6; EX1050<sup>4</sup> & EX1092, 11:20-34:6; EX1054 & EX1091, 13:4-14:11, 15:14-:22, 32:7-56:20, 59:10-60:15 (discussing Exhibits 1071-75);<sup>5</sup> EX1077, 10:1-:6, 33:13-:24, 50:25-52:7, 53:22-

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<sup>3</sup> Discussing EX1051 (Ex.A), EX1015 (Ex.B), EX1037 (Ex.C), EX1052 (Ex.D), EX1036 (Ex.E), and EX1053 (Ex.F).

<sup>4</sup> Discussing EX1015 (Ex.A), EX1051 (Ex.B), EX1037 (Ex.C), EX1036 (Ex.D), EX1052 (Ex.E), EX1053 (Ex.F), EX1039 (Ex.G), EX1046 (Ex.H), EX1049 (Ex.I), and EX1048 (Ex.J).

<sup>5</sup> Exhibits 1071-75 are JEDEC webpages from April and May 2009, authenticated by the Internet Archive, *see* EX1076; *Valve Corp. v. Ironburg Inventions Ltd.*, 8 F.4th 1364, 1374-76 (Fed. Cir. 2021) (relying on the Internet Archive to reverse the Board), and by John Halbert, who was personally active in JEDEC during that timeframe, *see* EX1091, 13:4-14:11, 15:14-:22, 32:11-:20.

57:25, 62:1-:18. It is therefore a “printed publication” under pre-AIA §102(a), as recognized by previous Institution Decisions. EX1108, 28-32; EX1109, 26-30.

JEDEC (EX1015) and the related PowerPoint (EX1039) are also admitted prior art, EX1008, 22 (“recent proposal in JEDEC”), and thus “permissible evidence in an [IPR] for establishing the background knowledge possessed by a [POSITA],” *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1375-76 (Fed. Cir. 2022).

The facts here are similar to *M&K* and *Weber*. In *M&K* (after a remand to the Board in *Infobridge*),<sup>6</sup> the Federal Circuit affirmed the Board’s decision that a “working draft” (WD4) of a standard within a standard setting organization (like JEDEC here) was a “printed publication” because of the “prominence and public awareness of the [standard setting organization], showing that interested members

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<sup>6</sup> In *Infobridge*, the Federal Circuit disagreed with the Board’s analysis of the public accessibility of proposals to a standard setting organization, and remanded: “[T]he Board should have considered whether...an ordinarily skilled artisan could have accessed the WD4 reference, after exercising reasonable diligence, based on the listserv email. This might include examining whether a person of ordinary skill, exercising reasonable diligence, would have joined the listserv.” *Samsung Elecs. Co. v. Infobridge Pte. Ltd.*, 929 F.3d 1363, 1374-75 (Fed. Cir. 2019).

of the public exercising reasonable diligence reasonably should have been able to obtain [the draft] documents ‘if they wanted to.’” *Samsung Electronics Co. v. M&K Holdings Inc.*, IPR2018-00696, Paper 48, at 37 (PTAB Sept. 4, 2019) (quoting *GoPro, Inc. v. Contour IP Holding LLC*, 908 F.3d 690, 694 (Fed. Cir. 2018)), *aff’d in relevant part*, 985 F.3d 1376, 1379-83 (Fed. Cir. 2021).

In *Weber*, the Federal Circuit held that a “copyright notice” (similar to that for JEDEC’s documents, and similar to the limitations on any copyrighted publication such as the N.Y. Times<sup>7</sup>) is **not** a “confidentiality restriction[.]” *Weber, Inc. v. Provisur Techs., Inc.*, 92 F.4th 1059, 1062, 1068-69 (Fed. Cir. 2024) (reversing “Board’s printed publication determinations” because the copyrighted “manuals were accessible to interested members of the relevant public by reasonable diligence”). Moreover, the Federal Circuit held that the “high cost” of obtaining the copyrighted documents (analogous to the cost of joining JEDEC) did not negate the document’s public accessibility: “[c]ost alone cannot be dispositive because the printed-publication inquiry is focused on the interested public, not the general public. Here, the interested public includes commercial entities that can

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<sup>7</sup> See <<https://help.nytimes.com/hc/en-us/articles/115014792127-Copyright-notice>> (“All materials [on nytimes.com] are protected by...copyright law and may not be reproduced [or] **distributed**...without...permission”); EX1091, 50:8-51:18.

afford high-cost [materials].” *Weber*, 92 F.4th at 1068 n.6; *see also Centripetal Networks, Inc. v. Cisco Sys., Inc.*, 847 F. App’x 869, 878 (Fed. Cir. 2021) (“[p]ublic accessibility is not limited to circumstances of free or academic distributions”).

Here, JEDEC was highly prominent to the relevant public, and interested members of the public easily could have obtained EX1015 from JEDEC if they so desired, as discussed below in more detail.

**1. JEDEC’s prominence**

JEDEC was created over 50 years ago “to serve the public interest.” EX1050, ¶¶4, 15 & p.146. By 2009-2010, JEDEC was the only standard-setting organization for the industry, EX1091, 44:15-45:1; EX1050, ¶4; EX1073, so it was well known to POSITAs, as Netlist’s expert admitted in previous IPRs, EX1077, 33:13-:24, 50:25-52:7. Netlist’s expert also admitted that “the vast majority” of DRAM memory devices and modules sold in this time frame complied with the JEDEC standards. EX1107, 145:17-146:24, 283:18-286:15; *see also Rambus Inc. v. FTC*, 522 F.3d 456, 459-60 (D.C. Cir. 2008) (“90%”). JEDEC’s meetings were publicized on the Internet and took place at hotels where anyone could walk in and observe the presentations. EX1071; EX1091, 33:5-37:17, 59:10-60:15. Nothing about JEDEC, its meetings, or its documents was confidential. EX1054, ¶¶6, 11; EX1091, 13:4-14:11, 32:11-:20, 55:10-56:20; *Rambus Inc. v. Infineon Techs. Ag*,

31 F.3d 1081, 1102 n.9 (Fed. Cir. 2003) (noting that “there are no confidentiality agreements between individual [JEDEC] members”).<sup>8</sup> Indeed, Netlist’s expert in related IPRs admitted to participating as a “guest” at JEDEC, despite not being “a voting member.” EX1107, 178:23-179:18; *Rambus*, 318 F.3d at 1085 (“JEDEC meetings are open meetings, but nonmembers must receive an invitation to attend.”).

In 2009-2010, virtually every company in the industry was a JEDEC member, including Samsung and Netlist. EX1074; EX1050, ¶4; EX1091, 45:19-47:19. Membership was available as a flat fee that gave everyone in a company access to all documents and meetings for a given JEDEC committee. EX1073; EX1074; EX1075; EX1091, 43:9-47:19, 48:18-50:6; EX1092, 26:25-27:10; EX1050, ¶5. “Minutes of the JEDEC meetings...[we]re available to members and nonmembers alike.” *Rambus*, 318 F.3d at 1085. There is no evidence that JEDEC ever denied anyone membership. EX1091, 43:9-:20; EX1073.

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<sup>8</sup> According to the JEDEC Manual, the only thing that was “confidential” was “[s]urvey ballots,” see EX1048, 19; EX1049, 18; EX1050, ¶15; EX1092, 26:21-:24, **not** proposed standards, which were copyrighted but not confidential as discussed above (p.38 & n.7), see EX1048, 14-15; EX1049, 14-15.

## 2. Indexing/cataloging

JEDEC organized its committees (and their documents) by technical area, using a numbering convention—similar to the Dewey Decimal system—making them easy to find. EX1072, 59-62; EX1091, 39:21-43:7, 52:16-55:8. Here, the relevant committee was “JC-40,” which concerned the “CMOS Digital Logic” for memory modules, and JEDEC publicized information about JC-40 and its meetings on the Internet. *Id.*; EX1071, 2; EX1091, 37:19-38:25; EX1092, 31:24-33:3; EX1050, ¶5. Thus, a POSITA interested in that technical area could easily find the relevant JEDEC committee and its documents and meeting dates. *Id.*

Furthermore, JEDEC indexed its documents by keywords, *see* EX1015; EX1072, 63-113, and assigned each presentation a unique “item number” (such as 142.35) that was included in meeting agendas and minutes to make it easier to find later, *see* EX1039; EX1046, 21-22; EX1015; EX1091, 53:17-54:18. JEDEC also provided a search feature on its website to find documents. EX1091, 53:3-:16; EX1071 (“Search our Documents”). Finally, you could simply call the JEDEC office to help you find what you were looking for. EX1091, 54:20-55:8.

## 3. Dissemination

JEDEC (EX1015) was a proposed standard for LR-DIMM memory modules disseminated to JEDEC’s JC-40 committee members by November 11, 2009, so they could vote on whether to approve it at their December 2009 meeting at a

publicly accessible resort in Maui. EX1071, 2; EX1091, 34:25-37:17, 59:10-60:15; EX1055, ¶¶4-8 & Exs.A-C, pp.40-41; EX1093, 13:16-14:25, 27:20-31:11, 35:18-37:8, 42:16-44:6; EX1050, ¶¶6-9 & Exs.A-C, pp.43-44; EX1075 (“JEDEC...has E-mail distribution”); EX1092, 16:9-:23, 20:8-:12, 21:18-23:4. As admitted by Netlist’s expert in previous IPRs, EX1015 related to an earlier presentation (EX1039) made to JEDEC on June 4, 2009 (before Netlist’s June 12, 2009 Provisional application). EX1105, 18; EX1106, 23; EX1046, 1-2, 21-22 (#142.35). Thus, as was typical, EX1015’s contents were discussed within JEDEC for months before the formal vote in November/December 2009, including at weekly “task group” (TG) meetings where EX1015 was distributed and approved. EX1046, 1-2, 21-22 (#142.35); EX1091, 13:25-14:11, 26:4-27:13, 51:20-52:14; EX1093, 28:2-:13, 32:23-33:10, 35:11-:16.

Neither the June 2009 JEDEC presentation (EX1039) nor the November 2009 JEDEC proposal (EX1015) was confidential or is marked “confidential.” EX1054, ¶11; EX1091, 16:3-17:19, 19:1-:20, 20:16-22:14, 55:10-56:20. To the contrary, as admitted by Netlist’s expert in previous IPRs, their content would have been quickly disseminated by “word-of-mouth” throughout the entire industry such that a POSITA would have known the complete contents (regardless of whether a POSITA had their own copies). EX1077, 33:13-:24, 51:18-52:7, 53:22-57:25, 62:1-:18; EX1107, 39:9-:24 (“it’s not a secret process....people talk”). The

Federal Circuit has previously found “word of mouth” dissemination sufficient. *See M & K Holdings*, 985 F.3d at 1380-83. And as discussed above (pp.39-40), a POSITA could easily join JEDEC to get copies of any documents they did not already have. Indeed, the entire point of JEDEC was (and still is) so ***interested*** members of the public could review proposals like EX1015 and decide whether to make them a standard ***for the public***.

**B. Grounds 1-3**

Grounds 1-3 render obvious claims 1-20.

**1. Combinations for Grounds 1-3: Hazelzet (EX1014) and either JEDEC (EX1015), Buchmann (EX1016), or Wang (EX1090)**

***a) The Combinations Relied on Here***

The combinations analyzed here—Hazelzet/Buchmann, Hazelzet/JEDEC, and Hazelzet/Wang—are straightforward. In each, the functionality of buffering the data signals would be added to Hazelzet’s memory module, similar to that in JEDEC or in Wang, and corresponding training would be added, including training sequences and reporting their completion over an open-drain output (e.g., UE 121) of Hazelzet. EX1003, ¶¶187-192.

As discussed above (pp.5-7), Netlist is precluded from challenging the Hazelzet/Buchmann combination in Ground 2 that the Board has repeatedly relied on to invalidate similar claims. EX1034, 7-20; EX1102, 15-44; EX1103, 16-44. In the Hazelzet/Buchmann combination, the training sequences would be like those

in TS0 or TS3, with Hazelzet's UE open-drain output conveying respective TS0\_done or TS3\_done information. EX1016, Figs. 4 & 6, 5:51-7:2 & Tables 1-2, 8:24-9:18 & Tables 5-6. EX1003, ¶¶188, 191-192.

In the Hazelzet/JEDEC combination (Ground 1), the training sequences would be like those of MB-DRAM Training in the JEDEC proposal, with Hazelzet's open drain output signaling completion like ERROUT# in JEDEC. EX1015, 3, 8; EX1036, 8; EX1003, ¶¶189, 191-192.

In the Hazelzet/Wang combination (Ground 3), the training sequences would be like Wang's training between the interface circuits and the memory devices, with Hazelzet's open-drain output indicating that all data signal interfaces are trained. EX1090, 3:17-:22, 8:63-9:67, Fig.4C; EX1003, ¶¶190-192.

In each combination, the module does not communicate any data or perform any normal read or write operations during the training in accordance with the disclosure of these references and a POSITA's understanding. EX1003, ¶¶70, 188-190.

***b) Reasons to Combine***

Hazelzet, JEDEC, Buchmann, Wang, and Kim are analogous art to the '024 Patent because all are in the same field of memory module design and are reasonably pertinent to similar problems, including improving memory module operation to achieve improved capacity, speed, reliability, and efficiency by

techniques such as data buffering, error detection and correction, initialization, training, and the use of pins/paths for multiple purposes during different operations/modes. EX1001, Abstract, 1:22-:38, 3:30-:39, 6:41-:56, 8:46-9:23; EX1014, Abstract, ¶¶[0007], [0069-70], [0123]; EX1015, 1, 3, 8; EX1016, 1:7-:9, 3:49-:60, 4:51-5:50, 12:60-13:41, 14:1-:63, 20:20-21:19, 33:45-:67; EX1090, 1:5-:8, 2:16-:18, 2:40-:45, 8:1-:10, 9:9-:15; EX1017, 1:16-:22, 5:49-:57, 6:8-:18, 11:20-:34, 12:36-:53; EX1003, ¶¶193-194. The prior art relied on to illustrate the knowledge of a Skilled Artisan is also analogous art. *See, e.g.*, EX1022, ¶¶[0004-05], [0032-33], [0052]; EX1025, 15-18; EX1027, 1:61-2:19, 6:24-:25, 10:24-:45; EX1003, ¶195.

A POSITA would have considered each of the combinations analyzed here to be merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement, including known data buffering, training, and reporting techniques. Combining them as described here would therefore have been well within the level of ordinary skill in the art, would not have resulted in any unpredictable results, and could have been readily accomplished without undue experimentation and with a reasonable expectation of success. EX1003, ¶196.

**(1) Motivation to add data buffering and corresponding training**

A POSITA would have been motivated to add data buffering and corresponding training to the memory module of Hazelzet, which emphasizes the need for a “high density high reliability memory module” and “improved overall system reliability.” EX1014, Abstract, ¶¶[0001], [0003], [0004], [0007], [0042], [0044]; EX1003, ¶198. Hazelzet’s Registered DIMM (RDIMM), which buffers address and command signals, but not data, can support up to 4 ranks of memory. EX1014, Abstract, Fig.1, ¶[0036]. A POSITA understood that increasing the number of ranks without data buffering creates more electrical load on the data bus, limiting speed. EX1028, ¶[0031]; EX1003, ¶199. Thus, a POSITA would have been motivated to lower the electrical load by updating Hazelzet’s RDIMM to also buffer data signals. EX1003, ¶199. Data buffering was well known and had been already used in JEDEC’s LR-DIMM, in Buchmann’s fully-buffered DIMM, and in Ellsberry and Wang. EX1003, ¶¶199, 202; EX1079, pp.8-10 (illustrating RDIMM, FBDIMM, and LRDIMM arrangements).

For example, a POSITA would have known, as the provisional admits, about DDR3 LR-DIMMs with data buffers and corresponding training, including MB-DRAM training for optimal read and write operations, thereby motivating her to add these functionalities to other systems, such as Hazelzet’s. EX1008, 22;

EX1015, 3, 8-9; EX1003, ¶200. The well-known advantages of reduced load and increased performance and capacity of the data buffering functionality were designed to be added to an RDIMM, like Hazelzet's module. EX1036, 5 (“LRDIMM is intended to function in all RDIMM platforms”); EX1003, ¶202.

A POSITA would have also known about Wang's interface circuit and corresponding training to “provide higher memory performance” which can “reduce or eliminate idle time...between the data transfers” and “provide the higher capacity, higher parallelism that the memory controller desires” and the “accurate timing reference for data transmission that is critical.” EX1090, 2:40-:45, 6:52-:60, 8:1-:10, 7:44-:51 (nano-second data cycles and skew), 9:9-:15 (“training...to establish the clock-to-data phase relationship”); EX1003, ¶201. Wang's interface circuits, by buffering data signals, provide advantages over an RDIMM design (similar to LRDIMM), including that they “may be used with previously existing memory controllers, without modification to their logic or interfacing requirements.” EX1090, 1:41-2:15; EX1003, ¶203.

Therefore, a POSITA would have been motivated to upgrade Hazelzet's RDIMM with data buffering functionality like that of JEDEC's LRDIMM or Wang's interface circuit to achieve the known advantages of data buffering, including increased capacity and performance by reducing load on the data pins of Hazelzet's 4-rank RDIMM module and being able to work even in RDIMM

platforms (with appropriate BIOS changes). EX1028, [0031]; EX1077, 86:12-:21, 104:6-:24; EX1003, ¶204.

Moreover, Hazelzet's emphasis on the need for initialization in a "high reliability memory module" to achieve "improved overall system reliability," in light of the increased speed of DDR3, would have motivated a POSITA to add training to achieve these goals. EX1014, ¶¶[0001-0003], [0123]; EX1027, 1:35-2:12 (training enables being "reliable, fast, and efficient"); EX1025, pp.15-18 (training needed to communicate "Channel and DRAM commands"); EX1045, 22-24 (training for reads and writes); EX1090, 6:33-:37, 7:44-:51 ("account[] for the inter-device skew and jitter characteristics"); EX1017, 12:36-:53; EX1003, ¶205.

Such combinations would have been well within the level of skill and provided nothing more than expected from the combination: a load-reduced DIMM with a memory buffer (MB) or Wang's interface circuit that buffered data signals and implemented training to ensure reliable reading/writing during normal operation. EX1003, ¶206.

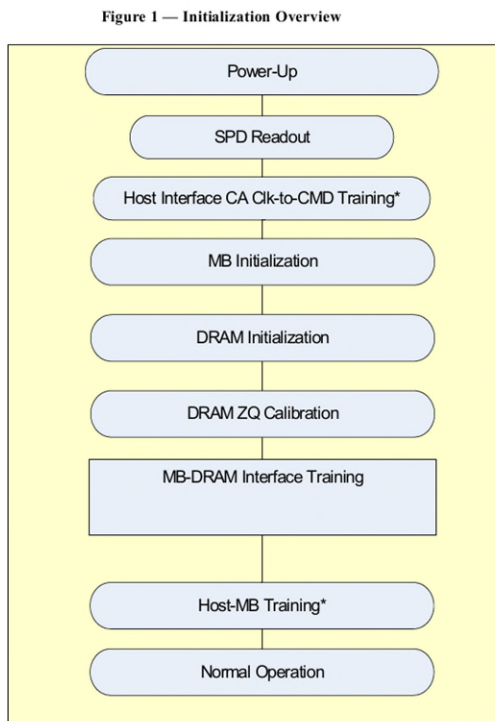
Similar to JEDEC and Wang, Buchmann also discloses a buffer/register that buffers data signals, as discussed above (pp.30-32), providing additional motivation to add data-signal-buffering functionality to Hazelzet's 4-rank RDIMM in order to lower the load on the data lines, allowing improved performance, higher frequencies of operation, and higher capacity. EX1003, ¶¶198-199,

208. Furthermore, Buchmann's "SBC mode" uses "error correcting code" and a "training phase...during start-up" to establish "reliable communication" on the bus, further motivating a POSITA to look to systems such as JEDEC's, Wang's, and Buchmann's that were designed to improve reliability (as desired by Hazelzet). EX1016, 3:64-:67, 14:5-:8, 14:25-:35; EX1003, ¶207. Thus, a POSITA would have also been motivated to use Buchmann's known, reliable, and efficient initialization techniques for Hazelzet's upgraded module, including Buchmann's training and corresponding notifications, which was well within the level of skill and provided nothing more than expected from the combination: a DIMM with a buffer to buffer data, address, and command signals and efficient training of that buffer during initialization to ensure optimal read and write performance during normal operation. EX1003, ¶208.

**(2) *Motivation to use training without normal memory read or write operations***

A POSITA would have been further motivated to combine Hazelzet with JEDEC, Buchmann, or Wang by using training without normal memory read or write operations, because training is designed to minimize errors for subsequent normal memory read and write operations by "ensur[ing] successful writes" and "ensur[ing] [the Memory Buffer (MB) on the DIMM] can capture read data from the DRAMs correctly." EX1015, 3, 8 ("No DRAM commands...can be issued to the MB until the MB-DRAM Interface training is complete"), p.4 Fig.1 (below,

left); EX1090, 7:44-:51 (training whenever data “can no longer [be] reliably capture[d]”), Figs.4C (below, right) & 4D, 9:9-:52 (“normal operation” following training); EX1025, 15-18 (initialization including “Calibrate...Training, Testing, and Polling,” which “prevent[s]...DRAM commands from being communicated to the AMBs”); EX1022, Fig. 4, ¶¶[0032], [0052], [0088-89]; EX1056, 18, 22, 25-26, 42-44; EX1057, Fig.5, Abstract, 2:13-:34, 2:60-3:3, 9:11-10:44; EX1003, ¶¶70, 209.



\* This step is optional for the MB but may be done by some platforms

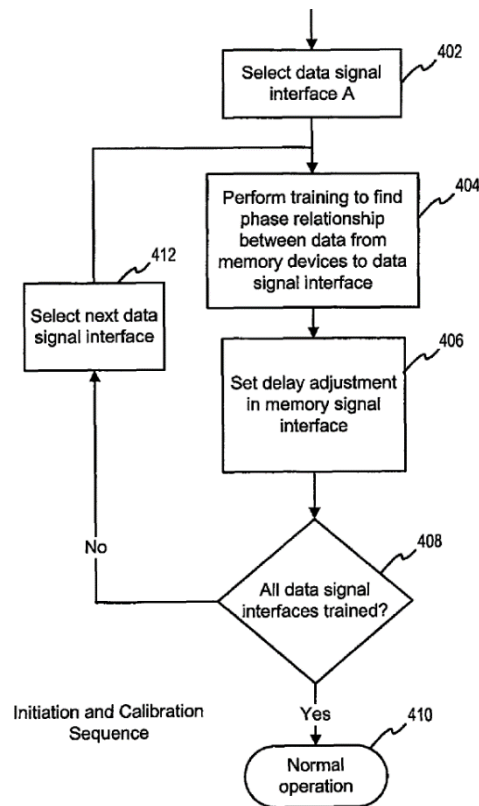


FIG. 4C

Likewise, Buchmann’s “initialization training sequence” is completed at “power-on,” teaching the importance of training before normal memory read and write

operations. EX1016, Abstract; EX1003, ¶209. Hazelzet is also initialized upon power-on, as was standard. EX1014, ¶[0123]; *see also* EX1025, 15-18; EX1027, 1:61-2:19; 6:24-:25; 10:24-:45. Thus, JEDEC's, Buchmann's, and Wang's training would have complemented Hazelzet's initialization, and a POSITA would have been motivated to combine Hazelzet and JEDEC or Buchmann or Wang such that the training occurred separate from normal read and write operations, to ensure that subsequent normal read and write operations can be reliable and efficiently performed. EX1003, ¶210.

**(3) Motivation to use Hazelzet's open-drain signaling for training notifications**

It would have been further obvious to combine Hazelzet with JEDEC, Buchmann, or Wang and use Hazelzet's open-drain output (e.g., UE) and corresponding techniques to report a status of the respective JEDEC, Buchmann, or Wang training sequences. EX1003, ¶¶211-212. The open-drain output can indicate that the modules are performing training operations and cannot be accessed for any normal read or write operations during that training. *Id.* The system memory controller can return to "Normal Operation" after the completion of the training. *Id.*

As discussed above (pp.17-22), open-drain outputs were well known, as was their use for handshaking, including interrupts and reporting status of pending operations, thereby avoiding the need to interrogate when a port is ready. EX1003,

¶213; EX1089, pp.15-16. Using interrupts to indicate completion of initialization was a known, standardized alternative to polling. EX1003, ¶39; EX1025, p.114. A POSITA would have understood and been motivated to use interrupt-like handshaking between memory modules and their memory controller to avoid the memory controller interrogating the modules to determine if they are ready. *Id.* Hazelzet's module already had open-drain outputs for interrupt-like handshaking, rendering obvious to use one of these (e.g., UE) to inform the memory controller when the modules' training is complete and it can initiate normal read and write operations. EX1003, ¶213; EX1089, 14-15, 89 ("The handshake lines have a role analogous to traffic lights on a roadway.").

As explained by textbooks, Hazelzet's open-drain outputs provided a "wired-OR" configuration which is particularly useful to indicate to a memory controller when **all** modules have completed training and are ready for data. EX1003, ¶214; EX1089, 281, 219-20. Furthermore, as discussed above (pp.25-27), Hazelzet uses the same open-drain "UE" output in two different modes—parity and ECC—motivating a POSITA to use that same output for reporting status of training, which is implemented before Hazelzet's parity and ECC modes. EX1003, ¶215; EX1014, Figs.4B, 7A, [0044], [0049], [0059], [0064], [0069-70], [0072], [0109]. Because normal memory read and write operations are performed

in the ECC and parity modes, those operations would not use the open drain outputs during training. *Id.*

A POSITA would have similarly viewed JEDEC's proposed open-drain training notification technique as a natural fit with Hazelzet's memory module (updated with data buffering). EX1015, pp.3, 8; EX1003, ¶216. A POSITA therefore would have been motivated to use JEDEC's training notification technique in Hazelzet, even when combined with Buchmann or Wang. *Id.*; EX1016, 6:19-:20, 8:43-:44; EX1090, 4:55-:62. And a POSITA would have been motivated to use the same output pin to notify both error and training status in different modes of operation because it would have been considered a known and efficient use of the limited number of output pins, as discussed above (pp.14-17). EX1003, ¶217.

For example, Kim discloses a system similar to Hazelzet's, *compare* EX1014, *with* EX1017, with additional details about the use of open-drain outputs, EX1017, 1:16-:22, 5:49-:57, 6:8-:16. Kim teaches, for example, (1) "completing a training process to establish reliable communication," EX1017, 12:36-:53, (2) "initialization circuitry" which "may reside local" to the memory module, resulting in "added performance...while making use of unused circuits within the subsystem," *id.* 11:20-:34, and (3) that functions other than the ECC and parity error may "also share the error feedback pin," *id.* 6:16-:18, further motivating a

POSITA to use Hazelzet's open-drain output (UE, corresponding to Kim's "error feedback pin") to notify the memory controller about training status, EX1003, ¶217.

Similarly, Talbot discloses memory modules with two modes: "a normal operation mode" and a "configuration and test mode," the latter including "training mode" during which a "CRC signal path," normally used for error detection and correction, is used to "loop[] back" "training patterns." EX1022, ¶¶[0004]-[0005], [0032]-[0033], [0052]. Thus, Talbot teaches that a path for CRC (a type of ECC) can also be used to return other signals during training when the CRC functionality is off, *id.*, [0033], [0052], further motivating a POSITA to use Hazelzet's open-drain output (UE, corresponding to Talbot's "CRC signal path") to notify the memory controller about training status, EX1003, ¶218.

Moreover, a POSITA would have been motivated to arrange the updated Hazelzet modules to signal completion of training to the memory controller only when all memory modules completed training, to ensure that the entire memory system had been trained before proceeding to normal operations. EX1003, ¶219. This would permit orderly and systematic training, limiting the complexity of the control circuitry needed for training. *Id.*; EX1043, 7:30-:51. As discussed above (pp.17-22), use of an open-drain signal in this manner was a known, efficient way to communicate information about multiple circuits because it effectively OR'd the

inputs into a single output. EX1003, ¶219; EX1017, Fig.4, 5:65-6:12; *see also* EX1014, ¶[0018], [0109]. Hazelzet's memory system includes multiple memory modules in need of training, thus a normal mode of operation is available when all memory modules had signaled the completion of training. EX1003, ¶220; EX1014, ¶[0018], [0109]; EX1017, Fig4, 5:65-6:12; EX1043, 7:30-:51; EX1090, 9:58-:67. Hazelzet's open-drain output allows notifying the host when all modules have completed training, because as discussed above (pp.17-22) any of the modules can pull the open-drain output to "low" if it is still executing its training sequence, regardless of whether other modules have completed training and are no longer pulling that pin low. EX1003, ¶220.

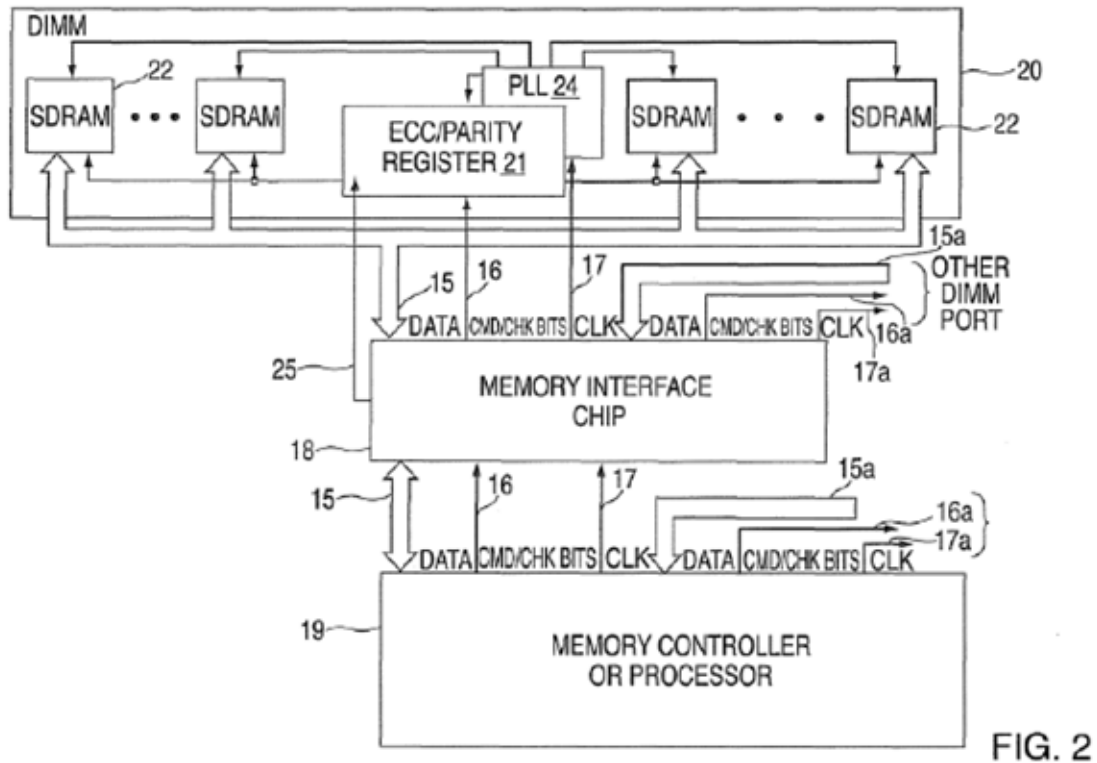
## **2. Independent Claim 1**

Claim 1 is obvious in view of Grounds 1-3. The limitations of claim 1 correspond to claim limitations of the '623, '218, and '595 patents, EX1003, ¶¶153-155, which the Board already found obvious over the combination of Hazelzet and Buchmann. EX1034 ('623 FWD), pp.9-20; EX1102 ('218 FWD), pp.15-53; EX1103 ('595 FWD), pp.16-53.

### **a) [1.a] Preamble**

To the extent the preamble is limiting, Grounds 1-3 teach "[a] *memory module* [Hazelzet's dual inline memory modules 20 ("DIMMs")] *operable with a memory controller* [Hazelzet's "memory controller" 19] *of a host system.*"

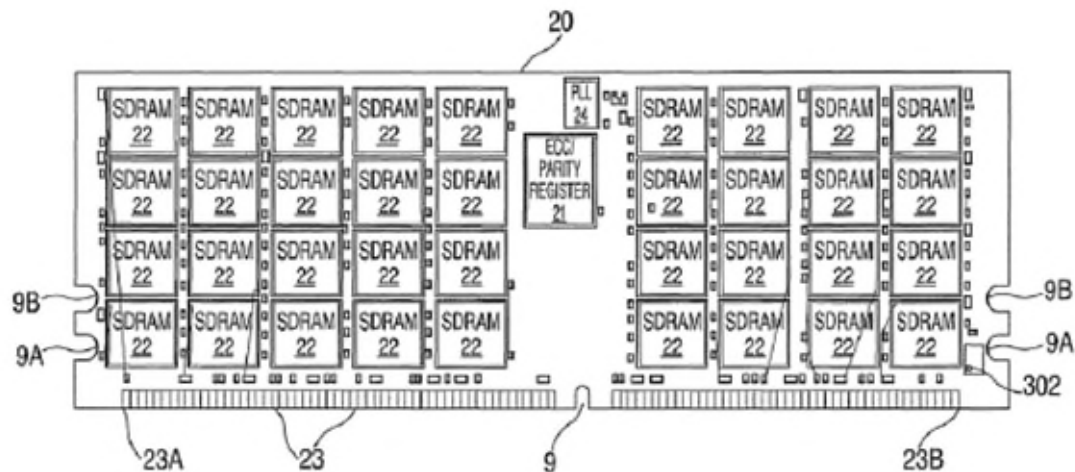
EX1003, ¶¶223-225; EX1014, Figs.2 (below), 3A-3D, ¶¶[0036]-[0039]. The Board's previous decisions confirm Ground 2 teaches equivalent limitations in '623 claim [1.a], '218 claim [1.a], and '595 claim [1.a]. EX1003, ¶¶153-155, 223; EX1034, 9; EX1102, 44; EX1103, 44.



**b) [1.b.1] Printed Circuit Board**

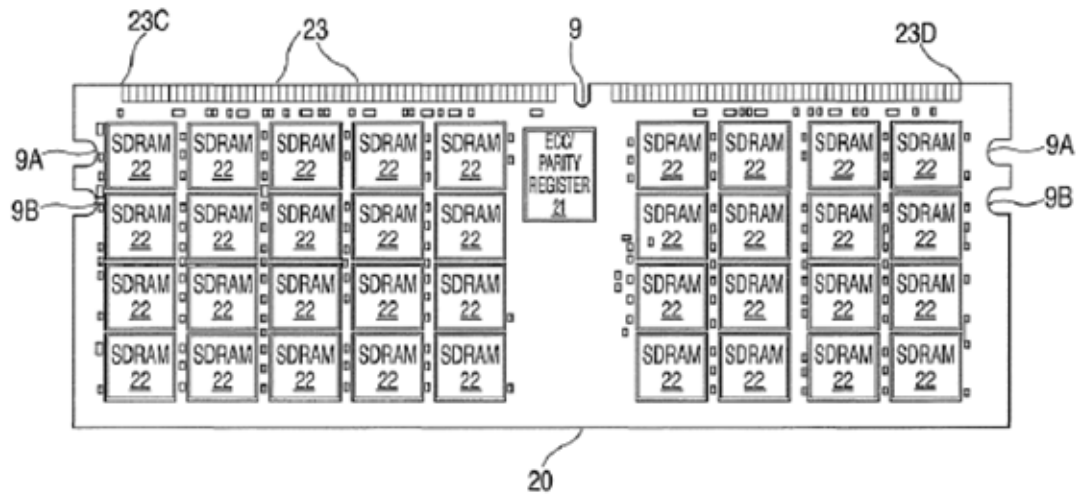
Grounds 1-3 teach that the memory module is “a printed circuit board [e.g., Hazelzet’s “printed circuit board having a front side and a back side and a plurality of double data rate (DDR) DRAMs...affixed to both the front surface and the back surface.” EX1014, ¶[0015], Figs.2, 3A, 3B, 3C, 3d] *having edge connections* [including “connectors 23 along the edge of both the back and front sides” of the

PCB, EX1014, ¶[0039]] *that fit into a corresponding slot of the host system [e.g., “DIMM Slot” 1102, EX1014, Figs. 11, 9, ¶¶ [0097], [0032]] so as to be in electrical communication with the memory controller.”* EX1003, ¶¶226-229. The Board’s previous decisions confirm Ground 2 teaches equivalent limitations in ’623 claims [1.a] and [1.d], ’218 claim [1.b], and ’595 claim [1.b]. EX1003, ¶¶153-155, 226; EX1034, 9-20; EX1102, 44-46; EX1103, 44-45.



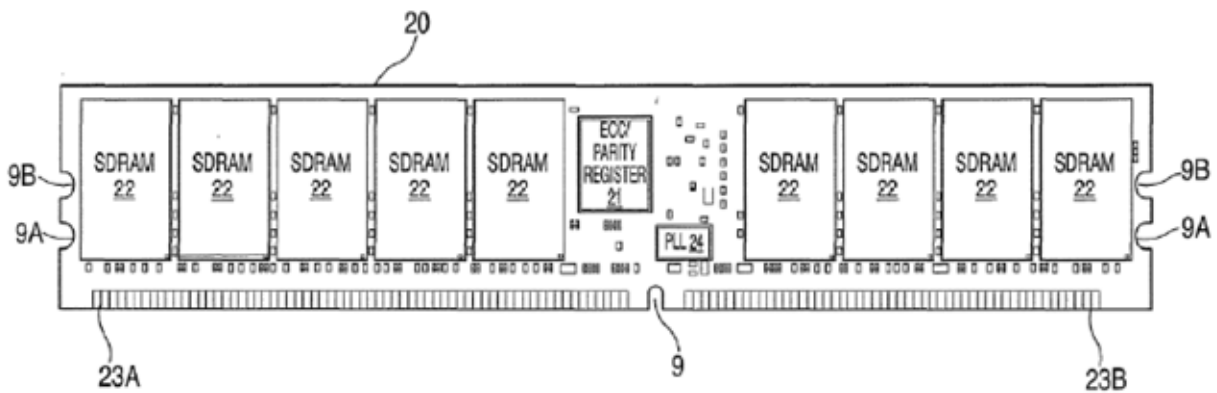
FRONT SIDE OF DIMM - 72 PLANAR

FIG. 3A



BACK SIDE OF DIMM - 72 PLANAR

FIG. 3B



FRONT SIDE OF DIMM - 4 HIGH STACK

FIG. 3C

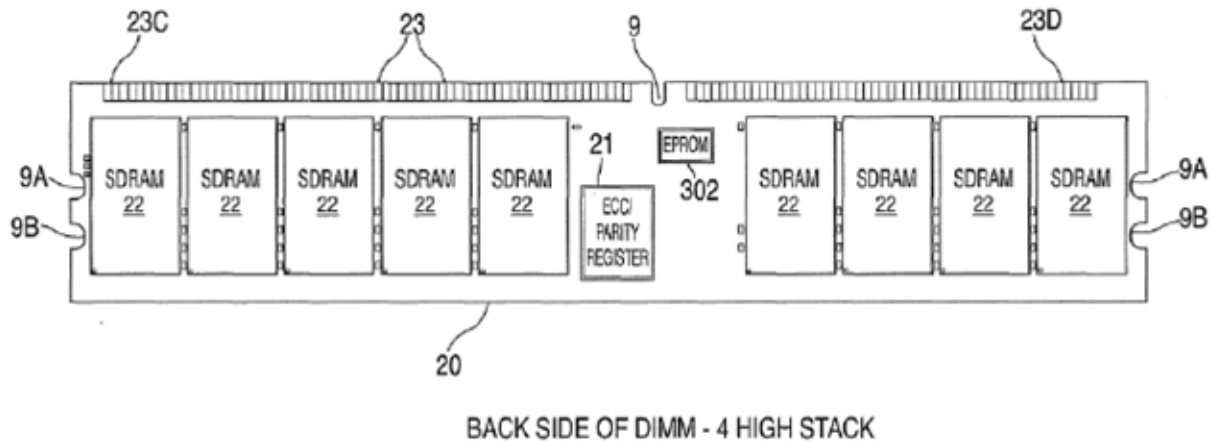
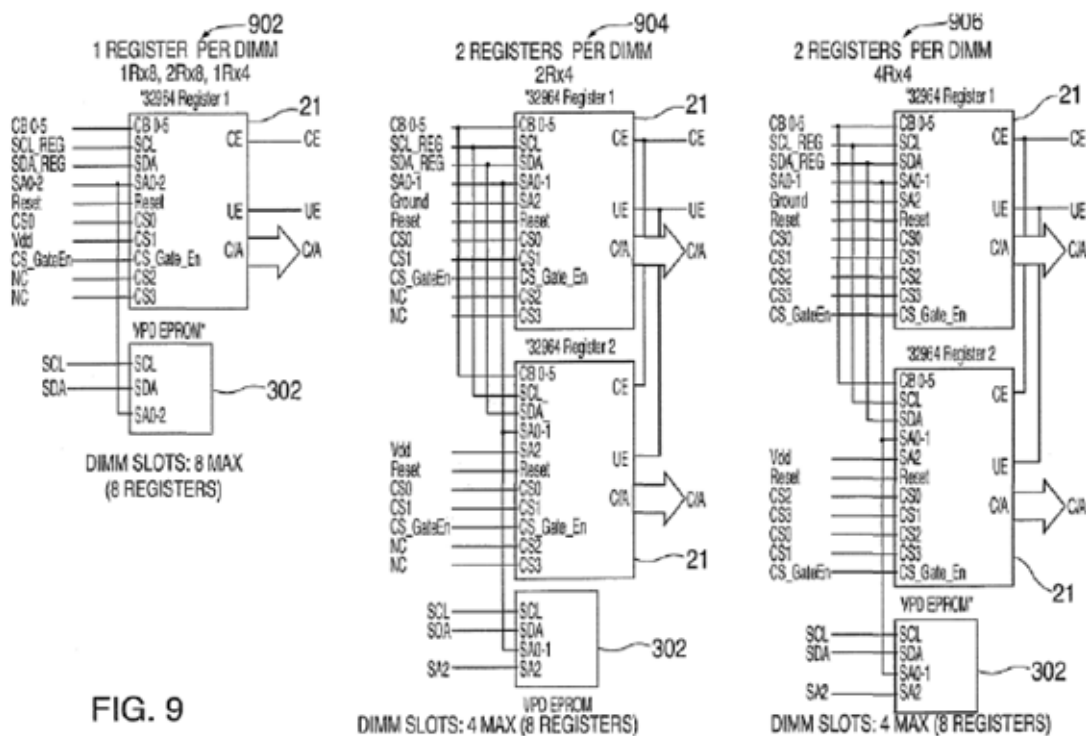


FIG. 3D



**c) [1.b.2] First, Second and Error Edge Connections**

Grounds 1-3 teach “the edge connections including first edge connections [e.g., green, for address and control signals from the host memory controller, EX1014, Figs.7A-7C, ¶¶[0072], [0068], [0038]], second edge connections [e.g.,

blue, DQ0-DQ63, for data signals between the memory module and the host memory controller, EX1014, Figs.7A-7C], *and an error edge connection* [e.g., red, uncorrectable error pin UE (4, 142) coupled to the open-drain output UE, EX1014, Fig.7A] *in addition to the first edge connections and the second edge connections.*” EX1003, ¶¶230-234. The Board’s previous decisions confirm Ground 2 teaches equivalent limitations in ’623 claim [1.d], ’218 claim [1.b], and ’595 claim [1.b]. EX1003, ¶¶153-155, 230; EX1034, 9-20; EX1102, 44-46, EX1103, 44-45.

| SERVER DIMM<br>PIN NUMBER PIN NAME | SERVER DIMM<br>PIN NUMBER PIN NAME |
|------------------------------------|------------------------------------|
| 1 Vref                             | 139 Vref                           |
| 2 SCL                              | 140 SCL                            |
| 3 SDA                              | 141 SDA                            |
| 4 UE                               | 142 UE                             |
| 5 CE                               | 143 CE                             |
| 6 VDD                              | 144 VDD                            |
| 7 ECCMODE                          | 145 ECCMODE                        |
| 8 DLY CKE/ODT                      | 146 DLY CKE/ODT                    |
| 9 CS GATE EN                       | 147 CS GATE EN                     |
| 10 GND                             | 148 GND                            |
| 11 DQ0                             | 149 DQ4                            |
| 12 DQ1                             | 150 DQ5                            |
| 13 GND                             | 151 GND                            |
| 14 DQS0*                           | 152 DQS9                           |
| 15 DQS0                            | 153 DQS9*                          |
| 16 GND                             | 154 GND                            |
| 17 DQ2                             | 155 DQ8                            |
| 18 DQ3                             | 156 DQ7                            |
| 19 GND                             | 157 GND                            |
| 20 VDD                             | 158 VDD                            |
| 21 GND                             | 159 GND                            |
| 22 DQ8                             | 160 DQ12                           |
| 23 DQ9                             | 161 DQ13                           |
| 24 GND                             | 162 GND                            |
| 25 DQS1*                           | 163 DQS10                          |
| 26 DQS1                            | 164 DQS10*                         |
| 27 GND                             | 165 GND                            |
| 28 DQ10                            | 166 GND                            |
| 29 DQ11                            | 167 DQ14                           |
| 30 GND                             | 168 GND                            |
| 31 DQ16                            | 169 DQ20                           |
| 32 DQ17                            | 170 DQ21                           |
| 33 GND                             | 171 GND                            |
| 34 DQS2*                           | 172 DQS11                          |
| 35 DQS2                            | 173 DQS11*                         |
| 36 GND                             | 174 GND                            |
| 37 DQ18                            | 175 DQ22                           |
| 38 DQ19                            | 176 DQ23                           |
| 39 GND                             | 177 GND                            |
| 40 RESET                           | 178 RESET                          |
| 41 VDD                             | 179 VDD                            |
| 42 GND                             | 180 GND                            |
| 43 DQ24                            | 181 DQ28                           |
| 44 DQ25                            | 182 DQ29                           |
| 45 GND                             | 183 GND                            |
| 46 DQS3*                           | 184 DQS12                          |
| 47 DQS3                            | 185 DQS12*                         |
| 48 GND                             | 186 GND                            |
| 49 DQ26                            | 187 DQ30                           |
| 50 DQ27                            | 188 DQ31                           |
| 51 GND                             | 189 GND                            |
| 52 CB0                             | 190 CB4                            |

FIG. 7A

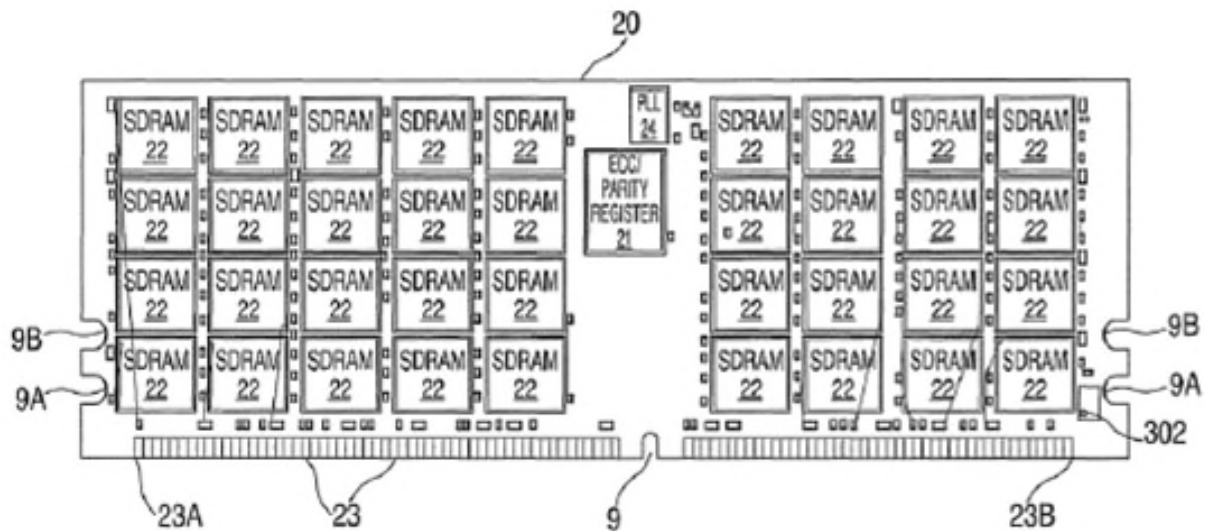
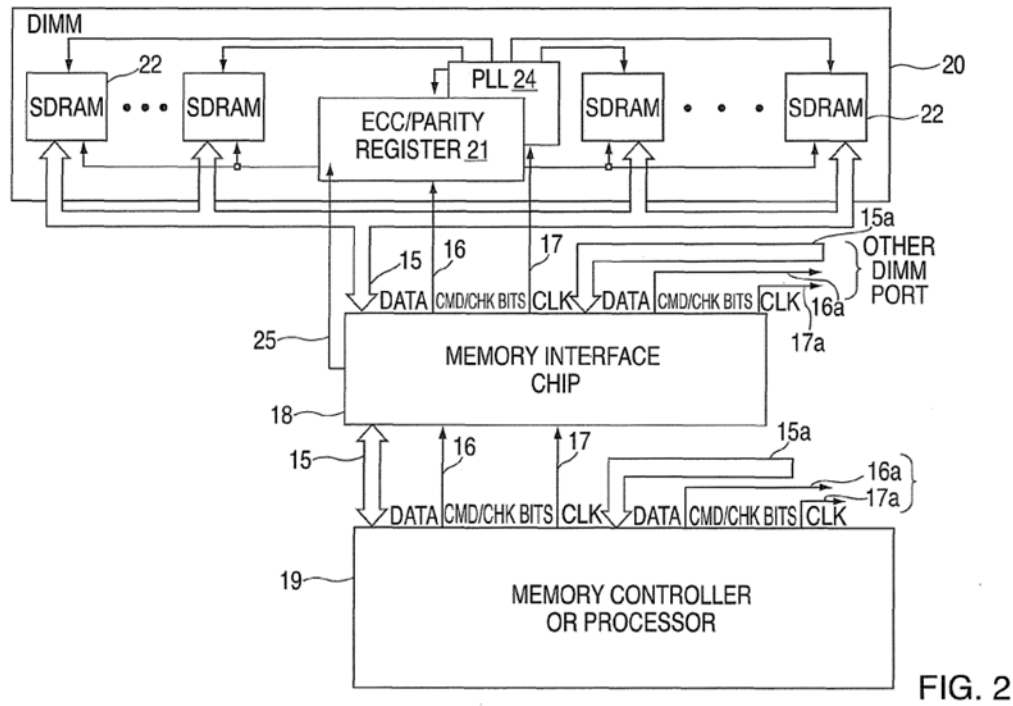
|               |            |
|---------------|------------|
| 53 CB1        | 191 CB5    |
| 54 GND        | 192 GND    |
| 55 DQS8*      | 193 DQS17  |
| 56 DQS8       | 194 DQS17* |
| 57 GND        | 195 GND    |
| 58 CB2        | 196 CB6    |
| 59 CB3        | 197 CB7    |
| 60 GND        | 198 GND    |
| 61 VDD        | 199 VDD    |
| 62 CKE1       | 200 CKE1   |
| 63 CHKBT4     | 201 CHKBT1 |
| 64 CHKBT5     | 202 CHKBT3 |
| 65 CKE0       | 203 CKE0   |
| 66 VDD        | 204 VDD    |
| 67 A15        | 205 A14    |
| 68 BA2        | 206 A12    |
| 69 CHKBT0/PTY | 207 A9     |
| 70 A11        | 208 CHKBT2 |
| 71 VDD        | 209 VDD    |
| 72 A7         | 210 A8     |
| 73 A5         | 211 A6     |
| 74 A4         | 212 A3     |
| 75 A2         | 213 A1     |
| 76 VDD        | 214 VDD    |
| 77 CK0        | 215 CK0    |
| 78 CK0B       | 216 CK0B   |
| 79 VDD        | 217 VDD    |
| 80 GND        | 218 GND    |
| 81 VDD        | 219 VDD    |
| 82 A10        | 220 A0     |
| 83 BA0        | 221 BA1    |
| 84 WE         | 222 RAS    |
| 85 VDD        | 223 VDD    |
| 86 CS0        | 224 CS0    |
| 87 CAS        | 225 CS3    |
| 88 ODT0       | 226 ODT0   |
| 89 CS3        | 227 A13    |
| 90 VDD        | 228 VDD    |
| 91 CS1        | 229 CS1    |
| 92 ODT1       | 230 ODT1   |
| 93 CS2        | 231 CS2    |
| 94 VDD        | 232 VDD    |
| 95 GND        | 233 GND    |
| 96 DQ32       | 234 DQ36   |
| 97 DQ33       | 235 DQ37   |
| 98 GND        | 236 GND    |
| 99 DQS4*      | 237 DQS13  |
| 100 DQS4      | 238 DQS13* |
| 101 GND       | 239 GND    |
| 102 DQ34      | 240 DQ38   |

FIG. 7B

Hazelzet's "*first edge connections*" communicate address and control signals from the host system's memory controller. EX1014, Figs.7A-7C, ¶[0072] ("/CS"), ¶[0068] (address and control signals including "chip select (CS), address (Addr), row address strobe (RAS), column address strobe (CAS) and write enable (WE)"), ¶[0038] ("address and command information to the register chip 21 via add/cmd line 16"), Fig.2, ¶¶[0015], [0035], [0041]. The "*second edge connections*" (DQ0-DQ63) are used for data communication with the memory module in "parity" or "ECC" modes. *Id.*, Fig.8 ("Data In" and "Data Out" in "parity" and "ECC" modes). Hazelzet's "*error edge connection*," e.g., error pin UE, is coupled to an open-drain output 121 of the module controller. EX1014, Fig.7A (above, red), Fig.4B, ¶¶[0072], [0109].

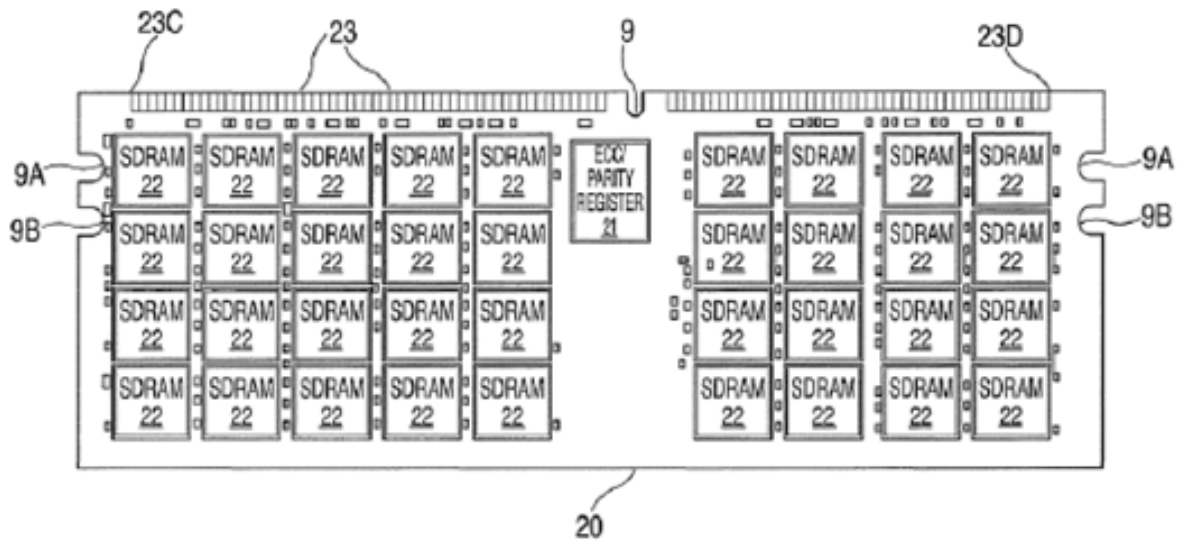
**d) [1.c.1] Module Controller**

Grounds 1-3 teach "*a module controller* [including one or more ECC/Parity register 21] *on the printed circuit board* [e.g., DIMM]." EX1003, ¶¶235-237; EX1014, Figs.2-3D (below, ECC/Parity register on DIMM), Fig.9, Figs.4A-4B (details of ECC/Parity register), ¶¶[0032], [0039]-[0042], [0044]. The Board's previous decisions confirm Ground 2 teaches equivalent limitations in '623 claims [1.a], [1.b], and [1.d], '218 claim [1.d], and '595 claim [1.d]. EX1003, ¶¶153-155, 235; EX1034, 9-20; EX1102, 46-47; EX1103, 45-46.

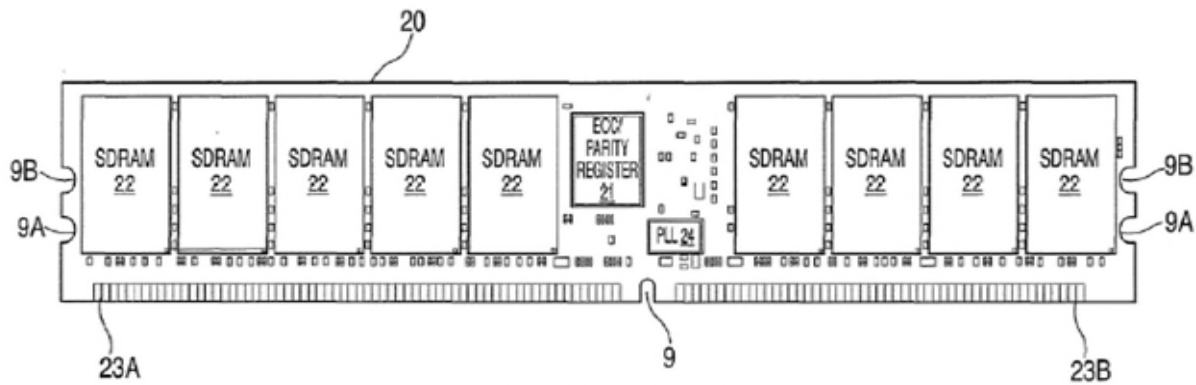


FRONT SIDE OF DIMM - 72 PLANAR

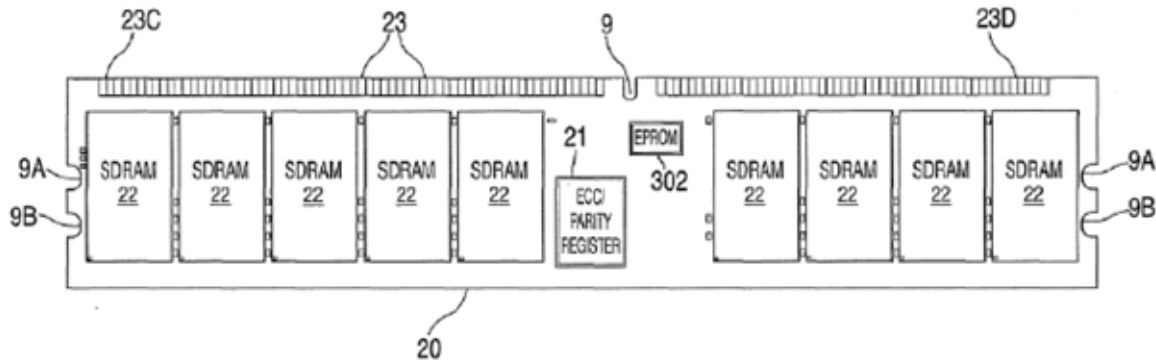
FIG. 3A



BACK SIDE OF DIMM - 72 PLANAR  
FIG. 3B



FRONT SIDE OF DIMM - 4 HIGH STACK  
FIG. 3C



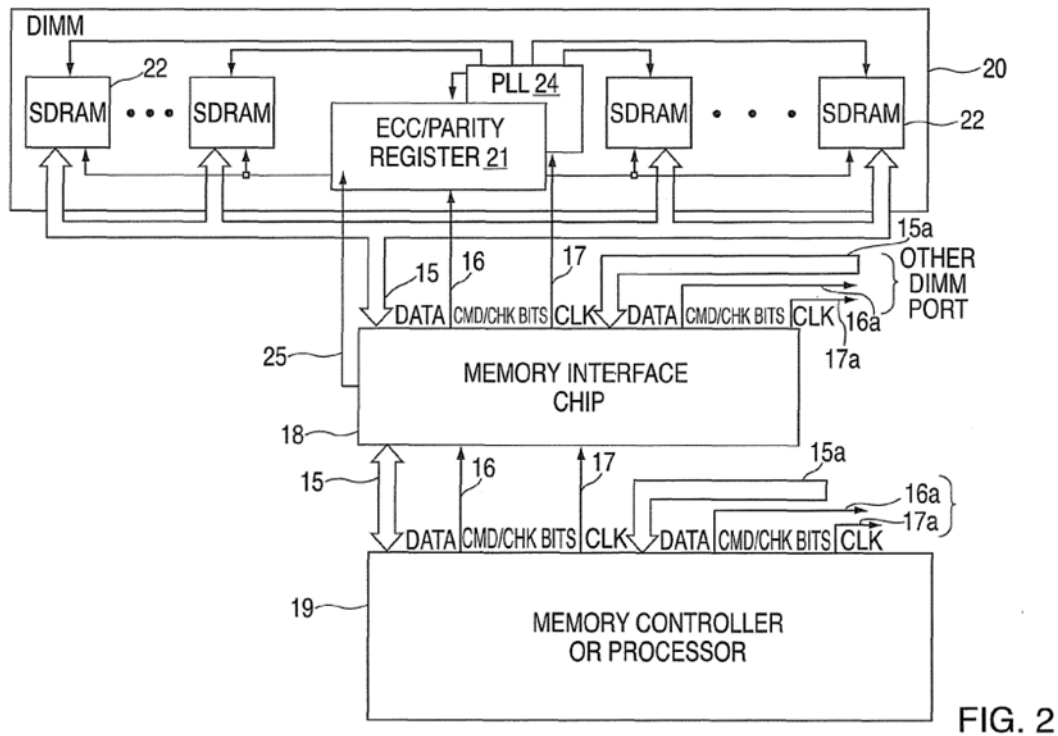
BACK SIDE OF DIMM - 4 HIGH STACK

FIG. 3D

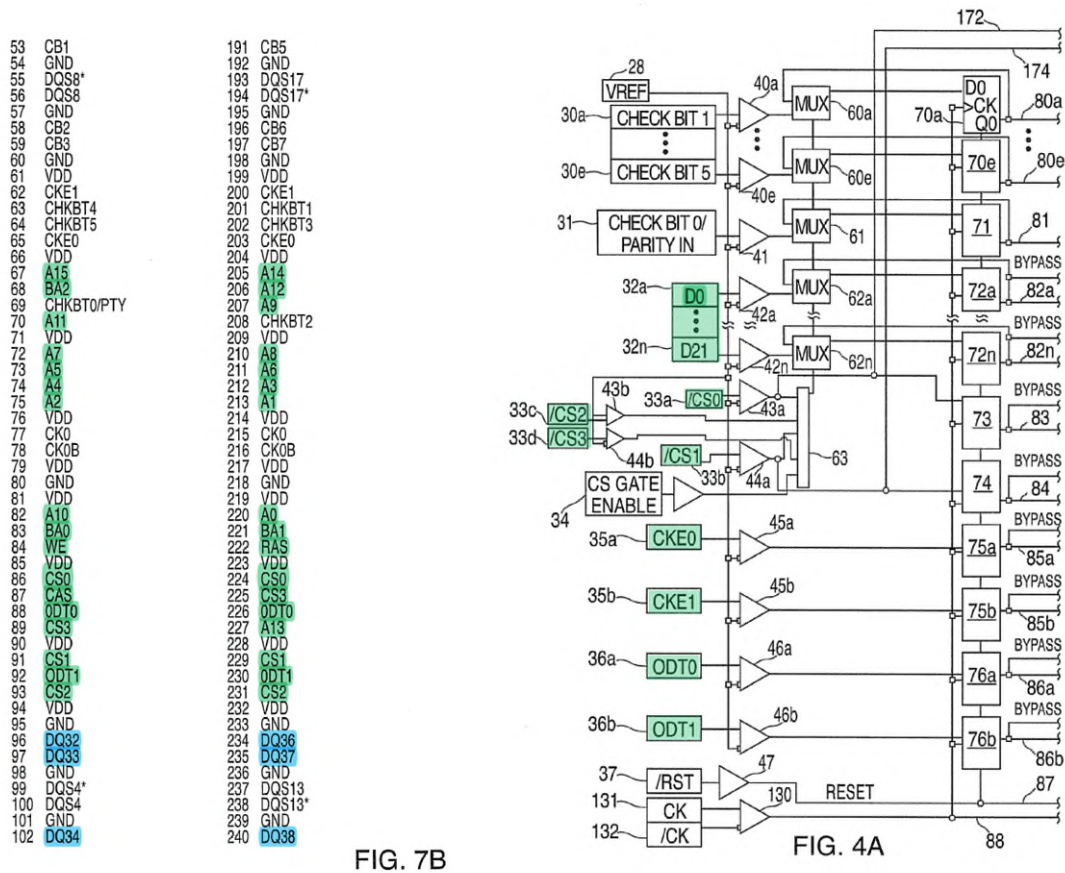
**e) [1.c.2] Receive Address and Control Signals**

Grounds 1-3 teach the module controller being “*configured to receive address and control signals associated with normal memory read or write operations via the first edge connections.*” EX1003, ¶¶238-242. The Board’s previous decisions confirm Ground 2 teaches equivalent limitations in ’623 claims [1.d] and 2, ’218 claim [1.g.i], and ’595 claim [1.f.i]. EX1003, ¶¶153-155, 238; EX1034, 9-21; EX1102, 50-51; EX1103, 48-49.

Hazelzet discloses its ECC/Parity Register 21 receiving “address and commands via line 16.” EX1014, ¶[0038], Fig.2 (below).



A POSITA would have understood that lines 16 are coupled to the module's edge connections for address and control, thus Hazelzet discloses its “*module controller*,” including ECC/Parity register 21, receiving “*address and control signals*” (green) “*via the first edge connections.*” EX1014, Figs.7B and 4A (annotated below left and right, respectively, showing corresponding address and control lines, green: /CS0-/CS3, CKE0-CKE1, ODT0-ODT1, 32a-32n for A0-A15, BA0-BA2, RAS, CAS, WE), [0027], [0044], [0048]; EX1003, ¶239.



Hazelzet's ECC/Parity register receives the “*address and control signals*” and includes buffers to drive those signals to the memory devices. EX1014, ¶¶[0024], [0044], [0015], [0035], [0038], [0041]; EX1003, ¶239. During normal operation of Hazelzet's module, those “*address and control signals* [including A0-A15, BA0-BA2, RAS, CAS, WE, CS] [are] *associated with normal memory read or write operations*” to read/write data from/into the module memory devices (SDRAMs 22) according to the JEDEC standards. EX1003, ¶240; EX1014, ¶¶[0068], [0073], [0084], Fig.2 (reproduced below, illustrating the address and command lines, green); EX1056, 33 (Command Truth Table, below, annotated,

Read/Write commands conveyed by signals including CS#, RAS#, CAS#, WE#, A0-A15, BA0-BA2); EX1084 (JESD79-2B), 46-47 (similar); EX1024 (JESD79), 13 (similar).

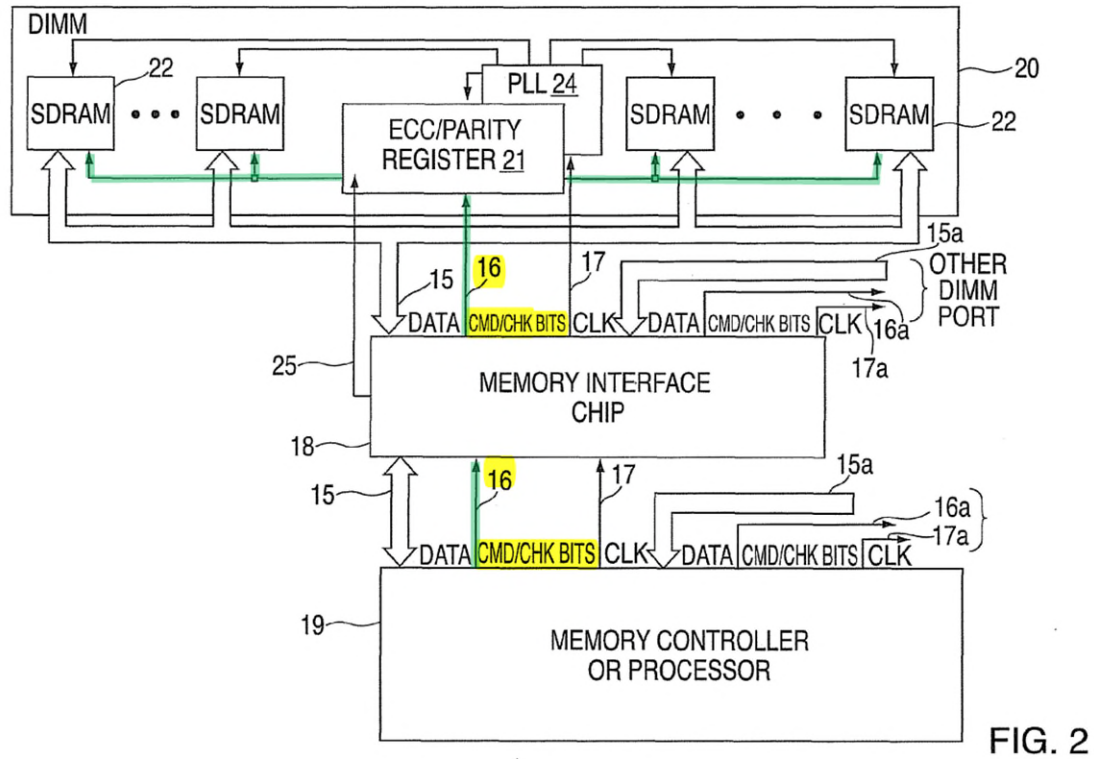
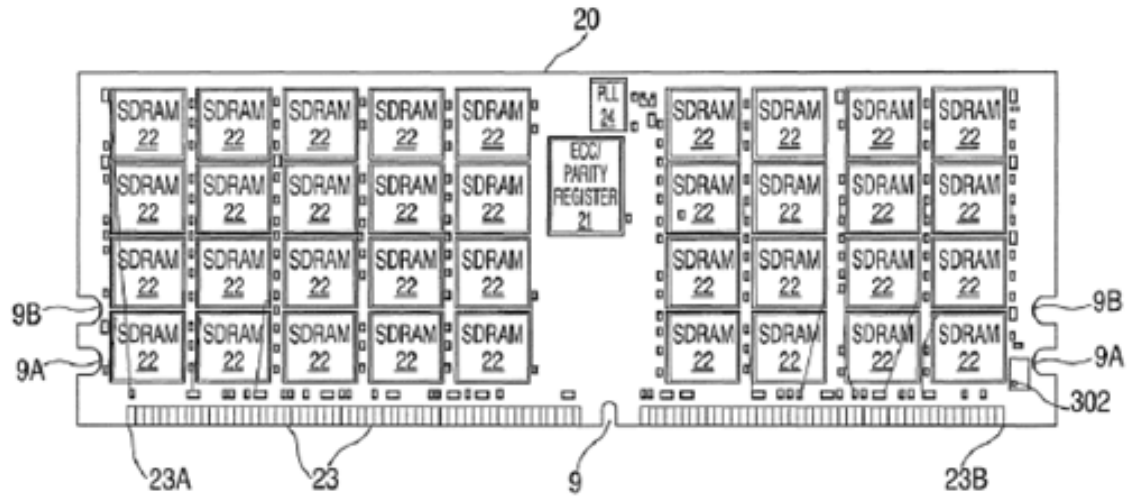


Table 6 — Command Truth Table

| Function                                     | Abbreviation | CKE            |               | CS# | RAS# | CAS# | WE# | BA0-BA2 | A13-A15          | A12-BC# | A10-AP | A0-A9, A11 | Notes    |
|----------------------------------------------|--------------|----------------|---------------|-----|------|------|-----|---------|------------------|---------|--------|------------|----------|
|                                              |              | Previous Cycle | Current Cycle |     |      |      |     |         |                  |         |        |            |          |
| Mode Register Set                            | MRS          | H              | H             | L   | L    | L    | L   | BA      | OP Code          |         |        |            |          |
| Refresh                                      | REF          | H              | H             | L   | L    | L    | H   | V       | V                | V       | V      | V          | 7,9,12   |
| Self Refresh Entry                           | SRE          | H              | L             | L   | L    | L    | H   | V       | V                | V       | V      | V          |          |
| Self Refresh Exit                            | SRX          | L              | H             | H   | X    | X    | X   | X       | X                | X       | X      | X          |          |
| Single Bank Precharge                        | PRE          | H              | H             | L   | L    | H    | L   | BA      | V                | V       | L      | V          | 7,8,9,12 |
| Precharge all Banks                          | PREA         | H              | H             | L   | L    | H    | L   | V       | V                | V       | H      | V          |          |
| Bank Activate                                | ACT          | H              | H             | L   | L    | H    | H   | BA      | Row Address (RA) |         |        |            |          |
| Write (Fixed BL8 or BC4)                     | WR           | H              | H             | L   | H    | L    | L   | BA      | RFU              | V       | L      | CA         |          |
| Write (BC4, on the Fly)                      | WRS4         | H              | H             | L   | H    | L    | L   | BA      | RFU              | H       | L      | CA         |          |
| Write (BL8, on the Fly)                      | WRS8         | H              | H             | L   | H    | L    | L   | BA      | RFU              | H       | L      | CA         |          |
| Write with Auto Precharge (Fixed BL8 or BC4) | WRA          | H              | H             | L   | H    | L    | L   | BA      | RFU              | V       | H      | CA         |          |
| Write with Auto Precharge (BC4, on the Fly)  | WRAS4        | H              | H             | L   | H    | L    | L   | BA      | RFU              | L       | H      | CA         |          |
| Write with Auto Precharge (BL8, on the Fly)  | WRAS8        | H              | H             | L   | H    | L    | L   | BA      | RFU              | H       | H      | CA         |          |
| Read (Fixed BL8 or BC4)                      | RD           | H              | H             | L   | H    | L    | H   | BA      | RFU              | V       | L      | CA         |          |
| Read (BC4, on the Fly)                       | RDS4         | H              | H             | L   | H    | L    | H   | BA      | RFU              | L       | L      | CA         |          |
| Read (BL8, on the Fly)                       | RDS8         | H              | H             | L   | H    | L    | H   | BA      | RFU              | H       | L      | CA         |          |
| Read with Auto Precharge (Fixed BL8 or BC4)  | RDA          | H              | H             | L   | H    | L    | H   | BA      | RFU              | V       | H      | CA         |          |
| Read with Auto Precharge (BC4, on the Fly)   | RDAS4        | H              | H             | L   | H    | L    | H   | BA      | RFU              | L       | H      | CA         |          |
| Read with Auto Precharge (BL8, on the Fly)   | RDAS8        | H              | H             | L   | H    | L    | H   | BA      | RFU              | H       | H      | CA         |          |
| No Operation                                 | NOP          | H              | H             | L   | H    | H    | H   | V       | V                | V       | V      | V          | 10       |
| Device Deselected                            | DES          | H              | H             | H   | X    | X    | X   | X       | X                | X       | X      | X          | 11       |

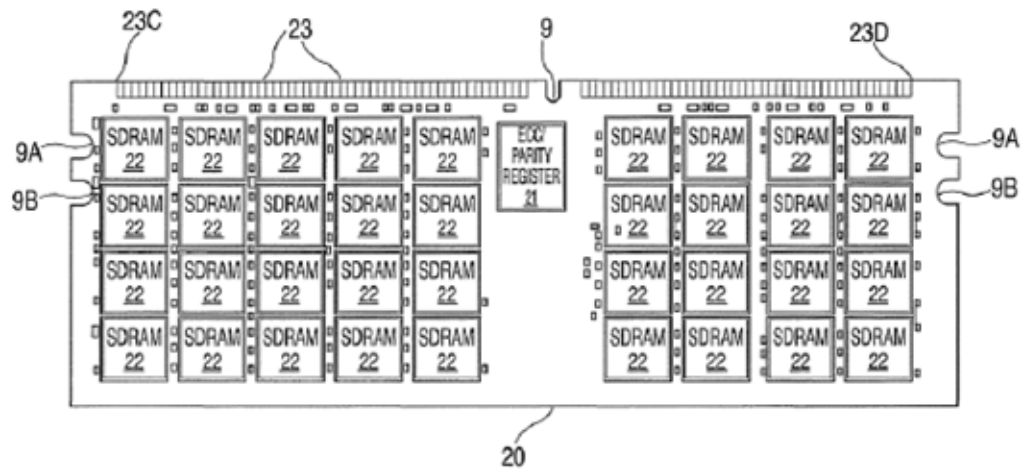
## f) [1.d.1] DRAM

Grounds 1-3 teach “*dynamic random access memory elements* [SDRAMs 22] *on the printed circuit board* [DIMM].” EX1003, ¶¶243-245; EX1014, ¶[0015] (“The DIMM...is comprised of a printed circuit board having... [DDR] DRAMs or [SDRAMs] affixed to both the front surface and the back surface.”), Figs.2-3D (below), ¶¶[0037], [0039]. The Board’s previous decisions confirm Ground 2 teaches equivalent limitations in ’623 claims [1.a], [1.d], and 2, ’218 claim [1.c], and ’595 claim [1.c]. EX1003, ¶¶153-155, 243; EX1034, 9-21; EX1102, 46; EX1103, 45.



FRONT SIDE OF DIMM - 72 PLANAR

FIG. 3A



BACK SIDE OF DIMM - 72 PLANAR

FIG. 3B

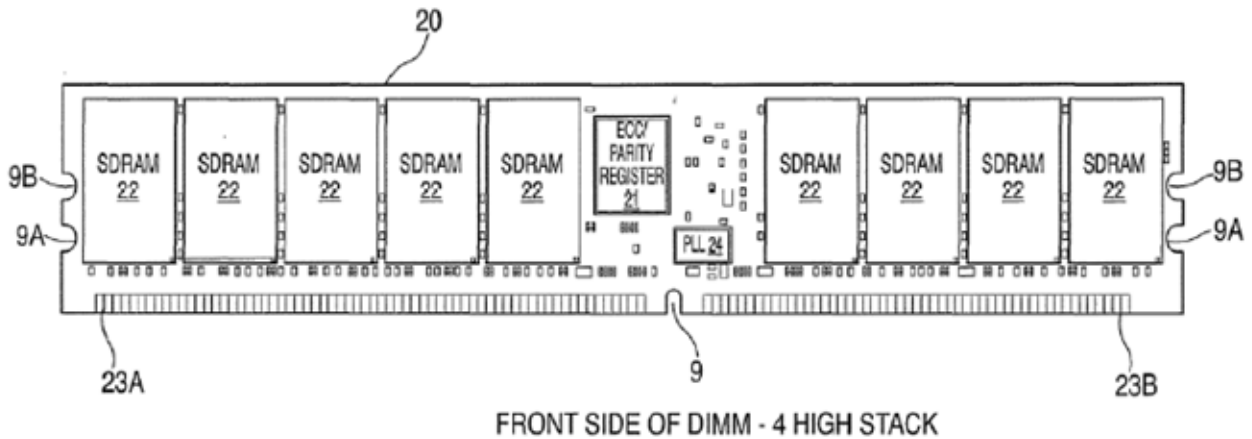


FIG. 3C

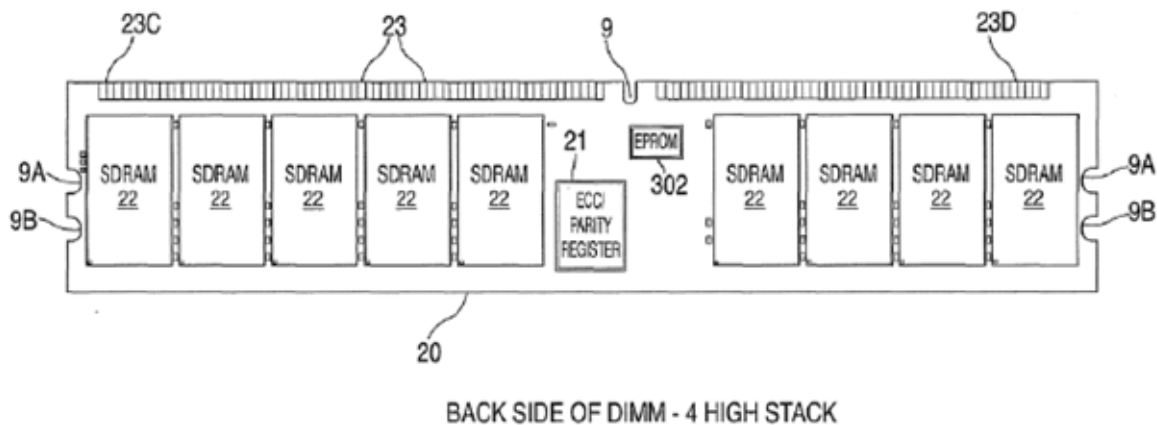


FIG. 3D

**g) [1.d.2] Communicate Data Signals**

Grounds 1-3 teach “dynamic random access memory elements [SDRAMs 22]...configured to communicate data signals [DATA, through lines 15] with the memory controller [Memory Controller 19] via the second edge connections [e.g., DQ0-DQ63] in accordance with the address and control signals.” EX1003, ¶¶246-252. The Board’s previous decisions confirm Ground 2 teaches equivalent

The diagram illustrates a memory system architecture. At the top, a DIMM (20) contains multiple SDRAM modules (22). A PLL (24) is connected to the SDRAM modules. An ECC/PARITY REGISTER (21) is also connected to the SDRAM modules. The DIMM is connected to a MEMORY INTERFACE CHIP (25) via a bus (15). The MEMORY INTERFACE CHIP (25) is connected to a MEMORY CONTROLLER OR PROCESSOR (19) via a bus (16). The MEMORY CONTROLLER OR PROCESSOR (19) is also connected to the MEMORY INTERFACE CHIP (25) via a bus (17). The MEMORY INTERFACE CHIP (25) is connected to the DIMM (20) via a bus (15a). The MEMORY CONTROLLER OR PROCESSOR (19) is connected to the MEMORY INTERFACE CHIP (25) via a bus (16a). The MEMORY CONTROLLER OR PROCESSOR (19) is also connected to the MEMORY INTERFACE CHIP (25) via a bus (17a). The MEMORY CONTROLLER OR PROCESSOR (19) is connected to the MEMORY INTERFACE CHIP (25) via a bus (15a). The MEMORY CONTROLLER OR PROCESSOR (19) is connected to the MEMORY INTERFACE CHIP (25) via a bus (16a). The MEMORY CONTROLLER OR PROCESSOR (19) is connected to the MEMORY INTERFACE CHIP (25) via a bus (17a).

FIG. 2

Those data signals are communicated “*via the second edge connections*” (blue) as discussed above. EX1014, Figs.2, 7A-7C (7A-B reproduced below, annotated), ¶¶[0015], [0035], [0038], [0041]; EX1003, ¶248.

| SERVER DIMM<br>PIN NUMBER PIN NAME | SERVER DIMM<br>PIN NUMBER PIN NAME |
|------------------------------------|------------------------------------|
| 1 Vref                             | 139 Vref                           |
| 2 SCL                              | 140 SCL                            |
| 3 SDA                              | 141 SDA                            |
| 4 UE                               | 142 UE                             |
| 5 CE                               | 143 CE                             |
| 6 VDD                              | 144 VDD                            |
| 7 ECCMODE                          | 145 ECCMODE                        |
| 8 DLY CKE/ODT                      | 146 DLY CKE/ODT                    |
| 9 CS GATE EN                       | 147 CS GATE EN                     |
| 10 GND                             | 148 GND                            |
| 11 DQ0                             | 149 DQ4                            |
| 12 DQ1                             | 150 DQ5                            |
| 13 GND                             | 151 GND                            |
| 14 DQS0*                           | 152 DQS9                           |
| 15 DQS0                            | 153 DQS9*                          |
| 16 GND                             | 154 GND                            |
| 17 DQ2                             | 155 DQ6                            |
| 18 DQ3                             | 156 DQ7                            |
| 19 GND                             | 157 GND                            |
| 20 VDD                             | 158 VDD                            |
| 21 GND                             | 159 GND                            |
| 22 DQ8                             | 160 DQ12                           |
| 23 DQ9                             | 161 DQ13                           |
| 24 GND                             | 162 GND                            |
| 25 DQS1*                           | 163 DQS10                          |
| 26 DQS1                            | 164 DQS10*                         |
| 27 GND                             | 165 GND                            |
| 28 DQ10                            | 166 DQ14                           |
| 29 DQ11                            | 167 DQ15                           |
| 30 GND                             | 168 GND                            |
| 31 DQ16                            | 169 DQ20                           |
| 32 DQ17                            | 170 DQ21                           |
| 33 GND                             | 171 GND                            |
| 34 DQS2*                           | 172 DQS11                          |
| 35 DQS2                            | 173 DQS11*                         |
| 36 GND                             | 174 GND                            |
| 37 DQ18                            | 175 DQ22                           |
| 38 DQ19                            | 176 DQ23                           |
| 39 GND                             | 177 GND                            |
| 40 RESET                           | 178 RESET                          |
| 41 VDD                             | 179 VDD                            |
| 42 GND                             | 180 GND                            |
| 43 DQ24                            | 181 DQ28                           |
| 44 DQ25                            | 182 DQ29                           |
| 45 GND                             | 183 GND                            |
| 46 DQS3*                           | 184 DQS12                          |
| 47 DQS3                            | 185 DQS12*                         |
| 48 GND                             | 186 GND                            |
| 49 DQ26                            | 187 DQ30                           |
| 50 DQ27                            | 188 DQ31                           |
| 51 GND                             | 189 GND                            |
| 52 CB0                             | 190 CB4                            |

FIG. 7A

|               |            |
|---------------|------------|
| 53 CB1        | 191 CB5    |
| 54 GND        | 192 GND    |
| 55 DQS8*      | 193 DQS17  |
| 56 DQS8       | 194 DQS17* |
| 57 GND        | 195 GND    |
| 58 CB2        | 196 CB6    |
| 59 CB3        | 197 CB7    |
| 60 GND        | 198 GND    |
| 61 VDD        | 199 VDD    |
| 62 CKE1       | 200 CKE1   |
| 63 CHKBT4     | 201 CHKBT1 |
| 64 CHKBT5     | 202 CHKBT3 |
| 65 CKE0       | 203 CKE0   |
| 66 VDD        | 204 VDD    |
| 67 A15        | 205 A14    |
| 68 BA2        | 206 A12    |
| 69 CHKBT0/PTY | 207 A9     |
| 70 A11        | 208 CHKBT2 |
| 71 VDD        | 209 VDD    |
| 72 A7         | 210 A8     |
| 73 A5         | 211 A6     |
| 74 A4         | 212 A3     |
| 75 A2         | 213 A1     |
| 76 VDD        | 214 VDD    |
| 77 CK0        | 215 CK0    |
| 78 CK0B       | 216 CK0B   |
| 79 VDD        | 217 VDD    |
| 80 GND        | 218 GND    |
| 81 VDD        | 219 VDD    |
| 82 A10        | 220 A0     |
| 83 BA0        | 221 BA1    |
| 84 WE         | 222 RAS    |
| 85 VDD        | 223 VDD    |
| 86 CS0        | 224 CS0    |
| 87 CAS        | 225 CS3    |
| 88 ODT0       | 226 ODT0   |
| 89 CS3        | 227 A13    |
| 90 VDD        | 228 VDD    |
| 91 CS1        | 229 CS1    |
| 92 ODT1       | 230 ODT1   |
| 93 CS2        | 231 CS2    |
| 94 VDD        | 232 VDD    |
| 95 GND        | 233 GND    |
| 96 DQ32       | 234 DQ36   |
| 97 DQ33       | 235 DQ37   |
| 98 GND        | 236 GND    |
| 99 DQS4*      | 237 DQS13  |
| 100 DQS4      | 238 DQS13* |
| 101 GND       | 239 GND    |
| 102 DQ34      | 240 DQ38   |

FIG. 7B

Moreover, JEDEC, Buchmann, and Wang disclose improvements to Hazelzet's data communication, including buffering the data signals as discussed above (pp.46-49). In each combination, the data buffering circuitry is implemented on Hazelzet's memory module between the “second edge connections” and the module’s SDRAMs, to communicate data with the memory controller in accordance with the address and control signals of the normal read and write operations. *Id.*; EX1003, ¶¶248-249.

For example, Wang discloses communicating data signals through Wang's interface circuit using the system data signal interface 274 (blue, coupled to the memory controller at the bottom of Figure 2C) and the memory data signal interface 278 (blue, coupled to one or more memory devices at the top of Figure 2C), in accordance with the address and control signals (green) corresponding to normal memory read and write operations. EX1090, Figs.2C (below), & 4D (below, illustrating processing data (blue) and address and command (green) signals for normal read and write operations through the interface).

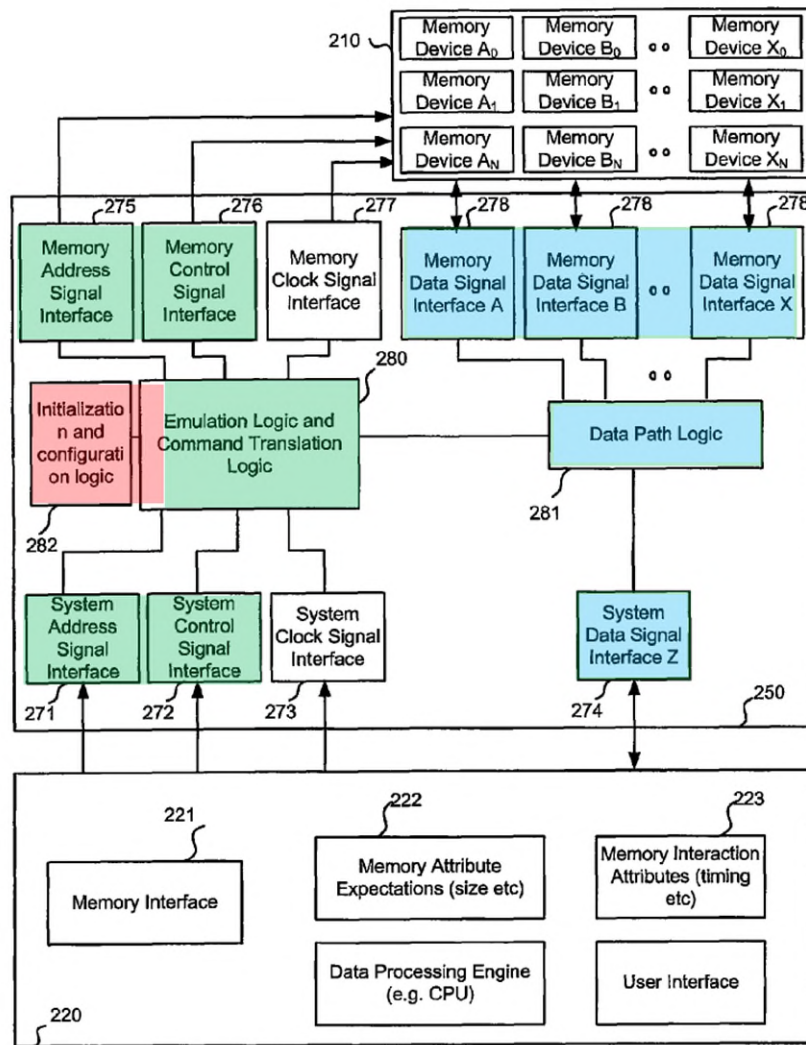


FIG. 2C

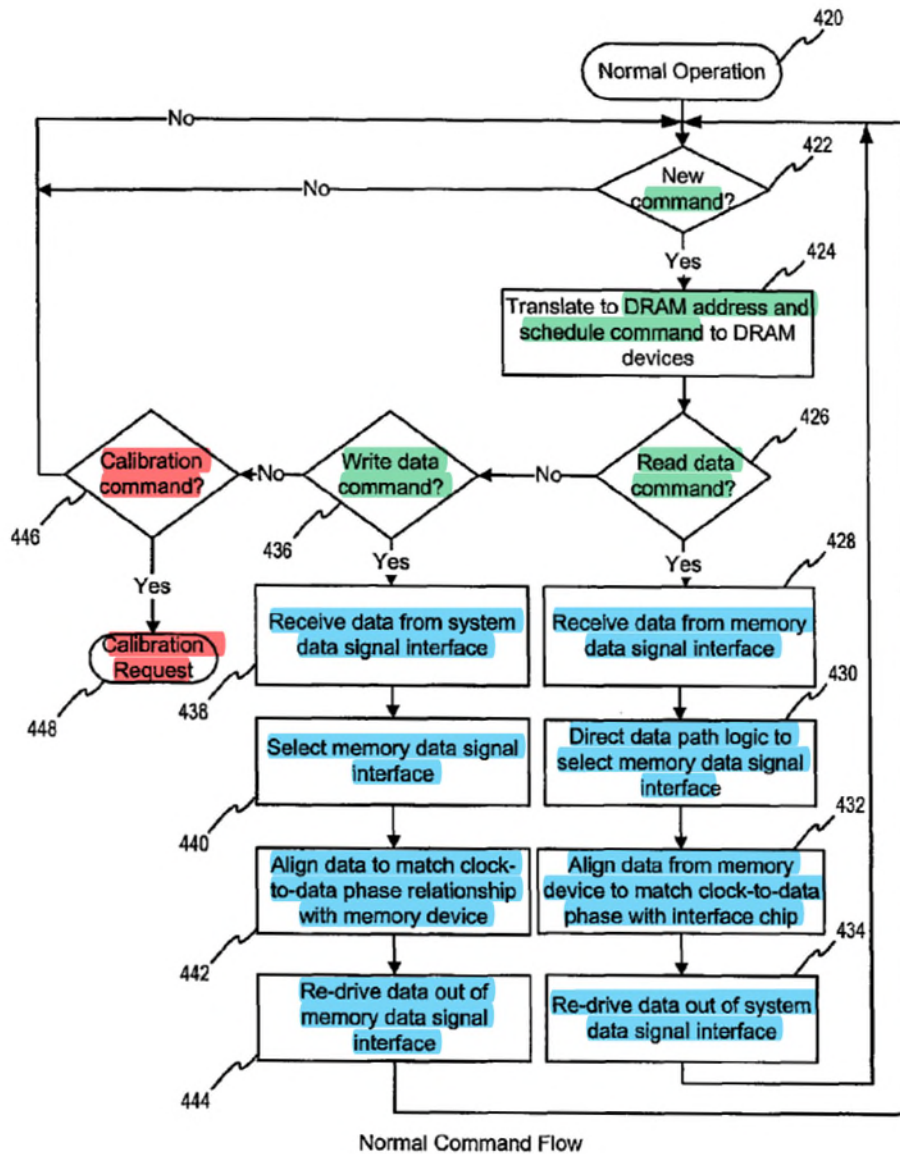


FIG. 4D

Wang's teaching of achieving higher capacity and parallelism in an infrastructure-compatible system without the cost of idle cycles would have further motivated using the functionality of Wang's interface circuit in Hazelzet's system. *Id.* 8:1-:10; EX1003, ¶250.

JEDEC's disclosure that the "LRDIMM...Memory Buffer (MB) buffers both address and data...[and] is intended to function in all RDIMM platforms with appropriate BIOS changes" would have also motivated a POSITA to upgrade Hazelzet's RDIMM to an LRDIMM. EX1036, p.5. Buchmann also discloses the details of communicating data with the memory controller through a buffer using its Memory Device Data Interface (blue) according to address and control signals provided by its Memory Hub Control (green). EX1016, Fig.16 (below), 21:20-:60; EX1003, ¶251.

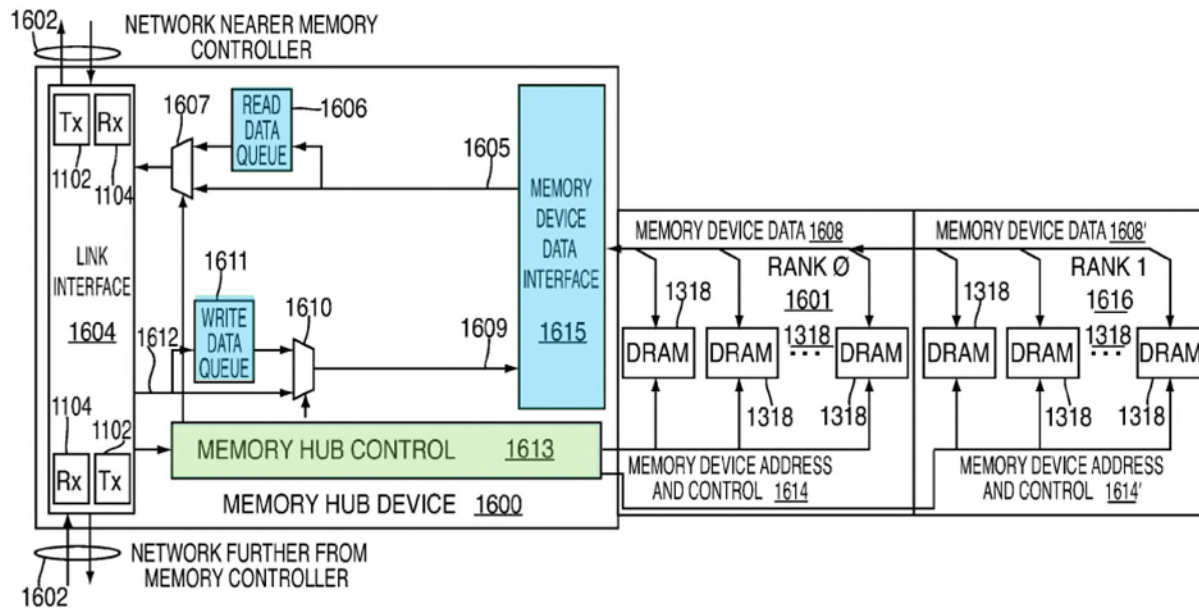


FIG. 16

Accordingly, Hazelzet alone or in combination with JEDEC, Buchmann, or Wang discloses these limitations. EX1003, ¶252.

***h) [1.e.1] Transistor***

Grounds 1-3 teach “*wherein the module controller includes a transistor having an open drain [Hazelzet’s open-drain output, see claim [1.b.2] (pp.59-61)] coupled to the error edge connection [see, e.g., EX1014, FIGS. 4B, 7A (below)], a source coupled to ground, and a gate.*” EX1003, ¶¶46-54, 253-272. The Board’s previous decisions confirm Ground 2 teaches equivalent limitations in ’623 claims [1.d] and 7-8, ’218 claims [1.d] and 3-4, and ’595 claims [1.d] and 3-4. EX1003, ¶¶153-155, 253; EX1034, 9-21; EX1102, 46-47, 62-64; EX1103, 45-46, 66-69.

As explained above (pp.59-61), Hazelzet discloses that the “ECC/Parity register” (in the “*module controller*”) has an open-drain output (UE, red), “*coupled to the error edge connection,*” which includes “*a transistor having an open drain..., a source coupled to ground and a gate*” as discussed above (pp.17-22). EX1014, Figs.4B, 7A (below); EX1003, ¶254.

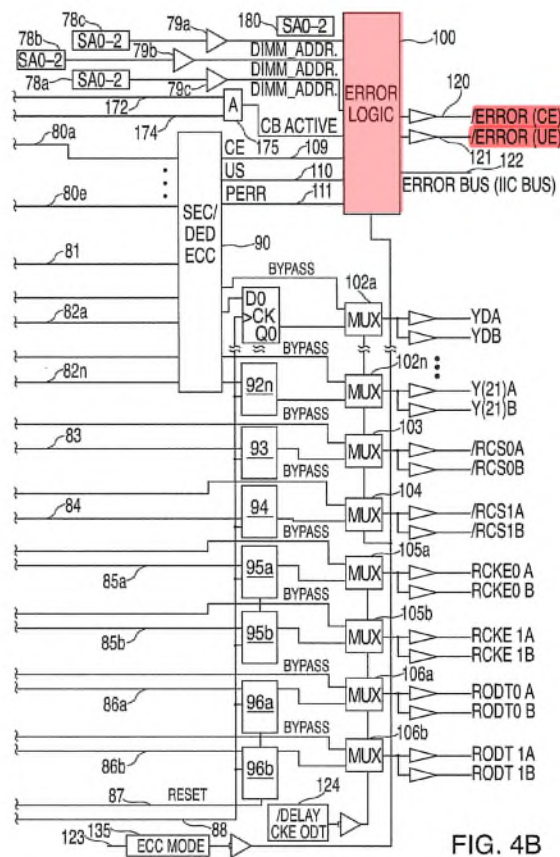


FIG. 4B

| SERVER DIMM<br>PIN NUMBER | PIN NAME    | SERVER DIMM<br>PIN NUMBER | PIN NAME    |
|---------------------------|-------------|---------------------------|-------------|
| 1                         | Vref        | 139                       | Vref        |
| 2                         | SCL         | 140                       | SCL         |
| 3                         | SDA         | 141                       | SDA         |
| 4                         | UE          | 142                       | UE          |
| 5                         | CE          | 143                       | CE          |
| 6                         | VDD         | 144                       | VDD         |
| 7                         | ECCMODE     | 145                       | ECCMODE     |
| 8                         | DLY CKE/ODT | 146                       | DLY CKE/ODT |
| 9                         | CS GATE EN  | 147                       | CS GATE EN  |
| 10                        | GND         | 148                       | GND         |
| 11                        | DQ0         | 149                       | DQ4         |
| 12                        | DQ1         | 150                       | DQ5         |
| 13                        | GND         | 151                       | GND         |
| 14                        | DQS0*       | 152                       | DQS9        |
| 15                        | DQS0        | 153                       | DQS9*       |
| 16                        | GND         | 154                       | GND         |
| 17                        | DQ2         | 155                       | DQ6         |
| 18                        | DQ3         | 156                       | DQ7         |
| 19                        | GND         | 157                       | GND         |
| 20                        | VDD         | 158                       | VDD         |
| 21                        | GND         | 159                       | GND         |
| 22                        | DQ8         | 160                       | DQ12        |
| 23                        | DQ9         | 161                       | DQ13        |
| 24                        | GND         | 162                       | GND         |
| 25                        | DQS1*       | 163                       | DQS10       |
| 26                        | DQS1        | 164                       | DQS10*      |
| 27                        | GND         | 165                       | GND         |
| 28                        | DQ10        | 166                       | DQ14        |
| 29                        | DQ11        | 167                       | DQ15        |
| 30                        | GND         | 168                       | GND         |
| 31                        | DQ16        | 169                       | DQ20        |
| 32                        | DQ17        | 170                       | DQ21        |
| 33                        | GND         | 171                       | GND         |
| 34                        | DQS2*       | 172                       | DQS11       |
| 35                        | DQS2        | 173                       | DQS11*      |
| 36                        | GND         | 174                       | GND         |
| 37                        | DQ18        | 175                       | DQ22        |
| 38                        | DQ19        | 176                       | DQ23        |
| 39                        | GND         | 177                       | GND         |
| 40                        | RESET       | 178                       | RESET       |
| 41                        | VDD         | 179                       | VDD         |
| 42                        | GND         | 180                       | GND         |
| 43                        | DQ24        | 181                       | DQ28        |
| 44                        | DQ25        | 182                       | DQ29        |
| 45                        | GND         | 183                       | GND         |
| 46                        | DQS3*       | 184                       | DQS12       |
| 47                        | DQS3        | 185                       | DQS12*      |
| 48                        | GND         | 186                       | GND         |
| 49                        | DQ26        | 187                       | DQ30        |
| 50                        | DQ27        | 188                       | DQ31        |
| 51                        | GND         | 189                       | GND         |
| 52                        | CB0         | 190                       | CB4         |

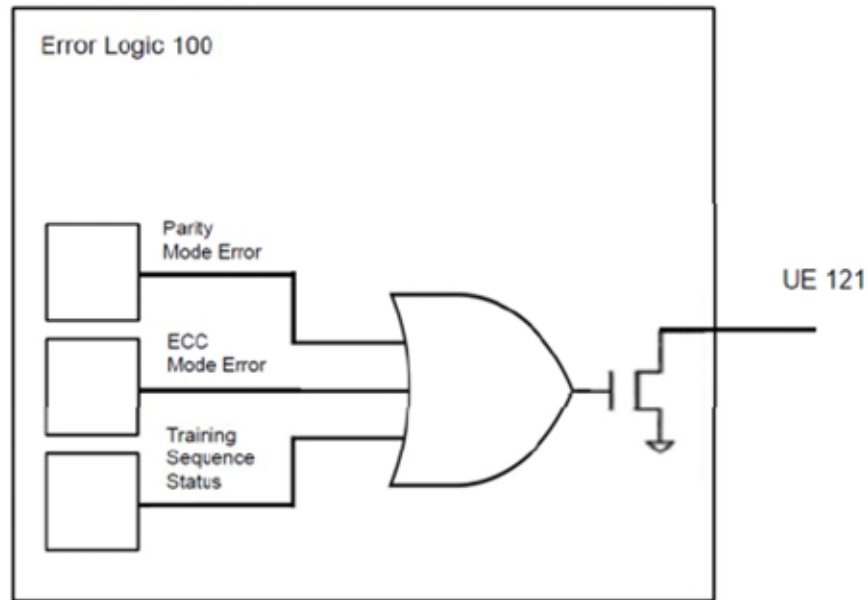
FIG. 7A

Hazelzet's "ECC/Parity register" has open-drain outputs, including UE 121 to notify the system memory controller of uncorrectable and parity errors. EX1014, ¶¶[0044], [0059], [0072], Fig.4B; EX1003, ¶255. Hazelzet's "***open-drain outputs***...permit multiple modules to share a common signal line for reporting an error" and "depending on the mode selected," report "an uncorrectable ECC error or a parity error." EX1014, ¶[0072]. Hazelzet's open-drain output is driven "low" (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage, turning on the transistor) and "[is] permitted to return to an un-driven state

(high impedance)” when the “driver [is] disabled” (i.e., gate receives a low/ground voltage, turning off the transistor). EX1014, ¶¶0099; EX1003, ¶¶256, 267.

As discussed above (pp.17-22), a POSITA would have understood “open drain output” in Hazelzet’s context to mean an output that is driven by a field effect transistor (FET), having three terminals (gate, source, and drain), the drain being connected to the output, the source to ground, and the gate to a logic element that performed, e.g., an OR operation, to select an error signal to drive the gate, as depicted in Kim’s Figure 5. EX1017, Figs.4-5, 5:49-:57, 4:40-:48, 5:65-6:18; EX1020 (FET structure); *supra* pp.51-55; EX1003, ¶¶46-54, 257-258. A POSITA would have also found it obvious to implement Hazelzet in this fashion. *Id.*

Indeed, Hazelzet’s output UE 121 is used in both Parity Mode and ECC Mode, necessitating circuitry within Error Logic 100 for selecting which signal to drive the open-drain output. An OR gate may be used for that function (as in Kim, *infra* pp.107-112) or a multiplexor or similar selection circuitry, each of which would have been obvious to a POSITA. EX1003, ¶263. In case of an OR-gate implementation, each signal input to the OR gate would remain low when the module was not in its associated mode, and the signal whose mode was active could be high to indicate the occurrence of the event to be signaled (error in Parity Mode or ECC Mode; ongoing training in Training Mode), or low to indicate that the event is not occurring (Parity/ECC) or acknowledge/completed (training):



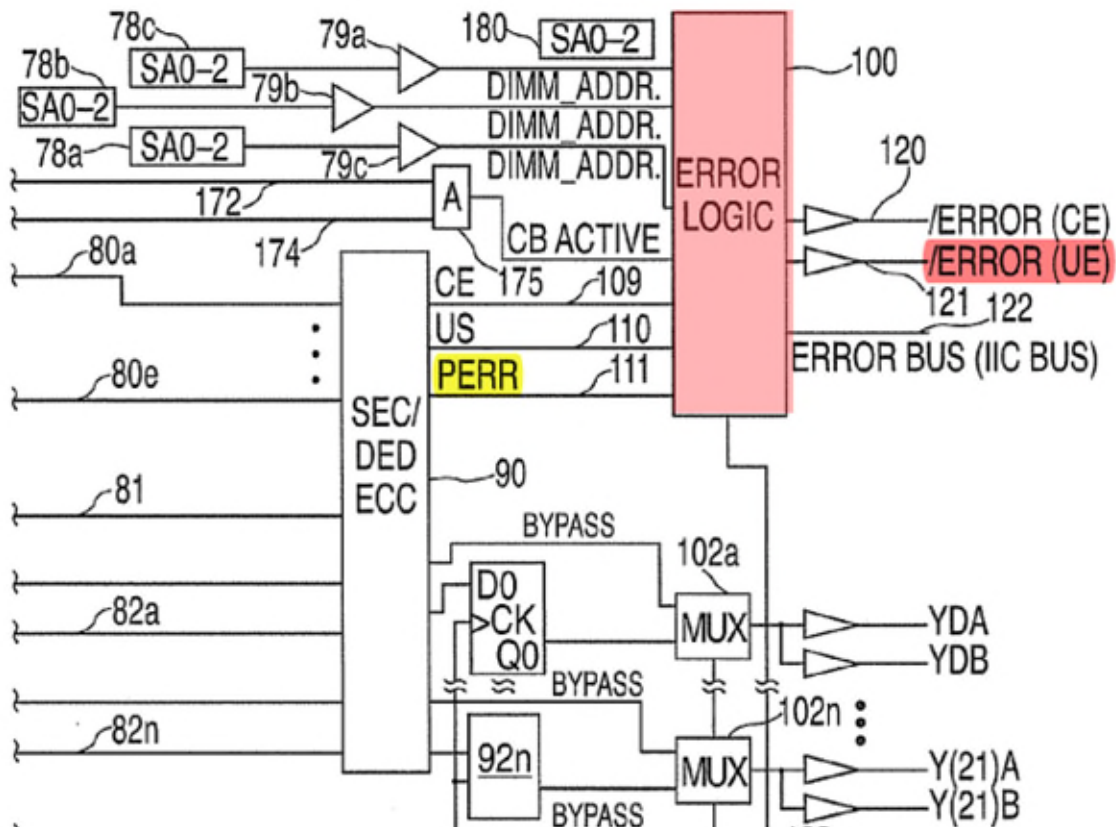
EX1003, ¶261. The signal whose mode was active would be passed through the OR gate to drive the gate of the transistor having an open drain. EX1003, ¶264.

**i) [1.e.2] Indicate Parity Error**

Grounds 1-3 teach “*wherein the module controller is configured to apply a first signal to the gate of the transistor to indicate a parity error having occurred when the memory module is being accessed for a normal memory read or write operation.*” EX1003, ¶¶273-279. The Board’s previous decisions confirm Ground 2 teaches equivalent limitations in ’623 claims [1.b], 2, 7, and 9, ’218 claims [1.f], [1.h] and 5, and ’595 claims [1.e.ii], [1.f.iii] and 5. EX1003, ¶¶153-155, 273; EX1034, 9-21; EX1102, 47-52, 62-63; EX1103, 46-47, 50, 69-71.

As discussed for [1.e.1] (pp.77-80), Hazelzet discloses that its “ECC/Parity register” (in the “*module controller*”) has open-drain output UE 121 to indicate a parity error. EX1014, ¶¶[0059], [0070], [0072], [0076]; EX1003, ¶¶253-272.

When in “parity mode,” the memory module’s “parity generator/checker circuit 231” (within SEC/DED ECC circuit 90) generates and sends “parity error signal (PERR)” to “error logic circuit” 100. EX1014, Figs.4B, 5 (both below), 8 (further below), ¶¶[0018], [0059], [0070], [0072], [0076]; EX1003, ¶¶274-275.



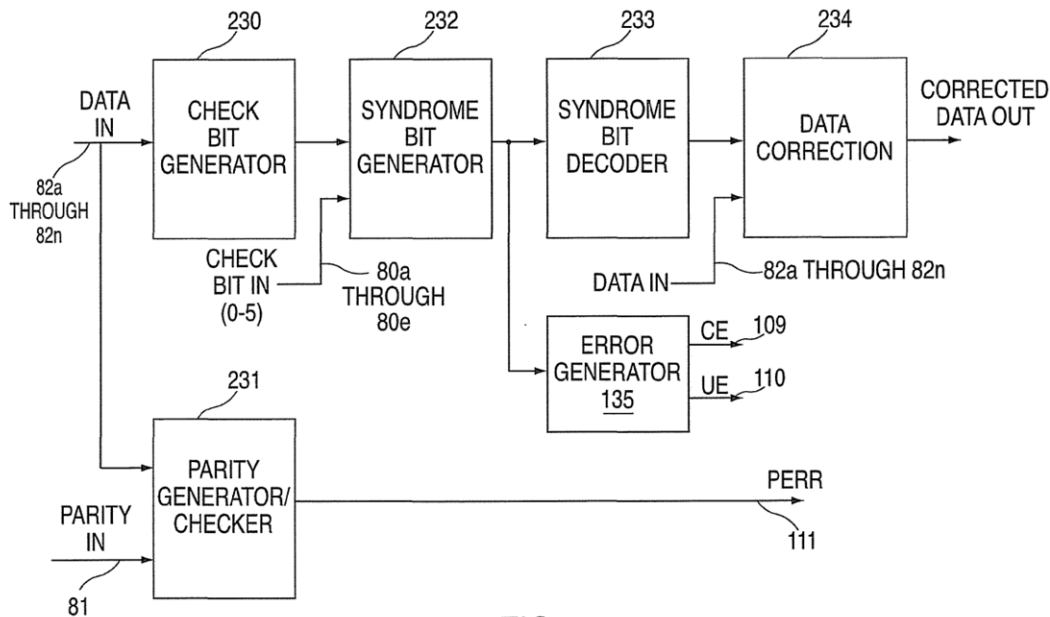
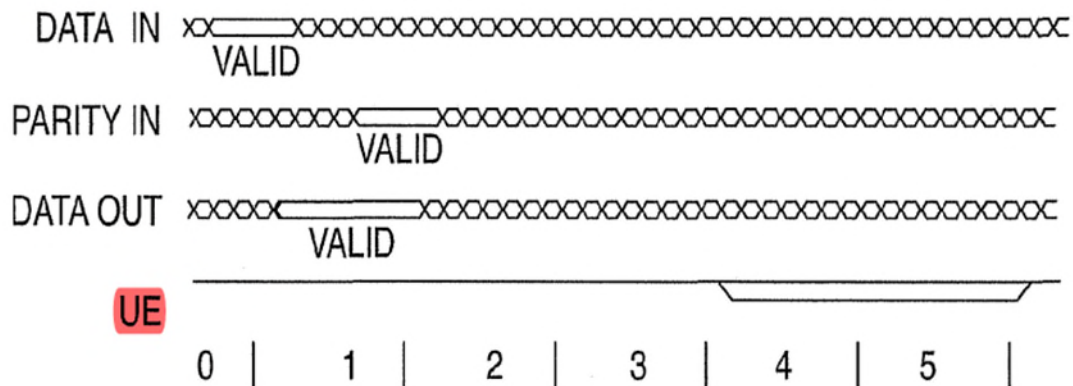


FIG. 5

### PARITY MODE



NOTES: CS GATING DISABLED

PARITY IN AND CHECK BIT 0 SHARE A COMMON PIN (CHK0/ PARITY\_IN)

IF AN ERROR OCCURS, CE OR UE ARE DRIVEN LOW

FIG. 8

Moreover, as discussed for [1.e.1] (pp.77-80), Hazelzet's open-drain output is driven "low" when the driver is enabled, and its open-drain "output [is]

permitted to return to an un-driven state (high impedance)” when the “driver [is] disabled.” EX1014, ¶[0099]; EX1003, ¶¶253-272. Thus, a high voltage applied to the transistor’s gate drives the open-drain output low, indicating a parity error in the “parity” mode. EX1003, ¶¶46-54, 267, 276. Hazelzet’s “parity” mode allows the host system to “determine the error condition” of the memory module, which is reported to the host “via the Uncorrectable Error (UE) line” by driving it “low, i.e., ‘0’,” when “an error is detected.” EX1014, ¶¶[0064], [0070], [0099], ¶[0018], Fig.8 (illustrating that UE is driven low “if an error occurs” in the “parity mode”); EX1003, ¶277.

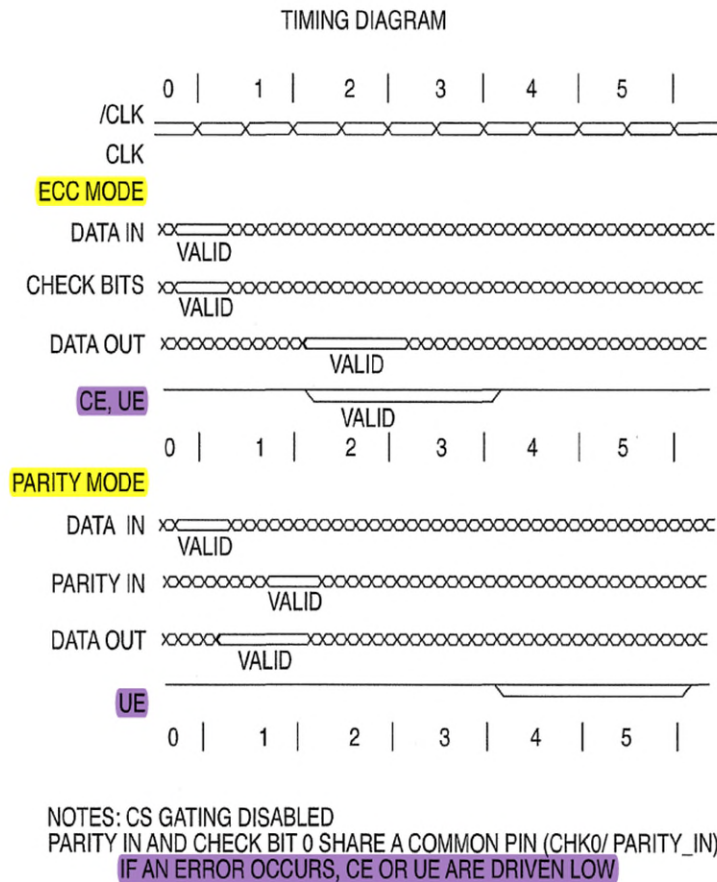
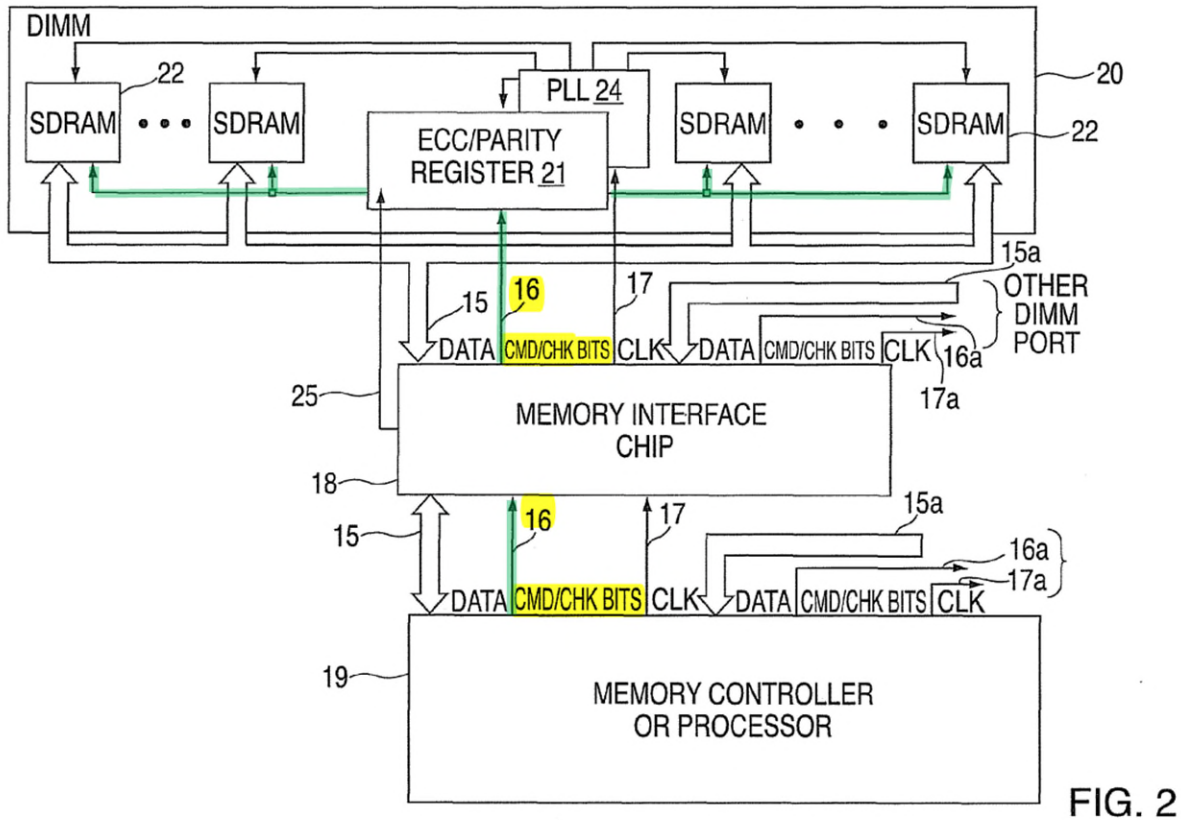


FIG. 8

Hazelzet's parity error signal is related to the received address and command signals. EX1014, ¶¶[0018] ("Parity error reporting...one cycle after the address and command"), [0099] (similar), [0072], Fig.2 (reproduced below, showing ECC/Parity Register 21 receiving address and command signals on line 16 and the corresponding check bits on line 25), ¶[0038].



A POSITA would have understood that normal memory read and write operations are initiated by a valid command (with a low chip select signal) using such address and command signals, *see, e.g.*, EX1056, p.33; EX1014, ¶[0109], meaning that Hazelzet's parity reporting based on such signals indicate a parity error “*having occurred when the memory module is being accessed for a normal memory read or write operation.*” EX1003, ¶¶278-279.

**j) [1.e.3] Training Sequences**

Grounds 1-3 teach “*wherein the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one*

*or more training sequences and when the dynamic random access memory elements are not accessed for any normal memory read or write operations.”*

EX1003, ¶¶280-289. The Board’s previous decisions confirm Ground 2 teaches equivalent limitations in ’623 claims [1.c], 2, and 8, ’218 claims [1.e.ii], [1.f], [1.i], 4, and 7, and ’595 claims [1.e.iii] and 7. EX1003, ¶¶153-155, 280; EX1034, 9-21; EX1102, 47-50, 63-64, 67-68; EX1103, 47-48, 73-74.

In the proposed combinations, Hazelzet’s open-drain output is configured such that the output is driven low (to ground) during “*one or more training sequences*” (e.g., MB-DRAM, TS0/TS3, or Wang’s interface training) by applying to the gate of the transistor a “*second signal*” which is “high” during the training, and the open-drain output would be in a high-impedance state (allowing a pull-up resistor to pull the voltage at the output “high”) after completing the respective training by applying to the gate of the transistor a “*second signal*” which is “low,” as discussed above (pp.17-22, 51-55). EX1003, ¶¶211-220, 281-282. Thus, Hazelzet alone or in combination with JEDEC or Buchmann or Wang renders obvious that “*the module controller is further configured to apply a second signal related to one or more training sequences to the gate of the transistor when the memory module performs operations associated with the one or more training sequences.*”

As also discussed above (pp.49-51), each combination further renders obvious that, while the module performs training-related operations, “*the dynamic random access memory elements are not accessed for any normal memory read or write operations.*” EX1003, ¶¶209-210. JEDEC, for example, expressly teaches that during training performed by the memory module, the memory devices are not accessed for any normal memory read or write operations since “[n]o DRAM commands....over the Command/Address and Control buses...can be issued to the MB until...training is complete.” EX1015, 8; EX1056, pp.33-34, pp.56-76; EX1024, p.13, pp.17-45; EX1056, 42-45 (Write leveling performed without any normal read/write operations), 48-51 (MPR for read calibration, similar); EX1003, ¶283. Buchmann also teaches training during power-on initialization, before normal operations, as discussed above (pp.49-51). EX1003, ¶¶209-210, 284; EX1016, Abstract (power-on and initialization training), 5:51-6:50 (TS0 training during initialization), 8:24-9:18 (TS3 training during initialization), 6:25-:50 (TABLE 2 listing Clock Detection and Repair Training States without any normal memory operations), 8:50-9:15 (TABLE 6 listing US Lane Training and Repair Training States without any normal memory operations). Wang similarly teaches that the module returns to normal operations only after training the memory interfaces is complete (Steps 408 and 410 below). EX1090, Fig.4C (below), 9:58-

:67 (training repeated for all interfaces until complete as shown in Steps 408-412 below).

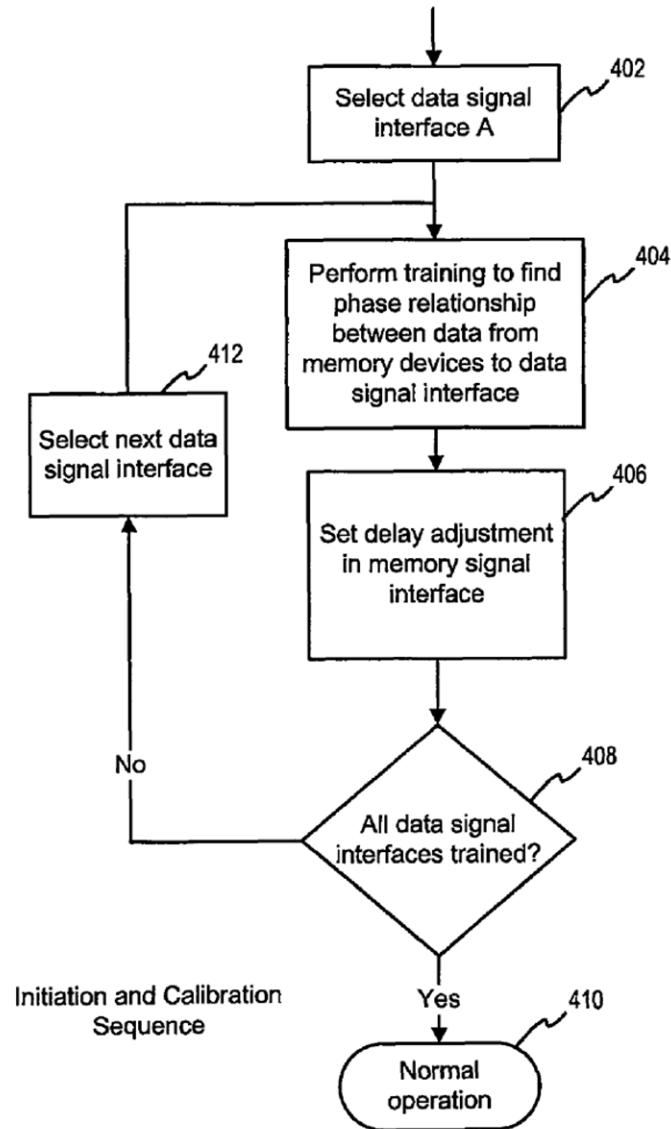


**FIG. 4C**

Wang also teaches that the normal memory read and write operations (426 and 436, green below) are separate and distinct from the training, which is performed

in response to a calibration command (red below). EX1090, Fig.4D (below), 11:1-9.

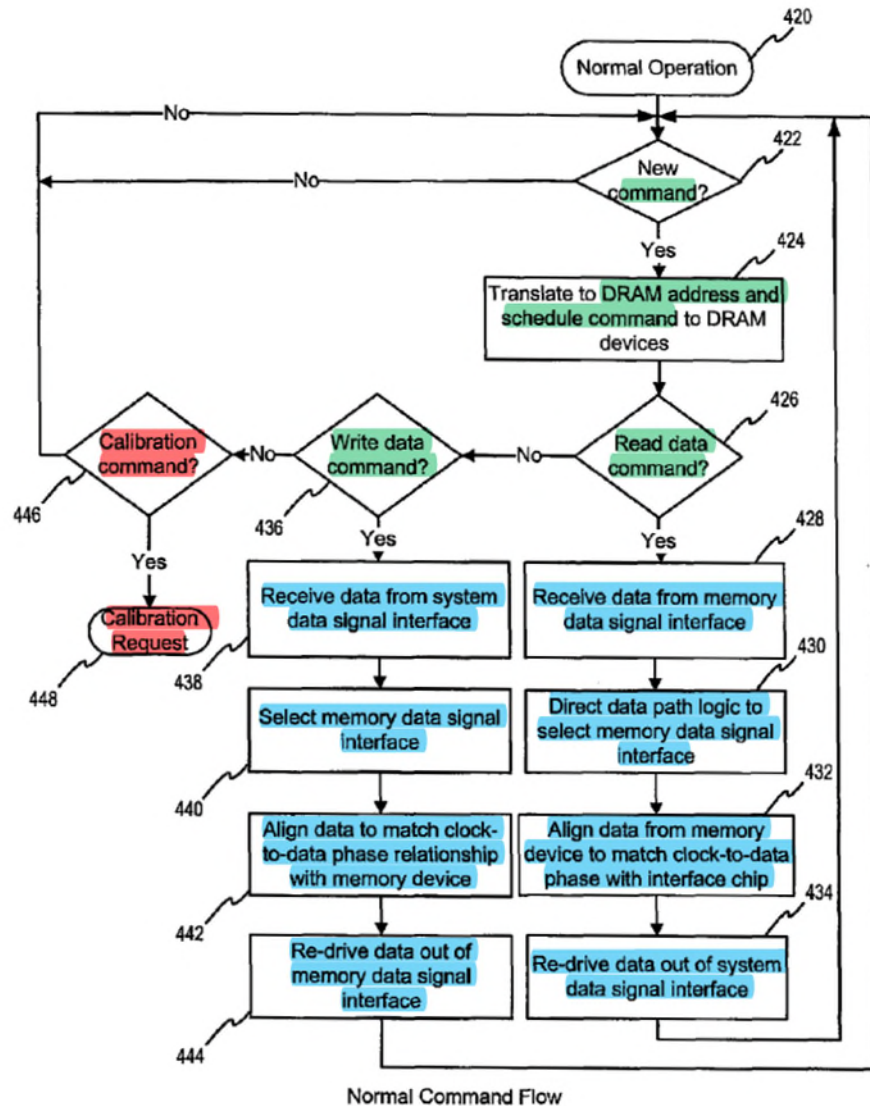


FIG. 4D

Wang's training is performed by initialization and configuration logic 282 (red) in interface circuit 250 in response to a memory controller's "Calibrate" command. *Id.*, Fig.2C (below). As Wang discloses using DDR3 SDRAMs, *id.*, 4:1-9, 5:37-43, a POSITA would have understood that Wang's interface training

for DDR3 memories can be performed using standard Write Leveling and MPR modes, without any normal read/write operations, as well-known in the field at the time. EX1056 (JESD79-3C), pp.40-45, 48-54; EX1003, ¶¶70, 190, 285.

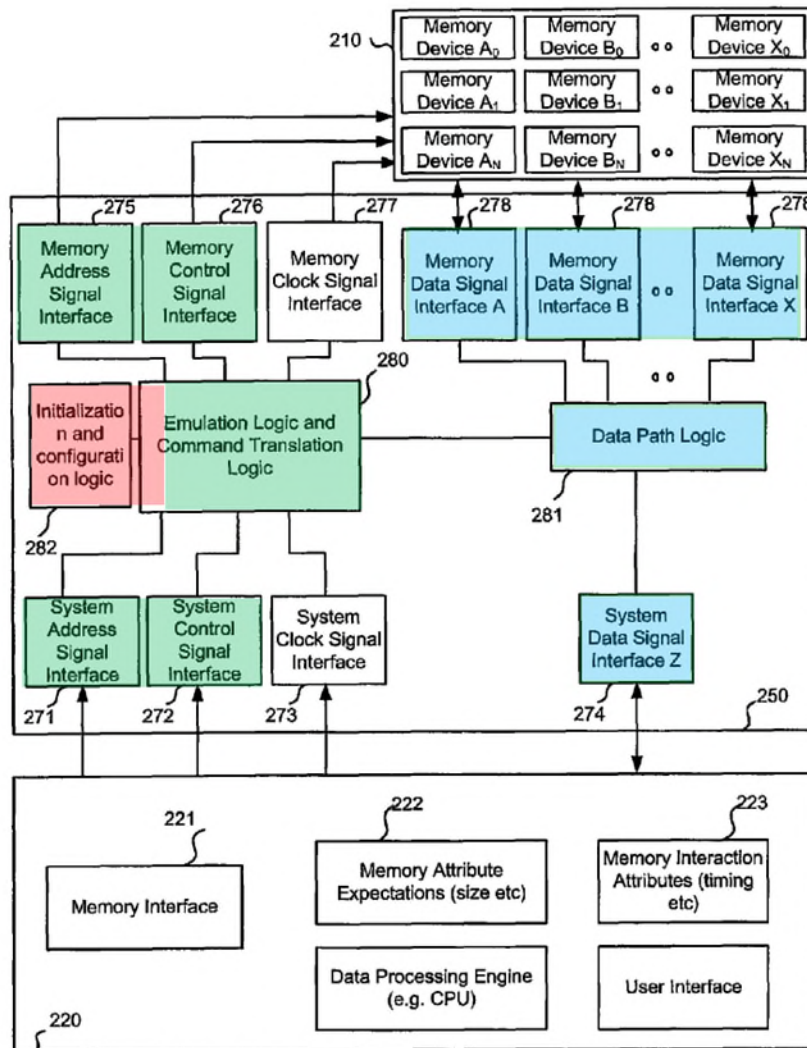


FIG. 2C

Thus, as discussed above (pp.51-55), a POSITA would have been motivated to use Hazelzet's open-drain output to indicate training completion to the controller and the return to the normal memory read and write operations as taught by

JEDEC, Buchmann, and Wang. EX1003, ¶¶211-220. A POSITA would have understood that Hazelzet's UE pin is available to report the status of training, since the memory module cannot be accessed for normal read or write operations during the training, so there is no need for the UE pin to indicate parity (or ECC) errors in the received commands as in normal mode. EX1014, ¶[0122]. Thus, a POSITA would have been motivated to use the UE pin for other purposes, such as reporting training status to the controller, as discussed above (pp.51-55). Indeed, a POSITA would have known about the JEDEC proposal which expressly teaches using the ERROUT# pin to signal completion of training. EX1015, pp. 3, 8; EX1003, ¶286.

Similarly, Buchmann teaches that, during TS0 training for example, the address/control and data signals are not used for normal memory read and write operations because TS0 training involves training of the "clock" itself, and no address/control or data signals are transmitted between the host and the memory module. EX1016, 5:51-7:2. It therefore would have been obvious to use Hazelzet's open-drain output to convey a TS\_done or similar signal to indicate training completion as discussed above (pp.43-44). EX1003, ¶¶187-192. A POSITA would have been motivated to use Hazelzet's open-drain output to indicate to the memory controller training completion, so that the controller can perform the next training steps or to return to the normal memory operations. EX1003, ¶287.

Additionally, a POSITA would have found it obvious not to perform normal memory read and write operations using any data, control or address signals while the clock or clock-to-data relationships are being trained for the same reasons set forth above, e.g., to avoid unreliable operation during periods of clock instability or when the clock-to-data phase relationship is not established. EX1003, ¶288.

### 3. Claims 2-4

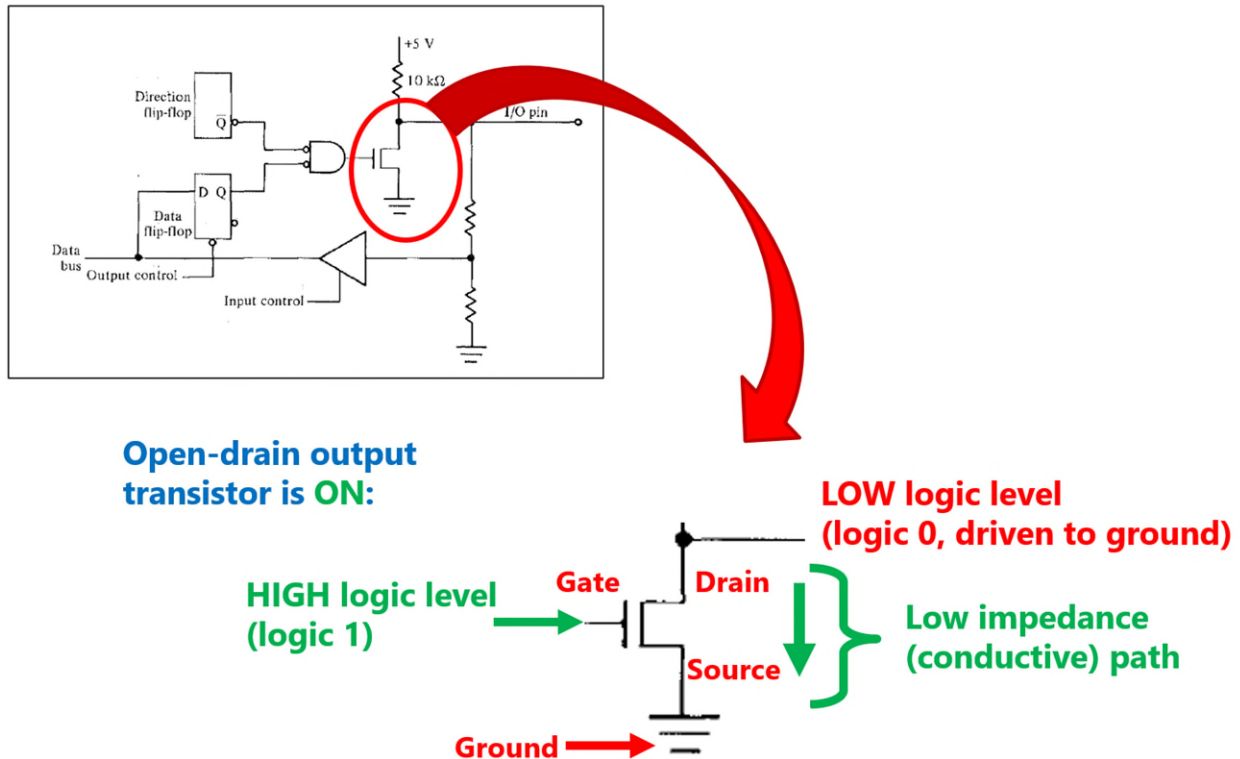
Consistent with the well-known operation of open-drain outputs (pp.17-22), Grounds 1-3 teach “[t]he memory module of claim 1, wherein the second signal drives the error edge connection from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state,” EX1003, ¶¶290-294, “[t]he memory module of claim 2, wherein the second signal drives the error edge connection from the high impedance state to the low logic level and from the low logic level to the high impedance state,” EX1003, ¶¶295-299, and “[t]he memory module of claim 2, wherein the second signal drives the gate of the transistor high so as to drive the error edge connection to the low logic level [e.g., conducting and connecting the drain to ground], and drives the gate of the transistor low [turning the transistor off] so as to drive the error edge connection to the high impedance state,” EX1003, ¶¶300-302. The Board’s previous decisions confirm Ground 2 teaches equivalent limitations (1) for Claim 2 in ’623 claim 8, ’218 claim 4, and

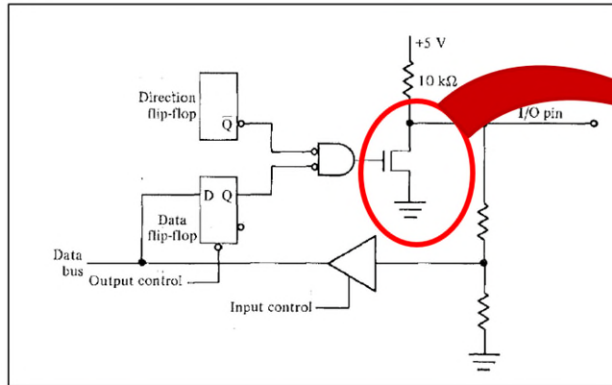
'595 claim [1.g] and 7, EX1003, ¶¶153-155, 290; EX1034, 20-21; EX1102, 63-64; EX1103, 50-52, 73-74, (2) for Claim 3 in '623 claim 8, '218 claim 4, and '595 claims [1.g] and 7, EX1003, ¶¶153-155, 295; EX1034, 20-21; EX1102, 63-64; EX1103, 50-52, 73-74, and (3) for Claim 4 in '623 claim 8, '218 claim 4, and '595 claims [1.g] and 7, EX1003, ¶¶153-155, 300; EX1034, 20-21; EX1102, 63-64; EX1103, 50-52, 73-74.

As discussed above (pp.17-22), the combinations' open-drain output is configured such that the output is driven to a “*low logic level*” (ground, “*first state*”) during training when the “*second signal drives the gate of the transistor high,*” turning the transistor on; and the output is in a “*high impedance state*” (“*second state*”) upon training completion when “*the second signal...drives the gate of the transistor low,*” turning the transistor off. EX1003, ¶¶46-54, 291, 296, 301.

Likewise, Hazelzet's open-drain output is driven “low” (to ground) when the driver is enabled, and is “permitted to return to an un-driven state (high impedance)” when the “driver [is] disabled.” EX1014, ¶[0099]. Thus, as discussed above (pp.51-55), a POSITA would have understood that Hazelzet used the known open-drain output, such as disclosed in Kim. EX1003, ¶¶211-220, 292, 297; EX1017, Figs. 4-5, 5:65-6:18. Thus, a POSITA would have known that the open-drain output, and connected edge connection, would be driven to ground

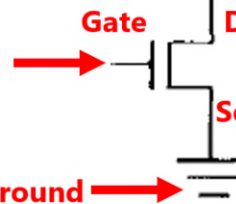
when the gate is driven high and would be in a high impedance state when the gate is driven low. EX1003, ¶¶46-54. This was decades-old technology. EX1089, 207-208 (Fig. 6.2, annotated below); EX1003, ¶¶293-294, 298-299, 302.





**Open-drain output  
transistor is OFF:**

**LOW logic level  
(logic 0)**



**High impedance state  
(voltage determined by  
external circuit)**

**High impedance  
(non-conductive) path**

#### 4. Claim 5

Grounds 1-3 teach “[t]he memory module of claim 4, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the error edge connection and ground.” EX1003, ¶¶303-307. The Board’s previous decisions confirm Ground 2 teaches equivalent limitations in ’623 claim 9, ’218 claim 5, and ’595 claim 5. EX1003, ¶¶153-155, 303; EX1034, 20-21; EX1102, 64-66; EX1103, 69-71.

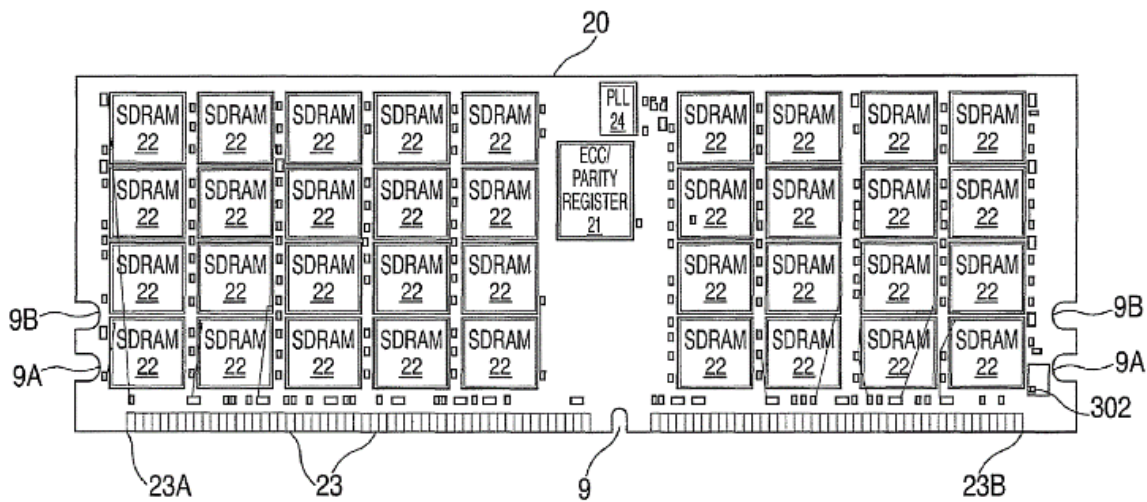
As discussed above with respect to [1.e.2] (pp.80-85), a high voltage applied to Hazelzet’s transistor’s gate turns the transistor “on” and provides a low impedance path between the error edge connection and ground, driving the open-

drain output low as discussed above (pp.17-22), indicating a parity error in the “parity” mode. The same principles apply here, when “*the first signal drives the gate of the transistor high*” to indicate a parity error. EX1014, ¶[0099]; EX1003, ¶¶303-307.

## 5. Claim 6

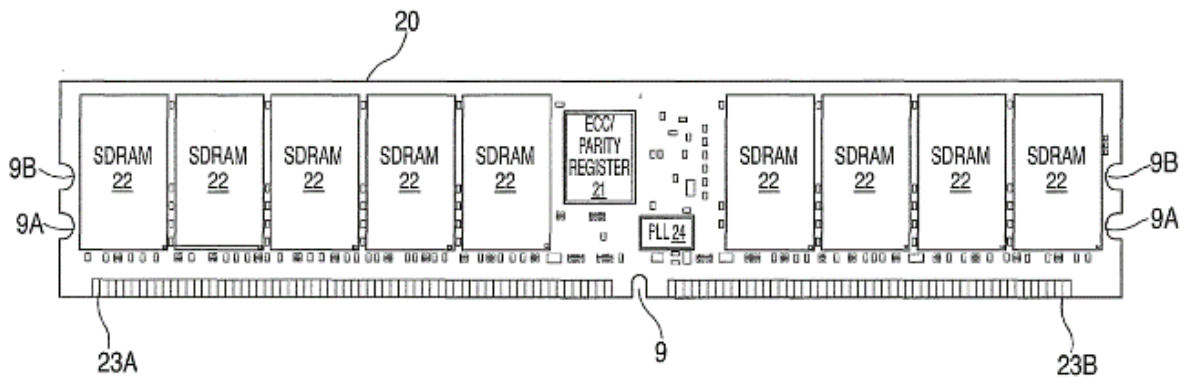
Grounds 1-3 teach “[t]he memory module of claim 1, wherein the module controller comprises an integrated circuit that includes the transistor [in Hazelzet’s “ECC/Parity register,” referred to as a “buffer chip,” EX1014, ¶[0038]].” EX1003, ¶¶308-310. The Board’s previous decisions confirm Ground 2 teaches equivalent limitations in ’623 claims 6-7, ’218 claims 2-3, and ’595 claims 2-3. EX1003, ¶¶153-155, 308; EX1034, 20-21; EX1102, 61-63; EX1103, 66-68.

As discussed above for [1.e.1] (pp.77-80), the claimed “*transistor*” is in Hazelzet’s “ECC/Parity register” (in the “*module controller*”), also called a “buffer chip.” EX1014 (Hazelzet) at ¶[0038]. Hazelzet explains that its module’s devices, including “buffers” (in the “*module controller*”), “registers,” and “PLL” may be comprised of “multiple separate chips” or “combined onto a single package or even ***integrated*** onto a single device,” e.g., as shown in Figures 3A-3D (ECC/Parity ICs in Figs. 3A and 3C below). EX1014, ¶[0115], Figs. 3A-3D, ¶[0039], ¶[0042].



FRONT SIDE OF DIMM - 72 PLANAR

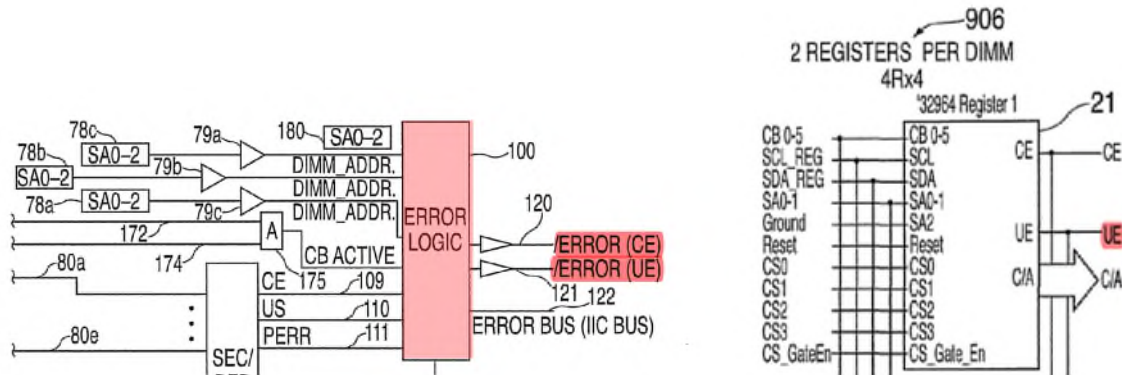
FIG. 3A



FRONT SIDE OF DIMM - 4 HIGH STACK

FIG. 3C

Specifically, Hazelzet's ECC/Parity buffer chip 21 includes error logic circuit 100 which generates the open-drain output UE. EX1014, ¶¶[0044], [0059], Fig.4B (below in part, on the left), Fig.9 (showing integrated circuits with respective UE output pins, below in part, on the right).



A POSITA would have understood from this disclosure that the module controller includes an integrated circuit, such as ECC/Parity buffer chip, which includes the transistor with the open-drain output UE. EX1003, ¶¶309-310.

## 6. Claim 7

Grounds 1-3 teach “[t]he memory module of claim 1, wherein the operation associated with the one or more training sequences are performed when the dynamic random access memory elements are not communicating data signals associated with any normal memory read or write operations [see [1.e.3] (pp.85-92), e.g., when operations associated with the training sequences are performed, EX1003, ¶¶280-289] with the memory controller via the second edge connections.” EX1003, ¶¶311-316. The Board’s previous decisions confirm Ground 2 teaches equivalent limitations in ’623 claims [1.c], [1.d], and 2, ’218 claims [1.e.ii], [1.f] and 7, and ’595 claims [1.e.iii] and 9. EX1003, ¶¶153-155, 311; EX1034, 9-21; EX1102, 47-50, 67-68; EX1103, 47-48, 74-75.

In Hazelzet-JEDEC, JEDEC explains that during MB-DRAM training (the training added to Hazelzet), “[n]o DRAM commands or control word writes...can be issued to the MB until the MB-DRAM Interface training is complete.” EX1015, 8. A POSITA would thus have understood that during such training, in the absence of “DRAM commands,” there would be no read or write operations, and no data signals would be communicated on the data pins. *Id.*; EX1003, ¶313.

Likewise in Hazelzet-Buchmann, the memory module can execute a training sequence (e.g., TS0 training, which involves training of the “clock”) in the SBC mode. EX1016, 5:51-7:2; *supra* pp.85-92 (claim [1.e.3]). Since this trains the “clock” itself, a POSITA would have understood that no “data” signals are transmitted between the host and the memory module during the TS0 training. EX1003, ¶314.

Similarly in Hazelzet-Wang, Wang’s training uses the memory devices’ data signal lines, rendering obvious that the memory devices are not accessed by the memory controller for normal read or write operations, meaning that no associated data is communicated through the “*second edge connections*.” *Supra* pp.85-92 (claim [1.e.3]); EX1003, ¶315.

**7. Claim 8**

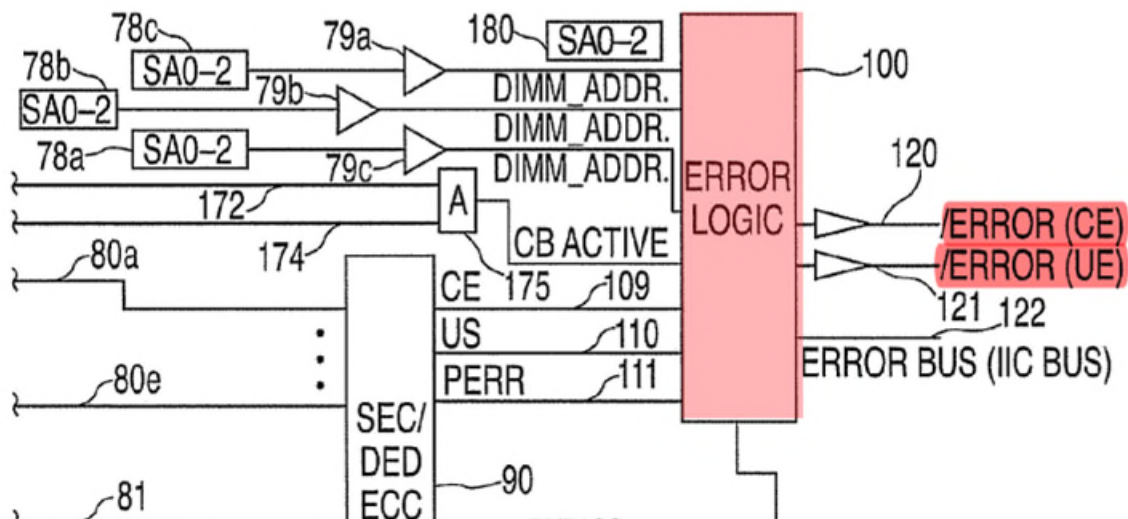
For reasons similar to those above for claim 7 (pp.98-99), Grounds 1-3 teach “[t]he memory module of claim 1, wherein the second edge connections are not active [e.g., when no data signals are communicated] during the operations associated with the one or more training sequences.” EX1003, ¶¶317-319. The Board’s previous decisions confirm Ground 2 teaches equivalent limitations in ’623 claims [1.c], [1.d], and 2, ’218 claims [1.e.ii], [1.f] and 7, and ’595 claims [1.e.iv] and 8. EX1003, ¶¶153-155, 317; EX1034, 9-21; EX1102, 47-50, 67-68; EX1103, 48, 74-75.

**8. Claim 9**

As explained for [1.e.3] (pp.85-92), Grounds 1-3 teach “[t]he memory module of claim 1, wherein the module controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input configured to receive the first signal, and a second input configured to receive the second signal, and wherein the module controller is configured to couple the first input to the output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.” EX1003, ¶¶320-325. The Board’s previous decisions confirm Ground 2 teaches equivalent limitations in ’623 claims 8-10,

'218 claims [1.f], [1.h], [1.i], and 4-6, and '595 claims [1.e.ii] and 6. EX1003, ¶¶153-155, 320; EX1034, 20-21; EX1102, 47-53, 63-67; EX1103, 46-47, 71-73.

For example, as explained for [1.e.3] (pp.85-92), Hazelzet's "Error Logic 100" (red) receives the "US [sic: UE] 110" signal indicating uncorrectable errors and "PERR 111" signal indicating parity errors, one of which determines the value of the "/ERROR (UE)" pin depending on the memory module's mode being ECC or parity mode. EX1014, ¶[0044], [0059], [0069-72], FIG. 4B (below, in part, annotated); EX1003, ¶321.



See also EX1014, Fig.8 (below, annotated, showing the same UE pin being used in "ECC" and "Parity" modes).

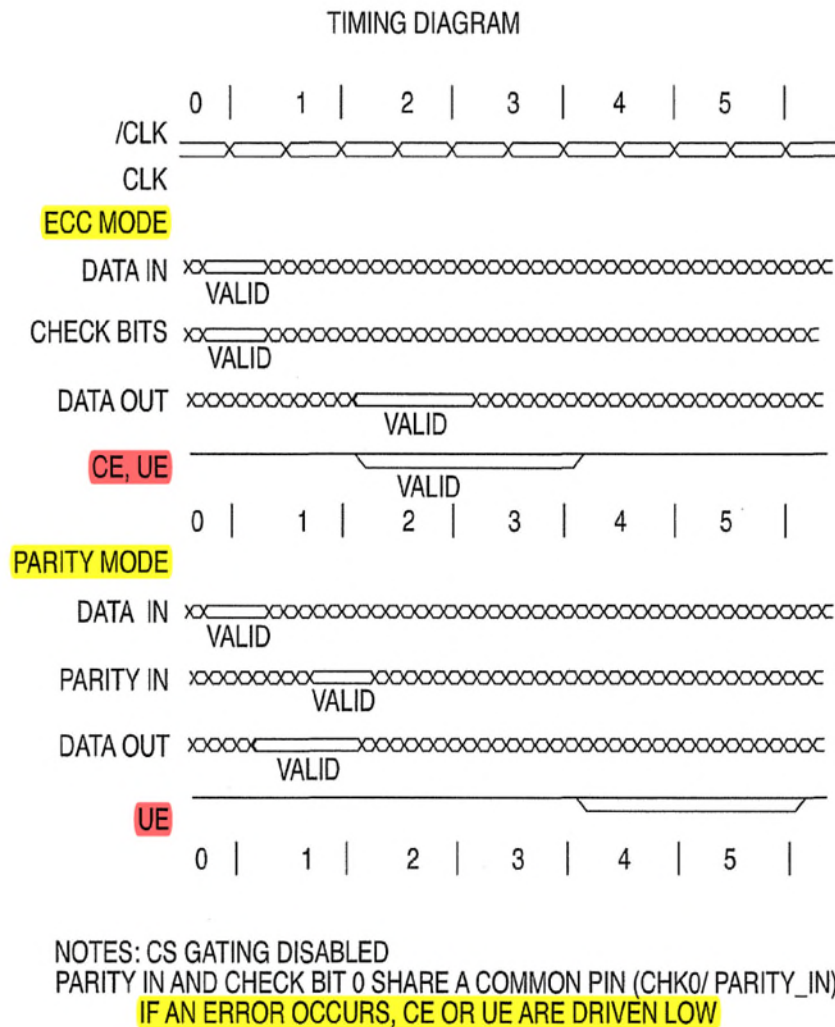


FIG. 8

In the proposed combinations, as discussed above (pp.51-55), Hazelzet's circuitry would be modified to implement notifications about the additional training, in which the UE 121 open-drain output would, when the module is performing training-related operations, send the notification/status signals identified above. EX1003, ¶322.

Hazelzet's UE 121 is an open-drain output, EX1014, ¶[0072], having a transistor with a gate to control the open-drain output as discussed above (pp.17-22). EX1017, Figs.4-5, 5:65-6:18; EX1003, ¶323. In the combination, Error Logic 100 receives a training mode notification signal in addition to the error signals 110 and 111. EX1003, ¶324. Because only one such (mode-dependent) signal would drive the UE 121 output, a POSITA would have understood, and it would have been obvious to her, that Error Logic 100 included logic circuitry (in addition to the open-drain transistor) to determine which signal to drive the transistor. EX1017, Figs.4-5, 5:65-6:18 (Fig.5, below, including OR logic coupled to the transistor's gate used for such purpose).

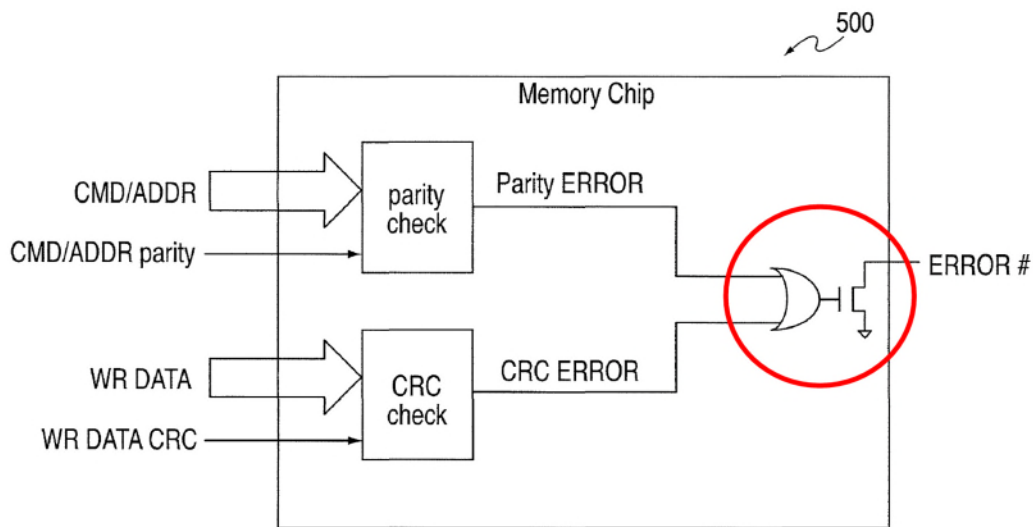
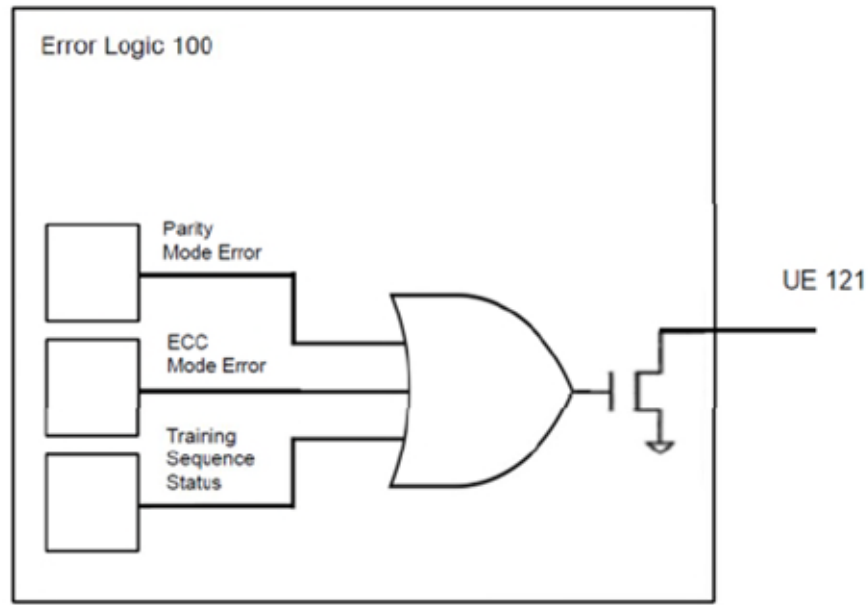


FIG. 5

As explained for claim [1.e.1] (pp.85-92), a POSITA would have understood that adding the training notification functionality would be straightforward and could use a three-input OR circuit or a multiplexer:



EX1003, ¶324. This additional logic circuitry is a “*logic circuit*,” and has “*an output coupled to a gate of the transistor*” since that is how a transistor in an open-drain configuration is driven (by a signal driving the gate) as discussed above (pp.17-22). EX1017, Figs.4-5, 5:65-6:18. Furthermore, the signal driving that gate is related to one of the signals input to Error Logic 100 (e.g., “PERR 111” (“*first signal*”) or the training notification signals (“*second signal*”), depending on selected mode, so the additional logic circuitry has “*a first input configured to receive the first signal, and a second input configured to receive the second signal, and wherein the module controller is configured to couple the first input to the*

*output during the normal memory read or write operation, and to couple the second input to the output during the operations associated with the one or more training sequences.”* EX1003, ¶¶324-325.

## 9. Claims 10-20

The limitations of claims 10-20 are substantially identical to earlier limitations, and they are obvious in light of Grounds 1-3 for at least the same reasons discussed above:

| This limitation... | ...is substantially similar to this limitation... | ...and thus obvious for at least the same reasons above and as discussed in EX1003: |
|--------------------|---------------------------------------------------|-------------------------------------------------------------------------------------|
| [10.a]-[10.b.1]    | [1.a]                                             | ¶¶327-329 (¶¶223-225)                                                               |
| [10.b.2]           | [1.a]-[1.b.1]                                     | ¶¶330-332 (¶¶223-229)                                                               |
| [10.c]             | [1.c.1]                                           | ¶¶333-335 (¶¶235-237)                                                               |
| [10.d]             | [1.d.1]                                           | ¶¶336-338 (¶¶243-245)                                                               |
| [10.e.1]           | [1.b.1]                                           | ¶¶339-341 (¶¶226-229)                                                               |
| [10.e.2]           | [1.b.2]                                           | ¶¶342-344 (¶¶230-234)                                                               |
| [10.f]             | [1.e.1]                                           | ¶¶345-347 (¶¶253-272)                                                               |
| [10.g]             | [1.b.1], [1.c.2]                                  | ¶¶348-350 (¶¶226-229, ¶¶238-242)                                                    |
| [10.h]             | [1.c.2], [1.d.2]                                  | ¶¶351-353 (¶¶238-242, 246-252)                                                      |
| [10.i]             | [1.e.2]                                           | ¶¶354-356 (¶¶273-279)                                                               |
| [10.j]             | [1.e.3]                                           | ¶¶357-359 (¶¶280-289)                                                               |
| [10.k]             | [1.e.3]                                           | ¶¶360-362 (¶¶280-289)                                                               |

| This limitation... | ...is substantially similar to this limitation... | ...and thus obvious for at least the same reasons above and as discussed in EX1003: |
|--------------------|---------------------------------------------------|-------------------------------------------------------------------------------------|
| [11]               | [2]                                               | ¶¶363-365 (¶¶290-294)                                                               |
| [12]               | [3]                                               | ¶¶366-368 (¶¶295-299)                                                               |
| [13]               | [4]                                               | ¶¶369-371 (¶¶300-302)                                                               |
| [14]               | [5]                                               | ¶¶372-374 (¶¶303-307)                                                               |
| [15]               | [6]                                               | ¶¶375-377 (¶¶308-310)                                                               |
| [16]               | [7]                                               | ¶¶378-380 (¶¶311-316)                                                               |
| [17]               | [8]                                               | ¶¶381-383 (¶¶317-319)                                                               |
| [18]               | [9]                                               | ¶¶384-386 (¶¶320-325)                                                               |
| [19.a]             | [1.a]                                             | ¶¶387-389 (¶¶223-225)                                                               |
| [19.b.1]           | [1.b.1]                                           | ¶¶390-392 (¶¶226-229)                                                               |
| [19.b.2]           | [1.b.2]                                           | ¶¶393-395 (¶¶230-234)                                                               |
| [19.c.1]           | [1.c.1]                                           | ¶¶396-398 (¶¶235-237)                                                               |
| [19.c.2]           | [1.b.1], [1.c.2]                                  | ¶¶399-401 (¶¶226-229, 238-242)                                                      |
| [19.d.1]           | [1.d.1]                                           | ¶¶402-404 (¶¶243-245)                                                               |
| [19.d.2]           | [1.d.2]                                           | ¶¶405-407 (¶¶246-252)                                                               |
| [19.e.1]           | [1.e.1]                                           | ¶¶408-410 (¶¶253-272)                                                               |
| [19.e.2]           | [1.e.2]                                           | ¶¶411-413 (¶¶273-279)                                                               |
| [19.e.3]           | [1.e.3]                                           | ¶¶414-416 (¶¶280-289)                                                               |
| [19.f]             | [5]                                               | ¶¶417-419 (¶¶303-307)                                                               |

| This limitation... | ...is substantially similar to this limitation... | ...and thus obvious for at least the same reasons above and as discussed in EX1003: |
|--------------------|---------------------------------------------------|-------------------------------------------------------------------------------------|
| [19.g]             | [4] <sup>9</sup>                                  | ¶¶420-422 (¶¶300-302)                                                               |
| [19.h]             | [6]                                               | ¶¶423-425 (¶¶308-310)                                                               |
| [19.i]             | [9]                                               | ¶¶426-428 (¶¶320-325)                                                               |
| [20]               | [7]                                               | ¶¶429-431 (¶¶311-316)                                                               |

### C. Grounds 4–6

#### 1. Grounds 4-6: Claims 1-20 Are Obvious Over the Combination of Grounds 1-3 And Kim (EX1017)

To the extent one might argue that Grounds 1-3 (Hazelzet-JEDEC, Hazelzet-Buchmann, Hazelzet-Wang) do not satisfy claims 1-20, these claims would have been obvious in view of those combinations further combined with Kim. As discussed above (pp.5-7), Netlist is precluded from challenging the Hazelzet/Buchmann/Kim combination in Ground 5 that the Board has repeatedly relied on to invalidate similar claims. EX1034, 20-21; EX1102, 71-75; EX1103, 78-82.

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<sup>9</sup> When the transistor of an open-drain output is in a “*low impedance state*,” the output is driven to ground, i.e., “*the low logic level*,” as discussed above (pp.17-22). EX1003, ¶422.

Kim discloses an “open drain output” (ERROR#) with an output pin coupled to the drain of a transistor having a gate, a source, and a drain. EX1017, Fig.4 (below). Kim’s open-drain output is coupled to a pull-up resistor (i.e., connected to a high voltage via a pull-up resistor), the source of the transistor is coupled to ground, and the gate is coupled to an “ERR” signal. EX1003, ¶259.

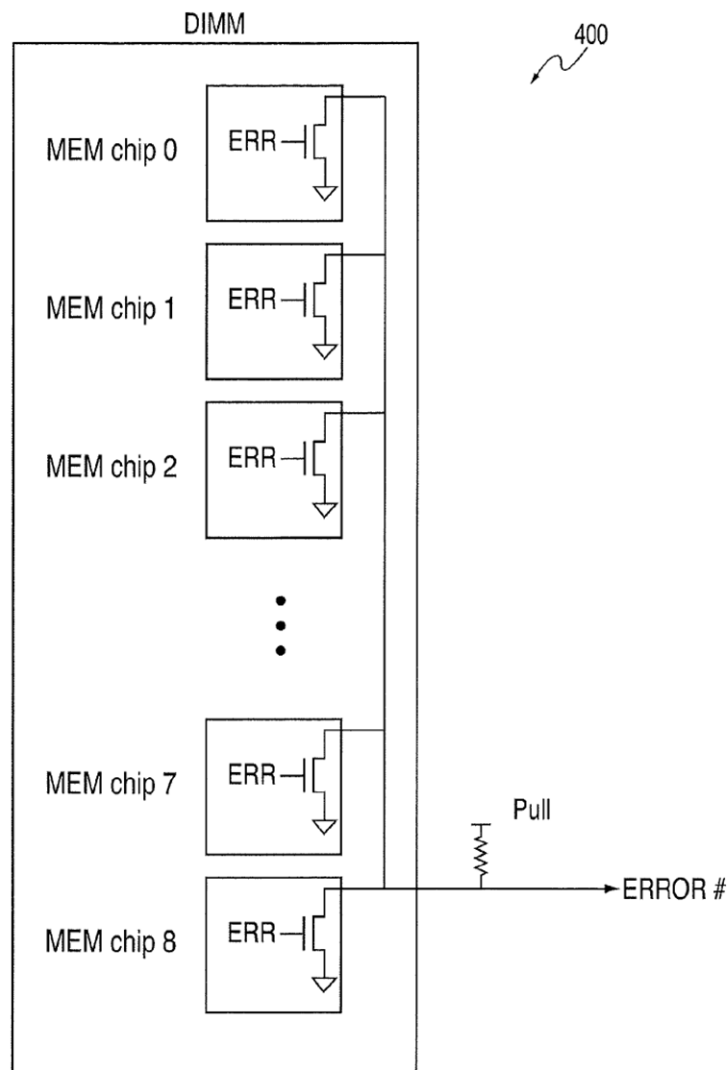


FIG. 4

Kim also discloses using a logic element (an OR gate) such that multiple error signals could drive the gate of the open-drain transistor. EX1017, Fig.5 (below), 6:13-6:18; EX1003, ¶260.

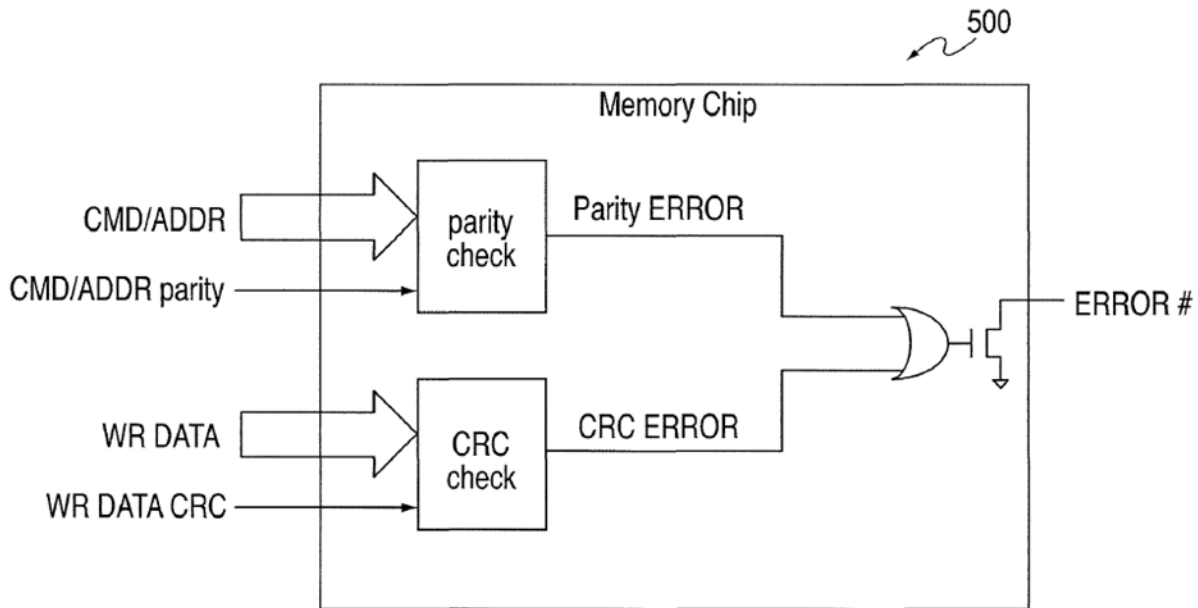
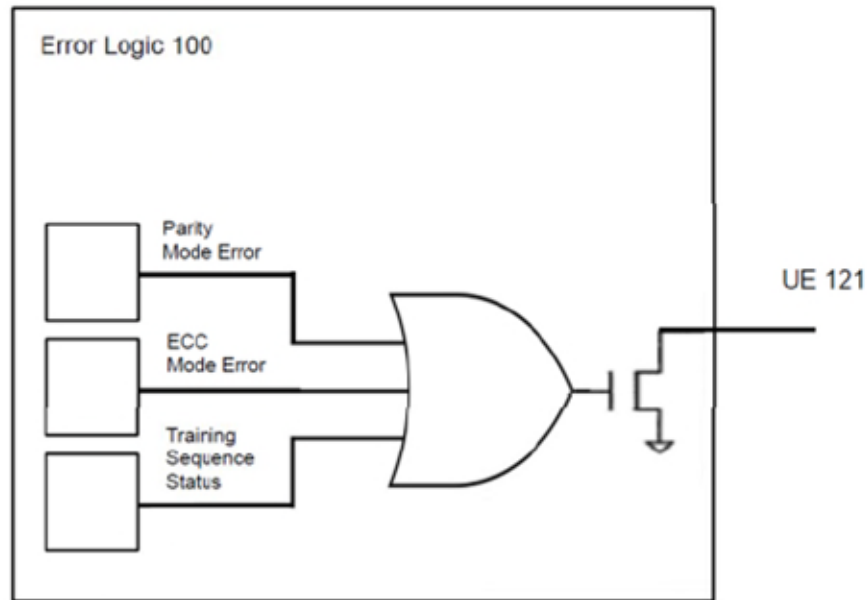


FIG. 5

In the combination, Kim's open-drain transistor functionality would be included within Hazelzet's error logic 100 such that signals indicating parity mode error, ECC mode error, and training status would be provided to a logic gate, e.g., Kim's OR gate, which would select among them based on the module's mode, as in Hazelzet. The output of the OR gate would be coupled to drive an open-drain transistor's gate, which itself drives UE 121, as shown in the annotation below:



EX1003, ¶¶261-262. Instead of an OR gate, a multiplexor can also be used.

EX1003, ¶263.

If an OR gate is used, each of its inputs would remain low when the module was not in its associated mode; the control signal whose mode was active could be high to indicate the occurrence of the signaled event (error in Parity Mode or ECC Mode; ongoing training in Training Mode), or the control signal could be low to indicate that no error is occurring (Parity/ECC Mode) or training is completed (Training Mode). The active control signal would then be passed through the OR gate to drive the gate of the transistor. EX1003, ¶264.

A POSITA would have understood that an open-drain output as in the above figure would be in a high impedance state when the transistor gate is low, since the transistor would be off, as discussed above (pp.17-22, 51-55). EX1003, ¶¶211-

220; EX1017, Fig.4, ¶[0099]. On the other hand, the open-drain output would be driven to a low logic level (to ground) and be put in a low impedance state when the transistor gate is high, since the transistor would be on and there is a low impedance path through the transistor to ground. *Id.*; EX1003, ¶267. This combined circuit would thus include the transistor configurations, signaling, and logic elements as recited in the claims. EX1003, ¶¶265-268, 261.

A POSITA would have been motivated to combine Kim with the combinations of Hazelzet and JEDEC, Buchmann, or Wang, each being analogous art to the '024 Patent as discussed above (pp.44-45). EX1003, ¶270. Kim was filed soon after Hazelzet and includes similar disclosures with additional details about the use of an open-drain output to notify the memory controller of the module's status, such as having errors during parity and ECC normal operating modes, motivating a POSITA to consider them together. EX1017, 1:16-:22, 5:49-:57, 6:8-:16. Using Kim's output-pin functionality in Hazelzet's system would have achieved predictable results, i.e., using an open-drain output to provide error or status information from multiple components. EX1003, ¶269.

A POSITA would have been motivated to use Kim's open-drain techniques in the above combinations because it represented a well-known, reliable, and simple technique to provide error and/or status information from a number of components. EX1014, ¶¶[0072], [0122]; EX1017, Figs.4-5, 5:65-6:18, 12:18-:23;

EX1003, ¶271. Kim's open-drain technique permitted a single signal line with an OR logic element to indicate error or training status information, simplifying the design of Hazelzet's system and saving the finite pins on the various integrated circuits connected to the bus. EX1003, ¶271.

Indeed, as discussed above with respect to [1.e.3] (pp.85-92), a POSITA would have understood that the disclosed "open drain" output is the output of "a transistor having an open drain" with the "source" of that transistor being "coupled to the ground" as discussed above (pp.17-22), and it thus would have been obvious to a POSITA to implement it in this fashion. It would have also been obvious to a POSITA to use an OR gate (as in Kim, here) or a multiplexor for logic circuitry within Hazelzet's Error Logic 100 to select which signal to drive the open-drain output, and any of these three modes would have been obvious. *See id.*

## VIII. OTHER CONSIDERATIONS

### A. §325(d)

*Advanced Bionics* and §325(d) do not support discretionary denial because the Examiner did not consider the Grounds discussed above. Specifically, although the Examiner considered the combination of Hazelzet with a JEDEC publication **different than** the JEDEC reference (EX1015) in Ground 1 (*e.g.*, EX1002, 192-96, 222 (discussing JESD206, EX1025), *see* EX1003, ¶¶142-151), the Examiner did **not** consider the combination of Hazelzet with JEDEC,

Buchmann, or Wang, or the addition of Kim to these combinations. Further, contrary to 37 C.F.R. §42.73(d)(3), neither the Applicants nor the Examiner offered any analysis of the claims in view of the Board’s decisions (EX1034; EX1102; EX1103) cancelling the substantially similar claims of the ’623, ’218, and ’595 Patents (discussed above, pp.5-7). These decisions demonstrate that the Examiner materially erred in allowing the claims. *See Samsung Elecs. Co. v. Netlist, Inc.*, IPR2022-00639, Paper 15, at 11 (PTAB Oct. 19, 2022) (citing §42.73(d)(3)(i)). “[I]f the record of the Office’s previous consideration of the art is not well developed or silent, then a petitioner may show the Office erred by overlooking something persuasive[.]” *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6, at 10 (PTAB Feb. 13, 2020) (precedential); *see also Yita LLC v. MacNeil IP LLC*, IPR2023-00172, Paper 12, at 45-46 (PTAB June 13, 2023); *HTC Corp. v. Motiva Patents, LLC*, IPR2019-01666, Paper 9, at 6-10 (PTAB Apr. 3, 2020).

**B. *Fintiv***

The *Fintiv* factors and Interim *Fintiv* Guidance (EX1113) favor institution. There is no “parallel district court litigation” addressing the unpatentability of the ’024 Patent, EX1113, pp.1-2, because Netlist has not asserted the ’024 Patent against Samsung, and Samsung has pursued only a declaratory judgment of non-infringement, *see* EX1114. Furthermore, the merits of this petition are compelling,

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as confirmed by the repeated invalidation of similar claims based on Grounds 2 and 5, thus favoring institution here. EX1113, pp.3-5.

## **IX. CONCLUSION**

Petitioner respectfully requests that Trial be instituted and that claims 1-20 be canceled as unpatentable.

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**CERTIFICATE OF COMPLIANCE**

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. §42.24 because it contains 13,973 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. §42.24.

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**CERTIFICATE OF SERVICE**

I hereby certify that on this 8th day of October, 2024, a copy of this Petition, including all exhibits, has been served in its entirety by FedEx Express on the following counsel of record for Patent Owner:

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