JEDEC STANDARD

LRDIMM DDR3 Memory Buffer (MB)
Version 1.0

JESD82-30

OCTOBER 2014

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

Netlist EX2001
Samsung v. Netlist
IPR2025-00001

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2014
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107
This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information.

LRDIMM: Memory Buffer (MB), Version 1.0

Contents

1 Introduction 1

1.1 LRDIMM Memory Buffer Overview....1
1.2 Memory Buffer Functionality 1
1.2.1 Memory Buffer Key Features....1
1.2.2 DDR SDRAM 1
1.2.3 Byte Group Signal Mapping 2
1.3 LRDIMM DDR3 Memory Buffer Block Diagram 3
1.4 Interfaces 4
1.4.1 HOST Interface 4
1.4.2 DDR3 DRAM Interface....4
1.4.3 SMBus Slave Interface....4
1.5 References....4
1.6 Glossary 5

2 Ballout and Package Information 7

2.1 588-Ball FBGA (20x38 Array, 25.2x13.5 mm Body Size, 0.65 mm Pitch, MO-301A Variation A) Pin configuration 7
2.2 Pin Assignments for the LR-DIMM DDR3 Memory Buffer (MB)....8
2.3 Package Information 16

3 Pin Descriptions 17

3.1 Pin Description 17

4 Host Interface Protocol and Requirement 21

4.1 MB Modes of operation 21
4.1.1 Direct Rank Addressing Mode 21
4.1.2 Rank Multiplication Mode 22
4.2 Command, Address, and Control Signal usage 34
4.2.1 Command Signals....34
4.2.2 Address Signals 35
4.2.3 Control Signals....36
4.3 Parity 39
4.3.1 Parity Timing Scheme Waveforms....39
4.4 Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling 41
4.5 Control Word Access Mechanism 45
4.6 Address Mirroring....46

5 DRAM Interface Protocol and Requirement....47

5.1 Signals and Usage....47
5.1.1 Command / Address 47
5.1.2 Control Signals.....48
5.1.3 Clock Outputs....49
5.1.4 Reset....50
5.1.5 DRAM data bus.....50
5.2 Turnaround Cycles....50

6 Initialization 51

6.1 Initialization Overview 51
6.2 Power-on Initialization....52
6.2.1 Clock Stabilization Time tSTAB 53
6.3 Initialization with Stable Power (Soft Reset) 55
6.4 Host RCW to Configure MB....56
6.5 Host MRS to Configure DRAM 56
6.6 Host to DRAM ZQ Calibration....57
6.7 MB-DRAM Training....57
6.8 Host-MB Training....57

7 Electrical, Timing, Power and Thermal 59

7.1 Electrical DC and AC Parameters 59
7.1.1 Absolute maximum ratings 59
7.1.2 DC and AC Specifications 60
7.1.3 DC specifications, IDD Specifications....66
7.1.4 Input/Output Capacitance 67
7.2 AC and DC Input and Output Measurement Levels 68
7.2.1 Differential swing requirements for clock (CK - CK#) and strobe (DQS - DQS#) 68
7.2.2 Slew Rate Definitions for Differential Input Signals 69

Contents (cont'd)

7.2.3 Single Ended AC and DC Output Levels 70
7.2.4 Differential AC and DC Output Levels 70
7.2.5 Single Ended Output Slew Rate 71
7.2.6 Differential Output Slew Rate 72
7.2.7 Reference Load for AC Timing and Output Slew Rate 73
7.2.8 Overshoot and Undershoot Specifications 74
7.3 Host Interface Electrical / Timing Specifications 76
7.3.1 CMD/ADDR/CTRL Input Bus Termination Requirement 76
7.3.2 DQ/DQS On-Die Termination (ODT) Requirement 77
7.3.3 DQ/DQS Output Driver DC Electrical Characteristics 78
7.3.4 Host Interface Input Timing and DQ/DQS Output Timing 79
7.4 DRAM Interface Electrical / Timing Specifications 83
7.4.1 MDQ/MDQS On-Die Termination (MODT) Requirement 83
7.4.2 QCMD/QADDR/QCTRL/Yn_t/Yn_c DC and AC Output Parameters 84
7.4.3 MDQ/MDQS DC and AC Output Parameters 85
7.4.4 DRAM Interface Input and Output Timing 87
7.5 Data Setup, Hold and Slew Rate Derating 96
7.6 Nominal and Tangent line slew rate measurement for Setup and Hold De-rating 98
7.7 Test circuits and switching waveforms for CMD/ADD/CNTRL/CK Inputs 106
7.7.1 Parameter measurement information 106
7.7.2 Error output load circuit and voltage measurement information 109

8 Power Management 111

8.1 CKE Power Management 111
8.1.1 2 DCKE mode (RDIMM Compatible Mode) 112
8.1.2 4 DCKE mode 112
8.1.3 Soft CKE mode 112
8.2 Memory Buffer Power Savings Modes 113
8.2.1 Memory Buffer CKE Power Down 113
8.2.2 Clock Stopped Power Down Mode 117
8.3 Dual Frequency Support 120

9 Control Words 121

9.1 Control Word Decoding 121
9.2 Control Words Overview Map 122
9.3 Function 0 Control Word Registers 127
9.4 Function 1 Control Word Registers 138
9.5 Function 2 Control Word Registers 145
9.6 Function [3-11] Control Word Registers 152
9.7 Function 12 Control Registers 157
9.8 Function 13 Control Registers 158
9.9 Function 14 Control Word Registers 160
9.10 Function 15 Control Word Registers 161

10 MEMBIST 163

10.1 MEMBIST - Memory Built-In Self-Test 163
10.2 MemBIST Feature Summary 164
10.3 Function Overview 166
10.3.1 Initialization MemBIST 166
10.3.2 Full Membist 166
10.4 Address Generation 168
10.4.1 Address Definition 168
10.4.2 Row addressing 168
10.4.3 Column addressing 168
10.4.4 Diagonal addressing (aka FastXY addressing) 169
10.4.5 Bank addressing 169
10.4.6 Rank addressing 169
10.4.7 Dynamic Address inversion 170
10.5 Memory Data Formatting 171
10.5.1 Static Data Formats 171
10.5.2 Dynamic Data Formats 171
10.5.3 Circular shift register 171
10.5.4 Random data generator 172
10.6 Error Reporting and Control 172
10.6.1 Failure Address Reporting 173

Contents (cont'd)

10.6.2 Multiple Failures 173
10.7 Per Address operations 174
10.8 Algorithmic Testing 176
10.8.1 Initialization Tests 176
10.8.2 Memory Stress Tests 176
10.9 Membist Flow Control FSM 177
10.10 Command State Finite State Machine 179
10.11 Timing parameters 181
10.12 Memory BIST Registers 182
10.12.1 MBCSR: MemBIST Control 183
10.12.2 MB_START_ADDR: Memory Test Start Address 186
10.12.3 MB_END_ADDR: Memory Test End Address 186
10.12.4 MBFADDRPTR: Memory Test failure address pointer register 187
10.12.5 MB_ERR_ADDR0: Memory Test Failure address 0 190
10.12.6 MB_ERR_ADDR1: Memory Test Failure address 1 191
10.12.7 MB_ERR_ADDR2: Memory Test Failure address 2 191
10.12.8 MB_ERR_ADDR3: Memory Test Failure address 3 191
10.12.9 MB_ERR_ADDR4: Memory Test Failure address 4 192
10.12.10 MB_ERR_ADDR5: Memory Test Failure address 5 192
10.12.11 MB_ERR_ADDR6: Memory Test Failure address 6 192
10.12.12 MB_ERR_ADDR7: Memory Test Failure address 7 193
10.12.13 MB_ERRDATA_BYTE0_1_0: Memory Test Error Data 1/0 198
10.12.14 MB_ERRDATA_BYTE1_1_0: Memory Test Error Data 1/0 199
10.12.15 MBLFSRSED: Memory Test Circular Shift and LFSR Seed 207

11 Transparent Mode 209

11.1 Transparent Mode 209
11.1.1 Functions 209
11.1.2 CA Signal mapping 210
11.1.3 CA timing 210
11.1.4 DQ Functionality and Timing 211
11.1.5 Entry Procedure 211
11.1.6 Exit Procedure 211
11.1.7 Control Word 212
11.1.8 Timing diagram 213

12 LAI Mode 215

12.1 LAI Mode Support (Optional) 215

13 SMBus Interface and Temperature Sensor 217

13.1 SMBus 2.0 Specification Compatibility 217
13.2 Operating Range 217
13.3 External Pins 217
13.3.1 Serial Clock (SCL) 217
13.3.2 Serial Data (SDA) 217
13.3.3 Select Address (SA0, SA1, SA2) 218
13.4 System Management Access 219
13.4.1 Slave Address 219
13.4.2 Supported SMBus Commands 220
13.4.3 MB Register Access Protocols 220
13.5 SMBus Error Handling 224
13.6 SMBus Resets 224
13.6.1 SMBus Interface State Machine Reset 224
13.6.2 SMBus transactions during reset 224
13.7 Temperature Sensor (TS) 224
13.7.1 EVENT_n Pin 225
13.7.2 TS Register Address Map 226
13.7.3 Capabilities Register 227
13.7.4 Configuration Register 229
13.7.5 Temperature Registers 231

14 Reset 235

14.1 Introduction 235
14.2 Platform Reset Functionality 235
14.2.1 Platform RESET_n Requirements 235
14.2.2 DDR3 LRDIMM Memory Buffer RESET_n Requirements 235
14.2.3 Power-Up and Suspend-to-RAM Considerations 236

14.3 Reset Types 236

15 Configuration and Status Registers 237

15.1 Access Mechanism 237
15.1.1 Register Attribute Definition 238
15.1.2 Number Notation 239
15.1.3 Function Spaces 239
15.2 Registers 240
15.2.1 Register Map 240
15.2.2 Register Description 244

Tables

1 DQ and DQS Mapping 2
2 MDQ and MDQS Mapping 2
3 588-Ball FBGA (20x38 Array, 13.5x25.2 mm Body Size, 0.65 mm Pitch, MO-301A Variation A) (Transparent, Top View) - Left Side 8
4 588-Ball FBGA (20x38 Array, 13.5x25.2 mm Body Size, 0.65 mm Pitch, MO-301A Variation A) (Transparent, Top View) - Right Side 9
5 Memory Buffer Signals By Ball Number 10
6 Memory Buffer Signal Types 17
7 Pin Description 17
8 Modes of operation for each DIMM type 21
9 Rank Multiplication Command Details 22
10 RM bits for each DIMM type. 23
11 Normal and Rank Multiplication Control Signal Connectivity without Rank 1 and Rank 5 Swap (F[0]RC2 DA4 = 1b) 24
12 Normal and Rank Multiplication Control Signal Connectivity with Rank 1 and Rank 5 Swap (F[0]RC2 DA4 = 0b) 25
13 Normal (1:1), 2 Way (1:2) and 4 Way (1:4) Rank Multiplication Control Signal Decoding without Rank 1 and Rank 5 Swap (F[0]RC2 DA4 = 1b) 26
14 Normal (1:1), 2 Way (1:2) and 4 Way (1:4) Rank Multiplication Control Signal Decoding with Rank 1 and Rank 5 Swap (F[0]RC2 DA4 = 0b) 28
15 Precharge Single and Precharge All Command Control 31
16 MRS Control 34
17 Command and MB Action 35
18 CKE Modes 37
19 Soft CKE command 38
20 Address Mirroring 46
21 Command / Address signals 47
22 Address Mirroring 48
23 Control Signals 49
24 Data bus connections. 50
25 MB Device Initialization Sequence 54
26 MB Device Initialization Sequence when Power and Clock are Stable 56
27 Absolute maximum ratings over operating free-air temperature range 59
28 Operating Conditions for the SMBUS interface 60
29 AC Measurement Conditions for SMBUS interface 60
30 Input Parameters for SMBUS interface 60
31 DC Characteristics for SMBUS interface 61
32 AC Characteristics for SMBUS interface 63
33 Operating Electrical Characteristics 65
34 DC Electrical characteristics 66
35 Capacitance values 67
36 Differential AC and DC Input Levels 68

Contents (cont'd)

37 Differential Input Slew Rate Definition....69
38 Single-ended AC and DC Output Levels....70
39 Differential AC and DC Output Levels....70
40 Single-ended Output Slew Rate Definition....71
41 Differential Output Slew Rate Definition....72
42 AC overshoot/undershoot specification for Address, Command and Control pins....74
43 AC overshoot/undershoot specification for Clock, Data, and Strobe....75
44 CMD/ADDR/CTRL Input Bus Termination....76
45 DQ/DQS On-Die Termination....77
46 DQ/DQS Output Driver Impedance RON Requirement....78
47 Host Interface Input Timing Parameters....79
48 Host Interface DQ/DQS Output Timing Parameters....82
49 MDQ/MDQS On-Die Termination (MODT) for READ Operation....83
50 QCMD/QADDR/QCTRL/Yn_t/Yn_c Ron and Output Slew Rate....84
51 AC level for Slew Rate Measurement....85
52 MDQ/MDQS Ron Requirement (for DRAM Interface WRITE Operation)....86
53 DRAM Interface MDQ/MDQS Input Timing Parameters....87
54 Output timing requirements....88
55 DRAM Interface Output Timing Parameters....90
56 MB Operating Spec for Different Physical Ranks....92
57 MB Operating Spec for Different Physical Ranks....92
58 Clock driver Characteristics at application frequency....95
59 Derating values for DDR3-800/1066/1333/1600 tDS/tDH - (AC100)....96
60 Derating values for DDR3L-800/1066/1333/1600 tDS/tDH - (AC90)....97
61 CKE Management Control Register (in F0RC6)....111
62 Soft CKE Command Definition....112
63 Control Word Decoding....121
64 F[0] Control Word Decoding....122
65 F[1] Control Word Decoding....122
66 F[2] Control Word Decoding....123
67 F[3] Control Word Decoding....123
68 F[3-10] RC[10-11] Control Word Decoding....124
69 F[3-11] RC[12-13] Control Word Decoding....124
70 F[4-11] RC[0-9, 14-15] Control Word Decoding....124
71 F[11] RC[10-11] Control Word Decoding....124
72 F[12] Control Word Decoding....125
73 F[13] Control Word Decoding....125
74 F[14] Control Word Decoding....126
75 F[15] Control Word Decoding....126
76 F[0]RC0: Global Features Control Word....127
77 F[0]RC1: Clock Driver Enable Control Word....127
78 F[0]RC2: Timing Control Word....128
79 F[0]RC3: Address/Command & QxCS_n Signals Driver Characteristics Control Word....128
80 F[0]RC4: QxODT & QxCKE Signals Driver Characteristics Control Word....129
81 F[0]RC5: CK Driver Characteristics Control Word....129
82 F[0]RC6: CKE and ODT Management Control Word....130
83 Host - Buffer Interface Command Definition,....131
84 F[0]RC7: Function Select Control Word....132
85 F[0]RC8 - IBT Setting Control Word for Address, Command & PAR_IN Signal & Input reference voltage setting for Address, Command, Control & Parity inputs....132
86 F[0]RC9: Power Saving Settings Control Word....133
87 F[0]RC10: Encoding for LRDIMM Operating Speed....133
88 F[0]RC11: Operating Voltage & Parity Calculation Control Word....134
89 F[0]RC12 Training Control Word....134
90 F[0]RC13 DIMM Configuration Control Word....135

Contents (cont'd)

91 F[0]RC14: DRAM Configuration & DRAM Command Control Word 136
92 F[0]RC15: Rank Multiplication Control Word....137
93 F[1] RC0: IBT Settings for DCS_n Pins Control Word 138
94 F[1] RC1: IBT Settings for DCKE Pins Control Word 138
95 F[1] RC2: IBT Settings for DODT Pins Control Word....139
96 F[1] RC[3:6] Reserved 139
97 F[1] RC7: Function Select Control Word (See F[0]RC7 for definition) 139
98 F[1] RC8 Extended Delay Control Word - Optional....140
99 F[1] RC9 - Refresh Stagger 140
100 F[1] RC10 - Refresh Stagger Limit....141
101 F[1] RC11 Extended Delay Control Word - Optional....141
102 F[1] RC12: Additive QCA Pre-launch Control Word....142
103 F[1] RC13: Additive QCS_n Delay Control Word....142
104 F[1] RC14: Additive QODT Delay Control Word 143
105 F[1] RC15: Additive QCKE Delay Control Word....143
106 F[2] RC0 Transparent Mode 145
107 F[2] RC1 Reset Control....145
108 F[2] RC2 SMBus Access Control 145
109 F[2] RC3: Training & Errout_n Control Word....146
110 F[2] RC4 MEMBIST Rank Control....146
111 F[2] RC5: DRAM Row & Column Addressing 147
112 F[2] RC6: MEMBIST Control....148
113 F[2] RC8: MEMBIST ECC Pattern - 1 149
114 F[2] RC9: MEMBIST ECC Pattern - 2 149
115 F[2] RC10: MEMBIST ECC Pattern - 3 149
116 F[2] RC11: MEMBIST ECC Pattern - 4 149
117 F[2] RC12: MEMBIST ECC Pattern - 5 149
118 F[2] RC13: MEMBIST ECC Pattern - 6 149
119 F[2] RC14: MEMBIST ECC Pattern - 7 150
120 F[2] RC15: MEMBIST ECC Pattern - 8 150
121 MEMBIST - 8 Bits ECC Mapping 151
122 MEMBIST - 16 bits ECC Mapping....151
123 MEMBIST - 32 bits ECC Mapping....151
124 F[3] RC0: Connector Interface DQ RTT_Nom Termination Control Word 152
125 F[3] RC1: Connector Interface DQ RTT_WR Termination & Reference Voltage Control Word....152
126 F[3] RC2: Connector Interface DQ Driver Control Word 153
127 F[3] RC[3:5] Reserved 153
128 F[3] RC6: Connector Interface Misc Control Word....153
129 F[3] RC7: Function Select Control Word (see F[0] RC7 for definition)....154
130 F[3] RC8: DRAM Interface MDQ Termination Control Word....154
131 F[3] RC9: DRAM Interface MDQ Driver Control Word 154
132 F[3-10]RC10: Read QODT Control Words; F[3:10] = Rank[0:7] respectively. F11 RC10 Reserved 155
133 F[3-10]RC11: Write QODT Control Words; F[3-10] = Rank[0:7] respectively. F11RC11 Reserved 155
134 F[3-11] RC12: Reserved 156
135 F[3-11] RC13: Reserved 156
136 F[3] RC[14-15]: Reserved 157
137 F[4-11] RC[0-6, 8-9, 14-15] & F[11] RC[10-11]: Reserved....157
138 F[12] RC[0:6, 8:15]: Reserved 157
139 F[12] RC7: Function Select Control Word (see F0RC7 for definition)....157
140 F[13] RC[0:6, 8]: Reserved 157
141 F[13] RC7: Function Select Control Word (see F0RC7 for definition)....157
142 F13 RC9: SMBus Function Select 158
143 F13 RC10: LSB of Address Port 158
144 F13 RC11: MSB of Address Port 158

Contents (cont'd)

145 F13 RC12: Extended Address Port (Optional) 159
146 F13 RC13: Reserved 159
147 F13 RC14: LSB of Data Port 159
148 F13 RC15: MSB of Data Port 159
149 F[14] RC[0]: MB Vendor Specific Bytes 160
150 F[14] RC[1]: MB Vendor Specific Bytes 160
151 F[14] RC[2:5]: MB Vendor Specific Bytes 160
152 F[14] RC[6]: MB Vendor Specific Bits 160
153 F[14] RC7: Function Select Control Word (see F0RC7 for definition) 160
154 F[14] RC[8:15]: MB Vendor Specific Bytes 160
155 F[15] RC[0:5]: MB Vendor Specific Bytes 161
156 F[15] RC[6]: MB Vendor Specific Bits 161
157 F[15] RC7: Function Select Control Word (see F0RC7 for definition) 161
158 F[15] RC[8:15]: MB Vendor Specific Bytes 161
159 MemBIST Feature Summary 164
160 Memory Address Definition, BC4 168
161 Memory Address Definition, BL=8 168
162 Address Inversion 170
163 Failure Address Format 173
164 Timing parameters 181
165 Function 3: MemBIST Registers 182
166 F2RC0: Transparent Mode 214
167 Unique Addressing of SPDs in DIMM Applications 220
168 SMBus command Encoding 222
169 SMBus Protocol Addressing fields 223
170 Status Field Encoding for SMBus Reads 223
171 Temperature Register Addresses 229
172 Capabilities Register 230
173 TRES Bit Decode 230
174 Configuration Register 231
175 HYST Bit Decode 231
176 High Limit Register 233
177 Low Limit Register 234
178 TCRIT Limit Register 234
179 Temperature Data Register 234
180 Temperature-to-Digital Conversion Performance 235
181 Function 0 SMBus Address Map 239
182 Double word byte order for SMBus control word accesses 240
183 Register Base Attributes 240
184 Register Attribute Modifier 240
185 Control Word and Temperature Sensor Register Map 242
186 Vendor ID Register 246
187 Device ID Register 246
188 Revision ID Register 246
189 F0RC1_0 Register 247
190 F0RC3_2 Register 248
191 F0RC5_4 Register 249
192 F0RC7_6 Register 250
193 F0RC9_8 Register 251
194 F0RC11_10 Register 252
195 F0RC13_12 Register 253
196 F0RC15_14 Register 254
197 F1RC1_0 Register 255
198 F1RC3_2 Register 256
199 F1RC7_6 Register 256

Contents (cont'd)

200 F1RC9_8 Register 257
201 F1RC11_10 Register 258
202 F1RC13_12 Register 259
203 F1RC15_14 Register 260
204 F2RC1_0 Register 261
205 F2RC3_2 Register 262
206 F2RC5_4 Register 263
207 F2RC7_6 Register 264
208 F2RC9_8 Register 264
209 F2RC11_10 Register 264
210 F2RC13_12 Register 265
211 F2RC15_14 Register 265
212 F3RC1_0 Register 265
213 F3RC3_2 Register 266
214 F3RC7_6 Register 266
215 F3RC9_8 Register 267
216 F3RC11_10 Register 267
217 F3RC13_12 Register 268
218 F4RC7_6 Register 269
219 F4RC11_10 Register 269
220 F4RC13_12 Register 270
221 F5RC7_6 Register 271
222 F5RC11_10 Register 271
223 F5RC13_12 Register 272
224 F6RC7_6 Register 273
225 F6RC11_10 Register 273
226 F6RC13_12 Register 274
227 F7RC7_6 Register 275
228 F7RC11_10 Register 275
229 F7RC13_12 Register 276
230 F8RC7_6 Register 277
231 F8RC11_10 Register 277
232 F8RC13_12 Register 278
233 F9RC7_6 Register 279
234 F9RC11_10 Register 279
235 F9RC13_12 Register 280
236 F10RC7_6 Register 281
237 F10RC11_10 Register 281
238 F10RC13_12 Register 282
239 F11RC7_6 Register 283
240 F11RC13_12 Register 284
241 F13RC9_8 Register 285
242 F13RC11_10 Register 285
243 F13RC13_12 Register 285
244 F13RC15_14 Register 286
245 F14RC1_0 Register 286
246 F14RC3_2 Register 286
247 F14RC5_4 Register 286
248 F14RC7_6 Register 286
249 F14RC9_8 Register 286
250 F14RC11_10 Register 287
251 F14RC13_12 Register 287
252 F14RC15_14 Register 287
253 F15RC1_0 Register 287

254 F15RC3_2 Register 287
255 F15RC5_4 Register 287
256 F15RC7_6 Register 288
257 F15RC9_8 Register 288
258 F15RC11_10 Register 288
259 F15RC13_12 Register 288
260 F15RC15_14 Register 288
261 TS Capabilities Register 289
262 TS Configuration Register 290
263 TS High Limit Register 291
264 TS Low Limit Register 291
265 TS Critical Temperature Register 292
266 TS Current Ambient Temperature Register 293
267 MRS Control Register 294
268 Rank 0 MR1,2 Register 295
269 Rank 1 MR1,2 Register 295
270 Rank 2 MR1,2 Register 296
271 Rank 3 MR1,2 Register 296
272 Rank 4 MR1,2 Register 298
273 Rank 5 MR1,2 Override Register 298
274 Rank 6 MR1,2 Register 300
275 Rank 7 MR1,2 Register 302
276 MR0 Snoop Register 303
277 MR1 Snoop Register 304
278 MR2 Snoop Register 305
279 MR3 Snoop Register 305

Figures

1 LRDIMM DDR3 Memory Buffer Block Diagram 3
2 Pinout Configuration 7
3 Timing of clock, data and parity signals 40
4 Two Consecutive Parity-Error Occurrences 40
5 Two Parity-Error Occurrences Separated by a Clock Cycle of no Error Occurrence 40
6 Two Parity-Error Occurrences Separated by two Clock Cycle of no Error Occurrence 41
7 Parity-Error Occurrence In Chip-Deselect Mode 41
8 Parity-Error Occurrences During Control Word Programming 42
9 Output Inversion Functional Diagram 42
10 1T Timing During Normal Operation 43
11 3T Timing During DRAM MRS Command 44
12 3T Timing During Multiple DRAM MRS Commands 45
13 Initialization Overview 52
14 Timing of clock and data during power-on initialization sequence 54
15 Timing of clock and data during initialization sequence with stable power 55
16 AC Measurement I/O Waveform 60
17 AC Waveforms 63
18 Differential Input Slew Rate Definition for DQS_t, DQS_c, MDQS_t, MDQS_c and CK_t, CK_c 69
19 Single Ended Output Slew Rate Definition 71
20 Differential Output Slew Rate Definition 72
21 Reference Load for AC Timing and Output Slew Rate 73
22 Address, Command and Control Overshoot and Undershoot definition 74
23 Clock, Data, and Strobe Overshoot and Undershoot definition 75
24 Input Bus Termination: Definition of Voltages and Currents 76
25 On-Die Termination: Definition of Voltages and Currents 77
26 Read Timing Definition 82
27 On-Die Termination: Definition of Voltages and Currents 83

Contents (cont'd)

28 Voltage waveforms, HIGH-to-LOW slew rate measurement....85
29 Voltage waveforms, LOW-to-HIGH slew rate measurement....85
30 tPDM Latency Measurement....89
31 tPDMMDQS Latency Measurement....90
32 tDVA and tDVB Timing Diagram....92
33 Twrwr Timing Spec....94
34 Trdrd Timing Spec....94
35 Twrrd Spec....94
36 Trdwr Spec....94
37 Definition for tstaoff....96
38 Clock Output (Yn) Skew....96
39 Qn Output Skew for Standard 1/2-Clock Pre-Launch....97
40 Illustration of nominal slew rate for setup time tIS (for ADD/CMD with respect to clock).....100
41 Illustration of nominal slew rate for hold time tIH (for ADD/CMD with respect to clock).....101
42 Illustration of tangent line for setup time tIS (for ADD/CMD with respect to clock)....102
43 Illustration of tangent line for hold time tIH (for ADD/CMD with respect to clock)....103
44 Illustration of nominal slew rate for setup time tDS (for DQ with respect to strobe).....104
45 Illustration of nominal slew rate for hold time tDH (for DQ with respect to strobe)....105
46 Illustration of tangent line for setup time tDS (for DQ with respect to strobe)....106
47 Illustration of tangent line for hold time tDH (for DQ with respect to strobe)....107
48 Voltage waveforms; input clock....108
49 Qn and Yn Load circuit for propagation delay and slew measurement....108
50 Voltage waveforms; propagation delay times....108
51 Voltage waveforms address floating....109
52 Calculating the virtual VTT crossing point....110
53 Load circuit, ERROUT_n Outputs....111
54 Power Down Mode Entry and Exit with IBT Off....115
55 Power Down Mode Entry and Exit with IBT On....117
56 Clock Stopped Power Down Entry and Exit with IBT On....119
57 Clock Stopped Power Down Entry and Exit with IBT Off....120
58 Errout_n Signal During DDR3 MB Training....135
59 QCA Prelaunch, OCS_n, QODT, and QCKE Delay Features....144
60 Errout_n Signal from MBIST to Normal Operation....148
61 Diagonal addressing examples....172
62 Write Operation....177
63 Read Operation....177
64 Read, Modify....177
65 MemBIST Flow Control State Machine....181
66 Command State Machine....185
67 Transparent Mode Timing Diagram....215
68 Maximum RL Value Versus Bus Capacitance (CBUS) for an SMBUS Bus....219
69 SMBUS WIRING DIAGRAM....220
70 SMBus Configuration Read (Block Write / Block Read, PEC enabled)....223
71 SMBus Configuration Read (Write Bytes / Read Bytes, PEC enabled)....223
72 SMBus Configuration Double Word Write (Block Write, PEC enabled)....225
73 SMBus Configuration Double Word Write (Write Bytes, PEC enabled)....225
74 SMBus Configuration Word Write (Block Write, PEC disabled)....225
75 SMBus Configuration Byte Write (Write Bytes, PEC disabled)....226
76 EVENT_n Pin Mode functionality....228

LRDIMM DDR3 Memory Buffer (MB)

(From JEDEC BoD Ballot JCB-11-85, formulated under the cognizance of the JC-40.4 Subcommittee on FBDIMM Support Components.)

1 Introduction

1.1 LRDIMM Memory Buffer Overview

The Load Reduced DIMM (LRDIMM) Memory Buffer (MB) supports DDR3 SDRAM main memory. The Memory Buffer allows buffering of memory traffic to support large memory capacities. Unlike DDR3 Register Buffer (SSTE32882), which only buffers Command, Address, Control and Clock, the LRDIMM Memory Buffer also buffers the Data (DQ) interface between the Memory Controller and the DRAM components. As the data electrical load is reduced for the Memory Controller interface, the system can now support more DIMMs per channel at a faster speed and higher density. All memory control for the DRAM resides in the host, including memory request initiation, timing, scrubbing, sparing, and power management. The Memory Buffer interface is responsible for memory requests to and from the local DIMM.

LRDIMM provides a high memory bandwidth, large capacity channel solution for DDR3 main memory systems. LRDIMM uses commodity DRAMs isolated from the channel behind the Memory Buffer on the DIMM. The supported capacity exceeds 144 devices per channel (depends on channel and individual system design) and total memory capacity scales with DRAM bit density.

1.2 Memory Buffer Functionality

1.2.1 Memory Buffer Key Features

- Acts as DRAM memory buffer for all read and write accesses addressed to the DIMM.
- Provides logic to support MEMBIST and Transparent Mode design for DRAM Test Support.
- Built-in MEMBIST engine to support back side memory voltage and timing training.
- Uses external supply VREFCA and VREFDQ as CA and DQ input buffer reference voltage. Support VREF WRITE margining capability for Host and DRAM interface. Supports internally generated VREFCA and VREFDQ for MB and DRAM CA and DQ input buffer reference voltage. Even though VREF level is internally generated by MB, it is still controlled by the host through configuration registers.
- Supports parity checking function to ensure the correct command and address signals are propagating correctly through the Memory Buffer.
- Supports an SMBus protocol interface for access to the MB configuration registers.
- Supports Control Word and Output Inversion features as used in SSTE32882.
- Supports built-in Temperature Sensor with T_{case} readout and three thermal trip point settings (accessed through MB configuration registers).
- Optional Logic Analyzer Interface (LAI) support for Failure Analysis (FA) and debug.

1.2.2 DDR SDRAM

DDR3 SDRAM support:

- Supports DDR3/DDR3L
- Supports 1Gb, 2Gb and 4Gb devices in x4 and x8 configurations
- 576 devices/channel (4 DIMMs/channel, 1, 2, 4 and 8 ranks/DIMM) - actual support varies by channel and individual system design
- 72-bit DDR3 SDRAM buffered memory interface

1.2.3 Byte Group Signal Mapping

The Memory Buffer (MB) HOST interface and DRAM interface DQ/MDQ and DQS/MDQS buses are divided into byte groups, according to Table 1 and Table 2.

Table 1 — DQ and DQS Mapping

		DQ								DQS			
		0	1	2	3	4	5	6	7				
Byte Group	0	DQ[0]	DQ[1]	DQ[2]	DQ[3]	DQ[4]	DQ[5]	DQ[6]	DQ[7]	DQS[0]_t	DQS[0]_c	DQS[9]_t	DQS[9]_c
	1	DQ[8]	DQ[9]	DQ[10]	DQ[11]	DQ[12]	DQ[13]	DQ[14]	DQ[15]	DQS[1]_t	DQS[1]_c	DQS[10]_t	DQS[10]_c
	2	DQ[16]	DQ[17]	DQ[18]	DQ[19]	DQ[20]	DQ[21]	DQ[22]	DQ[23]	DQS[2]_t	DQS[2]_c	DQS[11]_t	DQS[11]_c
	3	DQ[24]	DQ[25]	DQ[26]	DQ[27]	DQ[28]	DQ[29]	DQ[30]	DQ[31]	DQS[3]_t	DQS[3]_c	DQS[12]_t	DQS[12]_c
	4	DQ[32]	DQ[33]	DQ[34]	DQ[35]	DQ[36]	DQ[37]	DQ[38]	DQ[39]	DQS[4]_t	DQS[4]_c	DQS[13]_t	DQS[13]_c
	5	DQ[40]	DQ[41]	DQ[42]	DQ[43]	DQ[44]	DQ[45]	DQ[46]	DQ[47]	DQS[5]_t	DQS[5]_c	DQS[14]_t	DQS[14]_c
	6	DQ[48]	DQ[49]	DQ[50]	DQ[51]	DQ[52]	DQ[53]	DQ[54]	DQ[55]	DQS[6]_t	DQS[6]_c	DQS[15]_t	DQS[15]_c
	7	DQ[56]	DQ[57]	DQ[58]	DQ[59]	DQ[60]	DQ[61]	DQ[62]	DQ[63]	DQS[7]_t	DQS[7]_c	DQS[16]_t	DQS[16]_c
	8	DQ[64]	DQ[65]	DQ[66]	DQ[67]	DQ[68]	DQ[69]	DQ[70]	DQ[71]	DQS[8]_t	DQS[8]_c	DQS[17]_t	DQS[17]_c

Table 2 — MDQ and MDQS Mapping

		MDQ								MDQS			
		0	1	2	3	4	5	6	7				
Byte Group	0	MDQ[0]	MDQ[1]	MDQ[2]	MDQ[3]	MDQ[4]	MDQ[5]	MDQ[6]	MDQ[7]	MDQS[0]_t	MDQS[0]_c	MDQS[9]_t	MDQS[9]_c
	1	MDQ[8]	MDQ[9]	MDQ[10]	MDQ[11]	MDQ[12]	MDQ[13]	MDQ[14]	MDQ[15]	MDQS[1]_t	MDQS[1]_c	MDQS[10]_t	MDQS[10]_c
	2	MDQ[16]	MDQ[17]	MDQ[18]	MDQ[19]	MDQ[20]	MDQ[21]	MDQ[22]	MDQ[23]	MDQS[2]_t	MDQS[2]_c	MDQS[11]_t	MDQS[11]_c
	3	MDQ[24]	MDQ[25]	MDQ[26]	MDQ[27]	MDQ[28]	MDQ[29]	MDQ[30]	MDQ[31]	MDQS[3]_t	MDQS[3]_c	MDQS[12]_t	MDQS[12]_c
	4	MDQ[32]	MDQ[33]	MDQ[34]	MDQ[35]	MDQ[36]	MDQ[37]	MDQ[38]	MDQ[39]	MDQS[4]_t	MDQS[4]_c	MDQS[13]_t	MDQS[13]_c
	5	MDQ[40]	MDQ[41]	MDQ[42]	MDQ[43]	MDQ[44]	MDQ[45]	MDQ[46]	MDQ[47]	MDQS[5]_t	MDQS[5]_c	MDQS[14]_t	MDQS[14]_c
	6	MDQ[48]	MDQ[49]	MDQ[50]	MDQ[51]	MDQ[52]	MDQ[53]	MDQ[54]	MDQ[55]	MDQS[6]_t	MDQS[6]_c	MDQS[15]_t	MDQS[15]_c
	7	MDQ[56]	MDQ[57]	MDQ[58]	MDQ[59]	MDQ[60]	MDQ[61]	MDQ[62]	MDQ[63]	MDQS[7]_t	MDQS[7]_c	MDQS[16]_t	MDQS[16]_c
	8	MDQ[64]	MDQ[65]	MDQ[66]	MDQ[67]	MDQ[68]	MDQ[69]	MDQ[70]	MDQ[71]	MDQS[8]_t	MDQS[8]_c	MDQS[17]_t	MDQS[17]_c

1.3 LRDIMM DDR3 Memory Buffer Block Diagram

Figure 1 is a conceptual block diagram of the LRDIMM Memory Buffer's data flow and its interfaces.

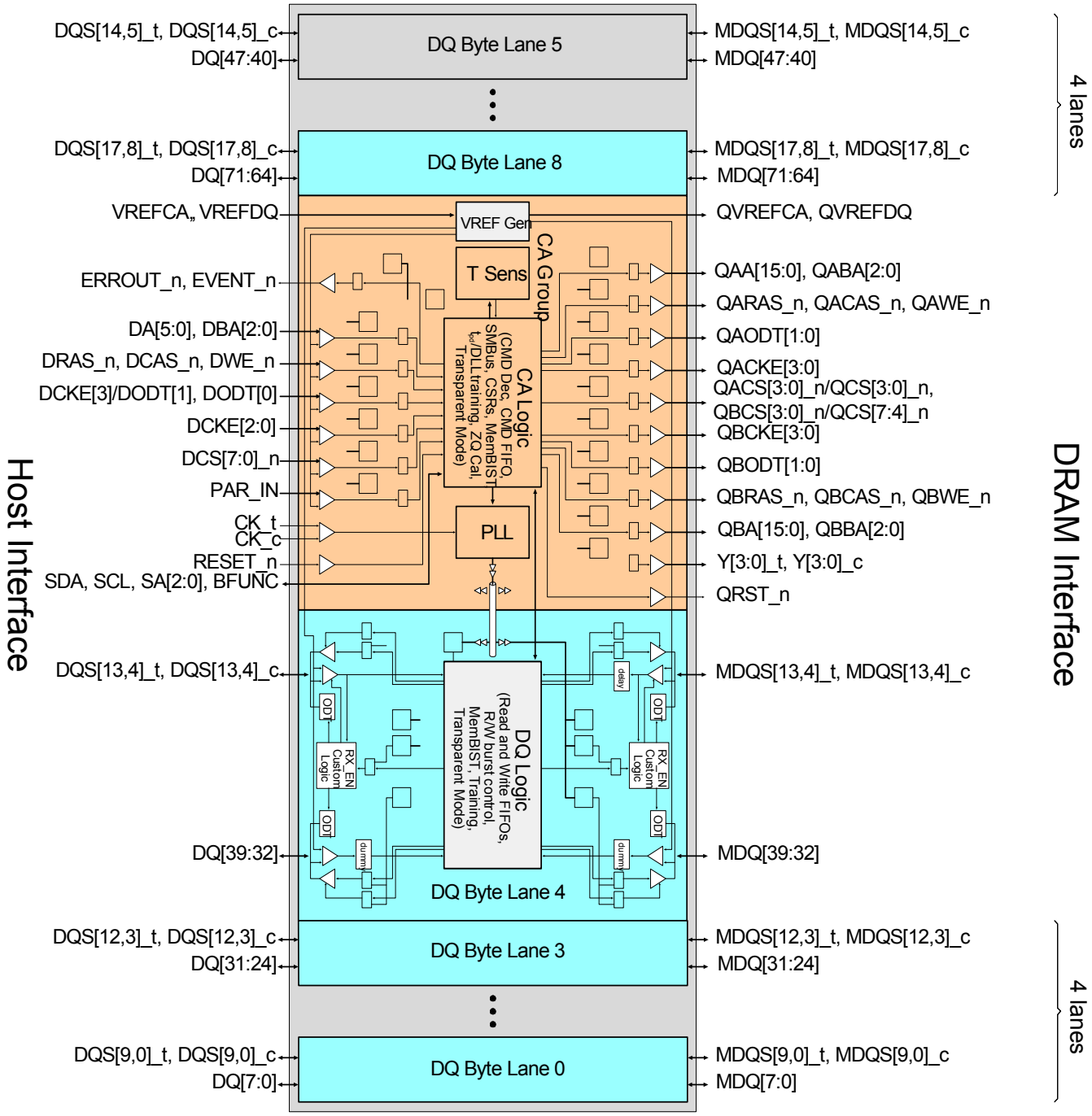


Figure 1 — LRDIMM DDR3 Memory Buffer Block Diagram

1.4 Interfaces

Figure 1 illustrates the LRDIMM Memory Buffer and all of its interfaces. They consist of one HOST interface, one DDR3 DRAM interface and an SMBus interface. The HOST interface connects the LRDIMM Memory Buffer to a host memory controller. The DDR3 DRAM interface supports direct connection to the DDR3 SDRAMs on a Load Reduced DIMM (LRDIMM)

1.4.1 HOST Interface

The LRDIMM Memory Buffer supports one HOST interface, which consists of Command, Address, Control, Clock, Data Strobe and Data. It also supports PAR_IN input as used in SSTE32882.

For the actual pin name and function description of the HOST Interface, please refer to Chapter 3 Pin Description.

1.4.2 DDR3 DRAM Interface

The DDR3 DRAM interface on the LRDIMM Memory Buffer supports direct connection to DDR3 SDRAMs. The DDR3 DRAM interface supports up to 8 ranks of eight banks with 16 row/column address signals, 64 data signals, and eight check-bit signals. There are two copies (A and B) of address and command signals to support DIMM routing and electrical requirements. Either a burst length of eight or a ‘chopped’ burst of four transfers are driven on the data and check-bit lines.

For the actual pin name and function description of the DRAM Interface, please refer to Chapter 3 Pin Description.

1.4.3 SMBus Slave Interface

The LRDIMM Memory Buffer supports an SMBus interface to allow system access to configuration registers and temperature sensor. The Memory Buffer will never be a master on the SMBus, only a slave. Serial SMBus data transfer is supported at 100 kHz.

SMBus access to Memory Buffer may be required to boot a system. It is also required for system diagnostic and debug support.

More information is available in this standard, see clause 13, SMBus.

1.5 References

This Standard is consistent with the following documents:

- JEDEC JESD79-3D, *DDR3 SDRAM Standard*, [1]
- JEDEC JESD82-29, *Definition of the SSTE32882 Registering Clock Driver with Parity and Quad Chip Selects for DDR3/DDR3L/DDR3U RDIMM 1.5 V/1.35 V/1.25 V Applications* [2]
- JEDEC JESD21C, *JEDEC Configurations for Solid State Memories* (DDR3 SDRAM Registered DIMM Design Specification), [3]
- *System Management Bus (SMBus) Specification Version 2.0*, published by www.smbus.org [4]
- JEDEC JESD8-11, *Addendum No. 11 to JESD8 - 1.5 V +/- 0.1 V (Normal Range) and 0.9 V - 1.6 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits* [5]

1.6 Glossary

Term	Definition
MB	Memory Buffer
CA	Command/Address; RAS#, CAS#, WE#, BA[2:0], and A[15:0] signals to the DRAM, or associated I/O pins and wires
CSR	Control and Status Register
DDR	Double Data Rate: a description of contemporary synchronous DRAM characterized by data communications at a rate of two bits per clock cycle per wire
DDR Channel	A DDR channel consists of a data channel with 72 bits of data and an ADDR/CNTRL channel
DLL	Delay-Locked Loop
DIMM	Dual In-Line Memory Module. A packaging arrangement of memory devices on a socketable substrate.
DRAM	Dynamic Random Access Memory
ECC	Error Correction Code
Host	Memory controller agent on a DDR channel
IBT	Input Bus Termination; termination for input-only memory buffer pins, specifically command/address and control signal pins
JEDEC	JEDEC Solid State Technology Association (once known as the Joint Electron Device Engineering Council)
JESD79	JEDEC Standard 79, *DDR SDRAM Specification*
LRDIMM	Load Reduced DIMM
LA	Logic Analyzer
LAI	Logic Analyzer Interface
MRS	Mode Register Set; mode control registers in DDR SDRAM devices
ODT	On-Die Termination; termination for input-output memory buffer pins, specifically data and strobe signal pins
PLL	Phase Locked Loop
PVT	Process, Voltage and Temperature
Rank	A DIMM is organized as one, two, four or eight physical sets of memory, called ranks.
RAS	When not used in reference to a SDRAM signal, RAS is the short form for “Reliability, Availability, Serviceability”
RDIMM	Registered DIMM; contemporary buffered DIMM technology using a registering clock driver to buffer clock, command/address, and control signals to the DRAM devices
SDRAM	Synchronous Dynamic Random Access Memory
SI	Signal Integrity
SMBus	System Management Bus. Mastered by a system management controller to read and write configuration registers. Limited to 100 kHz.
SSC	Spread Spectrum Clocking; a technique for reducing EMI in a clocked digital system by frequency modulating the clock, reducing the peak radiated energy by spreading radiated energy over a frequency band

Term	Definition
SSO	Simultaneously Switching Outputs
Transparent Mode	A mode to provide “pass through” access from ATE tester through the DDR3 Memory Buffer to the SDRAM on LRDIMM
UI	Unit Interval: average time interval between voltage transitions of a signal
V_{SS}	Ground (0V)
V_{DDQ}	I/O buffer voltage for DDR3/DDR3L buffers. Nominally 1.5/1.35V

2 Ballout and Package Information

2.1 588-Ball FBGA (20x38 Array, 25.2x13.5 mm Body Size, 0.65 mm Pitch, MO-301A Variation A) Pin configuration

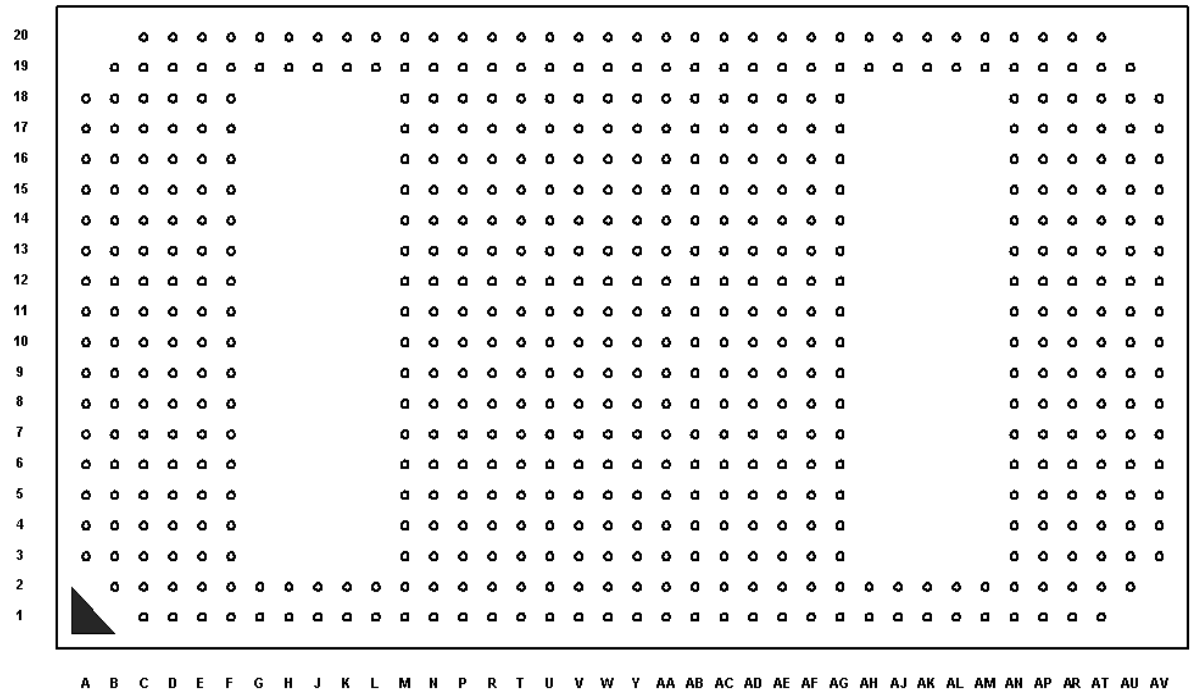


Figure 2 — Pinout Configuration

2.2 Pin Assignments for the LR-DIMM DDR3 Memory Buffer (MB)

Table 3 — 588-Ball FBGA (20x38 Array, 13.5x25.2 mm Body Size, 0.65 mm Pitch, MO-301A Variation A) (Transparent, Top View) - Left Side

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W
20	NB	NB	VSS	DQ7	DQS9_t	DQ2	DQ3	VDD	DQ68	DQS17_t	DQ70	VSS	DQ66	VDD	Y3_c	Y3_t	Y1_t	Y1_c	Y2_c
19	NB	VSS	DQ4	DQ6	DQS9_c	VSS	DQ1	VSS	DQ69	DQS17_c	DQ71	VSS	DQ67	VDD	VSS	PVDD	VSS	PVDD	VSS
18	VSS	VDD	VSS	DQ5	DQS0_c	DQ0	NB	NB	NB	NB	NB	DQS8_t	DQ64	VSS	MDQ68	MDQS17_t	MDQ70	MDQ64	MDQS8_c
17	MDQ5	MDQ4	MDQ0	VSS	DQS0_t	VSS	NB	NB	NB	NB	NB	DQS8_c	DQ65	VSS	MDQ69	MDQS17_c	MDQ71	MDQ65	MDQS8_t
16	MDQS9_t	MDQS9_c	MDQS0_c	MDQS0_t	VDD	QACAS_n	NB	NB	NB	NB	NB	VDD	VDD	VDD	VSS	VDD	VSS	VDD	VSS
15	MDQ6	MDQ7	MDQ2	MDQ1	VDD	QARAS_n	NB	NB	NB	NB	NB	RFU	RFU	VSS	VDD	VSS	VDD	VSS	VDD
14	VSS	VSS	VSS	MDQ3	VDD	QAA15	NB	NB	NB	NB	NB	VDD	VDD	RFU	VSS	VDD	VSS	VDD	VSS
13	DQS1_t	DQS1_c	VSS	VDD	QAA10	QACKE1	NB	NB	NB	NB	NB	QAWE_n	VDD	QAODT1	VDD	VSS	VDD	VSS	VDD
12	VDD	VSS	DQ8	VDD	QACKE0	QAA12	NB	NB	NB	NB	NB	QABA0	QABA2	QAODT0	VSS	RESET_n	VSS	VDD	VSS
11	DQ11	DQ10	DQ9	VDD	QABA1	QACKE2	NB	NB	NB	NB	NB	QAA0	VDD	VSS	VDD	DCKE2	VDD	DA1	VDD
10	DQ15	DQ14	DQ13	VDD	QACKE3	QAA4	NB	NB	NB	NB	NB	QAA3	QACS0_n/QCS0_n	QACS1_n/QCS1_n	QRST_n	DCKE1	DA12	DA6	DA4
9	VDD	VSS	DQ12	VDD	QAA1	QAA6	NB	NB	NB	NB	NB	QACS3_n/QCS3_n	QACS2_n/QCS2_n	VDD	DCKE0	DBA2	DA11	DA3	DA5
8	DQS10_t	DQS10_c	VSS	VDD	VDD	QAA11	NB	NB	NB	NB	NB	QAA5	QAA2	VDD	DA15	DA14	DA9	DA8	DA7
7	VSS	VSS	VSS	MDQ9	VDD	QAA8	NB	NB	NB	NB	NB	QAA13	QAA9	VDD	VDD	ERROUT_n	VDD	VDD	VDD
6	MDQ12	MDQ13	MDQ8	MDQ11	VDD	QAA14	NB	NB	NB	NB	NB	QAA7	VDD	DQ24	DQ25	VSS	MDQ29	MDQS12_t	VSS
5	MDQS10_t	MDQS10_c	MDQS1_c	MDQS1_t	VSS	VDD	NB	NB	NB	NB	NB	VDD	VSS	DQS3_t	DQS3_c	VSS	MDQ30	MDQS12_c	MDQ28
4	MDQ14	MDQ15	MDQ10	VSS	DQS2_t	DQ16	NB	NB	NB	NB	NB	MDQS2_c	VSS	DQ26	DQ27	VSS	MDQ31	MDQS3_c	VSS
3	VSS	VDD	VSS	DQ19	DQS2_c	DQ17	NB	NB	NB	NB	NB	MDQS2_t	VSS	VDD	DQ28	DQ29	VSS	MDQS3_t	MDQ24
2	NB	VSS	DQ18	DQ22	DQS11_c	DQ20	VSS	MDQ20	MDQS11_c	MDQ22	VSS	MDQ16	MDQ18	VSS	DQS12_t	DQS12_c	VSS	MDQ25	VSS
1	NB	NB	VSS	DQ23	DQS11_t	DQ21	VSS	MDQ21	MDQS11_t	MDQ23	VSS	MDQ17	MDQ19	VSS	DQ30	DQ31	VSS	MDQ26	MDQ27

Table 4 — 588-Ball FBGA (20x38 Array, 13.5x25.2 mm Body Size, 0.65 mm Pitch, MO-301A Variation A) (Transparent, Top View) - Right Side

Y2_t	Y0_t	Y0_c	VDD	ZQ	SCL	SA[2]	SA[0]	QVREFCA	VDD	QVREFDQ	VDD	DQ59	DQ58	DQS7_t	DQ63	VSS	NB	NB	20
PVDD	VSS	PVDD	VSS	ZQVSS	SDA	VCCSPD	SA[1]	VREFCA	VSS	VREFDQ	VSS	DQ57	VSS	DQS7_c	DQ62	DQ60	VSS	NB	19
MDQ66	VSS	CK_t	CK_c	VSS	VDD	EVENT_n	BFUNC	NB	NB	NB	NB	NB	DQ56	DQS16_c	DQ61	VSS	VDD	VSS	18
MDQ67	TEST[0]	AVSS	AVDD	AOUT	TEST[2]	VSS	VDD	NB	NB	NB	NB	NB	VSS	DQS16_t	VSS	MDQ58	MDQ63	MDQ62	17
VDD	TEST[1]	VDD	VSS	VDD	VSS	VDD	VSS	NB	NB	NB	NB	NB	QBWE_n	VDD	MDQS7_t	MDQS7_c	MDQS16_c	MDQS16_t	16
VSS	VDD	VSS	VDD	VSS	VDD	QBCAS_n	QBRAS_n	NB	NB	NB	NB	NB	QBBA0	VDD	MDQ59	MDQ57	MDQ61	MDQ60	15
VDD	VSS	VDD	VSS	VDD	VSS	VDD	VDD	NB	NB	NB	NB	NB	QBA0	VDD	MDQ56	VSS	VSS	VSS	14
VSS	VDD	VSS	VDD	VSS	QBCKE1	QBA10	QBA15	NB	NB	NB	NB	NB	QBA3	QBODT1	VDD	VSS	DQS6_c	DQS6_t	13
VDD	VSS	VDD	VSS	VDD	QBCKE0	VDD	VDD	NB	NB	NB	NB	NB	QBA2	QBBA2	VDD	DQ48	VSS	VDD	12
VSS	DCS2_n	DCS4_n	DCS3_n	VSS	QBCKE3	QBBA1	QBA12	NB	NB	NB	NB	NB	QBA5	QBODT0	VDD	DQ49	DQ50	DQ51	11
DA2	DA13	DCS0_n	DCS5_n	DBA1	VDD	QBCKE2	QBA4	NB	NB	NB	NB	NB	QBCS1_n/QCS5_n	QBCS0_n/QCS4_n	VDD	DQ53	DQ54	DQ55	10
PAR_IN	DODT0	DA0	DBA0	DODT1/DCKE3	VSS	QBA1	QBA6	NB	NB	NB	NB	NB	QBCS3_n/QCS7_n	QBCS2_n/QCS6_n	VDD	DQ52	VSS	VDD	9
DCS1_n	DCAS_n	DRAS_n	DA10	DCS6_n	DCS7_n	VDD	VDD	NB	NB	NB	NB	NB	QBA9	VDD	VDD	VSS	DQS15_c	DQS15_t	8
VDD	VDD	VDD	DWE_n	VDD	VDD	QBA11	QBA8	NB	NB	NB	NB	NB	QBA13	VDD	MDQ51	VSS	VSS	VSS	7
MDQ36	MDQS13_t	MDQ37	VSS	DQ32	DQ33	VDD	QBA14	NB	NB	NB	NB	NB	QBA7	VDD	MDQ49	MDQ50	MDQ55	MDQ54	6
VSS	MDQS13_c	MDQ38	VSS	DQS4_t	DQS4_c	VSS	VDD	NB	NB	NB	NB	NB	VDD	VSS	MDQS6_t	MDQS6_c	MDQS15_c	MDQS15_t	5
MDQ32	MDQS4_c	MDQ39	VSS	DQ34	DQ35	VSS	MDQS5_c	NB	NB	NB	NB	NB	DQ40	DQS5_t	VSS	MDQ48	MDQ53	MDQ52	4
VSS	MDQS4_t	VSS	DQ36	DQ37	VDD	VSS	MDQS5_t	NB	NB	NB	NB	NB	DQ41	DQS5_c	DQ45	VSS	VDD	VSS	3
MDQ33	MDQ34	VSS	DQS13_t	DQS13_c	VSS	MDQ40	MDQ43	VSS	MDQ44	MDQS14_t	MDQ47	VSS	DQ42	DQS14_c	DQ46	DQ44	VSS	NB	2
VSS	MDQ35	VSS	DQ38	DQ39	VSS	MDQ41	MDQ42	VSS	MDQ45	MDQS14_c	MDQ46	VSS	DQ43	DQS14_t	DQ47	VSS	NB	NB	1
Y	**AA**	**AB**	**AC**	**AD**	**AE**	**AF**	**AG**	**AH**	**AJ**	**AK**	**AL**	**AM**	**AN**	**AP**	**AR**	**AT**	**AU**	**AV**	

Table 5 — Memory Buffer Signals By Ball Number (Sheet 1 of 7)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	NB	B1	NB	C1	VSS
A2	NB	B2	VSS	C2	DQ18
A3	VSS	B3	VDD	C3	VSS
A4	MDQ14	B4	MDQ15	C4	MDQ10
A5	MDQS10_t	B5	MDQS10_c	C5	MDQS1_c
A6	MDQ12	B6	MDQ13	C6	MDQ8
A7	VSS	B7	VSS	C7	VSS
A8	DQS10_t	B8	DQS10_c	C8	VSS
A9	VDD	B9	VSS	C9	DQ12
A10	DQ15	B10	DQ14	C10	DQ13
A11	DQ11	B11	DQ10	C11	DQ9
A12	VDD	B12	VSS	C12	DQ8
A13	DQS1_t	B13	DQS1_c	C13	VSS
A14	VSS	B14	VSS	C14	VSS
A15	MDQ6	B15	MDQ7	C15	MDQ2
A16	MDQS9_t	B16	MDQS9_c	C16	MDQS0_c
A17	MDQ5	B17	MDQ4	C17	MDQ0
A18	VSS	B18	VDD	C18	VSS
A19	NB	B19	VSS	C19	DQ4
A20	NB	B20	NB	C20	VSS
D1	DQ23	E1	DQS11_t	F1	DQ21
D2	DQ22	E2	DQS11_c	F2	DQ20
D3	DQ19	E3	DQS2_c	F3	DQ17
D4	VSS	E4	DQS2_t	F4	DQ16
D5	MDQS1_t	E5	VSS	F5	VDD
D6	MDQ11	E6	VDD	F6	QAA14
D7	MDQ9	E7	VDD	F7	QAA8
D8	VDD	E8	VDD	F8	QAA11
D9	VDD	E9	QAA1	F9	QAA6
D10	VDD	E10	QACKE3	F10	QAA4
D11	VDD	E11	QABA1	F11	QACKE2
D12	VDD	E12	QACKE0	F12	QAA12
D13	VDD	E13	QAA10	F13	QACKE1
D14	MDQ3	E14	VDD	F14	QAA15
D15	MDQ1	E15	VDD	F15	QARAS_n
D16	MDQS0_t	E16	VDD	F16	QACAS_n
D17	VSS	E17	DQS0_t	F17	VSS
D18	DQ5	E18	DQS0_c	F18	DQ0
D19	DQ6	E19	DQS9_c	F19	VSS

Table 5 — Memory Buffer Signals By Ball Number (Sheet 2 of 7)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
D20	DQ7	E20	DQS9_t	F20	DQ2
G1	VSS	H1	MDQ21	J1	MDQS11_t
G2	VSS	H2	MDQ20	J2	MDQS11_c
G3	NB	H3	NB	J3	NB
G4	NB	H4	NB	J4	NB
G5	NB	H5	NB	J5	NB
G6	NB	H6	NB	J6	NB
G7	NB	H7	NB	J7	NB
G8	NB	H8	NB	J8	NB
G9	NB	H9	NB	J9	NB
G10	NB	H10	NB	J10	NB
G11	NB	H11	NB	J11	NB
G12	NB	H12	NB	J12	NB
G13	NB	H13	NB	J13	NB
G14	NB	H14	NB	J14	NB
G15	NB	H15	NB	J15	NB
G16	NB	H16	NB	J16	NB
G17	NB	H17	NB	J17	NB
G18	NB	H18	NB	J18	NB
G19	DQ1	H19	VSS	J19	DQ69
G20	DQ3	H20	VDD	J20	DQ68
K1	MDQ23	L1	VSS	M1	MDQ17
K2	MDQ22	L2	VSS	M2	MDQ16
K3	NB	L3	NB	M3	MDQS2_t
K4	NB	L4	NB	M4	MDQS2_c
K5	NB	L5	NB	M5	VDD
K6	NB	L6	NB	M6	QAA7
K7	NB	L7	NB	M7	QAA13
K8	NB	L8	NB	M8	QAA5
K9	NB	L9	NB	M9	QACS3_n/ QCS3_n
K10	NB	L10	NB	M10	QAA3
K11	NB	L11	NB	M11	QAA0
K12	NB	L12	NB	M12	QABA0
K13	NB	L13	NB	M13	QAWE_n
K14	NB	L14	NB	M14	VDD
K15	NB	L15	NB	M15	RFU
K16	NB	L16	NB	M16	VDD
K17	NB	L17	NB	M17	DQS8_c
K18	NB	L18	NB	M18	DQS8_t
K19	DQS17_c	L19	DQ71	M19	VSS

Table 5 — Memory Buffer Signals By Ball Number (Sheet 3 of 7)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
K20	DQS17_t	L20	DQ70	M20	VSS
N1	MDQ19	P1	VSS	R1	DQ30
N2	MDQ18	P2	VSS	R2	DQS12_t
N3	VSS	P3	VDD	R3	DQ28
N4	VSS	P4	DQ26	R4	DQ27
N5	VSS	P5	DQS3_t	R5	DQS3_c
N6	VDD	P6	DQ24	R6	DQ25
N7	QAA9	P7	VDD	R7	VDD
N8	QAA2	P8	VDD	R8	DA15
N9	QACS2_n/ QCS2_n	P9	VDD	R9	DCKE0
N10	QACS0_n/ QCS0_n	P10	QACS1_n/ QCS1_n	R10	QRST_n
N11	VDD	P11	VSS	R11	VDD
N12	QABA2	P12	QAODT0	R12	VSS
N13	VDD	P13	QAODT1	R13	VDD
N14	VDD	P14	RFU	R14	VSS
N15	RFU	P15	VSS	R15	VDD
N16	VDD	P16	VDD	R16	VSS
N17	DQ65	P17	VSS	R17	MDQ69
N18	DQ64	P18	VSS	R18	MDQ68
N19	DQ67	P19	VDD	R19	VSS
N20	DQ66	P20	VDD	R20	Y3_c
T1	DQ31	U1	VSS	V1	MDQ26
T2	DQS12_c	U2	VSS	V2	MDQ25
T3	DQ29	U3	VSS	V3	MDQS3_t
T4	VSS	U4	MDQ31	V4	MDQS3_c
T5	VSS	U5	MDQ30	V5	MDQS12_c
T6	VSS	U6	MDQ29	V6	MDQS12_t
T7	ERROUT_n	U7	VDD	V7	VDD
T8	DA14	U8	DA9	V8	DA8
T9	DBA2	U9	DA11	V9	DA3
T10	DCKE1	U10	DA12	V10	DA6
T11	DCKE2	U11	VDD	V11	DA1
T12	RESET_n	U12	VSS	V12	VDD
T13	VSS	U13	VDD	V13	VSS
T14	VDD	U14	VSS	V14	VDD
T15	VSS	U15	VDD	V15	VSS
T16	VDD	U16	VSS	V16	VDD
T17	MDQS17_c	U17	MDQ71	V17	MDQ65
T18	MDQS17_t	U18	MDQ70	V18	MDQ64

Table 5 — Memory Buffer Signals By Ball Number (Sheet 4 of 7)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
T19	PVDD	U19	VSS	V19	PVDD
T20	Y3_t	U20	Y1_t	V20	Y1_c
W1	MDQ27	Y1	VSS	AA1	MDQ35
W2	VSS	Y2	MDQ33	AA2	MDQ34
W3	MDQ24	Y3	VSS	AA3	MDQS4_t
W4	VSS	Y4	MDQ32	AA4	MDQS4_c
W5	MDQ28	Y5	VSS	AA5	MDQS13_c
W6	VSS	Y6	MDQ36	AA6	MDQS13_t
W7	VDD	Y7	VDD	AA7	VDD
W8	DA7	Y8	DCS1_n	AA8	DCAS_n
W9	DA5	Y9	PAR_IN	AA9	DODT0
W10	DA4	Y10	DA2	AA10	DA13
W11	VDD	Y11	VSS	AA11	DCS2_n
W12	VSS	Y12	VDD	AA12	VSS
W13	VDD	Y13	VSS	AA13	VDD
W14	VSS	Y14	VDD	AA14	VSS
W15	VDD	Y15	VSS	AA15	VDD
W16	VSS	Y16	VDD	AA16	TEST[1]
W17	MDQS8_t	Y17	MDQ67	AA17	TEST[0]
W18	MDQS8_c	Y18	MDQ66	AA18	VSS
W19	VSS	Y19	PVDD	AA19	VSS
W20	Y2_c	Y20	Y2_t	AA20	Y0_t
AB1	VSS	AC1	DQ38	AD1	DQ39
AB2	VSS	AC2	DQS13_t	AD2	DQS13_c
AB3	VSS	AC3	DQ36	AD3	DQ37
AB4	MDQ39	AC4	VSS	AD4	DQ34
AB5	MDQ38	AC5	VSS	AD5	DQS4_t
AB6	MDQ37	AC6	VSS	AD6	DQ32
AB7	VDD	AC7	DWE_n	AD7	VDD
AB8	DRAS_n	AC8	DA10	AD8	DCS6_n
AB9	DA0	AC9	DBA0	AD9	DODT1/ DCKE3
AB10	DCS0_n	AC10	DCS5_n	AD10	DBA1
AB11	DCS4_n	AC11	DCS3_n	AD11	VSS
AB12	VDD	AC12	VSS	AD12	VDD
AB13	VSS	AC13	VDD	AD13	VSS
AB14	VDD	AC14	VSS	AD14	VDD
AB15	VSS	AC15	VDD	AD15	VSS
AB16	VDD	AC16	VSS	AD16	VDD
AB17	AVSS	AC17	AVDD	AD17	AOUT
AB18	CK_t	AC18	CK_c	AD18	VSS

Table 5 — Memory Buffer Signals By Ball Number (Sheet 5 of 7)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
AB19	PVDD	AC19	VSS	AD19	ZQVSS
AB20	Y0_c	AC20	VDD	AD20	ZQ
AE1	VSS	AF1	MDQ41	AG1	MDQ42
AE2	VSS	AF2	MDQ40	AG2	MDQ43
AE3	VDD	AF3	VSS	AG3	MDQS5_t
AE4	DQ35	AF4	VSS	AG4	MDQS5_c
AE5	DQS4_c	AF5	VSS	AG5	VDD
AE6	DQ33	AF6	VDD	AG6	QBA14
AE7	VDD	AF7	QBA11	AG7	QBA8
AE8	DCS7_n	AF8	VDD	AG8	VDD
AE9	VSS	AF9	QBA1	AG9	QBA6
AE10	VDD	AF10	QBCKE2	AG10	QBA4
AE11	QBCKE3	AF11	QBBA1	AG11	QBA12
AE12	QBCKE0	AF12	VDD	AG12	VDD
AE13	QBCKE1	AF13	QBA10	AG13	QBA15
AE14	VSS	AF14	VDD	AG14	VDD
AE15	VDD	AF15	QBCAS_n	AG15	QBRAS_n
AE16	VSS	AF16	VDD	AG16	VSS
AE17	TEST[2]	AF17	VSS	AG17	VDD
AE18	VDD	AF18	EVENT_n	AG18	BFUNC
AE19	SDA	AF19	VCCSPD	AG19	SA[1]
AE20	SCL	AF20	SA[2]	AG20	SA[0]
AH1	VSS	AJ1	MDQ45	AK1	MDQS14_c
AH2	VSS	AJ2	MDQ44	AK2	MDQS14_t
AH3	NB	AJ3	NB	AK3	NB
AH4	NB	AJ4	NB	AK4	NB
AH5	NB	AJ5	NB	AK5	NB
AH6	NB	AJ6	NB	AK6	NB
AH7	NB	AJ7	NB	AK7	NB
AH8	NB	AJ8	NB	AK8	NB
AH9	NB	AJ9	NB	AK9	NB
AH10	NB	AJ10	NB	AK10	NB
AH11	NB	AJ11	NB	AK11	NB
AH12	NB	AJ12	NB	AK12	NB
AH13	NB	AJ13	NB	AK13	NB
AH14	NB	AJ14	NB	AK14	NB
AH15	NB	AJ15	NB	AK15	NB
AH16	NB	AJ16	NB	AK16	NB
AH17	NB	AJ17	NB	AK17	NB
AH18	NB	AJ18	NB	AK18	NB

Table 5 — Memory Buffer Signals By Ball Number (Sheet 6 of 7)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
AH19	VREFCA	AJ19	VSS	AK19	VREFDQ
AH20	QVREFCA	AJ20	VDD	AK20	QVREFDQ
AL1	MDQ46	AM1	VSS	AN1	DQ43
AL2	MDQ47	AM2	VSS	AN2	DQ42
AL3	NB	AM3	NB	AN3	DQ41
AL4	NB	AM4	NB	AN4	DQ40
AL5	NB	AM5	NB	AN5	VDD
AL6	NB	AM6	NB	AN6	QBA7
AL7	NB	AM7	NB	AN7	QBA13
AL8	NB	AM8	NB	AN8	QBA9
AL9	NB	AM9	NB	AN9	QBCS3_n/ QCS7_n
AL10	NB	AM10	NB	AN10	QBCS1_n/ QCS5_n
AL11	NB	AM11	NB	AN11	QBA5
AL12	NB	AM12	NB	AN12	QBA2
AL13	NB	AM13	NB	AN13	QBA3
AL14	NB	AM14	NB	AN14	QBA0
AL15	NB	AM15	NB	AN15	QBBA0
AL16	NB	AM16	NB	AN16	QBWE_n
AL17	NB	AM17	NB	AN17	VSS
AL18	NB	AM18	NB	AN18	DQ56
AL19	VSS	AM19	DQ57	AN19	VSS
AL20	VDD	AM20	DQ59	AN20	DQ58
AP1	DQS14_t	AR1	DQ47	AT1	VSS
AP2	DQS14_c	AR2	DQ46	AT2	DQ44
AP3	DQS5_c	AR3	DQ45	AT3	VSS
AP4	DQS5_t	AR4	VSS	AT4	MDQ48
AP5	VSS	AR5	MDQS6_t	AT5	MDQS6_c
AP6	VDD	AR6	MDQ49	AT6	MDQ50
AP7	VDD	AR7	MDQ51	AT7	VSS
AP8	VDD	AR8	VDD	AT8	VSS
AP9	QBCS2_n/ QCS6_n	AR9	VDD	AT9	DQ52
AP10	QBCS0_n/ QCS4_n	AR10	VDD	AT10	DQ53
AP11	QBODT0	AR11	VDD	AT11	DQ49
AP12	QBBA2	AR12	VDD	AT12	DQ48
AP13	QBODT1	AR13	VDD	AT13	VSS
AP14	VDD	AR14	MDQ56	AT14	VSS
AP15	VDD	AR15	MDQ59	AT15	MDQ57
AP16	VDD	AR16	MDQS7_t	AT16	MDQS7_c

Table 5 — Memory Buffer Signals By Ball Number (Sheet 7 of 7)

Ball No.	Signal		Ball No.	Signal		Ball No.	Signal
AP17	DQS16_t		AR17	VSS		AT17	MDQ58
AP18	DQS16_c		AR18	DQ61		AT18	VSS
AP19	DQS7_c		AR19	DQ62		AT19	DQ60
AP20	DQS7_t		AR20	DQ63		AT20	VSS
AU1	NB		AV1	NB			
AU2	VSS		AV2	NB			
AU3	VDD		AV3	VSS			
AU4	MDQ53		AV4	MDQ52			
AU5	MDQS15_c		AV5	MDQS15_t			
AU6	MDQ55		AV6	MDQ54			
AU7	VSS		AV7	VSS			
AU8	DQS15_c		AV8	DQS15_t			
AU9	VSS		AV9	VDD			
AU10	DQ54		AV10	DQ55			
AU11	DQ50		AV11	DQ51			
AU12	VSS		AV12	VDD			
AU13	DQS6_c		AV13	DQS6_t			
AU14	VSS		AV14	VSS			
AU15	MDQ61		AV15	MDQ60			
AU16	MDQS16_c		AV16	MDQS16_t			
AU17	MDQ63		AV17	MDQ62			
AU18	VDD		AV18	VSS			
AU19	VSS		AV19	NB			
AU20	NB		AV20	NB			

2.3 Package Information

Refer to Registered Outline MO-301A published by JC-11 committee for LR-DIMM DDR3 MB package info.

3 Pin Descriptions

3.1 Pin Description

Table 6 — Memory Buffer Signal Types

Buffer Direction	Description
I	Input signal
O	Output signal
A	Analog
I/O	Bidirectional (input/output) signal
NC	No Connect

Table 7 — Pin Description (Sheet 1 of 3)

Signal	Type	Count	Description
Host Interface			
DQ[71:64]	I/O	8	**Check bits** (re: DQ for ECC DRAM)
DQ[63:0]	I/O	64	**Data**
DQS[17:0]_t	I/O	18	**Data Strobe:** DDR3 data and check-bit strobe.
DQS[17:0]_c	I/O	18	**Data Strobe Complement:** DDR3 data and check-bit strobe complements.
DA[15:0]	I	16	**Address:** Used for providing multiplexed row and column address to SDRAM.
DBA[2:0]	I	3	**Bank Active:** Used to select the bank within a rank.
DRAS_n	I	1	**Row Address Strobe:** Used with DCS_n, DCAS_n, and DWE_n to specify the SDRAM command.
DCAS_n	I	1	**Column Address Strobe:** Used with DCS_n, DRAS_n, and DWE_n to specify the SDRAM command.
DWE_n	I	1	**Write Enable:** Used with DCS_n, DCAS_n, and DRAS_n to specify the SDRAM command.
DCS[7:0]_n	I	8	**Chip Select:** Used with DCAS_n, DRAS_n, and DWE_n to specify the SDRAM command. These signals are used for selecting one of eight SDRAM ranks. DCS0_n is used to select the first rank, DCS1_n is used to select the second rank...., and DCS7_n is used to select the 8^{th} rank
DCKE[2:0]	I	3	**Clock Enable**
DCKE[3]/DODT[1]	I	1	Clock Enable or On-Die-Termination (selection controlled by Control Word F0RC6)
DODT[0]	I	1	**On-Die-Termination:** Dynamic ODT enables for each DIMM on the channel
CK_t/CK_c	I	2	**Differential clock input**

Table 7 — Pin Description (Sheet 2 of 3)

Signal	Type	Count	Description
PAR_IN	I	1	**Parity Input**
ERROUT_n	O	1	**Parity error output:** An Open Drain output. When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs
DRAM Interface			
MDQ[71:64]	I/O	8	**Check bits** (re: DQ for ECC DRAM)
MDQ[63:0]	I/O	64	**Data**
MDQS[17:0]_t	I/O	18	**DRAM Data Strobe:** DDR3 data and check-bit strobe.
MDQS[17:0]_c	I/O	18	**DRAM Data Strobe Complement:** DDR3 data and check-bit strobe complements.
QAA[15:0], QBA[15:0]	O	32	**Address (A, B Copy):** Used for providing multiplexed row and column address to SDRAM.
QABA[2:0], QBBA[2:0]	O	6	**Bank Active (A, B Copy):** Used to select the bank within a rank.
QARAS_n, QBRAS_n	O	2	**Row Address Strobe (A, B Copy):** Used with CS_n, CAS_n, and WE_n to specify the SDRAM command.
QACAS_n, QBCAS_n	O	2	**Column Address Strobe (A, B Copy):** Used with CS_n, RAS_n, and WE_n to specify the SDRAM command.
QAWE_n, QBWE_n	O	2	**Write Enable (A, B Copy):** Used with DCS_n, DCAS_n, and DRAS_n to specify the SDRAM command.
QACS[3:0]_n/ QCS[3:0]_n	O	4	**Chip select (A copy)/(Single copy) lower 4 chip-selects for 8-rank case:** Used with CAS_n, RAS_n, and WE_n to specify the SDRAM command. These signals are used for selecting one of eight physical ranks. CS0_n is used to select the 1st rank, CS1_n is used to select the 2nd rank, CS2_n is used to select the 3rd rank, and CS3_n is used to select the 4th rank.
QBCS[3:0]_n/ QCS[7:4]_n	O	4	**Chip select (B copy)/(Single copy) upper 4 chip-selects for 8-rank case:** Used with CAS_n, RAS_n, and WE_n to specify the SDRAM command. These signals are used for selecting one of eight physical ranks. CS0_n is used to select the 1st rank (or 5th rank in the 8R case), CS1_n is used to select the 2nd rank (or 6th rank in the 8R case), CS2_n is used to select the 3rd rank (or 7th rank in the 8R case), and CS3_n is used to select the 4th rank (or 8th rank in the 8R case).
QACKE[3:0], QBCKE[3:0]	O	8	**Clock Enable (A, B Copy)**
QAODT[1:0], QBODT[1:0]	O	4	**DRAM On-Die-Termination Control (A, B Copy)**
Y[3:0]_t/Y[3:0]_c	O	8	Differential DRAM clock.
System Management			
SCL	I/O	1	SMBus Clock
SDA	I/O	1	SMBus Address/Data
SA[2:0]	I	3	DIMM Select ID (SMBus device address)
EVENT_n	O	1	Temperature trip point event pin
Reset			

Table 7 — Pin Description (Sheet 3 of 3)

Signal	Type	Count	Description
RESET_n	I	1	Asynchronous Power Good Reset
QRST_n	O	1	Buffered Reset to DRAM (if used on DIMM)
Miscellaneous Test			
TEST[2:0]	NC	3	Pin for debug and test. Must be floated on DIMM.
AOUT	NC	1	Test output pin. Must be floated on DIMM
ZQ	A	1	ZQ Calibration resistor
ZQVSS	A	1	ZQ Calibration resistor ground reference
CA and DQ Reference Supplies			
VREFCA	A	1	CA receiver reference voltage input from Host
QVREFCA	A	1	CA receiver reference voltage output to DRAM
VREFDQ	A	1	DQ receiver reference voltage input from Host
QVREFDQ	A	1	DQ receiver reference voltage output to DRAM
Power Supplies			
VDD	A	103	Nominal supply for DDR I/O (or Core if apply)
VSS	A	129	Ground
AVDD	A	1	Analog Power Supply
AVSS	A	1	Analog Ground
PVDD	A	4	PLL Clock driver supply
VCCSPD	A	1	SPD Power Supply
Other pins			
BFUNC	I	1	Buffer Function Bit: When BFUNC = 0, MB is used as a regular buffer on LR-DIMM. When BFUNC = 1, MB is used as a buffer for LAI function. On LR-DIMM, BFUNC is tied to Ground
RFU	NC	3	Reserved for Future Use. Must be floated on DIMM.
No Ball	172		
SUM of all pins	588		

4 Host Interface Protocol and Requirement

4.1 MB Modes of operation

The MB operates in one of two modes: Direct Rank Addressing and Rank Multiplication. The mode of operation is based on both the DIMM configuration and the configuration register programming. In most cases a DIMM can be programmed to operate in either mode, although there are DIMM types where the specific configuration allows for only one mode. For instance a 2 rank LRDIMM can only operate in Direct Rank Addressing mode.

For DIMMs which can operate in either mode the host controller determines which mode will be used and programs the DIMM accordingly. This determination is up the host and may involve the platform configuration (i.e. the number of chip selects supplied to the DIMM socket), performance trade-offs, and the capabilities of the host.

Within the Rank Multiplication mode there may be sub-modes which the host can choose. An 8 rank DIMM could be addressed as two logical ranks of 4 sub-ranks each (RM=4), or 4 logical ranks of 2 sub-ranks each (RM=2). The former would use two chip selects from the host while the latter would use four.

Table 8 — Modes of operation for each DIMM type

Physical Ranks	Mode (Direct or RM)	Host DCS_n signals used	RM Factor	Comments
1	Direct	1	NA	Direct Rank Addressing is the only choice
2	Direct	2	NA	Direct Rank Addressing is the only choice
4	Direct	4	NA	Available on a platform which supplies 4 chip selects to the DIMM socket.
4	RM	2	RM=2	
8	Direct	8	NA	The 8 DCS mode may not be supported on the DIMM.
8	RM	4	RM=2	Available on a platform which supplies 4 chip selects to the DIMM socket. Not available for 4Gbit DRAM devices since this would require A16 from the host, which is muxed with DCS2_n.
8	RM	2	RM=4	

4.1.1 Direct Rank Addressing Mode

Direct Rank Addressing works like a standard RDIMM. The host controller provides a chip select for each physical rank on the DIMM. Like the SSTE32882 register the MB will pass the DCS_n input from the host to the appropriate QCS_n outputs to the DRAMs. The DCS_n is not passed through under the following conditions:

- A Register Control Word is being written (chip selects 0 & 1 are active at the same time).
- All DCKE inputs to the MB are low and the CKE Power Down Mode Enable bit is set. The MB ignores the DCS inputs in this case.
- Soft CKE commands.

There is no special handling of refresh commands in Direct Rank Addressing mode. Any of the three CKE modes may be used with Direct Rank Addressing Mode.

As with RDIMMs, all 8 banks of each physical rank are exposed to the host controller, and may be all opened, adhering to the DRAM specifications.

4.1.2 Rank Multiplication Mode

In the Rank Multiplication Mode, multiple (2 or 4) physical ranks appear to the host controller as a single logical rank of a larger size. This is done by utilizing additional row address bits during the activate command as sub-rank select bits. The read and write commands do not require additional sub-rank select bits from the host since the sub-rank information is stored in the MB from the Activate command. Other commands such as Refresh may optionally use rank select bits based on configuration register settings. See the Rank Multiplication Command Details below.

The basic operation is as follows, assuming an 8 rank DIMM with 1Gbit x4 DRAMs using two host chip selects. Each host chip select will address 4 physical ranks of memory (RM=4). 1Gbit x4 DRAMs use A13:0 as row address bits, so A15 and A14 will be the two sub-rank select bits, or RM bits. DCS0_n will address physical ranks 0, 2, 4, and 6, while DCS1_n will address ranks 1, 3, 5, and 7.

Table 9 — Rank Multiplication Command Details

	Command	DCS_n	A15:14 (RM bits)	BA2:0	Physical Rank	Comment
1	Activate	0	01	100	2	MB registers that bank 4 for DCS0_n is open in Rank 2
2	Read	0	NA	100	2	Goes to Rank 2 since most recent Activate for Bank 4 DCS0_n was to Rank 2 (Uses RM bits stored above).
3	Activate	0	11	011	6	
4	Activate	1	00	011	1	This is legal since bank 3 can be opened independently in different logical ranks.
5	Write	0	NA	100	2	Again uses RM bits from the first step.
6	Read	0	NA	011	6	Most recent activate for bank 3 of DCS0 was to Rank 6
7	Read	1	NA	011	1	Most recent activate for bank 3 of DCS1 was to Rank 1
8	Precharge Single	0	NA	100	0, 2, 4, 6	Precharge is broadcast to all sub-ranks (this assumes MB is configured to broadcast precharges). Only rank 2 has a page open in bank 4. The other ranks do nothing since bank 4 is already closed.

Even though each physical rank has 8 banks which may be opened, only 8 banks in total are exposed to the host controller for each logical rank. At any given time a specific bank number can be open in only one of the sub-ranks. Effectively this increases the number of rows in each bank, which is what is done in a larger DRAM technology. A total of 8 banks per logical rank can be open at once. These open banks could all be in the same sub-rank, or scattered throughout the sub-ranks. This is solely based on the RM bits (A15:14 in the example above) during the activates.

Logical ranks are independent of each other. Each logical rank exposes 8 banks to the host. So in steps 3 and 4 above, bank 3 is open in two different physical ranks simultaneously because they are part of different logical ranks.

The MB is required to store the RM bits on each activate. They must be stored separately for each bank within each logical rank.

For two logical ranks this is 2 RM bits times 8 banks times 2 logical ranks.
For four logical ranks this is 1 RM bit times 8 banks times 4 logical ranks.

Both cases support the max 8 physical ranks.

4.1.2.1 RM bits for each configuration

Table 10 lists the rank multiplication bits used for each configuration.

Table 10 — RM bits for each DIMM type.

DRAM Tech	Physical ranks	Logical Ranks	RM Factor	Host Row Address Bits	RM bit(s)	Row address bits used by DRAM	Logical Rank size	DIMM size, x4 DRAMs	DIMM size, x8 DRAMs
1 Gbit	4	2	2	A14:0	A14	A13:0	2 Gbit	8 Gbytes	4 Gbytes
1 Gbit	8	2	4	A15:0	A15:14	A13:0	4 Gbit	16 Gbytes	8 Gbytes
1 Gbit	8	4	2	A14:0	A14	A13:0	2 Gbit	16 Gbytes	8 Gbytes
2 Gbit	4	2	2	A15:0	A15	A14:0	4 Gbit	16 Gbytes	8 Gbytes
2 Gbit	8	2	4	A16:0	A16:15	A14:0	8 Gbit	32 Gbytes	16 Gbytes
2 Gbit	8	4	2	A15:0	A15	A14:0	4 Gbit	32 Gbytes	16 Gbytes
4 Gbit	4	2	2	A16:0	A16	A15:0	8 Gbit	32 Gbytes	16 Gbytes
4 Gbit	8	2	4	A17:0	A17:16	A15:0	16 Gbit	64 Gbytes	32 Gbytes
4 Gbit	8	4	2	**Not Possible - A16 shared with DCS2_n**					

All combinations using Rank Multiplication are listed in Table 10. x4 and x8 DRAMs use the same row address bits, so the RM bits are the same for both.

Since A17 and A16 on the DIMM are muxed with DCS3_n and DCS2_n, the final row in Table 10 is not possible as A16 and CS2_n cannot be used at the same time.

4.1.2.2 Rank Decoding

Table 11, Table 12, Table 13, and Table 14 show the rank decoding for each mode of operation, as well as the matching of the QCS_n signals to the DCKE inputs and QCKE outputs.

Table 11 — Normal and Rank Multiplication Control Signal Connectivity without Rank 1 and Rank 5 Swap (F[0]RC2 DA4 = 1b)

Description	# Physical Ranks	DIMM Physical Rank #	Host DCS[]_n	Buffer Logical QCS Assertion	Buffer QACS[]_n	Buffer QBCS[]_n	Host CKE F[0]RC6[DA4, DA3] = 00 or 10	Host CKE F[0]RC6 [DA4, DA3] = 01	Buffer QACKE assertion	Buffer QBCKE assertion
Normal Mode (No Rank Multiplication)	1	0	DCS[0]_n	QCS0	QACS[0]_n	QBCS[0]_n	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
	2	0	DCS[0]_n	QCS0	QACS[0]_n	QBCS[0]_n	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		1 (m)	DCS[1]_n	QCS1	QACS[1]_n	QBCS[1]_n	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
	4	0	DCS[0]_n	QCS0	QACS[0]_n	QBCS[0]_n	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		1 (m)	DCS[1]_n	QCS1	QACS[1]_n	QBCS[1]_n	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
		2	DCS[2]_n	QCS2	QACS[2]_n	QBCS[2]_n	DCKE[0]	DCKE[2]	QACKE[2]	QBCKE[2]
		3 (m)	DCS[3]_n	QCS3	QACS[3]_n	QBCS[3]_n	DCKE[1]	DCKE[3]	QACKE[3]	QBCKE[3]
2 Way Rank Multi-plication	4	0	DCS[0]_n	QCS0	QACS[0]_n	QBCS[0]_n	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		2		QCS2	QACS[2]_n	QBCS[2]_n		DCKE[2]	QACKE[2]	QBCKE[2]
		1 (m)	DCS[1]_n	QCS1	QACS[1]_n	QBCS[1]_n	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
		3 (m)		QCS3	QACS[3]_n	QBCS[3]_n		DCKE[3]	QACKE[3]	QBCKE[3]
	8	0	DCS[0]_n	QCS0	QACS[0]_n	-	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		4		QCS4	-	QBCS[0]_n				
		1 (m)	DCS[1]_n	QCS1	QACS[1]_n	-	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
		5 (m)		QCS5	-	QBCS[1]_n				
		2	DCS[2]_n	QCS2	QACS[2]_n	-	DCKE[0]	DCKE[2]	QACKE[2]	QBCKE[2]
		6		QCS6	-	QBCS[2]_n				
		3 (m)	DCS[3]_n	QCS3	QACS[3]_n	-	DCKE[1]	DCKE[3]	QACKE[3]	QBCKE[3]
		7 (m)		QCS7	-	QBCS[3]_n				
4 Way Rank Multi-plication	8	0	DCS[0]_n	QCS0	QACS[0]_n	-	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		2		QCS2	QACS[2]_n	-		DCKE[2]	QACKE[2]	QBCKE[2]
		4		QCS4	-	QBCS[0]_n		DCKE[0]	QACKE[0]	QBCKE[0]
		6		QCS6	-	QBCS[2]_n		DCKE[2]	QACKE[2]	QBCKE[2]
		1 (m)	DCS[1]_n	QCS1	QACS[1]_n	-	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
		3 (m)		QCS3	QACS[3]_n	-		DCKE[3]	QACKE[3]	QBCKE[3]
		5 (m)		QCS5	-	QBCS[1]_n		DCKE[1]	QACKE[1]	QBCKE[1]
		7 (m)		QCS7	-	QBCS[3]_n		DCKE[3]	QACKE[3]	QBCKE[3]

NOTE For 4 Rank x4 QDP DIMM (one row) Raw Card, QxCKE[0] is connected to DIMM physical Rank 0 and Rank 2. QxCKE[1] is connected to DIMM physical Rank 1 and Rank 3.

Table 12 — Normal and Rank Multiplication Control Signal Connectivity with Rank 1 and Rank 5 Swap (F[0]RC2 DA4 = 0b)

Description	# Physical Ranks	DIMM Physical Rank #	Host DCS[]_n	Buffer Logical QCS Assertion	Buffer QACS[]_n	Buffer QBCS[]_n	Host CKE F[0]RC6[DA4, DA3] = 00 or 10	Host CKE F[0]RC6 [DA4, DA3] = 01	Buffer QACKE assertion	Buffer QBCKE assertion
Normal Mode (No Rank Multiplication)	1	0	DCS[0]_n	QCS0	QACS[0]_n	QBCS[0]_n	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
	2	0	DCS[0]_n	QCS0	QACS[0]_n	QBCS[0]_n	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		1 (m)	DCS[1]_n	QCS1	QACS[1]_n	QBCS[1]_n	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
	4	0	DCS[0]_n	QCS0	QACS[0]_n	QBCS[0]_n	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		1 (m)	DCS[1]_n	QCS1	QACS[1]_n	QBCS[1]_n	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
		2	DCS[2]_n	QCS2	QACS[2]_n	QBCS[2]_n	DCKE[0]	DCKE[2]	QACKE[2]	QBCKE[2]
		3 (m)	DCS[3]_n	QCS3	QACS[3]_n	QBCS[3]_n	DCKE[1]	DCKE[3]	QACKE[3]	QBCKE[3]
2 Way Rank Multi-plication	4	0	DCS[0]_n	QCS0	QACS[0]_n	QBCS[0]_n	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		2		QCS2	QACS[2]_n	QBCS[2]_n		DCKE[2]	QACKE[2]	QBCKE[2]
		1 (m)	DCS[1]_n	QCS1	QACS[1]_n	QBCS[1]_n	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
		3 (m)		QCS3	QACS[3]_n	QBCS[3]_n		DCKE[3]	QACKE[3]	QBCKE[3]
	8	0	DCS[0]_n	QCS0	QACS[0]_n	-	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		4		QCS4	-	QBCS[0]_n				
		1 (m)	DCS[1]_n	QCS1	QBCS[1]_n	-	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
		5 (m)		QCS5	-	QACS[1]_n				
		2	DCS[2]_n	QCS2	QACS[2]_n	-	DCKE[0]	DCKE[2]	QACKE[2]	QBCKE[2]
		6		QCS6	-	QBCS[2]_n				
		3 (m)	DCS[3]_n	QCS3	QACS[3]_n	-	DCKE[1]	DCKE[3]	QACKE[3]	QBCKE[3]
		7 (m)		QCS7	-	QBCS[3]_n				
4 Way Rank Multi-plication	8	0	DCS[0]_n	QCS0	QACS[0]_n	-	DCKE[0]	DCKE[0]	QACKE[0]	QBCKE[0]
		2		QCS2	QACS[2]_n	-		DCKE[2]	QACKE[2]	QBCKE[2]
		4		QCS4	-	QBCS[0]_n		DCKE[0]	QACKE[0]	QBCKE[0]
		6		QCS6	-	QBCS[2]_n		DCKE[2]	QACKE[2]	QBCKE[2]
		1 (m)	DCS[1]_n	QCS1	QBCS[1]_n	-	DCKE[1]	DCKE[1]	QACKE[1]	QBCKE[1]
		3 (m)		QCS3	QACS[3]_n	-		DCKE[3]	QACKE[3]	QBCKE[3]
		5 (m)		QCS5	-	QACS[1]_n		DCKE[1]	QACKE[1]	QBCKE[1]
		7 (m)		QCS7	-	QBCS[3]_n		DCKE[3]	QACKE[3]	QBCKE[3]

NOTE For 4 Rank x4 QDP DIMM (one row) Raw Card, QxCKE[0] is connected to DIMM physical Rank 0 and Rank 2. QxCKE[1] is connected to DIMM physical Rank 1 and Rank 3.

Host to DRAM CS Mapping

DCS[0]_n only goes to EVEN numbered QCS[x]_n ranks

DCS[1]_n only goes to ODD numbered QCS[x]_n ranks

Table 13 — Normal (1:1), 2 Way (1:2) and 4 Way (1:4) Rank Multiplication Control Signal Decoding without Rank 1 and Rank 5 Swap (F[0]RC2 DA4 = 1b)

F0RC15	Description	# DCS	CS [1]_n	CS [0]_n	A[17]/ CS [3]_n	A[16]/ CS [2]_n	A [15]	A [14]	Rank #	8 Rank QBCS[3:0]_n	8 Rank QACS[3:0]_n	1,2,4 Rank QBCS[3:0]_n	1,2,4 Rank QACS[3:0]_n	Comment
0000	Normal Mode (No Rank Multiplication)	1, 2 or 4	0	1	0	1	x	x	1, 3	-	-	0101	0101	
			0	1	1	0	x	x	1, 2	-	-	1001	1001	
			0	1	1	1	x	x	1	-	-	1101	1101	
			1	0	0	1	x	x	0, 3	-	-	0110	0110	
			1	0	1	0	x	x	0, 2			1010	1010	
			1	0	1	1	x	x	0	-	-	1110	1110	
			1	1	0	0	x	x	2, 3	-	-	0011	0011	
			1	1	0	1	x	x	3	-	-	0111	0111	
			1	1	1	0	x	x	2	-	-	1011	1011	
			1	1	1	1	x	x	x	-	-	1111	1111	
			0	0	x	x	x	x	RCW	-	-	1111	1111	RCW
0001	2 Way Rank Multi-plication using A[14]	2	1	0	x	x	x	0	0	-	-	1110	1110	1 Gbit DDR3 SDRAM
			1	0	x	x	x	1	2	-	-	1011	1011	
			0	1	x	x	x	0	1	-	-	1101	1101	
			0	1	x	x	x	1	3	-	-	0111	0111	
		4	1	0	1	1	x	0	0	1111	1110	-	-	
			1	0	1	1	x	1	4	1110	1111	-	-	
			0	1	1	1	x	0	1	1111	1101	-	-	
			0	1	1	1	x	1	5	1101	1111	-	-	
			1	1	1	0	x	0	2	1111	1011	-	-	
			1	1	1	0	x	1	6	1011	1111	-	-	
			1	1	0	1	x	0	3	1111	0111	-	-	
			1	1	0	1	x	1	7	0111	1111	-	-	
		2 or 4	1	1	1	1	x	x	x	1111	1111	1111	1111	
			0	0	x	x	x	x	RCW	1111	1111	1111	1111	RCW
0010	2 Way Rank Multi-plication using A[15]	2	1	0	x	x	0	x	0	-	-	1110	1110	2 Gbit DDR3 SDRAM
			1	0	x	x	1	x	2	-	-	1011	1011	
			0	1	x	x	0	x	1	-	-	1101	1101	
			0	1	x	x	1	x	3	-	-	0111	0111	
		4	1	0	1	1	0	x	0	1111	1110	-	-	
			1	0	1	1	1	x	4	1110	1111	-	-	
			0	1	1	1	0	x	1	1111	1101	-	-	
			0	1	1	1	1	x	5	1101	1111	-	-	
			1	1	1	0	0	x	2	1111	1011	-	-	
			1	1	1	0	1	x	6	1011	1111	-	-	
			1	1	0	1	0	x	3	1111	0111	-	-	
			1	1	0	1	1	x	7	0111	1111	-	-	
		2 or 4	1	1	1	1	x	x	x	1111	1111	1111	1111	
			0	0	x	x	x	x	RCW	1111	1111	1111	1111	RCW

Table 13 — Normal (1:1), 2 Way (1:2) and 4 Way (1:4) Rank Multiplication Control Signal Decoding without Rank 1 and Rank 5 Swap (F[0]RC2 DA4 = 1b)

F0RC15	Description	# DCS	CS [1]_n	CS [0]_n	A[17]/ CS [3]_n	A[16]/ CS [2]_n	A [15]	A [14]	Rank #	8 Rank QBCS[3:0]_n	8 Rank QACS[3:0]_n	1,2,4 Rank QBCS[3:0]_n	1,2,4 Rank QACS[3:0]_n	Comment
0011	2 Way Rank Multi-plication using A[16]	2	1	0	x	0	x	x	0	-	-	1110	1110	4 Gbit DDR3 SDRAM
			1	0	x	1	x	x	2	-	-	1011	1011	
			0	1	x	0	x	x	1	-	-	1101	1101	
			0	1	x	1	x	x	3	-	-	0111	0111	
		4	Not Supported							N/A	N/A	N/A	N/A	
		2 or 4	1	1	1	x	x	x	x	-	-	1111	1111	
			0	0	x	x	x	x	RCW	1111	1111	1111	1111	RCW
0101	4 Way Rank Multi-plication using A[15:14]	2	1	0	x	x	0	0	0	1111	1110	-	-	1 Gbit DDR3 SDRAM
			1	0	x	x	0	1	2	1111	1011	-	-	
			1	0	x	x	1	0	4	1110	1111	-	-	
			1	0	x	x	1	1	6	1011	1111	-	-	
			0	1	x	x	0	0	1	1111	1101	-	-	
			0	1	x	x	0	1	3	1111	0111	-	-	
			0	1	x	x	1	0	5	1101	1111	-	-	
			0	1	x	x	1	1	7	0111	1111	-	-	
			1	1	x	x	x	x	x	1111	1111	-	-	
			0	0	x	x	x	x	RCW	1111	1111	-	-	RCW
0110	4 Way Rank Multi-plication using A[16:15]	2	1	0	x	0	0	x	0	1111	1110	-	-	2 Gbit DDR3 SDRAM Host drives CS#[2] as A[16]
			1	0	x	0	1	x	2	1111	1011	-	-	
			1	0	x	1	0	x	4	1110	1111	-	-	
			1	0	x	1	1	x	6	1011	1111	-	-	
			0	1	x	0	0	x	1	1111	1101	-	-	
			0	1	x	0	1	x	3	1111	0111	-	-	
			0	1	x	1	0	x	5	1101	1111	-	-	
			0	1	x	1	1	x	7	0111	1111	-	-	
			1	1	x	x	x	x	x	1111	1111	-	-	
			0	0	x	x	x	x	RCW	1111	1111	-	-	RCW
0111	4 Way Rank Multi-plication using A[17:16]	2	1	0	0	0	x	x	0	1111	1110	-	-	4 Gbit DDR3 SDRAM Host drives CS#[3:2] as A[17:16]
			1	0	0	1	x	x	2	1111	1011	-	-	
			1	0	1	0	x	x	4	1110	1111	-	-	
			1	0	1	1	x	x	6	1011	1111	-	-	
			0	1	0	0	x	x	1	1111	1101	-	-	

Table 14 — Normal (1:1), 2 Way (1:2) and 4 Way (1:4) Rank Multiplication Control Signal Decoding with Rank 1 and Rank 5 Swap (F[0]RC2 DA4 = 0b)

F0RC15	Description	# DCS	CS [1]_n	CS [0]_n	A[17]/ CS [3]_n	A[16]/ CS [2]_n	A [15]	A [14]	Rank #	8 Rank QBCS [3:0]_n	8 Rank QACS[3:0]_n	1,2,4 Rank QBCS[3:0]_n	1,2,4 Rank QACS[3:0]_n	Comment
0000	Normal Mode (No Rank Multiplication)	1, 2 or 4	0	1	0	1	x	x	1, 3	-	-	0101	0101	
			0	1	1	0	x	x	1, 2	-	-	1001	1001	
			0	1	1	1	x	x	1	-	-	1101	1101	
			1	0	0	1	x	x	0, 3	-	-	0110	0110	
			1	0	1	0	x	x	0, 2			1010	1010	
			1	0	1	1	x	x	0	-	-	1110	1110	
			1	1	0	0	x	x	2, 3	-	-	0011	0011	
			1	1	0	1	x	x	3	-	-	0111	0111	
			1	1	1	0	x	x	2	-	-	1011	1011	
			1	1	1	1	x	x	x	-	-	1111	1111	
			0	0	x	x	x	x	RCW	-	-	1111	1111	RCW
0001	2 Way Rank Multi-plication using A[14]	2	1	0	x	x	x	0	0	-	-	1110	1110	1 Gbit DDR3 SDRAM
			1	0	x	x	x	1	2	-	-	1011	1011	
			0	1	x	x	x	0	1	-	-	1101	1101	
			0	1	x	x	x	1	3	-	-	0111	0111	
		4	1	0	1	1	x	0	0	1111	1110	-	-	
			1	0	1	1	x	1	4	1110	1111	-	-	
			0	1	1	1	x	0	1	1101	1111	-	-	
			0	1	1	1	x	1	5	1111	1101	-	-	
			1	1	1	0	x	0	2	1111	1011	-	-	
			1	1	1	0	x	1	6	1011	1111	-	-	
			1	1	0	1	x	0	3	1111	0111	-	-	
			1	1	0	1	x	1	7	0111	1111	-	-	
		2 or 4	1	1	1	1	x	x	x	1111	1111	1111	1111	
			0	0	x	x	x	x	RCW	1111	1111	1111	1111	RCW
0010	2 Way Rank Multi-plication using A[15]	2	1	0	x	x	0	x	0	-	-	1110	1110	2 Gbit DDR3 SDRAM
			1	0	x	x	1	x	2	-	-	1011	1011	
			0	1	x	x	0	x	1	-	-	1101	1101	
			0	1	x	x	1	x	3	-	-	0111	0111	
		4	1	0	1	1	0	x	0	1111	1110	-	-	
			1	0	1	1	1	x	4	1110	1111	-	-	
			0	1	1	1	0	x	1	1101	1111	-	-	
			0	1	1	1	1	x	5	1111	1101	-	-	
			1	1	1	0	0	x	2	1111	1011	-	-	
			1	1	1	0	1	x	6	1011	1111	-	-	
			1	1	0	1	0	x	3	1111	0111	-	-	
			1	1	0	1	1	x	7	0111	1111	-	-	
		2 or 4	1	1	1	1	x	x	x	1111	1111	1111	1111	
			0	0	x	x	x	x	RCW	1111	1111	1111	1111	RCW

Table 14 — Normal (1:1), 2 Way (1:2) and 4 Way (1:4) Rank Multiplication Control Signal Decoding with Rank 1 and Rank 5 Swap (F[0]RC2 DA4 = 0b)

F0RC15	Description	# DCS	CS [1]_n	CS [0]_n	A[17]/ CS [3]_n	A[16]/ CS [2]_n	A [15]	A [14]	Rank #	8 Rank QBCS [3:0]_n	8 Rank QACS[3: 0]_n	1,2,4 Rank QBCS[3: 0]_n	1,2,4 Rank QACS[3:0] _n	Comment
0011	2 Way Rank Multi-plication using A[16]	2	1	0	x	0	x	x	0	-	-	1110	1110	4 Gbit DDR3 SDRAM
			1	0	x	1	x	x	2	-	-	1011	1011	
			0	1	x	0	x	x	1	-	-	1101	1101	
			0	1	x	1	x	x	3	-	-	0111	0111	
		4	Not Supported							N/A	N/A	N/A	N/A	
		2 or 4	1	1	1	x	x	x	x	-	-	1111	1111	
			0	0	x	x	x	x	RCW	1111	1111	1111	1111	RCW
0101	4 Way Rank Multi-plication using A[15:14]	2	1	0	x	x	0	0	0	1111	1110	-	-	1 Gbit DDR3 SDRAM
			1	0	x	x	0	1	2	1111	1011	-	-	
			1	0	x	x	1	0	4	1110	1111	-	-	
			1	0	x	x	1	1	6	1011	1111	-	-	
			0	1	x	x	0	0	1	1101	1111	-	-	
			0	1	x	x	0	1	3	1111	0111	-	-	
			0	1	x	x	1	0	5	1111	1101	-	-	
			0	1	x	x	1	1	7	0111	1111	-	-	
			1	1	x	x	x	x	x	1111	1111	-	-	
			0	0	x	x	x	x	RCW	1111	1111	-	-	RCW
0110	4 Way Rank Multi-plication using A[16:15]	2	1	0	x	0	0	x	0	1111	1110	-	-	2 Gbit DDR3 SDRAM Host drives CS#[2] as A[16]
			1	0	x	0	1	x	2	1111	1011	-	-	
			1	0	x	1	0	x	4	1110	1111	-	-	
			1	0	x	1	1	x	6	1011	1111	-	-	
			0	1	x	0	0	x	1	1101	1111	-	-	
			0	1	x	0	1	x	3	1111	0111	-	-	
			0	1	x	1	0	x	5	1111	1101	-	-	
			0	1	x	1	1	x	7	0111	1111	-	-	
			1	1	x	x	x	x	x	1111	1111	-	-	
			0	0	x	x	x	x	RCW	1111	1111	-	-	RCW
0111	4 Way Rank Multi-plication using A[17:16]	2	1	0	0	0	x	x	0	1111	1110	-	-	4 Gbit DDR3 SDRAM Host drives CS#[3:2] as A[17:16]
			1	0	0	1	x	x	2	1111	1011	-	-	
			1	0	1	0	x	x	4	1110	1111	-	-	
			1	0	1	1	x	x	6	1011	1111	-	-	
			0	1	0	0	x	x	1	1101	1111	-	-	

4.1.2.3 Rank Multiplication Command Details

This section provides the operational details for each command which the host can send to the DIMM when in Rank Multiplication mode.

“RM bits” refer to the one (RM=2) or two (RM=4) address bits that are used for rank multiplication. These can be address bits A17 through A14, based the physical rank density. See the RM bit table above.

4.1.2.3.1 Activate Command

The activate command is sent a single sub-rank (physical rank), as determined by the RM bit(s). Decoding is done based on the Rank Decoding section above. It is the host’s responsibility to assure that no other pages are open in this logical rank / bank combination before issuing the Activate command. The RM bit(s) are stored by the MB for this logical rank / bank combination for later use by read and write commands.

4.1.2.3.2 Read or Write commands

Read and write commands are handled in the same manner. This also includes the Autoprecharge options (as determined by A10) and the burst length options (as determined by A12 and an MR bit).

The read and write commands are sent to a single sub-rank, as determined by the stored RM bits from the most recent Activate command to this logical rank / bank combination. For instance, if the most recent Activate command to logical rank 0, bank 2 targeted physical rank 4, then the read and write commands to logical rank 0 bank 2 will also target physical rank 4.

Unlike DRAMs, where the read data is always aligned to the edges of the incoming clock, the read data from the MB on the Host Bus is aligned to an internal clock phase based on the Receiver Enable training results of the MB to the DRAMs.

In Minimum latency mode (F3RC6 DA3,DA4=’00’) for speeds up to and including 1600 MT/s, each byte / nibble lane independently determines the internal Host side read data clock phase based on the longest read round trip latency from all the DRAMs attached to that particular byte / nibble lane. The result of this is that each byte/nibble lane will have different read timing as seen by the Host controller, but no matter which physical rank is read, the MB will have constant timing for that particular byte/nibble lane.

In Minimum latency mode (F3RC6 DA3,DA4=’00’) for speeds greater than 1600 MT/s (i.e., 1866 MT/s and 2133 MT/s), each byte lane independently determines the internal Host side read data clock phase based on the longest read round trip latency from all the DRAMs attached to that particular byte lane. The result of this is that each byte lane will have different read timing as seen by the Host controller, but no matter which physical rank is read, the MB will have constant timing for that particular byte lane.

In Minimum skew mode (F3RC6 DA3,DA4=’10’), the MB uses the longest read round trip latency from all of the byte/nibble lanes to derive the common internal read clock phase for all of the byte/nibble lanes. This result of this is that all 72 bits of the MB are driven in unison based on this common internal read clock no matter which physical rank is read.

4.1.2.3.3 Precharge Single and Precharge All Commands

The Precharge Single command operation is based on the Precharge Control configuration bit (F0RC14 bit DA4).

A configuration bit and address bit determine the operation of the Precharge Single and Precharge All commands.

Table 15 — Precharge Single and Precharge All Command Control

Refresh/ Precharge Control bit (F0RC14 DA4)	A0 of the command	Command action
0	X	Broadcast to all sub-ranks
1	0	Send to sub-rank specified by RM bits
1	1	Broadcast to all sub-ranks

When Broadcast to All Sub-ranks is specified, the Precharge command will be sent to all sub-ranks of the logical rank. A Precharge Single command targets only one bank, as specified by BA[2:0]. There can only be a page open in one sub-rank of a given bank. The other sub-ranks will not perform any operation. A Precharge All command affects all 8 banks of the logical rank. Different banks may have a page open in different sub-ranks. The Precharge All will close all banks in all sub-ranks associated with the logical rank.

When the Precharge command targets a single sub-rank, the RM bits from the host are used to specify the sub-rank. Note that it does NOT use the stored RM bits like the read and write commands, but uses the RM bit(s) sent by the host along with the Precharge Single Command. The RM bits are in the same location as they are for the Activate command, which is based on the physical DRAM density. The primary purpose of this mode is to allow the pages to be closed in an individual rank in preparation for a targeted refresh without closing pages in physical ranks that will not be targeted by the refresh. It also allows activity to some physical ranks while others are being refreshed. A rank being refreshed cannot accept a Precharge command.

4.1.2.3.4 Refresh Command

The Refresh Command has three modes of operation based on the Refresh Control bit and the Refresh_Stagger register.

4.1.2.3.4.1 Refresh Broadcast without Stagger

Refresh Broadcast without stagger is the default mode. In this mode the refresh command is sent to all sub-ranks associated with the logical rank. The refresh is sent at the same time to all of these ranks. This mode is selected when the Refresh control bit is set to a 0 and the Refresh_Stagger register is set to all 0s.

4.1.2.3.4.2 Refresh Broadcast with Stagger

Refresh Broadcast with Stagger is selected when the Refresh Control bit is set to a 0 and the Refresh_Stagger is non-zero. In this mode the refresh will be immediately sent to one of the sub-ranks, then sent to each successive sub-rank after a programmed amount of time. After the stagger time it is possible that the host controller is sending commands to other logical ranks on the DIMM, making the DRAM bus unavailable. The MB will wait for an available command slot by monitoring the command flow from the host. Following the 2nd sub-rank refresh the process is complete for RM=2. For RM=4 the stagger process repeats two more times.

The host controller must adjust its tRFC take into account the staggering of the refreshes, and the extra clocks that the controller may have to wait for an open command slot. In a very unusual case the number of extra clocks that the MB may have to wait for an empty slot could be very large. To avoid having to set a very large tRFC to accommodate this, a Refresh_Jitter_Limit is programmed. This limits the total number of extra clocks added due command slots being unavailable. If the limit is reached, the rest of the sub-rank refreshes are dropped. Dropping refreshes on very rare occasions is less hazardous than violating the tRFC of a DRAM.

4.1.2.3.4.2 Refresh Broadcast with Stagger (cont'd)

The following algorithm is used by the MB:

- 1) Host sends Refresh Command to MB
- 2) MB sends Refresh command to the physical rank pointed to by the Refresh_Subrank_Pointer for this logical rank. Refresh_Subrank_Pointer is incremented.
- 3) MB loads the Refresh_Jitter counter based on the Refresh_Jitter register setting.
- 4) MB loads the Refresh_Stagger counter based on the Refresh_Stagger register setting.
- 5) MB decrements the Refresh_Stagger counter on each DRAM clock. Refresh_Jitter_counter does NOT decrement.
- 6) When Refresh_Stagger counter reaches 0 the next Refresh is queued up and sent as soon as the DRAM command bus becomes available.
- 7) The Refresh_Jitter counter is decremented on each clock that the MB must wait on an unavailable DRAM command bus. If the Refresh_Jitter counter reaches 0, the refreshes for the rest of the sub-ranks, including the one queued up are cancelled. Go to step 10 in this case.
- 8) As soon as the DRAM bus becomes available the Refresh Command is sent to the sub-rank pointed to by the Refresh_Subrank_Pointer and the pointer is incremented.
- 9) If there are still subranks to refresh, return to step 4 (Note that the Jitter_counter is NOT reset).
- 10) If the Refresh_Start_rank bit is set to 0, set the Refresh_Subrank_Pointer to 0, else leave it where it was.

The host's tRFC is set to the

DRAM tRFC + (RM-1) * Refresh_Stagger + Refresh_Jitter_Limit

Where RM = the Rank Multiplication factor (2 or 4). It is the host's responsibility to set the Refresh_Jitter_Limit based on the controller design, and the frequency of dropped refreshes that is acceptable.

4.1.2.3.4.3 Targeted Refresh

The Targeted Refresh mode is used if the Refresh Control bit is set to a 1. In this case the refresh command is sent to the sub-rank determined by the RM bits sent by the host. It is the host's responsibility to manage refresh to each subrank.

4.1.2.3.5 ZQ Cal Command

ZQ Cal commands are to all sub-ranks associated with a logical rank. Note that this requires that each physical rank have separate ZQ resistors.

4.1.2.3.6 Enter Self Refresh

Self Refresh is entered by sending a Refresh on the command signals at the same time as CKE is sampled low, with CKE having been high on the previous clock. All sub-ranks of a logical rank will be put in self refresh together. The command will be broadcast to all sub-ranks even if the Refresh Control bit is set to the target refresh mode.

When the number of DCKE inputs being used matches the number of logical ranks (DCS_n inputs being used) the host has individual control of which ranks are put into self refresh.

There are several special cases when the number of DCKEs and DQCS_ns do not match.

4.1.2.3.6.1 2 DCKE mode with 4 or 8 logical ranks

In this case all of the even numbered logical ranks must be put into self refresh together, asserting all of the even numbered DCS_n signals. Likewise all odd numbered logical ranks must be put into self refresh together, asserting all of the odd numbered DCS_n signals. This is required due to the sharing of the DCKE input. Putting one logical rank into self refresh by asserting only one DCS_n signal would put the other ranks associated with that DCKE input into one of the power down states (Precharge powerdown if all paged closed). Raising CKE again to attempt to put another rank into self refresh would cause the first rank to exit self refresh.

4.1.2.3.6.2 4 DCKE mode with 8 logical ranks

In this case ranks 0 & 4 must be put into self refresh together. Likewise with ranks 1 & 5, 2 & 6, and 3 & 7 as each of these rank pairs share a DCKE. Note that 8 logical rank mode may not be supported on the DIMM.

4.1.2.3.6.3 4 DCKE mode with 2 logical ranks

This mode is possible to allow sub-rank granularity for CKE control. DCKE0 and DCKE2 will both be associated with the DCS0_n logical ranks, but control the QCKE to different subranks. The entire logical rank must be put into self refresh at the same time, which means that DCKE0 and DCKE2 must both transition during the self refresh entry command. Likewise for DCKE1 and DCKE3. Taking just one DCKE from high to low at the self refresh entry is not defined, and MB operation is indeterminate.

4.1.2.3.6.4 Soft CKE

With soft CKE the QCKE outputs are controlled by host commands, not directly by the DCKE inputs. Since a soft CKE command cannot be sent at the same time as a refresh command, enter self refresh and exit self refresh are special cases where the DCKE inputs DO affect the QCKE outputs. Soft CKE will always use 2 DCKE inputs. Normally transitions on the DCKE inputs are not transferred to the QCKE outputs, but are used to control the MB power state. When the MB detects an Enter Self Refresh command by means of a DCKE0 being sampled high followed by sampled low with a refresh command on the even numbered DCS_n inputs, the associated QCKE0 and QCKE2 will be taken low with refresh command sent to the DRAMs in order to put all of those physical ranks into self refresh. Likewise with DCKE1 and the odd DCS_n inputs.

It is the host's responsibility to have all QCKE outputs high (via a soft refresh command) before the Self Refresh Entry command. If the host has one or more of the QCKE outputs low, the self refresh command will be ignored by the physical ranks associated with that QCKE output and the DRAMs will not enter self refresh.

Exiting self refresh is also a special case where the DCKE low to high transition is passed through to the appropriate QCKE outputs. An Exit Self Refresh command looks the same to the MB as an Exit Powerdown command (MB powerdown in this case), but the MB must be able to take different actions based on which command it is. The MB accomplishes this by storing whether the most recent high to low transition on each DCKE input was an Enter Self Refresh or not. If it was a self refresh entry, the subsequent low to high transition on that DCKE is considered an Exit Self Refresh, and passed onto the QCKE output. Otherwise the DCKE transition is not passed onto the QCKE outputs and only used for power control of the MB itself.

A common restriction for all cases is that logical ranks 0 and 1 cannot be put into self refresh on the same clock as this would activate CS0_n and CS1_n simultaneously. The MB would interpret this as a Control Word write and the command would not be sent to the DRAMs.

4.1.2.3.7 Exit Self Refresh

Taking a DCKE high will cause the associated QCKE(s) to go high taking the DRAMs out of self refresh mode. Any number of DCKE signals may go high at once. See the Enter Self Refresh section above for special handling of the Exit Self Refresh command.

Taking a QCKE output from low to high will take the associated ranks out of whatever power down mode (self refresh, precharge powerdown slow, precharge powerdown fast, or active powerdown) that they were in.

4.1.2.3.8 Mode Register Set

The operation of the Mode Register Set command is controlled by the MRS control bit. When a 0, MRS commands are sent to all sub-ranks. When a 1 it targets only the sub-rank selected by the RM bits. The targeted commands will be necessary to set different sub-ranks Rtt_nom values and Precharge Powerdown modes.

A configuration bit and address bit determine the operation of the MRS command.

Table 16 — MRS Control

MRS Control bit (F0RC14 DBA0)	A13 of the command	Command action
0	X	Broadcast to all sub-ranks
1	0	Send to sub-rank specified by RM bits
1	1	Broadcast to all sub-ranks

When Broadcast to All Sub-ranks is specified, the MRS command will be sent to all sub-ranks of the logical rank

When the MRS command targets a single sub-rank, the RM bits from the host are used to specify the sub-rank. Note that it does NOT use the stored RM bits like the read and write commands, but uses the RM bit(s) sent by the host along with the Mode Register Set Command. The RM bits are in the same location as they are for the Activate command, which is based on the physical DRAM density.

4.1.2.3.9 NOP

A NOP is when DRAS_n, DCAS_n, and DWE_n are all high, and one of the DCS_n inputs is low. The MB will pass a NOP onto the DRAM bus, broadcasting to all sub-ranks.

4.1.2.3.10 Control Word Write

The control word is written into the MB when DCS0_n and DCS1_n are both asserted. This case is treated as a Deselect as far as the DRAM interface is concerned. The command and address are not sent on to the DRAM bus and no QCS is asserted. The control register in the MB is written according to the address bits.

4.1.2.3.11 Deselect

Deselect is when all DCS_n inputs remain high. The command and address signals are not passed onto the Q outputs on a deselect.

4.2 Command, Address, and Control Signal usage

The MB handles the Command, Address and Control signals somewhat differently than a standard RDIMM.

4.2.1 Command Signals

The Command signals are RAS_n, CAS_n, and WE_n. They are used for the DRAM command encoding, although the state or actions on both address and control signals sometimes are used in the encoding of the command.

In most cases the command signals are passed directly through the MB to the DRAM busses. The table below lists each command and the actions of the MB.

Table 17 — Command and MB Action

Command	RAS_n	CAS_n	WE_n	Oth Conditions	MB Action.
Activate	L	H	H		Pass through to DRAM bus. Single sub-rank receives Chip Select.
Read or Read with Auto Precharge	H	L	H		Pass through to DRAM bus. Single sub-rank receives Chip Select.
Write or Write with Auto Precharge	H	L	L		Pass through to DRAM bus. Single sub-rank receives Chip Select.
Precharge Single	L	H	L	A10=L	Pass through to DRAM bus. With Rank Multiplication, a configuration bit determines whether all sub-ranks receive a Chip Select or just one.
Precharge All	L	H	L	A10=H	Pass through to DRAM bus. With Rank Multiplication, a configuration bit determines whether all sub-ranks receive a Chip Select or just one.
Refresh	L	L	H	CKE=H	Pass through to DRAM bus. With Rank Multiplication, configuration bits determine whether it is broadcast, sent to sub-ranks with a stagger, or sent to a single sub-rank.
ZQ Calibration	H	H	L	A15:13=000 or Soft CKE disabled	Pass through to DRAM bus. Broadcast to all subranks.
Soft CKE	H	H	L	A15:13=001 and Soft CKE enabled	Command is not sent to DRAM bus. MB changes the QCKE outputs based on A3:0.
Reserved	H	H	L	A15:13 not 000 or 001 with soft CKE enabled	Command is not sent to the DRAM bus. Treated as NOP.
Enter Self Refresh	L	L	H	CKE transitions H to L	Pass through to DRAM bus. With Rank Multiplication, it is broadcast to all sub-ranks. See in previous section.
Exit Self Refresh				CMD is NOP or deselect, CKE transitions L to H.	See the CKE control section.
Mode Register Set	L	L	L		Pass through to DRAM bus. With Rank Multiplication, a configuration bit determines whether all sub-ranks receive a Chip Select or just one. The MB will snoop the Mode Register Set commands, storing the MRS bits for its own usage.
NOP	H	H	H		Command is not passed to the DRAM bus. It is treated the same as a Deselect.
Deselect	X	X	X	All CS_n inputs = H	Command is not passed to the DRAM bus.

Table 17 does not differentiate all permutations of commands, such as ZQ Calibration Long or Short. The address bits which select these permutations are passed to the DRAMs.

Individual Command actions are discussed in a previous section.

4.2.2 Address Signals

The address signals consist of A15:0 and BA2:0. In the Rank Multiplication mode one or two address bits are used as sub-rank select bits which are decoded by the MB.

All address bits are passed through to the DRAM busses whenever any of the Chip Selects are active with the following exceptions:

- A Register Control Word is being written (chip selects 0 & 1 are active at the same time).
- All DCKE inputs to the MB are low and the CKE Power Down Mode Enable bit is set. The MB ignores the DCS inputs in this case.
- Soft CKE commands.

4.2.3 Control Signals

Control Signals include the CS_n signals (anywhere from 2 to 8 inputs), CKE (2 or 4) and ODT (1 or 2).

4.2.3.1 Chip Select signals

The Chip Select signals are handled differently depending on whether Rank Multiplication or direct addressing is being used.

4.2.3.1.1 Chip Selects with Direct Addressing

The Chip Select inputs operate the same way in the MB as with LRDIMMs. Each DCS_n input is associated with one physical rank on the DIMM and is passed through the MB to the DRAM side QCS output(s) associated with that rank. The DCS_n is not passed through under the following conditions:

- A Register Control Word is being written (chip selects 0 & 1are active at the same time).
- All DCKE inputs to the MB are low and the CKE Power Down Mode Enable bit is set. The MB ignores the DCS inputs in this case.
- Soft CKE commands.

Direct addressing may be done with:

- Two physical ranks and two chip selects (DCS0_n and DCS1_n) with operation much like a dual rank RDIMM
- Four physical ranks and four chip selects (DCS[3:0]) with operation much like a quad rank RDIMM
- Eight physical ranks and eight chip selects (DCS[7:0]). A special non-JEDEC DIMM is required for eight chip select support.

4.2.3.1.2 Chip Selects with Rank Multiplication

In the Rank Multiplication mode, the MB will use one or two address bits to determine which sub-rank is targeted. The particular command, and configuration settings will determine how the CS is passed through.

See the Rank Multiplication section for more details.

4.2.3.2 CKE Signals

LRDIMMs have three modes of operation for CKE. These are summarized in Table 18.

Table 18 — CKE Modes

Mode	DCKE Inputs	Separately controlled QCKE outputs	Mapping	Description
2 DCKE mode	2	2	DCKE0 --> QCKE0 & QCKE2 DCKE1 --> QCKE1 & QCKE3	Same as RDIMM mapping. CKE inputs are passed onto outputs
4 DCKE mode	4	4	DCKE0 --> QCKE0 DCKE1 --> QCKE1 DCKE2 --> QCKE2 DCKE3 --> QCKE3	Extended to four CKE inputs, providing finer granularity CKE control.
Soft CKE mode	2	4	QCKE outputs individually controlled via a command.	QCKE outputs are controlled by commands. QCKE outputs do not follow the DCKE inputs EXCEPT for the Enter Self Refresh Entry command. DCKE inputs still control the power state of the buffer itself.

4.2.3.2.1 2 DCKE mode (RDIMM Compatible Mode)

Normal RDIMMs have two CKE inputs. CKE0 goes to Rank 0 and Rank 2 (quad rank DIMMs). CKE1 goes to Rank 1 (dual or quad rank DIMMs) and Rank 3 (quad rank DIMMs).

LRDIMMs use this same configuration by default, extending it to 8 rank DIMMs by having DCKE0 go to all even numbered ranks (both physical and logical), and DCKE1 go to all odd numbered ranks. The DCKE input is always sent on to the appropriate QCKE outputs in this mode.

This is the default mode of the DIMM following RESET.

4.2.3.2.2 4 DCKE mode

The buffer may be configured to have 4 DCKE inputs for finer granularity rank control of power management. The additional DCKE inputs are achieved by using a formerly NC pin for DCKE2 and the ODT1 pin for DCKE3. ODT1 is not required for LRDIMMs since there is a single load presented to the DIMM connector.

4.2.3.2.3 Soft CKE mode

In Soft CKE mode the QCKE outputs are controlled by commands sent by the host. The DCKE inputs do not affect the QCKE outputs except for the Self Refresh Entry and the Self Refresh Exit commands. The DCKE inputs do affect the power state of the MB, however. The MB will not accept commands when both DCKE inputs are low and the CKE Power Down Mode Enable bit is set.

The Soft CKE command uses a further decode of the ZQ cal command encoding, using address bits A15:13. The Soft CKE command controls all 4 QCKE outputs at once. It can be issued with any DCS_n input active and will perform the same function regardless of which DCS_n input is activated.

Table 19 — Soft CKE command

Command	RAS_n	CAS_n	WE_n	A15	A14	A13	A12:11	A10	A9:8	A7:4	A3	A2	A1	A0
ZQ Cal short	H	H	L	0	0	0	x	0	x	x	x	x	x	x
ZQ Cal long	H	H	L	0	0	0	x	1	x	x	x	x	x	x
Soft CKE	H	H	L	0	0	1	x	x	x	TBD	QCKE 3	QCKE 2	QCKE 1	QCKE 0
Reserved	H	H	L	x	1	x	x	x	x	x	x	x	x	x
Reserved	H	H	L	1	x	x	x	x	x	x	x	x	x	x

When Soft CKE is disabled, A15:13 are ignored and all combinations are considered ZQ cal commands. The MB will accept a Soft CKE command when any of the configured DCS_n inputs are active. All four QCKE outputs will be affected by the Soft CKE command regardless of which DCS_n input was active for the command. As usual, the soft CKE command is not accepted by the MB unless a DCS_n input is low and at least one of the DCKE inputs is high.

On a soft CKE command the QCKE outputs will be affected with the same timing as the address/command signals as if it were a DRAM command. The soft CKE command only affects the QCKE outputs. The address/command signals do not change and the QCS_n outputs are not asserted.

See the Rank Multiplication Enter Self Refresh command section for details on how self refresh is entered when in the Soft CKE mode.

4.2.3.3 ODT signals

ODT is handled separately for the host and DRAM sides of the MB. The DODT signals affect the termination applied by the MB onto the host side data bus. The QODT signals affect the termination applied by the DRAMs onto the DRAM side data bus. DDR3 MB will not be required to provide asynchronous DODT functionality as described for the SDRAM in JESD79-3

4.2.3.3.1 Host side ODT (DODT signals)

On the host bus the MB acts as a DRAM device as far as applying ODT to the data bus, i.e. the MB has the same ODT latencies and timing parameters as a DRAM in relationship to the clock edges. Since the MB appears as only one load to the host, it effectively appears as a single rank DIMM ODT wise. Only DODT0 is required for proper operation, but DODT1 may also be used, based on F0RC6 DBA0. When F0RC6 DBA0=0, only DODT0 is used. When F0RC6 DBA0=1 DODT0 and DODT1 are ORed together in the buffer, with either high enabling the termination.

When 4 DCKE mode is used, DCKE3 uses the DODT1 signal. In this case only DODT0 is used for ODT control by the buffer and F0RC6 DBA0 needs to be set to '0'.

The MB monitors the host commands, and applies Rtt_NOM and Rtt_WR in the same manner as a DRAM except that it looks at all configured DCS_n inputs, and both ODT inputs (unless 4 DCKE mode is used).

RTT_Nom and RTT_WR can be individually set to: Disabled, or 30, 40, 60, 80, 120 or 240 ohms. The 240 ohm selection is optional for the buffer for RTT_Nom. These are set through F[3]RC0 for RTT_Nom and F[3]RC1 for RTT_WR. See the Control Word chapter for the encodings.

The DODT input signals do not directly affect the QODT outputs.

4.2.3.3.2 DRAM side ODT (QODT signals)

On the DRAM side the MB acts like a host controller by enabling its internal termination on reads, and controlling the QODT output signals to the DRAMs. The control and timing of the QODT signals is controlled by the MB logic, as configured by the host.

There are two sets of ODT outputs with two copies each. They are named Q[A/B]ODT0 and Q[A/B]ODT1, with the A and B sets on opposite sides of the MB package. The two QODT output sets are controlled individually by the MB. QAODT0 and QBODT0 generally go to physical rank 0 while QAODT1 and QBODT1 generally go to physical rank 1. The remaining physical ranks have their ODT inputs tied to VDD. This allows physical ranks 0 and 1 to assert Rtt_NOM, while any physical rank can assert Rtt_WR when it is written to. All physical ranks with their ODT tied to VDD must have Rtt_NOM disabled. Refer to the raw card designs for exact connections.

The MB is has control word registers to determine when the QODT signals are asserted. For each rank there are separate bits for the two QODT output sets, and a separate set for reads and writes to the ranks. This is a total of 32 bits (8 ranks * 2 ODT signals * 2 for read & write).

4.3 Parity

The MB includes a parity checking function. The MB accepts a parity bit from the memory controller at its input pin PAR_IN one cycle after the corresponding data input, compares it with the data received on the D-inputs and indicates on its open-drain ERROUT_n pin (active low) whether a parity error has occurred. The computation only takes place for data which is qualified by at least one of the DCS[n:0]_n signals being LOW.

If an error occurs, ERROUT_n is driven low with the third input clock edge after the corresponding data on the D-inputs. It becomes high impedance with the 5th input clock cycle after the data corresponding with a parity error. In case of consecutive errors, ERROUT_n becomes high impedance with the 5th input clock cycle after the last data corresponding with a parity error. The DIMM-dependent signals (DCKEn, DCSn_n, and DODTn) are not included in the parity check computations.

The following signals are included in the parity calculation:

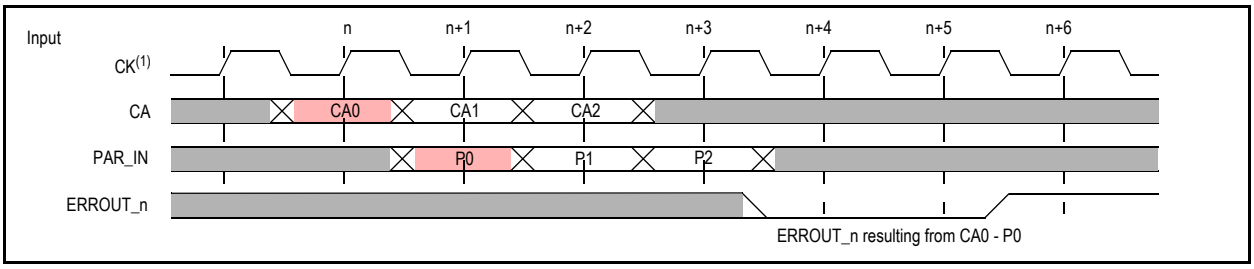
- PAR_IN
- RAS_n, CAS_n, WE_n
- BA2:0
- A15:0
- A17:16 are included only if the Parity Calculation field in F0RC11 = 01.

The F0RC11 control word contains a two bit Parity Calculation field allowing parity checking to be disabled (default), parity checking without A17 and A16, and parity checking with A17 and A16. Refer to the Control Word chapter for details.

4.3.1 Parity Timing Scheme Waveforms

The PAR_IN signal arrives one input clock cycle after the corresponding data input signals. ERROUT_n is generated three input clock cycles after the corresponding data is registered. If ERROUT_n goes low, it stays low for a minimum of two input clock cycles or until RESET_n is driven low. Figure 3 shows the parity diagram with single parity-error occurrence and assumes the occurrence of only one parity error when data is clocked in at the n input clock cycle (PAR_IN clocked in on the n+1 input clock cycle).

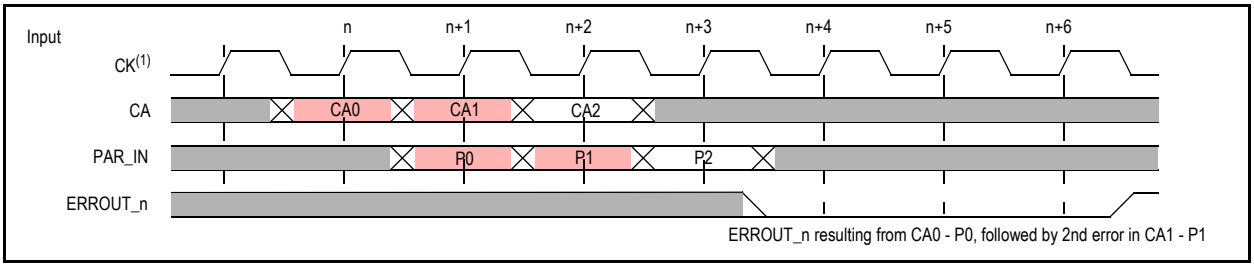
4.3.1 Parity Timing Scheme Waveforms (cont'd)



(1) CK_n left out for better visibility

Figure 3 — Timing of clock, data and parity signals

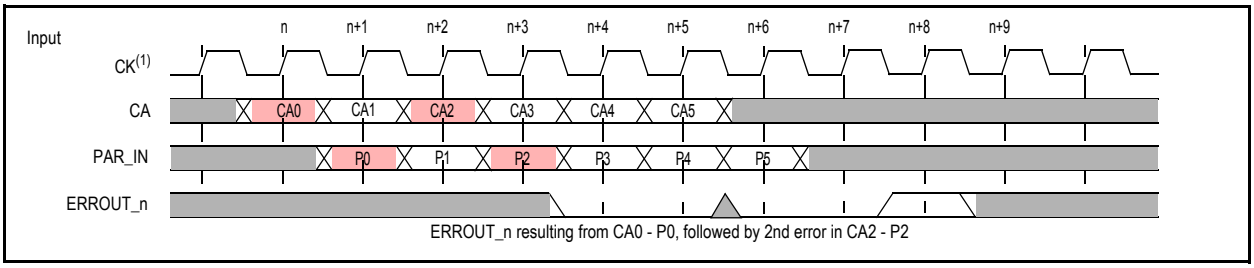
Figure 4 shows the parity diagram with two consecutive parity-error occurrences and assumes the occurrence of both parity errors when data is clocked in at the n and n+1 input clock cycles (PAR_IN clocked in on the n+1 and n+2 input clock cycles).



(1) CK_n left out for better visibility

Figure 4 — Two Consecutive Parity-Error Occurrences

Figure 5 shows the parity diagram with two parity-error occurrences separated by a clock cycle with no error occurrence. The diagram assumes the occurrence of two parity errors when data is clocked in at the n and n+2 input clock cycles (PAR_IN clocked in on the n+1 and n+3 input clock cycles).

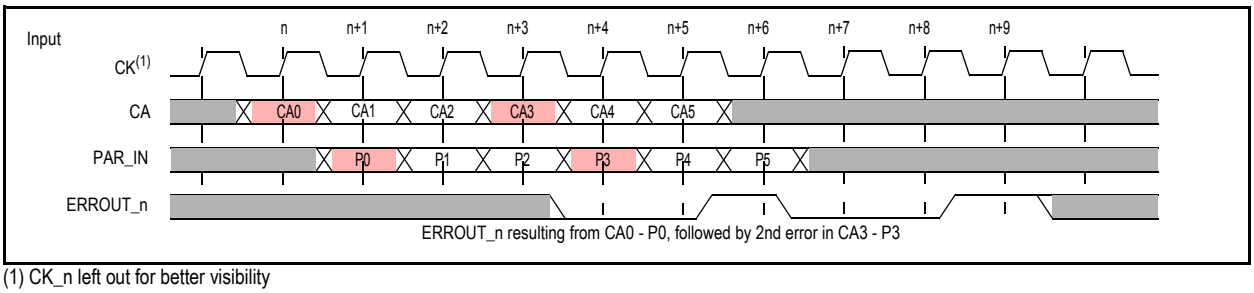


(1) CK_n left out for better visibility

Figure 5 — Two Parity-Error Occurrences Separated by a Clock Cycle of no Error Occurrence

4.3.1 Parity Timing Scheme Waveforms (cont'd)

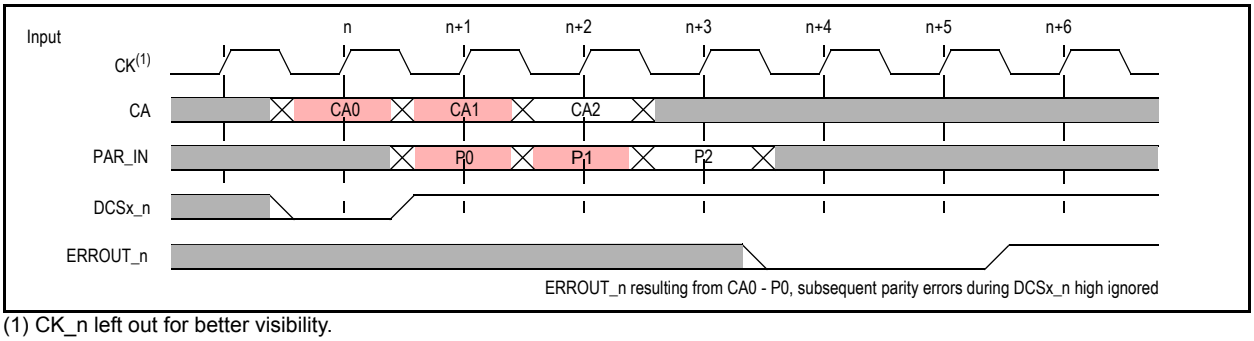
Figure 6 shows the parity diagram with two parity-error occurrences separated by two input clock cycles with no error occurrence. The diagram assumes the occurrence of two parity errors when data is clocked in at the n and n+3 input clock cycles (PAR_IN clocked in on the n+1 and n+4 input clock cycles).



(1) CK_n left out for better visibility

Figure 6 — Two Parity-Error Occurrences Separated by two Clock Cycle of no Error Occurrence

Figure 7 shows the parity diagram with two parity-error occurrences; during chip-select and chip-deselect modes. The diagram assumes the occurrence of both parity errors when data is clocked in at the n and n+4 input clock cycles (PAR_IN clocked in on the n+1 and n+5 input clock cycles). Parity error in the chip-select mode is detected, but parity error in the chip-deselect mode is ignored.

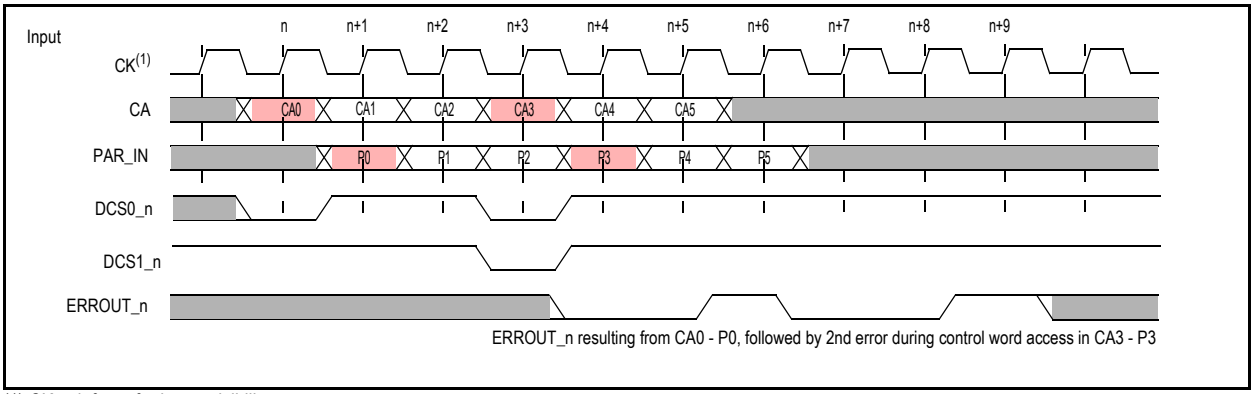


(1) CK_n left out for better visibility.

Figure 7 — Parity-Error Occurrence In Chip-Deselect Mode

4.3.1 Parity Timing Scheme Waveforms (cont'd)

Figure 8 shows the parity diagram with two parity-error occurrences; during normal operation and during control register programming. The diagram assumes the occurrence of both parity errors when data is clocked in at the n and n+4 input clock cycles (PAR_IN clocked in on the n+1 and n+5 input clock cycles). The data on the n+4 input clock pulse is intended for the control mode register. Parity error during control mode register programming is detected and the parity functionality is the same as during normal operation. If a parity error occurs, the command is ignored.



(1) CK_n left out for better visibility

Figure 8 — Parity-Error Occurrences During Control Word Programming

4.4 Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling

Output Inversion is always enabled by default, after RESET_n is de-asserted, to conserve power and reduce simultaneous output switching current. All A-outputs will follow the equivalent inputs, however the following B-outputs will be driven to the complement of the matching A-outputs: QBA3 - QBA9, QBA11, QBA13 - QBA15, QBBA0 - QBBA2.

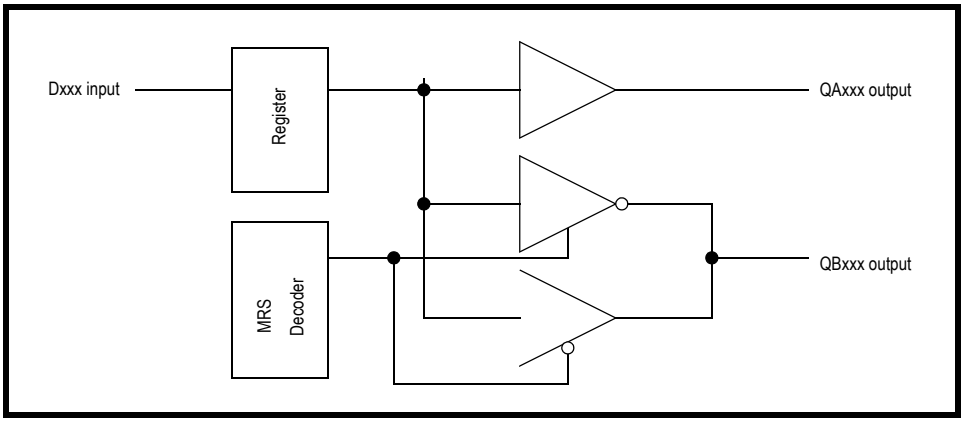


Figure 9 — Output Inversion Functional Diagram

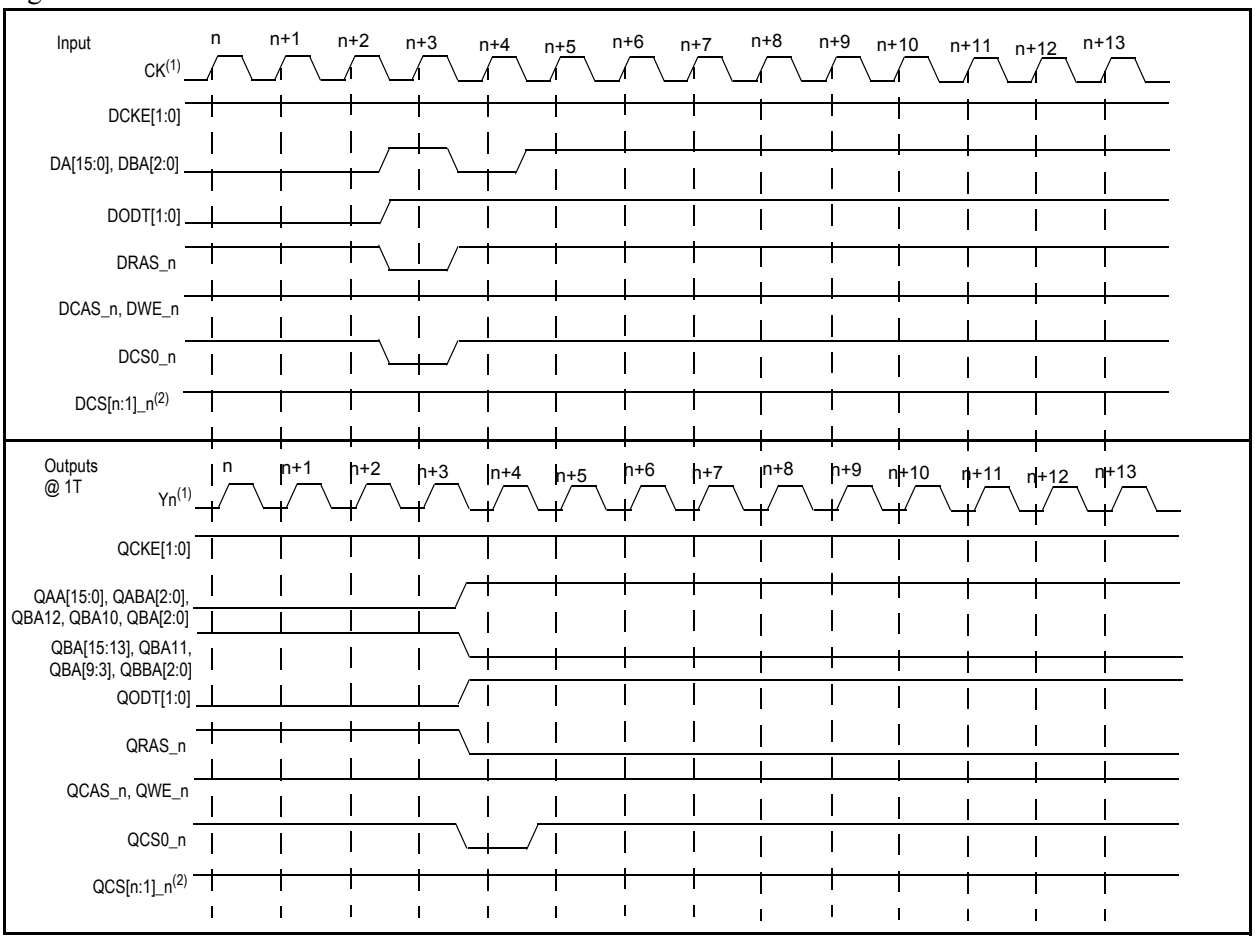
The Output Inversion feature is not used during DRAM MRS command access. When Output Inversion is disabled, all corresponding A and B output drivers of the MB are driven to the same logic levels. Output Inversion must be disabled when the MRS and EMRS commands must be issued to the DRAMs, for example, to assure that the same programming is issued to all DRAMs in a rank.

4.4 Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling (cont'd)

With Output Inversion disabled during MRS access, in order to allow correct DRAM accesses with the consequently increased simultaneous switching propagation delay the devices supports 3T timing. If this feature is invoked the device drives the received data on its outputs for thee cycles instead of one. The only exception are the QxCS[n:0]_n outputs.

When the device decodes the MRS command (DRAS_n=0, DCAS_n=0, DWE=0 and only one DCSn_n=0), it will disable the Output Inversion function and pass the DRAM MRS command with an additional (one) clock delay on the appropriate QnCSx_n signal to the DRAM. Back-to-back MRS command via the MB must have a minimum of tDRAM_MRS clock delays. The MB will automatically enable Output Inversion if there is no DRAM MRS command tDRAM_MRS clock after the previous MRS command. The MB will ignore commands on the (tDRAM_MRS - 1) clocks following an MRS command.

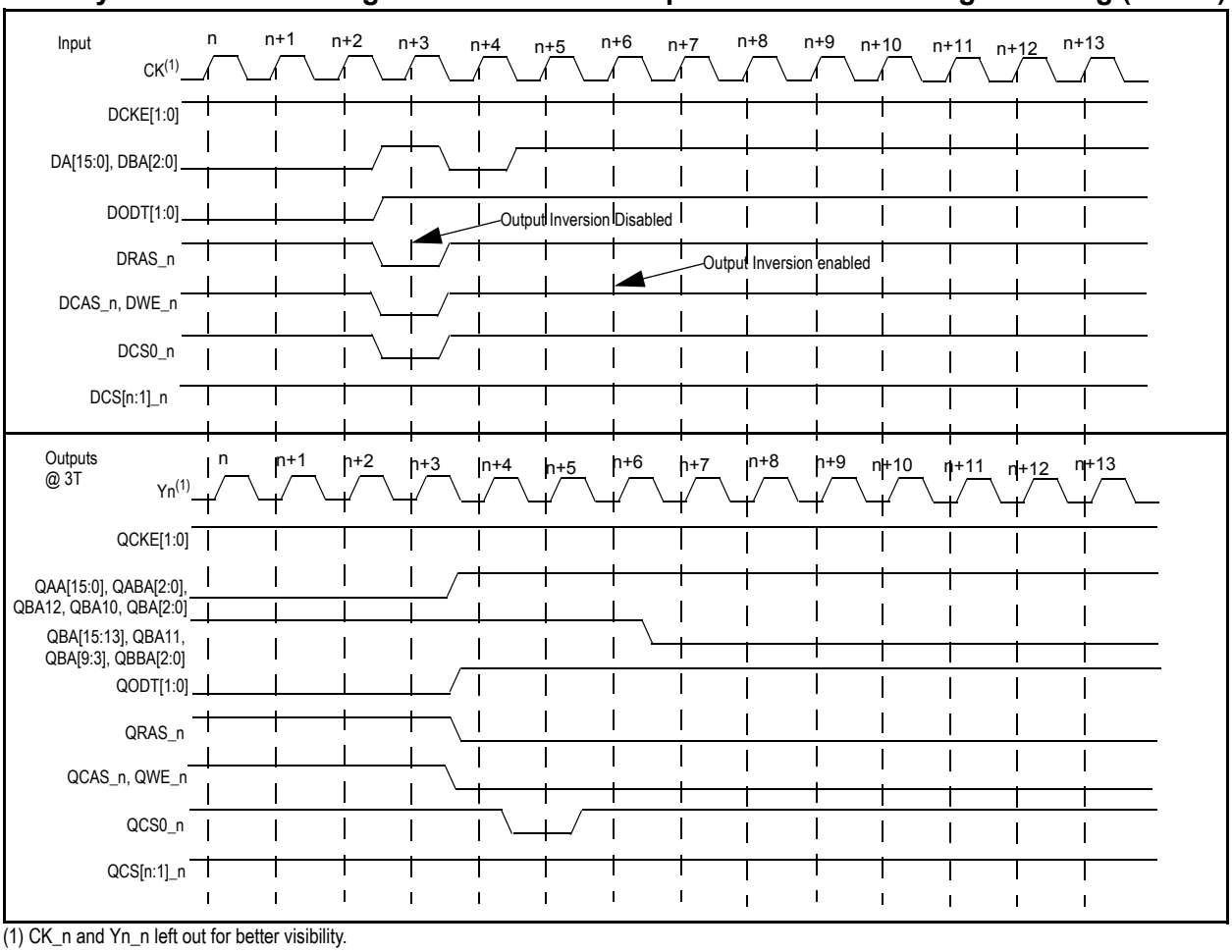
The inputs and outputs relationships for 1T timing and 3T timing are shown in Figure 10, Figure 11 and Figure 12.



(1) CK_n and Yn_n left out for better visibility

Figure 10 — 1T Timing During Normal Operation

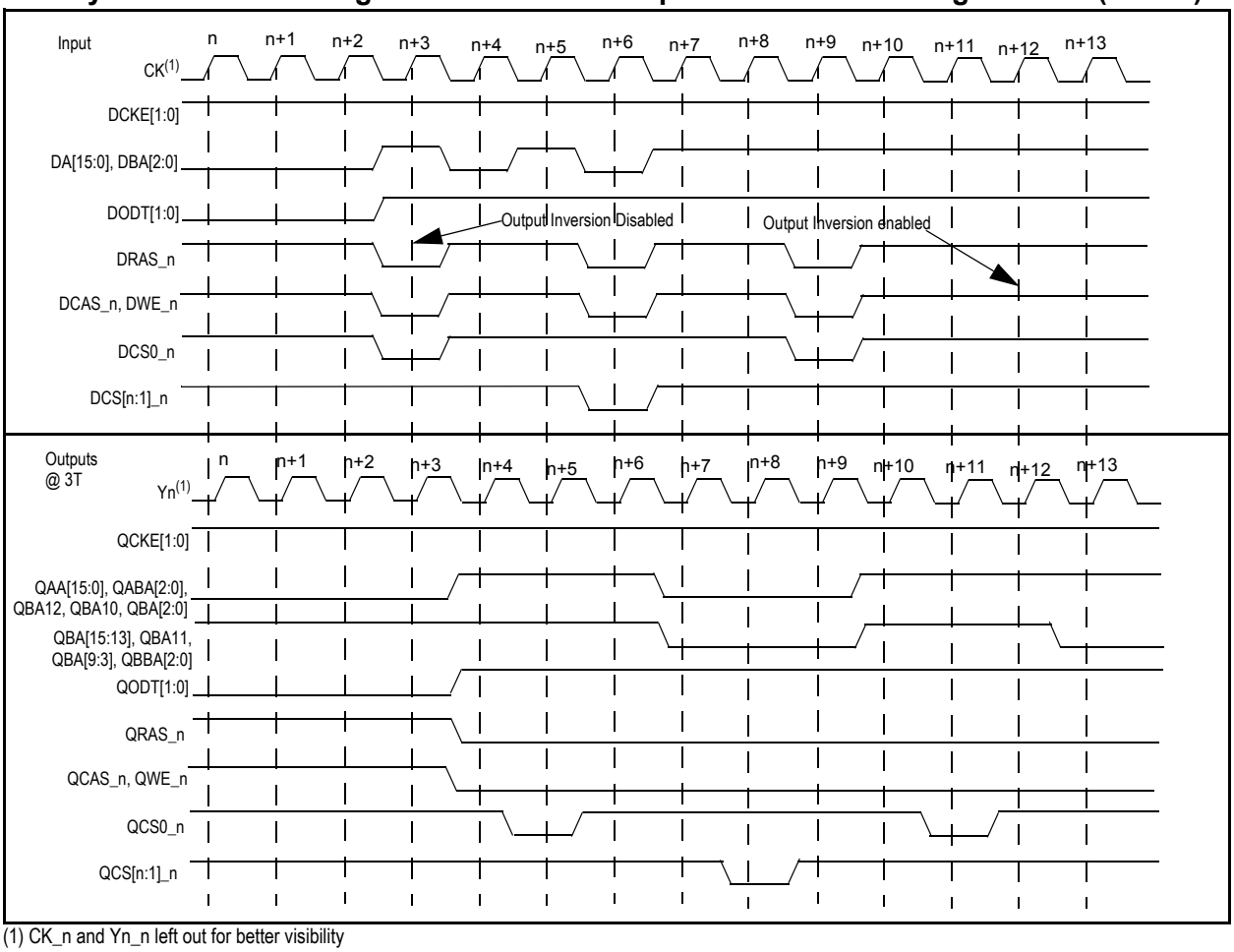
4.4 Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disabling (cont'd)



(1) CK_n and Yn_n left out for better visibility.

Figure 11 — 3T Timing During DRAM MRS Command

4.4 Dynamic 1T/3T Timing Transaction and Output Inversion Enabling/Disablin (cont'd)



(1) CK_n and Yn_n left out for better visibility

Figure 12 — 3T Timing During Multiple DRAM MRS Commands

4.5 Control Word Access Mechanism

The MB has internal control bits for adapting the configuration of certain device features. The control bits are accessed by the simultaneous assertion of both DCS0_n and DCS1_n. MB Qn outputs including QxCKE0, QxCKE1, QxODT0 and QxODT1 remain in their previous state. Select signals QxCS[n:0]_n are set to high during control word access. Control word accesses may only occur after all previous DRAM commands have completed, including the transfer of data.

RDIMM registers allocate 16 control words of 4 bits each. Due to the expanded configuration requirements of the LRDIMM, the MB allocates 16 separate functions of 16 control words each. Control word 7 of each function sets the function number, leaving 15 control words per function for the actual configuration bits. Function 0 is similar to the RDIMM register.

The functions are named F0 through F15 while the control words are named RC0 through RC15. A specific register is fully named by its function number and control word number as FxRCn. Selection of each word of control bits is presented on inputs DA0 through DA2 and DBA2. Data to be written into the configuration registers need to be presented on DA3, DA4, DBA0 and DBA1. Bits DA[15:5] must be low for a valid access. If Power-Down mode is enabled in RC9[DBA1] at least one DCKE must be high for valid Control word access. The inputs on DRAS_n, DCAS_n, DWE_n and DODT[1:0] can be either high or low and are ignored by the MB during control word access. In all cases Address and command parity is checked during control word write operations. ERROUT_n is asserted and the command is ignored if a parity error is detected. Using this mechanism, controllers may use the MB to validate the address and command bus signal integrity to the module as long as one or more of the parity checked input signals DA3..DA15, DBA0, DBA1, DRAS_n, DCAS_n, DWE_n are kept high.

4.6 Address Mirroring

Address mirroring allows for easier raw card routing by allowing specific pairs of address bits to be flipped on the back side of the board. The MB allows address mirroring to be enabled on odd numbered physical ranks. Since odd numbered physical ranks are always associated with odd numbered logical ranks (odd numbered DCSn_n inputs), it is also true that when address mirroring is enabled, it is enabled for odd numbered logical ranks.

It is the host controller's responsibility to switch the address bits in an MRS command to accommodate address mirroring. This functionality is identical as to what is required for UDIMMs utilizing address mirroring. The MB must be aware of mirroring, as it snoops MRS cycles, and is capable of generating its own MRS cycles during testing.

Table 20 is the address map for address mirroring.

Table 20 — Address Mirroring

Host bit (MB input)	MB output	Even rank DRAM connection	Odd rank DRAM connection, Mirroring off.	Odd Rank DRAM connection, Mirroring on	Note
DA0	QxA0	A0	A0	A0	A0 not flipped as it affects the burst start
DA1	QxA1	A1	A1	A1	A1 not flipped as it affects the burst start
DA2	QxA2	A2	A2	A2	A2 not flipped as it affects the burst start
DA3	QxA3	A3	A3	**A4**	A3 and A4 flipped
DA4	QxA4	A4	A4	**A3**	
DA5	QxA5	A5	A5	**A6**	A5 and A6 flipped
DA6	QxA6	A6	A6	**A5**	
DA7	QxA7	A7	A7	**A8**	A7 and A8 flipped
DA8	QxA8	A8	A8	**A7**	
DA9	QxA9	A9	A9	A9	
DA10	QxA10	A10	A10	A10	A10 cannot be flipped as it is Auto Precharge
DA11	QxA11	A11	A11	A11	
DA12	QxA12	A12	A12	A12	A12 cannot be flipped as it is Burst Length
DA13	QxA13	A13	A13	A13	A13 and above cannot be flipped because they are not present on all DRAM densities
DA14	QxA14	A14	A14	A14	
DA15	QxA15	A15	A15	A15	
DBA0	QxBA0	BA0	BA0	**BA1**	BA0 and BA1 flipped
DBA1	QxBA1	BA1	BA1	**BA0**	
DBA2	QxBA2	BA2	BA2	BA2	

Address signals can only be flipped if they perform no other special function. A0-2 set the burst start location for reads and writes, and cannot be flipped. A10 is the auto precharge bit for reads and writes. A12 is the burst length when burst on the fly is used for reads and writes. A13 and above are not present on all DRAM densities, so they cannot be flipped. Address signals can only be flipped in pairs as shown in the above table.

During MRS cycles, the address bits contain register information, so address all bits must be in their proper location. This is done by having the host controller flip the bits when sending an MRS command to the DRAMs. Since MRS cycles are not a critical path, it does not affect performance by requiring the controller (or the BIOS) to do this muxing.

The MB will always pass the address straight through during MRS commands. The MB must know when mirroring is being used, however, as it snoops the MRS commands in order to use this information as part of its configuration. When Mirroring is enabled (by F0RC14 DA3) the MB will flip the appropriate address bits during MRS accesses to odd ranks before storing the bits internally.

5 DRAM Interface Protocol and Requirement

5.1 Signals and Usage

5.1.1 Command / Address

There are two sets of Command / Address signals, for loading reasons. The two copies are identical except that the B copy of many of the address signals are normally inverted from the A copy to lower the worst case simultaneous switching conditions and to balance out the Vtt power supply loading.

Table 21 — Command / Address signals

Signal	Description
QAA[15:0]	A copy of the address bus.
QBA[15:13, 11, 9:3]	B copy of the address bus which is inverted from the A side when address inversion is enabled.
QBA[12,10,2:0]	B copy of the address bus which is never inverted. Inverting these signals would cause functional issues.
QABA[2:0]	A copy of the Bank Address bus.
QBBA[2:0]	B copy of the Bank Address bus. All bits are inverted when address inversion is enabled.
QARAS_n	A copy of RAS
QBRAS_n	B copy of RAS. Always the same state as QARAS_n
QACAS_n	A copy of CAS
QBCAS_n	B copy of CAS. Always the same state as QACAS_n
QAWE_n	A copy of WE
QBWE_n	B copy of WE. Always the same state as QAWE_n

5.1.1.1 Address Mirroring

Address mirroring allows the DRAMs on the back side of the DIMM to have some of the address bits flipped from what they are on the front side of the DIMM. Bits can only be flipped when they cause no functional issue, so only bits A[8:3] and BA[1:0] are mirrored. When mirroring is used, all odd numbered ranks are mirrored, and all even numbered ranks are not mirrored.

Mirroring must be accounted for during MRS cycles, as each address bit affects specific MR bits. It is the host controller's responsibility to switch the address bits in an MRS command to accommodate address mirroring. The functionality is identical as to what is required for UDIMMs utilizing address mirroring. The MB must be aware of mirroring, as it snoops MRS cycles to determine the DRAM settings, and it is capable of generating its own MRS cycles during training and testing.

An SPD bit determines whether the DIMM utilizes address mirroring. If mirroring is not used, all ranks are non-mirrored. If mirroring is used, all odd numbered ranks (both logical and physical) are mirrored. Even numbered ranks are never mirrored.

Table 22 indicates the address connections for both non-mirrored and mirrored ranks.

5.1.1.1 Address Mirroring (cont'd)

Table 22 — Address Mirroring

Buffer Output	DRAM pin, non mirrored ranks	DRAM pin, mirrored ranks
Q[B:A]A0	A0	A0
Q[B:A]A1	A1	A1
Q[B:A]A2	A2	A2
Q[B:A]A3	A3	**A4**
Q[B:A]A4	A4	**A3**
Q[B:A]A5	A5	**A6**
Q[B:A]A6	A6	**A5**
Q[B:A]A7	A7	**A8**
Q[B:A]A8	A8	**A7**
Q[B:A]A9	A9	A9
Q[B:A]A10	A10	A10
Q[B:A]A11	A11	A11
Q[B:A]A12	A12	A12
Q[B:A]A13	A13	A13
Q[B:A]A14	A14	A14
Q[B:A]A15	A15	A15
Q[B:A]BA0	BA0	**BA1**
Q[B:A]BA1	BA1	**BA0**
Q[B:A]BA2	BA2	BA2

5.1.2 Control Signals

Table 23 — Control Signals

Signal	Description.
QACS0_n / QCS0_n QACS1_n / QCS1_n QACS2_n / QCS2_n QACS3_n / QCS3_n	4 Chip select mode: The A copy of chip selects 3:0. 8 Chip select mode: Only copy of chip selects 3:0.
QBCS0_n / QCS4_n QBCS1_n / QCS5_n QBCS2_n / QCS6_n QBCS3_n / QCS7_n	4 Chip select mode: The B copy of chip selects 3:0. Identical function as QACS[3:0]_n copies. 8 Chip select mode: Only copy of chip selects 7:4.
QACKE[3:0]	Clock Enable outputs 3:0, A side CKE0 goes to ranks 0 and 4 CKE1 goes to ranks 1 and 5 CKE2 goes to ranks 2 and 6 CKE3 goes to ranks 3 and 7
QBCKE[3:0]	Clock Enable output 3:0, B side. Identical function as QACKE[3:0].
QAODT[1:0]	ODT output 1:0, A side.
QBODT[1:0]	ODT output 1:0, B side.

5.1.2.1 Chip Select outputs

The MB provides 8 chip select outputs which can be configured as either an A and B copy of four chip selects for 8 individual chip selects. For quad rank or smaller DIMMs there are two identical copies of each chip select which can be routed to the left and right side of the DIMM. For 8 rank DIMMs, only one copy is available, which must be used in a “T” configuration to both sides.

The chip select number indicates the physical rank number. The mapping to the DCKE inputs can be found in the Host Interface Protocol chapter.

5.1.2.2 Clock Enable output

The MB provides 8 Clock Enable outputs which consists of an A and B copy of four independently controlled Clock Enables. In 2 DCKE mode the CKE0 and CKE2 are controlled together and CKE1 and CKE3 are controlled together. In 4 DCKE mode or Soft CKE mode the 4 output sets are controlled together. See the Host Interface Protocol chapter for detail. The CKEs must be routed according to the table above.

5.1.2.3 On Die Termination outputs.

The MB provides 2 sets of ODT outputs with 2 copies each. Each set is independently controlled. In general ODT0 is connected to Rank 0 and ODT1 is connected to Rank 1, but this is Raw Card dependent. Refer to the Raw Card specifications for details.

For each set of ODT outputs there are 16 control bits to determine when it is activated. 8 bits for reads to each of the 8 physical ranks, and 8 bits for writes to each of the physical ranks.

5.1.3 Clock Outputs

There are four differential clock outputs to the DRAMs. Y[3:0]_t / Y[3:0]_c.

Each clock output can be enabled or disabled independently to allow unused clocks to be disabled. The drive strength of the clock output are controlled together as a group.

5.1.4 Reset

The MB supplies one RESET output, labeled QRST_n. This output goes to all DRAMs on the DIMM, if this output is used. Alternatively, the RESET_n signal from the DIMM connector may connect directly to the DRAMs.

5.1.5 DRAM data bus

The DRAM data bus consists of 72 data bits and 18 strobe pairs. For x4 devices there are 4 data bits and one strobe pair per DRAM of each rank. For x8 devices are there 8 data bits and one strobe pair per rank.

MDQS[17:9] are not used for x8 devices. The DM inputs of the DRAMs are tied to VSS.

Table 24 — Data bus connections

DRAM	x4 DQ bits	x4 DQS bits	x8 DQ bits	x8 DQS bits
0	MDQ[3:0]	MDQS[0]_t / _c	MDQ[7:0]	MDQS[0]_t / _c
1	MDQ[7:4]	MDQS[9]_t / _c	MDQ[15:8]	MDQS[1]_t / _c
2	MDQ[11:8]	MDQS[1]_t / _c	MDQ[23:16]	MDQS[2]_t / _c
3	MDQ[15:12]	MDQS[10]_t / _c	MDQ[31:24]	MDQS[3]_t / _c
4	MDQ[19:16]	MDQS[2]_t / _c	MDQ[39:32]	MDQS[4]_t / _c
5	MDQ[23:20]	MDQS[11]_t / _c	MDQ[47:40]	MDQS[5]_t / _c
6	MDQ[27:24]	MDQS[3]_t / _c	MDQ[55:48]	MDQS[6]_t / _c
7	MDQ[31:28]	MDQS[12]_t / _c	MDQ[63:56]	MDQS[7]_t / _c
8	MDQ[35:32]	MDQS[4]_t / _c	MDQ[71:64]	MDQS[8]_t / _c
9	MDQ[39:36]	MDQS[13]_t / _c	(NA)	(NA)
10	MDQ[43:40]	MDQS[5]_t / _c	(NA)	(NA)
11	MDQ[47:44]	MDQS[14]_t / _c	(NA)	(NA)
12	MDQ[51:48]	MDQS[6]_t / _c	(NA)	(NA)
13	MDQ[55:52]	MDQS[15]_t / _c	(NA)	(NA)
14	MDQ[59:56]	MDQS[7]_t / _c	(NA)	(NA)
15	MDQ[63:60]	MDQS[16]_t / _c	(NA)	(NA)
16	MDQ[67:64]	MDQS[8]_t / _c	(NA)	(NA)
17	MDQ[71:68]	MDQS[17]_t / _c	(NA)	(NA)

5.2 Turnaround Cycles

It is the host controller's responsibility to account for data bus turnaround cycles between accesses to different physical ranks. Normally back to back reads or back to back writes to the same rank require no turnaround cycles as the same termination will be used, and the same DRAMs drive the bus (for a read). When rank multiplication is used, the host controller has two choices. The controller can be designed to have knowledge of the physical ranks and their mapping, and only add turnaround cycles when there is a switch between physical ranks. If the controller does not have knowledge of the physical ranks it can add turnaround cycles at all times. This latter method is not as efficient, as it adds turnaround cycles when they are not required.

6 Initialization

6.1 Initialization Overview

The sequence of steps below is an overview of the power-up initialization of the Memory Buffer. Figure 13 shows a graphical representation of the same steps. Detailed requirements for each step are provided in the following sections. Note that the sequence below does not distinguish between host hardware and host software (i.e., BIOS).

1. Power-Up (Same requirements as SSTE32882)
   a. Ramp of voltage rails
   b. Generation of stable clock
   c. De-assertion of RESET_n
2. Determination of DIMM configuration via SPD read out
3. CA Clock to CMD Training[1]
   a. Sets the optimal phase of the clock to CA and Ctrl signals.
4. Memory Buffer Initialization
   a. Host initializes buffer control words
5. DRAM Initialization
   a. Host initializes DRAM MRS registers
6. DRAM ZQ Calibration
   a. Host issues ZQCAL command to DRAM
7. Memory Buffer to DRAM Interface Training
   a. Done by the buffer, triggered by host RCW write
   b. Write Leveling
   c. Read Enable training
   d. Read/Write DQ/DQS training[2]

Host can wait for a per-physical rank time-out of tCAL=10ms or periodically poll the buffer via SMBus CSR read or wait for ERROUT_n.

8. Host to Memory Buffer Interface Training[3]
   a. Done by host
9. Normal Operation

1.This step is optional for the MB but may be done by some platforms. No special support by the MB is required.
2.This step is optional for the MB but may be required for stable DIMM operation.
3.This step is optional for the MB but may be done by some platforms.

6.1 Initialization Overview (cont'd)

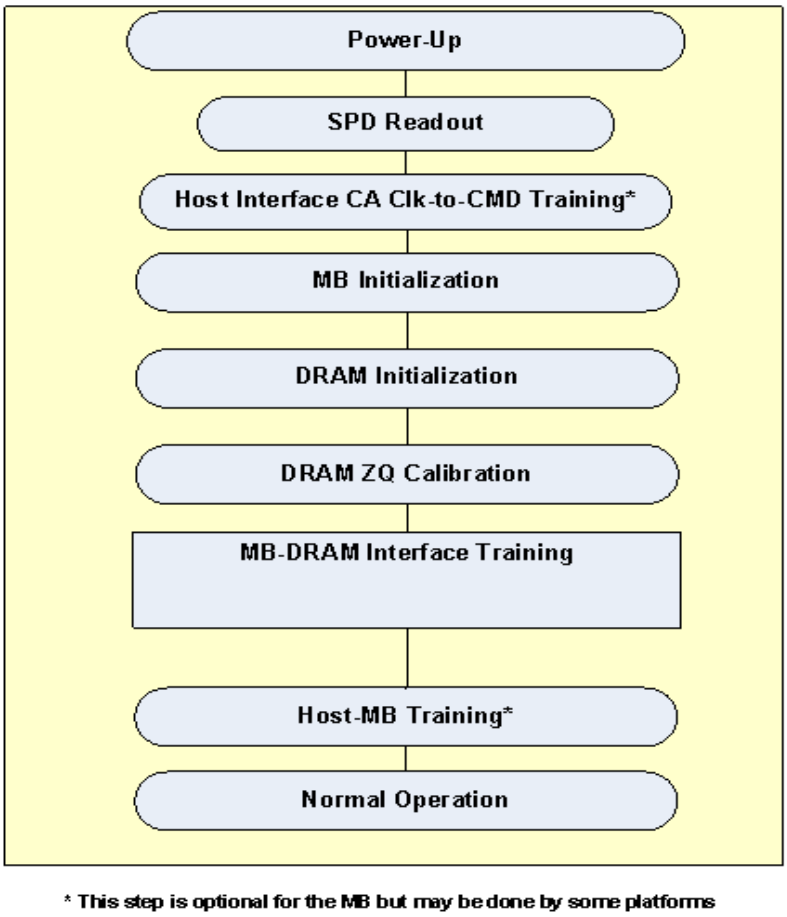


Figure 13 — Initialization Overview

6.2 Power-on Initialization

The Memory Buffer can be powered-on at 1.5 V or 1.35 V. After the voltage ramp, stable power is provided for a minimum of 200 uS with RESET_n asserted. When the reset input RESET_n is LOW, all input receivers are disabled, and can be left floating. The MB output pin QRST_n follows the MB input pin RESET_n. Therefore the reference voltage (V_{REF}) doesn't need to be stable. In addition, when RESET_n is LOW, all control registers are restored to their default states. The outputs QACKE[3:0] and QBCKE[3:0] must drive LOW during reset. All other outputs must float. As long as the RESET_n input is pulled LOW, the DDR3 MB is in low power state and input termination is not present. A certain period of time (t_{ACT}) before the RESET_n input is pulled HIGH the reference voltage needs to be stable within specification, the clock input signal must be stable, the register inputs DCS[1:0]_n must be pulled HIGH to prevent accidental access to the control registers and DCKE[2:0] as well as DCKE3/DODT[1] must be pulled LOW.

6.2.1 Clock Stabilization Time t_{STAB}

During PLL stabilization time t_{STAB} the memory buffer is not fully operational. In order to avoid invalid commands being sent to the DRAMs some rules apply to the inputs of the buffer:

- All DCS signals need to be kept high. No DRAM command or control word write[1] may take place.
- All DCKE signals don't change their state.
- DODT[0] or DODT[1:0] signals (depending on F0RC6 setting) are kept at a stable valid logic level.

These rules apply to any instance where stabilization time t_{STAB} is required:

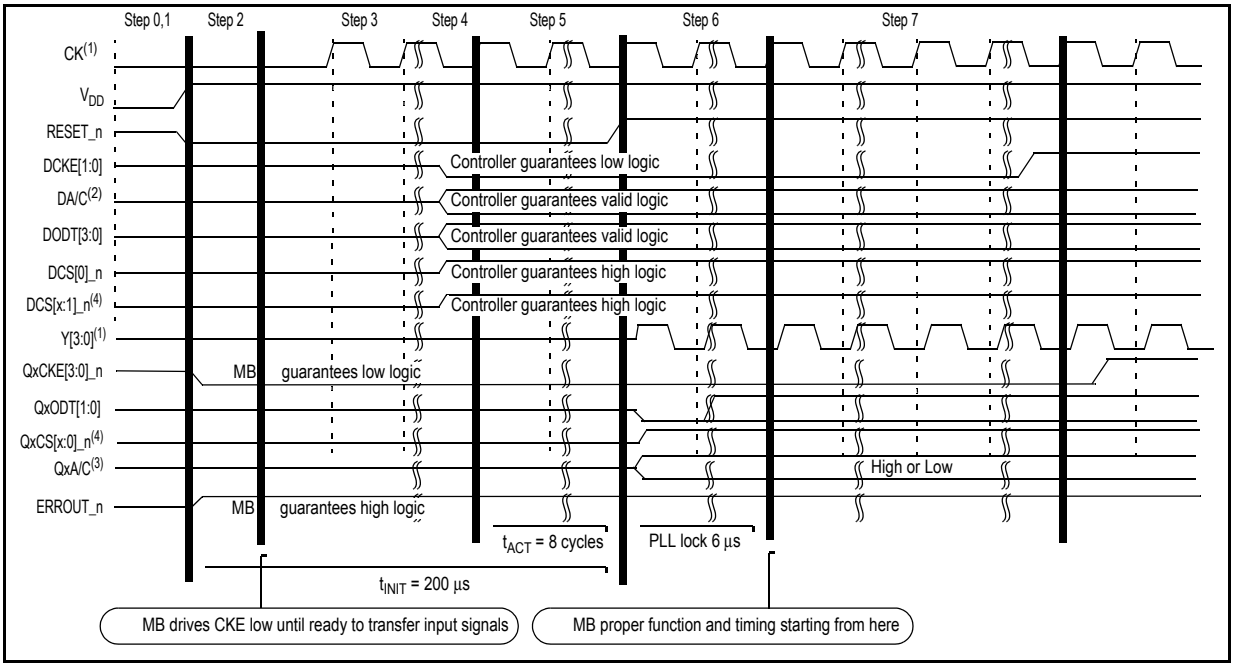
- Exit from Reset
- Exit from clock stop power down
- Changing clocking related registers (F0RC2, F0RC10, F0RC11, F1RC8, F1RC11-F1RC15)[2]
- Changing input clock frequency during boot or run time

Since the buffer has not reached a stable state the termination on the host interface will be undefined before the end of the stabilization time.

After reset and after the PLL stabilization time (t_{STAB}) the device must meet the input setup and hold specifications, as well as accept and transfer input signals to the corresponding outputs. The RESET_n input must always be held at a valid logic level once the input clock is present.

1. No control word writes are allowed during t_{STAB} after reset/frequency change/clock stop.
2. These requirements mean that we have to wait two t_{STAB} times during every initialization, one after RESET_n de-assertion and one after all the clocking related control words have been written.

6.2.1 Clock Stabilization Time t_{STAB} (cont'd)



(1) CK_c and Y[3:0]_c left out for better visibility

(2) DCKE[2:0], DCKE[3]/DODT[1], DODT[0] and DCS0[3:0]_n are not included in this range

(3) QxCKE[3:0], QxODT[1:0], QxCS[7:0]_n are not included in this range

(4) x = JEDEC standard DIMMs, x = 7 for non-JEDEC applications

(5) x = 3 for dual or quad rank DIMMs, x = 7 for octal rank DIMMs

Figure 14 — Timing of clock and data during power-on initialization sequence

From a device perspective, the initialization sequence must be as shown in Table 25.

Table 25 — MB Device Initialization Sequence[a]

Step	Power	Inputs: Signals provided by the controller								Outputs: Signals provided by the device					
	VDD, AVDD, PVDD	RESET_n	Vref	DCS [y:0]_n[b]	DODT [1:0]	DCKE [3:0]	DA/C	PAR_IN	CK_t CK_c	QCS [y:0]_n[c]	QODT [1:0]	QCKE [3:0]	QxA/C	ERR OUT_n	Y[3:0]_t Y[3:0]_c
0	0V	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	Z	Z	Z	Z	Z	Z
1	0-->V_{DD}	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z
2[d]	V_{DD} 1.5V-->1.35V 1.35V-->1.5V	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L	Z	Z	L[e]	Z	H[4]	Z
3	V_{DD}	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	running	Z	Z	L	Z	H	Z
4	V_{DD}	L	X or Z	H	X or Z	L	X or Z	X or Z	running	Z	Z	L	Z	H	Z
5	V_{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z
6	V_{DD}	H	stable voltage	H	X	L	X	X	running	H	L[f]	L	X	H	running
7[g]	V_{DD}	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the 'DRAM Protocol' chapter					

NOTES:

a. X = Logic LOW or logic HIGH. Z = floating.
b. y = 3 for JEDEC standard DIMM, y = 7 for non-JEDEC application
c. y = 3 for dual or quad rank DIMMs, y = 7 for octal rank DIMMs.
d. The system may power up using either 1.5V or 1.35V. The BIOS reads the SPD and adjusts the voltage if needed from 1.35V to 1.5V or from 1.5V to 1.35V. After the voltage transition, stable power is provided for a minimum of 200 uS with RESET_n asserted.
e. QxCKE[3:0] and ERROUT_n will be driven to these logic states by the register after RESET_n is driven LOW and VDD is 1.5V or 1.35V (nominal).
f. This indicates the state of QxODT[1:0] after RESET_n switches from LOW-to-HIGH and before the rising CK_t edge (falling CK_c edge).
g. Step 7 is a typical usage example and is not a MB requirement.

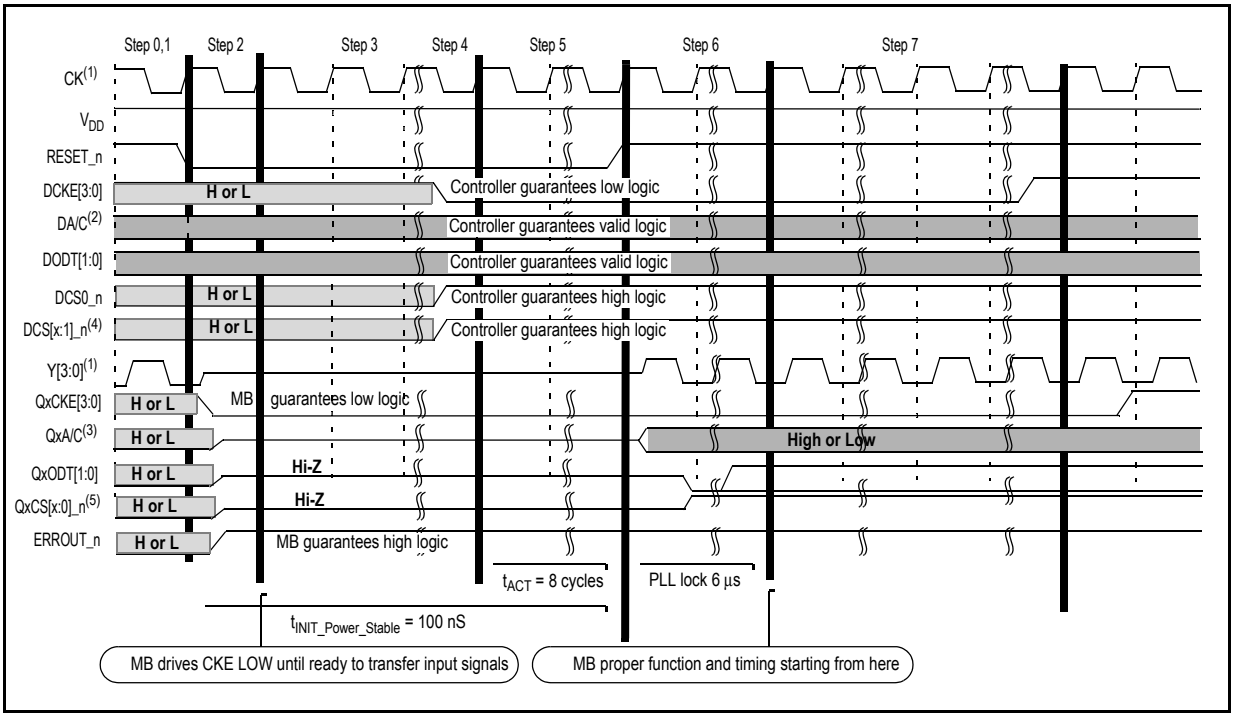
6.2.1 Clock Stabilization Time t_{STAB} (cont'd)

To ensure defined outputs from the memory buffer before a stable clock has been supplied, the memory buffer must enter the reset state during power-up. It may leave this state only after a LOW to HIGH transition on RESET_n while a stable clock signal is present on CK_t and CK_c. In the DDR3 LRDIMM application, RESET_n is specified to be completely asynchronous with respect to CK_t and CK_c. Therefore, no timing relationship can be guaranteed between the two.

As part of the initialization all control words are reset to their default state which is "0", except when explicitly defined otherwise. After initialization, the host only needs to write to those control registers whose contents need to be changed.

6.3 Initialization with Stable Power (Soft Reset)

The timing diagram in Figure 15 depicts the initialization sequence with stable power and clock. This will apply to the situation when we have a soft reset in the system. RESET_n will be asserted for minimum 100ns. This RESET_n timing is based on DDR3 DRAM Reset Initialization with Stable Power requirement, and is a minimum requirement. Actual RESET_n timing can vary base on specific system requirement, but it cannot be less than 100ns as required by JESD79-3.



(1) CK_c and Y[3:0]_c left out for better visibility

(2) DCKE[2:0], DCKE[3]/DODT[1], DODT[0] and DCS0[3:0]_n are not included in this range

(3) QxCKE[3:0], QxODT[1:0], QxCS[7:0]_n are not included in this range

(4) x = JEDEC standard DIMMs, x = 7 for non-JEDEC applications

(5) n = 3 for dual or quad rank DIMMs, n = 7 for octal rank DIMMs.

Figure 15 — Timing of clock and data during initialization sequence with stable power

6.3 Initialization with Stable Power (Soft Reset) (cont'd)

Table 26 — MB Device Initialization Sequence[a] when Power and Clock are Stable

Step	Power	Inputs: Signals provided by the controller								Outputs: Signals provided by the device					
	VDD, AVDD, PVDD	RESET_n	Vref	DCS [y:0]_n[b]	DODT [1:0]	DCKE [3:0]	DA/C	PAR_IN	CK_t CK_c	QCS [y:0]_n[c]	QODT [1:0]	QCKE [3:0]	QxA/C	ERR OUTn	Y[3:0]_t Y[3:0]_c
0	V_{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running
1	V_{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running
2	V_{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L[d]	Z	H[4]	Z
3	V_{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L	Z	H	Z
4	V_{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z
5	V_{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z
6	V_{DD}	H	stable voltage	H	X	L	X	X	running	H	L[e]	L	X	H	running
7	V_{DD}	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the 'DRAM Protocol' chapter					

NOTES:

a. X = Logic LOW or logic HIGH. Z = floating.

b. y = 3 for JEDEC standard DIMM, y = 7 for non-JEDEC application

c. y= 3 for dual or quad rank DIMMs, y = 7 for octal rank DIMMs.

d. QxCKE[3:0] and ERROUT_n will be driven to these logic states by the register after RESET_n is driven LOW and V_{DD} is nominal

e. This indicates the state of QxODT[1:0] after RESET_n switches from LOW-to-HIGH and before the rising CK_t edge (falling CK_c edge)

6.4 Host RCW to Configure MB

After the MB is ready to receive commands and addresses without error, the host needs to configure the MB with register control word writes and/or SMBUS writes (step 4). At reset all RCWs had been reset to their default state which is '0' except when explicitly noted otherwise. Therefore the host only needs to write those control words whose contents need to be changed.

For correct operation, as part of MB initialization sequence, host must write MRS Control Register (MRS_CTRL; Address ACh) bits 2:1 to either 00b or 10b via extended control word. Host must Write Rx_MR1,2 and MRx_Snoop registers using the correct per Rank Rtt_nom values via extended control word.

6.5 Host MRS to Configure DRAM

The host sends MRS commands to the DRAM mode registers (MR2, MR3, MR1, MR0) to configure proper DRAM operation for all physical ranks behind the MB. The host can utilize either the MB broadcast mode to send MRS commands to all physical ranks associated with a logical rank or the MB physical rank mode to target MRS commands to specific physical ranks by programming the corresponding mode to the F0RC14 DRAM MRS Control bits.

6.6 Host to DRAM ZQ Calibration

The host sends ZQCL (ZQ Calibration Long) commands to all ranks behind the MB. The MB broadcasts ZQ calibration commands (both ZQCL and ZQCS) to all physical ranks associated with a logical rank. The host may issue ZQ calibration commands sequentially to each logical rank (i.e., wait for tZQinit, tZQoper or tZQCS after each ZQ calibration command before issuing the next one) or it may overlap the ZQ calibration commands to all ranks.

The MB may or may not perform any calibration for its own I/O circuits on receipt of ZQCL or ZQCS calibration commands.

6.7 MB-DRAM Training

After all the DRAMs are fully operational, the host triggers the DRAM interface training by setting the control bit DA4 in F0RC12. Once enabled, the MB assumes autonomous control of the Command/ Address, Control and Data/Strobe signals to the DRAMs, without any further assistance from the host.

The MB performs ‘Write Leveling’ to the DRAMs to ensure successful writes, and ‘Read Enable Training’ to ensure it can capture read data from the DRAMs correctly, as part of the DRAM interface training.

No DRAM commands or control word writes either over the Command/Address and Control buses or via SMBus can be issued to the MB until the MB-DRAM Interface training is complete and the DODTn inputs must be kept low. The MB responds to SMBus CSR read accesses whether or not DRAM interface training is active. To determine DRAM interface training completion the host may either wait for a time ‘tCAL * number of physical ranks’ which is the maximum amount of time that the MB-DRAM Interface training is allowed to take, or it may periodically poll the content of the MB CSR ‘Training Completion’ (see 13.7.4, Configuration Register) over the SMBus.

In addition, training completion can be signaled by the assertion of ERROUT_n. This is not the power-up default but can be enabled by setting the DBA1 bit in the F2RC3 Training Completion Control Word.

6.8 Host-MB Training

Now the host can train the MB host interface. The host sets the ‘Connector DQ interface write leveling’ bits in F0RC12 (=0bx001) in order to perform host interface write leveling. Optionally a MB may support RDIMM backward compatible host interface write leveling by intercepting ‘Write leveling enable’ (MR1 A7) and ‘Qoff’ (MR1 A12) commands to the DRAMs. The MB asynchronously feeds back CK_t/CK_c, sampled with the rising edge of DQS_t/DQS_c, through the DQ bus (in the same way as a DDR3 DRAM does). Since write leveling requests from the host terminate at the MB, multiple write leveling requests to the MB (i.e., one per rank) will give the same result and are optional. It is sufficient to perform host interface write leveling only once regardless of how many logical or physical ranks are supported by the MB.

6.8 Host-MB Training (cont'd)

MB DRAM interface training must be completed before any MB host interface read training to reflect the correct read round trip delay to and from an LRDIMM. This delay consists of:

(1) Host to MB delay for command

(2) Command delay through the MB[1]

(3) MB command to DRAM delay

(4) DRAM latency

(5) DRAM data/strobe return time to MB

(6) Data/strobe delay through the MB

(7) MB to host delay for data/strobe

MB DRAM interface training must be completed before any MB host interface read or write training to ensure that the MB DRAM interface is configured optimally for DRAM reads and writes. The host performs normal writes to DRAM for write DQ/DQS margining, with failure occurring through incorrect strobing of write data through the MB. The host performs read DQ/DQS margining by using normal reads from DRAM or by using the DRAM multipurpose register (MPR) with failure occurring through invalid DQ/DQS alignment at the host I/O pins. No special support by the MB is required for host interface read training.

1. The data/strobe delay through the MB during writes can be different than the command delay through the MB.

7 Electrical, Timing, Power and Thermal

This section contains a description of the LRDIMM Memory Buffer (MB) electrical DC parameters, timing parameters, power considerations and thermal considerations.

7.1 Electrical DC and AC Parameters

7.1.1 Absolute maximum ratings

Table 27 — Absolute maximum ratings over operating free-air temperature range (1)

Symbol	Parameter	Conditions	Min	Max	Unit
VCCSPD	SMBus interface supply voltage		–0.5	+4.3	V
V_{IO_SPD}	SMBus Receiver input, Driver output and I/O voltage (SA[2:0], SCL, SDA, EVENT_n)		–0.5	+4.3	V
V_{DD}	Supply voltages (VDD, AVDD, PVDD)		–0.4	+1.975	V
V_I	Receiver input voltage	See Note 2 and 3	–0.4	V_{DD} + 0.5	V
V_{REF}	Reference voltage (VREFCA, QVREFCA, VREFDQ, QVREFDQ)		–0.4	V_{DD} + 0.5	V
V_O	Driver output voltage	See Note 2 and 3	–0.4	V_{DD} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$	-	±50	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$	-	±50	mA
I_O	Continuous output current	$0 < V_O < V_{DD}$	-	±50	mA
I_{CCC}	Continuous current through each V_{DD} or GND pin		-	±100	mA
T_{stg}	Storage temperature		-65	+150	°C
T_{case}	Case temperature		-	125	°C

NOTE 1 Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

NOTE 2 The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 3 This value is limited to 1.975 V maximum.

7.1.2 DC and AC Specifications

7.1.2.1 DC and AC Specifications for the SMBus Interface

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the MB SMBus interface. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 28 — Operating Conditions for the SMBUS interface

Symbol	Parameter	Min	Max	Units
V_{CCSPD}	Supply Voltage	3.0	3.6	V

Table 29 — AC Measurement Conditions for SMBUS interface

Symbol	Parameter	Min	Max	Units
C_L	Load capacitance	100		pF
	Input rise and fall times	--	50	ns
	Input levels	0.2 * V_{CCSPD} to 0.8 * V_{CCSPD}		V
	Input and output timing reference levels	0.3 * V_{CCSPD} to 0.7 * V_{CCSPD}		V

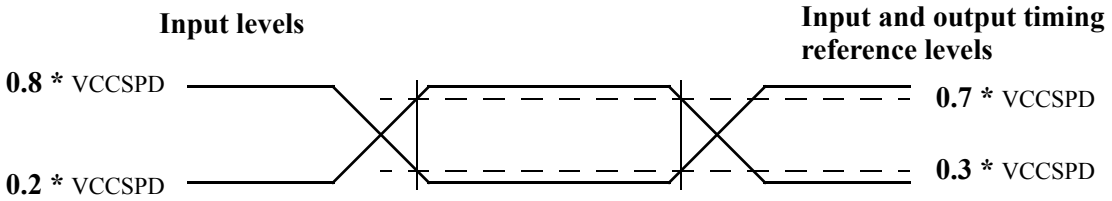


Figure 16 — AC Measurement I/O Waveform

Table 30 — Input Parameters for SMBUS interface

Symbol	Parameter[1,2]	Test Condition	Min	Max	Units
C_{IN}	Input capacitance (SDA)	--	--	8	pF
C_{IN}	Input capacitance (other pins)	--	--	6	pF
Z_{EIL}	Ei (SA0, SA1, SA2) input impedance	$V_{IN} < 0.3 * V_{CCSPD}$	30	--	kΩ
Z_{EIH}	Ei (SA0, SA1, SA2) input impedance	$V_{IN} > 0.7 * V_{CCSPD}$	800	--	kΩ

NOTE 1 T_A = 25 °C, f = 100 kHz
NOTE 2 Verified by design and characterization, not necessarily tested on all devices

Table 31 — DC Characteristics for SMBUS interface

Symbol	Parameter	Test Condition (in addition to those in Table 28 on page 60)	Min	Max	Units
I_{LI}	Input leakage current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CCSPD}	--	±5	µA
I_{LO}	Output leakage current	$V_{OUT} = V_{SS}$ or V_{CCSPD}, SDA in Hi-Z	--	±5	µA
I_{DD}	Supply current	$V_{CCSPD} = 3.3$ V, $f_C = 100$ kHz (rise/fall time < 30 ns)	--	5	mA
I_{DD1}	Standby Supply current	$V_{IN} = V_{SS}$ or V_{CCSPD}, $V_{CCSPD} = 3.6$ V	--	100	µA
V_{IL}	Input low voltage (SCL, SDA)	--	-0.5	0.3 * V_{CCSPD}	V
V_{IH}	Input high voltage (SCL, SDA)	--	0.7 * V_{CCSPD}	V_{CCSPD} + 1	V
V_{HV}[1]	SA0 high voltage	$V_{HV} - V_{CCSPD} \geq 4.8$ V	7	10	V
V_{OL}	Output low voltage	IOL = 2.1 mA, 3.0 V ≤ V_{CCSPD} ≤ 3.6 V	--	0.4	V
		IOL = 0.7 mA, V_{CCSPD} = 3.0 - 3.6V	--	0.2	V
V_{HYST}[2]	Input hysteresis		0.05 * V_{CCPD}	--	V

NOTE 1 V_{HV} is used by SPD device. For DDR3 LRDIMM, a series resistor is connected to the Memory Buffer SA0 input (refer to "Figure 12: Schematic of SPD/Thermal Sensor and MB" in the PC3-LRDIMM Design Specification Body V034). As such, the voltage at the MB SA0 input will not be higher than 4.3v ($V_{IO_SPD(max)}$) even when V_{HV} is applied at the LRDIMM SA0 connector pin.

NOTE 2 Optional.

7.1.2.1 DC and AC Specifications for the SMBus Interface (cont'd)

Table 32 — AC Characteristics for SMBUS interface

		$V_{CCSPD} \geq$ **3.0 V**		
Symbol	**Parameter**	**Min**	**Max**	**Units**
f_{SCL}	Clock frequency	10	100	kHz
t_{HIGH}	Clock pulse width high time	4000	--	ns
t_{LOW}[3]	Clock pulse width low time	4700	--	ns
$t_{TIMEOUT}$[4,5]	Detect clock low timeout, Capabilities Register bit 6 = 0	10	60	ms
$t_{TIMEOUT}$[4,5]	Detect clock low timeout, Capabilities Register bit 6 = 1	25	35	ms
t_R[2]	SDA rise time	20	300	ns
t_F[2]	SDA fall time	20	300	ns
$t_{SU:DAT}$	Data in setup time	250	--	ns
$t_{HD:DI}$	Data in hold time	0	--	ns
$t_{HD:DAT}$	Data out hold time	300	900	ns
$t_{SU:STA}$[1]	Start condition setup time	4700	--	ns
$t_{HD:STA}$	Start condition hold time	4000	--	ns
$t_{SU:STO}$	Stop condition setup time	4000	--	ns
t_{BUF}	Time between Stop Condition and next Start Condition	4700	--	ns
t_W	Write time	--	10	ms

NOTE 1 For a reSTART condition, or following a write cycle
NOTE 2 Guaranteed by design and characterization, not necessarily tested
NOTE 3 The MB SMBUS interface logic shall not initiate clock stretching
NOTE 4 Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of $t_{TIMEOUT,MIN}$. After the master in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT,MAX}$. Typical device examples include the host controller, and embedded controller and most devices that can master the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or a stop condition. A timeout condition can only be ensured if the device that is forcing the timeout holds SCL low for $t_{TIMEOUT,MAX}$ or longer.
NOTE 5 Bus timeout value supported depends on setting of TMOUT bit 6 in the Capabilities Register.

7.1.2.1 DC and AC Specifications for the SMBus Interface (cont'd)

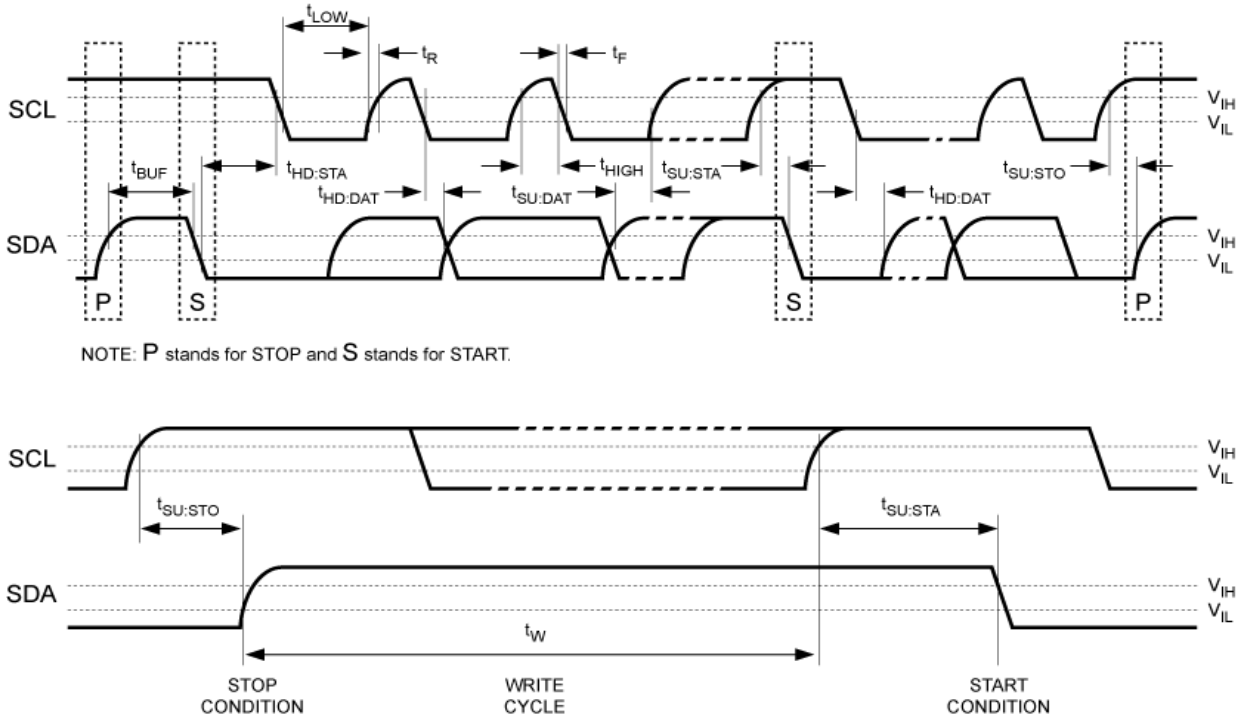


Figure 17 — AC Waveforms

7.1.2.2 DC and AC Specifications for the Host and DRAM Interface

The DDR3 LRDIMM MB parametric values are specified for the device default control word settings, unless otherwise stated. Note that the F[0]RC10 setting does not affect any of the parametric values.

Table 33 — Operating Electrical Characteristics

Symbol	Parameter	Signals	Min	Nom	Max	Unit
V_{DD}	DC Supply voltage (DDR3)	VDD, VDDA,VDDP	1.425	1.5	1.575	V
	DC Supply voltage (DDR3L)	VDD, VDDA,VDDP	1.283	1.35	1.451	V
VCCSPD	SMBus Interface Supply voltage	VCCSPD	3.0	3.3	3.6	V
V_{REF}	DC Reference voltage		0.49 x V_{DD}	0.50 x V_{DD}	0.51 x V_{DD}	V
V_{TT}	DC Termination voltage[a]		V_{REF} – 40 mV	V_{REF}	V_{REF} + 40 mV	V
$V_{IH(AC)}$	AC HIGH-level input voltage (DDR3)	CMD/ADD/CTRL inputs[b]	V_{REF} + 0.1	–	V_{DD} + 0.4	V
$V_{IL(AC)}$	AC LOW-level input voltage (DDR3)	CMD/ADD/CTRL inputs[a]	–0.4	–	V_{REF} – 0.1	V
$V_{IH(DC)}$	DC HIGH-level input voltage (DDR3)	CMD/ADD/CTRL inputs[a]	V_{REF} + 0.1	–	V_{DD}	V
$V_{IL(DC)}$	DC LOW-level input voltage (DDR3)	CMD/ADD/CTRL inputs[a]	V_{SS}	–	V_{REF} – 0.1	V
$V_{IH(AC)_DQ}$	AC HIGH-level input voltage (DDR3)	DQ inputs	V_{REF} + 0.1	–	V_{DD} + 0.4	V
$V_{IL(AC)_DQ}$	AC LOW-level input voltage (DDR3)	DQ inputs	–0.4	–	V_{REF} – 0.1	V
$V_{IH(DC)_DQ}$	DC HIGH-level input voltage (DDR3)	DQ inputs	V_{REF} + 0.1	–	V_{DD}	V
$V_{IL(DC)_DQ}$	DC LOW-level input voltage (DDR3)	DQ inputs	V_{SS}	–	V_{REF} – 0.1	V
$V_{IH(AC)_MDQ}$	AC HIGH-level input voltage (DDR3)	MDQ inputs	V_{REF} + 0.1	–	V_{DD} + 0.4	V
$V_{IL(AC)_MDQ}$	AC LOW-level input voltage (DDR3)	MDQ inputs	–0.4	–	V_{REF} – 0.1	V
$V_{IH(DC)_MDQ}$	DC HIGH-level input voltage (DDR3)	MDQ inputs	V_{REF} + 0.1	–	V_{DD}	V
$V_{IL(DC)_MDQ}$	DC LOW-level input voltage (DDR3)	MDQ inputs	V_{SS}	–	V_{REF} – 0.1	V
$V_{IH(AC)}$	AC HIGH-level input voltage (DDR3L)	CMD/ADD/CTRL inputs[b]	V_{REF} + 0.09	–	V_{DD} + 0.2	V
$V_{IL(AC)}$	AC LOW-level input voltage (DDR3L)	CMD/ADD/CTRL inputs[b]	–0.2	–	V_{REF} – 0.09	V
$V_{IH(DC)}$	DC HIGH-level input voltage (DDR3L)	CMD/ADD/CTRL inputs[b]	V_{REF} + 0.09	–	V_{DD}	V
$V_{IL(DC)}$	DC LOW-level input voltage (DDR3L)	CMD/ADD/CTRL inputs[b]	V_{SS}	–	V_{REF} – 0.09	V
$V_{IH(AC)_DQ}$	AC HIGH-level input voltage (DDR3L)	DQ inputs	V_{REF} + 0.09	–	V_{DD} + 0.2	V
$V_{IL(AC)_DQ}$	AC LOW-level input voltage (DDR3L)	DQ inputs	–0.2	–	V_{REF} – 0.09	V
$V_{IH(DC)_DQ}$	DC HIGH-level input voltage (DDR3L)	DQ inputs	V_{REF} + 0.09	–	V_{DD}	V
$V_{IL(DC)_DQ}$	DC LOW-level input voltage (DDR3L)	DQ inputs	V_{SS}	–	V_{REF} – 0.09	V
$V_{IH(AC)_MDQ}$	AC HIGH-level input voltage (DDR3L)	MDQ inputs	V_{REF} + 0.09	–	V_{DD} + 0.2	V
$V_{IL(AC)_MDQ}$	AC LOW-level input voltage (DDR3L)	MDQ inputs	–0.2	–	V_{REF} – 0.09	V
$V_{IH(DC)_MDQ}$	DC HIGH-level input voltage (DDR3L)	MDQ inputs	V_{REF} + 0.09	–	V_{DD}	V
$V_{IL(DC)_MDQ}$	DC LOW-level input voltage (DDR3L)	MDQ inputs	V_{SS}	–	V_{REF} – 0.09	V
$V_{IH(CMOS)}$	HIGH-level input voltage	RESET_n	0.65 x VDD	–	V_{DD}	V
$V_{IL(CMOS)}$	LOW-level input voltage	RESET_n	0	–	0.35 x VDD	V
$V_{IL\ (Static)}$	Static LOW-level input voltage[c]	CK_t, CK_c	–	–	0.35 x VDD	V
$V_{IX(AC)}$	Differential input crosspoint voltage range	CK_t, CK_c	0.5xV_{DD} - 0.2	0.5 x V_{DD}	0.5xV_{DD} + 0.2	V
$V_{ID(AC)}$	Differential input voltage[d] (DDR3)	CK_t, CK_c	0.2	–	V_{DD}	V
$V_{ID(AC)}$	Differential input voltage[d] (DDR3L)	CK_t, CK_c	0.18	–	V_{DD}	V
$V_{IX(AC)_DQS}$	Differential input crosspoint voltage range	DQS_t, DQS_c	0.5xV_{DD} - 0.2	0.5 x V_{DD}	0.5xV_{DD} + 0.2	V
$V_{ID(AC)_DQS}$	Differential input voltage[e] (DDR3)	DQS_t, DQS_c	0.2	–	V_{DD}	V
$V_{ID(AC)_DQS}$	Differential input voltage[e] (DDR3L)	DQS_t, DQS_c	0.18	–	V_{DD}	V
$V_{IX(AC)_MDQS}$	Differential input crosspoint voltage range	MDQS_t, MDQS_c	0.5xV_{DD} - 0.2	0.5 x V_{DD}	0.5xV_{DD} + 0.2	V
$V_{ID(AC)_MDQS}$	Differential input voltage[f] (DDR3)	MDQS_t, MDQS_c	0.2	–	V_{DD}	V
$V_{ID(AC)_MDQS}$	Differential input voltage[f] (DDR3L)	MDQS_t, MDQS_c	0.18	–	V_{DD}	V

Table 33 — Operating Electrical Characteristics

Symbol	Parameter	Signals	Min	Nom	Max	Unit
I_{OH}	HIGH-level output current[g]	All CA outputs	-11	–	–	mA
I_{OL}	LOW-level output current[g]	All CA outputs	11	–	–	mA
I_{OH}	HIGH-level output current[g]	All DQ outputs	-10.7	–	–	mA
I_{OL}	LOW-level output current[g]	All DQ outputs	10.7	–	–	mA
I_{OL_ERROUT}	LOW-level output current	ERROUT_n	25	–	–	mA
I_{OL_EVENT}	LOW-level output current	EVENT	25	–	–	mA
V_{OD}	Differential re-driven clock swing	Yn_t, Yn_c	0.45	–	V_{DD}	V
V_{OX}	Differential Output Crosspoint Voltage	Yn_t, Yn_c, DQS_t, DQS_c, MDQS_t, MDQS_c	$0.5xV_{DD} - 0.09$	–	$0.5xV_{DD} + 0.09$	V
$T_{case\ (max)}$	Case temperature[h]		-	-	125[i]	°C

NOTES:
a. VTT supply voltage specification is for QCMD/QADDR/QCTRL/Yn_t/Yn_c only
b. DCKE[2:0], DCKE[3]/DODT[1], DODT[0], DA0..DA15, DBA0..DBA2, DRAS_n, DCAS_n, DWE_n, PAR_IN, DCS[7:0]_n.
c. This spec applies only when both CK_t and CK_c are actively driven LOW. It does not apply when CK/CK# are floating.
d. VID is the magnitude of the difference between the input level on CK_t and the input level on CK_c See Diagram (Figure 48)
e. VID_DQS is the magnitude of the difference between the input level on DQS_t and the input level on DQS_c See Diagram (Figure 48)
f. VID_MDQS is the magnitude of the difference between the input level on MDQS_t and the input level on MDQS_c See Diagram (Figure 48)
g. Default settings
h. Measurement procedure, see JESD51-2
i. Since MB silicon is bare die on FBGA package, the assumption is Tcase (max) is very close to silicon Tj (max). Hence, tcase (max) of 125C is used for all speed grades.

7.1.3 DC specifications, IDD Specifications

Table 34 — DC Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH voltage (QCA pins)	I_{OH} = –11 mA	V_{DD}-0.4	-	-	V
V_{OL}	Output LOW voltage (QCA pins)	I_{OL} = 11 mA	-	-	0.4	V
V_{OH_DQ}	Output HIGH voltage (DQ pins)	I_{OH} = –10.7 mA	V_{DD}-0.4	-	-	V
V_{OL_DQ}	Output LOW voltage (DQ pins)	I_{OL} = 10.7 mA	-	-	0.4	V
V_{OL_ERROUT}	Output LOW voltage (ERROUT_n pin)	I_{OL} = 25 mA	-	-	0.4	V
V_{OL_EVENT}	Output LOW voltage (EVENT pin)	I_{OL} = 25 mA	-	-	0.4	V
I_{I_RST}	Input current for RESET_n pin	RESET_n, $V_I = V_{DD}$ or GND	-	-	±5	µA
I_{ID}	Input current for CMD, ADD, CNTRL and PAR_IN input pins **Note**: Spec value is for each pin	Data inputs[a], $V_I = V_{DD}$ or GND	-	-	±5	µA
I_{I_CK}	Input current for CK_t and CK_c input pins	CK_t, CK_c[b]; $V_I = V_{DD}$ or GND	-5		150	µA
I_{I_DQ}	Input current for DQ input pins **Note**: Spec value is for one DQ pin	DQ; $V_I = V_{DD}$ or GND	-	-	TBD	µA
I_{DD}	Static standby current	RESET# = GND, CK_t, CK_c = V_{IL}, DQ = VREF = VDD/2 (i.e. MID-LEVEL)	-	-	TBD	mA
	Static operating current	RESET# = V_{DD}, IBT OFF, Clock inputs not switching (held static LOW), $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, DQ = VREF = VDD/2 (i.e MID-LEVEL)	-	-	TBD	mA
I_{DDD}	Dynamic operating current — input clock only	RESET# = V_{DD}, for Data[a] and DQ inputs, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK_t, CK_c switching at 50% duty cycle. I_O = 0; $V_{DD} = V_{DD}$(max)	-	vs[c]	-	mA/MHz
	Dynamic operating current — per each Data[a] and DQ input	RESET# = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK_t and CK_c switching at 50% duty cycle. One Data[a] and DQ input switching at half clock frequency, 50% duty cycle. I_O = 0; $V_{DD} = V_{DD}$(max)	-	vs[c]	-	mA/MHz

NOTES:
a. DCKE[2:0], DCKE[3]/DODT[1], DODT[0], DA0..DA15, DBA0..DBA2, DRAS_n, DCAS_n, DWE_n, PAR_IN, DCS[7:0]_n are measured while RESET_n pin is pulled LOW.
b. The CK_t and CK_c inputs have internal pull-down resistors in the range of 10KΩ to 100KΩ.
c. Vendor Specific, must be supplied by register vendor for full device description.

7.1.4 Input/Output Capacitance

Table 35 — Capacitance values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_I	Input capacitance, CA and CTRL inputs (with any IBT)	see footnote[a,b]	0.7	-	1.2	pF
C_{CK}	Input capacitance, CK_t, CK_c	see footnote[a]	0.7	-	1.2	pF
C_{IO}	Input/output capacitance	DQ, DQS_t and DQS_c MDQ, MDQS_t and MDQS_c	1.4	-	2.1	pF
C_{DI_CTRL}	Delta capacitance CTRL inputs	C_{DI_CTRL} applies to DCKE[2:0], DCKE[3]/DODT[1], DODT[0] and DCS[7:0]_n	-0.4	-	0.2	pF
$C_{DI_ADD_CMD}$	Delta capacitance CMD/ADDR inputs	$C_{DI_ADD_CMD}$ applies to DA0..DA15, DBA0..DBA2, DRAS_n, DCAS_n, DWE_n	-0.4	-	0.4	pF
C_{DIO}	Delta Input/output capacitance	$C_{DIO}=C_{IO}(DQ) - 0.5*(C_{IO}(DQS_t)+C_{IO}(DQS_c))$ $=C_{IO}(MDQ)\ 0.5*(C_{IO}(MDQS_t)+C_{IO}(MDQS_c))$	-0.5	-	0.3	pF
C_{DDQS}	Delta capacitance within DQS_t/DQS_c or MDQS_t/MDQS_c pair	Absolute value of $C_{IO}(DQS_t)-C_{IO}(DQS_c)$ or $C_{IO}(MDQS_t)-C_{IO}(MDQS_c)$	0	-	0.15	pF
C_{DCK}	Delta capacitance between CK_t, CK_c	Absolute value of $C_{CK_t} - C_{CK_c}$	0	-	0.15	pF
C_{IR}	Input capacitance, RESET_n	$V_I = V_{DD}$ or GND; V_{DD} = 1.5V	-	-	3	pF

NOTES:

a. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147, Procedure for Measuring Input Capacitance Using a Vector Network Analyzer (VNA), with VDD, VSS applied and all other pins floating (except the pin under test, DCKE[2:0], DCKE[3]/DODT[1], RESET_n and ODT[0] as necessary). VDD=1.5V/1.35V, VBIAS=VDD/2 and on-die termination off. The specified values are on die cap only, and not including the package cap

b. Data inputs are DCKE[2:0], DCKE[3]/DODT[1], DODT[0], DA0..DA15, DBA0..DBA2, DRAS_n, DCAS_n, DWE_n, PAR_IN, DCS[7:0]_n.

7.2 AC and DC Input and Output Measurement Levels

7.2.1 Differential swing requirements for clock (CK - CK#) and strobe (DQS - DQS#)

Table 36 — Differential AC and DC Input Levels

Symbol	Parameter	DDR3-800/1066/1333/1600/ 1866/2133		DDR3L-800/1066/1333/1600		Unit	Notes
		Min	Max	Min	Max		
V_{IHdiff}	Differential input high	+ 0.200	note 2	+ 0.180	note 2	V	1
V_{ILdiff}	Differential input logic low	Note 2	- 0.200	Note 2	- 0.180	V	1

NOTE 1 Used to define a differential signal slew-rate.

NOTE 2 These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t and DQS_c need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Figure 23

7.2.2 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured as shown in Table 37 and Figure 18.

Table 37 — Differential Input Slew Rate Definition

Description	Measured		Notes
	from	to	
Differential input slew rate for rising edge (CK_t - CK_c and DQS_t - DQS_c).	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / DeltaTRdiff$
Differential input slew rate for falling edge (CK_t - CK_c and DQS_t - DQS_c).	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / DeltaTFdiff$
NOTE The differential signal (i.e., CK_t - CK_c and DQS_t - DQS_c) must be linear between these thresholds			

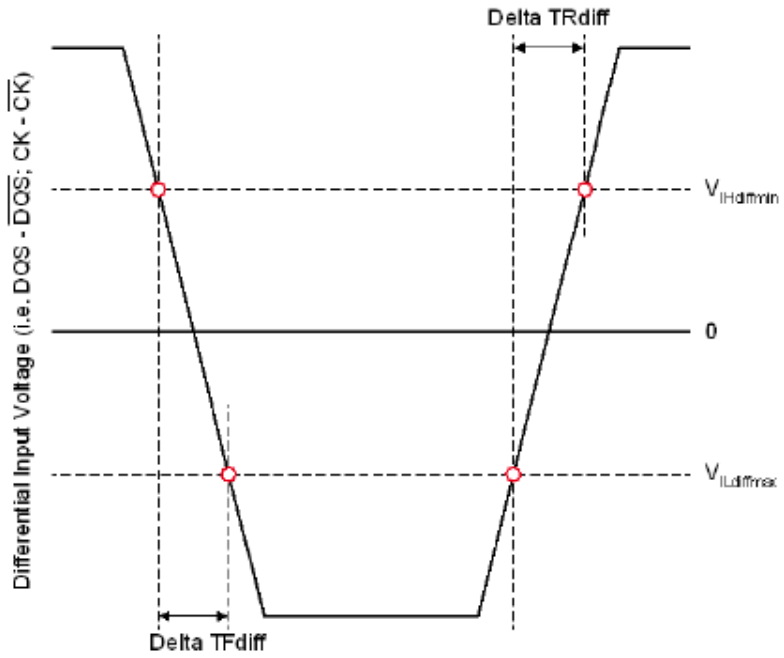


Figure 18 — Differential Input Slew Rate Definition for DQS_t, DQS_c, MDQS_t, MDQS_c and CK_t, CK_c

7.2.3 Single Ended AC and DC Output Levels

Table 38 shows the output levels used for measurements of single ended signals.

Table 38 — Single-ended AC and DC Output Levels

Symbol	Parameter	DDR3/DDR3L-800/1066/1333/ 1600, and DDR3-1866/2133	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	0.8 x V_{DD}	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.5 x V_{DD}	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.2 x V_{DD}	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	V_{TT} + 0.1 x V_{DD}	V	1
$V_{OL(AC)}$	AC output low measurement level (for output SR)	V_{TT} - 0.1 x V_{DD}	V	1
NOTE 1 The swing of ± 0.1 × V_{DD} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DD}/2.				

7.2.4 Differential AC and DC Output Levels

Table 39 shows the output levels used for measurements of differential signals.

Table 39 —Differential AC and DC Output Levels

Symbol	Parameter	DDR3/DDR3L-800/1066/1333/ 1600, and DDR3-1866/2133	Unit	Notes
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	+ 0.2 x V_{DD}	V	1
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	- 0.2 x V_{DD}	V	1
NOTE 1 The swing of ± 0.2 × V_{DD} is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DD}/2 at each of the differential outputs.				

7.2.5 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 40 and Figure 19.

Table 40 —Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTFse
NOTE Output slew rate is verified by design and characterization, and may not be subject to production test.			

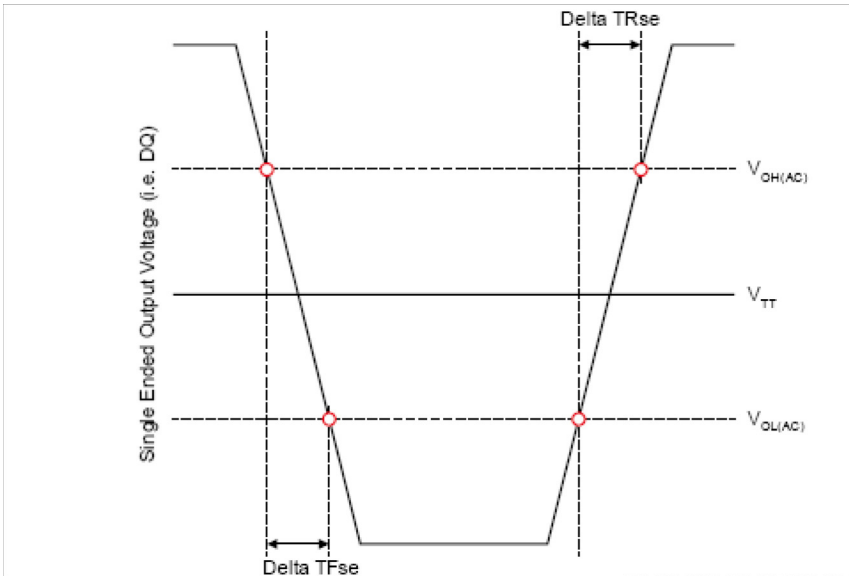


Figure 19 — Single Ended Output Slew Rate Definition

7.2.6 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 41 and Figure 20.

Table 41 — Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]$ / DeltaTRdiff
Differential output slew rate for falling edge	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]$ / DeltaTFdiff
NOTE Output slew rate is verified by design and characterization, and may not be subject to production test.			

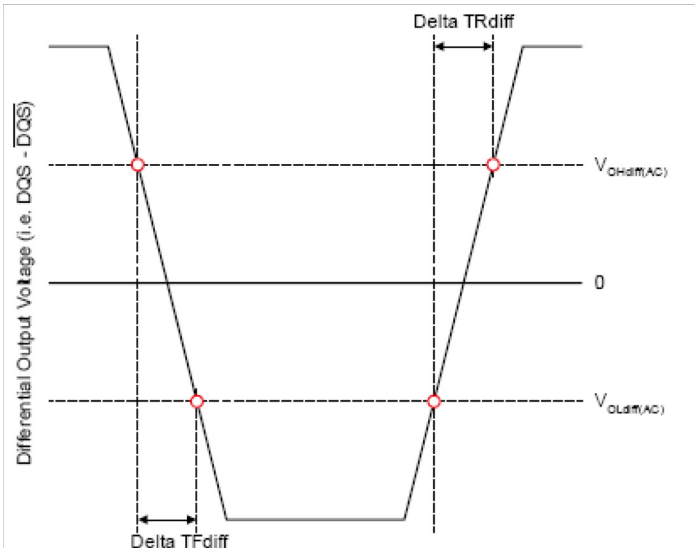


Figure 20 — Differential Output Slew Rate Definition

7.2.7 Reference Load for AC Timing and Output Slew Rate

Figure 21 represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

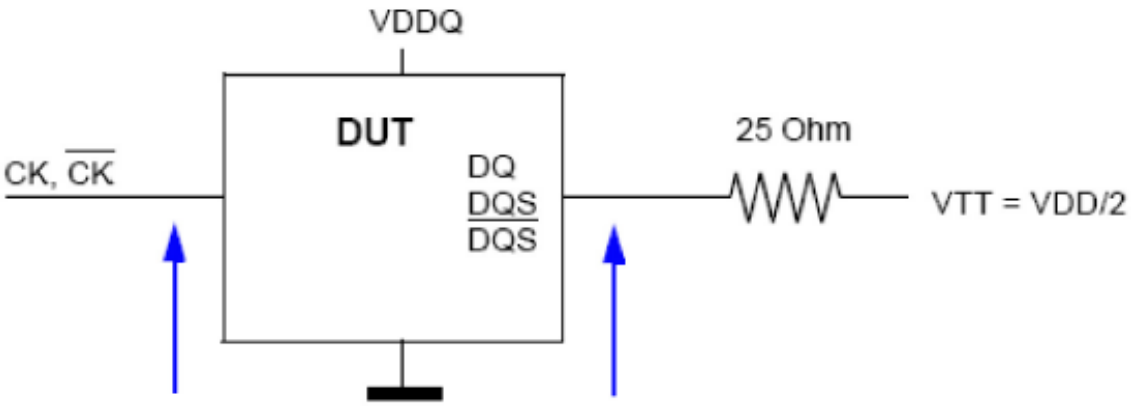


Figure 21 — Reference Load for AC Timing and Output Slew Rate

7.2.8 Overshoot and Undershoot Specifications

7.2.8.1 Address and Control Overshoot and Undershoot Specifications

Table 42 — AC overshoot/undershoot specification for Address, Command and Control pins

	DDR3/3L-800	DDR3/3L-1066	DDR3/3L-1333	DDR3/3L-1600	DDR3-1866	DDR3-2133
Maximum peak amplitude allowed for overshoot area (See Figure 22)	0.4V	0.4V	0.4V	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (See Figure 22)	0.4V	0.4V	0.4V	0.4V	0.4V	0.4V
Maximum overshoot area above VDD (See Figure 22)	0.7V-ns	0.53V-ns	0.42V-ns	0.35V-ns	0.30V-ns	0.26V-ns
Maximum undershoot area below VSS (See Figure 22)	0.7V-ns	0.53V-ns	0.42V-ns	0.35V-ns	0.30V-ns	0.26V-ns
(DA0..DA15, DBA0..DBA2, DRAS_n, DCAS_n, DWE_n, DCS[7:0]_n, DCKE[2:0], DCKE[3]/DODT[1], DODT[0]						

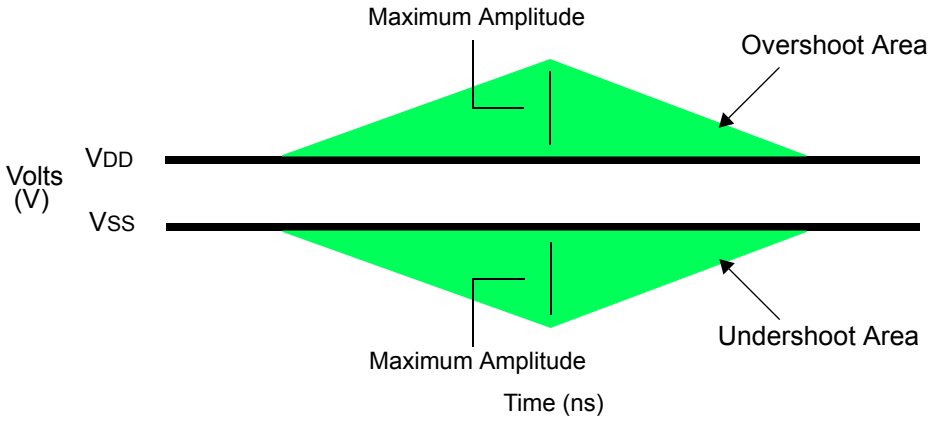


Figure 22 — Address, Command and Control Overshoot and Undershoot definition

7.2.8.2 Clock, Data, and Strobe Overshoot and Undershoot Specifications

Table 43 — AC overshoot/undershoot specification for Clock, Data, and Strobe

	DDR3/3L-800	DDR3/3L-1066	DDR3/3L-1333	DDR3/3L-1600	DDR3-1866	DDR3-2133
Maximum peak amplitude allowed for overshoot area (See Figure 23)	0.4V	0.4V	0.4V	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (See Figure 23)	0.4V	0.4V	0.4V	0.4V	0.4V	0.4V
Maximum overshoot area above VDDQ (See Figure 23)	0.5V-ns	0.38V-ns	0.30V-ns	0.25V-ns	0.21V-ns	0.19V-ns
Maximum undershoot area below VSSQ (See Figure 23)	0.5V-ns	0.38V-ns	0.30V-ns	0.25V-ns	0.21V-ns	0.19V-ns
(CK_t, CK_c, DQ, DQS_t, DQS_c,)						

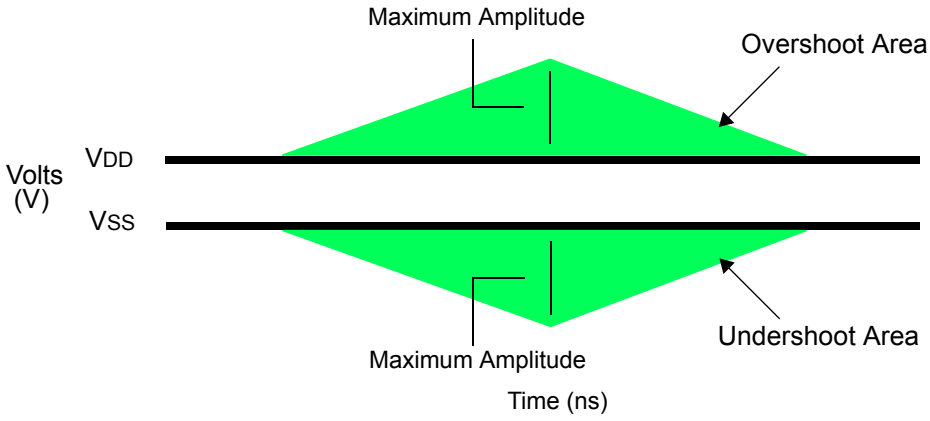


Figure 23 — Clock, Data, and Strobe Overshoot and Undershoot definition

7.3 Host Interface Electrical / Timing Specifications

This section specifies electrical and timing requirement for Memory Buffer Host interface.

7.3.1 CMD/ADDR/CTRL Input Bus Termination Requirement

Table 44 — CMD/ADDR/CTRL Input Bus Termination

Symbol	Parameter	DDR3/DDR3L-800/1066/1333/ 1600, and DDR3-1866/2133			Unit
		Min	Typ	Max	
$IBT_{(300)}$	Termination resistance	270	300	330	Ω
$IBT_{(200)}$	Termination resistance	180	200	220	Ω
$IBT_{(150)}$	Termination resistance	135	150	165	Ω
$IBT_{(100)}$	Termination resistance	90	100	110	Ω
IBT_{TOL}	Termination tolerance[a]	-10	-	+10	%
ΔV_M	Deviation of V_M w.r.t. $V_{DD}/2$[b]	-	-	2.5	%

[a] Apply $V_{IH(AC)}$ to pin under test and measure current $I_{IH(AC)}$, then apply $V_{IL(AC)}$ to pin under test and measure current $I_{IL(AC)}$. $R_{IBT} = (V_{IH(AC)} - V_{IL(AC)})/(I_{IH(AC)} - I_{IL(AC)})$.
[b] Measure voltage ($V_{OUT} = V_M$) at test pin with no load ($I_{OUT} = 0$). $\Delta V_M = |2 * V_M/V_{DD} - 1| * 100\%$.

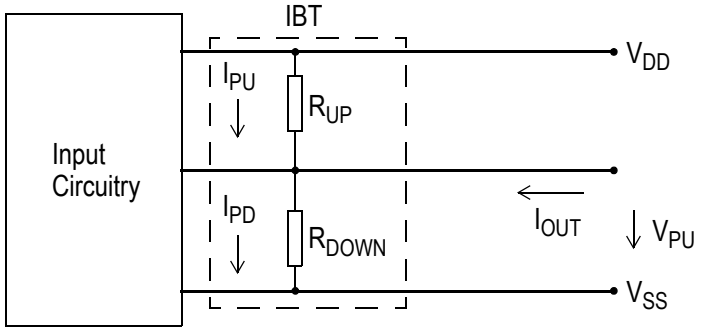


Figure 24 — Input Bus Termination: Definition of Voltages and Currents

7.3.2 DQ/DQS On-Die Termination (ODT) Requirement

Table 45 — DQ/DQS On-Die Termination

Symbol	Parameter	DDR3/DDR3L-800/1066/1333/1600, and DDR3-1866/2133			Unit
		Min	Typ	Max	
$R_{TT(240)}$	Termination resistance (R_{ZQ}) - DDR3	216	240	312	Ω
$R_{TT(120)}$	Termination resistance ($R_{ZQ}/2$) - DDR3	108	120	156	Ω
$R_{TT(80)}$	Termination resistance ($R_{ZQ}/3$) - DDR3	72	80	104	Ω
$R_{TT(60)}$	Termination resistance ($R_{ZQ}/4$) - DDR3	54	60	78	Ω
$R_{TT(40)}$	Termination resistance ($R_{ZQ}/6$) - DDR3	36	40	52	Ω
$R_{TT(30)}$	Termination resistance ($R_{ZQ}/8$) - DDR3	27	30	39	Ω
ODT_{TOL}	Termination tolerance[a] - DDR3	-10	-	+30	%
$R_{TT(240)}$	Termination resistance (R_{ZQ}) - DDR3L	216	240	348	Ω
$R_{TT(120)}$	Termination resistance ($R_{ZQ}/2$) - DDR3L	108	120	174	Ω
$R_{TT(80)}$	Termination resistance ($R_{ZQ}/3$) - DDR3L	72	80	116	Ω
$R_{TT(60)}$	Termination resistance ($R_{ZQ}/4$) - DDR3L	54	60	87	Ω
$R_{TT(40)}$	Termination resistance ($R_{ZQ}/6$) - DDR3L	36	40	58	Ω
$R_{TT(30)}$	Termination resistance ($R_{ZQ}/8$) - DDR3L	27	30	43.5	Ω
ODT_{TOL}	Termination tolerance[a] - DDR3L	-10	-	+45	%
ΔV_M	Deviation of V_M w.r.t. $V_{DD}/2$[b]	-	-	5.0	%

NOTES:

a. Measurement definition for ODT:
Apply $V_{IH(ac)}$ to pin under test and measure current $I(V_{IH(ac)})$, then apply $V_{IL(ac)}$ to pin under test and measure current $I(V_{IL(ac)})$ respectively.

$$ODT = \frac{VIH(ac) - VIL(ac)}{I(VIH(ac)) - I(VIL(ac))}$$

b. Measure voltage ($V_{OUT} = V_M$) at test pin with no load ($I_{OUT} = 0$). $\Delta V_M = |2 * V_M/V_{DD} - 1| * 100\%$.

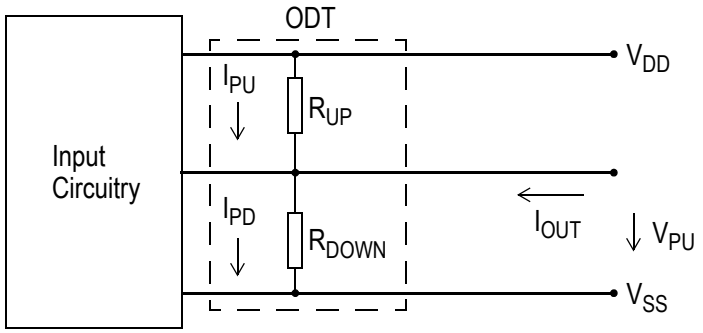


Figure 25 — On-Die Termination: Definition of Voltages and Currents

7.3.3 DQ/DQS Output Driver DC Electrical Characteristics

Table 46 — DQ/DQS Output Driver Impedance RON Requirement

Symbol	Parameter	DDR3/DDR3L-800/1066/1333/1600, and DDR3-1866/2133			Unit
		Min	Typ	Max	
$R_{on(VL)}$	Very Light Drive Impedance[a] $R_{ZQ}/5$	43.2	48	52.8	Ω
$R_{on(L)}$	Light Drive Impedance[a] $R_{ZQ}/6$	36	40	44	Ω
$R_{on(M)}$	Moderate Drive Impedance[a] $R_{ZQ}/7$	30.6	34	37.4	Ω
$R_{on(S)}$	Strong Drive Impedance[a] $R_{ZQ}/9$	24.3	27	29.7	Ω
$R_{on(VS)}$	Very Strong Drive Impedance[a] $R_{ZQ}/12$	18	20	22	Ω
ΔR_{PU-PD}	Mismatch between pull-up and pull-down impedance[b]	-10	-	+10	%
SR_{SE_OUTR}	SE Output Rising edge slew rate (default)[c] - DDR3	2.0	-	5.0	V/ns
	SE Output Rising edge slew rate (default)[c] - DDR3L	1.8	-	4.5	V/ns
SR_{SE_OUTF}	SE Output Falling edge slew rate (default)[c]- DDR3	2.0	-	5.0	V/ns
	SE Output Falling edge slew rate (default)[c]- DDR3L	1.8	-	4.5	V/ns
ΔSR_{SE_OUT}	SE Output Rising-falling edge slew rate difference	-	-	1	V/ns
SR_{DIFF_OUTR}	DIFF Output Rising edge slew rate (default)[d] - DDR3	4.0	-	10	V/ns
	DIFF Output Rising edge slew rate (default)[d]- DDR3L	3.6	-	9	V/ns
SR_{DIFF_OUTF}	DIFF Output Falling edge slew rate (default[d]- DDR3	4.0	-	10	V/ns
	DIFF Output Falling edge slew rate (default[d]- DDR3L	3.6	-	9	V/ns
ΔSR_{DIFF_OUT}	DIFF Output Rising-falling edge slew rate difference	-	-	2	V/ns

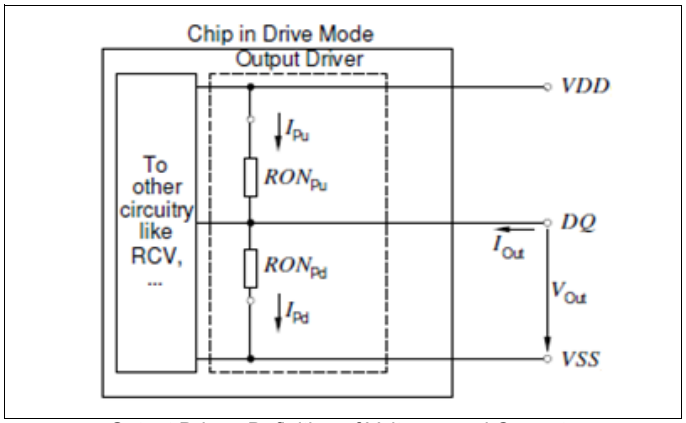
NOTES:

a. RON is defined as small signal output resistance measured at 0.5*VDD. RZQ = 240 Ω. Calibration needs to be performed before measurement are taken.

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{V_{DD} - V_{Out}}{|I_{Out}|}$$ under the condition that RON_{Pd} is turned off (1)

$$RON_{Pd} = \frac{V_{Out}}{|I_{Out}|}$$ under the condition that RON_{Pu} is turned off (2)



Output Driver: Definition of Voltages and Currents

b. is defined as the mismatch between pullup and pulldown impedances: ΔR_{PU-PD}=(RONpu - RONpd) / RON * 100%

c. Single-ended Output pullup and pulldown slew rate is measured into R_{TT} of 25 ohms to V_{TT} (see Figure 21).The slew rate is measured between $V_{OH(AC)}$ and $V_{OL(AC)}$ AC Level (see Table 38 for $V_{OH(AC)}$ and $V_{OL(AC)}$ AC Level definition, and see Table 40 for rising and falling edges measurement details). It is guaranteed for any pattern of data, including all outputs switching and only one output switching.

d. Differential Output pullup and pulldown slew rate is measured into R_{TT} of 25 ohms to V_{TT} (see Figure 21). The slew rate is measured between $V_{OHdiff(AC)}$ and $V_{OLdiff(AC)}$ AC Level (see Table 39 for $V_{OHdiff(AC)}$ and $V_{OLdiff(AC)}$ AC Level definition, and see Table 41 for rising and falling edges measurement details). It is guaranteed for any pattern of data, including all outputs switching and only one output switching.

7.3.4 Host Interface Input Timing and DQ/DQS Output Timing

This section specifies various input timing for command/Address/Control/Clock, DQ/DQS, CA setup and hold, Data setup and hold, initialization, control word write, power-down, write leveling, and RTT.

In addition, it also cover DQ/DQS output timing.

Table 47 — Host Interface Input Timing Parameters

Symbol	Parameter	DDR3/DDR3L-800		DDR3/DDR3L-1066		DDR3/DDR3L-1333		DDR3/DDR3L-1600		DDR3-1866		DDR3-2133		Units Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input Clock Timing														
f_{clock}	Input clock frequency	300	810	300	810	300	810	300	810	300	945	300	1080	MHz
f_{TEST}	Input clock frequency	70	300	70	300	70	300	70	300	70	300	70	300	MHz
t_{CH}/t_{CL}	Pulse duration, CK_t, CK_c HIGH or LOW	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}[a]
Initialization Timing														
t_{INIT}	Duration of reset after stable VDD	200	-	200	-	200	-	200	-	200	-	200	-	µs
t_{ACT}	Time for VREF, DCKEx, DCSx to be stable before RESET_n goes HIGH	8	-	8	-	8	-	8	-	8	-	8	-	t_{CK}[a]
t_{STAB}	PLL lock time (for Application Frequency Only)	6	-	6	-	6	-	6	-	5	-	5	-	µs
t_{QVREF}	QVREFCA/QVREFDQ voltage stable till RESET_n goes HIGH	1	-	1	-	1	-	1	-	1	-	1	-	µs
Control Word and DRAM MRS Write Timing														
t_{MRD}	Control word to control word (or next command) programming delay[b]	16	-	16	-	16	-	16	-	16	-	16	-	t_{CK}[a]
t_{DRAM_MRS}	DRAM MRS to MRS Command programming delay	6	-	6	-	6	-	6	-	6	-	6	-	t_{CK}[a]
Power Down Timing														
t_{InDIS}	Input buffers (except for CK_t/CK_c, DCKEn, DODTn and RESET_n) disable time after DCKE[1:0] is LOW	1	4	1	4	1	4	1	4	1	4	1	4	t_{CK}[a]
t_{QDIS}	Output buffers (except for Yn_t/Yn_c, QxCKEn, QxODTn) hi-z after QxCKEn is driven LOW	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	t_{CK}[a]
t_{CKoff}	Number of tCK required for both DCKE0 and DCKE1 to remain LOW before both CK_t/CK_c are driven LOW	5	-	5	-	5	-	5	-	5	-	5	-	t_{CK}[a]
t_{CKEV}	Input buffers (DCKE0 and DCKE1) disable time after CK_t/CK_c = LOW	2	-	2	-	2	-	2	-	2	-	2	-	t_{CK}[a]

Table 47 — Host Interface Input Timing Parameters (Continued)

Symbol	Parameter	DDR3/DDR3L-800		DDR3/DDR3L-1066		DDR3/DDR3L-1333		DDR3/DDR3L-1600		DDR3-1866		DDR3-2133		Units Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{Fixedoutput}$	Static register output after DCKE0 or DCKE1 is HIGH at the input (exit from Power saving state)	1	3	1	3	1	3	1	4	1	4	1	5	t_{CK}[a]
CMD/ADDR/CTL Inputs Timing														
tIS (AC100)	Setup time[c,d,e] (DDR3)	100	-	100	-	100	-	100	-	80	-	70	-	ps
tIH (DC100)	Hold time[f,d,e] (DDR3)	100	-	100	-	100	-	100	-	80	-	70	-	ps
tIS (AC90)	Setup time[c,d,e] (DDR3L)	110	-	110	-	110	-	110	-	90	-	80	-	ps
tIH (DC90)	Hold time[f,d,e] (DDR3L)	110	-	110	-	110	-	110	-	90	-	80	-	ps
ODTH4	DODTn high time without write command or with write command and BC4	4	-	4	-	4	-	4	-	4	-	4	-	t_{CK}[a]
ODTH8	DODTn high time without write command or with write command and BL8	6	-	6	-	6	-	6	-	6	-	6	-	t_{CK}[a]
DQ Inputs Timing														
tDS (AC100)	Setup time[g,h,i] (DDR3)	45	-	45	-	30	-	30	-	TBD	-	TBD	-	ps
tDH (DC100)	Hold time [h,i,j] (DDR3)	45	-	45	-	30	-	30	-	TBD	-	TBD	-	ps
tDS (AC90)	Setup time[h,g,i] (DDR3L)	55	-	55	-	40	-	40	-	TBD	-	TBD	-	ps
tDH (DC90)	Hold time[h,i,j] (DDR3L)	55	-	55	-	40	-	40	-	TBD	-	TBD	-	ps
Data Strobe (DQS) Inputs Timing														
tWPRE	DQS_t, DQS_c differential WRITE Preamble	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	t_{CK}[a]
tWPST	DQS_t, DQS_c differential WRITE Postamble	0.3	-	0.3	-	0.3	-	0.3	-	0.3	-	0.3	-	t_{CK}[a]
tDQSL	DQS_t, DQS_c differential input low pulse width	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}[a]
tDQSH	DQS_t, DQS_c differential input high pulse width	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}[a]
tDQSS	DQS_t, DQS_c rising edge to CK, CK# rising edge[k]	-0.25	0.25	-0.25	0.25	-0.25	0.25	-0.27	0.27	-0.27	0.27	-0.27	0.27	t_{CK}[a]
tDSS	DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge[k]	0.2	-	0.2	-	0.2	-	0.18	-	0.18	-	0.18	-	t_{CK}[a]
tDSH	DQS_t, DQS_c falling edge hold time to CK_t, CK_c rising edge[k]	0.2	-	0.2	-	0.2	-	0.18	-	0.18	-	0.18	-	t_{CK}[a]
Write Leveling Inputs Timing														
tWLMRD	First DQS_t, DQS_c rising edge after write leveling mode is programmed	40	-	40	-	40	-	40	-	40	-	40	-	nCK
tWLDQSEN	DQS_t, DQS_c delay after write leveling mode is programmed	25	-	25	-	25	-	25	-	25	-	25	-	nCK
tWLS	Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t, DQS_c crossing	325	-	245	-	195	-	165	-	140	-	125	-	ps

Table 47 — Host Interface Input Timing Parameters (Continued)

Symbol	Parameter	DDR3/DDR3L-800		DDR3/DDR3L-1066		DDR3/DDR3L-1333		DDR3/DDR3L-1600		DDR3-1866		DDR3-2133		Units Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tWLH	Write leveling hold time from rising CK_t, CK_c crossing to rising DQS_t, DQS_c crossing	325	-	245	-	195	-	165	-	140	-	125	-	ps
RTT Inputs Timing														
tAON	RTT turn-on	-400	400	-300	300	-250	250	-225	225	-195	195	-180	180	ps
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	t_{CK}[a]
tADC	RTT dynamic change skew	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	t_{CK}[a]

NOTES:

a. Clock cycle time.

b. The minimum spacing between MRS commands and any other command to the same physical rank must be at least 16 DRAM clock cycle.

c. Setup (t_{IS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and first crossing of $V_{IH(ac)}$min. Setup (t_{IS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max (see Figure). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to $V_{REF(dc)}$ level is used for derating value (see Figure 42).

d. Setup (t_{IS}) and Hold (t_{IH}): ac/dc referenced to 1V/ns Address/Command slew rate and 2V/ns differential CK_t/CK_c slew rate.

e. These parameters are measured from a command/control/address input signal (DCKE[1:0], DODT[1:0], DCS_n[7:0], DRAS_n, DCAS_n, DWE_n, DBA[2:0], DA[15:0]) transition edge to the rising differential input clock CK_t/CK_c crossing. For the case without induced jitter, a small amount jitter will be present in the input clock source depending on the manufacturer of the source equipment. The input clock source jitter distribution should be characterized prior to any measurement of the device. For the case of inducing jitter in the input clock signal source, a Gaussian jitter distribution should be used that does not exceed the PLL bandwidth of the device under test. The measurement for both cases is taken from the transition edge of command/control/address
signal to the mean of the input jitter distribution on the rising differential input CK_t/CK_c crossing. And, these parameters should be met whether clock jitter is present or not.

f. Hold (t_{IH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)max}$ and the first crossing of $V_{REF(dc)}$. Hold (t_{IH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)min}$ and the first crossing of $V_{REF(dc)}$ (see Figure 41). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region' use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 43).

g. Setup (t_{DS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and first crossing of $V_{IH(ac)}$min. Setup (t_{DS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (see Figure 44). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to $V_{REF(dc)}$ level is used for derating value (see Figure 46).

h. Setup (t_{DS}) and Hold (t_{DH}): ac/dc referenced to 1V/ns DQ slew rate and 2V/ns differential DQS_t/DQS_c slew rate.

i. These parameters are measured from a data signal (DQ) transition edge to its respective data strobe (DQS_t, DQS_c) crossing. The specification values must be met with clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the DQS_t, DQS_c signals crossing. That is, these parameters should be met whether clock jitter is present or not.

j. Hold (t_{DH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)max}$ and the first crossing of $V_{REF(dc)}$. Hold (t_{DH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)min}$ and the first crossing of $V_{REF(dc)}$ (see Figure 45). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region' use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 47).

k. These parameters are measured from any DQS_t/DQS_c crossing to the CK_t/CK_c crossing. For the case without induced jitter, a small amount jitter will be present in the input clock source depending on the manufacturer of the source equipment. The input clock source jitter distribution should be characterized prior to any measurement of the device. For the case of inducing jitter in the input clock signal source, a Gaussian jitter distribution should be used that does not exceed the PLL bandwidth of the device under test. The measurement for both cases is taken from the DQS_t/DQS_c crossing to the mean of the input jitter distribution on the rising differential input CK_t/CK_c crossing, and these parameters should be met whether clock jitter is present or not.

Table 48 — Host Interface DQ/DQS Output Timing Parameters

Symbol	Parameter	DDR3/DDR3L-800		DDR3/DDR3L-1066		DDR3/DDR3L-1333		DDR3/DDR3L-1600		DDR3-1866		DDR3-2133		Units Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
DQ Output Timing														
tDQSQ	DQS_t, DQS_c to DQ skew, per byte group, per access[a,b]	-	150	-	125	-	100	-	85	-	75	-	60	ps
tQH	DQ output hold time from DQS_t, DQS_c[b]	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	t_{CK}[c]
Write Leveling Output Timing														
tWLO	Write leveling output delay	0	7.5	0	7.5	0	7.5	0	7.5	0	7.5	0	7.5	ns
tWLOE	Write leveling output error	0	2	0	2	0	2	0	2	0	2	0	2	ns
Data Strobe (DQS) Output Timing														
tRPRE	DQS_t, DQS_c differential READ Preamble[d]	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	t_{CK}[c]
tRPST	DQS_t, DQS_c differential READ Postamble[d]	0.3	-	0.3	-	0.3	-	0.3	-	0.3	-	0.3	-	t_{CK}[c]
tQSH	DQS_t, DQS_c differential output high time[d]	0.46	-	0.46	-	0.46	-	0.46	-	0.46	-	0.46	-	t_{CK}[c]
tQSL	DQS_t, DQS_c differential output low time[d]	0.46	-	0.46	-	0.46	-	0.46	-	0.46	-	0.46	-	t_{CK}[c]

NOTES:
a. This skew represents the absolute output skew and contains the pad skew and package skew.
b. The specification values are NOT affected by the amount of clock jitter applied.
c. Clock cycle time.
d. The specification values are affected by the amount of clock jitter applied (i.e., tJIT(per), tJIT(cc), etc.), as MB outputs use PLL outputs. However, these parameters must be met whether clock jitter is present or not.

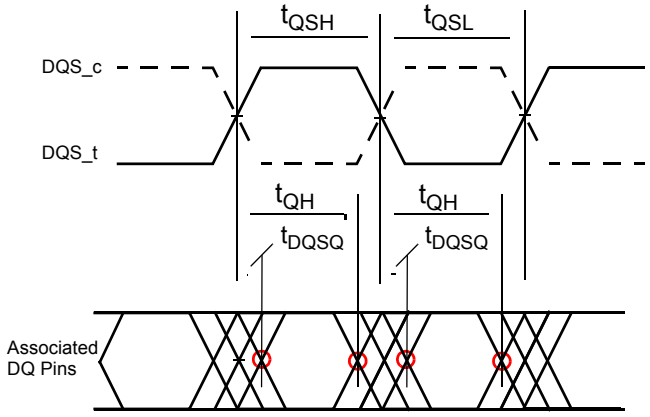


Figure 26 — Read Timing Definition

7.4 DRAM Interface Electrical / Timing Specifications

This section specifies electrical and timing requirement for Memory Buffer DRAM interface.

7.4.1 MDQ/MDQS On-Die Termination (MODT) Requirement

Table 49 — MDQ/MDQS On-Die Termination (MODT) for READ Operation

Symbol	Parameter	DDR3/DDR3L-800/1066/1333/1600, and DDR3-1866/2133			Unit
		Min	Typ	Max	
$R_{TT(240)}$	Termination resistance (R_{ZQ}) - DDR3	216	240	312	Ω
$R_{TT(120)}$	Termination resistance ($R_{ZQ}/2$) - DDR3	108	120	156	Ω
$R_{TT(80)}$	Termination resistance ($R_{ZQ}/3$) - DDR3	72	80	104	Ω
$R_{TT(60)}$	Termination resistance ($R_{ZQ}/4$) - DDR3	54	60	78	Ω
$R_{TT(40)}$	Termination resistance ($R_{ZQ}/6$) - DDR3	36	40	52	Ω
$R_{TT(30)}$	Termination resistance ($R_{ZQ}/8$) - DDR3	27	30	39	Ω
$MODT_{TOL}$	Termination tolerance[a] - DDR3	-10	-	+30	%
$R_{TT(240)}$	Termination resistance (R_{ZQ}) - DDR3L	216	240	348	Ω
$R_{TT(120)}$	Termination resistance ($R_{ZQ}/2$) - DDR3L	108	120	174	Ω
$R_{TT(80)}$	Termination resistance ($R_{ZQ}/3$) - DDR3L	72	80	116	Ω
$R_{TT(60)}$	Termination resistance ($R_{ZQ}/4$) - DDR3L	54	60	87	Ω
$R_{TT(40)}$	Termination resistance ($R_{ZQ}/6$) - DDR3L	36	40	58	Ω
$R_{TT(30)}$	Termination resistance ($R_{ZQ}/8$) - DDR3L	27	30	43.5	Ω
$MODT_{TOL}$	Termination tolerance[a] - DDR3L	-10	-	+45	%
ΔV_M	Deviation of V_M w.r.t. $V_{DD}/2$[b]	-	-	5.0	%

NOTES:

a. Measurement definition for MODT:
Apply $V_{IH(ac)}$ to pin under test and measure current $I(V_{IH(ac)})$, then apply $V_{IL(ac)}$ to pin under test and measure current $I(V_{IL(ac)})$ respectively.

$$MODT = \frac{VIH(ac) - VIL(ac)}{I(VIH(ac)) - I(VIL(ac))}$$

b. Measure voltage ($V_{OUT} = V_M$) at test pin with no load ($I_{OUT} = 0$). $\Delta V_M = |2 * V_M/V_{DD} - 1| * 100\%$.

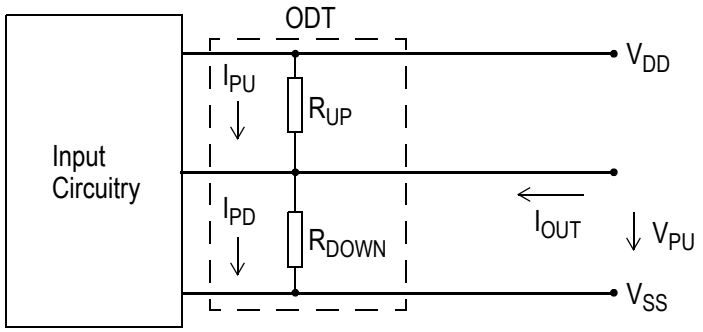


Figure 27 — On-Die Termination: Definition of Voltages and Currents

7.4.2 QCMD/QADDR/QCTRL/Yn_t/Yn_c DC and AC Output Parameters

Table 50 — QCMD/QADDR/QCTRL/Yn_t/Yn_c Ron and Output Slew Rate

Symbol	Parameter	DDR3/DDR3L-800/1066/1333/1600, and DDR3-1866/2133			Unit
		Min	Typ	Max	
QCMD/QADDR/QCTRL/Yn_t/Yn_c					
$R_{on(L)}$	Light Drive Impedance[a]	22	26	30	Ω
$R_{on(M)}$	Moderate Drive Impedance[a]	16	19	22	Ω
$R_{on(S)}$	Strong Drive Impedance[a]	12	14	16	Ω
$R_{on(W)}$	Weak Drive Impedance[a,b]	70	-	100	Ω
ΔR_{PU-PD}	Mismatch between pull-up and pull-down impedance[c]	-10	-	+10	%
SR_{SE_OUTR}	SE Output Rising edge slew rate (default)[d] - DDR3	2.0	-	5.0	V/ns
	SE Output Rising edge slew rate (default)[d] - DDR3L	1.8	-	5.0	V/ns
SR_{SE_OUTF}	SE Output Falling edge slew rate (default)[d] - DDR3	2.0	-	5.0	V/ns
	SE Output Falling edge slew rate (default[d] - DDR3L	1.8	-	5.0	V/ns
ΔSR_{SE_OUT}	SE Output Rising-falling edge slew rate difference	-	-	1	V/ns

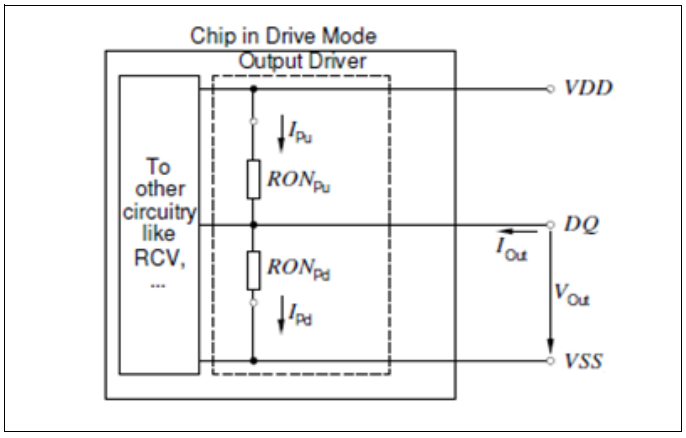
NOTES:

a. RON is defined as small signal output resistance measured at 0.5*VDD.

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{V_{DD} - V_{Out}}{|I_{Out}|}$$ under the condition that RON_{Pd} is turned off (1)

$$RON_{Pd} = \frac{V_{Out}}{|I_{Out}|}$$ under the condition that RON_{Pu} is turned off (2)

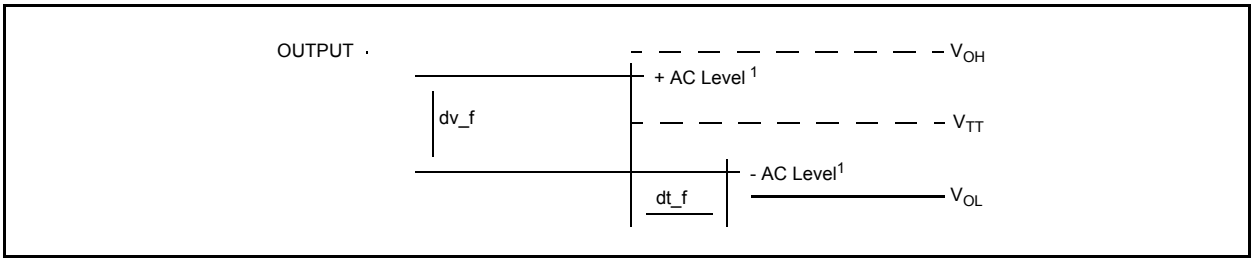


Output Driver: Definition of Voltages and Currents

b. Output weak drive refers to allowing many A/B outputs to enter a state of higher output impedance when they are not being used. This is to conserve power when the outputs are resistively terminated to a voltage (e.g., VTT).

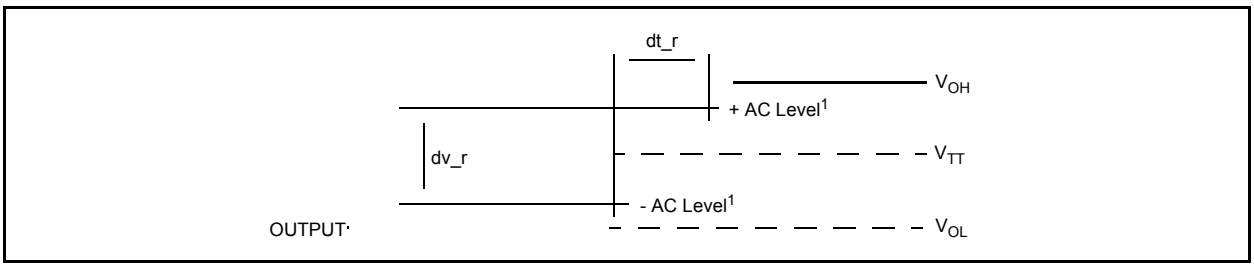
c. is defined as the mismatch between pullup and pulldown impedances: ΔR_{PU-PD}=(RONpu - RONpd) / RON * 100%

d. Output pullup and pulldown slew rate is measured into R_{TT} of 50 ohms to V_{TT}. The slew rate is measured between V_{TT} ± AC Level (see Figure and Figure 29) for rising and falling edges. It is guaranteed for any pattern of data, including all outputs switching and only one output switching.



NOTE 1 See Table 51, “AC level for Slew Rate Measurement” for AC Level value.

Figure 28 — Voltage waveforms, HIGH-to-LOW slew rate measurement



NOTE 1 See Table 51, “AC level for Slew Rate Measurement” for AC Level value.

Figure 29 — Voltage waveforms, LOW-to-HIGH slew rate measurement

Table 51 — AC level for Slew Rate Measurement

	DDR3/DDR3L-800/1066/1333/ 1600	DDR3-1866/2133
AC Level (1.5V)	150 mV	135 mV
AC Level (1.35V)	135 mV	TBD

7.4.3 MDQ/MDQS DC and AC Output Parameters

Table 52 — MDQ/MDQS Ron Requirement (for DRAM Interface WRITE Operation)

Symbol	Parameter	DDR3/DDR3L-800/1066/1333/1600, and DDR3-1866/2133			Unit
		Min	Typ	Max	
MDQ/MDQS					
$R_{on(VL)}$	Very Light Drive Impedance[a] $R_{ZQ}/5$	43.2	48	52.8	Ω
$R_{on(L)}$	Light Drive Impedance[a] $R_{ZQ}/6$	36	40	44	Ω
$R_{on(M)}$	Moderate Drive Impedance[a] $R_{ZQ}/7$	30.6	34	37.4	Ω
$R_{on(S)}$	Strong Drive Impedance[a] $R_{ZQ}/9$	24.3	27	29.7	Ω
$R_{on(VS)}$	Very Strong Drive Impedance[a] $R_{ZQ}/12$	18	20	22	Ω
ΔR_{PU-PD}	Mismatch between pull-up and pull-down impedance[b]	-10	-	+10	%
SR_{SE_OUTR}	SE Output Rising edge slew rate (default)[c] - DDR3	2.0	-	5.0	V/ns
	SE Output Rising edge slew rate (default)[c] - DDR3L	1.8	-	4.5	V/ns
SR_{SE_OUTF}	SE Output Falling edge slew rate (default)[c] - DDR3	2.0	-	5.0	V/ns
	SE Output Falling edge slew rate (default)[c] - DDR3L	1.8	-	4.5	V/ns
ΔSR_{SE_OUT}	SE Output Rising-falling edge slew rate difference	-	-	1	V/ns
SR_{DIFF_OUTR}	DIFF Output Rising edge slew rate (default)[d] - DDR3	4.0	-	10	V/ns
	DIFF Output Rising edge slew rate (default)[d] - DDR3L	3.6	-	9	V/ns
SR_{DIFF_OUTF}	DIFF Output Falling edge slew rate (default[d] - DDR3	4.0	-	10	V/ns
	DIFF Output Falling edge slew rate (default[d] - DDR3L	3.6	-	9	V/ns
ΔSR_{DIFF_OUT}	DIFF Output Rising-falling edge slew rate difference	-	-	2	V/ns

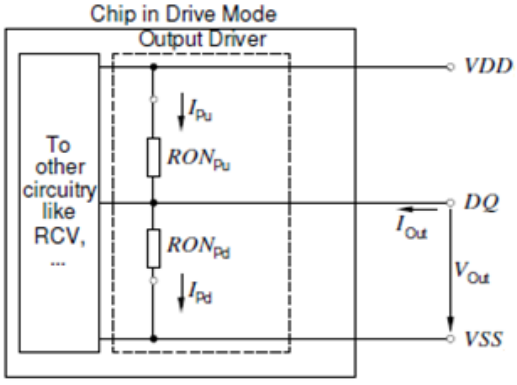
NOTES:

a. RON is defined as small signal output resistance measured at 0.5*VDD. RZQ = 240 Ω

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{V_{DD} - V_{Out}}{|I_{Out}|}$$ under the condition that RON_{Pd} is turned off (1)

$$RON_{Pd} = \frac{V_{Out}}{|I_{Out}|}$$ under the condition that RON_{Pu} is turned off (2)



Output Driver: Definition of Voltages and Currents

b. is defined as the mismatch between pullup and pulldown impedances: ΔR_{PU-PD}=(RONpu - RONpd) / RON * 100%

c. Single-ended Output pullup and pulldown slew rate is measured into R_{TT} of 25 ohms to V_{TT} (see Figure 21). The slew rate is measured between $V_{OH(AC)}$ and $V_{OL(AC)}$ AC Level (see Table 38 for $V_{OH(AC)}$ and $V_{OL(AC)}$ AC Level definition, and see Table 40 for rising and falling edges measurement details). It is guaranteed for any pattern of data, including all outputs switching and only one output switching.

d. Differential Output pullup and pulldown slew rate is measured into R_{TT} of 25 ohms to V_{TT} (see Figure 21). The slew rate is measured between $V_{OHdiff(AC)}$ and $V_{OLdiff(AC)}$ AC Level (see Table 39 for $V_{OHdiff(AC)}$ and $V_{OLdiff(AC)}$ AC Level definition, and see Table 41 for rising and falling edges measurement details). It is guaranteed for any pattern of data, including all outputs switching and only one output switching.

7.4.4 DRAM Interface Input and Output Timing

This section specifies various input and output timing for DRAM interface.

Table 53 — DRAM Interface MDQ/MDQS Input Timing Parameters

Symbol	Parameter	DDR3/DDR3L-800		DDR3/DDR3L-1066		DDR3/DDR3L-1333		DDR3/DDR3L-1600		DDR3-1866		DDR3-2133		Units Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
MDQ Inputs Timing														
tDS (AC100)	Setup time[a,b] (DDR3)	45 - tCK/4	-	45 - tCK/4	-	30 - tCK/4	-	30 - tCK/4	-	TBD	-	TBD	-	ps
tDH (DC100)	Hold time[c,b] (DDR3)	45 + tCK/4	-	45 + tCK/4	-	30 + tCK/4	-	30 + tCK/4	-	TBD	-	TBD	-	ps
tDS (AC90)	Setup time[a,b] (DDR3L)	55 - tCK/4	-	55 - tCK/4	-	40 - tCK/4	-	40 - tCK/4	-	TBD	-	TBD	-	ps
tDH (DC90)	Hold time[c,b] (DDR3L)	55 + tCK/4	-	55 + tCK/4	-	40 + tCK/4	-	40 + tCK/4	-	TBD	-	TBD	-	ps
Data Strobe (MDQS) Input Timing														
tRPRE	MDQS_t, MDQS_c differential READ Preamble	0.89	-	0.89	-	0.89	-	0.89	-	0.89	-	0.89	-	t_{CK}[d]
tRPST	MDQS_t, MDQS_c differential READ Postamble	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	t_{CK}[d]
tDQSL	MDQS_t, MDQS_c differential input low pulse width	0.36	0.64	0.36	0.64	0.37	0.63	0.37	0.63	TBD	TBD	TBD	TBD	t_{CK}[d]
tDQSH	MDQS_t, MDQS_c differential input high pulse width	0.36	0.64	0.36	0.64	0.37	0.63	0.37	0.63	TBD	TBD	TBD	TBD	t_{CK}[d]

NOTES:

a. Setup (t_{DS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and first crossing of $V_{IH(ac)}$min. Setup (t_{DS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (see Figure 44). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to $V_{REF(dc)}$ level is used for derating value (see Figure 46).

b. Setup (t_{DS}) and Hold (t_{DH}): ac/dc referenced to 1V/ns DQ slew rate and 2V/ns differential DQS_t/DQS_c slew rate.

c. Hold (t_{DH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)max}$ and the first crossing of $V_{REF(dc)}$. Hold (t_{DH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)min}$ and the first crossing of $V_{REF(dc)}$ (see Figure 45). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region' use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 47).

d. Clock cycle time

7.4.4 DRAM Interface Input and Output Timing (cont'd)

Table 54 — Output timing requirements[a]

Symbol	Parameter	Conditions	DDR3/DDR3L-800/1066/1333/1600, and DDR3-1866/2133		Unit
			Min	Max	
t_{PDM}[a]	Addr/CMD/Ctrl Propagation Delay (1.5V Operation)	Addr/CMD/Ctrl output CK_t/CK_ct[b]	2.2	2.9	ns
	Addr/CMD/Ctrl Propagation Delay (1.35V Operation)		2.2	3.4	ns
$t_{PDMMDQS}$[c]	MDQS to DQS Propagation Delay (1.5V Operation)	MDQS output to DQS[d,e,f,g]	1.8 + tCK/4	2.5 + tCK/4	ns
	MDQS to DQS Propagation Delay (1.35V Operation)		1.8 + tCK/4	2.9 + tCK/4	ns
t_{DIS}	Output disable time (1/2-Clock pre-launch)	Yn_t/Yn_c to output float[h]	0.5 tCK + tQSK1(min)	-	ps
t_{EN}	Output enable time (1/2-Clock pre-launch)	Output driving to Yn_t/ Yn_c[i]	0.5 tCK - tQSK1(max)	-	ps

NOTES:

a. t_{PDM} range (t_{PDM_max} - t_{PDM_min}) must remain as 350ps. For example, if t_{PDM_min} for a device is 2.2ns, it's t_{PDM_max} cannot be more than 2.55ns. If t_{PDM_max} for a device is 3.4ns, it's t_{PDM_min} cannot be less than 3.05ns.

b. See Figure 30.

c. $t_{PDMMDQS}$ range ($t_{PDMMDQS_max}$ - $t_{PDMMDQS_min}$) must remain as 350ps. For example, if $t_{PDMMDQS_min}$ for a device is 1.8 + tCK/4 ns, it's $t_{PDMMDQS_max}$ cannot be more than 2.15 + tCK/4 ns. If $t_{PDMMDQS_max}$ for a device is 2.9 + tCK/4 ns, it's t_{PDM_min} cannot be less than 2.55 + tCK/4 ns.

d. See Figure 31.

e. Minimum latency mode. Per byte, per access.

f. DQ signals are perfectly edge aligned at the input and at the output for ATE measurement.

g. No MDQS jitter at the input of the MB on DRAM interface.

h. See Figure 51.

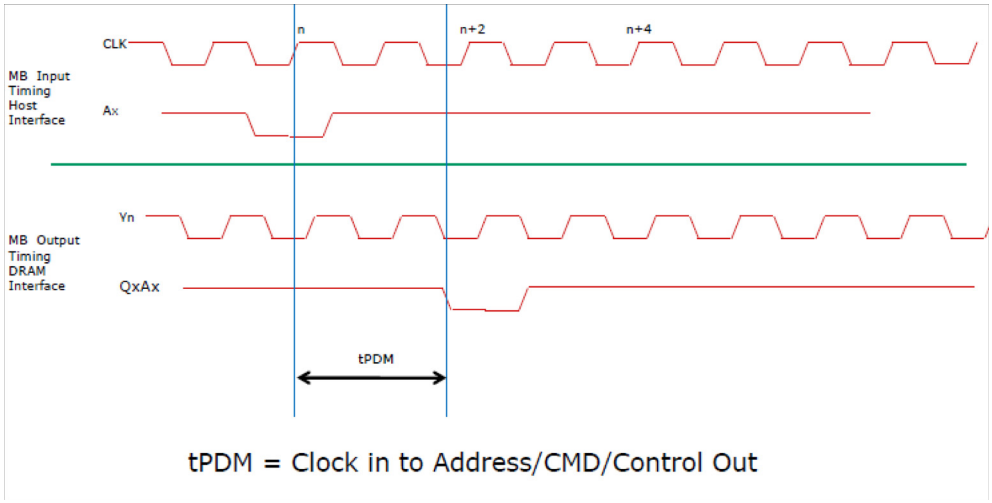


Figure 30 — tPDM Latency Measurement

7.4.4 DRAM Interface Input and Output Timing (cont'd)

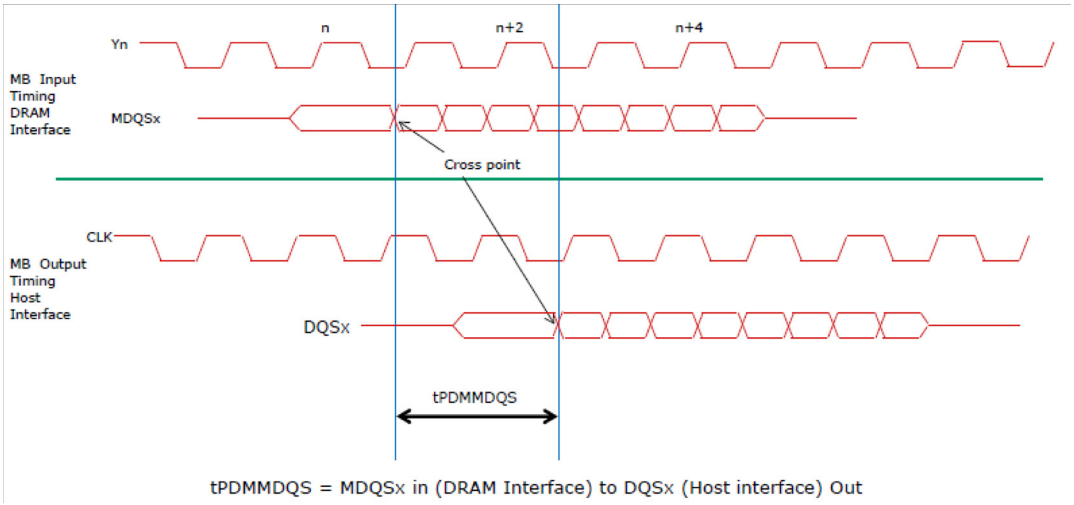


Figure 31 — tPDMMDQS Latency Measurement

7.4.4 DRAM Interface Input and Output Timing (cont'd)

Table 55 — DRAM Interface Output Timing Parameters

Symbol	Parameter	Conditions	DDR3/ DDR3L-800		DDR3/ DDR3L-1066		DDR3/ DDR3L-1333		DDR3/ DDR3L-1600		DDR3-1866		DDR3-2133		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Yn_t, Yn_c Output Clock Timing															
$t_{JIT}(cc)$	Cycle to Cycle Period Jitter		0	112	0	112	0	112	0	96	0	80	0	64	ps
t_{fdyn}	Dynamic phase offset		-50	50	-50	50	-50	50	-40	40	-30	30	-25	25	ps
t_{CKsk}	Fractional Clock Output skew[a]		-	15	-	15	-	15	-	10	-	10	-	10	ps
$t_{JIT}(per)$	Yn Clock Period jitter		- 56	56	- 56	56	- 56	56	- 48	48	- 40	40	- 32	32	ps
$t_{JIT}(hper)$	Half period jitter		- 66	66	- 66	66	- 66	66	- 58	58	- 50	50	- 42	42	ps
$t_{PWH/PWL}$	Yn pulse width HIGH/LOW duration[b]	tPW = 1/2tCK - $\|t_{jit}(hper)min\|$ to 1/2 tCK + $\|t_{jit}(hper)max\|$	1.200	1.300	0.888	0.988	0.700	0.800	0.585	0.665	0.501	0.571	0.439	0.499	ns
t_{QSK1}[c]	Qn Output to Yn clock tolerance (Standard 1/2 Clock Pre-Launch)	Output Inversion enabled	-150	250	-150	250	-150	250	-140	140	-135	125	-130	120	ps
		Output Inversion disabled	-150	350	-150	350	-150	350	-140	240	-135	225	-130	210	
tstaoff[d]	Average delay through the register between the input clock and output clock5.(1.5V Operation)	Standard 1/2 Clock Pre-Launch tstaoff = tPDM + 1/2 tCK	3.45	4.15	3.14	3.84	2.95	3.65	2.83	3.53	2.74	3.44	2.67	3.37	ns
	Average delay through the register between the input clock and output clock5.(1.35V Operation)		3.45	4.65	3.14	4.34	2.95	4.15	2.83	4.03	2.74	3.94	2.67	3.87	ns
MDQ Output Timing															
tDVB[e]	Data valid before MDQS		475	-	344	-	275	-	228	-	193	-	174	-	ps
tDVA[e]	Data valid after MDQS		475	-	344	-	275	-	228	-	193	-	174	-	ps
Data Strobe (MDQS) Output Timing															
tWPRE	MDQS_t, MDQS_c differential WRITE Preamble		0.95	-	0.95	-	0.95	-	0.95	-	0.95	-	0.95	-	t_{CK}[f]
tWPST	MDQS_t, MDQS_c differential WRITE Postamble		0.33	-	0.33	-	0.33	-	0.33	-	0.33	-	0.33	-	t_{CK}[f]
tQSL	MDQS_t, MDQS_c differential output low time		0.46	-	0.46	-	0.46	-	0.46	-	0.46	-	0.46	-	t_{CK}[gf]

Table 55 — DRAM Interface Output Timing Parameters (Continued)

Symbol	Parameter	Conditions	DDR3/ DDR3L-800		DDR3/ DDR3L-1066		DDR3/ DDR3L-1333		DDR3/ DDR3L-1600		DDR3-1866		DDR3-2133		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tQSH	MDQS_t, MDQS_c differential output high time		0.46	-	0.46	-	0.46	-	0.46	-	0.46	-	0.46	-	t_{CK}[f]

NOTES:

a. This skew represents the absolute output clock skew and contains the pad skew and package skew (See Table 38, “Clock Output (Yn) Skew”). This parameter is specified for the clock pairs on each side of the DDR3 Memory Buffer independently. The skew is applicable to right side clock pairs between Y0/Y0# and Y2/Y2#, as well as left side of the clock pairs between Y1/Y1# and Y3/Y3#. This is not a tested parameter and has to be considered as a design goal only.

b. This parameter is a measure of the output clock pulse width HIGH/LOW. The output clock duty cycle can be calculated based on tPW. For frequency that is not part of standard speed bin, tPWH/tPWL should be calculated base on the actual tCK value used (i.e. use formula in the “Condition” column).

c. This skew represents the cumulative of instantaneous Qn skew compared to the output clock (Yn), and contains the Memory Buffer (MB) pad skew, clock skew, package routing skew and the output clock jitter (See Figure 39, “Qn Output Skew for Standard 1/2-Clock Pre-Launch”). This parameter applies to each side of the MB independently. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late. For outputs QxA0.. QxA15, QxBA0 .. QxBA2, QxRAS_n, QxCAS_n, QxWE_n, QACS[3:0]_n/QCS[3:0]_n, QBCS[3:0]_n/QCS[7:4]_n, QxCKE[3:0], QxODT[1:0] this parameter applies to each side of the MB independently. The parameter is measured per JEPXX-XX (procedure defined by Validation TG).

d. This parameter measures the delay from the rising differential input clock which samples incoming CA to the rising differential output clock that will be used to sample the same CA data. tstaoff may not exceed the limits set by tstaoff(min) and tstaoff(max). See Figure 37, “Definition for tstaoff”

e. See Figure 32, “tDVA and tDVB Timing Diagram”. The timing parameters tDVA and tDVB indicate the time the MDQ is valid after or before MDQS. tDVA is used to indicate the time that Data is Valid After. tDVA is used for MDQ/MDQS write hold calculations (tDH). tDVB is used to indicate the time that Data is Valid Before. tDVB is used for MDQ/MDQS write setup calculations (tDS).

f. Clock cycle time.

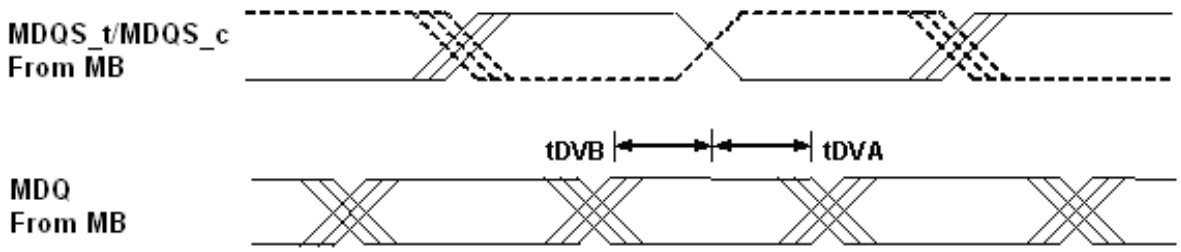


Figure 32 — tDVA and tDVB Timing Diagram

7.4.4 DRAM Interface Input and Output Timing (cont'd)

Table 56 — MB Operating Spec for Different Physical Ranks

		DDR3 800		DDR3 1066		DDR3 1333			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
TWRWR	Write to Write Command Spacing	BL/2 + 2		BL/2 + 2		BL/2 + 2		tCK(avg)	1, 2, 3
TRDRD	Read to Read Command Spacing	BL/2 + 2		BL/2 + 2		BL/2 + 2		tCK(avg)	1, 2, 3
TWRRD	Write to Read Command Spacing	BL/2 + 2 - (CL-CWL)		BL/2 + 2 - (CL - CWL)		BL/2 + 2 - (CL - CWL)		tCK(avg)	1, 2, 3
TRDWR	Read to Write Command Spacing	BL/2 + 4 + (CL - CWL)		BL/2 + 4 + (CL - CWL)		BL/2 + 4 + (CL - CWL)		tCK(avg)	1, 2, 3, 4

NOTE 1 Operation to different Physical Rank independent of Rank multiplication or Non Rank multiplication mode of operation.
NOTE 2 For operation to Same Physical Rank, this restriction does not apply. Host controller follows JESD79-3E. MB will guarantee the functionality in accordance with JESD79-3E.
NOTE 3 MB will guarantee the functionality with this minimum command spacing.
NOTE 4 This is meant for MB testing on ATE environment purpose to ensure proper buffer functionality. Host controller is likely to require additional separation to avoid the bus contention on Host controller and buffer input interface under normal operation.

Table 57 — MB Operating Spec for Different Physical Ranks

		DDR3 1600		DDR3 1866		DDR3 2133			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
TWRWR	Write to Write Command Spacing	BL/2 + 2		BL/2 + 2		BL/2 + 2		tCK(avg)	1, 2, 3
TRDRD	Read to Read Command Spacing	BL/2 + 2		BL/2 + 2		BL/2 + 2		tCK(avg)	1, 2, 3
TWRRD	Write to Read Command Spacing	BL/2 + 2 - (CL- CWL)		BL/2 + 2 - (CL - CWL)		BL/2 + 2 - (CL - CWL)		tCK(avg)	1, 2, 3
TRDWR	Read to Write Command Spacing	BL/2 + 4 + (CL - CWL)		BL/2 + 4 + (CL - CWL)		BL/2 + 4 + (CL - CWL)		tCK(avg)	1, 2, 3, 4

NOTE 1 Operation to different Physical Rank independent of Rank multiplication or Non Rank multiplication mode of operation.
NOTE 2 For operation to Same Physical Rank, this restriction does not apply. Host controller follows DRAM JESD79-3 Revision E Specification. MB will guarantee the functionality in accordance with DRAM JESD79-3 Revision E Specification.
NOTE 3 MB will guarantee the functionality with this minimum command spacing.
NOTE 4 This is meant for MB testing on ATE environment purpose only to ensure proper buffer functionality. Host controller is likely to require additional separation to avoid the bus contention on Host controller and buffer input interface under normal operation.

7.4.4 DRAM Interface Input and Output Timing (cont'd)

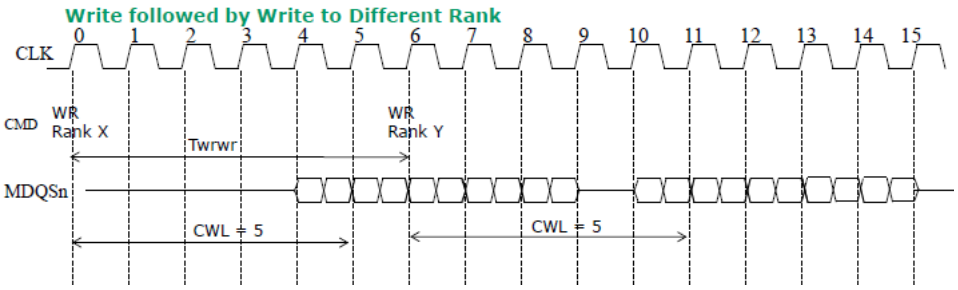


Figure 33 — Twrwr Timing Spec

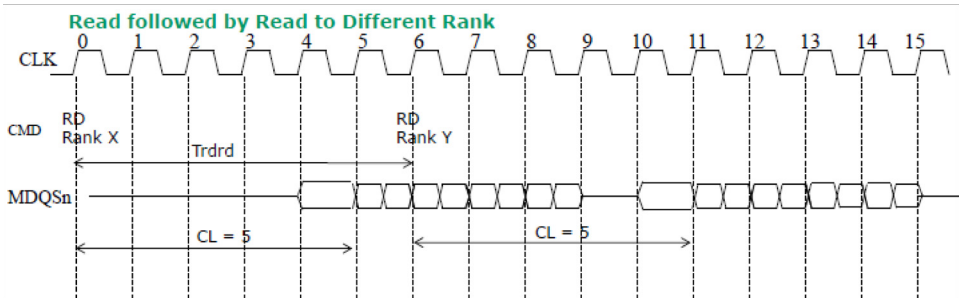


Figure 34 — Trdrd Timing Spec

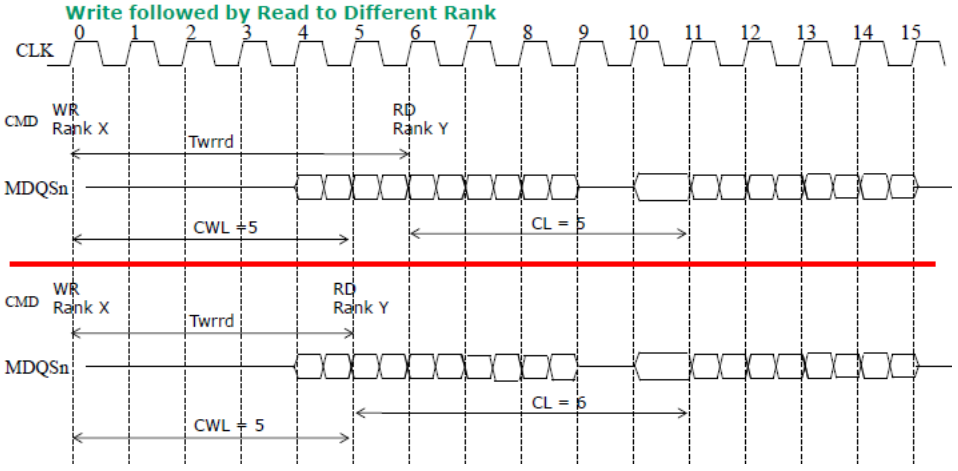


Figure 35 — Twrrd Spec

7.4.4 DRAM Interface Input and Output Timing (cont'd)

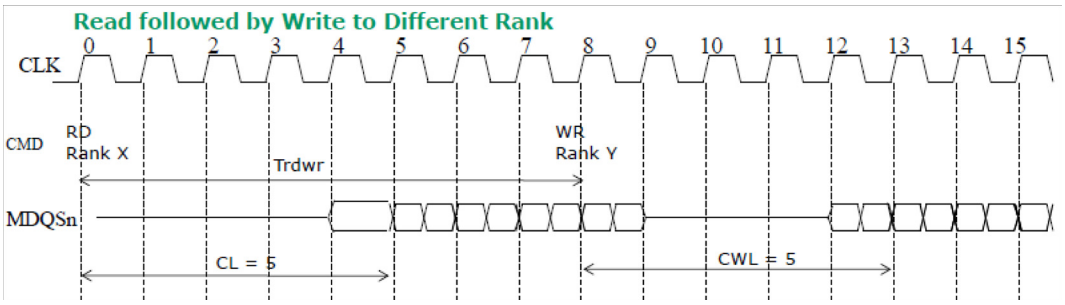
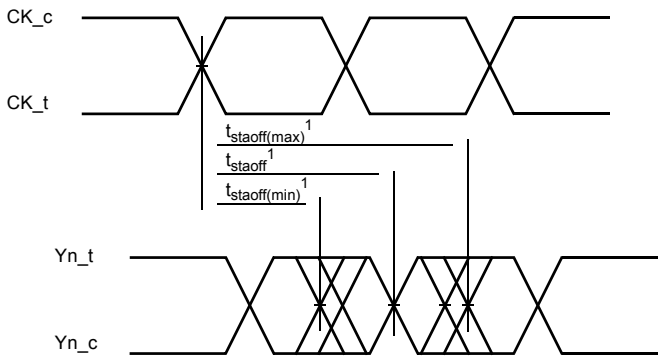


Figure 36 — Trdwr Spec



1. t_{staoff} = propagation delay for clock signal (rising CK input clock edge to rising Yn output clock edge).

Figure 37 — Definition for t_{staoff}

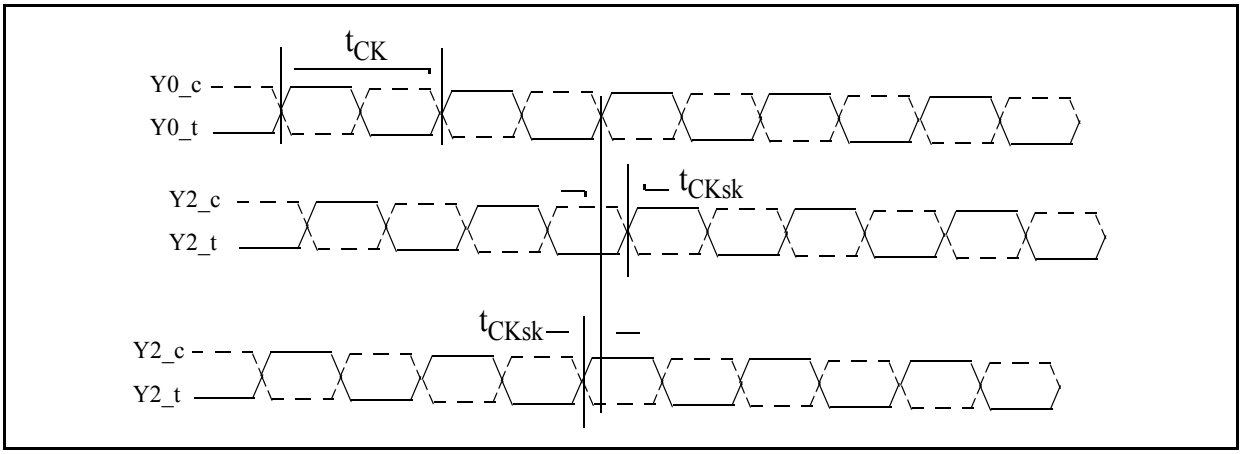
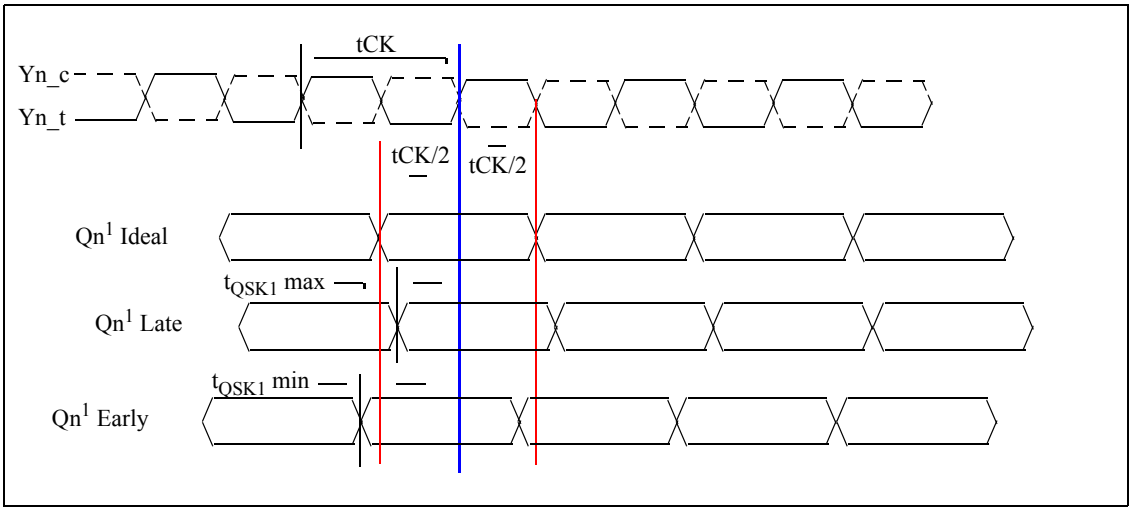


Figure 38 — Clock Output (Yn) Skew

7.4.4 DRAM Interface Input and Output Timing (cont'd)



1. Outputs as specified in Table 55, "DRAM Interface Output Timing Parameters", Footnote c

Figure 39 — Qn Output Skew for Standard 1/2-Clock Pre-Launch

Table 58 — Clock driver Characteristics at application frequency

Symbol	Parameter	DDR3/DDR3L-800		DDR3/DDR3L-1066		DDR3/DDR3L-1333		DDR3/DDR3L-1600		DDR3-1866		DDR3-2133		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
The DDR3 Memory Buffer must be capable of meeting all the above test parameters while supporting SSC synthesizers with the following parameters:														
	SSC modulation frequency	30	33	30	33	30	33	30	33	30	33	30	33	kHz
	SSC clock input frequency deviation	0.00	-0.5	0.00	-0.5	0.00	-0.5	0.00	-0.5	0.00	-0.5	0.00	-0.5	%
DDR3 Memory Buffer PLL designs should target the values below to improve tracking between CK_t/CK_c and Yn_t/Yn_c:														
t_{band}	PLL Loop bandwidth (-3 dB from unity gain)	25[a]	-	30[a]	-	35[a]	-	40[a]	-	45[a]	-	50[a]	-	MHz

NOTES:
a. Implies a -3 dB bandwidth and jitter peaking of 3 dB.

7.5 Data Setup, Hold and Slew Rate Derating

Table 59 — Derating values for DDR3-800/1066/1333/1600 tDS/tDH - (AC100)

ΔtDS, ΔDH derating in [ps] AC/DC based [a,b] AC100 Threshold -> VIH(ac)=VREF(dc)+100mV, VIL(ac)=VREF(dc)-100mV					
		DQS, DQS# Differential Slew Rate			
		> 2.0 V/ns		<= 2.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	5.0	60	60	-	-
	4.5	58	58	-	-
	4.0	56	56	-	-
	3.5	53	53	-	-
	3.0	50	50	-	-
	2.8	47	47	-	-
	2.6	46	46	-	-
	2.4	43	43	-	-
	2.2	40	40	-	-
	2.0	37	37	-	-
	1.8	32	32	-	-
	1.6	28	28	-	-
	1.4	21	21	-	-
	1.2	13	13	-	-
	1.0	0	0	-	-
	0.8	TBD	TBD	-	-
	0.6	TBD	TBD	-	-
	<0.6	-	-	-	-

NOTES:

a.Cell contents shaded in red are defined as ‘not supported’.

b.This Table is for MB HOST Interface and MB DRAM Interface.

7.5 Data Setup, Hold and Slew Rate Derating (cont'd)

Table 60 — Derating values for DDR3L-800/1066/1333/1600 tDS/tDH - (AC90)

ΔtDS, ΔDH derating in [ps] AC/DC based [a,b] AC90 Threshold -> VIH(ac)=VREF(dc)+90mV, VIL(ac)=VREF(dc)-90mV					
		DQS, DQS# Differential Slew Rate			
		> 2.0 V/ns		<= 2.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	5.0	52	52	-	-
	4.5	50	50	-	-
	4.0	49	49	-	-
	3.5	46	46	-	-
	3.0	43	43	-	-
	2.8	41	41	-	-
	2.6	39	39	-	-
	2.4	37	37	-	-
	2.2	34	34	-	-
	2.0	32	32	-	-
	1.8	28	28	-	-
	1.6	24	24	-	-
	1.4	18	18	-	-
	1.2	11	11	-	-
	1.0	0	0	-	-
	0.8	TBD	TBD	-	-
	0.6	TBD	TBD	-	-
	<0.6	-	-	-	-

NOTES:

a.Cell contents shaded in red are defined as 'not supported'.

b.This Table is for MB HOST Interface and MB DRAM Interface.

7.6 Nominal and Tangent line slew rate measurement for Setup and Hold De-rating

Figure 40 through Figure 47 can be used to determine the slew rate for tIS, tIH, tDS and tDH de-rating.

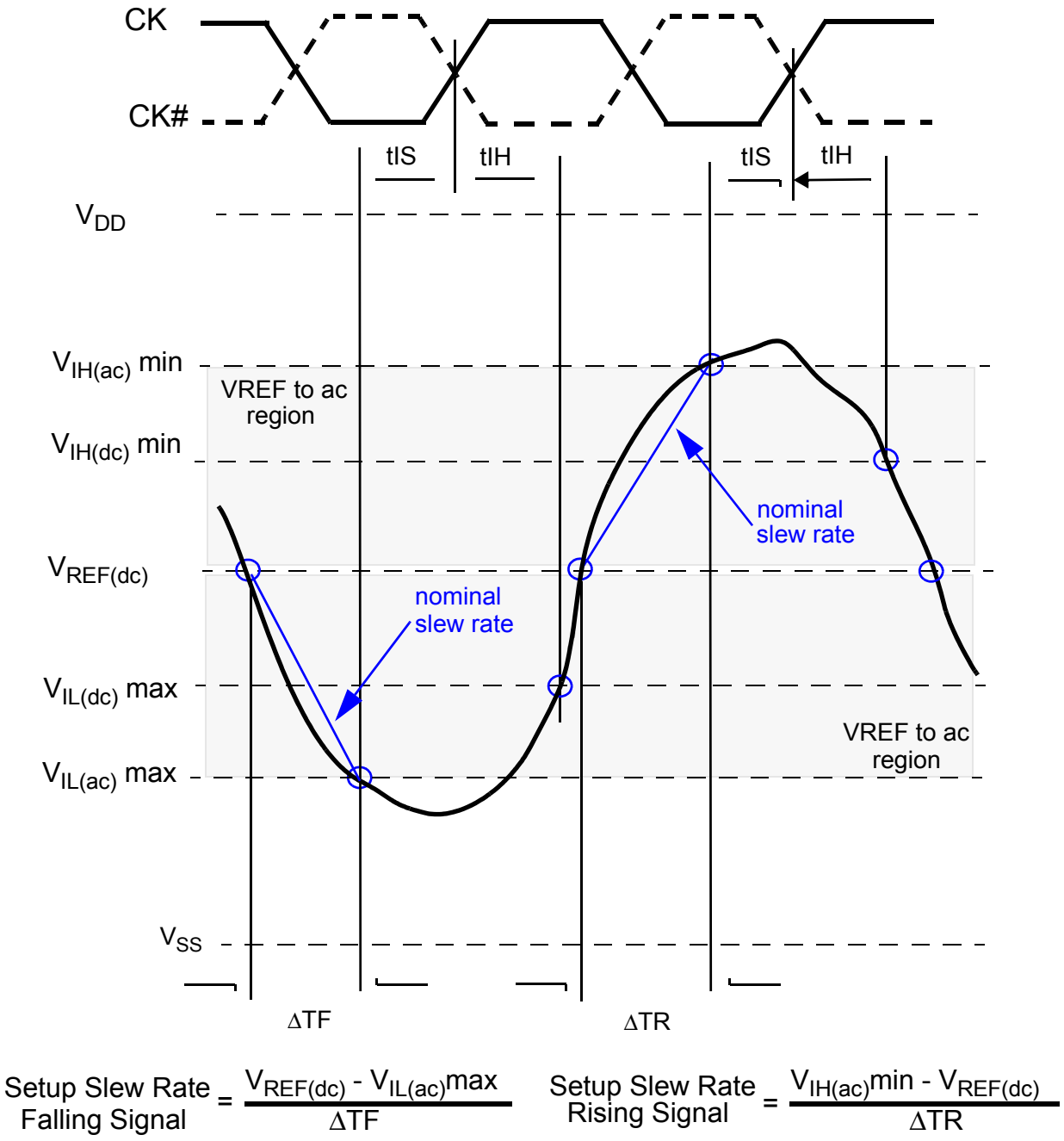


Figure 40 — Illustration of nominal slew rate for setup time tIS (for ADD/CMD with respect to clock)

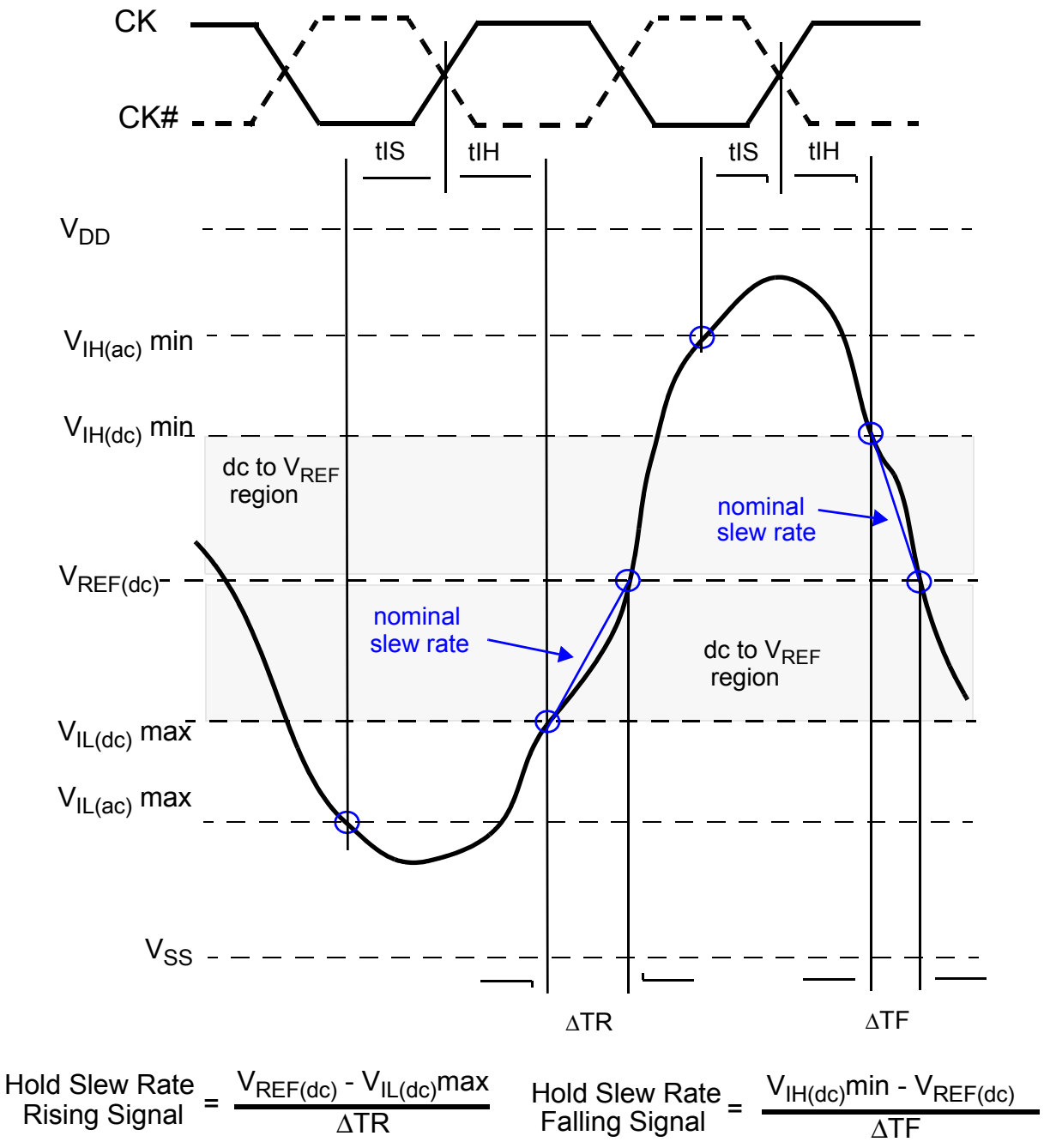


Figure 41 — Illustration of nominal slew rate for hold time tIH (for ADD/CMD with respect to clock).

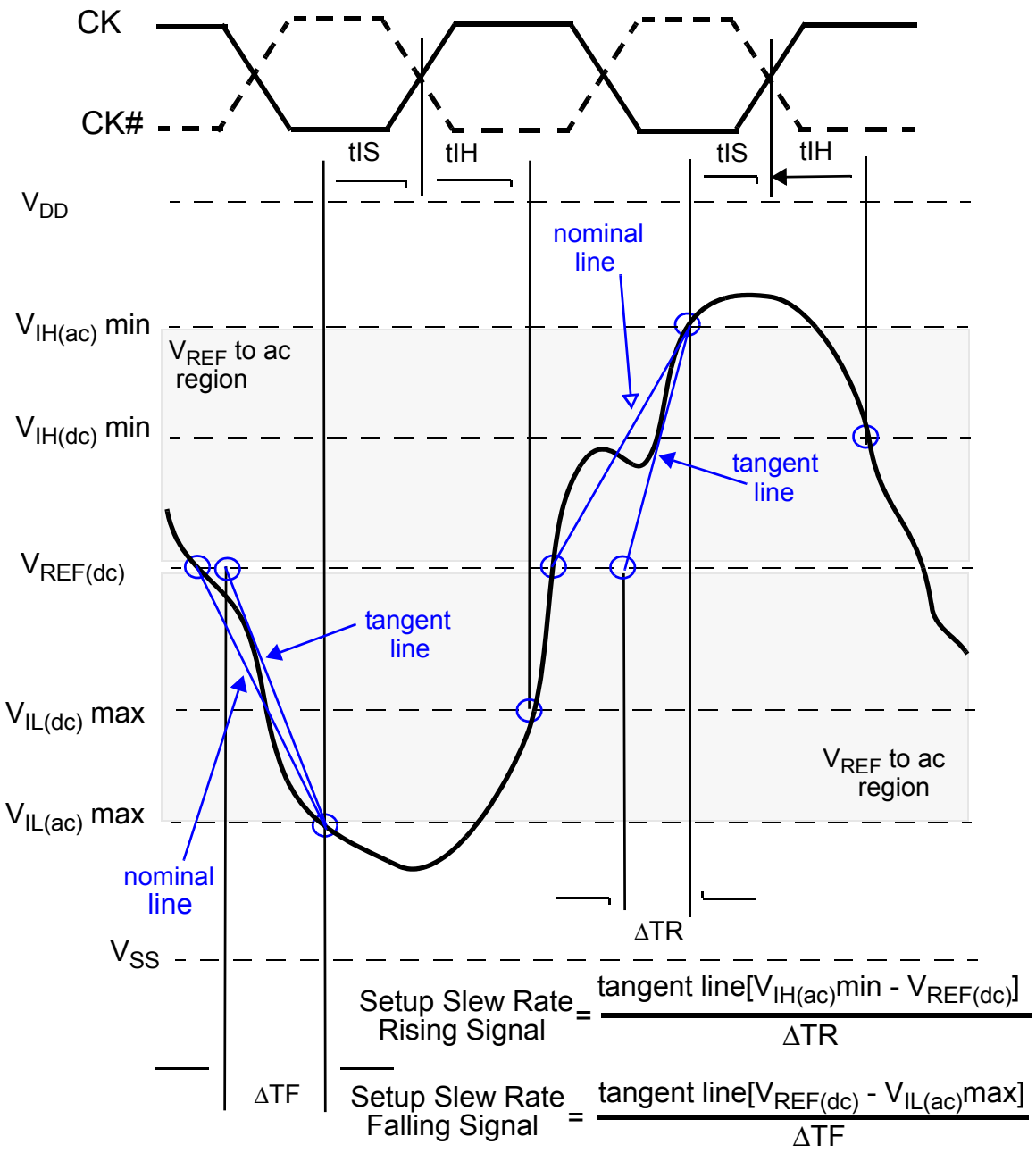


Figure 42 — Illustration of tangent line for setup time t_{IS} (for ADD/CMD with respect to clock)

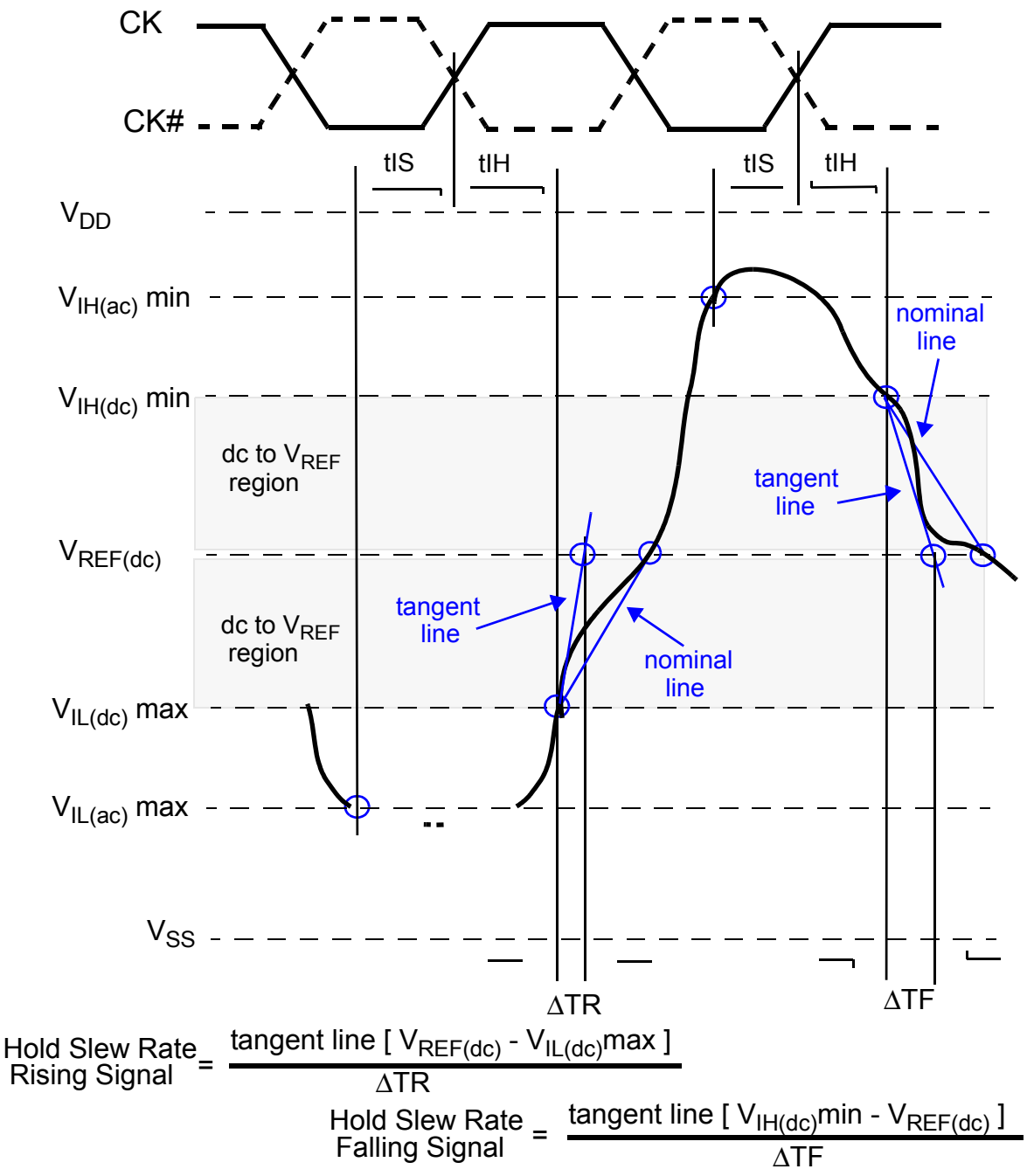


Figure 43 — Illustration of tangent line for hold time t_{IH} (for ADD/CMD with respect to clock)

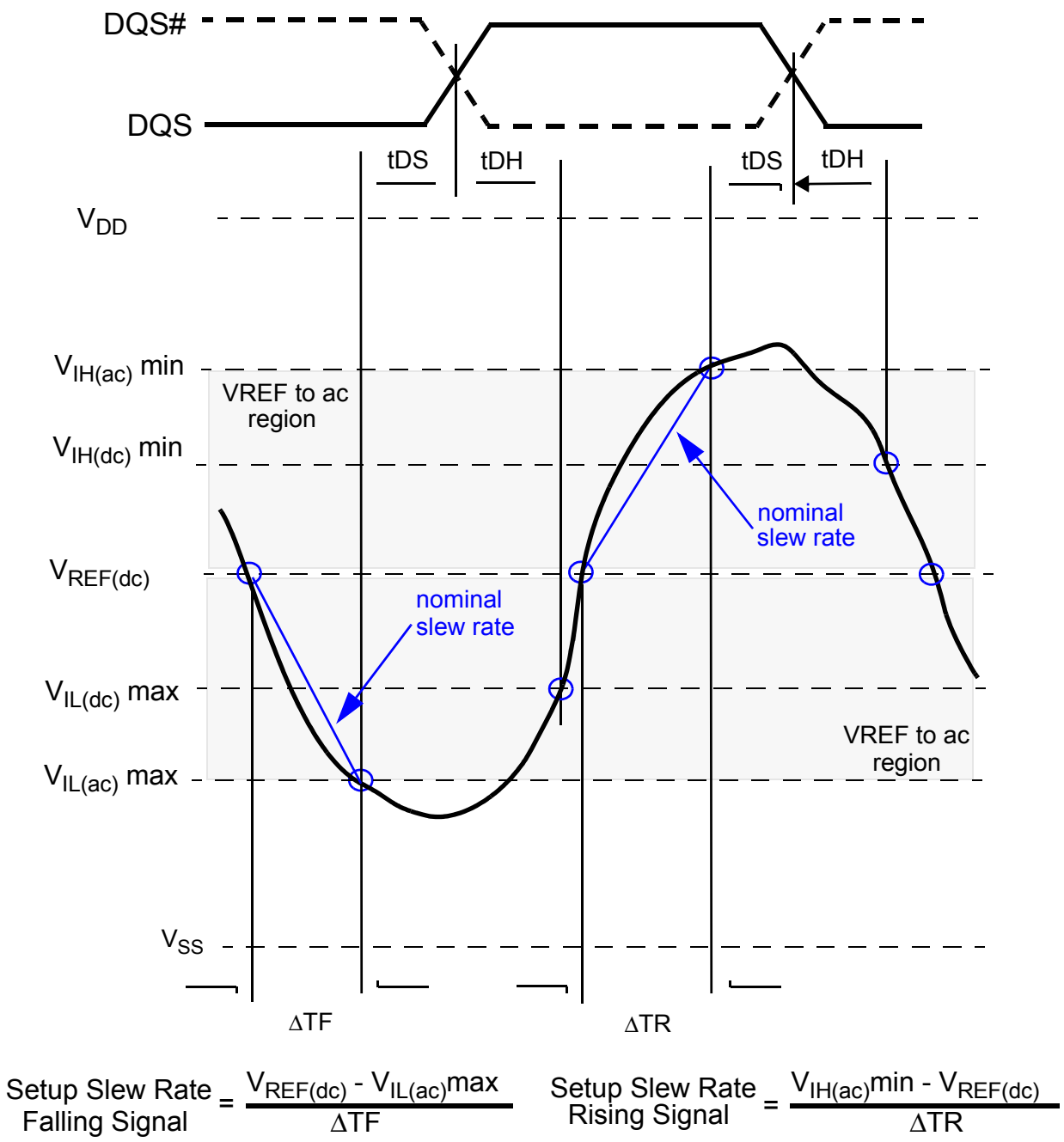


Figure 44 — Illustration of nominal slew rate for setup time t_{DS} (for DQ with respect to strobe).

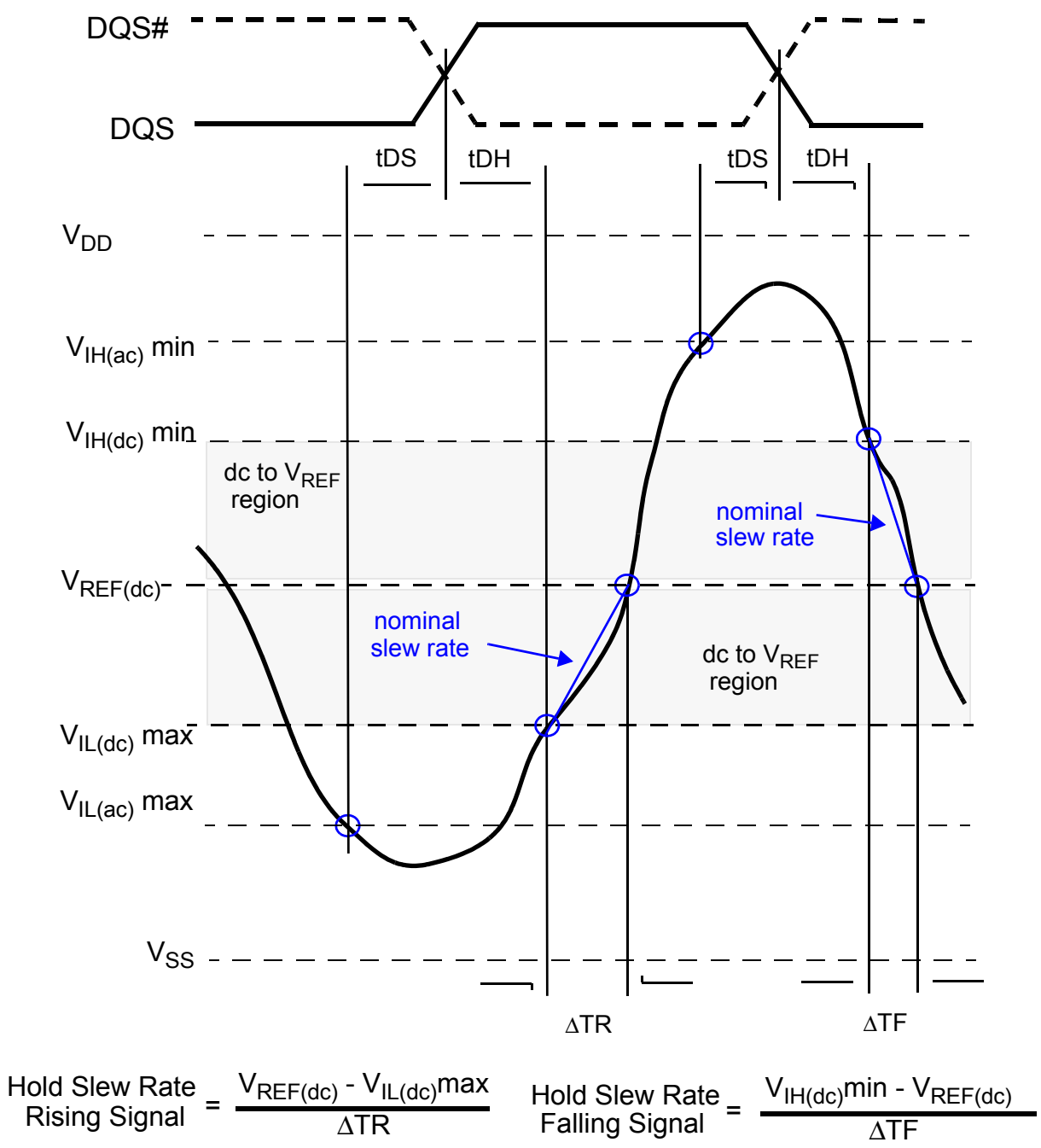


Figure 45 — Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe)

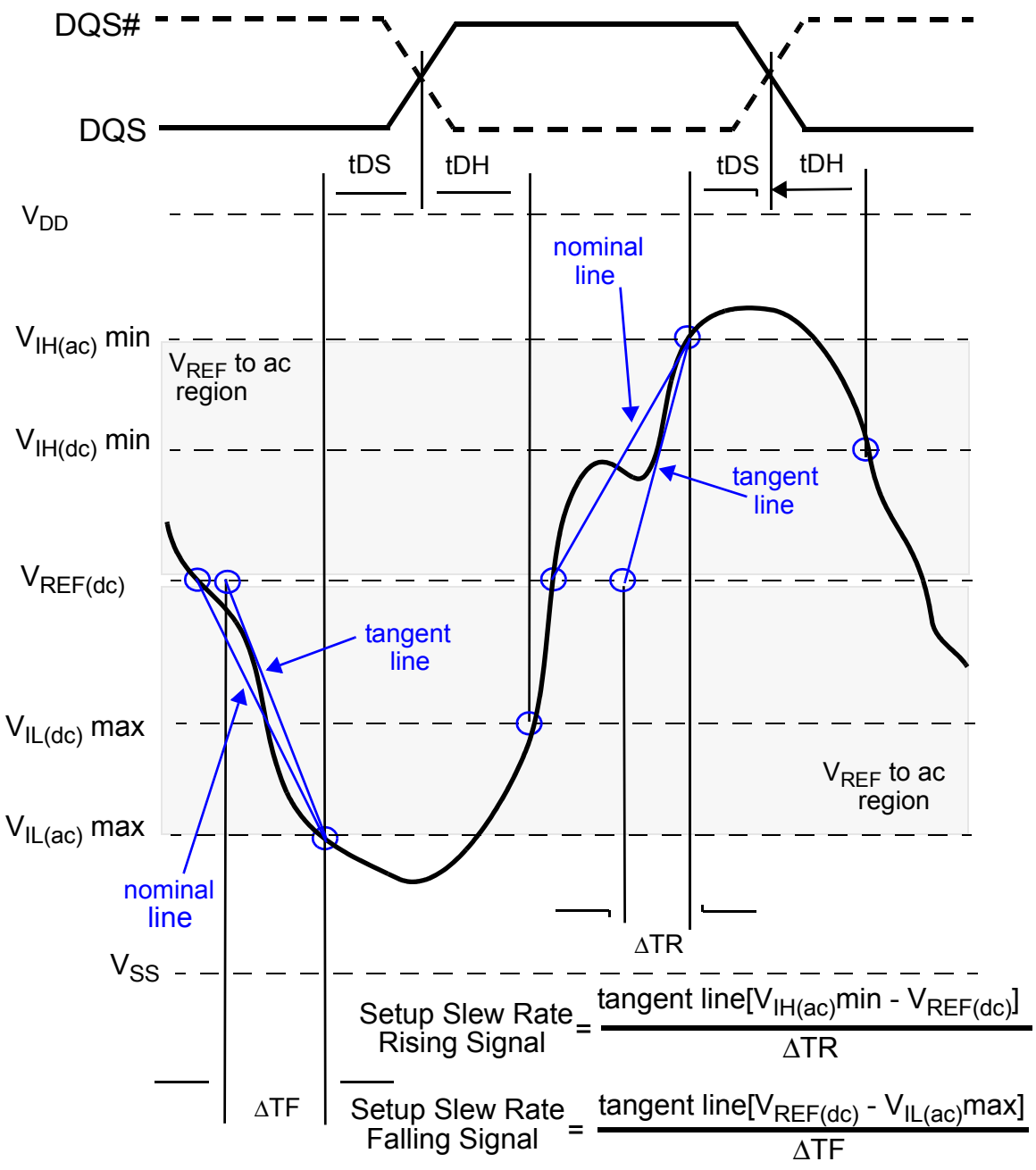


Figure 46 — Illustration of tangent line for setup time t_{DS} (for DQ with respect to strobe)

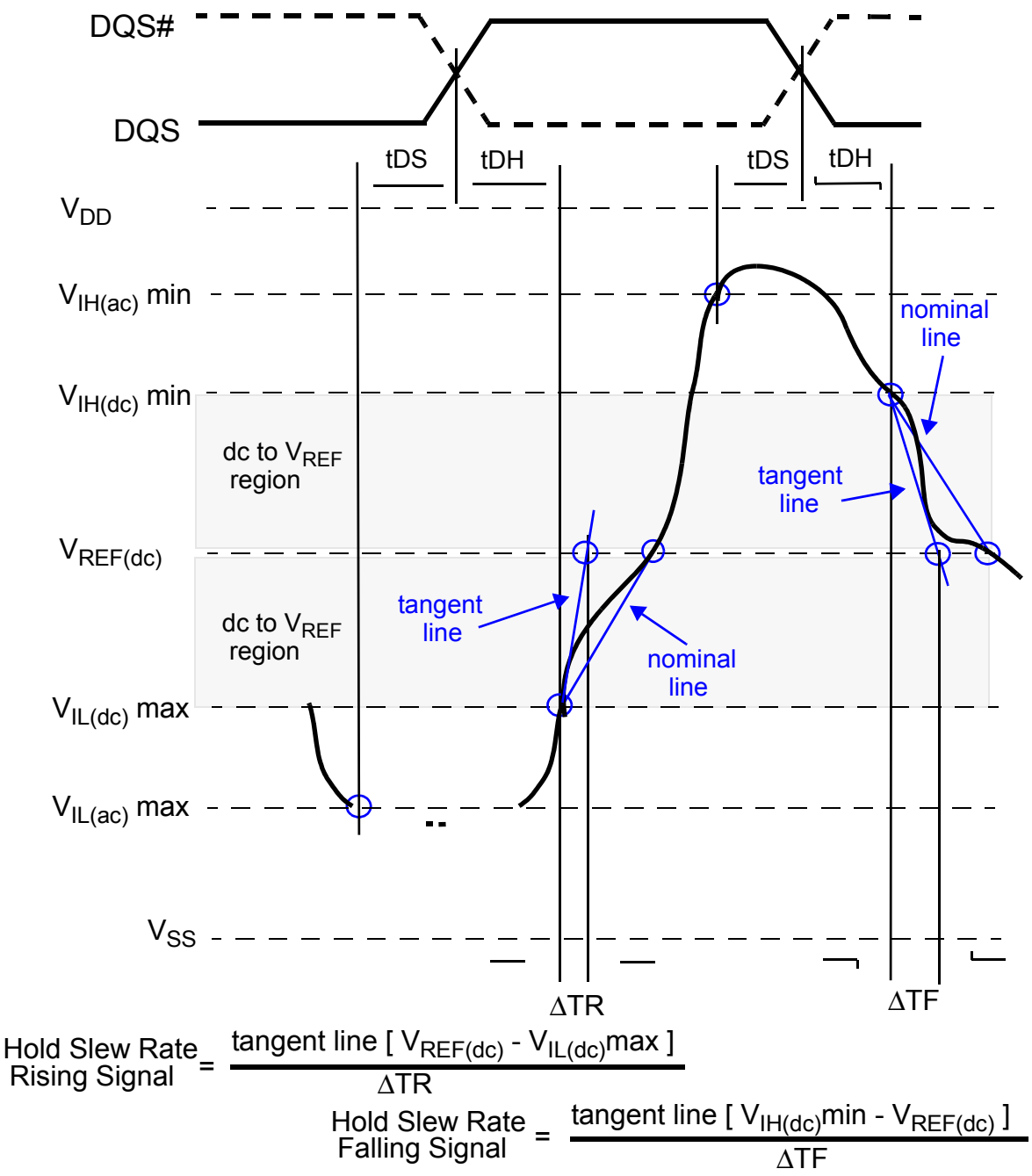


Figure 47 — Illustration of tangent line for hold time t_{DH} (for DQ with respect to strobe)

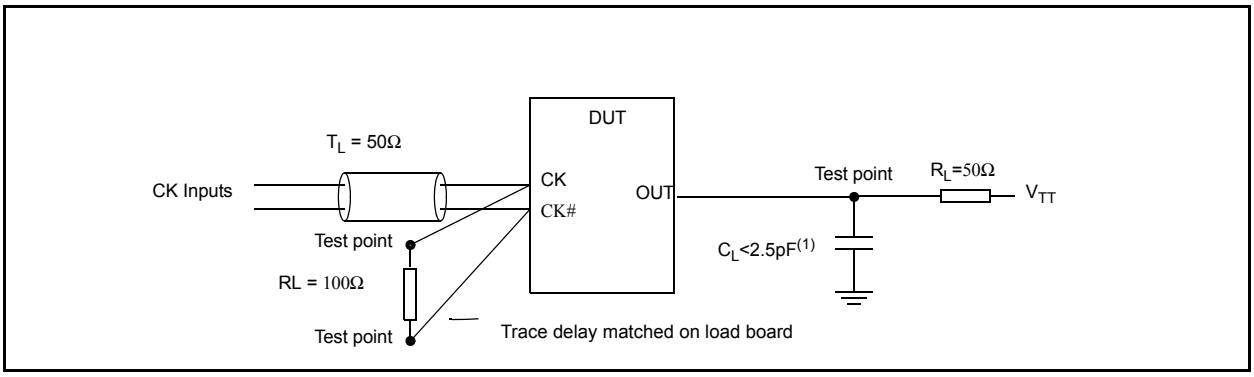
7.7 Test circuits and switching waveforms for CMD/ADD/CNTRL/CK Inputs

7.7.1 Parameter measurement information

All input pulses are supplied by generators having the following characteristics: 300MHz ≤ PRR ≤ 945 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

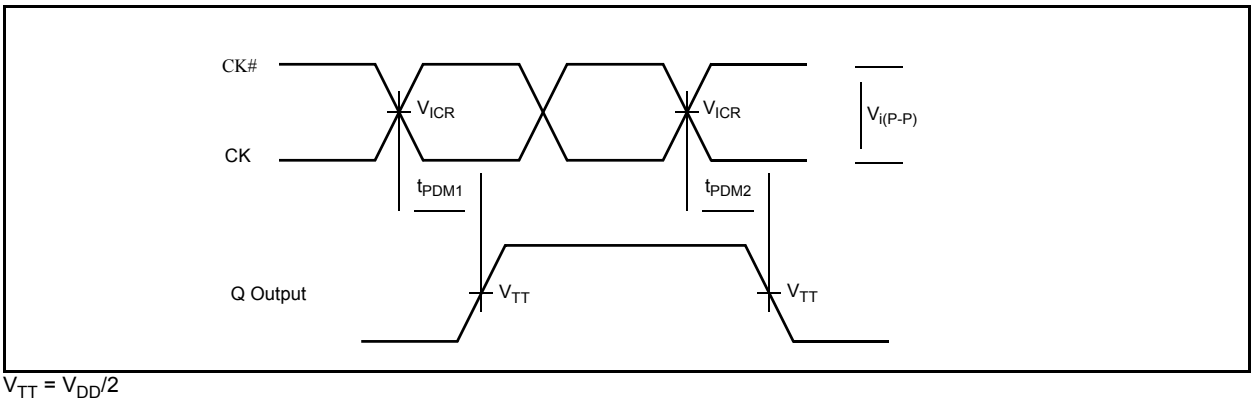
The outputs are measured one at a time with one transition per measurement.

Figure 48 — Voltage waveforms; input clock



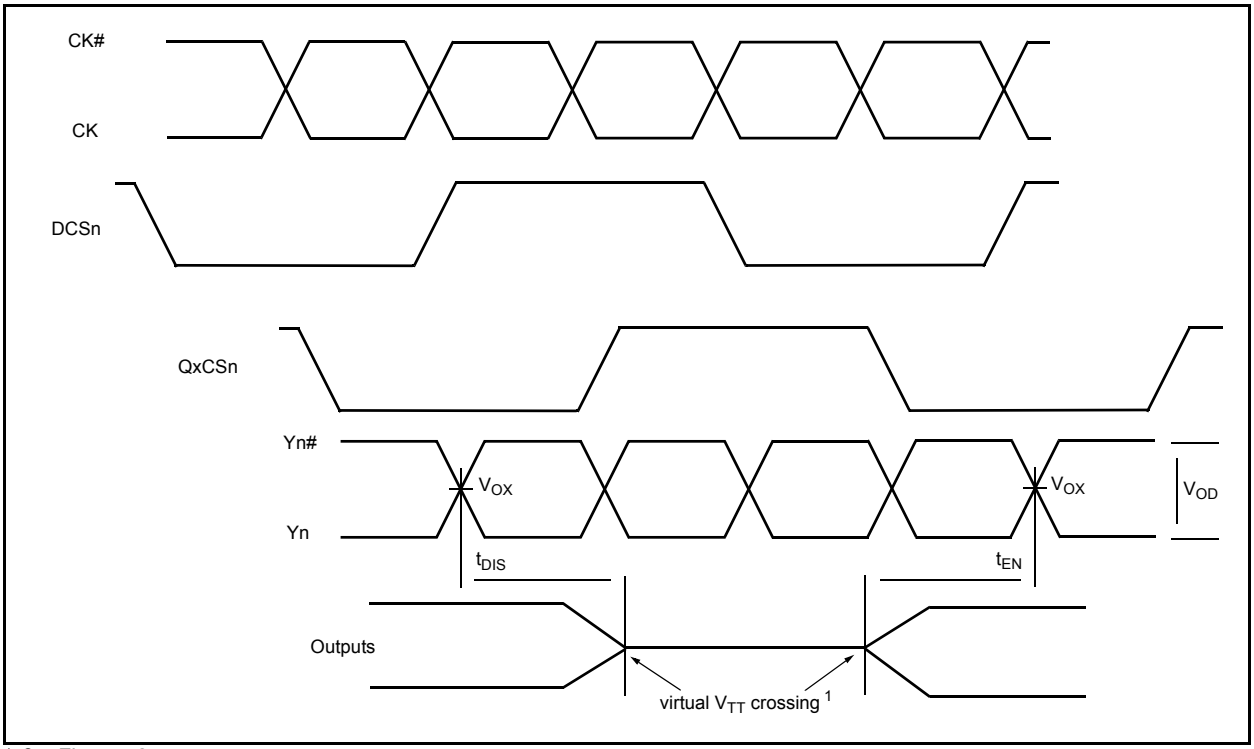
(1) C_L is parasitic (probe and jig capacitance)

Figure 49 — Qn and Yn Load circuit for propagation delay and slew measurement



$V_{TT} = V_{DD}/2$
V_{ICR} Cross Point Voltage
$V_{i(P-P)}$ = 450mV
t_{PDM1}, t_{PDM2} the larger number of both has to be taken when performing t_{PDM} max measurement, the smaller number of both has tobe taken when performing t_{PDM} min measurement

Figure 50 — Voltage waveforms; propagation delay times



1. See Figure 52

Figure 51 — Voltage waveforms address floating

.Enabling and disabling the CA outputs must not violate DRAM setup and hold time requirements. Therefore a t_{DIS} transition may not occur earlier than the earliest (HL/LH) transition and a t_{EN} transition may not occur later than the latest (HL/LH) transition. Regular transitions are measured between CK/CK# and CA/V_{TT} crossings however a V_{TT} crossing is not available in the state where the outputs are Hi-Z. To allow a correct and not overly conservative measurement a virtual V_{TT} crossing point is defined below. The calculation of the virtual V_{TT} crossing point is shown in Figure 52. The voltage levels for y_{xa} and y_{xb} are measured from V_{TT} (V_{DD}/2) and should be selected such that the region between t1 and t2 covers a linear range and represents a typical slope of the waveform within the transition area. They have to be used signed in the formula.

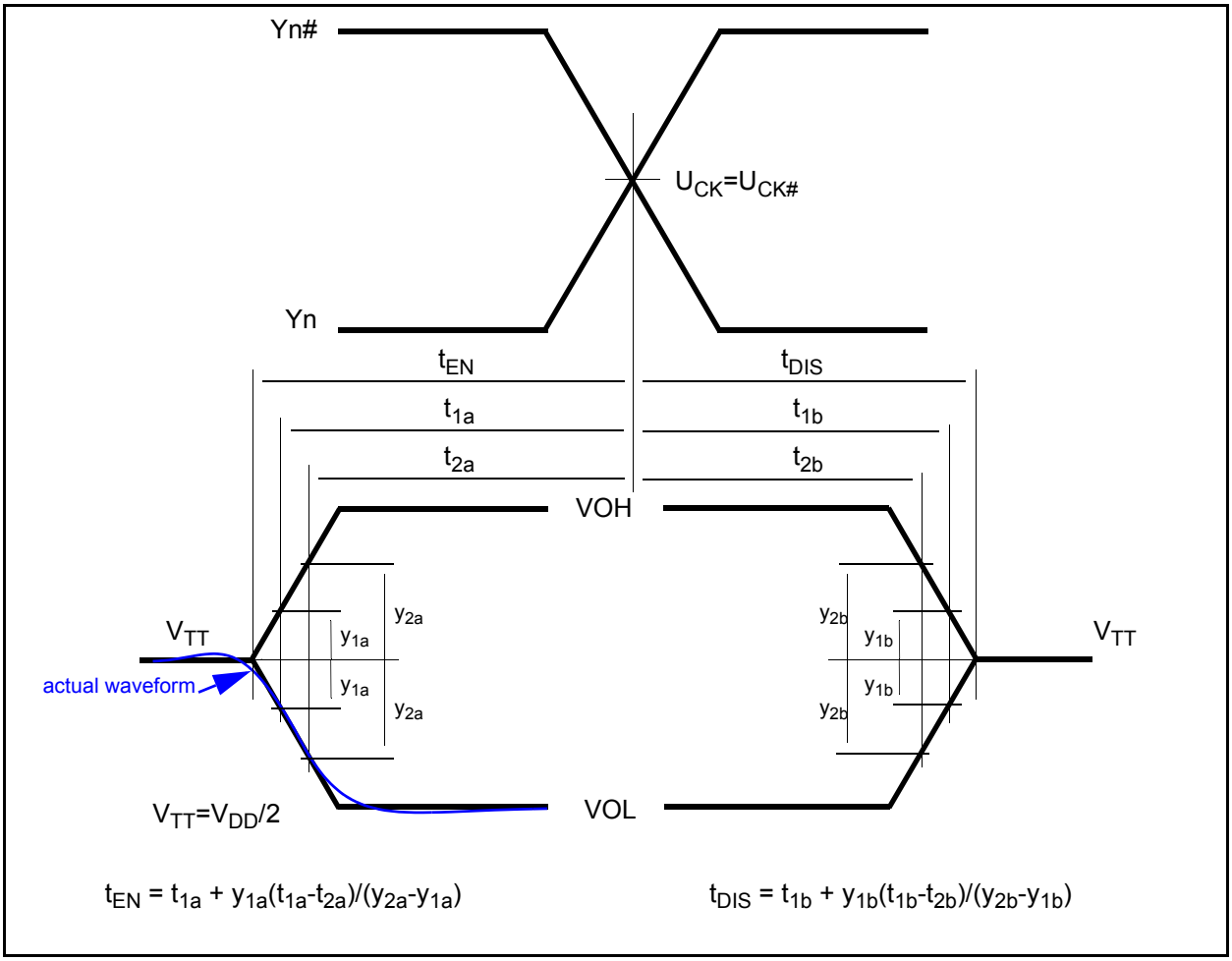
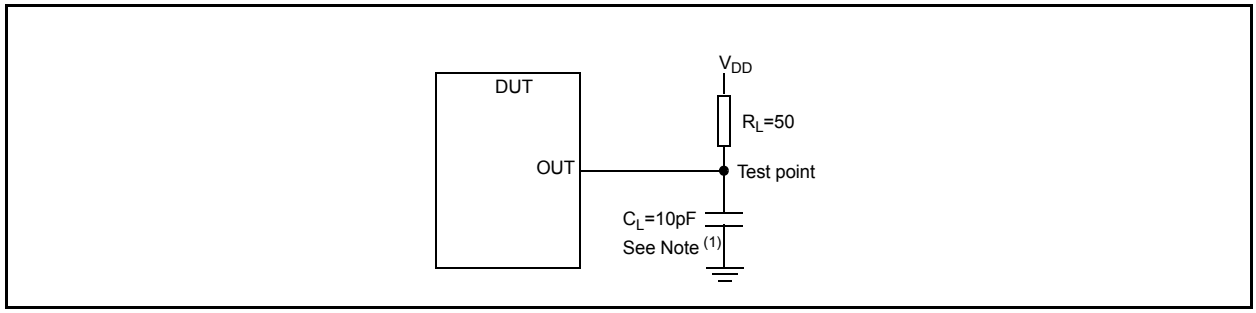


Figure 52 — Calculating the virtual V_{TT} crossing point

7.7.2 Error output load circuit and voltage measurement information

All input pulses are supplied by generators having the following characteristics: 300MHz ≤ PRR ≤ 1080 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Figure 53 — Load circuit, ERROUT_n Outputs

Output driver characteristics are separately controlled for outputs that are often loaded with twice as many DRAMs as the other outputs. Outputs are grouped as follows:

CA Signals =QxA0-QxAn, QxBA0-QxBAn, QxRAS_n, QxCAS_n, QxWE_n

Control Signals = QxCS_n, QxCKEn, QxODTn

CK = Yn_t.. Yn_c

8 Power Management

In order to minimize the power consumption of the Memory Buffer, the MB shall put blocks that are active only during initialization into a reduced power quiescent state during normal operation. These include:

(1) Host interface write leveling phase detector

(2) Read training logic

(3) DRAM interface write leveling logic

(4) MemBIST

(5) Transparent mode logic

(6) LAI mode logic

In addition the MB supports the following power management features.

8.1 CKE Power Management

The Memory buffer supports both traditional CKE control via two or four DCKE input pins, see Table 61, as well as a newly defined CKE command, see Table 62, which is defined in the same format as DRAM commands.

Table 61 — CKE Management Control Register (in F0RC6)

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	4 QxCKE outputs are controlled by 2 DCKE inputs	Default: DCKE[0] --> QxCKE[0] and QxCKE[2][a] DCKE[1] --> QxCKE[1] and QxCKE[3][1]
x	x	0	1	4 QxCKE outputs are controlled by 4 DCKE inputs	DCKE[0] --> QxCKE[0] DCKE[1] --> QxCKE[1] DCKE[2] --> QxCKE[2] DODT[1]/DCKE[3][b] --> QxCKE[3]
x	x	1	0	4 QxCKE outputs are controlled independent of 2 DCKE inputs: Buffer only asserts or de-asserts QxCKE[x] Ranks that is specified by host command	See Table 62

a. In 2 Rank case, buffer tri-states QxCKE[2] and QxCKE[3] outputs.
b. In 4 DCKE mode (DA4:DA3='01', DODT[1]/DCKE[3] pin will be used as DCKE[3]. In all other cases, the pin will be used as DODT[1] if DBA0='1' otherwise DODT1 pin is not used and it may be tri-stated and buffer turns off IBT for DODT1. Additionally in 4 DCKE mode (DA4:DA3 = '01'), bit DBA0 must be '0'.

NOTE 1 The three CKE modes are described in 8.1.1, 8.1.2, and 8.1.3.

8.1.1 2 DCKE mode (RDIMM Compatible Mode)

This is the default mode of the DIMM following RESET.

Normal RDIMMs have two DCKE inputs. DCKE0 goes to Rank 0 and Rank 2 (quad rank DIMMs). DCKE1 goes to Rank 1 (dual or quad rank DIMMs) and Rank 3 (quad rank DIMMs). LRDIMMs use this same configuration by default, extending it to 8 rank DIMMs by having DCKE0 go to all even numbered ranks (both physical and logical), and DCKE1 go to all odd numbered ranks. The DCKE input is always sent on to the appropriate QCKE outputs in this mode.

8.1.2 4 DCKE mode

The MB may be configured to have 4 DCKE inputs for finer granularity rank control of power management. The additional DCKE inputs are achieved by using a formerly NC/Test pin on the DIMM connector for DCKE2 and the DODT1 pin for DCKE3. The behavior of the DCKE3/DODT1 pin is determined by all three defined bits in F0RC6. Note that F0RC6 DBA0 must be set to '0' in 4 DCKE mode, otherwise the MB behavior is undefined.

8.1.3 Soft CKE mode

In Soft CKE mode the QxCKEx outputs are controlled by commands sent by the host, not directly by the DCKEx inputs. The DCKEx inputs do not affect the QxCKEx outputs except for the Entry and Self Refresh Exit commands. The DCKEx inputs do affect the power state of the MB, however. The MB will not accept commands when both DCKE inputs are low and the CKE Power Down Mode Enable bit is set.

The Soft CKE command uses a further decode of the ZQ cal command encoding, using address bits A[15:13].

Table 62 — Soft CKE Command Definition[1]

Function	CS_n	RAS_n	CAS_n	WE_n	BA[2:0]	A15	A14	A13	A[12:11]	A10	A[9:8]	A[7:4]	A[3:0]
ZQCL	L	H	H	L	x	0	0	0	x	H	x	x	x
ZQCS					x	0	0	0	x	L	x	x	x
CKE Control					**x**	**0**	**0**	**1**	**x**	**x**	**x**	**TBD**	**QxCKE [3:0][a]**
RSVD					x	0	1	x	x	x	x	x	x
RSVD					x	1	x	x	x	x	x	x	x

a. A[3:0] during CKE control command: 0 --> de-assert corresponding QxCKEx low; 1 --> assert corresponding QxCKEx high.

When Soft CKE is disabled, A[15:13] are ignored and all combinations are considered ZQ cal commands. The MB will accept a Soft CKE command when any of the configured DCSx_n inputs are active. All four QCKE outputs will be affected by the Soft CKE command regardless of which DCSx_n input was active for the command. As usual, the soft CKE command is not accepted by the MB unless a DCSx_n input is low and at least one of the DCKEx inputs is high.

On a soft CKE command the QxCKEx outputs will be affected with the same timing as the address/ command signals as if it were a DRAM command. The soft CKE command only affects the QxCKEx outputs. The address/command signals do not change and the QxCSx_n outputs are not asserted.

1.This definition only applies when F0RC6 DA4:DA3 = '10'

8.2 Memory Buffer Power Savings Modes

The device supports different power saving mechanisms.

When both inputs CK_t and CK_c are being held LOW the device stops operation and enters low-power static and standby operation. It stops its PLL and floats all outputs except QACKE[3:0] and QBCKE[3:0] which are kept driven LOW. Before the device is taken out of standby operation by applying a stable input clock signal, the MB inputs DCS[1:0]_n must be pulled HIGH to prevent accidental access to the control registers and DCKE[2:0] as well as DCKE3/DODT[1] must be pulled LOW for a certain period of time (t_{ACT}). The input clock must be stable for a time (t_{STAB}) before any access to the device takes place. Stopping the clocks (CK_t=CK_c=LOW) will only put the MB in the low-power mode and will not clear any configuration registers including SMBus registers. The control word registers will reset only when RESET_n is driven LOW.

A weak drive feature can be enabled by setting the corresponding bit in the control word F0RC0. This causes the device to monitor all the DCS[x:0]_n inputs and weakly drive outputs corresponding with the chip select gated inputs when all the DCS[x:0]_n inputs are HIGH. If any one of the DCS[x:0]_n input is LOW, the Qn outputs will function normally.

Once all the DCS[x:0]_n inputs are HIGH, the gated address command inputs to the MB can float to conserve input termination power. DCKE[2:0], DCKE[3]/DODT[1] and DODT0 need to be driven by the system all the time.

The RESET_n input has priority over all other power saving mechanisms. When RESET_n is driven LOW, it will force the Qn outputs to float, the ERROUT_n output HIGH, the QACKE[3:0] and QBCKE[3:0] outputs LOW and disables Input Bus Termination (IBT).

8.2.1 Memory Buffer CKE Power Down

The MB monitors all DCKEx input signals and enters into power saving state when it latches LOW on all DCKEx inputs and at least one of the DCKEx input has transitioned from HIGH to LOW.

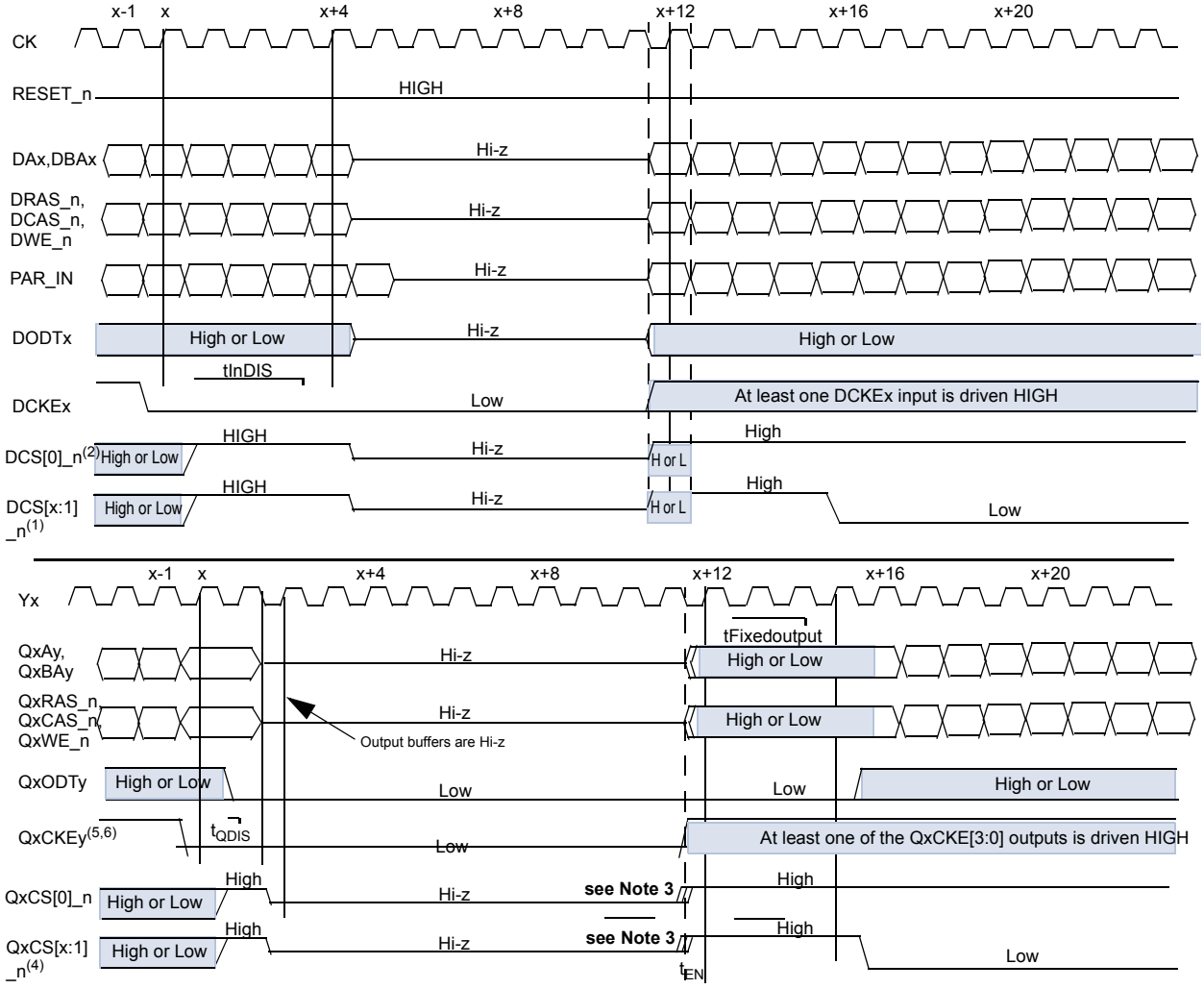
There are two modes of CKE Power Down selected by control word RC9. Bit DBA0 in RC9 determines whether the MB turns off IBT & DQ Rtt or keeps IBT & DQ Rtt on.

8.2.1.1 Memory Buffer CKE Power Down with IBT Off

Upon entry into CKE Power Down mode with IBT off, all MB input buffers including IBT are disabled except for CK_t/CK_c, DCKEx and RESET_n. The MB disables input buffers within t_{InDIS} clocks after latching all DCKE[x:0] inputs[1] LOW. In order to eliminate any false parity check error, the PAR_IN input buffer has to be kept active for 1 tCK after the Address and Command input buffers are disabled. After t_{InDIS}, the MB can tolerate floating input except for CK_t/CK_c, DCKEx and RESET_n. The MB also disables all its output buffers except for Yx_t/Yx_c, QxODT[1:0] and QxCKE[3:0]. The state of the output clocks Yx_t/Yx_c in CKE Power Down with IBT Off mode is determined by F0RC9 DA4. When DA4='0' the Yx_t/Yx_c outputs continue to drive a valid phase accurate clock signal. The QxODT[1:0] outputs are driven LOW. The QxCKE[3:0] outputs are driven LOW[2]. The MB output buffers are hi-z t_{QDIS} clock after the QxCKE[3:0] outputs are driven LOW. This is shown in Figure 54.

1. x=1 if F0RC6 DA4:DA3='00', x = 3 if F0RC6 DA4:DA3='01'
2. If F0RC6 DA4='0' OR if F0RC6 DA4:DA3='10' AND SRE command present

8.2.1.1 Memory Buffer CKE Power Down with IBT Off (cont'd)



(1) x = 3 for JEDEC standard DIMMs, x = 7 for non-JEDEC applications.
(2) During CKE Power Down Entry/Exit, driving DCS[1:0]_n LOW is illegal as it will force MB into Register Control Word access mode.
(3) Upon CKE Power Down exit, QxCS[x:0]_n will be held HIGH for maximum of 1 tCK regardless of what DCSx_n input level is. For all other operation QxCSx_n outputs will follow DCSx_n inputs.
(4) x = 3 for dual or quad-rank DIMMs, x =7 for octal rank DIMMs.
(5) DCKEx H-->L transition forwarded to QxCKEy if F0RC6 DA4='0' OR if F0RC6 DA4:DA3='10' AND SRE command present
(6) DCKEx L-->H transition forwarded to QxCKEy if F0RC6 DA4='0' OR if F0RC6 DA4:DA3='10' AND last DCKEx H-->L transition was a SRE

Figure 54 — Power Down Mode Entry and Exit with IBT

8.2.1.1 Memory Buffer CKE Power Down with IBT Off (cont'd)

When one or more of the DCKEx inputs[1] are driven HIGH, the MB exits from this Power Down Mode and valid logic levels are required at all MB inputs. Upon any one of the DCKEn inputs going HIGH, the MB immediately starts driving HIGH on the appropriate QxCKEy signals[2]. The QxCSx_n signals are driven HIGH and QxODTy signals are driven LOW and the host interface DQ termination stays disabled. Other output signals QxRAS_n, QxCAS_n, QxWE_n and QxAddr are driven either HIGH or LOW to ensure stable valid logic on all MB outputs when QxCKEy goes HIGH. The device drives output signals to these levels for $t_{Fixedoutput}$ to allow input receivers to be stabilized. After the input receivers are stabilized, the MB outputs follow their corresponding input levels, QxODT[1:0] is generated from the incoming commands and host interface DQ termination is controlled by DODTx inputs. When exiting CKE power down mode, all but one of the chip select inputs DCSx_n can be asserted for 1 tCK without causing the corresponding QxCSx_n outputs to be asserted. The device guarantees that input receivers are stabilized within $t_{Fixedoutput}$ clocks after DCKEx input is driven HIGH. This is shown in Figure 54.

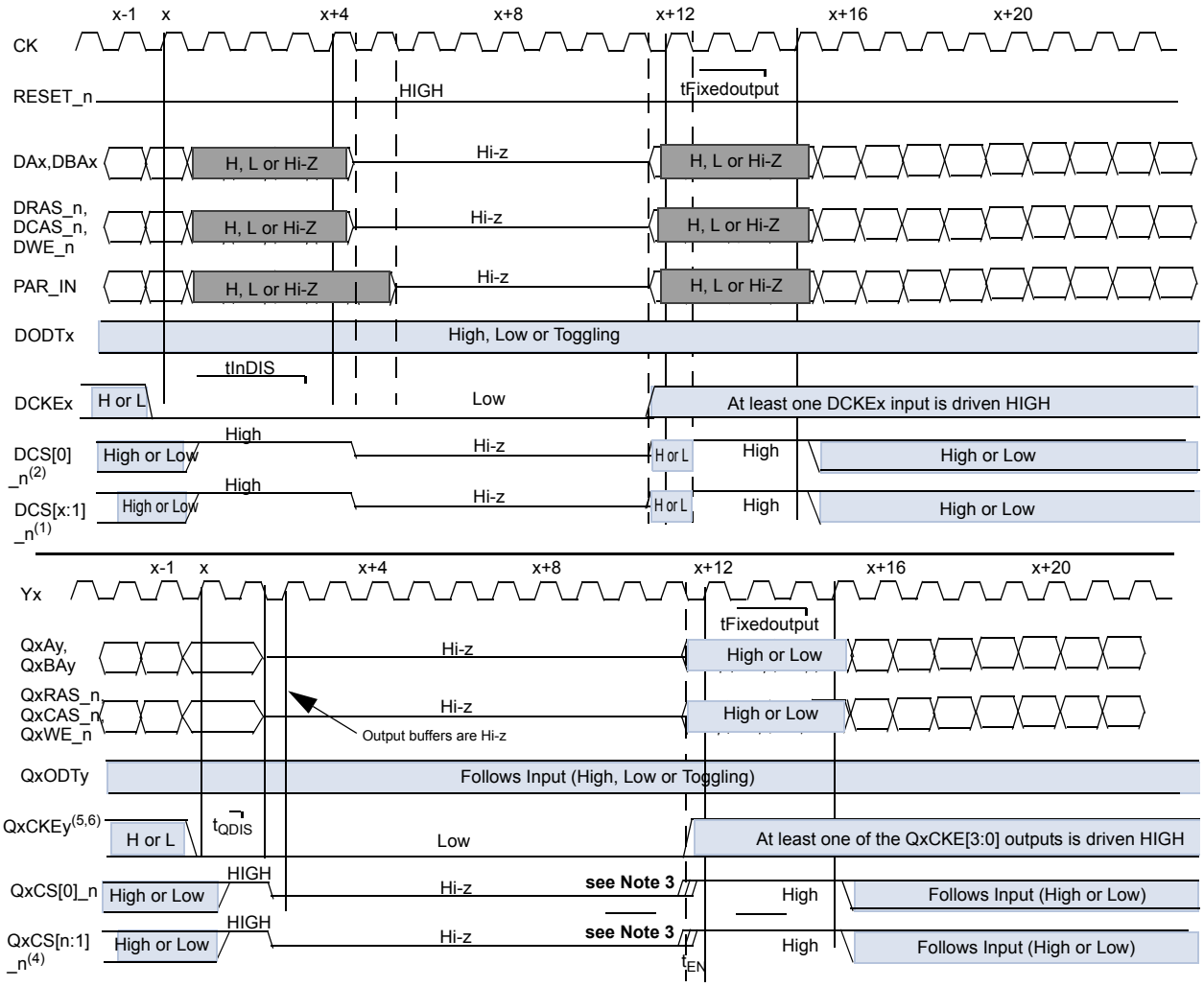
DODT registered HIGH in the first clock after $t_{Fixedoutput}$ will cause the host interface DQ termination to be turned on with synchronous ODT timing as defined for normal operation. Any read or write command issued in the first clock cycle after $t_{Fixedoutput}$ will be forwarded to the DRAMs and the associated data will be redriven by the MB. Since a fast MB may turn on receivers and forward signals as early as $t_{Fixedoutput}$(min) the host must not send any erroneous after $t_{Fixedoutput}$ min and the host must not send any valid commands before $t_{Fixedoutput}$(max) as a slow MB may not forward it.

8.2.1.2 Register CKE Power Down with IBT On

Upon entry into CKE Power Down Mode with IBT on, all MB input buffers excluding IBT are disabled except for CK_t/CK_c, DCKEx, DODTx and RESET_n. The MB disables input buffers within t_{InDIS} clocks after latching all DCKEx inputs[3] LOW. In order to eliminate any false parity check error, the PAR_IN input buffer has to be kept active for 1 tCK after the Address and Command input buffers are disabled. After t_{InDIS}, the MB can tolerate floating input except for CK_t/CK_c, DCKEx, DODTx and RESET_n. The MB also disables all its output buffers except for Yx_t/Yx_c, QxODT[1:0] and QxCKE[3:0]. The state of the output clocks Yx_t/Yx_c in CKE Power Down with IBT On mode is determined by F0RC9 DA4. When DA4='0' the Yx_t/Yx_c outputs continue to drive a valid phase accurate clock signal. The QxCKE[3:0] outputs are driven LOW[4]. The MB output buffers are hi-z t_{QDIS} clock after QxCKE[3:0] is driven LOW. This is shown in Figure 55.

1. x=1 if F0RC6 DA4:DA3='00', x = 3 if F0RC6 DA4:DA3='01'
2. If F0RC6 DA4='0' OR if F0RC6 DA4:DA3='10' AND last DCKEx H-->L transition was a SRE
3. x=1 if F0RC6 DA4:DA3='00', x = 3 if F0RC6 DA4:DA3='01'
4. If F0RC6 DA4='0' OR if F0RC6 DA4:DA3='10' AND SRE command present

8.2.1.2 Register CKE Power Down with IBT On (cont'd)



(1) x = 3 for JEDEC standard DIMMs, x = 7 for non-JEDEC applications.
(2) During CKE Power Down Entry/Exit, driving DCS[1:0]_n LOW is illegal as it will force MB into Register Control Word access mode.
(3) Upon CKE Power Down exit, QxCSx_n will be held HIGH for maximum of 1 tCK regardless of what DCSx_n input level is. For all other operation QxCSy_n outputs will follow DCSx_n inputs.
(4) x = 3 for dual or quad-rank DIMMs, x =7 for octal rank DIMMs.
(5) DCKEx H-->L transition forwarded to QxCKEy if F0RC6 DA4='0' OR if F0RC6 DA4:DA3='10' AND SRE command present
(6) DCKEx L-->H transition forwarded to QxCKEy if F0RC6 DA4='0' OR if F0RC6 DA4:DA3='10' AND last DCKEn H-->L transition was a SRE

Figure 55 — Power Down Mode Entry and Exit with IBT On

8.2.1.2 Register CKE Power Down with IBT On (cont'd)

When one or more of the DCKEx inputs[1] are driven HIGH, the MB exits from this Power Down Mode with IBT on and valid logic levels are required at all MB inputs. Upon any one of the DCKEx inputs going HIGH, the MB immediately starts driving HIGH on the appropriate QxCKEy signals[2]. The QxCSy_n signals are driven HIGH and the QxODTy signals are driven LOW. Other output signals QxRAS_n, QxCAS_n, QxWE_n and QxAddr are driven either HIGH or LOW to ensure stable valid logic on all device outputs when QxCKEy goes HIGH. The device drives output signals to these levels for $t_{Fixedoutput}$ to allow input receivers to be stabilized. After the input receivers are stabilized, the MB outputs follow their corresponding input levels, QxODT[1:0] is generated from the incoming commands and host interface DQ termination is controlled by the DODTx inputs. When exiting CKE power down mode, all but one of the chip select inputs DCSx_n can be asserted for 1 tCK without causing the corresponding QxCSx_n outputs to be asserted. The device guarantees that input receivers are stabilized within $t_{Fixedoutput}$ clocks after DCKEn input is driven HIGH. This is shown in Figure 55.

DODT is continuously processed with synchronous ODT timing for the host interface DQ termination with no interruption at Power Down with IBT on Exit. Any read or write command issued in the first clock cycle after $t_{Fixedoutput}$ will be forwarded to the DRAMs and the associated data will be redriven by the MB. Since a fast MB may turn on receivers and forward signals as early as $t_{Fixedoutput}$(min) the host must not send any erroneous after $t_{Fixedoutput}$ min and the host must not send any valid commands before $t_{Fixedoutput}$(max) as a slow MB may not forward it.

8.2.2 Clock Stopped Power Down Mode

To support S3 Power Management mode, the MB supports a Clock Stopped Power Down mode. To maximize power saving, DDR3 MB Temperature Sensor operation is not supported during Clock Stopped Power Down mode. When both inputs CK_t and CK_c are being held LOW ($V_{IL\ (static)}$) or float (will eventually settle at LOW because of the (10K-100K Ohm) pull-down resistor in the CK_t/CK_c input buffer), the device stops operation and enters low-power static and standby operation. The corresponding timing requirement are shown in Figure 56, and Figure 57. The device will stop its PLL and floats all outputs except QACKE[3:0] and QBCKE[3:0], which must be kept driven LOW. The Clock Stopped Power Down mode can only be utilized once the DRAM received a self refresh command. In this state, the DRAM ignores all inputs except CKE. Hence, all MB outputs besides QxCKE[3:0] can be disabled.

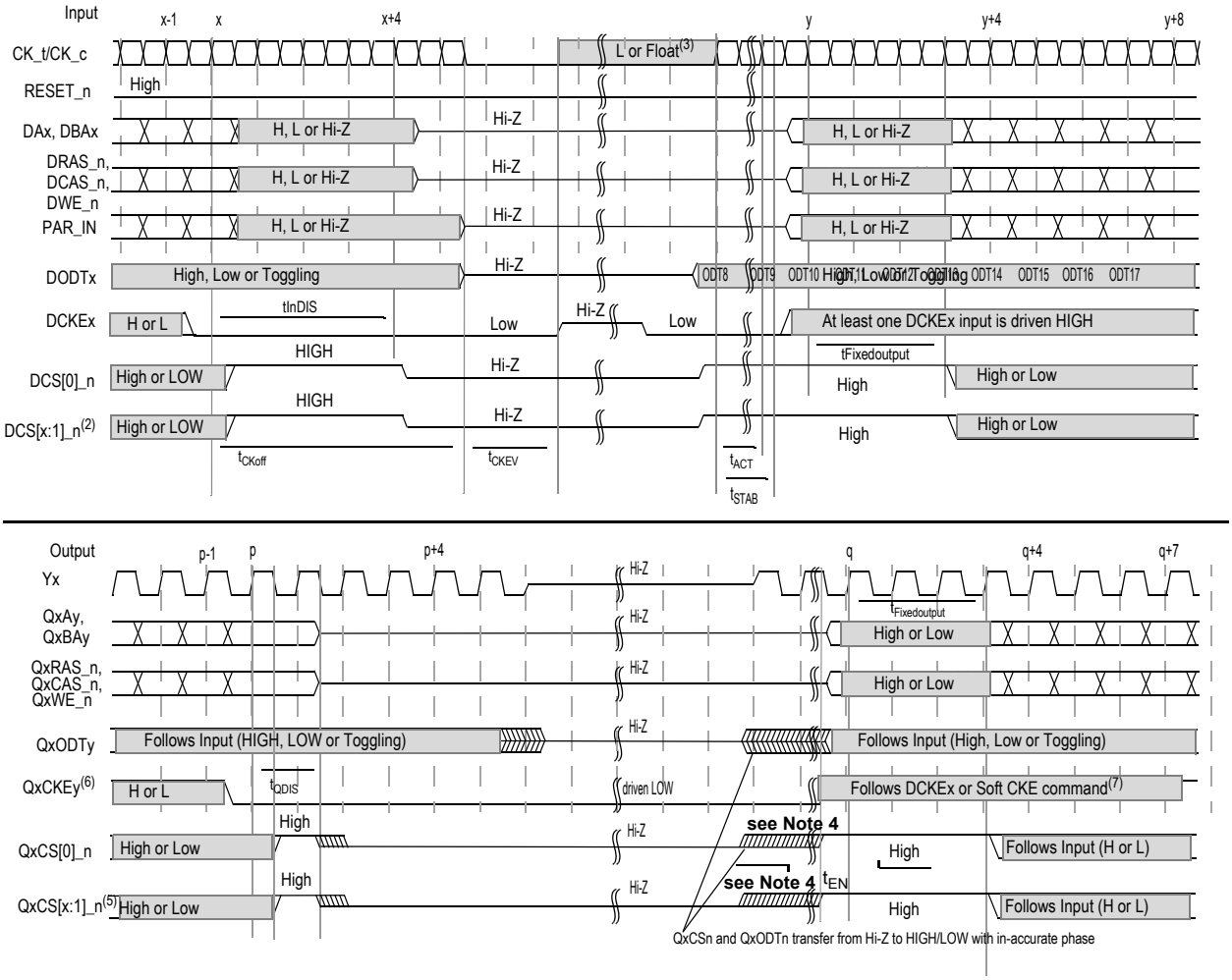
8.2.2.1 Clock Stopped Power Down Mode Entry

Upon entering Clock Stopped Power Down Mode, DDR3 MB must tri-state SDA output to prevent intermittent SMBus address failure (Optional Support - only if DDR3 MB supports Clock Stopped Power Down Mode). To enter Clock Stopped Power Down mode, the device will first enter CKE Power Down mode. Once in CKE Power Down mode, DCKEx will continue be de-asserted for a minimum of one tCKoff before pulling CK_t and CK_c LOW. After holding CK_t and CK_c LOW ($V_{IL\ (static)}$) for at least one tCKEV, both CK_t and CK_c can be floated (because of the 10K-100K Ohm pull-down resistor in the CK_t/CK_c input buffer, CK_t/CK_c will stay at LOW even though they are not being driven). The device is now in Clock Stopped Power Down mode. After CK_t and CK_c are pulled LOW, DCKEx will remain LOW for at least one tCKEV before it can float (if needed to be floated). At this point, all input receivers and input termination of the MB are disabled. The only active input circuits are CK_t and CK_c, which are required to detect the wake up request from the host.

1. x=1 if F0RC6 DA4:DA3='00', x = 3 if F0RC6 DA4:DA3='01'
2. If F0RC6 DA4='0'OR if F0RC6 DA4:DA3='10' AND last DCKEn H-->L transition was a SRE

8.2.2.2 Clock Stopped Power Down Mode Exit

DDR3 MB must reset SMBus state machine before exiting Clock Stopped Power Down Mode (Optional Support - only if DDR3 MB supports Clock Stopped Power Down Mode). To wake up the MB after entering Clock Stopped Power Down, the MB inputs DCS[1:0]_n must be driven to HIGH (to prevent accidental access to the control registers), and DCKEx to LOW. After that, a frequency and phase accurate input clock signal must be applied. Within tACT after CK_t and CK_c resumed normal operation, the device outputs start becoming a function of their corresponding inputs. The state of the DCS[x:0]_n inputs must not be changed before the end of tSTAB. If Clock Stopped Power Down mode had been entered from CKE Power Down with IBT off mode, the host interface DQ termination is disabled until the end of tSTAB and from then on works with synchronous timing. The input clock CK_t and CK_c must be stable for a time equal or greater than tSTAB before any access to the MB can take place. During PLL stabilization time (tSTAB), all DCSn signals need to be kept high. No DRAM command or control word write may take place. During PLL stabilization time (tSTAB), all DCKEx signals maintain their state.



(1) With RC9 DBA0='0'

(2) x = 3 for JEDEC standard DIMMs, x = 7 for non-JEDEC applications.

(3) When CK_t/CK_c inputs are floated, CK_t/CK_c inputs are pulled LOW by the (10K-100K Ohm) pulldown resistor in the CK_t/CK_c input buffer.

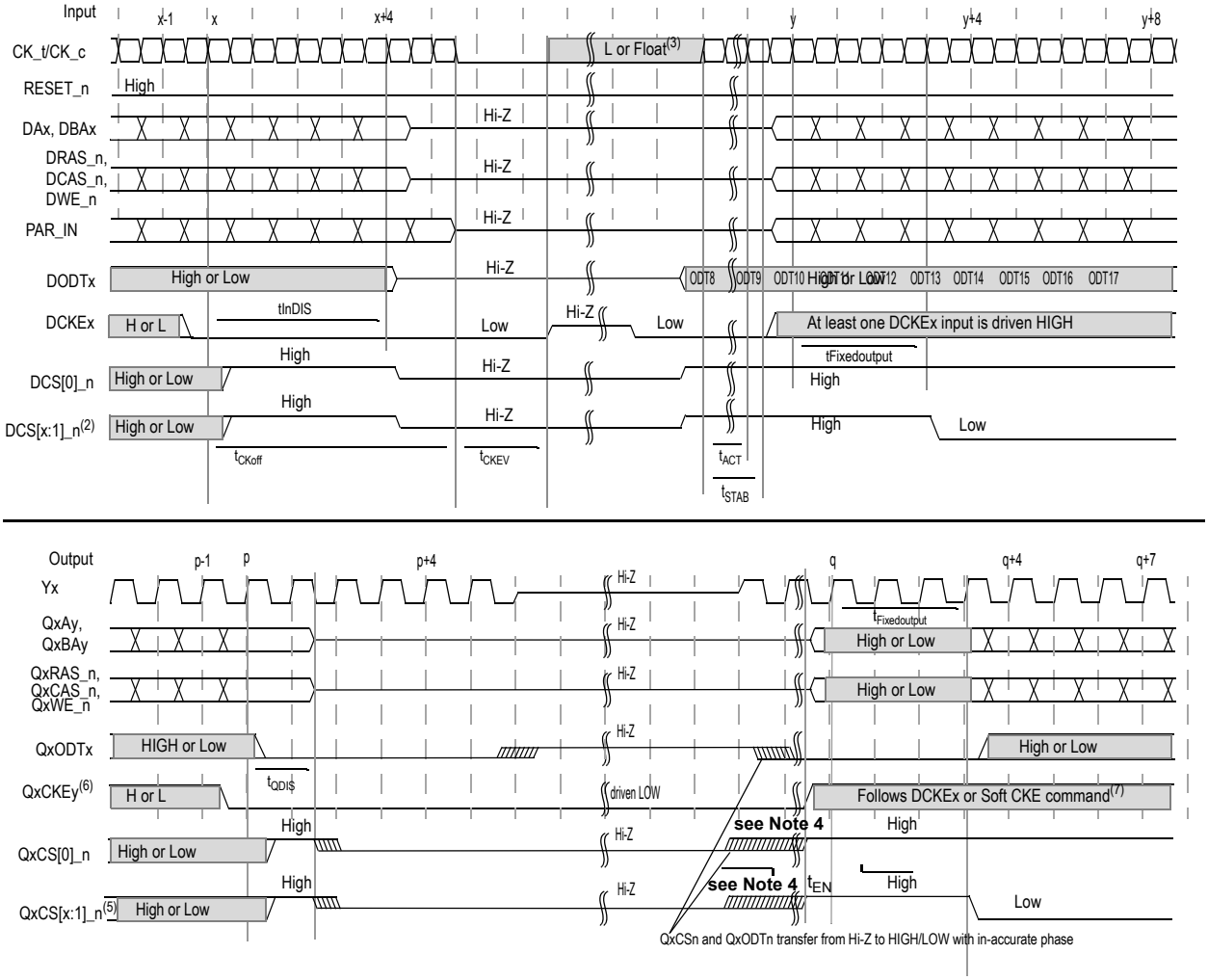
(4) Upon CKE Power Down exit, QxCSy_n will be held HIGH for maximum of 1 tCK regardless of what DCSx_n input level is. For all other operation QxCSy_n outputs will follow DCSx_n inputs.

(5) x = 3 for dual or quad-rank DIMMs, x =7 for octal rank DIMMs.

(6) DCKEx H-->L transition forwarded to QxCKEy if F0RC6 DA4='0' OR if F0RC6 DA4:DA3='10' AND SRE command present

(7) DCKEx L-->H transition forwarded to QxCKEy if F0RC6 DA4='0' OR if F0RC6 DA4:DA3='10' AND last DCKEn H-->L transition was a SRE

Figure 56 — Clock Stopped Power Down Entry and Exit with IBT On



(1) With RC9 DBA0='1'
(2) x = 3 for JEDEC standard DIMMs, x = 7 for non-JEDEC applications.
(3) When CK_t/CK_c inputs are floated, CK_t/CK_c inputs are pulled LOW by the (10K-100K Ohm) pulldown resistor in the CK_t/CK_c input buffer.
(4) Upon CKE Power Down exit, QxCSy_n will be held HIGH for maximum of 1 tCK regardless of what DCSx_n input level is. For all other operation QxCSy_n outputs will follow DCSx_n inputs.
(5) x = 3 for dual or quad-rank DIMMs, x =7 for octal rank DIMMs.
(6) DCKEx H-->L transition forwarded to QxCKEy if F0RC6 DA4='0' OR if F0RC6 DA4:DA3='10' AND SRE command present
(7) DCKEx L-->H transition forwarded to QxCKEy if F0RC6 DA4='0' OR if F0RC6 DA4:DA3='10' AND last DCKEn H-->L transition was a SRE

Figure 57 — Clock Stopped Power Down Entry and Exit with IBT Off

8.3 Dual Frequency Support

The MB supports operation at a second, i.e., lower than nominal, frequency as a means to save buffer and DRAM power when the memory bandwidth demand allows.

To enable fast frequency switching without the need for retraining every time the frequency is changed, the MB can be trained twice at two different frequencies at bootup time and retains register settings associated with each of the two frequencies. These two sets of register settings include internal timings, DRAM calibration status, etc as well as two different sets of configuration information from the SPD (programmed into the MB once at bootup time).

Switching between the two frequency contexts is achieved by writing to control word F0RC12 bit DBA1. DBA1=’0’ selects the default frequency context 1 while DBA1=’1’ selects frequency context 2.

Dual frequency training at bootup time requires selecting the appropriate frequency context, performing the training at that frequency and then selecting the other frequency context and performing the training at the other frequency. Subsequently, every time the operation frequency changes, the correct operating speed must be set in the MB via control word write to F0RC10 and the corresponding frequency context bit must be set in the MB via control word write to F0RC12, DBA1. The control word write to F0RC12, DBA1 must be the last access to the MB before the input frequency on the CK_t/CK_c pins changes. In addition the DRAMs must be put in self refresh mode before the frequency change occurs and the entire DDR3 DRAM frequency change procedure specified in JESD79-3 must be followed.

9 Control Words

The device features a set of control words, which allow the optimization of the device properties for different raw card designs. The different control words and settings are described below. Any change to these control words require some time for the device to settle. For changes to the control word setting, except for F[0]RC2 (bit DBA1 and DA3) and F[0]RC10, the controller needs to wait t_{MRD} after the last control word access, before further access to the DRAM can take place. For any changes to the clock timing (example: F[0]RC2: bit DBA1 and DA3, and F[0]RC10) this settling may take up to t_{STAB} time. All chip select inputs, DCS[n:0]_n, must be kept HIGH during that time. The Control Words can be accessed and written to when running within any one defined frequency band.

9.1 Control Word Decoding

The values to be programmed into each control word are presented on signals DA3, DA4, DBA0 and DBA1 simultaneously with the assertion of the control word access through DCS0_n and DCS1_n and the address of the control word on DA0, DA1, DA2 and DBA2.

Table 63 — Control Word Decoding

Control Word	Symbol	DCS[3:0]_n	DBA2	DA2	DA1	DA0	Definition
None	n/a	HXHX	X	X	X	X	No control word access
None	n/a	HXXH	X	X	X	X	
None	n/a	XHHX	X	X	X	X	
None	n/a	XHXH	X	X	X	X	
None	n/a	HLLL	X	X	X	X	Illegal input states[a]
None	n/a	LHLL	X	X	X	X	
None	n/a	LLHL	X	X	X	X	
None	n/a	LLLH	X	X	X	X	
none	n/a	LLHH	X	X	X	X	
none	n/a	LLLL	X	X	X	X	
Control Word	RCx	HHLL	X	X	X	X	Control Word Access

a. If DCS[3:2]_n are used as Address signals then all these combinations are valid legal states. Further three combinations HLLL, LHLL and LLLL are considered as Control Word Access.

The reset default state of all control word is “0”. Every time the device is reset, its default state is restored. Stopping the clocks (CK_t=CK_c=LOW) to put the device in lowpower mode will not alter the control word settings.

9.2 Control Words Overview Map

Table 64 — F[0] Control Word Decoding

Control Word	Symbol	DCS0_n	DCS1_n	DBA2	DA2	DA1	DA0	Definition
None	n/a	H	X	X	X	X	X	No control word access
None	n/a	X	H	X	X	X	X	No control word access
Control word 0	RC0	L	L	L	L	L	L	Global Features Control word
Control word 1	RC1	L	L	L	L	L	H	Clock Driver Enable Control word
Control word 2	RC2	L	L	L	L	H	L	Timing Control word
Control word 3	RC3	L	L	L	L	H	H	Address/Command & QCS_n Signals Driver Characteristics Control word
Control word 4	RC4	L	L	L	H	L	L	QxODT & QxCKE Signals Driver Characteristics Control word
Control word 5	RC5	L	L	L	H	L	H	CK Driver Characteristics Control word
Control word 6	RC6	L	L	L	H	H	L	CKE & ODT Management Control word
Control word 7	RC7	L	L	L	H	H	H	Function Select Control word
Control word 8	RC8	L	L	H	L	L	L	IBT & Vref Settings for Address, Command, Par_in
Control word 9	RC9	L	L	H	L	L	H	Power Saving Settings Control word
Control word 10	RC10	L	L	H	L	H	L	LRDIMM Operating Speed Control word
Control word 11	RC11	L	L	H	L	H	H	LRDIMM Operating voltage and Parity Calculation Control word
Control word 12	RC12	L	L	H	H	L	L	Training Control word
Control word 13	RC13	L	L	H	H	L	H	DIMM Configuration Control word
Control word 14	RC14	L	L	H	H	H	L	DRAM Configuration & DRAM Command Control word
Control word 15	RC15	L	L	H	H	H	H	Rank Multiplication Control word

Table 65 — F[1] Control Word Decoding

Control Word	Symbol	DCS0_n	DCS1_n	DBA2	DA2	DA1	DA0	Definition
None	n/a	H	X	X	X	X	X	No control word access
None	n/a	X	H	X	X	X	X	No control word access
Control word 0	RC0	L	L	L	L	L	L	IBT Settings for DCS_n Pins Control Word
Control word 1	RC1	L	L	L	L	L	H	IBT Settings for DCKE Pins Control Word
Control word 2	RC2	L	L	L	L	H	L	IBT Settings for DODT Pins Control Word
Control word 3	RC3	L	L	L	L	H	H	Reserved
Control word 4	RC4	L	L	L	H	L	L	Reserved
Control word 5	RC5	L	L	L	H	L	H	Reserved
Control word 6	RC6	L	L	L	H	H	L	Reserved
Control word 7	RC7	L	L	L	H	H	H	Function Select Control word
Control word 8	RC8	L	L	H	L	L	L	Optional - Extended Delay Control Word
Control word 9	RC9	L	L	H	L	L	H	Refresh Stagger
Control word 10	RC10	L	L	H	L	H	L	Refresh Stagger Limit
Control word 11	RC11	L	L	H	L	H	H	Optional - Extended Delay Control Word
Control word 12	RC12	L	L	H	H	L	L	Additive QCA Pre-launch Control Word
Control word 13	RC13	L	L	H	H	L	H	Additive QCS_n Delay Control Word
Control word 14	RC14	L	L	H	H	H	L	Additive QODT Delay Control Word
Control word 15	RC15	L	L	H	H	H	H	Additive QCKE Delay Control Word

9.2 Control Words Overview Map (cont'd)

Table 66 — F[2] Control Word Decoding

Control Word	Symbol	DCS0_n	DCS1_n	DBA2	DA2	DA1	DA0	Definition
None	n/a	H	X	X	X	X	X	No control word access
None	n/a	X	H	X	X	X	X	No control word access
Control word 0	RC0	L	L	L	L	L	L	Transparent Mode
Control word 1	RC1	L	L	L	L	L	H	Reset Control
Control word 2	RC2	L	L	L	L	H	L	SMBus Access Control
Control word 3	RC3	L	L	L	L	H	H	Training & Errout_n Control Word
Control word 4	RC4	L	L	L	H	L	L	MEMBIST Rank Control Word
Control word 5	RC5	L	L	L	H	L	H	DRAM Row & Column Addressing
Control word 6	RC6	L	L	L	H	H	L	MEMBIST Control
Control word 7	RC7	L	L	L	H	H	H	Function Select Control word
Control word 8	RC8	L	L	H	L	L	L	MEMBIST 8 bit ECC pattern
Control word 9	RC9	L	L	H	L	L	H	MEMBIST 8 bit ECC pattern
Control word 10	RC10	L	L	H	L	H	L	MEMBIST 16 bit ECC pattern
Control word 11	RC11	L	L	H	L	H	H	MEMBIST 16 bit ECC pattern
Control word 12	RC12	L	L	H	H	L	L	MEMBIST 32 bit ECC pattern
Control word 13	RC13	L	L	H	H	L	H	MEMBIST 32 bit ECC pattern
Control word 14	RC14	L	L	H	H	H	L	MEMBIST 32 bit ECC pattern
Control word 15	RC15	L	L	H	H	H	H	MEMBIST 32 bit ECC pattern

Table 67 — F[3] Control Word Decoding

Control Word	Symbol	DCS0_n	DCS1_n	DBA2	DA2	DA1	DA0	Definition
None	n/a	H	X	X	X	X	X	No control word access
None	n/a	X	H	X	X	X	X	No control word access
Control word 0	RC0	L	L	L	L	L	L	Connector Interface DQ RTT_Nom Termination Control Word
Control word 1	RC1	L	L	L	L	L	H	Connector Interface DQ RTT_WR Termination & Reference Voltage Control Word
Control word 2	RC2	L	L	L	L	H	L	Connector Interface DQ Driver Control Word
Control word 3	RC3	L	L	L	L	H	H	Reserved
Control word 4	RC4	L	L	L	H	L	L	Reserved
Control word 5	RC5	L	L	L	H	L	H	Reserved
Control word 6	RC6	L	L	L	H	H	L	Connector Interface Misc. Control Word
Control word 7	RC7	L	L	L	H	H	H	Function Select Control word
Control word 8	RC8	L	L	H	L	L	L	DRAM Interface MDQ Termination & Reference Voltage Control Word
Control word 9	RC9	L	L	H	L	L	H	DRAM Interface MDQ Driver Control Word
Control word 10	RC10	L	L	H	L	H	L	See Table 5 below
Control word 11	RC11	L	L	H	L	H	H	See Table 5 below
Control word 12	RC12	L	L	H	H	L	L	See Table 6 below
Control word 13	RC13	L	L	H	H	L	H	See Table 6 below
Control word 14	RC14	L	L	H	H	H	L	Reserved
Control word 15	RC15	L	L	H	H	H	H	Reserved

9.2 Control Words Overview Map (cont'd)

Table 68 — F[3-10] RC[10-11] Control Word Decoding

Control Word	Symbol	DCS0_n	DCS1_n	DBA2	DA2	DA1	DA0	Definition
Control word 10	RC10	L	L	H	L	H	L	Read QODT Control Words; F[3:10] = Rank[0:7] respectively
Control word 11	RC11	L	L	H	L	H	H	Write QODT Control Words; F[3:10] = Rank[0:7] respectively

Table 69 — F[3-11] RC[12-13] Control Word Decoding

Control Word	Symbol	DCS0_n	DCS1_n	DBA2	DA2	DA1	DA0	Definition
Control word 12	RC12	L	L	H	H	L	L	Reserved
Control word 13	RC13	L	L	H	H	L	H	Reserved

Table 70 — F[4-11] RC[0-9, 14-15] Control Word Decoding

Control Word	Symbol	DCS0_n	DCS1_n	DBA2	DA2	DA1	DA0	Definition
None	n/a	H	X	X	X	X	X	No control word access
None	n/a	X	H	X	X	X	X	No control word access
Control word 0	RC0	L	L	L	L	L	L	Reserved
Control word 1	RC1	L	L	L	L	L	H	Reserved
Control word 2	RC2	L	L	L	L	H	L	Reserved
Control word 3	RC3	L	L	L	L	H	H	Reserved
Control word 4	RC4	L	L	L	H	L	L	Reserved
Control word 5	RC5	L	L	L	H	L	H	Reserved
Control word 6	RC6	L	L	L	H	H	L	Reserved
Control word 7	RC7	L	L	L	H	H	H	Function Select Control Word
Control word 8	RC8	L	L	H	L	L	L	Reserved
Control word 9	RC9	L	L	H	L	L	H	Reserved
Control word 12	RC12	L	L	H	H	L	L	Reserved
Control word 13	RC13	L	L	H	H	L	H	Reserved
Control word 14	RC14	L	L	H	H	H	L	Reserved
Control word 15	RC15	L	L	H	H	H	H	Reserved

Table 71 — F[11] RC[10-11] Control Word Decoding

Control Word	Symbol	DCS0_n	DCS1_n	DBA2	DA2	DA1	DA0	Definition
Control word 10	RC10	L	L	H	L	H	L	Reserved
Control word 11	RC11	L	L	H	L	H	H	Reserved

9.2 Control Words Overview Map (cont'd)

Table 72 — F[12] Control Word Decoding

Control Word	Symbol	DCS0_n	DCS1_n	DBA2	DA2	DA1	DA0	Definition
None	n/a	H	X	X	X	X	X	No control word access
None	n/a	X	H	X	X	X	X	No control word access
Control word 0	RC0	L	L	L	L	L	L	Reserved
Control word 1	RC1	L	L	L	L	L	H	Reserved
Control word 2	RC2	L	L	L	L	H	L	Reserved
Control word 3	RC3	L	L	L	L	H	H	Reserved
Control word 4	RC4	L	L	L	H	L	L	Reserved
Control word 5	RC5	L	L	L	H	L	H	Reserved
Control word 6	RC6	L	L	L	H	H	L	Reserved
Control word 7	RC7	L	L	L	H	H	H	Function Select Control Word
Control word 8	RC8	L	L	H	L	L	L	Reserved
Control word 9	RC9	L	L	H	L	L	H	Reserved
Control word 10	RC10	L	L	H	L	H	L	Reserved
Control word 11	RC11	L	L	H	L	H	H	Reserved
Control word 12	RC12	L	L	H	H	L	L	Reserved
Control word 13	RC13	L	L	H	H	L	H	Reserved
Control word 14	RC14	L	L	H	H	H	L	Reserved
Control word 15	RC15	L	L	H	H	H	H	Reserved

Table 73 — F[13] Control Word Decoding

Control Word	Symbol	DCS0_n	DCS1_n	DBA2	DA2	DA1	DA0	Definition
None	n/a	H	X	X	X	X	X	No control word access
None	n/a	X	H	X	X	X	X	No control word access
Control word 0	RC0	L	L	L	L	L	L	Reserved
Control word 1	RC1	L	L	L	L	L	H	Reserved
Control word 2	RC2	L	L	L	L	H	L	Reserved
Control word 3	RC3	L	L	L	L	H	H	Reserved
Control word 4	RC4	L	L	L	H	L	L	Reserved
Control word 5	RC5	L	L	L	H	L	H	Reserved
Control word 6	RC6	L	L	L	H	H	L	Reserved
Control word 7	RC7	L	L	L	H	H	H	Function Select Control Word
Control word 8	RC8	L	L	H	L	L	L	Reserved
Control word 9	RC9	L	L	H	L	L	H	SMBus Function Select
Control word 10	RC10	L	L	H	L	H	L	LSB of Register Address Port
Control word 11	RC11	L	L	H	L	H	H	MSB of Register Address Port
Control word 12	RC12	L	L	H	H	L	L	Extended Address Port
Control word 13	RC13	L	L	H	H	L	H	Reserved
Control word 14	RC14	L	L	H	H	H	L	LSB of Register Data Port
Control word 15	RC15	L	L	H	H	H	H	MSB of Register Data Port

9.2 Control Words Overview Map (cont'd)

Table 74 — F[14] Control Word Decoding

Control Word	Symbol	DCS0_n	DCS1_n	DBA2	DA2	DA1	DA0	Definition
None	n/a	H	X	X	X	X	X	No control word access
None	n/a	X	H	X	X	X	X	No control word access
Control word 0	RC0	L	L	L	L	L	L	Vendor specific (lsb of Personality Byte 0)
Control word 1	RC1	L	L	L	L	L	H	Vendor specific (msb of Personality Byte 0)
Control word 2	RC2	L	L	L	L	H	L	Vendor specific (lsb of Personality Byte 1)
Control word 3	RC3	L	L	L	L	H	H	Vendor specific (msb of Personality Byte 1)
Control word 4	RC4	L	L	L	H	L	L	Vendor specific (lsb of Personality Byte 2)
Control word 5	RC5	L	L	L	H	L	H	Vendor specific (msb of Personality Byte 2)
Control word 6	RC6	L	L	L	H	H	L	Vendor specific (lsb of Personality Byte 3)
Control word 7	RC7	L	L	L	H	H	H	Function Select Control Word
Control word 8	RC8	L	L	H	L	L	L	Vendor specific (lsb of Personality Byte 4)
Control word 9	RC9	L	L	H	L	L	H	Vendor specific (msb of Personality Byte 4)
Control word 10	RC10	L	L	H	L	H	L	Vendor specific (lsb of Personality Byte 5)
Control word 11	RC11	L	L	H	L	H	H	Vendor specific (msb of Personality Byte 5)
Control word 12	RC12	L	L	H	H	L	L	Vendor specific (lsb of Personality Byte 6)
Control word 13	RC13	L	L	H	H	L	H	Vendor specific (msb of Personality Byte 6)
Control word 14	RC14	L	L	H	H	H	L	Vendor specific (lsb of Personality Byte 7)
Control word 15	RC15	L	L	H	H	H	H	Vendor specific (msb of Personality Byte 7)

Table 75 — F[15] Control Word Decoding

Control Word	Symbol	DCS0_n	DCS1_n	DBA2	DA2	DA1	DA0	Definition
None	n/a	H	X	X	X	X	X	No control word access
None	n/a	X	H	X	X	X	X	No control word access
Control word 0	RC0	L	L	L	L	L	L	Vendor specific (lsb of Personality Byte 8)
Control word 1	RC1	L	L	L	L	L	H	Vendor specific (msb of Personality Byte 8)
Control word 2	RC2	L	L	L	L	H	L	Vendor specific (lsb of Personality Byte 9)
Control word 3	RC3	L	L	L	L	H	H	Vendor specific (msb of Personality Byte 9)
Control word 4	RC4	L	L	L	H	L	L	Vendor specific (lsb of Personality Byte 10)
Control word 5	RC5	L	L	L	H	L	H	Vendor specific (msb of Personality Byte 10)
Control word 6	RC6	L	L	L	H	H	L	Vendor specific (msb of Personality Byte 3)
Control word 7	RC7	L	L	L	H	H	H	Function Select Control Word
Control word 8	RC8	L	L	H	L	L	L	Vendor specific (lsb of Personality Byte 11)
Control word 9	RC9	L	L	H	L	L	H	Vendor specific (msb of Personality Byte 11)
Control word 10	RC10	L	L	H	L	H	L	Vendor specific (lsb of Personality Byte 12)
Control word 11	RC11	L	L	H	L	H	H	Vendor specific (msb of Personality Byte 12)
Control word 12	RC12	L	L	H	H	L	L	Vendor specific (lsb of Personality Byte 13)
Control word 13	RC13	L	L	H	H	L	H	Vendor specific (msb of Personality Byte 13)
Control word 14	RC14	L	L	H	H	H	L	Vendor specific (lsb of Personality Byte 14)
Control word 15	RC15	L	L	H	H	H	H	Vendor specific (msb of Personality Byte 14)

9.3 Function 0 Control Word Registers

Table 76 — F[0]RC0: Global Features Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Output Inversion	Output Inversion enabled
x	x	x	1		Output Inversion disabled
x	x	0	x	Output Weak Drive	Disable output weak drive
x	x	1	x		Enable output weak drive; 70 Ohm min; 100 Ohm max
x	0	x	x	QVrefCA Output	Default; Enable; Drive valid and stable VrefCA
x	1	x	x		Disable and floating
0	x	x	x	QVrefDQ Output	Default; Enable; Drive valid and stable VrefDQ
1	x	x	x		Disable and floating

Output weak drive refers to allowing many A/B outputs to enter a state of higher output impedance when they are not being used. This is to conserve power when the outputs are resistively terminated to a voltage e.g., VTT.

Table 77 — F[0]RC1: Clock Driver Enable Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Disable Y0_t/Y0_c clock	Y0_t/Y0_c clock enabled
x	x	x	1		Y0_t/Y0_c clock disabled
x	x	0	x	Disable Y1_t/Y1_c clock	Y1_t/Y1_c clock enabled
x	x	1	x		Y1_t/Y1_c clock disabled
x	0	x	x	Disable Y2_t/Y2_c clock	Y2_t/Y2_c clock enabled
x	1	x	x		Y2_t/Y2_c clock disabled
0	x	x	x	Disable Y3_t/Y3_c clock	Y3_t/Y3_c clock enabled
1	x	x	x		Y3_t/Y3_c clock disabled

Output clocks may be individually turned on or off to conserve power. The system must read the module SPD to determine which clock outputs are used by the module. The PLL remains locked on CK_t/CK_c unless the system stops the clock inputs to the MB to enter the lowest power mode.

9.3 Function 0 Control Word Registers (cont'd)

Table 78 — F[0]RC2: Timing Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Address and command nets pre-launch (Control Signals QxCKE, QxCS_n, QxODT are controlled by F[1] RC[8,11,13,14,15]	Standard (1/2 Clock)
x	x	x	1		Address and command nets pre-launch controlled by F[1] RC[8,12]
x	x	0	x	Rank 1 and Rank 5 Swap[a]	Default; Disable - No Swap between Rank 1 and Rank 5. Rank 1 = QACS[1]_n; Rank 5 = QBCS[1]_n
x	x	1	x		Enable - Swap Rank 1 and Rank 5. Rank 1 = QBCS[1]_n; Rank 5 = QACS[1]_n
x	0	x	x	Reserved	Reserved
x	1	x	x		Reserved
0	x	x	x	Frequency Band Select	Operation (Frequency Band 1)
1	x	x	x		Test Mode (Frequency Band 2)

a. Host BIOS is responsible for configuring this bit based on DIMM type. DIMM SPD indicates whether DIMM has swapped Rank 1 and Rank 5. Typically, this bit is used for 8 Rank x8 DIMM configuration.

Output driver characteristics are separately controlled for buffer Address/Command and all control outputs. These outputs are grouped as following and also seen in the tables that follow:

Address/Command Signals: QxAn, QxBAn, QxRAS_n, QxCAS_n, QxWE_n

Chip Select Control Signals: QxCS_n

Clock Enable Control Signals: QxCKEn

On Die Termination Control Signals: QxODTn

Clock Signals = Yn_t, Yn_c

Table 79 — F[0]RC3: Address/Command & QxCS_n Signals Driver Characteristics Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Address/Command - QxAn, QxBAn, QxRAS_n, QxCAS_n, QxWE_n Outputs	Light Drive (8 to 10 DRAM Loads)
x	x	0	1		Moderate Drive (16 to 20 DRAM Loads)
x	x	1	0		Strong Drive (32 to 40 DRAM Loads)
x	x	1	1		Very Strong Drive (64 to 80 DRAM Loads)
0	0	x	x	QxCS[3:0]_n Outputs	Light Drive (8 to 10 DRAM Loads)
0	1	x	x		Moderate Drive (16 to 20 DRAM Loads)
1	0	x	x		Strong Drive (32 to 40 DRAM Loads)
1	1	x	x		Reserved

9.3 Function 0 Control Word Registers (cont'd)

Table 80 — F[0]RC4: QxODT & QxCKE Signals Driver Characteristics Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	QxODT[1:0] Outputs	Light Drive (8 to 10 DRAM Loads)
x	x	0	1		Moderate Drive (16 to 20 DRAM Loads)
x	x	1	0		Strong Drive (32 to 40 DRAM Loads)
x	x	1	1		Reserved
0	0	x	x	QxCKE[3:0] Outputs	Light Drive (8 to 10 DRAM Loads)
0	1	x	x		Moderate Drive (16 to 20 DRAM Loads)
1	0	x	x		Strong Drive (32 to 40 DRAM Loads)
1	1	x	x		Reserved

Table 81 — F[0]RC5: CK Driver Characteristics Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Clock Y1_t, Y1_c, Y3_t, and Y3_c Output Drivers (A side)	Light Drive (8 to 10 DRAM Loads)
x	x	0	1		Moderate Drive (16 to 20 DRAM Loads)
x	x	1	0		Strong Drive (32 to 40 DRAM Loads)
x	x	1	1		Reserved
0	0	x	x	Clock Y0_t, Y0_c, Y2_t, and Y2_c Output Drivers (B side)	Light Drive (8 to 10 DRAM Loads)
0	1	x	x		Moderate Drive (16 to 20 DRAM Loads)
1	0	x	x		Strong Drive (32 to 40 DRAM Loads)
1	1	x	x		Reserved

9.3 Function 0 Control Word Registers (cont'd)

Table 82 — F[0]RC6: CKE and ODT Management Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
0	x	0	0	4 QxCKE outputs are controlled by 2 DCKE inputs	Default: DCKE[0] --> QxCKE[0] and QxCKE[2][a] DCKE[1] --> QxCKE[1] and QxCKE[3][a]
0	x	0	1	4 QxCKE outputs are controlled by 4 DCKE inputs	DCKE[0] --> QxCKE[0] DCKE[1] --> QxCKE[1] DCKE[2] --> QxCKE[2] DODT[1]/DCKE[3][a] --> QxCKE[3]
0	x	1	0	4 QxCKE outputs are controlled independent of 2 DCKE inputs: Buffer only asserts or de-asserts QxCKE[x] Ranks that is specified by Host.	See Table 18 for details
0	x	1	1	Reserved	Reserved
0	0	x	x	Connector Interface DODT Control	Default: Buffer only evaluates DODT[0]
0	1	x	x		Buffer evaluates DODT[0] & DODT[1]/DCKE[3][b]
0	x	x	x	QxCKE Control	Default; DCKE0, DCKE1 inputs to the QxCKE outputs are controlled by F[0] RC6 DA4, DA3
1	x	x	x		QxCKE0 = DCKE0 + DCKE1[a]

a. In 2 Rank case, buffer tri-states QxCKE[2] and QxCKE[3] outputs.
b. In 4 DCKE mode (DA4:DA3='01', DODT[1]/DCKE[3] pin will be used as DCKE[3]. In all other cases, the pin will be used as DODT[1] if DBA0 = 1 otherwise DODT1 pin is not used and it may be tri-stated and buffer turns off IBT for DODT1. Additionally in 4 DCKE mode (DA4:DA3 = 01b, bit DBA0 must be 0b.
c. F[0] RC6 DA4, DA3 must be configured to 00b. QxCKE[3:1] outputs are floating.

9.3 Function 0 Control Word Registers (cont'd)

Table 83 — Host - Buffer Interface Command Definition[a,b]

Function	CS_n	RAS_n	CAS_n	WE_n	BA[2:0]	A15	A14	A13	A[12:11]	A10	A[9:8]	A[7:4]	A[3:0]
ZQCL	L	H	H	L	x	0	0	0	x	H	x	x	x
ZQCS					x	0	0	0	x	L	x	x	x
CKE Control[c]					x	0	0	1	x	x	x	x	QxCKE[3:0][d,e]
RSVD					x	0	1	0	x	x	x	x	x
RSVD					x	0	1	1	x	x	x	x	x
RSVD					x	1	0	0	x	x	x	x	x
RSVD					x	1	0	1	x	x	x	x	x
RSVD					x	1	1	0	x	x	x	x	x
RSVD					x	1	1	1	x	x	x	x	x

a. This definition only applies when F[0]RC6: DA4:DA3 = 10b

b. In F[0]RC6: DA4:DA3 = 10b mode, Self Refresh Entry command and Self Refresh Exit command is a broadcast command. Self Refresh Entry command & Self Refresh Exit command is not Rank accessible by host memory controller. Buffer de-asserts QxCKE[x] to all Ranks associated with DCKE[x] when it receives a Self Refresh Entry command. Buffer asserts QxCKE[x] to all Ranks associated with DCKE[x] when it receives a Self Refresh Exit command.

c. For CKE control command (Soft CKE command), buffer does not forward DCKE transitions (either high to low transition for power down entry or low to high transition for power down exit) on its QxCKE outputs. Further buffer does not forward DCSn_n inputs on its QxCSn_n outputs and QxCSn_n outputs are not asserted.

d. A[3:0] during CKE control command:
0 =de-assert corresponding QxCKE low for Power Down Entry command
1 = assert corresponding QxCKE high for Power Down Exit command.

e. Host controller is responsible for putting all ranks behind buffer in Power down mode via Soft CKE command before putting buffer into CKE power down mode. Host controller is not allowed to put half number of Ranks on LRDIMM in Power down mode and remaining other half number of Ranks on LRDIMM in Self Refresh mode when putting buffer into CKE power down mode. All Ranks on LRDIMM must be either in Power Down mode or Self Refresh mode when buffer enters into CKE power down mode.

9.3 Function 0 Control Word Registers (cont'd)

Table 84 — F[0]RC7: Function Select Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
0	0	0	0	Selects a bank of additional registers in the extended register space	RC0-6, 8-15=F[0]RC0-6, 8-15, SSTE32882 compatible function space
0	0	0	1		RC0-6, 8-15=F[1]RC0-6, 8-15, CA+Ctrl path for buffer
0	0	1	0		RC0-6, 8-15=F[2]RC0-6, 8-15, CA+Ctrl path for buffer
0	0	1	1		RC0-6, 8-15=F[3]RC0-6, 8-15, DQ extensions for buffer
0	1	0	0		RC0-6, 8-15=F[4]RC0-6, 8-15, DQ extensions for buffer
0	1	0	1		RC0-6, 8-15=F[5]RC0-6, 8-15, DQ extensions for buffer
0	1	1	0		RC0-6, 8-15=F[6]RC0-6, 8-15, DQ extensions for buffer
0	1	1	1		RC0-6, 8-15=F[7]RC0-6, 8-15, DQ extensions for buffer
1	0	0	0		RC0-6, 8-15=F[8]RC0-6, 8-15, DQ extensions for buffer
1	0	0	1		RC0-6, 8-15=F[9]RC0-6, 8-15, DQ extensions for buffer
1	0	1	0		RC0-6, 8-15=F[10]RC0-6, 8-15, DQ extensions for buffer
1	0	1	1		RC0-6, 8-15=F[11]RC0-6, 8-15, DQ extensions for buffer
1	1	0	0		Reserved
1	1	0	1		Reserved
1	1	1	0		Vendor specific
1	1	1	1		Vendor specific

Table 85 — F[0]RC8 - IBT Setting Control Word for Address, Command & PAR_IN Signal & Input reference voltage setting for Address, Command, Control & Parity inputs

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	Input Bus Termination for DAn, DBAn, DRAS_n, DCAS_n, DWE_n and PAR_IN	100 Ohm
x	0	0	1		150 Ohm
x	0	1	0		200 Ohm
x	0	1	1		300 Ohm
x	1	0	0		Reserved
x	1	0	1		Reserved
x	1	1	0		Reserved
x	1	1	1		Off[a]
0	x	x	x	Vref for DAn, DBAn, DRAS_n, DCAS_n, DWE_n and PAR_IN, DCSn_n, DCKEn, DODTn	Default; Use VrefCA input pin for receiver reference voltage
1	x	x	x		Use internally generated Vref for receiver reference voltage

a. With this setting, IBT on all inputs are turned off. IBT setting for DCSn_n, DCKEn and DODTn is controlled by control words F[1]RC0, F[1]RC1 and F[1]RC2 respectively.

9.3 Function 0 Control Word Registers (cont'd)

Table 86 — F[0]RC9: Power Saving Settings Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Reserved	Reserved
x	x	x	1		Reserved
1	x	0	x	Output Clock Disable in CKE Power Down Mode	Y clocks stay active in CKE power down
1	x	1	x		Y clocks disabled in CKE power down
1	0	x	x	CKE Power Down Mode	CKE power down with IBT ON, DQS RTT enabled
1	1	x	x		CKE power down with IBT off, DQS RTT disabled
0	x	x	x	CKE Power Down Mode Enable	Disabled
1	x	x	x		Enabled

The MB supports different power down modes. By default, the Power Down feature is disabled (RC9[DBA1]=0). The MB ignores CKE Power Down mode setting when this function is disabled. If the CKE Power Down mode is enabled (RC9[DBA1]=1), then power down is invoked once both DCKE0 and DCKE1 are LOW. Bit DBA0 selects how IBT and DQS RTT behave.

Table 87 — F[0]RC10: Encoding for LRDIMM Operating Speed

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	f ≤ 800 MT/s	DDR3/DDR3L-800 (default)
x	0	0	1	800 MTS < f ≤ 1066 MT/s	DDR3/DDR3L-1066
x	0	1	0	1066 MTS < f ≤ 1333 MT/s	DDR3/DDR3L-1333
x	0	1	1	1333 MTS < f ≤ 1600 MT/s	DDR3/DDR3L-1600
x	1	0	0	1600 MTS < f ≤ 1866 MT/s	DDR3/DDR3L-1866
x	1	0	1	1866 MTS < f ≤ 2133 MTs	DDR3/DDR3L-2133
x	1	1	0	Reserved	Reserved
x	1	1	1	Reserved	Reserved
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

NOTE The encoding value is used to inform the MB the operating speed that it is being run at in a system. It is not an indicator of how fast or slow a MB can run.

9.3 Function 0 Control Word Registers (cont'd)

F[0]RC11 is used to inform the MB under what operating voltage V_{DD} will be used. MB can use the information to optimize their functionality and performance at DDR3L conditions.

Table 88 — F[0]RC11: Operating Voltage & Parity Calculation Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	MB VDD Operating Voltage	DDR3 1.5V (default)
x	x	0	1		DDR3L 1.35V mode[a]
x	x	1	0		Reserved
x	x	1	1		Reserved
0	0	x	x	Parity Calculation	OFF[b]
0	1	x	x		A[15:0], BA[2:0], RAS_n, CAS_n, WE_n
1	0	x	x		A[17:0], BA[2:0], RAS_n, CAS_n, WE_n[c]
1	1	x	x		Reserved

a. DDR3L 1.35V MB is backward compatible and operable to DDR3 1.5V specification. To guarantee all timings and specification for DDR3 1.5V, the MB must be configured with F[0]RC11[DA4:DA3]=00b.
b. Buffer does not check for parity including control word programming commands.
c. This setting is independent from the setting in F0RC15. It is the host's responsibility to program F0RC11 and F0RC15 to compatible settings.

Table 89 — F[0]RC12 Training Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	Training Control	Normal operating mode[a]
x	0	0	1		Connector DQ interface write leveling
x	0	1	0		Start DRAM interface training[b]
x	0	1	1		Reserved for vendor specific debug
x	1	0	0		Reserved for vendor specific debug
x	1	0	1		Reserved for vendor specific debug
x	1	1	0		Reserved for vendor specific debug
x	1	1	1		Reserved for vendor specific debug
0	x	x	x	Context for operation training	Default; Context 1 operation and storage of DRAM interface calibration values to CSRs
1	x	x	x		Context 2 operation and storage of DRAM interface calibration values to CSRs

a. Buffer stops driving Errout_n Low when training had an error. Buffer stops training if it was previously started and will stop driving Errout_n Low. Buffer resets Fail and Valid bit in F2 RC3.
b. Buffer starts driving Errout_n Low 20 clocks after receiving this command.

9.3 Function 0 Control Word Registers (cont'd)

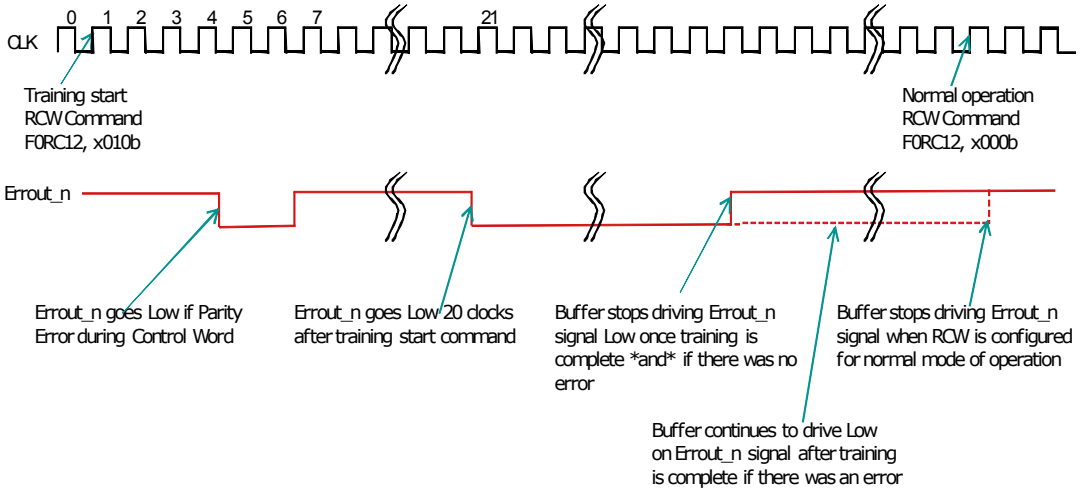


Figure 58 — Errout_n Signal During DDR3 MB Training

Table 90 — F[0]RC13 DIMM Configuration Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Number of physical Ranks - Post MB[a]	Default; 8 Ranks; QCS[7:0]_n
x	x	0	1		4 Ranks; QCS[3:0]_n
x	x	1	0		2 Ranks; QCS[1:0]_n
x	x	1	1		1 Rank; QCS[0]_n
0	0	x	x	Number of logical Ranks[a]	Buffer evaluates DCS[0]_n
0	1	x	x		Buffer evaluates DCS[1:0]_n
1	0	x	x		Buffer evaluates DCS[3:0]_n
1	1	x	x		Buffer evaluates DCS[7:0]_n

a. Host controller must configure F[0] RC13 and F[0] RC15 properly for normal operation. It is illegal to have default power up setting of 0000b in F[0] RC13 and F[0] RC15 at the same time for normal operation.

9.3 Function 0 Control Word Registers (cont'd)

Table 91 — F[0]RC14: DRAM Configuration & DRAM Command Control Word

Input				Definition	Encoding
DBA1	DBA0[1]	DA4[1]	DA3		
x	x	x	0	Address Mirror control for MRS commands	Disabled
x	x	x	1		Enabled. Buffer mirrors Address for ODD physical ranks.[2]
x	x	0	x	DRAM Refresh, Precharge single & Precharge All Command Control	Default.Precharge single and Precharge All command is broadcast to all physical ranks associated with a logical Rank as specified in F[0]RC13. Refresh command is broadcast command to all physical ranks associated with a logical Rank as specified in F[0]RC13 only when F[1]RC9 = 0000b (default). Otherwise Refresh command is staggered as specified in F[1]RC9.
x	x	1	x		Refresh, Precharge single and Precharge[a] All command is issued to a specific physical rank as specified by the host using the Rank multiplication addressing method specified in F[0]RC15.
x	0	x	x	DRAM MRS Control	Default. MRS command is broadcast to all physical ranks associated with a logical Rank as specified in F[0]RC13
x	1	x	x		MRS command is issued to a specific physical rank as specified by the host using the Rank multiplication addressing method specified in F[0]RC15[b]
0	x	x	x	DRAM Bus Width	x4
1	x	x	x		x8

a. Buffer evaluates address bit A0 for Precharge Single and Precharge All command. If A0=0, buffer steers Precharge Single and Precharge All command to a Rank specified by host as defined in F[0]RC15. If A0=1, buffer broadcasts Precharge Single and Precharge All command to all physical ranks associated with a logical rank.
b. Buffer evaluates address bit A13 for MRS command. If A13=0, buffer passes MRS command to a Rank specified by host as defined in F[0]RC15. If A13=1, buffer broadcasts MRS command to all physical ranks associated with a logical rank.

NOTE 1 Bit DA4 and DBA0 setting is only applicable in Rank multiplication mode as selected in F[0]RC15. In normal mode of operation (F[0]RC15 bits DBA1, DBA0, DA4, DA3 = '0000'b, F[0]RC14 bits DA4 and DBA0 do not apply and must be configured as '0'b.

NOTE 2 This is only applicable when Buffer executes MRS command on its own under training for its DRAM interface. Host memory controller is still responsible for Address Mirror when it issues MRS command under DRAM initialization phase as well as normal mode of operation.

9.3 Function 0 Control Word Registers (cont'd)

Table 92 — F[0]RC15: Rank Multiplication Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
0	0	0	0	Defines Rank select bits[a]	Normal operating mode
0	0	0	1		A[14]; 2x multiplication, 1 Gbit DDR3 SDRAM
0	0	1	0		A[15]; 2x multiplication, 2 Gbit DDR3 SDRAM
0	0	1	1		A[16]; 2x multiplication, 4 Gbit DDR3 SDRAM
0	1	0	0		Reserved
0	1	0	1		A[15:14]; 4x multiplication, 1 Gbit DDR3 SDRAM
0	1	1	0		A[16:15]; 4x multiplication, 2 Gbit DDR3 SDRAM
0	1	1	1		A[17:16]; 4x multiplication, 4 Gbit DDR3 SDRAM
1	0	0	0		Reserved
1	0	0	1		Reserved
1	0	1	0		Reserved
1	0	1	1		Reserved
1	1	0	0		Reserved
1	1	0	1		Reserved
1	1	1	0		Reserved
1	1	1	1		Reserved

a. Host controller must configure F[0] RC13 and F[0] RC15 properly for normal operation. It is illegal to have default power up setting of 0000b in F[0] RC13 and F[0] RC15 at the same time for normal operation.

Address pin to Chip Select pin mapping:

A16 <--> CS2_n

A17 <--> CS3_n

Buffer operation of DRAM commands in Rank Multiplication mode is as following:

Refresh command, MRS command, Precharge Single command, Precharge All command - As defined in F[0]RC14.

ZQ calibration command (both ZQCL and ZQCS), NOP command - Buffer broadcasts these commands to all physical ranks associated with a logical rank.

Self Refresh Entry command, Self Refresh Exit command - Buffer broadcasts these commands to all physical ranks associated with a given DCKEx. For additional description, see F[0]RC6; bit DA4:DA3 = 10b setting note.

Activate command, Read command, Write command, Read w/ AP command, Write w/ AP command - Activate command is as defined in Host to DRAM CS mapping table below. Upon receiving an Activate command to a given rank from host memory controller, buffer internally stores the DRAM bank information for that Rank and passes that Activate command to appropriate rank. Buffer allows maximum of only one row open per Bank across all physical ranks on a given logical rank. Buffer does not allow to open the same DRAM bank across all physical ranks behind the buffer on a given logical rank.When buffer receives a Read or Write or Read w/ AP or Write w/AP command, it uses the internally stored bank information to pass that command to appropriate rank. Buffer does not require or look at the Rank bits for Read or Write or Read w/ AP or Write w/AP command.

Deselect command - Buffer maintains its address, command & control signals in its previous state. It does not pass any commands to any ranks.

Power down entry command & Power down exit command - As defined in F0RC6.

9.4 Function 1 Control Word Registers

Table 93 — F[1] RC0: IBT Settings for DCS_n Pins Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	Input Bus Termination DCS[1:0]_n and DCS[3:2]_n[a]	100 Ohm
x	0	0	1		150 Ohm
x	0	1	0		200 Ohm
x	0	1	1		300 Ohm
x	1	0	0		Reserved
x	1	0	1		Reserved
x	1	1	0		Reserved
x	1	1	1		Off[b]
0	x	x	x	Input Bus Termination DCS[3:2]_n	IBT as defined in F[1] RC0
1	x	x	x		IBT as defined in F[0] RC8

a. If F[1] RC0 DBA1 =0
b. With this setting, IBT on all DCS_n inputs are turned Off.

Table 94 — F[1] RC1: IBT Settings for DCKE Pins Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	Input Bus Termination DCKE[1:0] and DCKE[3:2][a]	100 Ohm
x	0	0	1		150 Ohm
x	0	1	0		200 Ohm
x	0	1	1		300 Ohm
x	1	0	0		Reserved
x	1	0	1		Reserved
x	1	1	0		Reserved
x	1	1	1		Off[b]
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

a. If F[0]RC6 DA4, DA3 = 01b.
b. With this setting, IBT on all DCKE inputs are turned Off.

9.4 Function 1 Control Word Registers (cont'd)

Table 95 — F[1] RC2: IBT Settings for DODT Pins Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	Input Bus Termination DODT[1:0][a]	100 Ohm
x	0	0	1		150 Ohm
x	0	1	0		200 Ohm
x	0	1	1		300 Ohm
x	1	0	0		Reserved
x	1	0	1		Reserved
x	1	1	0		Reserved
x	1	1	1		Off[b]
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

a. Applies to DODT1 only if F[0]RC6 DBA0=1; otherwise IBT on DODT1 is off.
b. With this setting, IBT on all DODT inputs are turned Off.

Table 96 — F[1] RC[3:6] Reserved

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Reserved	Reserved
x	x	0	1		
x	x	1	0		
x	x	1	1		
x	0	x	x	Reserved	Reserved
x	1	x	x		
0	x	x	x		
1	x	x	x		

Table 97 — F[1] RC7: Function Select Control Word (See F[0]RC7 for definition)

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x		

9.4 Function 1 Control Word Registers (cont'd)

Table 98 — F[1] RC8 Extended Delay Control Word - Optional

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Total Y delay = Y Delay (F[1]RC12)+YDextended	YDextended = 0. No addition to Y Delay
x	x	0	1		YDextended = (1/128)*tCK
x	x	1	0		YDextended = (2/128)*tCK
x	x	1	1		YDextended = (3/128)*tCK
0	0	x	x	Total QCS delay = QCS Delay (F[1]RC13)+QCS-Dextended	QCSDextended = 0. No addition to QCS Delay
0	1	x	x		QCSDextended = (1/128)*tCK
1	0	x	x		QCSDextended = (2/128)*tCK
1	1	x	x		QCSDextended = (3/128)*tCK

Table 99 — F[1] RC9 - Refresh Stagger[a]

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
0	0	0	0	Ref_Stagger = 0 clocks (Broadcast refresh command to all ranks on the same clock)	This setting can disable the timers.
0	0	0	1	Ref_Stagger = 20 clocks	
0	0	1	0	Ref_Stagger = 30 clocks	
0	0	1	1	Ref_Stagger = 40 clocks	
0	1	0	0	Ref_Stagger = 60 clocks	
0	1	0	1	Ref_Stagger = 80 clocks	
0	1	1	0	Ref_Stagger = 100 clocks	
0	1	1	1	Ref_Stagger = 120 clocks	
1	x	x	x	Reserved	

a. This control word is only applicable when F[0]RC14 bit DA4 = 0b.

9.4 Function 1 Control Word Registers (cont'd)

Table 100 — F[1] RC10 - Refresh Stagger Limit[a]

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	Ref_Jitter_Limit = unlimited	
x	0	0	1	Ref_Jitter_Limit = 10 clocks	
x	0	1	0	Ref_Jitter_Limit = 20 clocks	
x	0	1	1	Ref_Jitter_Limit = 30 clocks	
x	1	0	0	Ref_Jitter_Limit = 40 clocks	
x	1	0	1	Ref_Jitter_Limit = 60 clocks	
x	1	1	0	Ref_Jitter_Limit = 80 clocks	
x	1	1	1	Undefined	
0	x	x	x	Always start with lowest numbered rank.	
1	x	x	x	Start rank is the rank after the last refresh (start rank only changes if a refresh was missed)	

a. This control word is only applicable when F[0]RC14 bit DA4 = 0b.

Table 101 — F[1] RC11 Extended Delay Control Word - Optional

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Total QODT delay = QODT delay (F[1]RC14) + QODT Dextended	QODTDextended = 0. No addition to QODT delay
x	x	0	1		QODTDextended = (1/128)*tCK
x	x	1	0		QODTDextended = (2/128)*tCK
x	x	1	1		QODTDextended = (3/128)*tCK
0	0	x	x	Total QCKE delay = QCKE Delay (F[1]RC15)+QCKE-Dextended	QCKEDextended = 0. No addition to QCKE Delay
0	1	x	x		QCKEDextended = (1/128)*tCK
1	0	x	x		QCKEDextended = (2/128)*tCK
1	1	x	x		QCKEDextended = (3/128)*tCK

9.4 Function 1 Control Word Registers (cont'd)

Table 102 — F[1] RC12: Additive QCA Pre-launch Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	Delay Y	Delay Y by (8/32)*tCK (QCA prelaunch = 0.75 tCK, n=8)[a]
x	0	0	1		Delay Y by (7/32)*tCK (QCA prelaunch = 0.71875 tCK, n=7)
x	0	1	0		Delay Y by (6/32)*tCK (QCA prelaunch = 0.6875 tCK, n=6)
x	0	1	1		Delay Y by (5/32)*tCK (QCA prelaunch = 0.65625 tCK, n=5)
x	1	0	0		Delay Y by (4/32)*tCK (QCA prelaunch = 0.625 tCK, n=4)
x	1	0	1		Delay Y by (3/32)*tCK (QCA prelaunch = 0.59375 tCK, n=3)
x	1	1	0		Delay Y by (2/32)*tCK (QCA prelaunch = 0.5625 tCK, n=2)
x	1	1	1		Delay Y by (1/32)*tCK (QCA prelaunch = 0.53125 tCK, n=1)
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

a. If F[0]RC2 DA3=1.

Table 103 — F[1] RC13: Additive QCS_n Delay Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
0	x	x	x	Controls QCS_n Delay	Disable QCS_n delay. Delay QCS_n by 0 tCK to Yn, (m=0)
1	x	x	x		Enable QCS_n delay according to F[1] RC13
1	0	0	0	QCS_n Delay	Delay QCS_n by (8/32)*tCK to Yn, (m=8)
1	0	0	1		Delay QCS_n by (7/32)*tCK to Yn, (m=7)
1	0	1	0		Delay QCS_n by (6/32)*tCK to Yn (m=6)
1	0	1	1		Delay QCS_n by (5/32)*tCK to Yn (m=5)
1	1	0	0		Delay QCS_n by (4/32)*tCK to Yn (m=4)
1	1	0	1		Delay QCS_n by (3/32)*tCK to Yn (m=3)
1	1	1	0		Delay QCS_n by (2/32)*tCK to Yn (m=2)
1	1	1	1		Delay QCS_n by (1/32)*tCK to Yn, (m=1)

9.4 Function 1 Control Word Registers (cont'd)

Table 104 — F[1] RC14: Additive QODT Delay Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
0	x	x	x	Controls QODT Delay	Disable QODT delay. Delay QODT by 0 tCK to Yn, (m=0)
1	x	x	x		Enable QODT delay according to F[1] RC14
1	0	0	0	QODT Delay	Delay QODT by (8/32)*tCK to Yn, (m=8)
1	0	0	1		Delay QODT by (7/32)*tCK to Yn, (m=7)
1	0	1	0		Delay QODT by (6/32)*tCK to Yn, (m=6)
1	0	1	1		Delay QODT by (5/32)*tCK to Yn, (m=5)
1	1	0	0		Delay QODT by (4/32)*tCK to Yn, (m=4)
1	1	0	1		Delay QODT by (3/32)*tCK to Yn, (m=3)
1	1	1	0		Delay QODT by (2/32)*tCK to Yn, (m=2)
1	1	1	1		Delay QODT by (1/32)*tCK to Yn, (m=1)

Table 105 — F[1] RC15: Additive QCKE Delay Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
0	x	x	x	Controls QCKE Delay	Disable QCKE delay. Delay QCKE by 0 tCK to Yn, (m=0)
1	x	x	x		Enable QCKE delay according to F[1] RC15
1	0	0	0	QCKE Delay	Delay QCKE by (8/32)*tCK to Yn, (m=8)
1	0	0	1		Delay QCKE by (7/32)*tCK to Yn, (m=7)
1	0	1	0		Delay QCKE by (6/32)*tCK to Yn, (m=6)
1	0	1	1		Delay QCKE by (5/32)*tCK to Yn, (m=5)
1	1	0	0		Delay QCKE by (4/32)*tCK to Yn, (m=4)
1	1	0	1		Delay QCKE by (3/32)*tCK to Yn, (m=3)
1	1	1	0		Delay QCKE by (2/32)*tCK to Yn, (m=2)
1	1	1	1		Delay QCKE by (1/32)*tCK to Yn, (m=1)

9.4 Function 1 Control Word Registers (cont'd)

FIigure 59 illustrates the QCA prelaunch, QCS_n, QODT and QCKE delay features.

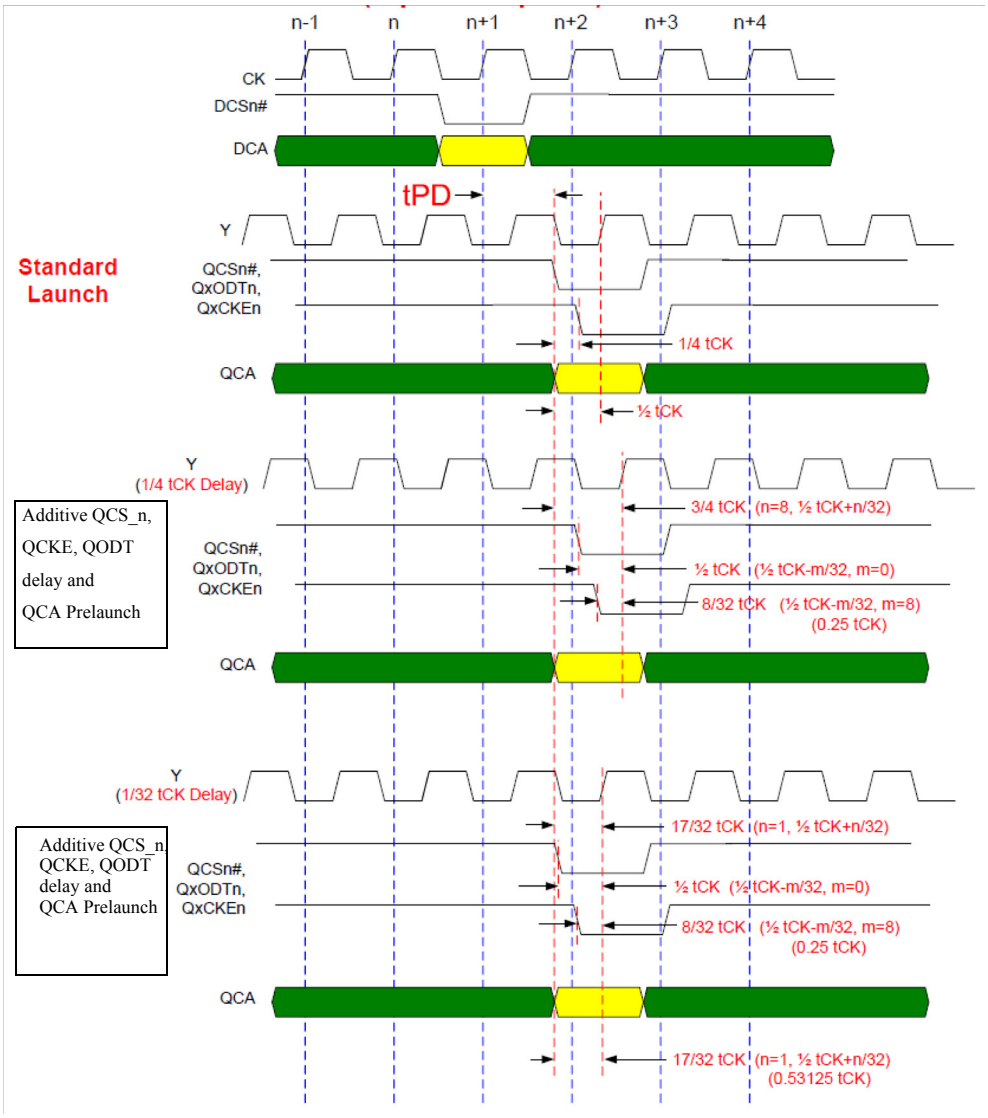


Figure 59 — QCA Prelaunch, QCS_n, QODT, and QCKE Delay Features

9.5 Function 2 Control Word Registers

Table 106 — F[2] RC0 Transparent Mode

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Enable transparent mode	Normal operation
x	x	x	1		Transparent mode enabled
x	x	0	x	Reserved	
x	x	1	x		
0	0	x	x	Chip select multiplication in transparent mode	QACS[3:0]_n=DCS[3:0]_n, QBCS[3:0]_n=DCS[3:0]_n
0	1	x	x		QACS[3:0]_n=DCS[3:0]_n, QBCS[3:0]_n=DCS[7:4]_n
1	0	x	x		QACS[2,0]_n=DCS[1,0]_n, QBCS[2,0]_n=DCS[3,2]_n, QACS[3,1]_n=2'b11, QBCS[3,1]_n=2'b11
1	1	x	x		QACS[2,0]_n=2'b11, QBCS[2,0]_n=2'b11 QACS[3,1]_n=DCS[1,0]_n, QBCS[3,1]_n=DCS[3,2]_n,

Table 107 — F[2] RC1 Reset Control

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Soft Reset	Writing a '0' has no effect
x	x	x	1		Writing a '1' initiates a Soft Reset (Self Clear in the next cycle)
x	x	0	x	Clear Sticky Register Bits	Don't clear sticky register bits during Soft Reset
x	x	1	x		Clear sticky register bits during Soft Reset
x	0	x	x	Mask DDR Reset	Soft Reset will cause assertion of the QRST_n output
x	1	x	x		Soft Reset will not assert the QRST_n output
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

Table 108 — F[2] RC2 SMBus Access Control

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	SMBus Access Control to function space 0	SMBus accesses to/from FN0 are executed
x	x	x	1		SMBus reads from FN0 return all zeros[a] SMBus writes to FN0 are acknowledged but not executed
x	x	0	x	SMBus Access Control to function spaces 1, 3 and 5	SMBus accesses to/from FN1, 3 and 5 are executed
x	x	1	x		SMBus reads from FN1, 3, 5 return all zeros[a] SMBus writes to FN1, 3, 5 are acknowledged but not executed
x	0	x	x	SMBus Access Control to function spaces 2, 4 and 6-15	SMBus accesses to/from FN2, 4 and 6-15 are executed
x	1	x	x		SMBus reads from FN2, 4, 6-15 return all zeros[a] SMBus writes to FN2, 4, 6-15 are acknowledged but not executed
0	x	x	x	SMBus Access Control to Temperature Sensor	SMBus accesses to/from TS are executed
1	x	x	x		SMBus reads from TS return all zeros[a] SMBus writes to TS are acknowledged but not executed

a. MB returns the status of "Internal Target Abort". The host controller should not try to access this through SMbus. However, if host ignores this then MB will return all zeros.

9.5 Function 2 Control Word Registers (cont'd)

Table 109 — F[2] RC3: Training & Errout_n Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Training Control	Normal operating mode; Reset Fail and Valid bit in F[2] RC3[a]
x	x	x	1		Normal operating mode; Do not reset Fail and Valid bit in F[2] RC3[b]
x	x	0	x	Reserved	Reserved for read only Failure bit in CSR
x	x	1	x		
x	0	x	x	Reserved	Reserved for read only Valid bit in CSR
x	1	x	x		
0	x	x	x	Errout_n Enable for Training & MEMBIST	Disable - Errout_n is not driven Low when Training/MEMBIST is started
1	x	x	x		Enable - Errout_n is driven Low when Training/MEMBIST is started

a. Buffer stops driving Errout_n Low when training had an error. Buffer stops training if it was previously started and will stop driving Errout_n Low. Buffer resets Fail and Valid bit in F2 RC3.
b. Buffer stops driving Errout_n Low when training had an error. Buffer stops training if it was previously started and will stop driving Errout_n Low. Buffer does not reset Fail and Valid bit in F2 RC3.

Table 110 — F[2] RC4 MEMBIST Rank Control

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
0	x	x	x	Rank control for MEMBIST	Default; MEMBIST applies to All Ranks
1	0	0	0		Rank 0
1	0	0	1		Rank 1
1	0	1	0		Rank 2
1	0	1	1		Rank 3
1	1	0	0		Rank 4
1	1	0	1		Rank 5
1	1	1	0		Rank 6
1	1	1	1		Rank 7

9.5 Function 2 Control Word Registers (cont'd)

Table 111 — F[2] RC5: DRAM Row & Column Addressing

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Number of Columns	CA[9:0]
x	x	0	1		CA[11, 9:0]
x	x	1	0		CA[13, 11, 9:0]
x	x	1	1		CA[2:0] (8 column addresses of BL=8 page size for testing purposes)
0	0	x	x	Number of Rows	RA[12:0]; 8192 Rows
0	1	x	x		RA[13:0]; 16384 Rows
1	0	x	x		RA[14:0]; 32768 Rows
1	1	x	x		RA[15:0]; 65536 Rows

Table 112 — F[2] RC6: MEMBIST Control

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Reserved	Reserved
x	x	x	1		Reserved
x	x	0	x	MEMBIST Algorithm	Fixed Data 0's (DQ[63:0] only), Full DRAM, Write Full, Read empty, compare, default XYZR order. X = Row (Outer most loop), Y = Column, Z = Bank; R = Rank (Inner most loop)
x	x	1	x		LFSR data (DQ[71:0]), Full DRAM, Write Full, Read empty, compare, default XYZR order. X = Row (Outer most loop), Y = Column, Z = Bank; R = Rank (Inner most loop)
0	0	x	x	MEMBIST, AREF and SREF Control	Default. Normal operation from RESET#. If MEMBIST was previously started, then[a]: 1. Stop MEMBIST. 2. Stop AREF.
0	1	x	x		Stop AREF, wait till it finishes, then put All Ranks of DRAMs into Self Refresh
1	0	x	x		Enable autorefresh generation engine for all physical ranks. Start MemBIST for ranks specified in F2RC4. Autorefresh engine will issue AREF commands as required to all physical ranks during MemBIST operation. Autorefresh engine continues to run after the MemBIST is complete.[b]
1	1	x	x		Reserved

a. Buffer stops driving Errout_n Low if MEMBIST had an error.
b. Buffer starts driving Errout_n Low 20 clocks after receiving this command.

9.5 Function 2 Control Word Registers (cont'd)

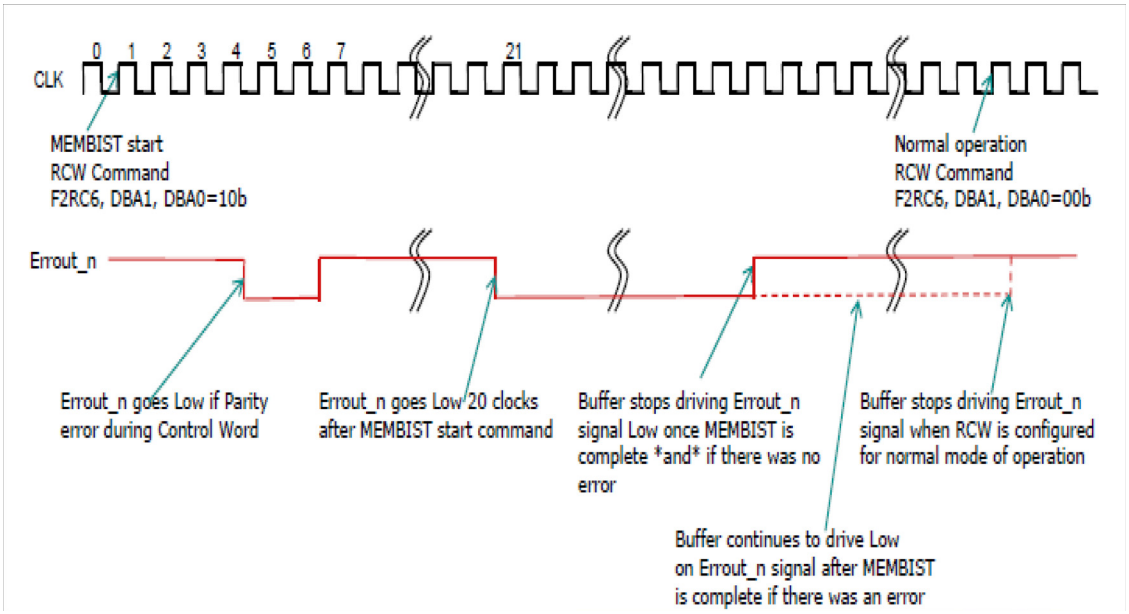


Figure 60 — Errout_n Signal from MBIST to Normal Operation

9.5 Function 2 Control Word Registers (cont'd)

Table 113 — F[2] RC8: MEMBIST ECC Pattern - 1

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	DQ[67:64] ECC Pattern	Lower 4 ECC bits; For F[2] RC6 DA4 = 0.

Table 114 — F[2] RC9: MEMBIST ECC Pattern - 2

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	DQ[71:68] ECC Pattern	Upper 4 ECC bits; For F[2] RC6 DA4 = 0.

Table 115 — F[2] RC10: MEMBIST ECC Pattern - 3

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	DQ[67:64] ECC Pattern	Lower 4 ECC bits; For F[2] RC6 DA4 = 0.

Table 116 — F[2] RC11: MEMBIST ECC Pattern - 4

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	DQ[71:68] ECC Pattern	Upper 4 ECC bits; For F[2] RC6 DA4 = 0.

9.5 Function 2 Control Word Registers (cont'd)

Table 117 — F[2] RC12: MEMBIST ECC Pattern - 5

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	DQ[67:64] ECC Pattern	Lower 4 ECC bits; For F[2] RC6 DA4 = 0.

Table 118 — F[2] RC13: MEMBIST ECC Pattern - 6

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	DQ[71:68] ECC Pattern	Upper 4 ECC bits; For F[2] RC6 DA4 = 0.

9.5 Function 2 Control Word Registers (cont'd)

Table 119 — F[2] RC14: MEMBIST ECC Pattern - 7

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	DQ[67:64] ECC Pattern	Lower 4 ECC bits; For F[2] RC6 DA4 = 0.

Table 120 — F[2] RC15: MEMBIST ECC Pattern - 8

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	DQ[71:68] ECC Pattern	Upper 4 ECC bits; For F[2] RC6 DA4 = 0.

NOTE 1 Host BIOS must always program F2 RC[8-15] regardless of whether it chooses to use 8 bit ECC or 16 bit ECC or 32 bit ECC. See Table 58, Table 59 and Table 60 as an example.

NOTE 2 For 8 bits ECC pattern host programs:

F2 RC[10, 12, 14] same as F2 RC8

F2 RC[11, 13, 15] same as F2 RC9.

NOTE 3 For 16 bits ECC pattern host programs:

F2 RC12 same as F2 RC8

F2 RC14 same as F2 RC10

F2 RC13 same as F2 RC9

F2 RC15 same as F2 RC11

NOTE 4 For 32 bits ECC pattern host programs:

F2 RC[8-15] with appropriate pattern.

9.5 Function 2 Control Word Registers (cont'd)

Table 121 — MEMBIST - 8 Bits ECC Mapping

	Bit Time (Burst)							
Byte Lanes (DIMM Gold Finger)	0	1	2	3	4	5	6	7
Byte lane 0 DQ[7:0]	64 bits Data	64 bits Data	64 bits Data	64 bits Data	64 bits Data	64 bits Data	64 bits Data	64 bits Data
Byte lane 1 DQ[15:8]								
Byte lane 2 DQ[23:16]								
Byte lane 3 DQ[31:24]								
Byte lane 4 DQ[39:32]								
Byte lane 5 DQ[47:40]								
Byte lane 6 DQ[55:48]								
Byte lane 7 DQ[63:56]								
ECC Byte lane DQ[71:64]	8 bits - F[2] RC8 & RC9	8 bits - F[2] RC10 & RC11	8 bits - F[2] RC12 & RC13	8 bits - F[2] RC14 & RC15	8 bits - F[2] RC8 & RC9	8 bits - F[2] RC10 & RC11	8 bits - F[2] RC12 & RC13	8 bits - F[2] RC14 & RC15

Table 122 — MEMBIST - 16 bits ECC Mapping

	Bit Time (Burst)							
Byte Lanes (DIMM Gold Finger)	0	1	2	3	4	5	6	7
Byte lane 0 DQ[7:0]	128 bits Data		128 bits Data		128 bits Data		128 bits Data	
Byte lane 1 DQ[15:8]								
Byte lane 2 DQ[23:16]								
Byte lane 3 DQ[31:24]								
Byte lane 4 DQ[39:32]								
Byte lane 5 DQ[47:40]								
Byte lane 6 DQ[55:48]								
Byte lane 7 DQ[63:56]								
ECC Byte lane DQ[71:64]	8 bits - F[2] RC8 & RC9	8 bits - F[2] RC10 & RC11	8 bits - F[2] RC12 & RC13	8 bits - F[2] RC14 & RC15	8 bits - F[2] RC8 & RC9	8 bits - F[2] RC10 & RC11	8 bits - F[2] RC12 & RC13	8 bits - F[2] RC14 & RC15

Table 123 — MEMBIST - 32 bits ECC Mapping

	Bit Time (Burst)							
Byte Lanes (DIMM Gold Finger)	0	1	2	3	4	5	6	7
Byte lane 0 DQ[7:0]	256 bits Data				256 bits Data			
Byte lane 1 DQ[15:8]								
Byte lane 2 DQ[23:16]								
Byte lane 3 DQ[31:24]								
Byte lane 4 DQ[39:32]								
Byte lane 5 DQ[47:40]								
Byte lane 6 DQ[55:48]								
Byte lane 7 DQ[63:56]								
ECC Byte lane DQ[71:64]	8 bits - F[2] RC8 & RC9	8 bits - F[2] RC10 & RC11	8 bits - F[2] RC12 & RC13	8 bits - F[2] RC14 & RC15	8 bits - F[2] RC8 & RC9	8 bits - F[2] RC10 & RC11	8 bits - F[2] RC12 & RC13	8 bits - F[2] RC14 & RC15

9.6 Function [3-11] Control Word Registers

The following sections describe the contents of each control word in the function 3 to 11 sets.

Table 124 — F[3] RC0: Connector Interface DQ RTT_Nom Termination Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	RTT_Nom	RTT_Nom disabled
x	0	0	1		RZQ/4 (60 Ohm)
x	0	1	0		RZQ/2 (120 Ohm)
x	0	1	1		RZQ/6 (40 Ohm)
x	1	0	0		Reserved
x	1	0	1		RZQ/8 (30 Ohm)
x	1	1	0		RZQ (240 Ohm)
x	1	1	1		RZQ/3 (80 Ohm)
0	x	x	x	TDQS Control	TDQS Disabled
1	x	x	x		TDQS Enabled

Table 125 — F[3] RC1: Connector Interface DQ RTT_WR Termination & Reference Voltage Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	RTT_WR	Dynamic ODT Off
x	0	0	1		RZQ/4 (60 Ohm)
x	0	1	0		RZQ/2 (120 Ohm)
x	0	1	1		RZQ/6 (40 Ohm)
x	1	0	0		Reserved
x	1	0	1		RZQ/8 (30 Ohm)
x	1	1	0		RZQ (240 Ohm)
x	1	1	1		RZQ/3 (80 Ohm)
0	x	x	x	Vref for DQ	Default; Use VrefDQ input pin for receiver reference voltage
1	x	x	x		Use internally generated Vref for receiver reference voltage

9.6 Function [3-11] Control Word Registers (cont'd)

Table 126 — F[3] RC2: Connector Interface DQ Driver Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	Connector Interface DQ/DQS Output Driver Impedance Control	RZQ/6 (40 Ohm)
x	0	0	1		RZQ/7 (34 Ohm)
x	0	1	0		RZQ/5 (48 Ohm)
x	0	1	1		RZQ/9 (27 Ohm)
x	1	0	0		RZQ/12 (20 Ohm)
x	1	0	1		Reserved
x	1	1	0		Reserved
x	1	1	1		Reserved
0	x	x	x	Connector Interface DQ Driver Enable	Connector interface DQ/DQS drivers enabled
1	x	x	x		Connector interface DQ/DQS drivers disabled

Table 127 — F[3] RC[3:5] Reserved

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	Reserved	Reserved

Table 128 — F[3] RC6: Connector Interface Misc Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Connector Interface DQ Timing Mode	Minimum latency
x	x	0	1		Minimum skew
x	x	1	0		Reserved
x	x	1	1		Reserved
x	0	x	x	Reserved	Reserved
x	1	x	x		Reserved
0	x	x	x	Connector Interface DRAM Width	same as DRAM bus width (in F[0]RC14)
1	x	x	x		Always 8 DQs per DQS[a]

a. MB transmits and receives only one strobe pair per byte for Read and Write operation respectively on connector interface. MB transmits and receives one strobe pair per DRAM for Write and Read on DRAM interface. MB turns off its input receivers and terminations for upper 9 strobe pairs on connector interface.

9.6 Function [3-11] Control Word Registers (cont'd)

Table 129 — F[3] RC7: Function Select Control Word (see F[0] RC7 for definition)

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0		

Table 130 — F[3] RC8: DRAM Interface MDQ Termination Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	DRAM Interface MDQ/MDQS ODT Strength for Buffer	DRAM Interface ODT disabled
x	0	0	1		RZQ/4 (60 Ohm)
x	0	1	0		RZQ/2 (120 Ohm)
x	0	1	1		RZQ/6 (40 Ohm)
x	1	0	0		Reserved
x	1	0	1		RZQ/8 (30 Ohm)
x	1	1	0		RZQ (240 Ohm)
x	1	1	1		RZQ/3 (80 Ohm)
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

Table 131 — F[3] RC9: DRAM Interface MDQ Driver Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	DRAM Interface Output Driver Impedance	RZQ/6 (40 Ohm)
x	0	0	1		RZQ/7 (34 Ohm)
x	0	1	0		RZQ/5 (48 Ohm)
x	0	1	1		RZQ/9 (27 Ohm)
x	1	0	0		RZQ/12 (20 Ohm)
x	1	0	1		Reserved
x	1	1	0		Reserved
x	1	1	1		Reserved
0	x	x	x	DRAM Interface Output Driver Disable	DRAM interface MDQ/MDQS drivers enabled
1	x	x	x		DRAM interface MDQ/MDQS drivers disabled

9.6 Function [3-11] Control Word Registers (cont'd)

Table 132 — F[3-10]RC10: Read QODT Control Words; F[3:10] = Rank[0:7] respectively. F11 RC10 Reserved

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	QxODT0	Not asserted during Read
x	x	x	1		Asserted during Read
x	x	0	x	QxODT1	Not asserted during Read
x	x	1	x		Asserted during Read
x	0	x	x	Reserved	Reserved
x	1	x	x		Reserved
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

Table 133 — F[3-10]RC11: Write QODT Control Words; F[3-10] = Rank[0:7] respectively. F11RC11 Reserved

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	QxODT0	Not asserted during Write
x	x	x	1		Asserted during Write
x	x	0	x	QxODT1	Not asserted during Write
x	x	1	x		Asserted during Write
x	0	x	x	Reserved	Reserved
x	1	x	x		Reserved
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

9.6 Function [3-11] Control Word Registers (cont'd)

Table 134 — F[3-11] RC12: Reserved

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
0	0	0	0	Reserved	Reserved
0	0	0	1		Reserved
0	0	1	0		Reserved
0	0	1	1		Reserved
0	1	0	0		Reserved
0	1	0	1		Reserved
0	1	1	0		Reserved
0	1	1	1		Reserved
1	0	0	0		Reserved
1	0	0	1		Reserved
1	0	1	0		Reserved
1	0	1	1		Reserved
1	1	0	0		Reserved
1	1	0	1		Reserved
1	1	1	0		Reserved
1	1	1	1		Reserved

Table 135 — F[3-11] RC13: Reserved

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
0	0	0	0	Reserved	Reserved
0	0	0	1		Reserved
0	0	1	0		Reserved
0	0	1	1		Reserved
0	1	0	0		Reserved
0	1	0	1		Reserved
0	1	1	0		Reserved
0	1	1	1		Reserved
1	0	0	0		Reserved
1	0	0	1		Reserved
1	0	1	0		Reserved
1	0	1	1		Reserved
1	1	0	0		Reserved
1	1	0	1		Reserved
1	1	1	0		Reserved
1	1	1	1		Reserved

9.6 Function [3-11] Control Word Registers (cont'd)

Table 136 — F[3] RC[14-15]: Reserved

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	Reserved	Reserved

Table 137 — F[4-11] RC[0-6, 8-9, 14-15] & F[11] RC[10-11]: Reserved

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x		

9.7 Function 12 Control Registers

Table 138 — F[12] RC[0:6, 8:15]: Reserved

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x		

Table 139 — F[12] RC7: Function Select Control Word (see F0RC7 for definition)

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x		

9.8 Function 13 Control Registers

Table 140 — F[13] RC[0:6, 8]: Reserved

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x		

Table 141 — F[13] RC7: Function Select Control Word (see F0RC7 for definition)

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x		

9.8 Function 13 Control Registers (cont'd)

In order to allow accesses to MB registers that are not control words, a mechanism for accessing ALL MB CSRs via control word writes utilizing address port and data port control words has been defined. This mechanism is similar to the common 0xCF8h/0xCFCh access mechanism used for the PCI CSR register space. To write a specific MB CSR, the SMBus function space where the CSR resides is selected by accessing F13RC9 and the register address within the function space is written into F13RC10 (least significant 4 bits), and F13RC11 (most significant 4 bits) with four optional extended address bits[11:8] in F13RC12. An access to F13RC14 followed by an access to F13RC15 writes to the selected register.

Table 142 — F13 RC9: SMBus Function Select

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
0	0	0	0	Selects SMBus Function	SMBus Function 0
0	0	0	1		SMBus Function 1
0	0	1	0		SMBus Function 2
0	0	1	1		SMBus Function 3
0	1	0	0		SMBus Function 4
0	1	0	1		SMBus Function 5
0	1	1	0		SMBus Function 6
0	1	1	1		SMBus Function 7
1	0	0	0		SMBus Function 8
1	0	0	1		SMBus Function 9
1	0	1	0		SMBus Function 10
1	0	1	1		SMBus Function 11
1	1	0	0		SMBus Function 12
1	1	0	1		SMBus Function 13
1	1	1	0		SMBus Function 14
1	1	1	1		SMBus Function 15

Table 143 — F13 RC10: LSB of Address Port

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	LSB of Register Address Port	Address Bits[3:0]

Table 144 — F13 RC11: MSB of Address Port

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	MSB of Register Address Port	Address bits[7:4]

9.8 Function 13 Control Registers (cont'd)

Table 145 — F13 RC12: Extended Address Port (Optional)

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	Vendor Specific Extended Address Port	Address Bits[11:8]

Table 146 — F13 RC13: Reserved

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x		

Table 147 — F13 RC14: LSB of Data Port

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	LSB of Register Data Port	Data of the LSB bits of the selected register. Bits[3:0]

Table 148 — F13 RC15: MSB of Data Port

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	MSB of Register Data Port	Data of the MSB bits of the selected register. Bits[7:4] Triggers the Control Word Write mechanism to the address defined in F13RC[10-12] with data from F13RC[14-15]

9.9 Function 14 Control Word Registers

Table 149 — F[14] RC[0]: MB Vendor Specific Bytes

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Vendor specific Bytes Disabled	
x	x	x	1	Vendor specific Bytes Enabled	
0	0	0	x	Vendor Specific bits	Personality Byte 0 bits [3:1]
0	0	1	x		
0	1	0	x		
0	1	1	x		
1	0	0	x		
1	0	1	x		
1	1	0	x		
1	1	1	x		

Table 150 — F[14] RC[1]: MB Vendor Specific Bytes

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	Vendor Specific bits	Personality Bytes 0 bits [7:4]

Table 151 — F[14] RC[2:5]: MB Vendor Specific Bytes

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	Vendor Specific bits	Personality Bytes 1 to 2

Table 152 — F[14] RC[6]: MB Vendor Specific Bits

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	Vendor Specific bits	Personality Byte 3 bits [3:0]

Table 153 — F[14] RC7: Function Select Control Word (see F0RC7 for definition)

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x		

Table 154 — F[14] RC[8:15]: MB Vendor Specific Bytes

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	Vendor Specific bits	Personality Bytes 4 to 7

9.10 Function 15 Control Word Registers

Table 155 — F[15] RC[0:5]: MB Vendor Specific Bytes

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	Vendor Specific bits	Personality Bytes 8 to 10

Table 156 — F[15] RC[6]: MB Vendor Specific Bits

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	Vendor Specific bits	Personality Byte 3 bits [7:4]

Table 157 — F[15] RC7: Function Select Control Word (see F0RC7 for definition)

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x		

Table 158 — F[15] RC[8:15]: MB Vendor Specific Bytes

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	x	Vendor Specific bits	Personality Bytes 11 to 14

10 MemBIST

10.1 MemBIST - Memory Built-In Self-Test

The DDR3 Memory Buffer (MB) supports Memory Built-In Self Test (MemBIST) for memory initialization during system boot up and for testing the installed memory. During system boot up and DIMM manufacturing, this mode may also be used to apply tests at speed to test MB to DRAM interface. At DIMM manufacturing, MemBIST offers a fast method to detect assembly related defects, interface defects and majority of the core-related defects during DIMM manufacturing. This testing may be initiated either in or out of band, making MemBIST compatible with motherboards, low cost ATE, or standalone equipment such as continuity testers.

At system level, MEMBIST may also be executed on multiple DIMMs simultaneously. This could be used to speed up memory test during system boot. Before MemBIST can be executed DRAM must be initialised per JESD79-3 requirements and MB functions for write leveling and read training.

DDR interface testing requires stress of the MB DDR I/O circuitry and the DDR I/O-to-core path in the DRAM. The test needs to be able to detect static faults (such as stuck signals) as well as dynamic faults (for example, slow timing paths) in the logic

Testing this logic requires:

- Delivering patterns at full speed (up to 2133MT/S, refer to Vendor Datasheet for actual speed support).
- Incrementing and decrementing addresses. The address decoders are best tested with marching or other non-linear patterns.
- Alternating data patterns (single rotating bits, checkerboards) to detect slow nodes or capacitive coupling in the data path.
- Using standard interface timing (nominal clock cycle time, setup, hold, pre and post-amble)

To accomplish the required testing, MemBIST has a number of modes of operation and data formats which can be chosen to meet the specific need. In addition, MemBIST supports a variety of DRAM timings and densities.

A fundamental feature of the MemBIST architecture is that, it can control individual bits in the 72 bit DQ bus. In addition, MemBIST can apply test patterns at a rate as high as the DRAM address rate. To accomplish this, the MemBIST architecture provides two 72 bit words, or 144 bits of test data for each DRAM clock cycle. The data is supplied to the DRAMs on “early” and “late” phases of the DDR clock cycle. Early data is provided on the rising edge of CK. Late data is provided one half cycle later on the falling edge of CK. DRAM compare data is treated in a similar manner with appropriate clock alignment.

10.2 MemBIST Feature Summary

Table 159 lists the features of MemBIST in summary form. Each feature is explained in subsequent sections. The registers used to control these features are detailed in the MemBIST register section.

Table 159 — MemBIST Feature Summary

Feature	Feature Description
Memory Address Control	
Address pattern in tests	User defined start and end physical address
	Fast X, Fast Y, Fast XY, XZY address modes
	Choice of incrementing or decrementing addresses
	Dynamic address inversion (DAI) inverts alternate addresses
X (row) address bits	Up to 16
Y (column) address bits	Up to 14
Z (bank) address bits	Up to 3
Data Patterns	
Fixed data pattern	Fixed nibble data patterns (0, 3, 5, 6, 9, A, C, F)
User defined data pattern	144-bit user defined data pattern (defined in the MB_USRDEF and MB_USRDEF_ECC registers by user)
	288-bit user defined data pattern (defined in the MB_USRDEF and MB_USRDEF_ECC registers by user)
	576-bit user defined data pattern (defined in the MB_USRDEF and MB_USRDEF_ECC registers by user)
	32-bit user defined circular shifted data pattern
Dynamic data patterns	Random data pattern derived from user-specified 32-bit seed using an LFSR (CRC32)
Data pattern inversion	Any data pattern can be inverted before being applied
Programmable DRAM Timing Control	
DDR3 DRAM timing	Supported by programmable registers in DDR3 MB (e.g. tRCD, tRP, tWR, tRC, tXS, tREF, tCKE, tRAS, tRTP, etc)
Burst Length	8 (default), other options need MR0[A1:A0] programming to support (see JESD79-3E)
Refresh control	DDR3 refresh intervals programmable in DDR3 MB registers
BIST Engine Control	
Fundamental commands	Block Write, Block Read, Block Read with data compare, Block Write + Block Read with data compare
Access method	All registers and settings accessible using SMBus
DRAM data width	x4 or x8

Table 159 — MemBIST Feature Summary

Feature	Feature Description
DRAM initialization and mode settings	Set by DDR3 MB registers
MemBIST throttling	A programmable number of deselect commands may be inserted after DRAM accesses to slow down the speed of DRAM access
Execution control	HALT on error or run to completion of test
	Test ABORT during the test
Failure data access	Failure data logged are accessible using SMBus
	Logging may be delayed to capture later failures
Algorithms Provided	
Algorithms operate over a specified address range with a user defined data in register MBDATA. Notation for algorithm definitions: ^ = increasing address from start to end v = decreasing address from end to start R/W = Read/Write W / R = Write / Read and check D / I = Data / Inverted Data number = sequence of events (x, y) = for each address, first x is applied, then y, before continuing to next address	
Scan	^ (WD_1); ^(RD_2); ^ (WI_3); ^ (RI_4)
Init	^ (WD_1)
Read	^ (RD_1)
Mats+	^(WD_1); ^(RD_2, WI_3); v(RI_4, WD_5);
MarchC–	^(WD_1); ^(RD_2, WI_3); ^(RI_4, WD_5); v(RD_6, WI_7); v(RI_8, WD_9); v(RD_{10});
Error Logging	
Error logging	Pass / fail indicator
	Log up to 8 failing addresses
	Record up to 4 sets of 144-bit failure data
	144-bit failure data bit location accumulator marking bit failures through entire test
Power Saving mode	
	MemBIST engine logic can be turned off during normal operation to save power.

10.3 Function Overview

For memory test at boot, a reduced Initialization MemBIST, which can be controlled with inband commands (RCWs), is available. The full functionality is available out of band through SMBus.

10.3.1 Initialization MemBIST

- Addressing
  - — Full Row Range
  - — Full Column Range or Single Column
  - — All Banks
  - — All Ranks or Single Rank
  - — Increasing Counting Direction
  - — Row-Column-Bank-Rank order
- Data
  - — Fixed 0 for D[63:0] with 4 user defined bytes (half burst) for D[71:64]
  - — Random data generated from LFSR 144-bit data using 32 bit CRC
- Algorithm
  - — Scan for detecting Stuck-At-Faults
- Error Reporting
  - — Use standard MemBIST error log registers
- Refresh
  - — At start of MemBIST, Autorefresh Engine is enabled
  - — Autorefresh always covers all physical ranks and runs parallel to MemBIST (i.e. DRAM data are retained during MemBIST)
  - — After finishing MemBIST test, Autorefresh continues to operate
  - — Issue command to put DRAMs into Self Refresh from Autorefresh State
  - — MemBIST and Autorefresh Engine can be disabled and the buffer returns to normal operation
- Control
  - — Operation can be controlled by F2 RCW registers
  - — Some general buffer setup variables (e.g. number of physical ranks) are also required
- Timing
  - — Timing parameters are given by normal MemBIST timing registers
  - — Reset value is set to DDR3-800. Value can be change through extended RCW interface

10.3.2 Full MemBIST

- Addressing
  - — Support sweeping of rank, bank, row, column
  - — Support 4 sweep orders (**Note**: By default, Rank is in the outer loop and the rank sequence is controlled by software. The rank is specified by F2RC4[3:0])
  - — (Notation: outer loop - … - inner loop):
  - — X: Row, Y: Column, Z: Bank R: Rank
    - – Row-Bank-Column XZY
    - – Bank-Column-Row Fast X
    - – Bank-Row-Column Fast Y
    - – Bank-(Sweep Row, Column diagonal Fast XY
  - — Scheduling
    - – Maximum DQ bus utilization
  - — Single increment/decrement control common for all dimensions
  - — Address inversion every other command
  - — Burst length 4 and 8 supported
- Data generation
  - — Byte individual data configuration, generation and compare
  - — Per byte compare enable mask
  - — Data patterns
    - – Fixed
    - – 64 bit user specified data:
      - full burst of 8 independent bits, repeated in time.
      - 64 user bits specified globally for all 9 bytes
    - – Random 144 bits data generated from 32 bit CRC data
      - LFSR with 32-bit CRC, providing 72 random bits per burst position
    - – 144 bit user defined circular shift data pattern
      - LFSR with 32-bit CRC, providing 72 random bits per burst position
- Per Address commands
  - — Write
  - — Read
  - — Read, Modify (write inverted)
- Algorithms (sequences of basic MemBIST operations)
  - — Memory write (Init), memory read (Read)
  - — Stuck at failure testing (Scan)
  - — Stuck at failure testing with fast read/write turnaround (Mats+)
  - — Memory stress test with incrementing and decrementing addressing (MarchC)
  - — Programmable customer specific test patterns
- Error logging
  - — 8 fail addresses
  - — failure counters
  - — Early/late error bit accumulators
  - — 16 bit error skip counter
- Command Timing
  - — Simple approach: Buffer checks timing values between adjacent commands
- Registers
  - — FN3 (mandatory features): 55 32 bit registers
    - – 19 32 bit registers global functions
    - – 9x4 32 bit registers byte specific functions
  - — FN5 (optional features): 40 32 bit registers
    - – 4 32 bit registers global functions
    - – 9x4 32 bit registers byte specific functions
- Further features
  - — Refresh generation

10.4 Address Generation

10.4.1 Address Definition

All addresses in MemBIST have three components: a row address, a column address and a bank address. These values are concatenated in a 32 bit register. Column address 0 is not stored since the MemBIST engine has an internal 144 bit architecture. Column address 10 is used for auto-precharge (always low in MemBIST) so it is not specified in the address register. Column address 12 is used as burst length value so it is also not part of the address register.

User-defined start and end addressing is constrained to a column address modulo the bust length. For instance, at BC4, a memory access could start at column 0. The next access would start at column 4 and so on. A burst will always end on a page boundary, eliminating boundary checking and simplifying the MemBIST sequencer and control logic. The address register bits will reflect these constraints. BC4 will allow specification of column bits 14..2, while BL=8 will allow specification of column bits 15..3.

Table 160 — Memory Address Definition, BC4

Address bit																												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	R	R	14	13	11	9	8	7	6	5	4	3	2	2	1	0
Row																Column													Bank		

NOTE Bit 14,15 “R” = Reserved for future use.

Table 161 — Memory Address Definition, BL=8

Address bit																												
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	R	R	15	14	13	11	9	8	7	6	5	4	3	2	1	0
Row																Column													Bank		

NOTE Bit 14,15 “R” = Reserved for future use.

10.4.2 Row addressing

- Two values specified in register:
  - Start address XS
  - End address XE
- Directions
  - Increment: Move in steps of 1 from start to end
  - Decrement: Move in steps of 1 from end to start
  - Requirement: XS≤XE

10.4.3 Column addressing

- Two values specified in register:
  - Start address YS
  - End address YE
- Directions
  - Increment: Move in steps of burst length from start to end
  - Decrement: Move in steps of burst length from end to start
  - Requirement: YS≤YE
- Support for burst chop 4 and burst length 8
  - According to DRAM MRS setting:
  - Fixed burst chop 4 => BL=4
  - Fixed burst length 8 => BL=8
- Lower 2(BL=4)/3(BL=8) column address bits will stay constant ‘0’
  - Transmit to DRAM
  - Defines DRAM burst order
  - Data pattern has to be chosen accordingly to take into account burst order scrambling

10.4.4 Diagonal addressing (aka FastXY addressing)

- Row and column addresses will be incremented/decremented simultaneously
- Row address will change in steps of 1
- Column address will change in steps of 4(BL=4) or 8(BL=8)
- If (YE-YS)/BL=(XE-XS) (same number of increments in row and column direction)
  - Buffer will count straight between (XS,YS) to (XE,YE)
- If (YE-YS)/BL!=(XE-XS)
  - Buffer will start at (XS,YS) or (XE,YE)
  - Buffer will increment/decrement row and column address
  - Row and column address will wrap around at rectangle defined by (XS,YS) and (XE,YE)
  - Algorithm finishes when row and column counters reach the target value at the same time

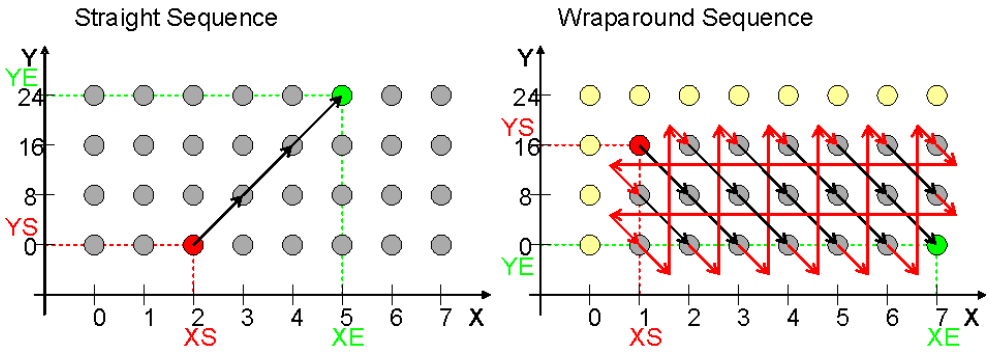


Figure 61 — Diagonal addressing examples

10.4.5 Bank addressing

- Sweeps full banks (default) or portion of the banks for XYZR, XZY address scheme
  - Start bank, default to 0
  - End bank default to 7
- Buffer test banks in increment or decrement order
  - Increment: test bank in the order of (start bank,+1,+2,..,end bank)
  - Decrement: test bank in the order of (end bank, -1, -2, ..., start bank)

10.4.6 Rank addressing

- Sweeps full rank when F2RC4[3:0] = 0XXX
  - Number of physical rank, N, is defined F0RC13[1:0]
  - Increment: test rank in the order of 0,1,2....N-1
  - Decrement: test rank in the order of N-1,N-2...0
- Target specific rank as defined by F2RC4[3:0]
  - 1000: Rank 0
  - 1001: Rank 1
  - 1010: Rank 2
  - 1011: Rank 3
  - 1100: Rank 4
  - 1101: Rank 5
  - 1110: Rank 6
  - 1111: Rank 7

10.4.7 Dynamic Address inversion

To further stress the DRAM there is a control bit to invert the address lines on every access. The least significant address bit is not inverted since it already toggles at the address rate. All address lines (X, Y, bank and rank) will be inverted, creating a ping-pong access pattern. If the starting and ending bank addresses differ as described above, the bank bits will also be inverted on every other access, creating a two-bank pattern. In this case, MemBIST will activate both banks, since otherwise the DDR3 MB would be constantly activating banks. Note that two bank behavior is limited to cases where addresses are applied column-wise, since row-wise operation requires precharge and activate on each row. As indicated in Table 162 (shaded rows are non-inverted, non-shaded rows show inverted addresses), it is possible to traverse 4 or 8 banks. However, only two banks (bank and bank bar) are required to be active at a given time. There is no dependency on the order of activation or precharge between banks in two bank mode. It is possible to activate bank a then bank b or b then a with no difference in the test result.

Also note that DAI will not invert during a single bank test and single rank FastY will not invert the rank. It is normal to think of accesses as being restricted to the address range specified in MB_START_ADDR and MB_END_ADDR. But with DAI enabled, the non-inverted accesses will be within the specified range, but the inverted accesses could possibly fall outside of the specified address range.

Table 162 — Address Inversion

Normal					Inverted, Single Bank					Inverted, 4 Bank				
bank	bit 3	bit 2	bit 1	bit 0	bank	not 3	not 2	not 1	not 0	bank	not 3	not 2	not 1	not 0
00	0	0	0	0	00	0	0	0	0	00	0	0	0	0
00	0	0	0	1	00	1	1	1	1	11	1	1	1	1
00	0	0	1	0	00	0	0	1	0	00	0	0	1	0
00	0	0	1	1	00	1	1	0	1	11	1	1	0	1
00	0	1	0	0	00	0	1	0	0	00	0	1	0	0
00	0	1	0	1	00	1	0	1	1	11	1	0	1	1
00	0	1	1	0	00	0	1	1	0	00	0	1	1	0
00	0	1	1	1	00	1	0	0	1	11	1	0	0	1
00	1	0	0	0	00	1	0	0	0	00	1	0	0	0
00	1	0	0	1	00	0	1	1	1	11	0	1	1	1
00	1	0	1	0	00	1	0	1	0	00	1	0	1	0
00	1	0	1	1	00	0	1	0	1	11	0	1	0	1
00	1	1	0	0	00	1	1	0	0	00	1	1	0	0
00	1	1	0	1	00	0	0	1	1	11	0	0	1	1
00	1	1	1	0	00	1	1	1	0	00	1	1	1	0
00	1	1	1	1	00	0	0	0	1	11	0	0	0	1
01	etc				00	etc				01	etc			
01	etc				00	etc				10	etc			

10.5 Memory Data Formatting

The generation of data pattern is done on a per byte basis. During MemBIST operation, 144-bit data is used to write to memory and to check data read from memory. The data register MBDATA allows definition of a 144-bit data pattern. The 144-bit data will be written in two consecutive 72-bit locations within a memory burst. Since a burst is at least 4 data word (DW), early data is written to the first and third locations in the burst and late data to the second and fourth locations. An 8 bit burst (BL8) will be treated in similar manner.

10.5.1 Static Data Formats

MemBIST provides a number of static (or fixed) data patterns which can be selected using bits in MBCSR. Among these are 0x00, 0x33, 0x55, 0x66, 0x99, 0xAA, 0xCC and 0xFF. A static data pattern is one in which the data remains the same throughout the MemBIST operation. The MB_USRDEF registers can be used to supply 144/288/576 bits of user defined data. The data from this static pattern is also concatenated together multiple times to make up the required number of bits for MemBIST use.

10.5.2 Dynamic Data Formats

In addition to the static data formats, MemBIST has the ability to provide dynamically changing data patterns. Dynamic data changes each time a new address is accessed. Dynamic data can be supplied by either shifted data or pseudo-random data.

MemBIST has the ability to shift data. The 144 bits of DQ data will be circular shifted one bit to the left at the DRAM address rate, which is once per 144 bits. This allows the creation of diagonal patterns such as walking ones or zeros. A lone one in a field of zeros (and vice-versa) is an effective test for continuity on a DIMM DQ bus.

The final data source for dynamic data is a random data generator. This generator will create (CRC 32) pseudo-random patterns starting from a user-defined 32 bit seed. This type of data is useful for general memory stress patterns. The 144 bits of random data will be updated at the DRAM address rate as with the data shifter.

10.5.3 Circular shift register

Rotating data patterns are needed for certain memory tests. One of the applications is walking a 1 or 0 across the DQ bus to detect open or shorted data lines during DIMM manufacturing test. Another anticipated use would be creating rotating or diagonal data patterns to test the DRAM decoders or array.

MemBIST provides a 144 bit circular shift register to allow generation of shifting or rotating data patterns. Rather than requiring the user to load the entire 144 bits, the LFSR seed register is used to specify a 32 bit starting pattern. The 32 bit pattern will be loaded into the least significant 32 bits (early_data[31..0]) of the shift register at the start of test. The upper bits of the register will be cleared to all zeros at the start of test. To generate ‘1’ data, set the data invert bit. The register will shift one position to the left every time new data is required. For example, when BL=4 the register will shift once for the first 144 bits and again for the second 144 bits of the burst. The 144 bits are organized as follows: Late LFSR/Circ Data [71..0] Early LFSR/Circ Data [71..0] <= shift direction.

10.5.4 Random data generator

Random patterns are useful in situations where DRAM topology is not known. A common usage would be to write and read the entire array with random data. Random data may be combined with various addressing modes to create a variety of pseudo-random tests. By default MemBIST does not support random address generation so the test will not be completely random.

The random data generator is a 32-stage LFSR conforming to the IEEE 802.3 (Ethernet) standard. Specifically the LFSR implements the polynomial:

$$P(x) = x32 + x26 + x23 + x22 + x16 + x12 + x11 + x10 + x8 + x7 + x5 + x4 + x2 + x + 1$$

At the start of random data generation the LFSR is seeded with 32 bits from the seed register as described above. These 32 bits are also copied to the least significant bits of a 144 bits data register (MB_LFSRCIRC) The upper bits of MB_LFSRCIRC are loaded with user-defined data. On subsequent updates the 144 bit data register is shifted one bit to the left and the lowest 32 bits are replaced with the next CRC code determined by: invert crc32(invert(bits 31:0)). Other implementations are possible, provided the test setup is the same and the result is a pseudo-random bit stream using the above polynomial. The value of the seed register and MB_LFSRCIRC registers at completion of an LFSR test sequence is implementation specific. If the test is stopped (either by normal termination or an error) and then restarted (e.g., to locate the next error) the MB must continue with the next number in the LFSR sequence. To reset the LFSR, write a new seed in the seed register. In most cases the Scan, Mats+ and MarchC- algorithms will be incompatible with random data. These algorithms require resetting the LFSR seed in the middle of the test or generating different LFSR sequences for back to back write/read traversals. There is no standard mechanism to alter LFSR generation in this way.

10.6 Error Reporting and Control

When MemBIST is enabled, DDR3 MB provides a 144 bit Failure Bit Location Accumulator. During execution, the bits in the Failure Bit Location Accumulator are “sticky” (once set they will stay set). The bit positions will indicate which bits have failed some time during the test. This register is used primarily for detected failed data lines to facilitate DRAM replacement during DIMM manufacturing.

After the MBFADDRPTR (Memory Test Address Pointer Register) has counted down to zero, the first failing DQ data is recorded in the Error Data Register (MB_ERRDATA). Unlike the Failure Bit Location Accumulator, this register reflects only a single failure. The address corresponding to the data in the Error Data Register is also recorded to aid in diagnosis of the failure (see Table 165 for the Fail Address register location).

Normally testing will stop on a failure, leaving appropriate information in the failing address and data registers. If the MemBIST engine is restarted, data in these registers will be overwritten if there is a subsequent failure.

10.6.1 Failure Address Reporting

Failure addresses are reported in a slightly different format than they are specified. The reason is there are a few more bits needed to specify the location of a failure within the burst. Column bit 0 is not needed due to the 144bit architecture of the MemBIST engine.

Column bit0 is not logged as it is always zero and because the address is logged per 144 bit data chunks. Column bit A1 logs failing chunk address for BL4 mode and column bits A[2:1] logs failing chuck address for BL8 mode. A10 and A12 for column address are not logged as A10 is autoprecharge bit and A12 is burst chop bit and so do not constitute part of the column address. Row Address A16 is added for future extension.

Table 163 — Failure Address Format

Address bit																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2	1	0	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	14	13	11	9	8	7	6	5	4	3	2	1
Bank			Row																	Column											

10.6.2 Multiple Failures

Multiple failures require the ability to isolate specific failing addresses (including location in a burst). This is accomplished with a 32 bit register that counts the number of failing 144 bit “chunks” of data.

When a failure occurs MemBIST will stop and report the Fail Address (including burst position), and failure data recorded in the Error Data Register (MB_ERRDATA).

To record all failures the host maintains a failure counter which should be incremented by the number of failures counted by the MB and the test restarted. This process can continue in a loop until the desired end address and burst position (or end of memory) is reached. Internally, MemBIST will load the failure number into a counter and count down each time it encounters a failure. MemBIST will stop at the next failure after the counter reaches zero.

The general procedure for using this feature is to run MemBIST, read and record the address and data failure information from the logs, and then add the number of failure logs received to the value in MBFADDRPTR to cause the failure information already captured to be ignored on the next pass. This process is repeated until MemBIST completes with zeros in the address logs. This indicates that no further errors were detected beyond those already logged.

To generate a complete data log of all failures, use the following procedure:

1. Define starting and ending addresses, address modes and data patterns, set MBFADDRPTR to zero, set halt on error to 0 (don’t halt on error).
2. Start MemBIST and check the result. If pass, exit. If fail, continue.
3. Add the number of complete logs (for which both address and data were read) obtained during this pass to the value in MBFADDRPTR so that these failures will not be seen again on the next pass of MemBIST.
4. Go to step 2

10.7 Per Address operations

The MemBIST engine takes an address from the address generator and performs one of four operations:

— Write
— Read
— Read, Modify (write inverted)

The engine itself takes care of issuing the appropriate command or command sequence to address a specific memory cell in the DRAM.

In the following illustrations the timing parameter in the upper row applies if two consecutive commands go to different ranks. If the two commands go to the same rank the lower timing parameter applies.

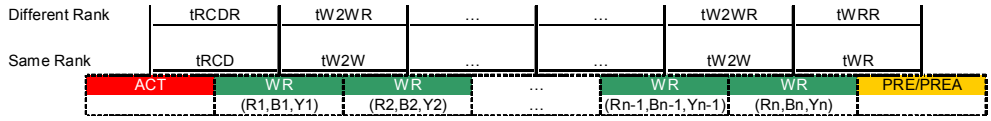


Figure 62 — Write Operation

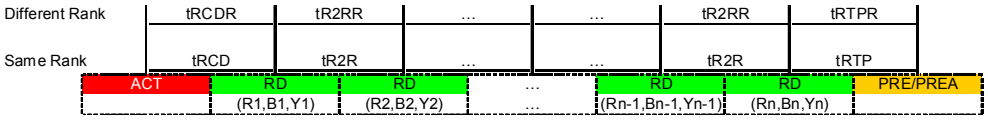


Figure 63 — Read Operation

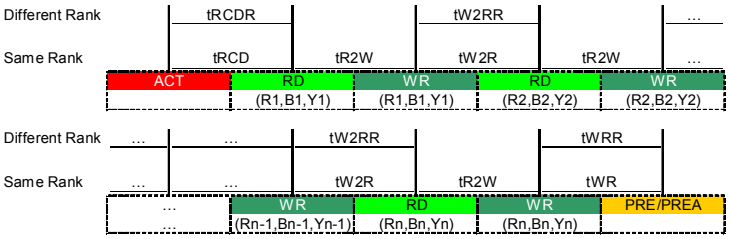


Figure 64 — Read, Modify

10.8 Algorithmic Testing

MemBIST supports several of the more common algorithmic tests. Several of the traversal methods are directed at basic operation such as initializing memory or verifying proper connectivity of the DDR3 MB and DRAM on a DIMM. In addition there are a few tests that are intended to perform testing of the DDR3 MB address generators and DRAM internal address decoders, multiplexers and related logic that is not otherwise testable at speed.

The examples below use the following notation:

^ = increasing addressing. Addresses will be counted up, starting at 0,0 or the user-defined start address.

v = decreasing addressing. Addresses will be counted down, starting at the end of the array or from the user-defined start address.

r or w = Read or Write

D or I = Data or Inverted Data

number = sequence of events

( ) = back to back operations. Example: (wD, rD) will read then write the same cell before moving to the next cell.

Several of these algorithms are implemented in the DDR3 Memory Buffer:

10.8.1 Initialization Tests

- Init: $\hat{}(wD)_1$
  This is a simple memory initialization algorithm. Data will be written to the array with incrementing addressing
  - Traverse Address Range in given Direction, do
    - Write Data according to configuration

- Read:$\hat{}(rD)_1$
  This test is used to verify memory contents. One use of this is data retention testing. Init may be used to write known data in the array. The tester or system can then alter an environmental condition, or simply wait for some period of time, and then read the array to see if the data changed.
  - Traverse Address Range in given Direction, do
    - Read and Compare Data (on the bytes with compare enabled) according to configuration

- Test: $\hat{}(wD)_1$; $\hat{}(rD)_2$
  This test writes data to the array then reads the data back. Test is a 2N pattern, meaning test time will be 2 traversals, times the size of the array (rows * columns * banks, also known as ‘N’) times the average time a read or write operation.
  - Traverse Address Range in given Direction, do
    - Write Data according to configuration
  - Reset data generators
  - Traverse Address Range in given Direction, do
    - Read and Compare Data (on the bytes with compare enabled) according to configuration

- Scan $\hat{}(wD)_1$; $\hat{}(rD)_2$; $\hat{}\ (wI)_3$; $\hat{}\ (rI)_4$
  The scan test writes data to the array then reads the data back. The second half of the test writes inverted data and reads it back. Scan is a 4N pattern, meaning test time will be 4 traversals, times the size of the array (rows * columns * banks, also known as ‘N’) times the average time a read or write operation.
  - Traverse Address Range in given Direction, do
    - Write Data according to configuration
  - Reset Data Generators
  - Traverse Address Range in given Direction, do
    - Read Data, Compare according to compare enable
  - Reset Data Generators, Invert Byte Inversion Bits
  - Traverse Address Range in given Direction, do
    - Write Data according to configuration
  - Reset Data Generators
  - Traverse Address Range in given Direction, do
    - Read Data, Compare according to compare enable

10.8.2 Memory Stress Tests

- Mats+: ^$(wD)_1$; ^(rD_2, wI_3); v(rI_4, wD_5)
  The Mats+ algorithm initializes the array to a known data background and steps through with a read-write sequence. The algorithm is performed with both incrementing and decrementing addressing. Mats+ will detect stuck at faults and basic address decoder faults. The algorithm is order 5N.
  - Traverse Address Range in given Direction, do
    - Write Data according to configuration
  - Reset Data Generators
  - Traverse Address Range in given Direction, do
    - Read-Modify, Compare according to compare enable
  - Reset Data Generators, Invert Byte Inversion Bits, Invert Direction Control Bits
  - Traverse Address Range in opposite Direction, do
    - Read-Modify, Compare according to compare enable

- MarchC-: ^$(wD)_1$; ^(rD_2, wI_3); ^(rI_4, wD_5); v(rD_6, wI_7); v(rI_8, wD_9); v$(rD)_{10}$
  The MarchC- algorithm initializes the array to a known data background and steps through the array in both count-up and count-down addressing with a read-write sequence. MarchC- tests the array decoders and basic neighboring faults. As might be determined from the sequence numbering this is a 10N pattern.
  - Traverse Address Range in given Direction, do
    - Write Data according to configuration
  - Reset Data Generators
  - Traverse Address Range in given Direction, do
    - Read-Modify, Compare according to compare enable
  - Reset Data Generators, Invert Byte Inversion Bits
  - Traverse Address Range in given Direction, do
    - Read-Modify, Compare according to compare enable
  - Reset Data Generators, Invert Byte Inversion Bits, Invert Direction Control Bits
  - Traverse Address Range in opposite Direction, do
    - Read-Modify, Compare according to compare enable
  - Reset Data Generators, Invert Byte Inversion Bits
  - Traverse Address Range in opposite Direction, do
    - Read-Modify, Compare according to compare enable
  - Reset Data Generators, Invert Byte Inversion Bits
  - Traverse Address Range in opposite Direction, do
    - Read, Compare according to compare enable

10.9 MemBIST Flow Control FSM

This FSM controls the MemBIST flow and generates read/write commands for MemBIST. This is only one example of how this functionality might be implemented.

- When MBCSR bit[31] is programmed to begin execution, the MemBIST FSM will transition out of the IDLE state to either WR_START or RD_START, depending upon the MemBIST command programmed in MBCSR:cmd.
- In WR_START state, FSM will look at the decoding of DATA type selection. If LFSR data type generation is selected, FSM will go to WR_SEED state. If not, FSM will directly go to WR_NXTAD state.
- In WR_SEED state, MemBIST will create 5 crc32 data sets and load from the initial seed register MBLFSRSED. When 5 sets of random data are loaded into MBDATA, the FSM will transition out of this state to WR_NXTAD state.
- In the WR_NXTAD state, the next address for the operation is calculated and the address issued. The FSM then transitions to the WR_AVAIL state immediately.
- The FSM will alternate between WR_NXTAD and WR_AVAIL until all writes are issued. In the WR_AVAIL state, a write command will be issued. Once the previous cycle's DRAM timing requirements are met (indicated by cget true), the FSM leaves the WR_AVAIL state. If the write command issued was not to the last address, the FSM will transition to WR_NXTAD. If this was the last address, the FSM will go to WR_WAIT state.
- In the WR_WAIT state, the FSM will wait for the timing for the last write to be met, and then will transition to the WR_DONE state.
- If this is a write only operation, then the FSM will go back to the IDLE state. If this is a write with read comparison test, the FSM will go to the RD_START state.
- In RD_START state, FSM will look at the decoding of DATA type selection. If LFSR data type generation is selected, FSM will go to RD_SEED state. If not, FSM will directly go to RD_NXTAD state.
- In RD_SEED state, MemBIST will create 9 crc32 data sets (16 bits per data set) and load them into MB_LFSRCIRCDAT_ERRACC_BYTE[8:0] from the initial seed register MBLFSRSED. When all 9 sets of random data is set and loaded, FSM will transit out of this state to RD_NXTAD state.
- In the RD_NXTAD state, the next address for the operation is calculated and the address issued. The FSM transitions to the RD_AVAIL state immediately.
- The FSM will alternate between RD_NXTAD and RD_AVAIL until all reads are issued. In the RD_AVAIL state, a read command will be issued. Once the previous cycle's DRAM timing requirements are met (indicated by cget true), the FSM leaves the RD_AVAIL state. If the read command issued was not to the last address, the FSM will transition to RD_NXTAD. If this was the last address, the FSM will go to RD_WAIT state. If this is a back to back read/write operation, the FSM will transit from the RD_AVAIL state to the RD_NXTWR state.
- In the RD_NXTWR state, the address for the write command will be issued (which is the same as the read address previously used). The FSM then transitions to the RD_WRAVL state immediately.
- From the RD_WRAVL state, if this is the last address, the FSM will go to the RD_WAIT state after meeting the DRAM timing requirements. If this is not the last address, the FSM will go back to the RD_NXTAD state again after meeting the DRAM timing requirements.
- In the RD_WAIT state, the FSM will wait for the timing requirements for the last read or write to be met, and then transition to the RD_DONE state.
- From the RD_DONE state the FSM will always go to the IDLE state.

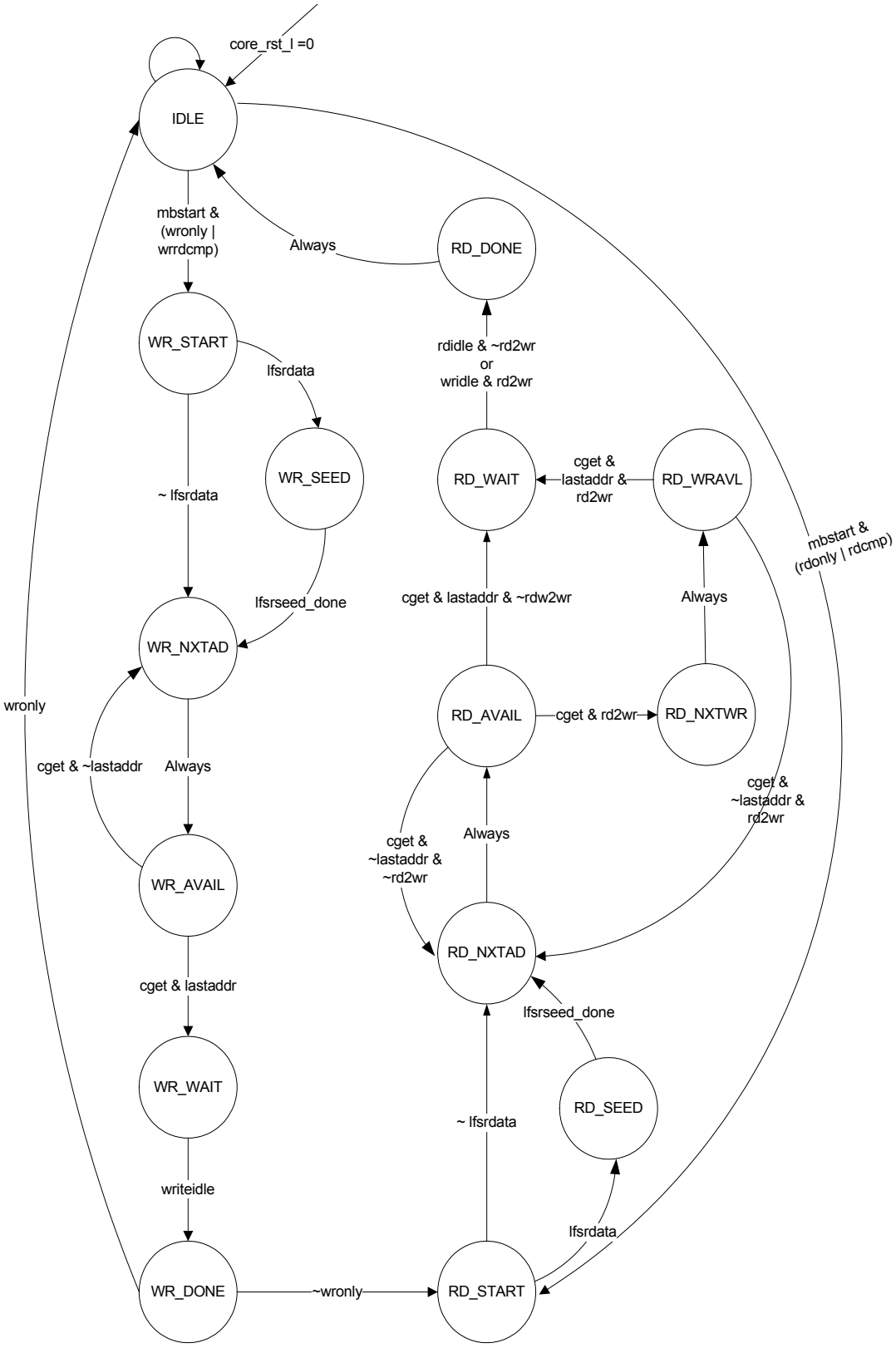


Figure 65 — MemBIST Flow Control State Machine

10.10 Command State Finite State Machine

DDR3 MB MemBIST CSFSM

This FSM creates DRAM commands for MemBIST.

- When read or write command is available and tRP/tRC timing are met, MemBIST CSFSM will transit out of IDLE state to ACT state.
- In ACT state, FSM will wait for tRCD timing parameter qualified and go to RDWT state.
- If the next coming read or write command is in same page and DRAM timing is qualified, FSM will be looping in this state. If the next command is not in the same page or there is an auto-refresh/self-refresh request, FSM will go to PRECHARGE state.
- In PRECHARGE state, FSM always go back to IDLE state.
- In IDLE state, if there is a self refresh or an auto refresh request, FSM will wait for self refresh logic accept signal or auto refresh accept signal.

§

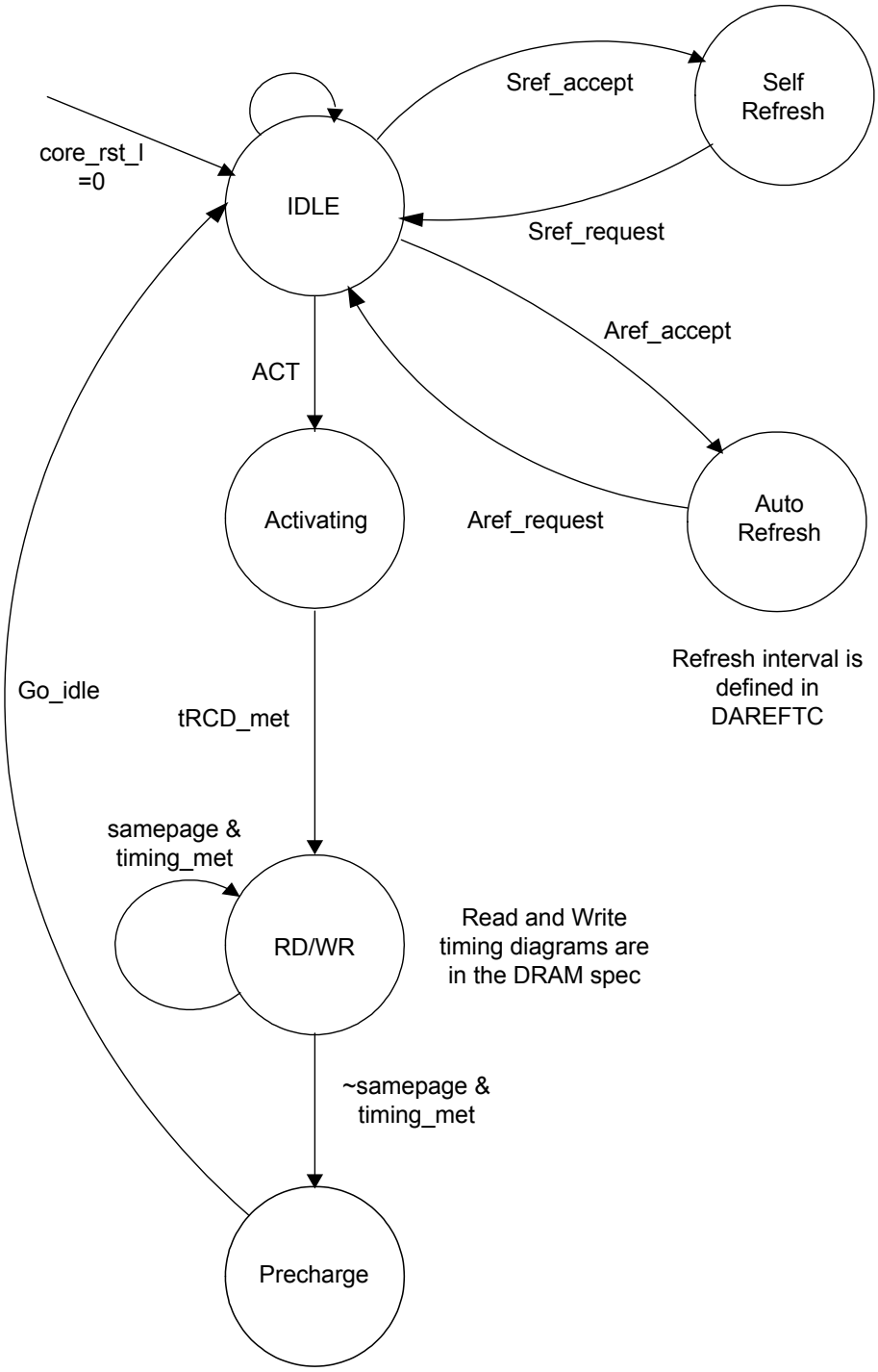


Figure 66 — Command State Machine

10.11 Timing parameters

For sending commands to the DRAMs certain timing constraints need to be observed. Checking and optimizing all of the various timing requirements is far beyond the capabilities of the buffer. Therefore a simplified timing is implemented.

The buffer observes the timing between two consecutive commands and the refresh timing. The following table shows the setup parameters for this timing:

Table 164 — Timing parameters

Row Commands	
t_{RC}	Activate to activate or refresh same rank, different bank
tRAS	Minimum distance last activate to first precharge same rank (not checking bank)
tRP	Last Precharge to first Activate same rank (independent of bank)
Refresh	
tRFC	Refresh to Refresh or Activate same rank
tREFI	Refresh Interval
Row to Column Command	
tRCD	Last Activate to first Read or Write same rank
tRTP	Last Read to first Precharge same rank
tWR	Last Write to first Precharge same rank (as opposed to DRAM end of write burst to precharge!)
Column Command	
tR2R	Read to Read same rank
tR2W	Read to Write same rank
tW2W	Write to Write same rank
tW2R	Write to Read same rank

10.12 Memory BIST Registers

This section describes register for MemBIST engine.

Table 165 — Function 3: MemBIST Registers

MBCSR	00h	**MB_ERRDATA_BYTE0_1_0**	80h
MB_START_ADDR	04h	**MB_ERRDATA_BYTE1_1_0**	84h
MB_END_ADDR	08h	**MB_ERRDATA_BYTE2_1_0**	88h
MBFADDRPTR	0Ch	**MB_ERRDATA_BYTE3_1_0**	8Ch
DAREFTC	10h	**MB_ERRDATA_BYTE4_1_0**	90h
RESERVED	14h	**MB_ERRDATA_BYTE5_1_0**	94h
DRT	18h	**MB_ERRDATA_BYTE6_1_0**	98h
MB_ERR_ADDR0	1Ch	**MB_ERRDATA_BYTE7_1_0**	9Ch
MB_ERR_ADDR1	20h	**MB_ERRDATA_BYTE0_3_2**	A0h
MB_ERR_ADDR2	24h	**MB_ERRDATA_BYTE1_3_2**	A4h
MB_ERR_ADDR3	28h	**MB_ERRDATA_BYTE2_3_2**	A8h
MB_ERR_ADDR4	2Ch	**MB_ERRDATA_BYTE3_3_2**	ACh
MB_ERR_ADDR5	30h	**MB_ERRDATA_BYTE4_3_2**	B0h
MB_ERR_ADDR6	34h	**MB_ERRDATA_BYTE5_3_2**	B4h
MB_ERR_ADDR7	38h	**MB_ERRDATA_BYTE6_3_2**	B8h
RESERVED	3Ch	**MB_ERRDATA_BYTE7_3_2**	BCh
MB_USRDEF144_288_BYTE0	40h	**MB_LFSRCIRCDAT_ERRACC_BYTE0**	C0h
MB_USRDEF144_288_BYTE1	44h	**MB_LFSRCIRCDAT_ERRACC_BYTE1**	C4h
MB_USRDEF144_288_BYTE2	48h	**MB_LFSRCIRCDAT_ERRACC_BYTE2**	C8h
MB_USRDEF144_288_BYTE3	4Ch	**MB_LFSRCIRCDAT_ERRACC_BYTE3**	CCh
MB_USRDEF144_288_BYTE4	50h	**MB_USRDEF144_288_BYTE8**	D0h
MB_USRDEF144_288_BYTE5	54h	**MB_USRDEF576_BYTE8**	D4h
MB_USRDEF144_288_BYTE6	58h	**MB_ERRDATA_BYTE8_1_0**	D8h
MB_USRDEF144_288_BYTE7	5Ch	**MB_ERRDATA_BYTE8_3_2**	DCh
MB_USRDEF576H_L_BYTE0	60h	**MB_LFSCIRCDAT_ERRACC_BYTE8**	E0h
MB_USRDEF576H_L_BYTE1	64h	**MBLFSRSED**	E4h
MB_USRDEF576H_L_BYTE2	68h	**MB_LFSRCIRCDAT_ERRACC_BYTE4**	E8h
MB_USRDEF576H_L_BYTE3	6Ch	**MB_LFSRCIRCDAT_ERRACC_BYTE5**	ECh
MB_USRDEF576H_L_BYTE4	70h	**MB_LFSRCIRCDAT_ERRACC_BYTE6**	F0h
MB_USRDEF576H_L_BYTE5	74h	**MB_LFSRCIRCDAT_ERRACC_BYTE7**	F4h
MB_USRDEF576H_L_BYTE6	78h	**RESERVED**	F8h
MB_USRDEF576H_L_BYTE7	7Ch	**DRC**	FCh

10.12.1 MBCSR: MemBIST Control

Function:3 **Offset:00h**			
Bit	**Attr**	**Default**	**Description**
31	RWS	0	START: Start operation: 1 => Set this bit to begin MemBIST execution. 0 => Hardware will clear this bit when MemBIST execution is completed. BIOS should poll MBCSR.start bit and make sure it is reset to '0' before starting a new MemBIST operation. BIOS should never reset this bit. This bit is always set by BIOS and reset by hardware.
30	RW	0	PF: Fail/Pass indicator: Write to 0 when start MemBIST. Hardware will set to 1 when a failure is detected. 0 => Pass 1 => Fail **N**OTE Read/Write for firmware debug purposes ONLY
29	RW	0	HALT: Halt on Error 0 => Operation will not halt due to a detected error. 1 => Operation will halt after read-compare data error is detected. MemBIST will complete the current transaction before halting. This may result in multiple errors being logged.
28	RW	0	ABORT: MemBIST test abort. 0 => Normal operation. 1 => Need to abort the test during MemBIST operation. When this bit is set to '1' by BIOS, MB will gracefully abort the current operation and reset the MBCSR.START bit to '0'. If there is any MemBIST test following the MemBIST test abort command, bit [28] needs to be cleared. The Write to set MBCSR.abort must occur at least tRFC after the Write to set MBCSR.start. Otherwise subsequent MemBIST operations may fail. tRFC value is set in DAREFTC.trfc (Function3, offset70h, bit field 23:16).
27	RV	0	Reserved

Function:3 **Offset:00h**			
Bit	**Attr**	**Default**	**Description**
26:24	RW	000	ALGO: Embedded Algorithm selection: When Embedded algorithm is applied, please program the following bits at the same time. • I/ Select bit[5:4] for the initial command execution mode. • II/ Program MBCSR bit[11:10] to select FastX, FastY, FastXY • III/Program proper start/end address registers and correspondent MTR value for DIMM type. Do not leave start and end address register as default “00” or the same value. Algorithm did not support single address mode. • IV/ Program MBCSR bit 14 to select failure address logger or failure bits location accumulator. Embedded Algorithm selection: 000 => No embedded algorithm is selected. Normal command will be executed from the selection of MBCSR bits field [5:4] 001 => Scan: ^ (WD1); ^(RD2); ^ (WI3); ^ (RI4) 010 => Undefined 011 => Data Retention (Step I) Write or Init: ^ (WD1); 100 => Data Retention (Step II) Read: ^ (RD2); 101 => Mats +: ^(WD1); ^(RD2, WI3); v(RI4, WD5); 110 => March C-: ^(WD1); ^(RD2, WI3); ^(RI4, WD5); v(RD6, WI7); v(RI8, WD9); v(RD10); 111 => Undefined
23:21	RV	000	Reserved
20	RWS	0	MemBIST PowerSave: When set, this bit will turn off clock that is used in DDR3 MB MemBIST logic during normal operation to save power. If the MB automatically disables MemBIST logic clock this bit is ignored.
19	RW	0	INVERT: Invert data pattern when data is written out to DRAM.
18:16	RW	000	FIXED: Fixed data pattern selection for MemBIST operation 000 => 0 001 => F 010 => A 011 => 5 100 => C 101 => 3 110 => 9 111 => 6
15:14	RW	00	DATA_ENABLE: Enable user defined data patterns for memory fill write only. 00 => 144 bits user defined data pattern when MBCSR[9:8] selects user defined data. 01 => 288 bits user defined data pattern when MBCSR[9:8] selects user defined data. 10 => 576 bits user defined data pattern when MBCSR[9:8] selects user defined data. 11 -> Reserved.

Function:3 **Offset:00h**			
Bit	**Attr**	**Default**	**Description**
13	RW	0	ABAR: MemBIST output address compliment for FastX, FastY, and FastXY. Whenever this bit is enabled, Bank, Row, Column address will be inverted on alternate addresses as described in the MemBIST chapter. 0 => Regular addressing 1 => Dynamic address inversion (see more description in MemBIST Chapter).
12	RW	0	ADIR: Address decode direction for FastX, Fast Y, FastXY 0 => Address increments 1 => Address decrements
11:10	RW	00	FAST: Address sequencing 00 => addressing with XZY toggling (row-bank-column) 01 => Fast Y with fixed rank (bank-row-column) 10 => Fast X with fixed rank (bank-column-row) 11 => Fast XY with fixed rank (bank-(Sweep Row, Column diagonal)) **N**OTE Default value for F2RC4[3:0] is '0000', MemBIST applies to All Ranks. To select a specific Rank for MemBIST, user needs to change the value of F2RC4[3:0].
9:8	RW	00	DTYPE: Data type selection: 00 => Fixed data pattern, selected by MBCSR bits 18:16 01 => 144 or 288 bits user defined data 10 => Circular shift data 11 => LFSR data, seeded from 32 bit LFSR seed register. Circular shift data and LFSR data type should not be used for single address operation (ATYPE = 01).
7:6	RW	00	ATYPE: Address type 00 => Reserved 01 => Single physical address operation, contained in MBADDR row/column/ bank. 10 => start/end physical address range defined in MB_START_ADDR & MB_END_ADDR registers. 11 => full address range of the DIMM as defined in MTR register which specify the number of banks, rows, and columns. Full address test supports XZY addressing (row-bank-column) and fastX/fastY/ fastXY.
5:4	RW	00	CMD: Command execution: 00 => Read only without data comparison 01 => Write only without data comparison 10 => Read with data comparison 11 => Write followed by Read with data comparison
3:0	RV	0	Reserved

10.12.2 MB_START_ADDR: Memory Test Start Address

MB_END_ADDR row and column address must be larger than MB_START_ADDR row and column address in either increasing or decreasing address mode.

This register is only used when MBCSR.atype = 2b'10, and when MBCSR.algo is non-zero.

Function:3 **Offset:04h**			
Bit	**Attr**	**Default**	**Description**
31:16	RW	0000h	ROW: MemBIST Start Row Address 15:0
15:14	RW	00	SPARE:
13:3	RW	0000h	COL: Column Address BL8[13:3] <==> DRAM Column Address 15:13,11,9:3 BC4[13:3] <==> DRAM Column Address 14:13,11,9:2
2:0	RW	000	BA: MemBIST Start Bank Address 2:0

10.12.3 MB_END_ADDR: Memory Test End Address

This register is only used when MBCSR.atype = 2b'10, and when MBCSR.algo is non-zero.

Function:3 **Offset:08h**			
Bit	**Attr**	**Default**	**Description**
31:16	RW	0000h	ROW: MemBIST End Row Address 15:0
15:14	RW	00	SPARE:
13:3	RW	0000h	COL: Column Address BL8[13:3] <==> DRAM Column Address 15:13,11,9:3 BC4[13:3] <==> DRAM Column Address 14:13,11,9:2
2:0	RW	000	BA: MemBIST End Bank Address 2:0

10.12.4 MBFADDRPTR: Memory Test failure address pointer register

Function:3 **Offset:0Ch**			
Bit	**Attr**	**Default**	**Description**
31:16	RW	00h	MBFADDRPTR: This 16 bit register designates which MemBIST failures to log in the available failure address locations. The default value of this register is zero. It means MemBIST always starts logging on the first failure address. For example, if it is programmed to hex A (10 in decimal), MemBIST will log failure addresses starting from the11th failure. The corresponding MB_ERRDATA register will log corrupted data in the first designated failure address. NOTE This register does not affect the MBDATA failure bit location accumulators, neither the error count.
15:0	RW	00h	MB_ERR_CNT: This 16 bit register counts MemBIST test errors. Errors in a 144 bit data Chunk is counted as one error

10.12.4.1 DAREFTC: DRAM Auto-Refresh Timing and Control

Function:3 **Offset:10h**			
Bit	**Attr**	**Default**	**Description**
31:24	RV	0	Reserved
23:16	RW	2Ch	**tRFC**: DRAM refresh period Number of Clocks required for tRFC delay NOTE tRFC value of 110ns (or 44 nCK at DDR3-800) for 1Gb device is used as default value.
15	RW	0	AREFEN: auto-refresh enable **N**OTE This bit can also be cleared by the DDR3 MB FSM as described in Figure 66.
14:0	RW	0C30h	**tREFI**: DRAM refresh interval Number of Clocks required for tREFI delay NOTE tREFI = 7.8µS (7800ns or 3120 nCK at DDR3-800)

10.12.4.2 DRT: DRAM Timing Control

Function:3 Offset:18h			
Bit	**Attr**	**Default**	**Description**
31:29	RW	000	tRAS: DRAM tRAS minimum required delay from active command to precharge command. Delay cycles based on JESD79-3E spec 37.5 ns for DDR3 800/1066, 36 ns for DDR3-1333, 35ns for DDR3-1600, 34ns for DDR3-1866 and 33ns for DDR3-2133. tRAS(min) clocks delay: 000 => 15 for DDR3-800 001 => 20 for DDR3-1066 010 => 24 for DDR3-1333 011 => 28 for DDR3-1600 100 => 32 for DDR3-1866 101 => 35 for DDR3-2133 110 => Reserved 111 => Reserved
28:26	RW	000	tRTP: DRAM cell internal read to precharge command delay. tRTP clocks delay: 000 => 4 for DDR3-800/1066 001 => 5 for DDR3-1333 010 => 6 for DDR3-1600 011 => 7 for DDR3-1866 100 => 8 for DDR3-2133 101 => Reserved 110 => Reserved 111 => Reserved
25:23	RW	000	BBRW: Back to Back Read-Write turn around. This field determines the minimum number of CMDCLK between Read-Write commands. The purpose of these 3 bits are to control the turnaround time on the DQ bus. Regular setting will be based on BL/2 + 2 tCK. BL4: tR2W = 4 tCK BL8: tR2W = 6 tCK Command clocks spacing based on the following encoding: 000 => 10 001 => 9 010 => 8 011 => 7 100 => 6 101 => 5 110 => 4 111 => 3 (stress mode, not recommended)

Function:3 **Offset:18h**			
Bit	**Attr**	**Default**	**Description**
22:20	RW	000	BBWR: Back to Back Write-Read turn around. This field determines the minimum number of CMDCLK between Write-Read commands. The purpose of these 3 bits are to control the turnaround time on the DQ bus. Regular setting will be based on (CL-1)+BL/2+tW2R. Command clocks apart based on the following encoding: 000 => 25 for DDR3-2133 001 => 23 for DDR3-1866 010 => 20 for DDR3-1600 011 => 17 for DDR3-1333 100 => 14 for DDR3-1066 101 => 13 for DDR3-800 110 => 12 111 => 11 (stress mode, not recommended
19:17	RW	000	tWR: tWR DRAM Write Recovery delay Overall delay clocks will be (CL+AL-1) +BL/2 + tWR from write command to precharge command. 000 => 33 for DDR3-2133 001 => 30 for DDR3-1866 010 => 26 for DDR3-1600 011 => 22 for DDR3-1333 100 => 18 for DDR3-1066 101 => 17 for DDR3-800 110 => 14 111 => 13
16:14	RW	000	tRC: tRC DRAM activate to another activate delay 000 => 49 for DDR3-2133 001 => 45 for DDR3-1866 010 => 39 for DDR3-1600 011 => 34 for DDR3-1333 100 => 28 for DDR3-1066 101 => 21 for DDR3-800 110 => 20 111 => 19

Function:3 Offset:18h			
Bit	**Attr**	**Default**	**Description**
13:11	RW	000	tRCD: tRCD DRAM RAS# to CAS# delay 000 => 14 for DDR3-2133 001 => 13 for DDR3-1866 010 => 11 for DDR3-1600 011 => 9 for DDR3-1333 100 => 7 for DDR3-1066 101 => 6 for DDR3-800 110 => 5 111 => 4 If AL >= tRCD, Read/Write command will be issued right after ACT cycle.
10:8	RW	000	tRP: tRP DRAM RAS# to Precharge delay 000 => 14 for DDR3-2133 001 => 13 for DDR3-1866 010 => 11 for DDR3-1600 011 => 9 for DDR3-1333 100 => 7 for DDR3-1066 101 => 6 for DDR3-800 110 => 5 111 => 4
7:0	RW	00h	NOPCNT: Programmable NOP insertion (Device Deselect actually). Number of Nops will be inserted between read/write commands to slow down MemBIST activities. For example: tR2R = 4 + NOPCNT (when NOPs are inserted between READ to READ) tW2W = 4 + NOPCNT (when NOPs are inserted between WRITE to WRITE) Up to 255 clocks NOPs can be programmed to insert delay between read/write commands. If NOPs delay is programmable less than the required DRAM timing, Overall NOP delay from command to command will not be seen.

10.12.5 MB_ERR_ADDR0: Memory Test Failure address 0

This register stores 32 bits of the first failing memory location.

Function:3 Offset:1Ch			
Bit	**Attr**	**Default**	**Description**
31:29	RW	000b	Failed bank address
28:12	RW	00h	Failed Row Address
11:0	RW	00h	Failed column address

10.12.6 MB_ERR_ADDR1: Memory Test Failure address 1

This register stores 32 bits of the second failing memory location.

Function:3 **Offset:20h**			
Bit	**Attr**	**Default**	**Description**
31:29	RW	000b	Failed bank address
28:12	RW	00h	Failed Row Address
11:0	RW	00h	Failed column address

10.12.7 MB_ERR_ADDR2: Memory Test Failure address 2

This register stores 32 bits of the third failing memory location.

Function:3 **Offset:24h**			
Bit	**Attr**	**Default**	**Description**
31:29	RW	000b	Failed bank address
28:12	RW	00h	Failed Row Address
11:0	RW	00h	Failed column address

10.12.8 MB_ERR_ADDR3: Memory Test Failure address 3

This register stores 32 bits of the fourth failing memory location.

Function:3 **Offset:28h**			
Bit	**Attr**	**Default**	**Description**
31:29	RW	000b	Failed bank address
28:12	RW	00h	Failed Row Address
11:0	RW	00h	Failed column address

10.12.9 MB_ERR_ADDR4: Memory Test Failure address 4

This register stores 32 bits of the fifth failing memory location.

Function:3 Offset:2Ch			
Bit	**Attr**	**Default**	**Description**
31:29	RW	000b	Failed bank address
28:12	RW	00h	Failed Row Address
11:0	RW	00h	Failed column address

10.12.10 MB_ERR_ADDR5: Memory Test Failure address 5

This register stores 32 bits of the sixth failing memory location.

Function:3 Offset:30h			
Bit	**Attr**	**Default**	**Description**
31:29	RW	000b	Failed bank address
28:12	RW	00h	Failed Row Address
11:0	RW	00h	Failed column address

10.12.11 MB_ERR_ADDR6: Memory Test Failure address 6

This register stores 32 bits of the seventh failing memory location.

Function:3 Offset:34h			
Bit	**Attr**	**Default**	**Description**
31:29	RW	000b	Failed bank address
28:12	RW	00h	Failed Row Address
11:0	RW	00h	Failed column address

10.12.12 MB_ERR_ADDR7: Memory Test Failure address 7

This register stores 32 bits of the eighth failing memory location.

Function:3 Offset:38h			
Bit	**Attr**	**Default**	**Description**
31:29	RW	000b	Failed bank address
28:12	RW	00h	Failed Row Address
11:0	RW	00h	Failed column address

10.12.12.1 MB_USRDEF144_288_BYTE0: Memory Test User Defined Data for 144 and 288 bit mode

Data for burst 0 and burst 1 (144 bit mode) or bursts 0, 1, 2, and 3 (288 bit mode) is defined in the CSR. ECC bits are defined in MB_USRDEF144_288_BYTE8. Offset 40h contains bits 7:0 data.

Function:3 Offset:40h			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Burst 3 user defined data for Byte 0 (288 bit mode)
23:16	RW	00h	Burst 2 user defined data for Byte 0 (288 bit mode)
15:8	RW	00h	Burst 1 user defined data for Byte 0
7:0	RW	00h	Burst 0 user defined data for Byte 0

10.12.12.2 MB_USRDEF144_288_BYTE1: Memory Test User Defined Data for 144 and 288 bit mode

Data for burst 0 and burst 1 (144 bit mode) or bursts 0, 1, 2, and 3 (288 bit mode) is defined in the CSR. ECC bits are defined in MB_USRDEF144_288_BYTE8. Offset 44h contains bits 15:8 data.

Function:3 Offset:44h			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Burst 3 user defined data for Byte 1 (288 bit mode)
23:16	RW	00h	Burst 2 user defined data for Byte1 (288 bit mode)
15:8	RW	00h	Burst 1 user defined data for Byte 1
7:0	RW	00h	Burst 0 user defined data for Byte 1

10.12.12.3 MB_USRDEF144_288_BYTE2: Memory Test User Defined Data for 144 and 288 bit mode

Data for burst 0 and burst 1 (144 bit mode) or bursts 0, 1, 2, and 3 (288 bit mode) is defined in the CSR. ECC bits are defined in MB_USRDEF144_288_BYTE8. Offset 48h contains bits 23:16 data.

Function:3 **Offset:48h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Burst 3 user defined data for Byte 2
23:16	RW	00h	Burst 2 user defined data for Byte 2
15:8	RW	00h	Burst 1 user defined data for Byte 2
7:0	RW	00h	Burst 0 user defined data for Byte 2

10.12.12.4 MB_USRDEF144_288_BYTE3: Memory Test User Defined Data for 144 and 288 bit mode

Data for burst 0 and burst 1 (144 bit mode) or bursts 0, 1, 2, and 3 (288 bit mode) is defined in the CSR. ECC bits are defined in MB_USRDEF144_288_BYTE8. Offset 4Ch contains bits 31:24 data.

Function:3 **Offset:4Ch**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Burst 3 user defined data for Byte 3
23:16	RW	00h	Burst 2 user defined data for Byte 3
15:8	RW	00h	Burst 1 user defined data for Byte 3
7:0	RW	00h	Burst 0 user defined data for Byte 3

10.12.12.5 MB_USRDEF144_288_BYTE4: Memory Test User Defined Data for 144 and 288 bit mode

Data for burst 0 and burst 1 (144 bit mode) or bursts 0, 1, 2, and 3 (288 bit mode) is defined in the CSR. ECC bits are defined in MB_USRDEF144_288_BYTE8. Offset 50h contains bits 39:32 data.

Function:3 **Offset:50h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Burst 3 user defined data for Byte 4
23:16	RW	00h	Burst 2 user defined data for Byte 4
15:8	RW	00h	Burst 1 user defined data for Byte 4
7:0	RW	00h	Burst 0 user defined data for Byte 4

10.12.12.6 MB_USRDEF144_288_BYTE5: Memory Test User Defined Data for 144 and 288 bit mode

Data for burst 0 and burst 1 (144 bit mode) or bursts 0, 1, 2, and 3 (288 bit mode) is defined in the CSR. ECC bits are defined in MB_USRDEF144_288_BYTE8. Offset 54h contains bits 47:40 data.

Function:3 **Offset:54h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Burst 3 user defined data for Byte 5
23:16	RW	00h	Burst 2 user defined data for Byte 5
15:8	RW	00h	Burst 1 user defined data for Byte 5
7:0	RW	00h	Burst 0 user defined data for Byte 5

10.12.12.7 MB_USRDEF144_288_BYTE6: Memory Test User Defined Data for 144 and 288 bit mode

Data for burst 0 and burst 1 (144 bit mode) or bursts 0, 1, 2, and 3 (288 bit mode) is defined in the CSR. ECC bits are defined in MB_USRDEF144_288_BYTE8. Offset 58h contains bits 55:48 data.

Function:3 **Offset:58h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Burst 3 user defined data for Byte 6
23:16	RW	00h	Burst 2 user defined data for Byte 6
15:8	RW	00h	Burst 1 user defined data for Byte 6
7:0	RW	00h	Burst 0 user defined data for Byte 6

10.12.12.8 MB_USRDEF144_288_BYTE7: Memory Test User Defined Data for 144 and 288 bit mode

Data for burst 0 and burst 1 is defined in the CSR. ECC bits are defined in MB_USRDEF144_288_BYTE8. Offset 5Ch contains bits 63:56 data.

Function:3 **Offset:5Ch**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Burst 3 user defined data for Byte 7
23:16	RW	00h	Burst 2 user defined data for Byte 7
15:8	RW	00h	Burst 1 user defined data for Byte 7
7:0	RW	00h	Burst 0 user defined data for Byte 7

10.12.12.9 MB_USRDEF576H_L_BYTE0: Memory Test User Defined Data for 576 bit mode

Data for bursts 4, 5, 6, and 7 is defined in the CSR. ECC bits are defined in MB_USRDEF576_BYTE8. Offset 60h contains bits 7:0 data.

Function:3 **Offset:60h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Burst 7 user defined data for Byte 0
23:16	RW	00h	Burst 6 user defined data for Byte 0
15:8	RW	00h	Burst 5 user defined data for Byte 0
7:0	RW	00h	Burst 4 user defined data for Byte 0

10.12.12.10 MB_USRDEF576H_L_BYTE1: Memory Test User Defined Data for 576 bit mode

Data for bursts 4, 5, 6, and 7 is defined in the CSR. ECC bits are defined in MB_USRDEF576_BYTE8. Offset 64h contains bits 15:8 data.

Function:3 **Offset:64h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Burst 7 user defined data for Byte 1
23:16	RW	00h	Burst 6 user defined data for Byte 1
15:8	RW	00h	Burst 5 user defined data for Byte 1
7:0	RW	00h	Burst 4 user defined data for Byte 1

10.12.12.11 MB_USRDEF576H_L_BYTE2: Memory Test User Defined Data for 576 bit mode

Data for bursts 4, 5, 6, and 7 is defined in the CSR. ECC bits are defined in MB_USRDEF576_BYTE8. Offset 68h contains bits23:16 data.

Function:3 **Offset:68h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Burst 7 user defined data for Byte 2
23:16	RW	00h	Burst 6 user defined data for Byte 2
15:8	RW	00h	Burst 5 user defined data for Byte 2
7:0	RW	00h	Burst 4 user defined data for Byte 2

10.12.12.12 MB_USRDEF576H_L_BYTE3: Memory Test User Defined Data for 576 bit mode

Data for bursts 4, 5, 6, and 7 is defined in the CSR. ECC bits are defined in MB_USRDEF576_BYTE8. Offset 6Ch contains bits 31:24 data.

Function:3 **Offset:6Ch**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Burst 7 user defined data for Byte 3
23:16	RW	00h	Burst 6 user defined data for Byte 3
15:8	RW	00h	Burst 5 user defined data for Byte 3
7:0	RW	00h	Burst 4 user defined data for Byte 3

10.12.12.13 MB_USRDEF576H_L_BYTE4: Memory Test User Defined Data for 576 bit mode

Data for bursts 4, 5, 6, and 7 is defined in the CSR. ECC bits are defined in MB_USRDEF576_BYTE8. Offset 70h contains bits 39:32 data.

Function:3 **Offset:70h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Burst 7 user defined data for Byte 4
23:16	RW	00h	Burst 6 user defined data for Byte 4
15:8	RW	00h	Burst 5 user defined data for Byte 4
7:0	RW	00h	Burst 4 user defined data for Byte 4

10.12.12.14 MB_USRDEF576H_L_BYTE5: Memory Test User Defined Data for 576 bit mode

Data for bursts 4, 5, 6, and 7 is defined in the CSR. ECC bits are defined in MB_USRDEF576_BYTE8. Offset 74h contains bits 47:40 data.

Function:3 **Offset:74h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Burst 7 user defined data for Byte 5
23:16	RW	00h	Burst 6 user defined data for Byte 5
15:8	RW	00h	Burst 5 user defined data for Byte 5
7:0	RW	00h	Burst 4 user defined data for Byte 5

10.12.12.15 MB_USRDEF576H_L_BYTE6: Memory Test User Defined Data for 576 bit mode

Data for bursts 4, 5, 6, and 7 is defined in the CSR. ECC bits are defined in MB_USRDEF576_BYTE8. Offset 78h contains bits 55:48 data.

Function:3 Offset:78h			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Burst 7 user defined data for Byte 6
23:16	RW	00h	Burst 6 user defined data for Byte 6
15:8	RW	00h	Burst 5 user defined data for Byte 6
7:0	RW	00h	Burst 4 user defined data for Byte 6

10.12.12.16 MB_USRDEF576H_L_BYTE7: Memory Test User Defined Data for 576 bit mode

Data for bursts 4, 5, 6, and 7 is defined in the CSR. ECC bits are defined in MB_USRDEF576_BYTE8. Offset 7Ch contains bits 63:56 data.

Function:3 Offset:7Ch			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Burst 7 user defined data for Byte 7
23:16	RW	00h	Burst 6 user defined data for Byte 7
15:8	RW	00h	Burst 5 user defined data for Byte 7
7:0	RW	00h	Burst 4 user defined data for Byte 7

10.12.13 MB_ERRDATA_BYTE0_1_0: Memory Test Error Data 1/0

Stores 16 bits of failure data for Byte 0. ECC data is stored in MB_ERRDATA00_ECC. Offset 80h stores early and late first and second failed data for bits 7:0.

Function:3 Offset:80h			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Second failed late data for Byte 0
23:16	RW	00h	Second failed early data for Byte 0
15:8	RW	00h	First failed late data for Byte 0
7:0	RW	00h	First failed early data for Byte 0

10.12.14 MB_ERRDATA_BYTE1_1_0: Memory Test Error Data 1/0

Stores 16 bits of failure data for Byte 1. ECC data is stored in MB_ERRDATA00_ECC. Offset 84h stores early and late first and second failed data for bits 15:8.

Function:3 **Offset:84h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Second failed late data for Byte 1
23:16	RW	00h	Second failed early data for Byte 1
15:8	RW	00h	First failed late data for Byte 1
7:0	RW	00h	First failed early data for Byte 1

10.12.14.1 MB_ERRDATA_BYTE2_1_0: Memory Test Error Data 1/0

Stores 16 bits of failure data for Byte 2. ECC data is stored in MB_ERRDATA00_ECC. Offset 88h stores early and late first and second failed data for bits 23:16.

Function:3 **Offset:88h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Second failed late data for Byte 2
23:16	RW	00h	Second failed early data Byte 2
15:8	RW	00h	First failed late data for Byte 2
7:0	RW	00h	First failed early data for Byte 2

10.12.14.2 MB_ERRDATA_BYTE3_1_0: Memory Test Error Data 1/0

Stores 16 bits of failure data for Byte 3. ECC data is stored in MB_ERRDATA00_ECC. Offset 8ch stores early and late first and second failed data for bits 31:24.

Function:3 **Offset:8ch**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Second failed late data for Byte 3
23:16	RW	00h	Second failed early data for Byte 3
15:8	RW	00h	First failed late data for Byte 3
7:0	RW	00h	First failed early data for Byte 3

10.12.14.3 MB_ERRDATA_BYTE4_1_0: Memory Test Error Data 1/0

Stores 16 bits of failure data for Byte 4. ECC data is stored in MB_ERRDATA_BYTE8_1_0. Offset 90h stores early and late first and second failed data for bits 39:32.

Function:3 **Offset:90h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Second failed late data for Byte 4
23:16	RW	00h	Second failed early data for Byte 4
15:8	RW	00h	First failed late data for Byte 4
7:0	RW	00h	First failed early data for Byte 4

10.12.14.4 MB_ERRDATA_BYTE5 1_0: Memory Test Error Data 1/0

Stores 16 bits of failure data for Byte 5. ECC data is stored in MB_ERRDATA_BYTE8_1_0. Offset 94h stores early and late first and second failed data for bits 47:40.

Function:3 **Offset:94h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Second failed late data for Byte 5
23:16	RW	00h	Second failed early data for Byte 5
15:8	RW	00h	First failed late data for Byte 5
7:0	RW	00h	Fist failed early data for Byte 5

10.12.14.5 MB_ERRDATA_BYTE6 _1_0: Memory Test Error Data 1/0

Stores 16 bits of failure data for Byte 6. ECC data is stored in MB_ERRDATA_BYTE8_1_0. Offset 98h stores early and late first and second failed data for bits 55:48.

Function:3 **Offset:98h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Second failed late data for Byte 6
23:16	RW	00h	Second failed early data Byte 6
15:8	RW	00h	First failed late data for Byte 6
7:0	RW	00h	First failed early data for Byte 6

10.12.14.6 MB_ERRDATA_BYTE7_1_0: Memory Test Error Data 1/0

Stores 16 bits of failure data for Byte 7. ECC data is stored in MB_ERRDATA_BYTE8_1_0. Offset 9ch stores early and late first and second failed data for bits 63:56.

Function:3 **Offset:9Ch**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Second failed late data for Byte 7
23:16	RW	00h	Second failed early data for Byte 7
15:8	RW	00h	First failed late data for Byte 7
7:0	RW	00h	First failed early data for Byte 7

10.12.14.7 MB_ERRDATA_BYTE0_3_2: Memory Test Error Data 3/2

Stores 16 bits of failure data for Byte 0. ECC data is stored in MB_ERRDATA02_ECC. Offset A0h stores early and late third and fourth failed data for bits 7:0.

Function:3 **Offset:A0h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Fourth failed late data for Byte 0
23:16	RW	00h	Fourth failed early data for Byte 0
15:8	RW	00h	Third failed late data for Byte 0
7:0	RW	00h	Third failed early data for Byte 0

10.12.14.8 MB_ERRDATA_BYTE1_3_2: Memory Test Error Data 3/2

Stores 16 bits of failure data for Byte 1. ECC data is stored in MB_ERRDATA02_ECC. Offset A4h stores early and late third and fourth failed data for bits 15:8.

Function:3 **Offset:A4h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Fourth failed late data for Byte 1
23:16	RW	00h	Fourth failed early data for Byte 1
15:8	RW	00h	Third failed late data for Byte 1
7:0	RW	00h	Third failed early data for Byte 1

10.12.14.9 MB_ERRDATA_BYTE2_3_2: Memory Test Error Data 3/2

Stores 16 bits of failure data for Byte 2. ECC data is stored in MB_ERRDATA02_ECC. Offset A8h stores early and late third and fourth failed data for bits 23:16.

Function:3 **Offset:A8h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Fourth failed late data for Byte 2
23:16	RW	00h	Fourth failed early data for Byte 2
15:8	RW	00h	Third failed late data for Byte 2
7:0	RW	00h	Third failed early data for Byte 2

10.12.14.10 MB_ERRDATA_BYTE3_3_2: Memory Test Error Data 3/2

Stores 16 bits of failure data for Byte 3. ECC data is stored in MB_ERRDATA02_ECC. Offset Ach stores early and late third and fourth failed data for bits 31:24.

Function:3 **Offset:ACh**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Fourth failed late data for Byte 3
23:16	RW	00h	Fourth failed early data for Byte 3
15:8	RW	00h	Third failed late data for Byte 3
7:0	RW	00h	Third failed early data for Byte 3

10.12.14.11 MB_ERRDATA_BYTE4_3_2: Memory Test Error Data 3/2

Stores 16 bits of failure data for Byte 4. ECC data is stored in MB_ERRDATA_BYTE8_3_2. Offset B0h stores early and late third and fourth failed data for bits 39:32.

Function:3 **Offset:B0h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Fourth failed late data for Byte 4
23:16	RW	00h	Fourth failed early data for Byte 4
15:8	RW	00h	Third failed late data for Byte 4
7:0	RW	00h	Third failed early data for Byte 4

10.12.14.12 MB_ERRDATA_BYTE5_3_2: Memory Test Error Data 3/2

Stores 16 bits of failure data for Byte 5. ECC data is stored in MB_ERRDATA_BYTE8_3_2. Offset B4h stores early and late third and fourth failed data for bits 47:40.

Function:3 **Offset:B4h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Fourth failed late data for Byte 5
23:16	RW	00h	Fourth failed early data for Byte 5
15:8	RW	00h	Third failed late data for Byte 5
7:0	RW	00h	Third failed early data for Byte 5

10.12.14.13 MB_ERRDATA_BYTE6_3_2: Memory Test Error Data 3/2

Stores 16 bits of failure data for Byte 6. ECC data is stored in MB_ERRDATA_BYTE8_3_2. Offset B8h stores early and late third and fourth failed data for bits 55:48.

Function:3 **Offset:B8h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Fourth failed late data for Byte 6
23:16	RW	00h	Fourth failed early data for Byte 6
15:8	RW	00h	Third failed late data for Byte 6
7:0	RW	00h	Third failed early data for Byte 6

10.12.14.14 MB_ERRDATA_BYTE7_3_2: Memory Test Error Data 3/2

Stores 16 bits of failure data for Byte 7. ECC data is stored in MB_ERRDATA_BYTE8_3_2. Offset BCh stores early and late third and fourth failed data for bits 63:56.

Function:3 **Offset:BCh**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Fourth failed late data for Byte 7
23:16	RW	00h	Fourth failed early data for Byte 7
15:8	RW	00h	Third failed late data for Byte 7
7:0	RW	00h	Third failed early data for Byte 7

10.12.14.15 MB_LFSRCIRCDAT_ERRACC_BYTE0: Memory Test Accumulator 0

Stores 16 bits of accumulated bit error data from memory and 16 bits of LFSR/Circular shift data for Byte 0. ECC error accumulator data is stored in MB_LFSCIRCDAT_ERRACC_ BYTE8. Offset C0h stores error data and LFSR/ Circular shift data for bits 7:0.

Function:3 **Offset:C0h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Late LFSR/Circ data for Byte 0
23:16	RW	00h	Early LFSR/Circ data for Byte 0
15:8	RW	00h	Late error accumulator for Byte 0
7:0	RW	00h	Early error accumulator for Byte 0

10.12.14.16 MB_LFSRCIRCDAT_ERRACC_BYTE1: Memory Test Accumulator 1

Stores 16 bits of accumulated bit error data from memory and 16 bits of LFS/Circular shift data for Byte 1. ECC error accumulator data is stored in MB_LFSCIRCDAT_ERRACC_ BYTE8. Offset C4h stores error data and LFSR/ Circular shift data for bits 15:8.

Function:3 **Offset:C4h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Late LFSR/Circ data for Byte 1
23:16	RW	00h	Early LFSR/Circ data for Byte 1
15:8	RW	00h	Late error accumulator for Byte 1
7:0	RW	00h	Early error accumulator for Byte 1

10.12.14.17 MB_LFSRCIRCDAT_ERRACC_BYTE2: Memory Test Accumulator 2

Stores 16 bits of accumulated bit error data from memory and 16 bits of LFSR/Circular shift data for Byte 2. ECC error accumulator data is stored in MB_LFSCIRCDAT_ERRACC_ BYTE8. Offset C8h stores error data and LFSR/ Circular shift data for bits 23:16.

Function:3 **Offset:C8h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Late LFSR/Circ data for Byte 2
23:16	RW	00h	Early LFSR/Circ data for Byte 2
15:8	RW	00h	Late error accumulator for Byte 2
7:0	RW	00h	Early error accumulator for Byte 2

10.12.14.18 MB_LFSRCIRCDAT_ERRACC_BYTE3: Memory Test Accumulator 3

Stores 16 bits of accumulated bit error data from memory and 16 bits of LFSR/Circular shift data for Byte 3. ECC error accumulator data is stored in MB_LFSCIRCDAT_ERRACC_ BYTE8. Offset CCh stores error data and LFSR/ Circular shift data for bits 31:24.

Function:3 **Offset:CCh**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Late LFSR/Circ data for Byte 3
23:16	RW	00h	Early LFSR/Circ data for Byte 3
15:8	RW	00h	Late error accumulator for Byte 3
7:0	RW	00h	Early error accumulator for Byte 3

10.12.14.19 MB_USRDEF144_288_BYTE8: Memory Test User Defined ECC Data for 144 and 288 bit modes

Data for burst 0, burst 1, burst 2 and burst3 is defined in the CSR. Offset D0h contains ECC bits early and late data.

Function:3 **Offset:D0h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	User defined ECC late data for 288 bit mode (burst 3)
23:16	RW	00h	User defined ECC early data for 288 bit mode (burst 2)
15:8	RW	00h	User defined ECC late data for 144 and 288 bit mode (burst 1)
7:0	RW	00h	User defined ECC early data for 144 and 288 bit mode (burst 0)

10.12.14.20 MB_USRDEF576_BYTE8: Memory Test User Defined ECC Data for 576 bit mode

Data for burst 4, burst 5, burst 6 and burst7 is defined in the CSR. Offset D4h contains ECC bits early and late data.

Function:3 **Offset:D4h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	User defined ECC late data for 576 bit mode (burst 7)
23:16	RW	00h	User defined ECC early data for 576 bit mode (burst 6)
15:8	RW	00h	User defined ECC late data for 576 bit mode (burst 5)
7:0	RW	00h	User defined ECC early data for 576 bit mode (burst 4)

10.12.14.21 MB_ERRDATA_BYTE8_1_0: Memory Test ECC Fail Data

Stores 16 bits of failure data from memory for ECC bits. Offset D8h stores early and late failed data bits.

Function:3 **Offset:D8h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Second fail ECC late data
23:16	RW	00h	Second fail ECC early data
15:8	RW	00h	First fail ECC late data
7:0	RW	00h	First fail ECC early data

10.12.14.22 MB_ERRDATA_BYTE8_3_2: Memory Test ECC Fail Data

Stores 16 bits of failure data from memory for ECC bits. Offset DCh stores early and late failed data bits.

Function:3 **Offset:DCh**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Fourth fail ECC late data
23:16	RW	00h	Fourth fail ECC early data
15:8	RW	00h	Third fail ECC late data
7:0	RW	00h	Third fail ECC early data

10.12.14.23 MB_LFSCIRCDAT_ERRACC_ BYTE8: Memory Test LFSR/Circular/ Accumulator for ECC

Stores 16 bits of accumulated bit error data for ECC bits and LFSR/Circular data for ECC byte.

Function:3 **Offset:E0h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	ECC LFSR/Circular late data
23:16	RW	00h	ECC LFSR/Circular early data
15:8	RW	00h	ECC Error Accumulator late data
7:0	RW	00h	ECC Error Accumulator early data

10.12.15 MBLFSRSED: Memory Test Circular Shift and LFSR Seed

Function:3 Offset:E4h			
Bit	**Attr**	**Default**	**Description**
31:0	RW	0000h	MBLFSRSED:MemBIST LFSR Seed This 32 bit register will be used as the initial data seed for LFSR or Circular shift data pattern.

10.12.15.1 MB_LFSRCIRCDAT_ERRACC_BYTE4: Memory Test Accumulator 4

Stores 16 bits of accumulated bit error data from memory and 16 bits of LFSR/Circular shift data for Byte 4. ECC error accumulator data is stored in MB_LFSCIRCDAT_ERRACC_ BYTE8. Offset E8h stores error data and LFSR/ Circular shift data for bits 39:32.

Function:3 Offset:E8h			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Late LFSR/Circ data for Byte 4
23:16	RW	00h	Early LFSR/Circ data for Byte 4
15:8	RW	00h	Late error accumulator for Byte 4
7:0	RW	00h	Early error accumulator for Byte 4

10.12.15.2 MB_LFSRCIRCDAT_ERRACC_BYTE5: Memory Test Accumulator 5

Stores 16 bits of accumulated bit error data from memory and 16 bits of LFSR/Circular shift data for Byte 5. ECC error accumulator data is stored in MB_LFSCIRCDAT_ERRACC_ BYTE8. Offset ECh stores error data and LFSR/ Circular shift data for bits 47:40.

Function:3 Offset:ECh			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Late LFSR/Circ data for Byte 5
23:16	RW	00h	Early LFSR/Circ data for Byte 5
15:8	RW	00h	Late error accumulator for Byte 5
7:0	RW	00h	Early error accumulator for Byte 5

10.12.15.3 MB_LFSRCIRCDAT_ERRACC_BYTE6: Memory Test Accumulator 6

Stores 16 bits of accumulated bit error data from memory and 16 bits of LFSR/Circular shift data for Byte 6. ECC error accumulator data is stored in MB_LFSCIRCDAT_ERRACC_ BYTE8. Offset F0h stores error data and LFSR/ Circular shift data for bits 55:48.

Function:3 **Offset:F0h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Late LFSR/Circ data for Byte 6
23:16	RW	00h	Early LFSR/Circ data for Byte 6
15:8	RW	00h	Late error accumulator for Byte 6
7:0	RW	00h	Early error accumulator for Byte 6

10.12.15.4 MB_LFSRCIRCDAT_ERRACC_BYTE7: Memory Test Accumulator 7

Stores 16 bits of accumulated bit error data from memory and 16 bits of LFSR/Circular shift data for Byte 7. ECC error accumulator data is stored in MB_LFSCIRCDAT_ERRACC_ BYTE8. Offset F4h stores error data and LFSR/ Circular shift data for bits 63:56.

Function:3 **Offset:F4h**			
Bit	**Attr**	**Default**	**Description**
31:24	RW	00h	Late LFSR/Circ data for Byte 7
23:16	RW	00h	Early LFSR/Circ data for Byte 7
15:8	RW	00h	Late error accumulator for Byte 7
7:0	RW	00h	Early error accumulator for Byte 7

10.12.15.5 DRC: DRAM Controller Mode Register

This register controls the mode of the DRAM Controller.

Function:3 **Offset:FCh**			
Bit	**Attr**	**Default**	**Description**
31:30	RV	00	Reserved
29	RW	0	**INITDONE: Initialization Complete.** This scratch bit communicates software state from the DDR3 MB to BIOS. BIOS sets this bit to 1 after initialization of the DRAM memory array is complete. This bit has no effect on DDR3 MB operation.
28:0	RV	0	Reserved

11 Transparent Mode

11.1 Transparent Mode

In normal operation access to the DRAMs is filtered by the memory buffer. For tests where direct access to the DRAMs is needed the transparent mode is available.

It enables the test equipment to send commands to the DRAMs that are blocked in normal operation because they have a special meaning for the buffer or because they violate the protocol

In transparent mode most operational functions are not available. This mode is designed such as the commands go through the buffer with the least possible change.

11.1.1 Functions

In order to have as low impact on the normal operation as possible the transparent mode is designed to be used in the test frequency band only.

In transparent mode many functions of the normal mode are not available:

- 3T MRS
- Rank combining
- RCW access
- Parity checking
- Powerdown
- Address Inversion

During transparent mode inband writing of the control registers is not available. The only way to change the settings is to write them via SMBus.

The only way to leave transparent mode without SMBus is by a device reset.

Independent functions like voltage referencing and SMBus do not change in this mode.

11.1.2 CA Signal mapping

All address and command signals are copied from the Dxy inputs to the Qxy output without modification:

- DAx -> QAAx and QBAx
- DBAx -> QABAx and QBBAx
- DRAS_n -> QARAS_n and QBRAS_n
- DCAS_n -> QACAs_n and QBCAS_n
- DWE_n -> QAWE_n and QBWE_n

For the control signals some remapping is needed because the number of independent outputs can be higher then the number of independent inputs.

- DCKE0 -> QACKE0 and QBCKE0 and QACKE2 and QBCKE2
- DCKE1 -> QACKE1 and QBCKE1 and QACKE3 and QBCKE3
- DODT0 -> QAODT0 and QBODT0
- DODT1/DCKE3 -> QAODT1 and QBODT1

For CS the setting of the transparent mode control word Table 166 changes the mapping of inputs to outputs:

- setting 4'b00xx:
  - DCS0_n -> QACS0_n and QBCS0_n
  - DCS1_n -> QACS1_n and QBCS1_n
  - DCS2_n -> QACS2_n and QBCS2_n
  - DCS3_n -> QACS3_n and QBCS3_n
- setting 4'b01xx:
  - DCS0_n -> QACS0_n
  - DCS1_n -> QACS1_n
  - DCS2_n -> QACS2_n
  - DCS3_n -> QACS3_n
  - DCS4_n -> QBCS0_n
  - DCS5_n -> QBCS1_n
  - DCS6_n -> QBCS2_n
  - DCS7_n -> QBCS3_n
- setting 4'b10xx:
  - DCS0_n -> QACS0_n
  - DCS1_n -> QACS2_n
  - DCS2_n -> QBCS0_n
  - DCS3_n -> QBCS2_n
  - 1'b1 -> QACS1_n and QBCS1_n and QACS3_n and QBCS3_n
- setting 4'b11xx:
  - DCS0_n -> QACS1_n
  - DCS1_n -> QACS3_n
  - DCS2_n -> QBCS1_n
  - DCS3_n -> QBCS3_n
  - 1'b1 -> QACS0_n and QBCS0_n and QACS2_n and QBCS2_n

CA input signals will provide IBT as defined in registers F0RC8, F1RC0, F1RC1, F1RC2

11.1.3 CA timing

All CA signals are sampled and retimed like in normal mode. The Clock frequency for this test mode can be between 70MHz and 300MHz.

By this the LRDIMM looks almost like a RDIMM to the tester. The exact timing of the CA signals at the DRAM does not change from normal mode and therefore no extra trimming is needed in order for the DRAM to understand the commands.

11.1.4 DQ Functionality and Timing

The automatic switching between write and read of normal operation is not available. For selecting the direction of the data bus the PAR_IN ball is used.

The switch occurs asynchronously on the change of the PAR_IN signal:
- PAR_IN = 1'b0: Write (DQ->MDQ)
- PAR_IN = 1'b1: Read (MDQ->DQ)

The data bus is redriven from input to output in an asynchronous way. The direction for DQ and DQS is always the same.

DQSs are treated as differential. This means if a DQSx_t and the corresponding DQSx_c are both high or both low the associated MDQSx_t and MDQSx_c will be invalid.

Since the inputs are directly redriven to the outputs floating inputs can generate noise on the outputs.

The termination scheme on the data bus depends on the redriving direction:
- Write direction: Host side (DQx) provides ODT with RTT_NOM value (F3RC0)
- Read direction: DRAM side (MDQx) provides ODT with RTT_NOM value (F3RC8)

ODT can be disabled by according setting in F3RC0 and F3RC8

11.1.5 Entry Procedure

To enter the transparent mode the following procedure is used:
- Release Reset
- Let PLL lock
- Setup test frequency band, supply voltage and CA timing parameters
- Let PLL relock
- Configure IBT, ODT, Ron, Transparent mode CS settings
- Turn on transparent mode
- Wait t_{TRMEN}

11.1.6 Exit Procedure

To exit transparent mode the following procedure is used:
- Disable transparent DQ/CA mode by SM-Bus
  - If no SM-Bus access is possible: reset the device
- Wait t_{STAB}

11.1.7 Control Word

To enable transparent mode and to select the CS mapping a control word is needed:

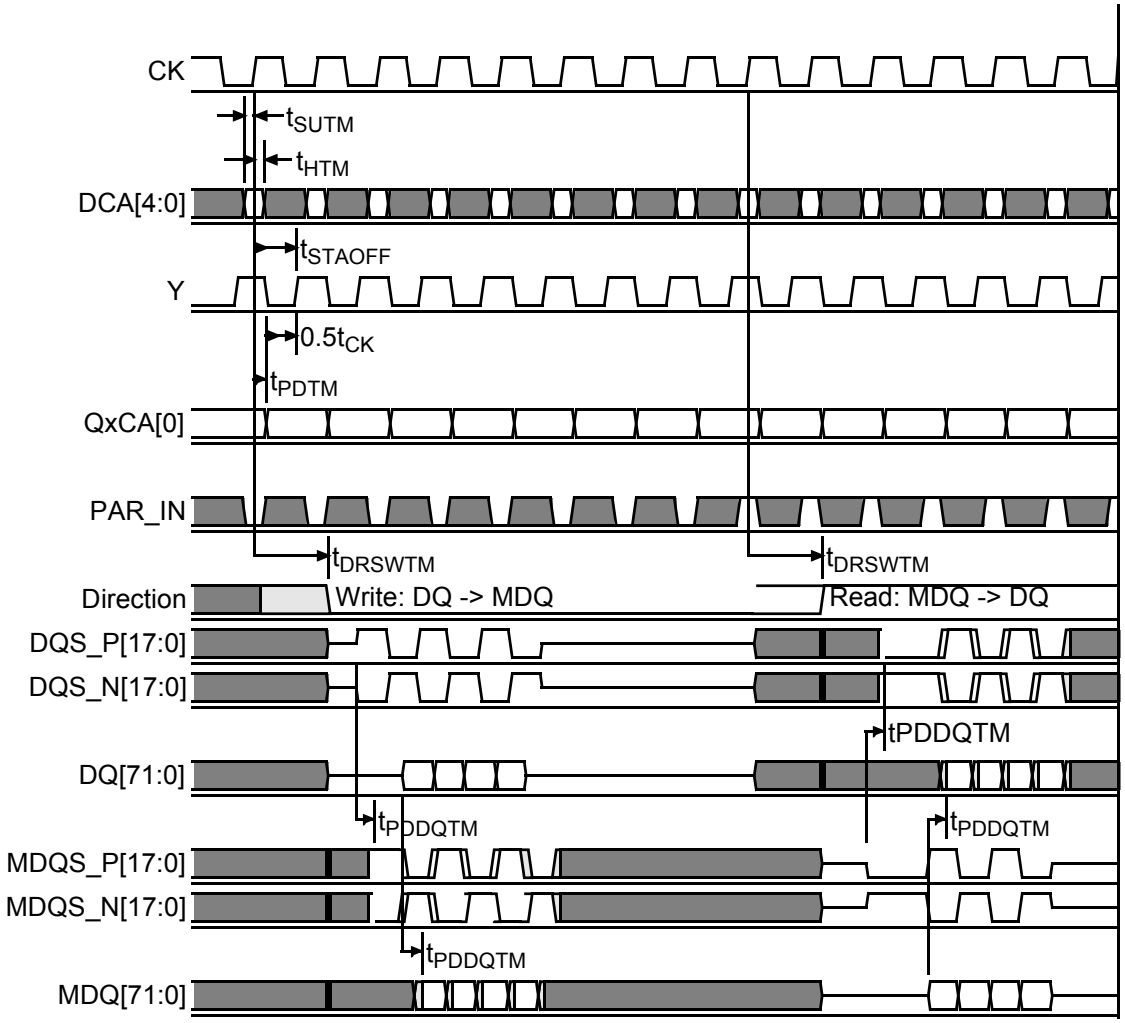
Table 166 — F2RC0: Transparent Mode

Input				Definition	Encoding
DBA1	**DBA0**	**DA4**	**DA3**		
X	X	X	**0**	Enable transparent mode	**Normal operation**
X	X	X	1		Transparent mode enabled
X	X	0	X	Reserved	
X	X	1	X		
0	**0**	X	X	Chip select multiplication in transparent mode	**QACS_n[3:0]=DCS_n[3:0], QBCS_n[3:0]=DCS_n[3:0]**
0	1	X	X		QACS_n[3:0]=DCS_n[3:0], QBCS_n[3:0]=DCS_n[7:4]
1	0	X	X		QACS_n[2,0]=DCS_n[1:0], QBCS_n[2,0]=DCS_n[3:2], QACS_n[3,1]=2'b11, QBCS_n[3,1]=2'b11
1	1	X	X		QACS_n[2,0]=2'b11, QBCS_n[2,0]=2'b11, QACS_n[3,1]=DCS_n[1:0], QBCS_n[3,1]=DCS_n[3:2]

11.1.8 Timing diagram

In transparent mode all command, address and control signals are sampled. The data bus is forwarded analog and the direction of the bus is determined by the PAR_IN signal.

For the switch from write to read or vice versa some timing is involved.



The timing parameters used here are:

t_{SUTM} : setup time in transparent mode

t_{HTM} : hold time in transparent mode

t_{PDTM} : CA bus propagation delay in transparent mode

t_{DRSWTM}: direction switch time

t_{PDDQTM} : DQ bus propagation delay in transparent mode

Figure 67 — Transparent Mode Timing Diagram

12 LAI Mode

12.1 LAI Mode Support (Optional)

13 SMBus Interface and Temperature Sensor

For all configuration and temperature sensor registers, the Memory Buffer supports register access mechanisms through SMBus as well as through in-band channel commands. The registers may be read by software from the SMBus host at any time the MB is powered on, except in the MB clock stopped power down mode or when the device RESET_n pin is asserted.

The MB SMBus interface shall not initiate clock stretching.

The MB SMBus interface must co-exist with an external Temperature Sensor/SPD device on an LRDIMM and shall not inhibit the operation of the SMBus when it has no V_{DD} but V_{CCSPD}.

13.1 SMBus 2.0 Specification Compatibility

The principal requirement from the SMBus 2.0 specification is support of the “high power” bus electrical specifications described in the layer 1 (Physical layer) chapter.

For the simple register access requirements of LRDIMM, no layer 2 (Link layer) or layer 3 (Network layer) extensions provided by the 2.0 specification are used. In particular, there is no support for Address Resolution Protocol (ARP). Additionally, only a subset of the network packet protocols described in the standard are needed and these are described below.

MB’s are required to support read and write transactions without requiring clock stretching in order to simplify host controller requirements. For similar reasons, MB’s shall not master SMBus transactions in normal operation.

13.2 Operating Range

The MB SMBus interface is designed to operate at a voltage range of 3.0-3.6 V and shall operate up to a maximum frequency of 100 kHz.

13.3 External Pins

The MB SMBus interfaces uses the following five external device pins, as well as an EVENT_n pin that is described in 13.7, Temperature Sensor (TS).

13.3.1 Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to V_{CCSPD}. (Figure 68 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

13.3.2 Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-ORed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to the most positive V_{CCSPD} in the SMBUS chain. (Figure 68 indicates how the value of the pull-up resistor can be calculated).

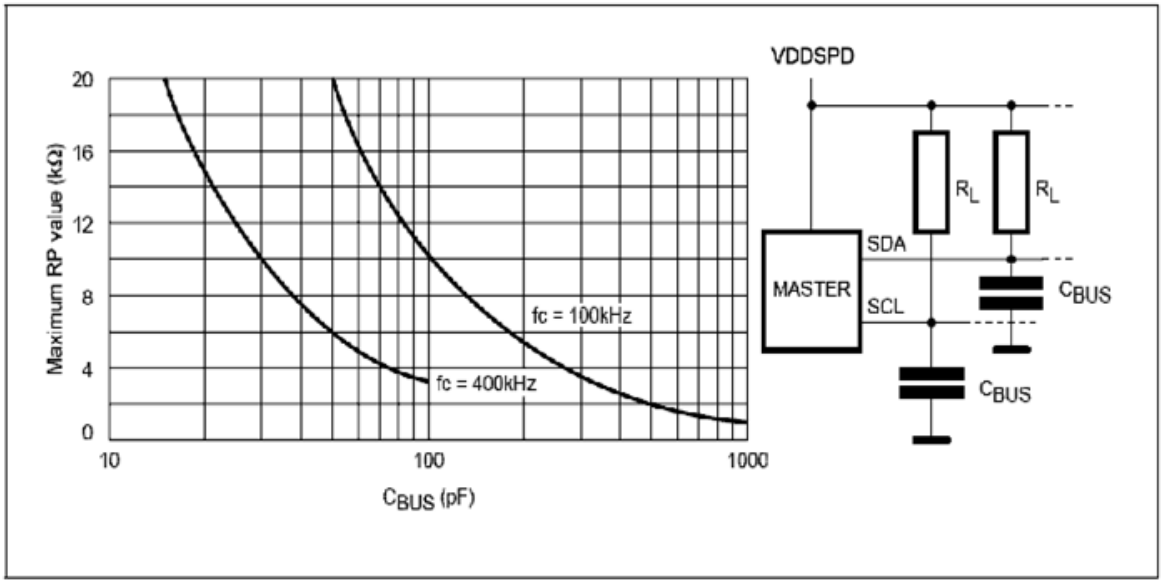


Figure 68 — Maximum R_L Value Versus Bus Capacitance (C_{BUS}) for an SMBUS Bus

13.3.3 Select Address (SA0, SA1, SA2)

These input signals are used to set the value of the three least significant bits of the 7-bit Slave Address. In the Dual Inline Memory Module (DIMM) application, the Select Address inputs SA1 and SA2 of the MB must be connected to V_{SS} or V_{CCSPD} directly (that is without using a pull-up or pull-down resistor) through the DIMM socket (see Table 69). SA0 is connected through a series resistor used during high voltage programming of the SPD device on the DIMM. The pull-up resistors needed for correct operation of the SMBUS bus are located on the motherboard. The device shall interpret V_{CCSPD} on the SA[2:0] pins as a logic '1' and V_{SS} as a logic '0'.

Table 167 — Unique Addressing of SPDs in DIMM Applications

DIMM Position	SA2	SA1	SA0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
NOTE 0 = V_{SS}, 1 = V_{CCSPD}			

The address bits (SA0-SA2) of the buffer are connected to corresponding address pins (SA0-SA2) of the SPD and/or TSOD device on the DIMM. The MB EVENT_n pin is shared with the EVENT_n pin of the external SPD/TS device, see Figure 69.

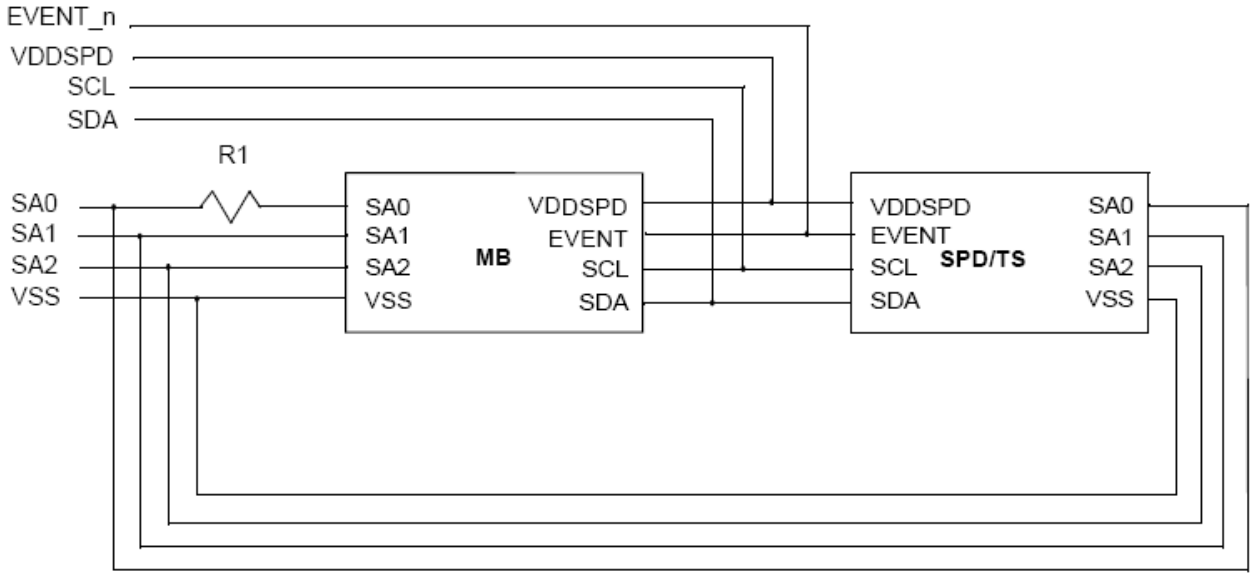


Figure 69 — SMBUS WIRING DIAGRAM

The EVENT_n pin is expected to be used in a wire-OR configuration with a pullup resistor to V_{CCSPD} on the motherboard. In this configuration, EVENT_n should be programmed for the active low mode. Also note that comparator mode or TCRIT-only mode for EVENT_n on a wire-OR bus will show the combined results of all devices wired to the EVENT_n signal.

13.4 System Management Access

System Management software in the platform can initiate system management access to the configuration and temperature sensor registers. This can be done through SMBus accesses.

Since the MB can get read or write access to the DRAMs behind the buffer through MEMBIST, access to MB SMBus registers is controlled by access control bits - see control word and CSR chapters for details.

The mechanism for the Server Management (SM) software to access configuration registers is through a *SMBus Specification*, Rev. 2.0-compliant slave port. Memory Buffer components contain this slave port and allow access to the configuration registers.

SMBus operations are made up of two major steps: (1) writing information to registers within each component and (2) reading configuration registers from each component. The following sections will describe the protocol for an SMBus master to access an Memory Buffer component's internal configuration registers. Refer to the *SMBus Specification*, Rev. 2.0 for the bus protocol, timings, and waveforms.

13.4.1 Slave Address

The 7-bit slave address used for each primitive SMBus transaction is determined by the SA[2:0] pins and the 4-bit device address.

- Primary SMBus address (BFUNC pin strapped to Vss):
  - — Slave Address[6:3] = 4'b**1011**
  - — Slave Address[2:0] = SA[2:0]
- Secondary SMBus address (e.g. for a "repeater" MB; BFUNC pin strapped to Vdd):
  - — Slave Address[6:3] = 4'b**1000**
  - — Slave Address[2:0] = SA[2:0]

13.4.2 Supported SMBus Commands

The Memory Buffer component's SMBus Rev. 2.0 slave port supports register reads and writes built out of the following four SMBus primitive commands:

Block Write **Byte Write**

Block Read **Byte Read**

The Memory Buffer is not required to support block accesses larger than a double word.

Each SMBus transaction has an 8-bit command driven by the master. The format for this command is illustrated in Table 70 below.

Table 168 — SMBus command Encoding

7	6	5	4	3:2	1:0
Begin	End	Rsvd	PEC_en	Internal Command: 00 - Read DWord 01 - Write Byte 10 - Write Word 11 - Write DWord	SMBus Command: 00 - Byte 01 - *Rsvd* 10 - Block 11 - *Rsvd*

The *Begin* bit indicates the first transaction of a read or write sequence.

The *End* bit indicates the last transaction of a read or write sequence.

The *PEC_en* bit enables the 8-bit PEC generation and checking logic.

The *Internal Command* field specifies the internal command to be issued by the SMBus slave logic. Note that the Internal Command must remain consistent (i.e. not change) during a sequence that accesses a configuration register. Operation cannot be guaranteed if it is not consistent when the command setup sequence is done.

The *SMBus Command* field specifies the SMBus command to be issued on the bus. This field is used as an indication of the length of transfer so the slave knows when to expect the PEC packet (if enabled).

Reserved bits should be written to zero to preserve future compatibility.

Hosts are required to form commands that are internally self consistent. The length indicated by the internal command should be consistent with the byte count and the MB behavior will be undefined when the internal command is inconsistent with the bye count.

13.4.3 MB Register Access Protocols

Sequences of these basic commands will initiate internal accesses to the component's configuration registers.

Each configuration read or write first consists of an SMBus write sequence which initializes the register's address. The term sequence is used since these variables may be written with a single block write or multiple byte writes. Once these parameters are initialized, the SMBus master can initiate a read sequence (which performs a configuration read) or a write sequence (which performs a configuration write).

NOTE All MB control words are located in the SMBus Function 0 address space (even the F1RCnn to F15RCnn control words). This leaves the address space of the other seven SMBus functions available for vendor specific test and debug registers which are not defined in this standard.

Table 169 — SMBus Protocol Addressing fields

Address Field Name	Bits	Description
Reserved	7:0	Reserved - MB may alias all these addresses to 00h
Dev	3:0	Reserved - MB may alias all these addresses to 00h
Function	3:0	Function Address
Reg_Num[15:8]	7:0	Reserved - MB may alias all these addresses to 00h
Reg_Num[7:0]	7:0	Register Address within Function

13.4.3.1 Configuration Register Read Protocol

Configuration reads are accomplished through an SMBus write(s) and later followed by an SMBus read. The write sequence is used to initialize the Bus Number, Device, Function, and Register Number for the configuration access. The writing of this information can be accomplished through any combination of the supported SMBus write commands (Block, Byte). The *Internal Command* field for each write should specify Read DWord.

All SMBus configuration reads should be Dword aligned. The MB will ignore the lowest two bits of the register address and return the four bytes within a DWord in the byte order shown in the following examples, i.e. most significant byte (Data[31:24]) first and least significant byte (Data[7:0]) last.

After all the information is set up, the last write (*End* bit is set) initiates an internal configuration read. If an error occurs during the internal access, the last write command will receive a NACK. A status field indicates abnormal termination and contains status information such as target abort, master abort, and time-outs. The status field encoding is defined Table 170.

Table 170 — Status Field Encoding for SMBus Reads

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Internal Target Abort
3:1	Reserved
0	Successful

13.4.3.1 Configuration Register Read Protocol (cont'd)

Examples of configuration reads are illustrated below. All of these examples have PEC (Packet Error Code) enabled. If the master does not support PEC, then bit 4 of the command would be cleared and there would not be a PEC phase. For the definition of the diagram conventions below, refer to the *SMBus Specification*, Rev. 2.0. For SMBus read transactions, the last byte of data (or the PEC byte if enabled) is NACKed by the master to indicate the end of the transaction. For diagram compactness, "Register Number[]" is also sometimes referred to as "Reg Number" or "Reg Num".

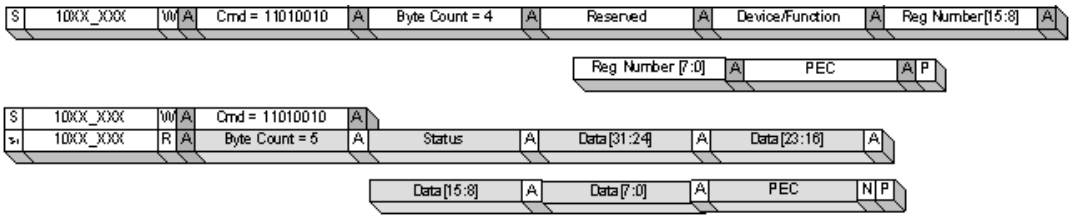


Figure 70 — SMBus Configuration Read (Block Write / Block Read, PEC enabled)

The following example uses byte writes and reads.

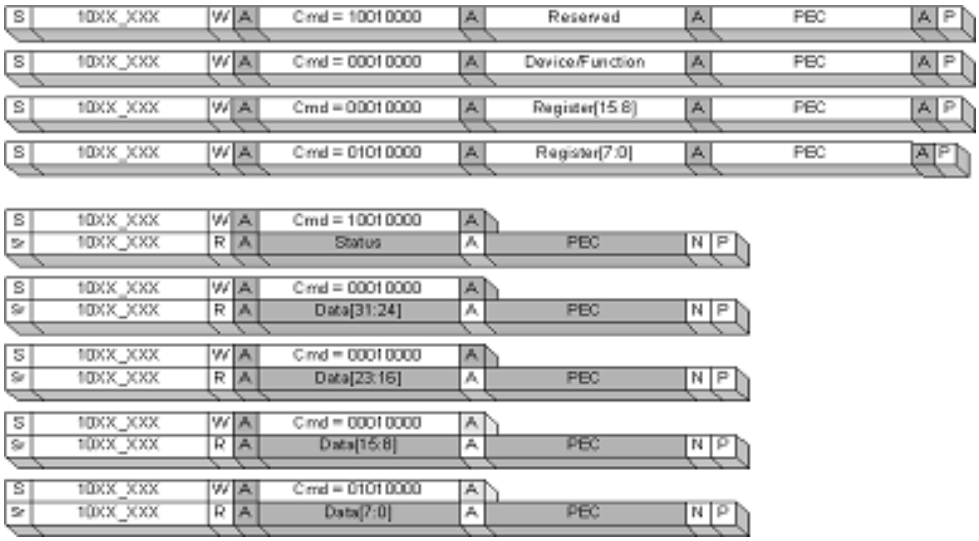


Figure 71 — SMBus Configuration Read (Write Bytes / Read Bytes, PEC enabled)

13.4.3.2 Configuration Register Write Protocol

Configuration writes are accomplished through a series of SMBus writes. As with configuration reads, a write sequence is first used to initialize the Bus Number, Device, Function, and Register Number for the configuration access. The writing of this information can be accomplished through any combination of the supported SMBus write commands (Block, Byte).

On SMBus, there is no concept of byte enables. Therefore, the Register Number written to the slave is assumed to be aligned to the length of the Internal Command. In other words, for a Write Byte internal command, the Register Number specifies the byte address. For a Write DWord internal command, the two least-significant bits of the Register Number are ignored. This is different from PCI where the byte enables are used to indicate the byte of interest.

After all the information is set up, the SMBus master initiates one or more writes which sets up the data to be written. The final write (*End* bit is set) initiates an internal configuration write. If an error occurred, the SMBus interface NACKs the last write operation just before the stop bit.

Examples of configuration writes are illustrated below. For the definition of the diagram conventions below, refer to the *SMBus Specification*, Rev. 2.0.

Figure 72 — SMBus Configuration Double Word Write (Block Write, PEC enabled)

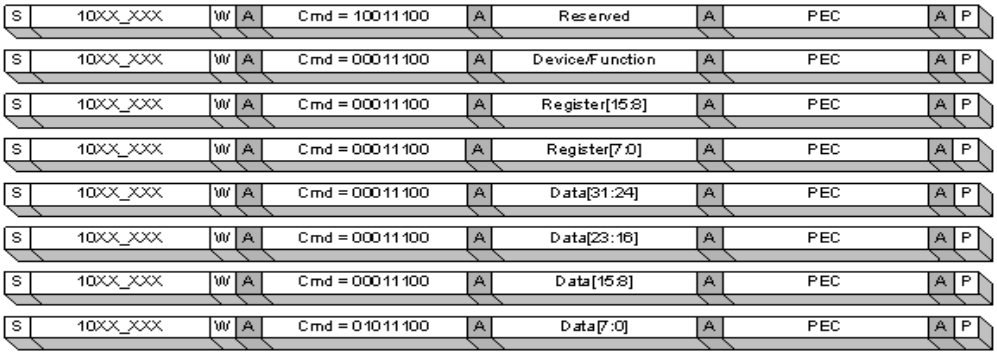


Figure 73 — SMBus Configuration Double Word Write (Write Bytes, PEC enabled)

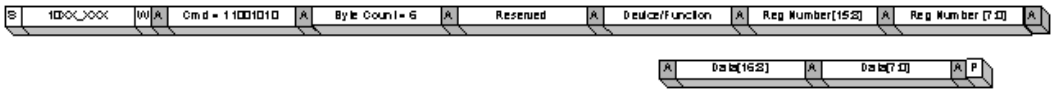


Figure 74 — SMBus Configuration Word Write (Block Write, PEC disabled)

13.4.3.2 Configuration Register Write Protocol (cont'd)

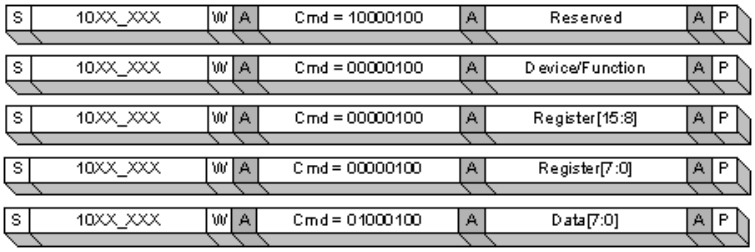


Figure 75 — SMBus Configuration Byte Write (Write Bytes, PEC disabled)

13.5 SMBus Error Handling

The SMBus slave interface handles two types of errors: internal and PEC. These errors manifest as a Not-Acknowledge (NACK) for the read command (*End* bit is set). If an internal error occurs during a configuration write, the final write command receives a NACK just before the stop bit. If the master receives a NACK, the entire configuration transaction should be reattempted.

If the master supports packet error checking (PEC) and the PEC_en bit in the command is set, then the PEC byte is checked in the slave interface. If the check indicates a failure, then the slave will NACK the PEC packet.

13.6 SMBus Resets

13.6.1 SMBus Interface State Machine Reset

The slave interface state machine can be reset by the master in two ways:

- The master holds SCL low for 35ms cumulative. Cumulative in this case means that all the “low time” for SCL is counted between the Start and Stop bit. If this totals 35ms before reaching the Stop bit, the interface is reset.
  - — Timing is set up to be 35ms for 800MT/s and may scale down at higher frequencies
    * 26.25ms at 1066MT/s
    * 21ms at 1333MT/s
    * 17.5ms at 1600MT/s
    * 15ms at 1866MT/s
    * 13.1ms at 2133MT/s
- The master holds SCL continuously high for 100us.
  - — Timing is set up to be 100us for 800MT/s and may scale down at higher frequencies
    * 75us at 1066MT/s
    * 60us at 1333MT/s
    * 50us at 1600MT/s
    * 42.9us at 1866MT/s
    * 37.5us at 2133MT/s

13.6.2 SMBus transactions during reset

Since the configuration registers are affected by the RESET_n pin, SMBus masters will NOT be able to access the MB registers while the device is reset.

13.7 Temperature Sensor (TS)

The MB contains an SMBus accessible on-die temperature sensor that shall meet the following requirements:

Buffer temperature sensor		
Grade	Sensor Accuracy	Supply Voltage
B	1.0 °C max from 75 °C-95 °C	3.0 to 3.6 V
	2.0 °C max from 40 °C-125 °C	
	3.0 °C max from -20 °C-125 °C	
C	2.0 °C max from 75 °C-95 °C	3.0 to 3.6 V
	3.0 °C max from 40 °C-125 °C	
	4.0 °C max from -20 °C-125 °C	

- Ambient temperature (TA) sense through an operating range of -20 °C to +125 °C
- Typical accuracy of 2.0 °C or 3.0 °C for the entire operating range from -20 °C to +125 °C
- Typical accuracy of 1.0 °C or 2.0 °C accuracy for the monitor range from +40 °C to +125 °C
- Support for higher accuracy of 0.5 °C or 1.0 °C (typical) over the active range from +75 °C to +95 °C
- Temperature sample rate minimum of 8 samples/s
- Selectable 0, 1.5 °C, 3 °C, 6 °C Hysteresis on set point

The MB TS continuously monitors the temperature and updates the temperature data minimum of eight times per second. Temperature data is latched internally by the device and may be read by software from the SMBus host at any time the MB is powered on, except in the MB clock stopped power down mode or when the device RESET_n pin is asserted. Internal registers are used to configure both the TS performance and response to over-temperature conditions. The device contains programmable high, low, and critical temperature limits. The buffer EVENT_n pin can be configured as active high or active low and can be configured to operate as an interrupt or as a comparator output.

13.7.1 EVENT_n Pin

The EVENT_n pin is an open drain output that requires a pull-up to V_{CCSPD} on the system motherboard or integrated into the master controller. EVENT_n has three operating modes, depending on configuration settings and any current out-of-limit conditions. These modes are Interrupt, Comparator, or TCRIT Only.

In Interrupt Mode the EVENT_n pin will remain asserted until it is released by writing a '1' to the "Clear Event" bit in the Status Register. The value to write is independent of the EVENT_n polarity bit.

In Comparator Mode the EVENT_n pin will clear itself when the error condition that caused the pin to be asserted is removed. When the temperature is compared against the TCRIT limit, then this mode is always used.

Finally, in the TCRIT Only Mode the EVENT_n pin will only be asserted if the measured temperature exceeds the TCRIT Limit. Once the pin has been asserted, it will remain asserted until the temperature drops below the TCRIT Limit minus the TCRIT hysteresis. Figure 76 illustrates the operation of the different modes over time and temperature.

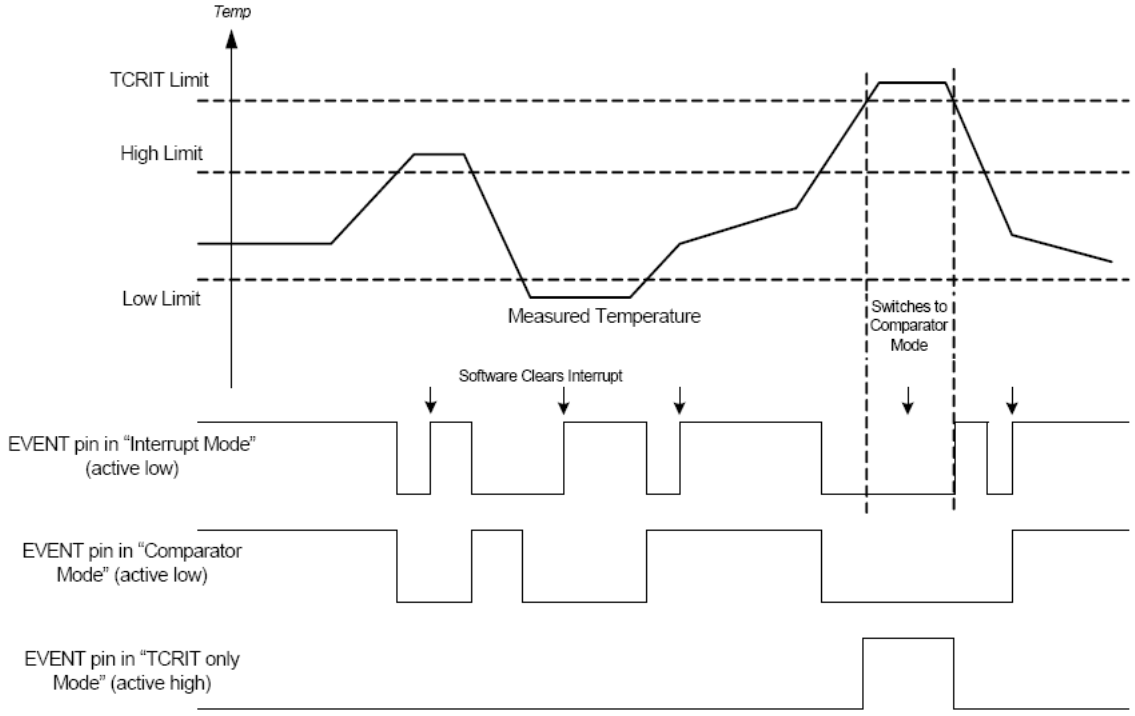


Figure 76 — EVENT_n Pin Mode functionality

Systems that use the active high mode for EVENT_n must be wired point to point between the buffer and the sensing controller. Wire-OR configurations should not be used with active high EVENT_n since any device pulling the EVENT_n signal low will mask the other devices on the bus. Also note that the normal state of EVENT_n in active high mode is a 0 which will constantly draw power through the pull-up resistor.

13.7.2 TS Register Address Map

The Temperature Register Set stores the temperature data, limits, and configuration values. All 8-bit TS registers are in the register address space from 0xA0 through 0xAB (see Table 73 for detailed information), accessed through block or byte read and write commands.

Table 171 — Temperature Register Addresses

REG_ NUM	R/W	NAME	FUNCTION	DEFAULT
A0h	R	Capabilities LSB [7:0]	Indicates the functions and capabilities of the temperature sensor	0F or 2F
A1h		Capabilities MSB [15:8]		00
A2h	R/W	Configuration LSB [7:0]	Controls the operation of the temperature monitor	00
A3h		Configuration MSB [15:8]		00
A4h	R/W	High Limit LSB [7:0]	Temperature High Limit	00
A5h		High Limit MSB [15:8]		00
A6h	R/W	Low Limit LSB [7:0]	Temperature Low Limit	00
A7h		Low Limit MSB [15:8]		00
A8h	R/W	TCRIT Limit LSB [7:0]	Critical Temperature	00
A9h		TCRIT Limit MSB [15:8]		00
AAh	R	Ambient Temperature LSB [7:0]	Current Ambient temperature	N/A
ABh		Ambient Temperature MSB [15:8]		

13.7.3 Capabilities Register

Table 172 — Capabilities Register

REG_ NUM	R/W	B15 / B7	B14 / B6	B13 / B5	B12 / B4	B11 / B3	B10 / B2	B9 / B1	B8 / B0	DEFAULT
00	R	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	000F or 002F
		EVSD	TMOUT	X	TRES[1:0]		RANGE	ACC	EVENT	

The Capabilities Register indicates the supported features of the temperature sensor.

Bits 15 - Bit 8 - RFU - Reserved for future use. These bits will always read ‘0’ and writing to them will have no effect.

Bit 7 - EVSD - EVENT_n with Shutdown action.

‘0’ - The EVENT_n output freezes in its current state when entering shutdown. Upon exiting shutdown, the EVENT_n output remains in the previous state until the next thermal sample is taken, or possibly sooner if EVENT_n is programmed for comparator mode.

‘1’ - The EVENT_n output is deasserted (not driven) when entering shutdown, and remains deasserted upon exit from shutdown until the next thermal sample is taken, or possibly sooner if EVENT_n is programmed for comparator mode.

Bit 6 - TMOUT - Bus timeout period for thermal sensor access during normal operation. Note that bus timeout support is optional in shutdown mode.

‘0’ - NA

‘1’ - Parameter $t_{TIMEOUT}$ is supported within the range of 25 to 35 ms (SMBus compatible).

Bit 5 - X - May be 0 or 1; applications must accept either code.

Bits 4 - 3 - TRES[1:0] - Indicates the resolution of the temperature monitor as shown in Table 75.

Table 173 — TRES Bit Decode

TRES[1:0]		TEMPERATURE RESOLUTION
TRES1	TRES0	
0	0	0.5 °C (9-bit)
0	1	0.25 °C (10-bit) (default)
1	0	0.125 °C (11-bit)
1	1	0.0625 °C (12-bit)

Bit 2 - RANGE - Indicates the supported temperature range.

‘0’ - The temperature monitor clamps values lower than 0 °C.

‘1’ - The temperature monitor can read temperatures below 0 °C and sets the sign bit appropriately.

Bit 1 - ACC - Indicates the supported temperature accuracy.

‘0’ - The temperature monitor has ±2 °C typ accuracy over the active range (75 °C to 95 °C) and 3°C typ accuracy over the monitoring range (40 °C to 125 °C)

‘1’ - The temperature monitor has ±1 °C typ accuracy over the active range (75 °C to 95 °C) and 2°C typ accuracy over the monitoring range (40 °C to 125 °C)

Bit 0 - EVENT - Indicates whether the temperature monitor supports interrupt capabilities

‘0’ - NA

‘1’ - The device supports interrupt capabilities.

13.7.4 Configuration Register

Table 174 — Configuration Register

REG_ NUM	R/W	B15 / B7	B14 / B6	B13 / B5	B12 / B4	B11 / B3	B10 / B2	B9 / B1	B8 / B0	DEFAULT
01	R/W	RFU	RFU	RFU	RFU	RFU	HYST[1:0]		SHDN	0000
		TCRIT_ LOCK	EVENT _LOCK	CLEAR	EVENT _ STS	EVENT _CTRL	TCRIT_ ONLY	EVENT _ POL	EVENT _MODE	

The Configuration Register holds the control and status bits of the EVENT_n pin as well as general hysteresis on all limits.

Bits 15 - 11 - RFU - Reserved for future use. These bits will always read ‘0’ and writing to them will have no affect. For future compatibility, all RFU bits must be programmed as ‘0’.

Bits 10 - 9 - HYST[1:0] - Control the hysteresis that is applied to all limits as shown in Table 77. This hysteresis applies to all limits when the temperature is dropping below the threshold so that once the temperature is above a given threshold, it must drop below the threshold minus the hysteresis in order to be flagged as an interrupt event. Note that hysteresis is also applied to EVENT_n pin functionality. When either of the lock bits is set, these bits cannot be altered.

Table 175 — HYST Bit Decode

HYST[1:0]		HYSTERESIS
HYST1	HYST0	
0	0	disable hysteresis (default)
0	1	1.5 °C
1	0	3 °C
1	1	6 °C

Bit 8 - SHDN - Shutdown. The thermal sensing device and A/D converter are disabled to save power, no events will be generated. When either of the lock bits is set, this bit cannot be set until unlocked. However it can be cleared at any time. When in shutdown mode, the device still responds to commands normally, however bus timeout may or may not be supported in this mode.

‘0’ (default) - The thermal sensor is active and converting.

‘1’ - The thermal sensor is disabled and will not generate interrupts or update the temperature data.

Bit 7 - TCRIT_LOCK - Locks the TCRIT Limit Register from being updated.

‘0’ (default) - The TCRIT Limit Register can be updated normally.

‘1’ - The TCRIT Limit Register is locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal power on reset.

Bit 6 - EVENT_LOCK - Locks the High and Low Limit Registers from being updated.

‘0’ (default) - The High and Low Limit Registers can be updated normally.

‘1’ - The High and Low Limit Registers are locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal power on reset.

Bit 5 - CLEAR - Clears the EVENT_n pin when it has been asserted. This bit is write only and will always read ‘0’.

‘0’ - does nothing

‘1’ - The EVENT_n pin is released and will not be asserted until a new interrupt condition occurs. This bit is ignored if the device is operating in Comparator Mode. This bit is self clearing.

Bit 4 - EVENT_STS - Indicates if the EVENT_n pin is asserted. This bit is read only.

‘0’ (default) - The EVENT_n pin is not being asserted by the device.

‘1’ - The EVENT_n pin is being asserted by the device.

Bit 3 - EVENT_CTRL - Masks the EVENT_n pin from generating an interrupt. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.

‘0’ (default) - The EVENT_n pin is disabled and will not generate interrupts.

‘1’ - The EVENT_n pin is enabled.

Bit 2 - TCRIT_ONLY - Controls whether the EVENT_n pin will be asserted from a high / low out-of-limit condition. When the EVENT_LOCK bit is set, this bit cannot be altered.

‘0’ (default) - The EVENT_n pin will be asserted if the measured temperature is above the High Limit or below the Low Limit in addition to if the temperature is above the TCRIT Limit.

‘1’ - The EVENT_n pin will only be asserted if the measured temperature is above the TCRIT Limit.

Bit 1 - EVENT_POL - Controls the “active” state of the EVENT_n pin. The EVENT_n pin is driven to this state when it is asserted. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.

‘0’ (default) - The EVENT_n pin is active low. The “active” state of the pin will be logical ‘0’.

‘1’ - The EVENT_n pin is active high. The “active” state of the pin will be logical ‘1’.

Bit 0 - EVENT_MODE - Controls the behavior of the EVENT_n pin. The EVENT_n pin may function in either comparator or interrupt mode. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.

‘0’ - The EVENT_n pin will function in comparator mode

‘1’ - The EVENT_n pin will function in interrupt mode

13.7.5 Temperature Registers

13.7.5.1 Temperature Register Value Definitions

Temperatures in the High Limit Register, Low Limit Register, TCRIT Register, and Temperature Data Register are expressed in two's complement format. Bits B12 through B2 for each of these registers are defined for all device resolutions as defined in the TRES field of the Capabilities Register, hence a 0.25 °C minimum granularity is supported in all registers. Examples of valid settings and interpretation of temperature register bits:

Temperature Register Coding Examples		
B15~B0 (binary)	**Value**	**Units**
xxx0 0000 0010 11xx	+2.75	°C
xxx0 0000 0001 00xx	+1.00	°C
xxx0 0000 0000 01xx	+0.25	°C
xxx0 0000 0000 00xx	0	°C
xxx1 1111 1111 11xx	-0.25	°C
xxx1 1111 1111 00xx	-1.00	°C
xxx1 1111 1101 01xx	-2.75	°C

The TRES field of the Capabilities Register optionally defines higher resolution devices. For compatibility and simplicity, this additional resolution affects only the Temperature Data Register but none of the Limit Registers. When higher resolution devices generate status or EVENT_n changes, only bits B12 through B2 are used in the comparison; however, all 11 bits (TRES[1-0] = 10) or all 12 bits (TRES[1-0] = 11) are visible in reads from the Temperature Data Register.

When a lower resolution device is indicated in the Capabilities Register (TRES[1-0] = 00), the finest resolution supported is 0.5 °C. When this is detected, bit 2 of all Limit Registers should be programmed to 0 to assure correct operation of the temperature comparators.

13.7.5.2 High Limit Register

The temperature limit registers (High, Low, and TCrit) define the temperatures to be used by various on-chip comparators to determine device temperature status and thermal EVENTs. For future compatibility, unused bits "-" must be programmed as 0.

Table 176 — High Limit Register

REG_ NUM	R/W	B15 / B7	B14 / B6	B13 / B5	B12 / B4	B11 / B3	B10 / B2	B9 / B1	B8 / B0	DEFAULT
02	R/W	-	-	-	Sign	128	64	32	16	
		8	4	2	1	0.5	0.25	-	-	

The High Limit Register holds the High Limit for the nominal operating window. When the temperature rises above the High Limit, or drops below or equal to the High Limit, then the EVENT_n pin is asserted (if enabled). If the EVENT_LOCK bit is set in the Configuration Register see Table 76 on page 231), then this register becomes read-only.

13.7.5.3 Low Limit Register

Table 177 — Low Limit Register

REG_ NUM	R/W	B15 / B7	B14 / B6	B13 / B5	B12 / B4	B11 / B3	B10 / B2	B9 / B1	B8 / B0	DEFAULT
03	R/W	-	-	-	Sign	128	64	32	16	
		8	4	2	1	0.5	0.25	-	-	

The Low Limit Register holds the lower limit for the nominal operating window. When the temperature drops below the Low Limit or rises up to meet or exceed the Low Limit, then the EVENT_n pin is asserted (if enabled). If the EVENT_LOCK bit is set in the Configuration Register see Table 76), then this register becomes read-only.

13.7.5.4 TCRIT Limit Register

Table 178 — TCRIT Limit Register

REG_ NUM	R/W	B15 / B7	B14 / B6	B13 / B5	B12 / B4	B11 / B3	B10 / B2	B9 / B1	B8 / B0	DEFAULT
04	R/W	-	-	-	Sign	128	64	32	16	
		8	4	2	1	0.5	0.25	-	-	

The TCRIT Limit Register holds the TCRIT Limit. If the temperature exceeds the limit, the EVENT_n pin will be asserted. It will remain asserted until the temperature drops below or equal to the limit minus hysteresis. If the TCRIT_LOCK bit is set in the Configuration Register (see Table 76), then this register becomes read-only.

13.7.5.5 Temperature Data Register

Table 179 — Temperature Data Register

REG_ NUM	R/W	B15 / B7	B14 / B6	B13 / B5	B12 / B4	B11 / B3	B10 / B2	B9 / B1	B8 / B0	DEFAULT
05	R	TCRIT	HIGH	LOW	Sign	128	64	32	16	N/A (0000)
		8	4	2	1	0.5	0.25*	0.125*	0.0625*	
* Resolution defined based on value of TRES field of the Capabilities Register. Unused/unsupported bits will read as 0.										

The Temperature Data Register holds the 10-bit + sign data for the internal temperature measurement as well as the status bits indicating which error conditions, if any, are active. The encoding of bits B12 through B0 is the same as for the temperature limit registers.

Bit 15 - TCRIT - When set, the temperature is above the TCRIT Limit. This bit will remain set so long as the temperature is above TCRIT and will automatically clear once the temperature has dropped below the limit minus the hysteresis.

Bit 14 - HIGH - When set, the temperature is above the High Limit. This bit will remain set so long as the temperature is above the HIGH limit. Once set, it will only be cleared when the temperature drops below or equal to the HIGH Limit minus the hysteresis.

Bit 13 - LOW - When set, the temperature is below the Low Limit. This bit will remain set so long as the temperature is below the Low Limit minus the hysteresis. Once set, it will only be cleared when the temperature meets or exceeds the Low Limit.

13.7.5.5 Temperature Data Register (cont'd)

Table 180 — Temperature-to-Digital Conversion Performance

Parameter	Min	Typ	Max	Unit	Test Conditions[3]
Temperature Sensor Accuracy (B grade)[1]	--	±0.5	±1.0	°C	75 °C = T_A = 95 °C, Active Range
	--	±1.0	±2.0	°C	40 °C = T_A = 125 °C, Monitor Range
	--	±2.0	±3.0	°C	-20 °C = T_A = 125 °C
Temperature Sensor Accuracy (C grade)[1]	--	±1.0	±2.0	°C	75 °C = T_A = 95 °C, Active Range
	--	±2.0	±3.0	°C	40 °C = T_A = 125 °C, Monitor Range
	--	±3.0	±4.0	°C	-20 °C = T_A = 125 °C
Resolution		0.25		°C	
Conversion Time[2]			125	ms	Worst case conversion time

1 Refer to individual vendor datasheets for explanation of accuracy testing methodology.

2 Assuming 10-bit resolution. Conversion times may range from 62.5 ms for 9-bit to 500 ms for 12-bit accuracy.

3 $V_{CCSPD(MIN)} \leq V_{CCSPD} \leq V_{CCSPD(MAX)}$

14 Reset

14.1 Introduction

This chapter describes aspects of hardware reset specific to the DDR3 LRDIMM Memory Buffer (MB).

14.2 Platform Reset Functionality

The DDR3 memory channel provides a RESET_n signal to initialize all DDR3 LRDIMM memory buffers on the channel. The generation of this signal is platform dependent, and may be asynchronous to the clock. The platform will assert RESET_n at power-on.

It is possible that platform conditions cause RESET_n to be asserted at any time, including in the middle of DRAM commands. This could occur during a warm boot. Under these conditions, the DDR3 LRDIMM Memory Buffer will be reset and the contents of memory are not guaranteed. The state of the DRAMs must be guaranteed when re-initialized for proper response.

14.2.1 Platform RESET_n Requirements

RESET_n must be asserted at power-up, and may also be asserted at other times such as a warm boot.

During power-up, RESET_n timing shall follow Figure Timing of clock and data during power-on initialization sequence.

During reset with stable power, RESET_n timing shall follow Figure 15, Timing of clock and data during initialization sequence with stable power.

DDR3 Memory Buffer supports sticky bits in the registers to hold the results of DRAM interface training. These bits are only cleared on a hard reset. For soft resets, the MB is required to store the settings established during a previous DRAM interface training. This functionality enables the host to initiate multiple soft resets (if needed) during LRDIMM initialization but only performs the time consuming DRAM interface training once.

14.2.2 DDR3 LRDIMM Memory Buffer RESET_n Requirements

RESET_n is asynchronously applied to all storage elements.

Upon assertion of RESET_n:

- All input receivers are disabled, and can be left floating.
- DRAM CKE and RESET_n are driven LOW asynchronously.
- DQ/DQS are don’t care. All DRAM C/A inputs (except CKE) are floated.
- DRAM CK_t/CK_c are floated.
- All Configuration and Status Register (CSR) bits are set to their default values.
- All Control Word registers are restored to their default states.
- All internal state machines are put in their default state.

14.2.3 Power-Up and Suspend-to-RAM Considerations

In a suspend to RAM environment the DRAMs are put into self-refresh mode. The DRAM power supply remains active. This supply is used by the DDR3 LRDIMM memory buffer DRAM interface I/O circuits. The DDR3 LRDIMM MB QACKE[3:0] and QBCKE[3:0] pins must be kept LOW, without glitches through this transition.

During initial power-up, QACKE[3:0] and QBCKE[3:0] pins must be driven low. Once all power supplies are on and stable, all the other command/address pins are tri-stated to reduce current drawn from the Vtt power supply. QACKE[3:0] and QBCKE[3:0] pins maintained low during this time without glitches. The RESET_n signal must remain low during the power-up sequence, for a minimum of 200 μS after power is stable. Yn_t/Yn_c must be up and stable at the required frequency before QACKE[3:0] and QBCKE[3:0] goes from low to high.

14.3 Reset Types

Types of reset:

- Hard resets occur when the RESET_n signal is low and Vdd is being powered up or Vdd is stable.
- Soft resets are generated by setting control word F2 RC1, DA3 to ‘1’.
- SMBus resets affect only the SMBus interface.

15 Configuration and Status Registers

15.1 Access Mechanism

For all configuration & status and temperature sensor registers, the Memory Buffer supports register access mechanisms through SMBus as well as through in-band channel commands. The registers may be read by software from the SMBus host at any time the MB is powered on, except in the MB clock stopped power down mode or when the device RESET_n pin is asserted.

Table 83 shows the mapping between MB control words and SMBus register numbers. The entire register space of the MB is accessible with the SMBus Reg_Num[7:0] address field.

Table 181 — Function 0 SMBus Address Map

Register Address	Description	D7 D6 D5 D4 D3 D2 D1 D0	CW access
00h 01h	Vendor ID	VID[7:0] VID[15:8]	No No
02h 03h	Device ID	DID[7:0] DID[15:8]	No No
04h 05h	Revision ID Reserved	RID[7:0]	No No
06h 07h	Reserved Reserved	Reserved	No No
08h 09h	F0RC1, F0RC0 F0RC3, F0RC2	F0RC1 F0RC0 F0RC3 F0RC2	(F0), 882 (F0), 882
0Ah 0Bh	F0RC5, F0RC4 F0RC7, F0RC6	F0RC5 F0RC4 F0RC7 F0RC6	(F0), 882 (F0), 882
0Ch 0Dh	F0RC9, F0RC8 F0RC11, F0RC10	F0RC9 F0RC8 F0RC11 F0RC10	(F0), 882 (F0), 882
0Eh 0Fh	F0RC13, F0RC12 F0RC15, F0RC14	F0RC13 F0RC12 F0RC15 F0RC14	(F0), 882 (F0), 882
10-17h	F1RCnn+1, F1RCnn	F1RCnn+1 F1RCnn	F1, 882
18-1Fh	F2RCnn+1, F2RCnn	F2RCnn+1 F2RCnn	F2, 882
20-27h	F3RCnn+1, F3RCnn	F3RCnn+1 F3RCnn	F3, 882
28-2Fh	F4RCnn+1, F4RCnn	F4RCnn+1 F4RCnn	F4, 882
30-37h	F5RCnn+1, F5RCnn	F5RCnn+1 F5RCnn	F5, 882
38-3Fh	F6RCnn+1, F6RCnn	F6RCnn+1 F6RCnn	F6, 882
40-47h	F7RCnn+1, F7RCnn	F7RCnn+1 F7RCnn	F7, 882
48-4Fh	F8RCnn+1, F8RCnn	F8RCnn+1 F8RCnn	F8, 882
50-57h	F9RCnn+1, F9RCnn	F9RCnn+1 F9RCnn	F9, 882
58-5Fh	F10RCnn+1, F10RCnn	F10RCnn+1 F10RCnn	F10, 882
60-67h	F11RCnn+1, F11RCnn	F11RCnn+1 F11RCnn	F11, 882
68-6Fh	F12RCnn+1, F12RCnn	Reserved Reserved	F12, 882
70-77h	F13RCnn+1, F13RCnn	Reserved Reserved	F13, 882
78-7Fh	F14RCnn+1, F14RCnn	Vendor specific personality bytes	F14, 882
80-87h	F15RCnn+1, F15RCnn	Vendor specific personality bytes	F15, 882
88-9Fh	Reserved	Reserved	No
A0-ABh	TS	Temperature Sensor Registers	No
AC-FFh	Reserved	Reserved	No

15.1 Access Mechanism (cont'd)

"Reserved" means that this register space is reserved for future extensions (that are common to all implementations).

"Vendor specific" means that this register space is available now for vendor specific test and debug registers.

Each byte of the MB register space has its own unique address. For CSR writes the MB registers can be accessed in byte (8-bit), word (16-bit) or double word (32-bit) quantities. For CSR reads the MB registers can only be accessed in double word (32-bit) quantities. See the SMBus chapter for details on accessing MB registers through SMBus.

All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field). As an example Table 84 defines the byte order for double word accesses to the MB control words.

In this chapter CSRs are defined as 8-bit or 16-bit registers. Since a byte is the smallest access granularity for CSRs, a single 8-bit CSR contains two 4-bit control words.

Table 182 — Double word byte order for SMBus control word accesses

Register #	Description	Data[31:24]		Data[23:16]		Data[15:8]		Data[7:0]		CW access
8-11	FORC0-FORC7	FORC7	FORC6	FORC5	FORC4	FORC3	FORC2	FORC1	FORC0	(F0), 882
132-135	F15RC8-F15RC15	F15RC15	F15RC14	F15RC13	F15RC12	F15RC11	F15RC10	F15RC9	F15RC8	F15, 882

15.1.1 Register Attribute Definition

All registers have Base Attributes as defined in Table 85. Some register attributes are further modified with Attribute Modifiers, as defined in Table 86.

Table 183 — Register Base Attributes

Attribute	Abbreviation	Description
Read Only	RO	This bit can be read by software. Writes have no effect.
Read/Write	RW	This bit can be read or written by software.
Write Only	WO	This bit can only be written by software.
Reserved	RV	This bit is reserved for future expansion and its value must not be modified by software. The bit will return '0' when read. When writing this bit, software must preserve the value read unless otherwise indicated.

Table 184 — Register Attribute Modifier

Attribute	Abbreviation	Description
Write 1 Only	1O	This bit can only be set (i.e. write '1') but not reset (i.e. write '0') via SMBus
Sticky	S	The bit is "sticky" or unchanged by a device reset. This bit can only be defaulted by a power-up reset.

15.1.2 Number Notation

When references are made to numbers in register definitions, the following notation is used:

Binary: n'bxx

n = number of bits

b = indicates binary

xx = binary value

Hexadecimal: n'hxx

n = number of bits

h = indicates hexadecimal

xx = hexadecimal value

15.1.3 Function Spaces

The following functions are described in this chapter:

5. Function 0

Revision ID, Device ID and Vendor ID registers

JEDEC specified control words

Temperature Sensor registers

MRS snooping registers

6. Function(s) TBD

JEDEC DFX registers for MemBIST

JEDEC DFX registers for Transparent Mode

15.2 Registers

15.2.1 Register Map

Table 185 — Control Word and Temperature Sensor Register Map

Addr (hex)	Register Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
00h 01h	VID	Vendor ID							
02h 03h	DID	Device ID							
04h	RID	Revision ID							
05-07h	Reserved	Reserved							
08h	F0RC1_0	Y3ClockDis	Y2ClockDis	Y1ClockDis	Y0ClockDis	QVrefDQ	QVrefCA	WeakDrive	InvertDis
09h	F0RC3_2	QCSDrive		QCADrive		FreqBand	Reserved	R1/R5_swap	Prelaunch
0Ah	F0RC5_4	Y0Y2Drive		Y1Y3Drive		QCKEDrive		QODTDrive	
0Bh	F0RC7_6	FunctionSelect				Reserved	DODTCtrl	CKEMgmtMode	
0Ch	F0RC9_8	CKEPDEn	CKEPD-Mode	YDis	Reserved	DCAVref	IBTDCA		
0Dh	F0RC11_10	Parity Calculation		OpVolt		Reserved	OpFreq		
0Eh	F0RC13_12	NumLogRanks		NumPhyRanks		FreqContext	TrainingControl		
0Fh	F0RC15_14	RankMultCtrl				DRAMwidth	MRSCtrl	RefCtrl	MirrorCtrl
10h	F1RC1_0	Reserved	IBTDCKE			IBTDCS32	IBTDCS		
11h	F1RC3_2	Reserved				Reserved	IBTDODT		
12h	Reserved	Reserved				Reserved			
13h	F1RC7_6	FunctionSelect				Reserved			
14h	F1RC9_8	Refresh Stagger				QCS_ExtDelay (Optional)		QCA_ExtDelay (Optional)	
15h	F1RC11_10	QCKE_ExtDelay (Optional)		QODT_ExtDelay (Optional)		Refresh Stagger Limit			
16h	F1RC13_12	QCSDEn	QCSDelay			Reserved	YDelay		
17h	F1RC15_14	QCKEDEn	QCKEDelay			QODTDEn	QODTDelay		
18h	F2RC1_0	Reserved	Mask_QRST	Clear_Sticky	Soft_Reset	TM_CS_Mult		Reserved	TModeEn
19h	F2RC3_2	ERROut_En	Valid	Failure	TrainCtrl	AccCtlTS	AccCtlVendor	AccCtlJEDEC	AccCtlFN0
1Ah	F2RC5_4	NumRows		NumColumns		MEMBIST_RankCtrl			
1Bh	F2RC7_6	FunctionSelect				MEMBIST_RefCtrl			
1Ch	F2RC9_8	ECC_Pattern2				ECC_Pattern1			
1Dh	F2RC11_10	ECC_Pattern4				ECC_Pattern3			
1Eh	F2RC13_12[	ECC_Pattern6				ECC_Pattern5			
1Fh	F2RC15_14	ECC_Pattern8				ECC_Pattern7			
20h	F3RC1_0	DQVref	RTT_Wr			TDQS	RTT_Nom		
21h	F3RC3_2	Reserved				DQDrvDis	DQDrv		
22h	Reserved	Reserved							
23h	F3RC7_6	FunctionSelect				Connector IF DRAMwidth	Reserved	DQTiming	
24h	F3RC9_8	MDQDrvDis	MDQDrv			Reserved	MBQODT		
25h	F3RC11_10	Reserved		Rank0 Wr QxODT1	Rank0 Wr QxODT0	Reserved		Rank0 Rd QxODT1	Rank0 Rd QxODT0
26h	F3RC13_12	MDQWriteDelay - Byte 0 (Optional)				MDQReadDelay - Byte 0 (Optional)			
27h	Reserved	Reserved							

28–2Ch	Reserved	Reserved; F4RC7 is FuncionSelect					
2Dh	F4RC11_10	Reserved	Rank1 Wr QxODT1	Rank1 Wr QxODT0	Reserved	Rank1 Rd QxODT1	Rank1 Rd QxODT0
2Eh	F4RC13_12	MDQWriteDelay - Byte 1 (Optional)			MDQReadDelay - Byte 1 (Optional)		
2Fh	Reserved	Reserved					
30–34h	Reserved	Reserved; F5RC7 is FuncionSelect					
35h	F5RC11_10	Reserved	Rank2 Wr QxODT1	Rank2 Wr QxODT0	Reserved	Rank2 Rd QxODT1	Rank2 Rd QxODT0
36h	F5RC13_12	MDQWriteDelay - Byte 2 (Optional)			MDQReadDelay - Byte 2 (Optional)		
37h	Reserved	Reserved					
38–3Ch	Reserved	Reserved; F6RC7 is FuncionSelect					
3Dh	F6RC11_10	Reserved	Rank3 Wr QxODT1	Rank3 Wr QxODT0	Reserved	Rank3 Rd QxODT1	Rank3 Rd QxODT0
3E	F6RC13_12	MDQWriteDelay - Byte 3 (Optional)			MDQReadDelay - Byte 3(Optional)		
3Fh	Reserved	Reserved					
40–44h	Reserved	Reserved; F7RC7 is FuncionSelect					
45h	F7RC11_10	Reserved	Rank4 Wr QxODT1	Rank4 Wr QxODT0	Reserved	Rank4 Rd QxODT1	Rank4 Rd QxODT0
46h	F7RC13_12	MDQWriteDelay - Byte 4 (Optional)			MDQReadDelay - Byte 4 (Optional)		
47h	Reserved	Reserved					
48–4Ch	Reserved	Reserved; F8RC7 is FuncionSelect					
4Dh	F8RC11_10	Reserved	Rank5 Wr QxODT1	Rank5 Wr QxODT0	Reserved	Rank5 Rd QxODT1	Rank5 Rd QxODT0
4Eh	F8RC13_12	MDQWriteDelay - Byte 5 (Optional)			MDQReadDelay - Byte 5 (Optional)		
4Fh	Reserved	Reserved					
50–54h	Reserved	Reserved; F9RC7 is FuncionSelect					
55h	F9RC11_10	Reserved	Rank6 Wr QxODT1	Rank6 Wr QxODT0	Reserved	Rank6 Rd QxODT1	Rank6 Rd QxODT0
56h	F9RC13_12	MDQWriteDelay - Byte 6 (Optional)			MDQReadDelay - Byte 6 (Optional)		
57h	Reserved	Reserved					
58–5Ch	Reserved	Reserved; F10RC7 is FuncionSelect					
5Dh	F10RC11_10	Reserved	Rank7 Wr QxODT1	Rank7 Wr QxODT0	Reserved	Rank7 Rd QxODT1	Rank7 Rd QxODT0
5E	F10RC13_12	MDQWriteDelay - Byte 7 (Optional)			MDQReadDelay - Byte 7 (Optional)		
5F	Reserved	Reserved					
60–65h	Reserved	Reserved; F11RC7 is FuncionSelect					
66h	F11RC13_12	MDQWriteDelay - Byte 8			MDQReadDelay - Byte 8 (Optional)		
67h	Reserved	Reserved					
68 – 73h	Reserved	Reserved; F12RC7 and F13RC7 are FunctionSelect					
74h	F13RC9_8	SMBus Function			Reserved		
75h	F13RC11_10	MSB of Address Port			LSB of Address Port		
76h	F13RC13_12	Reserved			Extended Address Port		
77h	F13RC15_14	MSB of Data Port			LSB of Data POrt		

78h	F14RC1_0	Personality Byte 0	
79h	F14RC3_2	Personality Byte 1	
7Ah	F14RC5_4	Personality Byte 2	
7Bh	F14RC7_6	FunctionSelect	Personality Byte 3 bits 3:0
7Ch	F14RC9_8	Personality Byte 4	
7Dh	F14RC11_10	Personality Byte 5	
7Eh	F14RC13_12	Personality Byte 6	
7Fh	F14RC15_14	Personality Byte 7	
80h	F15RC1_0	Personality Byte 8	
81h	F15RC3_2	Personality Byte 9	
82h	F15RC5_4	Personality Byte 10	
83h	F15RC7_6	FunctionSelect	Personality Byte 3 bits 7:4
84h	F15RC9_8	Personality Byte 11	
85h	F15RC11_10	Personality Byte 12	
86h	F15RC13_12	Personality Byte 13	
87h	F15RC15_14	Personality Byte 14	
88 – 9Fh	Reserved	Reserved	
A0–A1h	TS-CAP	Temperature Sensor Capabilities Register	
A2–A3h	TS-CONF	Temperature Sensor Configuration Register	
A4–A5h	TS-HILIM	Temperature Sensor High Limit Register	
A6–A7h	TS-LOLIM	Temperature Sensor Low Limit Register	
A8–A9h	TS-TCRIT	Temperature Sensor Critical Temperature Register	
AA-ABh	TS-AMB	Temperature Current Ambient Temperature Register	
ACh	MRS_CTRL	MRS Control	
AD–B7h	Reserved	Reserved	
B8h	R0_MR12_OVER	Rank 0 MR1,2 Register	
B9h	R1_MR12_OVER	Rank 1 MR1,2 Register	
BAh	R2_MR12_OVER	Rank 2 MR1,2 Register	
BBh	R3_MR12_OVER	Rank 3 MR1,2 Register	
BCh	R4_MR12_OVER	Rank 4 MR1,2 Register	
BDh	R5_MR12_OVER	Rank 5 MR1,2 Register	
BEh	R6_MR12_OVER	Rank 6 MR1,2 Register	
BFh	R7_MR12_OVER	Rank 7 MR1,2 Register	
C0–C7h	Reserved	Reserved	
C8–C9h	MR0_SNOOP	MR0 Snoop Register	

CA–CBh	MR1_SNOOP	MR1 Snoop Register
CC–CDh	MR2_SNOOP	MR2 Snoop Register
CE–CFh	MR3_SNOOP	MR3 Snoop Register
D0-FFh	Reserved	Reserved

15.2.2 Register Description

Table 186 — Vendor ID Register

00h	Vendor ID		
Bits	**Attr**	**Default**	**Description**
15:0	RO	Vendor specific	Vendor ID

Table 187 — Device ID Register

02h	Device ID		
Bits	**Attr**	**Default**	**Description**
15:0	RO	0030h	Device ID

Table 188 — Revision ID Register

04h	Revision ID		
Bits	**Attr**	**Default**	**Description**
7:0	RO	0	Revision ID

15.2.2 Register Description (cont'd)

Table 189 — F0RC1_0 Register

08h	F0RC1 – F0RC0		
Bits	**Attr**	**Default**	**Description**
7	RW	0	**F0RC1[3]:**[1] Y3_t/Y3_c Clock Disable 0: Output enabled 1: Output disabled
6	RW	0	**F0RC1[2]:**[1] Y2_t/Y2_c Clock Disable 0: Output enabled 1: Output disabled
5	RW	0	**F0RC1[1]:**[1] Y1_t/Y1_c Clock Disable 0: Output enabled 1: Output disabled
4	RW	0	**F0RC1[0]:**[1] Y0_t/Y0_c Clock Disable 0: Output enabled 1: Output disabled
3	RW	0	**F0RC0[3]:** QVrefDQ Output 0: Output enabled 1: Output disabled and floating
2	RW	0	**F0RC0[2]**: QVrefCA Output 0: Output enabled 1: Output disabled and floating
1	RW	0	**F0RC0[1]:** Output Weak Drive[2,3] 0: Disabled 1: Enabled
0	RW	0	**F0RC0[0]:** Output Inversion 0: Enabled 1: Disabled

NOTE 1 Output clocks may be individually turned on or off to conserve power. The system must read the module SPD to determine which clock outputs are used by the module. The PLL remains locked on CK_t/CK_c unless the system stops the clock inputs to the MB to enter the lowest power mode.

NOTE 2 Output Weak Drive is applicable only when all DCS[x:0]_n are HIGH

NOTE 3 Output weak drive refers to allowing A/B outputs to enter a state of higher output impedance when they are not being used. This is to conserve power when the outputs are resistively terminated to a voltage (e.g., VDD, VTT, or VSS). When output Weak Drive is enabled, the following outputs (on both matching A and B outputs) are affected: QxA0, QxA1, QxA2, QxA3, QxA4, QxA5, QxA6, QxA7, QxA8, QxA9, QxA10/ AP, QxA11, QxA12/BC, QxA13, QxA14, QxA15, QxBA0, QxBA1, QxBA2, QxRAS_n, QxCAS_n, and QxWE_n.

15.2.2 Register Description (cont'd)

Table 190 — F0RC3_2 Register

09h	F0RC3 – F0RC2		
Bits	**Attr**	**Default**	**Description**
7:6	RW	0	**F0RC3[3:2]:** QxCS[3:0]_n Outputs 00: Light Drive (8 to 10 DRAM Loads) 01: Moderate Drive (16 to 20 DRAM Loads) 10: Strong Drive (32 to 40 DRAM Loads) 11: Reserved
5:4	RW	0	**F0RC3[1:0]:** Address/Command - QxAn, QxBAn, QxRAS_n, QxCAS_n, QxWE_n Outputs 00: Light Drive (8 to 10 DRAM Loads) 01: Moderate Drive (16 to 20 DRAM Loads) 10: Strong Drive (32 to 40 DRAM Loads) 11: Very Strong Drive (64 to 80 DRAM Loads)
3	RW	0	**F0RC2[3]:** Frequency Band Select 0: Operation (Frequency Band 1) 1: Test Mode (Frequency Band 2)
2	RV	0	**F0RC2[2]:** Reserved
1	RW	0	**F0RC2[1]:** Rank 1 and Rank 5 Swap[1] 0: Disabled; Rank 1 = QACS[1]_n; Rank 5 = QBCS[1]_n 1: Enabled; Rank 1 = QBCS[1]_n; Rank 5 = QACS[1]_n
0	RW	0	**F0RC2[0]:** Command/Address Prelaunch[1] 0: Standard timing (no prelaunch) 1: Prelaunch Address and command nets pre-launch controlled by F1RC8 and F1RC12 Control signals QxCKE, QxCS_n and QxODT controlled by F1RC8, F1RC11 and F1RC[15:13]

NOTE 1 Host BIOS is responsible for configuring this bit based on DIMM type. DIMM SPD indicates whether DIMM has swapped Rank 1 and Rank 5. Typically, this bit is used for 8Rx8 DIMM configuration.

15.2.2 Register Description (cont'd)

Table 191 — F0RC5_4 Register

0Ah	F0RC5 – F0RC4		
Bits	Attr	Default	Description
7:6	RW	0	**F0RC5[3:2]:** Clock Y0_t, Y0_c, Y2_t, and Y2_c Output Drivers (B side) 00: Light Drive (8 to 10 DRAM Loads) 01: Moderate Drive (16 to 20 DRAM Loads) 10: Strong Drive (32 to 40 DRAM Loads) 11: Reserved
5:4	RW	0	**F0RC5[1:0]:** Clock Y1_t, Y1_c, Y3_t, and Y3_c Output Drivers (A side) 00: Light Drive (8 to 10 DRAM Loads) 01: Moderate Drive (16 to 20 DRAM Loads) 10: Strong Drive (32 to 40 DRAM Loads) 11: Reserved
3:2	RW	0	**F0RC4[3:2]:** QxCKE[3:0] Outputs 00: Light Drive (8 to 10 DRAM Loads) 01: Moderate Drive (16 to 20 DRAM Loads) 10: Strong Drive (32 to 40 DRAM Loads) 11: Reserved
1:0	RW	0	**F0RC4[1:0]:** QxODT[1:0] Outputs 00: Light Drive (8 to 10 DRAM Loads) 01: Moderate Drive (16 to 20 DRAM Loads) 10: Strong Drive (32 to 40 DRAM Loads) 11: Reserved

15.2.2 Register Description (cont'd)

Table 192 — F0RC7_6 Register

0Bh	F0RC7 – F0RC6		
Bits	Attr	Default	Description
7:4	RW	0	**F0RC7[3:0]:** Function Select 0000: F0; RC0-6, 8-15=F0RC06, 8-15 0001: F1; RC0-6, 8-15=F1RC06, 8-15 0010: F2; RC0-6, 8-15=F2RC06, 8-15 0011: F3; RC0-6, 8-15=F3RC06, 8-15 0100: F4; RC0-6, 8-15=F4RC06, 8-15 0101: F5; RC0-6, 8-15=F5RC06, 8-15 0110: F6; RC0-6, 8-15=F6RC06, 8-15 0111: F7; RC0-6, 8-15=F7RC06, 8-15 1000: F8; RC0-6, 8-15=F8RC06, 8-15 1001: F9; RC0-6, 8-15=F9RC06, 8-15 1010: F10; RC0-6, 8-15=F10RC06, 8-15 1011: F11; RC0-6, 8-15=F11RC06, 8-15 1100: F12 (Reserved) 1101: F13 (Reserved) 1110: F14 (Vendor Specific) 1111: F15 (Vendor Specific)
3	RV	0	**F0RC6[3]:** Reserved
2	RW	0	**F0RC6[2]:** DODT Control 0: Buffer only evaluates DODT[0] 1: Buffer evaluates DODT[0] & Dodt[1]/DCKE[3][2]
1:0	RW	0	**F0RC6[1:0]:** CKE Management Mode 00: (default) CKE outputs are directly controlled by 2 CKE inputs DCKE[0] controls QxCKE[2,0][1] DCKE[1] controls QxCKE[3,1][1] 01: CKE outputs are directly controlled by 4 CKE inputs[1] DCKE[0] controls QxCKE[0] DCKE[1] controls QxCKE[1] DCKE[2] controls QxCKE[2] DODT[1]/DCKE[3][2] controls QxCKE[3] 10: 4 QxCKE outputs controlled independently of 2 DCKE inputs. Buffer only asserts or de-asserts QxCKE[x] Ranks that is specified by the host 11: Reserved

NOTE 1 In 2 rank case, buffer tri-states QxCKE[2] and QxCKE[3] outputs

NOTE 2 In 4 DCKE mode (bits 9:8='01'), DODT[1]/DCKE[3] pin will be used for DCKE[3]. In other cases the pin will be used as DODT[1] if bit 10=1 otherwise DODT[1] pin is not used and may be tri-stated and buffer turns off IBT for DODT[1]. Additionally in 4 DCKE mode (bits 9:8='01') bit 10 must be '0'.

15.2.2 Register Description (cont'd)

Table 193 — F0RC9_8 Register

0Ch	F0RC9 – F0RC8		
Bits	**Attr**	**Default**	**Description**
7	RW	0	**F0RC9[3]:** CKE Power Down Mode Enable[1] 0: Disabled 1: Enabled
6	RW	0	**F0RC9[2]:** CKE Power Down Mode (If CKE Power Down Enabled) 0: CKE Power Down with IBT On, DQS RTT enabled 1: CKE Power Down with IBT Off, DQS RTT disabled
5	RW	0	**F0RC9[1]:** Output Clock Disable in CKE Power Down Mode 0: Y clocks stay active in CKE power down 1: Y clocks disabled in CKE power down
4	RV	0	**F0RC9[0]:** Reserved
3	RW	0	**F0RC8[3]:** Vref for DAn, DBAn, DRAS_n, DCAS_n, DWE_n and PAR_IN, DCSx_n, DCKEn, DODTx 0: Use VrefCA input pin for receiver reference voltage 1: Use internally generated Vref for receiver reference voltage
2:0	RW	0	**F0RC8[2:0]:** Input Bus termination for DAn, DBAn, DRAS_n, DCAS_n, DWE_n and PAR_IN 000: 100 Ohm 001: 150 Ohm 010: 200 Ohm 011: 300 Ohm 100: Reserved 101: Reserved 110: Reserved 111: Off[2]

NOTE 1 The MB supports different power down modes. By default, the Power Down feature is disabled (bit 7=0). The register ignores CKE Power Down mode setting when this function is disabled. If the CKE Power Down mode is enabled (bit 7=1), then power down is invoked once both DCKE0 and DCKE1 are low. Bit DBA0 selects how IBT and DQS RTT behave and bit DA4 selects how Y clocks behave during CKE Power Down

NOTE 2 With this setting IBT on all inputs except DCSx_n, DCKEx and DODTx is turned off

15.2.2Register Description (cont'd)

Table 194 — F0RC11_10 Register

0Dh	F0RC11 – F0RC10		
Bits	**Attr**	**Default**	**Description**
7:6	RW	0	**F0RC11[3:2]:** Parity Calculation 00: OFF[1] 01: A[15:0], BA[2:0], RAS_n, CAS_n, WE_n 10: A[17:0], BA[2:0], RAS_n, CAS_n, WE_n 11: Reserved
5:4	RW	0	**F0RC11[1:0]:** MB VDD Operating Voltage 00: 1.5V DDR3 mode (default) 01: 1.35V DDR3L mode[2] 10: Reserved 11: Reserved
3:0	RW	0	**F0RC10[3:0]:** DIMM Operating Speed 0000: f ≤ 800 MT/s 0001: 800 MT/s < f ≤ 1066 MT/s 0010: 1066 MT/s < f ≤ 1333 MT/s 0011: 1333 MT/s < f ≤ 1600 MT/s 0100: 1600 MT/s < f ≤ 1866 MT/s 0101: 1866 MT/s < f ≤ 2133 MT/s 0110: Reserved 0111: Reserved 1XXX: Reserved

NOTE 1 Buffer does not check for parity including control word programming commands.

NOTE 2 DDR3L 1.35V MB is backward compatible and operable to DDR3 1.5V specification. To guarantee all timings and specification for DDR3 1.5V, the MB must be configured with bits[5:4]='00'

15.2.2 Register Description (cont'd)

Table 195 — F0RC13_12 Register

0Eh	F0RC13 – F0RC12		
Bits	**Attr**	**Default**	**Description**
7:6	RW	0	**F0RC13[3:2]:** Number of Logical Ranks 00: Buffer evaluates DCS[0]_n 01: Buffer evaluate DCS[1:0]_n 10: Buffer evaluates DCS[3:0]_n 11: Buffer evaluates DCS[7:0]_n
5:4	RW	0	**F0RC13[1:0]:** Number of Physical Ranks 00: 8 ranks connected to QCS[7:0]_n 01: 4 ranks connected to QxCS[3:0]_n 10: 2 ranks connected to QxCS[1:0]_n 11: 1 rank connected to QxCS[0]_n
3	RW	0	**F0RC12[3]:** Context for operating training 0: Context 1 operation and storage of DRAM interface calibration values to CSRs 1: Context 2 operation and storage of DRAM interface calibration values to CSRs
2:0	RW	0	**F0RC12[2:0]:** Training Control 000: Normal operating mode[1] 001: Connector DQ interface write leveling 010: Start DRAM interface training[2] 011: Reserved 1XX: Reserved

NOTE 1 Buffer stops driving Errout_n Low when training had error. Buffer stops training if it was previously started and will stop driving Errout_n Low. Buffer resets Fail and Valid bits in F2RC3_2 register.

NOTE 2 Buffer starts driving Errout_n Low 20 clocks after receiving this command.'

15.2.2 Register Description (cont'd)

Table 196 — F0RC15_14 Register

0Fh	F0RC15 – F0RC14		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F0RC15[3:0]:** Rank Select bits 0000: Normal operating mode 0001: RA[14]; 2x multiplication, 1 Gbit DDR3 SDRAM 0010: RA[15]; 2x multiplication, 2 Gbit DDR3 SDRAM 0011: RA[16]; 2x multiplication, 4 Gbit DDR3 SDRAM 0100: Reserved 0101: RA[15:14]; 4x multiplication, 1 Gbit DDR3 SDRAM 0110: RA[16:15]; 4x multiplication, 2 Gbit DDR3 SDRAM 0111: RA[17:16]; 4x multiplication, 4 Gbit DDR3 SDRAM 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved
3	RW	0	**F0RC14[3]:** DRAM Bus Width 0: X4 1: X8
2	RW	0	**F0RC14[2]:**[3] DRAM MRS Control 0: (default) MRS command is broadcast to all physical ranks associated with a logical rank as specified in F0RC13 1: MRS command is issued to a specific physical rank as specified by the host using the Rank multiplication addressing method specified in F0RC15[2]
1	RW	0	**F0RC14[1]:**[3] DRAM Refresh, Precharge single and Precharge All Command Control 0: (default) Refresh, Precharge single and Precharge All command is broadcast to all physical ranks associated with a logical rank as specified in F0RC13 1: Refresh, Precharge single and Precharge[1] All command is issued to a specific physical rank as specified by the host using the Rank multiplication addressing method specified in F0RC15[2]
0	RW	0	**F0RC14[0]:**[4] Address Mirroring Control 0: Disabled 1: Enabled. Buffer mirrors Address for ODD Physical Ranks. Buffer interprets information in host MRS commands to odd ranks as being mirrored.

NOTE 1 Buffer evaluates address bit A13 for MRS command. If A13=0, buffer passes MRS command to a Rank specified by host as defined in F0RC15. If A13=1, buffer broadcasts MRS command to all physical ranks associated with a logical rank.
NOTE 2 Buffer evaluates address bit A0 for Precharge Single and Precharge All command. If A0=0, buffer steers Precharge Single and Precharge All command to a Rank specified by host as defined in F0RC15. If A0=1, buffer broadcasts Precharge Single and Precharge All command to all physical ranks associated with a logical rank.
NOTE 3 Only applicable in Rank Multiplication mode as selected in F0RC15. In normal mode of operation these bits do not apply and must be configured as "0".
NOTE 4 This is only applicable when buffer executes MRS command on its own under training for its DRAM interface. Host memory controller is still responsible for Address Mirroring when it issues MRS command under DRAM initialization phase as well as normal mode of operation.

15.2.2 Register Description (cont'd)

Table 197 — F1RC1_0 Register

10h	F1RC1 – F1RC0		
Bits	**Attr**	**Default**	**Description**
7	RV	0	**F1RC1[3]:** Reserved
6:4	RW	0	**F1RC1[2:0]:** Input Bus Termination DCKE[1:0] an DCKE[3:2][1] 000: 100 Ohm 001: 150 Ohm 010: 200 Ohm 011: 300 Ohm 100: Reserved 101: Reserved 110: Reserved 111: Off[2]
3	RW	0	**F1RC0[3]:** Input Bus Termination DCS[3:2]_n 0: IBT as defined in F1RC0 1: IBT as defined in F0RC8
2:0	RW	0	**F1RC0[2:0]:** Input Bus Termination DCS[1:0] and DCS[3:2]_n[3] 000: 100 Ohm 001: 150 Ohm 010: 200 Ohm 011: 300 Ohm 100: Reserved 101: Reserved 110: Reserved 111: Off[4]

NOTE 1 If F0RC6[1:0]='01'

NOTE 2 With this setting, IBT on all DCKE inputs is turned off.

NOTE 3 If F1RC0[3]='0'

NOTE 4 With this setting, IBT on all DCS_n inputs is turned off.

15.2.2 Register Description (cont'd)

Table 198 — F1RC3_2 Register

11h	F1RC3 – F1RC2		
Bits	**Attr**	**Default**	**Description**
7:4	RV	0	**F1RC3[3:2]:** Reserved
3	RV	0	**F1RC2[3]:** Reserved
2:0	RW	0	**F1RC2[2:0]:** Input Bus Termination DODT[1:0][1] 000: 100 Ohm 001: 150 Ohm 010: 200 Ohm 011: 300 Ohm 100: Reserved 101: Reserved 110: Reserved 111: Off[2]

NOTE 1 Applies to DODT[1] only if F0RC6[2]='1'; otherwise IBT on DODT[1] is off.

NOTE 2 With this setting, IBT on all DODT inputs is turned off.

Table 199 — F1RC7_6 Register

13h	F1RC7– F1RC6		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F1RC7[3:0]:** Function Select (see F0RC7[3:0] for definition)
3:0	RV	0	**F1RC6[3:0]:** Reserved

15.2.2 Register Description (cont'd)

Table 200 — F1RC9_8 Register

14h	F1RC9— F1RC8		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F1RC9[3:0]:** Refresh Stagger 0000: Ref_Stagger = 0 clocks 0001: Ref_Stagger = 20 clocks 0010: Ref_Stagger = 30 clocks 0011: Ref_Stagger = 40 clocks 0100: Ref_Stagger = 60 clocks 0101: Ref_Stagger = 80 clocks 0110: Ref_Stagger = 100 clocks 0111: Ref_Stagger = 120 clocks 1XXX: Reserved
3:2	RW	0	**F1RC8[3:2]: (Optional)** Total QCS delay = QCS Delay (F1FC13) + QCSDextended 00: QCSDextended = 0. No addition to QCS Delay 01: QCSDextended = (1/128)*tCK 10: QCSDextended = (2/128)*tCK 11: QCSDextended = (3/128)*tCK
1:0	RW	0	**F1RC8[1:0]: (Optional)** Total Y delay = Y Delay (F1FC12) + YDextended 00: YDextended = 0. No addition to Y Delay 01: YDextended = (1/128)*tCK 10: YDextended = (2/128)*tCK 11: YDextended = (3/128)*tCK

15.2.2 Register Description (cont'd)

Table 201 — F1RC11_10 Register

15h	F1RC11— F1RC10		
Bits	**Attr**	**Default**	**Description**
7:6	RW	0	**F1RC11[3:2]: (Optional)** Total QCKE delay = QCKE Delay (F1FC15) + QCKEDextended 00: QCKEDextended = 0. No addition to QCKE Delay 01: QCKEDextended = (1/128)*tCK 10: QCKEDextended = (2/128)*tCK 11: QCKEDextended = (3/128)*tCK
5:4	RW	0	**F1RC11[1:0]: (Optional)** Total QODT delay = QODT Delay (F1FC14) + QODTDextended 00: QODTDextended = 0. No addition to QODT Delay 01: QODTDextended = (1/128)*tCK 10: QODTDextended = (2/128)*tCK 11: QODTDextended = (3/128)*tCK
3	RW	0	**F1RC10[3]:** 0: Always start with the lowest numbered rank 1: Start rank is the rank after the last refresh (start rank only changes if a refresh was missed)
2:0	RW	0	**F1RC10[2:0]:** Refresh Stagger Limit[1] 000: Ref_Stagger = unlimited 001: Ref_Stagger = 10 clocks 010: Ref_Stagger = 20 clocks 011: Ref_Stagger = 30 clocks 100: Ref_Stagger = 40 clocks 101: Ref_Stagger = 60 clocks 110: Ref_Stagger = 80 clocks 111: Reserved

NOTE 1 This control word is only applicable when F0RC14[0]='0'

15.2.2 Register Description (cont'd)

Table 202 — F1RC13_12 Register

16h	F1RC13 – F1RC12		
Bits	**Attr**	**Default**	**Description**
7	RW	0	**F1RC13[3]:** Controls QCS_n Delay 0: Disable QCS_n delay. Delay QCS_n by 0 tCK to Yn (m=0) 1: Enable QCS_n delay according to F1RC13
6:4	RW	0	**F1RC13[2:0]:** Delay QCS_n 000: Delay QCS by (8/32)*tCK to Yx (m=8) 001: Delay QCS by (7/32)*tCK to Yx (m=7) 010: Delay QCS by (6/32)* tCK to Yx (m=6) 011: Delay QCS by (5/32)*tCK to Yx (m=5) 100: Delay QCS by (4/32)*tCK to Yx (m=4) 101: Delay QCS by (3/32)*tCK to Yx (m=3) 110: Delay QCS by (2/32)*tCK to Yx (m=2) 111: Delay QCS by (1/32)*tCK to Yx (m=1)
3	RV	0	**F1RC12[3]:** Reserved
2:0	RW	0	**F1RC12[3]:** Delay Y 000: Delay Y by (8/32)*CK (QCA prelaunch = 0.75 tCK, n=8)[1] 001: Delay Y by (7/32)*tCK (QCA prelaunch = 0.71875 tCK, n=7) [1] 010: Delay Y by (6/32)*tCK (QCA prelaunch = 0.6875 tCK, n=6) [1] 011: Delay Y by (5/32)*tCK (QCA prelaunch = 0.65625 tCK, n=5) [1] 100: Delay Y by (4/32)*tCK (QCA prelaunch = 0.625 tCK, n=4)[1] 101: Delay Y by (3/32)*tCK (QCA prelaunch = 0.59375 tCK, n=3) [1] 110: Delay Y by (2/32)*tCK (QCA prelaunch = 0.5625 tCK, n=2) [1] 111: Delay Y by (1/32)*tCK (QCA prelaunch = 0.53125 tCK, n=0)[1]

NOTE 1 If F0RC2[0] = 1

15.2.2 Register Description (cont'd)

Table 203 — F1RC15_14 Register

17h	F1RC15 – F1RC14		
Bits	**Attr**	**Default**	**Description**
7	RW	0	**F1RC15[3]:** Controls QCKE Delay 0: Disable QCKE delay QCKE by 0 tCK to Yx (m=0) 1: Enable QCKE delay according to F1RC15
6:4	RW	0	**F1RC15[2:0]:** Delay QCKE 000: Delay QCKE by (8/32)*tCK to Yx (m=8) 001: Delay QCKE by (7/32)*tCK to Yx (m=7) 010: Delay QCKE by (6/32)*tCK to Yx (m=6) 011: Delay QCKE by (5/32)*tCK to Yx (m=5) 100: Delay QCKE by (4/32)*tCK to Yx (m=4) 101: Delay QCKE by (3/32)*tCK to Yx (m=3) 110: Delay QCKE by (2/32)*tCK to Yx (m=2) 111: Delay QCKE by (1/32)*tCK to Yx (m=1)
3	RW	0	**F1RC14[3]:** Controls QODT Delay 0: Disable QODT delay QODT by 0 tCK to Yx (m=0) 1: Enable QODT delay according to F1RC14
2:0	RW	0	**F1RC14[2:0]:** Delay QODT 000: Delay QODT by (8/32)*tCK to Yx (m=8) 001: Delay QODT by (7/32)*tCK to Yx (m=7) 010: Delay QODT by (6/32)*tCK to Yx (m=6) 011: Delay QODT by (5/32)*tCK to Yx (m=5) 100: Delay QODT by (4/32)*tCK to Yx (m=4) 101: Delay QODT by (3/32)*tCK to Yx (m=3) 110: Delay QODT by (2/32)*tCK to Yx (m=2) 111: Delay QODT by (1/32)*tCK to Yx (m=1)

15.2.2 Register Description (cont'd)

Table 204 — F2RC1_0 Register

18h	F2RC1 – F2RC0		
Bits	**Attr**	**Default**	**Description**
7	RV	0	**F2RC1[3]:** Reserved
6	RWS	0	**F2RC1[2]:** Mask DDR Reset 0: Soft Reset will cause assertion of the QRST_n output 1: Soft Reset will not assert the QRST_n output
5	RW	0	**F2RC1[1]:** Clear Sticky Register Bits 0: Don't clear sticky register bits during Soft Reset 1: Clear sticky register bits during Soft Reset
4	WO	0	**F2RC1[0]:** Soft Reset[a] 0: Writing a '0' has no effect 1: Writing a '1' initiates a Soft Reset
3:2	RW	0	**F2RC0[3:2]:** Chip select multiplication in transparent mode 00: QACS[3:0]_n=DCS[3:0]_n, QBCS[3:0]_n=DCS[3:0]_n 01: QACS[3:0]_n=DCS[3:0]_n, QBCS[3:0]_n=DCS[7:4]_n 10: QACS[2,0]_n=DCS[1,0]_n, QBCS[2,0]_n=DCS[3:2]_n QACS[3,1]_n=2'b11, QBS[3,1]_n=2'b11 11: QACS[2,0]_n=2'b11, QBS[2,0]_n=2'b11 QACS[3,1]_n=DCS[1,0]_n, QBCS[3,1]_n=DCS[3:2]_n
1	RV	0	**F1RC0[1]:** Reserved
0	RW	0	**F1RC0[0]:** Enable transparent mode 0: Normal operation 1: Transparent mode enabled

a. Valid clock with stable frequency needs to be supplied to MB until at least MB tMRD + DRAM tMOD + 100ns after writing a '1' to bit 4.

Table 205 — F2RC3_2 Register

19h	F2RC3 – F2RC2		
Bits	**Attr**	**Default**	**Description**
7	RW	0	**F2RC3[3]:** Errout_n Enable for Training & MEMBIST 0: Disable - Errout_n is not driven Low when Training/MEMBIST is started 1: Enable - Errout_n is driven Low when Training/MEMBIST is started
6	ROS	0	**F2RC3[2]:** Valid Bit 0: Training still running or results are not valid 1: Training completed and results are valid
5	ROS	0	**F2RC3[1]:** Failure Bit 0: Pass 1: Failure
4	RW	0	**F2RC3[0]:** Training Control 0: Training not running; writing '0' will stop training and clear Failure and Valid bits[1] 1: Training running; writing '1' will stop training but not clear Failure and Valid bits[2]
3	RW1O	0	**F2RC2[3]:** SMBus Access control to Temperature Sensor This bit can only be written by control word write 0: SMBus accesses to/from TS are executed[3] 1: SMBus reads from TS return all zeros SMBus writes to TS are acknowledged but not executed
2	RW1O	0	**F2RC2[2]:** SMBus Access control to function spaces 2, 4, 6-15 (Vendor specific) This bit can only be written by control word write 0: SMBus accesses to FN[2,4,6-15] are executed 1: SMBus reads from FN[2,4,6-15] return all zeros SMBus writes to FN[2,4,6-15] are acknowledged but not executed
1	RW1O	0	**F2RC2[1]:** SMBus Access control to function spaces 1, 3, 5 (JEDEC) This bit can only be written by control word write 0: SMBus accesses to FN[1,3,5] are executed 1: SMBus reads from FN[1,3,5] return all zeros SMBus writes to FN[1,3,5] are acknowledged but not executed
0	RW1O	0	**F2RC2[0]:** SMBus Access control to function space 0 (except TS)[4] This bit can only be written by control word write 0: SMBus accesses to/from FN0 are executed 1: All SMBus reads from FN0 return zeros All SMBus writes to FN0 are acknowledged but not executed

NOTE 1 Buffer stops driving Errout_n Low when training had error. Buffer stops training if it was previously started and will stop driving Errout_n Low. Buffer resets Failure and Valid bits.

NOTE 2 Buffer stops driving Errout_n Low when training had error. Buffer stops training if it was previously started and will stop driving Errout_n Low. Buffer does not reset Failure and Valid bits.

NOTE 3 Write accesses to the TS Critical, High and Low Limit registers are controlled by the TCRIT_LOCK and EVENT_LOCK bits in the TS Configuration register

NOTE 4 Accesses to TS registers are unaffected by this bit

15.2.2 Register Description (cont'd)

Table 206 — F2RC5_4 Register

1Ah	F2RC5 – F2RC4		
Bits	**Attr**	**Default**	**Description**
7:6	RW	0	**F2RC5[3:2]:** Number of Rows 00: 8192 Rows; RA[12:0] 01: 16384 Rows; RA[13:0] 10: 32768 Rows; RA[14:0] 11: 65536 Rows; RA[15:0]
5:4	RW	0	**F2RC5[1:0]:** Number of Columns(=Page Size) 00: 1K; CA[9:0] 01: 2K; CA[11,9:0] 10: 4K; CA[13,11,9:0] 11: 8K; CA[2:0] (8 column addresses of BL=8 page size for testing purposes)
3:0	RW	0	**F2RC4[3:0]:** Rank control for MEMBIST 0XXX:MEMBIST applies to All Ranks 1000: Rank 0 1001: Rank 1 1010: Rank 2 1011: Rank 3 1100: Rank 4 1101: Rank 5 1110: Rank 6 1111: Rank 7

15.2.2 Register Description (cont'd)

Table 207 — F2RC7_6 Register

1Bh	F2RC7 – F2RC6		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F2RC7[3:0]:** Function Select (see F0RC7[3:0] for definition)
3	RV	0	**F2RC6[3]:** Reserved
2	RW	0	**F2RC6[2]:** MEMBIST Algorithm 0: Fixed Data 0's (DQ[63:0] only), Full DRAM, Write Full, Read empty, compare, default XYZR order, all physical ranks 1: LFSR data (DQ[71:0]), Full DRAM, Write Full, Read empty, compare, default XYZR order, all physical ranks
1:0	RW	0	**F2RC6[1:0]:** MEMBIST, AREF and SREF Control 00: Normal operation from RESET_n. If MEMBIST was previously started, then[1] 1. Stop MEMBIST 2. Stop AREF 01: Stop AREF, wait till it finishes, then put all ranks of DRAMs into SR 10: Start AREF for all ranks ignoring any rank specified in F2RC4, then start MEMBIST using F2RC4. AREF continues to run after the MEMBIST is complete.[2] 11: Reserved

NOTE 1 Buffer stops driving Errout_n Low if MEMBIST had an error.

NOTE 2 Buffer starts driving Errout_n Low 20 clocks after receiving this command.

Table 208 — F2RC9_8 Register

1Ch	F2RC9 – F2RC8		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F2RC9[3:0]:** DQ[71:68] ECC Pattern 2 (see control word definition for details)
3:0	RW	0	**F2RC8[3:0]:** DQ[67:64] ECC Pattern 1 (see control word definition for details)

Table 209 — F2RC11_10 Register

1Dh	F2RC11 – F2RC10		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F2RC11[3:0]:** DQ[71:68] ECC Pattern 4 (see control word definition for details)
3:0	RW	0	**F2RC10[3:0]:** DQ[67:64] ECC Pattern 3 (see control word definition for details)

15.2.2 Register Description (cont'd)

Table 210 — F2RC13_12 Register

1Eh	F2RC13 – F2RC12		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F2RC13[3:0]:** DQ[71:68] ECC Pattern 6 (see control word definition for details)
3:0	RW	0	**F2RC12[3:0]:** DQ[67:64] ECC Pattern 5 (see control word definition for details)

Table 211 — F2RC15_14 Register

1Fh	F2RC15 – F2RC14		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F2RC15[3:0]:** DQ[71:68] ECC Pattern 8 (see control word definition for details)
3:0	RW	0	**F2RC14[3:0]:** DQ[67:64] ECC Pattern 7 (see control word definition for details)

Table 212 — F3RC1_0 Register

20h	F3RC1 – F3RC0		
Bits	**Attr**	**Default**	**Description**
7	RW	0	**F3RC1[3]:** Vref for DQ 0: Use VrefDQ input pin for receiver reference voltage 1: Use internally generated Vref for receiver reference voltage
6:4	RW	0	**F3RC1[2:0]:** RTT_WR 000: Dynamic ODT off 001: RZQ/4 (60 Ohm) 010: RZQ/2 (120 Ohm) 011: RZQ/6 (40 Ohm) 100: Reserved 101: RZQ/8 (30 Ohm) 110: RZQ (240 Ohm) 111: RZQ/3 (80 Ohm)
3	RW	0	**F3RC0[3]:** TDQS Enable 0: TDQS disabled 1: TDQS enabled
2:0	RW	0	**F3RC0[2:0]:** RTT_Nom 000: RTT_Nom disabled 001: RZQ/4 (60 Ohm) 010: RZQ/2 (120 Ohm) 011: RZQ/6 (40 Ohm) 100: Reserved 101: RZQ/8 (30 Ohm) 110: RZQ (240 Ohm) 111: RZQ/3 (80 Ohm)

15.2.2 Register Description (cont'd)

Table 213 — F3RC3_2 Register

21h	F3RC3 – F3RC2		
Bits	**Attr**	**Default**	**Description**
7:4	RV	0	**F3RC3[3:0]:** Reserved
3	RW	0	F3RC2[3]: Connector Interface DQ Driver Enable 0: Connector interface DQ/DQS drivers enabled 1: Connector interface DQ/DQS drivers disabled
2:0	RW	0	**F3RC2[2:0]:** Connector Interface DQ/DQS Output Driver Impedance Control 000: RZQ/6 (40 Ohm) 001: RZQ/7 (34 Ohm) 010: RZQ/5 (48 Ohm) 011: RZQ/9 (27 Ohm) 100: RZQ/12 (20 Ohm) 101: Reserved 110: Reserved 111: Reserved

Table 214 — F3RC7_6 Register

23h	F3RC7 – F3RC6		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F3RC7[3:0]:** Function Select (see F0RC7[3:0] for definition)
3	RW	0	**F3RC6[3]:** Connector Interface DRAM Width 0: same as DRAM bus width (in F0RC14) 1: Always 8 DQs per DQS[1]
2	RV	0	**F3RC6[2]:** Reserved
1:0	RW	0	**F3RC6[1:0]:** Connector Interface DQ Timing Mode 00: Minimum latency 01: Minimum skew 10: Reserved 11: Reserved

NOTE 1 MB transmits and receives only one strobe per byte for Read and Write operation respectively on connector interface. MB transmits and receives one strobe pair per DRAM for Write and Read on DRAM interface. MB turns off its input receivers and terminations for upper 9 strobe pairs on connector interface.

Table 215 — F3RC9_8 Register

24h	F3RC9 – F3RC8		
Bits	**Attr**	**Default**	**Description**
7	RW	0	**F3RC9[3]:** DRAM Interface Output Driver Disable 0: DRAM interface MDQ/MDQS output drivers enabled 1: DRAM interface MDQ/MDQS output drivers disabled
6:4	RW	0	**F3RC9[2:0]:** DRAM Interface Output Driver Impedance Control 000: RZQ/6 (40 Ohm) 001: RZQ/7 (34 Ohm) 010: RZQ/5 (48 Ohm) 011: RZQ/9 (27 Ohm) 100: RZQ/12 (20 Ohm) 101: Reserved 110: Reserved 111: Reserved
3	RV	0	**F3RC8[3]:** Reserved
2:0	RW	0	**F3RC8[2:0]:** DRAM Interface MDQ/MDQS ODT Strength 000: DRAM interface ODT disabled 001: RZQ/4 (60 Ohm) 010: RZQ/2 (120 Ohm) 011: RZQ/6 (40 Ohm) 100: Reserved 101: RZQ/8 (30 Ohm) 110: RZQ (240 Ohm) 111: RZQ/3 (80 Ohm)

Table 216 — F3RC11_10 Register

25h	F3RC11 – F3RC10		
Bits	**Attr**	**Default**	**Description**
7:6	RV	0	**F3RC11[3:2]:** Reserved
5	RW	0	**F3RC11[1]:** Rank0 Write QxODT1 Control 0: Not asserted during Write 1: Asserted during Write
4	RW	0	**F3RC11[0]:** Rank0 Write QxODT0 Control 0: Not asserted during Write 1: Asserted during Write
3:2	RV	0	**F3RC10[3:2]:** Reserved
1	RW	0	**F3RC10[1]:** Rank0 Read QxODT1 Control 0: Not asserted during Read 1: Asserted during Read
0	RW	0	**F3RC10[0]:** Rank0 Read QxODT0 Control 0: Not asserted during Read 1: Asserted during Read

15.2.2 Register Description (cont'd)

Table 217 — F3RC13_12 Register

26h	F3RC13 – F3RC12		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F3RC13[3:0]:** Byte 0 Minimum Skew Mode Additive Write Offset 0000: tWOFFSET=0 0001: tWOFFSET=1/16 tCK 0010: tWOFFSET=2/16 tCK 0011: tWOFFSET=3/16 tCK 0100: tWOFFSET=4/16 tCK 0101: tWOFFSET=5/16 tCK 0110: tWOFFSET=6/16 tCK 0111: tWOFFSET=7/16 tCK 1000: tWOFFSET=8/16 tCK 1001: tWOFFSET=9/16 tCK 1010: tWOFFSET=10/16 tCK 1011: tWOFFSET=11/16 tCK 1100: tWOFFSET=12/16 tCK 1101: tWOFFSET=13/16 tCK 1110: tWOFFSET=14/16 tCK 1111: tWOFFSET=15/16 tCK
3:0	RW	0	**F3RC12[3:0]:** Byte 0 Minimum Skew Mode Additive Read Offset 0000: tROFFSET=0 0001: tROFFSET=1/16 tCK 0010: tROFFSET=2/16 tCK 0011: tROFFSET=3/16 tCK 0100: tROFFSET=4/16 tCK 0101: tROFFSET=5/16 tCK 0110: tROFFSET=6/16 tCK 0111: tROFFSET=7/16 tCK 1000: tROFFSET=8/16 tCK 1001: tROFFSET=9/16 tCK 1010: tROFFSET=10/16 tCK 1011: tROFFSET=11/16 tCK 1100: tROFFSET=12/16 tCK 1101: tROFFSET=13/16 tCK 1110: tROFFSET=14/16 tCK 1111: tROFFSET=15/16 tCK

15.2.2 Register Description (cont'd)

Table 218 — F4RC7_6 Register

2Bh	F4RC7 – F4RC6		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F4RC7[3:0]:** Function Select (see F0RC7[3:0] for definition)
3:0	RV	0	**F4RC6[3:0]:** Reserved

Table 219 — F4RC11_10 Register

2Dh	F4RC11 – F4RC10		
Bits	**Attr**	**Default**	**Description**
7:6	RV	0	**F4RC11[3:2]:** Reserved
5	RW	0	**F4RC11[1]:** Rank1 Write QxODT1 Control 0: Not asserted during write 1: Asserted during write
4	RW	0	**F4RC11[0]:** Rank1 Write QxODT0 Control 0: Not asserted during write 1: Asserted during write
3:2	RV	0	**F4RC10[3:2]:** Reserved
1	RW	0	**F4RC10[1]:** Rank1 Read QxODT1 Control 0: Not asserted during read 1: Asserted during read
0	RW	0	**F4RC10[0]:** Rank1 Read QxODT0 Control 0: Not asserted during read 1: Asserted during read

15.2.2 Register Description (cont'd)

Table 220 — F4RC13_12 Register

2Eh	F4RC13 – F4RC12		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F4RC13[3:0]:** Byte 1 Minimum Skew Mode Additive Write Offset 0000: tWOFFSET=0 0001: tWOFFSET=1/16 tCK 0010: tWOFFSET=2/16 tCK 0011: tWOFFSET=3/16 tCK 0100: tWOFFSET=4/16 tCK 0101: tWOFFSET=5/16 tCK 0110: tWOFFSET=6/16 tCK 0111: tWOFFSET=7/16 tCK 1000: tWOFFSET=8/16 tCK 1001: tWOFFSET=9/16 tCK 1010: tWOFFSET=10/16 tCK 1011: tWOFFSET=11/16 tCK 1100: tWOFFSET=12/16 tCK 1101: tWOFFSET=13/16 tCK 1110: tWOFFSET=14/16 tCK 1111: tWOFFSET=15/16 tCK
3:0	RW	0	**F4RC12[3:0]:** Byte 1 Minimum Skew Mode Additive Read Offset 0000: tROFFSET=0 0001: tROFFSET=1/16 tCK 0010: tROFFSET=2/16 tCK 0011: tROFFSET=3/16 tCK 0100: tROFFSET=4/16 tCK 0101: tROFFSET=5/16 tCK 0110: tROFFSET=6/16 tCK 0111: tROFFSET=7/16 tCK 1000: tROFFSET=8/16 tCK 1001: tROFFSET=9/16 tCK 1010: tROFFSET=10/16 tCK 1011: tROFFSET=11/16 tCK 1100: tROFFSET=12/16 tCK 1101: tROFFSET=13/16 tCK 1110: tROFFSET=14/16 tCK 1111: tROFFSET=15/16 tCK

15.2.2 Register Description (cont'd)

Table 221 — F5RC7_6 Register

33h	F5RC7 – F5RC6		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F5RC7[3:0]:** Function Select (see F0RC7[3:0] for definition)
3:0	RV	0	**F5RC6[3:0]:** Reserved

Table 222 — F5RC11_10 Register

35h	F5RC11 – F5RC8		
Bits	**Attr**	**Default**	**Description**
7:6	RV	0	**F5RC11[3:2]:** Reserved
5	RW	0	**F5RC11[1]:** Rank2 Write QxODT1 Control 0: Not asserted during write 1: Asserted during write
4	RW	0	**F5RC11[0]:** Rank2 Write QxODT0 Control 0: Not asserted during write 1: Asserted during write
3:2	RV	0	**F5RC10[3:2]:** Reserved
1	RW	0	**F5RC10[1]:** Rank2 Read QxODT1 Control 0: Not asserted during read 1: Asserted during read
0	RW	0	**F5RC10[0]:** Rank2 Read QxODT0 Control 0: Not asserted during read 1: Asserted during read

15.2.2 Register Description (cont'd)

Table 223 — F5RC13_12 Register

36h	F5RC13 – F5RC12		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F5RC13[3:0]:** Byte 2 Minimum Skew Mode Additive Write Offset 0000: tWOFFSET=0 0001: tWOFFSET=1/16 tCK 0010: tWOFFSET=2/16 tCK 0011: tWOFFSET=3/16 tCK 0100: tWOFFSET=4/16 tCK 0101: tWOFFSET=5/16 tCK 0110: tWOFFSET=6/16 tCK 0111: tWOFFSET=7/16 tCK 1000: tWOFFSET=8/16 tCK 1001: tWOFFSET=9/16 tCK 1010: tWOFFSET=10/16 tCK 1011: tWOFFSET=11/16 tCK 1100: tWOFFSET=12/16 tCK 1101: tWOFFSET=13/16 tCK 1110: tWOFFSET=14/16 tCK 1111: tWOFFSET=15/16 tCK
3:0	RW	0	**F5RC12[3:0]:** Byte 2 Minimum Skew Mode Additive Read Offset 0000: tROFFSET=0 0001: tROFFSET=1/16 tCK 0010: tROFFSET=2/16 tCK 0011: tROFFSET=3/16 tCK 0100: tROFFSET=4/16 tCK 0101: tROFFSET=5/16 tCK 0110: tROFFSET=6/16 tCK 0111: tROFFSET=7/16 tCK 1000: tROFFSET=8/16 tCK 1001: tROFFSET=9/16 tCK 1010: tROFFSET=10/16 tCK 1011: tROFFSET=11/16 tCK 1100: tROFFSET=12/16 tCK 1101: tROFFSET=13/16 tCK 1110: tROFFSET=14/16 tCK 1111: tROFFSET=15/16 tCK

15.2.2 Register Description (cont'd)

Table 224 — F6RC7_6 Register

3Bh	F6RC7 – F6RC6		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F6RC7[3:0]:** Function Select (see F0RC7[3:0] for definition)
3:0	RV	0	**F6RC6[3:0]:** Reserved

Table 225 — F6RC11_10 Register

3Dh	F6RC11 – F6RC10		
Bits	**Attr**	**Default**	**Description**
7:6	RV	0	**F6RC11[3:2]:** Reserved
5	RW	0	**F6RC11[1]:** Rank3 Write QxODT1 Control 0: Not asserted during write 1: Asserted during write
4	RW	0	**F6RC11[0]:** Rank3 Write QxODT0 Control 0: Not asserted during write 1: Asserted during write
3:2	RV	0	**F6RC10[3:2]:** Reserved
1	RW	0	**F6RC10[1]:** Rank3 Read QxODT1 Control 0: Not asserted during read 1: Asserted during read
0	RW	0	**F6RC10[0]:** Rank3 Read QxODT0 Control 0: Not asserted during read 1: Asserted during read

15.2.2 Register Description (cont'd)

Table 226 — F6RC13_12 Register

3Eh	F6RC13 – F6RC12		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F6RC13[3:0]:** Byte 3 Minimum Skew Mode Additive Write Offset 0000: tWOFFSET=0 0001: tWOFFSET=1/16 tCK 0010: tWOFFSET=2/16 tCK 0011: tWOFFSET=3/16 tCK 0100: tWOFFSET=4/16 tCK 0101: tWOFFSET=5/16 tCK 0110: tWOFFSET=6/16 tCK 0111: tWOFFSET=7/16 tCK 1000: tWOFFSET=8/16 tCK 1001: tWOFFSET=9/16 tCK 1010: tWOFFSET=10/16 tCK 1011: tWOFFSET=11/16 tCK 1100: tWOFFSET=12/16 tCK 1101: tWOFFSET=13/16 tCK 1110: tWOFFSET=14/16 tCK 1111: tWOFFSET=15/16 tCK
3:0	RW	0	**F6RC12[3:0]:** Byte 3 Minimum Skew Mode Additive Read Offset 0000: tROFFSET=0 0001: tROFFSET=1/16 tCK 0010: tROFFSET=2/16 tCK 0011: tROFFSET=3/16 tCK 0100: tROFFSET=4/16 tCK 0101: tROFFSET=5/16 tCK 0110: tROFFSET=6/16 tCK 0111: tROFFSET=7/16 tCK 1000: tROFFSET=8/16 tCK 1001: tROFFSET=9/16 tCK 1010: tROFFSET=10/16 tCK 1011: tROFFSET=11/16 tCK 1100: tROFFSET=12/16 tCK 1101: tROFFSET=13/16 tCK 1110: tROFFSET=14/16 tCK 1111: tROFFSET=15/16 tCK

15.2.2 Register Description (cont'd)

Table 227 — F7RC7_6 Register

43h	F7RC7 – F7RC6		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F7RC7[3:0]:** Function Select (see F0RC7[3:0] for definition)
3:0	RV	0	**F7RC6[3:0]:** Reserved

Table 228 — F7RC11_10 Register

45h	F7RC11 – F7RC10		
Bits	**Attr**	**Default**	**Description**
7:6	RV	0	**F7RC11[3:2]:** Reserved
15	RW	0	**F7RC11[1]:** Rank4 Write QxODT1 Control 0: Not asserted during write 1: Asserted during write
4	RW	0	**F7RC11[0]:** Rank4 Write QxODT0 Control 0: Not asserted during write 1: Asserted during write
3:2	RV	0	**F7RC10[3:2]:** Reserved
1	RW	0	**F7RC10[1]:** Rank4 Read QxODT1 Control 0: Not asserted during read 1: Asserted during read
0	RW	0	**F7RC10[0]:** Rank4 Read QxODT0 Control 0: Not asserted during read 1: Asserted during read

Table 229 — F7RC13_12 Register

46h	F7RC13 – F7RC12		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F7RC13[3:0]:** Byte 4 Minimum Skew Mode Additive Write Offset 0000: tWOFFSET=0 0001: tWOFFSET=1/16 tCK 0010: tWOFFSET=2/16 tCK 0011: tWOFFSET=3/16 tCK 0100: tWOFFSET=4/16 tCK 0101: tWOFFSET=5/16 tCK 0110: tWOFFSET=6/16 tCK 0111: tWOFFSET=7/16 tCK 1000: tWOFFSET=8/16 tCK 1001: tWOFFSET=9/16 tCK 1010: tWOFFSET=10/16 tCK 1011: tWOFFSET=11/16 tCK 1100: tWOFFSET=12/16 tCK 1101: tWOFFSET=13/16 tCK 1110: tWOFFSET=14/16 tCK 1111: tWOFFSET=15/16 tCK
3:0	RW	0	**F7RC12[3:0]:** Byte 4 Minimum Skew Mode Additive Read Offset 0000: tROFFSET=0 0001: tROFFSET=1/16 tCK 0010: tROFFSET=2/16 tCK 0011: tROFFSET=3/16 tCK 0100: tROFFSET=4/16 tCK 0101: tROFFSET=5/16 tCK 0110: tROFFSET=6/16 tCK 0111: tROFFSET=7/16 tCK 1000: tROFFSET=8/16 tCK 1001: tROFFSET=9/16 tCK 1010: tROFFSET=10/16 tCK 1011: tROFFSET=11/16 tCK 1100: tROFFSET=12/16 tCK 1101: tROFFSET=13/16 tCK 1110: tROFFSET=14/16 tCK 1111: tROFFSET=15/16 tCK

Table 230 — F8RC7_6 Register

4Bh	F8RC7 – F8RC6		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F8RC7[3:0]:** Function Select (see F0RC7[3:0] for definition)
3:0	RV	0	**F8RC6[3:0]:** Reserved

Table 231 — F8RC11_10 Register

4Dh	F8RC11 – F8RC10		
Bits	**Attr**	**Default**	**Description**
7:6	RV	0	**F8RC11[3:2]:** Reserved
5	RW	0	**F8RC11[1]:** Rank5 Write QxODT1 Control 0: Not asserted during write 1: Asserted during write
4	RW	0	**F8RC11[0]:** Rank5 Write QxODT0 Control 0: Not asserted during write 1: Asserted during write
3:2	RV	0	**F8RC10[3:2]:** Reserved
1	RW	0	**F8RC10[1]:** Rank5 Read QxODT1 Control 0: Not asserted during read 1: Asserted during read
0	RW	0	**F8RC10[0]:** Rank5 Read QxODT0 Control 0: Not asserted during read 1: Asserted during read

Table 232 — F8RC13_12 Register

4Eh	F8RC13 – F8RC12		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F8RC13[3:0]:** Byte 5 Minimum Skew Mode Additive Write Offset 0000: tWOFFSET=0 0001: tWOFFSET=1/16 tCK 0010: tWOFFSET=2/16 tCK 0011: tWOFFSET=3/16 tCK 0100: tWOFFSET=4/16 tCK 0101: tWOFFSET=5/16 tCK 0110: tWOFFSET=6/16 tCK 0111: tWOFFSET=7/16 tCK 1000: tWOFFSET=8/16 tCK 1001: tWOFFSET=9/16 tCK 1010: tWOFFSET=10/16 tCK 1011: tWOFFSET=11/16 tCK 1100: tWOFFSET=12/16 tCK 1101: tWOFFSET=13/16 tCK 1110: tWOFFSET=14/16 tCK 1111: tWOFFSET=15/16 tCK
3:0	RW	0	**F8RC12[3:0]:** Byte 5 Minimum Skew Mode Additive Read Offset 0000: tROFFSET=0 0001: tROFFSET=1/16 tCK 0010: tROFFSET=2/16 tCK 0011: tROFFSET=3/16 tCK 0100: tROFFSET=4/16 tCK 0101: tROFFSET=5/16 tCK 0110: tROFFSET=6/16 tCK 0111: tROFFSET=7/16 tCK 1000: tROFFSET=8/16 tCK 1001: tROFFSET=9/16 tCK 1010: tROFFSET=10/16 tCK 1011: tROFFSET=11/16 tCK 1100: tROFFSET=12/16 tCK 1101: tROFFSET=13/16 tCK 1110: tROFFSET=14/16 tCK 1111: tROFFSET=15/16 tCK

Table 233 — F9RC7_6 Register

53h	F9RC7 – F9RC6		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F9RC7[3:0]:** Function Select (see F0RC7[3:0] for definition)
3:0	RV	0	**F9RC6[3:0]:** Reserved

Table 234 — F9RC11_10 Register

55h	F9RC11 – F9RC10		
Bits	**Attr**	**Default**	**Description**
7:6	RV	0	**F9RC11[3:2]:** Reserved
5	RW	0	**F9RC11[1]:** Rank6 Write QxODT1 Control 0: Not asserted during write 1: Asserted during write
4	RW	0	**F9RC11[0]:** Rank6 Write QxODT0 Control 0: Not asserted during write 1: Asserted during write
3:2	RV	0	**F9RC10[3:2]:** Reserved
1	RW	0	**F9RC10[1]:** Rank6 Read QxODT1 Control 0: Not asserted during read 1: Asserted during read
0	RW	0	**F9RC10[0]:** Rank6 Read QxODT0 Control 0: Not asserted during read 1: Asserted during read

Table 235 — F9RC13_12 Register

56h	F9RC13 – F9RC12		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F9RC13[3:0]:** Byte 6 Minimum Skew Mode Additive Write Offset 0000: tWOFFSET=0 0001: tWOFFSET=1/16 tCK 0010: tWOFFSET=2/16 tCK 0011: tWOFFSET=3/16 tCK 0100: tWOFFSET=4/16 tCK 0101: tWOFFSET=5/16 tCK 0110: tWOFFSET=6/16 tCK 0111: tWOFFSET=7/16 tCK 1000: tWOFFSET=8/16 tCK 1001: tWOFFSET=9/16 tCK 1010: tWOFFSET=10/16 tCK 1011: tWOFFSET=11/16 tCK 1100: tWOFFSET=12/16 tCK 1101: tWOFFSET=13/16 tCK 1110: tWOFFSET=14/16 tCK 1111: tWOFFSET=15/16 tCK
3:0	RW	0	**F9RC12[3:0]:** Byte 6 Minimum Skew Mode Additive Read Offset 0000: tROFFSET=0 0001: tROFFSET=1/16 tCK 0010: tROFFSET=2/16 tCK 0011: tROFFSET=3/16 tCK 0100: tROFFSET=4/16 tCK 0101: tROFFSET=5/16 tCK 0110: tROFFSET=6/16 tCK 0111: tROFFSET=7/16 tCK 1000: tROFFSET=8/16 tCK 1001: tROFFSET=9/16 tCK 1010: tROFFSET=10/16 tCK 1011: tROFFSET=11/16 tCK 1100: tROFFSET=12/16 tCK 1101: tROFFSET=13/16 tCK 1110: tROFFSET=14/16 tCK 1111: tROFFSET=15/16 tCK

Table 236 — F10RC7_6 Register

5Bh	F10RC7 – F10RC6		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F10RC7[3:0]:** Function Select (see F0RC7[3:0] for definition)
3:0	RV	0	**F10RC6[3:0]:** Reserved

Table 237 — F10RC11_10 Register

5Dh	F10RC11 – F10RC10		
Bits	**Attr**	**Default**	**Description**
7:6	RV	0	**F10RC11[3:2]:** Reserved
5	RW	0	**F10RC11[1]:** Rank7 Write QxODT1 Control 0: Not asserted during write 1: Asserted during write
4	RW	0	**F10RC11[0]:** Rank7 Write QxODT0 Control 0: Not asserted during write 1: Asserted during write
3:2	RV	0	**F10RC10[3:2]:** Reserved
1	RW	0	**F10RC10[1]:** Rank7 Read QxODT1 Control 0: Not asserted during read 1: Asserted during read
0	RW	0	**F10RC10[0]:** Rank7 Read QxODT0 Control 0: Not asserted during read 1: Asserted during read

Table 238 — F10RC13_12 Register

5Eh	F10RC13 – F10RC12		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F10RC13[3:0]:** Byte 7 Minimum Skew Mode Additive Write Offset 0000: tWOFFSET=0 0001: tWOFFSET=1/16 tCK 0010: tWOFFSET=2/16 tCK 0011: tWOFFSET=3/16 tCK 0100: tWOFFSET=4/16 tCK 0101: tWOFFSET=5/16 tCK 0110: tWOFFSET=6/16 tCK 0111: tWOFFSET=7/16 tCK 1000: tWOFFSET=8/16 tCK 1001: tWOFFSET=9/16 tCK 1010: tWOFFSET=10/16 tCK 1011: tWOFFSET=11/16 tCK 1100: tWOFFSET=12/16 tCK 1101: tWOFFSET=13/16 tCK 1110: tWOFFSET=14/16 tCK 1111: tWOFFSET=15/16 tCK
3:0	RW	0	**F10RC12[3:0]:** Byte 7 Minimum Skew Mode Additive Read Offset 0000: tROFFSET=0 0001: tROFFSET=1/16 tCK 0010: tROFFSET=2/16 tCK 0011: tROFFSET=3/16 tCK 0100: tROFFSET=4/16 tCK 0101: tROFFSET=5/16 tCK 0110: tROFFSET=6/16 tCK 0111: tROFFSET=7/16 tCK 1000: tROFFSET=8/16 tCK 1001: tROFFSET=9/16 tCK 1010: tROFFSET=10/16 tCK 1011: tROFFSET=11/16 tCK 1100: tROFFSET=12/16 tCK 1101: tROFFSET=13/16 tCK 1110: tROFFSET=14/16 tCK 1111: tROFFSET=15/16 tCK

Table 239 — F11RC7_6 Register

63h	F5RC7 – F5RC6		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F11RC7[3:0]:** Function Select (see F0RC7[3:0] for definition)
3:0	RV	0	**F11RC6[3:0]:** Reserved

Table 240 — F11RC13_12 Register

66h	F11RC13 – F11RC12		
Bits	**Attr**	**Default**	**Description**
15:8	RO	0	**F11RC15[3:0] - F11RC14[3:0]:** Reserved
7:4	RW	0	**F11RC13[3:0]:** Byte 8 Minimum Skew Mode Additive Write Offset 0000: tWOFFSET=0 0001: tWOFFSET=1/16 tCK 0010: tWOFFSET=2/16 tCK 0011: tWOFFSET=3/16 tCK 0100: tWOFFSET=4/16 tCK 0101: tWOFFSET=5/16 tCK 0110: tWOFFSET=6/16 tCK 0111: tWOFFSET=7/16 tCK 1000: tWOFFSET=8/16 tCK 1001: tWOFFSET=9/16 tCK 1010: tWOFFSET=10/16 tCK 1011: tWOFFSET=11/16 tCK 1100: tWOFFSET=12/16 tCK 1101: tWOFFSET=13/16 tCK 1110: tWOFFSET=14/16 tCK 1111: tWOFFSET=15/16 tCK
3:0	RW	0	**F11RC12[3:0]:** Byte 8 Minimum Skew Mode Additive Read Offset 0000: tROFFSET=0 0001: tROFFSET=1/16 tCK 0010: tROFFSET=2/16 tCK 0011: tROFFSET=3/16 tCK 0100: tROFFSET=4/16 tCK 0101: tROFFSET=5/16 tCK 0110: tROFFSET=6/16 tCK 0111: tROFFSET=7/16 tCK 1000: tROFFSET=8/16 tCK 1001: tROFFSET=9/16 tCK 1010: tROFFSET=10/16 tCK 1011: tROFFSET=11/16 tCK 1100: tROFFSET=12/16 tCK 1101: tROFFSET=13/16 tCK 1110: tROFFSET=14/16 tCK 1111: tROFFSET=15/16 tCK

Table 241 — F13RC9_8 Register

74h	F13RC9 – F13RC8		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F13RC9[3:0]:** Selects SMBus Function 0000: SMBus Function 0 0001: SMBus Function 1 0010: SMBus Function 2 0011: SMBus Function 3 0100: SMBus Function 4 0101: SMBus Function 5 0110: SMBus Function 6 0111: SMBus Function 7 1000: SMBus Function 8 1001: SMBus Function 9 1010: SMBus Function 10 1011: SMBus Function 11 1100: SMBus Function 12 1101: SMBus Function 13 1110: SMBus Function 14 1111: SMBus Function 15
3:0	RV	0	**F13RC8[3:0]:** Reserved

Table 242 — F13RC11_10 Register

75h	F13RC11 – F13RC10		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F13RC11[3:0]:** MSB of Register Address Port (Address Bits[7:4])
3:0	RW	0	**F13RC10[3:0]:** LSB of Register Address Port (Address Bits[3:0])

Table 243 — F13RC13_12 Register

76h	F13RC13 – F13RC12		
Bits	**Attr**	**Default**	**Description**
7:4	RV	0	**F13RC13[3:0**] Reserved
3:0	RW	0	**F13RC12[3:0]:** Extended Address Port (Bits[11:8])

Table 244 — F13RC15_14 Register

77h	F13RC15 – F13RC14		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F13RC15[3:0]:** MSB of Data Port
3:0	RW	0	**F13RC14[3:0]:** LSB of Data Port

Table 245 — F14RC1_0 Register

78h	F14RC1 – F14RC0		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F14RC1[3:0]:** Personality Byte 0 bits 7:4
3:0	RW	0	**F14RC0[3:0]:** Personality Byte 0 bits 3:0

Table 246 — F14RC3_2 Register

79h	F14RC3 – F14RC2		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F14RC3[3:0]:** Personality Byte 1 bits 7:4
3:0	RW	0	**F14RC2[3:0]:** Personality Byte 1 bits 3:0

Table 247 — F14RC5_4 Register

7Ah	F14RC5 – F14RC4		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F14RC5[3:0]:** Personality Byte 2 bits 7:4
3:0	RW	0	**F14RC4[3:0]:** Personality Byte 2 bits 3:0

Table 248 — F14RC7_6 Register

7Bh	F14RC7 – F14RC6		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F14RC7[3:0]:** Function Select (see F0RC7[3:0] for definition)
3:0	RV	0	**F14RC6[3:0]:** Personality Byte 3 bits 3:0

Table 249 — F14RC9_8 Register

7Ch	F14RC9 – F14RC8		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F14RC9[3:0]:** Personality Byte 4 bits 7:4
3:0	RW	0	**F14RC8[3:0]:** Personality Byte 4 bits 3:0

Table 250 — F14RC11_10 Register

7Dh	F14RC11 – F14RC10		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F14RC11[3:0]:** Personality Byte 5 bits 7:4
3:0	RW	0	**F14RC10[3:0]:** Personality Byte 5 bits 3:0

Table 251 — F14RC13_12 Register

7Eh	F14RC13 – F14RC12		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F14RC13[3:0]:** Personality Byte 6 bits 7:4
3:0	RW	0	**F14RC12[3:0]:** Personality Byte 6 bits 3:0

Table 252 — F14RC15_14 Register

7Fh	F14RC15 – F14RC14		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F14RC15[3:0]:** Personality Byte 7 bits 7:4
3:0	RW	0	**F14RC14[3:0]:** Personality Byte 7 bits 3:0

Table 253 — F15RC1_0 Register

80h	F15RC1 – F15RC0		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F15RC1[3:0]:** Personality Byte 8 bits 7:4
3:0	RW	0	**F15RC0[3:0]:** Personality Byte 8 bits 3:0

Table 254 — F15RC3_2 Register

81h	F15RC3 – F15RC2		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F15RC3[3:0]:** Personality Byte 9 bits 7:4
3:0	RW	0	**F15RC2[3:0]:** Personality Byte 9 bits 3:0

Table 255 — F15RC5_4 Register

82h	F15RC5 – F15RC4		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F15RC5[3:0]:** Personality Byte 10 bits 7:4
3:0	RW	0	**F15RC4[3:0]:** Personality Byte 10 bits 3:0

Table 256 — F15RC7_6 Register

83h	F15RC7 – F15RC6		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F15RC7[3:0]:** Function Select (see F0RC7[3:0] for definition)
3:0	RV	0	**F15RC6[3:0]:** Personality Byte 3 bits 7:4

Table 257 — F15RC9_8 Register

84h	F15RC9 – F15RC8		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F15RC9[3:0]:** Personality Byte 11 bits 7:4
3:0	RW	0	**F15RC8[3:0]:** Personality Byte 11 bits 3:0

Table 258 — F15RC11_10 Register

85h	F15RC11 – F15RC10		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F15RC11[3:0]:** Personality Byte 12 bits 7:4
3:0	RW	0	**F15RC10[3:0]:** Personality Byte 12 bits 3:0

Table 259 — F15RC13_12 Register

86h	F15RC13 – F15RC12		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F15RC13[3:0]:** Personality Byte 13 bits 7:4
3:0	RW	0	**F15RC12[3:0]:** Personality Byte 13 bits 3:0

Table 260 — F15RC15_14 Register

87h	F15RC15 – F15RC14		
Bits	**Attr**	**Default**	**Description**
7:4	RW	0	**F15RC15[3:0]:** Personality Byte 14 bits 7:4
3:0	RW	0	**F15RC14[3:0]:** Personality Byte 14 bits 3:0

Table 261 — TS Capabilities Register

A1:A0h	TS Capabilities		
Bits	**Attr**	**Default**	**Description**
15:8	RV	0	Reserved. Must be programmed as '0' for future compatibility.
7	RO	0	EVSD - EVENT_n with Shutdown action '0' (default) - The EVENT_n output freezes in its current state when entering shutdown. Upon exiting shutdown, the EVENT_n output remains in the previous state until the next thermal sample is taken, or possibly sooner if EVENT_n is programmed for comparator mode. '1' - The EVENT_n output is deasserted (not driven) when entering shutdown, and remains deasserted upon exit from shutdown until the next thermal sample is taken, or possibly sooner if EVENT_n is programmed for comparator mode.
6	RO	0	TMOUT - Bus timeout period for thermal sensor access during normal operation. Note that bus timeout support is optional in shutdown mode. '0' (default) - Parameter $t_{TIMEOUT}$ is supported within the range of 10 to 60 ms. '1' - Parameter $t_{TIMEOUT}$ is supported within the range of 25 to 35 ms (SMBus compatible).
5	RV	X	X - May be 0 or 1; applications must accept either code.
4:3	RO	0	TRES[1:0] - Indicates the resolution of the temperature monitor. See Temperature Sensor section for details.
2	RO	0	RANGE - Indicates the supported temperature range. '0' - The temperature monitor clamps values lower than 0 °C. '1' (default) - The temperature monitor can read temperatures below 0 °C and sets the sign bit appropriately.
1	RO	1	ACC - Indicates the supported temperature accuracy. '0' - NA '1' (default) - The temperature monitor has ±1 °C accuracy over the active range (75 °C to 95 °C) and 2°C accuracy over the monitoring range (40 °C to 125 °C)
0	RO	1	EVENT - Indicates whether the temperature monitor supports interrupt capabilities '0' - NA '1' (default) - The device supports interrupt capabilities.

Table 262 — TS Configuration Register

A3:A2h	TS Configuration		
Bits	**Attr**	**Default**	**Description**
15:11	RV	0	Reserved. Must be programmed as '0' for future compatibility.
10:9	RW	0	HYSTERESIS bits. See Temperature Sensor section for details.
8	RW	0	SHDN - Shutdown. The thermal sensing device and A/D converter are disabled to save power, no events will be generated. When either of the lock bits is set, this bit cannot be set until unlocked. However it can be cleared at any time. When in shutdown mode, the device still responds to commands normally, however, bus timeout may or may not be supported in this mode. '0' (default) - The thermal sensor is active and converting. '1' - The thermal sensor is disabled and will not generate interrupts or update the temperature data.
7	RW	0	TCRIT_LOCK - Locks the TCRIT Limit Register from being updated. '0' (default) - The TCRIT Limit Register can be updated normally. '1' - The TCRIT Limit Register is locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal power on reset.
6	RW	0	EVENT_LOCK - Locks the High and Low Limit Registers from being updated. '0' (default) - The High and Low Limit Registers can be updated normally. '1' - The High and Low Limit Registers are locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal power on reset.
5	WO	0	CLEAR - Clears the EVENT_n pin when it has been asserted. This bit is write only and will always read '0'. '0' - does nothing '1' - The EVENT_n pin is released and will not be asserted until a new interrupt condition occurs. This bit is ignored if the device is operating in Comparator Mode. This bit is self clearing.
4	RO	0	EVENT_STS - Indicates if the EVENT_n pin is asserted. This bit is read only. '0' (default) - The EVENT_n pin is not being asserted by the device. '1' - The EVENT_n pin is being asserted by the device.
3	RW	0	EVENT_CTRL - Masks the EVENT_n pin from generating an interrupt. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered. '0' (default) - The EVENT_n pin is disabled and will not generate interrupts. '1' - The EVENT_n pin is enabled.
2	RW	0	TCRIT_ONLY - Controls whether the EVENT_n pin will be asserted from a high / low out-of-limit condition. When the EVENT_LOCK bit is set, this bit cannot be altered. '0' (default) - The EVENT_n pin will be asserted if the measured temperature is above the High Limit or below the Low Limit in addition to if the temperature is above the TCRIT Limit. '1' - The EVENT_n pin will only be asserted if the measured temperature is above the TCRIT Limit.
1	RW	1	EVENT_POL - Controls the "active" state of the EVENT_n pin. The EVENT_n pin is driven to this state when it is asserted. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered. '0' (default) - The EVENT_n pin is active low. The "active" state of the pin will be logical '0'. '1' - The EVENT_n pin is active high. The "active" state of the pin will be logical '1'.
0	RW	1	EVENT_MODE - Controls the behavior of the EVENT_n pin. The EVENT_n pin may function in either comparator or interrupt mode. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered. '0' - The EVENT_n pin will function in comparator mode '1' - The EVENT_n pin will function in interrupt mode

Table 263 — TS High Limit Register

A5:A4h	TS High Limit		
Bits	**Attr**	**Default**	**Description[a]**
15:13	RV	0	Reserved. Must be programmed as ‘0’ for future compatibility.
12	RW	0	Sign
11	RW	0	128
10	RW	0	64
9	RW	0	32
8	RW	0	16
7	RW	0	8
6	RW	0	4
5	RW	0	2
4	RW	0	1
3	RW	0	0.5
2	RW	0	0.25
1:0	RV	0	Reserved. Must be programmed as ‘0’ for future compatibility.

NOTES:
a. Temperature is in two’s complement format. See Temperature Sensor section for details.

Table 264 — TS Low Limit Register

A7:A6h	TS Low Limit		
Bits	**Attr**	**Default**	**Description[a]**
15:13	RV	0	Reserved. Must be programmed as ‘0’ for future compatibility.
12	RW	0	Sign
11	RW	0	128
10	RW	0	64
9	RW	0	32
8	RW	0	16
7	RW	0	8
6	RW	0	4
5	RW	0	2
4	RW	0	1
3	RW	0	0.5
2	RW	0	0.25
1:0	RV	0	Reserved. Must be programmed as ‘0’ for future compatibility.

NOTES:
a. Temperature is in two’s complement format. See Temperature Sensor section for details.

Table 265 — TS Critical Temperature Register

A9:A8h	TS Critical Temperature		
Bits	**Attr**	**Default**	**Description**[a]
15:13	RV	0	Reserved. Must be programmed as ‘0’ for future compatibility.
12	RW	0	Sign
11	RW	0	128
10	RW	0	64
9	RW	0	32
8	RW	0	16
7	RW	0	8
6	RW	0	4
5	RW	0	2
4	RW	0	1
3	RW	0	0.5
2	RW	0	0.25
1:0	RV	0	Reserved. Must be programmed as ‘0’ for future compatibility.

NOTES:

a. Temperature is in two’s complement format. See Temperature Sensor section for details.

Table 266 — TS Current Ambient Temperature Register

AB:AAh	TS Current Ambient Temperature		
Bits	**Attr**	**Default**	**Description[a]**
15	RO		TCRIT - When set, the temperature is above the TCRIT Limit. This bit will remain set so long as the temperature is above TCRIT and will automatically clear once the temperature has dropped below the limit minus the hysteresis.
14	RO		HIGH - When set, the temperature is above the High Limit. This bit will remain set so long as the temperature is above the HIGH limit. Once set, it will only be cleared when the temperature drops below or equal to the HIGH Limit minus the hysteresis.
13	RO		LOW - When set, the temperature is below the Low Limit. This bit will remain set so long as the temperature is below the Low Limit minus the hysteresis. Once set, it will only be cleared when the temperature meets or exceeds the Low Limit.
12	RO		Sign
11	RO		128
10	RO		64
9	RO		32
8	RO		16
7	RO		8
6	RO		4
5	RO		2
4	RO		1
3	RO		0.5
2	RO		0.25*
1	RO		0.125*
0	RO		0.0625*

NOTES:

a. Temperature is in two’s complement format. See Temperature Sensor section for details.

* Resolution based on value of TRES field of the Capabilities Register.

Table 267 — MRS Control Register

ACh	MRS_CTRL		
Bits	**Attr**	**Default**	**Description**
7:6	RV	0	**MRS_CTRL7:6]:** Reserved
5:4	RW	0	**MRS_CTRL[5:4]:** MRS Broadcast Control 00: Per RCW F0RC14 - DRAM MRS Control 01: Reserved 10: All physical ranks at the same time (optional) 11: Reserved
3	RW	0	**MRS_CTRL[3]:** Host Bus Write Leveling Control 0: Never perform host bus write leveling based on MR1 decode 1: Decode MR1 from host, perform host bus write leveling (optional)
2:1	RW	0	**MRS_CTRL[2:1]:** Host MRS Snooping/Forwarding 00: Snoop host MRS, store & forward to DRAM bus 01: Snoop host MRS, store, do not forward to DRAM bus (optional) 10: Forward host MRS to DRAM but do not store 11: Block host MRS commands and do not store (optional)
0	RW	0	**MRS_CTRL[0]:** MRS Register Source 0: MRx_SNOOP + RxMR12 1: Reserved

For proper MB operation, host controller is responsible for configuring Rx_MR1,2 and MRx_Snoop registers as described in 6.4 and 6.5.

Table 268 — Rank 0 MR1,2 Register

B8h	R0_MR12		
Bits	**Attr**	**Default**	**Description**
7:6	RW	0	**R0_MR12[7:6]:** Rtt_WR 00: Dynamic ODT Off (Write does not affect Rtt value) 01: RZQ/4 10: RZQ/2 11: Reserved
5	RV	0	**R0_MR12[5]:** Reserved
4:2	RW	0	**R0_MR12[4:2]:** Rtt_Nom 000: Rtt_Nom disabled 001: RZQ/4 010: RZQ/2 011: RZQ/6 100: RZQ/12 101: RZQ/8 110: Reserved 111: Reserved
1:0	RW	0	**R0_MR12[1:0]:** Output Driver Impedance Control 00: RZQ/6 01: RZQ/7 10: RZQ/TBD 11: RZQ/TBD

Table 269 — Rank 1 MR1,2 Register

B9h	R1_MR12		
Bits	**Attr**	**Default**	**Description**
7:6	RW	0	**R1_MR12[7:6]:** Rtt_WR 00: Dynamic ODT Off (Write does not affect Rtt value) 01: RZQ/4 10: RZQ/2 11: Reserved
5	RV	0	**R1_MR12[5]:** Reserved
4:2	RW	0	**R1_MR12[4:2]:** Rtt_Nom 000: Rtt_Nom disabled 001: RZQ/4 010: RZQ/2 011: RZQ/6 100: RZQ/12 101: RZQ/8 110: Reserved 111: Reserved
1:0	RW	0	**R1_MR12[1:0]:** Output Driver Impedance Control 00: RZQ/6 01: RZQ/7 10: RZQ/TBD 11: RZQ/TBD

Table 270 — Rank 2 MR1,2 Register

BAh	R2_MR12		
Bits	**Attr**	**Default**	**Description**
7:6	RW	0	**R2_MR12[7:6]:** Rtt_WR 00: Dynamic ODT Off (Write does not affect Rtt value) 01: RZQ/4 10: RZQ/2 11: Reserved
5	RV	0	**R2_MR12[5]:** Reserved
4:2	RW	0	**R2_MR12[4:2]:** Rtt_Nom 000: Rtt_Nom disabled 001: RZQ/4 010: RZQ/2 011: RZQ/6 100: RZQ/12 101: RZQ/8 110: Reserved 111: Reserved
1:0	RW	0	**R2_MR12[1:0]:** Output Driver Impedance Control 00: RZQ/6 01: RZQ/7 10: RZQ/TBD 11: RZQ/TBD

Table 271 — Rank 3 MR1,2 Register

BBh	R3_MR12		
Bits	**Attr**	**Default**	**Description**
7:6	RW	0	**R3_MR12[7:6]:** Rtt_WR 00: Dynamic ODT Off (Write does not affect Rtt value) 01: RZQ/4 10: RZQ/2 11: Reserved
5	RV	0	**R3_MR12[5]:** Reserved
4:2	RW	0	**R3_MR12[4:2]:** Rtt_Nom 000: Rtt_Nom disabled 001: RZQ/4 010: RZQ/2 011: RZQ/6 100: RZQ/12 101: RZQ/8 110: Reserved 111: Reserved
1:0	RW	0	**R3_MR12[1:0]:** Output Driver Impedance Control 00: RZQ/6 01: RZQ/7 10: RZQ/TBD 11: RZQ/TBD

Table 272 — Rank 4 MR1,2 Register

BCh	R4_MR12		
Bits	**Attr**	**Default**	**Description**
7:6	RW	0	**R4_MR12[7:6]:** Rtt_WR 00: Dynamic ODT Off (Write does not affect Rtt value) 01: RZQ/4 10: RZQ/2 11: Reserved
5	RV	0	**R4_MR12[5]:** Reserved
4:2	RW	0	**R4_MR12[4:2]:** Rtt_Nom 000: Rtt_Nom disabled 001: RZQ/4 010: RZQ/2 011: RZQ/6 100: RZQ/12 101: RZQ/8 110: Reserved 111: Reserved
1:0	RW	0	**R4_MR12[1:0]:** Output Driver Impedance Control 00: RZQ/6 01: RZQ/7 10: RZQ/TBD 11: RZQ/TBD

Table 273 — Rank 5 MR1,2 Register

BDh	R5_MR12		
Bits	**Attr**	**Default**	**Description**
7:6	RW	0	**R5_MR12[7:6]:** Rtt_WR 00: Dynamic ODT Off (Write does not affect Rtt value) 01: RZQ/4 10: RZQ/2 11: Reserved
5	RV	0	**R5_MR12[5]:** Reserved
4:2	RW	0	**R5_MR12[4:2]:** Rtt_Nom 000: Rtt_Nom disabled 001: RZQ/4 010: RZQ/2 011: RZQ/6 100: RZQ/12 101: RZQ/8 110: Reserved 111: Reserved
1:0	RW	0	**R5_MR12[1:0]:** Output Driver Impedance Control 00: RZQ/6 01: RZQ/7 10: RZQ/TBD 11: RZQ/TBD

Table 274 — Rank 6 MR1,2 Register

BEh	R6_MR12		
Bits	**Attr**	**Default**	**Description**
7:6	RW	0	**R6_MR12[7:6]:** Rtt_WR 00: Dynamic ODT Off (Write does not affect Rtt value) 01: RZQ/4 10: RZQ/2 11: Reserved
5	RV	0	**R6_MR12[5]:** Reserved
4:2	RW	0	**R6_MR12[4:2]:** Rtt_Nom 000: Rtt_Nom disabled 001: RZQ/4 010: RZQ/2 011: RZQ/6 100: RZQ/12 101: RZQ/8 110: Reserved 111: Reserved
1:0	RW	0	**R6_MR12[1:0]:** Output Driver Impedance Control 00: RZQ/6 01: RZQ/7 10: RZQ/TBD 11: RZQ/TBD

Table 275 — Rank 7 MR1,2 Register

BFh	R7_MR12		
Bits	**Attr**	**Default**	**Description**
7:6	RW	0	**R7_MR12[7:6]:** Rtt_WR 00: Dynamic ODT Off (Write does not affect Rtt value) 01: RZQ/4 10: RZQ/2 11: Reserved
5	RV	0	**R7_MR12[5]:** Reserved
4:2	RW	0	**R7_MR12[4:2]:** Rtt_Nom 000: Rtt_Nom disabled 001: RZQ/4 010: RZQ/2 011: RZQ/6 100: RZQ/12 101: RZQ/8 110: Reserved 111: Reserved
1:0	RW	0	**R7_MR12[1:0]:** Output Driver Impedance Control 00: RZQ/6 01: RZQ/7 10: RZQ/TBD 11: RZQ/TBD

Table 276 — MR0 Snoop Register

C9:C8h	MR0_SNOOP (common to all Ranks)		
Bits	**Attr**	**Default**	**Description**
15:13	RW	0	**MR0_Snoop[15:13]:** A[15:13] Captured from host These bits have no function, but the MB captures what the host sent
12	RW	0	**MR0_Snoop[12]:** A[12] DLL Control for Precharge Power Down 0: Slow Exit (DLL Off) 1: Fast Exit (DLL On)
11:9	RW	0	**MR0_Snoop[11:9]:** A[11:9] Write Recovery for Auto Precharge 000: 16 cycles 001: 5 cycles 010: 6 cycles 011: 7 cycles 100: 8 cycles 101: 10 cycles 110: 12 cycles 111: 14 cycles
8	RW	0	**MR0_Snoop[8]** A[8] DLL Reset 0: No 1: Yes
7	RW	0	**MR0_Snoop[7]** A[7] Mode 0: Normal 1: Test
6:3	RW	0	**MR0_Snoop[6:3]:** A[6,5,4,2] CAS Latency 0000: Reserved 0010: 5 cycles 0100: 6 cycles 0110: 7 cycles 1000: 8 cycles 1010: 9 cycles 1100: 10 cycles 1110: 11 cycles 0001: 12 cycles 0011: 13 cycles 0101: 14 cycles 0111: Reserved for 15 cycles 1001: Reserved for 16 cycles 1011: Reserved 1101: Reserved 1111: Reserved
2	RW	0	**MR0_Snoop[2]:** A[3] Read Burst Type 0: Nibble sequential 1: Interleaved
1:0	RW	0	**MR0_Snoop[1:0]:** A[1:0] Burst Length 00: 8 (Fixed) 01: BC4 or 8 (on the fly) 10: BC4 (Fixed) 11: Reserved

Table 277 — MR1 Snoop Register

CB:CAh	MR1_SNOOP (common to all Ranks)		
Bits	**Attr**	**Default**	**Description**
15:13	RW	0	**MR1_Snoop[15:13]:** These bits have no function, but the MB captures what the host sent
12	RV	0	**MR1_Snoop[12]:** Reserved A[12] Qoff bit is captured per physical rank
11	RW	0	**MR1_Snoop[11]:** A[11] TDQS Enable 0: Disabled 1: Enabled
10	RW	0	**MR1_Snoop[10]** A[10] Captured from host This bit has no function, but the MB captures what the host sent
9	RV	0	**MR1_Snoop[9]** Reserved This bit is captured per physical rank
8	RW	0	**MR1_Snoop[8]** A[8] Captured from host This bit has no function, but the MB captures what the host sent
7	RV	0	**MR1_Snoop[7]** Reserved A[7] Write Leveling Enable bit is captured per physical rank
6	RV	0	**MR1_Snoop[6]** Reserved This bit is captured per physical rank
5	RV	0	**MR1_Snoop[5]** Reserved This bit is captured per physical rank
4:3	RW	0	**MR1_Snoop[4:3]:** A[4:3] Additive Latency 00: 0 (AL disabled) 01: CL-1 10: CL-2 11: Reserved
2	RV	0	**MR1_Snoop[2]** Reserved This bit is captured per physical rank
1	RV	0	**MR1_Snoop[1]** Reserved This bit is captured per physical rank
0	RW	0	**MR1_Snoop[0]:** A[0] DLL Enable 0: Enabled 1: Disabled

Table 278 — MR2 Snoop Register

CD:CCh	MR2_SNOOP (common to all Ranks)		
Bits	**Attr**	**Default**	**Description**
15:11	RW	0	**MR2_Snoop[15:11]:** These bits have no function, but the MB captures what the host sent
10:9	RV	0	**MR2_Snoop[10:9]:** Reserved A[10:9] Rtt_WRT bits are captured per physical rank
8	RW	0	**MR2_Snoop[8]** A[8] Captured from host This bit has no function, but the MB captures what the host sent
7	RW	0	**MR2_Snoop[7]** Self Refresh Temperature Range 0: Normal operating temp range 1: Extended operating temp range
6	RW	0	**MR2_Snoop[6]** Auto Self Refresh 0: Manual SR Reference (SRT) 1: Auto Self Refresh enabled (optional)
5:3	RW	0	**MR2_Snoop[5:3]:** A[5:3] CAS Write Latency 000: 5 cycles 001: 6 cycles 010: 7 cycles 011: 8 cycles 100: 9 cycles 101: 10 cycles 110: 11 cycles 111: 12 cycles
2:0	RW	0	**MR2_Snoop[2:0]:** A[2:0] Partial Array Self Refresh 000: Full Array 001: Half Array (BA[2:0] = 000, 001, 010, 011) 010: Quarter Array (BA[2:0] = 000, 001) 011:1/8th Array (BA[2:0] = 000) 100: 3/4 Array (BA[2:0] = 010, 0111, 100, 101, 110, 111) 101: Half Array (BA[2:0] = 100, 101, 110, 111) 110: Quarter Array (BA[2:0] = 110, 111) 111: 1/8th Array (BA[2:0] = 111)

Table 279 — MR3 Snoop Register

CF:CEh	MR3_SNOOP (common to all Ranks)		
Bits	**Attr**	**Default**	**Description**
15:3	RW	0	**MR3_Snoop[15:3]:** These bits have no function, but the MB captures what the host sent
2	RV	0	**MR3_Snoop[2]:** A[2] MPR 0: Normal Operation 1: Dataflow from MPR

Annex A (informative) Differences between Document Revisions

A.1 Initial Release JESD82-30

Table 1 — Changes from JESD82-30

Changes	Sections Affected	Description of Changes

Standard Improvement Form

JEDEC _____

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC
Attn: Publications Department
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

Fax: 703.907.7583

1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

Address: _____

City/State/Zip: _____ Date: _____

Rev. 8/13

JEDEC®