UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

Case No. IPR2022-00062
U.S. Patent No. 9,858,218

DECLARATION OF DR. FENG YANG

I, Feng Yang, make this declaration in connection with the proceeding identified above.

1. I have personal knowledge of the facts set forth herein, and if called to testify, I could and would competently testify to the same. In preparing this declaration, I also reviewed the declarations from Sung Joo Park, Julie Carlson, and John Halbert, along with their associated exhibits and deposition testimony.

2. I earned my Ph.D. in Computer Science from Syracuse University in 1993. I have over twenty years of first-hand experience in the area of memory and storage technologies and regularly consult for major manufacturers and designers in the memory industry. Throughout my career, I have provided analysis of competition and industry trends for the memory industry and conducted strategic planning for memory products. A copy of my CV is attached here as Exhibit A. I am being paid my standard rate of $350 per hour for my time in preparing this declaration.

3. I worked at Intel Corporation for over two decades between 1994 and 2015 and served as the Chief Platform Architect- Mobility & Communications Group between 2005 and 2015. While at Intel, I successfully delivered numerous leading computer products from architecture concept development through silicon products. As Chief Platform Architect, I led the development of products storage subsystem (including smartphone and tablet storage) and architected next-

generation mobile storage standard Universal Flash System (UFS) which positioned Intel as a leader in mobile storage technology.

4. Between 2015 and 2019, I worked as the Director of Technology Planning and Standards at Futurewei Technologies (Huawei USA). At Huawei USA, I was responsible for the development of memory technology roadmaps. I led memory standard development effort and successfully made some of the innovations from Huawei become a part of JEDEC memory standards.

5. My roles as the Chief Platform Architect and the Director of Technology Planning and Standards at Huawei USA provided me with insights in memory industry development trends and general knowledge in the implementation of memory technologies in various applications.

6. Since 2005, including during my time as the Chief Platform Architect at Intel, I have held multiple senior leadership roles in JEDEC. JEDEC establishes memory technology standards for computer industry, including LRDIMM. In addition to serving as a committee member at JEDEC for 14 years, I also served as Vice Chairman of JEDEC's Board of Directors and Chairman of the JC64/UFS HCI Task Group, all of which required nomination and election by the members. As vice chairman of JEDEC's Board, I was responsible for establishing charter and rules and procedures to run operations with JEDEC affiliations overseas. As a

member of the Board, I participated in ratifying each JEDEC standard and rules and procedures during that time period. As chairman of the Task Group, I chaired regular meetings to discuss technical details of the standards under development.

7. I understand that the JEDEC reference at issue in this case is a committee ballot that the JEDEC JC40.4 committee voted on in 2009, which has been identified as Exhibit 1015 (also Exhibit A to Ms. Carlson's declaration and Exhibit B to Mr. Park's declaration). As such, unless stated otherwise, my opinion below specifically addresses the May 2008 to May 2010 timeframe, during which I served as a committee representative at JEDEC.

8. To start, JEDEC membership is not (and never has been) available to individuals. I understand that Petitioner has submitted and Mr. Halbert testified regarding a "Wayback Machine" capture from the JEDEC website (www.jedec.org) as it existed on April 10, 2009, which has been labeled Exhibit 1073 in this case. Exhibit 1073 states that, in April 2009 (as is also the case in later years), "[m]embership in JEDEC [was] open to independent entities that manufacture semiconductor products, or provide related services or equipment. Membership [was] company based, not by individual." According to Exhibit 1073, in 2009 JEDEC membership cost $4000/year to join a single committee, $6500/year to join two committees, $9000/year to join three

committees, and $12,000/year to join four or more. This is consistent with my memory of the requirements and costs for JEDEC membership at this time.

9. In 2009, JEDEC meetings were closed to the public. JEDEC committee and subcommittee meetings are only open to members of the specific committee or subcommittee. The same restriction applied to access to documents or files related to a committee—access to a committee's files were limited to members of that committee. Standards developed by a committee are made public by JEDEC only after they have been approved by the full committee, ratified by the Board of Directors, and formally published by JEDEC. These policies and practices of course predated 2009, and continued after that time as well.

10. JEDEC technology proposals originated in JEDEC task groups within committees. Task groups were formed by members of a particular JEDEC committee or subcommittee for investigating and developing new technology proposals. Members of a task group could bring new technology proposals to that task group for consideration in the form of a presentation. After a presentation was made, a task group member could make a motion for a ballot calling for a majority vote by the task group members. If the vote passed, the proposal was elevated to the full committee as a committee ballot. Exhibit 1015 in this case is an example of one such committee ballot.

11. The mechanism by which the relevant committee members reviewed and voted on a JEDEC committee ballot, both in 2009 and after, was an internal JEDEC software program called the JEDEC "Voting Machine," hosted by JEDEC on JEDEC's private intranet servers. Access to JEDEC's private intranet and the JEDEC Voting Machine was limited to relevant committee members and required a JEDEC login and password. I had such access in 2009 and used the Voting Machine software to review and vote on committee ballots during that time.

12. When a committee ballot was prepared for a vote, it was placed on the internal JEDEC Voting Machine. A ballot posted on JEDEC's Voting Machine could only be accessed using JEDEC-issued credentials by JEDEC committee members designated to vote on the particular ballot (or members designated as alternates for voting), and by members of the related JEDEC committee as needed to solicit their comments. As such, committee ballots were not accessible by all JEDEC members, much less by members of the general public.

13. When a ballot became available for committee members to vote or comment on, the ballot was *not* distributed or sent to JEDEC committee members (by email, mail, or otherwise). Instead, as noted above, the committee ballot would be placed on JEDEC's internal Voting Machine. JEDEC would then send an email to a set mailing list of members of the relevant committee(s) indicating

that there was a committee ballot ready for vote. The email did not contain or attach the committee ballot and did not provide a description of the technology proposal. Instead, the email contained a URL link to access JEDEC's internal Voting Machine. Upon clicking on the link, a committee member would need to log into the JEDEC Voting Machine and could then navigate to the specific committee ballots to which they have access and on which they may vote.

14. Once logged into JEDEC's internal Voting Machine, a committee member would be able to access any notices for committee ballots to which they were allowed to vote. I have reviewed Exhibit 1051 (see also Exhibit B to Ms. Carlson's declaration and Exhibit A to Mr. Park's declaration), which is an example of one such notice. That is, Exhibit 1051 is a printout of an internal page on JEDEC's Voting Machine program that summarizes a specific committee ballot. JEDEC's Voting Machine logo appears at the top-right and bottom-center of the page reflecting that it is a printout from JEDEC's Voting Machine program.

15. In 2009, once a committee member navigated on JEDEC's Voting Machine to a ballot notice such as Exhibit 1051, the member could then click on a further link in the notice to review the committee ballot itself (that is, a document like Exhibit 1015). But, access to a notice like Exhibit 1051 or the ballot itself like Exhibit 1015 was still limited to members of respective underlying committees.

Members who can access the notice and ballot are identified in the notice (for example, see Exhibit 1051, referring to "Distribution" to members of JC-404 for voting and JC-40 for comment).

16. For this reason, even if a JEDEC committee member were to have forwarded an email received from JEDEC announcing that a ballot was available to a non-committee member or member of the public, the recipient of such email could not access or view the committee ballot at issue. Even if supplied with the link contained in the email announcing a ballot's availability, a person clicking on the link would still need log-in credentials for JEDEC, and specifically credentials tied to the particular relevant committee to which the ballot pertained. Ballot notices such as Exhibit 1051 or committee ballots like Exhibit 1015 were not themselves emailed or otherwise distributed to committee members.

17. Thus, when for example Ms. Carlson states in her declaration (paragraph 7) that such items are "distributed to the members" of related committees, I understand her to mean that such items were made available for member review on JEDEC's Voting Machine (as any other connotation would be factually inaccurate). Indeed, I understand that Ms. Carlson later clarified this in her deposition, stating that the "Voting Machine" is "[JEDEC's] system where members access ballots." 7/27/22 Carlson Depo. Tr. [Exbibit 2024] at 19:3-9.

Likewise, when Mr. Park states in his declaration that such materials were "received" or "distributed" (paragraphs 6-7), I understand him to refer to member access on JEDEC's Voting Machine (not to actually "receiving" or being "distributed" a copy such as by email or mail, etc.).

18. Committee ballots (like Exhibit 1015) and related notices (like Exhibit 1051) were therefore only accessible to be viewed via the internal JEDEC Voting Machine by related JEDEC committee members. Thus, according to the practice and procedure at JEDEC, when a ballot or notice is referred to as being "distributed" to committee members, the mechanism of "distribution" is JEDEC's posting of a ballot on its internal Voting Machine as described above (not actual physical or electronic distribution to members or otherwise).

19. If a committee ballot passed by a majority vote in the corresponding JEDEC committee, the proposal was then submitted to the JEDEC Board of Directors as a board ballot for further consideration and voting by the Board. The board ballot itself was provided to the Board via the JEDEC's internal Voting Machine software as described above. Only after a balloted proposal has been approved by the Board is it then approved for formal publication to the general public. The JEDEC office then publishes the final, approved standard, which then becomes available to the public on the JEDEC's website.

20. Both in the 2009-2010 timeframe and throughout my time at JEDEC, it was understood and the practice of JEDEC members that committee ballots were treated as confidential within the committee.[1] Of course, I and other JEDEC member representatives would discuss technology proposals or ballots internally and among committee members as necessary to determine how to vote or comment on proposals.[2] But it was understood that pending committee ballots could not be distributed *outside* of the relevant group of JEDEC members to other, non-JEDEC entities. This is further reflected by the fact that, as noted above, access to ballots was limited on JEDEC's Voting Machine platform, where only specific relevant committee members (not all members) could access a related committee ballot.

21. In my entire experience, including my many years at Intel where I worked with Mr. Halbert, I have never heard of any JEDEC committee ballot being distributed or sent to a non-JEDEC member (that is, to a third party) prior to any standard being formally adopted. This would have been improper, and I see in

[1] In this regard, I disagree with Mr. Halbert to the extent he states that there was no confidentiality obligation in place or observed concerning JEDEC balloting. This material was *always* treated as confidential, including within Intel (a JEDEC member) where Mr. Halbert and I both worked at the time.

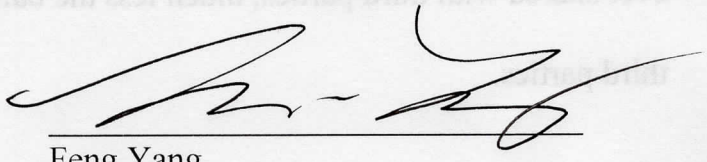
[2] When Mr. Halbert states in his declaration that ballots were "freely" discussed "*within* JEDEC's committees and subcommittees" (paragraph 11, emphasis added), this is what I understand him to be referring to—that, as noted above, there was discussion internally and *within* the relevant committee members.

Mr. Halpert's deposition that he agrees with me on this point. 7/22/22 Halbert Depo. Tr. [Exhibit 2022] at 23:14–17. When Mr. Halbert states in his declaration (paragraph 11) that ballots were discussed "among all third-parties," I do not understand him to be saying that the ballots themselves were circulated to third-parties (versus technical issues related to such being discussed). And Mr. Halbert clarified in his deposition that his understanding matches mine that ballots were *not* distributed to third parties. Exhibit 2022 at 23:14–17. Regardless, as I note above, I am not aware of any instance when the content of JEDEC ballots were ever shared with third parties, much less the ballots themselves being distributed to third parties.

* * * * *

I, Feng Yang, declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. I hereby also declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that willful false statements and the like so made could jeopardize the validity of the patent at issue in this proceeding.

Executed on 08/14, 2022



Feng Yang

FRANK YANG

DIRECTOR/PRINCIPAL PLATFORM ARCHITECT

Technical Professional with 20+ years of hardware/software experience with leading companies including Intel and Huawei. Leverage strong background in platform architecture, including industry-recognized expertise in computing technologies. Proven track record of driving end-to-end SoC/platform development initiatives in support of key products as leader. Well connected with leading industry and academia leaders and insightful of the latest technology trends.

Key Strengths & Areas of Expertise

Platform Architecture: Hardware Accelerator architecture for Artificial Intelligence. AR/VR, Platform Power and Thermal management, Memory and Storage, Security, Audio, Manageability, Windows/Android/Linux Software Architecture ▪ SoC Architecture ▪

PROFESSIONAL EXPERIENCE

A&B Computing Technology Consulting Services | Portland, OR 2020-present
Chief Consultant

- Provided consulting services for major investment firms in USA and Asia. The service includes evaluation of the core technologies from the investment targets.
- Provided consulting services for a major computer memory company. The service provides the competition landscape analysis, industrial trends in computer memory technologies and a strategic plan for their products.
- As a technology advisor, provided evaluation of architecture design for two startup companies. One focus on development of Artificial Intelligence technologies; the other focus on AR/VR technologies.

FUTUREWEI TECHNOLOGIES (Huawei USA) | Bellevue, WA 2015-2019
Director of Technology Planning and Standards

- Represented Huawei in memory industry standard organization (JEDEC). Drove development of key technologies in memory subsystem and made them a part of JEDEC memory standards including NVDIMM-P, HBM, and next generation DDR5.
- Led architectural development of energy efficient hardware accelerators for Artificial Intelligence. The work will power Huawei next generation products including smartphone, cloud applications and telecommunications.
- Led strategic planning teams to develop technology roadmaps on memory/storage subsystem for Huawei product lines including mobile and enterprise products.
- Led architectural development of next-generation memory/storage subsystem based on Storage Class Memory (SCM). The technology will enable Huawei to establish its leadership position in next generation memory/storage technology.

INTEL CORPORATION | Hillsboro, OR 1994-2015
Chief Platform Architect – Mobility & Communications Group (2005-2015)

FRANK YANG

- Headed several generations of product development for smartphone and tablet storage subsystem, providing robust architecture design enabling easy implementation of new features.
- Oversaw all phases of silicon SoC development, created design specifications, and facilitated design review and ratification through production releases.
- Led strategic planning and marketing teams to create product/technology roadmap and technical requirements for Intel mobile platforms.
- Architected next-generation mobile storage standard Universal Flash System (UFS) that will position Intel as a leader in mobile storage technology.

Senior Staff Platform Architect – Mobile Platform Group (2001-2005)

- Co-inventor of power and thermal management technology on Intel mobile platforms, resulting in adoption of the technology and its extension for all Intel mobile platforms for the past 15 years. The technology enables Intel to deploy x86 architecture to smartphone and tablet and be competitive with other competitions in smartphone and tablet. The technology is also adopted by major OS vendors in kernels.
- Responsible for development of mobile-specific features of Intel HD Audio specification and led implementation on Intel Mobile Platforms; the technology has also shipped with all x86-based PCs.

Engineering Manager – Intel Internet Media Services (2000-2001)

- Led a large engineering team through development of key technology for Media Distribution Services, including application-level routing and application-level multicast.

Engineering Manager – LAN Access Division (1998-2000)

- Directed 30+ person software engineering team through development of advanced networking technology such as VLAN and teaming, silicon diagnostic, and validation tools. Delivered them to multiple generations of Intel Ethernet product lines.

Staff Architect – Server Software Technology (1997-1998)

- Built e-commerce roadmap for Internet Marketing Group of Enterprise Server Group (ESG):
- Executed ESG security initiatives and delivered security solutions for server management product group:
  - Held key role in developing and supporting Intel server security plan.
  - Crafted long-term ESG security strategy and structured security roadmaps for ESG products.
- Led development of secured server management in pre-OS environment for Intel server platforms.

Staff Software Engineer – Intel Architecture Labs (1996-1997)

- Led development of security architecture for managing within distributed computing environment as part of Intel Wired for Management (WfM) initiative; drove architecture design and specification.
- Spearheaded development of Pro-Boot Integrity Services as reference implementation for WfM.
- Held role in development of WfM 2.0 specification, an industry standard.

Senior Software Engineer – Internet Product Division (1995-1996)

- Steered internet software initiative, including development of internet real-time multimedia streaming capability and web usage tracking/reporting.

FRANK YANG

- Drove design of generic architecture for software installation and update of division's products as team lead/architect for Software Installation/Upgrade Group.

Senior Software Engineer – ProShare Video Conferencing Product Division (1994-1995)
- Key contributor to the design and implementation of an online meeting application to enable user to easily draw sketches, collaborate and share with others.

INDUSTRY STANDARD EXPERIENCE

Vice-Chairman – JEDEC Board of Directors

Chairman – JEDEC JC64/TG641_4 UFS HCI Task Group (TG)
- Chair all working meetings for the Task Group. Led the Task Group to establish standards for UFS Host Controller Interface.
- Author of JEDEC UFS and UFS HCI specifications (from version 1.0 – version 3.0).

Intel chief representative – SD Association.
- Represent Intel and drove key Intel-favored initiatives into various SD standards.

Huawei chief representative /Key contributor – NVM Express.
- Main representative of Huawei in NVM Express standard body and led development of NVM Express standards within Huawei.

Intel chief representative /Key contributor – MIPI UniPro Working Group.

Chairman – MIPI NAND Software Working Group

EDUCATION

PhD in Computer Science
Syracuse University, 1993

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