

Minutes of Meeting No. 160
JC-40 Digital Logic Committee

December 10, 2009

Maui, Hawaii

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1.0 JC-40 Digital Logic Plenary

The JC-40 Plenary meeting opened at 8:00 AM on December 10, 2009.
Mr. Smolka led the discussion of this group.

Self-introductions were completed by the attendees.

1.1.0 Patent Policy

The patent policy was reviewed.

1.2.0 Minutes

The minutes of the September 2009 meeting were reviewed and approved as written with a motion by Samsung and seconded by Montage.
The motion passed by acclamation.

1.3.0 Elections

Mr. Quddus reviewed the nominations compiled by the Nominating Committee, with that information also posted on the wireless server. The nominations were:

JC-40:

JC-40 Chairman: John Smolka (incumbent)

JC-40 Vice-Chairman: Joe Quddus (Montage)

Nominations were then closed after no additional nominations were received from the floor.

Mr. Smolka and Mr. J. Quddus were elected to their respective positions by acclamation.

JC-40.1:

JC-40.1 Chairman: Rick Williams (incumbent)

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Nominations were then closed after no additional nominations were received from the floor.

Mr. Williams was elected by acclamation.

JC-40.3:

JC-40.3 Chairman:

- Ramzi Ammar (incumbent)
- Ingolf Frank (TI)

Nominations were then closed after no additional nominations were received from the floor.

Each nominee provided a brief background and ideas regarding the committee future direction. A secret ballot process was then completed, with one vote permitted for each member company. Mr. Kellogg completed the validation and counting of the ballots.

Upon completion of the secret ballot process, Mr. Ammar was announced as the JC-40.3 Chairman.

JC-40.4:

JC-40.4 Chairman:

- Jeffrey Chung (Silego)
- Chris Haywood (Inphi)
- Christian Harrieder (TI)

Each nominee provided a brief background and ideas regarding the committee future direction. A secret ballot process was then completed, with one vote permitted for each member company. The committee was informed that >50% of the votes would be required for one candidate to prevent a runoff election. Mr. Kellogg completed the validation and counting of the ballots.

Upon completion of the secret ballot process, Mr. Kellogg announced that a runoff election would be required between Mr. Chung and Mr. Haywood.

Upon completion of the second secret ballot process, Mr. Chung was announced as the JC-40.4 Chairman.

JC-40.5:

JC-40.5 Chairman: Perry Keller (incumbent)

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Nominations were then closed after no additional nominations were received from the floor.

Mr. Keller was elected by acclamation.

1.4.0 Agenda

The agenda was reviewed.

1.5.0 BoD Ballot Review

- JCB-09-82, committee item #150.00, passed BoD voting. The material is to be published in JM21.

1.6.0 Ballot Review

There were no ballots for review in this committee.

2.0 JC-40.1 CMOS/BiCMOS Digital Logic

The JC-40.1 meeting opened at 8:16 on December 9, 2009. Mr. Williams led the discussion of this group.

2.1.0 Agenda

The agenda was reviewed.

2.2.0 Ballot Review

There were no ballots for review in this sub-committee.

2.3.0 Second Presentations

2.3.1.0 #121.02 TG

**JEDEC Instrumentation Chip
Status**

Mr. Williams provided a background, followed by the meeting days and times, companies attending, etc. A status update was reviewed – work

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efforts were reported as moving slowly due to resource re-focusing. The TG found some concerns in the IChip specification, with the intent to clean-up these items in the next quarter.

A TG authorization to ballot the material was received in 45.4 – a JC-40.1 authorization was also planned.

Motion by Sun and seconded Montage to authorize the TG to issue a ballot for modifications to the Instrumentation Chip specification.

Discussion:

- Is activity going to be started for the LRDIMM? Response: Current plans are to focus on DDR4.

The motion passed by acclamation.

2.4.0 First Presentations

There were no first presentations in this sub-committee.

3.0 JC-40.3 RDIMM Support Devices

The JC-40.3 meeting opened at 8:29 on December 10, 2009. Mr. Ammar led the discussion of this group.

3.1.0 Agenda

The agenda was reviewed and updated.

3.2.0 Ballot Review

3.2.1.0 #104.75 JC-40.3-09-282 DDR3 Register (SSTE32882) – DDR3 1866 Specification

The vote count was 15 yes, 0 no and 5 abstentions.

The ballot passed by acclamation and was left on pass/hold.

3.3.0 Second Presentations

3.3.1.0 #104.76 Intel

DDR3 SSTE32882 AC Overshoot/ Undershoot

Intel indicated that the material was not changed since the first showing, and that the TG had reached a consensus on the material.

Motion by Intel and seconded by Silego to authorize the TG to issue a ballot on the material.

The motion passed by acclamation.

3.3.2.0 #104.72 Silego #104.73

DDR3 3T and $\frac{3}{4}$ Pre-launch Mode

Background information was shown, with direction given at the September meeting to make the proposed features as "optional". The proposed modifications are intended to apply to both the DDR3 and DDR3L (SSTE32882) specifications.

The current RCW table (Table 21, RC2) was shown, followed by the proposed RCW table - showing the changes in red (optional).

Discussion:

- These features are not currently used, so can be considered optional.
- Discussion ensued as to whether the proposal would affect the SPD – the committee decided that it appeared as though the SPD would not be affected as the bytes are optional in the SPD.

The presentation continued:

A proposed modification to the AC table was shown, which comprised a sentence addition to note 4.related to $\frac{3}{4}$ prelaunch.

Motion by Silego and seconded by TI to authorize the TG to issue one or more ballots on the DDR3 SSTE32882 3T & $\frac{3}{4}$ pre-launch mode, item #'s 104.72 and 104.73.

The motion passed by acclamation.

3.3.3.0 #153.01 Silego

**DDR3U SSTE32882 RCD
Specification Proposal (1.25V
Support)**

The showing was based on a proposed SSTE32882 specification for 1.25V applications. The specification was loaded on the server, with changes to the existing specification, to support the proposed 1.25V application, shown in red.

The material was quickly shown to the committee.

Motion by Silego and seconded by AMD to authorize the TG to issue a ballot on the material.

Discussion:

- There was no authorization in JC-42.3 – if no memory device specification exists, is it appropriate to ballot this device at this time?

The motion was withdrawn.

3.4.0 First Presentations

3.4.1.0 #104.78 Micron

**CKE Power-Down Wording
Change**

Micron suggested that the existing SSTE32882 specification wording is not clear for CKE power-down. The current wording was shown, followed by the proposed wording (both as the bottom text on page 2, as well as in red on page 3).

Micron indicated that the TG had agreed on the proposed wording.

Motion by Silego and seconded by TI to adopt the proposed wording shown in the presentation as an editorial change to the wording in the existing SSTE32882 specification.

Discussion:

- Some concerns were raised in regard to the proposed wording.

Response: The objective is to appropriately correct the existing text so all ambiguity is removed.

An amendment was proposed by Silego, and accepted by TI, to authorize

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the TG to make the proposed changes as editorial changes to the specification if 100% consensus is achieved on the wording change. If 100% consensus is not achieved, the TG would be authorized to issue a ballot on the proposed wording modifications.
The amended motion passed by acclamation.

3.4.2.0 #104.77 Intel

**DDR3 SSTE32882 RC11 VREFCA
Proposal**

Intel indicated that the DDR3 register has a VREFCA input – it was originally expected that registers would use this as a reference to the buffer. Intel proposed that the external VREF be the default (mandatory at 1866 and higher applications), with the internal VREF being available if some wish to use it.

Motion by Intel and seconded by Silego to elevate the material to be considered as a second showing.
The motion passed by acclamation.

Motion by Intel and seconded by Silego to authorize the TG to issue one or more ballots on the material.
The motion passed by acclamation.

3.5.0 Task Group Update

3.5.1.0 122.00 TG

DDR PLL/Reg TG Update

The TG logistics were shown, including the website information, call details, scope and chairman information. TG activities since the September meeting were summarized, with several of the items covered in the current meeting. DDR3 consensus votes were summarized, including the CKE power-down clarification, keeping manual 3T mode optional and keeping manual $\frac{3}{4}$ pre-launch mode optional.

The TG chairman then indicated that there was an error in ballot #09-282 (item #104.75), counted earlier in the meeting. The ballot material was then re-opened for review. On page 9 of the ballot material, the maximum frequency limit should be 945 MHz and not 933 MHz. It was shown that the frequency table on page 5 of the ballot was correct (945 MHz).

Motion by Silego and seconded by LSI to make the proposed change from 933 to 945 MHz on page 9 of the material in ballot #09-282 (item #104.75) as an editorial change, and to include this editorial change in the ballot material currently on pass/hold.

The motion passed by acclamation.

The TG report continued with a review of planned future discussions, including the DDR3-2133 specification, JESD65 document update and DDR4 activities.

Motion Silego and seconded by FormFactor to authorize the DDR3 TG to issue a committee ballot on the DDR3 SSTE32882 Register Specification, including all specification updates, editorial changes and passed committee ballots.

The motion passed by acclamation.

4.0 JC-40.4 FBDIMM Support Devices

The JC-40.4 meeting opened at 9:23 AM on December 10, 2009. Mr. Chung led the discussion of this group.

4.1.0 Agenda

The agenda was reviewed and updated.

4.2.0 Ballot Review

4.2.1.0 #142.12 JC-40.4-09-255 Transparent Mode Functionality

The vote count was 11 yes, 0 no and 8 abstentions.

Patent disclosure:

- Netlist: Netlist indicated that their disclosure includes prior disclosures in the tracking list and recent IP (patent) awards. Mr. Martinez indicated that they will follow-up with the JEDEC office.

Yes comments:

- Micron: There is nothing in the ballot indicating that it applies to the memory buffer.

The ballot material was left on pass/hold.

Patent disclosure:

- Google indicated that they may have IP associated with any LRDIMM buffer specification(s), and will follow-up with the JEDEC office.

4.2.2.0 #142.51 JC-40.4-09-297 Transparent Mode CA Timing

The vote count was 14 yes, 0 no and 6 abstentions.

Patent Disclosure:

- Netlist: Same as #09-255. Mr. Kellogg read-back the earlier text, which was accepted by Mr. Martinez.

The ballot was left on pass/hold.

4.2.3.0 #142.54 JC-40.4-09-299 LRDIMM DDR3 Memory Buffer Pin Description Proposal

The vote count was 18 yes, 0 no and 3 abstentions.

Patent disclosure:

- Netlist: Same as #09-255.

Yes comments:

- AMD: The TG has agreed to remove the QAECC[9,6,2] pins – which should therefore be removed from ballot. Response: Agreed.
- Elpida: An editorial change was proposed. Response: Agreed.
- FormFactor: ERROUT_n should include a statement that it is open drain, and requires a pull-up. Response: Accepted.
- Inphi: Clarification on voting material.
- IDT: An editorial change was proposed. Response: Agreed.

Motion by Inphi and seconded by IDT to adopt the AMD, Elpida (change to RFU), FormFactor and IDT comments as editorial changes to the ballot material, and to leave the editorially updated material on pass/hold.

The motion passed by acclamation.

4.2.4.0 #142.53 JC-40.4-09-300 LR-DIMM DDR3 Memory Buffer Ballout Proposal

The vote count was 14 yes, 0 no and 6 abstentions.

Patent disclosure:

- Netlist: Same as #09-255.

Yes comments:

- Elpida: Same as #09-299. Response: Accepted.
- IDT: Same as #09-299. Response: Accepted.

Motion by Silego and seconded by IDT to change QAECC pins to RFU, as editorial changes, and to place the editorially modified ballot material on pass/hold.

The motion passed by acclamation.

**4.2.5.0 #142.46 JC-40.4-09-316 LR-DIMM DDR3 Memory Buffer
Host Interface Protocol and
Requirements**

The vote count was 15 yes, 0 no and 5 abstentions.

Patent disclosure:

- Netlist: Same as #09-255.

Yes comments:

- AMD: AMD indicated that the first item in their response was in error and should be disregarded. Add a statement indicating that the buffer does not permit putting half of the ranks in self refresh mode while the other half of the ranks on the DIMM are in power-down mode, in an effort to reduce the test/validation combinations. Response: This is not clearly an editorial change – prefer to have TG review this item.
- Inphi: Clarification on voting material.
- Texas Instruments: TI proposed editorial changes on pages 7 and 15.

Motion by Silego and seconded by (no second) to authorize the TG to issue one or more ballots to address the AMD comment and to place the editorially updated material, including the TI comment, on pass/hold.

The motion was withdrawn.

Motion by Silego and seconded by AMD to authorize the TG to issue one or more ballots to address the AMD comment.

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changes in TG and re-ballot the material.

- Elpida: Proposed several changes to the material.
- Inphi: Similar to several AMD comments.
- Intel: Remove DDR3U references, etc.
- Texas Instruments: Several changes to the ballot material were listed.

Additional comment:

- FormFactor: Definition of minus-active signaling.

Motion by AMD and seconded by IDT to adopt the approved editorial changes to the ballot material and to re-authorize the TG to issue a ballot on the material.

Discussion:

- Unwilling to adopt the proposed changes as being editorial changes.

The motion failed as at least one company did not approve the editorial changes.

Motion by AMD and seconded by (no second) to accept the following changes as editorial changes to the ballot material:

- AMD indicated that they have received comments that they would like to include in the ballot as editorial changes – however, these proposed changes were not shown to the committee.

Discussion:

What did AMD receive as editorial changes? Response: No response.

The motion was dropped due to the lack of a second for the motion.

Later in the meeting, the following motion was recorded:

Motion by AMD and seconded by Inphi to authorize the TG to issue one or more ballots to address the comments in the original ballot material for committee ballot #09-318.

Discussion:

- Is the ballot intended to cover only the comments? Response: The ballot is intended to cover just the comments.

The motion passed by acclamation.

**4.2.8.0 #142.09 JC-40.4-09-319 LR-DIMM DDR3 Memory Power
Management Chapter Proposal**

The vote count was 15 yes, 0 no and 6 abstentions.

Patent disclosure:

- Netlist: Same as #09-255.

Yes comments:

- AMD: Same as ballot #09-316. Response: Same as #09-316.

- Inphi: Same as AMD comment.

- Intel: Intel proposed corrections for locations in specification having incorrect minus active labeling. Response: Accepted.

Motion by Intel and seconded by Silego to adopt the Intel modifications to the ballot material as editorial changes and to place the editorially updated material on pass/hold.

The motion passed by acclamation.

**4.2.9.0 #142.35 JC-40.4-09-320 LR-DIMM DDR3 Memory
Initialization Chapter Proposal**

The vote count was 15 yes, 0 no and 5 abstentions.

Patent disclosure:

- Netlist: Same as #09-255.

Yes comments:

- Intel: Same as ballot #09-319. Response: Accepted.

Motion by Intel and seconded by Silego to adopt the Intel modifications to the ballot material as editorial changes and to place the editorially updated material on pass/hold.

The motion passed by acclamation.

4.3.0 Second Presentations

4.3.1.0 #142.57 TI MB MEMBIST Register Map

TI presented the MB MEMBIST register map.

Motion by TI and seconded by IDT to authorize the TG to issue one ballot on the MB MEMBIST register map.
The motion passed by acclamation.

4.3.2.0 142.56 Elpida MB Vref

Elpida showed two cases where QVrefDQ is sourced from the same Vref generator or a different Vref generator than the Vref for MDQ. They asked for committee input as to which is the default setting of Vref for MDQ to MB.

Discussion:

- Several companies agreed to case #2.
- No need for the option 2? (no control word needed)

Motion by IDT and seconded Montage to adopt case #2 for the default setting for Vref for the memory buffer, with no control word needed for this feature.

The motion passed by acclamation.

4.4.0 First Presentations

4.4.1.0 #152.02 IBM DDR4 on DIMM VPP & VTT Generation

IBM repeated the showing made in JC-45. A regulator was proposed on the DIMM for VPP and VTT generation. IBM indicated that the proposal was being considered by the DDR4 DIMM Physical TG in JC-45. The showing to JC-40 was identified as being informational at this time.

4.4.2.0 #142.00 Intel LRDIMM MB Specification Body

Intel indicated that the material shown included a compilation of the pass/hold ballots in one document, using a standard template. Ongoing efforts will add additional passed ballots as they are available.

4.5.0 Task Group Update

Prior to the LRDIMM MB TG presentation (#142.10), Intel made the following presentation on the LRDIMM MB Specification:

4.5.1.0 #142.01 Intel

**LR-DIMM Memory Buffer Spec
Outline Proposal**

Intel made a presentation, from the September meeting, including a timeline for expected LRDIMM adoption, demonstrating the need for an LRDIMM memory buffer specification in early 2010. Item #142.00 (LRDIMM MB Specification Body) was prepared to facilitate the specification development.

Intel indicated that ballot authorization is needed for the MB specification introduction chapter (have item #), the electrical/ac timing specification chapter (have item #), Membist chapter (have item #, LAI mode chapter, configuration and status register chapter, SMBus chapter, and the reset chapter.

Motion by Intel and seconded by Montage to authorize the TG to issue one or more ballots on the MB specification chapters 1, 7, 10, 12, 13, 14, 15 (chapters defined in current showing for item #142.01).
The motion passed by acclamation.

4.5.2.0 #142.10 TG

DDR3 MB TG Report

The TG logistics were shown, including the chairmen, website information and TG call schedule. Ballots prepared and counted in the current quarter were listed, followed by the TG consensus list.

A request has been made for a time change for the TG calls. The chairman indicated that some world region is always negatively impacted by the time of the call, as the TG consistently has international participation. A matrix of possible conference call times were shown, with suggested timeslots in red.

Discussion:

- Of the possible options, the Asian TG members indicated that an early morning timeslot is better.

Discussion:

- Use rotating timeslot as it spreads the impact.
- JC-64.8 dropped rotating calls due to confusion and reduced participation.

Motion by Silego and seconded by Montage to move the TG calls to 2PM DST Pacific (stay at PST time).

Discussion:

- Asia: Prefer no earlier than 7 AM, Asian time.

The motion was amended to stay at 2 PM non-DST, 3 PM DST, with both the original first and second to the motion approving the change.

Discussion:

- An observation was made that there is a conflict at 3 PM (Pacific) start time in DST due to another TG meeting.

The motion was amended to remain at 2 PM PST, with a 1 hour duration. The amendment to the previously amended motion was accepted by the first and second to the original motion. The amended motion passed by acclamation.

The presentation continued:

The consensus list was reviewed and the IP disclosure list was shown. The recent IP disclosures will be added to the list. Google and Netlist were asked to send letters to the JEDEC office, if they have not already done so.

5.0 JC-40.5 Logic Verification and Validation

The JC-40.5 meeting opened at 11:10 AM on December 10, 2009. Mr. Keller led the discussion of this group.

5.1.0 Agenda

The agenda was reviewed and updated.

5.2.0 Ballot Review

5.2.1.0 #155.00 JC-40.5-09-257 LR-DIMM Buffer Validation Requirements Survey Ballot

The survey ballot was issued in an effort to compile a consensus from the committee regarding buffer validation.

A summary table of the survey results was shown. The breakout of vendors and users included some double counting, as several companies fit both cases. Items in green are intended to show an apparent consensus.

The results were then reviewed, by question, in greater detail. Members

can review the material in greater detail on the server.

5.3.0 Second Presentations

There were no second presentations for this sub-committee.

5.4.0 First Presentations

5.4.1.0 #133.07 Silego tPDM Measurement Procedure

Silego proposed a test procedure for tPDM, using the JEDEC plug-in card used for register component validation. The set-up procedure and measurement procedure was shown, followed by measurement examples. The test points were also shown. Follow-up items include whether 20K or 200K cycles should be measured to ensure a valid sample time. A >33uS capture was currently recommended.

Motion by Silego and seconded by Agilent to elevate the material to be considered as a second showing.
The motion passed by acclamation.

Motion by Silego and seconded by FormFactor to authorize the TG to issue one or more ballots on the tPDM measurement procedure.
The motion passed by acclamation.

5.4.2.0 #133.08 Agilent tSU & tH Measurement

The tSU and tH specifications were shown, describing the specified measurement points. The proposed measurement set-up was then shown, followed by an example sweep of tSU through the tSU range to determine the failing point.

The TG needs to discuss control register settings (if necessary), probe points on register/PLL test DIMM, A/C jitter characteristics and conditions for inputs not being tested – in addition to preparing a ballot, etc.

Motion by Agilent and seconded by Silego to elevate the material to be considered as a second showing.
The motion passed by acclamation.

Motion by Agilent and seconded by Silego to authorize the TG to issue one or more ballots on set-up/hold measurements.
The motion passed by acclamation.

5.4.3.0 #149.05 Agilent

LRDIMM Test Fixture Update

The parametric fixture goals were reviewed, including a low noise environment, access to all LRDIMM pins and functions, daughter card support for post-buffer/register signals, test pads, on-fixture coupons for impedance calibration, etc.

To achieve the stated purpose of providing a test fixture for LRDIMM characterization, five items were identified as being required: experimental layout board, calibration DIMM, LRDIMM test fixture, common control processor and common user interface software.

An overview of the DIMM parametric test fixture was reviewed. The “DOE” test board design, schematics, cross-section and other information was shown and connector tradeoffs were reviewed. Agilent indicated that the DOE board has been taped-out and calibration DIMMs are ready for tape-out pending a ground-relief decision in JC-45.4. Agilent further indicated that they are not doing the DOE board – it is being done by a 3rd party with the intent that it will be available to others.

Some basic work has been done on the software interface – with the intent that the software all be open-source to permit modifications as-needed.

5.5.0 Task Group Update

5.5.1.0 #149.04 Inphi

LRDIMM Validation TG Report

The TG’s mission was shown, followed by the TG logistics, consensus list (unchanged) and the recent survey ballot they issued (reviewed this meeting).

Remaining work in the TG is to digest the survey results, begin to develop functional and parametric requirements for platforms, develop testing procedures for key parameters, etc.

5.5.2.0 #133.00 TG

DDR3 Register/PLL Validation

The meeting logistics were reviewed – the TG is generally meeting every

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week. The TG includes approximately 34 member companies, with 6-12 people on each call. Showings and discussions are primarily related to tIS, tIH, tPDM and 1867/2133 support. Remaining TG work includes tracking register and PLL speed increases, completing work on current topics and making validation determinations for remaining parameters. The consensus list was shown but was unchanged.

6.0 Other Committee Business

Mr. Smolka requested input regarding other committee business:

6.1.0 Future Meetings

Mr. Rhoden indicated that the agenda included an error regarding the September, 2010 meeting – which is in Denver, not Chicago.

Mr. Kellogg provided information regarding the Taipei meeting (March, 2010). A dinner will also be held during that meeting week, sponsored by TSIA. More information will be provided to members as the meeting approaches.

6.2.0 Additional JC-40 Elections

Mr. Smolka indicated that JC-40.3 and JC-40.4 are busy - vice-chairmen may be needed to help manage the workload in these sub-committees. With the support of the committee and current chairmen, nominations were requested for the new vice-chairmen:

JC-40.3 Nominations:

- JC-40.3 Vice-Chairman: Ingolf Frank (TI)

Nominations were closed after no additional nominations were received from the floor.

Mr. Frank was elected by acclamation.

JC-40.4 Nominations:

- JC-40.4 Vice-Chairman: Christian Harrieder (TI)

Nominations were closed after no additional nominations were received from the floor.

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Mr. Harrieder was elected by acclamation.

7.0 Adjournment

Motion by Agilent and seconded by Montage to adjourn the meeting.
The motion passed by acclamation.

The meeting adjourned at 12:03 PM on December 10, 2009

**THIS MEETING WAS CONDUCTED IN ACCORDANCE WITH JEDEC
LEGAL GUIDES, JM5, AND THE JEDEC MANUAL OF ORGANIZATION
AND PROCEDURE, JM21-N.**

REVIEWED/CORRECTED AND AUTHORIZED FOR RELEASE BY:

Approved on: January 4, 2010
JC-40 Chairman, John Smolka

The following individuals did review/approve the minutes:

Approved on: January 1, 2010
JC-40.1 Sub-Committee Chairman, Rick Williams

Approved on: January 4, 2010
JC-40.3 Sub-Committee Chairman, Ramzi Ammar

Approved on: January 6, 2010
JC-40.4 Sub-Committee Chairman, Jeffrey Chung

Approved on: January 2, 2010
JC-40.5 Sub-Committee Chairman, Perry Keller

Approved on: December 29, 2009
Legal Approval, John Kelly

Approved on: December 29, 2009
Secretary, Mark Kellogg