UTILITY PATENT APPLICATION TRANSMITTAL Only for new nonprovisional applications under 37 CFR § 1.53(b))	Attorney Docket No.	NL066-13US02
	First Inventor	Hyun LEE
	Title	*MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION*
	Electronically filed	June 14, 2022

APPLICATION ELEMENTS
See MPEP Chapter 600 concerning utility patent application contents.

Address to: **Commissioner for Patents**
P.O. Box 1450
Alexandria, VA 22313-1450

1. ☐ Fee Transmittal Form (with duplicate for fee processing)
2. ☐ Applicant claims Small Entity status, see 37 C.F.R. § 1.27
3. ☐ Applicant certifies Micro Entity status, see 37 C.F.R. § 1.29
4. ☒ Specification [Total Pages 21]
5. ☒ Drawing(s) (35 USC § 113) [Total Sheets 3]
6. ☒ Oath and Declaration [Total Pages 2]
   a. ☐ Newly executed (original or copy)
   b. ☒ Copy from a prior application (37 CFR § 1.63(d))
7. ☒ Application Data Sheet, see 37 C.F.R. § 1.76
8. ☐ CD-Rom or CD-R in duplicate, large table or Computer Program (Appendix)
   ☐ Landscape Table on CD
9. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   a. ☐ Computer Readable Form (CRF)
   b. ☐ Specification Sequence Listing on
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

10. ☐ Assignment Papers (cover sheet & document(s))
    Name of Assignee: Netlist, Inc.
11. ☐ 37 CFR § 3.73(c) Statement
    ☐ Power of Attorney
12. ☐ English Translation Document (if applicable)
13. ☐ Information Disclosure Statement and PTO-1449
    ☐ Copies of citations attached
14. ☐ Preliminary Amendment
15. ☐ Return Receipt Postcard (MPEP 503)
16. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)
17. ☐ Non-Publication Request under 35 U.S.C. § 122 (b)(2)(B)(i)
18. ☐ Other:

Note: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 MUST be included in an Application Data Sheet (ADS).

(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS: Customer Number 79141

Signature	/Jamie J. Zheng/	Date	June 14, 2022
Name (Print/Type)	Jamie J. Zheng	Registration No. (Attorney/Agent)	51,167

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NL066-13US02
	Application Number	
Title of Invention	MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hyun		Lee	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	State/Province	Country of Residence
Ladera Ranch	CA	US

Mailing Address of Inventor:

Address 1	175 Technology, Suite 150
Address 2	

City	State/Province	Postal Code	Country
Irvine	CA	92618	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	79141	
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Application Information:

Title of the Invention	MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION		
Attorney Docket Number	NL066-13US02	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	3	Suggested Figure for Publication (if any)	

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Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
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Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	79141		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	16/680060	2019-11-11

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NL066-13US02
	Application Number	
Title of Invention	MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION	

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16/680060	Continuation of	15/857553	2017-12-28	10474595	2019-11-12

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/857553	Continuation of	15/088155	2016-04-01	9858218	2018-01-02

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/088155	Continuation of	13/942721	2013-07-16	9311116	2016-04-12

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/942721	Continuation of	12/815339	2010-06-14	8489837	2013-07-16

Prior Application Status	Expired	Remove

Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12/815339	Claims benefit of provisional	61/186799	2009-06-12

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

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Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[j] (if applicable)

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

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2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

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☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

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	Application Number	
Title of Invention	MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION	

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Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Netlist, Inc.		
Mailing Address Information For Applicant:			
Address 1	175 Technology, Suite 150		
Address 2			
City	Irvine	**State/Province**	CA
Country	US	Postal Code	92618
Phone Number		Fax Number	
Email Address			

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Assignee Information including Non-Applicant Assignee Information:

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Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

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Mailing Address Information For Assignee including Non-Applicant Assignee:

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Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
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See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Jamie J. Zheng/			Date (YYYY-MM-DD)	2022-06-14
First Name	Jamie J.	Last Name	Zheng	Registration Number	51167

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This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. App. No. 16/680,060, filed November 11, 2019, which is a continuation of U.S. App. No. 15/857,553, filed December 28, 2017, now U.S. Pat. No. 10474595, which is a continuation of U.S. App. No. 15/088,155, filed April 1, 2016, now U.S. Pat. No. 9858218, which is a continuation of U.S. App. No. 13/942,721, filed July 16, 2013, now U.S. Pat. No. 9,311,116, which is a continuation of U.S. App. No. 12/815,339, filed June 14, 2010, now U.S. Pat. No. 8,489,837, which claims the benefit of priority from U.S. Provisional App. No. 61/186,799, filed June 12, 2009, each of which is incorporated in its entirety by reference herein.

FIELD OF THE DISCLOSURE

[0002] The present disclosure relates to the operation of memory modules. Specifically, the present disclosure relates to systems and methods for handshaking with a memory module during or upon completion of initialization.

BACKGROUND OF THE DISCLOSURE

[0003] Memory subsystems such as memory modules are generally involved in the initialization procedure for computer systems, including servers, personal computers, and the like. For example, during system-wide initialization, the memory subsystems may undergo internal initialization procedures, or the system memory controller may otherwise interact with the memory subsystems during the initialization procedure. As part of this interaction, the system memory controller may request that the memory subsystem perform one or more requested tasks during system initialization.

SUMMARY

[0004] According to certain aspects, a memory module is coupled to a memory controller of a host computer system via an interface. The interface includes data, address and control signal pins and an output pin in addition to the data, address and control signal pins. The memory module receives a first command from the memory controller via the address and control signal pins, and enters a

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first mode in response to the first command. The memory module in the first mode responds to at least one initialization sequence, and sends a first output signal via the output pin to indicate a status of the at least one initialization sequence to the memory controller. The memory module enters a second mode in which the memory module performs memory operations including memory read/write operations according to an industry standard. During the read/write operations, the memory module communicates data with the memory controller via the data signal pins in response to second memory commands received via the address and control signal pins. The memory module may output a second output signal related to the read/write operations via the output pin.

[0005] According to certain aspects, a memory module is coupled to a memory controller of a host computer system via an interface. The interface includes data, address and control signal pins and an output pin in addition to the data, address and control signal pins. The memory module performs an internal procedure in a first mode in response to a first command from the memory controller whereby the memory controller hands off control of the internal procedure to the first memory module. The memory module sends a first output signal via the output pin to indicate a status of the internal procedure to the memory controller. The memory module enters a second mode in which the memory module performs standard operations including one or more of memory read/write, pre-charge, refresh operations according to an industry standard. The memory module may output a second output signal related to the standard operations via the output pin.

[0006] In another aspect, a memory module is operable in a first mode and in a second mode. The memory module operates according to an industry standard in the second mode by performing standard operations including memory read/write operations in response to address and control signals from a memory controller of a host computer system. The memory module comprises a standard interface including data, address and control signal pins and an output pin in addition to the data, address and control signal pins. The memory module enters the first mode in response to a first command from the memory controller, in which the memory module responds to at least one initialization sequence. The memory module further comprises a notification circuit to output a notification signal indicating a status of the at least one initialization sequence to the memory controller via the output pin.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Figure 1 shows an example host computer system including an example memory module configured to perform handshaking with a memory controller of the host computer system according to certain embodiments described herein.

[0008] Figure 2 shows an example host computer system including example first and second memory modules configured to perform handshaking with a system memory controller of the host computer system according to certain embodiments described herein.

[0009] Figure 3 shows a host computer system including example first and second memory modules configured to perform handshaking with a memory controller of the host system, where the notification circuits of the first and second memory modules have another example configuration according to certain embodiments described herein.

[0010] Figure 4 and Figure 5 show example methods of using at least one memory module according to certain embodiments described herein.

DETAILED DESCRIPTION

[0011] Existing initialization schemes have certain inefficiencies which lead to wasted time and expense. Thus, there is a need to reduce the time and complexity involved in system memory controller interactions with memory subsystems during initialization. Certain embodiments described herein advantageously satisfy at least a portion of this need by providing a system and method which utilizes a feedback path from a memory subsystem such as a memory module to a system memory controller, such as a Memory Controller Hub (MCH) of a computer system during initialization.

[0012] In general, there is no existing method of handshaking between the MCH (e.g., system memory controller) and a memory subsystem (e.g., memory module) during initialization. For example, in conventional systems, the system memory controller does not monitor the error-out signal from the memory subsystem. This causes the MCH to perform blind execution. In a typical server (e.g., an Intel or AMD or other chipset based server), the lack of any handshaking between the MCH and the memory subsystem during the server initialization period has not been a serious issue since the MCH generally has complete control over the initialization procedure. However, one possible configuration for LR-DIMM (Load Reduced DIMM) includes the MCH handing over

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one or more parts of the initialization operation sequence to the memory subsystem. This raises an unprecedented issue not addressed in conventional systems because, in such proposed configurations, the system can benefit from the MCH handshaking with the memory subsystem controller, as described more fully below.

[0013] Such an LR-DIMM configuration may have the MCH inserting a waiting period of predetermined length during which the MCH is idle and the memory subsystem controller undergoes initialization. However, one shortcoming of this LR-DIMM configuration would be that it requires the MCH to be in standby (idle, or wait) while the memory subsystem controller completes its task. Under such an arrangement, since the time to complete a task can be dependent on the density, speed and configuration of the memory subsystem, and these parameters may be unknown to the MCH, the MCH may have to insert a single, predetermined standby period. In addition, if there are multiple occasions that the MCH needs to hand off control to the memory subsystem controller, the required MCH wait periods can be different from one occasion to another, and it complicates the correlation between the MCH and the memory subsystem controller. For example, the MCH according to such a scheme may give control to the local memory controller of a memory subsystem (e.g., memory module) for execution of a training sequence. The MCH may wait for a pre-determined period of time and then assume that the local memory controller has completed the training sequence. However, depending on the memory subsystem parameters (e.g., memory capacity, speed, number of ranks, etc.), the time for actually completing the training sequence may vary and may be longer or shorter than predetermined period of time.

[0014] In general, handshaking can be implemented in at least two ways; polling and notifying. In the polling method, the MCH reads a status register in the memory subsystem controller to find out if the memory subsystem controller has completed the required or requested operation. For example, a status register may be read out through a serial interface such as System Management Bus (SMBus). However, a register polling method is generally inefficient because the system memory controller does not know exactly when the memory subsystem will have completed the required or requested operation. Thus, the system memory controller may wait longer than necessary to poll the memory subsystem, thereby delaying the overall initialization process. Additionally, the problem may be compounded because multiple training sequences or other initialization sequences may be run on the memory subsystem during a particular initialization period, resulting in accumulation of such unnecessary delays. Moreover, polling generally involves

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scheduling polling intervals during which the system memory controller is not performing other operations, resulting in further inefficiency.

[0015] Alternatively, the notifying method is an advantageous handshaking method between the MCH and the memory subsystem controller. According to a notifying method, the memory subsystem controller sends a signal to the MCH when the memory subsystem controller completes the required or requested operation. This method allows the MCH to execute one or more independent commands while it is waiting for a notification signal from the memory subsystem controller.

[0016] Certain embodiments described herein provide a method of establishing a handshake mechanism based on notification signaling. In certain embodiments, this mechanism can be implemented by adding a new interface (notifying) signal between the MCH and the memory subsystem controller, or by adding an additional functionality to an existing, non-timing critical signal without altering the memory subsystem hardware. In either case, the interface between the MCH and the memory subsystem controller of certain embodiments can be an open drain signaling from the memory subsystem controller to the MCH, although a variety of other configurations are possible. As will be appreciated by persons skilled in the art, the terms MCH, system memory controller, and memory subsystem are used generally interchangeable throughout this disclosure, and the terms memory module, memory subsystem controller, and local memory controller are used generally interchangeably throughout this disclosure.

[0017] FIG. 1 illustrates an example host computer system 16 including an example memory module 10 according to certain embodiments described herein. The memory module 10 can comprise at least one output 12 configured to be operatively coupled to a system memory controller 14 of the host computer system 16. In certain embodiments, the memory module 10 is configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode. The memory module 10 may further include a controller circuit 18. In some embodiments, the controller circuit 18 is configured to cause the memory module 10 to enter the initialization mode. The memory module 10 can further include a notification circuit 20 configured to drive the at least one output 12 while the memory module 10 is in the initialization mode to provide at least one notification signal to the memory controller 14 indicating at least one status of the at least one initialization

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sequence.

[0018] The memory module 10 may comprise a printed-circuit board (PCB) 22. In certain embodiments, the memory module 10 has a memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, 16-GB, or higher. Other memory capacities are also compatible with certain embodiments described herein. In addition, memory modules 10 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. The PCB 22 can have an industry-standard form factor. For example, the PCB 22 can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB 20 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB 22 has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FBDIMM), mini-DIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein. In other embodiments, certain non-DIMM form factors are possible such as, for example, single in-line memory module (SIMM), multi-media card (MMC), and small computer system interface (SCSI).

[0019] In certain embodiments, the memory module 10 is operatively coupled to (e.g., in electrical communication with) the host computer system 16. In certain other embodiments, the memory module 10 may communicate with the host computer system 16 using some other type of communication, such as, for example, optical communication. Examples of host computer systems 16 include, but are not limited to, blade servers, 1U servers, personal computers (PCs), and other applications in which space is constrained or limited. The PCB 22 can comprise an interface (not shown) that is configured to be in electrical communication with the host computer system 16. For example, the interface can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system 16. The interface of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory module 10 and the host system 16. For example, the interface can comprise a standard 240-pin DDR2 edge connector. The at least one output 12 may be routed over the interface, for example.

[0020] The memory module 10 may also comprise one or more memory elements (not shown),

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such as dynamic random-access memory (DRAM) elements, for example. Types of DRAM elements compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, DDR4, and synchronous DRAM (SDRAM). In addition, memory elements having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Memory elements compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP). In certain embodiments, the memory module 10 may also include one or more non-volatile memory elements, such as one or more flash memory elements. Types of flash memory elements compatible with certain embodiments described herein include, but are not limited to, NOR flash, NAND flash, ONE-NAND flash, and multi-level cell (MLC).

[0021] The controller circuit 18 of certain embodiments generally controls the operation of the memory module 10. For example, the controller circuit 18 may control the memory elements of the memory module 10 and/or communicate with the system memory controller 14. For example, the controller circuit 18 may receive and process address and command signals (e.g., read, write commands) from the system memory controller 14 and transmit appropriate address and commands to the memory elements in response. See, e.g., U.S. Pat. Appl. Publ. Nos. 2006/0062047 A1 and 2006/0262586 A1, each of which is incorporated in its entirety by reference herein. In certain embodiments, the controller circuit 18 comprises a local memory controller. Additionally, depending on the architecture of the memory module 10, such as for an FB-DIMM, the controller circuit 18 may comprise an advanced memory buffer (AMB). The controller circuit 18 can comprise one or more of a field-programmable gate array (FPGA), a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, and a complex programmable logic device (CPLD), for example. In certain embodiments, the controller circuit 18 comprises various discrete electrical elements, while in certain other embodiments, the controller circuit 18 comprises one or more integrated circuits.

[0022] As discussed, the memory module 10 is configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode. In one embodiment, for example, the at least one initialization sequence may comprise one or more training sequences. The initialization sequence (e.g., comprising one or more training sequences) may be initiated by the system memory

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controller 14. In some embodiments, the controller circuit 18 is configured to cause the memory module 10 to enter the initialization mode. For example, the controller circuit 18 may be configured to execute a routine implementing the at least one initialization sequence when the appropriate signal or command is received from the memory controller 14 or is otherwise received from the host computer system 16 (e.g., upon receipt of a reset signal).

[0023] In certain embodiments, for example, the computer system 16 is coupled to a plurality of memory modules 10, 26 including the memory module 10 and at least a second memory module 26, and the memory controller 14 (e.g., MCH) trains each module 10, 26 separately, in series. In one example scenario, the memory controller 14 issues a first command to the memory module 10, and, in response, the memory module 10 executes an initialization sequence (e.g., one or more training sequences). Upon completion of the initialization sequence, the first memory module 10 advantageously issues a notification to the memory controller 14 in accordance with embodiments described herein. In response, the memory controller 14 issues a second command, this time to the memory module 26, and, in response, the memory module 26 executes an initialization sequence (e.g., one or more training sequences). Upon completion of the initialization sequence, the second memory module 26, similar to the first memory module 10, advantageously issues a notification to the memory controller 14 in accordance with embodiments described herein. In response, where there are more than two memory modules 10, 26, the memory controller 14 issues a third command to a third memory module (not shown), and so forth. One example computer system 16 capable of implementing such a scenario is configured to execute an Intel Basic Input/Output System (BIOS), and comprises a plurality of memory modules 10, 26 having an LRDIMM configuration. In such an example system, the Intel BIOS causes the system memory controller 14 to initialize the LRDIMM memory modules 10, 26 serially.

[0024] The operational mode is the normal mode of the memory module 10. For example, during the operational mode, the memory module 10 is generally accessed by the system memory controller 14 of the host computer 16 during standard computer operation not associated with initialization. For example, the system memory controller 14 may cause the memory module 10 to perform standard operations such as memory read/write, pre-charge, refresh, etc., while in operational mode, although it will be appreciated that one or more of these operations can also be performed by the memory module 10 while in initialization mode in certain embodiments.

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[0025] The notification circuit 20 can be configured to drive the at least one output 12, while the memory module 10 is in the initialization mode or after the memory module 10 completes one or more initialization sequences, to provide the at least one notification signal to the memory controller 14 indicating at least one status of the at least one initialization sequence. While shown in FIGS. 1-3 as forming a part of the controller circuit 18, the notification circuit 20 may be a physically and/or logically separate circuit in certain embodiments. While a variety of configurations are possible, the notification circuit 20 may comprise one or more transistors, one or more logic elements (e.g., AND, OR, NOR, NAND, XOR gates, and the like), or a combination thereof. In some embodiments, the notification circuit 20 may additionally or alternatively comprise one or more of an FPGA, PLD, CPLD, ASIC, custom-designed semiconductor device, discrete electrical elements, and an integrated circuit.

[0026] The at least one status of certain embodiments comprises completion of the at least one initialization sequence, such that the at least one notification signal is indicative of the completion of the at least one initialization sequence. The at least one status of certain embodiments comprises execution of the at least one initialization sequence. For example, the at least one status may indicate that the at least one initialization sequence is currently being executed. In some embodiments, the at least one status may provide an indication that a certain task has been completed by the memory module 10, such as a training task requested by the system memory controller 14. In certain embodiments, the notification circuit 20 can be configured to drive the at least one output 12 to a first state indicative of execution of the at least one initialization sequence or to a second state indicative of completion of the at least one initialization sequence. As one example, the first state may be a high or low logic level, and the second state may be a high impedance state. In another case, the first state is a high or low logic level, and the second state is the inverse logic level of the first state.

[0027] The at least one output 12 of certain embodiments is configured to be operatively coupled to at least one interrupt of the system memory controller 14, and the system memory controller 14 is responsive to the at least one notification signal indicating completion of the at least one initialization sequence. For example, the system memory controller 14 may trigger execution of an interrupt routine upon receipt of the notification signal on the output 12. The interrupt routine generally executes the appropriate operations for the at least one status indicated by the at least one notification signal. For example, if the at least one status indicates that the at least one

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initialization sequence is complete, execution of the interrupt routine may cause the system memory controller 14 to notify the host computer system 16 that the system initialization, or a portion thereof, is completed. In one embodiment, for example, the execution of the interrupt routine causes the system memory controller 14 to initiate a subsequent training sequence for the memory module 10 or on another memory module connected to the host system 16. For example, in one embodiment, a central processing unit (CPU) of the host system 16 (not shown) enters a "Wait" state after issuing a command to the memory module 10 to enter the initialization mode. Receipt of the at least one notification signal on the output 12 triggers execution of the interrupt routine, which interrupts the CPU, causing the "Wait" state to be aborted and allowing the host system 16 to continue operation. In this manner, generation of the interrupt on the at least one output 12 can allow completion of the at least one initialization sequence to receive generally immediate attention from the CPU and/or memory controller 14 of the host system 16. As will be appreciated, the CPU and memory controller 14 of the host system 16 may comprise separate modules, or may alternatively comprise a single integrated module, depending on the architecture of the host system 16 chip-set.

[0028] In certain embodiments, execution of the interrupt routine causes the system memory controller 14 to cause the memory module 10 to exit the initialization mode and to enter the operational mode. In another embodiment, the memory module 10 automatically enters the operational mode upon completion of the at least one initialization sequence without intervention from the memory controller 14.

[0029] In some embodiments, the at least one output 12 is operated in conformance with a standard (e.g., an industry standard) when the memory module 10 is in the operational mode, but is not operated in conformance with the standard when the memory module 10 is in the initialization mode. An example of a standard in accordance with certain embodiments described herein is one or more of the industry standard promulgated by the Joint Electronic Devices Engineering Counsel (JEDEC). For example, the operation and behavior of the at least one output 12 may conform to an industry standard when the memory module 10 is in the operational mode, but the operation and behavior of the at least one output 12 may not conform to the industry standard when the memory module 10 is in the initialization mode. Because the at least one output 12 does not conform to the standard during initialization mode, an existing (e.g., JEDEC-specified) pin may be utilized to provide the at least one notification signal to the system memory controller 14 from

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the memory module 10 during the initialization mode. In one embodiment, for example, the at least one output 12 comprises an error-out pin of the memory module 10. In conventional systems, the operation of the error-out pin is undefined by the standard during initialization. However, in certain embodiments described herein, during the operational mode, the error-out pin may be used according a conventional industry standard (e.g., a JEDEC standard) to indicate a parity error has occurred in the memory module 10. During the initialization mode, the error-out pin can be used to transmit the at least one notification signal to the system memory controller 14.

[0030] It is advantageous to use the error-out pin for initialization status notification according to certain embodiments because the error-out pin can be asserted by the memory module 10 independent from system memory controller 14 requests or commands. Also, because the error-out pin is a JEDEC-specified pin, design cost and complexity are reduced because additional pin-outs and interrupt design changes can be avoided (e.g., in cases where such changes in hardware or chipset may not be feasible to provide the at least one status to the system memory controller 14). However, in certain other embodiments, providing the at least one status may be implemented by adding one or more pins to the system memory controller 14 (e.g., MCH) and to the controller circuit 18 (e.g., local memory controller), thereby utilizing changes in hardware or the chipset.

[0031] Moreover, the error-out pin may be coupled to an interrupt of the system memory controller 14 (e.g., according to the JEDEC standard). Thus, where the error-out pin is used, from the system point of view in accordance with certain embodiments, the notification of completion of the required or requested task from the memory module 10 (e.g., by the local memory controller) generates an interrupt communicated to the system during the initialization period and indicative of completion of the required or requested task. Assertion of the same pin during normal (non-initialization) operation upon an error occurring, on the other hand, generates an interrupt communicated to the system during the normal operation indicative of the occurrence of the error condition. Thus, in certain embodiments, the error-out pin and corresponding signal memory module 10 can be used to support the notifying function and to provide the at least one status generally without changing hardware. Certain other such embodiments involve modifying the basic input/output system (BIOS) or other programming change. For example, the BIOS may be modified to indicate to the system memory controller 14 how to respond to the notification signal (e.g., to the error_out signal or the interrupt corresponding thereto).

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[0032] In certain other embodiments, the at least one output 12 may include other existing (e.g., JEDEC specified) pins instead of, or in addition to, the error-out pin. In yet other configurations, at least one additional (e.g., non-JEDEC specified) pin may be employed. In general, any pin not otherwise active during the initialization mode may be used (e.g., high-order address pins, read/write pins, data pins, etc.).

[0033] The at least one output 12 can further be configured to be operatively coupled to at least one second output 24 of a second memory module 26 in some embodiments, as schematically illustrated in FIGS. 1-3. The second memory module 26 may be generally similar in structure and function to the memory module 10, and may comprise a controller circuit 28 and a notification circuit 30, for example. The second memory module 26 may be generally identical to the first memory module 10, or may have a different memory capacity, form factor, etc., than the first memory module 10. More than two such memory modules may be present in certain embodiments. As described above, the second memory module 26 can be configured to operate in at least two modes comprising an initialization mode during which the second memory module 26 executes at least one initialization sequence, and an operational mode. For example, the initialization and operational modes may be similar to those describe above in relation to the first memory module 10.

[0034] The second memory module 26 can also be configured to drive the at least one second output 24 to a third state indicative of execution of at least one initialization sequence of the second memory module 26 or to a fourth state indicative of completion of the at least one initialization sequence of the second memory module 26. Additionally, in some embodiments, the at least one first output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are operatively coupled together by a bus 32 which is also operatively coupled to at least one input 34 of the system memory controller 14. In other embodiments (not shown), the at least one first output 12 and the at least one second output 24 are not coupled together, and are coupled to two separate inputs of the system memory controller 14.

[0035] FIG. 2 shows an example host computer system 16 including example first and second memory modules 10, 26. As shown, the notification circuits 20, 30 of the first and second memory modules 10, 26 each comprise at least one transistor 36, 38. The at least one transistor 36, 38 can be in an open-drain configuration, as shown, although other configurations are possible. In certain

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such embodiments, the first state of the at least one first output 12 is a first logic level, the second state of the at least one first output 12 is a high-impedance state, the third state of the at least one second output 24 is the first logic level, and the fourth state of the at least one second output 24 is the high-impedance state. In the illustrated example, while the at least one initialization sequence is in progress, the first and second memory modules 10, 26 drive the gates of the respective transistors 36, 38 high. Thus, the transistors 36, 38 are respectively low impedance while the memory modules 10, 26 are executing each section of the initialization sequence, thereby pulling the first and second outputs 12, 24 low. Thus, the first state and the third state are low logic levels (ground) in the example configuration. Also, because the first and second outputs 12, 24 are coupled together by the bus 32, if the at least one initialization sequence of either one of the first and second memory modules 10, 26 are in progress, the bus 32 will be pulled to a low logic level.

[0036] As each of the two memory modules 10, 26 completes its at least one initialization sequence, it can drive the corresponding at least one first and second outputs 12, 24 respectively to a high impedance state, For example, once the at least one initialization sequence on each of the first and second memory modules 10, 26 is completed, the first and second memory modules 10, 26 can drive the gates of the respective transistors 36, 38 low, resulting in a high-impedance state on the at least one first and second outputs 12, 24 causing the bus 32 to be pulled high by the system memory controller 14. Accordingly, only once the at least one initialization sequence of both the first and second memory modules 10, 26 are complete, the bus 32 will be pulled high by the internal pull-up configuration 40 of the system memory controller 14. The second state and the fourth state are therefore high-impedance values in the example embodiment. Thus, the system memory controller 14 can monitor the value on the bus 32 via the first input 34 to determine when both of the memory modules 10, 26 have completed the at least one initialization sequence. As discussed, in other configurations the at least one first and second outputs 12, 24 may be received on separate inputs of the system memory controller 14, and the status of the at least one initialization sequence of each memory module 10, 26 may be monitored independently.

[0037] As discussed above, in certain embodiments in which more than one memory module 10, 26 is connected to the system memory controller 14, each memory module 10, 26 or associated controller circuit 18 (e.g., local memory controller) causes the corresponding notification circuit 20, 30 to drive the at least one output 12, 24 to the high impedance state from the low impedance state when it completes the requested or required operation. Thus, in certain such embodiments,

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the system memory controller 14 (e.g., MCH) can only pull the notifying signal high when all memory modules 10, 26 or associated controller circuits (e.g., local memory controllers) have completed the required or requested operation (e.g., initialization sequence). This configuration allows the system memory controller 14 (e.g., MCH) to work with a non-homogenous memory subsystem. For example, the system memory controller 14 may be able to monitor the progress of multiple memory modules 10, 26 including a mix of DIMMs or other memory modules having differing characteristics, such as DIMM density, rank configurations, DRAM density, speed, DRAM configuration, etc.

[0038] Additionally, the at least one output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are configured to be operatively coupled to at least one interrupt of the system memory controller 14 in certain embodiments. In certain such embodiments, the system memory controller 14 can be responsive to the second state of the first memory module 10 and the fourth state of the second memory module 26 by triggering execution of an interrupt routine by a processor of the system memory controller 14. For example, in the example system of FIG. 2, when the bus 32 is pulled high by the pull-up configuration 40 indicating the second state of the first memory module 10 and the fourth state of the second memory module 26, the system memory controller 14 triggers execution of the interrupt routine.

[0039] In some embodiments, in which the at least one first output 12 and the at least one second output 24 are operatively coupled to separate inputs of the system memory controller 14, the at least one first output 12 and the at least out second output 24 may be operatively coupled to two separate interrupts. For example, the system memory controller 14 may be responsive to the second state of the first memory module 10 by triggering execution of a first interrupt routine associated with a first interrupt, and may be responsive to the fourth state of the second memory module 26 by triggering execution of a second interrupt routine associated with the second interrupt. In yet other embodiments, the separate inputs of the memory controller 14 are internally operatively coupled to the same interrupt, or are operatively coupled to separate interrupts which trigger the same interrupt routine.

[0040] FIG. 3 shows a host computer system 16 including an example memory module 10 where the notification circuit 20 of the memory module 10 has another example configuration in accordance with certain embodiments described herein. In the example configuration of FIG. 3,

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the at least one first output 12 is operatively coupled to an error-out pin of the memory module 10, and a multiplexor 42 drives the transistor 36 with either of a task_in_progress signal 44 or an error signal 46 (e.g., parity error signal). In one embodiment, for example, the multiplexor 42 may be configured to drive the transistor 36 with the task_in_progress signal 44 when the memory module 10 is in the initialization mode or is executing the at least one initialization sequence, and with the error signal 46 when the memory module 10 is in the operational mode. Thus, the memory module 10 can be advantageously configured to both perform the standard (e.g., JEDEC-specified) error reporting functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode, as described herein. As shown in FIG. 3, a second memory module 26 including a similar configuration can also be operatively coupled to the host computer system 16. In certain embodiments, the at least one second output 24 of the second memory module 26 can be operatively coupled to the at least one first output 12 by the bus 32, as described above (e.g., with respect to FIG. 2).

[0041] FIG. 4 shows an example method 100 of using the at least one memory module 10 in accordance with certain embodiments described herein. While the description below of the method 100 refers to structure shown in FIGS. 1-3, other structures may also be used in accordance with certain embodiments described herein. At block 102, the method 100 of certain embodiments comprises providing a first memory module 10 comprising at least one first output 12 operatively coupled to a memory controller 14 of a host computer system 16. The first memory module 10 can be configured to operate in at least two modes comprising an initialization mode during which the first memory module 10 executes at least one initialization sequence, and an operational mode. For example, the at least one initialization sequence may comprise one or more steps of a series of steps associated with an initialization procedure of the host computer system 16.

[0042] At block 104, the method 100 in some embodiments comprises causing the first memory module 10 to enter the initialization mode. At block 106, the method 100 of certain embodiments comprises driving the at least one first output 12 to a first state while the memory module 10 executes the at least one initialization sequence. Upon completion of the at least one initialization sequence, the method of certain embodiments comprises driving the at least one first output 12 to a second state different than the first state. In certain embodiments, the first state is a first logic level and the second state is a high impedance state. Additionally, in certain embodiments, the at least one first output 12 is operatively coupled to at least one interrupt of the memory controller

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14 such that driving the at least one output 12 to the second state triggers the memory controller to execute an interrupt routine.

[0043] In certain embodiments, the at least one output 12 is operated in conformance with JEDEC standard when the first memory module 10 is in the operational mode, but is not operated in conformance with the JEDEC standard when the first memory module 10 is in the initialization mode. The at least one first output 12 of certain embodiments include an error-out pin of the first memory module, for example.

[0044] The method 100 can further include providing a second memory module 26 comprising at least one second output 24 operatively coupled to the memory controller 14. The second memory module 26 can be configured to operate in one of at least two modes comprising an initialization mode, during which the second memory module 26 executes at least one initialization sequence, and an operational mode. The method 100 can further include causing the second memory module 26 to enter the initialization mode. In certain embodiments, the method 100 also includes driving the at least one second output 24 of the second memory module 26 to a third state while the second memory module 26 executes the at least one initialization sequence. Upon completion of the at least one initialization sequence, the method 100 can further include driving the at least one second output 24 of the second memory module 26 to a fourth state different from the third state.

[0045] In certain embodiments, the at least one first output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are operatively coupled together by a bus 32 which is also operatively coupled to at least one input 34 of the memory controller 14. In certain other embodiments, the at least one first output 12 of the first memory module 10 is operatively coupled to a first input 34 of the memory controller 14 and the at least one second output 24 of the second memory module 26 is operatively coupled to a second input (not shown) of the memory controller 14.

[0046] FIG. 5 shows another example method 200 of using at least one memory module 10 in accordance with certain embodiments described herein. At block 202, the method 200 may include providing a memory module 10 comprising at least one output 12 operatively coupled to a memory controller 14 of a host computer system 16. The memory module 10 may be configured to operate in at least two modes comprising an initialization mode, during which the memory module 10 executes at least one initialization sequence, and an operational mode.

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[0047] The method 200 can further include causing the memory module 10 to enter the initialization mode at block 204. At block 206, the method 200 can include receiving a notification signal from the at least one output 12 of the memory module 10. The notification signal may indicate that the memory module 10 has completed the initialization sequence, for example. In certain embodiments, the method 200 further comprises executing an interrupt routine by the memory controller 14 in response to the notification signal.

TERMINOLOGY/ALTERNATIVE EMBODIMENTS

[0048] Embodiments have been described in connection with the accompanying drawings. However, it should be understood that the figures are not drawn to scale. Distances, angles, etc. are merely illustrative and do not necessarily bear an exact relationship to actual dimensions and layout of the devices illustrated. In addition, the foregoing embodiments have been described at a level of detail to allow one of ordinary skill in the art to make and use the devices, systems, etc. described herein. A wide variety of variation is possible. Components, elements, and/or steps can be altered, added, removed, or rearranged. While certain embodiments have been explicitly described, other embodiments will become apparent to those of ordinary skill in the art based on this disclosure.

[0049] Conditional language used herein, such as, among others, "can," "could," "might," "may," "e.g.," and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment.

[0050] Depending on the embodiment, certain acts, events, or functions of any of the methods described herein can be performed in a different sequence, can be added, merged, or left out all together (e.g., not all described acts or events are necessary for the practice of the method). Moreover, in certain embodiments, acts or events can be performed concurrently, e.g., through multi-threaded processing, interrupt processing, or multiple processors or processor cores, rather than sequentially.

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[0051] The various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein can be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. The described functionality can be implemented in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the disclosure.

[0052] The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein can be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor can be a microprocessor, but in the alternative, the processor can be any conventional processor, controller, microcontroller, or state machine. A processor can also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0053] The blocks of the methods and algorithms described in connection with the embodiments disclosed herein can be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module can reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, a hard disk, a removable disk, a CD-ROM, or any other form of computer-readable storage medium known in the art. An exemplary storage medium is coupled to a processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium can be integral to the processor. The processor and the storage medium can reside in an ASIC. The ASIC can reside in a user terminal. In the alternative, the processor and the storage medium can reside as discrete components in a user terminal.

[0054] Certain embodiments described herein are compatible with a memory system including

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memory devices with various attributes (see, e.g., FIGS. 2 and 3). For example, the memory system of certain embodiments may include various data slice sizes (e.g., two, four, eight, or 16 bit data slices) and corresponding memories (e.g., memories having two, four, eight, or 16 bit data widths).

[0055] Although certain embodiments and examples are discussed above, it is understood that the inventive subject matter extends beyond the specifically disclosed embodiments to other alternative embodiments and/or uses of the invention and obvious modifications and equivalents thereof. It is intended that the scope of the inventions disclosed herein should not be limited by the particular disclosed embodiments. Thus, for example, in any method or process disclosed herein, the acts or operations making up the method/process may be performed in any suitable sequence and are not necessarily limited to any particular disclosed sequence.

[0056] Various aspects and advantages of the embodiments have been described where appropriate. It is to be understood that not necessarily all such aspects or advantages may be achieved in accordance with any particular embodiment. Thus, for example, it should be recognized that the various embodiments may be carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other aspects or advantages as may be taught or suggested herein.

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WHAT IS CLAIMED IS:

1. A memory subsystem operable with a memory controller of a host system, comprising:

dynamic random access memory elements on a printed circuit board and configurable to communicate data signals with the memory controller; and

a memory subsystem controller on the printed circuit board and coupled to the dynamic random access memory elements, the memory subsystem controller having an open drain output;

wherein, during a normal memory read or write operation, the memory subsystem controller is configured to receive address and command signals associated with the memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals, and the memory subsystem controller is further configured to output via the open drain output a parity error signal in response to a parity error having occurred during the memory read or write operation; and

wherein, during an initialization operation, the memory subsystem controller is configured to output via the open train output a signal related to one or more parts of initialization operation sequences.

MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

ABSTRACT OF THE DISCLOSURE

According to certain aspects, a memory subsystem is coupled to a memory controller of a host computer system via an interface. The memory subsystem comprises dynamic random access memory elements and a memory subsystem controller. During a normal memory read or write operation, the memory subsystem controller is configured to receive address and command signals associated with the memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals. The memory subsystem controller is further configured to output via the open drain output a parity error signal in response to a parity error having occurred during the memory read or write operation. During an initialization operation, the memory subsystem controller is configured to output via the open train output a signal related to one or more parts of initialization operation sequences.

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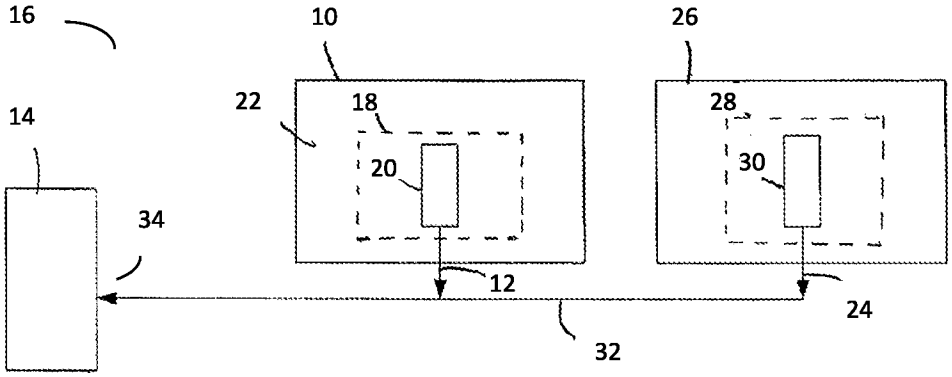


Figure 1

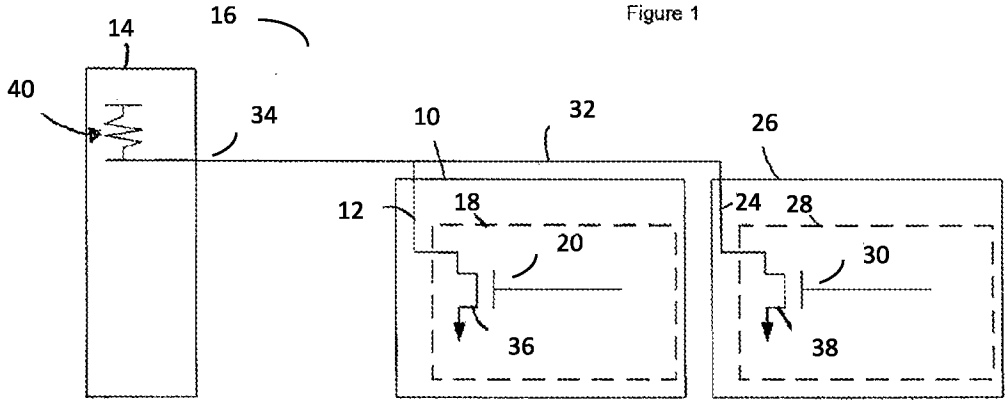


Figure 2

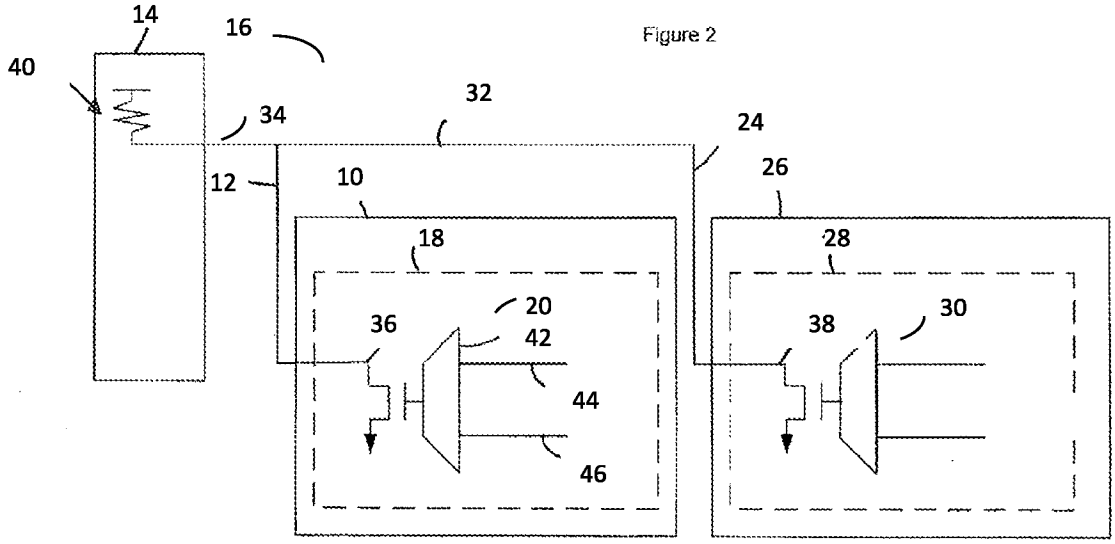


Figure 3

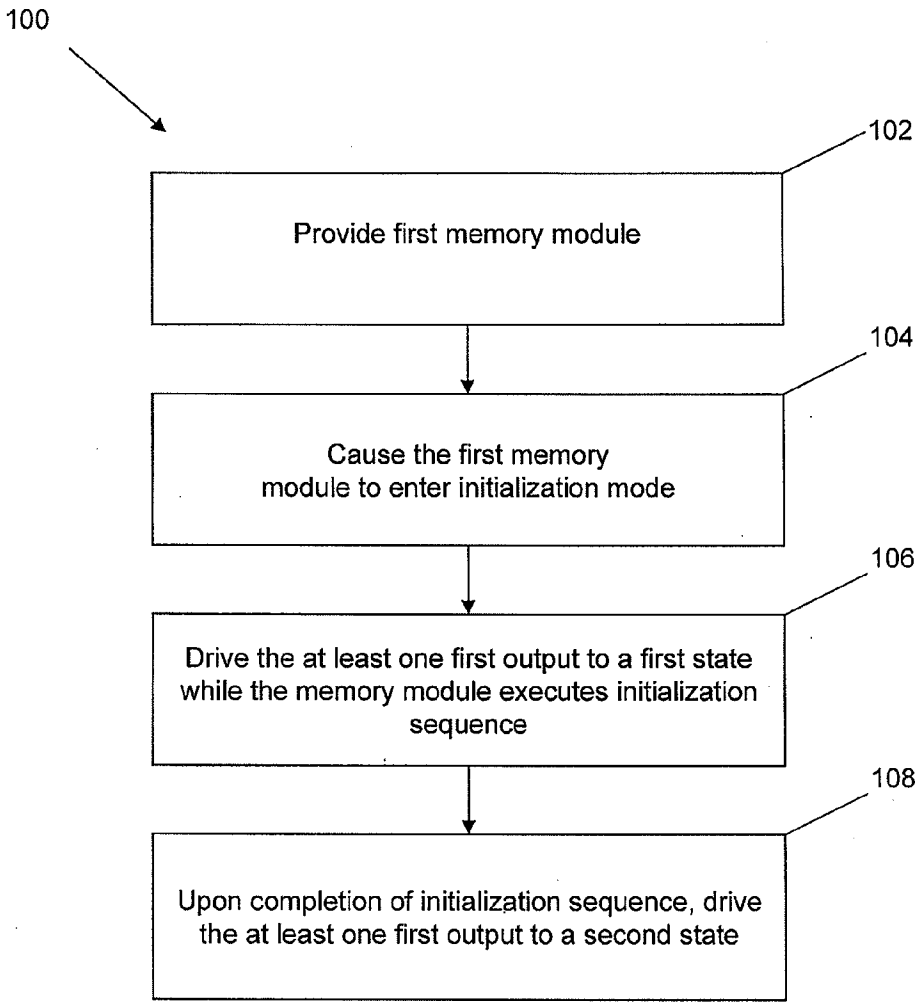

100
102
Provide first memory module
104
Cause the first memory module to enter initialization mode
106
Drive the at least one first output to a first state while the memory module executes initialization sequence
108
Upon completion of initialization sequence, drive the at least one first output to a second state

Figure 4

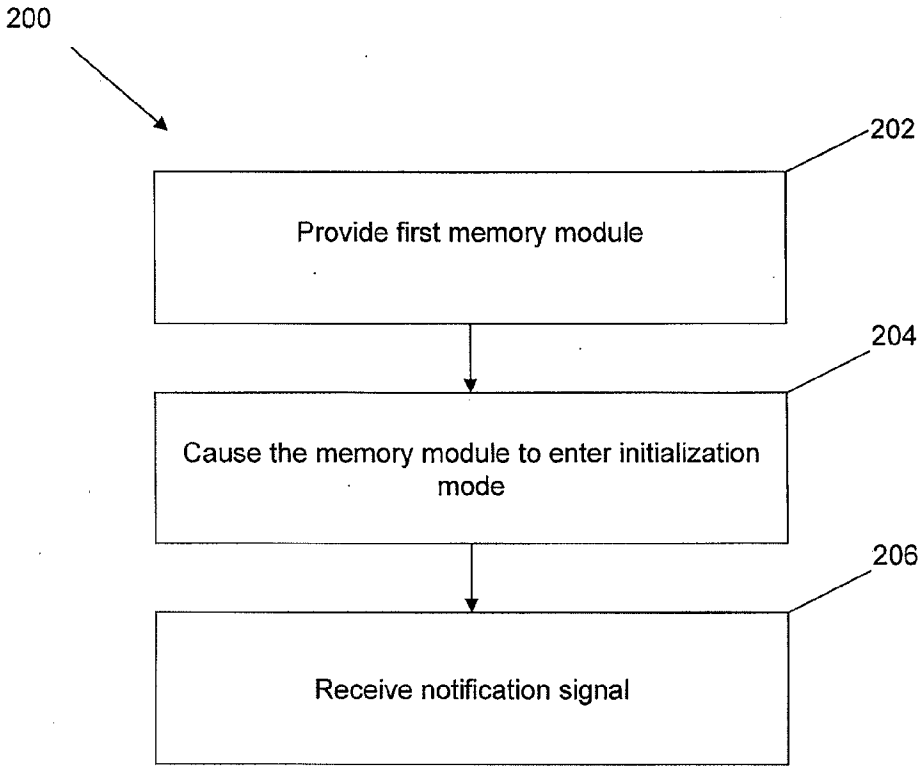

200
202
Provide first memory module
204
Cause the memory module to enter initialization mode
206
Receive notification signal

Figure 5

COMBINED DECLARATION AND ASSIGNMENT FOR UTILITY OR DESIGN APPLICATION

Title of Invention	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

DECLARATION

As a below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 13/942,721 filed on July 16, 2013 .

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) and other good and valuable consideration paid, I hereby sell and assign to

Netlist, Inc.
(Name of Assignee)

of 51 Discovery, Suite #150, Irvine, CA 92618
(Address of Assignee)

(hereinafter designated as the Assignee) my entire right, title and interest for the United States as defined in 35 USC 100, for any invention set forth in the above-identified application.

I agree to execute all papers necessary in connection with this application for patent in the USPTO for the invention, and any continuation, divisional or reissue applications thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient.

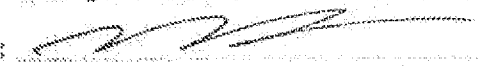
I agree to execute all papers necessary in connection with any post-grant proceeding which may occur in connection with this application or continuation, divisional or reissue thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such post-grant proceeding.

I agree to execute all papers and documents and perform any act which may be necessary in connection with claims or provisions of the International Convention for Protection of Industrial Property or similar agreements.

I agree to perform all affirmative acts which may be necessary to obtain a grant of a valid United States patent to the Assignee.

I hereby authorize and request the USPTO to issue any and all Letters Patents of the United States resulting from the application or any continuation, divisional or reissue applications thereof to the Assignee, as Assignee of my entire interest, and covenant that I have not executed, and will not execute, any agreement in conflict herewith.

First Inventor (Legal Name): Hyun Lee

Signature: 

Date: 10/9/2013

Electronic Acknowledgement Receipt

EFS ID:	45957431
Application Number:	17840593
International Application Number:	
Confirmation Number:	3678
Title of Invention:	MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION
First Named Inventor/Applicant Name:	Hyun LEE
Customer Number:	79141
Filer:	Jamie Jie Zheng/Marya Li
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	NL066-13US02
Receipt Date:	14-JUN-2022
Filing Date:	
Time Stamp:	23:38:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	NL066-13US02_App_Transmittal.pdf	100340 9e47f8c3d74483d9e221adbc97c6aba2adbaa1c8	no	1

Warnings:

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Information:					
2	Application Data Sheet	NL066-13US02_ADS.pdf	1256428 c1e17c733f0c02817bc4df8027643c8c7f9ae669	no	9
Warnings:					
Information:					
3		NL066-13US02_Specification.pdf	191637 b30d584daf3593b6ac27f227e7f44664096bdb3f	yes	21

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	19
	Claims	20	20
	Abstract	21	21

Warnings:					
Information:					
4	Drawings-only black and white line drawings	NL066-13US02_Drawings.pdf	569448 d32ae17144959e44ea616e0b77b1a5c87e37fd65	no	3
Warnings:					
Information:					
5	Oath or Declaration filed	NL066-13US02_Declaration.pdf	559369 0ab42a2ae188447d4de45b9de725866904a32496	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2677222		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/840,593	06/14/2022	Hyun Lee	NL066-13US02

CONFIRMATION NO. 3678

79141
USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

FORMALITIES LETTER

OC000000134662535

Date Mailed: 06/22/2022

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **320** basic filing fee.
- $ **160** surcharge.
- $ **700** search fee.
- $ **800** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1980** TOTAL FEE BALANCE DUE.

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Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/zmoguss/

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/840,593	06/14/2022	2185	0.00	NL066-13US02	1	1

CONFIRMATION NO. 3678

79141
USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

FILING RECEIPT

OC000000134662534

Date Mailed: 06/22/2022

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Hyun Lee, Ladera Ranch, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 16/680,060 11/11/2019
which is a CON of 15/857,553 12/28/2017 PAT 10474595
which is a CON of 15/088,155 04/01/2016 PAT 9667001
which is a CON of 13/942,721 07/16/2013 PAT 9311116
which is a CON of 12/815,339 06/14/2010 PAT 8489837
which claims benefit of 61/186,799 06/12/2009

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

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Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 06/21/2022

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/840,593**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

Preliminary Class

710

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

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countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/840,593

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE($)	FEE($)		RATE($)	FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	700
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 480 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1820

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1)		(Column 2)	(Column 3)					
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

Courtesy Reminder for
Application Serial No: 17/840,593

Attorney Docket No: NL066-13US02
Customer Number: 79141
Date of Electronic Notification: 06/22/2022

This is a courtesy reminder that new correspondence is available for this application. If you have not done so already, please review the correspondence. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com

To view your correspondence online or update your email addresses, please visit us anytime at **https://ppair-my.uspto.gov/pair/PrivatePair.**
If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov or call 1-866-217-9197.

Electronically filed August 22, 2022

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3678
Serial No.:	17/840,593	Group Art Unit:	2185
Filed:	June 14, 2022	Examiner:	TBA
For:	*MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION*	Attorney Docket No.:	NL066-13US02

RESPONSE TO THE NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

Mail Stop: MISSING PARTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice to File Missing Parts of Nonprovisional Application mailed June 22, 2022, a copy of which is enclosed, submitted herewith are the statutory basic filing, search and examination fees. The surcharge for the late payment of the statutory basic filing fee is also submitted herewith.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. NL066-13US02).

Respectfully submitted,

Date: August 22, 2022

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828

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Ex. 1002, p. 48

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/840,593	**08/22/2022 09:12:00 PM ET**	**NL066-13US02**

Title of Invention

MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3678	FILED BY	Jamie Zheng
PATENT CENTER #	60896350	FILING DATE	06/14/2022
CUSTOMER #	79141	FIRST NAMED INVENTOR	Hyun Lee
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
NL066-13US02_MP_Response.pdf	1	Miscellaneous Incoming Letter	68 KB
NL066-13US02_NTC_MISS_PRT.PDF	2	Miscellaneous Incoming Letter	69 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
NL066-	1F2AFF11E02C191BEC7F9016CEF07F1B1A9656054164D54237

13US02_MP_Response.pdf	A423ACC6907C65CE8879E42C14D3BE95E31C67480A688F87A D3BA8AE3D7EAC35449B25B6B96F4B
NL066-13US02_NTC_MISS_PRT.PDF	23E139C74038D2FE48637135DD8FF694B617C7520948D1F19A A7D04002BC47DD8080321A38B7D8206069B5DB18147FC66DC DD496C5210267B6F3C7A83DB20392

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/840,593	06/14/2022	Hyun Lee	NL066-13US02

CONFIRMATION NO. 3678

79141
USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

FORMALITIES LETTER

OC000000134662535

Date Mailed: 06/22/2022

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **320** basic filing fee.
- $ **160** surcharge.
- $ **700** search fee.
- $ **800** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1980** TOTAL FEE BALANCE DUE.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/zmoguss/

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Ex. 1002, p. 52

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/840,593	08/22/2022 09:12:00 PM ET	NL066-13US02

Title of Invention

MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3678	FILED BY	Jamie Zheng
PATENT CENTER #	60896350	AUTHORIZED BY	-
CUSTOMER #	79141	FILING DATE	06/14/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Hyun Lee

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 2819	E20228LL12422068	Jamie Zheng

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1051	SURCHARGE- LATE FILING FEE, SEARCH FEE, EXAMINATION FEE, INVENTOR'S OATH OR DECLARATION, OR APPLICATION FILED WITHOUT AT LEAST ONE CLAIM OR BY REFERENCE	160.00	1	160.00
1111	UTILITY PATENT APPL. SEARCH FEE	700.00	1	700.00
1011	BASIC FILING FEE - UTILITY (PAPER FILING ALSO REQUIRES NON-ELECTRONIC FILING FEE UNDER 1.16(T))	320.00	1	320.00

1311	PATENT APPL. EXAMINATION FEE	800.00	1	800.00

TOTAL AMOUNT: **$1,980.00**

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/840,593	06/14/2022	2185	1980	NL066-13US02	1	1

CONFIRMATION NO. 3678

UPDATED FILING RECEIPT

79141
USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

OC000000136006280

Date Mailed: 08/25/2022

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Hyun Lee, Ladera Ranch, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 16/680,060 11/11/2019 PAT 11386024
which is a CON of 15/857,553 12/28/2017 PAT 10474595
which is a CON of 15/088,155 04/01/2016 PAT 9667001
which is a CON of 13/942,721 07/16/2013 PAT 9311116
which is a CON of 12/815,339 06/14/2010 PAT 8489837
which claims benefit of 61/186,799 06/12/2009

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

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Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 06/21/2022

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/840,593**

Projected Publication Date: 12/01/2022

Non-Publication Request: No

Early Publication Request: No

Title

MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

Preliminary Class

710

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

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Ex. 1002, p. 56

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

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technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

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Ex. 1002, p. 58

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 17/840,593

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	700
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 480 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1820

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/840,593	06/14/2022	Hyun Lee	NL066-13US02	3678

79141 7590 10/05/2022

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER
CHERY, MARDOCHEE

ART UNIT	PAPER NUMBER
2133	

NOTIFICATION DATE	DELIVERY MODE
10/05/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com

Samsung Electronics Co., Ltd.
Ex. 1002, p. 60

Office Action Summary	Application No. 17/840,593	Applicant(s) Lee, Hyun	
	Examiner MARDOCHEE CHERY	Art Unit 2133	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 6/14/22.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 6/14/22 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claim Objections

2. Claim 1 objected to because of the following informalities: in line 13, "open train" should read – open drain--. Appropriate correction is required.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP § 2146 *et seq.* for applications not subject

to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. **A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp**.

4. Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 11386024; claims 1-24 of U.S. Patent No. 10474595; claims 1-20 of U.S. Patent No. 9311116; claims 1-18 of U.S. Patent No. 8489837. Although the claims at issue are not identical, they are not patentably distinct from each other because Although the claims at issue are not identical, they are not patentably distinct from each other because the claims of the issued patents make obvious the claims of the pending application in that the limitations claimed in the pending application are found in the issued patents even though the claimed limitations are not presented necessarily in the same order. "A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim Rejections - 35 USC § 103

5. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 1 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Hazelzet (20080098277 cited in IDS of 09/02/2020) and JEDEC (cited in IDS of 09/02/2020).

Regarding claim 1, Hazelnet discloses a memory subsystem operable with a memory controller of a host system, comprising: dynamic random access memory elements on a printed circuit board and configurable to communicate data signals with the memory controller [FIG. 2: *a DIMM with ECC/Parity buffer chip coupled to a memory interface chip which in turn coupled to a memory controller or processor; memory interface chip sends and receives data from the DIMM via data line and sends address and commands via a line; the memory interface chip then sends and receives data via the line to the DRAMs and sends address and command information to the register chip via the line; the memory interface chip further sends check bits for error correction purposes to the ECC/Parity register chip via another line*]; and a memory subsystem controller on the printed circuit board and coupled to the dynamic random access memory elements,

the memory subsystem controller having an open drain output [FIG. 2: *memory controller receiving address and control signals through DATA line, CMD/CHK BITS line*]; and the memory subsystem controller is further configured to output via the open drain output a parity error signal in response to a parity error having occurred during the memory read or write operation [FIGs. 4A, 4B; ¶0062, 0067, 0072, 0109: *ECC mode signal source coupled to selection input of multiplexers and to error logic circuit, the multiplexers having their selection inputs coupled to a source; two open-drain outputs available for reporting an error are driven low;* ¶0072, 0076, 0109: *UE indicates that a parity error occurred*]; and wherein, during an initialization operation, the memory subsystem controller is configured to output via the open train output a signal related to one or more parts of initialization operation sequences [FIGs. 4A, 4B; ¶0062, 0067, 0072, 0109: *ECC mode signal source coupled to selection input of multiplexers and to error logic circuit, the multiplexers having their selection inputs coupled to a source; two open-drain outputs available for reporting an error are driven low;* ¶0072, 0076, 0109: *UE indicates that a parity error occurred*].

Although Hazelzet discloses a test mode in which the controller apply a signal to training sequences [¶0082], Hazelzet does not explicitly disclose during a normal memory read or write operation, the memory subsystem controller is configured to receive address and command signals associated with the memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals.

JEDEC, however, discloses during a normal memory read or write operation, the memory subsystem controller is configured to receive address and command signals associated with the memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals [See JEDEC's Figures 3-4, 3-7, 3-6, 3-9, 3-11, 3-13, 3-14; Pages 14-54: *during the training sequences, JEDEC's memory controller communicates no data with the module and performs no operations to read or write to the memory devices, and that the training is carried out by memory*

buffer (module controller) itself; additionally Hazelzet's memory module can be placed into a training mode to implement JEDEC's training sequences].

It would have been obvious to a POSITA to combine Hazelzet and JEDEC in order to perform multiple functions during multiple operations/modes including initialization/training because such was well known to improve memory module reliability (Pages 14-54).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Emma et al. (9389876) discloses a memory array accessible by a plurality of word lines and bit lines; each memory cell comprises a transistor wherein the transistor has a gate, a source and a drain; Wyatt (2007/0140030) discloses a configuration in which outputs from SO-DIMMs connected via pins of edge connectors using an open drain signal.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARDOCHEE CHERY whose telephone number is (571)272-4246. The examiner can normally be reached from 900-500.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Jared Rutz** can be reached at **(571)272-5535**. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit

https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Respectfully Submitted,
USPTO

Dated: September 28, 2022

By: /MARDOCHEE CHERY/
Primary Examiner
Art Unit 2133
Email:Mardochee.Chery@uspto.gov
Telephone: 571-272-4246
Facsimile: 571-273-4246

Notice of References Cited	Application/Control No. 17/840,593	Applicant(s)/Patent Under Reexamination Lee, Hyun	
	Examiner MARDOCHEE CHERY	Art Unit 2133	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20070140030-A1	06-2007	Wyatt; David A.	G11C5/00	365/212
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N	WO-2004090723-A2	10-2004	WO	BRUCE H	G06F11/1044
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/840,593	Lee, Hyun
	Examiner	Art Unit
	MARDOCHEE CHERY	2133

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant			☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE								
Final	Original	09/28/2022								
	1	✓								

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Ex. 1002, p. 69

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/840,593	Lee, Hyun
	Examiner	Art Unit
	MARDOCHEE CHERY	2133

CPC - Searched*		
Symbol	Date	Examiner
(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254)	09/28/2022	MC

CPC Combination Sets - Searched*		
Symbol	Date	Examiner
(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254)	09/28/2022	MC

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	154	09/28/2022	MC

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
PE2E Search; CPC; Inventor; Assignee	09/28/2022	MC

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	9/28/22

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	9	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/18 02:54 PM
L2	2	L1 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/18 02:55 PM
L3	50	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/18 02:57 PM
L4	3	L3 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/18 02:57 PM
L6	4	"8621170".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/19 06:18 PM
L7	2	("8489837" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/09/03 06:03 PM
L9	54	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:33 PM
L10	3	L9 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:33 PM
L11	1	L10 and (manufactur$3 industry) near3 standard	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:33 PM
L12	1	L10 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:35 PM
L13	9	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:36 PM
L14	5	L13 and	(US-PGPUB; USPAT;	OR	ON	ON	2016/03/02

		@ad<"20090612"	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				05:36 PM
L15	51	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:55 PM
L16	0	L15 and (parity near3 (error signal bit check)) with (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:57 PM
L17	0	L15 and (parity near3 (error signal bit check)) same (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:57 PM
L18	2	L15 and (parity near3 (error signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:57 PM
L19	2	L15 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:57 PM
L20	41	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 12:53 AM
L21	0	L20 and (drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 12:55 AM
L22	2094169	(FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 12:56 AM
L23	1	L20 and (FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 12:56 AM
L24	0	controller near3 (open near2 drain) with (parity ECC) with controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:17 AM
L25	0	controller near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:18 AM
L26	0	(controller hub switch channel) near5 (open	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2016/09/24 01:19 AM

		near2 drain) with (parity ECC) with controller near5 (host computer node engine)	JPO; DERWENT; IBM_TDB)				
L27	0	(controller hub switch channel) with (open near2 drain) with (parity ECC) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:19 AM
L28	0	(controller hub switch channel) with (open near2 drain) with (parity ECC redundancy (correct$3 near2 code)) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:20 AM
L29	47	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:20 AM
L30	0	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) same (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:21 AM
L31	2	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:21 AM
L32	31	L29 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:23 AM
L33	3	L32 and (parity ECC redundancy error (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:24 AM
L34	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2016/11/14 11:55 AM

		"6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.					
L35	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2016/11/14 11:57 AM
L36	3	mardochee and filter near3 snoop	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2016/11/14 11:59 AM
L37	71	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:00 PM
L38	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:06 PM
L39	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:08 PM
L40	2	L37 and edg$3 near5 (wire port connect$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2016/11/14 12:09 PM

		attach$5 bond$3 drain source gate pin) near5 ($3RAM DIM DIMM SODIMM)	JPO; DERWENT; IBM_TDB)				
L41	3	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:12 PM
L42	2	L41 and (error fault ECC)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:13 PM
L43	2	L41 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:13 PM
L44	2	L43 and (transistor $3FET drain$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:14 PM
L45	2	L43 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:15 PM
L46	2	L45 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:31 PM
L47	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:32 PM
L48	2	L47 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:32 PM
L49	1	L47 and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:35 PM
L50	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/05/24 02:13 PM

L51	3	"20060062047".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/05/24 02:41 PM
L52	27512	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:09 PM
L53	44	L52 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:11 PM
L54	0	L53 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:12 PM
L55	0	L53 and (controller hub switch channel) same (open$3 near2 drain) same controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:13 PM
L56	23	L53 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:13 PM
L57	14	L56 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:14 PM
L58	11	L56 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:19 PM
L60	5	("20060262586" "20060062047").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/29 12:37 AM
L61	14	("9858218" "9311116" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2018/08/22 05:23 PM

			IBM_TDB)				
L62	0	L61 and edge near3 connect$3 near5 ("not" "don't" "doesn't") near2 (active activat$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:31 PM
L63	14	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:32 PM
L64	78	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:32 PM
L65	66	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:32 PM
L66	6	L65 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:32 PM
L67	53	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:33 PM
L68	4	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:33 PM
L69	29963	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:34 PM
L70	48	L69 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:34 PM

		controller)					
L71	24	L70 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:34 PM
L72	12	L71 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:34 PM
L74	142	("3414781" "3560935" "4672570" "5388074" "5438536" "5511152" "5450576" "5606662" "5684979" "5835733" "6693840" "6754787" "6763437" "6886109" "7024518" "7065688" "7093115" "7155579" "7221699" "7266633" "7489163" "7525860" "7539909" "7568130" "7586350" "7647467" "7757101" "8074034" "8139430" "8359521" "8429493" "20030115427" "20050071580" "20050193161" "200600062047" "20060262586" "20070091702" "20070136523" "20070214347" "20080098277" "20080147897" "20080155378" "20080256281" "20090119464" "20100005218" "20100042778" "20100142383" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/03/15 01:19 PM
L75	7	L74 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/03/15 01:19 PM
L76	714	"2" and edg$3 near5	(US-PGPUB; USPAT;	OR	ON	ON	2019/03/15

		(wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				01:20 PM
L77	4	L74 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/03/15 01:20 PM
L78	6	L75 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/03/15 01:20 PM
L79	138210	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:42 PM
L80	4275	L79 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:42 PM
L81	30	L80 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:44 PM

		SODIMM) same (controller microcontroller micro-controller)					
L82	15	L81 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:45 PM
L83	1	L82 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:45 PM
L84	0	L83 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:46 PM
L85	1	L82 and (handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:46 PM
L86	4	L82 and (FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:47 PM
L87	2	L86 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:48 PM
L88	2	L87 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:52 PM
L89	48967	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:54 PM
L90	18643	L89 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:54 PM
L91	8	L90 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:55 PM

L92	0	L91 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:56 PM
L95	2	"6798891".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/11 12:39 PM
L96	36607	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L97	55	L96 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L98	25	L97 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L99	13	L98 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L100	162327	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM

		G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.					
L101	5271	L100 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L102	31	L101 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L103	15	L102 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L104	1	L103 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L105	0	L104 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L106	52734	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:26 PM
L107	18670	L106 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:26 PM
L108	8	L107 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:26 PM

		controller) and drain$3					
L109	0	L108 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:26 PM
L110	162327	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2029/4402 or G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:29 PM
L111	5271	L110 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:32 PM
L112	31	L111 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:32 PM
L113	6	L112 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:34 PM
L114	211	netlist.as.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2020/08/30 08:35 PM

			IBM_TDB)				
L115	6	L114 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:35 PM
L116	1	L115 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:36 PM
L117	3	"20080098277".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 09:06 PM
L118	2	L117 and (transistor mosfet fet (discrete near2 element) source drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 09:53 PM
L119	0	L117 and (transistor mosfet fet (discrete near2 element) source drain gate) with (controller) with (parity error)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 09:55 PM
L120	1	L117 and (train$3 test$3 diagnosys sampl$3) near5 (signal input$4 output$4 sequence series operation command read$3 writ$4)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 10:23 PM
L121	1	L117 and (train$3 test$3 diagnosys sampl$3) near5 (mode signal input$4 output$4 sequence series operation command read$3 writ$4) with (transistor mosfet fet (discrete near2 element) source drain gate memory)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 10:26 PM
L122	0	L117 and (low near5 state)	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2021/02/20 11:05 PM

			JPO; DERWENT; IBM_TDB)				
L123	1	L117 and (low high) near5 (pull$3 state level impedance)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:06 PM
L124	1	L117 and edge	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:21 PM
L125	0	L117 and (edge pin connector) near5 (first primary second$3) near5 (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:23 PM
L126	0	L117 and (edge pin connector) near5 (first primary second$3) with (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:23 PM
L127	1	L117 and (edge pin connector) near5 (first primary second$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:23 PM
L128	1	L117 and (edge pin connector contact) with (active inactive enabl$3 disabl$3 off on)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:26 PM
L139	35	("20060277355"|"7411862"|"20030115427"|"20050071580"|"3414781"|"3560935"|"4672570"|"5388074"|"5438536"|"5450576"|"5511152"|"5606662"|"5684979"|"5835733"|"6693840"|"6754787"|"6763437"|"6886109"|"7024518"|"7065688"|"7093115"|"7155579"|"7221699"|"7266633"|"7489163"|"7525860"|"7539909"|"7568130"|"7586350"|"7647467"|"7757101"|"8074034"|"8139430"|"8359521"|"8429493").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2022/02/12 02:59 PM
L140	2	L139 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:00 PM
L141	0	L140 and controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:01 PM
L142	101	(handshak$3 hand-	(US-PGPUB; USPAT;	OR	ON	ON	2022/02/12

		shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				03:18 PM
L143	13	L142 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:18 PM
L144	12	L143 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:19 PM
L145	4	L144 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:20 PM
L146	4	L145 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:21 PM
L147	4	L146 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:21 PM
L148	1	L147 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:26 PM
L149	304352	(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:04 PM

		G11C2029/4402 OR G11C2207/2254).cpc.					
L150	99	((("NETLIST") near3 ("INC"))).AS,AANM.	(USPAT)	OR	ON	ON	2022/09/28 06:05 PM
L151	406	((("NETLIST") near3 ("INC"))).AS,AANM.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:05 PM
L152	14962	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/28 06:06 PM
L153	107524	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:06 PM
L154	373	L149 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:07 PM
L155	14	L151 AND edg$3 near5	(US-PGPUB; USPAT;	OR	ON	ON	2022/09/28

		(wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				06:07 PM
L156	2	L153 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:07 PM
L157	381	154 155 156	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:07 PM
L158	15	L157 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO,	OR	ON	ON	2022/09/28 06:08 PM

			NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L159	15	L158 AND (transistor $3FET drain$3) SAME (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:08 PM
L160	3	L159 AND @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:09 PM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N8	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational	(USPAT)	SAME	ON	ON	2016/02/18 12:10 AM

		mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.					
N59	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.	(USPAT)	SAME	ON	ON	2017/09/28 04:08 PM
N73	3	("9858218" "9311116" "8489837").pn.	(USPAT)	OR	ON	ON	2018/08/22 05:23 PM
N93	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification	(USPAT)	SAME	ON	ON	2019/08/05 02:40 PM

		circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.					
N94	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.	(USPAT)	SAME	ON	ON	2019/08/05 02:40 PM
N129	0	"20080098277".pn.	(USPAT)	OR	ON	ON	2021/02/20 09:05 PM
N130	1	(output$4 issu$3 broadcast$3) near5 (parity near3 error) with (output$4 issu$3 broadcast$3) near5 (train$3) with (open near3 (drain gate source transistor))	(USPAT)	OR	ON	ON	2021/09/10 08:58 PM
N131	1	(output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) same (output$4 issu$3 broadcast$3) near5 (train$3 test$3) near4 (signal operation code instruction) same ((open$3 clos$3 shun$4) near3 (drain gate source transistor))	(USPAT)	OR	ON	ON	2021/09/10 09:03 PM
N132	148	(send$3 sent receiv$3 deliver$3 output$4	(USPAT)	OR	ON	ON	2021/09/10 09:10 PM

		issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) and (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) and ((open$3 clos$3 shun$4) near3 (drain gate source transistor))					
N133	145	N132 and @ad<"20090612"	(USPAT)	OR	ON	ON	2021/09/10 09:13 PM
N134	4	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) and (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) and ("same") near3 ((open$3 clos$3 shun$4) near3 (drain gate source transistor))	(USPAT)	OR	ON	ON	2021/09/10 09:14 PM
N135	4	N134 and @ad<"20090612"	(USPAT)	OR	ON	ON	2021/09/10 09:15 PM
N136	124	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) and (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) and ("same") near3 ((drain gate source transistor))	(USPAT)	OR	ON	ON	2021/09/10 09:15 PM
N137	121	N136 and @ad<"20090612"	(USPAT)	OR	ON	ON	2021/09/10 09:17 PM
N138	0	(send$3 sent receiv$3	(USPAT)	OR	ON	ON	2021/09/10

		deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) same (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) same ("same") near3 ((drain gate source transistor))					09:20 PM
N149	0	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) same (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) same ("same") near3 ((drain gate source transistor))	(USPAT)	OR	ON	ON	2022/02/12 02:59 PM

PE2E SEARCH - Search History (Similarity Search)

No Similarity Results available

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/840,593	06/14/2022	Hyun Lee	NL066-13US02

CONFIRMATION NO. 3678

79141
USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

PUBLICATION NOTICE

OC00000136950028

Title:MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

Publication No.US-2022-0382693-A1
Publication Date:12/01/2022

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/840,593	Filing Date 06/14/2022	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	04/05/2023	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/VERNON A TOWLER/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronically filed April 5, 2023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3678
Serial No.:	17/840,593	Group Art Unit:	2133
Filed:	June 14, 2022	Examiner:	Mardochee CHERY
For:	*MEMORY SUBSYSTEM HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION*	Attorney Docket No.:	NL066-13US02

RESPONSE TO NON-FINAL OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Non-Final Office Action dated October 5, 2022, for the above identified patent application.

Applicant petitions for a three-month extension of time, which extends the due date for responding to the Office Action from January 5, 2023, to April 5, 2023.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. NL066-13US02).

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Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory subsystem operable with a system memory controller of a host system, comprising:

dynamic random access memory elements on a printed circuit board and configurable to communicate data signals with the system memory controller; and

a memory subsystem controller on the printed circuit board and coupled to the dynamic random access memory elements, the memory subsystem controller having an open drain output, wherein the memory subsystem is configured to provide a first signaling interface via the open drain output during normal operations and a second signaling interface via the open drain output during an initialization operation including initialization operation sequences, wherein the second signaling interface is distinct from the first signaling interface and the initialization operation is distinct from any of the normal operations;

wherein, during [[~~a~~]]the normal memory read or write operations, the memory subsystem controller is configured to receive address and command signals associated with the memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals, and the memory subsystem controller is further configured to output via the open drain output a parity error signal in response to a parity error having occurred during the normal memory read or write operations; and

wherein, during [[~~an~~]]the initialization operation, the memory subsystem controller is configured to output via the open ~~train~~ drain output a signal related to one or more parts of the initialization operation sequences.

2. (New) The memory subsystem of claim 1, wherein

the memory subsystem controller includes a transistor having an open drain coupled to the open drain output, a source coupled to ground, and a gate;

wherein the memory subsystem controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred during the normal memory read or write operations; and

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wherein the memory subsystem controller is further configurable to apply a second signal related to one or more parts of the initialization operation sequences to the gate of the transistor during the initialization operation.

3. (New) The memory subsystem of claim 2, wherein the second signal drives the open drain output from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

4. (New) The memory subsystem of claim 3, wherein the second signal drives the open drain output from the high impedance state to the low logic level and from the low logic level to the high impedance state.

5. (New) The memory subsystem of claim 3, wherein the second signal drives the gate of the transistor high so as to drive the open drain output to the low logic level, and drives the gate of the transistor low so as to drive the open drain output to the high impedance state.

6. (New) The memory subsystem of claim 5, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the open drain output and ground.

7. (New) The memory subsystem of claim 2, wherein the memory subsystem controller comprises an integrated circuit that includes the transistor.

8. (New) The memory subsystem of claim 2, wherein the memory subsystem controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the memory subsystem controller is configurable to couple the first input to the output during the normal memory read or write operations, and to couple the second input to the output during the initialization operation.

9. (New) The memory subsystem of claim 1, wherein the dynamic random access memory elements are not accessed for any normal memory read or write operations by the system memory controller during the initialization operation.

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10. (New) The memory subsystem of claim 1, wherein the printed circuit board has edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the system memory controller, the edge connections including first edge connections via which the memory subsystem communicates data with the system memory controller, second edge connections via which the memory subsystem receives command/address signals from the system memory controller, and an open drain output pin coupled to the open drain output.

11. (New) A method of operation in a host system having a system memory controller, comprising:

at a memory subsystem coupled to the system memory controller, the memory subsystem including a printed circuit board, a memory subsystem controller on the printed circuit board, and dynamic random access memory elements on the printed circuit board, the memory subsystem controller having an open drain output, wherein the memory subsystem is configured to provide a first signaling interface via the open drain output during normal operations and a second signaling interface via the open drain output during an initialization operation including initialization operation sequences, wherein the second signaling interface is distinct from the first signaling interface and the initialization operation is distinct from any of the normal operations,

performing the normal memory read or write operations, including receiving address and command signals associated with the memory read or write operations, controlling the dynamic random access memory elements in accordance with the address and command signals, and outputting via the open drain output a parity error signal in response to a parity error having occurred during the normal memory read or write operations; and

performing the initialization operation, including outputting via the open drain output a signal related to one or more parts of the initialization operation sequences.

12. (New) The method of claim 11, wherein

the memory subsystem controller includes a transistor having an open drain coupled to the open drain output, a source coupled to ground, and a gate;

outputting via the open drain output a parity error signal includes applying a first signal to the gate of the transistor to indicate the parity error having occurred during the normal memory read or write operations; and

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outputting via the open drain a signal related to one or more parts of the initialization operation sequences includes applying a second signal related to the one or more training sequences to the gate of the transistor during the initialization operation.

13. (New) The method of claim 12, wherein the open drain output is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

14. (New) The method of claim 12, wherein the open drain output is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state.

15. (New) The method of claim 12, wherein the second signal drives the gate of the transistor high so as to drive the open drain output to the low logic level, and drives the gate of the transistor low so as to drive the open drain output to the high impedance state.

16. (New) The method of claim 15, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the open drain output and ground.

17. (New) The method of claim 12, wherein the memory subsystem controller comprises an integrated circuit that includes the transistor.

18. (New) The method of claim 12, wherein the memory subsystem controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, the method further comprising coupling the first input to the output during the normal memory read or write operations, and coupling the second input to the output during the initialization operation.

19. (New) The method of claim 11, wherein the dynamic random access memory elements are not accessed for any normal memory read or write operations by the system memory controller during the initialization operation.

20. (New) The method of claim 11, wherein the printed circuit board has edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with

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the system memory controller, the edge connections including first edge connections via which the memory subsystem communicates data with the system memory controller, second edge connections via which the memory subsystem receives command/address signals from the system memory controller, and an open drain output pin coupled to the open drain output.

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REMARKS

This amendment responds to the Office Action dated October 5, 2021. In the Office Action, the Examiner:

- objected to claim 1 because of informalities;
- rejected claim 1 on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 11386024; claims 1-24 of U.S. Patent No. 10474595; claims 1-20 of U.S. Patent No. 9311116; and claims 1-18 of U.S. Patent No. 8489837; and
- rejected claim 1 under 35 U.S.C. 103(a) as being unpatentable over Hazelzet (US 20080098277 cited in IDS of 09/02/2020, hereafter "Hazelzet") and JEDEC (cited in IDS of 09/02/2020).

REMARKS CONCERNING CLAIMS

Claim 1 has been amended.

New claims 2-20 are added. Support for the amendments and the new claims can be found throughout the specification as filed with reference to the drawings as filed.

No new matter has been added.

With respect to all amendments, Applicant has not dedicated or abandoned any unclaimed subject matter. Moreover, Applicant has not acquiesced to any characterizations of the invention, nor any rejections or objections of the claims, made by the Examiner. Moreover, the Applicant hereby rescinds any prior disclaimer of claim scope, to the extent they exist, made during the prosecution of this application or made during the prosecution of any patent or other related patents/applications, and advises the Examiner that any such previous disclaimers and the cited references that they were made to avoid may need to be revisited.

After entry of this amendment, the pending claims are: claims 1-20.

REMARKS CONCERNING CLAIM OBJECTIONS

Claim 1 is objected to because of a typographical error in line 13 of the original claim 1, where the phrase "open drain" is erroneously written as "open train." This error has been corrected in the amendments, and withdrawal of the objection is thus respectfully requested.

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REMARKS CONCERNING DOUBLE PATENTING REJECTIONS

The original claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 11386024; claims 1-24 of U.S. Patent No. 10474595; claims 1-20 of U.S. Patent No. 9311116; and claims 1-18 of U.S. Patent No. 8489837.

Applicant believes that the amendments in claim 1 overcome the above double-patenting rejections because claim 1 as amended recite limitations not found in any of claims 1-20 of U.S. Patent No. 11386024; claims 1-24 of U.S. Patent No. 10474595; claims 1-20 of U.S. Patent No. 9311116; and claims 1-18 of U.S. Patent No. 8489837. Therefore, Applicant respectfully requests withdrawal of the rejections or that these rejections be held in abeyance until at least one claim is found to be allowable.

REMARKS CONCERNING REJECTIONS UNDER 35 U.S.C. 103(A)

In rejecting original claim 1 under 35 U.S.C. 103(a) over Hazelzet in view of JEDEC, the Office Action alleges that Hazelzet teaches, in FIGs. 4A, 4B; ¶0062, 0067, 0072, 0109:

> "wherein . . . the memory subsystem controller is further configured to output via the open drain output a parity error signal in response to a parity error having occurred during the memory read or write operation."

The Office Action then alleges that Hazelzet further teaches, also in in FIGs. 4A, 4B; ¶0062, 0067, 0072, 0109:

> "wherein, during an initialization operation, the memory subsystem controller is configured to output via the open train output a signal related to one or more parts of initialization operation sequences."

Applicant respectfully disagrees.

Hazelzet describes a registered DIMM (or RDIMM) with error detection capabilities and error reporting using two open drain outputs. Although Hazelzet mentions a test mode [¶0082], Hazelzet does not teach or suggest signaling using any of the two open drain outputs during the test mode. In fact, Hazelzet does not output any signals via the open drain outputs in any operation other than normal memory read or write operations, or for any purpose other than

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reporting errors during the normal memory read or write operations. As described in Hazelzet ¶0072:

> Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during **a valid command (/CS=low) cycle** (consistent with the re-driven signals). These two outputs are driven low for two clocks to allow the memory controller time to sense the error. /Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic, /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error. Note that the timing of/Error (UE) is different in parity mode vs. ECC mode.

Thus, Hazelzet is clear in ¶0072 that, for both the parity mode and the ECC mode, the error reporting is performed during a normal memory operation corresponding to **a valid command (/CS=low) cycle**. This is also made clear throughout Hazelzet. For example, Hazelzet describes, in ¶0018:

> "Still another object of the invention is to provide for Parity error reporting in which the parity signal is delivered one cycle **after the address and command** to which it applies, and the error line be driven low two clocks **after the address and command bits are driven to the DRAMs** from the register on the DIMM."

Thus, the parity error reporting occurs during normal memory operations when address and command bits are driven to the DRAMs from the register on the DIMM. Further, Hazelzet describes, in ¶0059:

> "When either error line (CE) 109 or uncorrectable error line (UE) 110 is low this indicates that an error was identified as being **associated with the address and/or command inputs** (either correctable or uncorrectable). The error lines 120,121 will be active, i.e., low, for two clock cycles simultaneous **with the re-driven address/command data** when operating in ECC mode or delayed by two clock cycles when operating in parity mode."

In other words, whether for correctable or uncorrectable errors, and whether operating in ECC mode or parity mode, the errors reported via the correctable error line (CE) 109 and/or

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uncorrectable error line (UE) 110 are associated with the address and/or command inputs, which are active during normal memory read or write operations.

Therefore, Hazelzet does not teach or suggest "wherein the memory subsystem is configured to provide a first signaling interface via the open drain output during normal operations and a second signaling interface via the open drain output during an initialization operation including initialization operation sequences, wherein the second signaling interface is distinct from the first signaling interface and the initialization operation is distinct from any of the normal operations," as recited in claim 1 as amended.

Furthermore, Hazelzet does not teach or suggest signaling using any of its open-drain output, ERROR (CE) and ERROR (UE), in any operation other than normal memory read or write operations. Therefore, Hazelzet does not teach or suggest "wherein, during the initialization operation (which is distinct from any of the normal memory read or write operations according to claim 1), the memory subsystem controller is configured to output via the open train output a signal related to one or more parts of the initialization operation sequences," as further recited in claim 1 as amended.

JEDEC does not make up for the above deficiencies of Hazelzet.

Therefore, claim 1 as amended is not a combination of of know elements found in Hazelzet and JEDEC, and is thus patentable over Hazelzet in view of JEDEC.

Claims 2-10 depend from claim 1 as amended and include further limitations in addition to the limitations in claim 1 as amended. Therefore, claims 2-10 are patentable for at least analogous reasons claim 1 as amended is patentable.

The above arguments regarding claim 1 as amended apply to claim 11 as amended. Therefore, claim 11 as amended is also patentable over Hazelzet in view of JEDEC.

Claims 12-20 depend from claim 11 and include further limitations in addition to the limitations in claim 11. Therefore, claims 12-20 are patentable for at least analogous reasons claim 11 as amended is patentable.

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Withdrawal of the rejections under pre-AIA 35 U.S.C. 103(a) is therefore respectfully requested.

CONCLUDING REMARKS

By responding in the foregoing remarks only to particular positions asserted by the examiner, the Applicant does not necessarily acquiesce in other positions that have not been explicitly addressed. In addition, the Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: April 5, 2023

/Jamie J. Zheng/ 51,167
Jamie J. Zheng (Reg. No.)
Customer No. 79141

Samsung Electronics Co., Ltd.
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UNITED STATES
PATENT AND TRADEMARK OFFICE

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Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/840,593	**04/05/2023 10:24:41 PM ET**	**NL066-13US02**

Title of Invention

MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3678	FILED BY	Jamie Zheng
PATENT CENTER #	61874972	FILING DATE	06/14/2022
CUSTOMER #	79141	FIRST NAMED INVENTOR	Hyun Lee
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 5

DOCUMENT		PAGES	DESCRIPTION	SIZE (KB)
NL066-13US02_USPTO_AIA82_20230405.pdf		4	Power of Attorney	322 KB
POA_Netlist_General.pdf		1	Power of Attorney	148 KB
NL066-13US02_Amendment_NFOA.pdf		11	-	206 KB
NL066-13US02_Amendment_NFOA-A....pdf	(1-1)	1	Amendment/Request for Reconsideration-After Non-Final Rejection	113 KB

NL066-13US02_Amendment_NFOA-CLM.pdf	(2-6)	5	Claims	113 KB
NL066-13US02_Amendment_NFOA-REM.pdf	(7-11)	5	Applicant Arguments/Remarks Made in an Amendment	171 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
NL066-13US02_USPTO_AIA82_20230405.pdf	2CE7F80AA657EDF855E3DC2AAD67925506C0574ED5DEF8E2487410C1675F7AFE281CEF1BEAA50C5B6663BFA04DA3D61DFF662F1E2F550AB4F5FC65F929E4004E
POA_Netlist_General.pdf	2FE78DEA6BFC66E618E33621B66BCD5F24F333C1612D21DF6B8DBA7009D1F9DDD58002B66344E58D142B8D92DC2AE1AE10947C3B63049EDE034C10A82BA4F3DB
NL066-13US02_Amendment_NFOA.pdf	91BF0E9CBCB0FBF92A612CB5E35DC25610F632DE792D8489489A9F106C509F0238B6DE609A5C62B3901AD7D24E4F8AF2766D79733DC1F24FA4EFCCD37E50D904
NL066-13US02_Amendment_NFOA-A....pdf	0B8D6AE6CBF7C5272EFB38AC3BAF93D49C65D010B02969EB1F5F3E21C8DFC91CD820AE6E735ACF1DC73E2D5C961F1A64B6389C6BA3D09127C8FC69BE30AC704E
NL066-13US02_Amendment_NFOA-CLM.pdf	C2A7E47A12AEA74DD0731D35257401009C059512E485C6F504F3C5FFC534F07B3C362E52D5B9199D7B483902999C660A3956CAF9AA06F8A295802B6C09F2BA88
NL066-13US02_Amendment_NFOA-REM.pdf	AE051FB313EAA0043EFF909245BA9DFF41B0721EB3C1D734F0470119E1E20E3412721F476B7E7149B37E7EC9B3EA38E65AD0F21D99FD5FE84F691CF103F46F49

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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Doc Code: PA..
Document Description: Power of Attorney

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Application Number	17/840,593
Filing Date	2022-06-14
First Named Inventor	Hyun LEE
Title	MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION
Art Unit	2133
Examiner Name	Mardochee CHERY
Attorney Docket Number	NL066-13US02

SIGNATURE of Applicant or Patent Practitioner

Signature	/Jamie J. Zheng/	Date (Optional)	2023-04-05
Name	Jamie J. Zheng	Registration Number	51167
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)	Netlist, Inc.		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ *Total of _____ forms are submitted.

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Application Number	Filing Date
17/840,593	2022-06-14

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I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Netlist, Inc.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

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SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	2023-04-05
Name	Hyun LEE		
Title			

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

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☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

■ Assignee or Person to Whom the Inventor is Under an Obligation to Assign

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is currently being filed in this document)

SIGNATURE of Applicant for Patent

Signature		Date: January 9, 2013
Name	**Gail Sasaki**	
Title	Vice President and Chief Financial Officer	
Company	Netlist, Inc.	

Note: Signature - this form must be signed by the Applicant or a person authorized to act on behalf of Applicant.

Submit multiple forms for more than one signature
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Electronic Patent Application Fee Transmittal

Application Number:	17840593
Filing Date:	14-Jun-2022
Title of Invention:	MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NL066-13US02

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 3 months with $0 paid	1253	1	1480	1480
Miscellaneous:				
			Total in USD ($)	**1480**

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EFS ID:	47799734
Application Number:	17840593
International Application Number:	
Confirmation Number:	3678
Title of Invention:	MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NL066-13US02
Receipt Date:	05-APR-2023
Filing Date:	14-JUN-2022
Time Stamp:	23:04:51
Application Type:	Utility under 35 USC 111(a)

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Payment Type	CARD
Payment was successfully received in RAM	$1480
RAM confirmation Number	E202345N05366000
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1	Fee Worksheet (SB06)	fee-info.pdf	38439 4302f2a5b234f70c1a5e17d34b43bcbe2726d603	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	38439		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/840,593	06/14/2022	Hyun Lee	NL066-13US02

CONFIRMATION NO. 3678

79141
USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

POA ACCEPTANCE LETTER

OC000000137741953

Date Mailed: 04/14/2023

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 04/05/2023.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/sleutchit/

Samsung Electronics Co., Ltd.
Ex. 1002, p. 119

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 05/03/2023

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER
CHERY, MARDOCHEE

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/03/2023

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/840,593	06/14/2022	Hyun Lee	NL066-13US02	3678

TITLE OF INVENTION: MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	08/03/2023

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

Samsung Electronics Co., Ltd.
Ex. 1002, p. 120

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 05/03/2023

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/840,593	06/14/2022	Hyun Lee	NL066-13US02	3678

TITLE OF INVENTION: MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	08/03/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHERY, MARDOCHEE	2133	711-154000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required)

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via Patent Center or EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Samsung Electronics Co., Ltd.
Ex. 1002, p. 121

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/840,593	06/14/2022	Hyun Lee	NL066-13US02	3678

79141 7590 05/03/2023

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER	
CHERY, MARDOCHEE	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/03/2023

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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Ex. 1002, p. 122

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Samsung Electronics Co., Ltd.
Ex. 1002, p. 123

Notice of Allowability	Application No. 17/840,593	Applicant(s) Lee, Hyun	
	Examiner MARDOCHEE CHERY	Art Unit 2133	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 04/14/2023.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-20 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	04/22/2023

Samsung Electronics Co., Ltd.
Ex. 1002, p. 124

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/840,593	Lee, Hyun
	Examiner	**Art Unit**
	MARDOCHEE CHERY	2133

CPC						
Symbol					**Type**	**Version**
G06F	/	13	/	1694	F	2013-01-01
G11C	/	5	/	04	I	2013-01-01
G11C	/	7	/	1063	I	2013-01-01
G06F	/	13	/	1668	I	2013-01-01
G06F	/	9	/	445	I	2013-01-01
G06F	/	13	/	24	I	2013-01-01
G06F	/	3	/	0619	I	2013-01-01
G06F	/	3	/	0632	I	2013-01-01
G06F	/	3	/	0659	I	2013-01-01
G06F	/	3	/	0673	I	2013-01-01
G06F	/	11	/	1068	I	2013-01-01
G11C	/	29	/	52	I	2013-01-01
G06F	/	12	/	0646	I	2013-01-01
G11C	/	2207	/	2254	A	2013-01-01
G11C	/	5	/	00	A	2013-01-01
G11C	/	7	/	1066	A	2013-01-01
G11C	/	16	/	26	A	2013-01-01
G11C	/	29	/	78	A	2013-01-01
G11C	/	2029	/	4402	A	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	22 April 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

U.S. Patent and Trademark Office

Part of Paper No.: 20230407

Samsung Electronics Co., Ltd.
Ex. 1002, p. 125

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/840,593	Lee, Hyun
	Examiner	**Art Unit**
	MARDOCHEE CHERY	2133

INTERNATIONAL CLASSIFICATION					
CLAIMED					
G06F	/	12	/	00	
NON-CLAIMED					
	/		/		

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
711	154

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE (Assistant Examiner) (Date)	**Total Claims Allowed:** 20	
/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133 (Primary Examiner) 22 April 2023 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3

Samsung Electronics Co., Ltd.
Ex. 1002, p. 126

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/840,593	Lee, Hyun
	Examiner	**Art Unit**
	MARDOCHEE CHERY	2133

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10		19										
	2		11		20										
	3		12												
	4		13												
	5		14												
	6		15												
	7		16												
	8		17												
	9		18												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	22 April 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

U.S. Patent and Trademark Office

Part of Paper No.: 20230407

Samsung Electronics Co., Ltd.
Ex. 1002, p. 127

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/840,593	Lee, Hyun
	Examiner	Art Unit
	MARDOCHEE CHERY	2133

CPC - Searched*		
Symbol	Date	Examiner
(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254)	09/28/2022	MC

CPC Combination Sets - Searched*		
Symbol	Date	Examiner
(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254)	09/28/2022	MC

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	154	09/28/2022	MC

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
PE2E Search; CPC; Inventor; Assignee	09/28/2022	MC
PE2E; CPC	04/22/2023	MC

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	4/22/23

Samsung Electronics Co., Ltd.
Ex. 1002, p. 128

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/840,593	Lee, Hyun
	Examiner	Art Unit
	MARDOCHEE CHERY	2133

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	See Attached	04/22/2023	MC

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	4/22/23

Samsung Electronics Co., Ltd.
Ex. 1002, p. 129

Bibliographic Data

Application No: 17/840,593

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /MARDOCHEE CHERY/ Examiner's Signature | Initials

Title: MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
06/14/2022	711	2133	NL066-13US02
RULE			

APPLICANTS

Netlist, Inc., Irvine, CA,

INVENTORS

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CONTINUING DATA

This application is a CON of 16680060 11/11/2019 PAT 11386024

16680060 is a CON of 15857553 12/28/2017 PAT 10474595

15857553 is a CON of 15088155 04/01/2016 PAT 9667001

15088155 is a CON of 13942721 07/16/2013 PAT 9311116

13942721 is a CON of 12815339 06/14/2010 PAT 8489837

12815339 has PRO of 61186799 06/12/2009

FOREIGN APPLICATIONS

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06/21/2022

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	9	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/18 02:54 PM
L2	2	L1 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/18 02:55 PM
L3	50	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/18 02:57 PM
L4	3	L3 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/18 02:57 PM
L6	4	"8621170".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/19 06:18 PM
L7	2	("8489837" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/09/03 06:03 PM
L9	54	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:33 PM
L10	3	L9 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:33 PM
L11	1	L10 and (manufactur$3 industry) near3 standard	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:33 PM
L12	1	L10 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:35 PM
L13	9	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:36 PM
L14	5	L13 and	(US-PGPUB; USPAT;	OR	ON	ON	2016/03/02

		@ad<"20090612"	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				05:36 PM
L15	51	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:55 PM
L16	0	L15 and (parity near3 (error signal bit check)) with (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:57 PM
L17	0	L15 and (parity near3 (error signal bit check)) same (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:57 PM
L18	2	L15 and (parity near3 (error signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:57 PM
L19	2	L15 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:57 PM
L20	41	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 12:53 AM
L21	0	L20 and (drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 12:55 AM
L22	2094169	(FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 12:56 AM
L23	1	L20 and (FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 12:56 AM
L24	0	controller near3 (open near2 drain) with (parity ECC) with controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:17 AM
L25	0	controller near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:18 AM
L26	0	(controller hub switch channel) near5 (open	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2016/09/24 01:19 AM

		near2 drain) with (parity ECC) with controller near5 (host computer node engine)	JPO; DERWENT; IBM_TDB)				
L27	0	(controller hub switch channel) with (open near2 drain) with (parity ECC) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:19 AM
L28	0	(controller hub switch channel) with (open near2 drain) with (parity ECC redundancy (correct$3 near2 code)) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:20 AM
L29	47	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:20 AM
L30	0	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) same (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:21 AM
L31	2	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:21 AM
L32	31	L29 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:23 AM
L33	3	L32 and (parity ECC redundancy error (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:24 AM
L34	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2016/11/14 11:55 AM

		"6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.					
L35	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2016/11/14 11:57 AM
L36	3	mardochee and filter near3 snoop	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2016/11/14 11:59 AM
L37	71	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:00 PM
L38	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:06 PM
L39	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:08 PM
L40	2	L37 and edg$3 near5 (wire port connect$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2016/11/14 12:09 PM

		attach$5 bond$3 drain source gate pin) near5 ($3RAM DIM DIMM SODIMM)	JPO; DERWENT; IBM_TDB)				
L41	3	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:12 PM
L42	2	L41 and (error fault ECC)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:13 PM
L43	2	L41 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:13 PM
L44	2	L43 and (transistor $3FET drain$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:14 PM
L45	2	L43 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:15 PM
L46	2	L45 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:31 PM
L47	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:32 PM
L48	2	L47 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:32 PM
L49	1	L47 and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:35 PM
L50	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/05/24 02:13 PM

L51	3	"20060062047".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/05/24 02:41 PM
L52	27512	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:09 PM
L53	44	L52 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:11 PM
L54	0	L53 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:12 PM
L55	0	L53 and (controller hub switch channel) same (open$3 near2 drain) same controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:13 PM
L56	23	L53 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:13 PM
L57	14	L56 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:14 PM
L58	11	L56 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:19 PM
L60	5	("20060262586" "20060062047").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/29 12:37 AM
L61	14	("9858218" "9311116" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2018/08/22 05:23 PM

			IBM_TDB)				
L62	0	L61 and edge near3 connect$3 near5 ("not" "don't" "doesn't") near2 (active activat$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:31 PM
L63	14	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:32 PM
L64	78	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:32 PM
L65	66	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:32 PM
L66	6	L65 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:32 PM
L67	53	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:33 PM
L68	4	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:33 PM
L69	29963	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:34 PM
L70	48	L69 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:34 PM

		controller)					
L71	24	L70 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:34 PM
L72	12	L71 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:34 PM
L74	142	("3414781" "3560935" "4672570" "5388074" "5438536" "5511152" "5450576" "5606662" "5684979" "5835733" "6693840" "6754787" "6763437" "6886109" "7024518" "7065688" "7093115" "7155579" "7221699" "7266633" "7489163" "7525860" "7539909" "7568130" "7586350" "7647467" "7757101" "8074034" "8139430" "8359521" "8429493" "20030115427" "20050071580" "20050193161" "200600062047" "20060262586" "20070091702" "20070136523" "20070214347" "20080098277" "20080147897" "20080155378" "20080256281" "20090119464" "20100005218" "20100042778" "20100142383" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/03/15 01:19 PM
L75	7	L74 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/03/15 01:19 PM
L76	714	"2" and edg$3 near5	(US-PGPUB; USPAT;	OR	ON	ON	2019/03/15

		(wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				01:20 PM
L77	4	L74 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/03/15 01:20 PM
L78	6	L75 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/03/15 01:20 PM
L79	138210	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:42 PM
L80	4275	L79 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:42 PM
L81	30	L80 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:44 PM

		SODIMM) same (controller microcontroller micro-controller)					
L82	15	L81 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:45 PM
L83	1	L82 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:45 PM
L84	0	L83 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:46 PM
L85	1	L82 and (handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:46 PM
L86	4	L82 and (FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:47 PM
L87	2	L86 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:48 PM
L88	2	L87 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:52 PM
L89	48967	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:54 PM
L90	18643	L89 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:54 PM
L91	8	L90 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:55 PM

L92	0	L91 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:56 PM
L95	2	"6798891".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/11 12:39 PM
L96	36607	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L97	55	L96 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L98	25	L97 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L99	13	L98 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L100	162327	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM

		G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.					
L101	5271	L100 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L102	31	L101 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L103	15	L102 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L104	1	L103 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L105	0	L104 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L106	52734	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:26 PM
L107	18670	L106 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:26 PM
L108	8	L107 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:26 PM

		controller) and drain$3					
L109	0	L108 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:26 PM
L110	162327	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2029/4402 or G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:29 PM
L111	5271	L110 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:32 PM
L112	31	L111 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:32 PM
L113	6	L112 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:34 PM
L114	211	netlist.as.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2020/08/30 08:35 PM

			IBM_TDB)				
L115	6	L114 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:35 PM
L116	1	L115 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:36 PM
L117	3	"20080098277".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 09:06 PM
L118	2	L117 and (transistor mosfet fet (discrete near2 element) source drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 09:53 PM
L119	0	L117 and (transistor mosfet fet (discrete near2 element) source drain gate) with (controller) with (parity error)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 09:55 PM
L120	1	L117 and (train$3 test$3 diagnosys sampl$3) near5 (signal input$4 output$4 sequence series operation command read$3 writ$4)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 10:23 PM
L121	1	L117 and (train$3 test$3 diagnosys sampl$3) near5 (mode signal input$4 output$4 sequence series operation command read$3 writ$4) with (transistor mosfet fet (discrete near2 element) source drain gate memory)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 10:26 PM
L122	0	L117 and (low near5 state)	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2021/02/20 11:05 PM

			JPO; DERWENT; IBM_TDB)				
L123	1	L117 and (low high) near5 (pull$3 state level impedance)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:06 PM
L124	1	L117 and edge	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:21 PM
L125	0	L117 and (edge pin connector) near5 (first primary second$3) near5 (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:23 PM
L126	0	L117 and (edge pin connector) near5 (first primary second$3) with (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:23 PM
L127	1	L117 and (edge pin connector) near5 (first primary second$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:23 PM
L128	1	L117 and (edge pin connector contact) with (active inactive enabl$3 disabl$3 off on)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:26 PM
L139	35	("20060277355"|"7411862"|"20030115427"|"20050071580"|"3414781"|"3560935"|"4672570"|"5388074"|"5438536"|"5450576"|"5511152"|"5606662"|"5684979"|"5835733"|"6693840"|"6754787"|"6763437"|"6886109"|"7024518"|"7065688"|"7093115"|"7155579"|"7221699"|"7266633"|"7489163"|"7525860"|"7539909"|"7568130"|"7586350"|"7647467"|"7757101"|"8074034"|"8139430"|"8359521"|"8429493").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2022/02/12 02:59 PM
L140	2	L139 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:00 PM
L141	0	L140 and controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:01 PM
L142	101	(handshak$3 hand-	(US-PGPUB; USPAT;	OR	ON	ON	2022/02/12

		shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				03:18 PM
L143	13	L142 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:18 PM
L144	12	L143 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:19 PM
L145	4	L144 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:20 PM
L146	4	L145 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:21 PM
L147	4	L146 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:21 PM
L148	1	L147 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:26 PM
L149	304352	(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:04 PM

		G11C2029/4402 OR G11C2207/2254).cpc.					
L150	99	((("NETLIST") near3 ("INC"))).AS,AANM.	(USPAT)	OR	ON	ON	2022/09/28 06:05 PM
L151	406	((("NETLIST") near3 ("INC"))).AS,AANM.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:05 PM
L152	14962	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/28 06:06 PM
L153	107524	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:06 PM
L154	373	L149 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:07 PM
L155	14	L151 AND edg$3 near5	(US-PGPUB; USPAT;	OR	ON	ON	2022/09/28

		(wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				06:07 PM
L156	2	L153 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:07 PM
L157	381	154 155 156	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:07 PM
L158	15	L157 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO,	OR	ON	ON	2022/09/28 06:08 PM

			NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L159	15	L158 AND (transistor $3FET drain$3) SAME (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:08 PM
L160	3	L159 AND @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:09 PM
L161	33	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L162	15	L1 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L163	84	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L164	18	L3 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L165	2	"8621170".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L166	2	("8489837" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L167	84	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L168	18	L9 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L169	9	L10 and (manufactur$3 industry) near3 standard	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L170	1	L10 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L171	33	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L172	5	L13 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L173	105	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L174	2	L15 and (parity near3 (error signal bit check)) with (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L175	14	L15 and (parity near3 (error signal bit check)) same (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L176	14	L15 and (parity near3 (error signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L177	16	L15 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L178	47	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L179	1	L20 and (drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L180	3234820	(FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L181	1	L20 and (FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L182	2	controller near3 (open near2 drain) with (parity ECC) with controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L183	2	controller near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L184	2	(controller hub switch channel) near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L185	2	(controller hub switch channel) with (open near2 drain) with (parity ECC) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L186	2	(controller hub switch channel) with (open near2 drain) with (parity ECC redundancy (correct$3 near2 code)) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L187	99	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L188	6	(controller hub switch channel) with (open	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/04/22 10:13 PM

		near2 drain) with controller with (host computer node engine) same (parity ECC redundancy (correct$3 near2 code))	JPO; DERWENT; IBM_TDB)				
L189	24	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L190	31	L29 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L191	3	L32 and (parity ECC redundancy error (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L192	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/04/22 10:13 PM
L193	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/04/22 10:13 PM

L194	7	mardochee and filter near3 snoop	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/04/22 10:13 PM
L195	79	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L196	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L197	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L198	2	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) near5 ($3RAM DIM DIMM SODIMM)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L199	2	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L200	2	L41 and (error fault ECC)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L201	2	L41 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L202	2	L43 and (transistor $3FET drain$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/04/22 10:13 PM

			JPO; DERWENT; IBM_TDB)				
L203	2	L43 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L204	2	L45 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L205	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L206	2	L47 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L207	1	L47 and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L208	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L209	3	"20060062047".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L210	47193	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L211	52	L52 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L212	1	L53 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L213	1	L53 and (controller hub switch channel) same (open$3 near2 drain) same controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L214	19	L53 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L215	4	L56 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L216	13	L56 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L217	5	("20060262586" "20060062047").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L218	15	("9858218" "9311116" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L219	0	L61 and edge near3 connect$3 near5 ("not" "don't" "doesn't") near2 (active activat$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L220	33	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L221	84	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L222	105	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L223	16	L65 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L224	99	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L225	24	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L226	47193	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L227	52	L69 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L228	19	L70 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L229	13	L71 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L230	160	("3414781" "3560935" "4672570" "5388074" "5438536" "5511152" "5450576" "5606662" "5684979" "5835733" "6693840" "6754787" "6763437" "6886109" "7024518" "7065688" "7093115" "7155579" "7221699" "7266633" "7489163" "7525860" "7539909" "7568130" "7586350" "7647467" "7757101" "8074034"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

		"8139430" "8359521" "8429493" "20030115427" "20050071580" "20050193161" "200600062047" "20060262586" "20070091702" "20070136523" "20070214347" "20080098277" "20080147897" "20080155378" "20080256281" "20090119464" "20100005218" "20100042778" "20100142383" "20100202240" "20110022789").pn.					
L231	7	L74 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L232	770	"2" and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L233	2	L74 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L234	6	L75 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L235	237657	(G06F13/1694 or G06F12/0646 or G06F3/0619 or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2023/04/22 10:13 PM

		G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	IBM_TDB)				
L236	8346	L79 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L237	33	L80 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L238	16	L81 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L239	1	L82 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L240	0	L83 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L241	1	L82 and (handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L242	2	L82 and (FET MOSFET transistor p-junction n-	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/04/22 10:13 PM

		junction)	JPO; DERWENT; IBM_TDB)				
L243	0	L86 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L244	0	L87 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L245	65380	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L246	18713	L89 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L247	8	L90 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L248	0	L91 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L249	4	"6798891".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L250	47193	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L251	52	L96 and edg$3 near5	(US-PGPUB; USPAT;	OR	ON	ON	2023/04/22

		(wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				10:13 PM
L252	19	L97 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L253	13	L98 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L254	237657	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L255	8346	L100 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L256	33	L101 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L257	16	L102 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L258	1	L103 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L259	0	L104 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L260	65380	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L261	18713	L106 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L262	8	L107 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L263	0	L108 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L264	237657	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

		G11C29/78 or G11C2029/4402 or G11C2207/2254).cpc.					
L265	8346	L110 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L266	33	L111 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L267	4	L112 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L268	249	netlist.as.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L269	9	L114 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L270	1	L115 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L271	3	"20080098277".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L272	2	L117 and (transistor mosfet fet (discrete near2 element) source drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L273	0	L117 and (transistor mosfet fet (discrete near2 element) source drain gate) with (controller) with (parity error)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L274	0	L117 and (train$3 test$3 diagnosys sampl$3) near5 (signal input$4 output$4 sequence series operation command read$3 writ$4)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L275	1	L117 and (train$3 test$3 diagnosys sampl$3) near5 (mode signal input$4 output$4 sequence series operation command read$3 writ$4) with (transistor mosfet fet (discrete near2 element) source drain gate memory)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L276	0	L117 and (low near5 state)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L277	1	L117 and (low high) near5 (pull$3 state level impedance)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L278	1	L117 and edge	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L279	0	L117 and (edge pin connector) near5 (first primary second$3) near5 (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L280	0	L117 and (edge pin connector) near5 (first primary second$3) with (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L281	1	L117 and (edge pin connector) near5 (first primary second$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L282	1	L117 and (edge pin	(US-PGPUB; USPAT;	OR	ON	ON	2023/04/22

		connector contact) with (active inactive enabl$3 disabl$3 off on)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				10:13 PM
L283	35	("20060277355"|"7411862"|"20030115427"|"20050071580"|"3414781"|"3560935"|"4672570"|"5388074"|"5438536"|"5450576"|"5511152"|"5606662"|"5684979"|"5835733"|"6693840"|"6754787"|"6763437"|"6886109"|"7024518"|"7065688"|"7093115"|"7155579"|"7221699"|"7266633"|"7489163"|"7525860"|"7539909"|"7568130"|"7586350"|"7647467"|"7757101"|"8074034"|"8139430"|"8359521"|"8429493").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2023/04/22 10:13 PM
L284	3	L139 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L285	0	L140 and controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L286	84	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L287	18	L142 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L288	15	L143 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L289	6	L144 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L290	6	L145 and (transistor $3FET drain$3) same (controller device microcontroller micro-	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

		controller)					
L291	6	L146 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L292	1	L147 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L293	326894	(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L294	103	((("NETLIST") near3 ("INC"))).AS,AANM.	(USPAT)	OR	ON	ON	2023/04/22 10:13 PM
L295	417	((("NETLIST") near3 ("INC"))).AS,AANM.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L296	15489	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2023/04/22 10:13 PM
L297	114436	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP,	OR	ON	ON	2023/04/22 10:13 PM

			AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L298	388	L149 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L299	15	L151 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L300	2	L153 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO,	OR	ON	ON	2023/04/22 10:13 PM

			RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L301	397	154 155 156	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L302	17	L157 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L303	17	L158 AND (transistor $3FET drain$3) SAME (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L304	3	L159 AND @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU,	OR	ON	ON	2023/04/22 10:13 PM

			CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L305	326894	(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:39 PM
L306	388	L305 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:40 PM
L307	94	L306 AND (transistor $3FET drain$3) SAME (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL,	OR	ON	ON	2023/04/22 10:40 PM

			PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L308	17	L307 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:41 PM
L309	3	L308 AND @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:41 PM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N8	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational	(USPAT)	SAME	ON	ON	2016/02/18 12:10 AM

		mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.					
N59	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.	(USPAT)	SAME	ON	ON	2017/09/28 04:08 PM
N73	3	("9858218" "9311116" "8489837").pn.	(USPAT)	OR	ON	ON	2018/08/22 05:23 PM
N93	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification	(USPAT)	SAME	ON	ON	2019/08/05 02:40 PM

		circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.					
N94	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.	(USPAT)	SAME	ON	ON	2019/08/05 02:40 PM
N129	0	"20080098277".pn.	(USPAT)	OR	ON	ON	2021/02/20 09:05 PM
N130	1	(output$4 issu$3 broadcast$3) near5 (parity near3 error) with (output$4 issu$3 broadcast$3) near5 (train$3) with (open near3 (drain gate source transistor))	(USPAT)	OR	ON	ON	2021/09/10 08:58 PM
N131	1	(output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) same (output$4 issu$3 broadcast$3) near5 (train$3 test$3) near4 (signal operation code instruction) same ((open$3 clos$3 shun$4) near3 (drain gate source transistor))	(USPAT)	OR	ON	ON	2021/09/10 09:03 PM
N132	148	(send$3 sent receiv$3 deliver$3 output$4	(USPAT)	OR	ON	ON	2021/09/10 09:10 PM

		issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) and (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) and ((open$3 clos$3 shun$4) near3 (drain gate source transistor))					
N133	145	N132 and @ad<"20090612"	(USPAT)	OR	ON	ON	2021/09/10 09:13 PM
N134	4	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) and (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) and ("same") near3 ((open$3 clos$3 shun$4) near3 (drain gate source transistor))	(USPAT)	OR	ON	ON	2021/09/10 09:14 PM
N135	4	N134 and @ad<"20090612"	(USPAT)	OR	ON	ON	2021/09/10 09:15 PM
N136	124	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) and (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) and ("same") near3 ((drain gate source transistor))	(USPAT)	OR	ON	ON	2021/09/10 09:15 PM
N137	121	N136 and @ad<"20090612"	(USPAT)	OR	ON	ON	2021/09/10 09:17 PM
N138	0	(send$3 sent receiv$3	(USPAT)	OR	ON	ON	2021/09/10

		deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) same (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) same ("same") near3 ((drain gate source transistor))					09:20 PM
N149	0	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) same (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) same ("same") near3 ((drain gate source transistor))	(USPAT)	OR	ON	ON	2022/02/12 02:59 PM

PE2E SEARCH - Search History (Similarity Search)

No Similarity Results available

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	17/840,593	Filing Date	2022-06-14	Docket Number (if applicable)	NL066-13US02	Art Unit	2133
First Named Inventor	Hyun LEE			Examiner Name	Mardochee CHERY		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 603916

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

Applicant Signature

PTO/SB/30EFS (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Jamie J. Zheng/	Date (YYYY-MM-DD)	2023-08-01
Name	Jamie J. Zheng	Registration Number	51167

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronically filed August 1, 2023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3678
Serial No.:	17/840,593	Group Art Unit:	2133
Filed:	June 14, 2022	Examiner:	Mardochee CHERY
For:	*MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION*	Attorney Docket No.:	NL066-13US02

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☒ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

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Ex. 1002, p. 177

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☒ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

3d. ☐ The $120 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

4d. ☐ The $120 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

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5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☒ Copies of publications listed on Form PTO-1449 from prior application Serial Nos. **12/815,339**, filed on **6/14/2010**, **13/942,732**, filed on **7/16/2013**, **15/088,155**, filed on **4/1/2016**, **15/857,553**, filed on **12/28/2017**, **16/680,060**, filed on **11/11/2019**, of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure

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Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Deposit Account No. 60-3916 (order no. NL066-13US02).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: August 1, 2023

/Jamie J. Zheng/ 51,167

Jamie Zheng (Reg. No.)
Customer No. 79141
(650) 521-4828

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Ex. 1002, p. 180

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/840,593	**08/01/2023 07:59:20 PM ET**	**NL066-13US02**

Title of Invention

MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3678	FILED BY	Jamie Zheng
PATENT CENTER #	62544180	FILING DATE	06/14/2022
CUSTOMER #	79141	FIRST NAMED INVENTOR	Hyun Lee
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 3

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
NL066-13US02_IDS1_Transmittal_2023-08-01.pdf	4	Information Disclosure Statement (IDS) Form (SB08)	157 KB
Warning: This is not a USPTO supplied IDS fillable form. Data in the form cannot be automatically loaded to other USPTO systems.			
NL066-13US02_IDS1_List.pdf	9	Information Disclosure Statement (IDS) Form (SB08)	311 KB
Warning: This is not a USPTO supplied IDS fillable form. Data in the form cannot be automatically loaded to other USPTO systems.			
NL066-	3	Request for Continued	1642 KB

13US02_RCE_20230801.pdf Examination (RCE)

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
NL066-13US02_IDS1_Transmittal_2023-08-01.pdf	71D3C422C4113AD905273288EAC2CC72BAB67F7B7654540A87EBE354007229509EEC149F7EA64A1C3E8CD444AD11474533EA3D486A333704CE9CBE95B2EE5E28
NL066-13US02_IDS1_List.pdf	9702CA23F041DE9F177D669FB6E651215DB64A7B9F5D259602F7AF11110BC0FFD788B26BBC2D657C8FD513C126E3DE5A3CD34A4D643E35C4DC26F7762D9D1593
NL066-13US02_RCE_20230801.pdf	015665F41DA76878AE56AD0193035C26045F351A2C68782E74E27A16ECDC33AC429FBAB9AC6DB8891EC5D33244C43858C8B52FEFBFDE66BB62055FE2E30E0E6F

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
Sheet	1	of	9	Attorney Docket Number	129980-5066US02

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		3,414,781	12-03-1968	Dill	
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Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
Sheet	2	of	9	Attorney Docket Number	129980-5066US02

		8,452,917 B2	05-28-2013	Amer et al.	
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Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review Case No. IPR2017-00548, Petition for Inter Partes Review of U.S. Patent No. 8,489,837, filed December 30, 2016.
		Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 1003 "Declaration of Donald Alpert", filed December 30, 2016.
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
Sheet	3	of	9	Attorney Docket Number	129980-5066US02

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
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				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
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				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
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				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
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Examiner Signature		Date Considered	

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				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
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				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
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Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
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				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
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Examiner Signature		Date Considered	

Electronically filed August 1, 2023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3678
Serial No.:	17/840,593	Group Art Unit:	2133
Filed:	June 14, 2022	Examiner:	Mardochee CHERY
For:	*MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION*	Attorney Docket No.:	NL066-13US02

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☒ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

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☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☒ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

3d. ☐ The $120 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

4d. ☐ The $120 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL066-13US01).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

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Ex. 1002, p. 193

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial Nos. _____, filed on _____, of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☒ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial Nos. **12/815,339**, filed on **6/14/2010**, **13/942,732**, filed on **7/16/2013**, **15/088,155**, filed on **4/1/2016**, **15/857,553**, filed on **12/28/2017**, **16/680,060**, filed on **11/11/2019**, are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

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9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Deposit Account No. 60-3916 (order no. NL066-13US02).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: August 1, 2023

/Jamie J. Zheng/ 51,167

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Samsung Electronics Co., Ltd.
Ex. 1002, p. 195

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
Sheet	1	of	3	Attorney Docket Number	129980-5066US02

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 1067 - 2021-10-15 Complaint, filed October 15, 2021
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 1061 - WDTX Claim Construction, filed October 15, 2021
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 2019 - Redline comparison of 2022IPR-00062 to IPR2020-01044, filed February 18, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 2017 - Microway, DDR4 RDIMM and LRDIMM Performance Comparison (July 10, 2015), https://www.microway.com/hpctech-tips/ddr4-rdimm-lrdimm-performance-comparison/, filed February 18, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 2016 - Intel, Fully Buffered DIMM (FB-DIMM) Design Considerations (Feb 18, 2004), http://www.csit-sun.pub.ro/~cpop/Documentatie_SMP/Intel_Microprocessor_Systems/PC_Memory/OSA-S009.pdf, filed February 18, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 2012 - Excerpt of Semiconductor Memories, A Handbook of Design, Manufacture, and Application Second Edition (1997), filed February 18, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 2011 - Excerpt of DRAM Circuit Design, Fundamental and High Speed Topics (2008), filed February 18, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 2006 - IT Solution Architects, Server Memory: RDIMM vs LRDIMM and When to Use Them (Aug. 16, 2017), https://medium.com/@ITsolutions/server-memory-rdimm-vslrdimm-and-when-to-use-them-a550f4b7cf39, filed February 18, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 2001 - Declaration of Robert J. Murphy, dated February 18, 2022 (corrected), filed February 18, 2022

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
Sheet	2	of	3	Attorney Docket Number	129980-5066US02

		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, NETLIST, INC.S PATENT OWNERS PRELIMINARY RESPONSE, filed February 18, 2022
		Inter Partes Review of US Patent No.10474595, Case No. IPR2022-00064, NETLIST, INC.S PATENT OWNERS PRELIMINARY RESPONSE, filed February 18, 2022
		Inter Partes Review of US Patent No.10474595, Case No. IPR2022-00064, Exhibit 2001 - Declaration of Robert J. Murphy, dated February 18, 2022 (corrected), filed February 18, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 1069 - Netlist's motion to dismiss in Delaware, filed March 18, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 1068 - Samsung's first amended complaint, filed March 18, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Petitioner's Authorized Reply to Patent Owner's Preliminary Response, filed March 18, 2022
		Inter Partes Review of US Patent No.10474595, Case No. IPR2022-00064, Petitioner's Authorized Reply to Patent Owner's Preliminary Response, filed March 18, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, PATENT OWNERS AUTHORIZED SUR-REPLY IN SUPPORT OF ITS PRELIMINARY RESPONSE, filed March 25, 2022
		Inter Partes Review of US Patent No.10474595, Case No. IPR2022-00064, PATENT OWNERS AUTHORIZED SUR-REPLY IN SUPPORT OF ITS PRELIMINARY RESPONSE, filed March 25, 2022
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		Inter Partes Review of US Patent No.10474595, Case No. IPR2022-00064, Institution Decision: Grant, issued May 16, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 2028 - AMD Geode LX Processor DDR2 BIOS Porting Guide (March 2009), filed August 15, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 2027 - Second Declaration of Dr. Robert Murphy, dated August 15, 2022, filed August 15, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, NETLIST, INC.S PATENT OWNERS RESPONSE, filed August 15, 2022
		Inter Partes Review of US Patent No.10474595, Case No. IPR2022-00064, NETLIST, INC.S PATENT OWNERS RESPONSE, filed August 15, 2022
		Inter Partes Review of US Patent No.10474595, Case No. IPR2022-00064, Exhibit 2027 - Second Declaration of Dr. Robert Murphy, dated August 15, 2022, filed August 15, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 1081 - Annotation of DDR3 LRDIMM, filed November 7, 2022

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
Sheet	3	of	3	Attorney Docket Number	129980-5066US02

		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 1080 - Annotation of DDR3 LRDIMM, filed November 7, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 1079 - Netlist's Technology Tutorial, filed November 7, 2022
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		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 1077 - Deposition of Robert Murphy (Oct. 27, 2022), filed November 7, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Petitioner's Reply to Patent Owner's Response, filed November 7, 2022
		Inter Partes Review of US Patent No.10474595, Case No. IPR2022-00064, Petitioner's Reply to Patent Owner's Response, filed November 7, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, NETLIST, INC.'S PATENT OWNER'S SUR-REPLY, filed December 19, 2022
		Inter Partes Review of US Patent No.10474595, Case No. IPR2022-00064, NETLIST, INC.'S PATENT OWNER'S SUR-REPLY, filed December 19, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 2029 - Patent Owner's Oral Hearing Demonstratives, filed February 9, 2023
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 1082 - Petitioner's demonstratives for oral argument, filed February 9, 2023
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Other: Hearing transcript, filed March 8, 2023
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Final Written Decision, entered May 8, 2023
		Inter Partes Review of US Patent No.10474595, Case No. IPR2022-00064, Final Written Decision, entered May 9, 2023

Examiner Signature		Date Considered	

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/840,593	**08/01/2023 08:31:19 PM ET**	**NL066-13US02**

Title of Invention

MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3678	FILED BY	Jamie Zheng
PATENT CENTER #	62544267	FILING DATE	06/14/2022
CUSTOMER #	79141	FIRST NAMED INVENTOR	Hyun Lee
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 41

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
NL066-13US02_IDS2_Transmittal_2023-08-01.pdf	4	Information Disclosure Statement (IDS) Form (SB08)	158 KB
Warning: This is not a USPTO supplied IDS fillable form. Data in the form cannot be automatically loaded to other USPTO systems.			
NL066-13US02_IDS2_List.pdf	3	Information Disclosure Statement (IDS) Form (SB08)	211 KB
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IPR2022-	41	Non Patent Literature	595 KB

00064_SRRPOR.pdf			
IPR2022-00064_FWD.pdf	86	Non Patent Literature	635 KB
IPR2022-00064_POR.pdf	84	Non Patent Literature	1069 KB
IPR2022-00064_Decision_Institution.pdf	56	Non Patent Literature	672 KB
IPR2022-00064_ASRRPOPR.pdf	11	Non Patent Literature	189 KB
IPR2022-00064_POPR.pdf	78	Non Patent Literature	749 KB
IPR2022-00064_ARPOPR.pdf	16	Non Patent Literature	385 KB
IPR2022-00064_Ex_2027_Murphy_Declaration.pdf	131	Non Patent Literature	1919 KB
IPR2022-00062_SRRPORpdf.pdf	39	Non Patent Literature	595 KB
IPR2022-00062_POPR.pdf	74	Non Patent Literature	728 KB
IPR2022-00062_POR.pdf	83	Non Patent Literature	1106 KB
IPR2022-00062_FWD.pdf	79	Non Patent Literature	592 KB
IPR2022-00062_OH.pdf	108	Non Patent Literature	926 KB
IPR2022-00064_Ex_2001_Decl_Robert_Murphy-CORRECTED.pdf	90	Non Patent Literature	2212 KB
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IPR2022-00062_Decision_Institution.pdf	58	Non Patent Literature	705 KB
IPR2022-00062_Ex_2027_Murphy_Declaration.pdf	127	Non Patent Literature	1847 KB
Ex_2017_DDR4_RDIMM_and_LRDIMM_Perf_Comp.pdf	7	Non Patent Literature	232 KB
Ex_2012_Semiconductor_Memories.pdf	6	Non Patent Literature	601 KB
Ex_2011_DRAM_Circuit_Design.pdf	4	Non Patent Literature	494 KB
Ex_2019_Redline_Comp_'218_IPR.pdf	96	Non Patent Literature	964 KB
IPR2022-00064_RPOR.pdf	55	Non Patent Literature	4091 KB
IPR2022-00062_RPOR.pdf	50	Non Patent Literature	3925 KB
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Ex_1080_Annotation_of_DDR3_LRDIMM.pdf	1	Non Patent Literature	121 KB

Ex_2016_FB-DIMM_Design_Considerations.pdf	36	Non Patent Literature	4486 KB
Ex_2006_RDIMM_LRDIMM_When_to_Use.pdf	5	Non Patent Literature	2351 KB
Ex_1078_Redline_Comparing_Murphy_Declarations_218_and_595_Patents.pdf	139	Non Patent Literature	1929 KB
Ex_1079_Netlist's_Technology_Tutorial.pdf	10	Non Patent Literature	1238 KB
Ex_1069_Netlist_MTD_Sams_FAC.pdf	2	Non Patent Literature	195 KB
Ex_1077_Depo_Robert_Murphy.pdf	206	Non Patent Literature	625 KB
Ex_1061_WDTX_Claim_Construction.pdf	5	Non Patent Literature	302 KB
Ex_1068_Sams_FAC.pdf	122	Non Patent Literature	1198 KB
Ex_1067_Complaint.pdf	82	Non Patent Literature	1271 KB
Ex_2029_PO_Demonstratives.pdf	93	Non Patent Literature	6690 KB
Ex_1082_Sams_Demonstratives.pdf	136	Non Patent Literature	13116 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
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Ex_2019_Redline_Comp_'218_IPR.pdf	349405B8C43E619FB22AECF11DE498D9D0F9D5464D4547246 050F17B3AA6F5830B585078FF6C6A1B09249374645E4AA4A68 22B49F92364AFB23874605F1DFBE0
IPR2022-00064_RPOR.pdf	12191692343BAE732DDAECA09D0328A99D76F296555077BED D3377A890F20F7F410AD12F2748CBDAFEC5636E8E7CB03366 31480CB80BA9F12E86456AFBB625FF
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Ex_2016_FB-	85D236DDC25E3C041D60C6EC23FF136EC54279E20B8115A13

DIMM_Design_Considerations.pdf	696575563A1D87E16248D3B644711608FEFAF72B50FBDDBDDE39C797866B2308A86C3EA8115FA1E
Ex_2006_RDIMM_LRDIMM_When_to_Use.pdf	39F33B05F2ED670CB66F1731302DE4B4E5292A05B20B254C76DB9185B53127FAC6B440BBF1089C6A2B0CC2A5B337BEB14AE081634B48E44D0E420D6D1EAF7EC3
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Ex_1068_Sams_FAC.pdf	AAD9FF0A8A0586CB141529E7A9A21DDE5C3F4982F0B3073D714BAC5312036708661C5AEB66DD673B4448AA45D00EF9E2D405398AEE2CC11DFCD64E51522D2268
Ex_1067_Complaint.pdf	249C1A60CC4B33FEE5B59806F9D8FDBA388CD5C57C93DAC84574DBD34D4D7105A26EE5ED69EC2C20FD23ED325B16CD05F79124E32C7667A298A7C52CFDACDE65
Ex_2029_PO_Demonstratives.pdf	B207253F02DCF2FC5499DA5CF6FB4A3D0F1DE5484937E260D36D496F2D01363726ED3976B63B53B5D3ED103DED4ACB94E59B4E5D209A9FEB8333402DA9092725
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s.pdf F2EBCD313D3D610D10A7A490863D51A8819F1168C1CB18FEF523ED4231D6DA1DB3C443B5E023F5

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/840,593	**08/01/2023 08:31:19 PM ET**	**NL066-13US02**

Title of Invention

MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3678	FILED BY	Jamie Zheng
PATENT CENTER #	62544267	AUTHORIZED BY	-
CUSTOMER #	79141	FILING DATE	06/14/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Hyun Lee

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 2819	**E202381K31527010**	**Jamie Zheng**

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1801	REQUEST FOR CONTINUED EXAMINATION (RCE) - 1ST REQUEST (SEE 37 CFR 1.114)	1360.00	1	1360.00
			TOTAL AMOUNT:	**$1,360.00**

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

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New International Application Filed with the USPTO as a Receiving Office

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 08/30/2023

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER	
CHERY, MARDOCHEE	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/30/2023

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/840,593	06/14/2022	Hyun Lee	NL066-13US02	3678

TITLE OF INVENTION: MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	11/30/2023

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 08/30/2023
USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/840,593	06/14/2022	Hyun Lee	NL066-13US02	3678

TITLE OF INVENTION: MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	11/30/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHERY, MARDOCHEE	2133	711-154000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required)

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via Patent Center or EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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Ex. 1002, p. 211

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/840,593	06/14/2022	Hyun Lee	NL066-13US02	3678

79141 7590 08/30/2023

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER	
CHERY, MARDOCHEE	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/30/2023

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Notice of Allowability	Application No. 17/840,593	Applicant(s) Lee, Hyun	
	Examiner MARDOCHEE CHERY	Art Unit 2133	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to the RCE filed 8/1/2023.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-20 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 8/1/2023.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	8/24/2023

Samsung Electronics Co., Ltd.
Ex. 1002, p. 214

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/840,593	Lee, Hyun
	Examiner	**Art Unit**
	MARDOCHEE CHERY	2133

CPC						
Symbol					**Type**	**Version**
G06F	/	13	/	1694	F	2013-01-01
G11C	/	5	/	04	I	2013-01-01
G11C	/	7	/	1063	I	2013-01-01
G06F	/	13	/	1668	I	2013-01-01
G06F	/	9	/	445	I	2013-01-01
G06F	/	13	/	24	I	2013-01-01
G06F	/	3	/	0619	I	2013-01-01
G06F	/	3	/	0632	I	2013-01-01
G06F	/	3	/	0659	I	2013-01-01
G06F	/	3	/	0673	I	2013-01-01
G06F	/	11	/	1068	I	2013-01-01
G11C	/	29	/	52	I	2013-01-01
G06F	/	12	/	0646	I	2013-01-01
G11C	/	2207	/	2254	A	2013-01-01
G11C	/	5	/	00	A	2013-01-01
G11C	/	7	/	1066	A	2013-01-01
G11C	/	16	/	26	A	2013-01-01
G11C	/	29	/	78	A	2013-01-01
G11C	/	2029	/	4402	A	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	24 August 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

U.S. Patent and Trademark Office

Part of Paper No.: 20230824

Samsung Electronics Co., Ltd.
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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/840,593	Lee, Hyun
	Examiner	**Art Unit**
	MARDOCHEE CHERY	2133

INTERNATIONAL CLASSIFICATION					
CLAIMED					
G06F	/	12	/	00	
NON-CLAIMED					
	/		/		

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
711	154

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133 (Primary Examiner)	24 August 2023 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3

U.S. Patent and Trademark Office

Part of Paper No.: 20230824

Samsung Electronics Co., Ltd.
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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/840,593	Lee, Hyun
	Examiner	**Art Unit**
	MARDOCHEE CHERY	2133

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10		19										
	2		11		20										
	3		12												
	4		13												
	5		14												
	6		15												
	7		16												
	8		17												
	9		18												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	24 August 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

U.S. Patent and Trademark Office

Part of Paper No.: 20230824

Samsung Electronics Co., Ltd.
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/840,593	Lee, Hyun
	Examiner	Art Unit
	MARDOCHEE CHERY	2133

CPC - Searched*		
Symbol	Date	Examiner
(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254)	09/28/2022	MC

CPC Combination Sets - Searched*		
Symbol	Date	Examiner
(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254)	09/28/2022	MC

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	154	09/28/2022	MC

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
PE2E Search; CPC; Inventor; Assignee	09/28/2022	MC
PE2E; CPC	04/22/2023	MC
PE2E	08/24/2023	MC

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	8/22/23

Samsung Electronics Co., Ltd.
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/840,593	Lee, Hyun
	Examiner	Art Unit
	MARDOCHEE CHERY	2133

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	See Attached	04/22/2023	MC

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	8/22/23

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
Sheet	1	of	3	Attorney Docket Number	129980-5066US02

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

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Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 1067 - 2021-10-15 Complaint, filed October 15, 2021
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 1061 - WDTX Claim Construction, filed October 15, 2021
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 2019 - Redline comparison of 2022IPR-00062 to IPR2020-01044, filed February 18, 2022
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		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 2012 - Excerpt of Semiconductor Memories, A Handbook of Design, Manufacture, and Application Second Edition (1997), filed February 18, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 2011 - Excerpt of DRAM Circuit Design, Fundamental and High Speed Topics (2008), filed February 18, 2022
		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, Exhibit 2006 - IT Solution Architects, Server Memory: RDIMM vs LRDIMM and When to Use Them (Aug. 16, 2017), https://medium.com/@ITsolutions/server-memory-rdimm-vslrdimm-and-when-to-use-them-a550f4b7cf39, filed February 18, 2022
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Examiner Signature	/MARDOCHEE CHERY/	Date Considered	08/24/2023

DB2/ 22684197.4

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
Sheet	2	of	3	Attorney Docket Number	129980-5066US02

		Inter Partes Review of US Patent No.9858218, Case No. IPR2022-00062, NETLIST, INC.S PATENT OWNERS PRELIMINARY RESPONSE, filed February 18, 2022
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		Inter Partes Review of US Patent No.10474595, Case No. IPR2022-00064, Exhibit 2001 - Declaration of Robert J. Murphy, dated February 18, 2022 (corrected), filed February 18, 2022
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Examiner Signature	/MARDOCHEE CHERY/	Date Considered	08/24/2023

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
Sheet	3	of	3	Attorney Docket Number	129980-5066US02

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Examiner Signature	/MARDOCHEE CHERY/	Date Considered	08/24/2023

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.C/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
Sheet	1	of	9	Attorney Docket Number	129980-5066US02

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Examiner Signature	/MARDOCHEE CHERY/	Date Considered	08/24/2023

DB2/ 22684197.4

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
Sheet	2	of	9	Attorney Docket Number	129980-5066US02

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
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		Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 1003 "Declaration of Donald Alpert", filed December 30, 2016.
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Examiner Signature	/MARDOCHEE CHERY/	Date Considered	08/24/2023

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
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				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
Sheet	3	of	9	Attorney Docket Number	129980-5066US02

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		Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Trial Instituted document, dated May 15, 2017.
		Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Patent Owner's Response, filed September 6, 2017.
		Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2001 - Declaration of Robert J Murphy, filed September 6, 2017.
		Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2002 - DEPOSITION OF DONALD ALPERT, Ph.D., filed September 6, 2017.
		Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2003 - Defendants' Opening Claim Construction Brief, filed September 6, 2017.
		Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2004 - PLAINTIFF NETLIST, NC.'S OPENING CLAIM CONSTRUCTION BRIEF, filed September 6, 2017.
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		Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 2006 - DEFENDANTS' REPLY CLAIM CONSTRUCTION BRIEF, filed September 6, 2017.
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		Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Petitioner's Reply to Patent Owner's Response, filed December 13, 2017.
		Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Petitioner's Demonstratives, filed February 9, 2018.
		Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Demonstratives of Patent Owner Netlist, Inc., filed February 9, 2018.
		Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Record of Oral Hearing, held February 14, 2018.

Examiner Signature	/MARDOCHEE CHERY/	Date Considered	08/24/2023

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
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		Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Final Written Decision, entered May 3, 2018.
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Petition for Inter Partes Review of U.S. Patent No. 9,535,623, filed December 14, 2017
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1003, 'Declaration of Donald Alpert,' filed December 14, 2017
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1003, 'Corrected Declaration of Donald Alpert,' filed December 19, 2017
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, PO Preliminary Response, filed March 19, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Patent Owner's Response, filed August 10, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Petitioners' Reply to Patent Owner's Response, filed November 9, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Patent Owner Submission of ITC Claim Construction Order, filed November 30, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Patent Owner Reply to Petitioner Opposition to Motion to Exclude, filed December 21, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Patent Owner Demonstratives, filed February 4, 2019
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		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Trial Instituted Document, dated May 24, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, Hearing Transcript, filed February 26, 2019
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 2001, DECLARATION OF ROBERT J. MURPHY, filed March 19, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 2002, 'Bruce Jacob, Memory Systems – Cache, DRAM, Disk, 2008 by Elsevier Inc.,' filed March 19, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 2004, 'Riser Card Tutorial, Orbit Micro News and Notes, September 6th, 2008,' filed March 19, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 2005, 'SUPPLEMENTAL DECLARATION OF ROBERT J. MURPHY,' filed August 10, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 2006, 'DEPOSITION OF DONALD ALPERT, Ph.D. on July 20, 2018,' filed August 10, 2018
		ITC Investigation No. 337-TA-1089, JOINT LIST OF CLAIM TERMS FOR CONSTRUCTION, dated March 12, 2018

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				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
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		ITC Investigation No. 337-TA-1089, ORDER NO. 17: CONSTRUING TERMS OF THE ASSERTED PATENTS, dated August 30, 2018
		ITC Investigation No. 337-TA-1089, COMMISSION OPINION, dated April 21, 2020
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1025, 'ITC Investigation No. 337-TA-1023, Initial Determination (Excerpts),' filed December 14, 2017
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		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 2009, 'The Authoritative Dictionary of IEEE Standard Terms, 7th Edition,' filed August 10, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1030, 'Declaration of Brian Nester PHV,' filed October 18, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1032, 'Annotated Page 37 of Ex. 2005,' filed November 9, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1034, 'ITC Expert Report of Robert Mr. Murphy Regarding 623 Patent (Public Version),' filed November 9, 2018
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		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1035, 'Mr. Murphy 623 IPR Deposition Transcript (October 25, 2018),' filed November 9, 2018
		Inter Partes Review of US Patent No.9535623, Case No. IPR2018-00303, EXHIBITS 1036, 'Mr. Murphy 623 ITC Deposition Transcript (October 19, 2018),' filed November 9, 2018
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		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, 'Petition for Inter Partes Review,' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, EXHIBITS 1003, 'Declaration of Donald Alpert,' filed June 9, 2020
		Inter Partes Review No. 2020-01044 of US Patent No. 9858218, 'Petition for Inter Partes Review,' filed June 9, 2020
		Inter Partes Review No. 2020-01044 of US Patent No. 9858218, EXHIBITS 1003, 'Declaration of Donald Alpert,' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1050, 'Declaration of Julie Carlson,' filed June 9, 2020

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
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		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1054, 'Declaration of John Halbert,' filed June 9, 2020
		Inter Partes Review No. 2020-01042 of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBITS 1055, 'Declaration of Roland Knaack,' filed June 9, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Patent Owner's Preliminary Response, filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Petitioners' Reply To Patent Owner's Preliminary Response, filed October 8, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Patent Owner's Sur-Reply to Petitioner's Reply to Patent Owner's Preliminary Response, filed October 15, 2020
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, Patent Owner's Preliminary Response, filed September 18, 2020
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, Petitioners' Reply To Patent's Owner Preliminary Response, filed October 8, 2020
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, Patent Owner's Sur-Reply to Petitioner's Reply to Patent Owner's Preliminary Response, filed October 15, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, Decision Granting Institution of Inter Partes Review, issued December 17, 2020, 47 pgs.
		Inter Partes Review of US Patent No. 9858218, Case No. IPR2020-01044, Decision Granting Institution of Inter Partes Review, issued December 17, 2020, 55 pgs.
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 1069, 'Netlist, Inc. Complaint for Patent Infringement, Netlist, Inc. v. SK hynix Inc. et al, 6:20-cv-00194 (March 17, 2020),' filed October 8, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2005, 'Claim Construction Order, STC.UNM v. Apple Inc., Civil No. 1:20-cv-00351-ADA (W.D. Tex. Jun8, 2020),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2006, 'Claim Construction Order, Uniloc 2017 LLC v. Apple Inc., Civil No. 6:19-cv-00532-ADA (W.D. Tex. Jun 8, 2020),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2007, 'Claim Construction Order, MV3 Partners LLC v. Roku Inc., Civil No. 6:18-cv-00308-ADA (W.D.Tex. Oct.19,2019),' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2009, 'Exhibit A1 of SK hynix's Invalidity Contentions, dated Aug. 7, 2020,' filed September 18, 2020
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
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		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2011, 'Exhibit A19 of SK hynix's Invalidity Contentions, dated Aug. 7, 2020,' filed September 18, 2020
		Inter Partes Review of US Patent No. 10474595, Case No. IPR2020-01042, EXHIBIT 2012, 'Exhibit A36 of SK hynix's Invalidity Contentions, dated Aug. 7, 2020,' filed September 18, 2020
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		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2026, "Remote Deposition Under Oral Examination of Dr. Donald Alpert, March 10, 2021," filed 11MAR2021, 493 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2027, "DDR3 SDRAM LRDIMM," filed 11MAR2021, 18 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2028, "Join JEDEC Membership Details," filed 11MAR2021, 2 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2029, "DRAM Circuit Design: Fundamental and High-Speed Topics," filed 11MAR2021, 4 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2030, "Semiconductor Memories: A Handbook and Design, Manufacture, and Application Second Edition," filed 11MAR2021, 6 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2031, "Deposition of Donald Alpert, Ph.D.," filed 11MAR2021, 218 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2032, "Declaration of Robert J. Murphy," filed 11MAR2021, 65 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, "Patent Owner's Response Under 37 C.F.R. Section 42.120," 11MAR2021, 68 pgs.
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		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, Exhibit 2025, "Declaration of Andrew H. DeVoogd," filed 08MAR2021, 4 pgs.
		Inter Partes Review of US Patent No. 10,474,595, Case No. IPR2020-01042, "Patent Owner's Request for Rehearing of Institution Decision," 30MAR2021, 12 pgs.
		Inter Partes Review of US Patent No. 9,858,218, Case No. IPR2020-01044, Exhibit 2032, "Declaration of Robert J. Murphy," filed 12MAR2021, 63 pgs.
		Inter Partes Review No. 2022-00062 of US Patent No. 9858218, EXHIBITS 1067, Samsung Electronics Co. LTD., et al. v. Netlist Inc., In the United States District Court for the District of Delaware, 'Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract,' filed October 15, 2021

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
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		Inter Partes Review No. 2022-00062 of US Patent No. 9858218, EXHIBITS 1061, Netlist, Inc. vs. SK Hynix Inc., et al., In the United States District Court for the Western District of Texas Waco Division, 'Claim Construction Order,' issued March 12, 2021, filed October 15, 2021
		Inter Partes Review No. 2022-00062 of US Patent No. 9858218, EXHIBITS 1055, 'Declaration of Sung Joo Park,' filed October 15, 2021
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		Inter Partes Review No. 2022-00062 of US Patent No. 9858218, 'Petition for Inter Partes Review of U.S. Patent No. 9,858,218,' October 15, 2021
		Inter Partes Review No. 2022-00064 of US Patent No. 10474595, EXHIBITS 1003, 'Declaration of Donald Alpert,' filed October 15, 2021
		Inter Partes Review No. 2022-00064 of US Patent No. 10474595, PAPER 1, 'Petition for Inter Partes Review of U.S. Patent No. 10,474,595,' October 15, 2021
		JEDEC COMMITTEE LETTER BALLOT, LRDIMM DDR3 Memory Initialization Chapter Proposal (Dec. 2009) ("JEDEC")
		Inphi Corporation, MB Initialization sequence Item 142.35, June 4, 2009
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		JEDEC Standard, Low Power Double Data Rate (LPDDR) SDRAM Specification (August 2007) ("JESD209")
		JEDEC COMMITTEE LETTER BALLOT, DDR3 LRDIMM Design Specification Body (Dec. 2009)
		JEDEC, Compilation of Tallies for JC-40 CMOS Digital Logic and point committees (Dec. 4, 2009)
		"Sequence," https://www.lexico.com/en/definition/sequence
		"28-Bit to 56-Bit Registered Buffer with Address Parity Test One Pair to Four Pair Differential Clock PLL Driver," Texas Instruments (October 2008)
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		"Minutes of Meeting No. 158 JC-40 Digital Logic Committee" JEDEC (June 4, 2009)
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		JEDEC, JEDEC Manual of Organization and Procedure, JM21N (Rev. of JM21M, December 2006), (May, 2008)
		JEDEC, "Committee Letter Ballot, JC-40.4-09-320, Item 142.35," (Dec. 2009)
		JEDEC, "Committee Letter Ballot, JC-45.4-09-321, Item 2192.44," (Dec. 2009)
		JEDEC, "Tally of Votes, Committee Letter Ballot, JC-45.4-09-321, 2192.44" (Dec. 9, 2009)
		JEDEC Standard, FBDIMM: Architecture and Protocol (January 2007) ("JESD206")
		Lee, Office Action, US15/088,115, 20MAY2016, 10 pgs.
		Lee, Office Action, US15/088,115, 16JUN2017, 9 pgs.

Examiner Signature	/MARDOCHEE CHERY/	Date Considered	08/24/2023

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				Art Unit	2133
				Examiner Name	Mardochee CHERY
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		Lee, Notice of Allowance, US15/088,115, 12OCT2017, 5 pgs.
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Examiner Signature	/MARDOCHEE CHERY/	Date Considered	08/24/2023

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	9	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/18 02:54 PM
L2	2	L1 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/18 02:55 PM
L3	50	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/18 02:57 PM
L4	3	L3 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/18 02:57 PM
L6	4	"8621170".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/19 06:18 PM
L7	2	("8489837" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/09/03 06:03 PM
L9	54	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:33 PM
L10	3	L9 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:33 PM
L11	1	L10 and (manufactur$3 industry) near3 standard	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:33 PM
L12	1	L10 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:35 PM
L13	9	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:36 PM
L14	5	L13 and	(US-PGPUB; USPAT;	OR	ON	ON	2016/03/02

		@ad<"20090612"	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				05:36 PM
L15	51	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:55 PM
L16	0	L15 and (parity near3 (error signal bit check)) with (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:57 PM
L17	0	L15 and (parity near3 (error signal bit check)) same (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:57 PM
L18	2	L15 and (parity near3 (error signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:57 PM
L19	2	L15 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:57 PM
L20	41	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 12:53 AM
L21	0	L20 and (drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 12:55 AM
L22	2094169	(FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 12:56 AM
L23	1	L20 and (FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 12:56 AM
L24	0	controller near3 (open near2 drain) with (parity ECC) with controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:17 AM
L25	0	controller near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:18 AM
L26	0	(controller hub switch channel) near5 (open	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2016/09/24 01:19 AM

		near2 drain) with (parity ECC) with controller near5 (host computer node engine)	JPO; DERWENT; IBM_TDB)				
L27	0	(controller hub switch channel) with (open near2 drain) with (parity ECC) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:19 AM
L28	0	(controller hub switch channel) with (open near2 drain) with (parity ECC redundancy (correct$3 near2 code)) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:20 AM
L29	47	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:20 AM
L30	0	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) same (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:21 AM
L31	2	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:21 AM
L32	31	L29 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:23 AM
L33	3	L32 and (parity ECC redundancy error (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:24 AM
L34	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2016/11/14 11:55 AM

		"6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.					
L35	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2016/11/14 11:57 AM
L36	3	mardochee and filter near3 snoop	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2016/11/14 11:59 AM
L37	71	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:00 PM
L38	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:06 PM
L39	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:08 PM
L40	2	L37 and edg$3 near5 (wire port connect$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2016/11/14 12:09 PM

		attach$5 bond$3 drain source gate pin) near5 ($3RAM DIM DIMM SODIMM)	JPO; DERWENT; IBM_TDB)				
L41	3	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:12 PM
L42	2	L41 and (error fault ECC)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:13 PM
L43	2	L41 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:13 PM
L44	2	L43 and (transistor $3FET drain$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:14 PM
L45	2	L43 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:15 PM
L46	2	L45 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:31 PM
L47	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:32 PM
L48	2	L47 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:32 PM
L49	1	L47 and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:35 PM
L50	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/05/24 02:13 PM

L51	3	"20060062047".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/05/24 02:41 PM
L52	27512	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:09 PM
L53	44	L52 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:11 PM
L54	0	L53 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:12 PM
L55	0	L53 and (controller hub switch channel) same (open$3 near2 drain) same controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:13 PM
L56	23	L53 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:13 PM
L57	14	L56 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:14 PM
L58	11	L56 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:19 PM
L60	5	("20060262586" "20060062047").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/29 12:37 AM
L61	14	("9858218" "9311116" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2018/08/22 05:23 PM

			IBM_TDB)				
L62	0	L61 and edge near3 connect$3 near5 ("not" "don't" "doesn't") near2 (active activat$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:31 PM
L63	14	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:32 PM
L64	78	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:32 PM
L65	66	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:32 PM
L66	6	L65 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:32 PM
L67	53	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:33 PM
L68	4	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:33 PM
L69	29963	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:34 PM
L70	48	L69 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:34 PM

		controller)					
L71	24	L70 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:34 PM
L72	12	L71 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:34 PM
L74	142	("3414781" "3560935" "4672570" "5388074" "5438536" "5511152" "5450576" "5606662" "5684979" "5835733" "6693840" "6754787" "6763437" "6886109" "7024518" "7065688" "7093115" "7155579" "7221699" "7266633" "7489163" "7525860" "7539909" "7568130" "7586350" "7647467" "7757101" "8074034" "8139430" "8359521" "8429493" "20030115427" "20050071580" "20050193161" "200600062047" "20060262586" "20070091702" "20070136523" "20070214347" "20080098277" "20080147897" "20080155378" "20080256281" "20090119464" "20100005218" "20100042778" "20100142383" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/03/15 01:19 PM
L75	7	L74 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/03/15 01:19 PM
L76	714	"2" and edg$3 near5	(US-PGPUB; USPAT;	OR	ON	ON	2019/03/15

		(wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				01:20 PM
L77	4	L74 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/03/15 01:20 PM
L78	6	L75 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/03/15 01:20 PM
L79	138210	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:42 PM
L80	4275	L79 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:42 PM
L81	30	L80 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:44 PM

		SODIMM) same (controller microcontroller micro-controller)					
L82	15	L81 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:45 PM
L83	1	L82 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:45 PM
L84	0	L83 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:46 PM
L85	1	L82 and (handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:46 PM
L86	4	L82 and (FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:47 PM
L87	2	L86 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:48 PM
L88	2	L87 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:52 PM
L89	48967	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:54 PM
L90	18643	L89 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:54 PM
L91	8	L90 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:55 PM

L92	0	L91 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:56 PM
L95	2	"6798891".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/11 12:39 PM
L96	36607	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L97	55	L96 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L98	25	L97 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L99	13	L98 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L100	162327	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM

		G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.					
L101	5271	L100 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L102	31	L101 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L103	15	L102 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L104	1	L103 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L105	0	L104 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L106	52734	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:26 PM
L107	18670	L106 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:26 PM
L108	8	L107 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:26 PM

		controller) and drain$3					
L109	0	L108 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:26 PM
L110	162327	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2029/4402 or G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:29 PM
L111	5271	L110 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:32 PM
L112	31	L111 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:32 PM
L113	6	L112 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:34 PM
L114	211	netlist.as.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2020/08/30 08:35 PM

			IBM_TDB)				
L115	6	L114 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:35 PM
L116	1	L115 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:36 PM
L117	3	"20080098277".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 09:06 PM
L118	2	L117 and (transistor mosfet fet (discrete near2 element) source drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 09:53 PM
L119	0	L117 and (transistor mosfet fet (discrete near2 element) source drain gate) with (controller) with (parity error)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 09:55 PM
L120	1	L117 and (train$3 test$3 diagnosys sampl$3) near5 (signal input$4 output$4 sequence series operation command read$3 writ$4)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 10:23 PM
L121	1	L117 and (train$3 test$3 diagnosys sampl$3) near5 (mode signal input$4 output$4 sequence series operation command read$3 writ$4) with (transistor mosfet fet (discrete near2 element) source drain gate memory)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 10:26 PM
L122	0	L117 and (low near5 state)	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2021/02/20 11:05 PM

			JPO; DERWENT; IBM_TDB)				
L123	1	L117 and (low high) near5 (pull$3 state level impedance)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:06 PM
L124	1	L117 and edge	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:21 PM
L125	0	L117 and (edge pin connector) near5 (first primary second$3) near5 (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:23 PM
L126	0	L117 and (edge pin connector) near5 (first primary second$3) with (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:23 PM
L127	1	L117 and (edge pin connector) near5 (first primary second$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:23 PM
L128	1	L117 and (edge pin connector contact) with (active inactive enabl$3 disabl$3 off on)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:26 PM
L139	35	("20060277355"|"7411862"|"20030115427"|"20050071580"|"3414781"|"3560935"|"4672570"|"5388074"|"5438536"|"5450576"|"5511152"|"5606662"|"5684979"|"5835733"|"6693840"|"6754787"|"6763437"|"6886109"|"7024518"|"7065688"|"7093115"|"7155579"|"7221699"|"7266633"|"7489163"|"7525860"|"7539909"|"7568130"|"7586350"|"7647467"|"7757101"|"8074034"|"8139430"|"8359521"|"8429493").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2022/02/12 02:59 PM
L140	2	L139 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:00 PM
L141	0	L140 and controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:01 PM
L142	101	(handshak$3 hand-	(US-PGPUB; USPAT;	OR	ON	ON	2022/02/12

		shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				03:18 PM
L143	13	L142 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:18 PM
L144	12	L143 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:19 PM
L145	4	L144 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:20 PM
L146	4	L145 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:21 PM
L147	4	L146 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:21 PM
L148	1	L147 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:26 PM
L149	304352	(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:04 PM

		G11C2029/4402 OR G11C2207/2254).cpc.					
L150	99	((("NETLIST") near3 ("INC"))).AS,AANM.	(USPAT)	OR	ON	ON	2022/09/28 06:05 PM
L151	406	((("NETLIST") near3 ("INC"))).AS,AANM.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:05 PM
L152	14962	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/28 06:06 PM
L153	107524	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:06 PM
L154	373	L149 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:07 PM
L155	14	L151 AND edg$3 near5	(US-PGPUB; USPAT;	OR	ON	ON	2022/09/28

		(wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				06:07 PM
L156	2	L153 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:07 PM
L157	381	154 155 156	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:07 PM
L158	15	L157 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO,	OR	ON	ON	2022/09/28 06:08 PM

			NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L159	15	L158 AND (transistor $3FET drain$3) SAME (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:08 PM
L160	3	L159 AND @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:09 PM
L161	33	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L162	15	L1 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L163	84	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L164	18	L3 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L165	2	"8621170".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L166	2	("8489837" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L167	84	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L168	18	L9 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L169	9	L10 and (manufactur$3 industry) near3 standard	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L170	1	L10 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L171	33	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L172	5	L13 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L173	105	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L174	2	L15 and (parity near3 (error signal bit check)) with (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L175	14	L15 and (parity near3 (error signal bit check)) same (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L176	14	L15 and (parity near3 (error signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L177	16	L15 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L178	47	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L179	1	L20 and (drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L180	3234820	(FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L181	1	L20 and (FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L182	2	controller near3 (open near2 drain) with (parity ECC) with controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L183	2	controller near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L184	2	(controller hub switch channel) near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L185	2	(controller hub switch channel) with (open near2 drain) with (parity ECC) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L186	2	(controller hub switch channel) with (open near2 drain) with (parity ECC redundancy (correct$3 near2 code)) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L187	99	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L188	6	(controller hub switch channel) with (open	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/04/22 10:13 PM

		near2 drain) with controller with (host computer node engine) same (parity ECC redundancy (correct$3 near2 code))	JPO; DERWENT; IBM_TDB)				
L189	24	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L190	31	L29 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L191	3	L32 and (parity ECC redundancy error (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L192	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/04/22 10:13 PM
L193	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/04/22 10:13 PM

L194	7	mardochee and filter near3 snoop	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/04/22 10:13 PM
L195	79	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L196	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L197	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L198	2	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) near5 ($3RAM DIM DIMM SODIMM)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L199	2	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L200	2	L41 and (error fault ECC)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L201	2	L41 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L202	2	L43 and (transistor $3FET drain$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/04/22 10:13 PM

			JPO; DERWENT; IBM_TDB)				
L203	2	L43 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L204	2	L45 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L205	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L206	2	L47 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L207	1	L47 and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L208	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L209	3	"20060062047".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L210	47193	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L211	52	L52 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L212	1	L53 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L213	1	L53 and (controller hub switch channel) same (open$3 near2 drain) same controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L214	19	L53 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L215	4	L56 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L216	13	L56 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L217	5	("20060262586" "20060062047").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L218	15	("9858218" "9311116" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L219	0	L61 and edge near3 connect$3 near5 ("not" "don't" "doesn't") near2 (active activat$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L220	33	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L221	84	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L222	105	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L223	16	L65 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L224	99	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L225	24	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L226	47193	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L227	52	L69 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L228	19	L70 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L229	13	L71 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L230	160	("3414781" "3560935" "4672570" "5388074" "5438536" "5511152" "5450576" "5606662" "5684979" "5835733" "6693840" "6754787" "6763437" "6886109" "7024518" "7065688" "7093115" "7155579" "7221699" "7266633" "7489163" "7525860" "7539909" "7568130" "7586350" "7647467" "7757101" "8074034"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

		"8139430" "8359521" "8429493" "20030115427" "20050071580" "20050193161" "200600062047" "20060262586" "20070091702" "20070136523" "20070214347" "20080098277" "20080147897" "20080155378" "20080256281" "20090119464" "20100005218" "20100042778" "20100142383" "20100202240" "20110022789").pn.					
L231	7	L74 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L232	770	"2" and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L233	2	L74 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L234	6	L75 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L235	237657	(G06F13/1694 or G06F12/0646 or G06F3/0619 or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2023/04/22 10:13 PM

		G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	IBM_TDB)				
L236	8346	L79 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L237	33	L80 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L238	16	L81 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L239	1	L82 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L240	0	L83 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L241	1	L82 and (handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L242	2	L82 and (FET MOSFET transistor p-junction n-	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/04/22 10:13 PM

		junction)	JPO; DERWENT; IBM_TDB)				
L243	0	L86 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L244	0	L87 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L245	65380	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L246	18713	L89 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L247	8	L90 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L248	0	L91 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L249	4	"6798891".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L250	47193	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L251	52	L96 and edg$3 near5	(US-PGPUB; USPAT;	OR	ON	ON	2023/04/22

		(wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				10:13 PM
L252	19	L97 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L253	13	L98 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L254	237657	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L255	8346	L100 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L256	33	L101 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L257	16	L102 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L258	1	L103 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L259	0	L104 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L260	65380	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L261	18713	L106 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L262	8	L107 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L263	0	L108 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L264	237657	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

		G11C29/78 or G11C2029/4402 or G11C2207/2254).cpc.					
L265	8346	L110 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L266	33	L111 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L267	4	L112 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L268	249	netlist.as.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L269	9	L114 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L270	1	L115 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L271	3	"20080098277".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L272	2	L117 and (transistor mosfet fet (discrete near2 element) source drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L273	0	L117 and (transistor mosfet fet (discrete near2 element) source drain gate) with (controller) with (parity error)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L274	0	L117 and (train$3 test$3 diagnosys sampl$3) near5 (signal input$4 output$4 sequence series operation command read$3 writ$4)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L275	1	L117 and (train$3 test$3 diagnosys sampl$3) near5 (mode signal input$4 output$4 sequence series operation command read$3 writ$4) with (transistor mosfet fet (discrete near2 element) source drain gate memory)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L276	0	L117 and (low near5 state)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L277	1	L117 and (low high) near5 (pull$3 state level impedance)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L278	1	L117 and edge	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L279	0	L117 and (edge pin connector) near5 (first primary second$3) near5 (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L280	0	L117 and (edge pin connector) near5 (first primary second$3) with (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L281	1	L117 and (edge pin connector) near5 (first primary second$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L282	1	L117 and (edge pin	(US-PGPUB; USPAT;	OR	ON	ON	2023/04/22

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		connector contact) with (active inactive enabl$3 disabl$3 off on)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				10:13 PM
L283	35	("20060277355"|"7411862"|"20030115427"|"20050071580"|"3414781"|"3560935"|"4672570"|"5388074"|"5438536"|"5450576"|"5511152"|"5606662"|"5684979"|"5835733"|"6693840"|"6754787"|"6763437"|"6886109"|"7024518"|"7065688"|"7093115"|"7155579"|"7221699"|"7266633"|"7489163"|"7525860"|"7539909"|"7568130"|"7586350"|"7647467"|"7757101"|"8074034"|"8139430"|"8359521"|"8429493").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2023/04/22 10:13 PM
L284	3	L139 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L285	0	L140 and controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L286	84	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L287	18	L142 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L288	15	L143 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L289	6	L144 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L290	6	L145 and (transistor $3FET drain$3) same (controller device microcontroller micro-	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

		controller)					
L291	6	L146 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L292	1	L147 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L293	326894	(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L294	103	((("NETLIST") near3 ("INC"))).AS,AANM.	(USPAT)	OR	ON	ON	2023/04/22 10:13 PM
L295	417	((("NETLIST") near3 ("INC"))).AS,AANM.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L296	15489	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2023/04/22 10:13 PM
L297	114436	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP,	OR	ON	ON	2023/04/22 10:13 PM

			AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L298	388	L149 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L299	15	L151 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L300	2	L153 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO,	OR	ON	ON	2023/04/22 10:13 PM

			RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L301	397	154 155 156	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L302	17	L157 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L303	17	L158 AND (transistor $3FET drain$3) SAME (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L304	3	L159 AND @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU,	OR	ON	ON	2023/04/22 10:13 PM

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			CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L305	326894	(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:39 PM
L306	388	L305 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:40 PM
L307	94	L306 AND (transistor $3FET drain$3) SAME (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL,	OR	ON	ON	2023/04/22 10:40 PM

			PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L308	17	L307 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:41 PM
L309	3	L308 AND @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:41 PM
L310	34	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L311	15	L1 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L312	85	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L313	18	L3 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L314	2	"8621170".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L315	2	("8489837" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L316	85	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L317	18	L9 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L318	9	L10 and (manufactur$3 industry) near3 standard	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L319	1	L10 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L320	34	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L321	5	L13 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L322	106	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L323	2	L15 and (parity near3 (error signal bit check)) with (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L324	14	L15 and (parity near3 (error signal bit check)) same (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L325	14	L15 and (parity near3 (error signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L326	17	L15 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L327	48	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L328	1	L20 and (drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L329	3281140	(FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L330	1	L20 and (FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L331	2	controller near3 (open near2 drain) with (parity ECC) with controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L332	2	controller near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L333	2	(controller hub switch channel) near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L334	2	(controller hub switch channel) with (open near2 drain) with (parity ECC) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L335	2	(controller hub switch channel) with (open near2 drain) with (parity ECC redundancy (correct$3 near2 code)) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L336	101	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L337	6	(controller hub switch channel) with (open	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/08/24 04:24 PM

		near2 drain) with controller with (host computer node engine) same (parity ECC redundancy (correct$3 near2 code))	JPO; DERWENT; IBM_TDB)				
L338	25	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L339	31	L29 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L340	3	L32 and (parity ECC redundancy error (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L341	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/08/24 04:24 PM
L342	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/08/24 04:24 PM

L343	8	mardochee and filter near3 snoop	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/08/24 04:24 PM
L344	80	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L345	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L346	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L347	2	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) near5 ($3RAM DIM DIMM SODIMM)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L348	2	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L349	2	L41 and (error fault ECC)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L350	2	L41 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L351	2	L43 and (transistor $3FET drain$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/08/24 04:24 PM

			JPO; DERWENT; IBM_TDB)				
L352	2	L43 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L353	2	L45 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L354	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L355	2	L47 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L356	1	L47 and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L357	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L358	3	"20060062047".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L359	48623	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L360	52	L52 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L361	1	L53 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L362	1	L53 and (controller hub switch channel) same (open$3 near2 drain) same controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L363	19	L53 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L364	4	L56 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L365	13	L56 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L366	5	("20060262586" "20060062047").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L367	15	("9858218" "9311116" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L368	0	L61 and edge near3 connect$3 near5 ("not" "don't" "doesn't") near2 (active activat$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L369	34	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L370	85	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L371	106	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L372	17	L65 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L373	101	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L374	25	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L375	48623	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L376	52	L69 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L377	19	L70 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L378	13	L71 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L379	161	("3414781" "3560935" "4672570" "5388074" "5438536" "5511152" "5450576" "5606662" "5684979" "5835733" "6693840" "6754787" "6763437" "6886109" "7024518" "7065688" "7093115" "7155579" "7221699" "7266633" "7489163" "7525860" "7539909" "7568130" "7586350" "7647467" "7757101" "8074034"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

		"8139430" "8359521" "8429493" "20030115427" "20050071580" "20050193161" "200600062047" "20060262586" "20070091702" "20070136523" "20070214347" "20080098277" "20080147897" "20080155378" "20080256281" "20090119464" "20100005218" "20100042778" "20100142383" "20100202240" "20110022789").pn.					
L380	7	L74 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L381	788	"2" and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L382	2	L74 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L383	6	L75 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L384	242229	(G06F13/1694 or G06F12/0646 or G06F3/0619 or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2023/08/24 04:24 PM

		G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	IBM_TDB)				
L385	8762	L79 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L386	33	L80 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L387	16	L81 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L388	1	L82 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L389	0	L83 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L390	1	L82 and (handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L391	0	L82 and (FET MOSFET transistor p-junction n-	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/08/24 04:24 PM

		junction)	JPO; DERWENT; IBM_TDB)				
L392	0	L86 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L393	0	L87 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L394	65726	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L395	18713	L89 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L396	8	L90 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L397	0	L91 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L398	4	"6798891".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L399	48623	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L400	52	L96 and edg$3 near5	(US-PGPUB; USPAT;	OR	ON	ON	2023/08/24

		(wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				04:24 PM
L401	19	L97 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L402	13	L98 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L403	242229	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L404	8762	L100 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L405	33	L101 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L406	16	L102 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L407	0	L103 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L408	0	L104 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L409	65726	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L410	18713	L106 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L411	8	L107 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L412	0	L108 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L413	242229	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

		G11C29/78 or G11C2029/4402 or G11C2207/2254).cpc.					
L414	8762	L110 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L415	33	L111 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L416	4	L112 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L417	250	netlist.as.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L418	9	L114 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L419	0	L115 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L420	3	"20080098277".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L421	2	L117 and (transistor mosfet fet (discrete near2 element) source drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L422	0	L117 and (transistor mosfet fet (discrete near2 element) source drain gate) with (controller) with (parity error)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L423	0	L117 and (train$3 test$3 diagnosys sampl$3) near5 (signal input$4 output$4 sequence series operation command read$3 writ$4)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L424	1	L117 and (train$3 test$3 diagnosys sampl$3) near5 (mode signal input$4 output$4 sequence series operation command read$3 writ$4) with (transistor mosfet fet (discrete near2 element) source drain gate memory)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L425	0	L117 and (low near5 state)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L426	1	L117 and (low high) near5 (pull$3 state level impedance)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L427	1	L117 and edge	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L428	0	L117 and (edge pin connector) near5 (first primary second$3) near5 (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L429	0	L117 and (edge pin connector) near5 (first primary second$3) with (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L430	1	L117 and (edge pin connector) near5 (first primary second$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L431	1	L117 and (edge pin	(US-PGPUB; USPAT;	OR	ON	ON	2023/08/24

		connector contact) with (active inactive enabl$3 disabl$3 off on)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				04:24 PM
L432	35	("20060277355"|"7411862"|"20030115427"|"20050071580"|"3414781"|"3560935"|"4672570"|"5388074"|"5438536"|"5450576"|"5511152"|"5606662"|"5684979"|"5835733"|"6693840"|"6754787"|"6763437"|"6886109"|"7024518"|"7065688"|"7093115"|"7155579"|"7221699"|"7266633"|"7489163"|"7525860"|"7539909"|"7568130"|"7586350"|"7647467"|"7757101"|"8074034"|"8139430"|"8359521"|"8429493").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2023/08/24 04:24 PM
L433	3	L139 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L434	0	L140 and controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L435	85	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L436	18	L142 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L437	15	L143 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L438	6	L144 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L439	6	L145 and (transistor $3FET drain$3) same (controller device microcontroller micro-	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

		controller)					
L440	6	L146 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L441	1	L147 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L442	334162	(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L443	104	((("NETLIST") near3 ("INC"))).AS,AANM.	(USPAT)	OR	ON	ON	2023/08/24 04:24 PM
L444	422	((("NETLIST") near3 ("INC"))).AS,AANM.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L445	15826	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2023/08/24 04:24 PM
L446	115728	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP,	OR	ON	ON	2023/08/24 04:24 PM

			AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L447	396	L149 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L448	15	L151 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L449	2	L153 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO,	OR	ON	ON	2023/08/24 04:24 PM

			RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L450	405	154 155 156	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L451	17	L157 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L452	17	L158 AND (transistor $3FET drain$3) SAME (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L453	3	L159 AND @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU,	OR	ON	ON	2023/08/24 04:24 PM

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			CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L454	34	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L455	15	L1 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L456	85	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L457	18	L3 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L458	2	"8621170".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L459	2	("8489837" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L460	85	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L461	18	L9 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L462	9	L10 and (manufactur$3 industry) near3 standard	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L463	1	L10 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2023/08/24 04:24 PM

			IBM_TDB)				
L465	5	L13 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L466	106	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L467	2	L15 and (parity near3 (error signal bit check)) with (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L468	14	L15 and (parity near3 (error signal bit check)) same (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L469	14	L15 and (parity near3 (error signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L470	17	L15 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L471	48	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L472	1	L20 and (drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L473	3281140	(FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L474	1	L20 and (FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L475	2	controller near3 (open near2 drain) with (parity ECC) with controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L476	2	controller near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L477	2	(controller hub switch channel) near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L478	2	(controller hub switch channel) with (open near2 drain) with (parity ECC) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L479	2	(controller hub switch channel) with (open near2 drain) with (parity ECC redundancy (correct$3 near2 code)) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L480	101	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L481	6	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) same (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L482	25	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L483	31	L29 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L484	3	L32 and (parity ECC redundancy error (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L485	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/08/24 04:24 PM

		"20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.					
L486	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/08/24 04:24 PM
L487	8	mardochee and filter near3 snoop	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/08/24 04:24 PM
L488	80	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L489	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L490	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L491	2	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) near5 ($3RAM DIM DIMM SODIMM)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L492	2	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L493	2	L41 and (error fault ECC)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L494	2	L41 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L495	2	L43 and (transistor $3FET drain$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L496	2	L43 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L497	2	L45 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L498	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L499	2	L47 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L500	1	L47 and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L501	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/08/24 04:24 PM

			JPO; DERWENT; IBM_TDB)				
L502	3	"20060062047".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L503	48623	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L504	52	L52 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L505	1	L53 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L506	1	L53 and (controller hub switch channel) same (open$3 near2 drain) same controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L507	19	L53 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L508	5	L56 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L509	13	L56 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L510	5	("20060262586" "20060062047").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L511	15	("9858218" "9311116"	(US-PGPUB; USPAT;	OR	ON	ON	2023/08/24

		"8489837").pn.	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				04:24 PM
L512	0	L61 and edge near3 connect$3 near5 ("not" "don't" "doesn't") near2 (active activat$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L513	34	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L514	85	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L515	106	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L516	17	L65 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L517	101	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L518	25	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L519	48623	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L520	52	L69 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

		(controller microcontroller micro-controller)					
L521	19	L70 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L522	13	L71 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L523	161	("3414781" "3560935" "4672570" "5388074" "5438536" "5511152" "5450576" "5606662" "5684979" "5835733" "6693840" "6754787" "6763437" "6886109" "7024518" "7065688" "7093115" "7155579" "7221699" "7266633" "7489163" "7525860" "7539909" "7568130" "7586350" "7647467" "7757101" "8074034" "8139430" "8359521" "8429493" "20030115427" "20050071580" "20050193161" "200600062047" "20060262586" "20070091702" "20070136523" "20070214347" "20080098277" "20080147897" "20080155378" "20080256281" "20090119464" "20100005218" "20100042778" "20100142383" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L524	7	L74 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L525	788	"2" and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L526	2	L74 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L527	6	L75 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L528	242229	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L529	8762	L79 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L530	33	L80 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

		($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)					
L531	0	L81 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L532	1	L82 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L533	0	L83 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L534	1	L82 and (handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L535	1	L82 and (FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L536	0	L86 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L537	0	L87 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L538	65726	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L539	18713	L89 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L540	8	L90 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L541	0	L91 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L542	4	"6798891".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L543	48623	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L544	52	L96 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L545	19	L97 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L546	13	L98 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L547	242229	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

		G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.					
L548	8762	L100 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L549	33	L101 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L550	16	L102 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L551	1	L103 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L552	0	L104 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L553	65726	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L554	18713	L106 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L555	8	L107 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

		controller) and drain$3					
L556	0	L108 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L557	242229	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2029/4402 or G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L558	8762	L110 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L559	33	L111 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L560	4	L112 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L561	250	netlist.as.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2023/08/24 04:24 PM

			IBM_TDB)				
L562	9	L114 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L563	1	L115 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L564	3	"20080098277".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L565	2	L117 and (transistor mosfet fet (discrete near2 element) source drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L566	0	L117 and (transistor mosfet fet (discrete near2 element) source drain gate) with (controller) with (parity error)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L567	0	L117 and (train$3 test$3 diagnosys sampl$3) near5 (signal input$4 output$4 sequence series operation command read$3 writ$4)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L568	1	L117 and (train$3 test$3 diagnosys sampl$3) near5 (mode signal input$4 output$4 sequence series operation command read$3 writ$4) with (transistor mosfet fet (discrete near2 element) source drain gate memory)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L569	0	L117 and (low near5 state)	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/08/24 04:24 PM

			JPO; DERWENT; IBM_TDB)				
L570	1	L117 and (low high) near5 (pull$3 state level impedance)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L571	1	L117 and edge	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L572	0	L117 and (edge pin connector) near5 (first primary second$3) near5 (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L573	0	L117 and (edge pin connector) near5 (first primary second$3) with (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L574	1	L117 and (edge pin connector) near5 (first primary second$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L575	1	L117 and (edge pin connector contact) with (active inactive enabl$3 disabl$3 off on)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L576	35	("20060277355"|"7411862"|"20030115427"|"20050071580"|"3414781"|"3560935"|"4672570"|"5388074"|"5438536"|"5450576"|"5511152"|"5606662"|"5684979"|"5835733"|"6693840"|"6754787"|"6763437"|"6886109"|"7024518"|"7065688"|"7093115"|"7155579"|"7221699"|"7266633"|"7489163"|"7525860"|"7539909"|"7568130"|"7586350"|"7647467"|"7757101"|"8074034"|"8139430"|"8359521"|"8429493").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2023/08/24 04:24 PM
L577	3	L139 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L578	0	L140 and controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L579	85	(handshak$3 hand-	(US-PGPUB; USPAT;	OR	ON	ON	2023/08/24

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		shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				04:24 PM
L580	18	L142 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L581	15	L143 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L583	6	L145 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L584	6	L146 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L585	1	L147 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L586	334162	(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L587	104	((("NETLIST") near3 ("INC"))).AS,AANM.	(USPAT)	OR	ON	ON	2023/08/24 04:24 PM
L588	422	((("NETLIST") near3 ("INC"))).AS,AANM.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY,	OR	ON	ON	2023/08/24 04:24 PM

			CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L589	15826	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2023/08/24 04:24 PM
L590	115728	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L591	396	L149 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L592	15	L151 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO,	OR	ON	ON	2023/08/24 04:24 PM

			MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L593	2	L153 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L594	8022937	154 155 156	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L595	17	L157 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L596	17	L158 AND (transistor $3FET drain$3) SAME	(US-PGPUB; USPAT; USOCR; FIT (AU, AP,	OR	ON	ON	2023/08/24 04:24 PM

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		(controller device microcontroller micro-controller)	AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L597	3	L159 AND @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L598	334162	(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L599	396	L305 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV,	OR	ON	ON	2023/08/24 04:24 PM

		controller)	MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L600	97	L306 AND (transistor $3FET drain$3) SAME (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L601	17	L307 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L602	3	L308 AND @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L603	282	("3414781" "3960935"	(US-PGPUB; USPAT;	OR	ON	ON	2023/08/24

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		"4672570" "5388074" "5438536" "5911152" "5450576" "5606662" "5684979" "5835733" "6363450" "6693840" "6754787" "6763437" "6886109" "7024518" "7065688" "7093115" "7155579" "1221699" "1222213" "1266633" "7411862" "7489163" "7925860" "7939909" "7968130" "7986350" "1647467" "1757101" "8054664" "8074034" "8139430" "8359521" "8386737" "8402208" "8407441" "8429493").pn.	USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				05:26 PM
L604	66	("8452917" "20030115427" "20050071580" "20050138302" "20050193161" "20060062047" "20060262586" "20060277355" "20070091702" "20070136523" "20070214347" "20080098277" "20080147897" "20080155378" "20080256281" "20090103373" "20090119464" "20100005218" "20100042778" "20100142383" "20100202240" "20110007585" "90110022789").pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 08:46 PM
L605	348	603 604	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2023/08/24 09:07 PM

			IBM_TDB)				
L606	5	605 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 09:08 PM
L607	5	606 AND (transistor $3FET drain$3) SAME (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 09:08 PM
L608	1	607 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 09:09 PM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N8	0	((controller circuit configured cause	(USPAT)	SAME	ON	ON	2016/02/18 12:10 AM

		memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.					
N59	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.	(USPAT)	SAME	ON	ON	2017/09/28 04:08 PM
N73	3	("9858218" "9311116" "8489837").pn.	(USPAT)	OR	ON	ON	2018/08/22 05:23 PM
N93	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system	(USPAT)	SAME	ON	ON	2019/08/05 02:40 PM

		memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.					
N94	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.	(USPAT)	SAME	ON	ON	2019/08/05 02:40 PM
N129	0	"20080098277".pn.	(USPAT)	OR	ON	ON	2021/02/20 09:05 PM
N130	1	(output$4 issu$3 broadcast$3) near5 (parity near3 error) with (output$4 issu$3 broadcast$3) near5 (train$3) with (open near3 (drain gate source transistor))	(USPAT)	OR	ON	ON	2021/09/10 08:58 PM
N131	1	(output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code	(USPAT)	OR	ON	ON	2021/09/10 09:03 PM

		instructionoperation)) same (output$4 issu$3 broadcast$3) near5 (train$3 test$3) near4 (signal operation code instruction) same ((open$3 clos$3 shun$4) near3 (drain gate source transistor))					
N132	148	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) and (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) and ((open$3 clos$3 shun$4) near3 (drain gate source transistor))	(USPAT)	OR	ON	ON	2021/09/10 09:10 PM
N133	145	N132 and @ad<"20090612"	(USPAT)	OR	ON	ON	2021/09/10 09:13 PM
N134	4	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) and (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) and ("same") near3 ((open$3 clos$3 shun$4) near3 (drain gate source transistor))	(USPAT)	OR	ON	ON	2021/09/10 09:14 PM
N135	4	N134 and @ad<"20090612"	(USPAT)	OR	ON	ON	2021/09/10 09:15 PM
N136	124	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) and (send$3 sent receiv$3 deliver$3	(USPAT)	OR	ON	ON	2021/09/10 09:15 PM

		output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) and ("same") near3 ((drain gate source transistor))					
N137	121	N136 and @ad<"20090612"	(USPAT)	OR	ON	ON	2021/09/10 09:17 PM
N138	0	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) same (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) same ("same") near3 ((drain gate source transistor))	(USPAT)	OR	ON	ON	2021/09/10 09:20 PM
N149	0	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) same (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) same ("same") near3 ((drain gate source transistor))	(USPAT)	OR	ON	ON	2022/02/12 02:59 PM

PE2E SEARCH - Search History (Similarity Search)

No Similarity Results available

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ISSUE FEE TRANSMITTAL FORM

APPLICATION #	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET #
17840593	06/14/2022	Hyun Lee	NL066-13US02

Title of Invention

MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

Application Information

APPLICATION TYPE	Nonprovisional Application under 35 USC 111(a)	DATE DUE	11/30/2023
CONFIRMATION #	3678	ISSUE FEE DUE	$ 1200
EXAMINER	MARDOCHEE CHERY	PUBLICATION DUE	$ 0
GROUP ART UNIT	2133	TOTAL FEES DUE	$1200
CLASS - SUBCLASS	711/154000	PREV. PAID FEE	$ 0
ENTITY STATUS	Regular Undiscounted		

1. CHANGE OF CORRESPONDENCE ADDRESS AND/OR INDICATION OF FEE ADDRESS (37 CFR 1.33 & 1.363)

Correspondence Address

CURRENT ADDRESS

Maintenance Fee Address

CURRENT ADDRESS

☐ Change of correspondence address requested,system generated AIA/122-PC form attached

☐ Fee address indication requested, system generatedSB/47-PC form attached

2. ENTITY STATUS

Change in Entity Status

NEW STATUS

3. THE FOLLOWING FEES ARE SUBMITTED

- [x] Issue Fee
- [x] Publication Fee

4. FEE AUTHORIZATION

- [ ] I authorize USPTO to apply my previously paid issue fee to the current fees due
- [ ] The Director is herby authorized to apply my previously paid issue fee to the current fee due and to charge deficient fees to Deposit Account Number:
- [x] If in addition to the payment of the issue fee amount submitted with this form, there are any discrepencies in any amount(s) due, the Director is authorized to charge any deficiency, or credit any overpayment, to Deposit Account Number: 603916

5. FIRM AND/OR ATTORNEY NAMES TO BE PRINTED

NOTE: If no name is listed, no name will be printed
For printing on the patent front page, list to be displayed as entered

USCH Law, PC

6. ASSIGNEE NAME(S) AND RESIDENCE DATA TO BE PRINTED

NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a susbstitute for filing an assignment.

Netlist, Inc.	Irvine, CA UNITED STATES	Corporation

Signature

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the

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Ex. 1002, p. 316

Patent and Trademark Office who has filed and has been granted power of attorney in this application. I also certify that this Fee(s) Transmittal form is being transmitted to the USPTO via Patent Center on the date indicated below.

Signature	Name	Registration #	Date
/Jamie J. Zheng/	Jamie Zheng	51167	11/29/2023

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Ex. 1002, p. 317

UNITED STATES
PATENT AND TRADEMARK OFFICE

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/840,593	**11/29/2023 09:52:15 PM Z ET**	**NL066-13US02**

Title of Invention

MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3678	FILED BY	Jamie Zheng
PATENT CENTER #	63429345	FILING DATE	06/14/2022
CUSTOMER #	79141	FIRST NAMED INVENTOR	Hyun Lee
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
web85b.pdf	3	Issue Fee Payment (PTO-85B)	61 KB
NL066-13US02_312_Amendment.pdf	7	Amendment after Notice of Allowance (Rule 312)	134 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
web85b.pdf	EF84C366BC18C8055768BBBD8D7066E625703D594376B3DE916D57B59880874EFE6ACE4EFA1028D8238B4FA09AF147FAEB

C8B32E65036C57160EDABA6C7EB4F2

NL066-13US02_312_Amendment.pdf	51E1D82AC73E7F439017A8CD0063EFEAA55C940ABADBD9D906A7960BD275491ABE3CADA8DD5375F005E2051A595B9F2A7B34C4220E6A12EDB5DB7E1B4255A37A

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES
PATENT AND TRADEMARK OFFICE

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/840,593	11/29/2023 09:52:15 PM Z ET	NL066-13US02

Title of Invention

MEMORY MODULE HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3678	FILED BY	Jamie Zheng
PATENT CENTER #	63429345	AUTHORIZED BY	-
CUSTOMER #	79141	FILING DATE	06/14/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Hyun Lee

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 2172	E2023ASL52526003	Jamie Zheng

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1501	UTILITY ISSUE FEE	1200.00	1	1200.00
			TOTAL AMOUNT:	$1,200.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C.

371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed November 29, 2023

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun LEE	Confirmation No.:	3678
Serial No.:	17/840,593	Group Art Unit:	2133
Filed:	June 14, 2022	Examiner:	Mardochee CHERY
For:	*MEMORY SUBSYSTEM HAVING OPEN-DRAIN OUTPUT FOR ERROR REPORTING AND FOR INITIALIZATION*	Attorney Docket No.:	NL066-13US02

AMENDMENT UNDER 37 C.F.R. 1.312

Mail Stop: Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Amendment is filed after the Notice of Allowance dated August 30, 2023, and is submitted under 37 C.F.R. 1.312.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 60-3916 (order no. NL066-13US02).

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Ex. 1002, p. 322

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory subsystem operable with a system memory controller of a host system, comprising:

dynamic random access memory elements on a printed circuit board and configurable to communicate data signals with the system memory controller; and

a memory subsystem controller on the printed circuit board and coupled to the dynamic random access memory elements, the memory subsystem controller having an open drain output, wherein the memory subsystem is configured to provide a first signaling interface via the open drain output during normal operations and a second signaling interface via the open drain output during an initialization operation including initialization operation sequences, wherein the second signaling interface is distinct from the first signaling interface and the initialization operation is distinct from any of the normal operations;

wherein, during the normal ~~memory read or write~~ operations, the memory subsystem controller is configured to receive address and command signals associated with the normal ~~memory read or write~~ operations and to control the dynamic random access memory elements in accordance with the address and command signals, and the memory subsystem controller is further configured to output via the open drain output a parity error signal in response to a parity error having occurred during the normal ~~memory read or write~~ operations; and

wherein, during the initialization operation, the memory subsystem controller is configured to output via the open drain output a signal related to one or more parts of the initialization operation sequences.

2. (Currently Amended) The memory subsystem of claim 1, wherein

the memory subsystem controller includes a transistor having an open drain coupled to the open drain output, a source coupled to ground, and a gate;

wherein the memory subsystem controller is configurable to apply a first signal to the gate of the transistor to indicate a parity error having occurred during the normal ~~memory read or write~~ operations; and

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wherein the memory subsystem controller is further configurable to apply a second signal related to the one or more parts of the initialization operation sequences to the gate of the transistor during the initialization operation.

3. (Previously Presented) The memory subsystem of claim 2, wherein the second signal drives the open drain output from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

4. (Previously Presented) The memory subsystem of claim 3, wherein the second signal drives the open drain output from the high impedance state to the low logic level and from the low logic level to the high impedance state.

5. (Previously Presented) The memory subsystem of claim 3, wherein the second signal drives the gate of the transistor high so as to drive the open drain output to the low logic level, and drives the gate of the transistor low so as to drive the open drain output to the high impedance state.

6. (Previously Presented) The memory subsystem of claim 5, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the open drain output and ground.

7. (Previously Presented) The memory subsystem of claim 2, wherein the memory subsystem controller comprises an integrated circuit that includes the transistor.

8. (Currently Amended) The memory subsystem of claim 2, wherein the memory subsystem controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, and wherein the memory subsystem controller is configurable to couple the first input to the output during the normal ~~memory read or write~~ operations, and to couple the second input to the output during the initialization operation.

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9. (Currently Amended) The memory subsystem of claim 1, wherein the dynamic random access memory elements are not accessed for any normal ~~memory read or write~~ operations by the system memory controller during the initialization operation.

10. (Previously Presented) The memory subsystem of claim 1, wherein the printed circuit board has edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the system memory controller, the edge connections including first edge connections via which the memory subsystem communicates data with the system memory controller, second edge connections via which the memory subsystem receives command/address signals from the system memory controller, and an open drain output pin coupled to the open drain output.

11. (Currently Amended) A method of operation in a host system having a system memory controller, comprising:

at a memory subsystem coupled to the system memory controller, the memory subsystem including a printed circuit board, a memory subsystem controller on the printed circuit board, and dynamic random access memory elements on the printed circuit board, the memory subsystem controller having an open drain output, wherein the memory subsystem is configured to provide a first signaling interface via the open drain output during normal operations and a second signaling interface via the open drain output during an initialization operation including initialization operation sequences, wherein the second signaling interface is distinct from the first signaling interface and the initialization operation is distinct from any of the normal operations,

performing the normal ~~memory read or write~~ operations, including receiving address and command signals associated with the normal ~~memory read or write~~ operations, controlling the dynamic random access memory elements in accordance with the address and command signals, and outputting via the open drain output a parity error signal in response to a parity error having occurred during the normal ~~memory read or write~~ operations; and

performing the initialization operation, including outputting via the open drain output a signal related to one or more parts of the initialization operation sequences.

12. (Currently Amended) The method of claim 11, wherein

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the memory subsystem controller includes a transistor having an open drain coupled to the open drain output, a source coupled to ground, and a gate;

outputting via the open drain output a parity error signal includes applying a first signal to the gate of the transistor to indicate the parity error having occurred during the normal ~~memory read or write~~ operations; and

outputting via the open drain a signal related to one or more parts of the initialization operation sequences includes applying a second signal related to the one or more parts of the initialization operation ~~training~~ sequences to the gate of the transistor during the initialization operation.

13. (Previously Presented) The method of claim 12, wherein the open drain output is driven by the second signal from a first state to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

14. (Previously Presented) The method of claim 12, wherein the open drain output is driven by the second signal from the high impedance state to the low logic level and from the low logic level to the high impedance state.

15. (Previously Presented) The method of claim 12, wherein the second signal drives the gate of the transistor high so as to drive the open drain output to the low logic level, and drives the gate of the transistor low so as to drive the open drain output to the high impedance state.

16. (Previously Presented) The method of claim 15, wherein the first signal drives the gate of the transistor high to provide a low impedance path between the open drain output and ground.

17. (Previously Presented) The method of claim 12, wherein the memory subsystem controller comprises an integrated circuit that includes the transistor.

18. (Currently Amended) The method of claim 12, wherein the memory subsystem controller further includes a multiplexor or logic circuit having an output coupled to the gate of the transistor, a first input to receive the first signal, and a second input to receive the second signal, the method further comprising coupling the first input to the output during the normal ~~memory~~

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~~read or write~~ operations, and coupling the second input to the output during the initialization operation.

19. (Currently Amended) The method of claim 11, wherein the dynamic random access memory elements are not accessed for any normal ~~memory read or write~~ operations by the system memory controller during the initialization operation.

20. (Previously Presented) The method of claim 11, wherein the printed circuit board has edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the system memory controller, the edge connections including first edge connections via which the memory subsystem communicates data with the system memory controller, second edge connections via which the memory subsystem receives command/address signals from the system memory controller, and an open drain output pin coupled to the open drain output.

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REMARKS

This amendment is submitted under 37 C.F.R. 1.312 and responds to the Notice of Allowance dated August 30, 2023, in which claims 1-20 are allowed.

REMARKS CONCERNING CLAIMS

Claims 1-2, 8-9, 11-12, and 18-19 have been amended to address potential antecedent basis issues.

The amendments do not add new matter and should not necessitate additional search or examination.

After entry of this amendment, the pending claims are: claims 1-20.

The Examiner is invited to call the undersigned attorney at (650) 521-4828 for any questions regarding this amendment and the application.

Respectfully submitted,

Date: November 29, 2023

/Jamie J. Zheng/ 51,167

Jamie J. Zheng (Reg. No.)

Customer No. 79141

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/840,593	06/14/2022	Hyun Lee	NL066-13US02	3678

79141 7590 12/11/2023

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER
CHERY, MARDOCHEE

ART UNIT	PAPER NUMBER
2133	

NOTIFICATION DATE	DELIVERY MODE
12/11/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com

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Ex. 1002, p. 329

Response to Rule 312 Communication	Application No.	Applicant(s)	
	17/840,593	Lee, Hyun	
	Examiner	Art Unit	AIA (FITF) Status
	MARDOCHEE CHERY	2133	Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☑ The amendment filed on 29 November 2023 under 37 CFR 1.312 has been considered, and has been:

a) ☐ entered.

b) ☐ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.

Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☑ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

f) ☐ not entered because the supplemental or corrected Application Data sheet (ADS)

☐ was not accompanied by a petition to accept an unintentionally delayed claim under 37 CFR 1.55 or 27 CFR 1.78;

☐ did not identify the information being changed in accordance with 37 CFR 1.76(c)(2);

☐ was not properly signed in accordance with 37 CFR 1.76(e) (or 37 CFR 1.33(b) for applications filed prior to September 16, 2012).

The amendment to claims 1-2, 8-9, 11-12, and 18-19 has substantially changed the scope of the claims and would not be entered.

/MARDOCHEE CHERY/ Primary Examiner, Art Unit 2133	12/04/2023

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	9	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/18 02:54 PM
L2	2	L1 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/18 02:55 PM
L3	50	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/18 02:57 PM
L4	3	L3 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/18 02:57 PM
L6	4	"8621170".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/05/19 06:18 PM
L7	2	("8489837" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2015/09/03 06:03 PM
L9	54	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:33 PM
L10	3	L9 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:33 PM
L11	1	L10 and (manufactur$3 industry) near3 standard	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:33 PM
L12	1	L10 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:35 PM
L13	9	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/03/02 05:36 PM
L14	5	L13 and	(US-PGPUB; USPAT;	OR	ON	ON	2016/03/02

		@ad<"20090612"	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				05:36 PM
L15	51	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:55 PM
L16	0	L15 and (parity near3 (error signal bit check)) with (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:57 PM
L17	0	L15 and (parity near3 (error signal bit check)) same (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:57 PM
L18	2	L15 and (parity near3 (error signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:57 PM
L19	2	L15 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/25 02:57 PM
L20	41	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 12:53 AM
L21	0	L20 and (drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 12:55 AM
L22	2094169	(FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 12:56 AM
L23	1	L20 and (FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 12:56 AM
L24	0	controller near3 (open near2 drain) with (parity ECC) with controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:17 AM
L25	0	controller near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:18 AM
L26	0	(controller hub switch channel) near5 (open	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2016/09/24 01:19 AM

		near2 drain) with (parity ECC) with controller near5 (host computer node engine)	JPO; DERWENT; IBM_TDB)				
L27	0	(controller hub switch channel) with (open near2 drain) with (parity ECC) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:19 AM
L28	0	(controller hub switch channel) with (open near2 drain) with (parity ECC redundancy (correct$3 near2 code)) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:20 AM
L29	47	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:20 AM
L30	0	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) same (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:21 AM
L31	2	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:21 AM
L32	31	L29 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:23 AM
L33	3	L32 and (parity ECC redundancy error (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/09/24 01:24 AM
L34	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2016/11/14 11:55 AM

		"6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.					
L35	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2016/11/14 11:57 AM
L36	3	mardochee and filter near3 snoop	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2016/11/14 11:59 AM
L37	71	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:00 PM
L38	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:06 PM
L39	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:08 PM
L40	2	L37 and edg$3 near5 (wire port connect$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2016/11/14 12:09 PM

		attach$5 bond$3 drain source gate pin) near5 ($3RAM DIM DIMM SODIMM)	JPO; DERWENT; IBM_TDB)				
L41	3	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:12 PM
L42	2	L41 and (error fault ECC)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:13 PM
L43	2	L41 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:13 PM
L44	2	L43 and (transistor $3FET drain$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:14 PM
L45	2	L43 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:15 PM
L46	2	L45 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:31 PM
L47	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:32 PM
L48	2	L47 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:32 PM
L49	1	L47 and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/14 12:35 PM
L50	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/05/24 02:13 PM

L51	3	"20060062047".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/05/24 02:41 PM
L52	27512	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:09 PM
L53	44	L52 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:11 PM
L54	0	L53 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:12 PM
L55	0	L53 and (controller hub switch channel) same (open$3 near2 drain) same controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:13 PM
L56	23	L53 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:13 PM
L57	14	L56 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:14 PM
L58	11	L56 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/28 04:19 PM
L60	5	("20060262586" "20060062047").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/09/29 12:37 AM
L61	14	("9858218" "9311116" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2018/08/22 05:23 PM

			IBM_TDB)				
L62	0	L61 and edge near3 connect$3 near5 ("not" "don't" "doesn't") near2 (active activat$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:31 PM
L63	14	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:32 PM
L64	78	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:32 PM
L65	66	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:32 PM
L66	6	L65 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:32 PM
L67	53	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:33 PM
L68	4	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:33 PM
L69	29963	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:34 PM
L70	48	L69 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:34 PM

		controller)					
L71	24	L70 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:34 PM
L72	12	L71 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/08/22 05:34 PM
L74	142	("3414781" "3560935" "4672570" "5388074" "5438536" "5511152" "5450576" "5606662" "5684979" "5835733" "6693840" "6754787" "6763437" "6886109" "7024518" "7065688" "7093115" "7155579" "7221699" "7266633" "7489163" "7525860" "7539909" "7568130" "7586350" "7647467" "7757101" "8074034" "8139430" "8359521" "8429493" "20030115427" "20050071580" "20050193161" "200600062047" "20060262586" "20070091702" "20070136523" "20070214347" "20080098277" "20080147897" "20080155378" "20080256281" "20090119464" "20100005218" "20100042778" "20100142383" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/03/15 01:19 PM
L75	7	L74 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/03/15 01:19 PM
L76	714	"2" and edg$3 near5	(US-PGPUB; USPAT;	OR	ON	ON	2019/03/15

		(wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				01:20 PM
L77	4	L74 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/03/15 01:20 PM
L78	6	L75 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/03/15 01:20 PM
L79	138210	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:42 PM
L80	4275	L79 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:42 PM
L81	30	L80 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:44 PM

		SODIMM) same (controller microcontroller micro-controller)					
L82	15	L81 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:45 PM
L83	1	L82 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:45 PM
L84	0	L83 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:46 PM
L85	1	L82 and (handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:46 PM
L86	4	L82 and (FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:47 PM
L87	2	L86 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:48 PM
L88	2	L87 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:52 PM
L89	48967	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:54 PM
L90	18643	L89 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:54 PM
L91	8	L90 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:55 PM

L92	0	L91 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/05 02:56 PM
L95	2	"6798891".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2019/08/11 12:39 PM
L96	36607	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L97	55	L96 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L98	25	L97 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L99	13	L98 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L100	162327	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM

		G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.					
L101	5271	L100 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L102	31	L101 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L103	15	L102 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L104	1	L103 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L105	0	L104 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:25 PM
L106	52734	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:26 PM
L107	18670	L106 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:26 PM
L108	8	L107 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:26 PM

		controller) and drain$3					
L109	0	L108 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:26 PM
L110	162327	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2029/4402 or G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:29 PM
L111	5271	L110 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:32 PM
L112	31	L111 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:32 PM
L113	6	L112 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:34 PM
L114	211	netlist.as.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2020/08/30 08:35 PM

			IBM_TDB)				
L115	6	L114 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:35 PM
L116	1	L115 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2020/08/30 08:36 PM
L117	3	"20080098277".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 09:06 PM
L118	2	L117 and (transistor mosfet fet (discrete near2 element) source drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 09:53 PM
L119	0	L117 and (transistor mosfet fet (discrete near2 element) source drain gate) with (controller) with (parity error)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 09:55 PM
L120	1	L117 and (train$3 test$3 diagnosys sampl$3) near5 (signal input$4 output$4 sequence series operation command read$3 writ$4)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 10:23 PM
L121	1	L117 and (train$3 test$3 diagnosys sampl$3) near5 (mode signal input$4 output$4 sequence series operation command read$3 writ$4) with (transistor mosfet fet (discrete near2 element) source drain gate memory)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 10:26 PM
L122	0	L117 and (low near5 state)	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2021/02/20 11:05 PM

			JPO; DERWENT; IBM_TDB)				
L123	1	L117 and (low high) near5 (pull$3 state level impedance)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:06 PM
L124	1	L117 and edge	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:21 PM
L125	0	L117 and (edge pin connector) near5 (first primary second$3) near5 (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:23 PM
L126	0	L117 and (edge pin connector) near5 (first primary second$3) with (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:23 PM
L127	1	L117 and (edge pin connector) near5 (first primary second$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:23 PM
L128	1	L117 and (edge pin connector contact) with (active inactive enabl$3 disabl$3 off on)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2021/02/20 11:26 PM
L139	35	("20060277355"|"7411862"|"20030115427"|"20050071580"|"3414781"|"3560935"|"4672570"|"5388074"|"5438536"|"5450576"|"5511152"|"5606662"|"5684979"|"5835733"|"6693840"|"6754787"|"6763437"|"6886109"|"7024518"|"7065688"|"7093115"|"7155579"|"7221699"|"7266633"|"7489163"|"7525860"|"7539909"|"7568130"|"7586350"|"7647467"|"7757101"|"8074034"|"8139430"|"8359521"|"8429493").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2022/02/12 02:59 PM
L140	2	L139 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:00 PM
L141	0	L140 and controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:01 PM
L142	101	(handshak$3 hand-	(US-PGPUB; USPAT;	OR	ON	ON	2022/02/12

		shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				03:18 PM
L143	13	L142 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:18 PM
L144	12	L143 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:19 PM
L145	4	L144 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:20 PM
L146	4	L145 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:21 PM
L147	4	L146 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:21 PM
L148	1	L147 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/12 03:26 PM
L149	304352	(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:04 PM

		G11C2029/4402 OR G11C2207/2254).cpc.					
L150	99	((("NETLIST") near3 ("INC"))).AS,AANM.	(USPAT)	OR	ON	ON	2022/09/28 06:05 PM
L151	406	((("NETLIST") near3 ("INC"))).AS,AANM.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:05 PM
L152	14962	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/09/28 06:06 PM
L153	107524	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:06 PM
L154	373	L149 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:07 PM
L155	14	L151 AND edg$3 near5	(US-PGPUB; USPAT;	OR	ON	ON	2022/09/28

		(wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				06:07 PM
L156	2	L153 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:07 PM
L157	381	154 155 156	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:07 PM
L158	15	L157 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO,	OR	ON	ON	2022/09/28 06:08 PM

			NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L159	15	L158 AND (transistor $3FET drain$3) SAME (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:08 PM
L160	3	L159 AND @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/28 06:09 PM
L161	33	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L162	15	L1 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L163	84	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L164	18	L3 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L165	2	"8621170".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L166	2	("8489837" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L167	84	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L168	18	L9 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L169	9	L10 and (manufactur$3 industry) near3 standard	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L170	1	L10 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L171	33	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L172	5	L13 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L173	105	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L174	2	L15 and (parity near3 (error signal bit check)) with (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L175	14	L15 and (parity near3 (error signal bit check)) same (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L176	14	L15 and (parity near3 (error signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L177	16	L15 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L178	47	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L179	1	L20 and (drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L180	3234820	(FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L181	1	L20 and (FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L182	2	controller near3 (open near2 drain) with (parity ECC) with controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L183	2	controller near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L184	2	(controller hub switch channel) near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L185	2	(controller hub switch channel) with (open near2 drain) with (parity ECC) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L186	2	(controller hub switch channel) with (open near2 drain) with (parity ECC redundancy (correct$3 near2 code)) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L187	99	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L188	6	(controller hub switch channel) with (open	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/04/22 10:13 PM

		near2 drain) with controller with (host computer node engine) same (parity ECC redundancy (correct$3 near2 code))	JPO; DERWENT; IBM_TDB)				
L189	24	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L190	31	L29 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L191	3	L32 and (parity ECC redundancy error (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L192	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/04/22 10:13 PM
L193	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/04/22 10:13 PM

L194	7	mardochee and filter near3 snoop	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/04/22 10:13 PM
L195	79	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L196	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L197	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L198	2	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) near5 ($3RAM DIM DIMM SODIMM)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L199	2	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L200	2	L41 and (error fault ECC)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L201	2	L41 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L202	2	L43 and (transistor $3FET drain$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/04/22 10:13 PM

			JPO; DERWENT; IBM_TDB)				
L203	2	L43 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L204	2	L45 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L205	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L206	2	L47 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L207	1	L47 and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L208	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L209	3	"20060062047".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L210	47193	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L211	52	L52 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L212	1	L53 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L213	1	L53 and (controller hub switch channel) same (open$3 near2 drain) same controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L214	19	L53 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L215	4	L56 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L216	13	L56 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L217	5	("20060262586" "20060062047").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L218	15	("9858218" "9311116" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L219	0	L61 and edge near3 connect$3 near5 ("not" "don't" "doesn't") near2 (active activat$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L220	33	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L221	84	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L222	105	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L223	16	L65 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L224	99	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L225	24	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L226	47193	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L227	52	L69 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L228	19	L70 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L229	13	L71 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L230	160	("3414781" "3560935" "4672570" "5388074" "5438536" "5511152" "5450576" "5606662" "5684979" "5835733" "6693840" "6754787" "6763437" "6886109" "7024518" "7065688" "7093115" "7155579" "7221699" "7266633" "7489163" "7525860" "7539909" "7568130" "7586350" "7647467" "7757101" "8074034"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

		"8139430" "8359521" "8429493" "20030115427" "20050071580" "20050193161" "200600062047" "20060262586" "20070091702" "20070136523" "20070214347" "20080098277" "20080147897" "20080155378" "20080256281" "20090119464" "20100005218" "20100042778" "20100142383" "20100202240" "20110022789").pn.					
L231	7	L74 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L232	770	"2" and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L233	2	L74 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L234	6	L75 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L235	237657	(G06F13/1694 or G06F12/0646 or G06F3/0619 or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2023/04/22 10:13 PM

		G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	IBM_TDB)				
L236	8346	L79 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L237	33	L80 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L238	16	L81 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L239	1	L82 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L240	0	L83 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L241	1	L82 and (handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L242	2	L82 and (FET MOSFET transistor p-junction n-	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/04/22 10:13 PM

		junction)	JPO; DERWENT; IBM_TDB)				
L243	0	L86 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L244	0	L87 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L245	65380	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L246	18713	L89 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L247	8	L90 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L248	0	L91 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L249	4	"6798891".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L250	47193	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L251	52	L96 and edg$3 near5	(US-PGPUB; USPAT;	OR	ON	ON	2023/04/22

		(wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				10:13 PM
L252	19	L97 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L253	13	L98 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L254	237657	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L255	8346	L100 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L256	33	L101 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L257	16	L102 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L258	1	L103 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L259	0	L104 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L260	65380	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L261	18713	L106 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L262	8	L107 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L263	0	L108 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L264	237657	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

		G11C29/78 or G11C2029/4402 or G11C2207/2254).cpc.					
L265	8346	L110 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L266	33	L111 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L267	4	L112 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L268	249	netlist.as.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L269	9	L114 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L270	1	L115 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L271	3	"20080098277".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

L272	2	L117 and (transistor mosfet fet (discrete near2 element) source drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L273	0	L117 and (transistor mosfet fet (discrete near2 element) source drain gate) with (controller) with (parity error)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L274	0	L117 and (train$3 test$3 diagnosys sampl$3) near5 (signal input$4 output$4 sequence series operation command read$3 writ$4)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L275	1	L117 and (train$3 test$3 diagnosys sampl$3) near5 (mode signal input$4 output$4 sequence series operation command read$3 writ$4) with (transistor mosfet fet (discrete near2 element) source drain gate memory)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L276	0	L117 and (low near5 state)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L277	1	L117 and (low high) near5 (pull$3 state level impedance)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L278	1	L117 and edge	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L279	0	L117 and (edge pin connector) near5 (first primary second$3) near5 (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L280	0	L117 and (edge pin connector) near5 (first primary second$3) with (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L281	1	L117 and (edge pin connector) near5 (first primary second$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L282	1	L117 and (edge pin	(US-PGPUB; USPAT;	OR	ON	ON	2023/04/22

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		connector contact) with (active inactive enabl$3 disabl$3 off on)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				10:13 PM
L283	35	("20060277355"|"7411862"|"20030115427"|"20050071580"|"3414781"|"3560935"|"4672570"|"5388074"|"5438536"|"5450576"|"5511152"|"5606662"|"5684979"|"5835733"|"6693840"|"6754787"|"6763437"|"6886109"|"7024518"|"7065688"|"7093115"|"7155579"|"7221699"|"7266633"|"7489163"|"7525860"|"7539909"|"7568130"|"7586350"|"7647467"|"7757101"|"8074034"|"8139430"|"8359521"|"8429493").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2023/04/22 10:13 PM
L284	3	L139 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L285	0	L140 and controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L286	84	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L287	18	L142 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L288	15	L143 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L289	6	L144 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L290	6	L145 and (transistor $3FET drain$3) same (controller device microcontroller micro-	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM

		controller)					
L291	6	L146 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L292	1	L147 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L293	326894	(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L294	103	((("NETLIST") near3 ("INC"))).AS,AANM.	(USPAT)	OR	ON	ON	2023/04/22 10:13 PM
L295	417	((("NETLIST") near3 ("INC"))).AS,AANM.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L296	15489	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2023/04/22 10:13 PM
L297	114436	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP,	OR	ON	ON	2023/04/22 10:13 PM

			AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L298	388	L149 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L299	15	L151 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L300	2	L153 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO,	OR	ON	ON	2023/04/22 10:13 PM

			RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L301	397	154 155 156	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L302	17	L157 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L303	17	L158 AND (transistor $3FET drain$3) SAME (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:13 PM
L304	3	L159 AND @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU,	OR	ON	ON	2023/04/22 10:13 PM

			CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L305	326894	(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:39 PM
L306	388	L305 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:40 PM
L307	94	L306 AND (transistor $3FET drain$3) SAME (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL,	OR	ON	ON	2023/04/22 10:40 PM

			PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L308	17	L307 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:41 PM
L309	3	L308 AND @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/04/22 10:41 PM
L310	34	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L311	15	L1 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L312	85	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L313	18	L3 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L314	2	"8621170".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L315	2	("8489837" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L316	85	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L317	18	L9 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L318	9	L10 and (manufactur$3 industry) near3 standard	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L319	1	L10 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L320	34	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L321	5	L13 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L322	106	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L323	2	L15 and (parity near3 (error signal bit check)) with (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L324	14	L15 and (parity near3 (error signal bit check)) same (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L325	14	L15 and (parity near3 (error signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L326	17	L15 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L327	48	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L328	1	L20 and (drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L329	3281140	(FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L330	1	L20 and (FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L331	2	controller near3 (open near2 drain) with (parity ECC) with controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L332	2	controller near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L333	2	(controller hub switch channel) near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L334	2	(controller hub switch channel) with (open near2 drain) with (parity ECC) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L335	2	(controller hub switch channel) with (open near2 drain) with (parity ECC redundancy (correct$3 near2 code)) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L336	101	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L337	6	(controller hub switch channel) with (open	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/08/24 04:24 PM

		near2 drain) with controller with (host computer node engine) same (parity ECC redundancy (correct$3 near2 code))	JPO; DERWENT; IBM_TDB)				
L338	25	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L339	31	L29 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L340	3	L32 and (parity ECC redundancy error (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L341	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/08/24 04:24 PM
L342	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/08/24 04:24 PM

L343	8	mardochee and filter near3 snoop	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/08/24 04:24 PM
L344	80	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L345	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L346	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L347	2	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) near5 ($3RAM DIM DIMM SODIMM)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L348	2	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L349	2	L41 and (error fault ECC)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L350	2	L41 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L351	2	L43 and (transistor $3FET drain$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/08/24 04:24 PM

			JPO; DERWENT; IBM_TDB)				
L352	2	L43 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L353	2	L45 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L354	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L355	2	L47 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L356	1	L47 and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L357	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L358	3	"20060062047".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L359	48623	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L360	52	L52 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L361	1	L53 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L362	1	L53 and (controller hub switch channel) same (open$3 near2 drain) same controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L363	19	L53 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L364	4	L56 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L365	13	L56 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L366	5	("20060262586" "20060062047").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L367	15	("9858218" "9311116" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L368	0	L61 and edge near3 connect$3 near5 ("not" "don't" "doesn't") near2 (active activat$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L369	34	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L370	85	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L371	106	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L372	17	L65 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L373	101	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L374	25	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L375	48623	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L376	52	L69 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L377	19	L70 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L378	13	L71 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L379	161	("3414781" "3560935" "4672570" "5388074" "5438536" "5511152" "5450576" "5606662" "5684979" "5835733" "6693840" "6754787" "6763437" "6886109" "7024518" "7065688" "7093115" "7155579" "7221699" "7266633" "7489163" "7525860" "7539909" "7568130" "7586350" "7647467" "7757101" "8074034"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

		"8139430" "8359521" "8429493" "20030115427" "20050071580" "20050193161" "200600062047" "20060262586" "20070091702" "20070136523" "20070214347" "20080098277" "20080147897" "20080155378" "20080256281" "20090119464" "20100005218" "20100042778" "20100142383" "20100202240" "20110022789").pn.					
L380	7	L74 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L381	788	"2" and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L382	2	L74 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L383	6	L75 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L384	242229	(G06F13/1694 or G06F12/0646 or G06F3/0619 or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2023/08/24 04:24 PM

		G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	IBM_TDB)				
L385	8762	L79 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L386	33	L80 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L387	16	L81 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L388	1	L82 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L389	0	L83 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L390	1	L82 and (handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L391	0	L82 and (FET MOSFET transistor p-junction n-	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/08/24 04:24 PM

		junction)	JPO; DERWENT; IBM_TDB)				
L392	0	L86 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L393	0	L87 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L394	65726	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L395	18713	L89 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L396	8	L90 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L397	0	L91 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L398	4	"6798891".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L399	48623	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L400	52	L96 and edg$3 near5	(US-PGPUB; USPAT;	OR	ON	ON	2023/08/24

		(wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				04:24 PM
L401	19	L97 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L402	13	L98 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L403	242229	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L404	8762	L100 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L405	33	L101 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L406	16	L102 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L407	0	L103 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L408	0	L104 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L409	65726	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L410	18713	L106 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L411	8	L107 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L412	0	L108 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L413	242229	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

		G11C29/78 or G11C2029/4402 or G11C2207/2254).cpc.					
L414	8762	L110 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L415	33	L111 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L416	4	L112 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L417	250	netlist.as.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L418	9	L114 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L419	0	L115 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L420	3	"20080098277".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L421	2	L117 and (transistor mosfet fet (discrete near2 element) source drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L422	0	L117 and (transistor mosfet fet (discrete near2 element) source drain gate) with (controller) with (parity error)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L423	0	L117 and (train$3 test$3 diagnosys sampl$3) near5 (signal input$4 output$4 sequence series operation command read$3 writ$4)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L424	1	L117 and (train$3 test$3 diagnosys sampl$3) near5 (mode signal input$4 output$4 sequence series operation command read$3 writ$4) with (transistor mosfet fet (discrete near2 element) source drain gate memory)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L425	0	L117 and (low near5 state)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L426	1	L117 and (low high) near5 (pull$3 state level impedance)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L427	1	L117 and edge	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L428	0	L117 and (edge pin connector) near5 (first primary second$3) near5 (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L429	0	L117 and (edge pin connector) near5 (first primary second$3) with (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L430	1	L117 and (edge pin connector) near5 (first primary second$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L431	1	L117 and (edge pin	(US-PGPUB; USPAT;	OR	ON	ON	2023/08/24

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		connector contact) with (active inactive enabl$3 disabl$3 off on)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				04:24 PM
L432	35	("20060277355"|"7411862"|"20030115427"|"20050071580"|"3414781"|"3560935"|"4672570"|"5388074"|"5438536"|"5450576"|"5511152"|"5606662"|"5684979"|"5835733"|"6693840"|"6754787"|"6763437"|"6886109"|"7024518"|"7065688"|"7093115"|"7155579"|"7221699"|"7266633"|"7489163"|"7525860"|"7539909"|"7568130"|"7586350"|"7647467"|"7757101"|"8074034"|"8139430"|"8359521"|"8429493").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2023/08/24 04:24 PM
L433	3	L139 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L434	0	L140 and controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L435	85	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L436	18	L142 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L437	15	L143 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L438	6	L144 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L439	6	L145 and (transistor $3FET drain$3) same (controller device microcontroller micro-	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

		controller)					
L440	6	L146 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L441	1	L147 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L442	334162	(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L443	104	((("NETLIST") near3 ("INC"))).AS,AANM.	(USPAT)	OR	ON	ON	2023/08/24 04:24 PM
L444	422	((("NETLIST") near3 ("INC"))).AS,AANM.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L445	15826	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2023/08/24 04:24 PM
L446	115728	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP,	OR	ON	ON	2023/08/24 04:24 PM

			AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L447	396	L149 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L448	15	L151 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L449	2	L153 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO,	OR	ON	ON	2023/08/24 04:24 PM

			RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L450	405	154 155 156	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L451	17	L157 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L452	17	L158 AND (transistor $3FET drain$3) SAME (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L453	3	L159 AND @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU,	OR	ON	ON	2023/08/24 04:24 PM

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			CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L454	34	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L455	15	L1 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L456	85	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L457	18	L3 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L458	2	"8621170".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L459	2	("8489837" "8489837").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L460	85	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L461	18	L9 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L462	9	L10 and (manufactur$3 industry) near3 standard	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L463	1	L10 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2023/08/24 04:24 PM

			IBM_TDB)				
L465	5	L13 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L466	106	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L467	2	L15 and (parity near3 (error signal bit check)) with (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L468	14	L15 and (parity near3 (error signal bit check)) same (host computer CPU node)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L469	14	L15 and (parity near3 (error signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L470	17	L15 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L471	48	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L472	1	L20 and (drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L473	3281140	(FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L474	1	L20 and (FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L475	2	controller near3 (open near2 drain) with (parity ECC) with controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L476	2	controller near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L477	2	(controller hub switch channel) near5 (open near2 drain) with (parity ECC) with controller near5 (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L478	2	(controller hub switch channel) with (open near2 drain) with (parity ECC) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L479	2	(controller hub switch channel) with (open near2 drain) with (parity ECC redundancy (correct$3 near2 code)) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L480	101	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L481	6	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) same (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L482	25	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L483	31	L29 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L484	3	L32 and (parity ECC redundancy error (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L485	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/08/24 04:24 PM

		"20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.					
L486	0	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/08/24 04:24 PM
L487	8	mardochee and filter near3 snoop	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	SAME	ON	ON	2023/08/24 04:24 PM
L488	80	("7266633" "7539909" "7065688" "5450576" "5684979" "6886109" "7024518" "7093115" "7489163" "8429493" "20050071580" "20070214347" "20100005218" "4672570" "5511152" "6763437" "7586350" "20030115427" "20070091702" "20080256281" "20090119464" "20100042778" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L489	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L490	3	L37 and edg$3 near3 (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L491	2	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) near5 ($3RAM DIM DIMM SODIMM)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L492	2	L37 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L493	2	L41 and (error fault ECC)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L494	2	L41 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L495	2	L43 and (transistor $3FET drain$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L496	2	L43 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L497	2	L45 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L498	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L499	2	L47 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L500	1	L47 and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L501	4	("20100202240" "20080256281").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/08/24 04:24 PM

			JPO; DERWENT; IBM_TDB)				
L502	3	"20060062047".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L503	48623	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L504	52	L52 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L505	1	L53 and (controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L506	1	L53 and (controller hub switch channel) same (open$3 near2 drain) same controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L507	19	L53 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L508	5	L56 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L509	13	L56 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L510	5	("20060262586" "20060062047").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L511	15	("9858218" "9311116"	(US-PGPUB; USPAT;	OR	ON	ON	2023/08/24

		"8489837").pn.	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				04:24 PM
L512	0	L61 and edge near3 connect$3 near5 ("not" "don't" "doesn't") near2 (active activat$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L513	34	(handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L514	85	(handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L515	106	controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L516	17	L65 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L517	101	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L518	25	(controller hub switch channel) with (open near2 drain) with controller with (host computer node engine) and (parity ECC redundancy (correct$3 near2 code))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L519	48623	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L520	52	L69 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

		(controller microcontroller micro-controller)					
L521	19	L70 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L522	13	L71 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L523	161	("3414781" "3560935" "4672570" "5388074" "5438536" "5511152" "5450576" "5606662" "5684979" "5835733" "6693840" "6754787" "6763437" "6886109" "7024518" "7065688" "7093115" "7155579" "7221699" "7266633" "7489163" "7525860" "7539909" "7568130" "7586350" "7647467" "7757101" "8074034" "8139430" "8359521" "8429493" "20030115427" "20050071580" "20050193161" "200600062047" "20060262586" "20070091702" "20070136523" "20070214347" "20080098277" "20080147897" "20080155378" "20080256281" "20090119464" "20100005218" "20100042778" "20100142383" "20100202240" "20110022789").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L524	7	L74 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L525	788	"2" and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L526	2	L74 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L527	6	L75 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L528	242229	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L529	8762	L79 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L530	33	L80 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

		($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)					
L531	0	L81 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L532	1	L82 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L533	0	L83 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L534	1	L82 and (handshak$3 hand-shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L535	1	L82 and (FET MOSFET transistor p-junction n-junction)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L536	0	L86 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L537	0	L87 and (error fault ECC) same (wire port connect$3 attach$5 bond$3 drain source gate pin)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L538	65726	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L539	18713	L89 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L540	8	L90 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

L541	0	L91 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L542	4	"6798891".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L543	48623	(controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L544	52	L96 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L545	19	L97 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L546	13	L98 AND ((G11C5/00 OR G11C16/26 OR G11C2029/4402 OR G11C29/78 OR G11C7/1066).CPC.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L547	242229	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G11C29/52 or G06F11/1068 or G06F3/0673 or G06F3/0659 or G06F3/0632 or G06F13/24 or G06F9/445 or G06F13/1668 or G11C7/1063 or G11C5/04 or G11C2029/4402 or	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

		G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2207/2254).cpc.					
L548	8762	L100 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L549	33	L101 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L550	16	L102 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L551	1	L103 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L552	0	L104 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L553	65726	(LEE near2 HYUN).in.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L554	18713	L106 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L555	8	L107 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM

		controller) and drain$3					
L556	0	L108 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L557	242229	(G06F13/1694 or G06F12/0646 or G06F3/0619 or G06F3/0632 or G06F3/0659 or G06F3/0673 or G06F11/1068 or G11C29/52 or G06F9/445 or G06F13/24 or G06F13/1668 or G11C5/04 or G11C7/1063 or G11C5/00 or G11C7/1066 or G11C16/26 or G11C29/78 or G11C2029/4402 or G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L558	8762	L110 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L559	33	L111 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L560	4	L112 and @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L561	250	netlist.as.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2023/08/24 04:24 PM

			IBM_TDB)				
L562	9	L114 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L563	1	L115 and (controller microcontroller micro-controller) same (memory $3RAM) with (read write pre-charg$3 precharg$3 refresh$3) and (transistor $3FET drain$3) same (controller device microcontroller micro-controller) and drain$3	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L564	3	"20080098277".pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L565	2	L117 and (transistor mosfet fet (discrete near2 element) source drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L566	0	L117 and (transistor mosfet fet (discrete near2 element) source drain gate) with (controller) with (parity error)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L567	0	L117 and (train$3 test$3 diagnosys sampl$3) near5 (signal input$4 output$4 sequence series operation command read$3 writ$4)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L568	1	L117 and (train$3 test$3 diagnosys sampl$3) near5 (mode signal input$4 output$4 sequence series operation command read$3 writ$4) with (transistor mosfet fet (discrete near2 element) source drain gate memory)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L569	0	L117 and (low near5 state)	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/08/24 04:24 PM

			JPO; DERWENT; IBM_TDB)				
L570	1	L117 and (low high) near5 (pull$3 state level impedance)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L571	1	L117 and edge	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L572	0	L117 and (edge pin connector) near5 (first primary second$3) near5 (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L573	0	L117 and (edge pin connector) near5 (first primary second$3) with (active inactive enabl$3 disabl$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L574	1	L117 and (edge pin connector) near5 (first primary second$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L575	1	L117 and (edge pin connector contact) with (active inactive enabl$3 disabl$3 off on)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L576	35	("20060277355"|"7411862"|"20030115427"|"20050071580"|"3414781"|"3560935"|"4672570"|"5388074"|"5438536"|"5450576"|"5511152"|"5606662"|"5684979"|"5835733"|"6693840"|"6754787"|"6763437"|"6886109"|"7024518"|"7065688"|"7093115"|"7155579"|"7221699"|"7266633"|"7489163"|"7525860"|"7539909"|"7568130"|"7586350"|"7647467"|"7757101"|"8074034"|"8139430"|"8359521"|"8429493").PN.	(US-PGPUB; USPAT)	OR	ON	ON	2023/08/24 04:24 PM
L577	3	L139 and (handshak$3 hand-shak$3) near3 memory near5 controller near5 host	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L578	0	L140 and controller near5 (open near2 drain near2 (I/O output))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L579	85	(handshak$3 hand-	(US-PGPUB; USPAT;	OR	ON	ON	2023/08/24

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		shak$3 (signal near3 (coordinat$3 arbitrat$3))) near7 memory near7 controller near7 host	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)				04:24 PM
L580	18	L142 and (initializ$5 POST BIOS boot$3 start$3) near3 mode	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L581	15	L143 and ((parity error) near5 (signal bit check))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L583	6	L145 and (transistor $3FET drain$3) same (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L584	6	L146 and (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L585	1	L147 and edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) same ($3RAM DIM DIMM SODIMM) same (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L586	334162	(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L587	104	((("NETLIST") near3 ("INC"))).AS,AANM.	(USPAT)	OR	ON	ON	2023/08/24 04:24 PM
L588	422	((("NETLIST") near3 ("INC"))).AS,AANM.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY,	OR	ON	ON	2023/08/24 04:24 PM

			CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L589	15826	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2023/08/24 04:24 PM
L590	115728	((("LEE") near3 ("Hyun"))).INV.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L591	396	L149 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L592	15	L151 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO,	OR	ON	ON	2023/08/24 04:24 PM

			MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L593	2	L153 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L594	8022937	154 155 156	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L595	17	L157 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L596	17	L158 AND (transistor $3FET drain$3) SAME	(US-PGPUB; USPAT; USOCR; FIT (AU, AP,	OR	ON	ON	2023/08/24 04:24 PM

		(controller device microcontroller micro-controller)	AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L597	3	L159 AND @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L598	334162	(G06F13/1694 OR G06F3/0619 OR G06F3/0632 OR G06F3/0659 OR G06F3/0673 OR G06F9/445 OR G06F11/1068 OR G06F12/0646 OR G06F13/1668 OR G06F13/24 OR G11C5/04 OR G11C7/1063 OR G11C29/52 OR G11C5/00 OR G11C7/1066 OR G11C16/26 OR G11C29/78 OR G11C2029/4402 OR G11C2207/2254).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L599	396	L305 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV,	OR	ON	ON	2023/08/24 04:24 PM

		controller)	MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L600	97	L306 AND (transistor $3FET drain$3) SAME (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L601	17	L307 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L602	3	L308 AND @ad<"20090612"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 04:24 PM
L603	282	("3414781" "3960935"	(US-PGPUB; USPAT;	OR	ON	ON	2023/08/24

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		"4672570" "5388074" "5438536" "5911152" "5450576" "5606662" "5684979" "5835733" "6363450" "6693840" "6754787" "6763437" "6886109" "7024518" "7065688" "7093115" "7155579" "1221699" "1222213" "1266633" "7411862" "7489163" "7925860" "7939909" "7968130" "7986350" "1647467" "1757101" "8054664" "8074034" "8139430" "8359521" "8386737" "8402208" "8407441" "8429493").pn.	USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				05:26 PM
L604	66	("8452917" "20030115427" "20050071580" "20050138302" "20050193161" "20060062047" "20060262586" "20060277355" "20070091702" "20070136523" "20070214347" "20080098277" "20080147897" "20080155378" "20080256281" "20090103373" "20090119464" "20100005218" "20100042778" "20100142383" "20100202240" "20110007585" "90110022789").pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 08:46 PM
L605	348	603 604	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2023/08/24 09:07 PM

			IBM_TDB)				
L606	5	605 AND (open$3 near2 drain)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 09:08 PM
L607	5	606 AND (transistor $3FET drain$3) SAME (controller device microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 09:08 PM
L608	1	607 AND edg$3 near5 (wire port connect$3 attach$5 bond$3 drain source gate pin) SAME ($3RAM DIM DIMM SODIMM) SAME (controller microcontroller micro-controller)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/08/24 09:09 PM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N8	0	((controller circuit configured cause	(USPAT)	SAME	ON	ON	2016/02/18 12:10 AM

		memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.					
N59	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.	(USPAT)	SAME	ON	ON	2017/09/28 04:08 PM
N73	3	("9858218" "9311116" "8489837").pn.	(USPAT)	OR	ON	ON	2018/08/22 05:23 PM
N93	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system	(USPAT)	SAME	ON	ON	2019/08/05 02:40 PM

		memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.					
N94	0	((controller circuit configured cause memory module enter$3 initialization mode in response command host computer system memory module execut$3 at least one initialization sequence during initialization mode) and (at least one output$3 defin$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output$3 notification signal indicat$3 status initialization mode memory controller via least output$4)).clm.	(USPAT)	SAME	ON	ON	2019/08/05 02:40 PM
N129	0	"20080098277".pn.	(USPAT)	OR	ON	ON	2021/02/20 09:05 PM
N130	1	(output$4 issu$3 broadcast$3) near5 (parity near3 error) with (output$4 issu$3 broadcast$3) near5 (train$3) with (open near3 (drain gate source transistor))	(USPAT)	OR	ON	ON	2021/09/10 08:58 PM
N131	1	(output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code	(USPAT)	OR	ON	ON	2021/09/10 09:03 PM

		instructionoperation)) same (output$4 issu$3 broadcast$3) near5 (train$3 test$3) near4 (signal operation code instruction) same ((open$3 clos$3 shun$4) near3 (drain gate source transistor))					
N132	148	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) and (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) and ((open$3 clos$3 shun$4) near3 (drain gate source transistor))	(USPAT)	OR	ON	ON	2021/09/10 09:10 PM
N133	145	N132 and @ad<"20090612"	(USPAT)	OR	ON	ON	2021/09/10 09:13 PM
N134	4	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) and (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) and ("same") near3 ((open$3 clos$3 shun$4) near3 (drain gate source transistor))	(USPAT)	OR	ON	ON	2021/09/10 09:14 PM
N135	4	N134 and @ad<"20090612"	(USPAT)	OR	ON	ON	2021/09/10 09:15 PM
N136	124	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) and (send$3 sent receiv$3 deliver$3	(USPAT)	OR	ON	ON	2021/09/10 09:15 PM

		output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) and ("same") near3 ((drain gate source transistor))					
N137	121	N136 and @ad<"20090612"	(USPAT)	OR	ON	ON	2021/09/10 09:17 PM
N138	0	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) same (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) same ("same") near3 ((drain gate source transistor))	(USPAT)	OR	ON	ON	2021/09/10 09:20 PM
N149	0	(send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (parity near3 (error signal code instructionoperation)) same (send$3 sent receiv$3 deliver$3 output$4 issu$3 broadcast$3) near5 (diagnosis diagnos$5 train$3 test$3) near4 (signal operation code instruction) same ("same") near3 ((drain gate source transistor))	(USPAT)	OR	ON	ON	2022/02/12 02:59 PM

PE2E SEARCH - Search History (Similarity Search)

No Similarity Results available

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
Sheet	1	of	9	Attorney Docket Number	129980-5066US02

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Examiner Signature	/MARDOCHEE CHERY/	Date Considered	08/24/2023

DB2/ 22684197.4

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 1, 2023	
				Application Number	17/840,593
				Filing Date	June 14, 2022
				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
Sheet	2	of	9	Attorney Docket Number	129980-5066US02

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Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review Case No. IPR2017-00548, Petition for Inter Partes Review of U.S. Patent No. 8,489,837, filed December 30, 2016.
		Inter Partes Review of U.S. Patent No. 8,489,837, Case No. IPR2017-00548, Exhibit 1003 "Declaration of Donald Alpert", filed December 30, 2016.
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				First Named Inventor	Hyun LEE
				Art Unit	2133
				Examiner Name	Mardochee CHERY
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				First Named Inventor	Hyun LEE
				Art Unit	2133
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				First Named Inventor	Hyun LEE
				Art Unit	2133
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				Art Unit	2133
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ISSUE NOTIFICATION

The projected patent number and issue date are specified above. The patent will issue electronically. The electronically issued patent is the official patent grant pursuant to 35 U.S.C. § 153. The patent may be accessed on or after the issue date through Patent Center at https://patentcenter.uspto.gov/. The patent will be available in both the public and the private sides of Patent Center. Further assistance in electronically accessing the patent, or about Patent Center, is available by calling the Patent Electronic Business Center at 1-888-217-9197.

The USPTO is implementing electronic patent issuance with a transition period, during which period the USPTO will mail a ceremonial paper copy of the electronic patent grant to the correspondence address of record. Additional copies of the patent (i.e., certified and presentation copies) may be ordered for a fee from the USPTO's Certified Copy Center at https://certifiedcopycenter.uspto.gov/index.html. The Certified Copy Center may be reached at (800)972-6382.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Center (https://patentcenter.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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