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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.062C1
		Application Number	
Title of Invention	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		
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Mailing Address of Inventor:						
Address 1		21 Thalia				
Address 2						
City	Ladera Ranch	State/Province	CA			
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Address 1	51 Discovery, #150		
Address 2			
City	Irvine	State/Province	CA
Country i	US	Postal Code	92618
Phone Number	949-435-0025	Fax Number	
Email Address	gsasaki@netlist.com		
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SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. App. No. 12/815,339, filed June 14, 2010, which claims the benefit of priority from U.S. Provisional App. No. 61/186,799, filed June 12, 2009, each of which is incorporated in its entirety by reference herein.

FIELD OF THE DISCLOSURE

[0002] The present disclosure relates to the operation of memory modules. Specifically, the present disclosure relates to systems and methods for handshaking with a memory module during or upon completion of initialization.

BACKGROUND OF THE DISCLOSURE

[0003] Memory subsystems such as memory modules are generally involved in the initialization procedure for computer systems, including servers, personal computers, and the like. For example, during system-wide initialization, the memory subsystems may undergo internal initialization procedures, or the system memory controller may otherwise interact with the memory subsystems during the initialization procedure. As part of this interaction, the system memory controller may request that the memory subsystem perform one or more requested tasks during system initialization.

SUMMARY

[0004] According to certain aspects, a memory module comprises at least one output configured to be operatively coupled to a memory controller of a host computer system. The memory module can be configured to operate in at least two modes comprising an initialization mode during which the memory module executes at least one initialization sequence and an operational mode. In certain embodiments, the memory module comprises a controller circuit configured to cause the memory module to enter the initialization mode. The memory module can also comprise a notification circuit configured to drive the at least one output while the memory module is in the initialization mode to provide at least one notification signal to the memory controller indicating at least one status of the at least one initialization sequence.

[0005] In another aspect, a method of using at least one memory module comprises providing a first memory module comprising at least one first output operatively coupled to a memory controller of a host computer system. The first memory module can be configured to operate in at least two modes comprising an initialization mode during which the first memory module executes at least one initialization sequence and an operational mode. The method can further comprise causing the first memory module to enter the initialization mode. In certain embodiments, the method comprises driving the at least one first output to a first state while the memory module executes the at least one initialization sequence. In certain embodiments, the method further comprises, upon completion of the at least one initialization sequence, driving the at least one first output to a second state different than the first state.

[0006] According to additional aspects, a method of using at least one memory module comprises providing a memory module comprising at least one output operatively coupled to a memory controller of a host computer system. In certain embodiments, the memory module is configured to operate in at least two modes comprising an initialization mode during which the memory module executes at least one initialization sequence and an operational mode. The method may comprise causing the memory module to enter the initialization mode. In some embodiments, the method comprises receiving a notification signal from the at least one output of the memory module, the notification signal indicating that the memory module has completed the at least one initialization sequence.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Figure 1 shows an example host computer system including an example memory module configured to perform handshaking with a memory controller of the host computer system according to certain embodiments described herein.

[0008] Figure 2 shows an example host computer system including example first and second memory modules configured to perform handshaking with a system memory controller of the host computer system according to certain embodiments described herein.

[0009] Figure 3 shows a host computer system including example first and second memory modules configured to perform handshaking with a memory controller of the host

system, where the notification circuits of the first and second memory modules have another example configuration according to certain embodiments described herein.

[0010] Figure 4 and Figure 5 show example methods of using at least one memory module according to certain embodiments described herein.

DETAILED DESCRIPTION

[0011] Existing initialization schemes have certain inefficiencies which lead to wasted time and expense. Thus, there is a need to reduce the time and complexity involved in system memory controller interactions with memory subsystems during initialization. Certain embodiments described herein advantageously satisfy at least a portion of this need by providing a system and method which utilizes a feedback path from a memory subsystem such as a memory module to a system memory controller, such as a Memory Controller Hub (MCH) of a computer system during initialization.

[0012] In general, there is no existing method of handshaking between the MCH (e.g., system memory controller) and a memory subsystem (e.g., memory module) during initialization. For example, in conventional systems, the system memory controller does not monitor the error-out signal from the memory subsystem. This causes the MCH to perform blind execution. In a typical server (e.g., an Intel or AMD or other chipset based server), the lack of any handshaking between the MCH and the memory subsystem during the server initialization period has not been a serious issue since the MCH generally has complete control over the initialization procedure. However, one possible configuration for LR-DIMM (Load Reduced DIMM) includes the MCH handing over one or more parts of the initialization operation sequence to the memory subsystem. This raises an unprecedented issue not addressed in conventional systems because, in such proposed configurations, the system can benefit from the MCH handshaking with the memory subsystem controller, as described more fully below.

[0013] Such an LR-DIMM configuration may have the MCH inserting a waiting period of predetermined length during which the MCH is idle and the memory subsystem controller undergoes initialization. However, one shortcoming of this LR-DIMM configuration would be that it requires the MCH to be in standby (idle, or wait) while the memory subsystem controller completes its task. Under such an arrangement, since the time

to complete a task can be dependent on the density, speed and configuration of the memory subsystem, and these parameters may be unknown to the MCH, the MCH may have to insert a single, predetermined standby period. In addition, if there are multiple occasions that the MCH needs to hand off control to the memory subsystem controller, the required MCH wait periods can be different from one occasion to another, and it complicates the correlation between the MCH and the memory subsystem controller. For example, the MCH according to such a scheme may give control to the local memory controller of a memory subsystem (e.g., memory module) for execution of a training sequence. The MCH may wait for a predetermined period of time and then assume that the local memory controller has completed the training sequence. However, depending on the memory subsystem parameters (e.g., memory capacity, speed, number of ranks, etc.), the time for actually completing the training sequence may vary and may be longer or shorter than predetermined period of time.

[0014] In general, handshaking can be implemented in at least two ways; polling and notifying. In the polling method, the MCH reads a status register in the memory subsystem controller to find out if the memory subsystem controller has completed the required or requested operation. For example, a status register may be read out through a serial interface such as System Management Bus (SMBus). However, a register polling method is generally inefficient because the system memory controller does not know exactly when the memory subsystem will have completed the required or requested operation. Thus, the system memory controller may wait longer than necessary to poll the memory subsystem, thereby delaying the overall initialization process. Additionally, the problem may be compounded because multiple training sequences or other initialization sequences may be run on the memory subsystem during a particular initialization period, resulting in accumulation of such unnecessary delays. Moreover, polling generally involves scheduling polling intervals during which the system memory controller is not performing other operations, resulting in further inefficiency.

[0015] Alternatively, the notifying method is an advantageous handshaking method between the MCH and the memory subsystem controller. According to a notifying method, the memory subsystem controller sends a signal to the MCH when the memory subsystem controller completes the required or requested operation. This method allows the

MCH to execute one or more independent commands while it is waiting for a notification signal from the memory subsystem controller.

[0016] Certain embodiments described herein provide a method of establishing a handshake mechanism based on notification signaling. In certain embodiments, this mechanism can be implemented by adding a new interface (notifying) signal between the MCH and the memory subsystem controller, or by adding an additional functionality to an existing, non-timing critical signal without altering the memory subsystem hardware. In either case, the interface between the MCH and the memory subsystem controller of certain embodiments can be an open drain signaling from the memory subsystem controller to the MCH, although a variety of other configurations are possible. As will be appreciated by persons skilled in the art, the terms MCH, system memory controller, and memory subsystem are used generally interchangeable throughout this disclosure, and the terms memory module, memory subsystem controller, and local memory controller are used generally interchangeably throughout this disclosure.

[0017] Figure 1 illustrates an example host computer system 16 including an example memory module 10 according to certain embodiments described herein. The memory module 10 can comprise at least one output 12 configured to be operatively coupled to a system memory controller 14 of the host computer system 16. In certain embodiments, the memory module 10 is configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode. The memory module 10 may further include a controller circuit 18. In some embodiments, the controller circuit 18 is configured to cause the memory module 10 to enter the initialization mode. The memory module 10 can further include a notification circuit 20 configured to drive the at least one output 12 while the memory module 10 is in the initialization mode to provide at least one notification signal to the memory controller 14 indicating at least one status of the at least one initialization sequence.

[0018] The memory module 10 may comprise a printed-circuit board (PCB) 22. In certain embodiments, the memory module 10 has a memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, 16-GB, or higher. Other memory capacities are also compatible with certain embodiments described herein. In addition, memory modules 10 having widths of

4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. The PCB 22 can have an industry-standard form factor. For example, the PCB 22 can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB 20 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB 22 has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FBDIMM), mini-DIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein. In other embodiments, certain non-DIMM form factors are possible such as, for example, single in-line memory module (SIMM), multi-media card (MMC), and small computer system interface (SCSI).

[0019] In certain embodiments, the memory module 10 is operatively coupled to (e.g., in electrical communication with) the host computer system 16. In certain other embodiments, the memory module 10 may communicate with the host computer system 16 using some other type of communication, such as, for example, optical communication. Examples of host computer systems 16 include, but are not limited to, blade servers, 1U servers, personal computers (PCs), and other applications in which space is constrained or limited. The PCB 22 can comprise an interface (not shown) that is configured to be in electrical communication with the host computer system 16. For example, the interface can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system 16. The interface of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory module 10 and the host system 16. For example, the interface can comprise a standard 240-pin DDR2 edge connector. The at least one output 12 may be routed over the interface, for example.

[0020] The memory module 10 may also comprise one or more memory elements (not shown), such as dynamic random-access memory (DRAM) elements, for example. Types of DRAM elements compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, DDR4, and synchronous DRAM (SDRAM). In addition,

memory elements having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Memory elements compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μ BGA), mini-BGA (mBGA), and chip-scale packaging (CSP). In certain embodiments, the memory module 10 may also include one or more non-volatile memory elements, such as one or more flash memory elements. Types of flash memory elements compatible with certain embodiments described herein include, but are not limited to, NOR flash, NAND flash, ONE-NAND flash, and multi-level cell (MLC).

[0021] The controller circuit 18 of certain embodiments generally controls the operation of the memory module 10. For example, the controller circuit 18 may control the memory elements of the memory module 10 and/or communicate with the system memory controller 14. For example, the controller circuit 18 may receive and process address and command signals (e.g., read, write commands) from the system memory controller 14 and transmit appropriate address and commands to the memory elements in response. See, e.g., U.S. Pat. Appl. Publ. Nos. 2006/0062047 A1 and 2006/0262586 A1, each of which is incorporated in its entirety by reference herein. In certain embodiments, the controller circuit 18 comprises a local memory controller. Additionally, depending on the architecture of the memory module 10, such as for an FB-DIMM, the controller circuit 18 may comprise an advanced memory buffer (AMB). The controller circuit 18 can comprise one or more of a field-programmable gate array (FPGA), a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, and a complex programmable logic device (CPLD), for example. In certain embodiments, the controller circuit 18 comprises various discrete electrical elements, while in certain other embodiments, the controller circuit 18 comprises one or more integrated circuits.

[0022] As discussed, the memory module 10 is configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode. In one embodiment, for example, the at least one initialization sequence may comprise one or more training sequences. The initialization sequence (e.g., comprising one or more training sequences) may be initiated by

the system memory controller 14. In some embodiments, the controller circuit 18 is configured to cause the memory module 10 to enter the initialization mode. For example, the controller circuit 18 may be configured to execute a routine implementing the at least one initialization sequence when the appropriate signal or command is received from the memory controller 14 or is otherwise received from the host computer system 16 (e.g., upon receipt of a reset signal).

[0023] In certain embodiments, for example, the computer system 16 is coupled to a plurality of memory modules 10, 26 including the memory module 10 and at least a second memory module 26, and the memory controller 14 (e.g., MCH) trains each module 10, 26 separately, in series. In one example scenario, the memory controller 14 issues a first command to the memory module 10, and, in response, the memory module 10 executes an initialization sequence (e.g., one or more training sequences). Upon completion of the initialization sequence, the first memory module 10 advantageously issues a notification to the memory controller 14 in accordance with embodiments described herein. In response, the memory controller 14 issues a second command, this time to the memory module 26, and, in response, the memory module 26 executes an initialization sequence (e.g., one or more training sequences). Upon completion of the initialization sequence, the second memory module 26, similar to the first memory module 10, advantageously issues a notification to the memory controller 14 in accordance with embodiments described herein. In response, where there are more than two memory modules 10, 26, the memory controller 14 issues a third command to a third memory module (not shown), and so forth. One example computer system 16 capable of implementing such a scenario is configured to execute an Intel Basic Input/Output System (BIOS), and comprises a plurality of memory modules 10, 26 having an LRDIMM configuration. In such an example system, the Intel BIOS causes the system memory controller 14 to initialize the LRDIMM memory modules 10, 26 serially.

[0024] The operational mode is the normal mode of the memory module 10. For example, during the operational mode, the memory module 10 is generally accessed by the system memory controller 14 of the host computer 16 during standard computer operation not associated with initialization. For example, the system memory controller 14 may cause the memory module 10 to perform standard operations such as memory read/write, pre-charge,

refresh, etc., while in operational mode, although it will be appreciated that one or more of these operations can also be performed by the memory module 10 while in initialization mode in certain embodiments.

[0025] The notification circuit 20 can be configured to drive the at least one output 12, while the memory module 10 is in the initialization mode or after the memory module 10 completes one or more initialization sequences, to provide the at least one notification signal to the memory controller 14 indicating at least one status of the at least one initialization sequence. While shown in Figures 1-3 as forming a part of the controller circuit 18, the notification circuit 20 may be a physically and/or logically separate circuit in certain embodiments. While a variety of configurations are possible, the notification circuit 20 may comprise one or more transistors, one or more logic elements (e.g., AND, OR, NOR, NAND, XOR gates, and the like), or a combination thereof. In some embodiments, the notification circuit 20 may additionally or alternatively comprise one or more of an FPGA, PLD, CPLD, ASIC, custom-designed semiconductor device, discrete electrical elements, and an integrated circuit.

[0026] The at least one status of certain embodiments comprises completion of the at least one initialization sequence, such that the at least one notification signal is indicative of the completion of the at least one initialization sequence. The at least one status of certain embodiments comprises execution of the at least one initialization sequence. For example, the at least one status may indicate that the at least one initialization sequence is currently being executed. In some embodiments, the at least one status may provide an indication that a certain task has been completed by the memory module 10, such as a training task requested by the system memory controller 14. In certain embodiments, the notification circuit 20 can be configured to drive the at least one output 12 to a first state indicative of execution of the at least one initialization sequence or to a second state indicative of completion of the at least one initialization sequence. As one example, the first state may be a high or low logic level, and the second state may be a high impedance state. In another case, the first state is a high or low logic level, and the second state is the inverse logic level of the first state.

[0027] The at least one output 12 of certain embodiments is configured to be operatively coupled to at least one interrupt of the system memory controller 14, and the

system memory controller 14 is responsive to the at least one notification signal indicating completion of the at least one initialization sequence. For example, the system memory controller 14 may trigger execution of an interrupt routine upon receipt of the notification signal on the output 12. The interrupt routine generally executes the appropriate operations for the at least one status indicated by the at least one notification signal. For example, if the at least one status indicates that the at least one initialization sequence is complete, execution of the interrupt routine may cause the system memory controller 14 to notify the host computer system 16 that the system initialization, or a portion thereof, is completed. In one embodiment, for example, the execution of the interrupt routine causes the system memory controller 14 to initiate a subsequent training sequence for the memory module 10 or on another memory module connected to the host system 16. For example, in one embodiment, a central processing unit (CPU) of the host system 16 (not shown) enters a “Wait” state after issuing a command to the memory module 10 to enter the initialization mode. Receipt of the at least one notification signal on the output 12 triggers execution of the interrupt routine, which interrupts the CPU, causing the “Wait” state to be aborted and allowing the host system 16 to continue operation. In this manner, generation of the interrupt on the at least one output 12 can allow completion of the at least one initialization sequence to receive generally immediate attention from the CPU and/or memory controller 14 of the host system 16. As will be appreciated, the CPU and memory controller 14 of the host system 16 may comprise separate modules, or may alternatively comprise a single integrated module, depending on the architecture of the host system 16 chip-set.

[0028] In certain embodiments, execution of the interrupt routine causes the system memory controller 14 to cause the memory module 10 to exit the initialization mode and to enter the operational mode. In another embodiment, the memory module 10 automatically enters the operational mode upon completion of the at least one initialization sequence without intervention from the memory controller 14.

[0029] In some embodiments, the at least one output 12 is operated in conformance with a standard (e.g., an industry standard) when the memory module 10 is in the operational mode, but is not operated in conformance with the standard when the memory module 10 is in the initialization mode. An example of a standard in accordance with certain

embodiments described herein is one or more of the industry standard promulgated by the Joint Electronic Devices Engineering Counsel (JEDEC). For example, the operation and behavior of the at least one output 12 may conform to an industry standard when the memory module 10 is in the operational mode, but the operation and behavior of the at least one output 12 may not conform to the industry standard when the memory module 10 is in the initialization mode. Because the at least one output 12 does not conform to the standard during initialization mode, an existing (e.g., JEDEC-specified) pin may be utilized to provide the at least one notification signal to the system memory controller 14 from the memory module 10 during the initialization mode. In one embodiment, for example, the at least one output 12 comprises an error-out pin of the memory module 10. In conventional systems, the operation of the error-out pin is undefined by the standard during initialization. However, in certain embodiments described herein, during the operational mode, the error-out pin may be used according a conventional industry standard (e.g., a JEDEC standard) to indicate a parity error has occurred in the memory module 10. During the initialization mode, the error-out pin can be used to transmit the at least one notification signal to the system memory controller 14.

[0030] It is advantageous to use the error-out pin for initialization status notification according to certain embodiments because the error-out pin can be asserted by the memory module 10 independent from system memory controller 14 requests or commands. Also, because the error-out pin is a JEDEC-specified pin, design cost and complexity are reduced because additional pin-outs and interrupt design changes can be avoided (e.g., in cases where such changes in hardware or chipset may not be feasible to provide the at least one status to the system memory controller 14). However, in certain other embodiments, providing the at least one status may be implemented by adding one or more pins to the system memory controller 14 (e.g., MCH) and to the controller circuit 18 (e.g., local memory controller), thereby utilizing changes in hardware or the chipset.

[0031] Moreover, the error-out pin may be coupled to an interrupt of the system memory controller 14 (e.g., according to the JEDEC standard). Thus, where the error-out pin is used, from the system point of view in accordance with certain embodiments, the notification of completion of the required or requested task from the memory module 10 (e.g., by the local memory controller) generates an interrupt communicated to the system during the

initialization period and indicative of completion of the required or requested task. Assertion of the same pin during normal (non-initialization) operation upon an error occurring, on the other hand, generates an interrupt communicated to the system during the normal operation indicative of the occurrence of the error condition. Thus, in certain embodiments, the error-out pin and corresponding signal memory module 10 can be used to support the notifying function and to provide the at least one status generally without changing hardware. Certain other such embodiments involve modifying the basic input/output system (BIOS) or other programming change. For example, the BIOS may be modified to indicate to the system memory controller 14 how to respond to the notification signal (e.g., to the error_out signal or the interrupt corresponding thereto).

[0032] In certain other embodiments, the at least one output 12 may include other existing (e.g., JEDEC specified) pins instead of, or in addition to, the error-out pin. In yet other configurations, at least one additional (e.g., non-JEDEC specified) pin may be employed. In general, any pin not otherwise active during the initialization mode may be used (e.g., high-order address pins, read/write pins, data pins, etc.).

[0033] The at least one output 12 can further be configured to be operatively coupled to at least one second output 24 of a second memory module 26 in some embodiments, as schematically illustrated in Figures 1-3. The second memory module 26 may be generally similar in structure and function to the memory module 10, and may comprise a controller circuit 28 and a notification circuit 30, for example. The second memory module 26 may be generally identical to the first memory module 10, or may have a different memory capacity, form factor, etc., than the first memory module 10. More than two such memory modules may be present in certain embodiments. As described above, the second memory module 26 can be configured to operate in at least two modes comprising an initialization mode during which the second memory module 26 executes at least one initialization sequence, and an operational mode. For example, the initialization and operational modes may be similar to those describe above in relation to the first memory module 10.

[0034] The second memory module 26 can also be configured to drive the at least one second output 24 to a third state indicative of execution of at least one initialization sequence of the second memory module 26 or to a fourth state indicative of completion of the

at least one initialization sequence of the second memory module 26. Additionally, in some embodiments, the at least one first output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are operatively coupled together by a bus 32 which is also operatively coupled to at least one input 34 of the system memory controller 14. In other embodiments (not shown), the at least one first output 12 and the at least one second output 24 are not coupled together, and are coupled to two separate inputs of the system memory controller 14.

[0035] Figure 2 shows an example host computer system 16 including example first and second memory modules 10, 26. As shown, the notification circuits 20, 30 of the first and second memory modules 10, 26 each comprise at least one transistor 36, 38. The at least one transistor 36, 38 can be in an open-drain configuration, as shown, although other configurations are possible. In certain such embodiments, the first state of the at least one first output 12 is a first logic level, the second state of the at least one first output 12 is a high-impedance state, the third state of the at least one second output 24 is the first logic level, and the fourth state of the at least one second output 24 is the high-impedance state. In the illustrated example, while the at least one initialization sequence is in progress, the first and second memory modules 10, 26 drive the gates of the respective transistors 36, 38 high. Thus, the transistors 36, 38 are respectively low impedance while the memory modules 10, 26 are executing each section of the initialization sequence, thereby pulling the first and second outputs 12, 24 low. Thus, the first state and the third state are low logic levels (ground) in the example configuration. Also, because the first and second outputs 12, 24 are coupled together by the bus 32, if the at least one initialization sequence of either one of the first and second memory modules 10, 26 are in progress, the bus 32 will be pulled to a low logic level.

[0036] As each of the two memory modules 10, 26 completes its at least one initialization sequence, it can drive the corresponding at least one first and second outputs 12, 24 respectively to a high impedance state. For example, once the at least one initialization sequence on each of the first and second memory modules 10, 26 is completed, the first and second memory modules 10, 26 can drive the gates of the respective transistors 36, 38 low, resulting in a high-impedance state on the at least one first and second outputs 12, 24 causing the bus 32 to be pulled high by the system memory controller 14. Accordingly, only once the

at least one initialization sequence of both the first and second memory modules 10, 26 are complete, the bus 32 will be pulled high by the internal pull-up configuration 40 of the system memory controller 14. The second state and the fourth state are therefore high-impedance values in the example embodiment. Thus, the system memory controller 14 can monitor the value on the bus 32 via the first input 34 to determine when both of the memory modules 10, 26 have completed the at least one initialization sequence. As discussed, in other configurations the at least one first and second outputs 12, 24 may be received on separate inputs of the system memory controller 14, and the status of the at least one initialization sequence of each memory module 10, 26 may be monitored independently.

[0037] As discussed above, in certain embodiments in which more than one memory module 10, 26 is connected to the system memory controller 14, each memory module 10, 26 or associated controller circuit 18 (e.g., local memory controller) causes the corresponding notification circuit 20, 30 to drive the at least one output 12, 24 to the high impedance state from the low impedance state when it completes the requested or required operation. Thus, in certain such embodiments, the system memory controller 14 (e.g., MCH) can only pull the notifying signal high when all memory modules 10, 26 or associated controller circuits (e.g., local memory controllers) have completed the required or requested operation (e.g., initialization sequence). This configuration allows the system memory controller 14 (e.g., MCH) to work with a non-homogenous memory subsystem. For example, the system memory controller 14 may be able to monitor the progress of multiple memory modules 10, 26 including a mix of DIMMs or other memory modules having differing characteristics, such as DIMM density, rank configurations, DRAM density, speed, DRAM configuration, etc.

[0038] Additionally, the at least one output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are configured to be operatively coupled to at least one interrupt of the system memory controller 14 in certain embodiments. In certain such embodiments, the system memory controller 14 can be responsive to the second state of the first memory module 10 and the fourth state of the second memory module 26 by triggering execution of an interrupt routine by a processor of the system memory controller 14. For example, in the example system of Figure 2, when the

bus 32 is pulled high by the pull-up configuration 40 indicating the second state of the first memory module 10 and the fourth state of the second memory module 26, the system memory controller 14 triggers execution of the interrupt routine.

[0039] In some embodiments, in which the at least one first output 12 and the at least one second output 24 are operatively coupled to separate inputs of the system memory controller 14, the at least one first output 12 and the at least one second output 24 may be operatively coupled to two separate interrupts. For example, the system memory controller 14 may be responsive to the second state of the first memory module 10 by triggering execution of a first interrupt routine associated with a first interrupt, and may be responsive to the fourth state of the second memory module 26 by triggering execution of a second interrupt routine associated with the second interrupt. In yet other embodiments, the separate inputs of the memory controller 14 are internally operatively coupled to the same interrupt, or are operatively coupled to separate interrupts which trigger the same interrupt routine.

[0040] Figure 3 shows a host computer system 16 including an example memory module 10 where the notification circuit 20 of the memory module 10 has another example configuration in accordance with certain embodiments described herein. In the example configuration of Figure 3, the at least one first output 12 is operatively coupled to an error-out pin of the memory module 10, and a multiplexor 42 drives the transistor 36 with either of a task_in_progress signal 44 or an error signal 46 (e.g., parity error signal). In one embodiment, for example, the multiplexor 42 may be configured to drive the transistor 36 with the task_in_progress signal 44 when the memory module 10 is in the initialization mode or is executing the at least one initialization sequence, and with the error signal 46 when the memory module 10 is in the operational mode. Thus, the memory module 10 can be advantageously configured to both perform the standard (e.g., JEDEC-specified) error reporting functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode, as described herein. As shown in Figure 3, a second memory module 26 including a similar configuration can also be operatively coupled to the host computer system 16. In certain embodiments, the at least one second output 24 of the second memory module 26 can be operatively coupled to the at least one first output 12 by the bus 32, as described above (e.g., with respect to Figure 2).

[0041] Figure 4 shows an example method 100 of using the at least one memory module 10 in accordance with certain embodiments described herein. While the description below of the method 100 refers to structure shown in Figures 1-3, other structures may also be used in accordance with certain embodiments described herein. At block 102, the method 100 of certain embodiments comprises providing a first memory module 10 comprising at least one first output 12 operatively coupled to a memory controller 14 of a host computer system 16. The first memory module 10 can be configured to operate in at least two modes comprising an initialization mode during which the first memory module 10 executes at least one initialization sequence, and an operational mode. For example, the at least one initialization sequence may comprise one or more steps of a series of steps associated with an initialization procedure of the host computer system 16.

[0042] At block 104, the method 100 in some embodiments comprises causing the first memory module 10 to enter the initialization mode. At block 106, the method 100 of certain embodiments comprises driving the at least one first output 12 to a first state while the memory module 10 executes the at least one initialization sequence. Upon completion of the at least one initialization sequence, the method of certain embodiments comprises driving the at least one first output 12 to a second state different than the first state. In certain embodiments, the first state is a first logic level and the second state is a high impedance state. Additionally, in certain embodiments, the at least one first output 12 is operatively coupled to at least one interrupt of the memory controller 14 such that driving the at least one output 12 to the second state triggers the memory controller to execute an interrupt routine.

[0043] In certain embodiments, the at least one output 12 is operated in conformance with JEDEC standard when the first memory module 10 is in the operational mode, but is not operated in conformance with the JEDEC standard when the first memory module 10 is in the initialization mode. The at least one first output 12 of certain embodiments include an error-out pin of the first memory module, for example.

[0044] The method 100 can further include providing a second memory module 26 comprising at least one second output 24 operatively coupled to the memory controller 14. The second memory module 26 can be configured to operate in one of at least two modes comprising an initialization mode, during which the second memory module 26 executes at

least one initialization sequence, and an operational mode. The method 100 can further include causing the second memory module 26 to enter the initialization mode. In certain embodiments, the method 100 also includes driving the at least one second output 24 of the second memory module 26 to a third state while the second memory module 26 executes the at least one initialization sequence. Upon completion of the at least one initialization sequence, the method 100 can further include driving the at least one second output 24 of the second memory module 26 to a fourth state different from the third state.

[0045] In certain embodiments, the at least one first output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are operatively coupled together by a bus 32 which is also operatively coupled to at least one input 34 of the memory controller 14. In certain other embodiments, the at least one first output 12 of the first memory module 10 is operatively coupled to a first input 34 of the memory controller 14 and the at least one second output 24 of the second memory module 26 is operatively coupled to a second input (not shown) of the memory controller 14.

[0046] Figure 5 shows another example method 200 of using at least one memory module 10 in accordance with certain embodiments described herein. At block 202, the method 200 may include providing a memory module 10 comprising at least one output 12 operatively coupled to a memory controller 14 of a host computer system 16. The memory module 10 may be configured to operate in at least two modes comprising an initialization mode, during which the memory module 10 executes at least one initialization sequence, and an operational mode.

[0047] The method 200 can further include causing the memory module 10 to enter the initialization mode at block 204. At block 206, the method 200 can include receiving a notification signal from the at least one output 12 of the memory module 10. The notification signal may indicate that the memory module 10 has completed the initialization sequence, for example. In certain embodiments, the method 200 further comprises executing an interrupt routine by the memory controller 14 in response to the notification signal.

Terminology / Alternative Embodiments

[0048] Embodiments have been described in connection with the accompanying drawings. However, it should be understood that the figures are not drawn to scale.

Distances, angles, etc. are merely illustrative and do not necessarily bear an exact relationship to actual dimensions and layout of the devices illustrated. In addition, the foregoing embodiments have been described at a level of detail to allow one of ordinary skill in the art to make and use the devices, systems, etc. described herein. A wide variety of variation is possible. Components, elements, and/or steps can be altered, added, removed, or rearranged. While certain embodiments have been explicitly described, other embodiments will become apparent to those of ordinary skill in the art based on this disclosure.

[0049] Conditional language used herein, such as, among others, "can," "could," "might," "may," "e.g.," and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment.

[0050] Depending on the embodiment, certain acts, events, or functions of any of the methods described herein can be performed in a different sequence, can be added, merged, or left out all together (e.g., not all described acts or events are necessary for the practice of the method). Moreover, in certain embodiments, acts or events can be performed concurrently, e.g., through multi-threaded processing, interrupt processing, or multiple processors or processor cores, rather than sequentially.

[0051] The various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein can be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. The described functionality can be implemented in varying ways for each particular application, but such

implementation decisions should not be interpreted as causing a departure from the scope of the disclosure.

[0052] The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein can be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor can be a microprocessor, but in the alternative, the processor can be any conventional processor, controller, microcontroller, or state machine. A processor can also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0053] The blocks of the methods and algorithms described in connection with the embodiments disclosed herein can be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module can reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, a hard disk, a removable disk, a CD-ROM, or any other form of computer-readable storage medium known in the art. An exemplary storage medium is coupled to a processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium can be integral to the processor. The processor and the storage medium can reside in an ASIC. The ASIC can reside in a user terminal. In the alternative, the processor and the storage medium can reside as discrete components in a user terminal.

[0054] Certain embodiments described herein are compatible with a memory system including memory devices with various attributes (see, e.g., Figures 2 and 3). For example, the memory system of certain embodiments may include various data slice sizes (e.g., two, four, eight, or 16 bit data slices) and corresponding memories (e.g., memories having two, four, eight, or 16 bit data widths).

[0055] Although certain embodiments and examples are discussed above, it is understood that the inventive subject matter extends beyond the specifically disclosed embodiments to other alternative embodiments and/or uses of the invention and obvious modifications and equivalents thereof. It is intended that the scope of the inventions disclosed herein should not be limited by the particular disclosed embodiments. Thus, for example, in any method or process disclosed herein, the acts or operations making up the method/process may be performed in any suitable sequence and are not necessarily limited to any particular disclosed sequence.

[0056] Various aspects and advantages of the embodiments have been described where appropriate. It is to be understood that not necessarily all such aspects or advantages may be achieved in accordance with any particular embodiment. Thus, for example, it should be recognized that the various embodiments may be carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other aspects or advantages as may be taught or suggested herein.

1. A memory module to be operatively coupled to a memory controller of a host computer system and configured to operate in at least two modes including an operational mode in which the memory module performs memory operations in response to memory commands from the memory controller in accordance with an industry standard, the memory module comprising:

a controller circuit configured to cause the memory module to enter an initialization mode during which the memory module executes at least one initialization sequence, the initialization mode being one of the at least two modes;

at least one output having a defined function in the operational mode according to the industry standard but is undefined by the industry standard in the initialization mode; and

a notification circuit outputting a notification signal indicating a status of the initialization mode to the memory controller via the at least one output.

2. The memory module of Claim 1, wherein the at least one status comprises completion of the at least one initialization sequence.

3. The memory module of Claim 1, wherein the at least one status comprises execution of the at least one initialization sequence.

4. The memory module of Claim 1, wherein the at least one output is configured to be operatively coupled to at least one interrupt of the memory controller.

5. The memory module of Claim 1, wherein the at least one notification signal triggers the memory controller to execute an interrupt routine.

6. The memory module of Claim 1, wherein the at least one output comprises an error-out pin of the memory module.

7. The memory module of Claim 1, wherein the notification circuit is configured to drive the at least one output to a first state indicative of execution of the at least one initialization sequence or to a second state indicative of completion of the at least one initialization sequence.

8. The memory module of Claim 7, wherein the at least one output is configured to be operatively coupled to at least one second output of a second memory module, the

second memory module configured to operate in at least two modes comprising an initialization mode during which the second memory module executes at least one initialization sequence and an operational mode, the second memory module configured to drive the at least one second output of the second memory module to a third state indicative of execution of the at least one initialization sequence of the second memory module or to a fourth state indicative of completion of the at least one initialization sequence of the second memory module.

9. The memory module of Claim 8, wherein the at least one output of the first memory module and the at least one second output of the second memory module are configured to be operatively coupled to at least one interrupt of the memory controller and the memory controller is responsive to the second state of the first memory module and the fourth state of the second memory module by triggering execution of an interrupt routine by a processor of the memory controller.

10. The memory module of Claim 8, wherein the first state is a first logic level, the second state is a high-impedance state, the third state is the first logic level, and the fourth state is the high-impedance state.

11. A method performed by a memory controller coupled to at least a first memory module, the memory module configured to operate in at least two modes including an operational mode in which the memory module performs memory operations in response to memory commands from the memory controller in accordance with an industry standard, the method comprising:

- outputting a command to the first memory module to cause the first memory module to enter an initialization mode during which the memory module executes at least one initialization sequence, the initialization mode being one of the at least two modes;

- receiving a notification signal from the first memory module indicating a status of the initialization mode; and

- executing an interrupt routine in response to the notification signal.

12. The method of Claim 11, wherein the notification signal is received from at least one first output of the first memory module, the at least one first output having a

defined function in the operational mode according to the industry standard but is undefined by the industry standard in the initialization mode

13. The method of Claim 11, wherein the notification signal indicates completion of the at least one initialization sequence.

14. The method of Claim 11, wherein the memory controller is further coupled to a second memory module and executing the interrupt routine comprises initiating a subsequent initialization sequence for one of the first memory module and the second memory module.

15. The method of Claim 11, wherein the at least one first output is a error-out pin of the first memory module.

SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

ABSTRACT OF THE DISCLOSURE

A memory module is operatively coupled to a memory controller of a host computer system and configured to operate in at least two modes including an operational mode in which the memory module performs memory operations in response to memory commands from the memory controller in accordance with an industry standard. The memory module comprises a controller circuit configured to cause the memory module to enter an initialization mode during which the memory module executes at least one initialization sequence, the initialization mode being one of the at least two modes. The memory module further comprises at least one output having a defined function in the operational mode according to the industry standard but is undefined by the industry standard in the initialization mode. During the initialization mode, the memory module is configured to output a notification signal indicating a status of the initialization mode to the memory controller via the at least one output. The memory controller is configured to execute an interrupt routine in response to the notification signal.

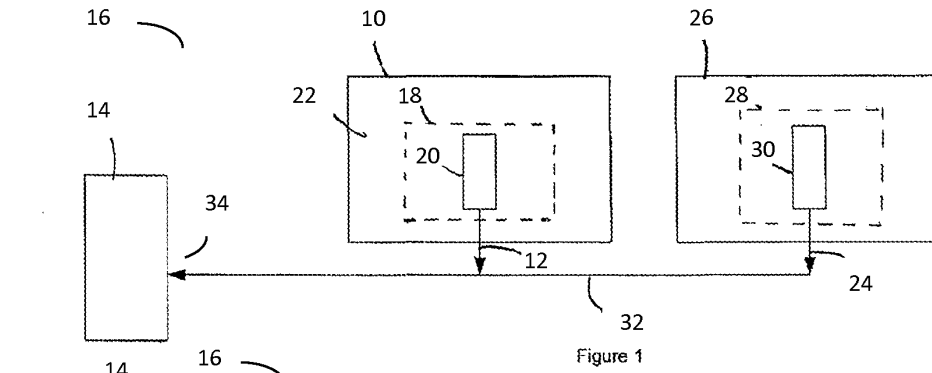


Figure 1

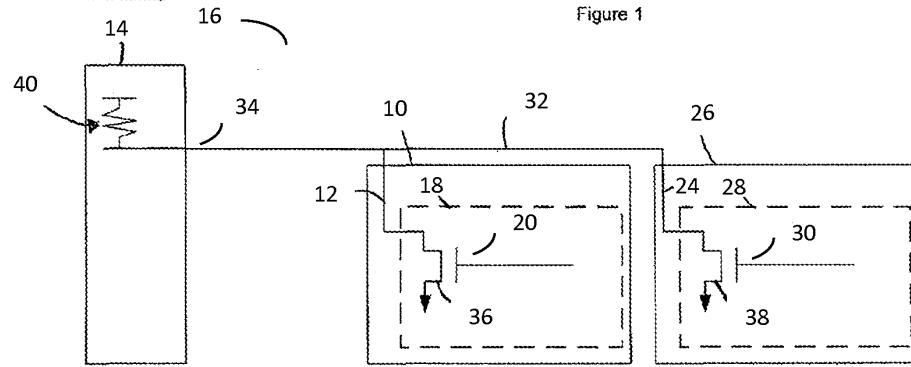


Figure 2

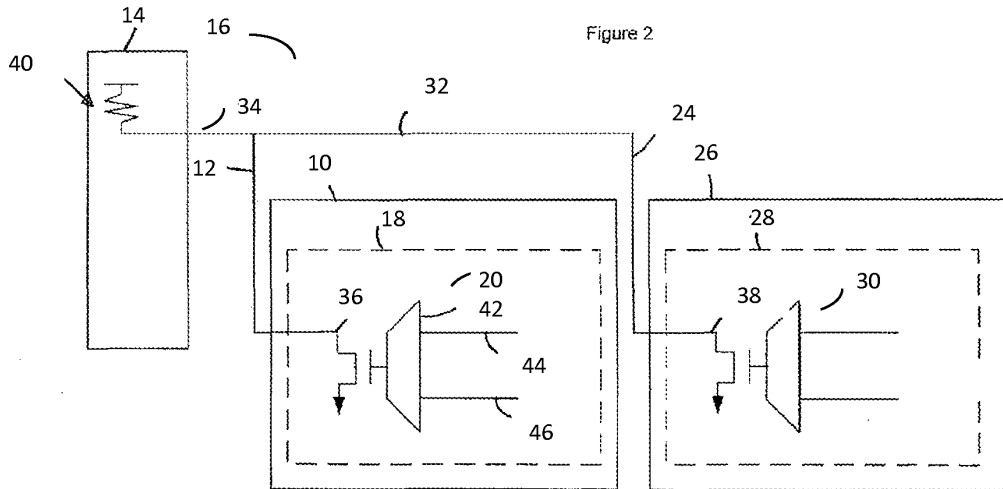


Figure 3

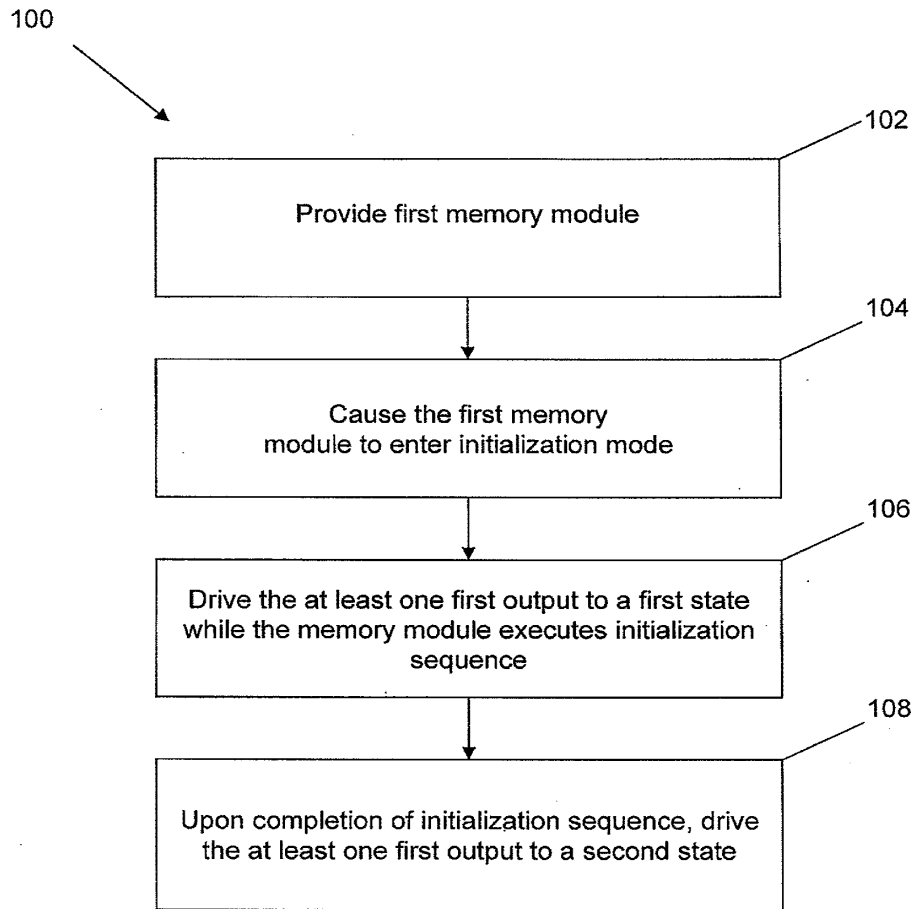


Figure 4

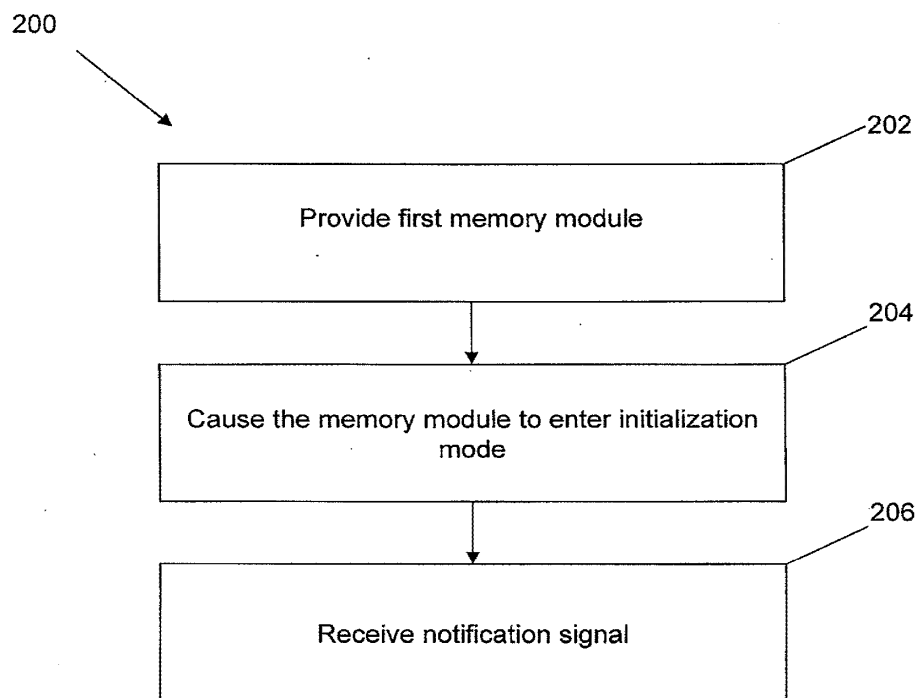


Figure 5

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		
First Named Inventor/Applicant Name:		Hyun Lee		
Filer:		Jamie Jie Zheng		
Attorney Docket Number:		NETL.062C1		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	70	70
Utility Search Fee	2111	1	300	300
Utility Examination Fee	2311	1	360	360
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
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Total in USD (\$)				730

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	2013-07-16_ApplicationDataSheet_NETL062C1.pdf	1437146 524c1e18aff05de63000aa07c3713a85afba89e8	no	6

Warnings:

Information:

2		2013-07-16_Specification_NET L062C1.pdf	3345182 cdc47954f8c17bb135c16e1a0746f7511c761be7	yes	24
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	Specification		1	20	
	Claims		21	23	
	Abstract		24	24	
Warnings:					
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3	Drawings-only black and white line drawings	2013-07-16_Drawings_NETL06 2C1.pdf	315352 a0b09f4c69e702af231499ca5c41de641049af6f	no	3
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Information:					
Total Files Size (in bytes):			5130487		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/942,721				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A				
SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A	300		N/A				
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	15	minus 20 = *	x 40 =	0.00	OR					
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *	x 210 =	0.00						
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00						
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	730		TOTAL				
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY DOCKET NO	TOT CLAIMS	IND CLAIMS
13/942,721	07/16/2013	2189	0.00	NETL.062C1	15	2

CONFIRMATION NO. 5636

79141

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

FILING RECEIPT



OC000000062979781

Date Mailed: 08/02/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Hyun Lee, Ladera Ranch, CA;

Applicant(s)

Netlist, Inc., Irvine, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 12/815,339 06/14/2010 PAT 8489837
which claims benefit of 61/186,799 06/12/2009

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 08/01/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/942,721**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

**** SMALL ENTITY ****

Title

SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/942,721	07/16/2013	Hyun Lee	NETL.062C1

CONFIRMATION NO. 5636

FORMALITIES LETTER

79141

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306



Date Mailed: 08/02/2013

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
Applicant must submit \$70 to complete the basic filing fee for a small entity.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- A surcharge (for late submission of the basic filing fee, search fee, examination fee or inventor's oath or declaration) as set forth in 37 CFR 1.16(f) of \$ **70** for a small entity in compliance with 37 CFR 1.27, must be submitted.

SUMMARY OF FEES DUE:

Total fee(s) required within **TWO MONTHS** from the date of this Notice is \$ **800** for a small entity

- \$ **70** Statutory basic filing fee.
- \$ **70** Surcharge.
- The application search fee has not been paid. Applicant must submit \$ **300** to complete the search fee.
- The application examination fee has not been paid. Applicant must submit \$ **360** to complete the examination fee for a small entity in compliance with 37 CFR 1.27.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):

page 1 of 2

Samsung Electronics Co., Ltd.

Ex. 1006, p. 42

Hyun Lee

Applicant may submit the inventor's oath or declaration at any time before the Notice of Allowance and Fee(s) Due, PTOL-85, is mailed.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.

<https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

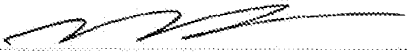
For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/fhadera/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

COMBINED DECLARATION AND ASSIGNMENT FOR UTILITY OR DESIGN APPLICATION	
Title of Invention	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
DECLARATION	
As a below named inventor, I hereby declare that:	
This declaration is directed to:	
☐ The attached application, or	
☒ United States application or PCT international application number 13/942,721 filed on July 16, 2013	
The above-identified application was made or authorized to be made by me.	
I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.	
I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.	
Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."	
ASSIGNMENT	
In consideration of the sum of One Dollar (\$1.00) and other good and valuable consideration paid, I hereby sell and assign to	
Netlist, Inc. (Name of Assignee)	
of 51 Discovery, Suite #150, Irvine, CA 92618 (Address of Assignee)	
(hereinafter designated as the Assignee) my entire right, title and interest for the United States as defined in 35 USC 100, for any invention set forth in the above-identified application.	
I agree to execute all papers necessary in connection with this application for patent in the USPTO for the invention, and any continuation, divisional or reissue applications thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient.	
I agree to execute all papers necessary in connection with any post-grant proceeding which may occur in connection with this application or continuation, divisional or reissue thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such post-grant proceeding.	

I agree to execute all papers and documents and perform any act which may be necessary in connection with claims or provisions of the International Convention for Protection of Industrial Property or similar agreements. I agree to perform all affirmative acts which may be necessary to obtain a grant of a valid United States patent to the Assignee. I hereby authorize and request the USPTO to issue any and all Letters Patents of the United States resulting from the application or any continuation, divisional or reissue applications thereof to the Assignee, as Assignee of my entire interest, and covenant that I have not executed, and will not execute, any agreement in conflict herewith.	
First Inventor (Legal Name): Hyun Lee Signature:  Date: 10/9/2013	

Electronic Patent Application Fee Transmittal				
Application Number:	13942721			
Filing Date:	16-Jul-2013			
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE			
First Named Inventor/Applicant Name:	Hyun Lee			
Filer:	Jamie Jie Zheng			
Attorney Docket Number:	NETL.062C1			
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	70	70
Utility Search Fee	2111	1	300	300
Utility Examination Fee	2311	1	360	360
Pages:				
Claims:				
Miscellaneous-Filing:				
Late Filing Fee for Oath or Declaration	2051	1	70	70
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with \$0 paid	2251	1	100	100
Miscellaneous:				
Total in USD (\$)				900

Electronic Acknowledgement Receipt	
EFS ID:	17174422
Application Number:	13942721
International Application Number:	
Confirmation Number:	5636
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062C1
Receipt Date:	19-OCT-2013
Filing Date:	16-JUL-2013
Time Stamp:	02:09:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 900
RAM confirmation Number	8593
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Oath or Declaration filed	2013-10-09_Declaration_NETLO 62C1.pdf	286314 ac827f939d7ed2ee5ec73035d1f3c9f0f8c5 09d	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	38705 7a467d5f7ef57d9bad616f171f0bdd3d3d6d 17d5	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			325019		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY DOCKET NO	TOT CLAIMS	IND CLAIMS
13/942,721	07/16/2013	2189	800	NETL.062C1	15	2

CONFIRMATION NO. 5636

UPDATED FILING RECEIPT



OC000000064603719

79141

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

Date Mailed: 10/29/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Hyun Lee, Ladera Ranch, CA;

Applicant(s)

Netlist, Inc., Irvine, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 12/815,339 06/14/2010 PAT 8489837
which claims benefit of 61/186,799 06/12/2009

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Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 08/01/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/942,721**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

**** SMALL ENTITY ****

Title

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Preliminary Class

711

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD						Application or Docket Number 13/942,721	
Substitute for Form PTO-875							
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	15	minus 20 = *	x 40 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *	x 210 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	730		TOTAL	
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE		
(Column 1)		(Column 2)		(Column 3)		OTHER THAN SMALL ENTITY	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist
App. No.	:	13/942,721
Filed	:	August 20, 2013
For	:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
Examiner	:	UNKNOWN
Art Unit	:	2189
Conf. No.	:	5636
Docket No.	:	NETL.062C1

PRELIMINARY AMENDMENT**Mail Stop Amendment**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

Applicant submits the following amendments and remarks in the above-identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

Amendments to the Claims: Begin on page 2 of this paper.

Remarks: Begin on page 7 of this paper.

In the Claims:

1. (Currently Amended) A memory module ~~to be operatively coupled to~~ operable with a memory controller of a host computer system ~~and configured to operate in at least two modes including in~~ an operational mode in which the memory module performs memory operations in response to memory commands from the memory controller in accordance with an industry standard, the memory module comprising:

a controller circuit configured to cause the memory module to enter an initialization mode in response to a command from the host computer system, ~~during which the memory module executes~~ executing at least one initialization sequence during the initialization mode, ~~the initialization mode being one of the at least two modes~~;

at least one output having a defined function in the operational mode according to the industry standard but is undefined by the industry standard in the initialization mode; and

a notification circuit outputting a notification signal indicating a status of the initialization mode to the memory controller via the at least one output.

2. (Previously Presented) The memory module of Claim 1, wherein the at least one status comprises completion of the at least one initialization sequence.

3. (Previously Presented) The memory module of Claim 1, wherein the at least one status comprises execution of the at least one initialization sequence.

4. (Cancelled)

5. (Previously Presented) The memory module of Claim 1, wherein the at least one notification signal triggers the memory controller to execute an interrupt routine.

6. (Previously Presented) The memory module of Claim 1, wherein the at least one output comprises an error-out pin of the memory module.

7. (Previously Presented) The memory module of Claim 1, wherein the notification circuit is configured to drive the at least one output to a first state indicative of execution

of the at least one initialization sequence or to a second state indicative of completion of the at least one initialization sequence.

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Currently Amended) A method performed by a memory controller coupled to at least a first memory module, the first memory module configured to ~~operate in at least two modes including an operational mode in which the memory module performs~~ perform memory operations in response to memory commands from the memory controller in accordance with an industry standard while operating in a first mode, the method comprising:

outputting a command to the first memory module to cause the first memory module to operate in a second mode so as to execute an internal procedure, whereby the memory controller hands off control of the internal procedure to the first memory module~~enter an initialization mode during which the memory module executes at least one initialization sequence, the initialization mode being one of the at least two modes;~~

receiving a notification signal ~~from the first memory module via at least one input of the memory controller~~ indicating a status of the internal procedure~~initialization mode, the at least one input of the memory controller being coupled to at least one output of the first memory module, the at least one output of the first memory module having a defined function according to the industry standard while the first memory module is operating in the first mode but is undefined by the industry standard while the first memory module is operating in the second mode;~~ and

resuming memory operations by issuing memory commands to the first memory module after receiving the notification signal~~executing an interrupt routine in response to the notification signal.~~

12. (Currently Amended) The method of Claim 11, wherein the memory controller enters a “Wait” state while the memory module executes the internal procedure and exits the “Wait” state in response to receiving the notification signal. ~~the notification signal is received from at least one first output of the first memory module, the at least one first output having a defined function in the operational mode according to the industry standard but is undefined by the industry standard in the initialization mode~~

13. (Currently Amended) The method of Claim 11, wherein the notification signal indicates completion of the internal procedure ~~at least one initialization sequence.~~

14. (Currently Amended) The method of Claim 11, wherein the memory controller is further coupled to a second memory module, the method further comprising: outputting a command to the second memory module to cause the second memory module to execute an internal procedure after receiving the notification signal and before resuming memory operations ~~and executing the interrupt routine comprises initiating a subsequent initialization sequence for one of the first memory module and the second memory module.~~

15. (Currently Amended) The method of Claim 11, wherein the at least one first output of the first memory module is an ~~a~~ error-out pin of the first memory module.

16. (New) A memory module operable with a memory controller of a host computer system in a first mode in which the memory module performs memory operations in response to memory commands from the memory controller in accordance with an industry standard, the memory module comprising:

a module controller circuit configured to cause the memory module to operate in a second mode in response to a command to execute an internal procedure from the host computer system;

at least one output having a defined function in the first mode according to the industry standard but is undefined by the industry standard in the second mode; and

a notification circuit outputting a notification signal indicating a status of the at least one internal procedure to the memory controller via the at least one output.

17. (New) The memory module of Claim 16, wherein the at least one status indicates completion of the internal procedure.
18. (New) The memory module of Claim 16, wherein the notification circuit is configured to drive the at least one output to a first state indicative of execution of the at least one internal procedure or to a second state indicative of completion of the internal procedure.
19. (New) The memory module of Claim 16, wherein the at least one notification signal is an open-drain signal.
20. (New) The memory module of Claim 16, wherein the at least one output comprises an error-out pin of the memory module.
21. (New) The memory module of claim 16, wherein the memory controller hands off control of to the module controller circuit by issuing the command to execute the internal procedure.
22. (New) The memory module of claim 16, wherein the module controller circuit is configured to process address and command signals from the memory controller in the first mode.
23. (New) The memory module of claim 16, wherein the notification circuit comprises a first input corresponding to the first mode, a second input corresponding to the second mode, and a multiplexor selecting between the first input and the second input based on whether the memory module is in the first mode or the second mode.
24. (New) The method of claim 11, wherein the at least one input of the memory controller is also coupled to at least one output of a second memory module, the at least one output of the second memory module having a defined function according to the industry standard while the second memory module is operating in a third mode but is

undefined by the industry standard while the second memory module is operating in a fourth mode, the second memory module in the third mode being configured to perform memory operations in response to memory commands from the memory controller in accordance with the industry standard, the second memory module being configured to execute an internal procedure in the fourth mode, and wherein the notification signal indicates completion of the internal procedure at the first memory module and completion of the internal procedure at the second memory module.

REMARKS

Claims 1 and 11-15 are amended. Claims 4 and 8-10 are cancelled. New claims 16-24 are presented. No new matter is added. After entry of this amendment, the pending claims are 1-3, 5-7, and 11-24.

The Examiner is invited to call the undersigned attorney at (650) 273-6008, if a telephone call could help resolve any issues.

Respectfully submitted,

Date: August 5, 2014

/Jamie J. Zheng/

51167

Jamie J. Zheng
Customer No. 79141

(Reg. No.)

Electronic Acknowledgement Receipt	
EFS ID:	19780354
Application Number:	13942721
International Application Number:	
Confirmation Number:	5636
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062C1
Receipt Date:	05-AUG-2014
Filing Date:	16-JUL-2013
Time Stamp:	16:01:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Preliminary Amendment	2014-08-05_Prelim_NETL062C1.pdf	103960	no	7
			771a272df3d64b4b2d542b7345f42a5532f2f1ab		
Warnings:					
Information:					

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 13/942,721		Filing Date 07/16/2013		☐ To be Mailed				
ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO													
APPLICATION AS FILED – PART I													
(Column 1)			(Column 2)										
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)					
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A		140					
☒ SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A		N/A		N/A		300					
☒ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A		360					
TOTAL CLAIMS (37 CFR 1.16(i))		15 minus 20 =		* 0		x \$40 =		0					
INDEPENDENT CLAIMS (37 CFR 1.16(h))		2 minus 3 =		* 0		x \$210 =		0					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).											
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))													
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL		800					
APPLICATION AS AMENDED – PART II													
(Column 1)			(Column 2)			(Column 3)							
AMENDMENT	08/05/2014		CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))		* 20		Minus	** 20		= 0		x \$40 =		0	
	Independent (37 CFR 1.16(h))		* 3		Minus	*** 3		= 0		x \$210 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))												
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
						TOTAL ADD'L FEE		0					
(Column 1)			(Column 2)			(Column 3)							
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))		*		Minus	**		=		x \$ =			
	Independent (37 CFR 1.16(h))		*		Minus	***		=		x \$ =			
	☐ Application Size Fee (37 CFR 1.16(s))												
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
						TOTAL ADD'L FEE							
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.													

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/942,721	07/16/2013	Hyun Lee	NETL.062C1	5636

79141	7590	05/22/2015
The Law Office of Jamie Zheng, Ph.D Esq. P.O. Box 60573 Palo Alto, CA 94306		

EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2133	

NOTIFICATION DATE	DELIVERY MODE
05/22/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jz@jzpatent.com

Office Action Summary	Application No. 13/942,721	Applicant(s) LEE, HYUN	
	Examiner Mardochee CHERY	Art Unit 2133	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08/05/2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-7 and 11-24 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-7 and 11-24 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☐ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413) |
| 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) | Paper No(s)/Mail Date. ____. |
| Paper No(s)/Mail Date ____. | 4) ☐ Other: ____. |

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Specification

1. The disclosure is objected to because of the following informalities:
corresponding patent number is missing for issued patent application referenced in paragraph 1 of the specification.

Appropriate correction is required.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit <http://www.uspto.gov/forms/>. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to <http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp>.

2. Claims 1-7 and 11-24 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-18 of **U.S. Patent #8489837**. Although the claims at issue are not identical, they are not patentably distinct from each other because claims 1-18 of **U.S. Patent #8489837** anticipate claims 1-7 and 11-24 of the current application.

3. "A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re

Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). “ ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee CHERY whose telephone number is (571)272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jared Ian Rutz can be reached on (571)272-5535. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Application/Control Number: 13/942,721
Art Unit: 2133

Page 5

May 18, 2015

/Mardochee CHERY/
Primary Examiner, Art Unit 2133

<i>Search Notes</i> 	Application/Control No. 13942721	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Search	5/18/15	MC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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<i>Index of Claims</i> 	Application/Control No. 13942721	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant			☐ CPA			☐ T.D.			☐ R.1.47		
CLAIM		DATE									
Final	Original	05/18/2015									
	1	✓									
	2	✓									
	3	✓									
	4	✓									
	5	✓									
	6	✓									
	7	✓									
	8	-									
	9	-									
	10	-									
	11	✓									
	12	✓									
	13	✓									
	14	✓									
	15	✓									
	16	✓									
	17	✓									
	18	✓									
	19	✓									
	20	✓									
	21	✓									
	22	✓									
	23	✓									
	24	✓									

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	9	(handshak\$3 hand-shak\$3) near3 memory near5 controller near5 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/18 14:54
L2	2	1 and (initializ\$5 POST BIOS boot\$3 start\$3) near3 mode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/18 14:55
L3	50	(handshak\$3 hand-shak\$3 (signal near3 (coordinat\$3 arbitrat\$3))) near7 memory near7 controller near7 host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/18 14:57
L4	3	3 and (initializ\$5 POST BIOS boot\$3 start\$3) near3 mode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/18 14:57
L5	1	4 and (manufactur\$3 industry) near3 standard	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/05/18 14:57

5/18/2015 2:58:07 PM**C:\Users\mchery\Documents\EAST\Workspaces\13942721.wsp**

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The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306



**Courtesy Reminder for
Application Serial No: 13/942,721**

Attorney Docket No: NETL.062C1

Customer Number: 79141

Date of Electronic Notification: 05/22/2015

This is a courtesy reminder that new correspondence is available for this application. If you have not done so already, please review the correspondence. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:

jz@jzpatent.com

To view your correspondence online or update your email addresses, please visit us anytime at <https://sportal.uspto.gov/secure/myportal/privatepair>. If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov or call 1-866-217-9197.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist
App. No.	:	13/942,721
Filed	:	July 16, 2013
For	:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
Examiner	:	CHERY, MARDOCHEE
Art Unit	:	2133
Conf. No.	:	5636
Docket No.	:	NETL.062C1

RESPONSE TO NON-FINAL OFFICE ACTION DATED MAY 22, 2015**Mail Stop Amendment**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

This submission is in response to the Non-Final Office Action dated May 22, 2015.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

Amendments to the Specification: Begin on page 2 of this paper.

Amendments to the Claims: Begin on page 3 of this paper.

Remarks: Begin on page 7 of this paper.

In the Specification:

Please replace Paragraph [0001] of the specification with the following:

[0001] This application is a continuation of U.S. App. No. 12/815,339, filed June 14, 2010, now U.S. Patent No. 8,489,837, which claims the benefit of priority from U.S. Provisional App. No. 61/186,799, filed June 12, 2009, each of which is incorporated in its entirety by reference herein.

In the Claims:

1. (Previously Presented) A memory module operable with a memory controller of a host computer system in an operational mode in which the memory module performs memory operations in response to memory commands from the memory controller in accordance with an industry standard, the memory module comprising:

a controller circuit configured to cause the memory module to enter an initialization mode in response to a command from the host computer system, the memory module executing at least one initialization sequence during the initialization mode;

at least one output having a defined function in the operational mode according to the industry standard but is undefined by the industry standard in the initialization mode; and

a notification circuit outputting a notification signal indicating a status of the initialization mode to the memory controller via the at least one output.

2. (Previously Presented) The memory module of Claim 1, wherein the at least one status comprises completion of the at least one initialization sequence.

3. (Previously Presented) The memory module of Claim 1, wherein the at least one status comprises execution of the at least one initialization sequence.

4. (Cancelled)

5. (Previously Presented) The memory module of Claim 1, wherein the at least one notification signal triggers the memory controller to execute an interrupt routine.

6. (Previously Presented) The memory module of Claim 1, wherein the at least one output comprises an error-out pin of the memory module.

7. (Previously Presented) The memory module of Claim 1, wherein the notification circuit is configured to drive the at least one output to a first state indicative of execution of the at least one initialization sequence or to a second state indicative of completion of the at least one initialization sequence.

8. (Cancelled)
9. (Cancelled)
10. (Cancelled)
11. (Previously Presented) A method performed by a memory controller coupled to at least a first memory module, the first memory module configured to perform memory operations in response to memory commands from the memory controller in accordance with an industry standard while operating in a first mode, the method comprising:
 - outputting a command to the first memory module to cause the first memory module to operate in a second mode so as to execute an internal procedure, whereby the memory controller hands off control of the internal procedure to the first memory module;
 - receiving a notification signal via at least one input of the memory controller indicating a status of the internal procedure, the at least one input of the memory controller being coupled to at least one output of the first memory module, the at least one output of the first memory module having a defined function according to the industry standard while the first memory module is operating in the first mode but is undefined by the industry standard while the first memory module is operating in the second mode; and
 - resuming memory operations by issuing memory commands to the first memory module after receiving the notification signal.
12. (Previously Presented) The method of Claim 11, wherein the memory controller enters a “Wait” state while the memory module executes the internal procedure and exits the “Wait” state in response to receiving the notification signal.
13. (Previously Presented) The method of Claim 11, wherein the notification signal indicates completion of the internal procedure.
14. (Previously Presented) The method of Claim 11, wherein the memory controller is further coupled to a second memory module, the method further comprising: outputting a command to the second memory module to cause the second memory module to

execute an internal procedure after receiving the notification signal and before resuming memory operations.

15. (Previously Presented) The method of Claim 11, wherein the at least one first output of the first memory module is an error-out pin of the first memory module.

16. (Previously Presented) A memory module operable with a memory controller of a host computer system in a first mode in which the memory module performs memory operations in response to memory commands from the memory controller in accordance with an industry standard, the memory module comprising:

- a module controller circuit configured to cause the memory module to operate in a second mode in response to a command to execute an internal procedure from the host computer system;

- at least one output having a defined function in the first mode according to the industry standard but is undefined by the industry standard in the second mode; and

- a notification circuit outputting a notification signal indicating a status of the at least one internal procedure to the memory controller via the at least one output.

17. (Previously Presented) The memory module of Claim 16, wherein the at least one status indicates completion of the internal procedure.

18. (Previously Presented) The memory module of Claim 16, wherein the notification circuit is configured to drive the at least one output to a first state indicative of execution of the at least one internal procedure or to a second state indicative of completion of the internal procedure.

19. (Previously Presented) The memory module of Claim 16, wherein the at least one notification signal is an open-drain signal.

20. (Previously Presented) The memory module of Claim 16, wherein the at least one output comprises an error-out pin of the memory module.

21. (Previously Presented) The memory module of claim 16, wherein the memory controller hands off control of to the module controller circuit by issuing the command to execute the internal procedure.
22. (Previously Presented) The memory module of claim 16, wherein the module controller circuit is configured to process address and command signals from the memory controller in the first mode.
23. (Previously Presented) The memory module of claim 16, wherein the notification circuit comprises a first input corresponding to the first mode, a second input corresponding to the second mode, and a multiplexor selecting between the first input and the second input based on whether the memory module is in the first mode or the second mode.
24. (Previously Presented) The method of claim 11, wherein the at least one input of the memory controller is also coupled to at least one output of a second memory module, the at least one output of the second memory module having a defined function according to the industry standard while the second memory module is operating in a third mode but is undefined by the industry standard while the second memory module is operating in a fourth mode, the second memory module in the third mode being configured to perform memory operations in response to memory commands from the memory controller in accordance with the industry standard, the second memory module being configured to execute an internal procedure in the fourth mode, and wherein the notification signal indicates completion of the internal procedure at the first memory module and completion of the internal procedure at the second memory module.

REMARKS

This amendment responds to the Non-Final Office Action dated May 22, 2015. In the Office Action, the Examiner:

- objected to the specification for informalities;
- rejected all pending claims on the ground of nonstatutory double patenting as being unpatentable over claims 1-18 of U.S. Patent No. 8,489,837.

I. OBJECTION TO THE SPECIFICATION

The specification is objected to for missing the corresponding patent number for issued patent application referenced in paragraph 1 of the specification. To address the objection, the specification has been amended by a replacement paragraph 1 with the patent number included.

I. REJECTION OF CLAIMS ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING

Applicant files herewith a terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) to overcome any nonstatutory double patenting rejection the Examiner may raise with regard to claims 1-3, 5-7, and 11-24.

Applicant submits that claims 1-3, 5-7, and 11-24 are in condition for allowance, and respectfully requests such action. The Examiner is invited to call the undersigned at (650) 273-6008 if such phone call would help resolve any remaining issues.

Respectfully submitted,

Date: August 23, 2015

/Jamie J. Zheng/

51167

Jamie J. Zheng
Customer No. 79141

(Reg. No.)

Electronic Patent Application Fee Transmittal				
Application Number:		13942721		
Filing Date:		16-Jul-2013		
Title of Invention:		SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		
First Named Inventor/Applicant Name:		Hyun Lee		
Filer:		Jamie Jie Zheng		
Attorney Docket Number:		NETL.062C1		
Filed as Small Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Statutory or Terminal Disclaimer	1814	1	160	160
Total in USD (\$)				160

Electronic Acknowledgement Receipt	
EFS ID:	23285090
Application Number:	13942721
International Application Number:	
Confirmation Number:	5636
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062C1
Receipt Date:	24-AUG-2015
Filing Date:	16-JUL-2013
Time Stamp:	02:25:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$160
RAM confirmation Number	8021
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer Filed	2015-08-23_Terminal_Disclaimer_NETL062C1.pdf	159918	no	2
			dcd48e1bef2ed3628f2d9b7dedf7068a466e5d1		
Warnings:					
Information:					
2		2015-08-23_Rsps_NFOA_NETL062C1.pdf	116176	yes	7
			320b92aa5a26d4a223be164ecb42c3b3f4907223		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Specification		2	2	
	Claims		3	6	
	Applicant Arguments/Remarks Made in an Amendment		7	7	
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30430	no	2
			7bf4f0dd71982710bd6bdd0c91103ac9bff97697		
Warnings:					
Information:					
Total Files Size (in bytes):			306524		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

TERMINAL DISCLAIMER TO OBTAIN A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) NETL.062C1
In re Application of: Netlist, Inc. Application No.: 13/942,721 Filed: July 16, 2013 For: SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE The applicant, <u>Netlist, Inc.</u>, owner of <u>100</u> percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent No. <u>8,489,837</u> as the term of said prior patent is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns. In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later: - expires for failure to pay a maintenance fee; - is held unenforceable; - is found invalid by a court of competent jurisdiction; - is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321; - has all claims canceled by a reexamination certificate; - is reissued; or - is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer. Check either box 1 or 2 below, if appropriate. 1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee. I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. 2. ☒ The undersigned is an attorney or agent of record. Reg. No. <u>51167</u> <u>/Jamie J. Zheng/</u> Signature <u>August 23, 2015</u> Date <u>Jamie J. Zheng</u> Typed or printed name <u></u> Title <u>650-273-6008</u> Telephone Number ☒ Terminal disclaimer fee under 37 CFR 1.20(d) included. WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.	

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 13/942,721		Filing Date 07/16/2013		☐ To be Mailed		
ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO										
APPLICATION AS FILED – PART I										
(Column 1)		(Column 2)								
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)		
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A		N/A		N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A				
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		X \$		=		
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		X \$		=		
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)		(Column 2)		(Column 3)						
AMENDMENT	08/24/2015		CLAIMS REMAINING AFTER AMENDMENT				HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA	
	Total (37 CFR 1.16(i))		* 20		Minus		** 20		= 0	
	Independent (37 CFR 1.16(h))		* 3		Minus		*** 3		= 0	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						RATE (\$)		ADDITIONAL FEE (\$)		
						X \$40 =		0		
						X \$210 =		0		
TOTAL ADD'L FEE						0				
(Column 1)		(Column 2)		(Column 3)						
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT				HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA	
	Total (37 CFR 1.16(i))		*		Minus		**		=	
	Independent (37 CFR 1.16(h))		*		Minus		***		=	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						RATE (\$)		ADDITIONAL FEE (\$)		
						X \$		=		
						X \$		=		
TOTAL ADD'L FEE										
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Application Number 	Application/Control No. 13/942,721	Applicant(s)/Patent under Reexamination LEE, HYUN	
Document Code - DISQ		Internal Document – DO NOT MAIL	

TERMINAL DISCLAIMER	☐ APPROVED	☒ DISAPPROVED
Date Filed : 8/24/15	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:

ANDRE ROBINSON

[X] We need a POA that gives power to the attorney who is signing the TD, along with another copy of the TD, unless they file a TD that is signed by the applicant.



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/942,721	07/16/2013	Hyun Lee	NETL.062C1	5636

79141	7590	11/16/2015
The Law Office of Jamie Zheng, Ph.D Esq. P.O. Box 60573 Palo Alto, CA 94306		

EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2133	

NOTIFICATION DATE	DELIVERY MODE
11/16/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jz@jzpatent.com
eofficeaction@appcoll.com

Office Action Summary	Application No. 13/942,721	Applicant(s) LEE, HYUN	
	Examiner Mardochee CHERY	Art Unit 2133	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 8/24/15.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-7 and 11-24 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-7 and 11-24 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 4) ☐ Other: ____.

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

Terminal Disclaimer

2. This application was filed before September 16, 2012. The person who signed the terminal disclaimer is not an attorney or agent of record, is not recognized as an officer of the assignee, and has not been established as being authorized to act on behalf of the assignee. See MPEP § 324. We need a POA that gives power to the attorney who is signing the TD, along with another copy of the TD, unless they file a TD that is signed by the applicant. Thus, claims 1-7 and 11-24 stand rejected under the nonstatutory double patenting statute.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*,

686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit <http://www.uspto.gov/forms/>. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to <http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp>.

4. Claims 1-7 and 11-24 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-18 of **U.S. Patent #8489837**. Although the claims at issue are not identical, they are not patentably distinct from each other because claims 1-18 of **U.S. Patent #8489837** anticipate claims 1-7 and 11-24 of the current application.
5. "A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at

896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). “ ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee CHERY whose telephone number is (571)272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jared Ian Rutz can be reached on (571)272-5535. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

November 10, 2015

/Mardochee CHERY/
Primary Examiner, Art Unit 2133

<i>Index of Claims</i> 	Application/Control No. 13942721	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	05/18/2015	11/10/2015						
	1	✓	✓						
	2	✓	✓						
	3	✓	✓						
	4	✓	✓						
	5	✓	✓						
	6	✓	✓						
	7	✓	✓						
	8	-	-						
	9	-	-						
	10	-	-						
	11	✓	✓						
	12	✓	✓						
	13	✓	✓						
	14	✓	✓						
	15	✓	✓						
	16	✓	✓						
	17	✓	✓						
	18	✓	✓						
	19	✓	✓						
	20	✓	✓						
	21	✓	✓						
	22	✓	✓						
	23	✓	✓						
	24	✓	✓						

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**TERMINAL DISCLAIMER TO OBTAIN A DOUBLE PATENTING
REJECTION OVER A "PRIOR" PATENT**

Docket Number (Optional)

NETL.062C1

In re Application of: Netlist, Inc.

Application No.: 13/942,721

Filed: July 16, 2013

For: SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

The applicant, Netlist, Inc., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent No. 8,489,837** as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;

is held unenforceable;

is found invalid by a court of competent jurisdiction:

is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;

has all claims canceled by a reexamination certificate:

is reissued; or

is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☒ The undersigned is an attorney or agent of record. Reg. No. 51167

/Jamie J. Zheng/

Signature _____

January 21, 2016

Date _____

Jamie J. Zheng

Typed or printed name

Title

650-273-6008

Telephone Number

- ☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist
App. No.	:	13/942,721
Filed	:	July 16, 2013
For	:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
Examiner	:	CHERY, MARDOCHEE
Art Unit	:	2133
Conf. No.	:	5636
Docket No.	:	NETL.062C1

RESPONSE TO NON-FINAL OFFICE ACTION DATED MAY 22, 2015**Mail Stop Amendment**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

This submission is in response to the Final Office Action dated November 16, 2015.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

Amendments to the Claims: Begin on page 2 of this paper.

Remarks: Begin on page 6 of this paper.

In the Claims:

1. (Currently Amended) A memory module operable with a memory controller of a host computer system in an operational mode in which the memory module performs memory operations in response to memory commands from the memory controller in accordance with an industry standard, the memory module comprising:

a controller circuit configured to cause the memory module to enter an initialization mode in response to a command from the host computer system, the memory module executing at least one initialization sequence during the initialization mode;

at least one output having a defined function in the operational mode according to the industry standard but is undefined by the industry standard in the initialization mode; and

a notification circuit ~~to output~~-outputting a notification signal indicating a status of the initialization mode to the memory controller via the at least one output.

2. (Previously Presented) The memory module of Claim 1, wherein the at least one status comprises completion of the at least one initialization sequence.

3. (Previously Presented) The memory module of Claim 1, wherein the at least one status comprises execution of the at least one initialization sequence.

4. (Cancelled)

5. (Previously Presented) The memory module of Claim 1, wherein the at least one notification signal triggers the memory controller to execute an interrupt routine.

6. (Previously Presented) The memory module of Claim 1, wherein the at least one output comprises an error-out pin of the memory module.

7. (Previously Presented) The memory module of Claim 1, wherein the notification circuit is configured to drive the at least one output to a first state indicative of execution

of the at least one initialization sequence or to a second state indicative of completion of the at least one initialization sequence.

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Previously Presented) A method performed by a memory controller coupled to at least a first memory module, the first memory module configured to perform memory operations in response to memory commands from the memory controller in accordance with an industry standard while operating in a first mode, the method comprising:

outputting a command to the first memory module to cause the first memory module to operate in a second mode so as to execute an internal procedure, whereby the memory controller hands off control of the internal procedure to the first memory module;

receiving a notification signal via at least one input of the memory controller indicating a status of the internal procedure, the at least one input of the memory controller being coupled to at least one output of the first memory module, the at least one output of the first memory module having a defined function according to the industry standard while the first memory module is operating in the first mode but is undefined by the industry standard while the first memory module is operating in the second mode; and

resuming memory operations by issuing memory commands to the first memory module after receiving the notification signal.

12. (Previously Presented) The method of Claim 11, wherein the memory controller enters a “Wait” state while the memory module executes the internal procedure and exits the “Wait” state in response to receiving the notification signal.

13. (Previously Presented) The method of Claim 11, wherein the notification signal indicates completion of the internal procedure.

14. (Previously Presented) The method of Claim 11, wherein the memory controller is further coupled to a second memory module, the method further comprising: outputting a command to the second memory module to cause the second memory module to execute an internal procedure after receiving the notification signal and before resuming memory operations.

15. (Previously Presented) The method of Claim 11, wherein the at least one first output of the first memory module is an error-out pin of the first memory module.

16. (Currently Amended) A memory module operable with a memory controller of a host computer system in a first mode in which the memory module performs memory operations in response to memory commands from the memory controller in accordance with an industry standard, the memory module comprising:

- a module controller circuit configured to cause the memory module to operate in a second mode in response to a command to execute an internal procedure from the host computer system;

- at least one output having a defined function in the first mode according to the industry standard but is undefined by the industry standard in the second mode; and

- a notification circuit ~~to output~~ ~~outputting~~ a notification signal indicating a status of the at least one internal procedure to the memory controller via the at least one output.

17. (Previously Presented) The memory module of Claim 16, wherein the at least one status indicates completion of the internal procedure.

18. (Previously Presented) The memory module of Claim 16, wherein the notification circuit is configured to drive the at least one output to a first state indicative of execution of the at least one internal procedure or to a second state indicative of completion of the internal procedure.

19. (Previously Presented) The memory module of Claim 16, wherein the at least one notification signal is an open-drain signal.

20. (Previously Presented) The memory module of Claim 16, wherein the at least one output comprises an error-out pin of the memory module.
21. (Previously Presented) The memory module of claim 16, wherein the memory controller hands off control of to the module controller circuit by issuing the command to execute the internal procedure.
22. (Previously Presented) The memory module of claim 16, wherein the module controller circuit is configured to process address and command signals from the memory controller in the first mode.
23. (Previously Presented) The memory module of claim 16, wherein the notification circuit comprises a first input corresponding to the first mode, a second input corresponding to the second mode, and a multiplexor selecting between the first input and the second input based on whether the memory module is in the first mode or the second mode.
24. (Previously Presented) The method of claim 11, wherein the at least one input of the memory controller is also coupled to at least one output of a second memory module, the at least one output of the second memory module having a defined function according to the industry standard while the second memory module is operating in a third mode but is undefined by the industry standard while the second memory module is operating in a fourth mode, the second memory module in the third mode being configured to perform memory operations in response to memory commands from the memory controller in accordance with the industry standard, the second memory module being configured to execute an internal procedure in the fourth mode, and wherein the notification signal indicates completion of the internal procedure at the first memory module and completion of the internal procedure at the second memory module.

REMARKS

This amendment responds to the Final Office Action dated November 16, 2015.

In the Office Action, the Examiner:

- maintained the rejection of claims 1-7 and 11-24 on the ground of nonstatutory double patenting as being unpatentable over claims 1-18 of U.S. Patent No. 8,489,837.

Claim 1 and 6 are amended for minor issues. No new matter is added.

Applicant files herewith a properly signed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) to overcome any nonstatutory double patenting rejection the Examiner may raise with regard to claims 1-3, 5-7, and 11-24.

Applicant submits that claims 1-3, 5-7, and 11-24 are in condition for allowance, and respectfully requests such action. The Examiner is invited to call the undersigned at (650) 521-4828 if such phone call would help resolve any remaining issues.

Respectfully submitted,

Date: January 21, 2016

/Jamie J. Zheng/

51167

Jamie J. Zheng
Customer No. 79141

(Reg. No.)

Electronic Acknowledgement Receipt	
EFS ID:	24693832
Application Number:	13942721
International Application Number:	
Confirmation Number:	5636
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062C1
Receipt Date:	21-JAN-2016
Filing Date:	16-JUL-2013
Time Stamp:	20:09:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	2016-02-21_AIA82A_transmittal_POA_NETL062C1.pdf	195952 473e5ae134afbfb81bda6b53c7b89bd77d67259e	no	3

Warnings:

Information:

2	Power of Attorney	AIA_General_POA_Netlist.pdf	133545 f8258889ee9edc63b1cc17705b3158faed49e9e	no	1
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
3	Terminal Disclaimer Filed	2016-01-20_Terminal_Disclaimer_NETL062C1.pdf	159910 c0ad062a8367bdfb254aab877149a0e420014524	no	2
Warnings:					
Information:					
4	Response After Final Action	2016-01-21_Rsps_FOA_NETL062C1.pdf	105768 219b512c6e05d730215d45e56e67b7f37ae39061	no	6
Warnings:					
Information:					
Total Files Size (in bytes):			595175		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

GENERAL POWER OF ATTORNEY BY APPLICANT FOR UNITED STATES PATENT

I hereby revoke all previous powers of attorney given in the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

I hereby appoint the practitioner associated with the following Customer Number :

79141

as my/our attorney or agent, and to transact all business in the United States Patent and Trademark Office in connection with the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

Please recognize or change the correspondence address for the application referenced in the attached transmittal letter to the address associated with the above-mentioned Customer Number.

I am the Applicant:

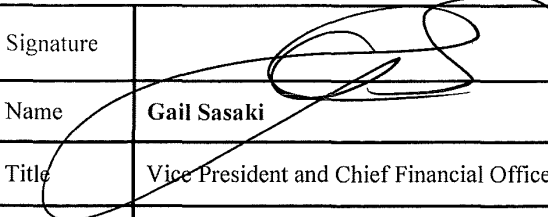
☐ Inventor or Joint Inventor

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is currently being filed in this document)

SIGNATURE of Applicant for Patent

Signature		Date: January 9, 2013
Name	Gail Sasaki	
Title	Vice President and Chief Financial Officer	
Company	Netlist, Inc.	

Note: Signature - this form must be signed by the Applicant or a person authorized to act on behalf of Applicant.

Submit multiple forms for more than one signature
Total of ___ forms are submitted.

Doc Code: PA..

Document Description: Power of Attorney

PTO/AIA/82A (07-12)

Approved for use through 11/30/2014. OMB 0651-0035

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE
REGISTERED PRACTITIONERS**

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B or equivalent) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5. If the Power of Attorney by Applicant form is not accompanied by this transmittal form or an equivalent, the Power of Attorney will not be recognized in the application.

Application Number	13/942,721
Filing Date	July 16, 2013
First Named Inventor	HYUN LEE
Title	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
Art Unit	2133
Examiner Name	Chery, Mardochee
Attorney Docket Number	NETL.062C1

SIGNATURE of Applicant or Patent Practitioner

Signature	/Jamie J. Zheng/	Date	January 21, 2016
Name	Jamie J. Zheng	Telephone	650-521-4828
Registration Number	51,167		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..

Document Description: Power of Attorney

PTO/AIA/82B(07-12)

Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in the attached transmittal letter.

- ☐ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

--

OR

- ☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

Name	Registration Number		Name	Registration Number

Please recognize or change the correspondence address for the application identified in the attached transmittal letter to:

- ☐ The address associated with the above-mentioned Customer Number.

OR

- ☐ The address associated with Customer Number:

--

OR

☐ Firm or Individual Name				
Address				
City		State		Zip
Country				
Telephone		Email		

I am the Applicant:

- ☐ Inventor or Joint Inventor
☐ Legal Representative of a Deceased or Legally Incapacitated Inventor
☐ Assignee or Person to Whom the Inventor is Under an Obligation to Assign
☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document)

SIGNATURE of Applicant for Patent

Signature		Date	
Name		Telephone	
Title and Company			

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms for more than one signature, see below *.

- ☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Samsung Electronics Co., Ltd.

Ex. 1006, p. 109

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 13/942,721		Filing Date 07/16/2013		☐ To be Mailed				
ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO													
APPLICATION AS FILED – PART I													
(Column 1)			(Column 2)										
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)					
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A							
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))		N/A		N/A		N/A							
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A							
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		X \$ =							
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		X \$ =							
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).											
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))													
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL							
APPLICATION AS AMENDED – PART II													
(Column 1)			(Column 2)			(Column 3)							
AMENDMENT	01/21/2016		CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))		* 20		Minus	** 20		= 0		X \$40 =		0	
	Independent (37 CFR 1.16(h))		* 3		Minus	***3		= 0		X \$210 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))												
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
						TOTAL ADD'L FEE				0			
(Column 1)			(Column 2)			(Column 3)							
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT			HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))		*		Minus	**		=		X \$ =			
	Independent (37 CFR 1.16(h))		*		Minus	***		=		X \$ =			
	☐ Application Size Fee (37 CFR 1.16(s))												
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
						TOTAL ADD'L FEE							
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.													

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Application Number 	Application/Control No. 13/942,721	Applicant(s)/Patent under Reexamination LEE, HYUN	
Document Code - DISQ	Internal Document – DO NOT MAIL		

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : 1/21/16	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:

Felicia D. Roberts

8,489,837

U.S. Patent and Trademark Office



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/942,721	07/16/2013	Hyun Lee	NETL.062C1

CONFIRMATION NO. 5636

POA ACCEPTANCE LETTER

79141

Jamie J. Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306



OC000000080299771

Date Mailed: 02/04/2016

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/21/2016.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/hteffer/

"OK TO ENTER"
2/8/2016
MC

NETL.062C1

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist
App. No.	:	13/942,721
Filed	:	July 16, 2013
For	:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
Examiner	:	CHERY, MARDOCHEE
Art Unit	:	2133
Conf. No.	:	5636
Docket No.	:	NETL.062C1

RESPONSE TO NON-FINAL OFFICE ACTION DATED MAY 22, 2015

Mail Stop Amendment

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This submission is in response to the Final Office Action dated November 16, 2015.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

Amendments to the Claims: Begin on page 2 of this paper.

Remarks: Begin on page 6 of this paper.

NETL.062C1

- 1 -



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 02/24/2016
Jamie J. Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

EXAMINER

CHERY, MARDOCHEE

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 02/24/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/942,721	07/16/2013	Hyun Lee	NETL062C1	5636

TITLE OF INVENTION: SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$480	\$0	\$0	\$480	05/24/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 02/24/2016
Jamie J. Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/942,721	07/16/2013	Hyun Lee	NETL.062C1	5636

TITLE OF INVENTION: SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$480	\$0	\$0	\$480	05/24/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHERY, MARDOCHEE	2133	711-170000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/942,721	07/16/2013	Hyun Lee	NETL.062C1	5636
79141	7590	02/24/2016	EXAMINER	
Jamie J. Zheng, Ph.D Esq. P.O. Box 60573 Palo Alto, CA 94306			CHERY, MARDOCHEE	
			ART UNIT	PAPER NUMBER

2133

DATE MAILED: 02/24/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/942,721	Applicant(s) LEE, HYUN	
	Examiner Mardochee CHERY	Art Unit 2133	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the after final filed 01/21/2016.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-3,5-7 and 11-24. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____	6. ☐ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____	

/Mardochee CHERY/ Primary Examiner, Art Unit 2133	2/8/16
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EAST Search History**EAST Search History (Interference)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	((controller circuit configured cause memory module enter\$3 initialization mode in response command host computer system memory module execut\$3 at least one initialization sequence during initialization mode) and (at least one output\$3 defin\$3 function operational mode according to industry standard but undefined industry standard initialization mode) and (notification circuit output\$3 notification signal indicat\$3 status initialization mode memory controller via least output\$4)).clm.	USPAT	SAME	ON	2016/02/18 00:10

2/ 18/ 2016 12:11:14 AM**C:\Users\mchery\Documents\EAST\Workspaces\13942721.wsp**

Issue Classification 	Application/Control No. 13942721	Applicant(s)/Patent Under Reexamination LEE, HYUN	
	Examiner MARDOCHEE CHERY	Art Unit 2133	

CPC						
Symbol					Type	Version
G06F		9		445	F	2013-01-01
G06F		13		24	I	2013-01-01

CPC Combination Sets									
Symbol				Type	Set	Ranking	Version		

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/MARDOCHEE CHERY/ Primary Examiner.Art Unit 2133	2/8/16	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

Issue Classification 	Application/Control No. 13942721	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION													
CLASS			SUBCLASS			CLAIMED					NON-CLAIMED								
711			170			G	0	6	F	12 / 00 (2006.01.01)									
CROSS REFERENCE(S)																			
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																		

NONE		Total Claims Allowed:	
		20	
(Assistant Examiner)	(Date)		
/MARDOCHEE CHERY/ Primary Examiner.Art Unit 2133	2/8/16	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

Issue Classification 	Application/Control No. 13942721	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

☐ Claims renumbered in the same order as presented by applicant								☐ CPA		☐ T.D.		☐ R.1.47			
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	13	17												
2	2	14	18												
3	3	15	19												
-	4	16	20												
4	5	17	21												
5	6	18	22												
6	7	19	23												
-	8	20	24												
-	9														
-	10														
7	11														
8	12														
9	13														
10	14														
11	15														
12	16														

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 20	
/MARDOCHEE CHERY/ Primary Examiner.Art Unit 2133 (Primary Examiner) _____ (Date) _____		O.G. Print Claim(s) 1	O.G. Print Figure 3

<i>Search Notes</i> 	Application/Control No. 13942721	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner MARDOCHEE CHERY	Art Unit 2133

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
711	170	2/18/16	MC

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Search	5/18/15	MC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	See attached EAST Interference Search	2/18/16	MC

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PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Customer No. 79141

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

	(Depositor's name)
	(Signature)
	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/942,721	07/16/2013	Hyun Lee	NETL.062C1	5636

TITLE OF INVENTION:

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	undiscounted	\$960	\$0	\$0	\$960	05/24/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 JAMIE J. ZHENG, Ph.D, Esq.
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE
Netlist, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)
Irvine, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-5863 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☒ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Jamie J. Zheng/
Typed or printed name Jamie J. Zheng

Date March 1, 2016
Registration No. 51,167

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		13942721		
Filing Date:		16-Jul-2013		
Title of Invention:		SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		
First Named Inventor/Applicant Name:		Hyun Lee		
Filer:		Jamie Jie Zheng		
Attorney Docket Number:		NETL.062C1		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt	
EFS ID:	25071445
Application Number:	13942721
International Application Number:	
Confirmation Number:	5636
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062C1
Receipt Date:	01-MAR-2016
Filing Date:	16-JUL-2013
Time Stamp:	23:04:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$960
RAM confirmation Number	6320
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	2016-03-01_Issue_Fee_Transmission_NetL062C1.pdf	74753 d5c6ce2df8a6f6816549388a976fa76de50930da	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30481 399fdae513fac74749d3230ce299c54bb8ed43	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			105234		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Notice of References Cited	Application/Control No. 13/942,721	Applicant(s)/Patent Under Reexamination LEE, HYUN	
	Examiner Mardochee CHERY	Art Unit 2133	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-4,672,570 A	06-1987	Benken; Richard P.	G06F13/128	709/250
*	B	US-5,511,152 A	04-1996	Lai; Charles C.	G06F13/1689	358/1.15
*	C	US-2003/0115427 A1	06-2003	Roohparvar, Frankie F.	G11C7/02	711/154
*	D	US-6,763,437 B1	07-2004	Nguyen; Trung	G06F3/0613	711/112
*	E	US-2007/0091702 A1	04-2007	Nikitin; Andrey	G11C29/12	365/233.1
*	F	US-2008/0256281 A1	10-2008	Fahr; Gerald J.	G06F13/16	710/305
*	G	US-2009/0119464 A1	05-2009	Grundy; Kevin P.	G06F12/06	711/154
*	H	US-7,586,350 B2	09-2009	Chung; Jin-Il	H03K3/0375	327/143
*	I	US-2010/0042778 A1	02-2010	Tanguay; Kevin B.	G06F13/1694	711/105
*	J	US-2010/0202240 A1	08-2010	MOSHAYEDI; Mark	G11C5/04	365/229
*	K	US-2011/0022789 A1	01-2011	Fujimoto; Akihisa	G06F1/266	711/103
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/942,721	04/12/2016	9311116	NETL.062C1	5636

79141 7590 03/23/2016
Jamie J. Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 248 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Netlist, Inc., Irvine, CA;
Hyun Lee, Ladera Ranch, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.