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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.062A
		Application Number	
Title of Invention	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		
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Attorney Docket Number	NETL.062A	Small Entity Status Claimed ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	3	Suggested Figure for Publication (if any)	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.062A
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Title of Invention	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.062A
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Title of Invention	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		

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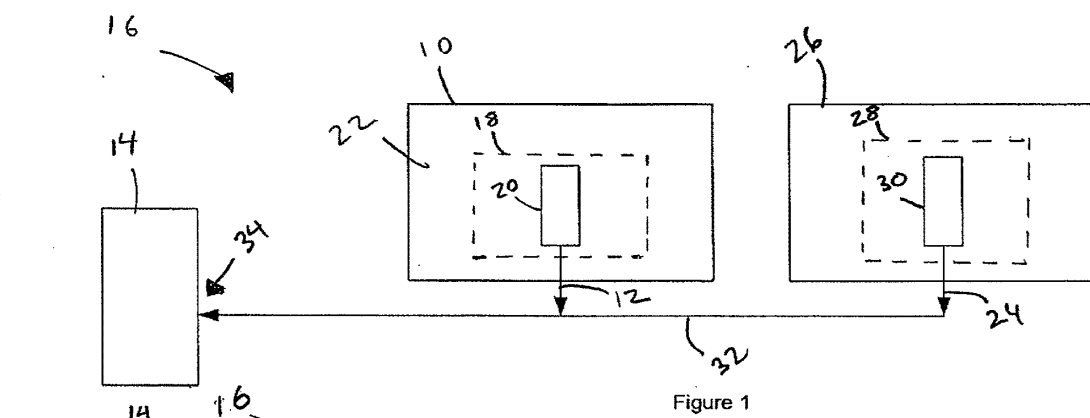


Figure 1

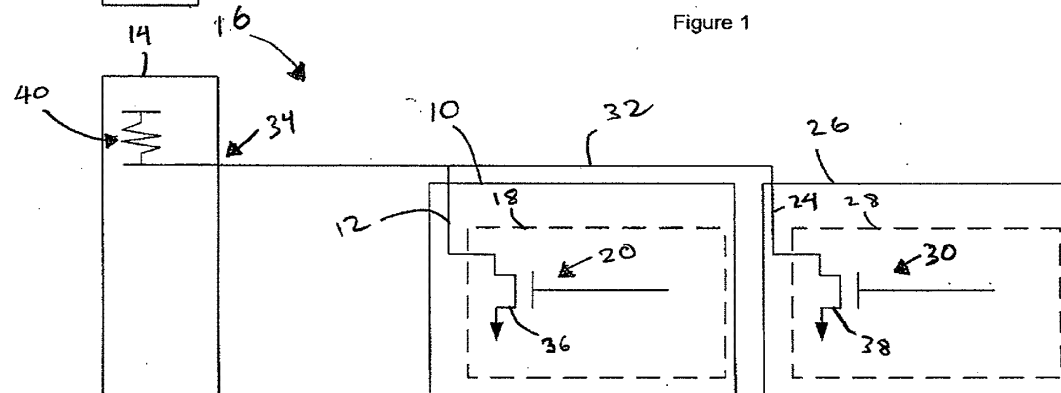


Figure 2

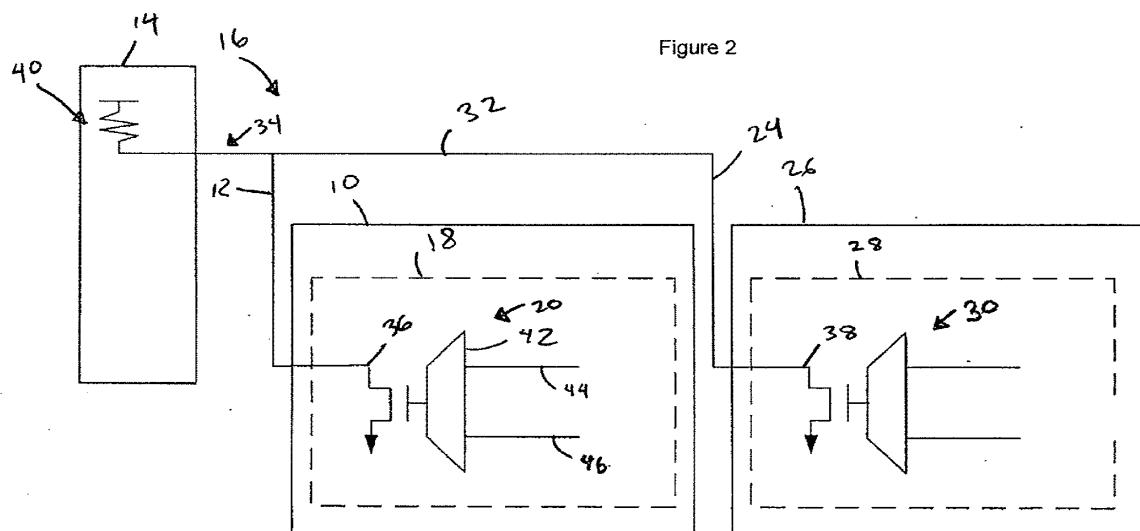


Figure 3

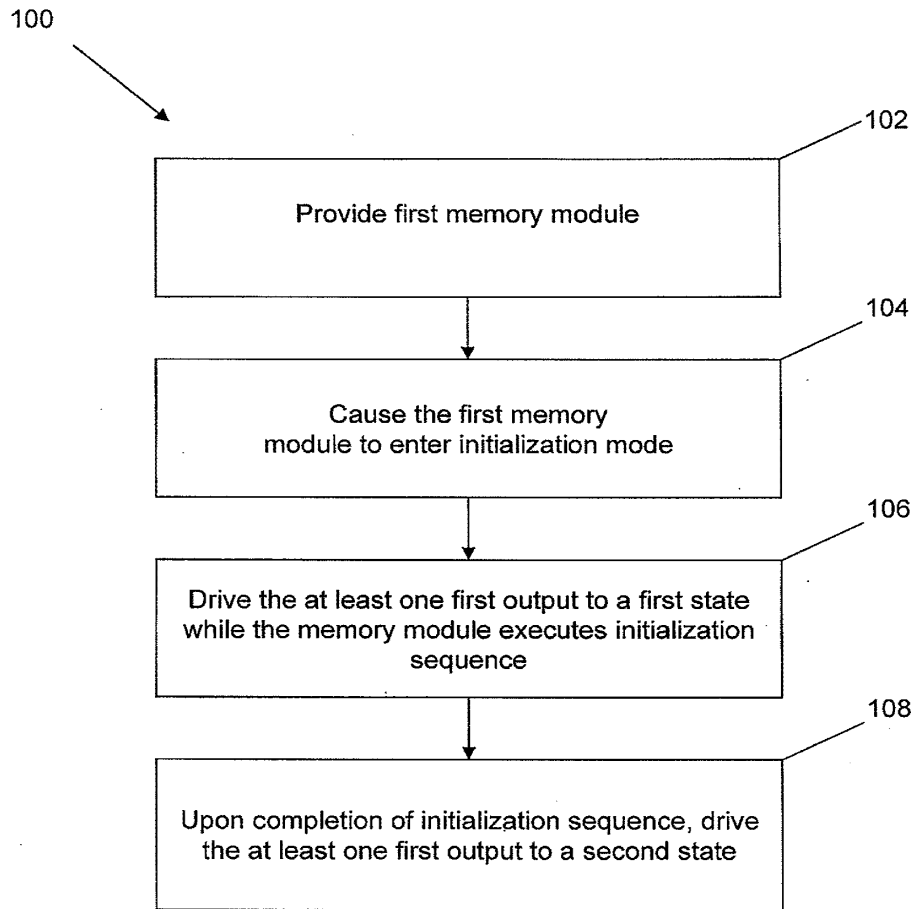


Figure 4

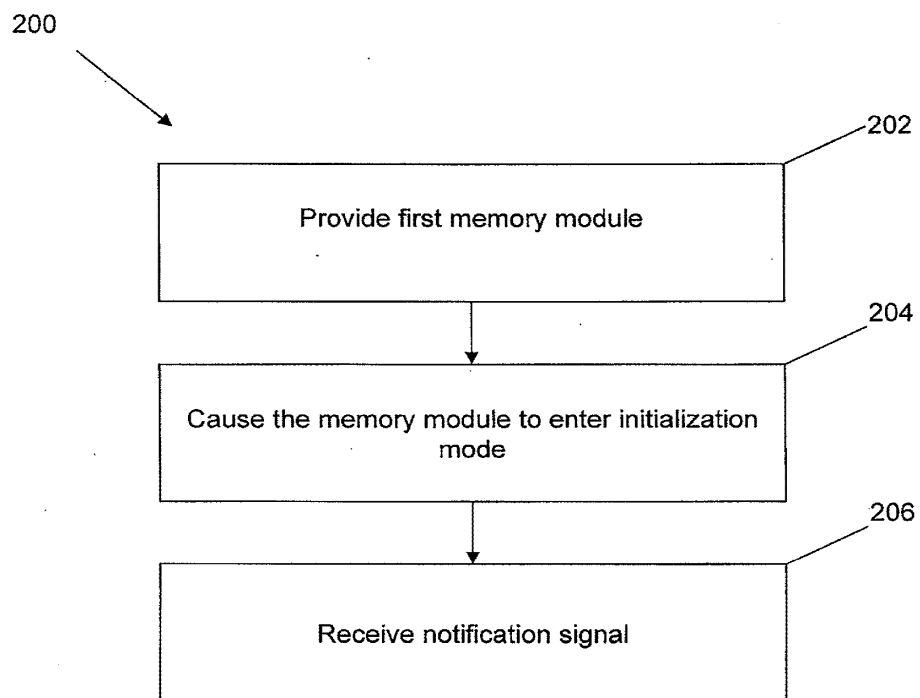


Figure 5

SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE**CROSS-REFERENCE TO RELATED APPLICATIONS**

[0001] This application claims the benefit of priority from U.S. Provisional Application Number 61/186,799, filed June 12, 2009, which is incorporated in its entirety by reference herein.

FIELD OF THE DISCLOSURE

[0002] The present disclosure relates to the operation of memory modules. Specifically, the present disclosure relates to systems and methods for handshaking with a memory module during or upon completion of initialization.

BACKGROUND OF THE DISCLOSURE

[0003] Memory subsystems such as memory modules are generally involved in the initialization procedure for computer systems, including servers, personal computers, and the like. For example, during system-wide initialization, the memory subsystems may undergo internal initialization procedures, or the system memory controller may otherwise interact with the memory subsystems during the initialization procedure. As part of this interaction, the system memory controller may request that the memory subsystem perform one or more requested tasks during system initialization.

SUMMARY

[0004] According to certain aspects, a memory module comprises at least one output configured to be operatively coupled to a memory controller of a host computer system. The memory module can be configured to operate in at least two modes comprising an initialization mode during which the memory module executes at least one initialization sequence and an operational mode. In certain embodiments, the memory module comprises a controller circuit configured to cause the memory module to enter the initialization mode. The memory module can also comprise a notification circuit configured to drive the at least one output while the memory module is in the initialization mode to provide at least one notification signal to the memory controller indicating at least one status of the at least one initialization sequence.

[0005] In another aspect, a method of using at least one memory module comprises providing a first memory module comprising at least one first output operatively coupled to a memory controller of a host computer system. The first memory module can be configured to operate in at least two modes comprising an initialization mode during which the first memory module executes at least one initialization sequence and an operational mode. The method can further comprise causing the first memory module to enter the initialization mode. In certain embodiments, the method comprises driving the at least one first output to a first state while the memory module executes the at least one initialization sequence. In certain embodiments, the method further comprises, upon completion of the at least one initialization sequence, driving the at least one first output to a second state different than the first state.

[0006] According to additional aspects, a method of using at least one memory module comprises providing a memory module comprising at least one output operatively coupled to a memory controller of a host computer system. In certain embodiments, the memory module is configured to operate in at least two modes comprising an initialization mode during which the memory module executes at least one initialization sequence and an operational mode. The method may comprise causing the memory module to enter the initialization mode. In some embodiments, the method comprises receiving a notification signal from the at least one output of the memory module, the notification signal indicating that the memory module has completed the at least one initialization sequence.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Figure 1 shows an example host computer system including an example memory module configured to perform handshaking with a memory controller of the host computer system according to certain embodiments described herein.

[0008] Figure 2 shows an example host computer system including example first and second memory modules configured to perform handshaking with a system memory controller of the host computer system according to certain embodiments described herein.

[0009] Figure 3 shows a host computer system including example first and second memory modules configured to perform handshaking with a memory controller of the host

system, where the notification circuits of the first and second memory modules have another example configuration according to certain embodiments described herein.

[0010] Figure 4 and Figure 5 show example methods of using at least one memory module according to certain embodiments described herein.

DETAILED DESCRIPTION

[0011] Existing initialization schemes have certain inefficiencies which lead to wasted time and expense. Thus, there is a need to reduce the time and complexity involved in system memory controller interactions with memory subsystems during initialization. Certain embodiments described herein advantageously satisfy at least a portion of this need by providing a system and method which utilizes a feedback path from a memory subsystem such as a memory module to a system memory controller, such as a Memory Controller Hub (MCH) of a computer system during initialization.

[0012] In general, there is no existing method of handshaking between the MCH (e.g., system memory controller) and a memory subsystem (e.g., memory module) during initialization. For example, in conventional systems, the system memory controller does not monitor the error-out signal from the memory subsystem. This causes the MCH to perform blind execution. In a typical server (e.g., an Intel or AMD or other chipset based server), the lack of any handshaking between the MCH and the memory subsystem during the server initialization period has not been a serious issue since the MCH generally has complete control over the initialization procedure. However, one possible configuration for LR-DIMM (Load Reduced DIMM) includes the MCH handing over one or more parts of the initialization operation sequence to the memory subsystem. This raises an unprecedented issue not addressed in conventional systems because, in such proposed configurations, the system can benefit from the MCH handshaking with the memory subsystem controller, as described more fully below.

[0013] Such an LR-DIMM configuration may have the MCH inserting a waiting period of predetermined length during which the MCH is idle and the memory subsystem controller undergoes initialization. However, one shortcoming of this LR-DIMM configuration would be that it requires the MCH to be in standby (idle, or wait) while the memory subsystem controller completes its task. Under such an arrangement, since the time

to complete a task can be dependent on the density, speed and configuration of the memory subsystem, and these parameters may be unknown to the MCH, the MCH may have to insert a single, predetermined standby period. In addition, if there are multiple occasions that the MCH needs to hand off control to the memory subsystem controller, the required MCH wait periods can be different from one occasion to another, and it complicates the correlation between the MCH and the memory subsystem controller. For example, the MCH according to such a scheme may give control to the local memory controller of a memory subsystem (e.g., memory module) for execution of a training sequence. The MCH may wait for a predetermined period of time and then assume that the local memory controller has completed the training sequence. However, depending on the memory subsystem parameters (e.g., memory capacity, speed, number of ranks, etc.), the time for actually completing the training sequence may vary and may be longer or shorter than predetermined period of time.

[0014] In general, handshaking can be implemented in at least two ways; polling and notifying. In the polling method, the MCH reads a status register in the memory subsystem controller to find out if the memory subsystem controller has completed the required or requested operation. For example, a status register may be read out through a serial interface such as System Management Bus (SMBus). However, a register polling method is generally inefficient because the system memory controller does not know exactly when the memory subsystem will have completed the required or requested operation. Thus, the system memory controller may wait longer than necessary to poll the memory subsystem, thereby delaying the overall initialization process. Additionally, the problem may be compounded because multiple training sequences or other initialization sequences may be run on the memory subsystem during a particular initialization period, resulting in accumulation of such unnecessary delays. Moreover, polling generally involves scheduling polling intervals during which the system memory controller is not performing other operations, resulting in further inefficiency.

[0015] Alternatively, the notifying method is an advantageous handshaking method between the MCH and the memory subsystem controller. According to a notifying method, the memory subsystem controller sends a signal to the MCH when the memory subsystem controller completes the required or requested operation. This method allows the

MCH to execute one or more independent commands while it is waiting for a notification signal from the memory subsystem controller.

[0016] Certain embodiments described herein provide a method of establishing a handshake mechanism based on notification signaling. In certain embodiments, this mechanism can be implemented by adding a new interface (notifying) signal between the MCH and the memory subsystem controller, or by adding an additional functionality to an existing, non-timing critical signal without altering the memory subsystem hardware. In either case, the interface between the MCH and the memory subsystem controller of certain embodiments can be an open drain signaling from the memory subsystem controller to the MCH, although a variety of other configurations are possible. As will be appreciated by persons skilled in the art, the terms MCH, system memory controller, and memory subsystem are used generally interchangeable throughout this disclosure, and the terms memory module, memory subsystem controller, and local memory controller are used generally interchangeably throughout this disclosure.

[0017] Figure 1 illustrates an example host computer system 16 including an example memory module 10 according to certain embodiments described herein. The memory module 10 can comprise at least one output 12 configured to be operatively coupled to a system memory controller 14 of the host computer system 16. In certain embodiments, the memory module 10 is configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode. The memory module 10 may further include a controller circuit 18. In some embodiments, the controller circuit 18 is configured to cause the memory module 10 to enter the initialization mode. The memory module 10 can further include a notification circuit 20 configured to drive the at least one output 12 while the memory module 10 is in the initialization mode to provide at least one notification signal to the memory controller 14 indicating at least one status of the at least one initialization sequence.

[0018] The memory module 10 may comprise a printed-circuit board (PCB) 22. In certain embodiments, the memory module 10 has a memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, 16-GB, or higher. Other memory capacities are also compatible with certain embodiments described herein. In addition, memory modules 10 having widths of

4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. The PCB 22 can have an industry-standard form factor. For example, the PCB 22 can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB 20 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB 22 has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FBDIMM), mini-DIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein. In other embodiments, certain non-DIMM form factors are possible such as, for example, single in-line memory module (SIMM), multi-media card (MMC), and small computer system interface (SCSI).

[0019] In certain embodiments, the memory module 10 is operatively coupled to (e.g., in electrical communication with) the host computer system 16. In certain other embodiments, the memory module 10 may communicate with the host computer system 16 using some other type of communication, such as, for example, optical communication. Examples of host computer systems 16 include, but are not limited to, blade servers, 1U servers, personal computers (PCs), and other applications in which space is constrained or limited. The PCB 22 can comprise an interface (not shown) that is configured to be in electrical communication with the host computer system 16. For example, the interface can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system 16. The interface of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory module 10 and the host system 16. For example, the interface can comprise a standard 240-pin DDR2 edge connector. The at least one output 12 may be routed over the interface, for example.

[0020] The memory module 10 may also comprise one or more memory elements (not shown), such as dynamic random-access memory (DRAM) elements, for example. Types of DRAM elements compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, DDR4, and synchronous DRAM (SDRAM). In addition,

memory elements having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Memory elements compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μ BGA), mini-BGA (mBGA), and chip-scale packaging (CSP). In certain embodiments, the memory module 10 may also include one or more non-volatile memory elements, such as one or more flash memory elements. Types of flash memory elements compatible with certain embodiments described herein include, but are not limited to, NOR flash, NAND flash, ONE-NAND flash, and multi-level cell (MLC).

[0021] The controller circuit 18 of certain embodiments generally controls the operation of the memory module 10. For example, the controller circuit 18 may control the memory elements of the memory module 10 and/or communicate with the system memory controller 14. For example, the controller circuit 18 may receive and process address and command signals (e.g., read, write commands) from the system memory controller 14 and transmit appropriate address and commands to the memory elements in response. See, e.g., U.S. Pat. Appl. Publ. Nos. 2006/0062047 A1 and 2006/0262586 A1, each of which is incorporated in its entirety by reference herein. In certain embodiments, the controller circuit 18 comprises a local memory controller. Additionally, depending on the architecture of the memory module 10, such as for an FB-DIMM, the controller circuit 18 may comprise an advanced memory buffer (AMB). The controller circuit 18 can comprise one or more of a field-programmable gate array (FPGA), a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, and a complex programmable logic device (CPLD), for example. In certain embodiments, the controller circuit 18 comprises various discrete electrical elements, while in certain other embodiments, the controller circuit 18 comprises one or more integrated circuits.

[0022] As discussed, the memory module 10 is configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode. In one embodiment, for example, the at least one initialization sequence may comprise one or more training sequences. The initialization sequence (e.g., comprising one or more training sequences) may be initiated by

the system memory controller 14. In some embodiments, the controller circuit 18 is configured to cause the memory module 10 to enter the initialization mode. For example, the controller circuit 18 may be configured to execute a routine implementing the at least one initialization sequence when the appropriate signal or command is received from the memory controller 14 or is otherwise received from the host computer system 16 (e.g., upon receipt of a reset signal).

[0023] In certain embodiments, for example, the computer system 16 is coupled to a plurality of memory modules 10, 26 including the memory module 10 and at least a second memory module 26, and the memory controller 14 (e.g., MCH) trains each module 10, 26 separately, in series. In one example scenario, the memory controller 14 issues a first command to the memory module 10, and, in response, the memory module 10 executes an initialization sequence (e.g., one or more training sequences). Upon completion of the initialization sequence, the first memory module 10 advantageously issues a notification to the memory controller 14 in accordance with embodiments described herein. In response, the memory controller 14 issues a second command, this time to the memory module 26, and, in response, the memory module 26 executes an initialization sequence (e.g., one or more training sequences). Upon completion of the initialization sequence, the second memory module 26, similar to the first memory module 10, advantageously issues a notification to the memory controller 14 in accordance with embodiments described herein. In response, where there are more than two memory modules 10, 26, the memory controller 14 issues a third command to a third memory module (not shown), and so forth. One example computer system 16 capable of implementing such a scenario is configured to execute an Intel Basic Input/Output System (BIOS), and comprises a plurality of memory modules 10, 26 having an LRDIMM configuration. In such an example system, the Intel BIOS causes the system memory controller 14 to initialize the LRDIMM memory modules 10, 26 serially.

[0024] The operational mode is the normal mode of the memory module 10. For example, during the operational mode, the memory module 10 is generally accessed by the system memory controller 14 of the host computer 16 during standard computer operation not associated with initialization. For example, the system memory controller 14 may cause the memory module 10 to perform standard operations such as memory read/write, pre-charge,

refresh, etc., while in operational mode, although it will be appreciated that one or more of these operations can also be performed by the memory module 10 while in initialization mode in certain embodiments.

[0025] The notification circuit 20 can be configured to drive the at least one output 12, while the memory module 10 is in the initialization mode or after the memory module 10 completes one or more initialization sequences, to provide the at least one notification signal to the memory controller 14 indicating at least one status of the at least one initialization sequence. While shown in Figures 1-3 as forming a part of the controller circuit 18, the notification circuit 20 may be a physically and/or logically separate circuit in certain embodiments. While a variety of configurations are possible, the notification circuit 20 may comprise one or more transistors, one or more logic elements (e.g., AND, OR, NOR, NAND, XOR gates, and the like), or a combination thereof. In some embodiments, the notification circuit 20 may additionally or alternatively comprise one or more of an FPGA, PLD, CPLD, ASIC, custom-designed semiconductor device, discrete electrical elements, and an integrated circuit.

[0026] The at least one status of certain embodiments comprises completion of the at least one initialization sequence, such that the at least one notification signal is indicative of the completion of the at least one initialization sequence. The at least one status of certain embodiments comprises execution of the at least one initialization sequence. For example, the at least one status may indicate that the at least one initialization sequence is currently being executed. In some embodiments, the at least one status may provide an indication that a certain task has been completed by the memory module 10, such as a training task requested by the system memory controller 14. In certain embodiments, the notification circuit 20 can be configured to drive the at least one output 12 to a first state indicative of execution of the at least one initialization sequence or to a second state indicative of completion of the at least one initialization sequence. As one example, the first state may be a high or low logic level, and the second state may be a high impedance state. In another case, the first state is a high or low logic level, and the second state is the inverse logic level of the first state.

[0027] The at least one output 12 of certain embodiments is configured to be operatively coupled to at least one interrupt of the system memory controller 14, and the

system memory controller 14 is responsive to the at least one notification signal indicating completion of the at least one initialization sequence. For example, the system memory controller 14 may trigger execution of an interrupt routine upon receipt of the notification signal on the output 12. The interrupt routine generally executes the appropriate operations for the at least one status indicated by the at least one notification signal. For example, if the at least one status indicates that the at least one initialization sequence is complete, execution of the interrupt routine may cause the system memory controller 14 to notify the host computer system 16 that the system initialization, or a portion thereof, is completed. In one embodiment, for example, the execution of the interrupt routine causes the system memory controller 14 to initiate a subsequent training sequence for the memory module 10 or on another memory module connected to the host system 16. For example, in one embodiment, a central processing unit (CPU) of the host system 16 (not shown) enters a “Wait” state after issuing a command to the memory module 10 to enter the initialization mode. Receipt of the at least one notification signal on the output 12 triggers execution of the interrupt routine, which interrupts the CPU, causing the “Wait” state to be aborted and allowing the host system 16 to continue operation. In this manner, generation of the interrupt on the at least one output 12 can allow completion of the at least one initialization sequence to receive generally immediate attention from the CPU and/or memory controller 14 of the host system 16. As will be appreciated, the CPU and memory controller 14 of the host system 16 may comprise separate modules, or may alternatively comprise a single integrated module, depending on the architecture of the host system 16 chip-set.

[0028] In certain embodiments, execution of the interrupt routine causes the system memory controller 14 to cause the memory module 10 to exit the initialization mode and to enter the operational mode. In another embodiment, the memory module 10 automatically enters the operational mode upon completion of the at least one initialization sequence without intervention from the memory controller 14.

[0029] In some embodiments, the at least one output 12 is operated in conformance with a standard (e.g., an industry standard) when the memory module 10 is in the operational mode, but is not operated in conformance with the standard when the memory module 10 is in the initialization mode. An example of a standard in accordance with certain

embodiments described herein is one or more of the industry standard promulgated by the Joint Electronic Devices Engineering Counsel (JEDEC). For example, the operation and behavior of the at least one output 12 may conform to an industry standard when the memory module 10 is in the operational mode, but the operation and behavior of the at least one output 12 may not conform to the industry standard when the memory module 10 is in the initialization mode. Because the at least one output 12 does not conform to the standard during initialization mode, an existing (e.g., JEDEC-specified) pin may be utilized to provide the at least one notification signal to the system memory controller 14 from the memory module 10 during the initialization mode. In one embodiment, for example, the at least one output 12 comprises an error-out pin of the memory module 10. In conventional systems, the operation of the error-out pin is undefined by the standard during initialization. However, in certain embodiments described herein, during the operational mode, the error-out pin may be used according a conventional industry standard (e.g., a JEDEC standard) to indicate a parity error has occurred in the memory module 10. During the initialization mode, the error-out pin can be used to transmit the at least one notification signal to the system memory controller 14.

[0030] It is advantageous to use the error-out pin for initialization status notification according to certain embodiments because the error-out pin can be asserted by the memory module 10 independent from system memory controller 14 requests or commands. Also, because the error-out pin is a JEDEC-specified pin, design cost and complexity are reduced because additional pin-outs and interrupt design changes can be avoided (e.g., in cases where such changes in hardware or chipset may not be feasible to provide the at least one status to the system memory controller 14). However, in certain other embodiments, providing the at least one status may be implemented by adding one or more pins to the system memory controller 14 (e.g., MCH) and to the controller circuit 18 (e.g., local memory controller), thereby utilizing changes in hardware or the chipset.

[0031] Moreover, the error-out pin may be coupled to an interrupt of the system memory controller 14 (e.g., according to the JEDEC standard). Thus, where the error-out pin is used, from the system point of view in accordance with certain embodiments, the notification of completion of the required or requested task from the memory module 10 (e.g., by the local memory controller) generates an interrupt communicated to the system during the

initialization period and indicative of completion of the required or requested task. Assertion of the same pin during normal (non-initialization) operation upon an error occurring, on the other hand, generates an interrupt communicated to the system during the normal operation indicative of the occurrence of the error condition. Thus, in certain embodiments, the error-out pin and corresponding signal memory module 10 can be used to support the notifying function and to provide the at least one status generally without changing hardware. Certain other such embodiments involve modifying the basic input/output system (BIOS) or other programming change. For example, the BIOS may be modified to indicate to the system memory controller 14 how to respond to the notification signal (e.g., to the error_out signal or the interrupt corresponding thereto).

[0032] In certain other embodiments, the at least one output 12 may include other existing (e.g., JEDEC specified) pins instead of, or in addition to, the error-out pin. In yet other configurations, at least one additional (e.g., non-JEDEC specified) pin may be employed. In general, any pin not otherwise active during the initialization mode may be used (e.g., high-order address pins, read/write pins, data pins, etc.).

[0033] The at least one output 12 can further be configured to be operatively coupled to at least one second output 24 of a second memory module 26 in some embodiments, as schematically illustrated in Figures 1-3. The second memory module 26 may be generally similar in structure and function to the memory module 10, and may comprise a controller circuit 28 and a notification circuit 30, for example. The second memory module 26 may be generally identical to the first memory module 10, or may have a different memory capacity, form factor, etc., than the first memory module 10. More than two such memory modules may be present in certain embodiments. As described above, the second memory module 26 can be configured to operate in at least two modes comprising an initialization mode during which the second memory module 26 executes at least one initialization sequence, and an operational mode. For example, the initialization and operational modes may be similar to those describe above in relation to the first memory module 10.

[0034] The second memory module 26 can also be configured to drive the at least one second output 24 to a third state indicative of execution of at least one initialization sequence of the second memory module 26 or to a fourth state indicative of completion of the

at least one initialization sequence of the second memory module 26. Additionally, in some embodiments, the at least one first output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are operatively coupled together by a bus 32 which is also operatively coupled to at least one input 34 of the system memory controller 14. In other embodiments (not shown), the at least one first output 12 and the at least one second output 24 are not coupled together, and are coupled to two separate inputs of the system memory controller 14.

[0035] Figure 2 shows an example host computer system 16 including example first and second memory modules 10, 26. As shown, the notification circuits 20, 30 of the first and second memory modules 10, 26 each comprise at least one transistor 36, 38. The at least one transistor 36, 38 can be in an open-drain configuration, as shown, although other configurations are possible. In certain such embodiments, the first state of the at least one first output 12 is a first logic level, the second state of the at least one first output 12 is a high-impedance state, the third state of the at least one second output 24 is the first logic level, and the fourth state of the at least one second output 24 is the high-impedance state. In the illustrated example, while the at least one initialization sequence is in progress, the first and second memory modules 10, 26 drive the gates of the respective transistors 36, 38 high. Thus, the transistors 36, 38 are respectively low impedance while the memory modules 10, 26 are executing each section of the initialization sequence, thereby pulling the first and second outputs 12, 24 low. Thus, the first state and the third state are low logic levels (ground) in the example configuration. Also, because the first and second outputs 12, 24 are coupled together by the bus 32, if the at least one initialization sequence of either one of the first and second memory modules 10, 26 are in progress, the bus 32 will be pulled to a low logic level.

[0036] As each of the two memory modules 10, 26 completes its at least one initialization sequence, it can drive the corresponding at least one first and second outputs 12, 24 respectively to a high impedance state. For example, once the at least one initialization sequence on each of the first and second memory modules 10, 26 is completed, the first and second memory modules 10, 26 can drive the gates of the respective transistors 36, 38 low, resulting in a high-impedance state on the at least one first and second outputs 12, 24 causing the bus 32 to be pulled high by the system memory controller 14. Accordingly, only once the

at least one initialization sequence of both the first and second memory modules 10, 26 are complete, the bus 32 will be pulled high by the internal pull-up configuration 40 of the system memory controller 14. The second state and the fourth state are therefore high-impedance values in the example embodiment. Thus, the system memory controller 14 can monitor the value on the bus 32 via the first input 34 to determine when both of the memory modules 10, 26 have completed the at least one initialization sequence. As discussed, in other configurations the at least one first and second outputs 12, 24 may be received on separate inputs of the system memory controller 14, and the status of the at least one initialization sequence of each memory module 10, 26 may be monitored independently.

[0037] As discussed above, in certain embodiments in which more than one memory module 10, 26 is connected to the system memory controller 14, each memory module 10, 26 or associated controller circuit 18 (e.g., local memory controller) causes the corresponding notification circuit 20, 30 to drive the at least one output 12, 24 to the high impedance state from the low impedance state when it completes the requested or required operation. Thus, in certain such embodiments, the system memory controller 14 (e.g., MCH) can only pull the notifying signal high when all memory modules 10, 26 or associated controller circuits (e.g., local memory controllers) have completed the required or requested operation (e.g., initialization sequence). This configuration allows the system memory controller 14 (e.g., MCH) to work with a non-homogenous memory subsystem. For example, the system memory controller 14 may be able to monitor the progress of multiple memory modules 10, 26 including a mix of DIMMs or other memory modules having differing characteristics, such as DIMM density, rank configurations, DRAM density, speed, DRAM configuration, etc.

[0038] Additionally, the at least one output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are configured to be operatively coupled to at least one interrupt of the system memory controller 14 in certain embodiments. In certain such embodiments, the system memory controller 14 can be responsive to the second state of the first memory module 10 and the fourth state of the second memory module 26 by triggering execution of an interrupt routine by a processor of the system memory controller 14. For example, in the example system of Figure 2, when the

bus 32 is pulled high by the pull-up configuration 40 indicating the second state of the first memory module 10 and the fourth state of the second memory module 26, the system memory controller 14 triggers execution of the interrupt routine.

[0039] In some embodiments, in which the at least one first output 12 and the at least one second output 24 are operatively coupled to separate inputs of the system memory controller 14, the at least one first output 12 and the at least one second output 24 may be operatively coupled to two separate interrupts. For example, the system memory controller 14 may be responsive to the second state of the first memory module 10 by triggering execution of a first interrupt routine associated with a first interrupt, and may be responsive to the fourth state of the second memory module 26 by triggering execution of a second interrupt routine associated with the second interrupt. In yet other embodiments, the separate inputs of the memory controller 14 are internally operatively coupled to the same interrupt, or are operatively coupled to separate interrupts which trigger the same interrupt routine.

[0040] Figure 3 shows a host computer system 16 including an example memory module 10 where the notification circuit 20 of the memory module 10 has another example configuration in accordance with certain embodiments described herein. In the example configuration of Figure 3, the at least one first output 12 is operatively coupled to an error-out pin of the memory module 10, and a multiplexor 42 drives the transistor 36 with either of a task_in_progress signal 44 or an error signal 46 (e.g., parity error signal). In one embodiment, for example, the multiplexor 42 may be configured to drive the transistor 36 with the task_in_progress signal 44 when the memory module 10 is in the initialization mode or is executing the at least one initialization sequence, and with the error signal 46 when the memory module 10 is in the operational mode. Thus, the memory module 10 can be advantageously configured to both perform the standard (e.g., JEDEC-specified) error reporting functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode, as described herein. As shown in Figure 3, a second memory module 26 including a similar configuration can also be operatively coupled to the host computer system 16. In certain embodiments, the at least one second output 24 of the second memory module 26 can be operatively coupled to the at least one first output 12 by the bus 32, as described above (e.g., with respect to Figure 2).

[0041] Figure 4 shows an example method 100 of using the at least one memory module 10 in accordance with certain embodiments described herein. While the description below of the method 100 refers to structure shown in Figures 1-3, other structures may also be used in accordance with certain embodiments described herein. At block 102, the method 100 of certain embodiments comprises providing a first memory module 10 comprising at least one first output 12 operatively coupled to a memory controller 14 of a host computer system 16. The first memory module 10 can be configured to operate in at least two modes comprising an initialization mode during which the first memory module 10 executes at least one initialization sequence, and an operational mode. For example, the at least one initialization sequence may comprise one or more steps of a series of steps associated with an initialization procedure of the host computer system 16.

[0042] At block 104, the method 100 in some embodiments comprises causing the first memory module 10 to enter the initialization mode. At block 106, the method 100 of certain embodiments comprises driving the at least one first output 12 to a first state while the memory module 10 executes the at least one initialization sequence. Upon completion of the at least one initialization sequence, the method of certain embodiments comprises driving the at least one first output 12 to a second state different than the first state. In certain embodiments, the first state is a first logic level and the second state is a high impedance state. Additionally, in certain embodiments, the at least one first output 12 is operatively coupled to at least one interrupt of the memory controller 14 such that driving the at least one output 12 to the second state triggers the memory controller to execute an interrupt routine.

[0043] In certain embodiments, the at least one output 12 is operated in conformance with JEDEC standard when the first memory module 10 is in the operational mode, but is not operated in conformance with the JEDEC standard when the first memory module 10 is in the initialization mode. The at least one first output 12 of certain embodiments include an error-out pin of the first memory module, for example.

[0044] The method 100 can further include providing a second memory module 26 comprising at least one second output 24 operatively coupled to the memory controller 14. The second memory module 26 can be configured to operate in one of at least two modes comprising an initialization mode, during which the second memory module 26 executes at

least one initialization sequence, and an operational mode. The method 100 can further include causing the second memory module 26 to enter the initialization mode. In certain embodiments, the method 100 also includes driving the at least one second output 24 of the second memory module 26 to a third state while the second memory module 26 executes the at least one initialization sequence. Upon completion of the at least one initialization sequence, the method 100 can further include driving the at least one second output 24 of the second memory module 26 to a fourth state different from the third state.

[0045] In certain embodiments, the at least one first output 12 of the first memory module 10 and the at least one second output 24 of the second memory module 26 are operatively coupled together by a bus 32 which is also operatively coupled to at least one input 34 of the memory controller 14. In certain other embodiments, the at least one first output 12 of the first memory module 10 is operatively coupled to a first input 34 of the memory controller 14 and the at least one second output 24 of the second memory module 26 is operatively coupled to a second input (not shown) of the memory controller 14.

[0046] Figure 5 shows another example method 200 of using at least one memory module 10 in accordance with certain embodiments described herein. At block 202, the method 200 may include providing a memory module 10 comprising at least one output 12 operatively coupled to a memory controller 14 of a host computer system 16. The memory module 10 may be configured to operate in at least two modes comprising an initialization mode, during which the memory module 10 executes at least one initialization sequence, and an operational mode.

[0047] The method 200 can further include causing the memory module 10 to enter the initialization mode at block 204. At block 206, the method 200 can include receiving a notification signal from the at least one output 12 of the memory module 10. The notification signal may indicate that the memory module 10 has completed the initialization sequence, for example. In certain embodiments, the method 200 further comprises executing an interrupt routine by the memory controller 14 in response to the notification signal.

Terminology / Alternative Embodiments

[0048] Embodiments have been described in connection with the accompanying drawings. However, it should be understood that the figures are not drawn to scale.

Distances, angles, etc. are merely illustrative and do not necessarily bear an exact relationship to actual dimensions and layout of the devices illustrated. In addition, the foregoing embodiments have been described at a level of detail to allow one of ordinary skill in the art to make and use the devices, systems, etc. described herein. A wide variety of variation is possible. Components, elements, and/or steps can be altered, added, removed, or rearranged. While certain embodiments have been explicitly described, other embodiments will become apparent to those of ordinary skill in the art based on this disclosure.

[0049] Conditional language used herein, such as, among others, "can," "could," "might," "may," "e.g.," and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment.

[0050] Depending on the embodiment, certain acts, events, or functions of any of the methods described herein can be performed in a different sequence, can be added, merged, or left out all together (e.g., not all described acts or events are necessary for the practice of the method). Moreover, in certain embodiments, acts or events can be performed concurrently, e.g., through multi-threaded processing, interrupt processing, or multiple processors or processor cores, rather than sequentially.

[0051] The various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein can be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. The described functionality can be implemented in varying ways for each particular application, but such

implementation decisions should not be interpreted as causing a departure from the scope of the disclosure.

[0052] The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein can be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor can be a microprocessor, but in the alternative, the processor can be any conventional processor, controller, microcontroller, or state machine. A processor can also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0053] The blocks of the methods and algorithms described in connection with the embodiments disclosed herein can be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module can reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, a hard disk, a removable disk, a CD-ROM, or any other form of computer-readable storage medium known in the art. An exemplary storage medium is coupled to a processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium can be integral to the processor. The processor and the storage medium can reside in an ASIC. The ASIC can reside in a user terminal. In the alternative, the processor and the storage medium can reside as discrete components in a user terminal.

[0054] Certain embodiments described herein are compatible with a memory system including memory devices with various attributes (see, e.g., Figures 2 and 3). For example, the memory system of certain embodiments may include various data slice sizes (e.g., two, four, eight, or 16 bit data slices) and corresponding memories (e.g., memories having two, four, eight, or 16 bit data widths).

[0055] Although certain embodiments and examples are discussed above, it is understood that the inventive subject matter extends beyond the specifically disclosed embodiments to other alternative embodiments and/or uses of the invention and obvious modifications and equivalents thereof. It is intended that the scope of the inventions disclosed herein should not be limited by the particular disclosed embodiments. Thus, for example, in any method or process disclosed herein, the acts or operations making up the method/process may be performed in any suitable sequence and are not necessarily limited to any particular disclosed sequence.

[0056] Various aspects and advantages of the embodiments have been described where appropriate. It is to be understood that not necessarily all such aspects or advantages may be achieved in accordance with any particular embodiment. Thus, for example, it should be recognized that the various embodiments may be carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other aspects or advantages as may be taught or suggested herein.

WHAT IS CLAIMED IS:

1. A memory module comprising:
 - at least one output configured to be operatively coupled to a memory controller of a host computer system, the memory module configured to operate in at least two modes comprising an initialization mode during which the memory module executes at least one initialization sequence and an operational mode;
 - a controller circuit configured to cause the memory module to enter the initialization mode; and
 - a notification circuit configured to drive the at least one output while the memory module is in the initialization mode to provide at least one notification signal to the memory controller indicating at least one status of the at least one initialization sequence.
2. The memory module of Claim 1, wherein the at least one status comprises completion of the at least one initialization sequence.
3. The memory module of Claim 1, wherein the at least one status comprises execution of the at least one initialization sequence.
4. The memory module of Claim 1, wherein the at least one output is configured to be operatively coupled to at least one interrupt of the memory controller and the memory controller is responsive the at least one notification signal indicating completion of the at least one initialization sequence by triggering execution of an interrupt routine by the memory controller.
5. The memory module of Claim 4, wherein the at least one output is configured to be operated in conformance with a JEDEC standard when the memory module is in the operational mode, but is configured to be operated not in conformance with the JEDEC standard when the memory module is operated in the initialization mode.
6. The memory module of Claim 5, wherein the at least one output comprises an error-out pin of the memory module.
7. The memory module of Claim 1, wherein the notification circuit is configured to drive the at least one output to a first state indicative of execution of the at least one

initialization sequence or to a second state indicative of completion of the at least one initialization sequence.

8. The memory module of Claim 7, wherein the at least one output is configured to be operatively coupled to at least one second output of a second memory module, the second memory module configured to operate in at least two modes comprising an initialization mode during which the second memory module executes at least one initialization sequence and an operational mode, the second memory module configured to drive the at least one second output of the second memory module to a third state indicative of execution of the at least one initialization sequence of the second memory module or to a fourth state indicative of completion of the at least one initialization sequence of the second memory module.

9. The memory module of Claim 8, wherein the at least one output of the first memory module and the at least one second output of the second memory module are configured to be operatively coupled to at least one interrupt of the memory controller and the memory controller is responsive to the second state of the first memory module and the fourth state of the second memory module by triggering execution of an interrupt routine by a processor of the memory controller.

10. The memory module of Claim 8, wherein the first state is a first logic level, the second state is a high-impedance state, the third state is the first logic level, and the fourth state is the high-impedance state.

11. A method of using at least one memory module, comprising:

providing a first memory module comprising at least one first output operatively coupled to a memory controller of a host computer system, the first memory module configured to operate in at least two modes comprising an initialization mode during which the first memory module executes at least one initialization sequence and an operational mode;

causing the first memory module to enter the initialization mode;

driving the at least one first output to a first state while the memory module executes the at least one initialization sequence;

upon completion of the at least one initialization sequence, driving the at least one first output to a second state different than the first state.

12. The method of Claim 11, wherein the first state is a first logic level and the second state is a high impedance state.

13. The method of Claim 11, wherein the at least one first output is operatively coupled to at least one interrupt of the memory controller such that driving the at least one output to the second state triggers the memory controller to execute an interrupt routine.

14. The method of Claim 11, wherein the at least one output is defined by the JEDEC standard when the first memory module is in the operational mode, but is not defined by the JEDEC standard when the first memory module is in the initialization mode.

15. The method of Claim 11, wherein the at least one first output is a error-out pin of the first memory module.

16. The method of Claim 11, further comprising:

providing a second memory module comprising at least one second output operatively coupled to the memory controller, the second memory module configured to operate in one of at least two modes comprising an initialization mode during which the second memory module executes at least one initialization sequence and an operational mode;

causing the second memory module to enter the initialization mode;

driving the at least one second output of the second memory module to a third state while the second memory module executes the at least one initialization sequence; and

upon completion of the at least one initialization sequence, driving the at least one second output of the second memory module to a fourth state different from the third state.

17. The method of Claim 16, wherein the at least one first output of the first memory module and the at least one second output of the second memory module are operatively coupled together by a bus which is also operatively coupled to at least one input of the memory controller.

18. The method of Claim 16, wherein the at least one first output of the first memory module is operatively coupled to a first input of the memory controller and the at least one second output of the second memory module is operatively coupled to a second input of the memory controller.

19. A method of using at least one memory module, comprising:

providing a memory module comprising at least one output operatively coupled to a memory controller of a host computer system, the memory module configured to operate in at least two modes comprising an initialization mode during which the memory module executes at least one initialization sequence and an operational mode;

causing the memory module to enter the initialization mode; and

receiving a notification signal from the at least one output of the memory module, the notification signal indicating that the memory module has completed the at least one initialization sequence.

20. The method of Claim 19, further comprising executing an interrupt routine by the memory controller in response to the notification signal.

SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

ABSTRACT

According to certain aspects, a memory module is provided having at least one output configured to be operatively coupled to a memory controller of a host computer system. The memory module can be configured to operate in at least two modes comprising an initialization mode during which the memory module executes at least one initialization sequence and an operational mode. The memory module may include a controller circuit configured to cause the memory module to enter the initialization mode. The memory module may also include a notification circuit configured to drive the at least one output while the memory module is in the initialization mode to provide at least one notification signal to the memory controller indicating at least one status of the at least one initialization sequence.

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Electronic Acknowledgement Receipt	
EFS ID:	7811283
Application Number:	12815339
International Application Number:	
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Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	To Be Provided Later
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Filer:	Sean Patrick Ambrosius/Chelsea Pearsall
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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	netl.pdf	966813 4c3217e6351851ea1d60a671fbc0659316c bc418	no	4
Warnings:					
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2	Drawings-only black and white line drawings	Figs.pdf	42227 fcd89a8259ea43c40b005b909b6f892e3cc4452	no	3
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3		spec.pdf	1256681 cd61b08443cdf8a967ae4e4a79eac095373ba018	yes	25
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Date: 06/14/10

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 12/815,339	
APPLICATION AS FILED – PART I					
(Column 1)		(Column 2)		SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 =	x\$26		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *	x\$110		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR				
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195		
			TOTAL		
			OR		
			OTHER THAN SMALL ENTITY		
			RATE (\$)	FEE (\$)	
			N/A	330	
			N/A	540	
			N/A	220	
			x\$52		
			x\$220		
			390		
			TOTAL	1090	
* If the difference in column 1 is less than zero, enter "0" in column 2.					
APPLICATION AS AMENDED – PART II					
(Column 1)		(Column 2)		(Column 3)	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		
	Total (37 CFR 1.16(i))	Minus **	=		
	Independent (37 CFR 1.16(h))	Minus ***	=		
	Application Size Fee (37 CFR 1.16(s))				
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))				
(Column 1)		(Column 2)		(Column 3)	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		
	Total (37 CFR 1.16(i))	Minus **	=		
	Independent (37 CFR 1.16(h))	Minus ***	=		
	Application Size Fee (37 CFR 1.16(s))				
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))				
(Column 1)		(Column 2)		(Column 3)	
SMALL ENTITY		OTHER THAN SMALL ENTITY			
RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
X =		X =			
X =		X =			
N/A		N/A			
TOTAL ADD'T FEE		TOTAL ADD'T FEE			

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/815,339	06/14/2010	2115	0.00	NETL.062A	20	3

CONFIRMATION NO. 1167

FILING RECEIPT



OC000000042249280

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Date Mailed: 06/28/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Assignment For Published Patent Application

NETLIST, INC., Irvine, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/186,799 06/12/2009

Foreign Applications

If Required, Foreign Filing License Granted: 06/23/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/815,339**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

Title

SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

Preliminary Class

713

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/815,339	06/14/2010		NETL.062A

CONFIRMATION NO. 1167

FORMALITIES LETTER



20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Date Mailed: 06/28/2010

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
Applicant must submit \$330 to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).
- The oath or declaration is missing.
A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
 - The drawings must be reasonably free from erasures and must be free from alterations, overwriting, interlineations, folds, and copy marks. See Figure(s) 1-3.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of **\$130** for a non-small entity, must be submitted with the missing items identified in this notice.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **\$1220** for a non-small entity

- **\$330** Statutory basic filing fee.
- **\$130** Surcharge.
- The application search fee has not been paid. Applicant must submit **\$540** to complete the search fee.
- The application examination fee has not been paid. Applicant must submit **\$220** to complete the examination fee for a non-small entity.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.

<https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/rgreen/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Please Direct All Correspondence to Customer Number 20995

RESPONSE TO FORMALITIES NOTICE

Applicant : Hyun Lee
App. No : 12/815,339
Filed : June 14, 2010
For : SYSTEMS AND METHODS FOR
HANDSHAKING WITH A MEMORY
MODULE
Art Unit : 2115
Conf No. : 1167

**CERTIFICATE OF EFS WEB
TRANSMISSION**

I hereby certify that this correspondence, and any other attachment noted on the automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web server on:

August 30, 2010

(Date)

/Sean Ambrosius/

Sean Ambrosius, Reg. No. 65,290

**Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450**

Dear Sir:

The above-captioned application was filed without a Declaration and/or filing fees.
Enclosed in compliance with 37 CFR 1.53(f) are the following.

- (X) A Declaration in 1 page.
- (X) A Supplemental Application Data Sheet in 3 pages
- (X) Replacement drawings in 3 pages. Applicant submits that the replacement drawings are in accordance with 37 C.F.R. 1.84 and 37 C.F.R. 1.121(d).
- (X) Fees will be paid via EFS Web. Extension of time is requested by payment of any extension fee.

The Commissioner is hereby authorized to charge any additional fees which may be required, now or in the future, or credit any overpayment, to Account No. 11-1410.

/Sean Ambrosius/

Sean Ambrosius
Registration No. 65,290
Attorney of Record
Customer No. 20,995
(949) 760-0404

9599086

**DECLARATION FOR UTILITY OR DESIGN APPLICATION
UNDER 37 CFR 1.63**

Docket No.: NETL062A

Page 1 of 1

Title: SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

Inventors: Hyun Lee

Please Direct All Correspondence to Customer Number 20995

This Declaration is directed to the invention described in the application that:

Was filed as Application No. 12/815,339 filed on June 14, 2010.

As a below named inventor:

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is described and claimed and for which a patent is sought;

I have reviewed and understand the contents of the above-identified application, including the claims, and any amendment filed herewith or identified above;

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56;

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of **first** inventor: Hyun Lee

Signature: _____

Date: _____

Citizenship: _____

US

Mailing Address: _____

21 Thalia, Ladera Ranch, CA 92694

Residence Address: _____

(if different than above)

Send Correspondence To:

KNOBBE, MARTENS, OLSON & BEAR, LLP

Customer No. 20995

9440761

SUPPLEMENTAL APPLICATION DATA SHEET**Application Information**

Application Number:: 12/815,339
Filing Date:: June 14, 2010
Application Type:: Nonprovisional
Subject Matter:: Utility
Title:: SYSTEMS AND METHODS FOR HANDSHAKING
WITH A MEMORY MODULE
Attorney Docket Number:: NETL.062A
Request for Early Publication?: No
Request for Non-Publication?: YES
Total Drawing Sheets:: 3
Small Entity?: No

Inventor Information 1

Applicant Authority Type:: Inventor
Primary Citizenship Country:: US
Status:: Full Capacity
Given Name:: Hyun
Family Name:: Lee
City of Residence:: Ladera Ranch
State or Prov. of Residence:: CA
Country of Residence:: US
Street:: 21 Thalia
City:: Ladera Ranch
State or Province:: CA
Country:: US

Correspondence Information

Correspondence Customer Number:: 20995

Phone Number:: (949) 760-0404

Fax Number:: (949) 760-9502

E-Mail Address:: efiling@kmob.com

Representative Information

Representative Customer Number:: 20995

Domestic Priority Information

Application::	Continuity Type::	Parent Application::	Parent Filing Date::
This Application	Nonprovisional of	61/186799	2009-06-12

Foreign Priority Information

Country::	Application Number::	Filing Date::	Priority Claimed::

Assignment Information

Assignee Name:: NETLIST, INC.

Street:: 51 Discovery, #150

City:: Irvine

State or Province:: CA

Country:: US

Postal or Zip Code:: 92618

Dated: August 30, 2010

By: Sean Ambrosius/

Sean Ambrosius

Registration No. 65,290

Attorney of Record

Customer No. 20995

(949) 760-0404

9598730

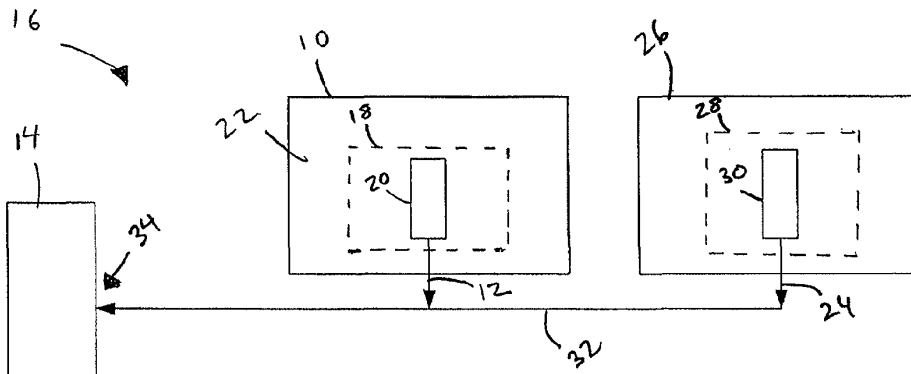


Figure 1

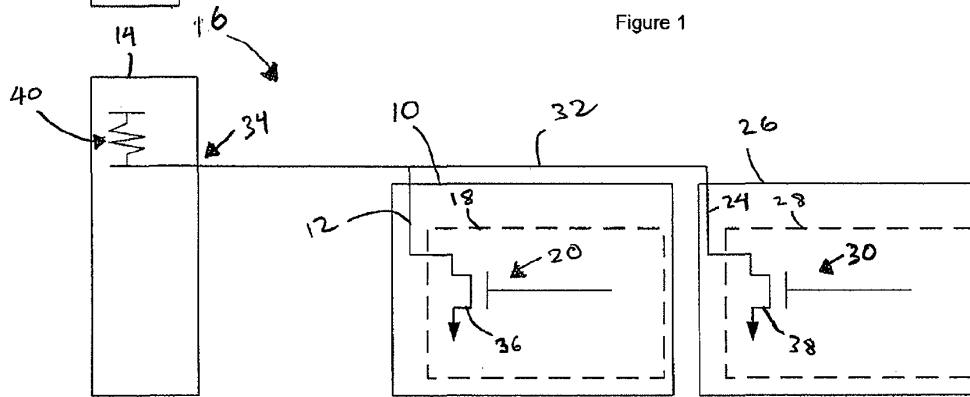


Figure 2

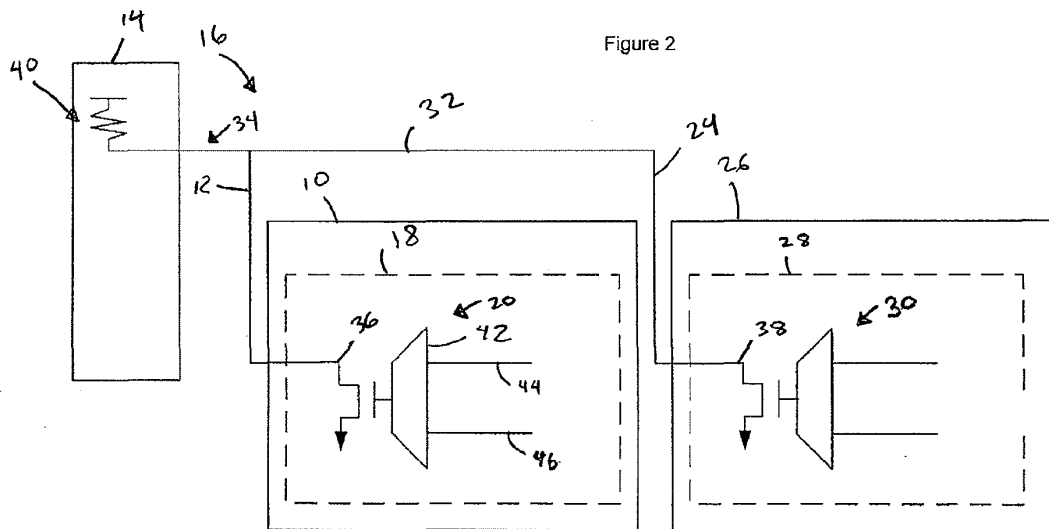


Figure 3

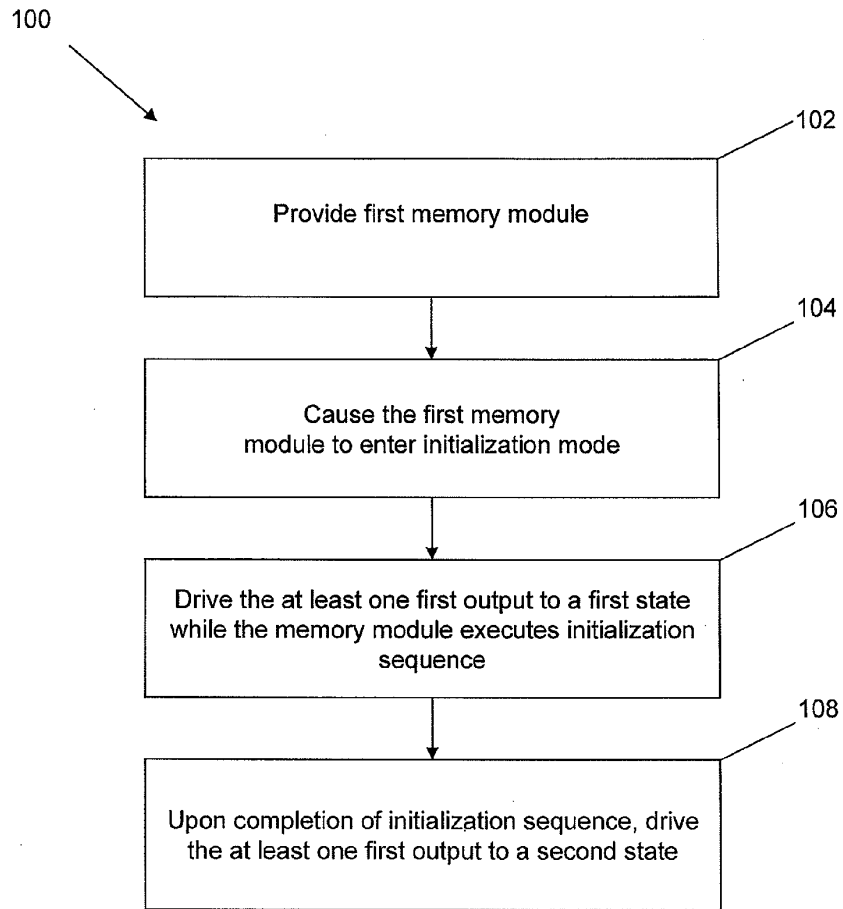


Figure 4

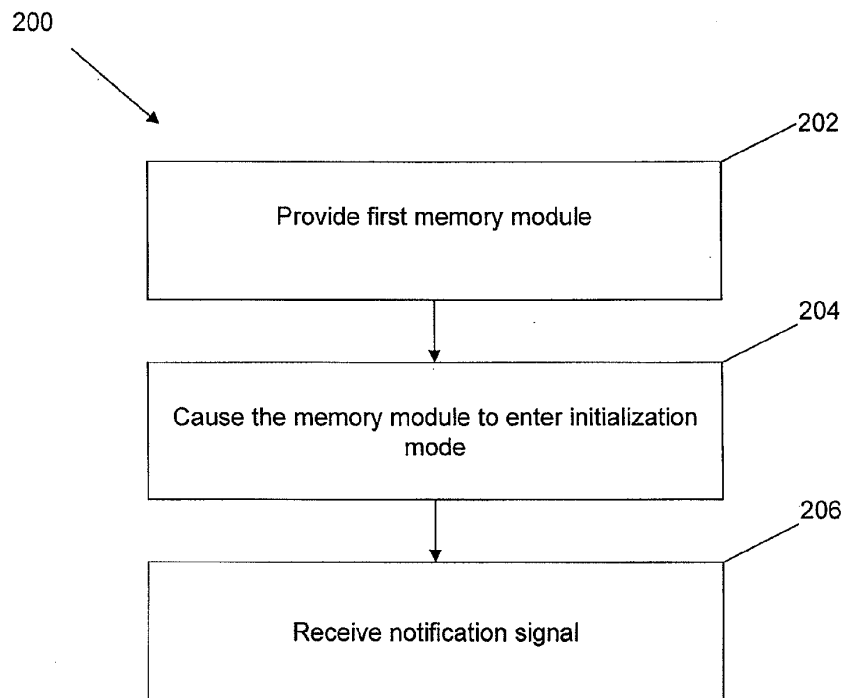


Figure 5

Electronic Patent Application Fee Transmittal				
Application Number:		12815339		
Filing Date:		14-Jun-2010		
Title of Invention:		SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		
First Named Inventor/Applicant Name:				
Filer:		Sean Patrick Ambrosius/Nadin Hamoui		
Attorney Docket Number:		NETL.062A		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Late filing fee for oath or declaration	1051	1	130	130
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1220

Electronic Acknowledgement Receipt	
EFS ID:	8323126
Application Number:	12815339
International Application Number:	
Confirmation Number:	1167
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	
Customer Number:	20995
Filer:	Sean Patrick Ambrosius/Khylo Rhoden
Filer Authorized By:	Sean Patrick Ambrosius
Attorney Docket Number:	NETL.062A
Receipt Date:	30-AUG-2010
Filing Date:	14-JUN-2010
Time Stamp:	22:02:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1220
RAM confirmation Number	6497
Deposit Account	111410
Authorized User	KNOBBE MARTENS OLSON AND BEAR
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	netl062a.pdf	36952	no	1
			cd5548c8fd21bda07fd20ae8e7dc1a848c7a6d5b		
Warnings:					
Information:					
2	Oath or Declaration filed	decl062a.pdf	268936	no	1
			57c834275d9ac1857ae6ec485067cd53d94239aa		
Warnings:					
Information:					
3	Application Data Sheet	ads062a.pdf	43232	no	3
			dc23f332115671c45eec37426712232868268e94		
Warnings:					
Information:					
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4	Drawings-only black and white line drawings	figs062a.pdf	40132	no	3
			896904440b7086d3c5097b8c57ff7e0ba9de8351		
Warnings:					
Information:					
5	Fee Worksheet (PTO-875)	fee-info.pdf	36998	no	2
			ac1a282045eca145a594df959dc598838b9be8d3		
Warnings:					
Information:					
Total Files Size (in bytes):			426250		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/815,339	06/14/2010	2115	1220	NETL.062A	20	3

CONFIRMATION NO. 1167

UPDATED FILING RECEIPT



0C000000043355999

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Date Mailed: 09/10/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Hyun Lee, Ladera Ranch, CA;

Assignment For Published Patent Application

NETLIST, INC., Irvine, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/186,799 06/12/2009

Foreign Applications

If Required, Foreign Filing License Granted: 06/23/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/815,339**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

Title

SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

Preliminary Class

713

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/815,339	06/14/2010	Hyun Lee	NETL.062A	1167

20995	7590	09/14/2012
KNOBBE MARTENS OLSON & BEAR LLP		
2040 MAIN STREET		
FOURTEENTH FLOOR		
IRVINE, CA 92614		

EXAMINER	
RUTZ, JARED IAN	

ART UNIT	PAPER NUMBER
2187	

NOTIFICATION DATE	DELIVERY MODE
09/14/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jayna.cartee@knobbe.com
efiling@knobbe.com

DETAILED ACTION

1. Claims 1-20, as originally filed on 6/14/2012, are pending in the instant application. Of these, there are 3 independent and 17 dependent claims.

Drawings

2. The drawings were received on 8/30/2010. These drawings are not acceptable.
3. The drawings are objected to because the hand written numbers are not clear, and the hand written arrows connecting the numbers to elements of the drawings to not clearly indicate what they are referring to. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required

corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. **Claims 5 and 11** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

6. **Claims 5 and 11** each make reference to “a JEDEC standard”. The Examiner notes that JEDEC is an organization that issues many standards, and can be reasonably expected to issue additional standards in the future. As there will be examples of a JEDEC standard that are not known at the time the application was filed, it is not possible for the instant application to enable embodiments that are not yet known.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. **Claims 5 and 11** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. As noted supra, **claims 5 and 11** each make reference to “a JEDEC standard”. As JEDEC may issue new standards in the future, the scope of the phrase “a JEDEC standard” is indefinite, depending on standards which have not yet been issued.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. **Claims 1-3, 5, 7, 11, 14, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanguay et al. (US 2010/0042778) in view of Roohparvar (US 2003/0115427).

Claim 1 is taught by Tanguay as:

A memory module comprising: at least one output configured to be operatively coupled to a memory controller of a host computer system. Figure 2 shows memory interface 140 between SDRAM controller 116 and DIMM 250.

The memory module configured to operate in at least two modes comprising an initialization mode during which the memory module executes at

least one initialization sequence and an operational mode. Paragraph 0028 shows that the memory device must be initialized, then it can be accessed.

A controller circuit configured to cause the memory module to enter the initialization mode. Paragraph 0026 shows that command translator receives a signal indicating that the memory is to be initialized, and controls whether the bus switch or command translator provides the address and data information to memories 260.

Tanguay does not expressly teach a notification circuit configured to drive the at least one output while the memory module is in the initialization mode to provide at least one notification signal to the memory controller indicating at least one status of the at least one initialization sequence.

With respect to claim 1, Roohparvar teaches:

And a notification circuit configured to drive the at least one output while the memory module is in the initialization mode to provide at least one notification signal to the memory controller indicating at least one status of the at least one initialization sequence. Paragraph 0030 shows that when memory 104 has completed initialization, it provides an output signal on its DQ lines 143 that indicate the completion of initialization.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a notification circuit in the memory of Tanguay.

The motivation for doing so would have been to provide a memory that is able to initialize itself, without requiring the memory controller to wait an unnecessary amount of time for the initialization to be performed, Roohparvar paragraphs 0028-0030.

Therefore, it would have been obvious to combine Roohparvar with Tanguay to obtain the invention as recited in **claims 1-3, 5, and 7**.

Claim 2 is taught by Roohparvar as:

The memory module of Claim 1, wherein the at least one status comprises completion of the at least one initialization sequence. Paragraph 0030 shows that an output signal is provided by memory 104 on its DQ lines when initialization is completed.

Claim 3 is taught by Roohparvar as:

The memory module of Claim 1, wherein the at least one status comprises execution of the at least one initialization sequence. Paragraph 0030 shows that an output signal is provided by memory 104 on its DQ lines when initialization is completed, accordingly, prior to the transmission of the output signal, the initialization sequence is being performed.

Claim 5 is taught by Tanguay and Roohparvar as:

The memory module of Claim 4, wherein the at least one output is configured to be operated in conformance with a JEDEC standard when the

memory module is in the operational mode, but is configured to be operated not in conformance with the JEDEC standard when the memory module is operated in the initialization mode. Tanguay paragraphs 0004 and 0018 show that the memory is accessed according to a JEDEC standard. However, the use of the DQ lines as taught by Roohparvar to initialize the memory is not defined by the JEDEC standard.

Claim 7 is taught by Roohparvar as:

The memory module of Claim 1, wherein the notification circuit is configured to drive the at least one output to a first state indicative of execution of the at least one initialization sequence or to a second state indicative of completion of the at least one initialization sequence. Paragraph 0030 shows that an output signal is provided by memory 104 on its DQ lines when initialization is completed.

Claim 11 is taught by Tanguay as:

A method of using at least one memory module, comprising: providing a first memory module comprising at least one first output operatively coupled to a memory controller of a host computer system. Figure 2 shows memory interface 140 between SDRAM controller 116 and DIMM 250.

The first memory module configured to operate in at least two modes comprising an initialization mode during which the first memory module executes

at least one initialization sequence and an operational mode. Paragraph 0028 shows that the memory device must be initialized, then it can be accessed.

Causing the first memory module to enter the initialization mode.

Paragraphs 0025 and 0026 show that the memory enters the initialization mode by performing a mode register select command.

Tanguay does not expressly teach driving the at least one first output to a first state while the memory module executes the at least one initialization sequence; upon completion of the at least one initialization sequence, driving the at least one first output to a second state different than the first state.

With respect to claim 11, Roohparvar teaches:

Driving the at least one first output to a first state while the memory module executes the at least one initialization sequence; upon completion of the at least one initialization sequence, driving the at least one first output to a second state different than the first state. Paragraph 0030 shows that an output signal is provided by memory 104 on its DQ lines when initialization is completed. Accordingly, prior to the transmission of the output signal, the initialization sequence is being performed and the DQ lines are in a first state that does not indicate the completion of initialization, and then when initialization is complete, the DQ lines are driven to the second state different from the first state.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a notification circuit in the memory of Tanguay.

The motivation for doing so would have been to provide a memory that is able to initialize itself, without requiring the memory controller to wait an unnecessary amount of time for the initialization to be performed, Roohparvar paragraphs 0028-0030.

Therefore, it would have been obvious to combine Roohparvar with Tanguay to obtain the invention as recited in **claims 11 and 14**.

Claim 14 is taught by Tanguay and Roohparvar as:

The method of Claim 11, wherein the at least one output is defined by the JEDEC standard when the first memory module is in the operational mode, but is not defined by the JEDEC standard when the first memory module is in the initialization mode. Tanguay paragraphs 0004 and 0018 show that the memory is accessed according to a JEDEC standard. However, the use of the DQ lines as taught by Roohparvar to initialize the memory is not defined by the JEDEC standard.

Claim 19 is taught by Tanguay as:

A method of using at least one memory module, comprising: providing a memory module comprising at least one output operatively coupled to a memory controller of a host computer system. Figure 2 shows memory interface 140 between SDRAM controller 116 and DIMM 250.

The memory module configured to operate in at least two modes comprising an initialization mode during which the memory module executes at

least one initialization sequence and an operational mode. Paragraph 0028 shows that the memory device must be initialized, then it can be accessed.

Causing the memory module to enter the initialization mode. Paragraphs 0025 and 0026 show that the memory enters the initialization mode by performing a mode register select command.

Tanguay does not expressly teach receiving a notification signal from the at least one output of the memory module, the notification signal indicating that the memory module has completed the at least one initialization sequence.

With respect to claim 19, Roohparvar teaches:

And receiving a notification signal from the at least one output of the memory module, the notification signal indicating that the memory module has completed the at least one initialization sequence. Paragraph 0030 shows that when memory 104 has completed initialization, it provides an output signal on its DQ lines 143 that indicate the completion of initialization.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a notification circuit in the memory of Tanguay.

The motivation for doing so would have been to provide a memory that is able to initialize itself, without requiring the memory controller to wait an unnecessary amount of time for the initialization to be performed, Roohparvar paragraphs 0028-0030.

Therefore, it would have been obvious to combine Roohparvar with Tanguay to obtain the invention as recited in **claim 19**.

Allowable Subject Matter

12. **Claims 4, 6, 8-10, 12, 13, 15-18, and 20** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JARED RUTZ whose telephone number is (571)272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
Primary Examiner
Art Unit 2187

/Jared I Rutz/
Primary Examiner, Art Unit 2187

Notice of References Cited	Application/Control No. 12/815,339	Applicant(s)/Patent Under Reexamination LEE, HYUN	
	Examiner JARED RUTZ	Art Unit 2187	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2010/0042778	02-2010	Tanguay et al.	711/105
*	B	US-2003/0115427	06-2003	Roohparvar, Frankie F.	711/154
*	C	US-2011/0022789	01-2011	Fujimoto, Akihisa	711/103
*	D	US-2007/0091702	04-2007	Nikitin et al.	365/210
*	E	US-7,586,350	09-2009	Chung et al.	327/198
*	F	US-2010/0202240	08-2010	MOSHAYEDI et al.	365/229
*	G	US-2008/0256281	10-2008	Fahr et al.	710/305
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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BIB DATA SHEET

CONFIRMATION NO. 1167

SERIAL NUMBER 12/815,339	FILING or 371(c) DATE 06/14/2010 RULE	CLASS 711	GROUP ART UNIT 2187	ATTORNEY DOCKET NO. NETL.062A		
APPLICANTS Hyun Lee, Ladera Ranch, CA; ** CONTINUING DATA ***** This appln claims benefit of 61/186,799 06/12/2009 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 06/23/2010						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /JARED IAN RUTZ/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 3	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS KNOBBE MARTENS OLSON & BEAR LLP 2040 MAIN STREET FOURTEENTH FLOOR IRVINE, CA 92614 UNITED STATES						
TITLE SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE						
FILING FEE RECEIVED 1220	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	5201	(lee near2 hyun).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/05 10:42
S2	66	S1 and (initialization or initializ\$3).clm.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/05 10:43
S3	59888	(initialization or initializ\$3) with memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/05 10:51
S4	21640	(711/101-105,154,166,167,170).OCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/05 10:53
S5	4904	(713/1).OCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/05 10:53
S6	100440	error near3 (pin or output)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/05 12:57
S7	59888	(initialization or initializ\$3) with memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/05 12:58
S8	73	S6 same S7	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/05 12:58
S9	70	S8 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/05 12:58
S10	23	jedec with initialization	US-PGPUB; USPAT;	ADJ	OFF	2012/09/05 18:19

			USOCR; EPO; DERWENT; IBM_TDB			
S11	20	S10 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/05 18:19
S12	1	("7586350").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/06 10:49
S13	13	("5686844" "5754879" "5905690" "6408415" "6751134" "6833741" "6903568" "6996023" "7239187").PN. OR ("7586350").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/06 10:55
S14	14	("20030179023" "4900950" "5378936" "5414378" "5438550" "5477176" "5731720" "5737612" "5929675" "5990730" "6304114").PN. OR ("6833741").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/06 11:15
S15	49549	(initializ\$3 or initialization) near3 (status or complet\$3 or indicat\$3 or signal)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/06 15:03
S16	3188	(mmu or controller) with S15	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/06 15:03
S17	120	S16 and jedec	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/06 15:04
S18	114	S17 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/06 15:04
S19	3515	(return\$3 or acknowlegd\$5) with (initializ\$3 or initialization) with (complet\$3 or status or finish\$3 or success\$3 or fail\$3 or error)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/06 17:41
S20	49549	(initializ\$3 or initialization) near3 (status or complet\$3 or indicat\$3 or signal)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/06 17:41
S21	3188	(mmu or controller) with S20	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/06 17:41
S22	66	S19 same S21	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/06 17:41
S23	63	S22 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO;	ADJ	OFF	2012/09/06 17:41

			DERWENT; IBM_TDB			
S24	23	(load reduced dimm) or "lr-dimm"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/06 17:58
S25	0	S20 and S24	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/06 17:58
S26	0	S19 and S24	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/06 17:58
S27	3	S24 and (initializ\$3 or initialization)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/06 17:59
S28	1	("7532537").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/06 18:06
S29	39	handshake with memory with (module or \$3dimm or chip) with controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/07 11:51
S30	30	S29 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/07 11:51
S31	53	inphi.as.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/07 13:00
S32	49549	(initializ\$3 or initialization) near3 (status or complet\$3 or indicat\$3 or signal)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/07 13:00
S33	0	S31 and S32	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/07 13:00
S34	2	isolation memory buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/07 13:12
S35	1310	(initializ\$3 or initialization) near3 (self or	US-PGPUB;	ADJ	OFF	2012/09/07

		internal) with memory	USPAT; USOCR			13:13
S36	515	S32 and S35	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/07 13:13
S37	3515	(return\$3 or acknowlegd\$5) with (initializ\$3 or initialization) with (complet\$3 or status or finish\$3 or success\$3 or fail\$3 or error)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/07 13:14
S38	19	S35 and S37	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/07 13:14
S39	17	S38 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/07 13:14
S40	20	("4862350" "5224124" "5414305" "5469376" "5615159" "5677885" "5736867" "5751641" "5760607" "5875353" "5956277" "5959485" "5983314" "6052321" "6178501" "6246623" "6246626" "6275961" "6307790" "6549975").PN. OR ("6938117").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/07 18:43
S41	49549	(initializ\$3 or initialization) near3 (status or complet\$3 or indicat\$3 or signal)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/08 08:36
S42	3188	(mmu or controller) with S41	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/08 08:36
S43	120	S42 and jedec	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/08 08:36
S44	1310	(initializ\$3 or initialization) near3 (self or internal) with memory	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/08 08:36
S45	14	S44 and S43	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/08 08:36
S46	14	S45 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/08 08:37
S47	0	(wait\$3 of halt\$3) near3 (controller or mmu)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/10 11:15
S48	18525	(wait\$3 or halt\$3) near3 (controller or mmu)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/10 11:15
S49	49549	(initializ\$3 or initialization) near3 (status or complet\$3 or indicat\$3 or signal)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/10 11:16

S50	1310	(initializ\$3 or initialization) near3 (self or internal) with memory	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/10 11:16
S51	515	S49 and S50	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/10 11:16
S52	25	S48 and S51	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/10 11:16
S53	23	S52 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/10 11:16
S54	1	("20100042778").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 12:41
S55	49549	(initializ\$3 or initialization) near3 (status or complet\$3 or indicat\$3 or signal)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/10 16:05
S56	928	S55 with interrupt\$3	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/10 16:05
S57	1310	(initializ\$3 or initialization) near3 (self or internal) with memory	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/10 16:06
S58	4	S56 and S57	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/10 16:06
S59	3515	(return\$3 or acknoweledg\$5) with (initializ\$3 or initialization) with (complet\$3 or status or finish\$3 or success\$3 or fail\$3 or error)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/10 16:09
S60	84	S59 with interrupt\$3	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/10 16:09
S61	80	S60 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/10 16:09

9/ 10/ 2012 5:32:37 PM

C:\Users\jrutz\Documents\EAST\Workspaces\12815339.wsp

<i>Index of Claims</i> 	Application/Control No. 12815339	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner JARED RUTZ	Art Unit 2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	09/10/2012								
	1	✓								
	2	✓								
	3	✓								
	4	O								
	5	✓								
	6	O								
	7	✓								
	8	O								
	9	O								
	10	O								
	11	✓								
	12	O								
	13	O								
	14	✓								
	15	O								
	16	O								
	17	O								
	18	O								
	19	✓								
	20	O								

<i>Search Notes</i> 	Application/Control No. 12815339	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner JARED RUTZ	Art Unit 2187

SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
inventor search in EAST	9/10/2012	jir
text search in EAST, see search history	9/10/2012	jir
internet search using google.com	9/10/2012	jir

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS	Application Number	12/815339
	Filing Date	14-Jun-2010
	First Named Inventor	Lee, Hyun
	Title	SYSTEMS AND METHODS FOR HANDSHAKING WITH
	Art Unit	2115
	Examiner Name	Unknown
	Attorney Docket Number	NETL.062A

I hereby revoke all previous powers of attorney given in the above-identified application.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

79141

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified application to:

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Address

City

State

Zip

Country

Telephone

Email

I am the:

☐ Applicant/Inventor.

OR

☒ Assignee of record of the entire interest. See 37 CFR 3.71.

Statement under 37 CFR 3.73(b) (Form PTO/SB/96) submitted herewith or filed on _____.

SIGNATURE of Applicant or Assignee of Record

Signature

Date

September 20, 2012

Name

Gail Sasaki

Telephone

949-435-0025

Title and Company

VP and CFO

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Netlist, Inc.

Application No./Patent No.: 12/815,339

Filed/Issue Date: 14-Jun-2010

Titled: SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

Netlist, Inc., a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;
2. ☐ an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or
3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 025216, Frame 0400, or for which a copy therefore is attached.

OR

- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

- ☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature

Gail Sasaki

Printed or Typed Name

SEPTEMBER 20, 2012

Date

VP and CFO

Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Electronic Acknowledgement Receipt	
EFS ID:	13837336
Application Number:	12815339
International Application Number:	
Confirmation Number:	1167
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	20995
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062A
Receipt Date:	25-SEP-2012
Filing Date:	14-JUN-2010
Time Stamp:	20:29:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	POA062A.pdf	348109 4c0bcd775d69ee175de35887a530db5e0cd fad99	no	2

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Information:

Total Files Size (in bytes):

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/815,339	06/14/2010	Hyun Lee	NETL.062A

CONFIRMATION NO. 1167

POA ACCEPTANCE LETTER

79141

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306



Date Mailed: 10/03/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/25/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/tnnguyen/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Hyun Lee
App. No. : 12/815,339
Filed : 6/14/2010
For : SYSTEM AND METHOD FOR
HANDSHAKING WITH A MEMORY
MODULE

Examiner : RUTZ, JARED IAN
Art Unit : 2187
Conf No. : 1167

CERTIFICATE OF EFS WEB

TRANSMISSION

I hereby certify that this correspondence and any other attachment noted on the Automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web Server on:

February 14, 2013

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Office Action dated September 14, 2012 for the above-identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

AMENDMENTS to the CLAIMS begin on Page 2 of this paper.

AMENDMENT TO THE DRAWINGS begin on Page 6 of this paper

REMARKS begin on Page 7 of this paper.

IN THE CLAIMS:

Rewrite the pending claims and add new claims as follows:

1. (Currently Amended) A memory module comprising:
at least one output configured to be operatively coupled to a memory controller of a host computer system, the memory module configured to operate in at least two modes comprising an initialization mode during which the memory module executes at least one initialization sequence and an operational mode;
a controller circuit configured to cause the memory module to enter the initialization mode; and
a notification circuit configured to drive the at least one output while the memory module is in the initialization mode to provide at least one notification signal to the memory controller indicating at least one status of the at least one initialization sequence; and
wherein the at least one notification signal triggers the memory controller to execute an interrupt routine.
2. (Original) The memory module of Claim 1, wherein the at least one status comprises completion of the at least one initialization sequence.
3. (Original) The memory module of Claim 1, wherein the at least one status comprises execution of the at least one initialization sequence.
4. (Currently Amended) The memory module of Claim 1, wherein the at least one output is configured to be operatively coupled to at least one interrupt of the memory controller ~~and the memory controller is responsive to the at least one notification signal indicating completion of the at least one initialization sequence by triggering execution of an interrupt routine by the memory controller.~~
5. (Cancelled) The memory module of Claim 4, wherein the at least one output is configured to be operated in conformance with a JEDEC standard when the memory module is in the operational mode, but is configured to be operated not in conformance with the JEDEC standard when the memory module is operated in the initialization mode.
6. (Original) The memory module of Claim 5, wherein the at least one output comprises an error-out pin of the memory module.

7. (Original) The memory module of Claim 1, wherein the notification circuit is configured to drive the at least one output to a first state indicative of execution of the at least one initialization sequence or to a second state indicative of completion of the at least one initialization sequence.

8. (Original) The memory module of Claim 7, wherein the at least one output is configured to be operatively coupled to at least one second output of a second memory module, the second memory module configured to operate in at least two modes comprising an initialization mode during which the second memory module executes at least one initialization sequence and an operational mode, the second memory module configured to drive the at least one second output of the second memory module to a third state indicative of execution of the at least one initialization sequence of the second memory module or to a fourth state indicative of completion of the at least one initialization sequence of the second memory module.

9. (Original) The memory module of Claim 8, wherein the at least one output of the first memory module and the at least one second output of the second memory module are configured to be operatively coupled to at least one interrupt of the memory controller and the memory controller is responsive to the second state of the first memory module and the fourth state of the second memory module by triggering execution of an interrupt routine by a processor of the memory controller.

10. (Original) The memory module of Claim 8, wherein the first state is a first logic level, the second state is a high-impedance state, the third state is the first logic level, and the fourth state is the high-impedance state.

11. (Currently Amended) A method of using at least one memory module, comprising:
providing a first memory module comprising at least one first output operatively coupled to a memory controller of a host computer system, the first memory module configured to operate in at least two modes comprising an initialization mode during which the first memory module executes at least one initialization sequence and an operational mode;

causing the first memory module to enter the initialization mode; driving the at least one first output to a first state while the memory module executes the at least one initialization sequence; and

upon completion of the at least one initialization sequence, driving the at least one first output to a second state different than the first state so as to trigger the memory controller to execute an interrupt routine.

12. (Original) The method of Claim 11, wherein the first state is a first logic level and the second state is a high impedance state

13. (Original) The method of Claim 11, wherein the at least one first output is operatively coupled to at least one interrupt of the memory controller such that driving the at least one output to the second state triggers the memory controller to execute an interrupt routine.

14. (Cancelled) The method of Claim 11, wherein the at least one output is defined by the JEDEC standard when the first memory module is in the operational mode, but is not defined by the JEDEC standard when the first memory module is in the initialization mode.

15. (Original) The method of Claim 11, wherein the at least one first output is a error-out pin of the first memory module.

16. (Original) The method of Claim 11, further comprising:

providing a second memory module comprising at least one second output operatively coupled to the memory controller, the second memory module configured to operate in one of at least two modes comprising an initialization mode during which the second memory module executes at least one initialization sequence and an operational mode;

causing the second memory module to enter the initialization mode;

driving the at least one second output of the second memory module to a third state while the second memory module executes the at least one initialization sequence; and

upon completion of the at least one initialization sequence, driving the at least one second output of the second memory module to a fourth state different from the third state.

17. (Original) The method of Claim 16, wherein the at least one first output of the first memory module and the at least one second output of the second memory module are operatively coupled together by a bus which is also operatively coupled to at least one input of the memory controller.

18. (Original) The method of Claim 16, wherein the at least one first output of the first memory module is operatively coupled to a first input of the memory controller and the at

least one second output of the second memory module is operatively coupled to a second input of the memory controller.

19. (Currently Amended) A method of using at least one memory module, comprising:
providing a memory module comprising at least one output operatively coupled to a memory controller of a host computer system, the memory module configured to operate in at least two modes comprising an initialization mode during which the memory module executes at least one initialization sequence and an operational mode;
causing the memory module to enter the initialization mode; and
~~receiving~~outputting a notification signal from the at least one output of the memory module, the notification signal indicating that the memory module has completed the at least one initialization sequence and triggering the memory controller to execute an interrupt routine.

20. (Currently Amended) The method of Claim 19, ~~further comprising executing an interrupt routine by the memory controller in response to the notification signal wherein the~~ notification signal is output via an error-out pin of the memory module.

AMENDMENT TO THE DRAWINGS

As shown in the Replacement Sheet filed herewith, Applicants have amended Figures 1-3 by replacing hand written number that are not clear and hand written arrows not clearly indicating what the associated numbers refer to.

REMARKS

This amendment responds to the office action mailed September 14, 2012. In the office action the Examiner:

- rejected claims 5 and 11 under 35 U.S.C. 112, first paragraph as failing to comply with the enablement requirement;
- rejected claims 5 and 11 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention;
- rejected claims 1-3, 5, 7, 11, 14, and 19 under 35 U.S.C. 103(a) as being unpatentable over Tanguay et al. (US 2010/0042778, hereinafter “Tanguay”) in view of Roohparvar (US 2003/0115427, hereafter “Roohparvar”); and
- objected to claims 4, 6, 8-10, 12, 13, 15-18, and 20 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

I. AMENDMENTS TO THE CLAIMS

Claims 5 and 14 have been canceled. Claims 1, 4, 11, 19 and 20 have been amended. After entry of this amendment, the pending claims are: claims 1-4, 6-13, and 15-20.

II. REJECTIONS OF CLAIMS 5 AND 11 UNDER 35 U.S.C. 112,

Claims 5 and 11 have been rejected under 35 U.S.C. 112, first paragraph as failing to comply with the enablement requirement. Claims 5 and 11 have also been rejected under 35 U.S.C. 112, second paragraph as failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner based these rejections on the reason that the claims make reference to “a JEDEC standard.” Since claim 11 does not make any reference to “a JEDEC standard,” the Examiner must have meant claims 5 and 14 instead of claims 5 and 11. Claims 5 and 14 are hereby cancelled, so the rejections are moot.

III. REJECTIONS OF CLAIMS 1-3, 5, 7, 11, 14, AND 19 UNDER 35 U.S.C. 103(A) AS BEING UNPATENTABLE OVER TANGUAY IN VIEW OF ROOHPARVAR

Claim 1 has been amended to include limitations recited in some of the allowable claims. For example, claims 1 as amended includes the limitation that “the at least one notification signal triggers the memory controller to execute an interrupt routine.” Claim 1 as amended is patentable over Tanguay in view of Roohparvar for at least the reason that Tanguay and Roohparvar, taken together or separately, do not disclose or suggest this limitation.

Claims 2-3, claim 4 as amended, and claims 7-10 depend from claim 1 as amended, and therefore include all of the limitations in claim 1 as amended. Thus, 2-3, claim 4 as amended, and claims 7-10 are patentable over Tanguay in view of Roohparvar for at least the same reasons as claim 1 as amended is patentable.

Claim 11 has been amended to include limitations recited in some of the allowable claims. For example, claims 11 as amended includes the limitation of: “upon completion of the at least one initialization sequence, driving the at least one first output to a second state different than the first state so as to trigger the memory controller to execute an interrupt routine.” Claim 11 as amended is patentable over Tanguay in view of Roohparvar for at least the reason that Tanguay and Roohparvar, taken together or separately, do not disclose or suggest this limitation.

Claims 12-13 and 15-18 depend from claim 11 as amended, and therefore include all of the limitations in claim 11 as amended. Thus, claims 12-13 and 15-18 are patentable over Tanguay in view of Roohparvar for at least the same reasons as claim 11 as amended is patentable.

Claim 19 has been amended to include limitations recited in some of the allowable claims. For example, claims 19 as amended includes the limitation of “the notification signal indicating that the memory module has completed the at least one initialization sequence and triggering the memory controller to execute an interrupt routine.” Claim 19 as amended is patentable over Tanguay in view of Roohparvar for at least the reason that Tanguay and Roohparvar, taken together or separately, do not disclose or suggest this limitation.

Claim 20 depends from claim 19 as amended, and therefore includes all of the limitations in claim 19 as amended. Thus, claim 20 is patentable over Tanguay in view of Roohparvar for at least the same reasons as claim 19 as amended is patentable.

Claims 5 and 14 are cancelled. Therefore, the rejection thereto is moot.

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, Applicants are not conceding in this application that previously pending claims are not patentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application. Applicants reserve the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that Applicants have made any disclaimers or disavowals of any subject matter supported by the present application.

In light of the above amendments and remarks, the Applicants respectfully request that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 273-6008, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: February 14, 2013

By: /Jamie J. Zheng/
Jamie J. Zheng
Registration No. 51,167
Customer No. 79,141
(650) 273-6008

Electronic Patent Application Fee Transmittal				
Application Number:		12815339		
Filing Date:		14-Jun-2010		
Title of Invention:		SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		
First Named Inventor/Applicant Name:		Hyun Lee		
Filer:		Jamie Jie Zheng		
Attorney Docket Number:		NETL.062A		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 2 months with \$0 paid	2252	1	285	285

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				285

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Application Number:	12815339
International Application Number:	
Confirmation Number:	1167
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062A
Receipt Date:	14-FEB-2013
Filing Date:	14-JUN-2010
Time Stamp:	23:57:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$285
RAM confirmation Number	7919
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Drawings-only black and white line drawings	Replacement_Drawing_Sheet.pdf	288273 c2e7e3871e6a2ff5e1801fdbf01401e0bb3732de	no	1
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Information:					
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	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	5	
	Drawings-only black and white line drawings		6	6	
	Applicant Arguments/Remarks Made in an Amendment		7	9	
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30449 aaae36befb9b5487d00e3c32ad82761a909e9257	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			436081		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

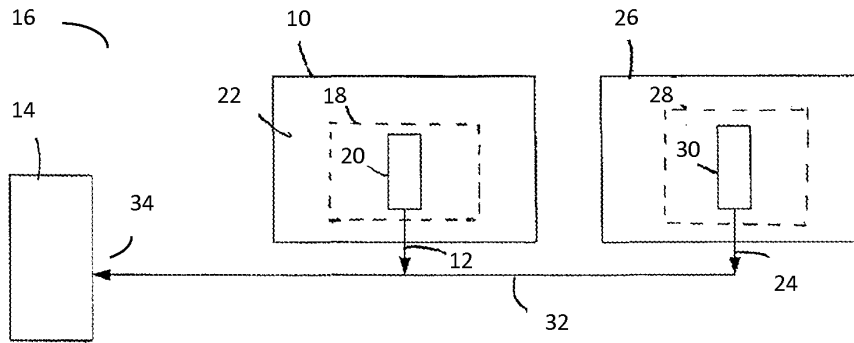


Figure 1

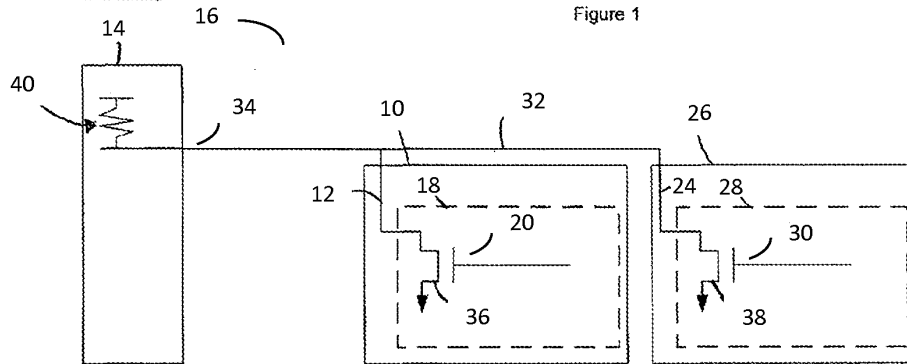


Figure 2

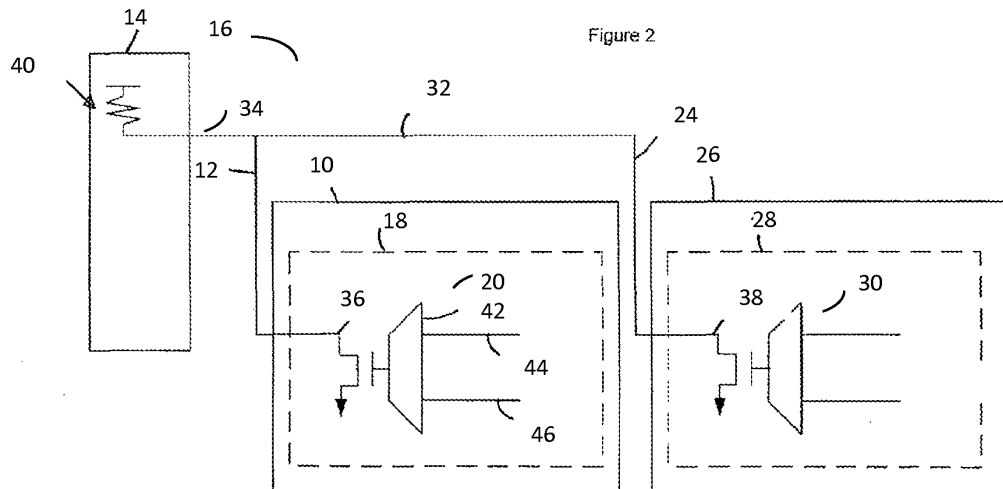


Figure 3

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/815,339		Filing Date 06/14/2010		☐ To be Mailed	
---	--	--	--	--	---	--	----------------------------------	--	---------------------------------------	--

APPLICATION AS FILED – PART I						OTHER THAN SMALL ENTITY			
(Column 1)		(Column 2)		SMALL ENTITY ☐		OR		SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A	330			
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A		N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A				
TOTAL CLAIMS (37 CFR 1.16(j))	minus 20 =	*	X \$ =		OR	X \$ =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =		OR	X \$ =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))			If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
			TOTAL		TOTAL	330			

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II						OTHER THAN SMALL ENTITY					
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR		SMALL ENTITY	
AMENDMENT	02/14/2013	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)			
Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X \$ =		OR	X \$62=	0		
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X \$ =		OR	X \$250=	0		
☐ Application Size Fee (37 CFR 1.16(s))											
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0		

(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR		SMALL ENTITY	
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)				
Total (37 CFR 1.16(i))	*	Minus	**	X \$ =		OR	X \$ =				
Independent (37 CFR 1.16(h))	*	Minus	***	X \$ =		OR	X \$ =				
☐ Application Size Fee (37 CFR 1.16(s))											
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE			

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

**ASSERTION OF ENTITLEMENT TO SMALL ENTITY STATUS UNDER 37 CFR 1.27
AND
REQUEST FOR REFUND OF EXCESS FEES PAID**

Applicant : Hyun Lee
App. No. : 12/815,339
Filed : 6/14/2010
For : SYSTEM AND METHOD FOR
HANDSHAKING WITH A MEMORY
MODULE
Examiner : RUTZ, JARED IAN
Art Unit : 2187
Conf No. : 1167

CERTIFICATE OF EFS WEB

TRANSMISSION

I hereby certify that this correspondence and any other attachment noted on the Automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web Server on:

February 14, 2013

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Assignee of all rights and title in the above-identified application, Netlist, Inc., is a small entity concern as defined in 37 C.F.R. 1.27(a). Assertion of entitlement to small entity status under 37 C.F.R. 1.27(c) is hereby made in this application.

Applicants acknowledge the duty to file notification of a loss of entitlement to small entity status in the application or patent prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate.

Respectfully submitted,

Date: February 14, 2013

/Jamie J. Zheng/

Jamie J. Zheng
Customer No. 79141

51167

(Reg. No.)

Electronic Acknowledgement Receipt	
EFS ID:	14966872
Application Number:	12815339
International Application Number:	
Confirmation Number:	1167
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062A
Receipt Date:	15-FEB-2013
Filing Date:	14-JUN-2010
Time Stamp:	01:28:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	Assertion_Small_Entity_Status.pdf	61156 5c90ca2163ecf380e8c8560a594720afd0dd299c	no	1

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

March 4, 2013

THE LAW OFFICE OF JAMIE ZHENG
P. O. BOX 60578
PALO ALTO, CA 94306
US

Dear Sir/Madam,

Your refund request for 12815339 in the amount of \$610.00 has been denied .

Small entity status fee not refundable. The time has expired for the refund of this fee. Refund under 37 CFR 1.128(a) of the MPEP 509.3 provides a three-month time period for requesting a refund of a portion of a non-small entity fee based on later establishment of small entity status. The start date of the three-month refund period of 37 CFR 1.28(a) is the date the full fee has been paid. Thus, the date of receipt of and authorization to charge fees start the three-month period for refunds under 37 CFR 1.28(a) not the date of debit of fee.

Sincerely,


Cynthia Streater
OPAP
703-756-1137



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 03/20/2013
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

EXAMINER

RUTZ, JARED IAN

ART UNIT

PAPER NUMBER

2187

DATE MAILED: 03/20/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/815,339	06/14/2010	INV001Hyun Lee	NETL.062A	1167

TITLE OF INVENTION: SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$0	\$0	\$1780	06/20/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 03/20/2013
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/815,339	06/14/2010	INV001Hyun Lee	NETL.062A	1167

TITLE OF INVENTION: SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$0	\$0	\$1780	06/20/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
RUTZ, JARED IAN	2187	711-170000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/815,339	06/14/2010	INV001Hyun Lee	NETL.062A	1167
79141	7590	03/20/2013	EXAMINER	
The Law Office of Jamie Zheng, Ph.D Esq. P.O. Box 60573 Palo Alto, CA 94306			RUTZ, JARED IAN	
			ART UNIT	PAPER NUMBER

2187

DATE MAILED: 03/20/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 335 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 335 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/815,339	LEE, HYUN	
	Examiner	Art Unit	
	JARED RUTZ	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 2/14/2013.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-4, 6-13, and 15-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. ____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date ____	6. ☐ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other ____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date ____.	

/Jared I Rutz/ Primary Examiner, Art Unit 2187	
---	--



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 1167

SERIAL NUMBER 12/815,339	FILING or 371(c) DATE 06/14/2010 RULE	CLASS 711	GROUP ART UNIT 2187	ATTORNEY DOCKET NO. NETL.062A		
APPLICANTS Hyun Lee, Ladera Ranch, CA; ** CONTINUING DATA ***** This appln claims benefit of 61/186,799 06/12/2009 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 06/23/2010						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /JARED IAN RUTZ/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 3	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS The Law Office of Jamie Zheng, Ph.D Esq. P.O. Box 60573 Palo Alto, CA 94306 UNITED STATES						
TITLE SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE						
FILING FEE RECEIVED 1220	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees			
			☐ 1.16 Fees (Filing)			
			☐ 1.17 Fees (Processing Ext. of time)			
			☐ 1.18 Fees (Issue)			
			☐ Other _____			
			☐ Credit			

Issue Classification 	Application/Control No. 12815339	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner JARED RUTZ	Art Unit 2187

CPC		
Symbol	Type	Version

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION													
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED								
711		166				G	0	6	F	9 / 00 (2006.01.01)									
CROSS REFERENCE(S)																			
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																		
713	1																		

NONE		Total Claims Allowed:	
		18	
(Assistant Examiner)	(Date)		
/JARED RUTZ/ Primary Examiner.Art Unit 2187	03/14/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

Issue Classification 	Application/Control No. 12815339	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner JARED RUTZ	Art Unit 2187

NONE		Total Claims Allowed:	
		18	
(Assistant Examiner)	(Date)		
/JARED RUTZ/ Primary Examiner.Art Unit 2187	03/14/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

<i>Search Notes</i> 	Application/Control No. 12815339	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner JARED RUTZ	Art Unit 2187

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
711	116	3/14/2013	jir
713	1	3/14/2013	jir

SEARCH NOTES		
Search Notes	Date	Examiner
inventor search in EAST	9/10/2012	jir
text search in EAST, see search history	9/10/2012	jir
internet search using google.com	9/10/2012	jir
updated search in EAST	3/14/2013	jir

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
711	166	3/14/2013	jir
713	1	3/14/2013	jir

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	5201	(lee near2 hyun).in.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/05 10:42
S2	66	S1 and (initialization or initializ\$3).clm.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/05 10:43
S3	59888	(initialization or initializ\$3) with memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/05 10:51
S4	21640	(711/101-105,154,166,167,170).OCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/05 10:53
S5	4904	(713/1).OCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/05 10:53
S6	100440	error near3 (pin or output)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/05 12:57
S7	59888	(initialization or initializ\$3) with memory	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/05 12:58
S8	73	S6 same S7	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/05 12:58
S9	70	S8 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/05 12:58
S10	23	jedec with initialization	US-PGPUB; USPAT;	ADJ	OFF	2012/09/05 18:19

			USOCR; EPO; DERWENT; IBM_TDB			
S11	20	S10 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/05 18:19
S12	1	("7586350").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/06 10:49
S13	13	("5686844" "5754879" "5905690" "6408415" "6751134" "6833741" "6903568" "6996023" "7239187").PN. OR ("7586350").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/06 10:55
S14	14	("20030179023" "4900950" "5378936" "5414378" "5438550" "5477176" "5731720" "5737612" "5929675" "5990730" "6304114").PN. OR ("6833741").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/06 11:15
S15	49549	(initializ\$3 or initialization) near3 (status or complet\$3 or indicat\$3 or signal)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/06 15:03
S16	3188	(mmu or controller) with S15	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/06 15:03
S17	120	S16 and jedec	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/06 15:04
S18	114	S17 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/06 15:04
S19	3515	(return\$3 or acknowlegd\$5) with (initializ\$3 or initialization) with (complet\$3 or status or finish\$3 or success\$3 or fail\$3 or error)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/06 17:41
S20	49549	(initializ\$3 or initialization) near3 (status or complet\$3 or indicat\$3 or signal)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/06 17:41
S21	3188	(mmu or controller) with S20	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/06 17:41
S22	66	S19 same S21	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/06 17:41
S23	63	S22 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO;	ADJ	OFF	2012/09/06 17:41

			DERWENT; IBM_TDB			
S24	23	(load reduced dimm) or "lr-dimm"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/06 17:58
S25	0	S20 and S24	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/06 17:58
S26	0	S19 and S24	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/06 17:58
S27	3	S24 and (initializ\$3 or initialization)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/06 17:59
S28	1	("7532537").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/06 18:06
S29	39	handshake with memory with (module or \$3dimm or chip) with controller	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/07 11:51
S30	30	S29 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/07 11:51
S31	53	inphi.as.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/07 13:00
S32	49549	(initializ\$3 or initialization) near3 (status or complet\$3 or indicat\$3 or signal)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/07 13:00
S33	0	S31 and S32	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/07 13:00
S34	2	isolation memory buffer	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/07 13:12
S35	1310	(initializ\$3 or initialization) near3 (self or	US-PGPUB;	ADJ	OFF	2012/09/07

		internal) with memory	USPAT; USOCR			13:13
S36	515	S32 and S35	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/07 13:13
S37	3515	(return\$3 or acknowlegd\$5) with (initializ\$3 or initialization) with (complet\$3 or status or finish\$3 or success\$3 or fail\$3 or error)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/07 13:14
S38	19	S35 and S37	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/07 13:14
S39	17	S38 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/07 13:14
S40	20	("4862350" "5224124" "5414305" "5469376" "5615159" "5677885" "5736867" "5751641" "5760607" "5875353" "5956277" "5959485" "5983314" "6052321" "6178501" "6246623" "6246626" "6275961" "6307790" "6549975").PN. OR ("6938117").URPN.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/07 18:43
S41	49549	(initializ\$3 or initialization) near3 (status or complet\$3 or indicat\$3 or signal)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/08 08:36
S42	3188	(mmu or controller) with S41	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/08 08:36
S43	120	S42 and jedec	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/08 08:36
S44	1310	(initializ\$3 or initialization) near3 (self or internal) with memory	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/08 08:36
S45	14	S44 and S43	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/08 08:36
S46	14	S45 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/08 08:37
S47	0	(wait\$3 of halt\$3) near3 (controller or mmu)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/10 11:15
S48	18525	(wait\$3 or halt\$3) near3 (controller or mmu)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/10 11:15
S49	49549	(initializ\$3 or initialization) near3 (status or complet\$3 or indicat\$3 or signal)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/10 11:16

S50	1310	(initializ\$3 or initialization) near3 (self or internal) with memory	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/10 11:16
S51	515	S49 and S50	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/10 11:16
S52	25	S48 and S51	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/10 11:16
S53	23	S52 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/10 11:16
S54	1	("20100042778").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 12:41
S55	49549	(initializ\$3 or initialization) near3 (status or complet\$3 or indicat\$3 or signal)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/10 16:05
S56	928	S55 with interrupt\$3	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/10 16:05
S57	1310	(initializ\$3 or initialization) near3 (self or internal) with memory	US-PGPUB; USPAT; USOCR	ADJ	OFF	2012/09/10 16:06
S58	4	S56 and S57	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/10 16:06
S59	3515	(return\$3 or acknowlegd\$5) with (initializ\$3 or initialization) with (complet\$3 or status or finish\$3 or success\$3 or fail\$3 or error)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/10 16:09
S60	84	S59 with interrupt\$3	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/10 16:09
S61	80	S60 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2012/09/10 16:09
S62	51522	(initializ\$3 or initialization) near3 (status or complet\$3 or indicat\$3 or signal)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2013/03/12 17:41
S63	3343	(mmu or controller) with S62	US-PGPUB; USPAT;	ADJ	OFF	2013/03/12 17:41

			USOCR			
S64	124	S63 and jedec	US-PGPUB; USPAT; USOCR	ADJ	OFF	2013/03/12 17:41
S65	1351	(initializ\$3 or initialization) near3 (self or internal) with memory	US-PGPUB; USPAT; USOCR	ADJ	OFF	2013/03/12 17:41
S66	15	S65 and S64	US-PGPUB; USPAT; USOCR	ADJ	OFF	2013/03/12 17:41
S67	14	S66 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/03/12 17:41
S68	1351	(initializ\$3 or initialization) near3 (self or internal) with memory	US-PGPUB; USPAT; USOCR	ADJ	OFF	2013/03/12 17:44
S69	3687	(return\$3 or acknoweledge\$5) with (initializ\$3 or initialization) with (complet\$3 or status or finish\$3 or success\$3 or fail\$3 or error)	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/03/12 17:44
S70	20	S68 and S69	US-PGPUB; USPAT; USOCR	ADJ	OFF	2013/03/12 17:44
S71	17	S70 and @ad<"20100614"	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/03/12 17:44
S75	1352	(initializ\$3 or initialization) near3 (self or internal) with memory	US-PGPUB; USPAT; USOCR	ADJ	OFF	2013/03/14 12:54
S76	3	S75 same (interrupt\$3 with (controller or mmu))	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	OFF	2013/03/14 12:54
S77	5598	((711/166) or (713/1)).OCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/03/14 13:00
S78	9908	(initializ\$3 or initialization) with (interrupt\$3)	US-PGPUB; USPAT; USOCR	ADJ	OFF	2013/03/14 13:45
S79	62	S77 and ((initializ\$3 or initialization) with (interrupt\$3)).clm.	US-PGPUB; USPAT; USOCR	ADJ	OFF	2013/03/14 13:46
S80	2	((("20100235579") or ("20080148048")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/03/14 14:06

3/14/2013 6:07:14 PM

C:\Users\jrtz\Documents\EAST\Workspaces\12815339.wsp



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/815,339	06/14/2010	Hyun Lee	NETL.062A	1167

79141	7590	04/29/2013
The Law Office of Jamie Zheng, Ph.D Esq. P.O. Box 60573 Palo Alto, CA 94306		

EXAMINER	
RUTZ, JARED IAN	

ART UNIT	PAPER NUMBER
2187	

NOTIFICATION DATE	DELIVERY MODE
04/29/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jz@jzpatent.com

Supplemental Notice of Allowability	Application No. 12/815,339 Examiner JARED RUTZ	Applicant(s) LEE, HYUN Art Unit 2187	AIA (First Inventor to File) Status No
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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 2/14/2013.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-4,6-13 and 15-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
 a) ☐ All b) ☐ Some *c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 * Certified copies not received: _____.

Interim copies:
 a) ☐ All b) ☐ Some c) ☐ None of the: Interim copies of the priority documents have been received.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____	5. ☒ Examiner's Amendment/Comment 6. ☐ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____
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EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jamie J. Zheng (Reg. No. 51,167) on 4/24/2013.

The application has been amended as follows:

In claim 6, line 1, replace "Claim 5" with --Claim 1--.

In claim 12, line 2, after "high impedance state" insert --.--

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JARED RUTZ whose telephone number is (571)272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christian Chace can be reached on (571)272-4190. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
Primary Examiner
Art Unit 2187

/Jared I Rutz/
Primary Examiner, Art Unit 2187

Search Notes 	Application/Control No. 12815339	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner JARED RUTZ	Art Unit 2187

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
711713	1161	3/14/20133/14/2013	jirjir

SEARCH NOTES		
Search Notes	Date	Examiner
inventor search in EASTtext search in EAST, see search historyinternet search using google.comupdated search in EAST	9/10/20129/10/20129/10/20123/14/2013	jirjirjirjir

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
711	166	3/14/2013	jir
713	1	3/14/2013	jir

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Issue Classification 	Application/Control No. 12815339	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner JARED RUTZ	Art Unit 2187

CPC		
Symbol	Type	Version

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION													
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED								
711		166				G	0	6	F	9 / 00 (2006.0)									
CROSS REFERENCE(S)																			
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																		
713	1																		

NONE		Total Claims Allowed:	
(Assistant Examiner)		18	
(Date)			
/JARED RUTZ/ Primary Examiner.Art Unit 2187		04/24/2013	
(Primary Examiner)		(Date)	
		O.G. Print Claim(s)	O.G. Print Figure
		1	4

Issue Classification 	Application/Control No. 12815339	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner JARED RUTZ	Art Unit 2187

NONE		Total Claims Allowed:	
		18	
(Assistant Examiner)	(Date)		
/JARED RUTZ/ Primary Examiner.Art Unit 2187	04/24/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

Issue Classification 	Application/Control No. 12815339	Applicant(s)/Patent Under Reexamination LEE, HYUN
	Examiner JARED RUTZ	Art Unit 2187

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

NONE		Total Claims Allowed:	
		18	
(Assistant Examiner)	(Date)		
/JARED RUTZ/ Primary Examiner.Art Unit 2187	04/24/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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Customer No. 79141

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

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Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/815,339	6/14/2010	Hyun Lee	NETL.062A	1167

TITLE OF INVENTION:

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	undiscounted	\$1780	\$0	\$0	\$1780	6/20/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.	2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 1 JAMIE J. ZHENG, Ph.D, Esq. 2 _____ 3 _____
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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE
Netlist, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)
Irvine, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☒ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-5963 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☒ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Jamie J. Zheng/

Date June 16, 2013

Typed or printed name Jamie J. Zheng

Registration No. 51,167

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		12815339		
Filing Date:		14-Jun-2010		
Title of Invention:		SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE		
First Named Inventor/Applicant Name:		Hyun Lee		
Filer:		Jamie Jie Zheng		
Attorney Docket Number:		NETL.062A		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	2501	1	890	890
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				890

Electronic Acknowledgement Receipt	
EFS ID:	16052429
Application Number:	12815339
International Application Number:	
Confirmation Number:	1167
Title of Invention:	SYSTEMS AND METHODS FOR HANDSHAKING WITH A MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.062A
Receipt Date:	17-JUN-2013
Filing Date:	14-JUN-2010
Time Stamp:	01:39:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 890
RAM confirmation Number	8590
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Issue Fee Payment (PTO-85B)	2013-06-16_Issue_Fee_Transmission_NETL062A.pdf	74181 530baaf55e7a28af71b40971c8bf586d0ab71ab	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30209 328d654ce25860e67d4628e8a613bdb99a442c34	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			104390		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/815,339	07/16/2013	8489837	NETL.062A	1167

79141 7590 06/26/2013
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 367 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Hyun Lee, Ladera Ranch, CA;

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