

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and SK HYNIX MEMORY
SOLUTIONS INC.,

Petitioners,

v.

NETLIST, INC.

Patent Owner

Patent No. 9,535,623

Issued: January 3, 2017

Filed: June 1, 2016

Inventors: Hyun Lee

Title: Memory Module Capable of Handshaking with a Memory Controller
of a Host System

Inter Partes Review No. IPR2018-00303

**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,535,623
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1-.80 & 42.100-.123**

TABLE OF CONTENTS

I.	COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW.....	1
A.	Introduction	1
B.	Certification the 623 Patent May Be Contested by Petitioner	1
C.	Fee for Inter Partes Review (§ 42.15(a)).....	2
D.	Mandatory Notices (37 CFR § 42.8(b))	2
E.	Proof of Service (§§ 42.6(e) and 42.105(a))	3
II.	Identification of Claims Being Challenged (§ 42.104(b)).....	3
III.	Relevant Information Concerning the Contested Patent	4
A.	Effective Filing Date of the 623 Patent.....	4
B.	Person of Ordinary Skill in the Art	4
C.	The 623 Patent.....	5
	1. Technical Overview	5
	2. Prosecution History	7
D.	Construction of Terms Used in the Claims	8
IV.	Overview of the Prior Art.....	15
V.	Precise Reasons for Relief Requested	20
A.	Claims 1-29 Are Obvious Over Hazelzet.....	20
B.	Claims 1-29 Are Obvious Over Hazelzet In View of Amidi.....	51
C.	Claims 1-29 Are Obvious Over Hazelzet In View of Talbot.....	57
D.	Claims 1-29 Are Obvious Over Hazelzet In View of Buchmann.....	61
E.	Claims 8, 9, 19, 20, 25, and 26 Are Obvious Over Hazelzet In View of Hokenmaier, With Or Without Amidi, Talbot, or Buchmann.....	66
F.	Claims 10, 15, and 27 Are Obvious Over Hazelzet In View of Kim, With Or Without Amidi, Talbot, or Buchmann.....	67
VI.	CONCLUSION	70

Attachment A. Proof of Service of the Petition

Attachment B. List of Evidence and Exhibits Relied Upon in Petition

I. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

A. Introduction

Petitioners respectfully request institution of trial on claims 1-29 of U.S. Patent No. 9,535,623 (“623 Patent”)(EX1001). Petitioners propose several grounds for trial, none of which is redundant. Moreover, Petitioners also address several arguments that Patent Owner may raise in response by proposing grounds that more closely satisfy the claim limitations to which such arguments would be directed. Such additional grounds are not redundant because they are “rational, narrowly targeted, and not burdensome considering only five claims with very similar limitations are at issue.” IPR2015-01912, Paper 10, 17-18. Petitioners therefore respectfully request that trial be instituted on all grounds and arguments advanced herein.

B. Certification the 623 Patent May Be Contested by Petitioner

Petitioners certify it is not barred or estopped from requesting *inter partes* review of the 623 Patent. Neither Petitioner, nor any party in privity with Petitioner, has filed a civil action challenging the validity of any claim of the 623 Patent. The 623 Patent has not been the subject of a prior *inter partes* review by Petitioner or a privy of Petitioner.

Petitioner also certifies this petition for *inter partes* review is filed within one year of the date of service of a complaint alleging infringement of a patent.

Petitioner therefore certifies this patent is available for *inter partes* review.

C. Fee for Inter Partes Review (§ 42.15(a))

The Director is authorized to charge the fee specified by 37 CFR § 42.15(a) to Deposit Account No. 50-1597.

D. Mandatory Notices (37 CFR § 42.8(b))

The real parties in interest are the Petitioners and their respective corporate parents: SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc.

The 623 Patent is involved in the following legal proceedings:

- *Netlist, Inc. v. SK Hynix Inc., SK Hynix America Inc., and SK Hynix Memory Solutions Inc.*, Case No. 8:17-cv-01030 (C.D. Ca.)
- *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1089 (International Trade Commission)

The 623 Patent is a continuation of U.S. Patent No. 8,489,837 (the “837 Patent”), which is involved in the following legal proceedings:

- *Netlist, Inc. v. SK Hynix Inc., SK Hynix America Inc., and SK Hynix Memory Solutions Inc.*, Case No. 8:16-cv-01605 (C.D. Ca.)

- *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (International Trade Commission)
- *SK Hynix Inc., SK Hynix America Inc., and SK Hynix Memory Solutions Inc. v Netlist, Inc.*, IPR2017-00548

Lead Counsel is Joseph A. Micallef (Reg. No. 39,772), Sidley-SKH-IPR@sidley.com, (202) 736-8492. Backup Lead Counsel is Wonjoo Suh (Reg. No. 64,124), Sidley-SKH-IPR@sidley.com, (202) 736-8831.

Service on Petitioner may be made by mail or hand delivery to: Sidley Austin LLP, 1501 K Street, N.W., Washington, D.C. 20005. The fax number for lead and backup counsel is (202) 736-8711.

E. Proof of Service (§§ 42.6(e) and 42.105(a))

Proof of service of this petition is provided in **Attachment A**.

II. Identification of Claims Being Challenged (§ 42.104(b))

Claims 1-29 of the 623 Patent are unpatentable as follows:

- Claims 1-29 of the 623 Patent are obvious under §103 by U.S. Patent Publication No. 2008/0098277 to Hazelzet (“Hazelzet”)(EX1014);
- Claims 1-29 of the 623 Patent are obvious under §103 by Hazelzet in view of U.S. Patent Publication No. 2008/0155378 to Amidi (“Amidi”)(EX1015);
- Claims 1-29 of the 623 Patent are obvious under §103 by Hazelzet in view of U.S. Patent Publication No. 2008/0147897 to Talbot (“Talbot”)(EX1016);

- (iv) Claims 1-29 of the 623 Patent are obvious under §103 by Hazelzet in view of U.S. Patent No. 8,139,430 to Buchmann *et al.* (“Buchmann”)(EX1017);
- (v) Claims 8, 9, 19, 20, 25, and 26 of the 623 Patent are obvious under §103 by Hazelzet in view of U.S. Patent No. 7,525,860 to Hokenmaier (“Hokenmaier”)(EX1018), with or without Amidi, Talbot, or Buchmann;
- (vi) Claims 10, 15, and 27 of the 623 Patent are obvious under §103 by Hazelzet in view of U.S. Patent No. 8,359,521 to Kim *et al.* (“Kim”)(EX1019), with or without Amidi, Talbot, or Buchmann.

Petitioner’s proposed claim constructions, the evidence relied upon, and the precise reasons why the claims are unpatentable are provided in §§ **III-V**, below. The evidence relied upon in this petition is listed in **Attachment B**.

III. Relevant Information Concerning the Contested Patent

A. Effective Filing Date of the 623 Patent

The 623 Patent claims priority to U.S. Provisional Application No. 61/186,799, filed June 12, 2009. EX1001, Face. For purposes of these proceedings Petitioners assume that the effective filing date of the 623 Patent is **June 12, 2009**. EX1008, 1; EX1003¶42.

B. Person of Ordinary Skill in the Art

A person of ordinary skill in the art in the field of the 623 Patent would be familiar with computer memory systems and basic CPU architecture documented in the literature and generally available in commercial systems as of 2009. EX1003¶43. Such literature and commercial systems would have included

techniques related to how computer components access a computer's memory, including the role of a memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory devices to the other components of the computer system. EX1003¶43. They would also include schemes for initialization of computer systems, including initialization of memory components. Such a person would also have been familiar with the standards that govern the operation of memory devices. EX1003¶43. The person of ordinary skill in the art would have had a bachelor's degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems. EX1003¶43; *see also* EX1026, 73:23-77:5.

C. The 623 Patent

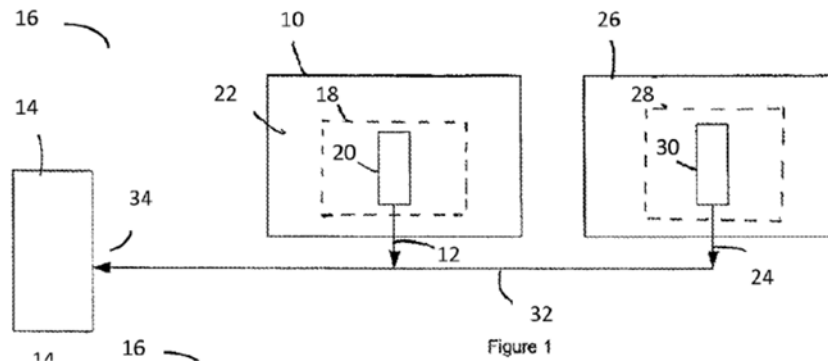
1. Technical Overview

The 623 Patent “relates to a memory module capable of handshaking with a memory controller of a host system.” EX1001, 1:23-26; EX1003¶44. The 623 Patent explains that such “initialization sequence may comprise one or more training sequences.” EX1001, 6:53-55; EX1003¶44.

According to the 623 Patent, memory controllers of the prior art would, after commencing an initialization function in a memory module, wait a predetermined amount of time and assume the memory subsystem had completed initialization. EX1001, 3:55-4:7; EX1003¶45. The 623 Patent instead suggests the use of

“handshaking” between memory controller and memory module. EX1001, 3:43-48; EX1003¶46. It states that “handshaking can be implemented in at least two ways; polling and notifying.” EX1001, 4:27-28; EX1003¶46.

Figure 1 shows a computer system including memory module 10 coupled to a memory controller 14 via “output 12” which is driven by notification circuit 20 of controller circuit 18. EX1003¶47.



EX1001, 5:8-26; FIG. 1. Memory module 26 is also shown, and has essentially in the same structure as module 14, having “output 24” driven by notification circuit 30 of controller circuit 28. EX1001, 7:7-28; EX1003¶47.

The interface between the memory controller and memory subsystem controller (of the memory module) is implemented using a technique called open drain signaling. EX1001, 4:64-5:1; *see also id.* at 10:30-36, FIGS. 2-3; EX1003¶48. Output 12 of module 10 and output 24 of module 26 are both tied to the same bus 32 using an open drain configured transistor. EX1001, 4:64-5:7; 10:34-54; FIGS. 2-3; EX1003¶48. In this manner, the system memory controller

may be provided the status of an initialization procedure using only a single line from multiple memory modules. EX1003¶49.

When starting an initialization procedure each memory module will drive its output active, placing an active signal on line 32. EX1003¶49. When the initialization is complete, the memory module can de-assert the signal on line 32. EX1003¶49. The patent states that line 32 could be tied to a standard-defined (such as JEDEC) error output pin that is not required by the standard to be used during initialization. EX1001, 8:54-9:16; EX1003¶49.

According to the 623 Patent, “the memory module 10 can be advantageously configured to both perform the standard (*e.g.*, JEDEC-specified) error reporting functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode.” EX1001, 12:12-17; EX1003¶50.

2. Prosecution History

The 623 Patent issued from U.S. Patent Application Serial No. 15/169,745 (“745 Application”), which is a continuation of various U.S. applications. EX1001, Face; EX1003¶51. The 745 Application issued after Patent Owner filed terminal disclaimers to overcome double patenting rejections. EX1002, 54-59, 63-71, 100-107; EX1003¶¶52, 53, 54. The parent applications of the 623 Patent were rejected as invalid in view of a number of prior art references, *see* EX1003¶¶55-77;

see also EX1005-EX1013, which were overcome by amendments and/or arguments. For example, during prosecution of U.S. Patent Application Serial No. 15/088,115, the applicants argued that Fahr describes “two open-drain outputs for two different error signals, /Error (CE) 120 and /Error (UE) 121, respectively,” while the claim requires “that the module controller ‘outputs to the memory controller a signal indicating a parity error’ AND ‘is further configured to drive a notification signal associated with the one or more training sequences to the memory controller’ **via the same open-drain output.**” Ex. 1005 at 143; EX1003¶60.

D. Construction of Terms Used in the Claims

In this proceeding, claims must be given their broadest reasonable construction in light of the specification. 37 CFR § 42.100(b). If Patent Owner contends terms in the claims should be read to have a special meaning, those contentions should be disregarded unless Patent Owner also amends the claims compliant with 35 U.S.C. § 112 to make them expressly correspond to those contentions. *See* 77 Fed. Reg. 48,764 at II.B.6 (August 14, 2012); *cf. In re Youman*, 679 F.3d 1335, 1343 (Fed. Cir. 2012).

1. “mode”

The 623 Patent does not purport to provide any special definition for the claim term “mode” but instead uses it in accordance with its plain and ordinary

meaning. EX1001, Abstract, 1:43-3:14, 5:13-26, 6:50-65, 7:29-40; EX1003¶¶82, 83; EX1026, 9:23-10:2. The term therefore need not be construed.

Nevertheless, in the related IPR proceeding involving the parent 837 Patent, Patent Owner argued that the term “*mode*” should be construed to mean “*a distinct behavioral state that a system may be switched to,*” IPR2017-00548, Patent Owner Response, 3. However, Patent Owner’s expert later admitted that Patent Owner’s proposed interpretation is not in accordance with the plain and ordinary meaning. EX1026, 77:14-25.

Moreover, Patent Owner’s understanding of its interpretation is inconsistent with the specification of the 837 and 623 Patents, since it precluded different claimed modes from using the same memory operations, even though the specification of the 837 and 623 Patents explicitly states the opposite. EX1001, 7:34-40; EX1026, 24:24-25:18, 25:24-29:25; EX1003¶¶84. Patent Owner’s specialized interpretation of the simple claim term “mode” is therefore legally erroneous. EX1003¶¶84. To the extent Patent Owner proposes it in this proceeding, it should be rejected.

However, to the extent the Board believes an interpretation of “mode” would be helpful, Petitioner proposes that the word “state” – when understood without all of the implicit limitations Patent Owner sought to have read into the claims in the 837 Patent IPR – is a synonym for “mode” in the context of the 623 Patent.

EX1003¶85. That word “state” is consistent with the disclosures of the 623 Patent and the dictionary Patent Owner has provided in the IPR for the parent 837 Patent. EX1028, 3; EX1003¶85. Petitioner observes that while Patent Owner’s dictionary uses the phrase “operational state,” EX1028, 3, the dictionary is clearly using the word “operational” more broadly than the 623 Patent does, since the patent explicitly equates the disclosed “operational mode” with normal memory operations and the dictionary includes no such limitation. EX1001, 7:29-34; EX1028, 3; EX1003¶85. Construing “mode” to mean “state” therefore captures the ordinary meaning of “mode” and avoids any confusion from the inconsistent use of the word “operational.” EX1003¶85.

To be clear, Petitioner does not believe interpreting “mode” to mean “state” alters the analysis set forth in this Petition or the accompanying declaration one whit, since in Petitioner’s view the two words mean the same thing to a person of skill, EX1003¶85, but Petitioner has no objection to the Board adopting that portion of Patent Owner’s dictionary definition if the Board sees it as helpful. As discussed below, the prior art discloses the first and second “*modes*” under any construction. EX1003¶¶85, 130.

2. “notification signal”

A person of ordinary skill in the art would conclude that the broadest reasonable construction of “*notification signal*” would include a “signal notifying

the memory controller of the status of the training sequence, either in response to polling or without polling.” EX1003¶86; *see also* EX1003¶¶79-81.

The claim language states that the notification signal “indicat[es] at least one status of one or more training sequences” to the memory controller. *See, e.g.*, EX1001, 15:39-43; EX1003¶87. The specification similarly describes the notification signal as “indicating at least one status of one or more training sequences ... to the memory controller,” EX1001, 1:55-60; *see also id.*, 5:20-26, 6:53-55; EX1003¶87.

Petitioner observes that it has taken the position before the International Trade Commission that the specification of the parent 837 Patent disparages “polling” as “delaying the overall initialization process,” which results in “inefficiency,” while describing the “notifying method” as an “advantageous handshaking method,” EX1001, 4:33-56; EX1003¶88, and that therefore under the *Phillips* claim construction standard this claim term should be interpreted to exclude polling, EX1025, 82-84. The ALJ did not adopt that analysis, but instead concluded that “one of ordinary skill in the art arriving at the ‘plain and ordinary’ meaning of the term ‘notification signal’ in the context of the ’837 patent would recognize that it does not utilize polling.” EX1025, 85; EX1003¶88.

Nevertheless, in the Institution Decision of IPR2017-00548 (involving the parent 837 Patent), the Board agreed, at least for purposes of institution, that the

“polling” embodiment of the prior art LeClerc patent satisfies the claimed “notification signal” under the broadest reasonable construction of that term. See IPR2017-00548, Institution Decision, at 9; EX1003¶89. Patent Owner has not disputed that conclusion and its expert has declined to interpret “notification signal” as excluding polling. EX1026, 63:17-21; EX1003¶89.

As discussed below, however, the prior art Hazelzet, Buchman, and Amidi references each disclose a “*notification signal*” whether or not polling is covered by this claim term, and Talbot discloses a “*notification signal*” under the broadest reasonable construction set forth here. EX1003¶¶90, 148, 153, 159, 167.

3. “training”

A person of ordinary skill in the art would conclude that the broadest reasonable construction of “*training*” would not be limited to “training of a memory module” but would also include “training of a memory system, including, among others, a memory module and/or a memory controller.” EX1003¶91; see also EX1003¶¶79-81.

With respect to the parent 837 Patent, Patent Owner argued in the ITC that the term “initialization” (or “training”) is broad enough to cover “initialization” (or “training”) of the “memory controller” (as opposed to the “memory module”). EX1003¶92. The ITC issued an Initial Determination concluding that “Clock-to-

CA training,” which is a training of the memory controller satisfies the “initialization” (or “training”) limitation. EX1025, 90-91; EX1003¶92.

Such a construction is not necessarily the most reasonable construction, given that the purpose of the alleged invention in the 623 Patent (and the 837 Patent) is to inform the memory controller when the memory module’s training/initialization is complete (*i.e.*, because the memory controller does not know the status of the training/initialization). *See, e.g.*, EX1001, 4:1-56; EX1003¶93. However, Patent Owner’s proposed construction should be within the broadest reasonable construction, given Patent Owner’s positions taken at the ITC. EX1003¶93.

As discussed below, Hazelzet in view of Talbot or Buchman discloses “*training*” under both the most reasonable construction and the broadest reasonable construction, and Hazelzet in view of Amidi discloses “*training*” under the broadest reasonable construction. EX1003¶¶94, 151-153, 159, 166.

4. “indicating ... status”

A person of ordinary skill in the art would conclude that the broadest reasonable construction of “*indicating ... status*” would not be limited to “providing the status that has already been determined,” but would also include “providing information that can be used to determine the status later when combined with other information.” EX1003¶95; *see also* EX1003¶¶79-81.

Initially, such a construction is not necessarily the most reasonable construction of the limitation “*indicating ... status*,” given that the “status” of the training sequence may not be considered to have been provided to the memory controller if the memory controller has to determine it later using other information. EX1003¶96. Moreover, with respect to the parent 837 Patent, the ITC issued an Initial Determination concluding that the feedback signals from the memory module do not indicate a status of the training because “these feedback signals passing through the memory module do not amount to a ‘status’ until the memory controller utilizes them to make a status determination.” EX1025, 95, 96; EX1003¶96.

However, with respect to the 837 Patent, Patent Owner argued in the ITC that a looped back training data from the memory module can indicate to the memory controller the “status” of the initialization sequence, because the memory controller can determine whether training is complete using, among others, the looped back training data. EX1025, 94; EX1003¶97. Patent Owner’s proposed construction should be within the broadest reasonable construction, given Patent Owner’s positions taken at the ITC. EX1003¶97.

As discussed below, the prior art Hazelzet, Buchman, and Amidi references each disclose “*indicating ... status*” under both the most reasonable construction and the broadest reasonable construction, and Talbot discloses “*indicating ...*

status” under the broadest reasonable construction. EX1003¶¶98, 148, 153, 159, 167.

IV. Overview of the Prior Art

A. U.S. 2008/0098277 to Hazelzet

Hazelzet was filed on October 23, 2006 and published on April 24, 2008. EX1014, Face; EX1003¶99. Hazelzet is prior art to the 623 Patent under 35 U.S.C. §§102(a), (b), and (e).

Hazelzet discloses memory modules that can operate in an “ECC mode” or a “parity mode.” EX1014, FIG. 8; *see also id.* at ¶¶[0020], [0022], [0049], [0059]-[0062], [0064], [0069]-[0070], [0072], [0075], [0081], [0101]-[0103], [0106]-[0107], [0109]; EX1003¶100.

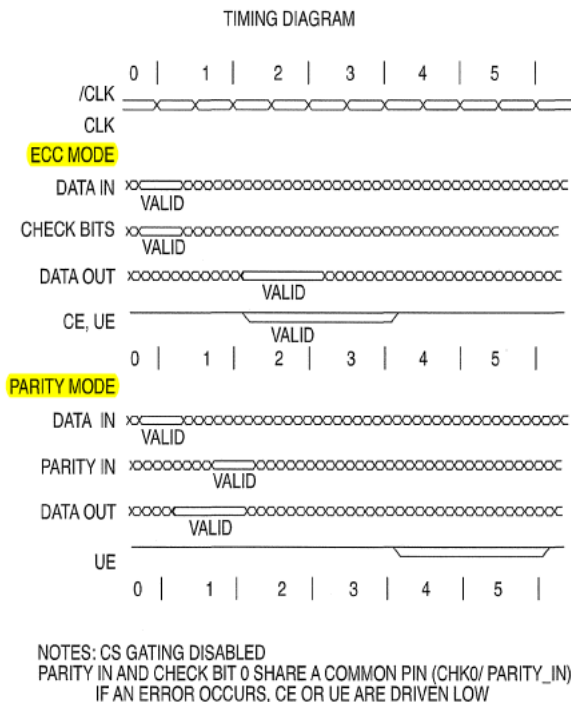


FIG. 8

Hazelzet explains that the “ECC mode” is a mode that allows the host system to detect and/or correct “correctible errors” or “uncorrectable errors.” EX1014, ¶[0069]; EX1003¶101. In the “ECC mode,” the detected correctable errors would be output through an “/Error (CE)” output pin and any uncorrectable errors (*e.g.*, double bit errors) would be reported through a “/Error (UE)” output pin. EX1014, ¶[0069]; EX1003¶101. Hazelzet explains that these two outputs (*i.e.*, CE and UE) are “open-drain outputs.” EX1014, ¶¶[0072], [0109]; EX1003¶101.

Hazelzet further explains that the “parity operating mode” is a mode that allows the host system to “interrogate the device to determine the error condition” of the memory module. EX1014, ¶[0064]; EX1003¶102. Hazelzet further explains that such “error condition” in the “parity mode” is reported to the host “via the Uncorrectable Error (UE) line” when the memory module is in the “parity mode,” EX1014, ¶[0070], which is the open-drain output that is used to report the uncorrectable errors in the “ECC mode.” EX1014, ¶¶[0072], [0109]; EX1003¶102.

Hazelzet further explains that its memory module is in the “ECC mode” when the “/ECC Mode” signal becomes “low,” EX1014, ¶[0069], and that the memory module switches to the “parity mode” when the “/ECC Mode” signal becomes “high.” EX1014, ¶[0070]; EX1003¶103.

B. U.S. 2008/0155378 to Amidi

Amidi was filed on December 21, 2006 and published on June 26, 2008.

EX1015, Face; EX1003¶104. Amidi is prior art to the 623 Patent under 35 U.S.C. §§102(a) and (e).

Amidi discloses memory systems that can enter a training mode, which is coincident with Amidi's error correction, during which the memory controller identifies "a bad memory location" so that it can avoid using that bad memory location in the future. EX1015, ¶¶[0024]-[0026]; EX1003¶105. The purpose of Amidi's training is thus to find out whether there is a bad memory location, and if so, where. EX1015, ¶[0026]; EX1003¶106.

C. U.S. 2008/0147897 to Talbot

Talbot was filed on October 31, 2006 and published on June 19, 2008.

EX1016, Face; EX1003¶107. Talbot is prior art to the 623 Patent under 35 U.S.C. §§102(a) and (e).

Talbot discloses a "training mode," during which the memory controller monitors the looped back training pattern data and shifts the training pattern data in increments until the looped back training pattern data is "byte-lock[ed]." EX1016, ¶[0052]; EX1003¶108. Once there is "byte-lock," the memory controller determines that the training has ended, and takes the memory system out of the "training mode." EX1016, ¶[0052]; EX1003¶109. Talbot explains that the

training patterns from the “buffer units” that take the memory system out of the training mode are output to the memory controller using the “CRC signal path.” EX1016, ¶[0052]; *see also* EX1016, ¶¶[0032], [0052], [0072], [0089], FIG. 4; EX1003¶110.

Talbot explains that “CRC” stands for “cyclic redundancy code.” EX1016, ¶¶[0011], [0026]; EX1003¶111. Talbot further explains that a “CRC code” may be used for error detection. EX1016, ¶[0073]; EX1003¶111.

D. U.S. 8,139,430 to Buchmann

Buchmann was filed on July 1, 2008 and issued on March 20, 2012. EX1017, Face; EX1003¶112. Buchmann is prior art to the 623 Patent under 35 U.S.C. §102(e).

Buchmann discloses two modes of operation (*i.e.*, “SBC mode” and “high-speed mode”), EX1017, Abstract, 1:39-44; EX1003¶113. The “high-speed mode” is a mode of operation “at a high nominal speed.” EX1017, 14:67-15:2; EX1003¶113. On the other hand, the “SBC mode” is a mode of operation “at a reduced rate” of communication. EX1017, 14:65-67; EX1003¶113. According to Buchmann, before the high-speed bus between the memory controller and the memory module (*e.g.*, downstream bus 110 and upstream bus 112 in FIG. 1) can be used reliably to communicate with the memory modules, the memory module operates in the SBC mode to train the high-speed bus. EX1017, 14:5-8, 3:52-54,

3:64-67; *see also id.* at FIG. 1, 4:11-14; EX1003¶113. In particular, Buchmann discloses executing training and/or initialization sequences in its “SBC mode,” which is also referred to as an “error correcting code protected quasi-static bit communication” mode. EX1017, 14:1-15:15; *see also id.* at 3:52-54, 5:6-22, 5:40-12:59, 11:48-53; EX1003¶114.

E. U.S. 7,525,860 to Hokenmaier

Hokenmaier was filed on April 30, 2007 and issued on April 28, 2009. EX1018, Face; EX1003¶115. Hokenmaier is prior art to the 623 Patent under 35 U.S.C. §102(a) and §102(e).

Hokenmaier discloses how one skilled in the art would design open-drain (or open-collector) outputs to drive notification signals. EX1018, 3:52-54, 6:27-8:7, FIGS. 4 and 6 (using MOS transistors for open-drain outputs); FIGS. 5 and 7 (using BJTs for open-collector outputs); EX1003¶116. Hokenmaier further explains that there are two ways to design open-drain outputs. EX1018, FIGS. 4 and 6; EX1003¶117. The first way is shown in FIG. 4 of Hokenmaier, *i.e.*, using an “open drain pull-down transistor,” and the second way is shown in FIG. 6 of Hokenmaier, *i.e.*, using an “open drain pull-up transistor.” EX1018, FIGS. 4 and 6; *id.* at 10:66-11:3; EX1003¶117. Likewise, there are two corresponding ways to design an open-collector output, *i.e.*, using an “open collector pull-down transistor”

or an “open collector pull-up transistor.” EX1018, FIGS. 5 and 7; *id.* at 10:66-11:3; EX1003¶117.

F. U.S. 8,359,521 to Kim

Kim was filed on January 22, 2008, the underlying application was published July 23, 2009, and the patent issued January 22, 2013. EX1019, Face; EX1003¶118. Kim is prior art to the 623 Patent pursuant to 35 U.S.C. § 102 (e).

Kim discloses a “system and method for providing a memory device having a shared error feedback pin.” EX1019, Abstract; EX1003¶119. Kim teaches how this shared error pin can be implemented using an open drain configuration and/or an OR-gate. EX1019, 5:49-57; *see also id.* at 4:40-48; 6:1-16; FIGS. 4-5; EX1003¶119.

V. Precise Reasons for Relief Requested

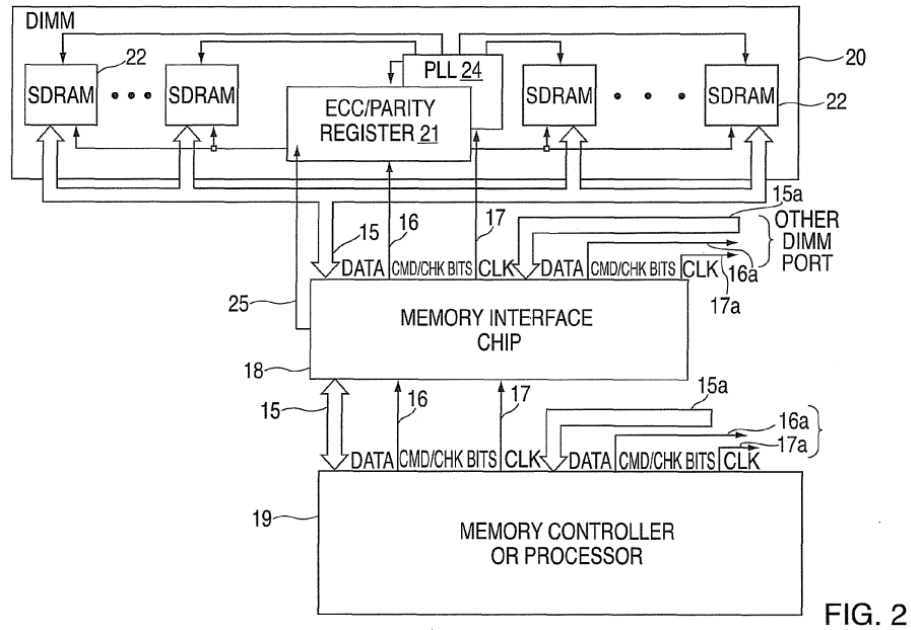
A. Claims 1-29 Are Obvious Over Hazelzet

1. Claim 1

a) Preamble

The preamble requires “[a] memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system, the memory module comprising.”

Hazelzet discloses dual inline memory modules (DIMM) that are configured to operate with the “memory controller” of the host system. EX1014, ¶¶[0037], [0038], FIG. 2; *see also* EX1014, ¶[0036]; EX1003¶122.



Hazelzet explains that the “DIMM of the present invention is comprised of a printed circuit board having a front side and a back side and a plurality of double data rate (DDR) DRAMs,” EX1014, ¶[0015], examples of which are shown in FIGS. 2, 3A, 3B, 3C, and 3D. *See* EX1014, FIGS. 2, 3A-3D; *see also id.* at ¶¶[0037], [0039]; EX1003¶123.

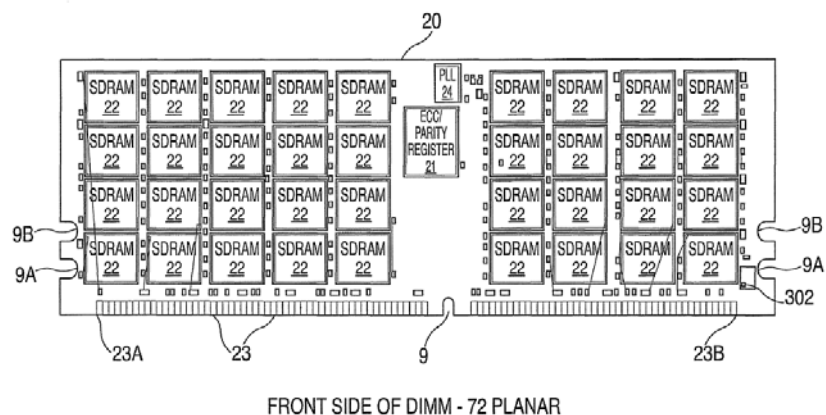
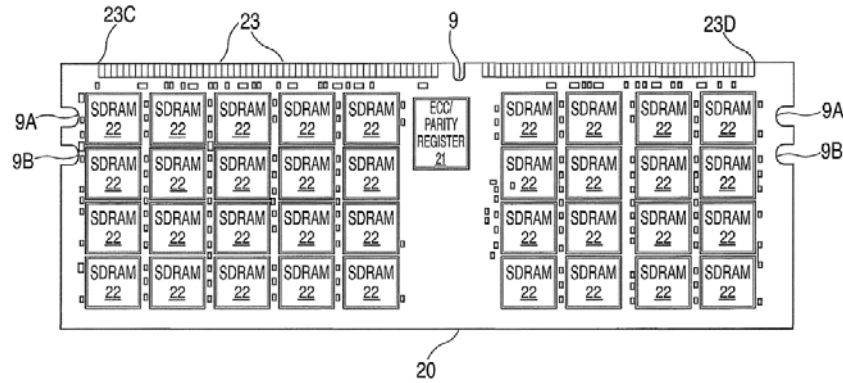
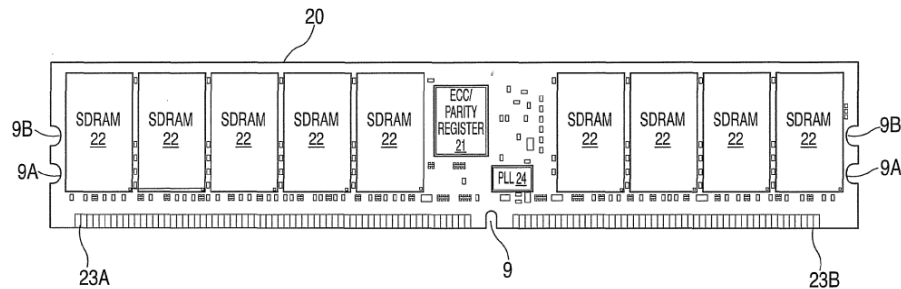


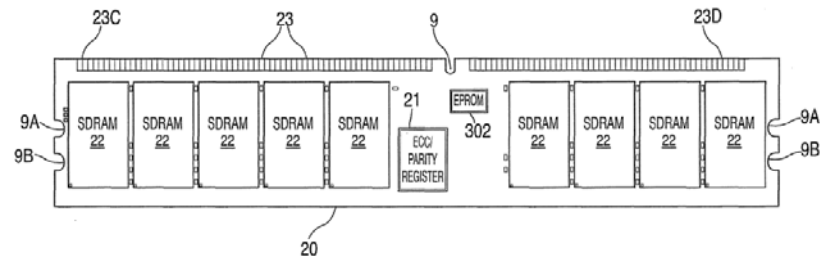
FIG. 3A



BACK SIDE OF DIMM - 72 PLANAR
FIG. 3B



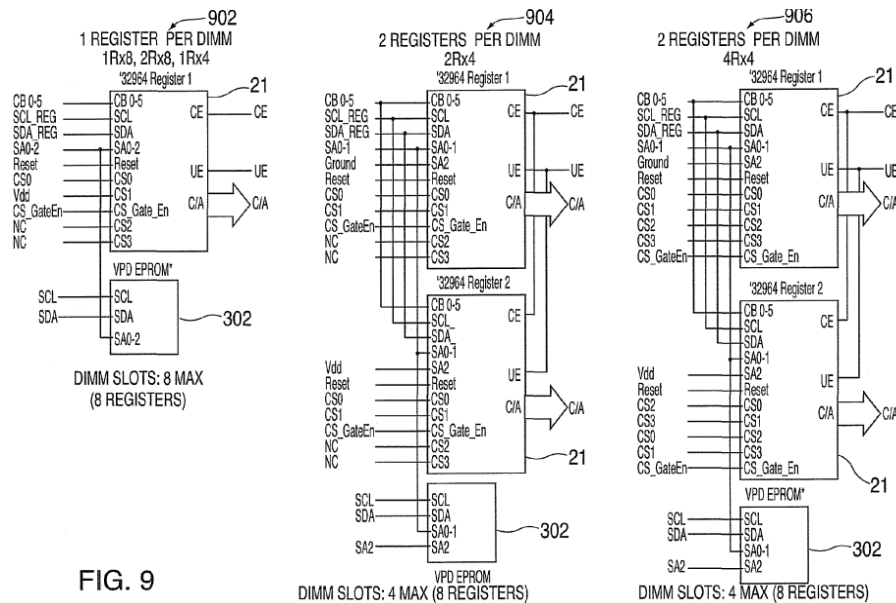
FRONT SIDE OF DIMM - 4 HIGH STACK
FIG. 3C



BACK SIDE OF DIMM - 4 HIGH STACK
FIG. 3D

Hazelzet further explains that its memory modules include “connectors 23 along the edge of both the back and front sides” of the printed circuit board, EX1014, ¶[0039], which are provided to form connections to the memory controller of the host system when the memory module is inserted into a

corresponding “slot” of the host system. EX1014, ¶¶0097]; *see also id.* at ¶¶0032], FIGS. 11, 9 (showing “DIMM slots”); EX1003¶124.



Accordingly, Hazelzet discloses the preamble. EX1003¶¶121-125.

*b) Module Controller Generating Parity Error Signal
In The First Mode*

Claim 1 requires “a module controller having an open drain output, the module controller generating a parity error signal and driving the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode, the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode.”

Hazelzet discloses an “ECC/Parity register” (“*module controller*”¹) having an output (“*open drain output*”) for uncorrectable errors (shown in FIG. 4B as “/ERROR (UE) 121”). EX1014, FIGS. 3A-3D, 4A, 4B, 5; EX1003¶127. FIGS. 4A and 4B of Hazelzet show the “ECC/Parity register” of FIGS. 3A-3D in greater detail, and FIG. 5 of Hazelzet shows the “single error correction / double error detection error correction code (SEC/DED ECC)” circuit of FIG. 4B. EX1014, ¶¶[0027], [0028]; EX1003¶127.

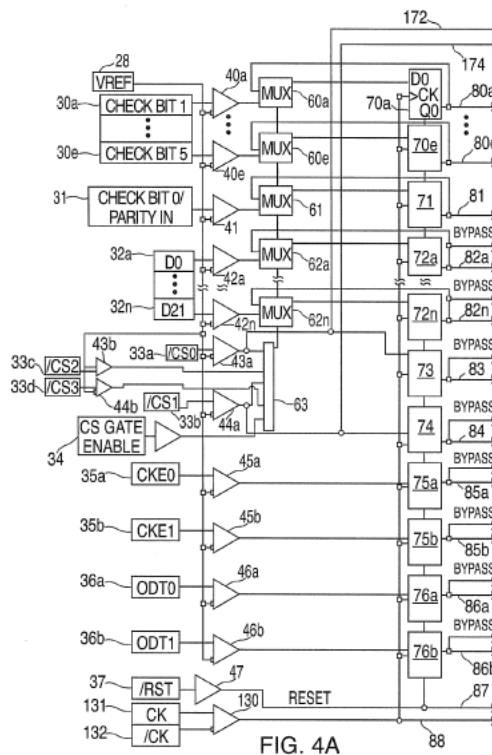


FIG. 4A

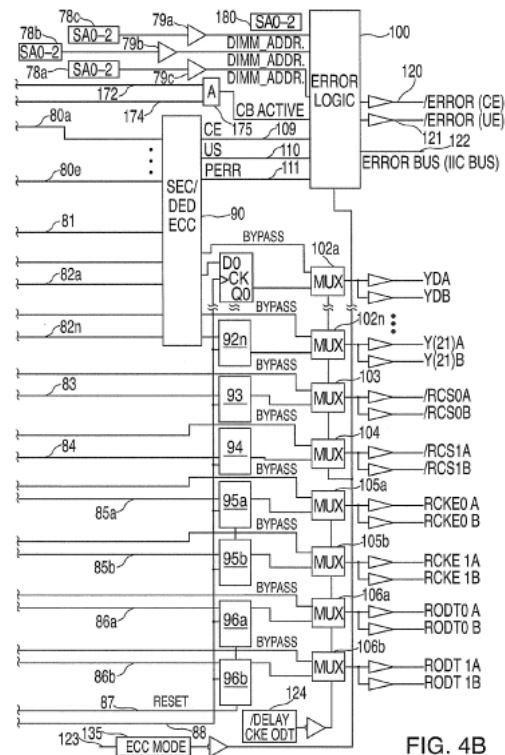


FIG. 4B

¹ Hazelzet explains that its “ECC/Parity register” is also referred to as a “buffer device” (or “ECC/Parity Buffer chip 21”). EX1014, ¶ [0038].

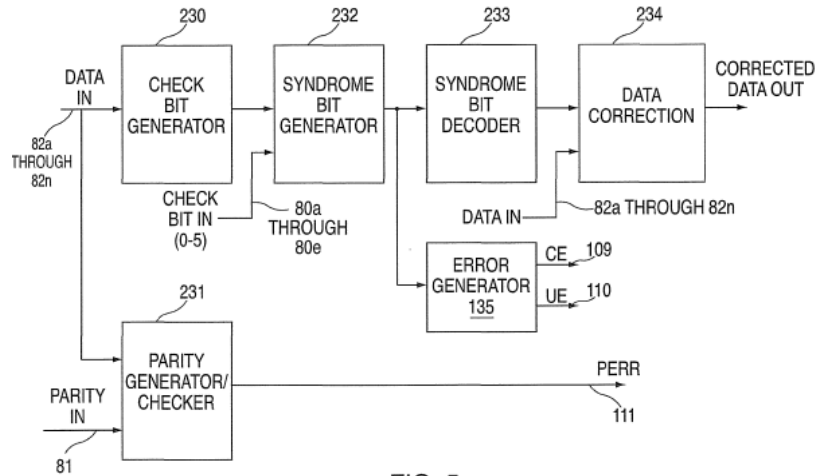


FIG. 5

As shown in FIG. 4B, the “SEC/DED ECC” circuit is coupled to an “ERROR LOGIC,” both of which being part of the “ECC/Parity register.” EX1003¶128. The “ERROR LOGIC” of the “ECC/Parity register” is coupled to an “error reporting circuitry” with two “open drain outputs,” one for correctable errors “CE” (120 of FIG. 4B) and another for uncorrectable errors “UE” (121 of FIG. 4B). EX1014, FIG. 4B, ¶¶[0072], [0109]; EX1003¶128. The output for uncorrectable errors (shown in FIG. 4B as “/ERROR (UE) 121”) is the “*open drain output*,” as claimed. EX1003¶¶128, 129.

Hazelzet explains that its memory modules operate in (1) a “parity mode,” which is the claimed “*first mode* (or state),” and (2) an “ECC mode,” which is the claimed “*second mode* (or state).” EX1014, FIG. 8; *see also id.* at ¶¶[0020], [0022], [0049], [0059]-[0062], [0064], [0069]-[0070], [0072], [0075], [0081], [0101]-[0103], [0106]-[0107], [0109]; EX1003¶130.

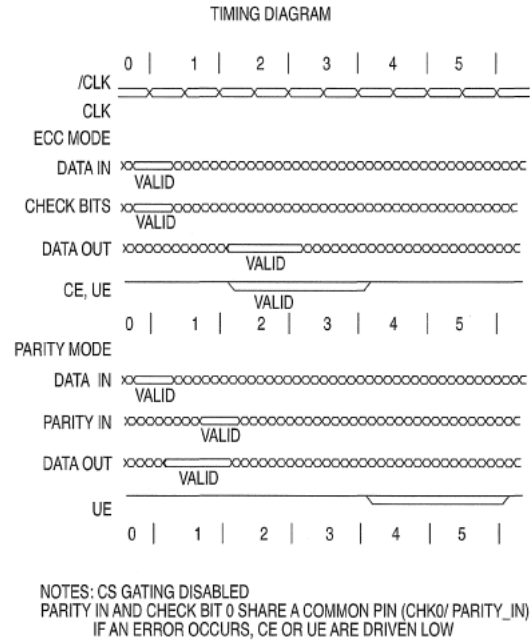


FIG. 8

Hazelzet uses the term “mode” in accordance with the plain and ordinary meaning, EX1014, FIG. 8, ¶¶[0044], [0049], [0059]-[0065], [0069]-[0072], [0075], [0095], [0102], [0103], [0107], [0109], and therefore its “parity mode” and “ECC mode” satisfy the plain and ordinary meaning of the term “mode.” EX1003¶130. Further, Hazelzet’s “parity mode” and “ECC mode” are in a “distinct behavioral state that a system may be switched to,” because Hazelzet’s system cannot be in both “modes,” or behavioral states, at the same time, Hazelzet’s two modes comprise different behaviors, EX1014, FIG. 8, ¶¶[0069], [0070], and also because Hazelzet’s system switches between each “mode,” or behavioral state, in response to the “/ECC Mode” pin. EX1014, ¶¶[0069], [0070], [0022]; EX1003¶130. The “ECC/Parity register” includes an “SEC/DED ECC” 90. EX1014, FIG. 4B; EX1003¶131. FIG. 5 of Hazelzet, which is a block diagram of the “SEC/DED

ECC” 90 in FIG. 4B, includes a “parity generator/checker circuit 231.” EX1014, ¶¶[0028], [0076], FIG. 5; EX1003¶131. When the memory module is in the “parity mode,” the “parity generator/checker circuit 231” generates and sends the “parity error signal (PERR)” to the “error logic circuit” 100. EX1014, ¶[0076], FIG. 5; *see also* EX1014, ¶[0070], FIG. 4B; EX1003¶132.

In the “parity mode,” the “parity error signal (PERR)” 111 that is fed into the “error logic circuit” 100 is output to the memory controller through the output line 121 (*i.e.*, output for uncorrectable error “UE”). EX1014, ¶[0059]; EX1003¶133. As explained above, the output line 121 (“UE”) is an open-drain output, EX1014, ¶¶[0072], [0109], which is coupled to the memory controller of the host system using pin number 142. EX1014, FIGS. 7A, FIG. 2; *see also id.* at ¶¶[0016], [0038]; EX1003¶133. Hazelzet explains that the generated parity error signal is driven to the memory controller of the host system. EX1014, ¶¶[0036], [0044], FIG. 2; *see also id.* at ¶[0072]; EX1003¶¶134, 135.

Hazelzet further explains that the parity error signal output from the “ECC/Parity register” indicates a parity error having occurred in the memory module while the memory module operates in the “parity mode.” EX1014, ¶¶[0064], [0070], [0107], [0099], [0018], FIG. 8; EX1003¶¶136, 137.

As such, Hazelzet discloses claim element 1.b. EX1003¶¶126-138.

c) Module Controller Generating Notification Signal

In The Second Mode

Claim 1 requires “*wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system, the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode and outputting the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode.*”

As demonstrated in claim 1.b., Hazelzet explains that its memory modules operate in (1) a “parity mode,” which is the claimed “*first mode*,” and (2) an “ECC mode,” which is the claimed “*second mode*.” EX1003¶¶130, 140.

Hazelzet explains that “CS gating” circuitry within its “ECC/Parity register” can “cause” the memory module to be in an inactive state when the “chip select” commands² from the memory controller of the host system is not active. EX1014, ¶[0104]; *see also id.*, ¶[0066], claim 1; EX1003¶141; EX1014, ¶[0027], FIG. 4A. Hazelzet further explains that the chip select (“CS”) commands are “from the memory controller of the host system.” EX1014, ¶[0074], FIG. 7B; EX1003¶141. Because the memory module can be in an “ECC mode” only when the

² See EX1014, ¶ [0072] (referring to “/CS” as “commands”).

“ECC/Parity register” is in an “active” state, Hazelzet’s “ECC/Parity register” is configured to cause the memory module to enter an “ECC mode” when at least one of the “chip select” commands from the memory controller of the host system is “active low.” EX1014, ¶¶[0027], [0066], [0074], [0104], FIG. 4A, claim 1; EX1003¶141. As such, under the broadest reasonable construction, Hazelzet discloses that the “*module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system.*” *Id.*

To the extent the Board concludes that Hazelzet’s “chip select” is not a “*command*,” as claimed, one skilled in the art would nevertheless have found this feature as obvious in view of Hazelzet. EX1003¶¶142-145. In particular, Hazelzet explains that its memory module is in the “ECC mode” when the “/ECC Mode” signal becomes “low,” EX1014, ¶[0069], and that the memory module is in the “parity mode” when the “/ECC Mode” signal becomes “high.” EX1014, ¶[0070]; EX1003¶143. Because the ECC Mode signals are output from the “/ECC mode signal source 135,” EX1014, FIG. 4B, the “/ECC mode signal source 135” of the “ECC/Parity register” instructs the memory module to enter into the “ECC mode” (i.e., “*second mode*”) by generating and outputting a low “/ECC Mode” signal, which is separate from and in addition to the CS commands from the memory controller. EX1014, ¶¶[0062], [0069]; EX1003¶143.

Further, Hazelzet explains that its ECC Mode input is “a programming pin.” EX1014, ¶[0106]; EX1003¶144. Hazelzet does not exclude any type of “programming” that can be used. *Id.* One skilled in the art would have recognized that there are two ways to implement such programming, *i.e.*, either (1) internally within the memory module, or alternatively (2) externally by the user through the memory controller of the host system, and would have found it obvious to try both options. EX1003¶144. Accordingly, one skilled in the art would have found it obvious to implement the “ECC/Parity register,” such that its “/ECC mode signal source 135,” is configured to instruct and cause the memory module to enter into the “ECC mode” in response to a command from the memory controller of the host system. EX1014, ¶¶[0027], [0060], [0062], [0066], [0069], [0070], [0074], [0104], [0106], FIG. 7A, FIG. 4A, FIG. 4B, FIG. 2; EX1003¶145.

Hazelzet explains that the notification signal from the “ECC/Parity register” (*i.e.*, “buffer chip”) indicates the status of the error correction sequence when the memory module is in the “ECC mode,” by indicating (1) whether “an error was identified” and (2) whether the error from the memory module is an “uncorrectable error.” EX1014, ¶¶[0059], [0069], [0072], FIG. 2, FIG. 4B, FIG. 7A; *see also id.*, at ¶¶[0079], [0081]-[0090], [0092], [0122]; EX1003¶¶146, 147, 148. Such notification signal is output through “/Error (UE)” 121, which is the “*open drain output*,” EX1014, FIG. 4B, ¶¶[0072], [0109]; EX1003¶149, coupled to the memory

controller of the host system using pin number 142. EX1014, FIG. 7A; EX1003¶149.

Hazelzet's notification signal is not a polled signal. EX1003¶148. In particular, the “address and/or command inputs” from the memory controller cannot be a request (*i.e.*, polling) for a status of the error correction sequence, because Hazelzet's notification is sent to the memory controller only when “an error was identified” as opposed to whenever the memory controller sends the “address and/or command inputs” to the memory module. EX1003¶148. Further, the “status” of the error correction sequence, *e.g.*, (1) whether “an error was identified” and/or (2) whether the error from the memory module is an “uncorrectable error,” EX1014, ¶[0059], is determined by Hazelzet's memory module before it is indicated to the memory controller via the notification signal. EX1014, FIG. 8, ¶[0069]; EX1003¶148. Accordingly, Hazelzet discloses “notification signal” and “indicating ... status” even under the narrower construction of these terms.

To the extent the Board finds that Hazelzet does not explicitly disclose that its notification signal indicates the status of a “*training*” sequence, one skilled in the art would have nevertheless found it obvious in view of Hazelzet. EX1003¶151. In particular, one skilled in the art would have understood that the purpose of “training” was to avoid errors during normal operation. *See, e.g.*,

EX1020, Abstract; EX1003¶151. Accordingly, one skilled in the art would have found it obvious to use Hazelzet's circuitry, which is capable of error detection/correction, for generating a notification signal that indicates the status of a training sequence along with error information. *See, e.g.*, EX1027, ¶[0091]; EX1003¶151; *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct., 1727, 1739-40 (2007)(“When a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result.”). Further, one skilled in the art would have understood that it was generally known to use error signals, as disclosed in Hazelzet, as part of a “training” sequence. *See, e.g.*, EX1020, 6:37-8:6, 7:21-52; EX1021, Abstract; EX1003¶151. In addition, one skilled in the art would have found this claim to be obvious over Hazelzet because it was generally known to generate and output error signals, as disclosed in Hazelzet, as part of a “training” sequence. *Id.*; EX1027, ¶[0091].

Accordingly, for reasons set forth above, Hazelzet renders claim element 1.c. obvious. EX1003¶¶139-150, 151.

d) Printed Circuit Board Communicating With Memory Controller

Claim 1 requires “a *printed circuit board having a first set of edge connections for communicating address and control signals from the memory controller of the host system, a second set of edge connections for communicating*

data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module controller.”

Hazelzet explains that the “DIMM of the present invention is comprised of a printed circuit board.” EX1014, ¶[0015]; *see also id.*, at FIGS. 3A-3D, ¶¶[0037], [0039], Abstract; EX1003¶178. Hazelzet further explains that the printed circuit board has a first set of edge connection for communicating address and control signals from the memory controller of the host system. EX1014, FIGs 7A-7C, ¶¶[0072], [0068], [0038], FIG. 2; EX1003¶179.

Hazelzet further explains that the printed circuit board has a second set of edge connection for communicating data signals between the memory module and the memory controller of the host system, EX1014, FIGs 7A-7C, while the memory module is in either the “parity mode” or the “ECC mode,” EX1014, FIG. 8; EX1003¶180.

Hazelzet further explains that the printed circuit board has an error edge connection coupled to the open drain output of the module controller. EX1014, FIGs 7A, FIG. 4B, ¶¶[0072], [0109]; EX1003¶181.

Accordingly, Hazelzet discloses claim element 1.d. EX1003¶¶177-182.

e) Memory Module's Communication With Memory

Controller In The First and Second Modes

Claim 1 requires “*the memory module communicating to the memory controller of the host system via the error edge connection the parity error signal while the memory module operates in the first mode and the notification signal while the memory module is in the second mode.*”

In the “parity mode,” the “parity error signal (PERR)” that is fed into the “error logic circuit” is output to the memory controller through the open-drain output line 121 (*i.e.*, output for uncorrectable error “UE”). EX1014, ¶¶[0059], [0070], [0072], [0076], [0109], FIGS. 2, FIG. 4B; *see also* claim element [1.b.]; EX1003¶184. The open-drain output line 121 is coupled to the memory controller of the host system using error edge connection number 142. EX1014, FIG. 7A; EX1003¶184. In the “ECC mode,” a notification signal is output to the memory controller through the open-drain output line and 121 (*i.e.*, output for uncorrectable error “UE”). EX1014, ¶¶[0059], [0069], [0072], [0092], [0109], FIG. 2, FIG. 4B; *see also* claim 1.c.; EX1003¶185. The open-drain output line 121 is coupled to the memory controller of the host system using error edge connection number 142. EX1014, FIG. 7A; EX1003¶185. Accordingly, Hazelzet discloses claim element 1.e. EX1003¶¶183-186.

2. Claim 2

Claim 2 requires “[t]he memory module of claim 1, further comprising: a plurality of synchronous dynamic random access memory elements, wherein, while the memory module is in the first mode, the module controller receives and processes address and control signals corresponding to read or write commands from the memory controller of the host system and transmits processed address and control signals to the plurality of synchronous dynamic random access memory elements.”

Hazelzet explains that its memory module includes a plurality of “synchronous dynamic random access memories,” EX1014, ¶[0015], examples of which are shown in FIGS. 2, 3A, 3B, 3C, and 3D. EX1014, FIGS. 2, 3A-3D; see also *id.*, ¶¶[0037], [0039]; EX1003¶189.

Hazelzet also explains that its memory module has connections for communicating address and control signals from the memory controller of the host system. EX1014, FIGs 7A-7C, ¶¶[0072], [0068]; EX1003¶190. One skilled in the art would have understood that the “write enable (WE)” is a control signal “corresponding to read or write commands from the memory controller of the host system.” EX1003¶190. Hazelzet further discloses driving “the address and command bits ... to the DRAMs from the memory interface chip” in the “parity mode.” EX1014, ¶[0099]; EX1003¶190. FIG. 2 of Hazelzet discloses that such

address and command bits are driven to the DRAMs from the memory interface chip through the “ECC/Parity register” using the address and command line (*i.e.*, “add/cmd line 16”). EX1014, ¶[0038], FIG. 2; EX1003¶190.

Accordingly, Hazelzet therefore renders claim 2 obvious. EX1003¶¶188-191.

3. Claim 3

Claim 3 requires “[t]he memory module of claim 1, wherein, while the memory module is in the second mode, the module controller drives the notification signal to a logic low level via the open drain output to indicate a status of the one or more training sequences.”

Hazelzet explains that, while its memory module is in the “ECC mode,” the “ECC/Parity register” drives the notification signal to a logic low level via the open drain output (*i.e.*, “/ERROR (UE) 121”) to indicate that a “double bit error” (*i.e.*, “uncorrectable error”) has been detected. EX1014, ¶¶[0069], [0059], FIG. 4B; *see also* EX1014, ¶[0072]; EX1003¶193.

Accordingly, Hazelzet renders this claim obvious. EX1003¶¶192-195.

4. Claims 4, 14, 22

Claims 4, 14 and 22 require “wherein the first mode is an operational mode of the memory module, and the second mode is a training mode of the memory module.”

Hazelzet explains that its “parity mode” is an “operating mode” with “no correction of errors.” EX1014, ¶¶[0064], [0103]; *see also id.* at ¶¶[0020], [0072], [0070]; EX1003¶197. Accordingly, Hazelzet discloses that its “parity mode” is “*an operational mode of the memory module*” under the broadest reasonable construction of the term “*operational mode*.” *Id.*

In the Institution Decision of the 837 Patent IPR, the Board “determined that it is not necessary to provide an express interpretation of any term of the claims” (including the term “operational mode”). IPR2017-00548, Paper No. 7, at 4; EX1003¶198. Even if the Board later concludes that the broadest reasonable construction of the term “operational mode” requires it to be a “normal mode of operation,” as proposed by Petitioners, Hazelzet nevertheless discloses or at least renders this claim obvious. EX1003¶198. In particular, the 623 Patent explains that “memory read/write” is an example of standard operations that are performed in the “normal mode” of operation. EX1001, 7:29-40; EX1003¶198. One skilled in the art would have known that memory systems routinely go through “parity” checking during such “normal operation” involving memory read/writes. *See, e.g.*, EX1022, 3:60-63; EX1023, 4:53-58; EX1015, ¶¶[0019]-[0021]; EX1003¶198. Accordingly, one skilled in the art would have considered Hazelzet’s “parity mode” to be a mode for “normal operation,” or alternatively, would have found it

obvious to try implementing Hazelzet's "parity mode" in a "normal mode of operation." *Id.*

On the other hand, Hazelzet explains that its "ECC mode" is a mode for "correcting single bit errors while permitting continuous memory operation independent of the existence of these errors." EX1014, ¶[0064]; EX1003¶199. As explained in claim 1.c., one skilled in the art would have found it obvious to use Hazelzet's "error correction" as part of a "training" sequence. *See, e.g.*, EX1027, ¶[0091]; EX1020, Abstract, 6:37-8:6, 7:21-52; EX1021, Abstract; EX1003¶¶151, 199; *see also* claim element [1.c.].

Accordingly, Hazelzet renders these claims obvious. EX1003¶¶196-200, 268-269, 296.

5. Claims 5, 11, 13, 23, 29

Claims 5 requires "[t]he memory module of claim 1, wherein the one or more training sequences are executed by the module controller in response to a command or a signal received from the memory controller of the host system."

Claims 11, 13, 23, 29 require "wherein the module controller [implements/executes/is further configured to implement] the one or more training sequences in response to a signal or a command received from the memory controller of the host system."

As explained in claim 1.c., Hazelzet discloses that the memory module enters into the “ECC mode” in response to a command from the memory controller of the host system, through the “ECC mode input 123.” EX1014, ¶¶[0060], [0062], [0069], [0070], FIGS. 2, 4B, 7A; *see also* claim element [1.c.]; EX1003¶¶202, 242. Hazelzet further discloses that error correction sequences are executed by the “ECC/Parity register” in the “ECC mode,” EX1003¶203, and that the “ECC/Parity register” implements the error correction sequences in the “ECC mode.” EX1003¶243. In particular, Hazelzet teaches that the “error correction code (ECC) logic” (within the “ECC/Parity register”) executes (or implements) the error correction sequences by identifying and correcting single bit errors on the command or address bus. EX1014, ¶¶[0008], [0044], [0069]; EX1003¶¶203, 243.

As explained in claim 1.c., one skilled in the art would have found it obvious to use Hazelzet’s “error correction” as part of a “training” sequence. *See, e.g.*, EX1027, ¶[0091]; EX1020, Abstract, 6:37-8:6, 7:21-52; EX1021, Abstract; EX1003¶¶151, 205, 245; *see also* claim element [1.c.].

Accordingly, Hazelzet renders these claims obvious. EX1003¶¶201-209, 241-245, 266-267, 298-299, 310-311.

6. Claims 6, 28

Claims 6 and 28 require “*wherein the module controller comprises one or more integrated circuit.*”

As explained in claim 1.b., Hazelzet's "ECC/Parity register" is also referred to as a "buffer device" or a "buffer chip." EX1014, ¶[0038]; EX1003¶211.

Hazelzet further explains that the module support devices, including "buffers," "registers," and "PLL" may be comprised of "multiple separate chips" or may be "combined onto a single package or even integrated onto a single device."

EX1014, ¶[0115] (emphasis added); *see also id.* at FIGS. 3A-3D, ¶¶[0039], [0042]; EX1003¶211. Accordingly, Hazelzet renders these claims obvious.

EX1003¶¶210-212, 308-309.

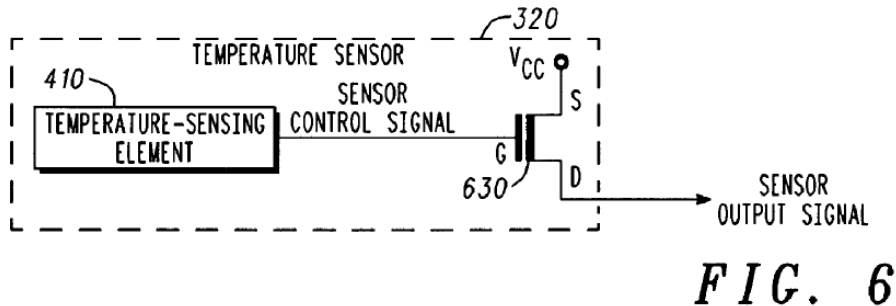
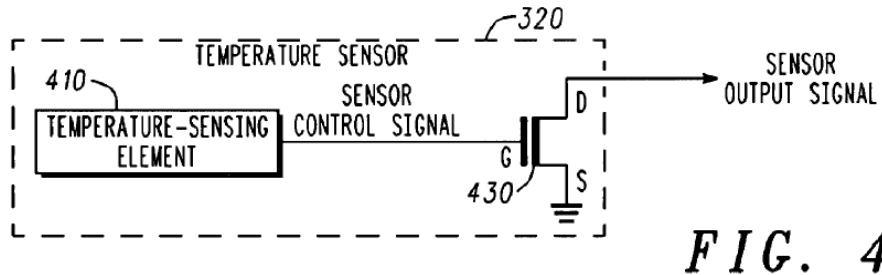
7. Claims 7, 17, 18, 24

Claim 7 requires "*wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.*" Claims 17, 18 and 24 include the same requirements.

Hazelzet explains that the "ECC/Parity register" has an "error reporting circuitry" (*i.e.*, "*notification circuit*," as claimed). EX1014, ¶¶[0072], [0044]; EX1003¶214. Hazelzet further explains that such "error reporting circuitry" includes "open-drain outputs." EX1014, ¶[0072]; EX1003¶214.

One skilled in the art would have understood that a field effect transistor necessarily has three terminals, *i.e.*, gate, source, and drain. EX1024, Title; *see also* EX1003¶215. Accordingly, one skilled in the art would understand that a circuit with an "open-drain output," which is a merely a circuit component with the

“drain” terminal “open,” includes “one or more transistors,” as claimed. *See, e.g.*, EX1018, FIGS. 4 and 6; EX1003¶¶215, 216.



As such, Hazelzet renders these claims obvious. EX1003¶¶213-217, 276-277, 278-279, 300-301.

8. Claims 8, 9, 19, 20, 25, 26

Claims 8, 9, 19, 20, 25 and 26 require “*wherein the notification circuit generates the [notification signal/parity signal] by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.*”

To the extent the Board finds that Hazelzet does not explicitly disclose driving the notification signal (claims 8, 19, 25) or a parity error signal (claims 9, 20, 26) “*by driving a gate of each of the one or more transistors to a logic high*

level such that the open drain of each of the one or more transistors provides a low impedance path to ground,” one skilled in the art would have nevertheless found this claim to be obvious in view of Hazelzet. EX1003¶¶219, 225. In particular, one skilled in the art would have known that there are only two ways to drive a notification signal using open-drain outputs, one of which is “by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground.” EX1003¶¶219, 225. Having known that there are only two options for driving a signal through an open drain output, one skilled in the art would have found it obvious to try both in the scheme of Hazelzet. See, e.g., EX1018, 3:52-60, 6:27-8:7, FIGs 4 and 6, 10:66-11:3; EX1003¶¶220, 226.

The use of either technique with the system of Hazelzet would have been only the use of known technique for its known purpose to achieve predictable results, *i.e.*, either driving a signal low or high. EX1003¶¶220, 226. A skilled artisan would have been motivated to use such techniques with Hazelzet because Hazelzet already discloses using open-drain outputs to drive its signals, and it would have been common sense to drive a signal to either a low value or a high value to convey information in a conventional digital circuit. EX1003¶¶220, 226.

Accordingly, Hazelzet renders these claims obvious. EX1003¶¶218-220, 224-226, 280-283, 302-305.

9. Claims 10, 15, 27

Claims 10, 15 and 27 require “*wherein the notification circuit [generates/is configured to generate] the notification signal using one or more OR logic elements.*”

Each of these claims requires an “open drain” circuit by virtue of dependency from claims 7, 12 and 24, respectively. As admitted by Patent Owner’s expert in the IPR for the parent 837 Patent, one skilled in the art would have understood that “open drain” signaling required a circuitry with one or more OR logic elements (*e.g.*, “wired-OR”) to send information. EX1026, 75:19-76:1; EX1003¶231. Accordingly, one skilled in the art would have found it obvious to use “*one or more OR logic elements*” to generate and output a notification signal through an “*open drain*” circuitry. *Id.*

To the extent the Board finds that Hazelzet does not explicitly disclose that “*the notification circuit generates the notification signal using one or more OR logic elements,*” as claimed, one skilled in the art would have nevertheless found this claim to be obvious in view of Hazelzet, because Hazelzet discloses using “open-drain outputs” as the output of the “*notification circuit [that] generates the notification signal[s]*” for the memory module. EX1014, ¶[0072]; EX1003¶232. In particular, Hazelzet explains that its “open-drain output” is “available to permit multiple modules to share a common signal line for reporting an error....”

EX1014, ¶[0072]; EX1003¶232. A skilled artisan would have understood that the coupling of several memory elements to a single out pin using an open drain connection effectively creates an “OR-gate” such that the pin would be asserted (i.e., active) so long as any of the memory elements so connected to the pin had asserted an active signal on that line. See EX1019, FIGS. 4, 4:5-18, 4:40-48, 4:50-57, 5:5-11, 5:49-57, 5:65-6:18, 15:7-10; see also EX1015, FIGS. 2, 4, ¶[0018]; EX1003¶232. Accordingly, these claims are obvious over Hazelzet. EX1003¶233; see also EX1003¶¶270-271, 306-307.

10. Claim 12

a) Preamble

The preamble of claim 12 requires “[a] memory module to be coupled to a memory controller of a host system, the memory module comprising.” Hazelzet discloses this claim element for the same reasons set forth in claim [1.a.] EX1003¶¶121-125, 251.

b) SDRAMs

Claim 12 requires “a plurality of synchronous dynamic random access memory elements.” Hazelzet discloses this claim element for the same reasons set forth in claim 2. EX1003¶¶188-191, 253.

c) Printed Circuit Board

Claim 12 requires “a printed circuit board (PCB) having a first set of edge connections for communicating address and control signals from the memory

controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in a first mode, the PCB further including an error edge connection in addition to the first set of edge connections and the second set of edge connections.”

Hazelzet discloses this claim element for the same reasons set forth in claim 1.d. EX1003¶¶177-182, 255.

d) Module Circuit Controlling SDRAMs In Response To Commands From Memory Controller

Claim 12 requires “*a module circuit controlling the plurality of synchronous dynamic random access memory elements in response to read and write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode.*”

Hazelzet explains that its memory module (DIMM) includes a plurality of “synchronous dynamic random access memories (SDRAMs),” EX1014, ¶[0015], examples of which are shown in FIGS. 2, 3A, 3B, 3C, and 3D. See EX1014, FIGS. 2, 3A-3D; see also *id.* at ¶¶[0037], [0039]; EX1003¶257.

Hazelzet explains that its memory module has connections for communicating address and control signals “*from the memory controller of the host system*” and that these signals are for “*controlling the plurality of synchronous dynamic random access memory elements.*” EX1014, FIGS. 7A-7C, ¶¶[0072],

[0068]; EX1003¶258. One skilled in the art would have understood that the “write enable (WE)” is an example of a “*read and write commands received from the memory controller of the host system,*” as claimed. Hazelzet further discloses driving these “address and command bits ... to the DRAMs from the memory interface chip” in the “parity mode.” EX1014, ¶[0099]; EX1003¶258. FIG. 2 of Hazelzet discloses that such address and command signals are driven to the DRAMs from the memory interface chip through the “*module circuit*” using the address and command line (*i.e.*, “add/cmd line 16”). EX1014, ¶[0038], FIG. 2; EX1003¶258. Because there are no address and command signals that are driven to the DRAMs without going through the “*module circuit,*” one skilled in the art would have understood that the “*module circuit*” controls the “*the plurality of synchronous dynamic random access memory elements in response to read and write commands received from the memory controller of the host system.*” EX1014, ¶[0038], FIG. 2; EX1003¶258.

Accordingly, Hazelzet discloses claim element 12.d. EX1003¶¶256-259; EX1003¶¶188-191; *see also* claim 2.

e) Module Circuit Generating Parity Error Signal In the First Mode

Claim 12 requires “*the module circuit generating a parity error signal indicative of a parity error having occurred in the memory module while the memory module operates in the first mode.*”

The “*module circuit*” in claim 12 is all or part of the “*module controller*” in claim 1. See dependent claims 16 and 17; EX1003¶261. Hazelzet discloses this claim element, or at least renders it obvious for the same reasons set forth in claim 1.b. EX1003¶¶126-138, 261.

f) Module Circuit Generating Notification Signal In the Second Mode

Claim 12 requires “*the module circuit causing the memory module to enter a second mode in response to a command from the memory controller of the host system, the module circuit generating a notification signal in response to one or more training sequences while the memory module is in the second mode, the notification signal indicating a status of the one or more training sequences.*”

The “*module circuit*” in claim 12 is all or part of the “*module controller*” in claim 1. See dependent claims 16 and 17; EX1003¶263. Hazelzet discloses this claim element, or at least renders it obvious for the same reasons set forth in claim 1.c. EX1003¶¶139-151, 176, 262-263.

g) Notification Circuit Of Memory Module Driving Signals To Memory Controller In The First and Second Modes

Claim 12 requires “*a notification circuit having an open drain output coupled to the error edge connection of the PCB, the notification circuit driving the parity error signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module operates in*

the first mode, the notification circuit driving the notification signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the second mode.”

The “notification circuit” in claim 12 is part of the “module controller” in claim 1. EX1003¶265. Hazelzet discloses this claim element, or at least renders it obvious for the same reasons set forth in claim 1.e. and claim 7. EX1003¶¶183-187, 213-217, 264-265.

11. Claim 16

Claim 16 requires “[t]he memory module of claim 12, wherein the notification circuit is a physically separate circuit from the module circuit.”

Hazelzet explains that the “ECC/Parity register” includes an “error reporting circuitry” (i.e., “notification circuit,” as claimed). EX1014, ¶¶[0072], [0044]; EX1003¶273.

One skilled in the art would understand that part of the “ECC/Parity register” (excluding the “error reporting circuitry”) also satisfies the “module circuit,” as claimed, for reasons set forth in claim 12. EX1003¶274. Under this mapping, Hazelzet discloses that “the notification circuit is a physically separate circuit from the module circuit,” as claimed. See claim 12; EX1014, ¶¶[0072], [0044]; EX1003¶274. Indeed, Hazelzet explains that the module support devices, including “buffers,” “registers,” and “PLL” may be comprised of “multiple

separate chips.” EX1014, ¶[0115]; EX1003¶274. As such, Hazelzet renders this claim obvious. EX1003¶¶272-275.

12. Claim 21

a) Preamble

The preamble of claim 21 requires “[a] memory module operable in at least a first mode and a second mode, the memory module comprising.”

Hazelzet discloses this claim element, or at least renders it obvious for the same reasons set forth in claim elements [1.a.], [1.b.], and [1.c.]. EX1003¶¶121-125, 126-138, 139-151, 176, 284-285.

b) SDRAMs

Claim 21 requires “a plurality of synchronous dynamic random access memory elements.”

Hazelzet discloses this claim element, or at least renders it obvious for the same reasons set forth in claim 2. EX1003¶¶188-191, 286-287.

c) Printed Circuit Board Communicating With Memory Controller

Claim 21 requires “a printed circuit board (PCB) having a first set of edge connections for communicating address and control signals from the memory controller of the host system, and a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system while the memory module operates in the first mode,

the PCB further including an error edge connection in addition to the first set of edge connections and the second set of edge connections.”

Hazelzet discloses this claim element, or at least renders it obvious for the same reasons set forth in claim 1.d. EX1003¶¶177-182, 288-289.

d) *Printed Circuit Board Fits Into Slot Connector Of Host System*

Claim 21 requires “*wherein the PCB is configured to fit into a corresponding slot connector of the host system.*”

Hazelzet discloses this claim element, or at least renders it obvious for the same reasons set forth in claim [1.a.] EX1003¶¶121-125, 290-291.

e) *Module Controller Generating/Transmitting Parity Error Signal In The First Mode*

Claim 21 requires “*a module controller having an open drain output coupled to the error edge connection, the module controller being configured to transmit address and control signals to the plurality of synchronous dynamic random access memory elements in response to read or write commands received from the memory controller of the host system via the first set of edge connections while the memory module operates in the first mode, to generate a parity error signal indicating a parity error having occurred in the memory module while the memory module is in the first mode, and to transmit the parity error signal to the memory*

controller of the host system via the open drain output and the error edge connection while the memory module is in the first mode.”

Hazelzet discloses this claim element, or at least renders it obvious for the same reasons set forth in claim 1.b., .1.e., and claim 2. EX1003¶¶126-138, 183-186, 188-191, 292-293.

f) Module Controller Generating/Transmitting Notification Signal In The Second Mode

Claim 21 requires “*the module controller being further configured to cause the memory module to enter the second mode in response to a command from the memory controller of the host system, to generate a notification signal indicating a status of one or more training sequences while the memory module is in the second mode, and to transmit the notification signal to the memory controller of the host system via the open drain output and the error edge connection while the memory module is in the second mode.*”

Hazelzet discloses this claim element, or at least renders it obvious for the same reasons set forth in claim elements [1.c] and [1.e]. EX1003¶¶139-151, 176, 183-186, 294-295.

B. Claims 1-29 Are Obvious Over Hazelzet In View of Amidi

1. Claims 1-9, 11-14, 16-26, 28-29

To the extent the Board finds that Hazelzet’s notification signal does not indicate the status of a “training” sequence nor render the claims obvious for this

reason, one skilled in the art would have nevertheless found claims 1-9, 11-14, 16-26, and 28-29 to be obvious over Hazelzet in view of Amidi, under the broadest reasonable construction of the term “*training*.” EX1003¶¶152-157; *see also* EX1003¶¶121-151, 176-229, 241-269, 272-305, 308-311.

Similar to Hazelzet, Amidi teaches a “*second mode*,” *i.e.*, error correction mode where the “memory controller” trains itself using the “error” signals from the “memory module” by learning whether the error was “random” or whether the error was due to “a bad memory location” so that it could remember not to use the bad memory location in the future (by “mark[ing]”). EX1015, ¶¶[0024], [0025], [0026]; EX1003¶153. The purpose of Amidi’s training is to find out whether there is a bad memory location, and if so, where. EX1015, ¶[0026]; EX1003¶153. Amidi’s training is done by an iterative process (*e.g.*, “retransmission”), whereby the memory controller 110 retransmits the correct address to the memory module 150 via the second bus 114. EX1015, ¶[0026]; EX1003¶153. After the retransmission, the memory module performs the error checking again, and sends a notification signal indicating the status of the training to the memory controller. EX1015, ¶[0026]; EX1003¶153.

Amidi’s notification signal is not a polled signal. EX1003¶153. In particular, the “address/command signals” from the memory controller cannot be a request (*i.e.*, polling) for a status of the training sequence, because Amidi’s

notification is sent to the memory controller only when “the error detection module 158 [of the memory module] declares an error” as opposed to whenever the memory controller sends the “address/command signals” to the memory module. EX1015, ¶¶[0026], [0024]; EX1003¶153. Accordingly, Amidi discloses “notification signal” even under the narrower construction of this term. *Id.*

One skilled in the art would have found it obvious to modify Hazelzet’s memory system such that the “memory controller” trains itself using the “error” signals from the “memory module,” during the ECC mode, by learning whether the error was “random” or whether the error was due to “a bad memory location” so that it could remember not to use the bad memory location in the future, as taught by Amidi. EX1003¶153. For example, one skilled in the art would have found it obvious to modify Hazelzet’s memory system such that, during the “ECC mode,” the memory controller trains itself not to use the bad memory location in the future upon receiving a notification signal (from the “ECC/Parity register” of the memory module). EX1014, ¶¶[0059], [0069], [0072], [0092], FIGS. 2, 4B, 7A; *see also* EX1015, ¶¶[0024]-[0026]; EX1003¶153. Such a notification signal would be indicating a “status” that had already been determined by the memory module, *i.e.*, whether the error from the specific memory location was an “uncorrectable error (UE).” EX1015, ¶¶[0026], [0024]; EX1003¶153.

This combination of Hazelzet and Amidi would have been an arrangement of old elements with each performing the same function it had been known to perform (*e.g.*, error checking/correcting) and yielding no more than what one would expect from such an arrangement (*e.g.*, improved overall system performance and/or reliability). EX1003¶153. Such a modification would have therefore been obvious. EX1003¶153.

Hazelzet and Amidi are analogous art to the 623 Patent because each is directed to the field of error detection and correction in memory modules, EX1001, Abstract, 2:35-43, 9:6-14; EX1014, ¶¶[0020], [0022], [0038], [0049], [0059]-[0062], [0069]-[0070], [0072], [0075], [0081], [0101]-[0102], [0106]-[0107], [0109]; EX1015, ¶¶[0003], [0013], [0017]-[0026], [0029], [0030], [0036]-[0037], and also because Hazelzet and Amidi are reasonably pertinent to the particular problem the inventor of the 623 Patent was trying to solve (increasing the memory system capacity, performance, and reliability by applying training sequences with errors reported using a shared output, EX1001, 9:6-14). EX1015, ¶¶[0003], [0018]; EX1014, ¶¶[0003], [0018], [0072], [0099], [0109]; EX1003¶154.

A person of ordinary skill in the art would have been motivated to combine Hazelzet and Amidi in this manner for various reasons. EX1003¶155. For example, Hazelzet emphasizes the need for “improved overall system reliability” and proposes “error correction” as a solution. EX1014, ¶[0003]; *see also* EX1014,

¶¶[0001], [0004], [0007], [0042], [0044], Abstract; EX1003¶155. One skilled in the art would have found it obvious to combine Hazelzet and Amidi because the error correction/training schemes of Amidi enhances “overall system performance” and “accuracy and operability for transmitting data...” EX1015, ¶¶[0003], [0029]; see also EX1014, ¶[0044]; EX1003¶155. For example, as explained in Amidi, once the memory controller goes through the error correction/training process, the memory controller would know the location of the “bad memory” that it should avoid in the future, thereby enhancing overall system reliability and performance. EX1015, ¶¶[0024]-[0026]; EX1003¶155. One skilled in the art would have recognized the error correction scheme of Amidi as merely another obvious variation of Hazelzet, especially given that the same “open drain” (or “open collector”) output configurations are used in both Amidi and Hazelzet to achieve the same purpose (i.e., enhancing accuracy through parity checking and/or error correction). EX1014, ¶[0072]; EX1015, ¶[0018]; EX1003¶155.

Further, given Hazelzet’s emphasis on the need for “improved overall system reliability,” one skilled in the art would have been motivated to combine Hazelzet and Amidi because normal operation could be made more reliable with error correction/training, as described in Amidi. EX1015, ¶¶[0024]-[0026]; EX1014, Abstract, ¶¶[0001], [0003], [0004], [0007], [0042], [0044]; EX1003¶156.

A person of ordinary skill in the art would have been motivated to combine Hazelzet and Amidi also because such a combination would have been merely a use of prior art techniques for prior art purposes with only expected results. EX1003¶157. For example, it was generally known to perform error correction, as disclosed in Hazelzet, as part of a “training” sequence, as disclosed in Amidi. EX1015, ¶¶[0024]-[0026]; *see also* EX1016, ¶[0088]; EX1027, ¶[0091]; EX1020, Abstract, 6:37-8:6, 7:21-52; EX1021, Abstract; EX1003¶151, 157; 205, 245. Moreover, the combination of Hazelzet and Amidi would have yielded the same result as each of the references. EX1014, ¶¶[0059], [0069]-[0072], FIGS. 2, 4A-4B, 8; EX1015, ¶¶[0024]-[0026]; EX1003¶157.

Accordingly, Hazelzet renders claims 1-9, 11-14, 16-26, and 28-29 obvious in view of Amidi. EX1003¶¶152-157; *see also* EX1003¶¶121-151, 176-229, 241-269, 272-305, 308-311.

2. Claims 10, 15, 27

To the extent the Board finds that Hazelzet does not disclose the “*one or more OR logic elements*” limitation nor render it obvious, one skilled in the art would have nevertheless found claims 10, 15, and 27 to be obvious over Hazelzet in view of Amidi. EX1003¶¶234, 270-271, 306-307; *see also* EX1003¶¶152-157.

Amidi explains that an “OR gate” or “logic OR” element can be used interchangeably with an “open collector” (*i.e.*, “open drain”) output. *See* EX1015,

¶[0018], FIGS. 2, 4, claim 17; EX1003¶234. One skilled in the art would have found it obvious to modify Hazelzet's open-drain output with the teachings of Amidi and would have been motivated to do so for reasons set forth in claim 1.c. See claim [1.c.]; EX1003¶234. Accordingly, claims 10, 15, and 27 are obvious over Hazelzet in view of Amidi. EX1003¶¶234, 270-271, 306-307; see also EX1003¶¶152-157.

C. Claims 1-29 Are Obvious Over Hazelzet In View of Talbot

To the extent the Board finds that Hazelzet's notification signal does not indicate the status of a “training” sequence nor render claims 1-29 obvious for this reason, one skilled in the art would have nevertheless found claims 1-29 to be obvious over Hazelzet in view of Talbot. EX1003¶¶158-163; see also EX1003¶¶121-151, 176-187, 188-311.

Talbot discloses a “training mode,” in which a “*notification signal indicating ... [the] status of one or more training sequences*” is sent to the memory controller, under the broadest reasonable construction of the terms “*notification signal*”³ and

³ To the extent the Board concludes that Talbot's notification signal is a polled signal because it is “looped back,” Talbot nevertheless discloses a “*notification signal*,” because under the broadest reasonable construction, the “*notification signal*” can be “in response to polling.” EX1003, ¶159

“indicating ... status.”⁴ EX1016, ¶[0052], FIGS. 1-11; EX1003¶159. Talbot further discloses that its “buffer unit 170” outputs that notification signal to the memory controller using the same output (*i.e.*, “CRC path”) that is used to send an error signal (*i.e.*, “CRC signal”) during normal operation (*i.e.*, “read and write operations”). *Id.*; see also EX1016, ¶[0049]; EX1003¶159. During its “training mode,” Talbot explains that the memory controller monitors the looped back training pattern data (*i.e.*, also referred to as the “CRC information”) and shifts the training pattern data in increments until the looped back training pattern data is “byte-locked.” EX1016, ¶¶[0053], [0052]; EX1003¶159. Once there is “byte-lock,” the memory controller determines that the training has ended, and takes the memory system out of the “training mode.” EX1016, ¶¶[0052], [0089]; EX1003¶159.

As such, one skilled in the art would have found it obvious to modify Hazelzet’s “buffer device,” such that it uses a shared notification output for both

⁴ To the extent the Board concludes that the determination of the status of the training sequence is made later by the “memory controller,” Talbot nevertheless discloses a buffer unit sending a notification signal indicating the status of the training sequence under the broadest reasonable construction. See § III.D.4; EX1003, ¶159.

training and error correction, as taught by Talbot (*e.g.*, “buffer unit 170”). *See, e.g.*, EX1016, ¶¶[0052], [0053], [0088], [0089], FIG. 2; EX1003¶159. Further, modifying Hazelzet’s “buffer device” in view of Talbot’s “buffer unit 170” would have rendered obvious the claim even under the narrower construction of “training”⁵ that is limited to “training of a memory module.” EX1003¶159.

Combination of Hazelzet and Talbot would have been an arrangement of old elements with each performing the same function it had been known to perform (*e.g.*, error checking/correcting) and yielding no more than what one would expect from such an arrangement (*e.g.*, improved overall system reliability using shared output pins). EX1003¶159. Indeed, Hazelzet explains that Talbot’s CRC is an example of its “error detection and/or correction methods.” EX1014, ¶[0127]; EX1003¶159. Such a modification would have therefore been obvious. *Id.*

Hazelzet and Talbot are analogous art to the 623 Patent because each is directed to the field of error detection and correction in memory modules, EX1001, Abstract, 2:35-43, 9:6-14; EX1014, ¶¶[0020], [0022], [0038], [0049], [0059]-

⁵ Talbot explains that its training involves “training” of the “buffer units 170.” EX1016, ¶¶[0032], [0052], [0072], [0089], FIG. 4; EX1003, ¶159. Accordingly, Talbot discloses “training” even under the narrower construction that excludes “training of a memory controller.” EX1003, ¶159.

[0062], [0069]-[0070], [0072], [0075], [0081], [0101]-[0102], [0106]-[0107], [0109], [0127]; EX1016, ¶¶[0033], [0035], [0073], and also because Hazelzet and Talbot are reasonably pertinent to the particular problem the inventor of the 623 Patent was trying to solve (increasing the memory system capacity, performance, and reliability by applying training sequences with errors reported using a shared output, EX1001, 9:6-14). *See* EX1016, ¶¶[0005], [0033], [0035], [0052], [0053], [0073]; EX1014, ¶¶[0003], [0018], [0072], [0099], [0109]; EX1003¶160.

A person of ordinary skill in the art would have been motivated to combine Hazelzet and Talbot for various reasons. EX1003¶161. For example, Hazelzet emphasizes the need for “improved overall system reliability” and proposes multiple-bit error detection and “error correction” as a solution. EX1014, ¶[0003]; *see also* EX1014, ¶¶[0001], [0004], [0007], [0042], [0044], [0063], Abstract; EX1003¶161. Similarly, Talbot notes the need for error correction as the data rates increases. *See, e.g.*, EX1016, ¶ [0033]; EX1003¶161. One skilled in the art would have found it obvious to combine Hazelzet and Talbot because the error correction/training schemes of Talbot allows the memory system to transmit data accurately and reliably even at a high rate. *Id.*

Further, given Hazelzet’s emphasis on the need for “improved overall system reliability,” one skilled in the art would have been motivated to combine Hazelzet and Talbot because normal operation could be made more reliable with

error correction/training, as described in Talbot. EX1016, ¶¶[0033], [0049], [0050], [0073]; EX1014, Abstract, ¶¶[0001], [0003], [0004], [0007], [0042], [0044]; EX1003¶162.

A person of ordinary skill in the art would have been motivated to combine Hazelzet and Talbot also because such a combination would have been merely a use of prior art techniques for prior art purposes with only expected results. EX1003¶163. For example, it was generally known to perform error correction, as disclosed in Hazelzet, as part of a “training” sequence, as disclosed in Talbot. See, e.g., EX1016, ¶[0088] (explaining that the “training pattern” is used to “calculate an error sign.”); see also EX1015, ¶¶[0024]-[0026]; EX1027, ¶[0091]; EX1020, Abstract, 6:37-8:6, 7:21-52; EX1021, Abstract; EX1003¶¶163, 151, 205, 245.

Accordingly, Hazelzet renders claims 1-29 obvious in view of Talbot. EX1003¶¶158-163; see also EX1003¶¶121-151, 176-187, 188-311.

D. Claims 1-29 Are Obvious Over Hazelzet In View of Buchmann

To the extent the Board finds that Hazelzet’s notification signal does not indicate the status of a “training” sequence nor render claims 1-29 obvious for this reason, one skilled in the art would have nevertheless found claims 1-29 to be obvious over Hazelzet in view of Buchmann. EX1003¶¶164-175; see also EX1003¶¶121-151, 176-187, 188-311.

Buchmann discloses two modes of operation (*i.e.*, “SBC mode” and “high-speed mode”), EX1017, Abstract, 1:39-44, and in particular, discloses executing training and/or initialization sequences in its “SBC mode,” which is also referred to as an “error correcting code protected quasi-static bit communication” mode (*i.e.*, a mode for establishing a “reliable communication” on the bus). EX1017, 14:1-15:15; 3:52-54, 3:64-67, 5:6-22, 5:40-12:59; EX1003¶¶165, 168. TS3, which is an example of Buchmann’s training, involves “upstream lane training” and is “used to perform upstream data lane training,” EX1017, 8:24-26, in the SBC mode, EX1017, 8:27-47, Table 5; EX1003¶¶169. Further, during the “upstream lane training” TS3, the memory module generates and outputs various notification signals indicating the status of the TS3 training sequence to the memory controller of the host system. EX1017, 8:24-9:18, Table 5, Table 6, FIG. 6; EX1003¶¶169.

One skilled in the art would have found it obvious to implement the notification techniques of Hazelzet in the “training” schemes of Buchmann that make use of the “SBC mode” (*i.e.*, error correcting mode). EX1017, 8:24-9:17; EX1003¶¶165, 171. Indeed, Buchmann explains that “multi-drop bus(es) or other shared or parallel bus(es)” can be used for such notification, EX1017, 28:23-31, and therefore one would have found it obvious to implement such notification using the open drain outputs in Hazelzet. EX1014, ¶¶[0072]; EX1003¶¶171. As such, one skilled in the art would have found the combination of Hazelzet and

Buchmann to be merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement. EX1003¶171.

Hazelzet and Buchmann are analogous art to the 623 Patent because each is directed to the field of error detection and correction in memory modules, EX1001, Abstract, 2:35-43, 9:6-14; EX1014, ¶¶[0020], [0022], [0038], [0049], [0059]-[0062], [0069]-[0070], [0072], [0075], [0081], [0101]-[0102], [0106]-[0107], [0109], [0127]; EX1017, 14:22-28, 15:33-35, 15:48-18:24, 28:23-31, 35:8-12, and also because Hazelzet and Buchmann are reasonably pertinent to the particular problem the inventor of the 623 Patent was trying to solve (increasing the memory system capacity, performance, and reliability by applying training sequences with errors reported using a shared output, EX1001, 9:6-14). *See* EX1017, 16:46-47, 28:23-65; EX1014, ¶¶[0003], [0018], [0072], [0099], [0109]; EX1003¶172.

A person of ordinary skill in the art would have been motivated to combine Hazelzet and Buchmann for various reasons. EX1003¶173. For example, Hazelzet emphasizes the need for “improved overall system reliability.” EX1014, ¶[0003]; *see also* EX1014, ¶¶[0001], [0004], [0007], [0042], [0044], Abstract; EX1003¶173. Given Hazelzet’s emphasis on the need for “improved overall system reliability,” one skilled in the art would have been motivated to combine Hazelzet and Buchmann because normal operation would be less reliable without

the training, as described in Buchmann. EX1017, 3:52-54, 14:22-35; EX1014, Abstract, ¶¶[0001], [0003], [0004], [0007], [0042], [0044]; EX1003¶173. In other words, one skilled in the art would have found it obvious to combine Hazelzet and Buchmann because the training schemes of Buchmann enhances reliability of the overall system. *Id.*

A person of ordinary skill in the art would have been motivated to combine Hazelzet and Buchmann also because one skilled in the art would have known that memory systems are initialized before normal operation. EX1003¶174. Buchmann's invention is about "initialization training sequence" once the memory system is powered on. EX1017, Abstract; EX1003¶174. Because the memory system in Hazelzet is initialized upon power-on, *see, e.g.*, EX1014, ¶[0123], one skilled in the art would have been motivated to combine Hazelzet and Buchmann. EX1003¶174. Moreover, Hazelzet expressly suggests using a "high speed bus" to "complete the initialization of the memory subsystem(s)." EX1014, ¶[0123]; EX1003¶174. Accordingly, one skilled in the art would have been motivated to initialize the memory system of Hazelzet using the initialization/error correction schemes of Buchmann, which are specifically for "high-speed channel[s]." EX1017, 1:63-67, 3:30-34, 5:13-16, 11:48-53; EX1003¶174.

A person of ordinary skill in the art would have been motivated to combine Hazelzet and Buchmann also because such a combination would have been merely

a use of prior art techniques for prior art purposes with only expected results.

EX1003¶175. For example, it was generally known to perform error correction, as disclosed in Hazelzet, as part of a “training” sequence, as disclosed in Buchmann.

See, e.g., EX1016, ¶[0088]; EX1015, ¶¶[0024]-[0026]; EX1027, ¶[0091]; EX1020, Abstract, 6:37-8:6, 7:21-52; EX1021, Abstract; EX1003¶175, 151, 205, 245.

Further, using the same output to notify error signals (e.g., CRC signals) and training status was known to one skilled in the art. See, e.g., EX1016, ¶¶[0052], [0053], FIGS. 1-11; see also EX1016, ¶[0049]; EX1003¶175.

Buchmann explains that its training involves training of components within the memory module. EX1017, 5:40-13:67, 11:48-53, FIG. 3; EX1003¶166.

Accordingly, Buchmann discloses “training” even under the narrower construction of “training” that is limited to “training of a memory module.” EX1003¶166.

Buchmann further discloses that its notifications signals can be both (1) without polling, e.g., EX1017, 8:24-9:18, Table 5, Table 6, FIG. 6, or (2) in response to polling, EX1017, 12:57-59; EX1003¶167. Accordingly, combination of Hazelzet and Buchmann would have rendered obvious the features related to the “notification signal” even under a construction that excludes “polled signal” from the scope of “notification signal.” EX1003¶167. Further, combination of Hazelzet and Buchmann would have rendered obvious the features related to the “indicating status” even under a narrower construction of that term, i.e., “providing the status

that has already been determined.” EX1017, Table 5, Table 6, FIG. 6; EX1003¶¶167, 170.

Accordingly, Hazelzet renders claims 1-29 obvious in view of Buchmann. EX1003¶¶164-175; *see also* EX1003¶¶121-151, 176-187, 188-311.

E. Claims 8, 9, 19, 20, 25, and 26 Are Obvious Over Hazelzet In View of Hokenmaier, With Or Without Amidi, Talbot, or Buchmann

To the extent claims 8, 9, 19, 20, 25, and 26 are not found to be obvious over Hazelzet, one skilled in the art would have found them to be obvious over Hazelzet in view of Hokenmaier, with or without Amidi, Talbot, or Buchmann. EX1003¶¶221-223, 227-229, 280-281, 282-283, 302-303, 304-305.

In particular, Hokenmaier discloses an open-drain output that is configured to generate a signal “*by driving a gate of each of the one or more transistors to a logic high level such that the open drain of each of the one or more transistors provides a low impedance path to ground,*” as claimed. *See* EX1018, FIG. 4; 6:38-47, 6:50-57; EX1003¶¶221, 227.

One skilled in the art would have been motivated to combine Hazelzet and Hokenmaier, because Hazelzet discloses using “open-drain outputs,” EX1014, ¶[0072], and Hokenmaier provides a comprehensive explanation as to how “open-drain outputs” can be configured. EX1018, 3:52-60, 6:27-8:7, FIGs 4 and 6, 10:66-11:3; EX1003¶¶222, 228. One skilled in the art would have been further

motivated to combine Hazelzet and Hokenmaier, because both prior art references provide schemes that address the need for connecting multiple outputs into a single output line using open-drain outputs, such that an output signal from any of the multiple lines would inform the host regarding various information (*e.g.*, notification of status or error). *See, e.g.*, EX1014, ¶[0072]; EX1018, 1:7-14; EX1003¶¶222, 228.

Accordingly, Hazelzet renders claims 8, 9, 19, 20, 25, and 26 obvious either singly or in combination with Talbot, Amidi, Buchmann, and/or Hokenmaier. EX1003¶¶221-223, 227-229, 280-281, 282-283, 302-303, 304-305.

F. Claims 10, 15, and 27 Are Obvious Over Hazelzet In View of Kim, With Or Without Amidi, Talbot, or Buchmann

To the extent claims 10, 15, and 27 are not found to be obvious over Hazelzet, these claims would have been obvious over Hazelzet in view of Kim, with or without Amidi, Talbot, or Buchmann. EX1003¶¶230-240, 270-271, 306-307.

Kim teaches coupling several memory devices to a single out pin using an open drain connection to effectively create an “OR-gate” such that the pin would be asserted (*i.e.*, active) so long as any of the memory devices so connected to the pin had asserted an active signal on that line. *See* EX1019, FIG. 4; EX1003¶235.

Alternatively, FIG. 5 of Kim shows that the signal from the “open drain output” is generated using an “OR-gate” receiving “parity error” and “CRC error” as input. EX1019, 6:13-16, FIG. 5; EX1003¶236.

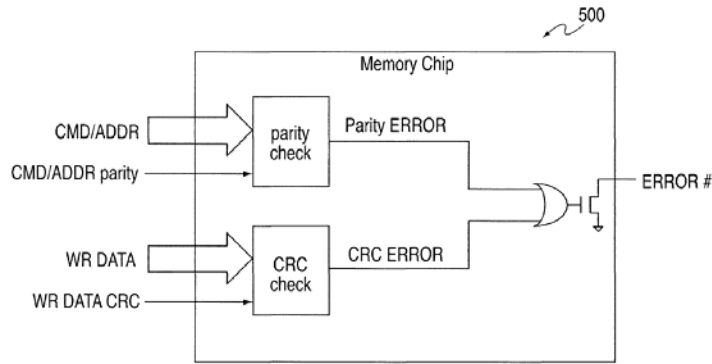


FIG. 5

Kim teaches the use of a single pin to report errors. EX1014, ¶[0072]; EX1019, 4:5-18, 4:50-57, 5:5-11, 5:49-57, 5:65-6:18, 15:7-10; EX1003¶237. Kim also proposes connecting his various memory elements to the output pin using an open drain approach. EX1014, ¶[0072]; EX1019, 5:49-57, 4:40-48; 6:1-12; FIG. 4; EX1003¶237. To use the output-pin scheme of Kim in the system of Hazelzet would therefore have been only the use of known techniques for their known purposes to achieve predictable results, *i.e.*, using a single line with an “OR logic element” to provide error or status information from multiple components. EX1003¶237.

Kim and Hazelzet are analogous art to the 623 Patent because each is directed to the field of memory systems and error detection/correction therein, EX1001, Abstract, 1:43-60, 2:20-34, 9:6-62; EX1014, FIG. 8; *see also id.*,

¶¶[0020], [0022], [0049], [0059]-[0062], [0064], [0069]-[0070], [0072], [0075], [0081], [0101]-[0103], [0106]-[0107], [0109]; EX1019, Abstract, 1:6-8, 2:7-3:2, 4:50-6:12, FIG. 4, and also because Kim and Hazelzet are reasonably pertinent to the particular problem the inventor of the 623 Patent was trying to solve (making error detection/correction of memory modules more efficient, by using shared lines, EX1001, 1:43-3:14, 9:6-26). See EX1014, ¶[0072]; EX1019, Abstract, 5:65-6:3, 6:13-16, 6:19-21, 8:33-38, 12:36-13:38, FIGS. 4-6; EX1003¶238.

Moreover, a person of ordinary skill in the art would have been motivated to use the open-drain output pin reporting technique of Kim in the scheme of Hazelzet because it represented a well-known and simply technique to provide error and/or status information from a number of memory components. EX1014, ¶¶[0072], [0122]; EX1019, FIG. 4, 12:18-23; EX1003¶239. The open-drain interrupt reporting technique of Kim permitted a single signal line with an “OR logic element” to indicate error or status information, thus simplifying the design of the system and saving pins on the various integrated circuits connected to the bus, which necessarily can have only a finite number of pins. EX1003¶239. Thus, a person of ordinary skill in the art could readily have modified Hazelzet’s open-drain output with the teachings of Kim and would have been motivated to do so. EX1003¶239.

Accordingly, Hazelzet renders claims 10, 15, and 27 obvious either singly or in combination with Talbot, Amidi, Buchmann, and/or Kim. EX1003¶¶230-240, 270-271, 306-307.

VI. CONCLUSION

Petitioner therefore respectfully requests that a Trial be instituted and that claims 1-29 be canceled as unpatentable.

Dated: December 14, 2017

Respectfully Submitted,

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**PETITION FOR INTER PARTES REVIEW
OF U.S. PATENT NO. 9,535,623**

**Attachment A:
Proof of Service of the Petition**

CERTIFICATE OF COMPLIANCE

I hereby certify that this brief complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 13,477 words (as determined by the Microsoft Word word-processing system used to prepare the brief), excluding the parts of the brief exempted by 37 C.F.R. § 42.24.

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CERTIFICATE OF SERVICE

I hereby certify that on this 14th day of December, 2017, a copy of this Petition, including all attachments, appendices and exhibits, has been served in its entirety by overnight mail on the following counsel of record for patent owner:

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**PETITION FOR INTER PARTES REVIEW
OF U.S. PATENT NO. 9,535,623**

Attachment B:

List of Evidence and Exhibits Relied Upon in Petition

Petition for *Inter Partes* Review of U.S. Patent No. 9,535,623

Exhibit #	Reference Name
1001	U.S. Patent No. 9,535,623
1002	File History of U.S. Patent No. 9,535,623
1003	Declaration of Donald Alpert
1004	Curriculum Vitae of Donald Alpert
1005	File History of U.S. Patent Application No. 15/088,115
1006	File History of U.S. Patent Application No. 13/942,721 (<i>i.e.</i> , U.S. Patent No. 9,311,116)
1007	File History of U.S. Patent Application No. 12/815,339 (<i>i.e.</i> , U.S. Patent No. 8,489,837)
1008	U.S. Provisional App. No. 61/186,799
1009	U.S. Patent Publication No. 2010/0042778 to Tanguay <i>et al.</i>
1010	U.S. Patent Publication No. 2003/0115427 to Roohparvar
1011	U.S. Patent Publication No. 2010/0202240 to Moshayedi <i>et al.</i>
1012	U.S. Patent Publication No. 2008/0256281 to Fahr <i>et al.</i>
1013	U.S. Patent Publication No. 2010/0142383 to Goishi <i>et al.</i>
1014	U.S. Patent Publication No. 2008/0098277 to Hazelzet
1015	U.S. Patent Publication No. 2008/0155378 to Amidi
1016	U.S. Patent Publication No. 2008/0147897 to Talbot
1017	U.S. Patent No. 8,139,430 to Buchmann <i>et al.</i>
1018	U.S. Patent No. 7,525,860 to Hokenmaier
1019	U.S. Patent No. 8,359,521 to Kim <i>et al.</i>
1020	U.S. Patent No. 7,647,467 to Hutsell <i>et al.</i>

Petition for *Inter Partes* Review of U.S. Patent No. 9,535,623

Exhibit #	Reference Name
1021	U.S. Patent No. 7,221,699 to Lindskog
1022	U.S. Patent No. 5,606,662 to Wisor
1023	U.S. Patent No. 7,568,130 to Smith <i>et al.</i>
1024	U.S. Patent No. 3,414,781 to Dill
1025	337-TA-1023, Initial Determination (Excerpts)
1026	Murphy Deposition Transcript in IPR2017-00548 (837 Patent)
1027	U.S. Patent Application Pub. 2005/0071580 to LeClerc <i>et al.</i>
1028	Patent Owner's Dictionary (Exhibit 2009 in IPR2017-00548)