

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SK HYNIX INC., SK HYNIX AMERICA INC., and SK HYNIX  
MEMORY SOLUTIONS INC.,  
Petitioner,

v.

NETLIST, INC.,  
Patent Owner.

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Case IPR2018-00303  
Patent 9,535,623 B1

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Before STEPHEN C. SIU, BRYAN F. MOORE, and  
SHEILA F. MCSHANE, *Administrative Patent Judges*.

SIU, *Administrative Patent Judge*.

FINAL WRITTEN DECISION  
35 U.S.C. § 318(a)

## I. INTRODUCTION

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed herein, we determine that Petitioner has shown, by a preponderance of the evidence, that claims 1–29 (“the challenged claims”) of U.S. Patent No. 9,535,623 B1 (Ex. 1001, “the ’623 patent”) are unpatentable.

## BACKGROUND

SK Hynix Inc., SK Hynix America Inc., and SK Hynix Memory Solutions Inc. (collectively, “Petitioner”) filed a Petition (Paper 1), with the supporting Declaration of Dr. Donald Alpert (Ex. 1003). Netlist, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 7), with the supporting Declaration of Robert J. Murphy (Ex. 2001). We instituted an *inter partes* review of all challenged claims (claims 1–29) of the ’623 patent. Paper 8. Patent Owner filed a Patent Owner Response (Paper 14, “PO Resp.”), with the Supplemental Declaration of Robert J. Murphy (Ex. 2005). Petitioner filed a Petitioner Reply (Paper 23, “Pet. Reply”).

Patent Owner filed a Motion to Exclude (Paper 30), Petitioner filed an Opposition to Patent Owner’s Motion to Exclude (Paper 33), and Patent Owner filed a Reply to Petitioner’s Opposition (Paper 36).

Petitioner filed a Motion to Exclude (Paper 25), Patent Owner filed an Opposition (Paper 34), and Petitioner filed a Reply to Patent Owner’s Opposition (Paper 35).

An oral hearing was held on February 6, 2019. A transcript of the hearing is included in the record. Paper 41.

## RELATED PROCEEDINGS

The '623 patent is involved in *Netlist, Inc. v. SK Hynix Inc., SK Hynix America Inc., and SK Hynix Memory Solutions Inc.*, Case No. 8:17-cv-01030 (C.D. Cal.) and *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1089 (Int'l Trade Comm'n). Pet. 2; Paper 6, 1. The '623 patent is a continuation of U.S. Patent No. 8,489,837, which is the subject of, *inter alia*, *SK Hynix Inc. v. Netlist, Inc.*, Case IPR2017-00548, in which a Final Written Decision holding claims unpatentable as obvious, issued on May 3, 2018. Case IPR2017-00548, Paper 25 (PTAB May 3, 2018).

## THE '623 PATENT (EXHIBIT 1001)

The '623 patent, titled "Memory Module Capable of Handshaking with a Memory Controller of a Host System," issued January 3, 2017, from U.S. Patent Application No. 15/169,745. Ex. 1001 at [54], [45], [21]. The '623 patent describes a memory module and a memory controller of a host system. *Id.* at 1:25–26. Figure 3 is reproduced below.

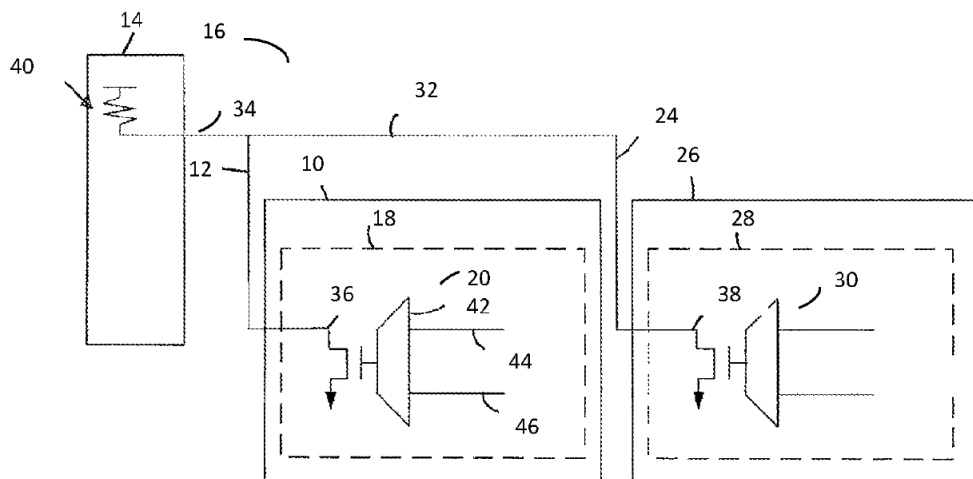


Figure 3

Figure 3 shows a host computer system including first and second memory modules configured to perform handshaking with a memory controller of the host system. Ex. 1001, 3:27–32. As shown in Figure 3, host computer system 16 includes memory controller 14, which is coupled to memory module 10 and to memory module 26. *Id.* at 5:8–25. “[M]emory module 10 is configured to operate in at least two modes comprising an initialization mode during which the memory module 10 executes at least one initialization sequence, and an operational mode.” *Id.* Memory module 10 includes controller circuit 18 configured to cause memory module 10 to enter the initialization mode and notification circuit 20 configured to provide a notification signal to memory controller 14 on output 12 while memory module 10 is in initialization mode. *Id.*

In one embodiment, for example, the at least one initialization sequence may comprise one or more training sequences.” Ex. 1001, 6:50–55. “The operational mode is the normal mode of the memory module 10.” *Id.* at 7:29–30. The status indicated by the notification signal may be, in certain embodiments, execution of the initialization sequence or completion of the initialization sequence. *Id.* at 7:48–8:10.

As shown in Figure 3, output 12 is operatively coupled to an error-out pin of memory module 10 and multiplexor 42 drives transistor 36 with either task\_in\_progress signal 44 or error signal 46 (e.g., parity error signal). *Id.* at 12:2–6. For example, multiplexor 42 may be configured to drive transistor 36 with task\_in\_progress signal 44 when memory module 10 is in initialization mode or is executing the at least one initialization sequence, and with error signal 46 when memory module 10 is in operational mode. *Id.* at 12:6–12. “Thus, the memory module 10 can be advantageously

configured to both perform the standard (e.g., JEDEC-specified) error reporting functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode.” *Id.* at 12:12–17.

### ILLUSTRATIVE CLAIM

Of the challenged claims, claims 1, 12, and 21 are independent; claims 2–11 depend, directly or indirectly, from claim 1; claims 13–20 depend, directly or indirectly, from claim 12; and claims 22–29 depend, directly or indirectly, from claim 21. Claim 1, reproduced below, is illustrative of the claimed subject matter:

1. A memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system, the memory module comprising:

a module controller having an open drain output, the module controller generating a parity error signal and driving the parity error signal to the memory controller of the host system via the open drain output while the memory module operates in a first mode, the parity error signal indicating a parity error having occurred in the memory module while the memory module operates in the first mode, wherein the module controller is configured to cause the memory module to enter a second mode in response to a command from the memory controller of the host system, the module controller generating a notification signal indicating at least one status of one or more training sequences while the memory module is in the second mode and outputting the notification signal to the memory controller of the host system via the open drain output while the memory module is in the second mode; and

a printed circuit board having a first set of edge connections for communicating address and control signals from the memory controller of the host system, a second set of edge connections for communicating data signals between the memory module and the memory controller of the host system

while the memory module operates in the first mode, and an error edge connection coupled to the open drain output of the module controller, the memory module communicating to the memory controller of the host system via the error edge connection the parity error signal while the memory module operates in the first mode and the notification signal while the memory module is in the second mode.

*Id.* at 15:26–58.

## INSTITUTED GROUNDS

We instituted trial on the following grounds of unpatentability: claims 1–29 as unpatentable under 35 U.S.C. § 103 over Hazelzet,<sup>1</sup> alone or in combination with any one of Amidi<sup>2</sup> Talbot,<sup>3</sup> or Buchmann;<sup>4</sup> claims 8, 9, 19, 20, 25, and 26 as unpatentable under 35 U.S.C. § 103 over Hazelzet and Hokenmaier,<sup>5</sup> with or without Amidi, Talbot, or Buchmann; and claims 10, 15, and 27 under 35 U.S.C. § 103 over Hazelzet and Kim,<sup>6</sup> with or without Amidi, Talbot, or Buchmann. Pet. 3–4.

## II. ANALYSIS

### THE PARTIES’ POST-INSTITUTION ARGUMENTS

In our Decision on Institution, we concluded that the arguments and evidence advanced by Petitioner demonstrated a reasonable likelihood that

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<sup>1</sup> US Patent Publication 2008/0098277 A1, dated April 24, 2008 (Ex. 1014, “Hazelzet”).

<sup>2</sup> US Patent Publication 2008/0155378 A1, published June 26, 2008 (Ex. 1015, “Amidi”).

<sup>3</sup> US Patent Publication 2008/0147897 A1, published June 19, 2008 (Ex. 1016, “Talbot”).

<sup>4</sup> US Patent 8,139,430 B2, issued March 20, 2012 (Ex. 1017, “Buchmann”).

<sup>5</sup> US Patent 7,525,860 B2, issued April 28, 2009 (Ex. 1018, “Hokenmaier”).

<sup>6</sup> US Patent 8,359,521 B2, issued January 22, 2013 (Ex. 1019, “Kim”).

claims 1–29 of the ’623 patent would have been unpatentable under 35 U.S.C. § 103 based on certain asserted grounds of unpatentability. Dec. 6–17. We now determine whether Petitioner has established by a preponderance of the evidence that claims 1–29 are unpatentable over the asserted prior art. 35 U.S.C. § 316(e). We previously instructed Patent Owner that “any arguments for patentability not raised and fully briefed in the response will be deemed waived.” Paper 9, 3; *see also* 37 C.F.R. § 42.23(a) (“Any material fact not specifically denied may be considered admitted.”); *In re NuVasive, Inc.*, 842 F.3d 1376, 1379–82 (Fed. Cir. 2016) (holding patent owner waived an argument addressed in Preliminary Response by not raising the same argument in the Patent Owner Response). Additionally, the Board’s Trial Practice Guide states that the Patent Owner Response “should identify all the involved claims that are believed to be patentable and state the basis for that belief.” Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012).

With a complete record before us, we note that we have reviewed all of the arguments and evidence advanced by Petitioner to support its unpatentability contentions, including arguments and evidence addressing limitations Patent Owner chose not to address in its Patent Owner Response. Based on the preponderance of the evidence before us, we conclude that certain asserted obviousness grounds render unpatentable claims 1–29 of the ’623 patent.

#### OBVIOUSNESS OVER HAZELZET AND ONE OF BUCHMANN OR TALBOT

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that

the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.<sup>7</sup> *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

*Person of Ordinary Skill in the Art*

Petitioner's expert, Dr. Alpert, testifies that one of ordinary skill in the art would be someone who was familiar with computer memory systems and basic CPU architecture, which includes knowledge of techniques related to how computer components access a computer's memory, including the role of a memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory, as well as applicable standards. Ex. 1003 ¶ 43; *see also* Pet. 4–5 (providing further explanation). Dr. Alpert also testifies that a person of ordinary skill in the art would have had a bachelor's degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems. *Id.* Patent Owner's expert, Mr. Murphy, agrees with Petitioner's proposed qualifications. Ex. 2001 ¶¶ 18–19.

We adopt the parties' agreed-upon qualifications. In addition, we note that the art of record in this proceeding and addressed here—including,

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<sup>7</sup> Patent Owner has not argued that there are objective indicia of nonobviousness.

Hazelzet, Buchmann, and Talbot—is indicative of the level of ordinary skill in the art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

Independent Claims

We will address claim 1 as representative of the independent claims. Claim 1 recites a memory module configured to fit into a corresponding slot of a host system to operate with a memory controller of the host system. Petitioner argues that the combination of Hazelzet and one of Buchmann or Talbot discloses this feature. Pet. 15–16, 18–23. For example, Petitioner explains that Hazelzet discloses “dual inline memory modules (DIMM) that are configured to operate with the ‘memory controller’ of the host system.” *Id.* at 20 (citing Ex. 1014, Fig. 2, ¶¶ [0036]–[0038]; Ex. 1003 ¶ 122). We agree with Petitioner’s showing that Hazelzet teaches this recitation.

Claim 1 recites that the module controller generates and drives “a parity error signal” to the memory controller of the host system via an open drain output when operating in a first mode. Petitioner argues that the combination of Hazelzet and one of Buchmann or Talbot discloses this feature. Pet. 23–27. For example, Petitioner explains that Hazelzet discloses “an ‘ECC/Parity register’ (*module controller*) [also referred to as a “buffer device”] having an output (*open drain output*)” that “operate[s] in . . . a ‘parity mode,’ which is the claimed ‘*first mode* (or state)’” in which “error reporting circuitry” reports “correctable” and “uncorrectable errors.” *Id.* at 24–25 (citing Ex. 1014, Figs. 3A–3D, 4A, 4B, 5, 8, ¶¶ [0020], [0022], [0027]–[0028], [0049], [0059]–[0062], [0064], [0069]–[0070], [0072], [0075], [0081], [0101]–[0103], [0106]–[0107], [0109]; Ex. 1003 ¶¶ 127–128, 130). We agree with Petitioner that Hazelzet teaches this claim limitation.

Claim 1 recites the memory module entering “a second mode in response to a command from the memory controller of the host system.” Petitioner argues that the combination of Hazelzet and one of Buchmann or Talbot discloses this feature. Pet. 28–29. For example, as Petitioner explains, Hazelzet discloses a memory module (or “buffer device”) that operates “in (1) a ‘parity mode,’ which is the claimed ‘*first mode*,’ and (2) an ‘ECC mode,’ which is the claimed ‘*second mode*’” and that a “chip select” command “from the memory controller of the host system” “cause[s] the memory module to enter an ‘ECC mode.’” *Id.* (citing Ex. 1014 Fig. 4A, 7B, ¶¶ [0027], [0066], [0074], [0104]; Ex. 1003 ¶ 141). Hence, one of skill in the art would have understood Hazelzet to teach a memory module that operates in different “modes” based on commands from a memory controller of a host system.

As Petitioner also points out, and we agree, Buchmann discloses a memory module (or “memory buffer”) that communicates with a “memory controller” of a host system in which the memory module operates in “two modes of operation” (“SBC mode” and “high-speed mode”), and Talbot discloses “normal operation (*i.e.*, ‘read and write operations’)” and a “training mode.” Pet. 57–58, 61–62 (citing Ex. 1016 ¶¶ [0049], [0052], [0053], [0089]; Ex. 1017, Abstract, 1:39–44, 3:52–54, 3:64–67, 5:6–22, 14:1–15:15; Ex. 1003 ¶¶ 159, 165, 168). Hence, each of Buchmann and Talbot confirms that one of skill in the art would have understood memory systems containing a memory module in communication with a memory controller of a host system may operate in different “modes.”

Claim 1 recites a “second mode” in which the module controller generates and outputs a notification signal indicating a status of a training

sequence. Petitioner argues that Hazelzet in combination with any one of Buchmann or Talbot discloses this feature. Pet. 57–66. For example, as Petitioner explains, Buchmann discloses a memory system with “two modes of operation” including a mode for “training” that is “used to perform upstream data lane training” and “outputs various notification signals indicating the status of the . . . training sequence to the memory controller of the host system” and Talbot discloses a “training mode.” *Id.* at 58, 62 (citing Ex. 1016 ¶¶ [0049], [0052], [0053], [0089]; Ex. 1017, 14:1–15:15, 3:52–54, 3:64–67, 5:6–22, 5:40–12:59, 8:24–9:18, Tables 5 and 6; Ex. 1003 ¶¶ 159, 165, 168–169).

As Petitioner points out, Buchmann discloses “a memory controller (MC)” connected to “memory modules” (or “memory buffers”). Ex. 1003 ¶ 113; Ex. 1017, 4:10–15. During “power-on and initialization” of the memory modules and “memory channel initialization” (Ex. 1017, 4:29–31, 5:32), “training states [are] accomplished” including “TS3 – upstream lane training and repair” in which the “host memory controller” “initiates a [training] state . . . to [a memory module]” such that the memory module “returns a handshake . . . to the [memory controller] to let it know that [training] has been completed and the status (e.g., successful).” Pet. 62; *see* Ex. 1017, 5:40–41, 43–44; 6:54–55, 58–62. Buchmann discloses that the memory module performs “upstream lane training and repair” in which the memory module sends a “response [that] indicates that all [memory modules] have returned the TS3a\_ack SBC” or a “response [that] indicates [that memory modules] are done with TS2 [i.e., “TS\_done”].” Ex. 1003 ¶¶ 167, 169; Ex. 1017, 8:24, 41–44, Table 5. Also, “[t]he last [memory module] . . . sends TS3a\_ack [which is] forwarded back to the host.” Ex.

1017, 8:59–61, Table 6. In other words, Buchmann discloses a memory controller connected to a memory module that operates in a mode in which the memory module executes a training sequence and notifies the memory controller of the status of the training sequence (e.g., successful). *See* Ex. 1003 ¶ 169. Likewise, we agree with Petitioner that Talbot teaches a “training mode” in which “memory controller 100 drives a training pattern” to “buffer unit 170” (or “memory module”) and receives “data patterns [or “notification signal”] on CRC path” from the buffer unit. Pet. 57–58 (citing Ex. 1016 ¶ 52).

We agree with Petitioner that Buchmann and Talbot are analogous art to Hazelzet and the ’623 patent because they are all directed to the field of error detection and correction in memory modules. Pet. 59, 63. We also agree with Petitioner that it would have been obvious to one of ordinary skill in the art to have combined the known memory system containing a memory controller connected to a memory module that may operate in more than one mode (e.g., Hazelzet, Buchmann, or Talbot), including a known mode in which the memory module performs a training sequence, to notify (send a notification signal to) the memory controller of the status of the training sequence (e.g., Buchmann or Talbot) in order to improve overall reliability. *Id.* at 59–61, 63–64. Dr. Alpert’s testimony supports that the combination of Hazelzet with Buchmann or Talbot would achieve the predictable and expected result of a known (multi-mode) memory system containing known components of a memory controller connected to a memory module performing a known function of executing a training sequence and notifying the memory controller of the status of the training sequence (e.g., Buchmann or Talbot). Ex. 1003 ¶¶ 159, 175. “The combination of familiar elements

according to known methods is likely to be obvious when it does no more than yield predictable results.” *KSR*, 550 U.S. at 416.

Petitioner further argues that the combination of Hazelzet and any one of Buchmann or Talbot discloses a printed circuit board as recited in claim 1. Pet. 32–34 (citing Ex. 1014 ¶¶ [0015], [0037]–[0039], [0059], [0068]–[0070], [0072], [0076], [0092], [0109], Figs. 2, 3A–3D, 4B, 7A–7C, 8; Ex. 1003 ¶¶ 177–186). Patent Owner does not dispute Petitioner’s contentions with respect to this issue. Based on our review of Petitioner’s argument and evidence, we find that Hazelzet teaches the printed circuit board recited in claim 1.

Notwithstanding Patent Owner’s contrary arguments, which we discuss below, we agree with Petitioner’s showing that the combination of Hazelzet and any one of Buchmann or Talbot teaches every limitation of claims 1, 12, and 21 of the ’623 patent and that a person of ordinary skill in the art would have had reason, with rational underpinning, to combine the references. Further, we credit Dr. Alpert’s supporting testimony (Ex. 1003 ¶¶ 121–150, 158–186), as it is consistent with the prior art disclosures.

Patent Owner argues that it would not have been obvious to one of ordinary skill in the art to have combined the teachings of a known memory system containing a memory module in communication with a memory controller of a host system, the memory module operating in any one of multiple modes (i.e., a system disclosed by any one of Hazelzet, Buchmann or Talbot) with the teachings of a known mode of operation of such a memory system in which the memory module sends a notification of a status of a training sequence to the memory controller (i.e., Buchmann or Talbot) because of an alleged “technological problem.” PO Resp. 11, 29. In

particular, Patent Owner argues that “[d]uring Hazelzet’s [second mode] . . . Hazelzet’s UE line . . . is busy” such that “implement[ing] Buchmann’s TS3 command signaling on Hazelzet’s UE line would run into a signal conflict with Hazelzet’s UE signaling already occurring [on] the UE line [of Hazelzet]” and that the “training pattern data” of Talbot “needs to occur ‘while [Hazelzet’s DIMM(s) 20] is in [Hazelzet’s ECC MODE]’” while “Hazelzet’s UE line . . . is busy.” *Id.* at 11–36.

In other words, Patent Owner argues that it would not be possible for one of ordinary skill in the art to perform a known mode of operation of a memory system (i.e., sending a notification signal of a status of a training sequence) while simultaneously performing a different operation using the same resources (i.e., performing Hazelzet’s “UE signal function”). We are not persuaded by Patent Owner’s argument.

Even assuming to be correct Patent Owner’s contention that sending a notification signal of a status of a training sequence over a particular bus would interfere with performing actions of a different mode of operation on the same bus at the same time, the basis of Patent Owner’s argument is nonetheless that discrete modes of operation are required to occur at the same time. For example, Patent Owner argues that the “training pattern data” of Talbot “needs to occur ‘while [Hazelzet’s DIMM(s) 20] is in [Hazelzet’s ECC MODE]’” but does not explain why transmitting “training pattern data,” in fact, “needs to occur” simultaneously with “Hazelzet’s ECC MODE.” PO Resp. 29. Given that neither Hazelzet nor Talbot discloses any specific temporal relationship between transmitting “training pattern data” and “Hazelzet’s ECC MODE,” there would be no specific requirement

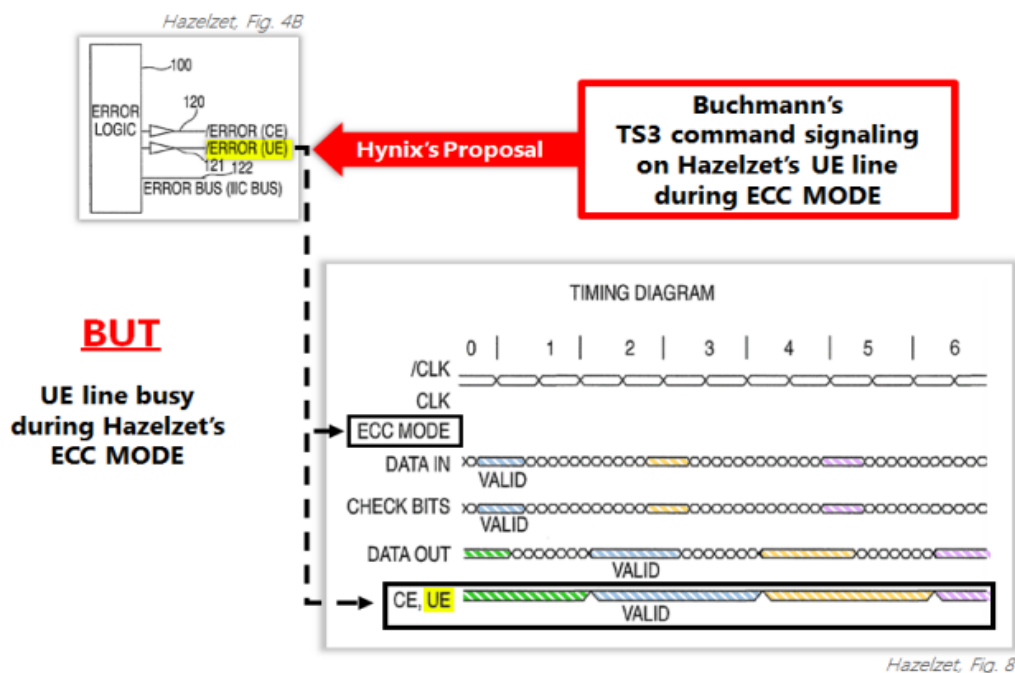
to perform the two modes of operation simultaneously using the same resources.

Similarly, as noted above, Patent Owner argues that “implement[ing] Buchmann’s TS3 command signaling on Hazelzet’s UE line would run into a signal conflict with Hazelzet’s UE signaling already occurring [on] the UE line [of Hazelzet]” but does not explain why “Buchmann’s TS3 command signaling” must be performed simultaneously “with Hazelzet’s UE signaling already occurring [on] the UE line.” PO Resp. 11–36. We also note that claim 1, for example, does not recite or require the performance of multiple modes of operation at the same time over the same bus.

To the extent that Patent Owner argues that it would not have been obvious to one of ordinary skill in the art to have bodily incorporated the teachings of either of Buchmann or Talbot (i.e., training mode) into those of Hazelzet (i.e., a mode during which training is not performed), we note that “[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference. . . . Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art.” *In re Keller*, 642 F.2d 413, 425 (CCPA 1981); *see also In re Sneed*, 710 F.2d 1544, 1550 (Fed. Cir. 1983) (“[I]t is not necessary that the inventions of the references be physically combinable to render obvious the invention under review.”); *In re Nievelt*, 482 F.2d 965, 968 (CCPA 1973) (“Combining the *teachings* of references does not involve an ability to combine their specific structures.”).

Moreover, even if discrete modes of operation and associated transmissions were required to occur at the same time, we do not agree with

Patent Owner's argument that a person of ordinary skill in the art would not be motivated to combine Hazelzet with Buchmann or Talbot because of technological problems. See PO Resp. 10–15, 27–32. More specifically, Patent Owner argues that during Hazelzet's ECC MODE its UE line would be busy and could not accommodate, for instance, Buchmann's TS3 command signaling. *Id.* at 11–12. To illustrate the alleged understanding of one of skill of Hazelzet's UE line being busy, Patent Owner modified Hazelzet's Figure 8, as reproduced in the version below. *Id.* at 12–13.



The version of Figure 8 of Hazelzet reproduced above was modified by Patent Owner to present the alleged “exemplary operation of the UE line for a data stream of four data operation,” with the four data operations on the bottom “CE, UE” line shown in different colors. PO Resp. 13. Patent Owner bases its depiction of a fully occupied UE line on Mr. Murphy’s testimony that in the view of one of skill in the art, the “close packing of segments back-to-back most accurately reflects the default industry design

goal to have maximum bus utilization.” Ex. 2005 ¶ 31. Mr. Murphy acknowledges that “it could be possible to increase the spacing between Hazelzet’s UE segments in order to ‘make room’ to implement Buchmann’s TS3 command signaling on the UE line during Hazelzet’s ECC MODE,” but one of ordinary skill would be highly motivated against doing so because Buchmann’s TS3 command signaling is a secondary design feature with less priority.” *Id.* ¶ 32.

We do not credit Mr. Murphy’s testimony because it conflicts with the actual disclosure of Hazelzet and also because, absent support, it applies a broad default industry design goal to a specific application to a bus used to send uncorrectable errors. Hazelzet’s unmodified Figure 8 is reproduced below.

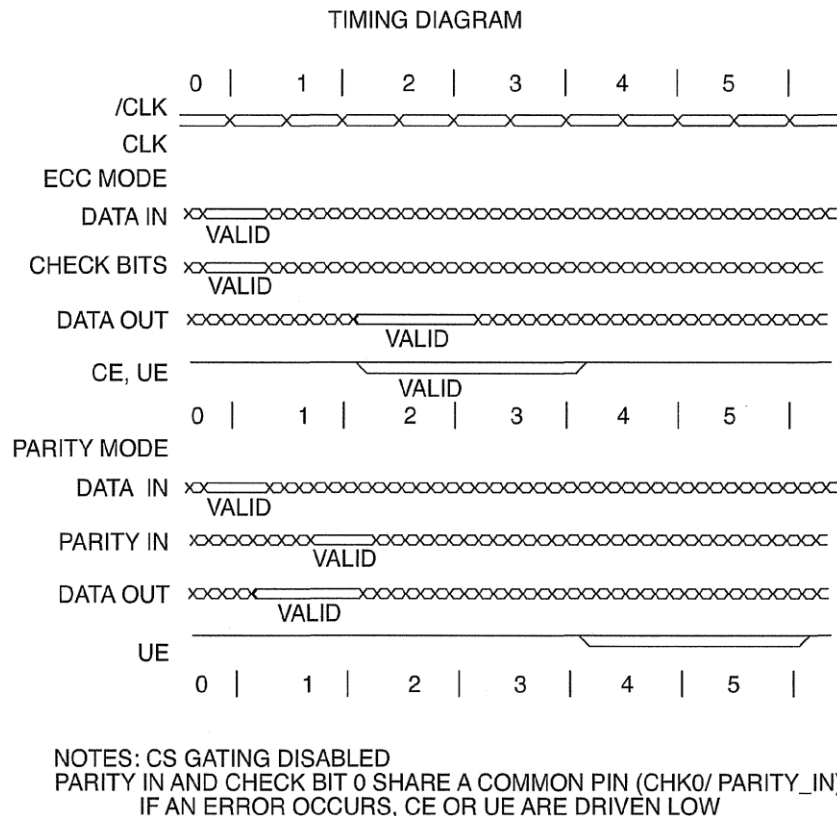


FIG. 8

Figure 8 of Hazelzet, reproduced above, depicts a timing diagram where the “ECC mode” is a mode that allows the host system to detect and/or correct correctible or uncorrectable errors. Ex. 1014 ¶ 69. As shown, the “CE, UE” signal line of the “ECC MODE” depicts more limited signaling in periods 2 and 3 compared to Patent Owner’s depiction in its modified figure that shows signals fully occupying the UE line.

Patent Owner’s justification for altering Buchmann’s TS3 command signaling disclosure is based on the premise that the default industry design goal is to have maximum bus utilization. Although that goal may generally be true, Patent Owner’s expert, Mr. Murphy fails to explain or provide support for applying this general goal to the specific transmissions of Hazelzet, which are limited to error detection. Rule 42.65(a) provides that “[e]xpert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.” We find Mr. Murphy’s testimony to be insufficient to support Patent Owner’s position because it fails to explain why an industry design goal, even if is a default, should be applied to the specific application here, namely a bus used to send uncorrectable errors, when the actual reference discloses conflicting alternative signaling.

Patent Owner further alleges that one of skill in the art would not be motivated to combine Hazelzet and Buchmann or Talbot because they have different design purposes and there would be a risk of failure if the references were combined. PO Resp. 16–27, 32–36. For instance, Patent Owner asserts that

Netlist’s point was not that their two different technical design purposes could not be combined or that doing so was beyond the skill level of a POSITA. Rather, to clarify, Netlist’s point was

that the difference at the design concept level (not implementation details) would have been recognized by a POSITA as a barrier to overcome in order to successfully accomplish the Hazelzet-Buchmann combination proposal, that barrier motivating a POSITA against doing so. For example, in the effort to combine the two fundamentally different technical design purposes, there is the risk that one or the other technical design purpose could be lost, and that risk of failure would be a significant factor leading a POSITA away from the Hazelzet-Buchmann combination proposal.

PO Resp. 17.

We do not agree with Patent Owner's arguments. Patent Owner neither asserts that the prior art would not be combinable in the view of a person of skill in the art, nor presents specific allegations of teaching away. Instead, Patent Owner's arguments are premised on alleged different design purposes and potential increased risk of failure. Petitioner's arguments focus on implementation details of the prior art based on bodily incorporation instead of what the combined teachings of those references would have suggested to those of ordinary skill in the art. See PO Resp. 16–27, 32–36. Patent Owner's assertions also allege tradeoffs in the combination, which we do not find persuasive in light of the Petition's demonstrated rationale to combine. See *Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 n.8 (Fed. Cir. 2000) ("The fact that the motivating benefit comes at the expense of another benefit . . . should not nullify its use as a basis to modify the disclosure of one reference with the teachings of another."); see also *Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1069 (Fed. Cir. 2018) (reference does not teach away "if it merely expresses a general preference for an alternative invention but does not 'criticize,

discredit, or otherwise discourage’ investigation into the invention claimed”).

We note that Patent Owner argues that under its proposed claim construction, Petitioner’s obviousness contentions under Hazelzet alone, or Hazelzet in combination with Amidi, would fail to teach the “one or more teaching sequence” limitations of the independent claims. PO Resp. 36–37, 43–56. Patent Owner presents no arguments based on this claim construction issue on Petitioner’s asserted grounds over Hazelzet in combination with Buchmann or Talbot. *See id.* at 10–36.

Dependent Claims

Claims 3, 4, 14 and 22 recite “training sequences” or “training mode.” Patent Owner argues that “Dr. Alpert does not say that [Hazelzet] teaches ‘training sequences’ [recited in claim 3]” and that Petitioner “and Dr. Alpert add nothing new to treat claims 4, 14, and 22.” PO Resp. 57–58. We are not persuaded by Patent Owner’s argument at least because Petitioner relies on the combination of Hazelzet and any one of Buchmann or Talbot, not on Hazelzet alone. For reasons previously discussed, we are persuaded by Petitioner that the combination of Hazelzet and any one of Buchmann or Talbot teaches the claimed “training sequences” and, thus, renders obvious claims 3, 4, 14, and 22.

Petitioner also argues that claims 2, 5–11, 13, 15–20, and 23–29 are unpatentable over the combination of Hazelzet and any of Buchmann or Talbot; claims 8, 9, 19, 20, 25, and 26 are unpatentable over the combination of Hazelzet, Hokenmaier, and any of Buchmann or Talbot; and claims 10, 15, and 27 are unpatentable over the combination of Hazelzet, Kim, and any of Buchmann or Talbot. Pet. 57–70. Patent Owner does not dispute

Petitioner's grounds of unpatentability for these claims and references. Any arguments not raised are deemed waived.

We have reviewed the arguments and evidence presented by Petitioner for dependent claims 2–11, 13–20, and 22–29 and conclude that Petitioner demonstrates that these claims would have been obvious over these asserted combinations of prior art. Pet. 35–44, 48–39, 57–70.

### Conclusion

For the reasons discussed above, Petitioner has shown by a preponderance of the evidence that claims 1–29 of the '623 patent are obvious over the combination of Hazelzet and Buchmann or Talbot; claims 8, 9, 19, 20, 25, and 26 are also obvious over the combination of Hazelzet, Hokenmaier, and Buchmann or Talbot; and claims 10, 15, and 27 are also obvious over the combination of Hazelzet, Kim, and Buchmann or Talbot.

### OTHER GROUNDS

The above discussion addresses and is dispositive as to the unpatentability of all challenged claims, rendering it unnecessary to reach the propriety of any remaining contentions. *See SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1359 (2018) (holding a petitioner “is entitled to a final written decision addressing all of the claims it has challenged”); *Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984); *see also Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *In re Gleave*, 560 F.3d 1331, 1338 (Fed. Cir. 2009).

### III. MOTIONS

#### PETITIONER'S MOTION TO EXCLUDE

Petitioner moves to exclude Exhibits 2003 and 2004 and portions of Exhibit 2001. Paper 25, 2. We did not rely on Exhibits 2003 or 2004, or the

cited portions of Exhibit 2001. Therefore, Petitioner's motion to exclude is dismissed as moot.

#### PATENT OWNER'S MOTION TO EXCLUDE

Patent Owner moves to exclude Exhibits 1034 and 1036. We did not rely on Exhibits 1034 or 1036. Therefore, Patent Owner's motion to exclude is dismissed as moot.

#### IV. CONCLUSION

For the foregoing reasons, we conclude that Petitioner has demonstrated by a preponderance of the evidence that claims 1–29 of the '623 patent are unpatentable. Specifically, Petitioner has demonstrated by a preponderance of the evidence that claims 1–29 are unpatentable under 35 U.S.C. § 103(a) over Hazelzet and any one of Buchmann or Talbot; claims 8, 9, 19, 20, 25, and 26 are unpatentable under 35 U.S.C. § 103(a) over Hazelzet, Hokenmaier and any one of Buchmann or Talbot; and claims 10, 15, and 27 are unpatentable under 35 U.S.C. § 103(a) over Hazelzet, Kim, and any one of Buchmann or Talbot.

#### ORDER

ORDERED that claims 1–29 of U.S. Patent No. 9,535,623 B1 are unpatentable;

FURTHER ORDERED that Petitioner's Motion to Exclude is DISMISSED;

FURTHER ORDERED that Patent Owner's Motion to Exclude is DISMISSED; and

FURTHER ORDERED, that because this is a final written decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Patent 9,535,623 B1

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