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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and SK HYNIX MEMORY
SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2017-00548
Patent 8,489,837 B1

Before STEPHEN C. SIU, MATTHEW R. CLEMENTS, and
SHEILA F. McSHANE, *Administrative Patent Judges*.

SIU, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

SK Hynix Inc. (“Petitioner”) requested *inter partes* review of claims 1–3, 5 and 6 of U.S. Patent No. 8,489,837 B1 (“the ’837 patent,” Ex. 1001). Paper 1 (“Pet.”). On May 15, 2017, we issued a Decision to Institute an *inter partes* review (Paper 7, “Inst. Dec.”) of the ’837 patent on the following grounds:

- 1) Claims 1–3 and 6 under 35 U.S.C. § 103(a) as unpatentable over LeClerc¹ and Lee.²
 - 2) Claims 1–3, 5, and 6 under 35 U.S.C. § 103(a) as unpatentable over LeClerc, Lee, and Kim.³
- Inst. Dec. 3, 15.

After institution of trial, Netlist, Inc. (“Patent Owner”) filed a Patent Owner’s Response (Paper 11, “PO Resp.”), to which Petitioner replied (Paper 14, “Pet. Reply”). Oral argument was conducted on February 14, 2018. A transcript of that argument has been made of record. Paper 24.

We have jurisdiction under 35 U.S.C. § 318(a). After considering the evidence and arguments of both parties, and for the reasons set forth below, we determine that Petitioner met its burden of showing, by a preponderance of the evidence, that claims 1–3, 5, and 6 of the ’837 patent are unpatentable.

RELATED MATTERS

The ’837 patent is the subject of the following: *Netlist, Inc. v. SK Hynix Inc.*, Case No. 8:16-cv-01605 (C.D. Cal.) and *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (International Trade Commission). See Pet. 3.

¹ US Patent Publication 2005/0071580 A1, published March 31, 2005 (“LeClerc,” Ex. 1005).

² US Patent Publication 2005/0193161 A1, published September 1, 2005 (“Lee,” Ex. 1007).

³ US 8,359,521 B2, issued January 22, 2013 (“Kim,” Ex. 1008).

THE '837 PATENT (EX. 1001)

The '837 Patent describes a system and method for handshaking with a memory module at initialization. Ex. 1001, 1:16–17.

ILLUSTRATIVE CLAIM

Independent claim 1 is representative of the claimed subject matter. Claim 1 is reproduced below:

1. A memory module comprising:
 - at least one output configured to be operatively coupled to a memory controller of a host computer system, the memory module configured to operate in at least two modes comprising an initialization mode during which the memory module executes at least one initialization sequence and an operational mode;
 - a controller circuit configured to cause the memory module to enter the initialization mode; and
 - a notification circuit configured to drive the at least one output while the memory module is in the initialization mode to provide at least one notification signal to the memory controller indicating at least one status of the at least one initialization sequence; and
 - wherein the at least one notification signal triggers the memory controller to execute an interrupt routine.

OVERVIEW OF PRIOR ART

LeClerg (Exhibit 1005)

LeClerg describes initializing and testing memory in a system that includes memory modules. Ex. 1005 ¶ 1.

Figure 1 of LeClerg is reproduced below.

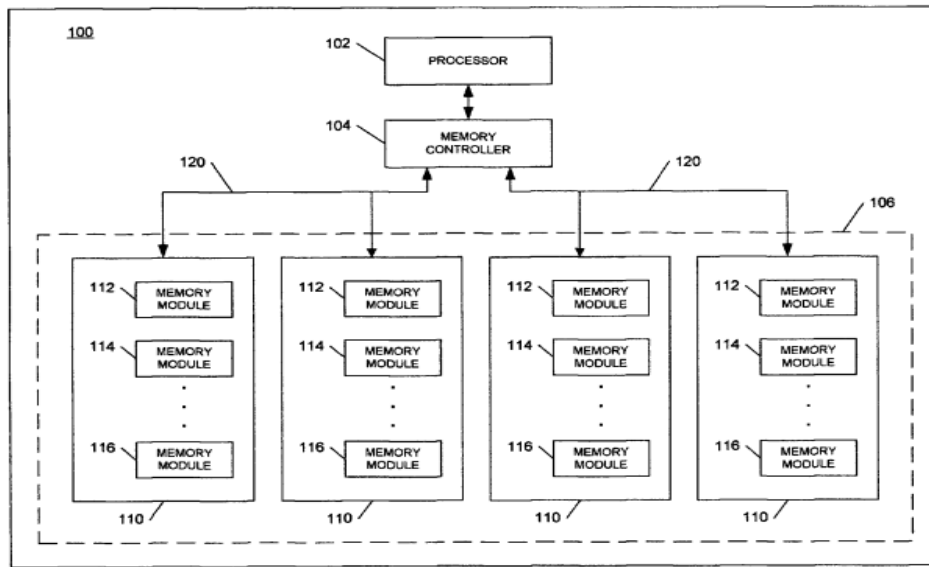


FIG. 1

As illustrated in Figure 1 of LeClerc, a computer system 100 includes a memory controller 104 and multiple memory modules in a main memory 106. *Id.* ¶ 19, Fig. 1. The memory controller 104 and main memory 106 communicate with each other such that the memory controller passes initialization commands to the memory modules. *Id.* ¶¶ 23, 26. In one embodiment, a memory module communicates with the memory controller via a buffer module, which receives an initialization command or initialization message. *Id.* ¶¶ 35, 39, 44. In response, the memory module begins to initialize or test memory devices associated with the memory module (i.e., the “initialization procedure . . . begins”). *Id.* ¶¶ 39, 57.

LeClerc also discloses that the memory module indicates that it has completed the initialization process (or not) by returning an “Initialization Status” message. This indication may be provided in response to an “Initialization Status Query” message received from a processor or the memory controller. *Id.* ¶¶ 59, 60.

Lee (Exhibit 1007)

Lee describes a memory system that includes a processor that contains an interrupt handler 148 that receives an interrupt signal 142. The interrupt signal 142 triggers an interrupt routine at the processor. Ex. 1007, Fig. 2, ¶ 57.

Kim (Exhibit 1008)

Kim describes a memory system including memory devices and a memory controller. Ex. 1008, Fig. 1. Kim also discloses adding an error pin to each memory device in a module and connecting those pins to an existing error pin that would have been available on many industry standard modules. *Id.* at Fig. 4, 5:49–55.

THE PARTIES' POST-INSTITUTION ARGUMENTS

In our Decision on Institution, we concluded that the arguments and evidence advanced by Petitioner demonstrated a reasonable likelihood that claims 1–3 and 6 of the '837 patent are unpatentable under 35 U.S.C. § 103(a) over LeClerc and Lee, and that claims 1–3, 5, and 6 are unpatentable under 35 U.S.C. § 103(a) over LeClerc, Lee, and Kim. Inst. Dec. 15. We must now determine whether Petitioner has established by a preponderance of the evidence that the specified claims are unpatentable over the cited prior art. 35 U.S.C. § 316(e). We previously instructed Patent Owner that “any arguments for patentability not raised in the [Patent Owner Response] will be deemed waived.” Paper 8, 3; *see also* 37 C.F.R. § 42.23(a) (“Any material fact not specifically denied may be considered admitted.”); *In re Nuvasive, Inc.*, 842 F.3d 1376, 1379–1382 (Fed. Cir. 2016) (holding Patent Owner waived an argument addressed in Preliminary Response by not raising the same argument in the Patent Owner Response). Additionally, the

Board's Trial Practice Guide states that the Patent Owner Response "should identify all the involved claims that are believed to be patentable and state the basis for that belief." Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012).

With a complete record before us, we note that we have reviewed arguments and evidence advanced by Petitioner to support its unpatentability contentions where Patent Owner chose not to address certain limitations in its Patent Owner Response. In this regard, the record now contains persuasive, unrebutted arguments and evidence presented by Petitioner regarding the manner in which the asserted prior art teaches corresponding limitations of the claims against which that prior art is asserted. Based on the preponderance of the evidence before us, we conclude that the prior art identified by Petitioner teaches or suggests all uncontested limitations of the reviewed claims. The limitations that Patent Owner contests in the Patent Owner Response are addressed below.

ANALYSIS

A. Claim Construction

We interpret claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear. See 37 C.F.R. § 42.100(b); see *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2142–46 (2016). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

Petitioner proposes constructions for “at least one output,” “an initialization mode,” “an operational mode,” “an initialization sequence,” “execute an interrupt routine,” and “the at least one status comprises execution of the at least one initialization sequence.” Pet. 9–14. Patent Owner proposes a construction only for the term “mode.” PO Resp. 3–6.

1. “mode”

Petitioner contends that “an initialization mode,” recited in claim 1, should be construed as “a mode during which initialization occurs” and that “an operational mode,” recited in claim 1, should be construed as “a normal mode of operation during which the memory module is generally accessed by the system memory controller of the host computer during standard computer operation not associated with initialization.” Pet. 10–11.

Patent Owner contends that “mode” should be construed as “a distinct behavioral state that a system may be switched to.” PO Resp. 3–6. As Petitioner points out, however, the Specification allows the operational and initialization modes to employ the same memory operations. Pet. Reply 4–5 (citing Ex. 1001, 6:27–33). As a result, we are not persuaded that the Specification supports Patent Owner’s argument that “mode” implies “distinct behavior states.” Patent Owner also fails to explain why one of skill in the art would have construed the term “initialization mode” to require the additional features of a “behavioral state” and “switching” under a broadest reasonable interpretation standard in light of the Specification.

Having considered the arguments and evidence, we determine that claim 1 specifies explicitly that the “initialization mode” is any mode “during which the memory module executes at least one initialization sequence,” and, therefore, we need not further construe the terms “mode” or “initialization mode.”

B. Obviousness over LeClerg and Lee

Petitioner's Initial Positions

Petitioner contends that claims 1–3 and 6 of the '837 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over LeClerg and Lee. Pet. 40–43. Petitioner relies upon LeClerg for most of the teachings of the limitations of claims 1–3, and 6. Pet. 21–43. For the claim 1 limitation of “wherein the at least one notification signal triggers the memory controller to execute an interrupt routine,” Petitioner relies additionally upon Lee in combination with LeClerg for confirmation that it would have been obvious to one of ordinary skill in the art to have provided for a notification signal that triggers the memory controller to execute an interrupt routine. Pet. 40–43.

For example, Petitioner contends that LeClerg discloses a “memory module” (Pet. 21–22 (citing Ex. 1005, Figs. 1, 2, 9, ¶¶ 8, 19)) that comprises an output configured to be operatively coupled to a memory controller (Pet. 22–24 (citing Ex. 1005, Fig. 1 – e.g., “memory module 112” illustrated as being operatively coupled to “memory controller 104”)), and that the memory module “undergo[es] an initialization process.” Pet. 24–25 (citing Ex. 1005, Figs. 4–5, ¶¶ 18, 19, 26, 39, 41, 44, 57, 78 – i.e., configured to operate in an “initialization mode”). Petitioner argues that one of skill in the art would have understood an “initialization mode,” as recited in claim 1 to include “a mode during which initialization occurs.” Pet. 10 (citing Ex. 1003 ¶¶ 62–65), 24. Petitioner also explains that LeClerg discloses “[w]hen a memory module receives an initialization command from a processor or the memory controller, the memory module performs an initialization procedure of the memory locations associated with the memory module” that may include “a specified series of actions to initialize itself.” Pet. 24–25 (citing Ex. 1005, Abstract, ¶ 26, Figs. 4, 5).

Petitioner has provided a similar detailed analysis of claims 2–3 and 6. *See* Pet. 54–62. Notwithstanding Patent Owner’s arguments, which we have considered and which we address below, we are persuaded by Petitioner’s showing, which we adopt as our own findings and conclusions, that claims 1–3 and 6 are unpatentable under 35 U.S.C. § 103(a) as obvious over LeClerc and Lee.

Patent Owner’s Arguments

“initialization mode”

Patent Owner argues that LeClerc’s “low-power mode” fails to disclose an “initialization mode during which the memory module executes at least one initialization sequence” as recited in claim 1 because, according to Patent Owner, “[i]n sleep mode, no operations occur” (PO Resp. 6) and “[n]o initialization procedure occurs in sleep mode” (PO Resp. 7). This argument is not persuasive because Petitioner is not relying upon LeClerc’s “low-power mode” for teaching the recited “initialization mode.” *See* Pet. 24–26 (relying on LeClerc’s teaching of an initialization process performed in response to an initialization command).

Patent Owner also argues that LeClerc’s “normal power mode” fails to disclose an “initialization mode during which the memory module executes at least one initialization sequence” as recited in claim 1 because, according to Patent Owner, “normal reads and writes occur” in this mode. PO Resp. 6. Specifically, Patent Owner argues that LeClerc fails to disclose “an initialization mode . . . that is ‘distinguished’ from an operational mode.” *Id.* at 8. Patent Owner also argues that LeClerc discloses “a mere time period” “during which” time an initialization procedure is performed but fails to disclose “a ‘distinct behavioral state that a system may be switched’” during which time an initialization procedure is performed” or a “mode.” *Id.* at 9–10.

These arguments are not persuasive because they are based upon Patent Owner's proposed construction of "mode," which we declined to adopt for the reasons discussed above. Claim 1 recites that the "initialization mode" is one "during which the memory module executes at least one initialization sequence." LeClerc discloses the execution of an "initialization procedure" that initiates an "initialization process" (*see, e.g.*, Ex. 1005 ¶¶ 19, 57, 58). We are persuaded by Petitioner that this teaches the claimed "initialization mode," which one of skill in the art would have understood to include a mode during which an initialization procedure or process is performed (*see* Ex. 1003 ¶ 107).

Even assuming that "initialization mode" should be construed properly to require "switching" into a "behavioral state," we are persuaded that LeClerc "switches" (i.e., initiates an initialization procedure) into a specified "behavioral state" (i.e., the "state" of performing the initialization procedure as opposed to the "state" of not performing (or prior to performing) the initialization procedure), and Patent Owner does not explain persuasively why LeClerc is not in a distinct behavioral state while performing its initialization procedure.

Accordingly, after consideration of the issues that Patent Owner raises in its Response related to this issue, we find that Petitioner has met its burden to demonstrate LeClerc's teaching of the "initialization mode" as recited in claim 1.

"controller circuit" / "notification circuit"

Patent Owner also argues that LeClerc fails to disclose a "controller circuit" (PO Resp. 13) or a "notification circuit" (PO Resp. 14), as recited in claim 1. These assertions, however, are based upon Patent Owner's arguments that LeClerc fails to disclose an "initialization mode." We are not persuaded by Patent Owner's arguments for at least the previously discussed reasons.

Further, claim 1 recites a notification circuit configured to drive the memory module to provide a notification signal to the memory controller. Petitioner argues that LeClerc discloses a “memory module [that] is connected to the processor by way of the memory controller” and that “the memory module outputs its initialization completion notifications to the memory controller, and the memory controller in turn signals the processor.” Pet. 31 (citing Ex 1003 ¶ 128; Ex. 1005, Fig. 1). As Petitioner points out, LeClerc discloses a “bus interface” (Fig. 3) and “buffer module” (Fig. 2) within a “memory module” (Figs. 1–3) with an output that is connected (via “210” – Figs. 2–3) to a memory controller (Fig. 1).

Patent Owner argues that LeClerc discloses “sending a notification signal ‘to the processor’ – not ‘to the memory controller.’” PO Resp. 15. This argument is not persuasive, however, given that the signal sent from a memory module to the processor in LeClerc is disclosed as passing through the memory controller, the signal sent from the memory module would be received at the memory controller. If the signal was not received at the memory controller, it could not be sent to the processor, which is disclosed as receiving signals from the memory controller after those signals are received by the memory controller from the memory module.

With respect to Petitioner’s alternative contention that signals sent to LeClerc’s processor are also “to the memory controller” because LeClerc’s memory controller and processor “are the same component” (Pet. 31–32), Patent Owner argues that LeClerc fails to disclose that the memory controller and the processor “are the same component.” PO Resp. 15. We need not resolve this dispute because we do not rely on Petitioner’s alternative contention.

Patent Owner does not assert additional arguments against dependent claims 2, 3, and 6, except for the alleged deficiencies as to claim 1, which we address above. PO Resp. 16.

Based on the record developed during trial, we find that Petitioner has demonstrated by a preponderance of the evidence that claims 1–3 and 6 would have been obvious over the combination of LeClerg and Lee.

C. Obviousness over LeClerg, Lee, and Kim

Petitioner contends that claims 3, 5 and 6 of the '837 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over LeClerg, Lee, and Kim. Pet. 43–47.

Claims 3 and 6

Claim 3 recites “wherein the at least one status comprises execution of the at least one initialization sequence.” Petitioner argues that “Kim teaches the use of a single pin to report, among other things, initialization errors,” and explains why and how a person of ordinary skill in the art would have combined Kim with LeClerg. Pet. 43–46. Claim 6 recites “wherein the notification circuit is configured to drive the at least one output to a first state indicative of execution of the at least one initialization sequence or to a second state indicative of completion of the at least one initialization sequence.” Petitioner argues that “it would have been obvious to include [the subject matter of claim 6] in the system of LeClerg, in view of Kim, for the reasons set forth above with respect to claim 3.” Pet. 47. Patent Owner does not argue separately dependent claims 3 and 6.

Having considered the arguments and evidence, we are persuaded that Petitioner has established, by a preponderance of the evidence, that claims 3 and 6 would have been obvious over LeClerg, Lee, and Kim.

Claim 5

Claim 5 recites “wherein the at least one output comprises an error-out pin of the memory module.” Petitioner argues that Kim (in combination with LeClerg)

discloses this feature. Pet. 46–47. For example, Kim discloses a pin in a “memory device for reporting . . . errors” (Ex. 1008, 5:49–55), and that this functionality “could also be merged with an existing error pin available on many industry standard modules for the reporting of address/command errors.” Pet. 46–47 (citing Ex. 1008, 5:53–55, 6:13–18, 11:20–34; Ex. 1003 ¶ 64).

Patent Owner argues that the claimed error-out pin must “be driven to ‘provide at least one notification signal . . . indicating at least one status of the at least one initialization sequence.’” PO Resp. 24. Patent Owner contends that the combination of LeClerc, Lee, and Kim fails to disclose or suggest this feature because “‘the ‘error-out pin’ of claim 5 does, in fact, have a specific function, even non-error reporting’” (PO Resp. 16–19), that Kim discloses “a ‘single pin’ and ‘to report write data errors . . .’” but “makes no mention of ‘initialization errors’,” and does not disclose reporting “initialization errors” on its single pin (PO Resp. 21). Instead, according to Patent Owner, Kim’s single pin is “actually for reporting transmission interface errors of failed data transfer operations.” PO Resp. 21–22. Even assuming Patent Owner is correct that Kim fails to disclose a “single pin” for reporting “initialization errors,” and even if the single pin of Kim may be used for “reporting transmission interface errors of failed data transfer operations,” as Patent Owner contends, these arguments fail at least because Petitioner relies upon the combination of LeClerc, Lee, and Kim to teach the limitations of claim 5. Nonobviousness cannot be established by attacking references individually where, as here, the ground of unpatentability is based upon the teachings of *a combination* of references. *In re Keller*, 642 F.2d 413, 426 (CCPA 1981). Rather, the test for obviousness is whether the combination of references, taken as a whole, would have suggested the patentee’s invention to a person of ordinary skill in the art. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). Here, we are

persuaded that a person of ordinary skill in the art would have combined LeClerc's teaching of "Completed" and "Not Completed" messages with Kim's teaching of an error out pin as articulated in the Petition:

LeClerc already discloses a channel connection between the memory module and the memory controller over which error information is sent (Ex. 1005 at ¶¶ 35, 91), which a skilled artisan would have understood as being physically implemented as a pin. Moreover, LeClerc already discloses the desirability of providing both "Not Completed" and "Completed" messages to notify the host system of the status of memory module notification, Ex. 1005 at ¶¶ 88, 91, which can be efficiently implemented with the open drain configuration as disclosed by Kim. Thus a person of skill in the art would readily have modified that LeClerc's channels with the teachings of Kim to be a open-drain output pin and have been motivated to do so. Ex. 1003 at ¶ 162.

Pet. 46.

Patent Owner asserts that its arguments "are not directed as a piecemeal attack on 'Kim in isolation'" but, instead "establish that the 'error-out pin' recitations of claim 5 are unknown [based on the combination of LeClerc, Lee, and Kim]." PO Resp. 23–24. In other words, Patent Owner argues that the combination of LeClerc, Lee, and Kim fails to disclose or suggest an "error-out pin" that is driven to "provide at least one notification signal . . . indicating at least one status of the at least one initialization sequence." PO Resp. 23–24. However, as Petitioner explains, Kim was analyzed in combination with LeClerc, where "the combination of LeClerc with the open-drain output pin scheme of Kim, an active signal on the output pin (in response **to an initialization command**) **would indicate that the initialization sequence had 'Not Completed'**" and "[t]o use the output-pin scheme of Kim in the system of LeClerc would therefore have been only the use of known techniques for their known purposes to achieve predictable results, i.e., using a single line **to provide status information from multiple**

components.”). Pet. Reply 18 (citing Pet. 44–45) (emphases added). As discussed above, we are persuaded by the evidence and rationale to combine LeClerg and Kim provided in the Petition, as well as LeClerg’s disclosure of output of initialization status, which would indicate whether the initialization process had not been completed (“Not Completed” status), i.e., initialization “error” reporting, or initialization had been completed, i.e., initialization “non-error” reporting. Accordingly, we find that Petitioner has met its burden of showing that the combination of LeClerg, Lee, and Kim teaches the limitation of claim 5, even under Patent Owner’s view that the claimed “one output comprises an error-out pin of the memory module” must be capable of transmitting a signal for initialization errors.

Patent Owner further argues that “[w]hen considered ‘as a whole,’ a POSITA would have found claim 5 to be not obvious over LeClerg in view of Lee and Kim” because, according to Patent Owner, Kim discloses a “technique of . . . an ‘open drain output’ [that] is suitable for Kim’s . . . ‘initiate a re-try of the failed write operation,’” but is not suitable for connecting LeClerg’s multiple memory modules because “it would not be possible to identify the specific memory module that is the source of the asserted signal” and, therefore, “LeClerg’s system would lose the ability to identify the source of the . . . initialization complete status messages asserted on Kim’s shared [pin].” PO Resp. 27–28. Petitioner counters that “the claims at issue here do not require identification of the specific memory module that is the source of the asserted signal” and that, even if they did, the identity could be determined from “initialization status information [] stored in registers on the memory module . . . which LeClerg’s system memory controller can obtain either by polling or a notification signal.” Pet. Reply 23–24. We agree with Petitioner that the claims do not require identification of the specific memory

module that is the source of the asserted signal. Thus, Patent Owner's arguments are not persuasive because they are not commensurate with the scope of the claims.

Based on the record developed during trial, we find that Petitioner has demonstrated by a preponderance of the evidence that the combination of LeClerg, Lee, and Kim renders claim 5 obvious.

PETITIONER'S MOTION TO EXCLUDE

Petitioner timely objected to and moves to exclude Exhibits 2001–2008. Papers 12, 16. Patent Owner opposes Petitioner's Motion to Exclude. Paper 19. Petitioner files "Petitioners' Reply in Support of its Motion to Exclude." Paper 22. Petitioner's motion to exclude is moot because we did not rely on Exhibits 2001–2008. Petitioner's motion to exclude is dismissed.

SAS INSTITUTE INC. v. IANCU

The Supreme Court issued its decision on April 24, 2018, in *SAS Institute Inc. v. Iancu* concerning final written decisions issued by the Board addressing all claims a petitioner challenged in a petition. *SAS Institute Inc. v. Iancu*, No. 16-969, 2018 WL 1914661 (April 24, 2018). To the extent either Patent Owner or Petitioner believes that the Court's decision in *SAS Institute* requires additional consideration in this proceeding, the parties may file a rehearing request pursuant to 37 C.F.R. § 42.71(d).

CONCLUSION

Petitioner has shown by a preponderance of the evidence that claims 1–3 and 6 are unpatentable under 35 U.S.C. § 103(a) over LeClerg and Lee, and claims 1–3, 5, and 6 are unpatentable under 35 U.S.C. § 103(a) over LeClerg, Lee, and Kim.

ORDER

After due consideration of the record before us, it is:

ORDERED that claims 1–3, 5, and 6 of the '837 patent are held unpatentable;

FURTHER ORDERED that Petitioner's Motion to Exclude with respect to Exhibits 2001–2008 is dismissed; and

FURTHER ORDERED that, because this is a Final Written Decision, the parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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